

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00911
U.S. Patent No. 10,937,806
Issue Date: March 2, 2021

Title: THROUGH ARRAY CONTACT (TAC) FOR
THREE-DIMENSIONAL MEMORY DEVICES

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 10,937,806
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

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LISTING OF EXHIBITS

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1001	U.S. Patent No. 10,937,806 B2 to Tao et al.
1002	File History of U.S. Patent No. 10,937,806 B2 to Tao et al.
1003	Declaration of Jack C. Lee
1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
1005	U.S. Patent Publ. No. 2017/0179026 A1 to Toyama et al. (“Toyama”).
1006	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1007	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1008	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1009	CN109075169A Office Action, dated November 14, 2019
1010	Certified Translation of CN109075169A Office Action, dated November 14, 2019
1011	CN109075169A Reexamination Decision, dated November 25, 2021
1012	Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021
1013	Micheloni, “3D Flash Memories” (2016)
1014	Aritome, “NAND Flash Memory Technologies” (2016)

Exhibit	Description
1015	U.S. Patent Publ. No. 2018/0108671 A1 to Yu et al.
1016	U.S. Patent Publ. No. 2019/0229125 A1 to Zhou et al.
1017	U.S. Patent No. 10,354,980 B1 to Mushiga et al.
1018	U.S. Patent No. 9,293,348 B2 to Lai et al.
1019	U.S. Patent No. 8,598,643 B2 to Kawasaki et al.
1020	U.S. Patent No. 8,697,519 B2 to Jee et al.
1021	Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
1022	Print out of https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides
1023	Michelson et al., “Inside Solid State Drives (SSDs)” (1 st Ed. 2013)
1024	U.S. Patent No. 10,043,558 to Shah et al.
1025	Michelson et al., “Inside NAND Flash Memories” (2010)
1026	Lau, “Ball Grid Array Technology” (1995)
1027	U.S. Patent No. 10,103,169 to Ge et al.
1028	U.S. Patent No. 9,935,050 to Dunga et al.
1029	Chang, “ULSI Technology” (1996)
1030	Chen, “CMS Devices & Technology for VLSI” (1988)
1031	Jaeger, “Volume V: Introduction to Microelectronic Fabrication” (1988)
1032	U.S. Patent No. 5,776,808 to Muller et al.
1033	U.S. Patent No. 9,236,393 to Cernea

Exhibit	Description
1034	Capogreco et al., “Integration and electrical evaluation of epitaxially grown Si and SiGe channels for vertical NAND Memory applications,” 2015 IEEE International Memory Workshop, 2015
1035	Kim et al., “Three-Dimensional NAND Flash Architecture Design Based on Single-Crystalline Stacked Array,” IEEE Transactions on Electron Devices, Vol. 59, No. 1, Jan. 2012, pp. 35-45
1036	Wagner, “The Use of HBr in Polysilicon Etching,” Gases & Instrumentation International, Vol. 7, Issue 4, July/August (2013) printed from https://www.pall.com/content/dam/pall/microelectronics/literature-library/non-gated/HBr_Polysilicon.pdf
1037	Baker, “CMOS Circuit Design, Layout, and Simulation,” Third Ed. (2010)
1038	Complaint for Patent Infringement, Dkt. No. 1, filed Nov. 9, 2023, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1039	First Amended Complaint for Patent Infringement, Dkt. No. 29, filed Feb. 2, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1040	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.’s Disclosure of Asserted Claims and Infringement Contentions, dated May 6, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL

LISTING OF CHALLENGED CLAIMS

Ref. #	Listing of Challenged Claims
Claim 8:	
[8.PRE]	A three-dimensional (3D) memory device, comprising:
[8.A]	an alternating conductor/dielectric layer stack;
[8.B.i]	a dielectric structure
[8.B.ii]	extending vertically through the alternating conductor/dielectric layer stack;
[8.C]	first and second channel regions comprising first and second pluralities of channel structures, respectively;
[8.D]	slit structures extending vertically through the alternating conductor/dielectric layer stack;
[8.E]	a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;
[8.F]	local contacts disposed on the first and second channel structures and the slit structures;
[8.G.i]	a through array contact (TAC) region
[8.G.ii]	formed between the first and second channel regions,
[8.G.iii]	wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and;
[8.H]	a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.

Ref. #	Listing of Challenged Claims
Claim 10:	
[10.PRE]	The 3D memory device of claim 8, further comprising:
[10.A]	a substrate;
[10.B]	an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and;
[10.C]	an epitaxial layer disposed between the substrate and the first or second channel structures.

I. INTRODUCTION

Pursuant to 35 U.S.C. §§311-319 and 37 C.F.R. §42, Petitioner Micron Technology, Inc. (“Micron” or “Petitioner”) respectfully requests *Inter Partes* Review (“IPR”) of claim 10 (“the Challenged Claim”) of U.S. Patent Number 10,937,806 (“806 Patent”) and cancel that claim as unpatentable. Micron previously filed IPR2024-00791, which challenges a different set of ’806 patent claims. Section II.D. Concurrently filed herewith, Micron’s Explanation for and Ranking of Two Petitions explains the basis for filing this second Petition. Challenged Claim 10 depends on claim 8. This Petition maintains Grounds 1-3 (Toyama) from IPR2024-00791 to demonstrate that the elements of claim 8 are disclosed or rendered obvious. The Petition relies on the same grounds to demonstrate that claim 10 is unpatentable.

The 806 Patent’s title is “Through Array Contact (TAC) for Three-Dimensional Memory Devices.” As its title suggests, the 806 Patent relates to a three-dimensional (3D) NAND memory device with “through array contacts” (“TACs”). TACs are electrical connections that extend through the device’s memory array.

Most of the elements of the Challenged Claim are conventional for 3D NAND memory devices, which existed long before the 806 Patent’s priority date. And the alleged point of novelty—the TACs—were not, in fact, new. The primary prior art

reference discussed in this Petition—Toyama—discloses and/or renders obvious the “through array contacts” and all other elements of the Challenged Claim.

After the Chinese Patent Office found that Toyama rendered unpatentable all claims of the Chinese application in the same family as the 806 Patent, Patent Owner cited Toyama to the U.S. Examiner as one of 22 references in an IDS. But Patent Owner did not provide the U.S. Examiner with the Chinese rejection, which identified specific elements of Toyama that disclose the 806 Patent’s claim limitations. Perhaps due to Patent Owner’s omission of the bases for the Chinese rejection, the Examiner never discussed or relied on Toyama in any rejection, overlooking that Toyama teaches or renders obvious all elements of the Challenged Claim. Confirming this, after Patent Owner appealed the Chinese rejection, a three-member panel of the Chinese Patent Office affirmed that all claims were unpatentable over Toyama. That the U.S. Examiner overlooked material teachings in Toyama means the Board should institute trial here.

Dependent claim 10 adds two trivial limitations: (1) “an epitaxial layer,” which Toyama discloses, and (2) “etch stop plug[s],” which Toyama discloses or renders obvious. Indeed, the Chinese Patent Office found Toyama to disclose these limitations.

In sum, because the Challenged Claim encompasses prior art 3D NAND memory devices, and reflects nothing more than a routine, predictable combination

of known elements, Petitioner requests that the Board institute trial and find the Challenged Claim unpatentable as obvious under Section 103.

II. REQUIREMENTS FOR INTER PARTES REVIEW

A. Grounds for Standing (37 C.F.R. §42.104(a))

Petitioner certifies that the 806 Patent is available for IPR and that no law bars Petitioner from requesting IPR of the Challenged Claim of the 806 Patent on the grounds identified herein.

B. Notice of Lead and Backup Counsel and Service Information (37 C.F.R. §§42.8(b)(3-4), 41.10(a))

Pursuant to 37 C.F.R. §§42.8(b)(3-4) and 41.10(a), Petitioner provides the following designation of Lead and Back-Up counsel.

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Petitioner consents to service by electronic mail at the following addresses: PTABDocketJJL2@orrick.com, P52PTABDocket@orrick.com, PTABDocketJ3B3@orrick.com, T61PTABDocket@orrick.com, PTABDocketP2S7@orrick.com, and micron-ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner attaches a Power of Attorney.

C. Notice of Real-Parties-in-Interest (37 C.F.R. §42.8(b)(1))

Petitioner, Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real-parties in interest.

D. Notice of Related Matters (37 C.F.R. §42.8(b)(2))

According to USPTO assignment records, the 806 Patent is currently assigned to Yangtze Memory Technologies Co., Ltd. (“YMTC” or “Patent Owner”). YMTC has asserted the 806 Patent and U.S. Patent Nos. 10,658,378, 10,861,872, 10,868,031, 10,950,623, 11,468,957, 11,501,822, and 11,600,342 in a co-pending litigation, *Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed November 9, 2023) (“Co-Pending Litigation”).

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation:

Petition for *Inter Partes* Review of U.S. Patent No. 10,937,806

Patent	PTAB Proceeding	Wave 1/Wave 2
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	

The Director and the Board should institute this Petition under 35 U.S.C. §314(a), 325(d), and/or 37 C.F.R. §42.108(a). Concurrently filed herewith, Micron’s Explanation for and Ranking of Two Petitions explains the basis for filing this second Petition challenging a different claim of the 806 Patent.

E. Fee for *Inter Partes* Review

The Director is authorized to charge the fee specified by 37 C.F.R. §42.15(a), and any other required fees, to Deposit Account No. 15-0665.

F. Proof of Service

Petitioner has attached proof of service of this Petition on the Patent Owner at the correspondence addresses of record for the 806 Patent.

III. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. Petitioner meets all other requirements for IPR. The Board should institute IPR.

A. There Are No Grounds for a § 314 Discretionary Denial

There is a pending district court action involving the 806 Patent. The Board should not “discretionarily deny” because the “petition presents compelling evidence of unpatentability.” 6/21/22 Interim Procedure, 2, 4-5.

The *Fintiv* factors also support institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) (“*Fintiv*”).

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”); *Fintiv* at 12 (similar)

2. Proximity of the Court’s Trial Date

Trial is set for December 1, 2025. *See* Ex. 1006. If IPR proceedings are instituted, they should be completed before the scheduled trial date. *See also* Ex.

1007 (on average, 48.9 months to reach trial in district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and Court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings, no substantive progress has been made. The parties are over a month away from completing the exchange of contentions and have not taken any depositions. Fact discovery is in its infancy. No claim construction positions have been exchanged, no claim construction order has issued, no infringement or invalidity expert discovery has occurred, and no summary judgment motions have been filed.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv* at 11. Against eight patents, Petitioner proceeded with diligence, filing eight petitions approximately six months after being served with the original complaint and approximately three months after the filing of an amended complaint. Exs. 1008, 1038-39. Then, Patent Owner asserted new claims against Petitioner on May 6, 2024. Ex. 1040, Within weeks, Petitioner has filed petitions on these new, unforeseen claims.

This factor weighs in favor of institution. *See Sand Revolution* at 11.

4. Issue Overlap

The wave 1 and wave 2 Petitions challenge all asserted claims in the District Court litigation. Should the Board institute, Micron stipulates that it will not advance in District Court any invalidity defense that formed the basis of any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its Petition has significant substantive merit, weighing in favor of institution.

B. Denial Under § 325(d) Would Be Inappropriate

The two-part *Advanced Bionics* framework weighs against section 325(d) denial. At Part I, Patent Owner cited Toyama in an IDS with 21 other references. Regardless, at Part II, the record demonstrates that the Examiner erred by overlooking Toyama's disclosures and failing to reject the claims in light of Toyama.

“[I]f the record of the Office's previous consideration of the art is not well developed or silent, then a petitioner may show the Office erred by overlooking something persuasive.” *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020), 10 (precedential).

The record here is silent as to what, if any, substantive consideration the Examiner gave Toyama. Patent Owner presented Toyama to the Examiner as one of 22 references cited at the same time, and said nothing to make Toyama's materiality over these other references clear. Perhaps reflecting this, the Examiner never discussed Toyama or used it in any rejection. *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 (PTAB Dec. 15, 2017), 22-23 (factor (c)).

What's more, Patent Owner's conduct during prosecution may have kept the Examiner from appreciating Toyama's significance. Before Patent Owner filed the continuation application that led to the 806 Patent, the Chinese Patent Office rejected all claims of the corresponding Chinese patent application as unpatentable over Toyama.¹ Ex. 1010 (CN109075169A Office Action, Nov. 14, 2019), 3-10. The Chinese Patent Office's rejection explained how specific elements of Toyama taught the claim limitations. *Id.* Of particular relevance to this Petition, rejected claim 32 of the Chinese patent application recites the elements ("etch stop plug," "epitaxial layer," and "substrate") of the Challenged Claim here. *Id.* at 9.

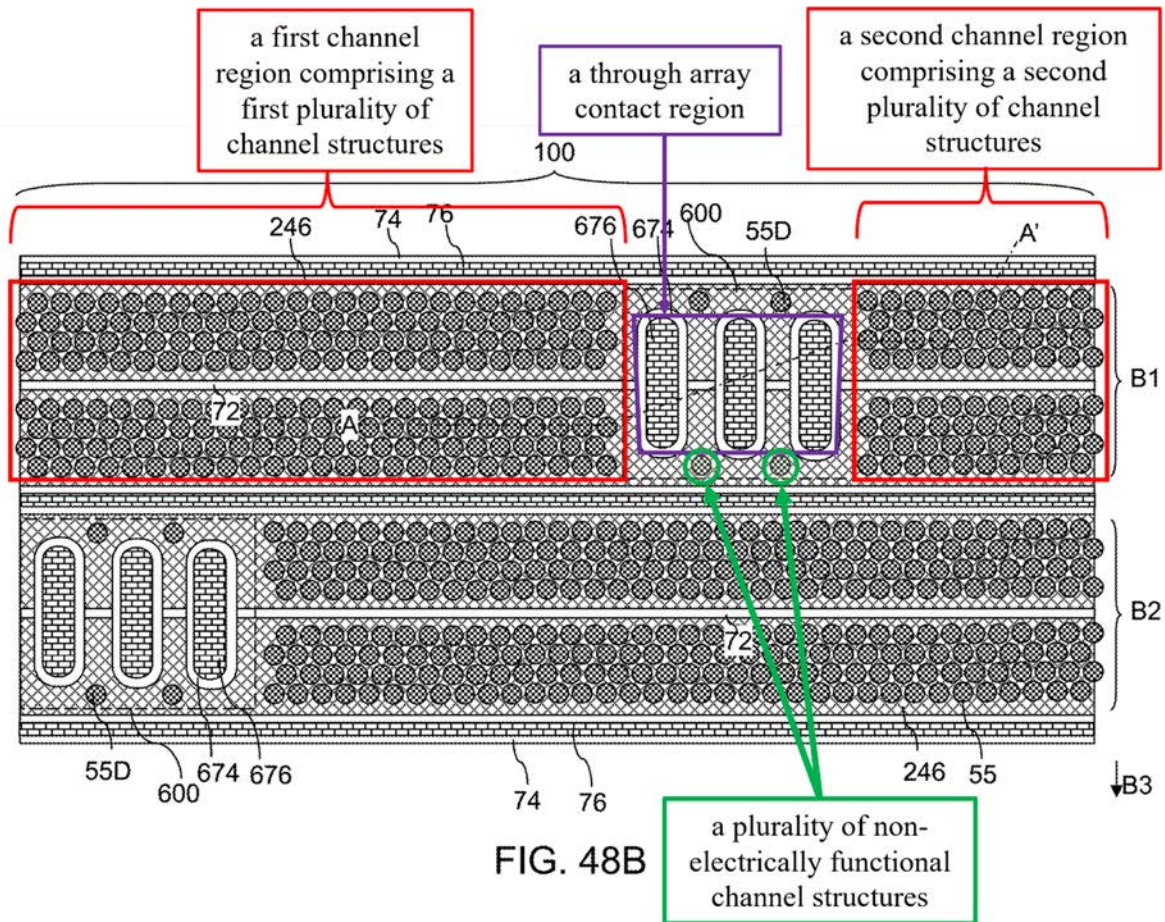
¹ Both the Chinese patent application and the application that issued as the 806 Patent claim priority to, and are national stage applications of, PCT App. No. PCT/CN2018/085421.

Despite this, Patent Owner never notified the Examiner of the rejection or provided the Examiner with the Chinese Patent Office's written rejection or its reasoning. Patent Owner's failure to disclose the Chinese Patent Office's reasoning—including the specific relied-upon elements of Toyama—may have been especially material because of Toyama's length (the reference spans 143 figures and 178 pages). In essence, Patent Owner only gave the Examiner a haystack (i.e., Toyama) despite also knowing the location of the needle (i.e., the specific elements of Toyama identified by the Chinese Patent Office).

The Petition demonstrates that the Examiner erred by overlooking specific teachings in Toyama. *Becton*, 24-25 (factor (e)). The Examiner found that the limitations recited in challenged claim 10 were known in the art.² The Examiner only allowed the Challenged Claim after the applicant amended the independent claim on which it depends (now claim 8) to include three additional elements. Ex. 1002, 130. As Ground 1 demonstrates, Toyama's Second Modification clearly discloses each of these elements (806 Patent claim language in red, exemplary disclosures from Toyama in parentheses):

² Challenged claim 10 was originally numbered as claim 12. Ex. 1002, 54. Original claim 12 was rejected as obvious in view of the prior art. *Id.*, 108-109.

1. *first and second channel regions* (first and second parts of “memory array region 100”) *comprising first and second pluralities of channel structures* (first and second pluralities of “memory stack structures 55”), *respectively*;
2. *a through array contact (TAC) region* (part of “through-memory-level via region 600”) *formed between the first and second channel regions* (first and second parts of “memory array region 100”), *wherein the TAC region* (part of “through-memory-level via region 600”) *comprises a plurality of through array contacts (TACs)* (“through-memory-level via structures 676”); and
3. *a plurality of non-electrically functional channel structures* (“dummy memory stack structures 55D”) *surrounding the TAC region* (part of “through-memory-level via region 600”) *and between the first and second channel regions* (first and second parts of “memory array region 100”):



Toyama, Fig. 48B;³ Ex. 1002, 130.

This Petition also provides evidence not before the Examiner. *Becton*, 25-28 (factor (f)). In Ground 2, Dr. Lee explains with reference to textbooks and other evidence that it was well-known and desirable to implement a flash memory device with multiple flash memory **planes**. As the Petition explains, implementing multiple planes of Toyama's first exemplary structure renders the Challenged Claim's independent claim obvious. See §X.A. The Examiner was apparently unaware that

³ All colored annotations in figures are added.

a POSITA would have known about flash memory planes. In Ground 3, Dr. Lee explains that it was well known and desirable to combine the teachings of Toyama’s first exemplary structure and its Second Modification to implement the obviousness combination. See §XI.A. There is no indication that the Examiner was aware that a POSITA would have been motivated to implement, with a reasonable expectation of success, this obviousness modification.

The prosecution history at the Chinese Patent Office confirms Toyama’s merit as an invalidating reference. After the Chinese final rejection, Patent Owner appealed. On appeal, a three-judge panel of the Chinese Patent Office affirmed. Ex. 1012 (Reexamination Decision, dated Nov. 25, 2021). Notably, the Chinese Patent Office relied on the same teachings as the present Petition for the elements of challenged claim 10: Toyama’s “planar semiconductor material layer 10” being *a substrate*, “drain region 63” being *an etch stop plug*, and Toyama’s “pedestal channel portions 11” being *an epitaxial layer*.

Because the Examiner overlooked specific teachings in Toyama that disclose the apparent point of novelty, the Board should not discretionarily deny institution.

IV. IDENTIFICATION OF CLAIMS BEING CHALLENGED (§42.104(B))

This Petition assumes the earliest-listed priority date of May 3, 2018 (the “Priority Date”).

Petitioner relies on the following primary reference: U.S. Pat. Pub. No. 2017/0179026 (Ex. 1005, “Toyama”). Toyama’s filing date is September 19, 2016, published on June 22, 2017, and is thus prior art under 35 U.S.C. §§ 102(a)(1) and 102(a)(2).

Petitioner challenges claim 10 on the following grounds:

Ground 1: Claim 10 is obvious in view of Toyama’s second modification to its fourth exemplary structure (“Second Modification”) and the knowledge of a POSITA.

Ground 2: Claim 10 is obvious in view of Toyama’s first exemplary structure and the knowledge of a POSITA.

Ground 3: Claim 10 is obvious in view of Toyama’s first exemplary structure, Toyama’s Second Modification, and the knowledge of a POSITA.

The Declaration of Dr. Jack C. Lee (Ex. 1003, “Lee”) supports these grounds.

V. THE 806 PATENT

A. Technology Background

1. 3D NAND Memories

“NAND” flash memory is a particular type of non-volatile flash memory. Ex. 1013, 41. Current flows from the “drain” of the memory cell to its “source.” *Id.*, 150. Lee ¶¶ 40-44.

Initially, a NAND flash memory was “planar” (2D). Ex. 1013, 86. Well before the Priority Date, Petitioner and others had developed 3D NAND flash

memory. In a 3D NAND flash memory, memory cells exist in vertical, cylindrical NAND flash “strings”:

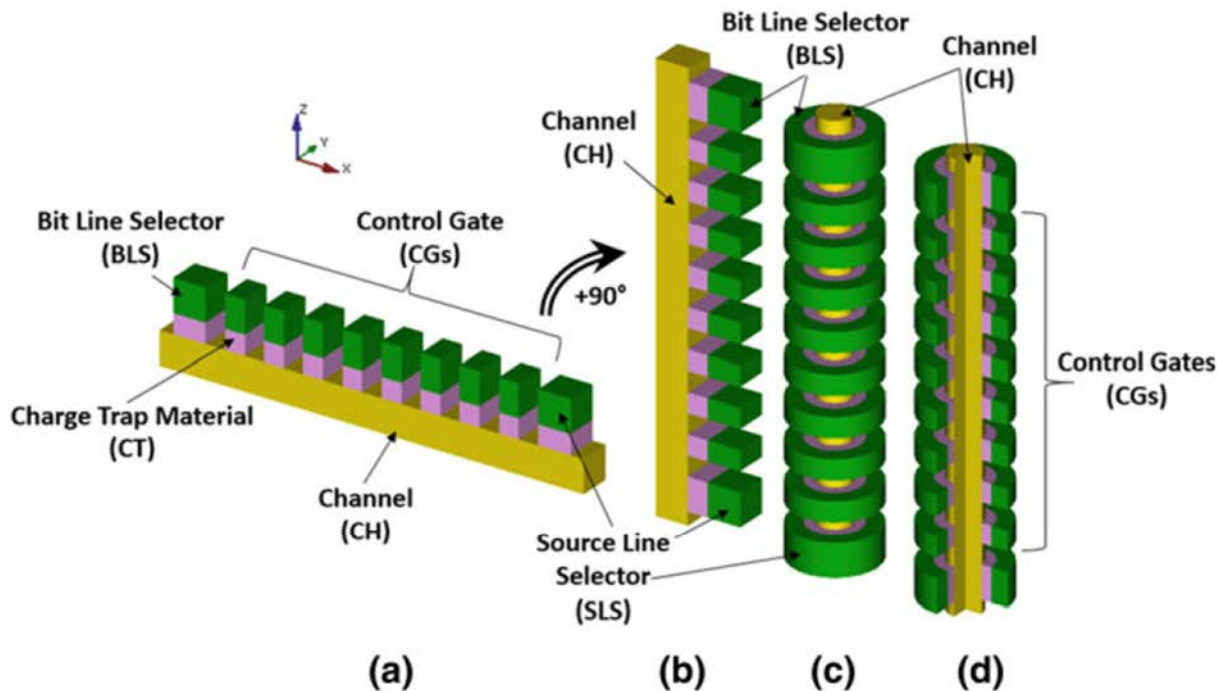


Fig. 4.1 NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

Id., 102; Lee ¶¶ 45-49.

For example, in the well-known BiCS (Bit Cost Scalable) architecture, several types of “contacts,” that is, electrical connections, are on top of the memory array. These include source line contacts, labeled a “SL connection,” for providing a ground connection to the memory cells:

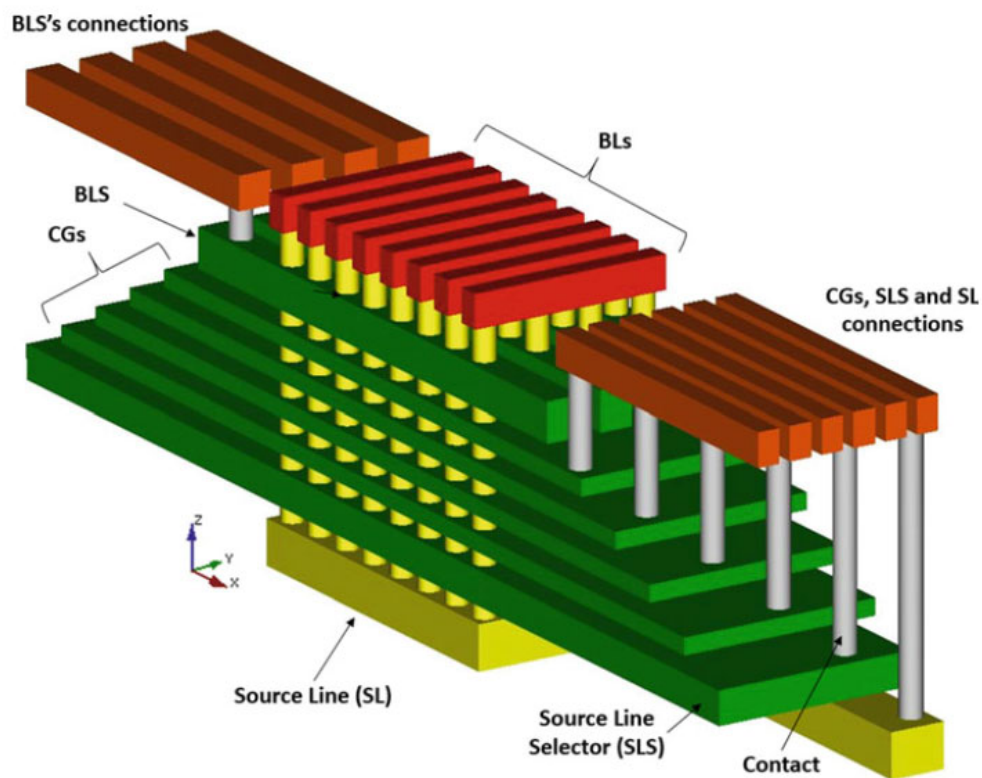


Fig. 4.13 Top bird's eye view of BiCS with gate connections

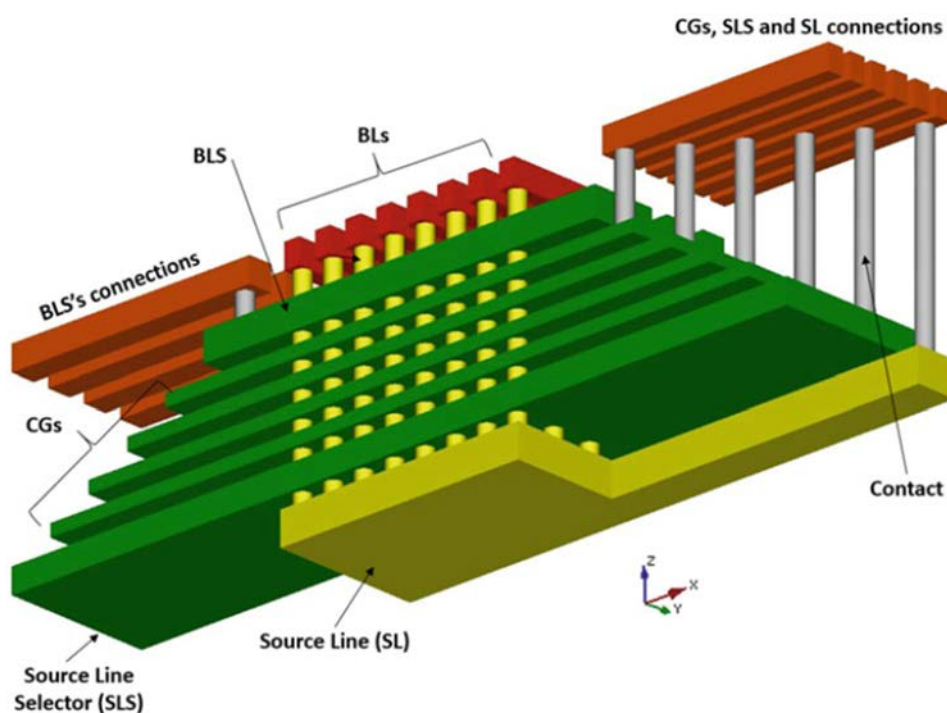


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1013, 109-110; Lee ¶ 50. The memory cells' control gates form a staircase structure as shown below:

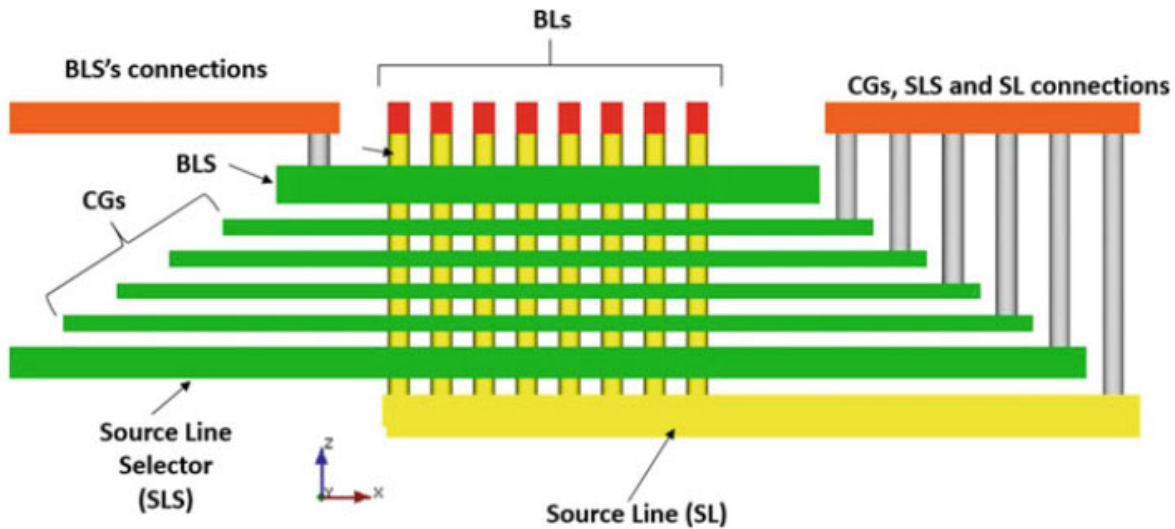


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1013, 109. The grey columns contacting the top surface of each control gate (shown above in green) are “word line contacts.” Lee ¶¶ 51-52.

Various modifications to the BiCS structure were known, including the use of slit structures to serve as a source line contact for the NAND strings:

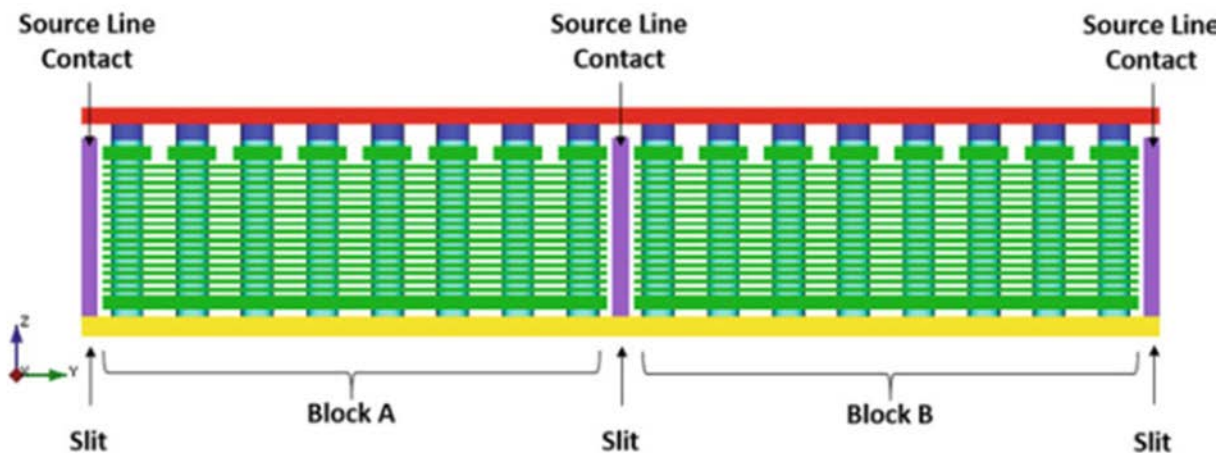


Fig. 6.8 Side view of Fig. 6.7

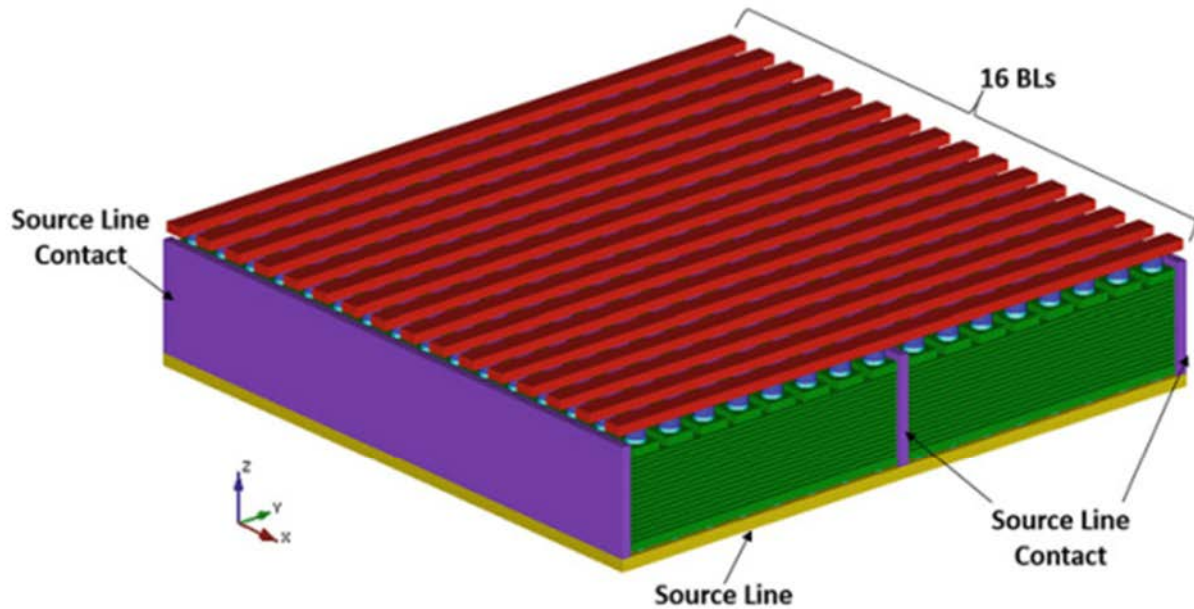


Fig. 6.7 Array slits

Ex. 1013, 185.

Three-dimensional NAND memory devices commonly used support pillars (e.g., dummy channels) to maintain the device's structural integrity, e.g., when etching away sacrificial gate layers. Ex. 1015, [0051]; Lee ¶¶ 55-59.

2. Epitaxy

As of the priority date, a POSITA would have well understood the semiconductor manufacturing process of "epitaxy," which involves depositing a crystalline layer of material onto a crystalline substrate in a way that the crystallographic orientation of the deposited material matches that of the substrate. Lee ¶¶ 60-64; Ex. 1029, 132 (discussing epitaxy); Ex. 1030, 65 (same). Epitaxy may involve chemicals such as "hydrogen and chlorosilanes, such as silicon tetrachloride (SiCl_4), trichlorosilane (SiHCl_3), and dichlorosilane (SiH_2Cl_2). In addition, silane

(SiH₄) has also been used when a lower growth temperature is desired.” Ex. 1029, 143.

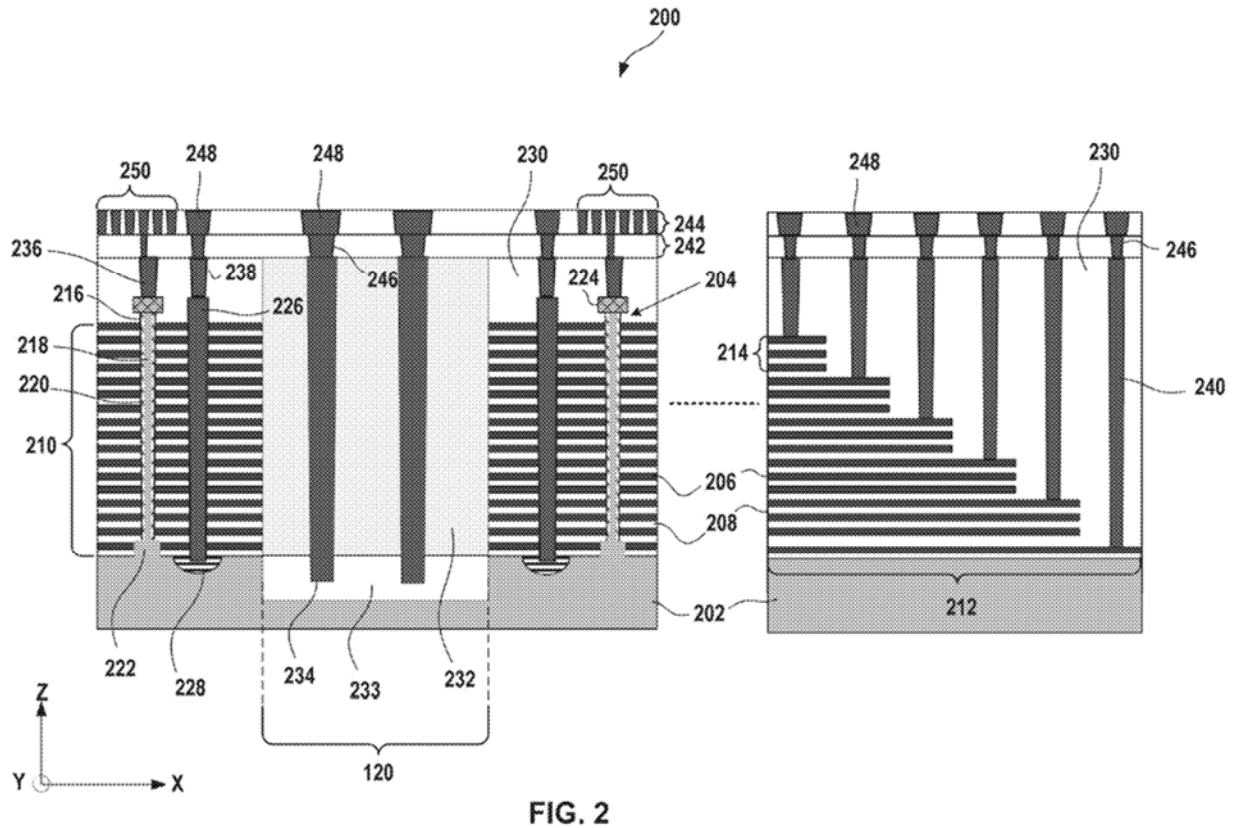
3. Etching

“Etching” is a well-known semiconductor manufacturing technique for removing material. Lee ¶¶ 65-70; Ex. 1029, 356-357; Ex. 1031, 35-36. A POSITA would have known of chemicals used for etching (etchants) that are “selective,” that is, they will react with some materials preferentially to others. Lee ¶ 66; Ex. 1031, 35.

A POSITA would have known of the common use of a material to which an etchant is **not** selective to serve as an “etch stop,” that is, to prevent the etch from removing material not intended to be removed. Lee ¶ 71. For example, a POSITA would have known of the use of polysilicon to stop an etch through silicon oxide. *Id.*; Ex. 1029, 363-364; Ex. 1032, 4:25-35; Ex. 1033, 17:20-24.

B. The 806 Patent

The 806 Patent’s title is “Through Array Contact (TAC) For Three-Dimensional Memory Devices.” The 806 Patent describes a “3D memory device 200” that, by and large, has a structure similar to the well-known and conventional BiCS architecture described above:



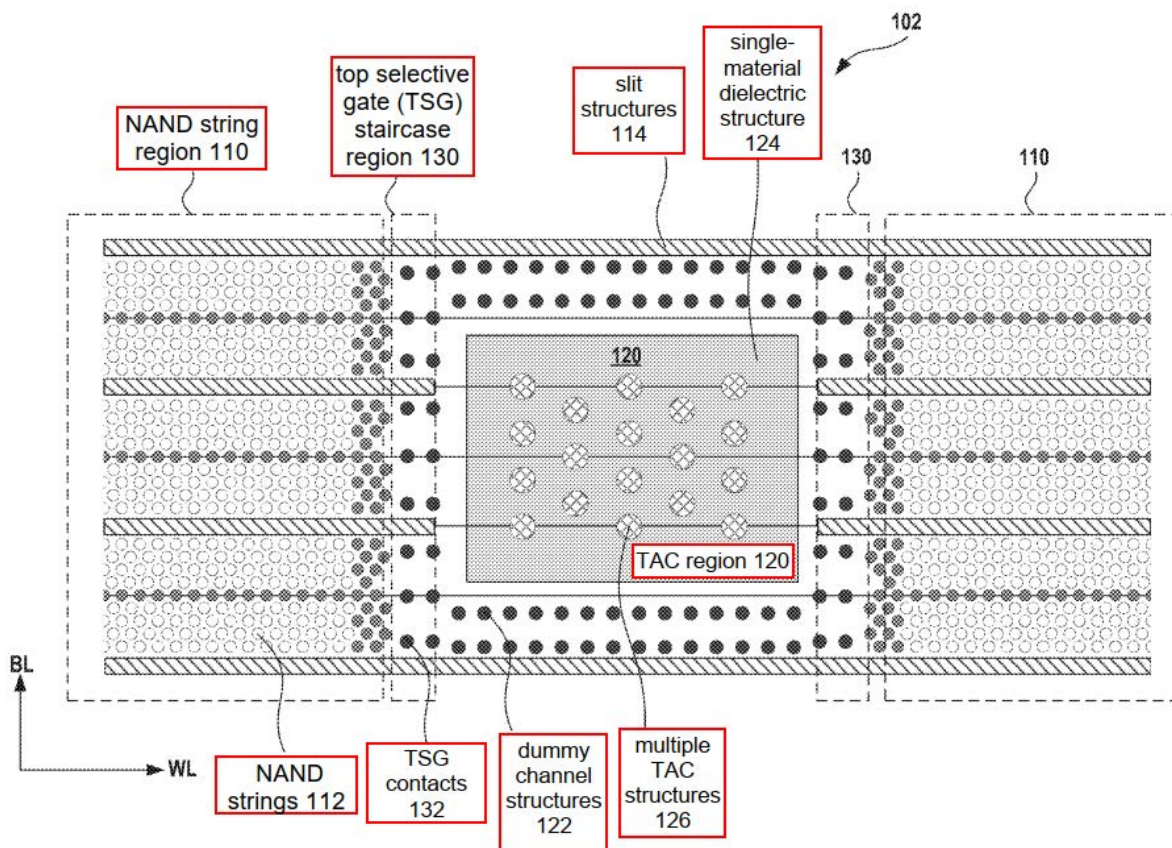
Ex. 1001, Fig. 2.

The memory cells of the 3D memory device are within “NAND strings 204,” each of which “includes a channel structure 216 that extends through alternating conductor/dielectric stack 210.” *Id.*, 9:7-9.

As reflected in the 806 Patent’s title, the disclosed 3D memory device’s alleged point of novelty is the “vertical interconnects between [a] stacked array device” (e.g., “3D memory device 200”) and “a peripheral device” (e.g., a control chip). *Id.*, 5:30-61. The 806 Patent refers to these “vertical interconnects” as “through array contacts” (“TACs”). *Id.*, 1:52-55. “In some embodiments, TACs

234 can provide electrical connections between 3D memory device 200 and the peripheral device (e.g., on a CMOS chip; not shown in FIG. 2).” *Id.*, 11:8-13.

“Multiple TAC structures 126 can be formed within TAC region 120 in dielectric structure 124.” *Id.*, 6:20-22. “In some embodiments, dummy (e.g., non-electrically functional) channel structures 122 are formed outside TAC region 120 to provide mechanical support to the memory structures.” *Id.*, 6:22-25. Fig. 1A, below, shows the “NAND string regions” 110, “dummy channel structures” 122, the “TAC region” 120, and “TAC structures” 126:



Id., Fig. 1A.

As to claim 10 and its reference to an epitaxial layer and etch stop plug, the '806 patent discloses: "each NAND string 204 includes an epitaxial layer 222 and an etch stop plug 224 at the respective bottom and top of NAND string 204." *Id.*, 9:36-53.

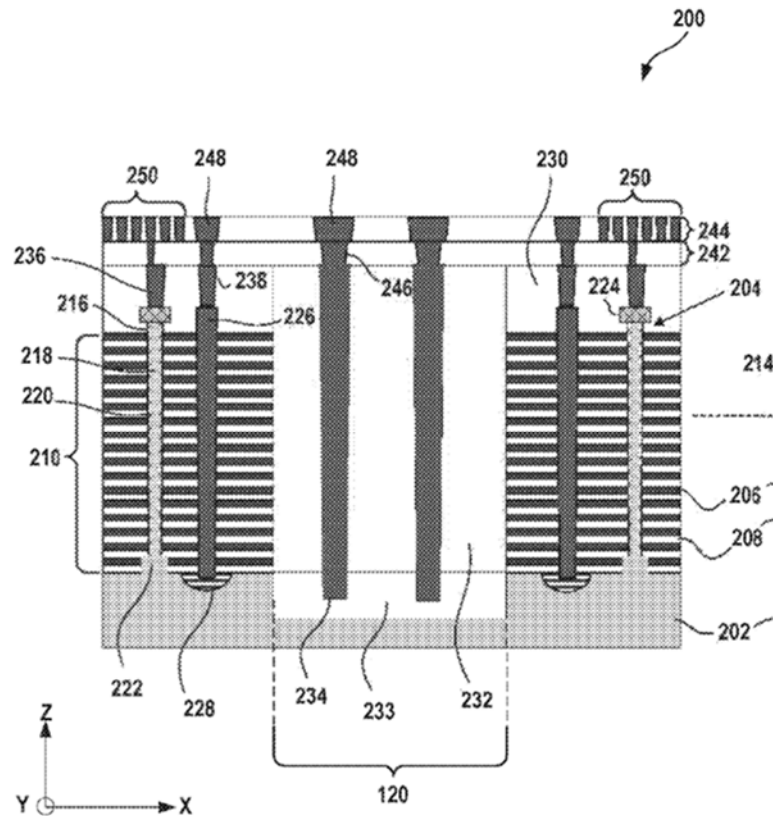


FIG. 2

Id., Fig. 2.

C. Prosecution History of the 806 Patent

During prosecution of the 806 Patent, the Examiner rejected the then-pending independent claims as obvious over U.S. Pat. No. 9,659,956 ("Pachamuthu") in view of U.S. Pat. Publ. 2017/0186758 ("Lee"). Ex. 1002, 105. The Examiner found

original claim 12 (now challenged claim 10) rendered obvious by these references. *Id.*, 108-109. In response, PO amended then claim 9 (issued independent claim 8, on which challenged claim 10 depends) to add the following three elements:

- “first and second channel regions comprising first and second pluralities of channel structures, respectively”;
- “a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs)”;
- “a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.”

Id., 130.

The Examiner allowed the claims after this amendment. *Id.*, 153. The Examiner did not indicate what elements of then claim 9 (now independent claim 8) distinguished the claim over the prior art.

Although Patent Owner cited the Toyama reference in an IDS at the same time as **twenty-one** other references, the Examiner never employed Toyama in any rejection or even discussed Toyama’s teachings. As the Petition explains below, Toyama teaches or renders obvious all elements of the Challenged Claim.

VI. DESCRIPTION OF THE PRIOR ART—TOYAMA

Toyama's title is "Through-Memory-Level Via Structures For A Three-Dimensional Memory Device." Toyama discloses the conventional features of a 3D memory device claimed by the 806 Patent. *E.g.*, Toyama, Figs. 17A-F. And, like the 806 Patent, Toyama discloses 3D NAND memory devices with electrical connections ("through-memory-level via structures" in Toyama's parlance) that extend through the memory array to provide a connection to "peripheral" devices. *Id.*, [0164] (discussing "peripheral device region 700" located underneath the "memory-level assembly").

Toyama discloses four "exemplary structures," each of which is an embodiment of Toyama's invention. Each exemplary structure incorporates the teachings of previously described exemplary structures. Toyama, [0261] (second exemplary structure), [0277] (third exemplary structure), [0310] (fourth exemplary structure). Toyama also discloses a number of "modifications" to its "exemplary structures," which also incorporate the teachings of previously described embodiments. *Id.*, [0332] (second modification to fourth exemplary structure).

Grounds 1 and 2 each focus on a different aspect of Toyama's disclosure. Ground 1 focuses on Toyama's Second Modification. Ground 2 focuses on Toyama's first exemplary structure. Ground 3 relates to a combination of these two structures.

VII. CLAIM CONSTRUCTION

For purposes of this Petition, Petitioner submits that the terms of the 806 Patent's claims do not require further construction and should receive their plain and ordinary meaning. Lee ¶¶ 88-91.

VIII. LEVEL OF SKILL IN THE ART

A POSITA in the field of the 806 Patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). Lee ¶¶ 35-39. This POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND's structure, its component parts, how it operates, and how it is controlled. *Id.*

IX. GROUND 1: TOYAMA'S SECOND MODIFICATION IN VIEW OF THE KNOWLEDGE OF A POSITA

For the following reasons, Toyama's second modification to its fourth exemplary structure ("Second Modification," in short) in view of the knowledge of a POSITA renders claim 10 obvious.

A. Claim 8:

1. [8.PRE]⁴

To the extent the preamble is limiting, Toyama discloses *a three-dimensional (3D) memory device*. Toyama, [0156] (“three-dimensional non-volatile memory devices”); Lee ¶ 105.

2. [8.A]

Toyama’s “alternating stack (132, 146, 232, 246)⁵” is *an alternating conductor/dielectric layer stack*:

⁴ For the limitations of claim 8 (which is challenged by Petitioner in IPR2024-00791 and is not the Challenged Claim here), the Petition refers to the above Listing of Challenged Claims.

⁵ In a clear typographical error, Fig. 49 (as well as Figs. 47A and 48A) labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142 and 242 are “sacrificial material layers” which, in a previous process step, were removed and replaced with “electrically conductive layers (146, 246).” Toyama, [0337], [0340]. That is also reflected in the figures, which depict how the sacrificial material layers (shaded in gray, as in Fig. 45A) are replaced by electrically conductive layers (cross-hatched, as in Fig. 46A). A POSITA would therefore have understood that elements 142 and 242 in Figs. 47A, 48A, and 49 were intended to be labeled 146 and 246, respectively. Lee ¶ 107.

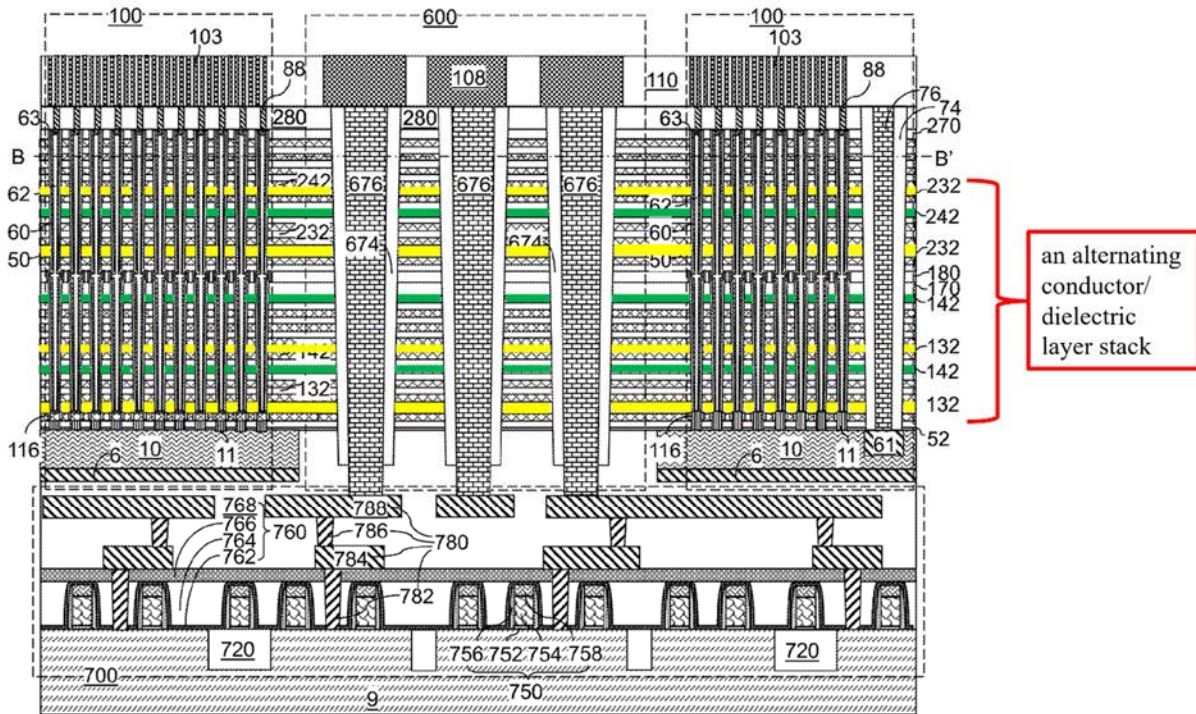


FIG. 49

Toyama, Fig. 49, [0337].

Toyama explains that its “alternating stack” comprises “electrically conductive layers (146, 246)” (representative layers highlighted in green above), and “insulating layers (132, 232)” (representative layers highlighted in yellow above).

Toyama, [0337]; Lee ¶ 108.

3. [8.B]

a. [8.B.i]

In Toyama’s Second Modification, “insulating liners 674” are *a dielectric structure*:

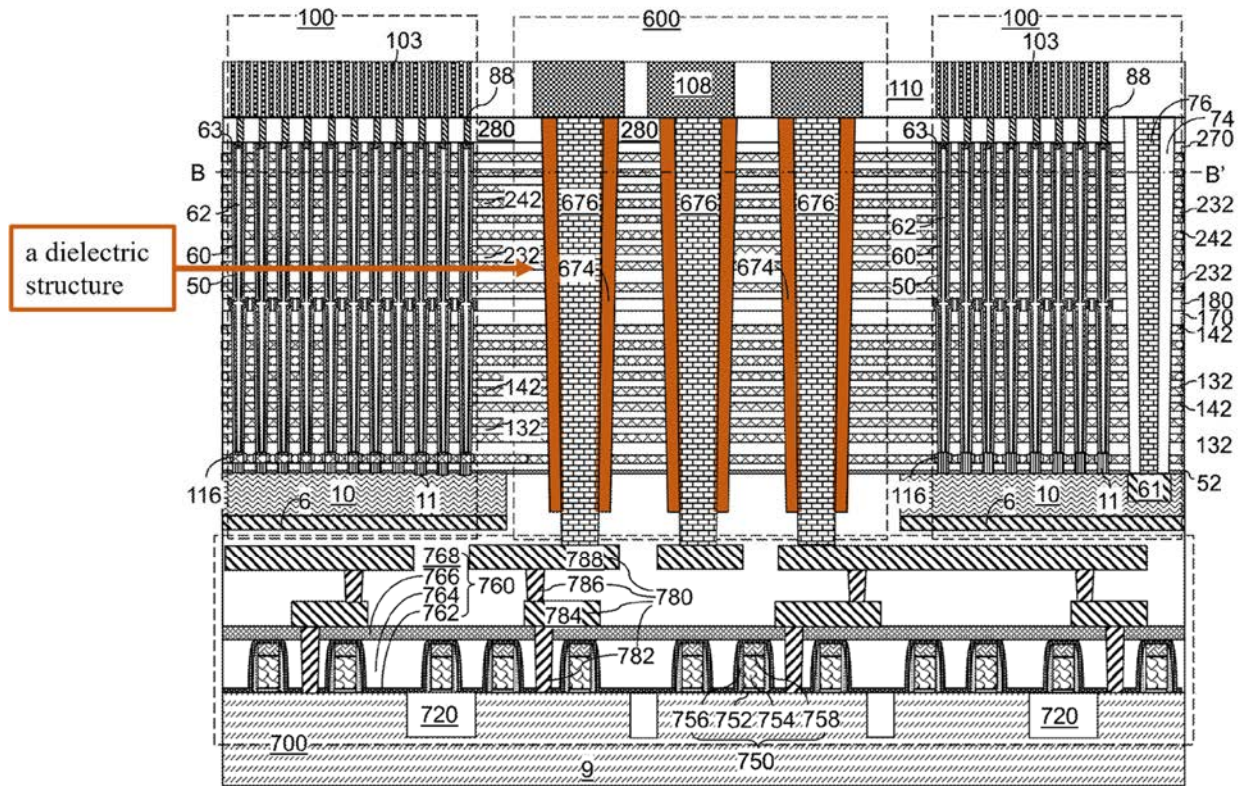


FIG. 49

Toyama, Fig. 49, [0340]; Lee ¶¶ 110-115.

“Insulating liners 674” are *dielectric*. Toyama forms “insulating liners 674” by depositing “a conformal insulating material layer” in “through-memory-level openings 679.”⁶ Toyama, [0338]-[0340]. Insulating liner 674 may be a “dielectric material.” *Id.*, [0233] (“[a]n insulating spacer 74 including a dielectric material”),

⁶ Although Toyama [0338] refers to “through-memory-level openings 689,” that is a typographical error. All of the relevant figures (*e.g.*, Figs. 47A-B to 49) and other textual description refer to the elements as “through-memory-level openings 679.”

[0381] (“insulating liner 674 having a same material composition and a same thickness as the insulating spacer 74”); Lee ¶¶ 111-112.

To the extent Toyama does not expressly disclose this limitation, it would have been obvious to a POSITA. Lee ¶ 114. By its very terms, “insulating liner 674” is insulating, and a POSITA would have known silicon oxide to be a commonplace and desirable (e.g., easy to form) insulating material from which to make “insulating liner 674.” Ex. 1018, 2:61-65 (“dielectric structure” may comprise an “oxide” such as “silicon oxide”); Ex. 1019, 7:37-38 (“silicon oxide film 44 serving as an insulating film”); Ex. 1020, 7:30-40 (“the liner insulating layer may include a silicon oxide layer”).

“Insulating liners 674” are a *structure*. Because these components together are something “that is constructed,” they are a structure. Ex. 1021, 5 (Merriam-Webster definition of “structure” as “something ([such] as a building) that is constructed”); Lee ¶ 113.⁷ And all of the “liners 674” have the same function of

⁷ If Patent Owner argues that “insulating liners 674” are multiple structures and not collectively a single structure, that would be incorrect for the reasons above. Regardless, the Federal Circuit has “repeatedly emphasized that an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’” *KCJ Corp. v. Kinetic*

insulating and electrically isolating the *through array contacts* (“through-memory-level via structures 676”) as they pass through the *alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246).”

Thus, Toyama’s Second Modification discloses, or renders obvious, *a dielectric structure* (“insulating liners 674”).

b. [8.B.ii]

As noted above, Toyama’s “insulating liners 674” are *a dielectric structure*. And Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating conductor/dielectric layer stack*. §IX.A.2IX.A.2. Thus, as shown in the figure below, Toyama discloses *a dielectric structure* (“insulating liners 674”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack 132, 146, 232, 246”):

Concepts, Inc., 223 F.3d 1351, 1356 (Fed. Cir. 2000). The claims encompass a device with multiple dielectric structures.

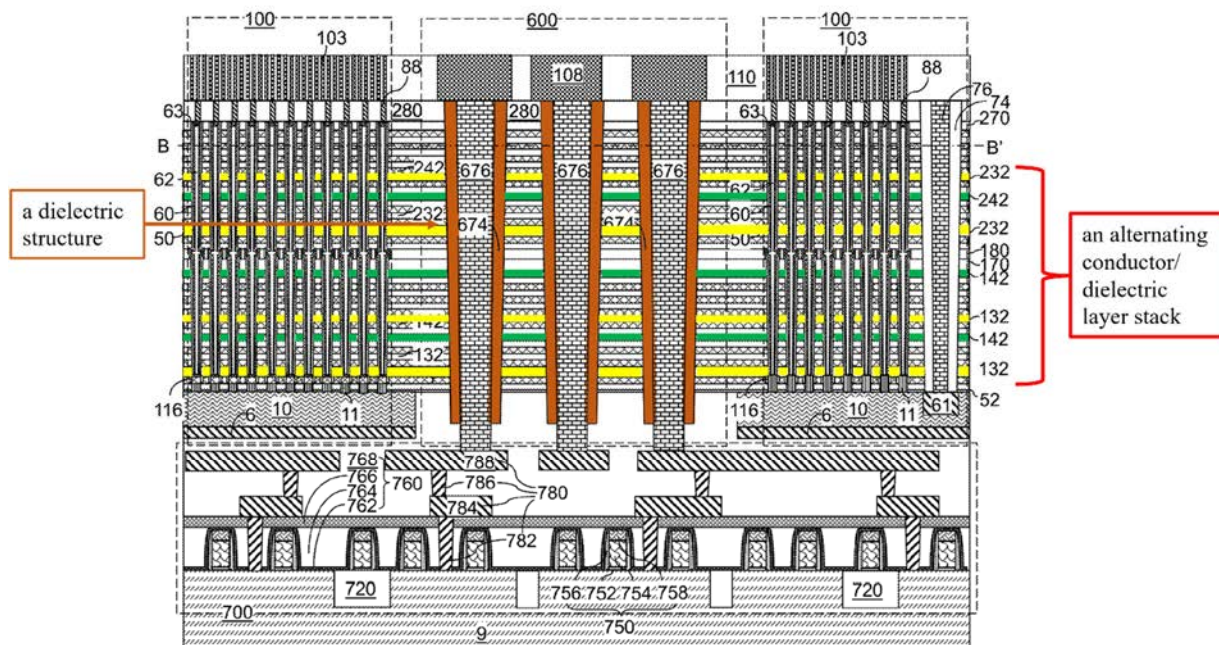


FIG. 49

Toyama, Fig. 49;⁸ Lee ¶ 116.

4. [8.C]

Each of Toyama’s “memory stack structures 55” is *a channel structure*, and parts of Toyama’s “memory array region 100” are each *a channel region*:

⁸ As noted in footnote 5, above, labels 142 and 242 are properly understood to refer to “electrically conductive layers (146, 246).”

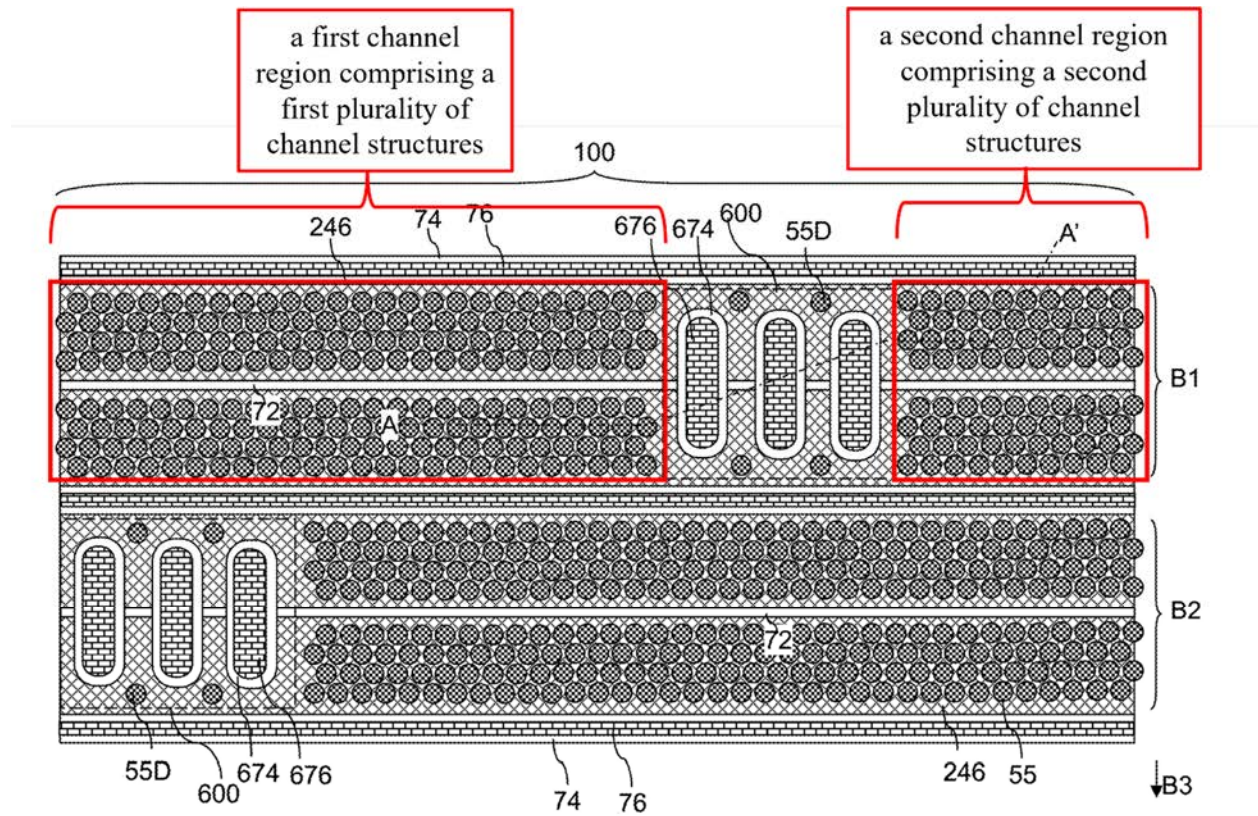


FIG. 48B

Toyama, Fig. 48B, [0323], [0333]; Lee ¶ 117.

Toyama also shows a side view of the *first and second channel regions* (first and second parts of “memory array region 100”):

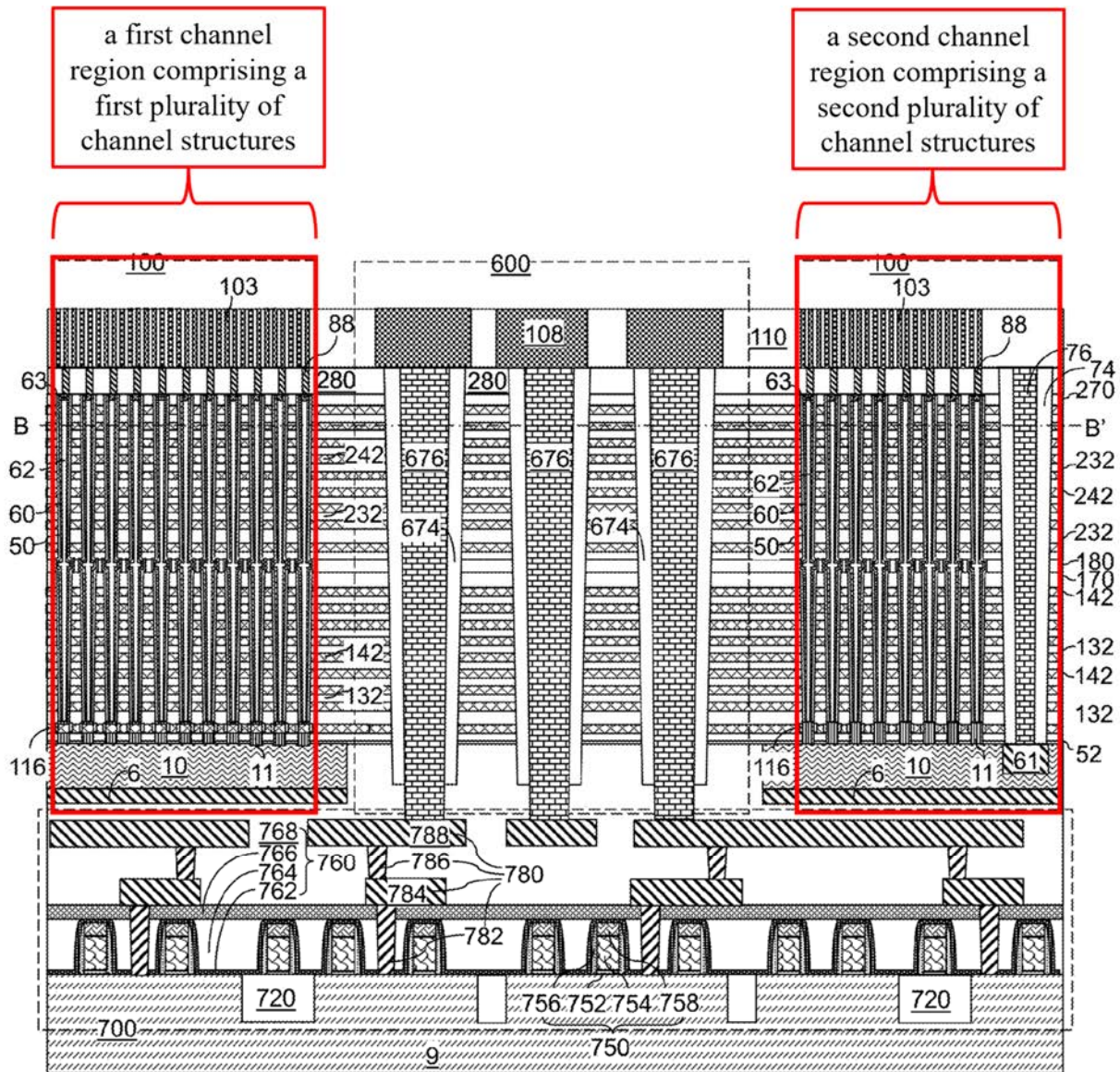


FIG. 49

Toyama, Fig. 49;⁹ Lee ¶¶ 118-120.

⁹ A POSITA would have understood Fig. 49 to include “memory stack structures” even though elements 55 is not labeled in this figure. Lee ¶ 118.

Although not a claim requirement, Toyama’s “memory stack structures 55” perform the same function and are composed of the same components as the 806 Patent’s *channel structures*. Compare Ex. 1001, 9:9-12, 14:8-19 with Toyama, [0210], [0388].

The first and second parts of the “memory array region 100” are *channel regions* because they comprise the regions where the *channel structures* (“memory stack structures 55”) are located.

Toyama thus discloses *first and second channel regions* (first and second parts of “memory array region 100”) *comprising first and second pluralities of channel structures* (first and second pluralities of “memory stack structures 55”).

5. [8.D]

Toyama discloses *slit structures* (“laterally-elongated contact via structures 76”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”):

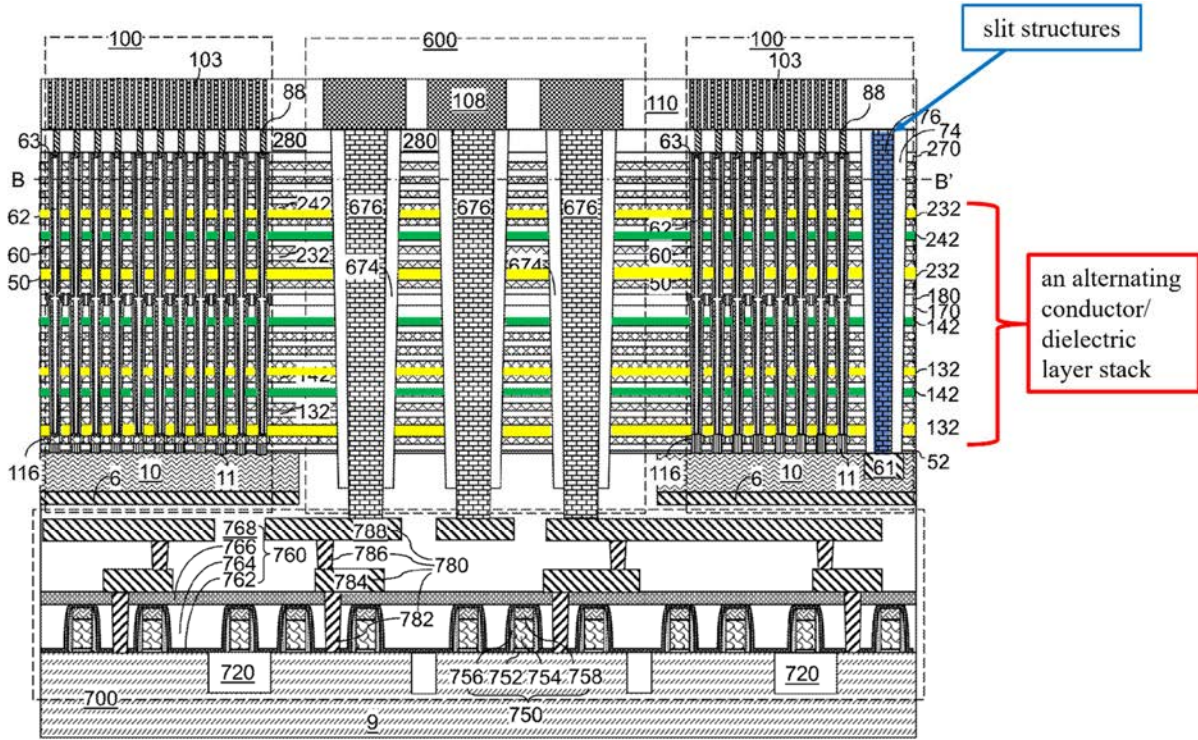


FIG. 49

Toyama, Fig. 49, [0318]-[0320]; Lee ¶¶ 121-123. Toyama also depicts its *slit structures* (“laterally-elongated contact via structures 76”) in a top view:

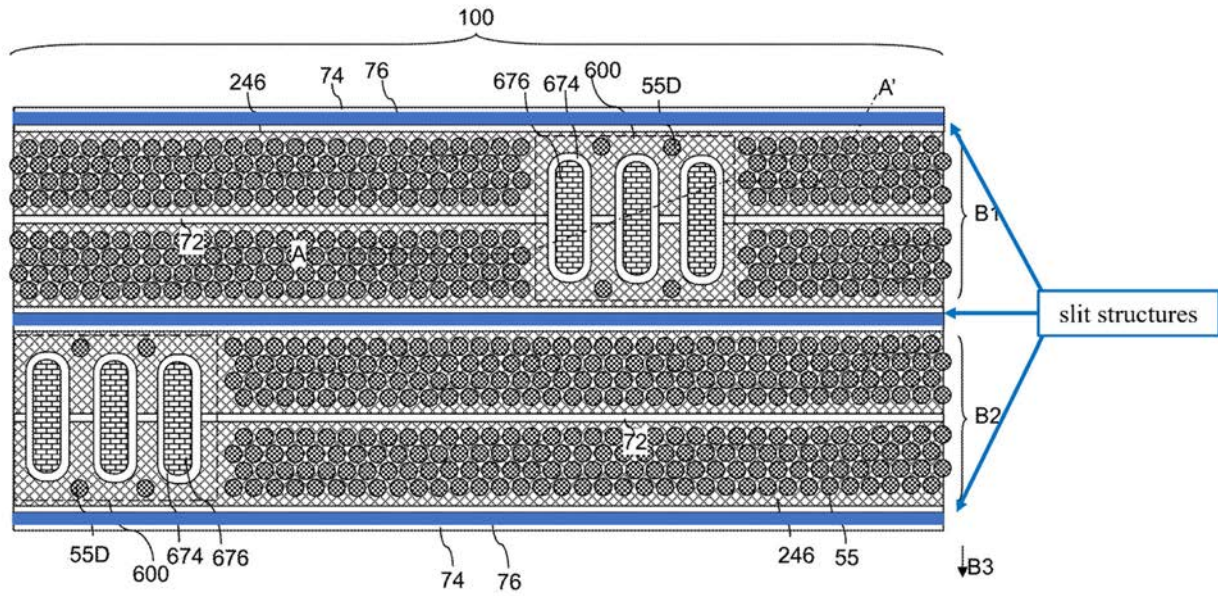


FIG. 48B

Toyama, Fig. 48B.

Although Toyama and the 806 Patent’s claim use slightly different terminology, each of Toyama’s “laterally-elongated contact via structures 76” is *a slit structure*. Lee ¶ 122. The plain meaning of “slit” is a laterally-elongated structure. *Id.*; Ex. 1021, 4 (definition of “slit” as “a long narrow cut or opening”); Toyama, Fig. 48B (structure 76 has a slit shape). And, as shown in Fig. 49, above, Toyama discloses “laterally-elongated contact via structure 76” *extending vertically in the alternating layer stack* (“alternating stack (132, 146, 232, 246)”). Thus, Toyama’s “laterally-elongated contact via structures 76” meets the plain language of the claims.

Although the claims do not place any functional limitation on the *slit structure*, Toyama’s “laterally-elongated contact via structures 76” serve the same

function as the 806 Patent’s “slit structures 226.” Lee ¶ 123. In the 806 Patent, each “slit structure 226” “acts as a source contact for NAND strings 204.” Ex. 1001, 9:63-10:2. Similarly, each of Toyama’s “laterally-elongated contact via structures 76” serves as a “source connection.” Toyama, [0241]. The 806 Patent’s “[s]lit structures 226 ... extend along the y-axis to separate alternating conductor/dielectric stack 210 into multiple blocks.” Ex. 1001, 9:57-59. Similarly, “structures 76 laterally extend along the first horizontal direction ... and laterally divide the at least one alternating stack ... into a plurality of laterally spaced-apart blocks.” Toyama, [0237].

6. [8.E]

As shown below, Toyama discloses *a staircase structure* (“staircase regions”) *disposed in the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”), *wherein the staircase structure comprises levels with each level having a conductor layer* (“electrically conductive layers 146, 246”) *thereon*:

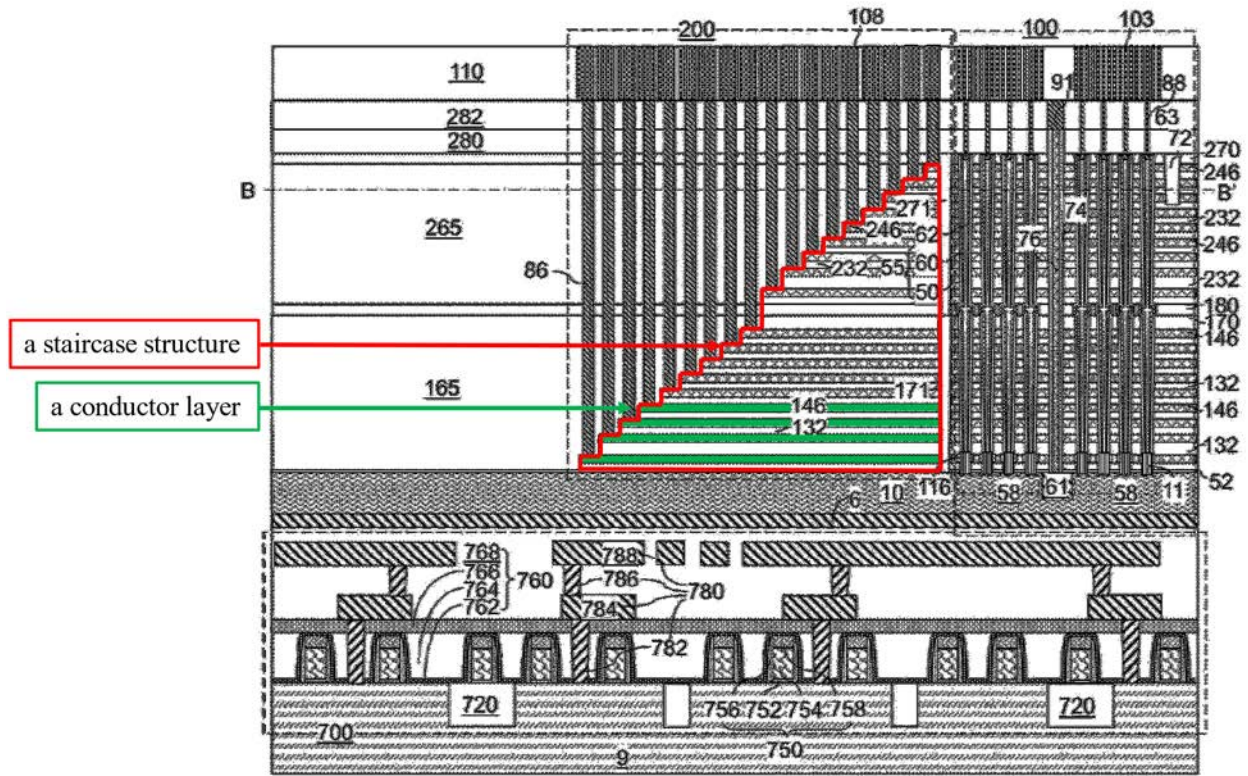


FIG. 17C

Toyama, Fig. 17C; Lee ¶¶ 124-126. Toyama explains: “[t]he at least one alternating stack (132, 146, 232, 246) comprises staircase regions that include terraces in which each underlying electrically conductive layer (146, 246) extends farther along the first horizontal direction hd1 than any overlying electrically conductive layer (146, 246).” Toyama, [0232].

Although the citations above are for Toyama’s “first exemplary structure,” a POSITA would have understood that Toyama’s Second Modification also teaches this limitation. In describing the fourth exemplary structure, Toyama notes that “word line contact via structures [86] can be formed as in the first through third embodiments.” Toyama, [0322]. As Toyama shows for the first embodiment, “word

line contact via structures 86” are in contact with the electrically conductive layers (146, 246) in the “staircase regions.” Toyama, Fig. 17C, [0243]. A POSITA therefore would have understood Toyama’s Second Modification to include *a staircase structure* (“staircase regions”). Lee ¶ 125.

At the very least, a POSITA would have found it obvious to implement a staircase structure (“staircase regions”) in Toyama’s Second Modification. A POSITA would have known that for the memory device to be functional, there must be some way of conveying signals to the “electrically conductive layers (146, 246)” because these layers are the word lines. Toyama, [0323]. A POSITA would have found it obvious to use *a staircase structure* (“staircase regions”), as Toyama already discloses, to enable word line connections. *Id.*, [0322]-[0323]; Lee ¶ 126. These were conventional in 3D memory devices and routine to implement. *See* §V.A.1.

7. [8.F]

As an initial matter, the 806 Patent states that “[i]n some embodiments, 3D memory device 200 includes a plurality of ‘local contacts.’” Ex. 1001, 11: 20-21. “The contacts are referred to herein as ‘local contacts’ because they are in direct contact with the memory array structures, and further because they are formed within dielectric layer 230.” *Id.*, 11: 24-28.

a. “local contacts disposed on the first and second channel structures”

Toyama discloses *local contacts* (“drain contact via structures 88”) *disposed on* (in contact with or extending above) *the channel structures* (“memory stack structures 55”):

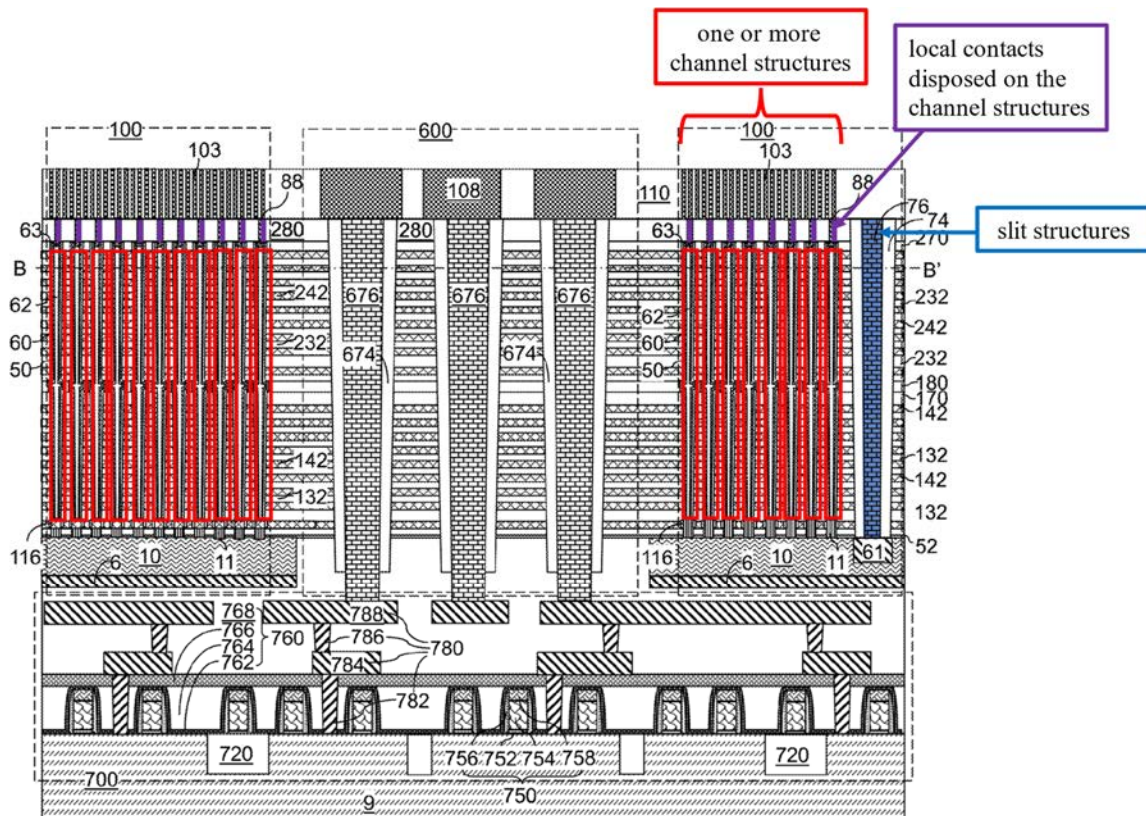


FIG. 49

Toyama, Fig. 49, [0251] (noting that bit lines couple to memory stack structures 55 via structures 88);¹⁰ Lee ¶ 128.

¹⁰ Here, as in Petitioner’s prior petition (IPR2024-00791) challenging the 806 Patent, Petitioner explains that Toyama’s “memory stack structures 55” are the claimed

b. “local contacts disposed on ... the slit structures”

Toyama does not expressly disclose *local contacts* (“source connection via structures 91”) *disposed on the slit structures* (“laterally-elongated contact via structures 76”) in the context of the Second Modification, likely because of where Toyama takes the cross section of Fig. 49. Lee ¶ 129.

However, a POSITA would have understood the Second Modification to include *local contacts disposed on the slit structures* (“source connection via structures 91”). Lee ¶ 130. As §IX.A.5IX.A.5 explains, “structures 76” are source contacts. Thus, “structures 76” interconnect an upper-level connection to the source regions in the substrate, and thus must include a local contact to function as an

channel structures. Petitioner notes, however, that the red boxes drawn around the *channel structures* in the earlier-filed Petition are larger than they are here, such that in the prior Petition, each box encompassed not just a “memory stack structure 55,” but arguably other structures (e.g., “pedestal channel portion 11,” the *epitaxial layer*, and “drain region 63,” the *etch stop plug*). This overinclusive annotation was of no moment in the prior case because the challenged claims there did not recite *an etch stop plug* or *an epitaxial layer*. The boundaries of the box drawn here make clear that the *channel structures* include “memory stack structures 55” but not “pedestal channel portions 11” or “drain regions 63.”

interconnect. Indeed, in describing the Second Modification, Toyama notes that “[t]he metal interconnect structures can include ... source connection line structures (not shown).” Toyama, [0342]. As expressly described in the first exemplary structure, “source connection line structures 101 ... contact the source connection via structures 91 to provide electrically conductive paths for biasing the source region 61 through the laterally-elongated contact via structures 76.” *Id.*, [0250]; §X.A.5 (Second Ground, limitation [8.D]). A POSITA would have understood that the Second Modification, which expressly includes “source connection line structures,” “source region 61,” and “laterally elongated contact via structure 76,” would also include “source connection via structures.”

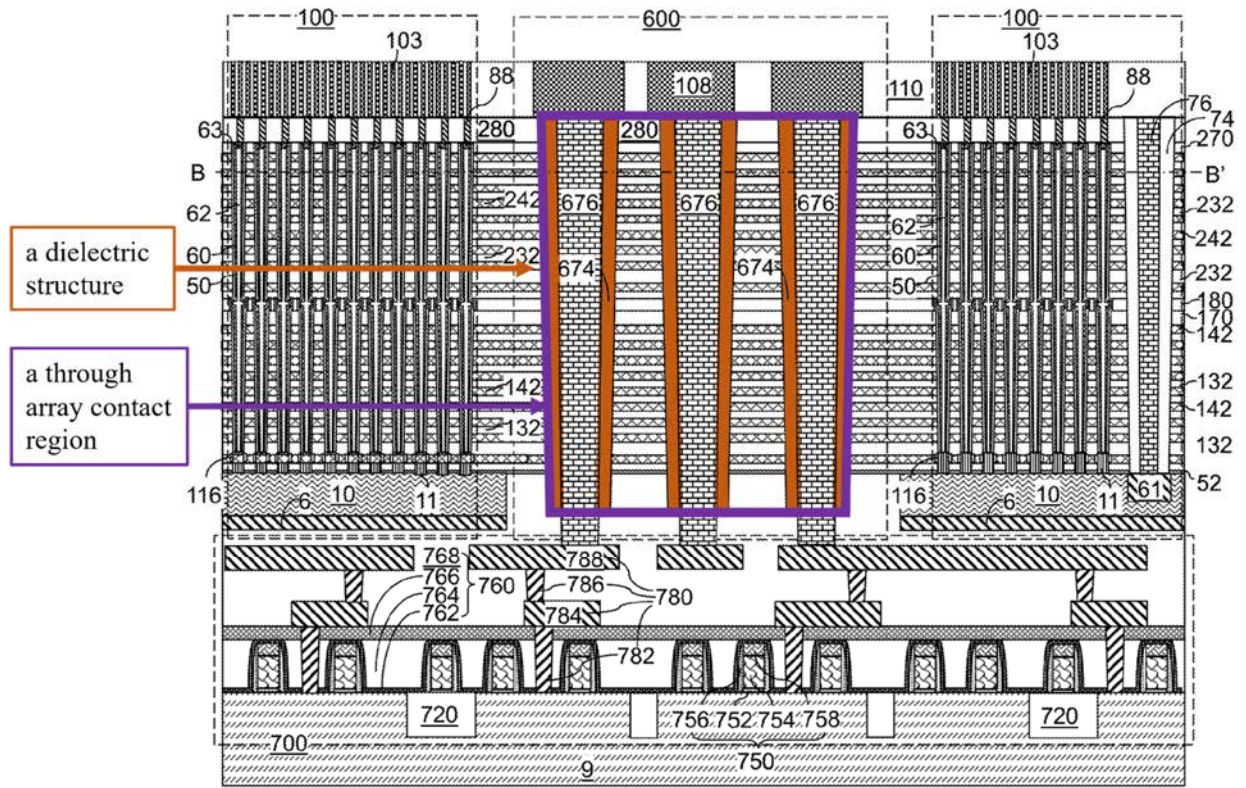
At the very least, a POSITA would have found the use of *local contacts disposed on the slit structures* (“source connection via structures 91”) obvious. Lee ¶ 131. Toyama explains that “laterally-elongated contact via structures 76” serve as source lines for “source region 61.” Toyama, [0382]. And a POSITA would have understood that in order for “via structures 76” to serve their purpose, they need to connect to a higher-level source connection. Lee ¶ 131. Given that other of Toyama’s embodiments expressly disclose the use of “source connection via structures 91” to serve this purpose, a POSITA would have been motivated to implement “source connection via structures 91” in the Second Modification so the structures 76 may server their function and would have had a reasonable expectation

of success in doing so, because Toyama already discloses how to implement such contacts. *Id.*

8. [8.G]

a. [8.G.i]

As “[i]n some embodiments” of the 806 Patent, Toyama’s “dielectric structure ... defines the boundaries, the shape, and the size of [Toyama’s] TAC region.” Ex. 1001, 10:26-28. The Second Modification’s *through array contact (TAC) region* (part of “through-memory-level via region 600”), shown below, is defined by the boundaries of its *dielectric structure* (“insulating liners 674”):



Toyama, Fig. 49, [0334]; Lee ¶ 135. Toyama also depicts its *through array contact (TAC) region* (part of “through-memory-level region 600”) in a top view:

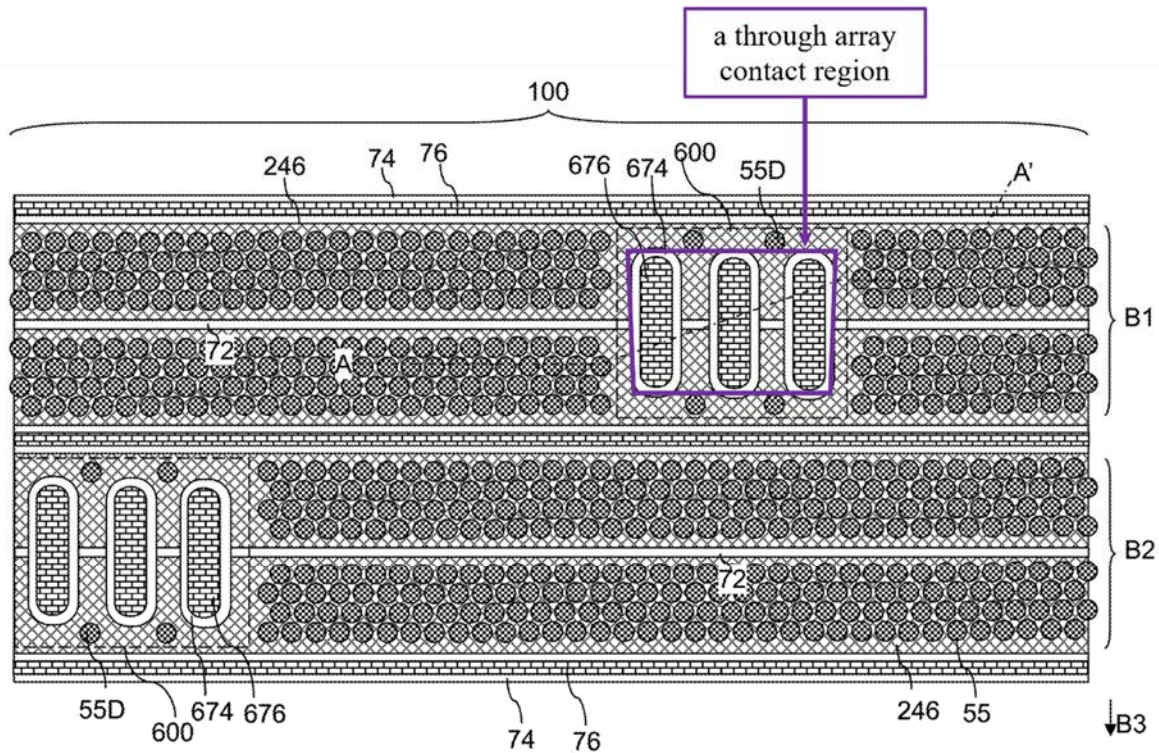


FIG. 48B

Toyama, Fig. 48B. As the Petition explains below, Toyama’s *through array contact (TAC) region* (part of “through-memory-level region 600”) *comprises a plurality of through array contacts (TACs)* (“through-memory-level via structures 676”).
 §IX.A.8.c (limitation [8.G.iii]).

b. [8.G.ii]

As discussed above, Toyama discloses *a through array contact (TAC) region* (part of “through-memory-level via region 600”). §IX.A.8.a. And, as discussed above for limitation [8.C], Toyama discloses *first and second channel regions* (first and second parts of “memory array region 100”). §IX.A.4.

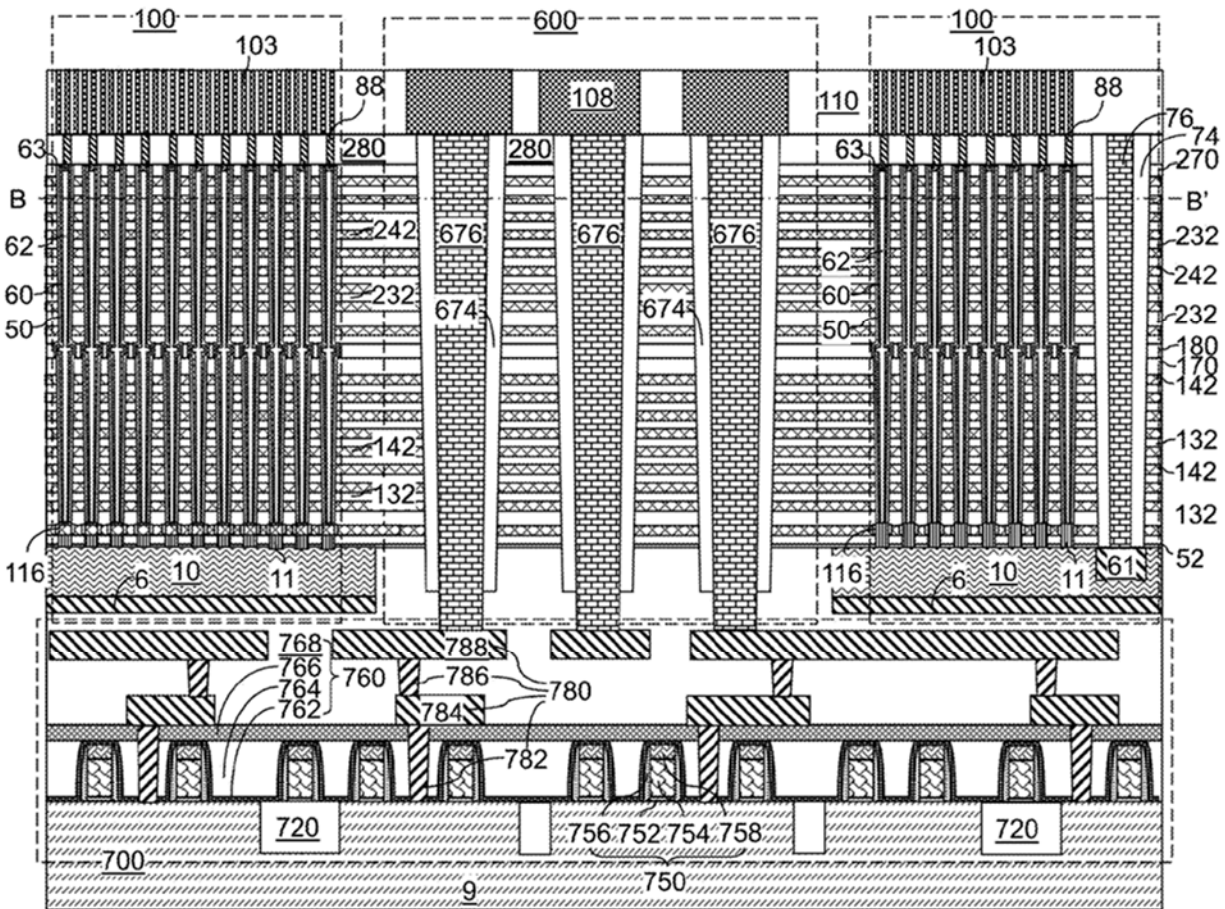


FIG. 49

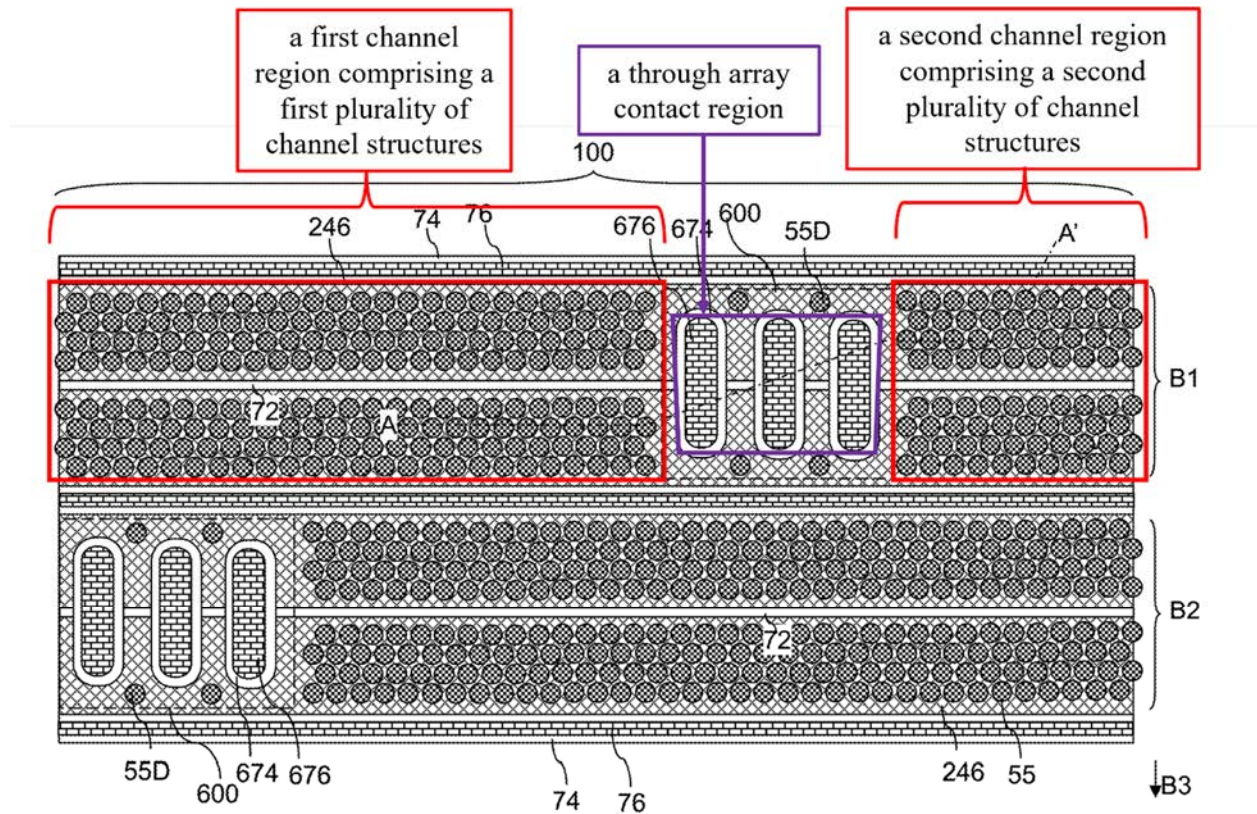


FIG. 48B

Toyama, Figs. 49, 48B. Toyama notes that the “through-memory-level via region ... is located ... between two groups of memory stack structures 55 located in [a] block.” *Id.*, [0378]. Thus, Toyama teaches that *the through array contact (TAC) region* (part of “through-memory-level via region 600”) is *formed between the first and second channel regions* (first and second parts of “memory array region 100”).

Lee ¶ 136.

c. [8.G.iii]

In Toyama’s Second Modification, “through-memory-level via structures 676” are *through array contacts*. Toyama discloses that *the TAC region* (part of

“through-memory-level via region 600”) *comprises a plurality of through array contacts (TACs)* (“through-memory-level via structures 676”) ¹¹ *extending vertically through the dielectric structure* (“insulating liners 674”):

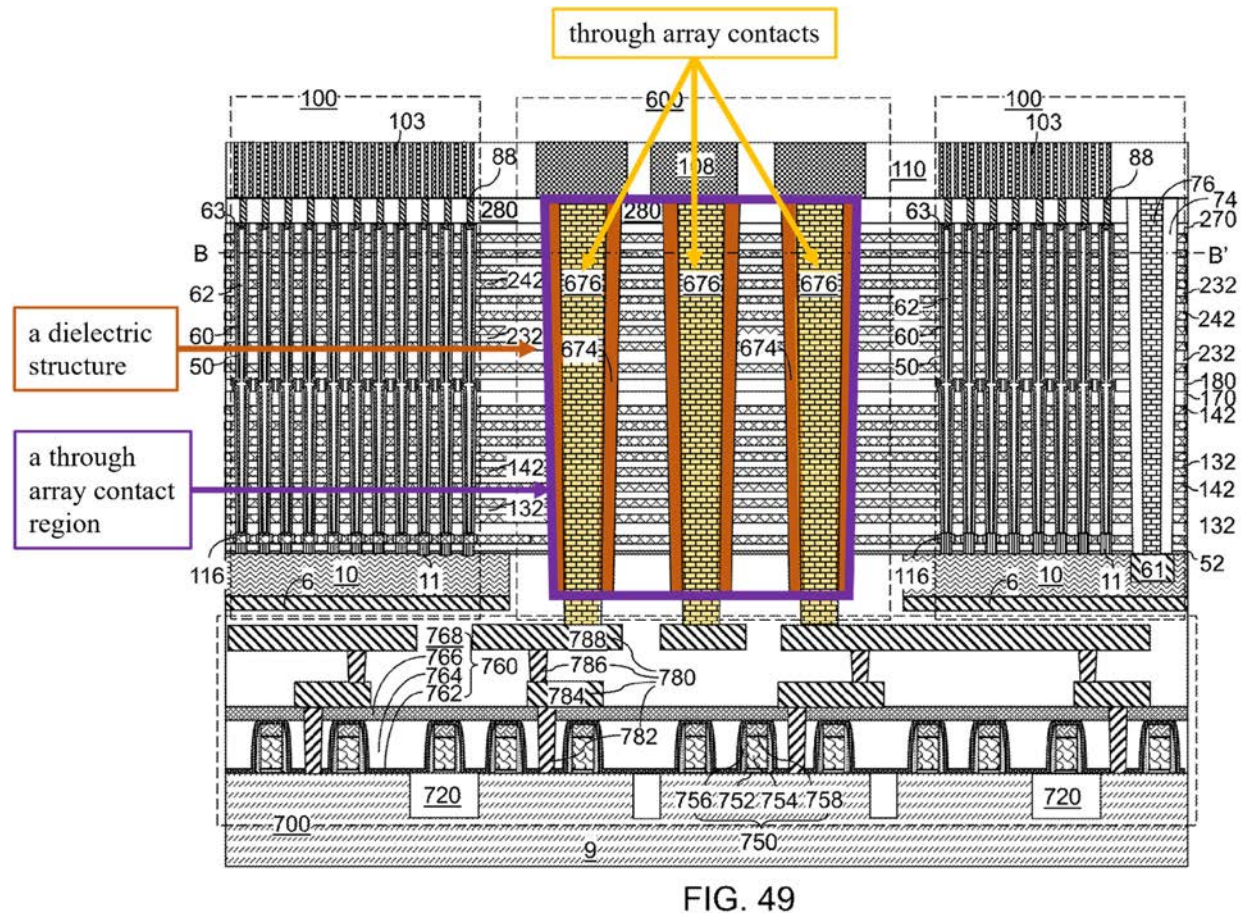


FIG. 49

Toyama, Fig. 49; [0341]-[0342]; §§IX.A.3, IX.A.8.a ; Lee ¶¶ 133-134. Just as water travels *through* a hose or a pipe extends *through* a wall, each of Toyama’s “through-

¹¹ Like Toyama’s “structures 676,” the 806 Patent’s “through array contacts” are composed of a “conductor material[.]” Ex. 1001, 11:14-15.

memory-level via structures 676” extends *through* “insulating liners 674.”¹²

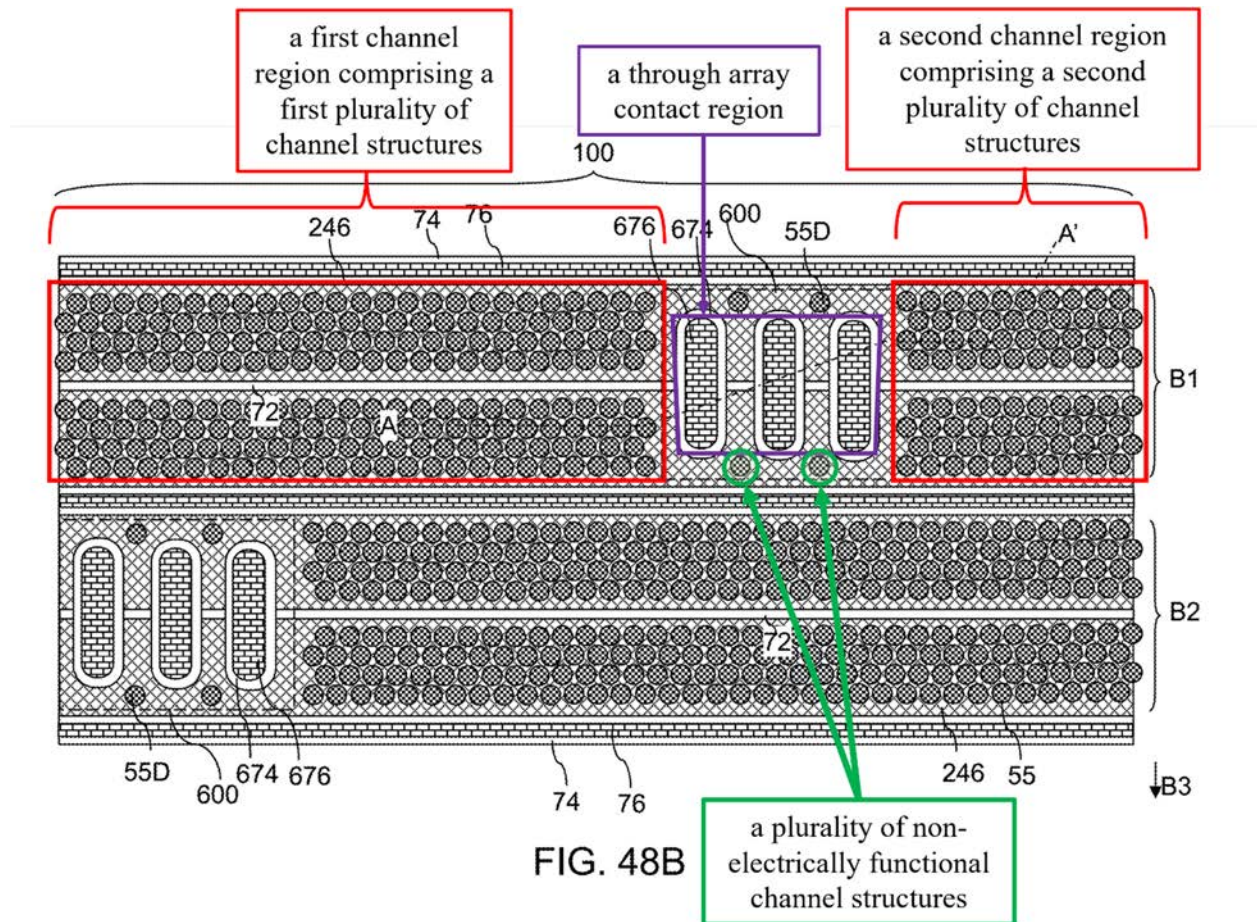
9. [8.H]

As Fig. 48B shows below, Toyama discloses *a plurality of non-electrically functional channel structures* (“dummy memory stack structures 55D”) *surrounding*¹³ *the TAC region* (part of “through-memory-level via region 600”) *and*

¹² As explained above, the claim term *a dielectric structure* is properly understood to include one *or more* dielectric structures. §IX.3.a. Accordingly, even if dielectric liners 674 are not considered to be a “structure” (which they are), the claim nonetheless encompasses embodiments in which each *through array contact* extends vertically through a different *dielectric structure*. *ABS Glob., Inc. v. Cytonome/ST, LLC*, 84 F.4th 1034, 1040 (Fed. Cir. 2023) (“The reference-back ‘the’ language takes its meaning from the meaning of the antecedent, so if ‘a sample stream’ has a plural-allowing meaning, so does the reference-back ‘the sample stream’ phrase.”).

¹³ The plain meaning of “surrounding” does not necessarily require full encirclement. For example, “[a]n isthmus is a thin strip of land surrounded by water on two sides, which connects two larger landmasses.” Ex. 1022. The same is true in the context of 3D NAND. Indeed, the 806 Patent appears to contemplate that if a first element borders a second element on two sides, the second element is

between the first and second channel regions (first and second parts of “memory array region 100”):



Toyama, Fig. 48B; Lee ¶¶ 137-140. Indeed, the 806 Patent describes embodiments, like Toyama’s Fig. 48B, in which the “dummy (e.g., non-electrically functional) channel structures” are above and below the TAC region. Ex. 1001, 6:47-54 (with reference to Fig. 1B, dummy channel structures are formed in NAND string regions

“surrounded by” the first element. Ex. 1001, 10:29-31 (describing the dielectric structure 232 in Fig. 1B as “surrounded by” the alternating stack 210).

110, which are above and below TAC region 120); *id.*, 7:1-10 (with reference to Fig. 1C, dummy channel structures are formed in staircase regions 140, which are above and below TAC region 120).

Even if Patent Owner argues that the claim requires *non-electrically functional channel structures* on four sides of *the TAC region* (it does not), a POSITA would have understood Toyama to disclose doing so. Lee ¶ 139. Toyama explains that “[d]ummy memory stack structures 55D can be provided at the periphery of the through-memory-level via regions 600.” Toyama, [0333]. As illustrated in Fig. 48B, above, the “periphery” of “region 600” encircles Toyama’s *TAC region*. Thus, a POSITA would have understood that Toyama’s “dummy memory stack structures 55D” to encircle Toyama’s *TAC region* (part of “through-memory-level via region 600”).

To the extent that the claim requires that “dummy memory stack structures 55D” border four sides of the *TAC region* (it does not), and Toyama does not expressly contemplate doing so (it does), a POSITA would nevertheless have found that obvious. Lee ¶ 140. As noted above, Toyama’s Fig. 48B expressly depicts placing *non-electrically functional channel structures* (“dummy memory stack structures 55D”) above and below *the TAC region* (part of “through-memory-level via region 600”). A POSITA would have found it desirable to form “dummy memory stack structures 55D” for structural support in regions (e.g., the left and

right periphery of the “through-memory-level via region”) where functional “memory stack structures are not formed at a sufficiently high density.” Toyama, [0182]. Placing dummy stack structures on all sides of the TAC region is therefore nothing “more than the predictable use of prior art elements [i.e., dummy memory stack structures 55D] according to their established functions [i.e., structural support on the periphery of the TAC region].” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007).

B. Claim 10

1. [10.Pre] “The 3D memory device of claim 8, further comprising:”

See §IX.A.1.

2. [10.A] “a substrate;”

As an initial matter, the ’806 patent defines a *substrate* as “a material onto which subsequent material layers are added, or otherwise ‘disposed.’” Ex. 1001, 4:47-49.

Toyama discloses a *substrate*, namely, “planar semiconductor material layer 10.” Toyama, [0170], [0335]. The figure below shows that subsequent material layers are added onto layer 10:

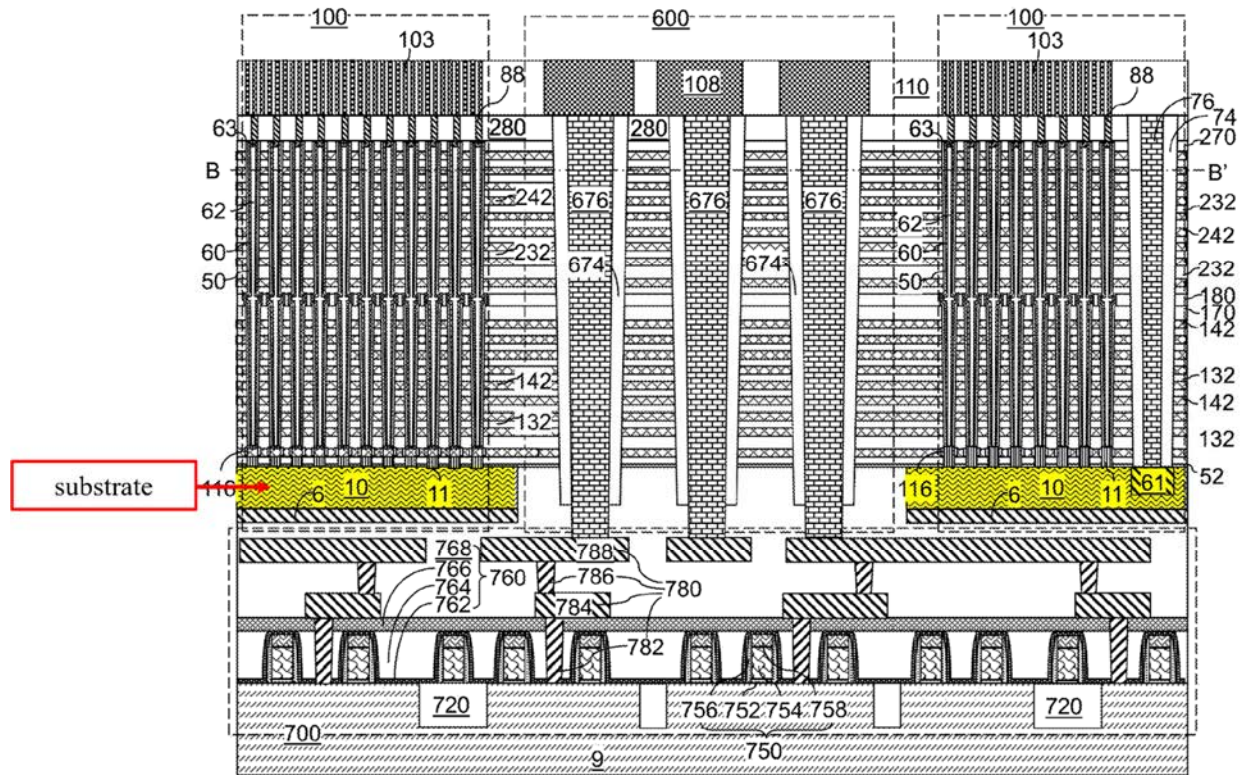


FIG. 49

Toyama, Fig. 49; Lee ¶¶ 141-143.

3. [10.B] “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and”

Recall that Toyama discloses *local contacts* (“drain contact via structures 88”) *disposed on* (in contact with or extending above) *the channel structures* (“memory stack structures 55”). See §IX.A.7.a. *[I]nterposed between each local contact of the local contacts and each channel structure of the first and second channel structures* are conductive, polysilicon drains, 63, which are *etch stop plugs*:

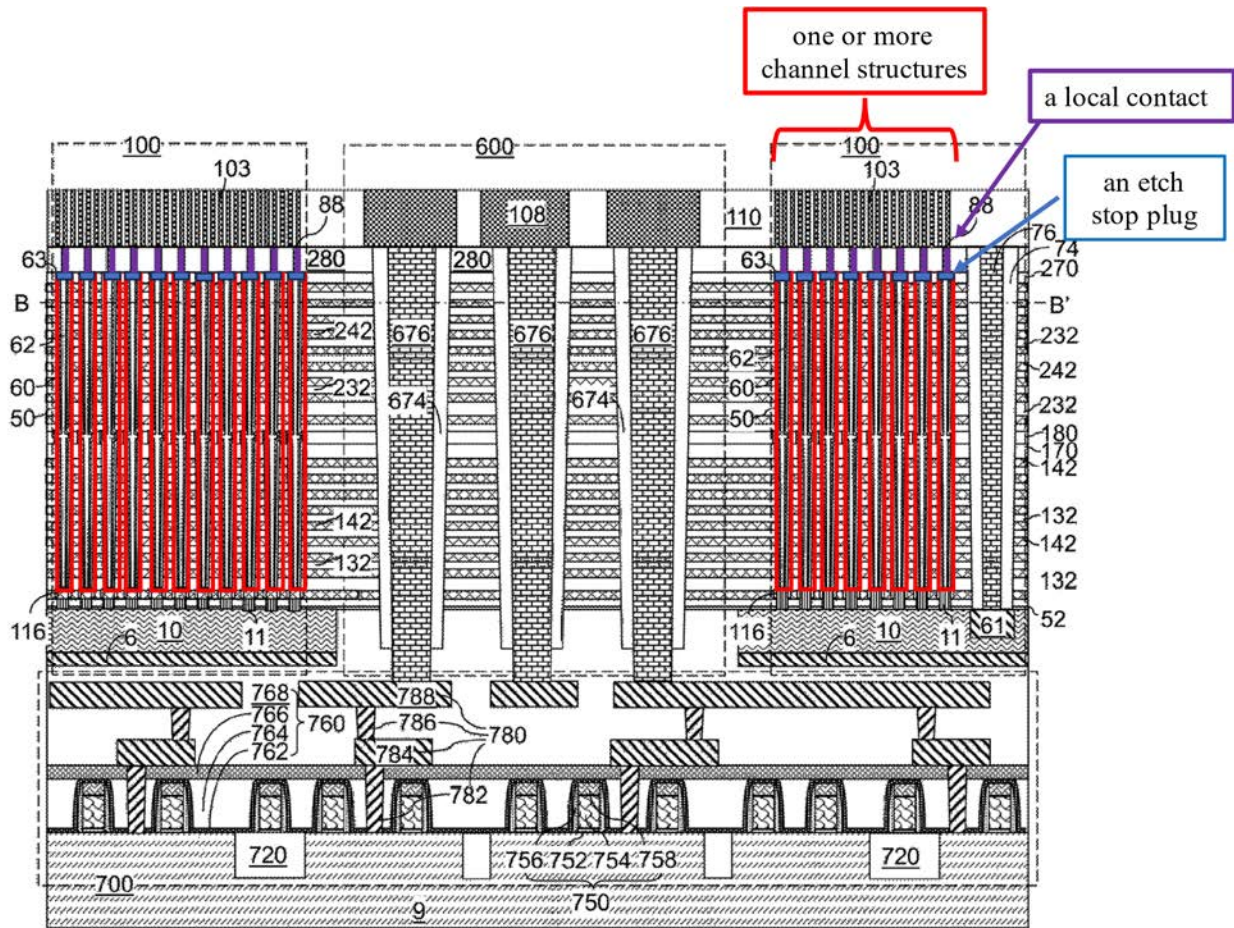


FIG. 49

Toyama, Figure 49; Lee ¶¶ 144-152.

Although Toyama does not expressly describe each of “drain regions 63” as being an “etch stop plug,” a POSITA would have understood, or at least found obvious, that “drain regions 63” are plugs that serve the purpose of stopping an etch. §V.A.3 (etching background); Lee ¶¶ 145.

Each of Toyama’s “drain regions 63” is a *plug*. As Toyama explains, “[a] doped semiconductor material ... can be deposited over the dielectric cores 62 and within the cavities in the memory openings to form drain regions 63. The doped

semiconductor material can be, for example, doped polysilicon. Excess portions of the deposited semiconductor material can be removed from above the top of the second insulating tier cap layer 270 ... to form the drain regions 63.” Toyama, [0209]. Because Toyama’s “drain regions 63” fill the cavities in the memory openings, they are plugs. Ex. 1021, 3 (Merriam-Webster’s definition of “plug” as “a piece used to fill a hole”); Lee ¶¶ 146.

As Figure 49 shows above, Toyama forms *local contacts* (“drain contact via structures 88”) *on* (in contact with or extending above) *the one or more channel structures* (“memory stack structures 55”) by etching through dielectric (i.e., the dielectric layer 280), and then filling the etched opening with a conductor. Toyama further explains that “drain contact via structures 88” “may be formed employing a respective set of patterning processes and fill processes.” Toyama, [0241]-[0242], [0342]; Lee ¶ 148.

A POSITA would have understood from Toyama’s disclosure that part of the “patterning” process includes a step of etching an opening in dielectric layer 280. *Id.*; §V.A.3 (etching background); Lee ¶¶ 149-150. And a POSITA would have understood from Toyama’s disclosure—or at least found obvious—that the dielectric layer 280 would be formed of a dielectric material such as silicon oxide.

Toyama, [0212], [0238].¹⁴ Thus, Toyama contemplates—or, at the very least, a POSITA would have found obvious—employing a dielectric-selective etchant (e.g., an etchant selective to silicon oxide) to form the opening that is ultimately filled by “drain contact via structures 88.” §V.A.3; Lee ¶ 149. Such selective etches were textbook material and routine to implement.

A POSITA would have understood that without “drain regions 63,” the etch to form “drain contact via structures 88” may risk damaging elements of “memory stack structures 55.” That is because “memory stack structures 55” may include dielectric elements (e.g., “blocking dielectric layer 51”) that are formed of the same

¹⁴ Toyama does not expressly state that “dielectric layer 280” is made of silicon oxide, but a POSITA would have understood Toyama to contemplate doing so. At the very least, forming layer 280 of silicon oxide would have been obvious to a POSITA. Toyama expressly notes that “dielectric layer 180” could be made of “a dielectric material such as silicon oxide.” Toyama, [0183]. Toyama further states that that “second contact level dielectric layer 282 includes a dielectric material such as silicon oxide.” *Id.*, [0238]. A POSITA would thus have understood from Toyama’s disclosure that “dielectric layer 280” would—or, at least, obviously could—similarly be made of silicon oxide, which was a well-known dielectric material with recognized advantages. Lee ¶ 148 n.5.

materials (e.g., silicon oxide) as the dielectric through which contact via 88 is formed. Toyama, [0204]. Thus, if the etchant that is used to etch through the dielectric layer were to contact the memory stack structures, it may damage the memory stack structures. §V.A.3; Lee ¶ 151.

That undesirable result is prevented by “drain regions 63,” which are between the opening that is filled to form “drain contact via structures 88” and the “memory stack structures 55.” Toyama, [0209], [0241]. “Drain regions 63” function as an etch stop because they are made of a material like doped polysilicon, which a POSITA would have understood would **not** react significantly with the etchant used to selectively etch the dielectric. §V.A.3 (e.g., CF₄); Lee ¶ 152. Even if the etchant were to remove a portion of “drain regions 63,” the thickness of “regions 63” acts as a buffer of sorts, so that the etchant might partially etch and stop before inadvertently etching through to the memory elements. Lee ¶ 152. Thus, “drain regions 63” serve to protect the dielectric materials in the memory stack from the etching process used to form “drain contact via structures 88.” §V.A.3; Lee ¶ 152. In other words, because “drain regions 63” effectively stop the etch that ultimately forms the holes for “drain contact via structures 88,” each of “drain regions 63” is *an etch stop plug* that beneficially protects the channel structure. §V.A.3; Lee ¶ 152.

Indeed, Toyama’s “drain region 63” and the 806 Patent’s “etch stop plug 224” share similarities even beyond what is required by the claim. The 806 Patent’s “etch

stop plug 224,” like Toyama’s “drain region 63,” “acts as the drain of NAND string 204.” Ex. 1001, 9:52-53; Toyama, [0209]. The 806 Patent discloses forming “etch stop plug 224” out of polysilicon, just like Toyama’s “drain region 63.” 806 Patent, 16:2-5; Toyama, [0209]. The 806 Patent deposits “etch stop plug 224” and then levels it using chemical mechanical planarization (CMP) so that it is flush with a dielectric layer, just like Toyama’s “drain regions 63.” 806 Patent, 16:2-5; Toyama, [0209]. Just as the 806 Patent forms contacts (“NAND string contacts 236”) over the “etch stop plug 224,” so too does Toyama form contacts (“drain contact via structures 88”) over “drain regions 63.” 806 Patent, 17:53-57; Toyama, [0241]. And, as explained above, just as the 806 Patent’s “etch stop plug 224” prevents etching of dielectrics in the channel structure during formation of the contacts, so too do Toyama’s “drain regions 63.” §V.A.3. These similarities further confirm that Toyama’s “drain region 63” is an *etch stop plug*.

4. [10.C] “an epitaxial layer disposed between the substrate and the first or second channel structures.”

Toyama discloses and renders obvious *an epitaxial layer* (“pedestal channel structures 11”) *disposed between the semiconductor substrate* (“planar semiconductor material layer 10”) and *the first or second channel structures* (both the first and second, as the channels are in region 100, which includes both):

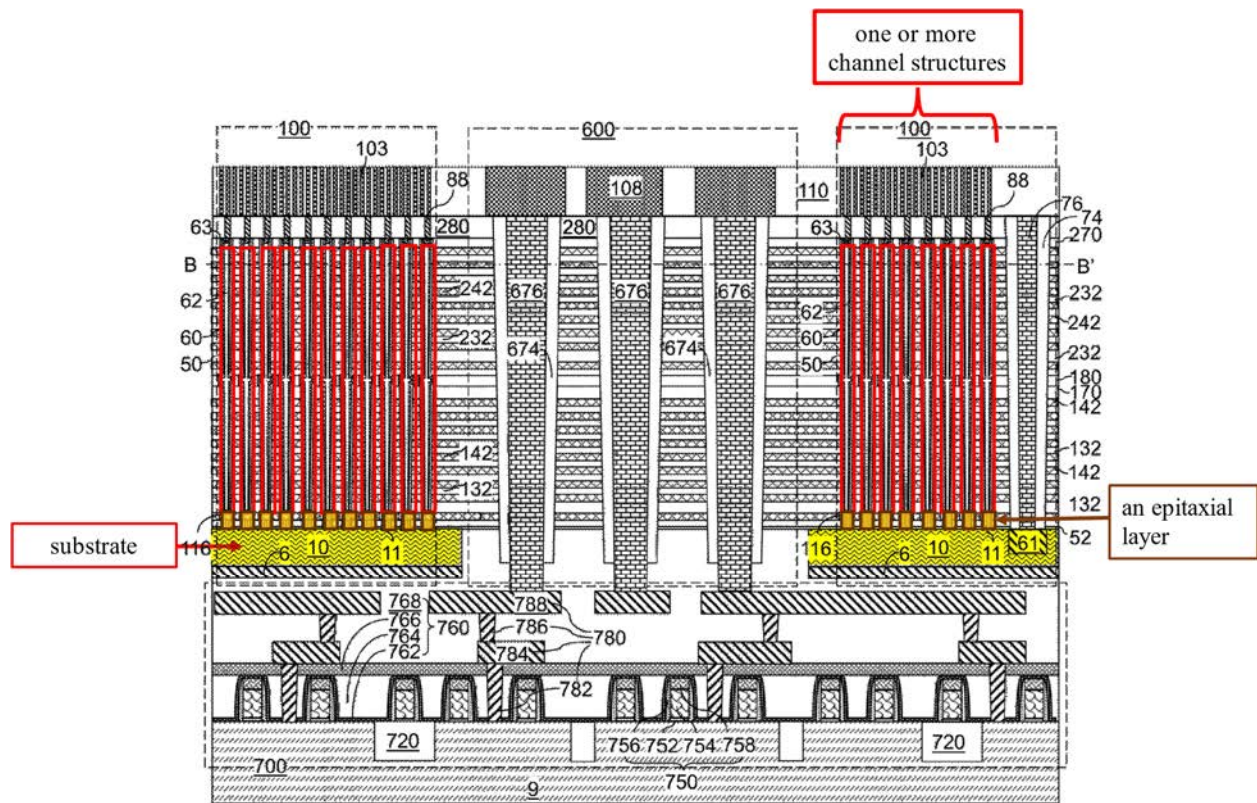


FIG. 49

Toyama, Figure 17A, [0208]; Lee ¶¶ 153-156.

Toyama refers to “pedestal channel portions 11” as “epitaxial channel portions 11,” confirming that these structures constitute *an epitaxial layer*. And a POSITA would have recognized that Toyama’s description of how “portions 11” are formed is consistent with an epitaxial process. Toyama, [0202] (“The selective semiconductor deposition *grows a semiconductor material*. ... During a selective semiconductor deposition process, a reactant (such as silane, dichlorosilane, trichlorosilane, disilane, etc.) can be flowed into a deposition chamber simultaneously with, or, alternatively with, an etchant (such as hydrogen chloride).”) (emphasis added); Section V.A.2; Lee ¶ 155.

At the very least, it would have been obvious to form “pedestal channel portions 11” (which a POSITA would have known to have the benefit of improving memory channel reliability) as an epitaxial layer (epitaxy being a known and desirable method of forming crystalline material). Lee ¶ 156.

X. GROUND 2: TOYAMA’S FIRST EXEMPLARY STRUCTURE IN VIEW OF THE KNOWLEDGE OF A POSITA

For the following reasons, Toyama’s first exemplary structure in view of the knowledge of a POSITA renders claim 10 obvious.

A. Claim 8:

1. [8.PRE]

To the extent that the preamble is limiting, Toyama discloses *a three-dimensional (3D) memory device*. Toyama, [0156] (“the present disclosure is directed to three-dimensional non-volatile memory devices”); Lee ¶ 158.

2. [8.A]

Toyama’s “alternating stack (132, 146, 232, 246)” is *an alternating conductor/dielectric layer stack*:

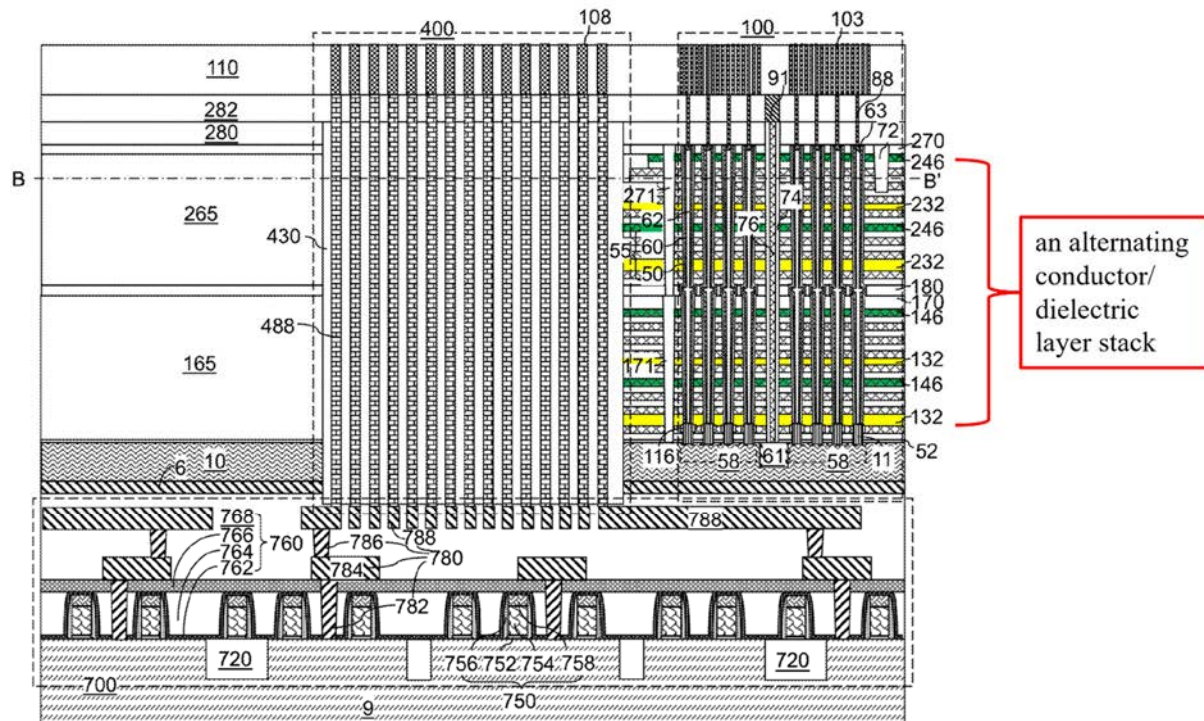


FIG. 17A

Toyama, Fig. 17A, [0172]; Lee ¶ 159. Toyama’s “alternating stack (132, 146, 232, 246)” is *an alternating conductor dielectric layer stack* for the reasons explained above with reference to Toyama’s Second Modification. §IX.A.2.

3. [8.B]

a. [8.B.i]

In Toyama's first exemplary structure, shown below, the upper part of "dielectric fill material portion 430" is a *dielectric structure*:

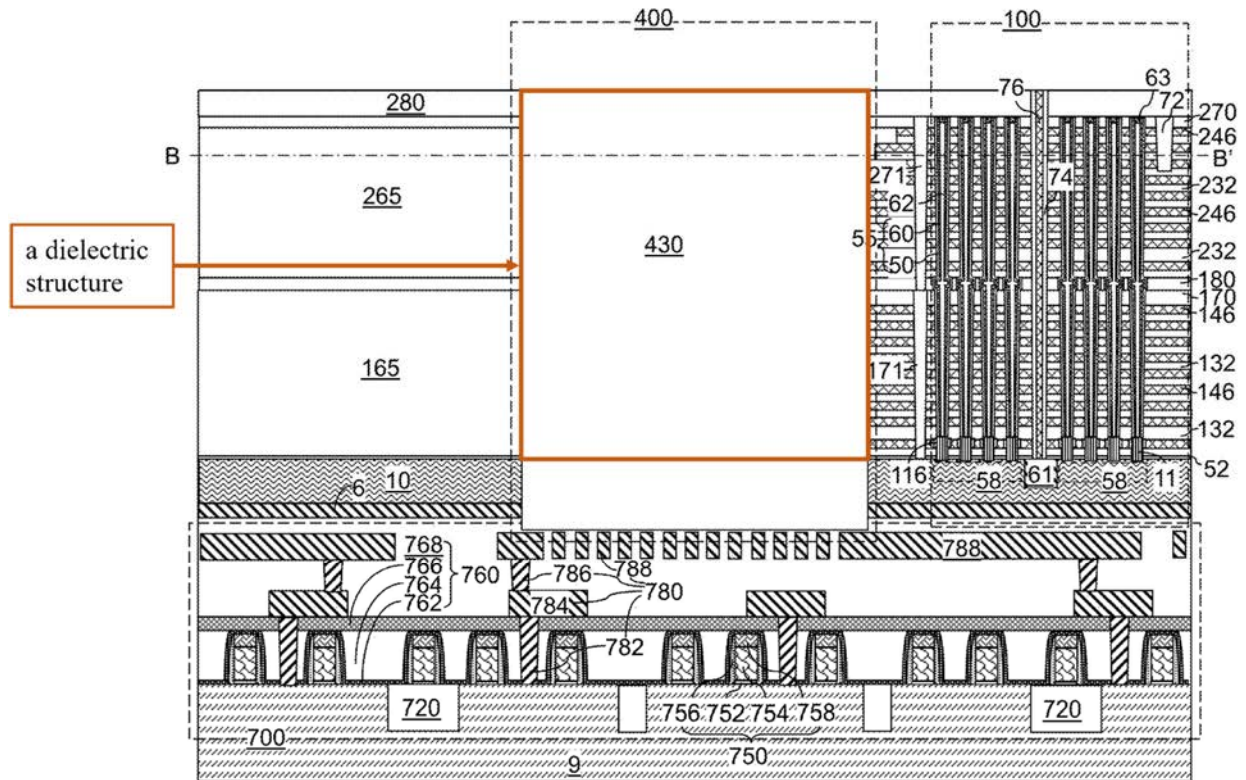
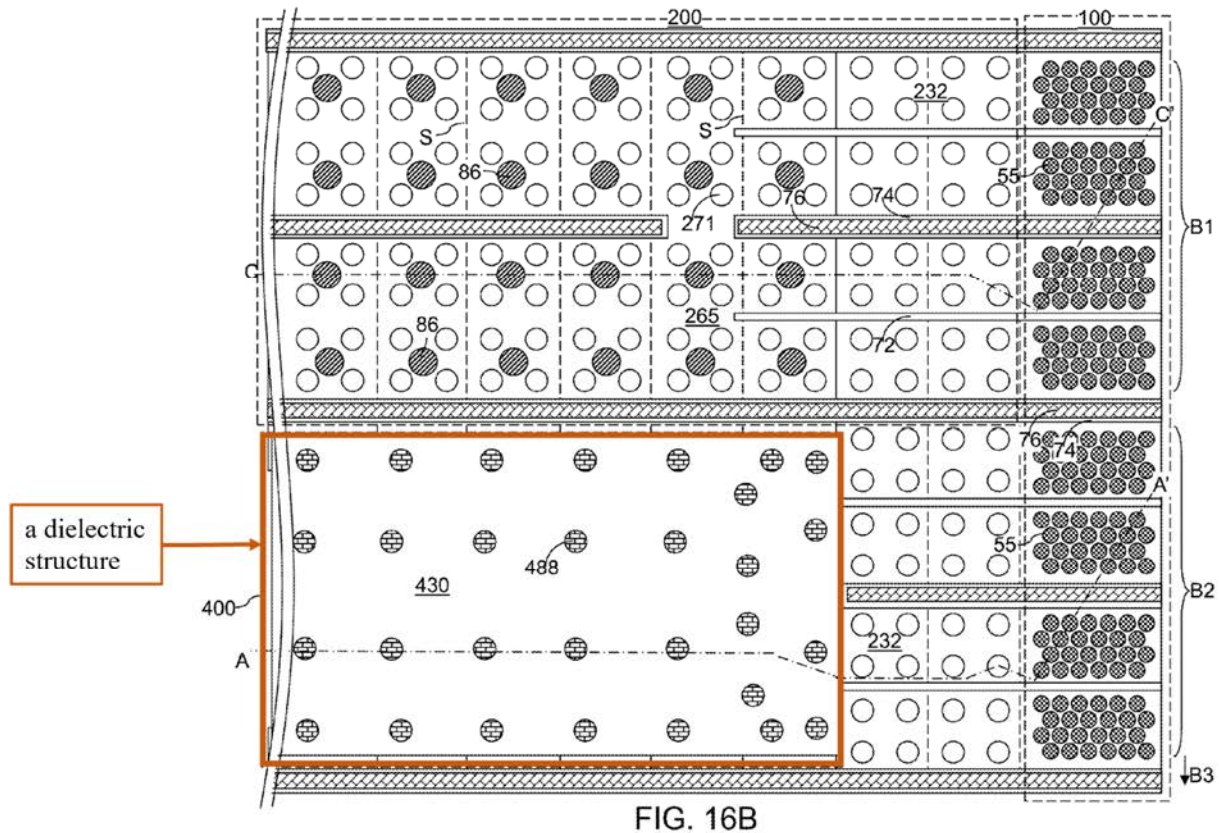


FIG. 15A

Toyama, Fig. 15A, [0216]; Lee ¶ 161. Toyama also provides a top view of the *dielectric structure* ("dielectric fill material portion 430"):



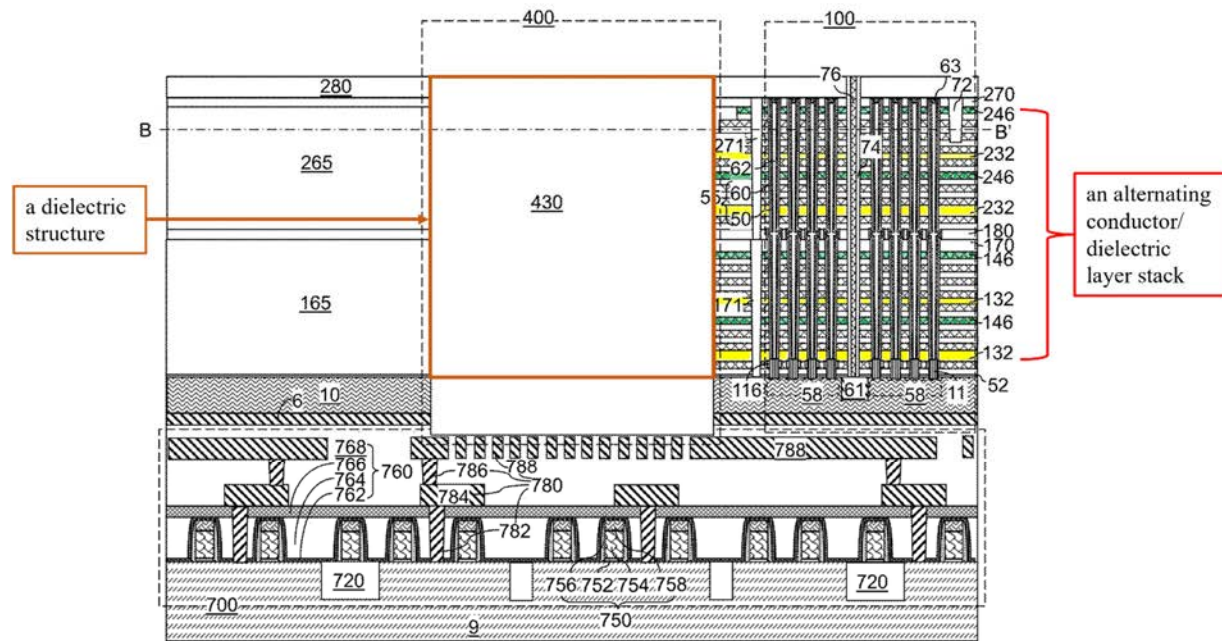
Id., Fig. 16B.

Toyama explains that “a dielectric fill material portion 430 is formed within each through-memory-level opening 769, for example, by deposition of a dielectric fill material.” Toyama, [0216]. The upper part of “dielectric fill material portion 430” is *a dielectric structure* because it is composed of “a dielectric fill material.”

Id.; Lee ¶ 161.

b. [8.B.ii]

As noted immediately above, the upper part of Toyama’s “dielectric fill material portion 430” is *a dielectric structure*. And, as noted above with reference to limitation [8.A], Toyama’s “alternating stack (132, 146, 232, 246)” is *the*



Toyama, Fig. 15A; Lee ¶¶ 162-166.

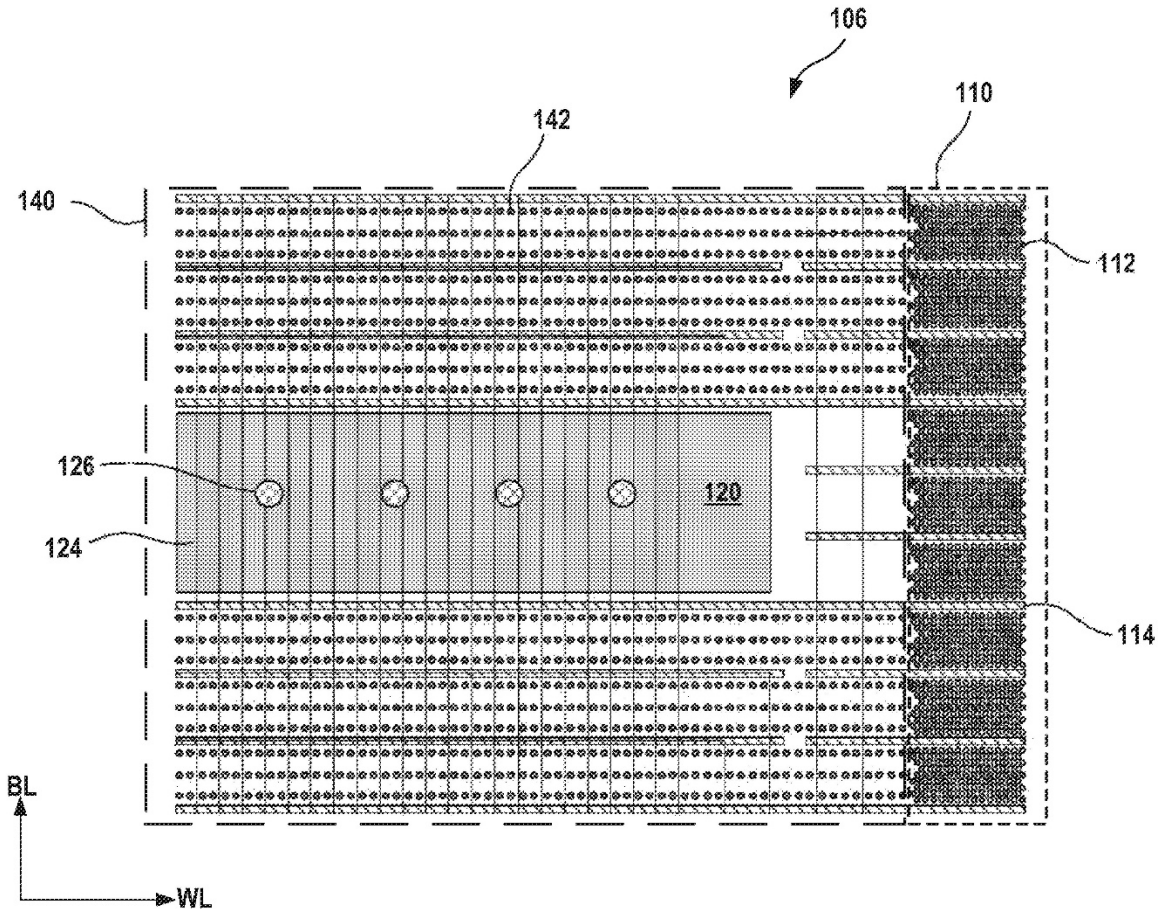


FIG. 1C

Ex. 1001, Fig. 1C. Similarly, in Toyama’s first exemplary structure, the *dielectric structure* (“dielectric fill material portion 430”) borders three regions including an alternating conductor/dielectric layer stack: above and below by staircase regions (“word line contact via region 200”) and to the right-hand side by a NAND string region (“memory array region 100”):

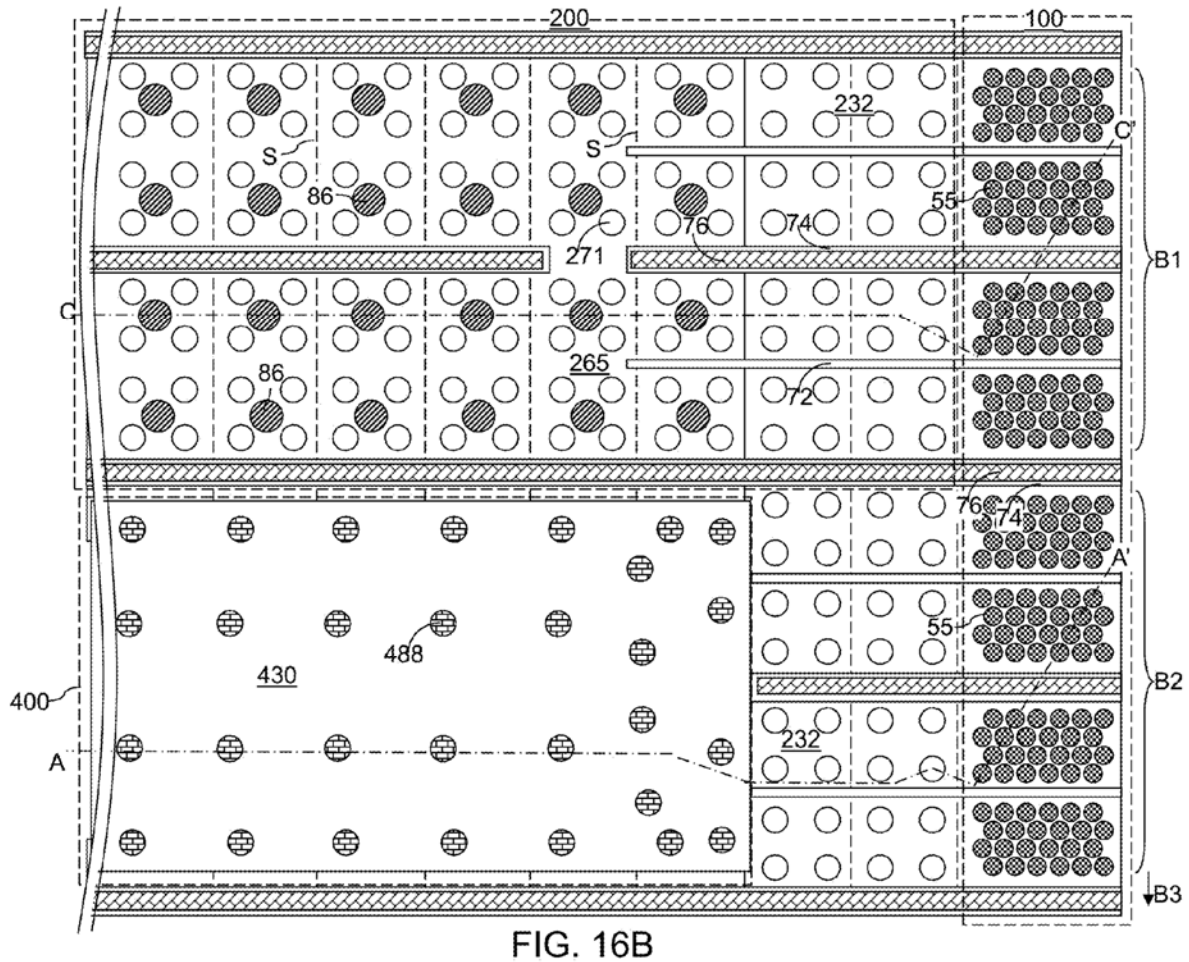


FIG. 16B

Toyama, Fig. 16B.

What's more, Toyama and the 806 Patent form the *dielectric structure* ("dielectric fill material portion 430" and "dielectric layer 702," respectively) in the same way. Lee ¶¶ 163-166. Toyama forms "dielectric fill material portion 430" like the 806 Patent forms "dielectric layer 702," by removing part of the dielectric stack before replacing the dielectric stack's sacrificial layers with electrically conductive layers. Specifically, the 806 Patent removes part of "dielectric stack 400" to form "opening 600":

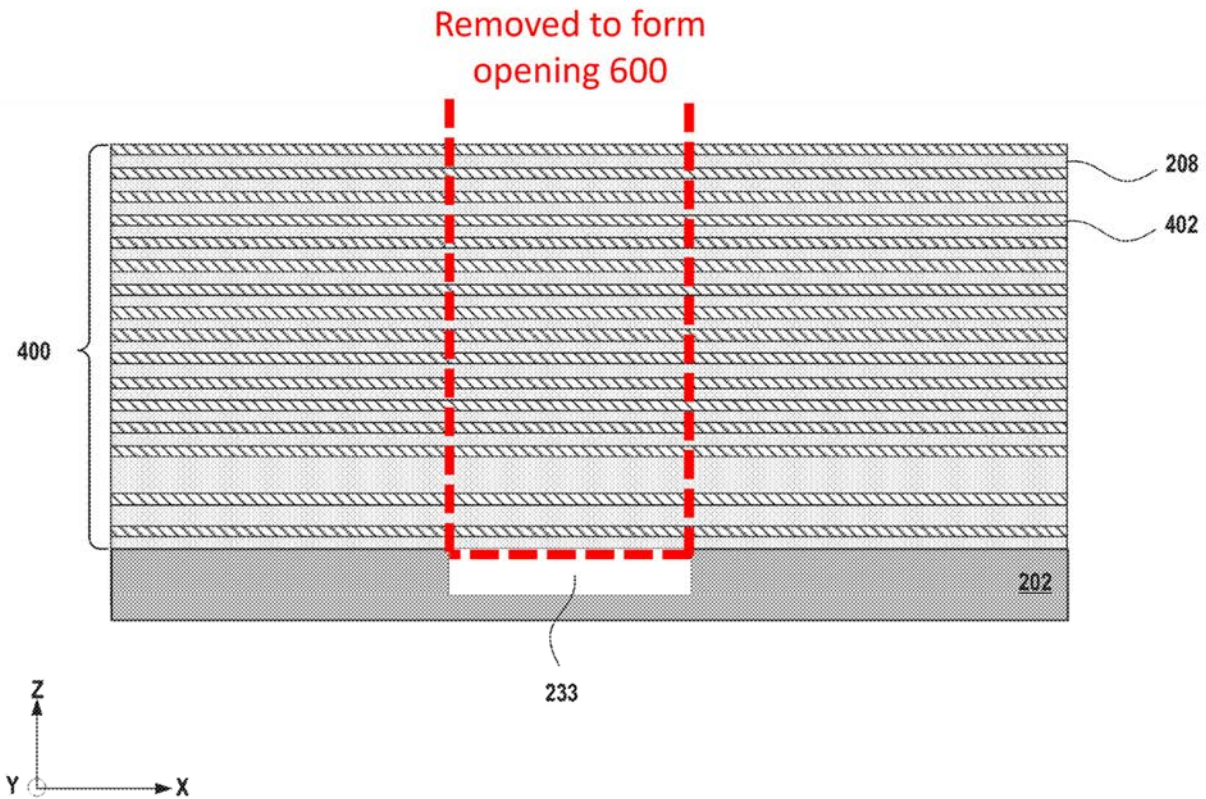


FIG. 4

Ex. 1001, Fig. 6, 15:16-17. The 806 Patent then fills “opening 600” with the dielectric structure (“dielectric layer 702”). *Id.*, 15:46-48.

Similarly, Toyama’s first exemplary structure removes “insulating layers” 132, 232 and “sacrificial material layers” 142, 242 to form “opening 769”:

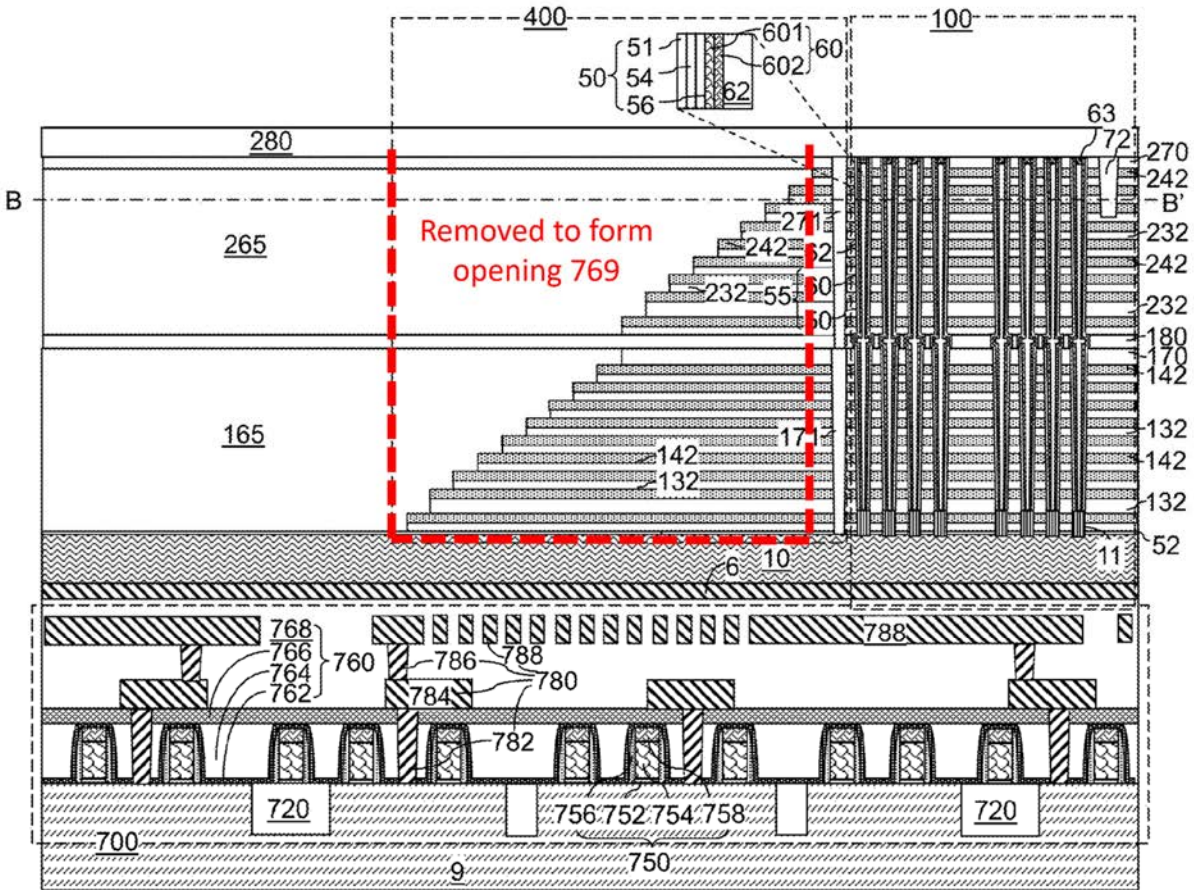
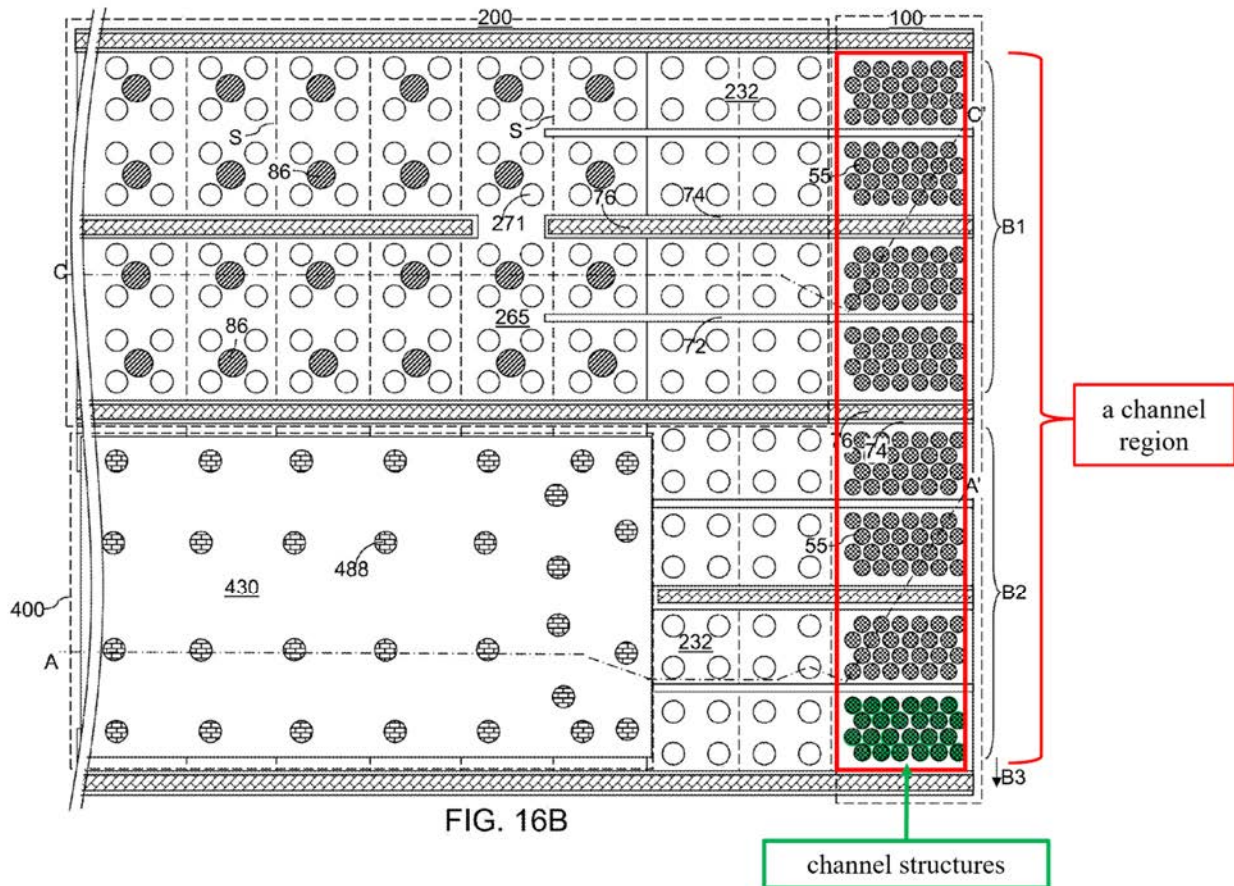


FIG. 10A

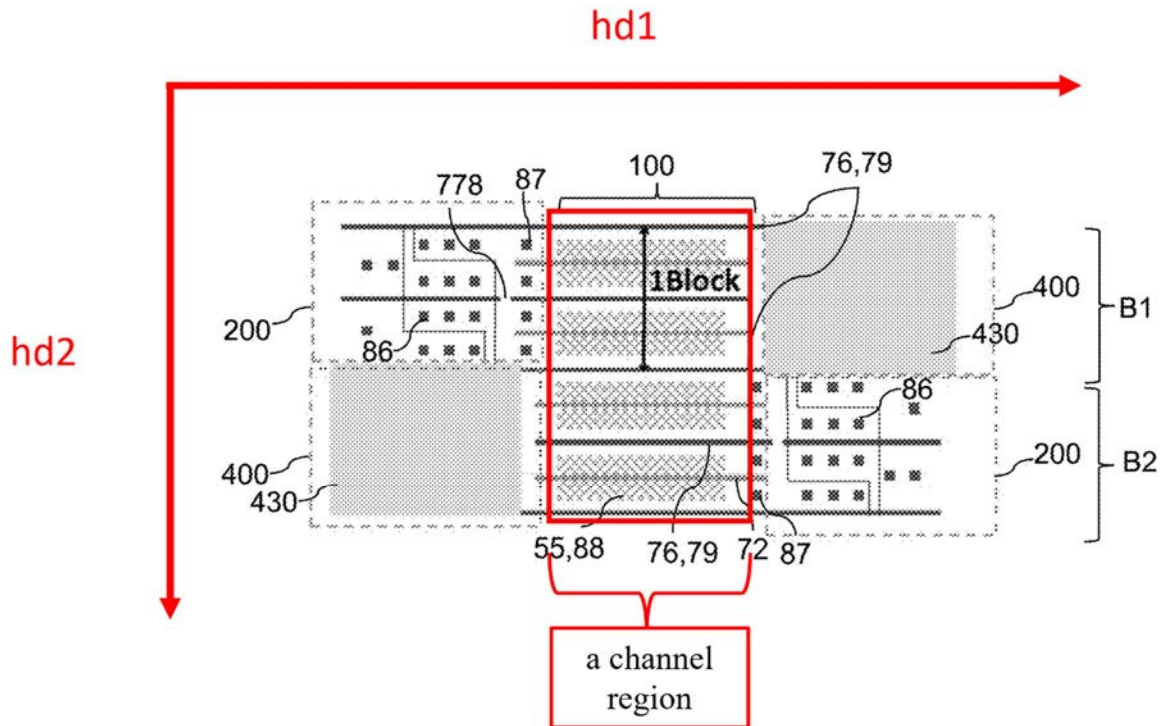
Toyama, Fig. 10A, [0173], [0190], [0213]. Toyama then fills “opening 769” with the dielectric structure (“dielectric fill material portion 430”).

Toyama’s first exemplary structure thus discloses this limitation.



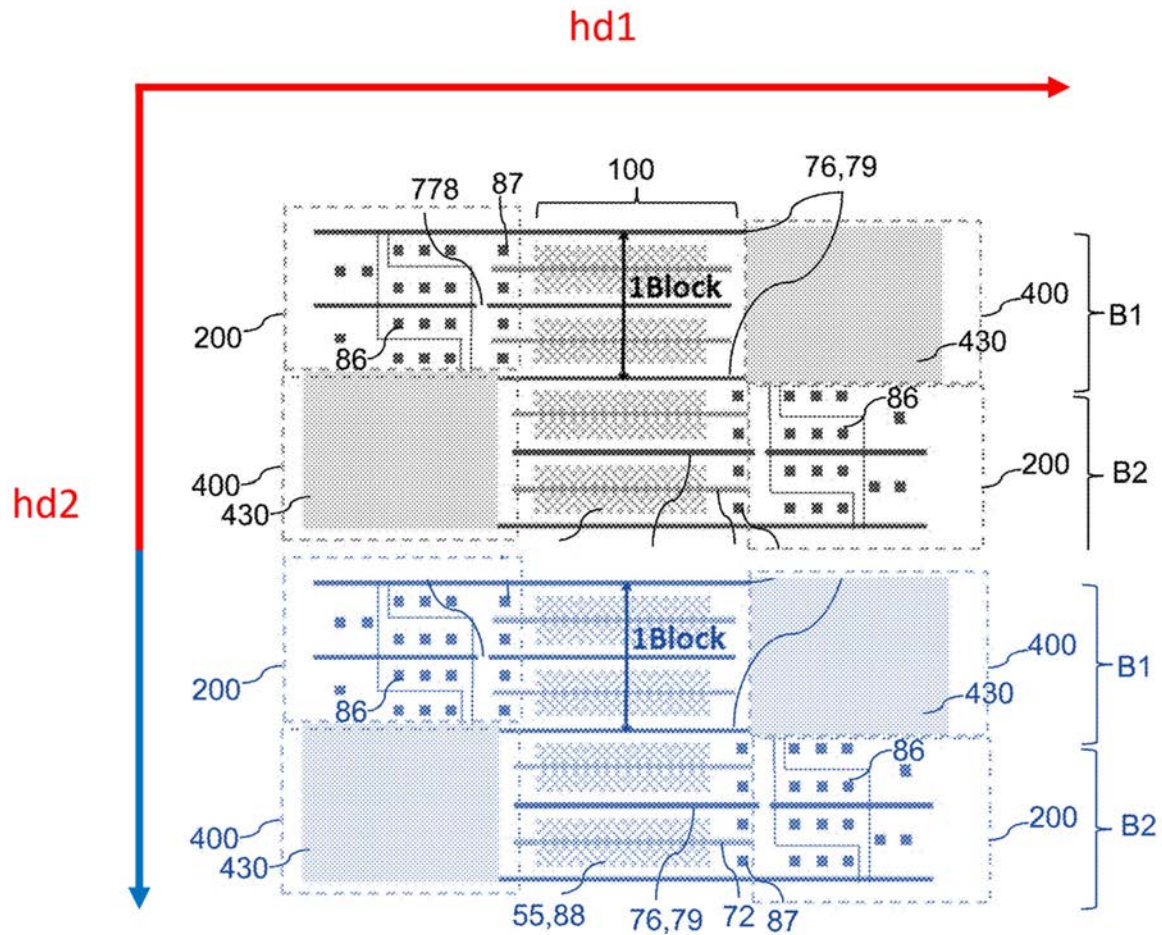
Toyama, Fig. 16B. Toyama’s *channel structures* (“memory stack structures 55”) form *a channel region* (part of “memory array region 100”). Lee ¶ 168.

Toyama’s Fig. 17E, which Toyama expressly teaches for use with its first exemplary structure, also shows a *channel region* (“memory array region 100”). Toyama, [0049].



Id., Fig. 17E; Lee ¶ 168.

Toyama expressly contemplates that the layout shown in Fig. 17E repeats in the hd2 (i.e., up-down) direction, as depicted in the below modified figure:

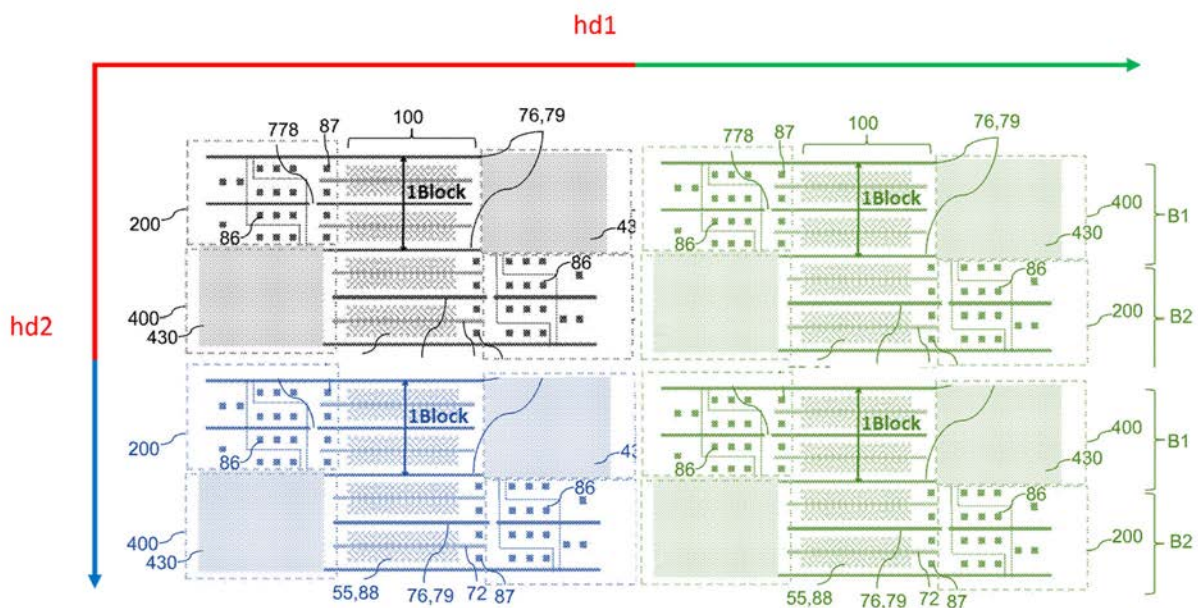


Toyama, Fig. 17E (modified); *id.*, [0220] (“[A] neighboring pair of an odd-numbered block and an even-numbered block (such as B1 and B2) can be periodically repeated along the second horizontal direction.”); Lee ¶ 169.

Toyama does not expressly repeat the layout shown in Fig. 17E in the **hd1** (i.e., left-right) direction. However, as explained below, a POSITA would have found it obvious to do so. Lee ¶ 170.

- a. **A POSITA would have found it obvious to implement multiple planes of Toyama's first exemplary structure in the hd1 direction.**

A POSITA would have found it obvious to implement Toyama's first exemplary structure in a 3D memory device with multiple *planes*. Thus, a POSITA would have found it obvious to repeat the layout shown in Fig. 17E in the hd1 *and* hd2 directions, as shown in the modified figure below:



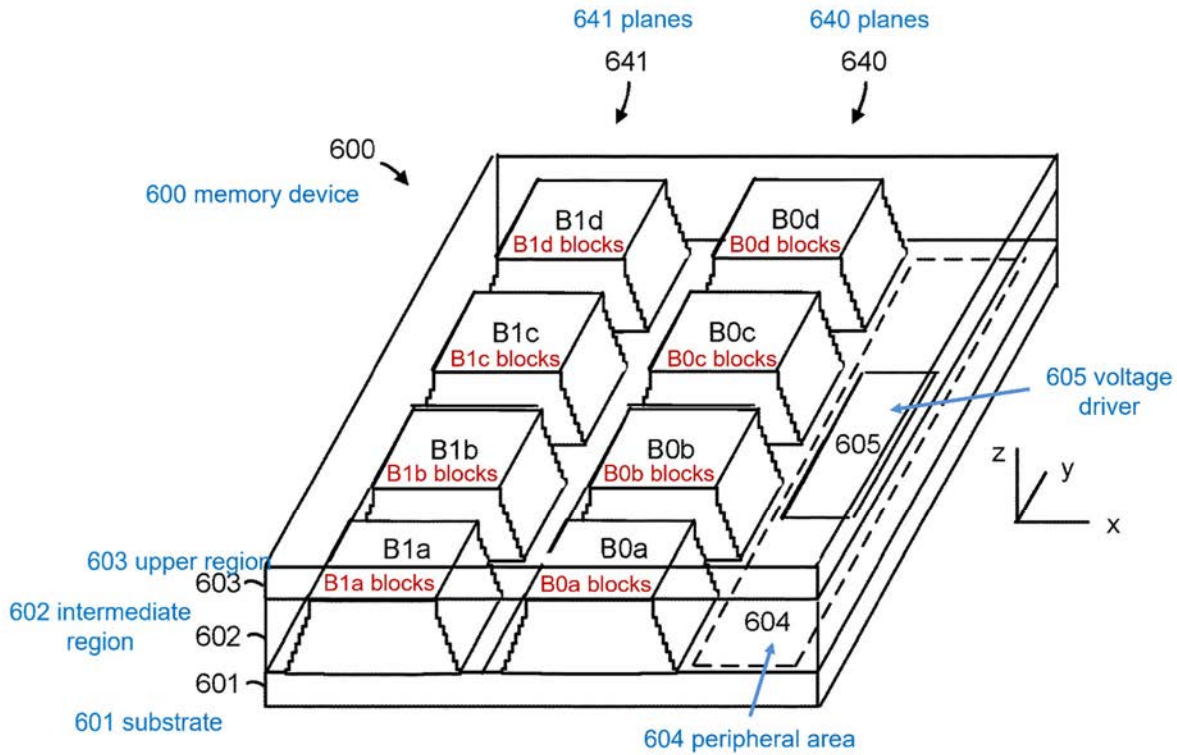
Toyama, Fig. 17E (modified); Lee ¶ 171.

- i. **A POSITA would have known how to implement multiple flash memory planes in a NAND flash memory device, and the benefits of doing so.**

Long before the 2018 priority date of the 806 Patent, a POSITA would have known to implement a flash memory device with multiple *planes*, each including a distinct memory array region and staircase structure. As a POSITA would have

known: “A NAND flash storage device or storage system, e.g., a solid-state disk (SSD) and flash cards, may be associated with multiple chips. Each chip is composed of one or more sub-chips or dies. Each sub-chip might have multiple planes. Each plane is organized in terms of blocks that are the basic unit for erase operations.” Ex. 1023, 247.

A POSITA would have known how to implement a flash memory device with multiple planes by placing the planes beside each other. Lee ¶¶ 172-178. For example, the below figure illustrates a flash memory device with two planes and four blocks:



Ex. 1024, 13:37-44 (“Two planes 640 and 641 of blocks of memory cells (storage elements) are formed on a substrate 601. ... The plane 640 includes blocks B0a, B0b, B0c and B0d. The plane 641 includes blocks B1a, B1b, B1c and B1d.”).

A POSITA’s knowledge of flash memory devices with multiple side-by-side planes is further demonstrated by the numerous such devices that had already been built before the priority date. The below figures illustrate numerous such devices:

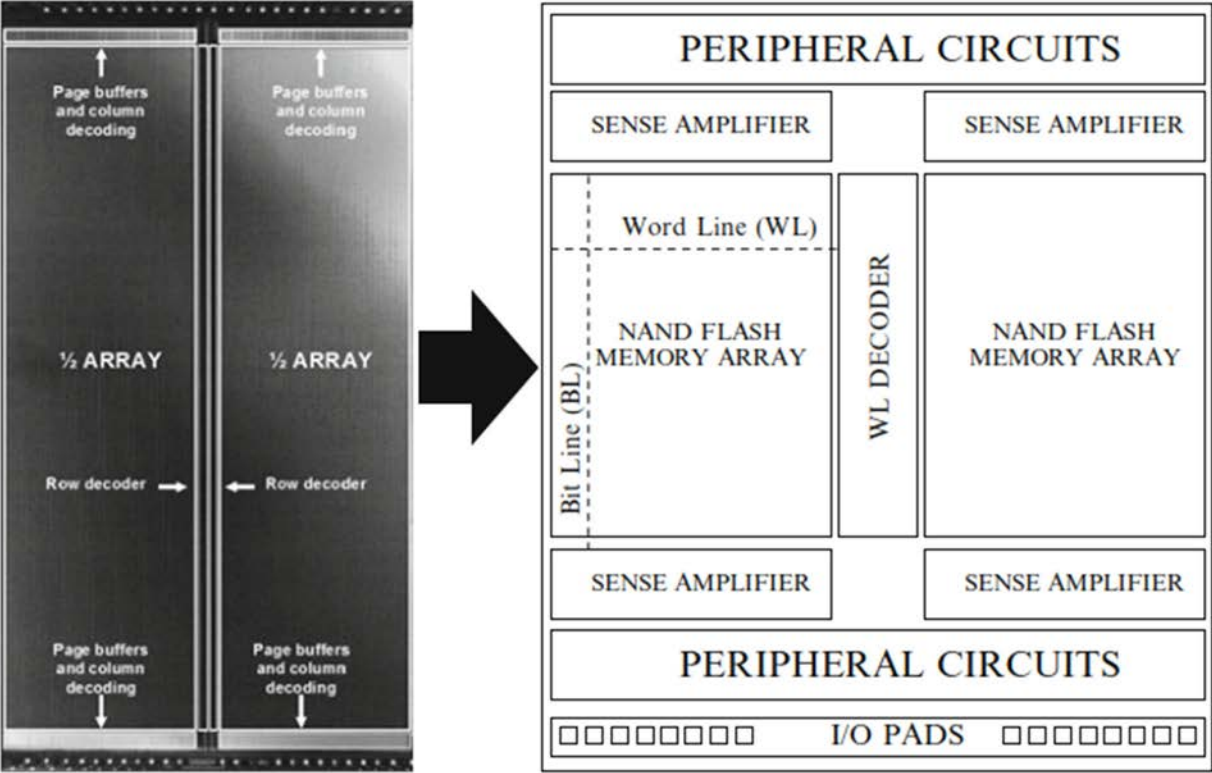


Fig. 6.1 A typical NAND Flash floorplan [1]

Ex. 1023, 144 (the “[flash] memory array has been split into two independent planes”).

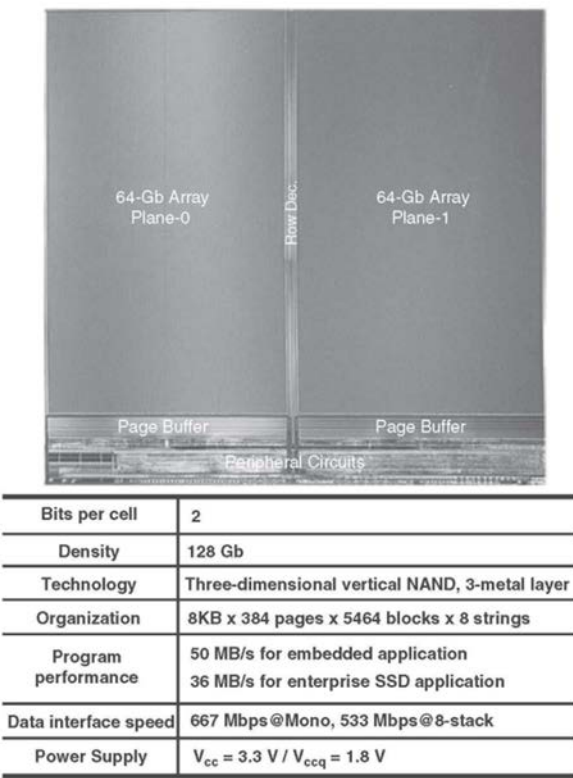


FIGURE 7.35 Die micrograph and main feature of 128-Gb 2-bit/cell 3D V-NAND flash. Die size is 133 mm².

Ex. 1014, 313-314 (“This memory chip has 24 stacked WL layers and consists of two planes each containing 64-Gb arrays (2732 of 3-MB blocks with 8-KB pages).”).

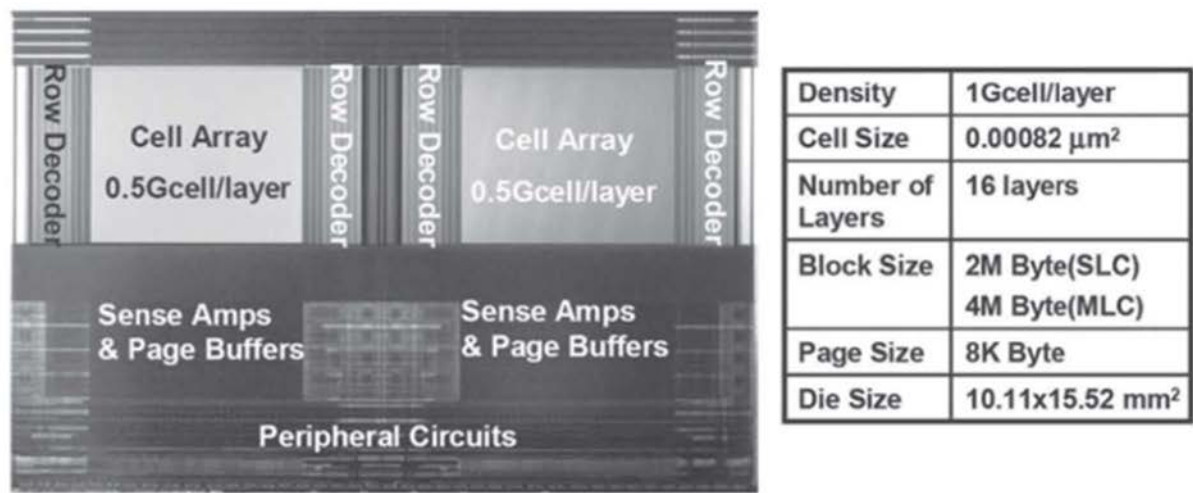


FIGURE 7.26 Image of 16-Gb pipe-shaped BiCS test chip.

Id., 308.

By the priority date, a POSITA understood numerous benefits of a multi-plane flash memory device. Lee ¶¶ 176. A POSITA would have known, for example, that “[o]n multi-plane device, it is possible to issue a read command on multiple planes simultaneously,” as illustrated below (see “double-plane page read”):

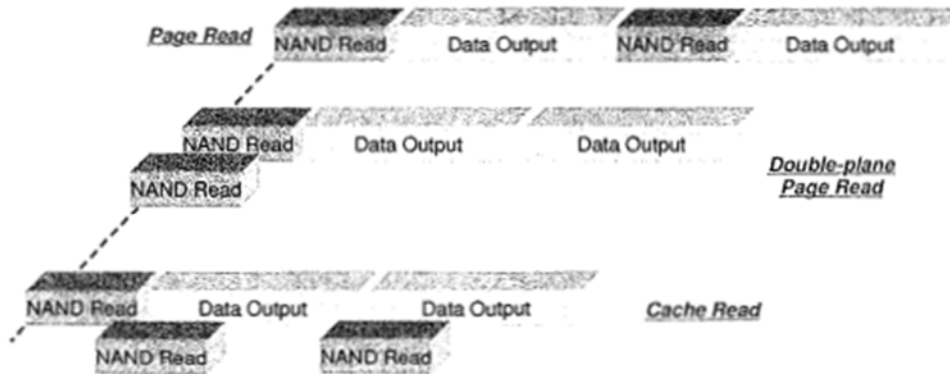


Fig. 2.19. Performance comparison among Read, Double-plane Read and Cache Read

Ex. 1025, 42.

Using multiple planes also can improve the throughput of program operations, that is, writing data to the flash memory, as illustrated below (see “double-plane overlapped program”):

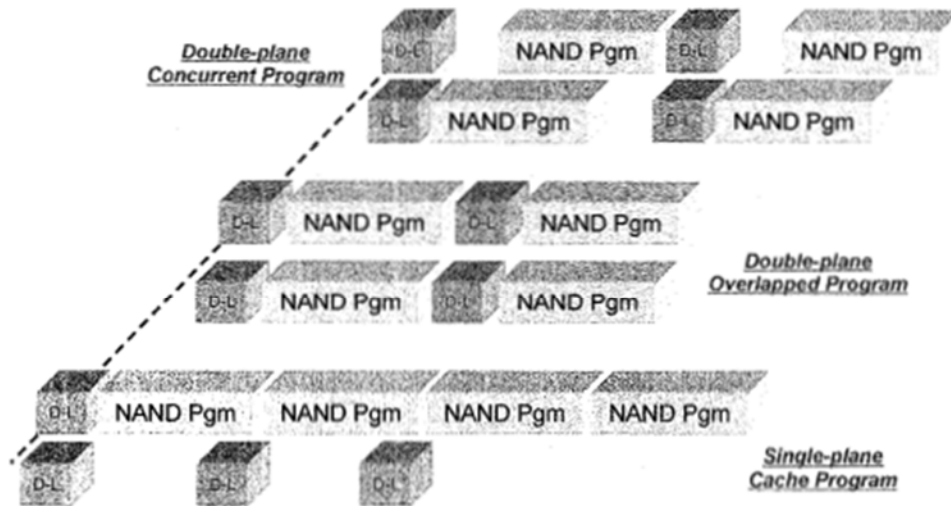


Fig. 2.24. Performance comparison among Cache Program, Overlapped Double Plane program and Concurrent Double Plane Program

Ex. 1025, 44-45. Thus, “double-plane program [is] used to increase write throughput.” *Id.*

A POSITA therefore would have known that “having two internal planes working interleaved” would “improve the performance of NAND based systems.” Ex. 1025, 171. Indeed, a POSITA would have known that “[t]his solution [was] quite common because the power issues related to this kind of solution are still manageable inside the chip and optimized versus two separate NAND devices active at the same time.” *Id.*

- ii. **A POSITA would have had a motivation to implement, and would have had a reasonable expectation of success in implementing, multiple planes of Toyama's first exemplary structure in the hd1 direction.**

Toyama does not expressly state that the layout shown in Fig. 17E, below, repeats in the hd1 (left-right) direction, but a POSITA would have been motivated to modify Toyama in this manner. That's because a POSITA would have been motivated to implement multiple planes of Toyama's first exemplary structure. As explained above, a POSITA would have known how to implement multiple planes in a flash memory device like Toyama's. §X.4.a.i. And, as explained above, a POSITA would have found it beneficial to implement multiple planes of Toyama's first exemplary structure (e.g., for improved performance). §X.4.a.i. An obvious technique for implementing multiple planes in a flash memory device is to repeat them laterally across the device, as in numerous prior art flash memory devices. §X.4.a.i. Indeed, although planes could theoretically be implemented in the hd2 (i.e., up-down direction), a POSITA would have found that less desirable because Toyama already contemplates using the hd2 direction to implement multiple blocks (within a single plane). Toyama, Fig. 17E, [0220]. And, although it would be theoretically possible to implement both blocks and planes in the hd2 direction, a POSITA would have recognized that this is less desirable than implementing planes in the hd1 direction. Lee ¶ 180. In short, a POSITA would have been motivated to

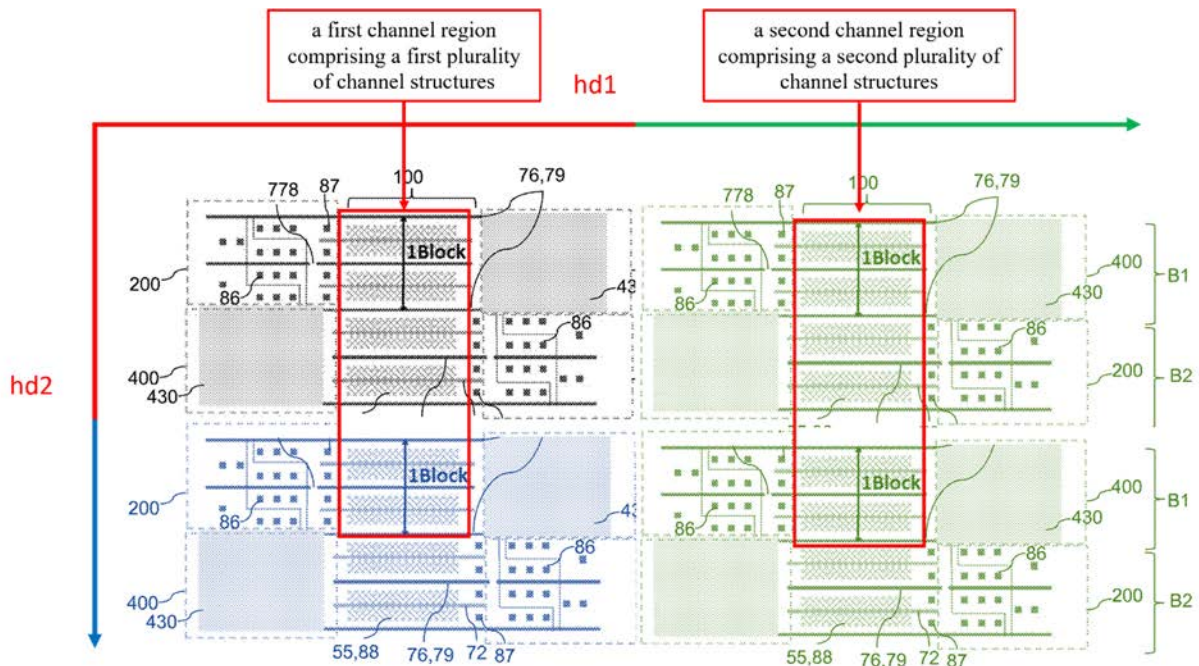
implement multiple planes of Toyama's first exemplary structure in the hd1 direction. *Id.*, ¶¶ 179-180.

A POSITA also would have had a reasonable expectation of success in implementing multiple planes of Toyama's first exemplary structure in the hd1 direction. Lee ¶ 181. As noted above, NAND flash memory devices with multiple planes existed for many years before the priority date of the 806 Patent. §X.A.4.a.i. Taking the layout shown in Toyama's Fig. 17E as the blueprint for a plane, and repeating that layout for each plane, would have been straightforward for a POSITA and a POSITA could have done so with predictable results.

Thus, the obviousness combination is nothing more than applying a known technique (implementing multiple planes of a NAND flash memory array) to a known device (Toyama's first exemplary structure) to yield predictable results (a NAND flash device with improved performance). Lee ¶ 182.

b. Modifying Toyama's first exemplary structure with a POSITA's knowledge of memory planes renders this limitation obvious

Implementing multiple planes of Toyama's first exemplary structure in the hd1 direction is shown in the modified figure below:



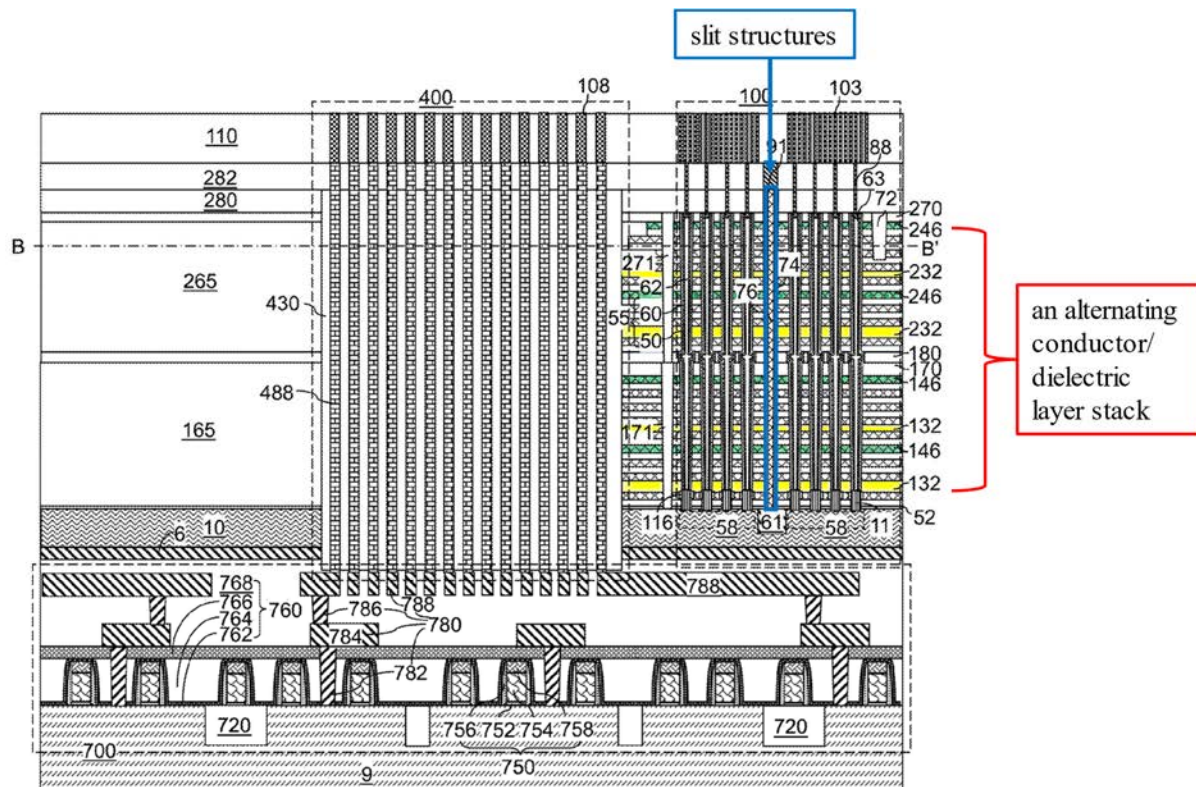
Toyama, Fig. 17E (modified). As the above figure indicates, the obviousness combination includes *first and second channel regions* (parts of the first and second “memory array regions 100”). Each of these *channel regions* comprise *a plurality of channel structures* (“memory stack structures 55”). Toyama, Fig. 16B.

Thus, Toyama renders obvious *first and second channel regions* (first and second parts of “memory array regions 100”) *comprising first and second pluralities of channel structures* (first and second pluralities of “memory stack structures 55”).

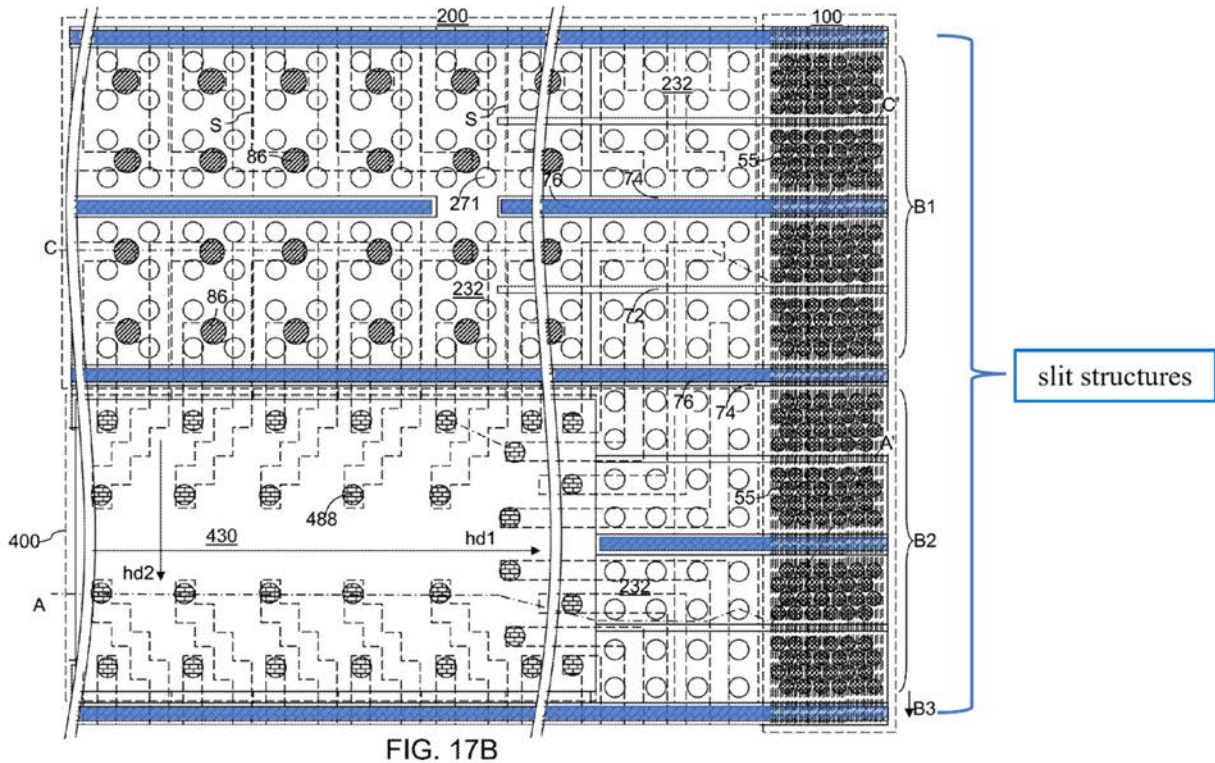
Lee ¶¶ 183-184.

5. [8.D]

Toyama discloses *slit structures* (“laterally-elongated contact via structures 76”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”):



Toyama, Fig. 17A; Lee ¶¶ 185-187. Toyama also depicts its *slit structures* (“laterally-elongated contact via structures 76”) in a top view:



Toyama, Fig. 17B. Toyama’s “laterally elongated contact via structures 76” are *slit structures* for the reasons explained above for Ground 1, limitation [8.D]. §IX.A.5.

6. [8.E]

As shown below, Toyama discloses *a staircase structure* (“staircase regions”) *disposed in the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”), *wherein the staircase structure comprises levels with each level having a conductor layer* (“electrically conductive layers 146, 246”) *thereon*:

7. [8.F]

Toyama discloses *local contacts* (“drain contact via structures 88”) *disposed on* (or and extending above) *the channel structures* (“memory stack structures 55”), and *local contacts* (“source connection via structures 91”) *disposed on* (above) *the slit structures* (“laterally-elongated contact via structures 76”):

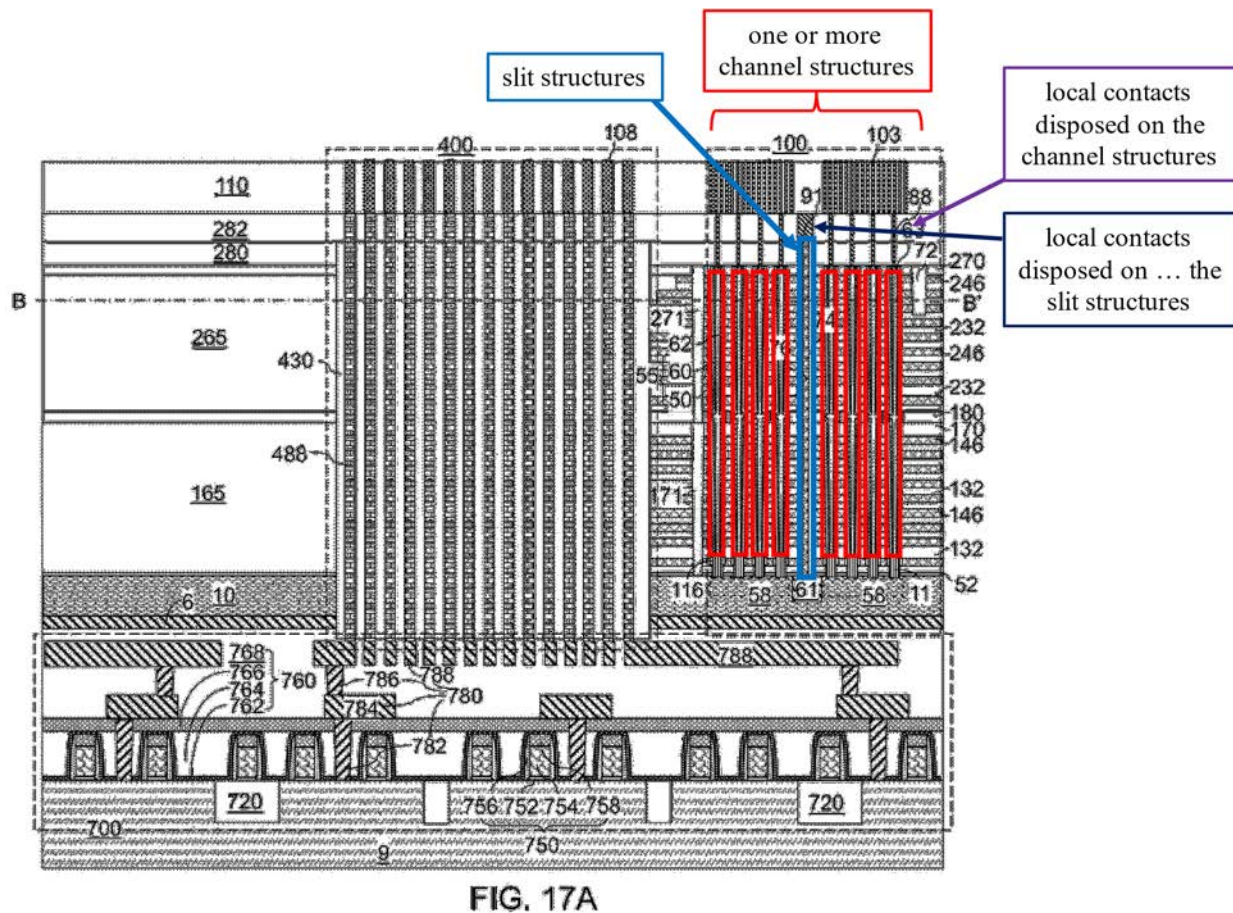


FIG. 17A

Toyama, Fig. 17A, [0251]; Lee ¶¶ 189-190. Toyama’s “drain contact via structures 88” are *local contacts disposed on the channel structures*, and Toyama’s “source connection via structures 91” are *local contacts disposed on the slit structures*, for the reasons explained above for Ground 1, limitation [8.F]. §IX.A.7.

8. [8.G]

a. [8.G.i]

The obviousness combination discloses or renders obvious *a through array contact (TAC) region*. As “[i]n some embodiments” of the 806 Patent, Toyama’s “dielectric structure ... defines the boundaries, the shape, and the size of [Toyama’s]

TAC region.” Ex. 1001, 10:26-28. The figure below shows the first exemplary structure’s *through array contact (TAC) region* (part of “through-memory-level via region 400”) along with, for reference, its *dielectric structure* (upper part of “dielectric fill material portion 430”):

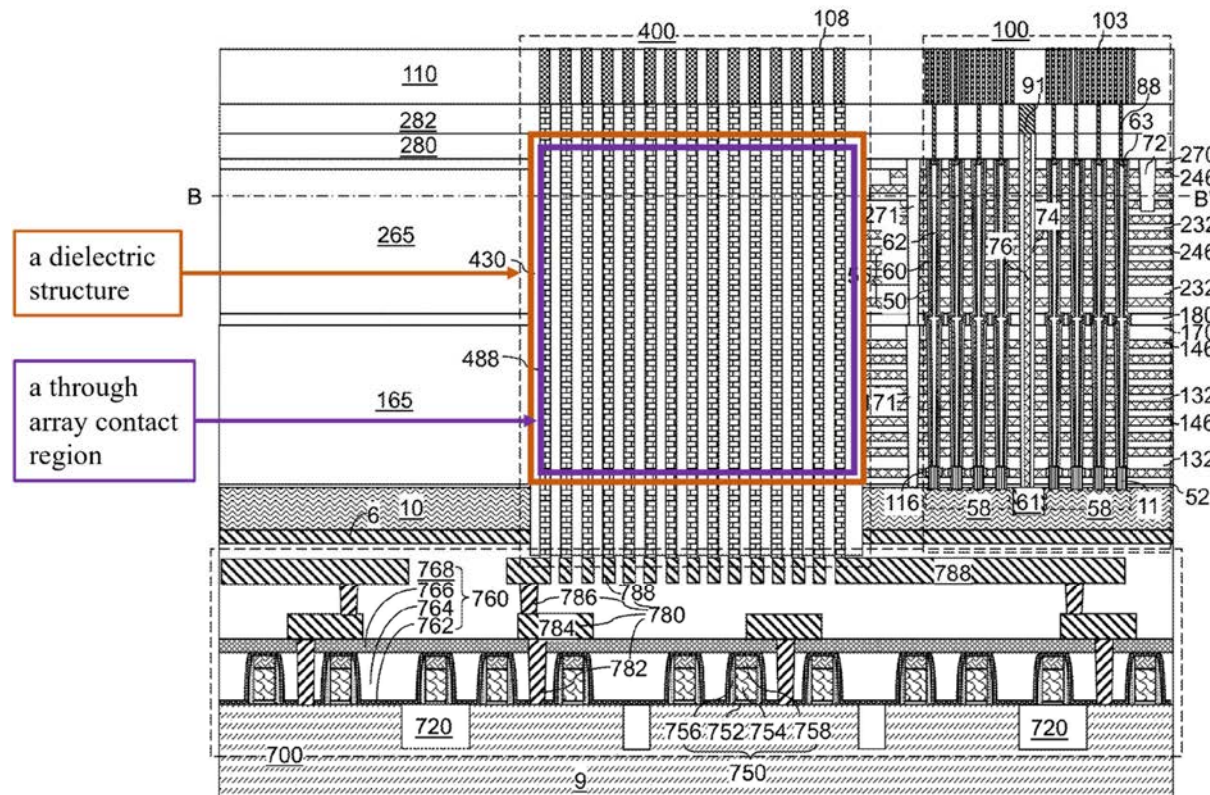
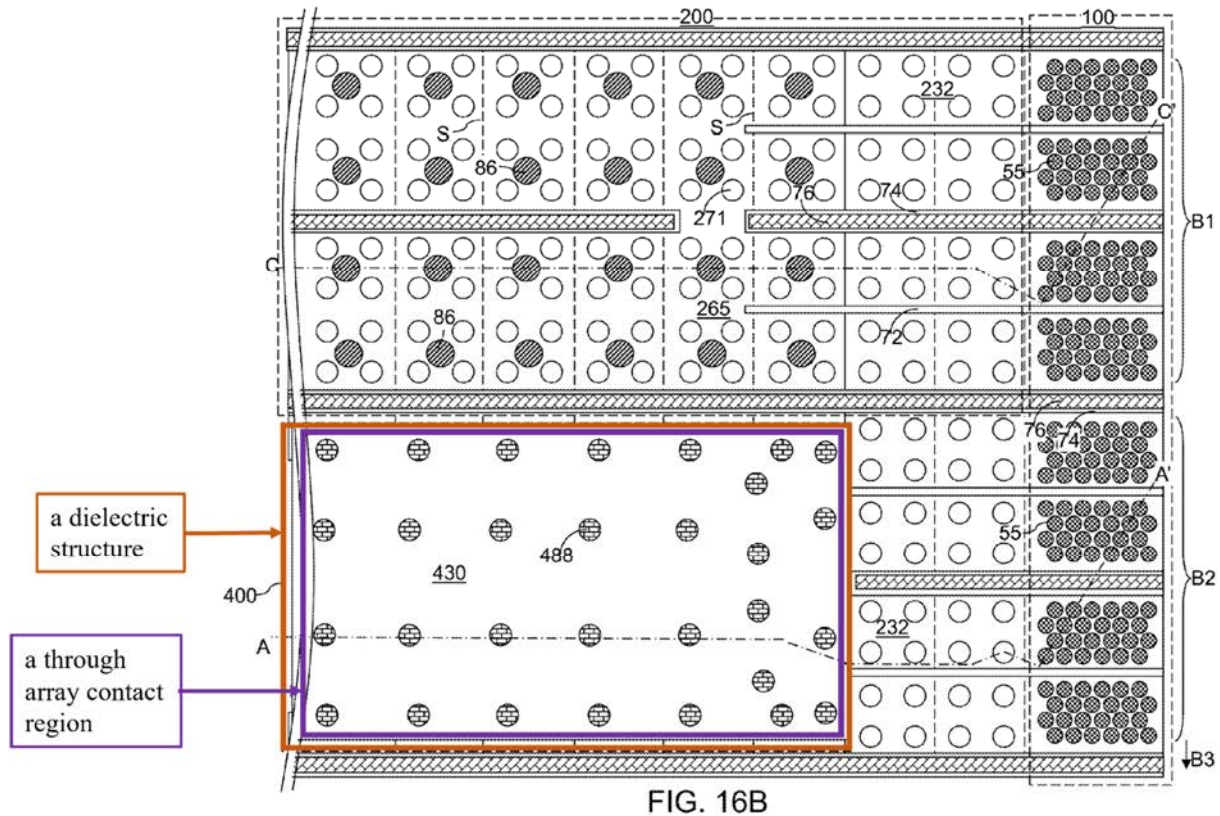


FIG. 17A

Toyama, Fig. 17A, [0165]-[0167]; Lee ¶ 195. Toyama also depicts its *through array contact (TAC) region* (part of “through-memory-level region 400”) in a top view:

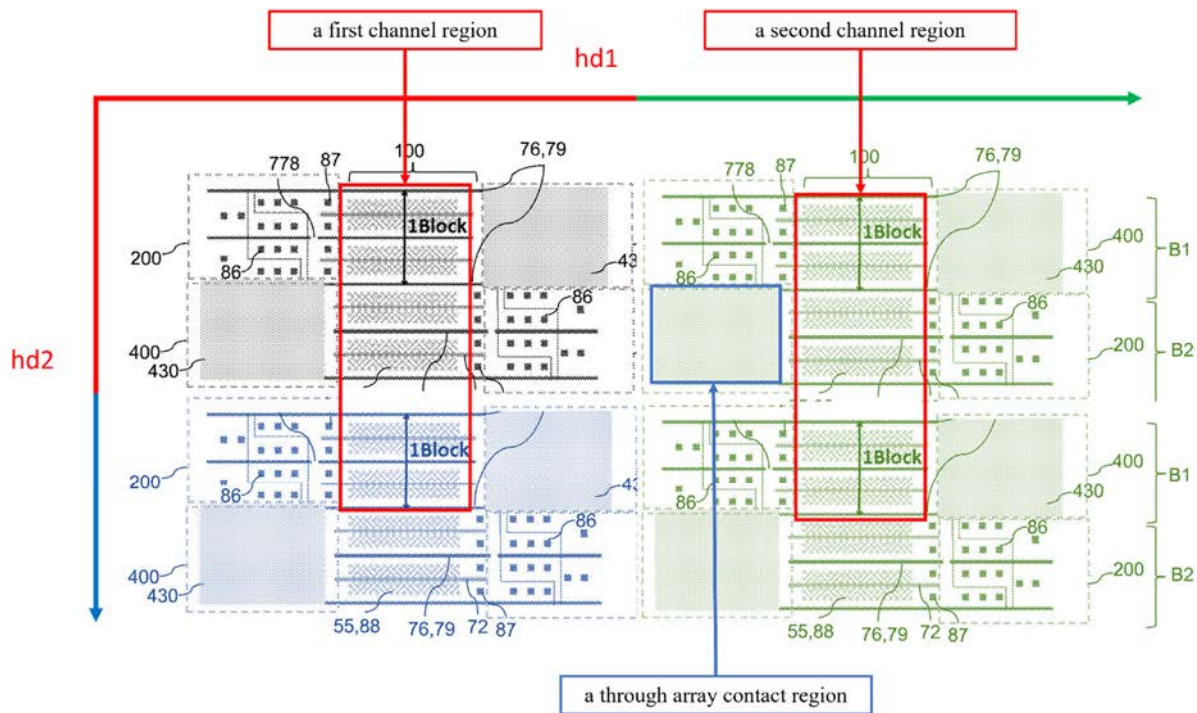


Toyama, Fig. 16B.

b. [8.G.ii]

Toyama does not expressly disclose that the first exemplary structure's *through array contact (TAC) region* (part of “through-memory-level via region 400”) is *formed between the first and second channel regions*. However, this limitation would have been obvious. As explained for limitation [8.C], above, a POSITA would have found it obvious to implement multiple planes of Toyama's first exemplary structure in the hd1 direction. §X.A.4. Thus, as depicted in the modified figure below, Toyama renders obvious *a through array contact (TAC)*

region (part of “through-memory-level via region 400”) *formed between the first and second channel regions* (first and second “memory array regions 100”):



Toyama, Fig. 17E (modified); Lee ¶¶ 196-197.

c. [8.G.iii]

Toyama’s “through-memory-level via structures 488” are *through array contacts (TACs)*. As shown below, Toyama teaches that *the TAC region* (part of “through-memory-level via region 400”) *comprises a plurality of through array contacts (TACs)* (“through-memory-level via structures 488”) *extending vertically through the dielectric structure* (part of “dielectric fill material portion 430”):

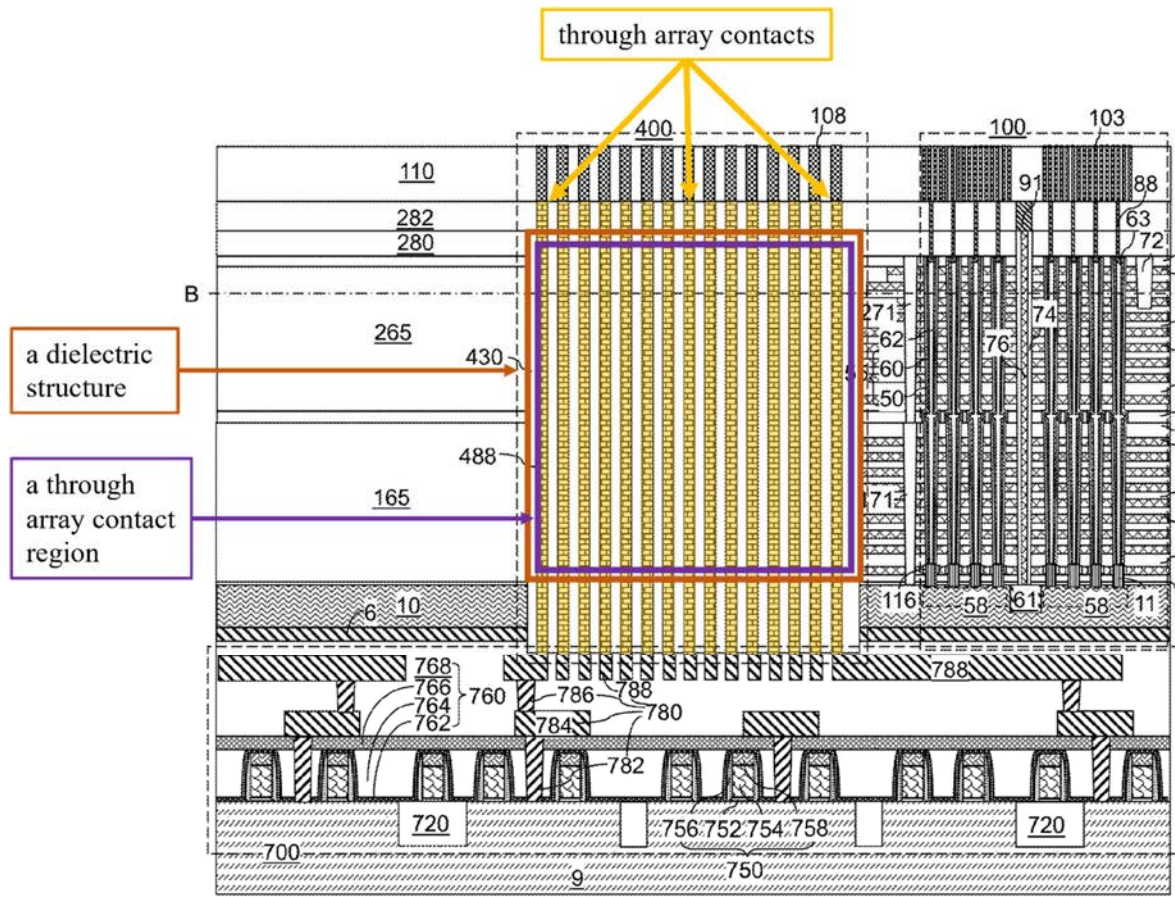
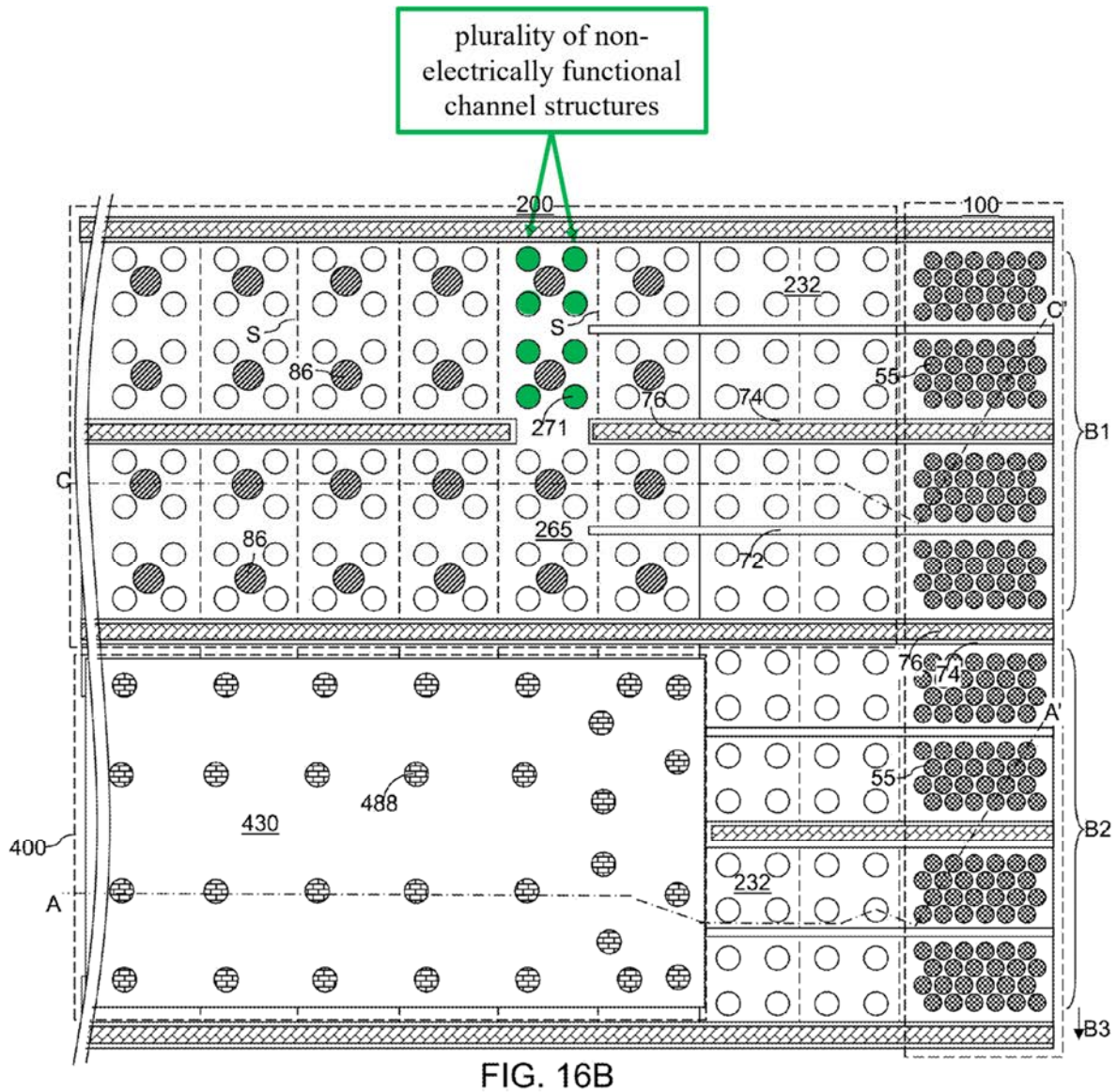


FIG. 17A

Toyama, Fig. 17A, [0239]; §§X.A.3 (limitation [8.B]), X.A.8.a (limitation [8.G.i]);

Lee ¶¶ 193-194.



Toyama, Figs. 17A, 16B, [0182], [0197]; Lee ¶ 199.

In the context of its first exemplary structure, Toyama discloses an embodiment in which “first-tier support pillar structures 171 are formed ... at the same time [that] the memory stack structures 55 are formed in the memory openings 49.” Toyama, [0203]. “In this embodiment, the first-tier support pillar structures 171 ... comprise dummy memory stack structures which are not electrically

connected to bit lines.” *Id.* A POSITA would have understood these “dummy memory stack structures” to be *non-electrically functional channel structures*; indeed, Toyama’s “dummy” memory stack structures are just like those of the ’806 Patent. *Compare id. with* Ex. 1001, 6:22-23, 14:36-49 (dummy channel structures with no local contact); Lee ¶ 200.

Although Toyama does not expressly state that “second-tier support pillar structures 271” are “dummy memory stack structures,” a POSITA would have understood them to be. Indeed, just as Toyama forms the first and second tiers of “memory stack structures 55” concurrently, so too would a POSITA have understood Toyama to form the first and second tiers of “support pillar structures” 171, 271 as “dummy memory stack structures” concurrently. Lee ¶ 201. And a POSITA would have recognized that doing the opposite—that is, forming “first-tier support pillar structures 171” as “dummy memory stack structures” (as Toyama expressly discloses) but **not** forming second-tier support pillar structures 271 as “dummy memory stack structures”—would make little sense; doing so would require additional processing steps and reduce the uniformity of the device. *Id.*

At the very least, a POSITA would have found it obvious to form Toyama’s “support pillar structures” 171, 271 as dummy memory stack structures. A POSITA would have known (not just from Toyama, but also from a POSITA’s general knowledge) how to create support pillar structures by depositing the components of

memory stack structures and how to make them *non-electrically functional* simply by not connecting those structures to anything. See, e.g., Toyama, [0311] (“dummy memory stack structures” can be formed “for structural support”); Ex. 1016, [0162] (“support pillar structure” includes same components as “memory stack structure”); Ex. 1017, 9:50-67 (“support pillar structures” includes same components as “memory stack structures”); Ex. 1015, [0073]-[0081] (“memory openings 49” and “support openings 19” are filled with the same materials); Lee ¶ 203.

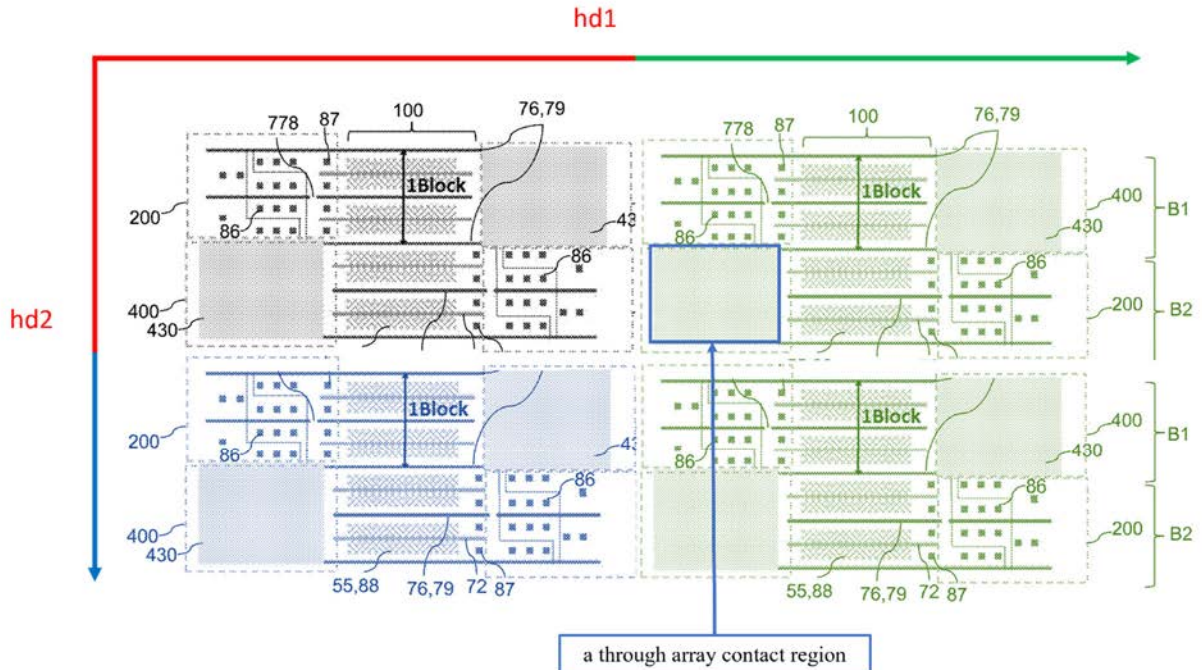
A POSITA would have been motivated to form *non-electrically functional channel structures* (“dummy memory stack structures”) because they provide structural support and because they can be formed in the same process steps as the functional *channel structures* (“memory stack structures”). Lee ¶ 204.

A POSITA also would have had a reasonable expectation of success in doing so because of the numerous references (including Toyama itself) that disclose techniques for forming dummy memory stack structures. *Id.*

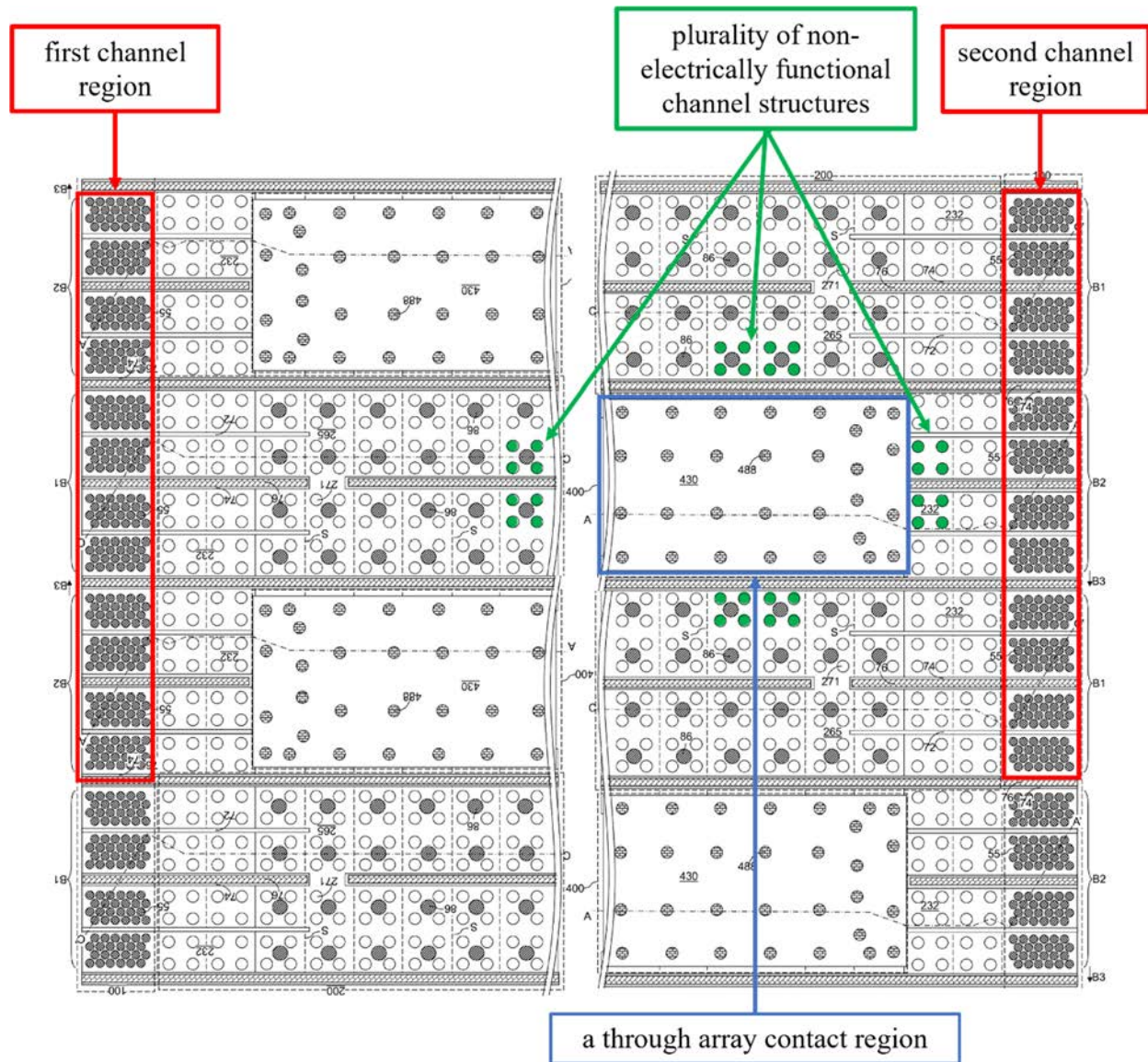
Toyama thus discloses (or at least renders obvious) this limitation.

b. “... surrounding the TAC region and between the first and second channel regions”

A POSITA would have found this limitation obvious. As explained for limitation [8.C], above, a POSITA would have found it obvious to implement multiple planes of Toyama’s first exemplary structure in the hd1 direction, as illustrated in the modified figure below:



Toyama, Fig. 17E (modified); §X.A.4. Extending the view shown in Fig. 16B to reflect this layout, the obvious modification to Toyama's first exemplary structure would appear as follows:



B. Claim 10

1. [10.Pre]

See §X.A.1.

2. [10.A]

Toyama discloses *a substrate* (layer 10) for the same reasons set forth in §IX.B.2. *See also* Toyama, [0211], Fig. 17A; Lee ¶ 207.

3. [10.B]

For the reasons explained in §IX.B.3 and illustrated below, Toyama discloses, or renders obvious, this limitation:

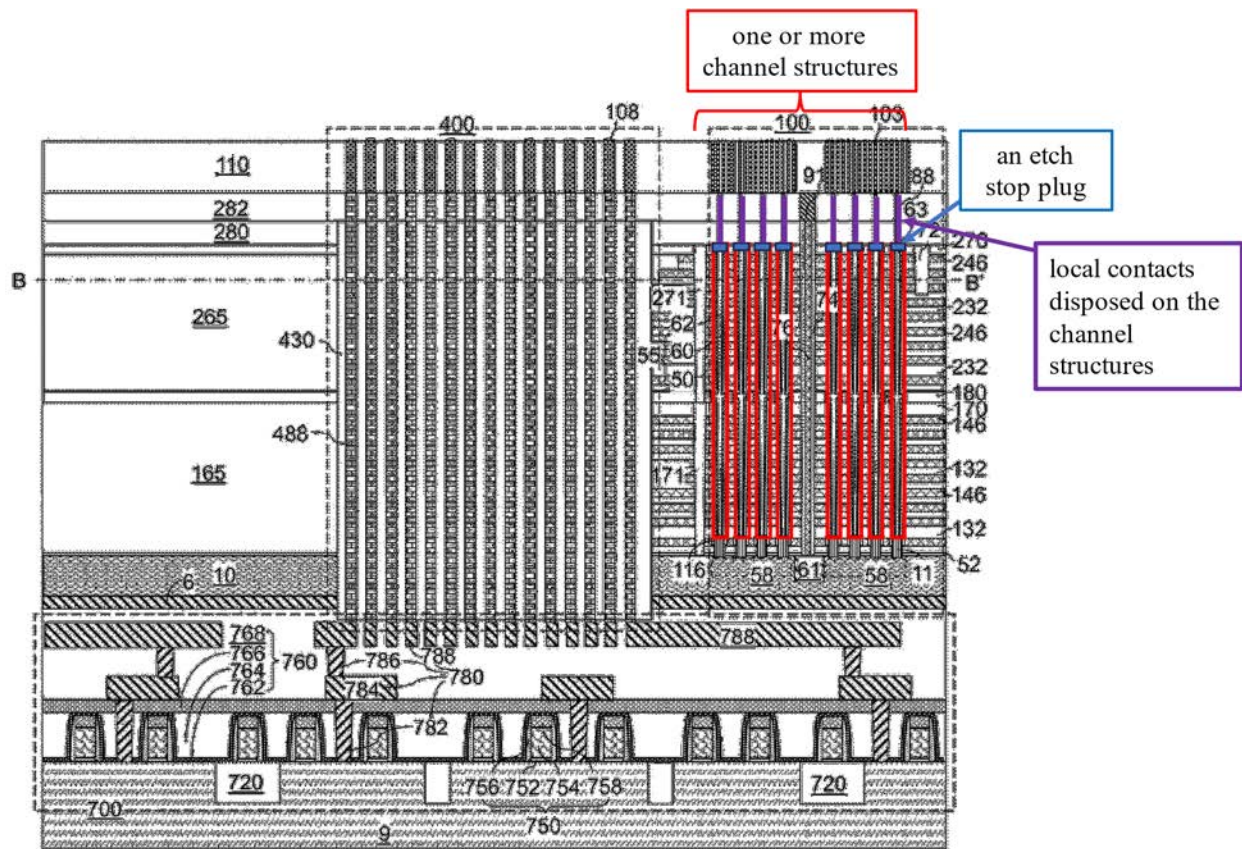
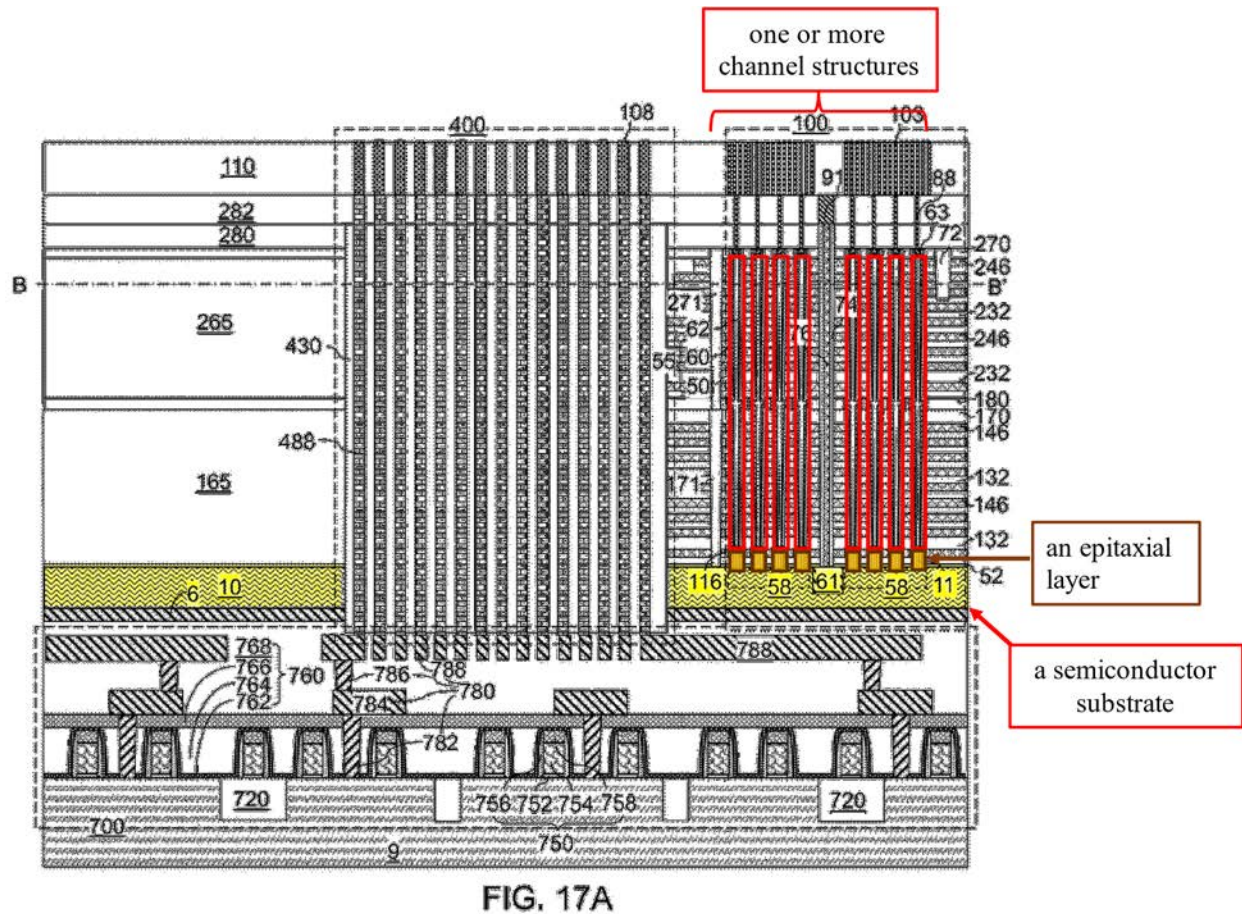


FIG. 17A

Toyama, Figure 17A, [0209], [0241]-[0242]; Lee ¶¶ 208-216. Indeed, just as the Second Modification’s “drain regions 63” stop the etch that forms “drain contact via structures 88,” so too do the first exemplary structure’s “drain regions 63.” *Id.*

4. [10.C]

For the reasons explained in §IX.B.4 and illustrated below, Toyama discloses or renders obvious this limitation:



Toyama, Figure 17A, [0202], [0208], [0225]; Lee ¶¶ 217-220.

XI. GROUND 3: TOYAMA’S FIRST EXEMPLARY STRUCTURE AND SECOND MODIFICATION TO ITS FOURTH EXEMPLARY STRUCTURE IN VIEW OF THE KNOWLEDGE OF A POSITA

In this Ground, the Petition discusses a modification of Toyama’s Second Modification that forms the “through-memory-level via structures” within a unitary dielectric fill material (as in Toyama’s first exemplary structure) instead of using the Second Modification’s “insulating liners 674.” §§IX.A.3.a (Second Modification), X.A.3.a (first exemplary structure). As the Petition explains below, a POSITA

would have been motivated to make the combination with a reasonable expectation of success. The combination renders the Challenged Claim obvious.

A. A POSITA would have found it obvious to form the Second Modification’s “through-memory-level via structures” in a unitary dielectric fill material

- 1. Toyama discloses, in the Toyama’s first exemplary context of its first exemplary structure, the use of a unitary dielectric fill material portion to insulate “through-memory-level via structures”**

As Ground 2 discusses in further detail, Toyama’s first exemplary structure expressly discloses that “through-memory-level via structures” can be electrically isolated from the “alternating stack” by a unitary “dielectric fill material portion 430,” as the below figure illustrates:

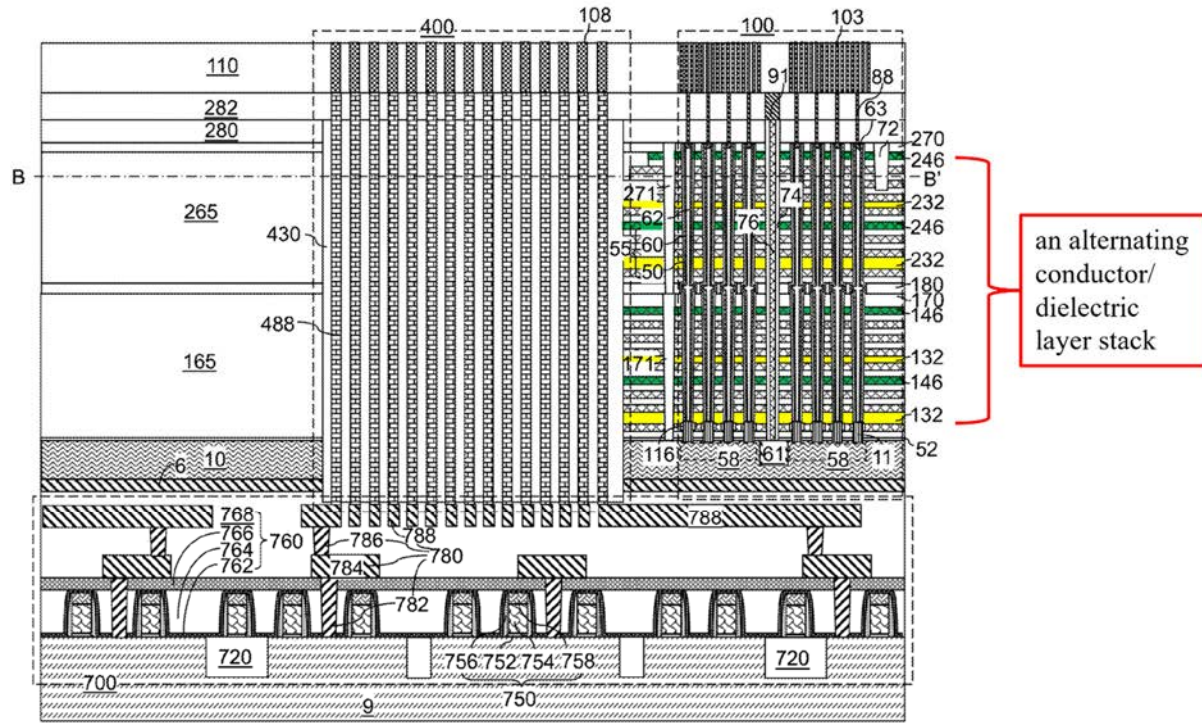


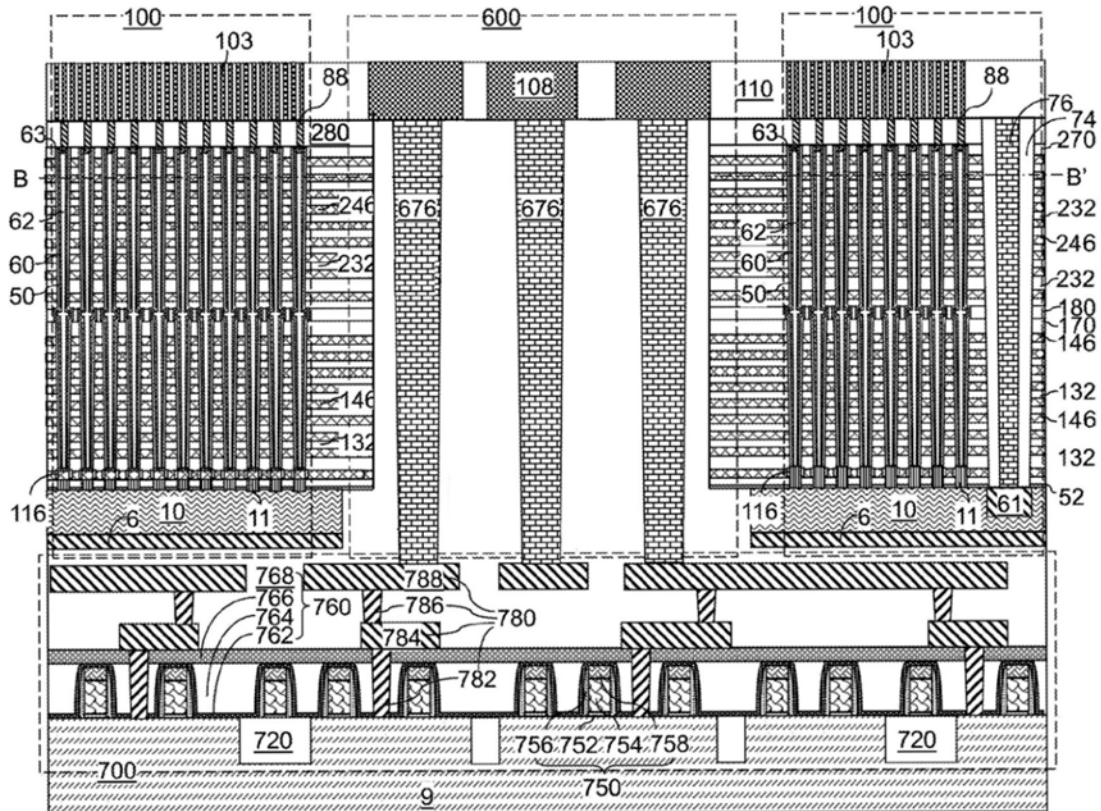
FIG. 17A

Toyama, Fig. 17A; Lee ¶ 222; §X.A.3.a. Thus, it was known in the art to insulate conductive elements (such as “through-memory-level via structures”) using a unitary dielectric fill material.

Toyama's Second Modification expressly discloses "through-memory-level via structures 676" that extend vertically through the "alternating stack" and that are electrically isolated from the alternating stack by "insulating liners 674," as the below figure illustrates:

FIG. 49

A POSITA would have found it obvious to modify Toyama’s Second Modification to electrically isolate “through-memory-level via structures 676” with



Toyama, Fig. 49 (modified).¹⁵ A modified version of Fig. 48B, below, illustrates a top view of the obviousness combination:

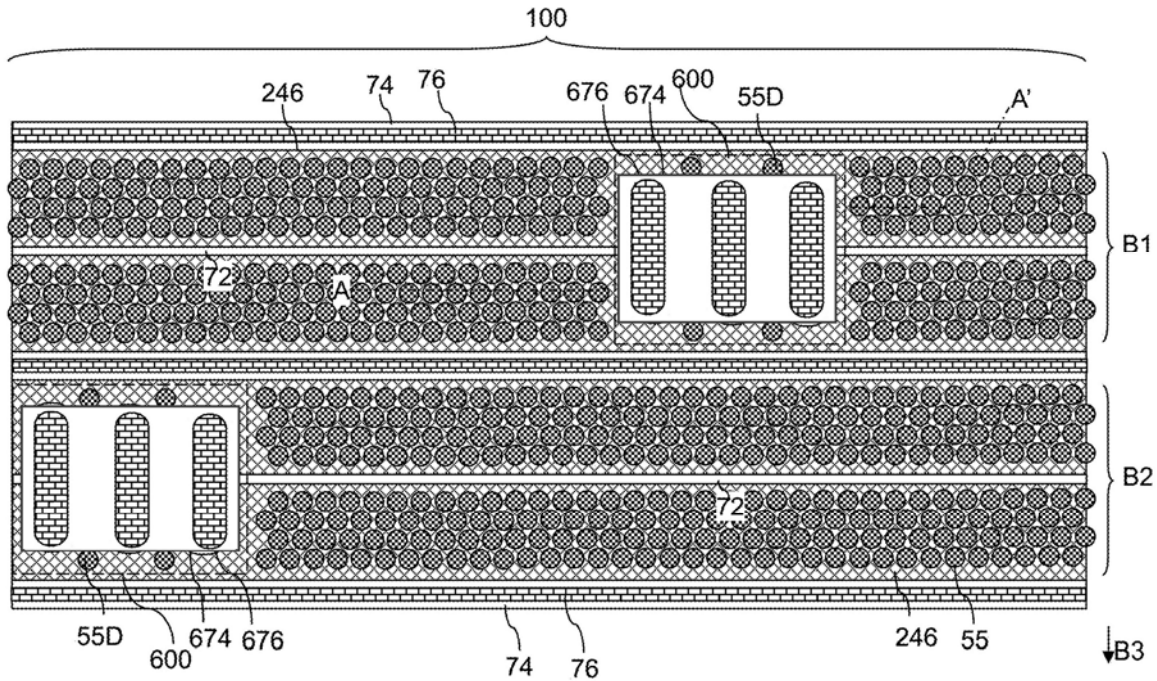


FIG. 48B

Toyama, Fig. 48B (modified).

As the Petition explains in further detail below, the obviousness combination is nothing more than the mere substitution of one element (the Second Modification’s “insulating liners 674”) for another known in the field (a unitary dielectric fill material, as in the first exemplary structure’s “dielectric fill material portion 430”) to yield a predictable result (e.g., electrically isolating the Second Modification’s “through-memory-level via structures”). *Lee ¶¶ 222-239; KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

3. Motivation to combine

A POSITA would have been motivated to use a unitary dielectric fill material to surround “through-memory-level via structures 676.” Lee ¶¶ 226-231.

A POSITA would have understood that forming the “through-memory-level via structures” inside a unitary dielectric fill material, as in the obviousness combination, would be desirable—and, indeed, serve a necessary function—because the dielectric fill material electrically isolates the “through-memory-level via structures.” Lee ¶ 227. A POSITA would have recognized that electrically isolating the “through-memory-level via structures” would be desirable because otherwise the “through-memory-level via structures” may electrically interfere with each other and/or with other of the Second Modification’s conductive elements, such as “electrically conductive layers (146, 246).” Toyama, [0316]; Lee ¶ 227.

As a legal matter, motivation to combine does not require that the obviousness combination be superior to Toyama’s expressly disclosed embodiments. “It’s not necessary to show that a combination is ‘the best option, only that it [is] a suitable option.’” *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021) (quoting *PAR Pharm., Inc. v. TWI Pharms., Inc.*, 773 F.3d 1186, 1197-98 (Fed. Cir. 2014)). Nevertheless, a POSITA would have understood that the obviousness combination has benefits over some of Toyama’s expressly disclosed embodiments.

First, a POSITA would have understood that the obviousness combination would reduce capacitive coupling as compared to Toyama's Second Modification as expressly disclosed. Capacitive coupling (also called crosstalk) is an undesirable phenomenon that causes a signal in one conductive element to affect a signal in a different conductive element where the two conductive elements are separated by an insulator. Ex. 1026, 39-40, 64, 77; Lee ¶ 228. Capacitive coupling is inversely proportional to distance so, all else equal, a greater separation between conductive elements will have less capacitive coupling. Ex. 1026, 39 (“[I]ncreasing the separation of conductors reduces capacitive coupling.”). Where a “through-memory-level via region” is within a block of “memory stack structures 55,” capacitive coupling may occur between the “through-memory-level via structures” and “electrically conductive layers (146, 246).” Lee ¶ 228. This is undesirable because it creates electrical noise in both the “through-memory-level via structures” and in the “electrically conductive layers.” Ex. 1026, 39 (noting that “electrical noise” caused by “coupling of signals between nearby conductors due to parasitic capacitance” is a “pressing issue” for electrical performance); Lee ¶ 229.

Toyama's Second Modification separates its “through-memory-level via structures 676” from its “electrically conductive layers (146, 246)” with “insulating liners 674” and layers 180, 280. Toyama, Fig. 49. By contrast, Toyama's first exemplary structure separates its “through-memory-level via structures” from its

“electrically conductive layers (146, 246)” with a single “dielectric fill material portion 430.” Toyama, Figs. 17A-B. A POSITA would have understood that because Toyama’s first exemplary structure includes a unitary “dielectric fill material portion 430” to isolate the “through-memory-level via structures” from the “electrically conductive layers” instead of “liners 674” and layers 180, 280, the first exemplary structure’s “through-memory-level via region” would be less susceptible to capacitive coupling between the “via structures” and the “electrically conductive layers” than that of Toyama’s Second Modification.¹⁶ Lee ¶ 230.

Second, a POSITA would have found the obviousness combination to have a benefit over Toyama’s first exemplary structure (which expressly discloses a “dielectric fill material portion 430”) because it places the “dielectric fill material portion” and “through-memory-level via structures” inside “memory array region 100.” A POSITA would have recognized that placing the “through-memory-level via structures” within “memory array region 100” has the benefit that the “through-

¹⁶ That is not to say that Toyama’s Second Modification is inoperative; it is operative and a POSITA would have appreciated its benefits. The Petition’s point here is merely that a POSITA would have understood that the obviousness combination has some benefits over some of Toyama’s expressly disclosed embodiments. Lee ¶¶ 226-231.

memory-level via structures” are closer to the elements that use the signals carried by the through-memory-level via structures. Lee ¶ 231.

For example, a POSITA would have understood that “through-memory-level via structures” can connect “memory stack structures 55” to peripheral devices underneath the memory array that provide control signals to “memory stack structures 55.” Toyama, [0003], [0163], Fig. 49; Lee ¶ 231. Similarly, a POSITA would have understood that “through-memory-level via structures” can connect “memory stack structures 55” to a “power distribution network” or to “control signals.” Toyama, [0361], [0377]; Lee ¶ 231. As a POSITA would have known, placing the “through-memory-level via structures” that carry the above-mentioned signals inside of a “memory array region 100”—that is, closer to “memory stack structures 55”—has numerous benefits, including reducing signal propagation delays and electrical losses. Lee ¶ 231.

4. Reasonable expectation of success

A POSITA would have had a reasonable expectation of success in implementing the obviousness combination, that is, modifying Toyama’s Second Modification to electrically isolate “through-memory-level via structures 676” with a unitary dielectric fill material. Lee ¶¶ 232-239.

As an initial matter, Toyama contemplates further modification of its expressly disclosed embodiments. Lee ¶¶ 232-238. The arrangement of Toyama’s

specification, which starts with an “exemplary structure” and describes modifications thereto, confirms that a POSITA would have been able to mix and match the relevant elements of Toyama’s exemplary structures. Toyama notes that the “second modification of the fourth exemplary structure can be formed concurrently with the formation of any of the first, second, and third exemplary structures or modifications thereof, or can be formed as a stand-alone structure.” Toyama, [0332]. And Toyama further notes that “where an embodiment employing a particular structure and/or configuration as illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that substitutions are not explicitly forbidden or otherwise known to be impossible to one of ordinary skill in the art.” *Id.*, [0390].

A POSITA also would have understood how to manufacture a device implementing the obviousness combination. Lee ¶ 239. Toyama discloses in great detail how to form “dielectric fill material portion 430” and the “through-memory-level via structures” within it. See Toyama, Figs. 1A-17F. For example, Toyama discloses patterning an opening 769, filling the opening with “dielectric fill material portion 430,” and performing another patterning and fill process to create the through array contacts (“through-memory-level via structures 488”). *Id.*, [0213]-

[0216], [0242]. Patterning and filling were well-known processes in the art of a 3D NAND device manufacture (and semiconductor manufacture, generally).

What’s more, a POSITA would have understood that the elements of the first exemplary structure and the Second Modification are compatible with each other. Lee ¶¶ 236-239. Indeed, outside of each structure’s “through-memory-level via region,” the elements of the first exemplary structure and the Second Modification are largely the same, e.g., *the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”), *the channel structures* (“memory stack structures 55”), *the slit structures* (“laterally elongated contact via structures 76”), *the staircase structure* (“staircase regions”), *the local contacts disposed on the channel structures* (“drain contact via structures 88”), and *the local contacts disposed on the slit structures* (“source connection via structures 91”). See §§IX.A, X.A.

Even within the “through-memory-level via region,” a POSITA would have understood each structure’s components to serve a similar purpose. Lee ¶ 237. The first exemplary structure’s *through array contacts* (“through-memory-level via structures 488”), like the Second Modification’s *through array contacts* (“through-memory-level via structures 676”), carry electrical signals vertically through the respective structure’s *dielectric structure*. And the first exemplary structure’s *dielectric structure* (the upper part of “dielectric fill material portion 430”), like the

Second Modification's *dielectric structure* ("insulating liners 674) electrically isolates the *through array contacts* ("through-memory-level via structures") from *the alternating conductor/dielectric layer stack* ("alternating stack (132, 146, 232, 246).” *Id.*

A POSITA would have also understood that the process steps for forming the structures are compatible. Lee ¶ 238. Indeed, Toyama expressly describes patterning and filling (which, as discussed above, are used to form the first exemplary structure's "through-memory-level via region 400") in the context of the fourth exemplary structure and its modifications. See, e.g., Toyama, [0314]-[0315], [0318], [0324], [0326], [0334]-[0335].

In sum, a POSITA would have found it straightforward to form a unitary dielectric fill material in "through-memory-level region 600" and subsequently forming "through-memory-level via structures 676" within the unitary dielectric.

The effect of the obviousness combination would have been predictable to a POSITA. Lee ¶ 239. Just as the physical characteristics of a house can be predicted from its constituent components (e.g., its foundation, studs, joists, drywall, etc.), the characteristics of Toyama's exemplary structures were at the relevant time predictable to a POSITA based on each structure's constituent components (e.g., the "memory stack structures," the components of the "through-memory-level via regions," the "alternating stack," etc.) and well-understood physical and electrical

phenomena. *Id.* Specifically, a POSITA would have understood that a unitary dielectric fill material would fulfill the purpose of the Second Modification’s “insulating liners 674,” namely, to electrically isolate the “through-memory-level via structures 676.” *Id.*

In summary, a POSITA would have understood that the relied-upon teachings in Toyama could be fit together “like pieces of a puzzle.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 420 (2007).

B. Claim 8:

1. [8.PRE]

For the reasons explained in Ground 1, above, Toyama’s Second Modification discloses this limitation. §IX.A.1. The obviousness combination remains *a three-dimensional (3D) memory device*. Lee ¶ 240.

2. [8.A]

As explained in Ground 1, above, the Second Modification’s “alternating stack (132, 146, 232, 246)” is *an alternating conductor/dielectric layer stack*. §IX.A.2 (limitation [8.A]). The obviousness combination does not alter the Second Modification’s “alternating stack.” *Id.* Thus, as shown below, the obviousness combination renders this limitation obvious:

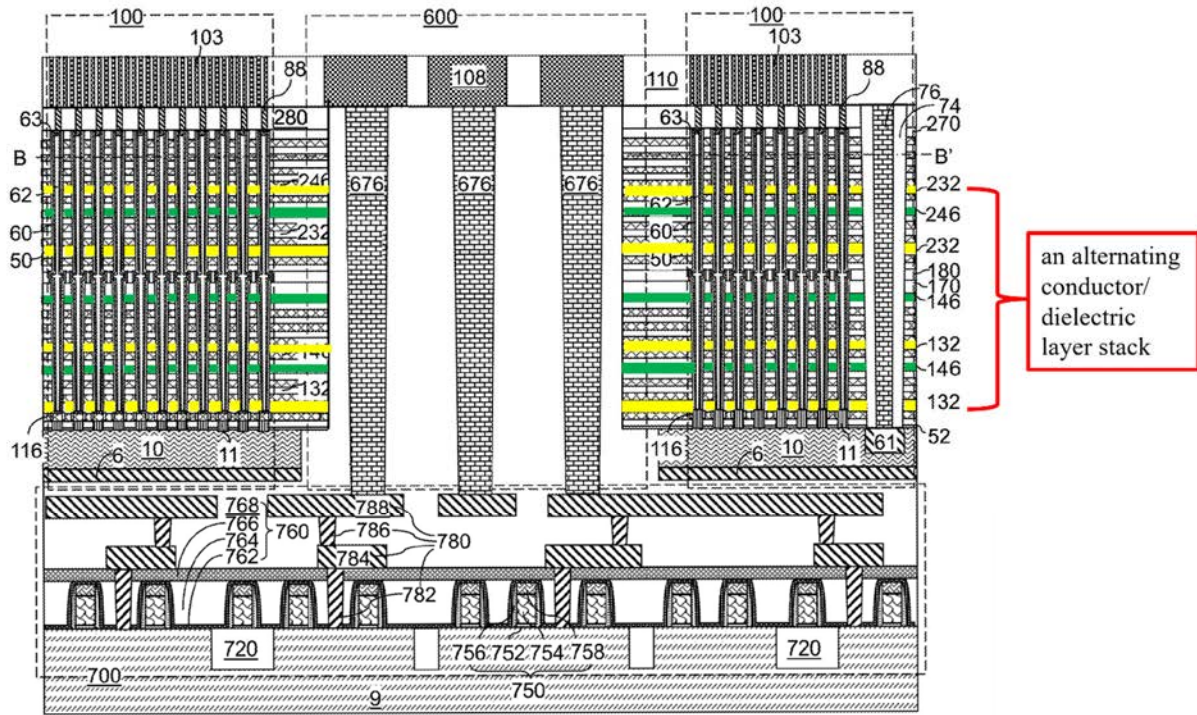


FIG. 49

Toyama, Fig. 49 (modified); Lee ¶ 241.

3. [8.B]

As explained above, the obviousness combination involves using a unitary dielectric fill material in place of the Second Modification’s “insulating liners 674.”

§XI.A.2. As shown below, this dielectric fill material is *a dielectric structure*:

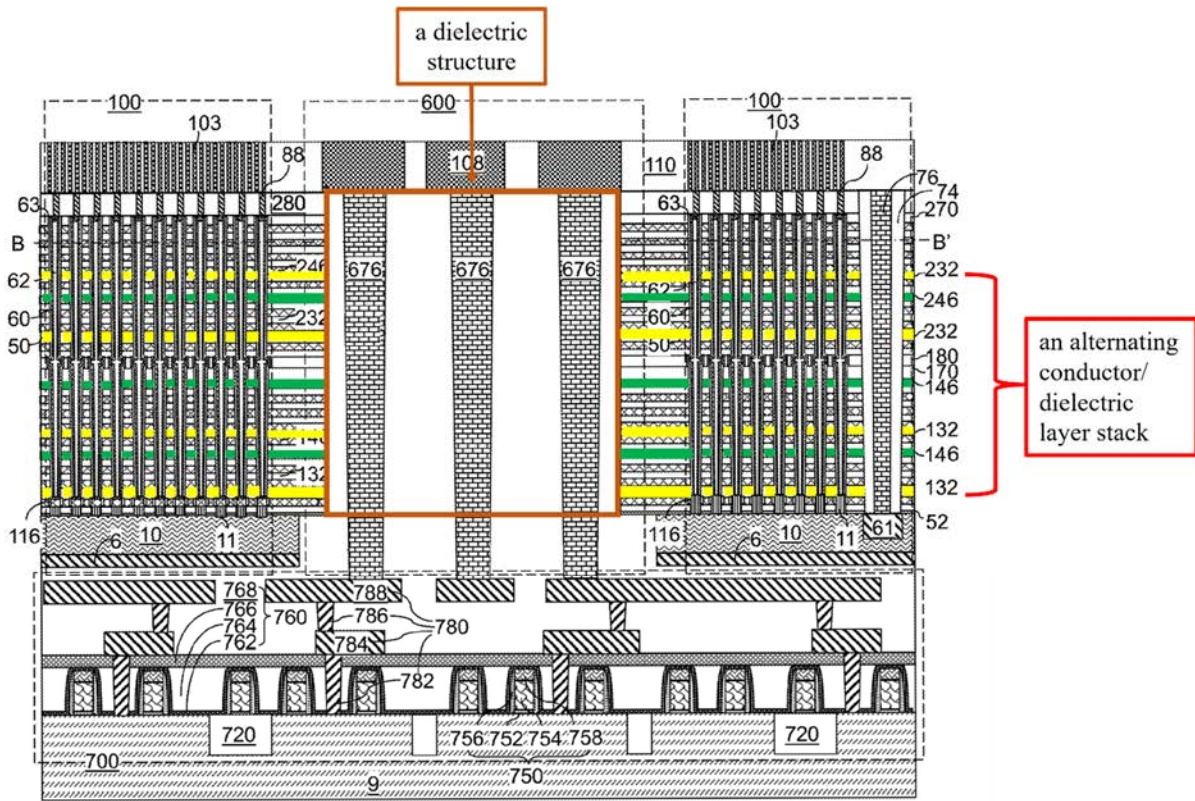


FIG. 49

Toyama, Fig. 49 (modified); Lee ¶ 242.

Just as the first exemplary structure’s “dielectric fill material portion 430” is *a dielectric structure extending vertically through the alternating conductor/dielectric layer stack*, so too is the dielectric fill material shown above.

§X.A.3 (Ground 2, limitation [8.B]); Toyama, [0216].

4. [8.C]

As explained in Ground 1, above, the Second Modification discloses *first and second channel regions* (first and second parts of “memory array region 100”) *comprising first and second pluralities of channel structures* (“memory stack structures 55”). §IX.A.4 (Ground 1, limitation [8.C]).

The obviousness combination does not alter the Second Modification's *first and second channel regions* (first and second parts of “memory array region 100”).

§XI.A.2. Thus, as shown below, the obviousness combination renders this limitation obvious:

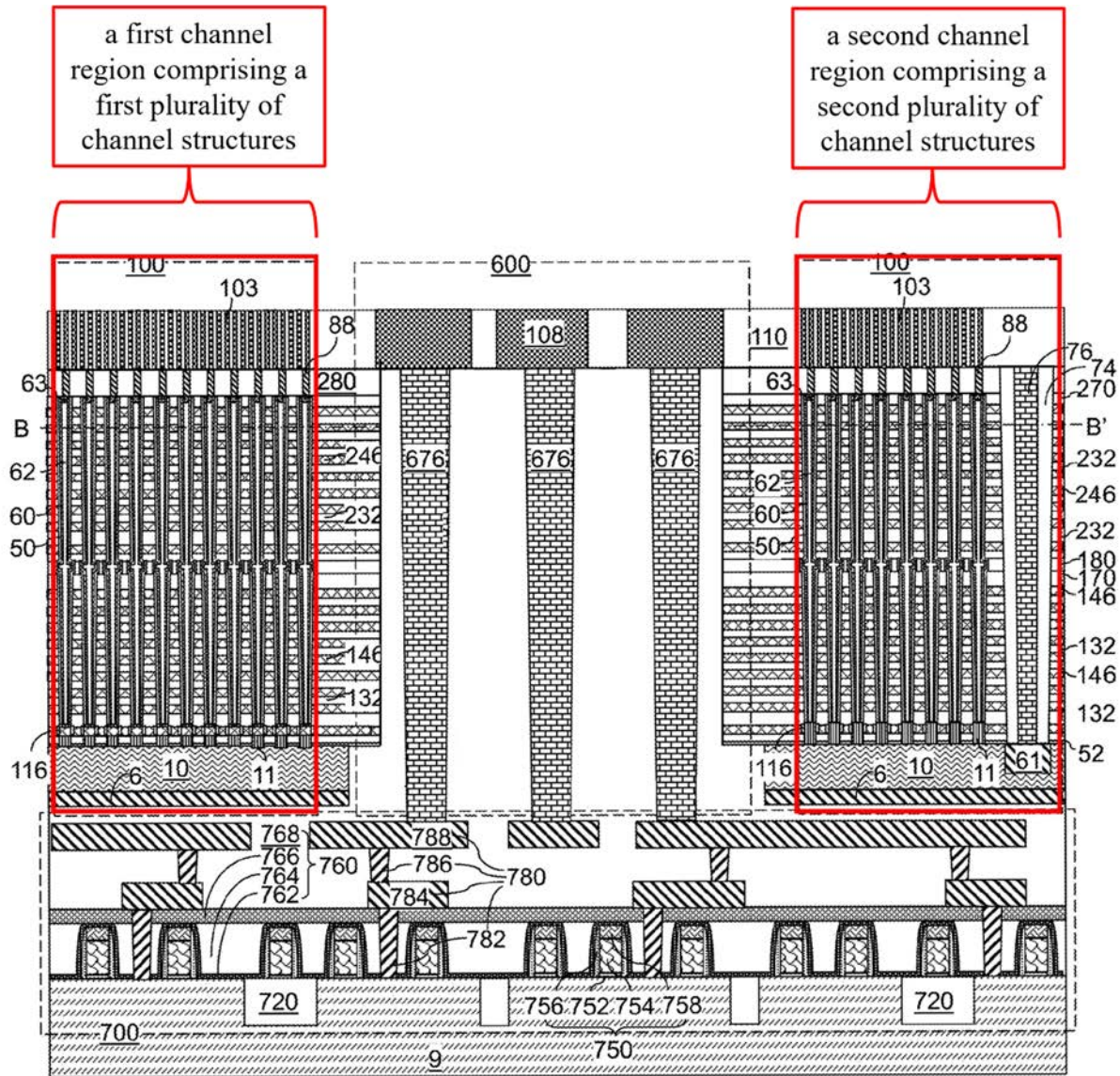


FIG. 49

Toyama, Fig. 49 (modified); Lee ¶ 243.

5. [8.D]

As explained in Ground 1, above, Toyama discloses *slit structures* (“laterally-elongated contact via structures 76”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”). §IX.A.5 (Ground 1, limitation [8.D]).

The obviousness combination does not alter the Second Modification’s *slit structures* (“laterally-elongated contact via structures 76”). §XI.A.2. Thus, the obviousness combination renders this limitation obvious. Lee ¶ 244.

6. [8.E]

As explained in Ground 1, above, Toyama’s Second Modification discloses or renders obvious *a staircase structure* (“staircase regions”) *disposed in the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”), *wherein the staircase structure comprises levels with each level having a conductor layer* (“electrically conductive layers 146, 246”) *thereon*. §IX.A.6.

The obviousness combination does not alter the Second Modification’s *staircase structure* (“staircase regions”). §XI.A.2. Thus, the obviousness combination renders this limitation obvious. Lee ¶ 245.

7. [8.F]

As explained in Ground 1, above, the Second Modification discloses or renders obvious *local contacts* (“drain contact via structures 88”) *disposed on* (in contact with or extending above) *the channel structures* (“memory stack structures

55”), and *local contacts* (“source connection via structures”) *disposed on* (above) *the slit structures* (“laterally-elongated contact via structures 76”). §IX.A.7.

The obviousness combination does not alter the Second Modification’s *local contacts*. §XI.A.2. Thus, the obviousness combination renders this limitation obvious. Lee ¶ 246.

8. [8.G]

a. [8.G.i]

The obviousness combination discloses or renders obvious *a through array contact (TAC) region*. As “[i]n some embodiments” of the 806 Patent, the obviousness combination’s “dielectric structure ... defines the boundaries, the shape, and the size of [its] TAC region.” Ex. 1001, 10:26-29. Specifically, the obviousness combination’s *dielectric structure* (the unitary dielectric fill material) defines the boundaries of its *through array contact (TAC) region* (part of “through-memory-level via region 600”), shown below:

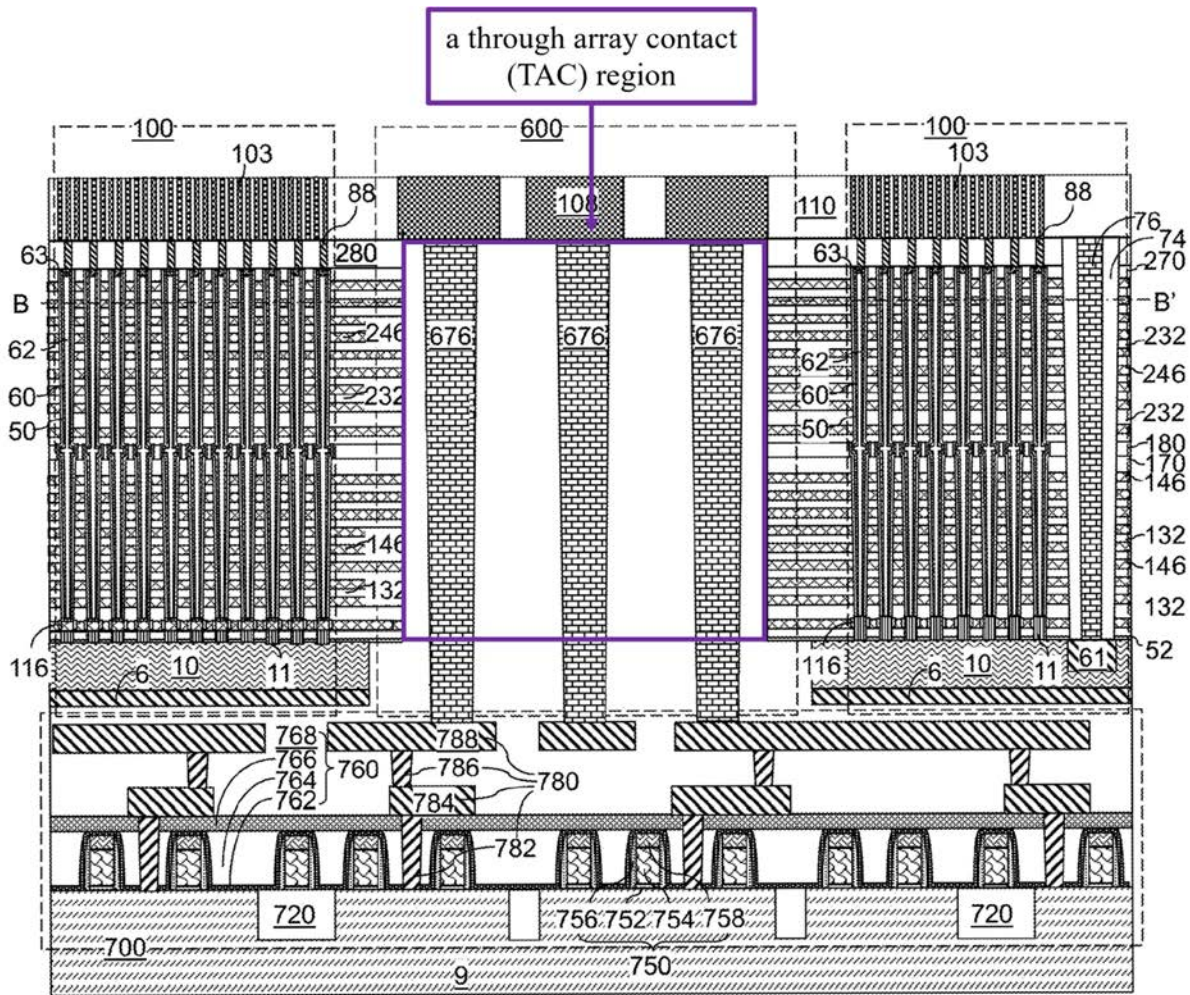


FIG. 49

Toyama, Fig. 49 (modified); Lee ¶¶ 249-250. The below modified figure shows a top view of the obviousness combination:

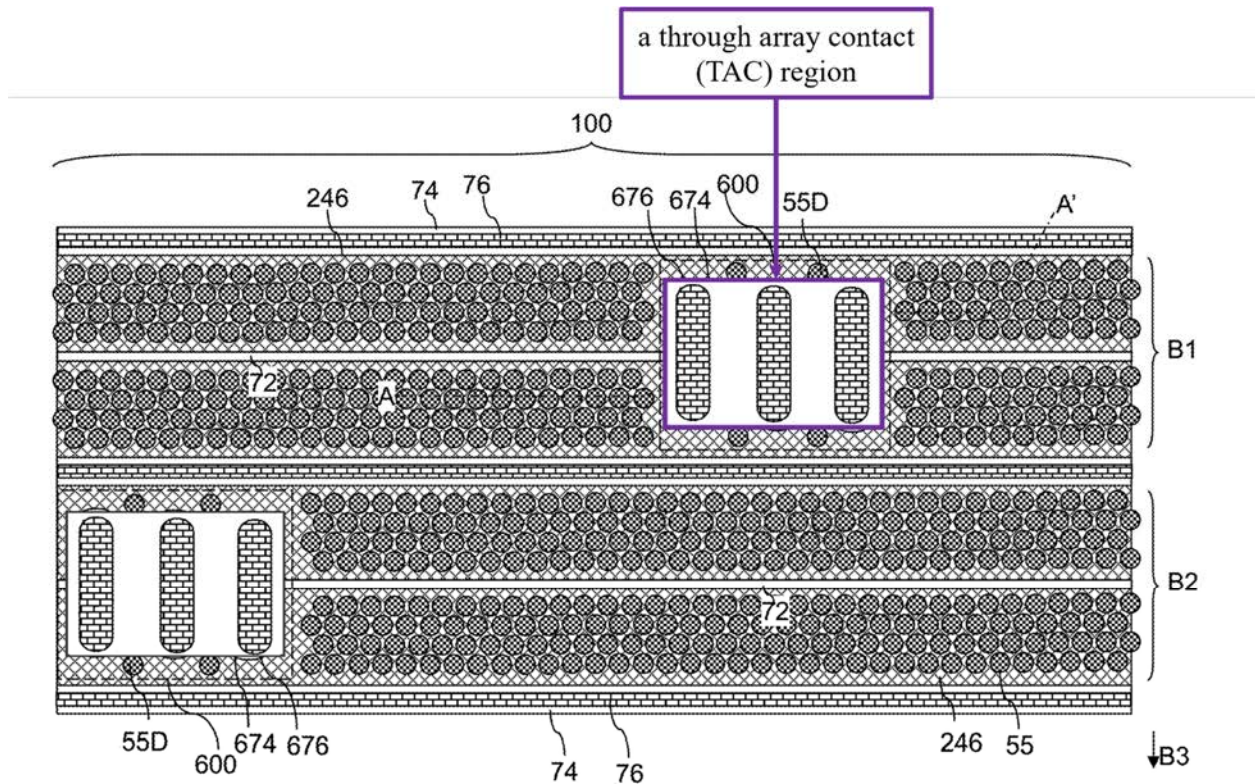


FIG. 48B

Toyama, Fig. 48B (modified).

b. [8.G.ii]

As discussed above for limitation [8.C], the obviousness combination renders obvious *first and second channel regions* (first and second parts of “memory array region 100”). Thus, as shown below, the obviousness combination’s *TAC region* (part of “through-memory-level via region 600”) is *formed between the first and second channel regions* (first and second parts of “memory array region 100”):

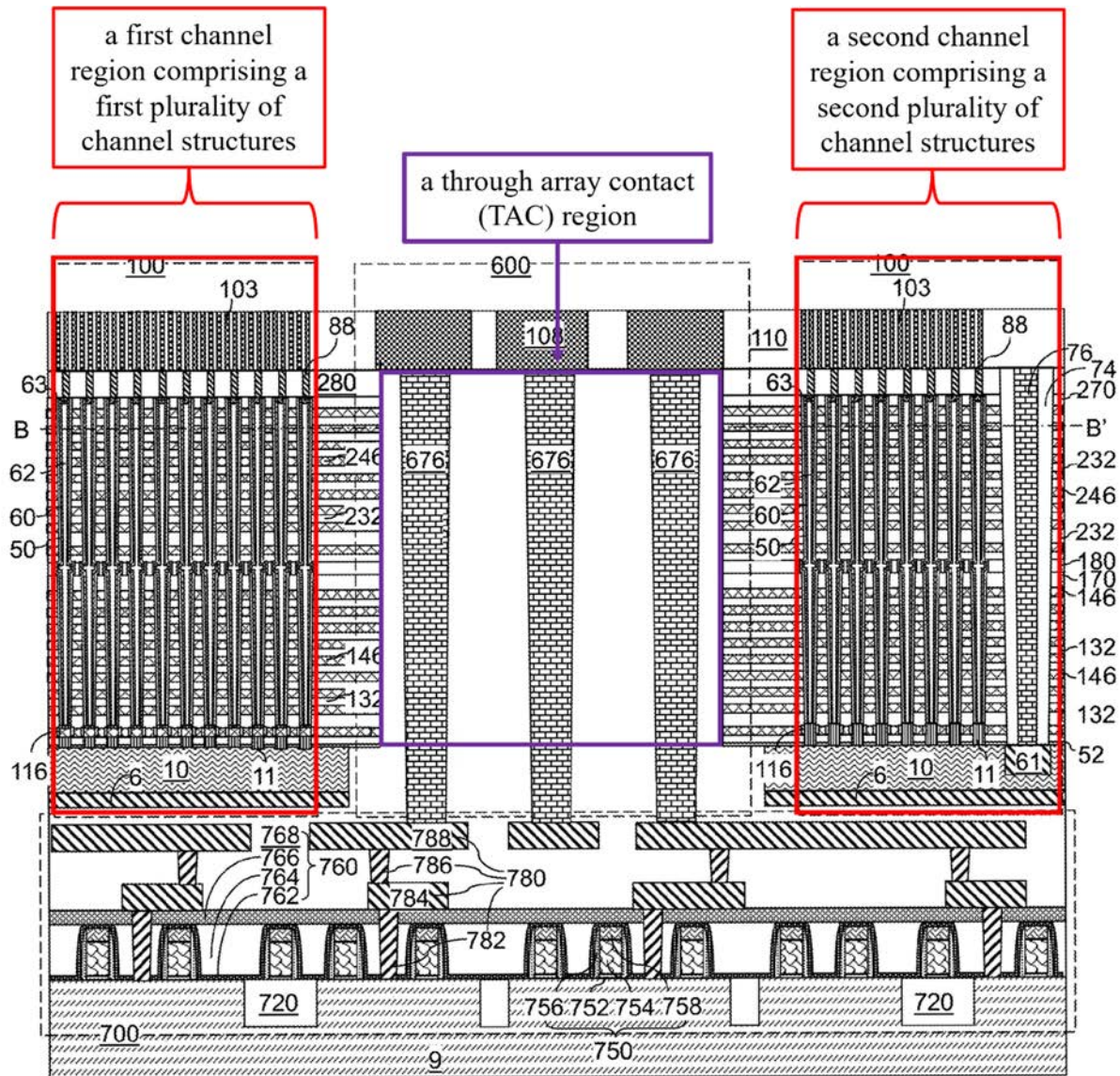


FIG. 49

Toyama, Fig. 49 (modified); Lee ¶ 250.

c. [8.G.iii]

As explained in Ground 1, above, Toyama’s Second Modification’s “through-memory-level via structures 676” are *through array contacts*. §IX.A.8.c (Ground 1, limitation [8.G.iii]). And, as explained above, the *dielectric structure* in the obviousness combination is a unitary dielectric fill material. §XI.B.3 (limitation

[8.B]). Thus, in the obviousness combination, the *TAC region* (part of “through-memory-level region 600”) *comprises a plurality of through array contacts* (TACs) (“through-memory-level via structures 676”) *extending vertically through the dielectric structure* (the unitary dielectric fill material):

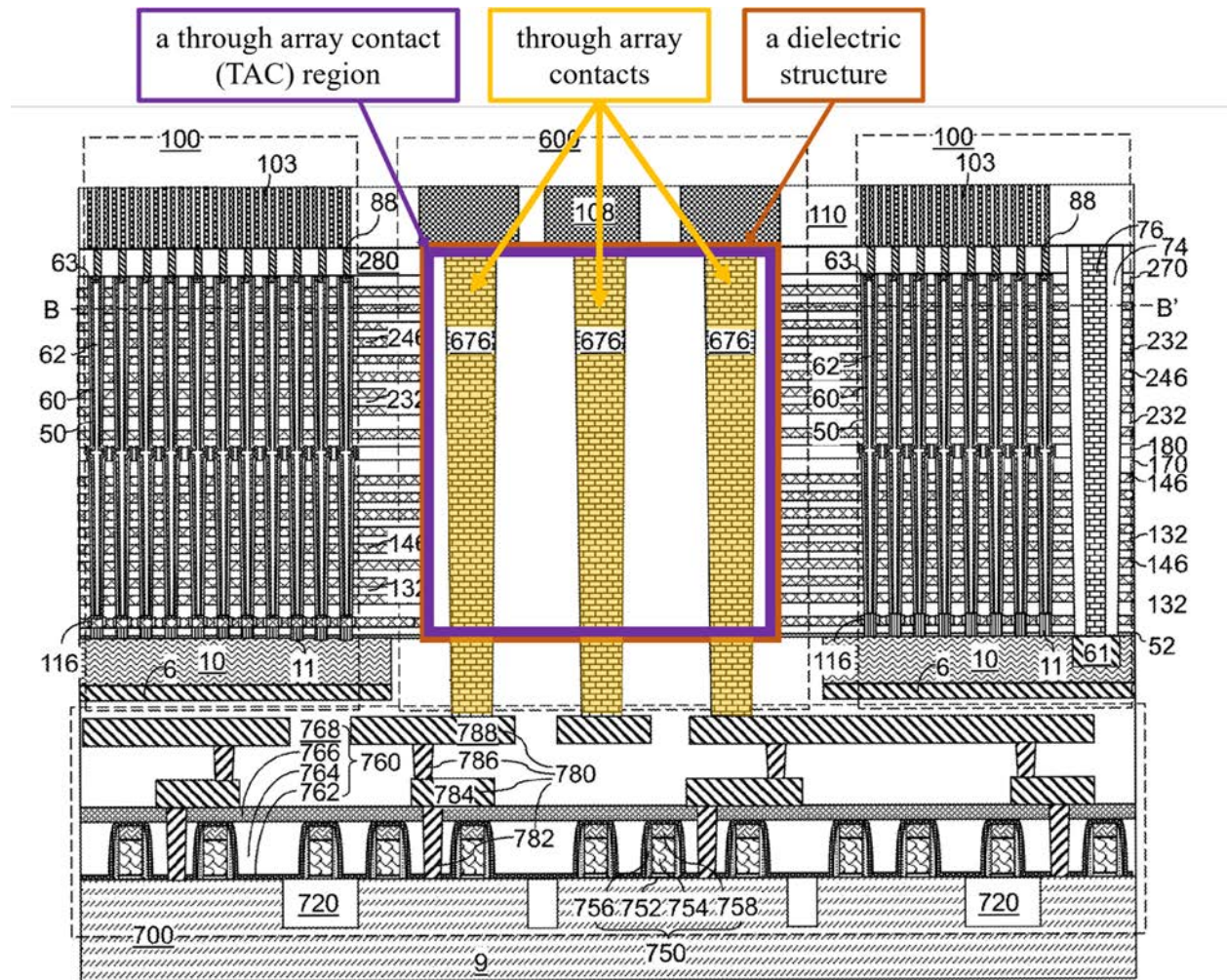
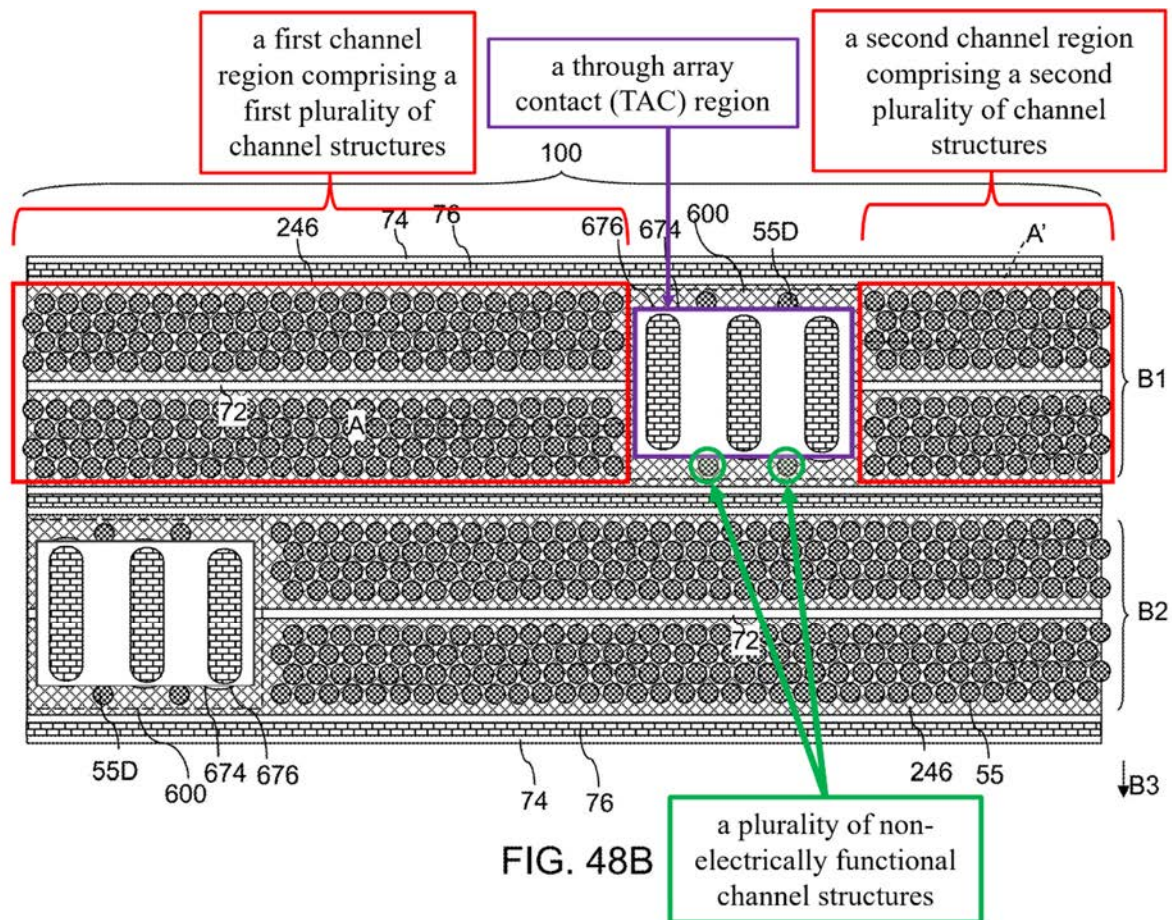


FIG. 49

Toyama, Fig. 49 (modified); Lee ¶ 248.

9. [8.H]

The obviousness combination does not alter the Second Modification’s “dummy memory stack structures 55D.” Toyama, Fig. 48B, §XI.A.2. Thus, for the reasons explained in Ground 1, the obviousness combination renders obvious *a plurality of non-electrically functional channel structures* (“dummy memory stack structures 55D”) *surrounding the TAC region* (part of “through-memory-level via region 600”) *and between the first and second channel regions* (first and second parts of “memory array region 100”):



Toyama, Fig. 48B (modified); Lee ¶ 251; §§IX.A.9 (Ground 1, limitation [8.H]), XI.B.8 (limitation [8.G]), XI.B.4 (limitation [8.C]).

C. Claim 10¹⁷

1. [10.Pre]

See §XI.B.1.

¹⁷ For the limitations of claim 10, which were already recited above for Ground 1, the Petition refers to the Listing of Challenged Claims.

2. [10.A]

Toyama discloses *a substrate* (“planar semiconductor material layer 10”) for the same reasons set forth in §IX.B.2. *See also* Toyama, [0211], Fig. 17A; Lee ¶ 252.

3. [10.B]

As explained in Ground 1, Toyama’s Second Modification discloses or renders obvious *an etch stop plug* (“drains region 63”) *interposed between each local contact of the local contacts* (“drain contact via structures 88”) *and each channel structure of the first and second channel structures* (“memory stack structures 55”). §IX.B.3.

The obviousness combination does not alter any of the foregoing components in the Second Modification. §XI.A.2. Thus, the obviousness combination renders this limitation obvious. Lee ¶ 253.

4. [10.C]

As explained in Ground 1, Toyama’s Second Modification discloses or renders obvious *an epitaxial layer* (“pedestal channel portions 11”) *disposed between the substrate* (“planar semiconductor material layer 10”) *and the first or second channel structures* (“memory stack structures 55”). §IX.B.4.

The obviousness combination does not alter any of the foregoing components in the Second Modification. §XI.A.2. Thus, the obviousness combination renders this limitation obvious. Lee ¶ 254.

XII. SECONDARY CONSIDERATIONS

There is no evidence in the prosecution history of this or any related application or patent that any arguments regarding secondary considerations exist. Lee ¶ 255. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,780 words.

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on May 20, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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