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Application Number: 16867404

Document Date: 05/05/2020

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UTILITY PATENT APPLICATION TRANSMITTAL <i>(Only for new nonprovisional applications under 37 CFR 1.53(b))</i>	Attorney Docket No.	4123.0190002
	First Named Inventor	Qian TAO
	Title	Through Array Contact (TAC) for Three-Dimensional Memory Devices
	Priority Mail Express® Label No.	

APPLICATION ELEMENTS <i>See MPEP chapter 600 concerning utility patent application contents.</i>	Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450
1. ☐ Fee Transmittal Form (PTO/SB/17 or equivalent) 2. ☐ Applicant asserts small entity status. See 37 CFR 1.27 3. ☐ Applicant certifies micro entity status. See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent. 4. ☒ Specification [Total Pages <u>36</u>] Both the claims and abstract must start on a new page. (See MPEP § 608.01(a) for information on the preferred arrangement) 5. ☒ Drawing(s) (35 U.S.C. 113) [Total Sheets <u>15</u>] 6. ☒ Inventor's Oath or Declaration [Total Pages <u>5</u>] (including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e)) a. ☐ Newly executed (original or copy) b. ☒ A copy from a prior application (37 CFR 1.63(d)) 7. ☒ Application Data Sheet * See note below. See 37 CFR 1.76 (PTO/AIA/14 or equivalent) 8. ☐ CD-ROM or CD-R in duplicate, large table, or Computer Program (Appendix) ☐ Landscape Table on CD 9. ☐ Nucleotide and/or Amino Acid Sequence Submission (if applicable, items a. – c. are required) a. ☐ Computer Readable Form (CRF) b. ☐ Specification Sequence Listing on: i. ☐ CD-ROM or CD-R (2 copies); or ii. ☐ Paper c. ☐ Statements verifying identity of above copies	ACCOMPANYING APPLICATION PAPERS 10. ☐ Assignment Papers (cover sheet & document(s)) Name of Assignee _____ Yangtze Memory Technologies Co., Ltd. 11. ☐ 37 CFR 3.73(c) Statement ☒ Power of Attorney (when there is an assignee) 12. ☐ English Translation Document (if applicable) 13. ☒ Information Disclosure Statement (PTO/SB/08 or PTO-1449) ☐ Copies of citations attached 14. ☐ Preliminary Amendment 15. ☐ Return Receipt Postcard (MPEP § 503) (Should be specifically itemized) 16. ☐ Certified Copy of Priority Document(s) (if foreign priority is claimed) 17. ☐ Nonpublication Request Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent. 18. ☒ Other: Authorization Under 37 C.F.R. § 1.136(a)(3) _____ _____ _____ _____

***Note:** (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
 (2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS					
☒ The address associated with Customer Number: <u>26111</u> OR ☐ Correspondence address below					
Name	Donald J. Featherstone				
Address					
City		State		Zip Code	
Country		Telephone		Email	
Signature	/Donald J. Featherstone/			Date	5/5/2020
Name (Print/Type)	Donald J. Featherstone			Registration No. (Attorney/Agent)	33,876

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: TAO *et al.*

Applicant: Yangtze Memory Technologies
Co., Ltd.

Application No.: *To Be Assigned*

(Continuation of Appl. No. 16/047,182;
Filed: July 27, 2018)

Filed: *Herewith*

Confirmation No.: *To Be Assigned*

Art Unit: *To Be Assigned*

Examiner: *To Be Assigned*

Atty. Docket: 4123.0190002

Title: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY
DEVICES**

**Authorization to Treat a Reply as Incorporating an
Extension of Time Under 37 C.F.R. § 1.136(a)(3)**

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

The U.S. Patent and Trademark Office is hereby authorized to treat any concurrent or future reply that requires a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. The U.S. Patent and Trademark Office is hereby authorized to charge all required extension of time fees to our Deposit Account No. 19-0036, if such fees are not otherwise provided for in such reply.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 5/5/2020

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Washington, D.C. 20005-3934
(202) 371-2600

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0190002
		Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Qian		TAO		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei	Country of Residence ⁱ	CN		
Mailing Address of Inventor:					
Address 1		Yangtze Memory Technologies Co., Ltd.			
Address 2		88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei	State/Province			
Postal Code		Country ⁱ	CN		
Inventor 2					Remove
Legal Name					
Prefix	Given Name	Middle Name	Family Name	Suffix	
	Yushi		HU		
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei	Country of Residence ⁱ	CN		
Mailing Address of Inventor:					
Address 1		Yangtze Memory Technologies Co., Ltd.			
Address 2		88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei	State/Province			
Postal Code		Country ⁱ	CN		
Inventor 3					Remove
Legal Name					

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0190002
		Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		

Prefix	Given Name	Middle Name	Family Name	Suffix
	Zhenyu		LU	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan, Hubei	Country of Residence ⁱ	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.			
Address 2	88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei	State/Province		
Postal Code		Country ⁱ	CN	

Inventor 4	Remove			
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Li Hong		XIAO	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan, Hubei	Country of Residence ⁱ	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.			
Address 2	88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei	State/Province		
Postal Code		Country ⁱ	CN	

Inventor 5	Remove			
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Xiaowang		DAI	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan, Hubei	Country of Residence ⁱ	CN	

Mailing Address of Inventor:

Address 1	Yangtze Memory Technologies Co., Ltd.			
Address 2	88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei	State/Province		
Postal Code		Country ⁱ	CN	

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0190002
		Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		

Inventor 6 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Yu Ting		ZHOU	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan, Hubei	Country of Residence ⁱ	CN	
Mailing Address of Inventor:				
Address 1		Yangtze Memory Technologies Co., Ltd.		
Address 2		88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	State/Province		
Postal Code		Country ⁱ	CN	
Inventor 7 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Zhao Hui		TANG	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan, Hubei	Country of Residence ⁱ	CN	
Mailing Address of Inventor:				
Address 1		Yangtze Memory Technologies Co., Ltd.		
Address 2		88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone		
City	Wuhan, Hubei	State/Province		
Postal Code		Country ⁱ	CN	
Inventor 8 Remove				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Mei Lan		GUO	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service				
City	Wuhan, Hubei	Country of Residence ⁱ	CN	
Mailing Address of Inventor:				
Address 1		Yangtze Memory Technologies Co., Ltd.		
Address 2		88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone		

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number		4123.0190002	
		Application Number			
Title of Invention		THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES			
City		Wuhan, Hubei		State/Province	
Postal Code				Country i	
				CN	
Inventor 9					Remove
Legal Name					
Prefix	Given Name	Middle Name		Family Name	Suffix
	ZhiWu			TANG	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei		Country of Residence i		CN
Mailing Address of Inventor:					
Address 1		Yangtze Memory Technologies Co., Ltd.			
Address 2		88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei		State/Province		
Postal Code				Country i	
				CN	
Inventor 10					Remove
Legal Name					
Prefix	Given Name	Middle Name		Family Name	Suffix
	Qinxiang			WEI	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei		Country of Residence i		CN
Mailing Address of Inventor:					
Address 1		Yangtze Memory Technologies Co., Ltd.			
Address 2		88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei		State/Province		
Postal Code				Country i	
				CN	
Inventor 11					Remove
Legal Name					
Prefix	Given Name	Middle Name		Family Name	Suffix
	Qianbing			XU	
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei		Country of Residence i		CN
Mailing Address of Inventor:					

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number		4123.0190002	
		Application Number			
Title of Invention		THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES			

Address 1		Yangtze Memory Technologies Co., Ltd.			
Address 2		88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei		State/Province		
Postal Code			Country i	CN	
Inventor 12					Remove
Legal Name					
Prefix	Given Name		Middle Name		Family Name
	Sha Sha				LIU
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei		Country of Residence i		CN
Mailing Address of Inventor:					
Address 1		Yangtze Memory Technologies Co., Ltd.			
Address 2		88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei		State/Province		
Postal Code			Country i	CN	
Inventor 13					Remove
Legal Name					
Prefix	Given Name		Middle Name		Family Name
	Jian Hua				SUN
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei		Country of Residence i		CN
Mailing Address of Inventor:					
Address 1		Yangtze Memory Technologies Co., Ltd.			
Address 2		88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone			
City	Wuhan, Hubei		State/Province		
Postal Code			Country i	CN	
Inventor 14					Remove
Legal Name					
Prefix	Given Name		Middle Name		Family Name
	EnBo				WANG
Residence Information (Select One) ☐ US Residency ☒ Non US Residency ☐ Active US Military Service					
City	Wuhan, Hubei		Country of Residence i		CN

Application Data Sheet 37 CFR 1.76		Attorney Docket Number		4123.0190002	
		Application Number			
Title of Invention		THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES			
Mailing Address of Inventor:					
Address 1		Yangtze Memory Technologies Co., Ltd.			
Address 2		88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone			
City		Wuhan, Hubei		State/Province	
Postal Code				Country i	
				CN	
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. 					

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number		26111	
Email Address		 	

Application Information:

Title of the Invention		THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES	
Attorney Docket Number		4123.0190002	
		Small Entity Status Claimed ☐	
Application Type		Nonprovisional	
Subject Matter		Utility	
Total Number of Drawing Sheets (if any)		15	
		Suggested Figure for Publication (if any)	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐ Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application has not and will not be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0190002
		Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	26111		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	16/047182	2018-07-27
Prior Application Status	Expired		
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
16/047182	Continuation of	PCT/CN2018/085421	2018-05-03
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)¹ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ¹	Filing Date (YYYY-MM-DD)	Access Code ¹ (if applicable)

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0190002
		Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0190002
		Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0190002
		Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.			
Applicant 1			
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.			
☒ Assignee		☐ Legal Representative under 35 U.S.C. 117	
		☐ Joint Inventor	
☐ Person to whom the inventor is obligated to assign.		☐ Person who shows sufficient proprietary interest	
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:			
Name of the Deceased or Legally Incapacitated Inventor:			
If the Applicant is an Organization check here. ☒			
Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Applicant:			
Address 1	88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone		
Address 2			
City	Wuhan, Hubei	State/Province	
Country	CN	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0190002
		Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		

Assignee 1			
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.			
If the Assignee or Non-Applicant Assignee is an Organization check here. ☒			
Organization Name	Yangtze Memory Technologies Co., Ltd.		
Mailing Address Information For Assignee including Non-Applicant Assignee:			
Address 1	88 Weilai 3rd Rd., East Lake High-Tech Dev. Zone		
Address 2			
City	Wuhan, Hubei	State/Province	
Country i	CN	Postal Code	
Phone Number		Fax Number	
Email Address			
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.			

Signature:

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This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

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Signature	/Donald J. Featherstone/		Date (YYYY-MM-DD)	2020-05-05	
First Name	Donald J.	Last Name	Featherstone	Registration Number	33,876
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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	4123.0190002
		Application Number	
Title of Invention	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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COMBINED DECLARATION AND ASSIGNMENT

DECLARATION

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application
number 16/047,182
- filed on July 27, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

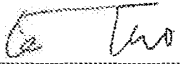
The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

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Atty. Docket No. 4123.0190001

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

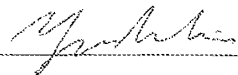
LEGAL NAME OF INVENTOR

Inventor: Qian TAO Date: 2018.9.12

Signature of Inventor: 

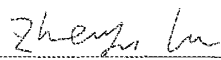
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Inventor: Yushi HU Date: 2018.9.12

Signature of Inventor: 

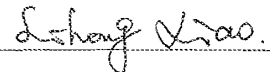
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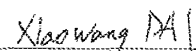
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Inventor: Xiaowang DAI Date: 2018.9.12

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Appl. No. 16/047,182
Atty. Docket No. 4123.0190O01

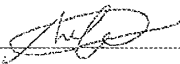
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Atty. Docket No. 4123.0190001

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Signature of Inventor: Jian Hua Sun

LEGAL NAME OF INVENTOR

Inventor: EnBo WANG Date: 2018.9.12

Signature of Inventor: Wang Enbo

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THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

CROSS-REFERENCES TO RELATED APPLICATIONS

[0001] This application is a continuation of U.S. Patent Application No. 16/047,182, titled “Through Array Contact (TAC) for Three-dimensional Memory Devices,” filed on July 27, 2018, which claims the priority of PCT Patent Application No. PCT/CN2018/085421 filed on May 3, 2018, both of which are incorporated herein by reference in their entireties.

TECHNICAL FIELD

[0002] The present disclosure generally relates to the field of semiconductor technology, and more particularly, to a channel hole plug structure of three-dimensional (3D) memory devices and a method for forming the same.

BACKGROUND

[0003] Planar memory cells have been continuously scaled down from one technology generation to the next by improvements in circuit design, fabrication integration, and fabrication process. However, as the feature sizes of the memory cells continuously shrink, the density for planar memory cells increases. Consequently, the fabrication techniques can become challenging and costly.

[0004] A three-dimensional (3D) memory architecture (e.g., planar memory cells stacked on top of each other) can address the density limitation of planar memory cells. The 3D memory architecture includes a memory array and peripheral devices for controlling signals to and from the memory array.

BRIEF SUMMARY

[0005] Embodiments of 3D memory and fabrication methods thereof are disclosed herein.

[0006] According to some embodiments of the present disclosure, a 3D NAND memory device includes an alternating layer stack with a staircase structure and one or more dielectric structures surrounded by the alternating layer stack. The alternating layer stack can include a stack of alternating conductor and dielectric layers, and the dielectric structures can include a single dielectric layer. The memory device further includes multiple vertical structures that extend

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vertically through the alternating conductor/dielectric stack, and multiple vertical structures that extend vertically through the dielectric structures. By way of example and not limitation, vertical structures extending vertically through the alternating conductor/dielectric stack can include “channel” structures and “slit” structures. Vertical structures extending vertically through the dielectric structures can include through array contact structures, referred to herein as “through array contacts” (“TAC” structures or “TACs”).

[0007] Additional elements of the 3D NAND memory device can include an etch stop layer disposed on each channel structure and a first contact layer with a plurality of first contacts. For example, each of the first contacts can be formed to physically connect to a respective conductor layer from each alternating conductor/dielectric stack in the staircase structure, a respective etch stop layer of the channel structures, and a respective slit structure.

[0008] In some embodiments, the etch stop layer includes polysilicon (e.g., polycrystalline silicon or “poly”), titanium (Ti), titanium nitride (TiN), tungsten (W), or combinations thereof. Further each of the plurality of conductor/dielectric layer pairs can include a metal and a silicon oxide (SiO₂) layer. The aforementioned materials are exemplary and are not limiting. As such, other appropriate materials can be used.

[0009] In some embodiments, the memory device includes dummy (e.g., electrically non-functional) channel structures extending vertically through the alternating conductor/dielectric stack.

[0010] In some embodiments, the memory device includes a second contact layer over the first contact layer and a third contact layer over the second contact layer. The second and third contact layers include respective second and third contacts. Some contacts of the third contact layer, via the respective second and first contacts, are electrically connected to the conductor layers from the alternating conductor/dielectric stack in the staircase structure, and to the channel and slit structures. In some embodiments, the first, second and third contact layers form an interconnect network for the 3D NAND memory device. The interconnect network can be used to transfer electrical signals between the various components of the 3D NAND memory device.

[0011] According to some embodiments of the present disclosure, a method for forming a 3D NAND memory device is disclosed herein. For example, an alternating dielectric stack can be formed over a substrate. The alternating dielectric stack can include a plurality of dielectric layer pairs, where each pair includes a first dielectric layer and a second dielectric layer different from

the first dielectric layer. A first staircase structure can be subsequently formed in the alternating dielectric stack. Subsequently, channel structures and a dielectric structure—each extending vertically through the alternating dielectric stack—are formed.

[0012] In some embodiments, the dielectric material of the dielectric structure can be the same as the material of the second dielectric layer in the alternating dielectric stack. A sacrificial etch stop layer can be disposed on each channel structure. Slit openings extending through the alternating dielectric stack are subsequently formed and the first dielectric layers of the alternating dielectric stack are replaced with conductor layers through the slit openings to form a plurality of conductor/dielectric layer pairs. The slit openings are then filled with a conductor material. Further, a first contact layer with a plurality of first contacts can be formed so that each first conductor layer from the alternating conductor/dielectric stack in the first staircase structure is connected to a first contact. Additionally, each channel and slit structure can also be connected to a respective first contact of the first contact layer. In some embodiments, and prior to the formation of the first contact layer, the sacrificial etch stop layer over each channel structure can be replaced with a “permanent” etch stop layer.

[0013] In some embodiments, TAC openings are etched through the dielectric structure and subsequently filled with a metal to form respective TAC structures that extend through the dielectric structure and a portion of the substrate. In some embodiments, TAC structures are part of the first contact layer. In other words, the TAC structures can be formed concurrently with the first contact layer.

[0014] In some embodiments, a second contact layer with a plurality of second contacts can be formed over the first contact layer. Second contacts can be connected to respective first contacts of the first contact layer.

[0015] In some embodiments, a third contact layer with a plurality of third contacts can be formed over the second contact layer. The third contact layer, via the respective second and first contact layers, can electrically connect to the various components of the memory device including the first conductor layers of the alternating conductor/dielectric stack in the first staircase structure, the channel structures, and the slit structures.

[0016] In some embodiments, prior to forming the slit structure, a doped region can be formed in the substrate. The slit structure can be in contact with the doped region.

[0017] In some embodiments, the permanent etch stop layer includes one or more of polysilicon, titanium, titanium nitride, and tungsten. The dielectric structure can include silicon oxide. Each of the plurality of dielectric layer pairs can include a silicon oxide layer and a silicon nitride layer. Each of the plurality of conductor/dielectric layer pairs can include a metal layer and a silicon oxide layer.

[0018] Further features and advantages of the invention, as well as the structure and operation of various embodiments of the invention, are described in detail below with reference to the accompanying drawings. It is noted that the invention is not limited to the specific embodiments described herein. Such embodiments are presented herein for illustrative purposes only. Additional embodiments will be apparent to persons skilled in the relevant art(s) based on the teachings contained herein.

BRIEF DESCRIPTION OF THE DRAWINGS

[0019] The accompanying drawings, which are incorporated herein and form a part of the specification, illustrate embodiments of the present disclosure and, together with the description, further serve to explain the principles of the present disclosure and to enable a person skilled in the pertinent art to make and use the present disclosure.

[0020] FIGs. 1A-1C illustrate various regions of a 3D memory device in the plan-view, according to some embodiments of the present disclosure.

[0021] FIG. 2 illustrates a cross-section of a 3D memory device, according to some embodiments of the present disclosure.

[0022] FIG. 3 is a flowchart of an exemplary method for forming a 3D memory device, according to some embodiments of the present disclosure.

[0023] FIGs. 4–13 illustrate an exemplary fabrication process for forming a 3D memory device, according to some embodiments of the present disclosure.

[0024] The features and advantages of the present disclosure will become more apparent from the detailed description set forth below when taken in conjunction with the drawings, in which like reference characters identify corresponding elements throughout. In the drawings, like reference numbers generally indicate identical, functionally similar, and/or structurally similar elements. Additionally, generally, the left-most digit(s) of a reference number identifies the

drawing in which the reference number first appears. Unless otherwise indicated, the drawings provided throughout the disclosure should not be interpreted as to-scale drawings.

DETAILED DESCRIPTION

[0025] Although specific configurations and arrangements are discussed, it should be understood that this is done for illustrative purposes only. A person skilled in the art will recognize that other configurations and arrangements can be used without departing from the spirit and scope of the present disclosure. It will be apparent to a person skilled in the art that the present disclosure can also be employed in a variety of other applications.

[0026] It is noted that references in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” “some embodiments,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic, but every embodiment may not necessarily include the particular feature, structure, or characteristic. Moreover, such phrases do not necessarily refer to the same embodiment. Further, when a particular feature, structure or characteristic is described in connection with an embodiment, it would be within the knowledge of a person skilled in the art to affect such feature, structure or characteristic in connection with other embodiments whether or not explicitly described.

[0027] In general, terminology may be understood at least in part from usage in context. For example, the term “one or more” as used herein, depending at least in part upon context, may be used to describe any feature, structure, or characteristic in a singular sense or may be used to describe combinations of features, structures or characteristics in a plural sense. Similarly, terms, such as “a,” “an,” or “the,” again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context.

[0028] It should be readily understood that the meaning of “on,” “above,” and “over” in the present disclosure should be interpreted in the broadest manner such that “on” not only means “directly on” something but also includes the meaning of “on” something with an intermediate feature or a layer therebetween, and that “above” or “over” not only means the meaning of “above” or “over” something but can also include the meaning it is “above” or “over” something with no intermediate feature or layer therebetween (i.e., directly on something).

[0029] Further, spatially relative terms, such as “beneath,” “below,” “lower,” “above,” “upper,” and the like, may be used herein for ease of description to describe one element or feature’s relationship to another element(s) or feature(s) as illustrated in the figures. The spatially

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relative terms are intended to encompass different orientations of the device in use or operation in addition to the orientation depicted in the figures. The apparatus may be otherwise oriented (rotated 90 degrees or at other orientations) and the spatially relative descriptors used herein may likewise be interpreted accordingly.

[0030] As used herein, the term “substrate” refers to a material onto which subsequent material layers are added, or otherwise “disposed.” The substrate itself can be patterned. Materials disposed on (e.g., on top) the substrate can be patterned or can remain unpatterned. Furthermore, the substrate can include a wide array of semiconductor materials, such as silicon, germanium, gallium arsenide, indium phosphide, etc. Alternatively, the substrate can be made from an electrically non-conductive material, such as a glass, a plastic, or a sapphire wafer.

[0031] As used herein, the term “layer” refers to a material portion including a region with a thickness. A layer can extend over the entirety of an underlying or overlying structure, or may have an extent less than the extent of an underlying or overlying structure. Further, a layer can be a region of a homogeneous or inhomogeneous continuous structure that has a thickness less than the thickness of the continuous structure. For example, a layer can be located between any pair of horizontal planes between, or at, a top surface and a bottom surface of the continuous structure. As used herein, the term “top surface” or “front side” of a structure, a layer, or an element refers to a surface where subsequent elements or structures can be formed thereon. Conversely, as used herein, the term “bottom surface” or “backside” refers to the side of the structure, layer, or element that is opposite to the top surface. It is noted that the terms “top surface” or “front side” and “bottom surface” or “backside” are used merely for description purposes and not to limit the orientation of the elements, layers, or structures. A layer can extend horizontally, vertically, and/or along a tapered surface. A substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow. A layer can include multiple layers. For example, an interconnect layer can include one or more conductor and contact layers (in which contacts, interconnect lines, and/or vias are formed) and one or more dielectric layers.

[0032] As used herein, the term “nominal/nominally” refers to a desired, or target, value of a characteristic or parameter for a component or a process operation, set during the design phase of a product or a process, together with a range of values above and/or below the desired value. The range of values can be due to slight variations in manufacturing processes or tolerances. As used herein, the term “about” indicates the value of a given quantity that can vary based on a particular

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technology node associated with the subject semiconductor device. Based on the particular technology node, the term “about” can indicate a value of a given quantity that varies within, for example, 10–30% of the value (e.g., $\pm 10\%$, $\pm 20\%$, or $\pm 30\%$ of the value).

[0033] As used herein, the term “3D memory device” refers to a semiconductor device with vertically-oriented strings of memory cell transistors (referred to herein as “memory strings,” such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate. As used herein, the term “vertical/vertically” means nominally perpendicular to the lateral surface of a substrate.

[0034] Various embodiments in accordance with the present disclosure provide a 3D memory device with interconnect structures for a memory array (also referred to herein as an “array device”). The interconnect structures allow contacts to various memory array structures (e.g., NAND strings, gate line slits, word lines, etc.) to be fabricated in a limited number of steps (e.g., in a single step or in two steps), thereby reducing the process complexity and manufacturing cost. In some embodiments, the interconnect structures disclosed herein include bit lines in the top interconnect layer, which are suitable for those 3D memory architectures where the array device and a peripheral device are formed on different substrates and are subsequently joined by hybrid bonding in a “face-to-face” configuration.

[0035] Moreover, the interconnect structures disclosed herein can include TAC structures for providing vertical interconnects between the stacked array device and a peripheral device (e.g., for power bus and metal routing), thereby reducing metal levels and shrinking die size. In some embodiments, the TAC structures, as part of the interconnect structures, are formed within “single-material” dielectric structures (e.g., dielectric structures that are made of a single dielectric as opposed to a stack of alternating dielectric layers). According to some embodiment, forming TAC structures in a single-material dielectric structure is advantageous compared to the formation of TAC structures in a stack of alternating dielectric layers in terms of etching capability and cost.

[0036] According to some embodiments, FIGs. 1A-1C are plan-views of various exemplary regions of a 3D memory device along a bit line (BL) and a word line (WL) direction as denoted by respective axes labeled BL and WL. For example, FIG. 1A is a plan-view of an exemplary WL TAC region 102 of the 3D memory device. TAC region 102 includes NAND string regions 110, a TAC region 120, and top selective gate (TSG) staircase regions 130. NAND string regions

110 can include an array of NAND strings 112, each including a plurality of stacked memory cells. TSG staircase regions 130 can be disposed on the sides of NAND string regions 110 and adjacent to TAC region 120 in the plan-view. TSG staircase regions 130 can include an array of TSG contacts 132 formed on a staircase structure having two levels or more. TSG contacts 132 can be electrically connected to the top selective gates of NAND strings 112 in NAND string region 110 through a network of interconnect contacts not shown in FIG. 1A.

[0037] In some embodiments, TAC region 120 is between two TSG staircase regions 130 in the WL direction of the 3D memory device. TAC region 120 can be defined by a single-material dielectric structure 124. Multiple TAC structures 126 can be formed within TAC region 120 in dielectric structure 124. In some embodiments, dummy (e.g., non-electrically functional) channel structures 122 are formed outside TAC region 120 to provide mechanical support to the memory array structures. By way of example and not limitation, dummy channel structures 122 can be formed in any regions outside TAC region 120, for example, along the edges of NAND string regions 110 adjacent to TSG staircase regions 130. As shown in FIG. 1A, WL TAC region 102 can also include a plurality of slit structures 114 with each extending in the WL direction. At least some slit structures 114 can function as the common source contact for an array of NAND strings 112 in NAND string regions 110. According to some embodiments, slit structures 114 can divide the 3D memory device into multiple memory blocks.

[0038] FIG. 1B is a plan-view of an exemplary bit line (BL) TAC region 104 of the 3D memory device, including NAND string regions 110 and a TAC region 120. NAND string regions 110 can include an array of NAND strings 112, each including a plurality of stacked memory cells. In some embodiments, TAC region 120 is disposed between two NAND string regions 110 in the bit line direction of the 3D memory device (labeled as “BL” in FIGs. 1A-1C). TAC region 120 can be defined by a single-material dielectric structure 124. More than one TAC structures 126 can be formed in TAC region 120 within dielectric structure 124, as shown in FIG. 1B. Further, BL TAC region 104 can also include slit structures 114 with each extending in the WL direction. At least some slit structures 114 can function as the common source contact for an array of NAND strings 112 in NAND string regions 110. Slit structures 114 can also divide the 3D memory device into multiple memory blocks. In some embodiments, dummy (e.g., non-electrically functional) channel structures 122 are formed in part of NAND string regions 110, for example, in the memory areas that are adjacent to TAC region 120 in the bit line direction.

[0039] FIG. 1C is a plan-view of an exemplary staircase TAC region 106 of the 3D memory device, including a NAND string region 110, a staircase region 140, and a TAC region 120. NAND string region 110 can include an array of NAND strings 112, each including a plurality of stacked memory cells. Staircase region 140 can include a staircase structure and an array of WL contacts 142 formed on the staircase structure. In some embodiments, TAC region 120 can be formed in staircase region 140. TAC region 120 is defined by the single-material dielectric structure 124. Multiple TAC structures 126 can be formed within TAC region 120 in single-material dielectric structure 124. As shown in FIG. 1C, staircase TAC region 106 can also include slit structures 114 with each extending in the WL direction. At least some slit structures 114 can function as the common source contact for an array of NAND strings 112 in NAND string region 110. Slit structures 114 can also divide the memory device into multiple memory blocks. In some embodiments, dummy (e.g., non-electrically functional) channel structures are formed in staircase region 140 outside TAC region 120 (not shown in FIG. 1C).

[0040] FIG. 2 is a cross-sectional view of an exemplary 3D memory device 200, according to some embodiments of the present disclosure. 3D memory device 200 can include a substrate 202. Substrate 202 can include single crystalline silicon (Si) or another elementary semiconductor such as, for example, (i) germanium (Ge); (ii) a compound semiconductor including silicon germanium (SiGe), silicon carbide (SiC), gallium arsenide (GaAs), gallium phosphide (GaP), indium phosphide (InP), indium arsenide (InAs), and/or indium antimonide (InSb); (iii) an alloy semiconductor including gallium arsenide phosphide (GaAsP), aluminum indium arsenide (AlInAs), aluminum gallium arsenide (AlGaAs), gallium indium arsenide (GaInAs), gallium indium phosphide (GaInP), and/or gallium indium arsenide phosphide (GaInAsP); or (iv) combinations thereof. Further, substrate 202 can be a “semiconductor-on-insulator” wafer, such as silicon on insulator (SOI) or germanium on insulator (GOI). For example purposes, substrate 202 will be described in the context of single crystalline Si (e.g., a Si wafer). Based on the disclosure herein, other materials, as discussed above, can be used. These materials are within the spirit and scope of this disclosure. In some embodiments, substrate 202 can be a thinned substrate, which was thinned by means of grinding, wet and/or dry etching, chemical mechanical planarization (CMP), or a combination thereof.

[0041] 3D memory device 200 can include an array device above substrate 202 (on a top surface of substrate 202). It is noted that x, y, and z axes are added in FIG. 2 to further illustrate the spatial relationship between the various components in 3D memory device 200. Substrate 202

includes two lateral surfaces (e.g., a top surface and a bottom surface) extending laterally in the x-direction (the lateral direction) and y-direction. As used herein, whether one component (e.g., a layer or a device) is “on,” “above,” or “below” another component (e.g., a layer or a device) of a semiconductor device (e.g., 3D memory device 200) is determined relative to substrate 202 in the z-direction (the vertical direction) when the substrate is positioned in the lowest plane of the semiconductor device in the z-direction. The same notion for describing spatial relationship is applied throughout the present disclosure. Further, the y-direction is pointing into the page of FIG. 2.

[0042] By way of example and not limitation, 3D memory device 200 can be part of a non-monolithic 3D memory device, in which components (e.g., the peripheral device and array device) can be fabricated independently on different substrates and then bonded in a “face-to-face” configuration. In some embodiments, the array device substrate (e.g., substrate 202) remains as the substrate of the bonded non-monolithic 3D memory device, and the peripheral device (e.g., any suitable digital, analog, and/or mixed-signal peripheral circuits used for facilitating the operation of 3D memory device 200, such as page buffers, decoders, and latches; not shown in FIG. 2) is positioned so that it faces the 3D memory device 200 prior to hybrid bonding. Alternatively, in some embodiments, 3D memory device 200 is positioned so that it faces the peripheral device (not shown in FIG. 2 merely for clarity) prior to hybrid bonding. The array device substrate (e.g., substrate 202) can be a thinned substrate and the back-end-of-line (BEOL) interconnects of the non-monolithic 3D memory device can be formed on the backside (e.g. bottom surface) of the thinned array device substrate 202.

[0043] In some embodiments, 3D memory device 200 can be part of a non-monolithic 3D memory device regardless of its relative position (e.g. above or below) with respect to the peripheral device. For ease of reference, FIG. 2 depicts a state of 3D memory device 200 in which substrate 202 (the array device substrate) is positioned below the array device in the x-y plane, regardless of whether substrate 202 is the substrate of the non-monolithic 3D memory device or a thinned substrate on which the BEOL interconnect layers of the non-monolithic 3D memory device are formed.

[0044] In some embodiments, 3D memory device 200 is a NAND Flash memory device in which memory cells are provided in the form of an array of NAND strings 204 extending vertically above substrate 202. The array device can include a plurality of NAND strings 204 that extend through a plurality of conductor layer 206 and dielectric layer 208 pairs. The plurality of

conductor/dielectric layer pairs are also referred to herein as “alternating conductor/dielectric stack” 210. In some embodiments, the number of the conductor/dielectric layer pairs in alternating conductor/dielectric stack 210 (e.g., 32, 64, or 96) defines the number of memory cells in 3D memory device 200. Conductor layers 206 and dielectric layers 208 in alternating conductor/dielectric stack 210 alternate in the vertical direction (e.g., along the z-axis). In other words, except the layers at the top or bottom of alternating conductor/dielectric stack 210, each conductor layer 206 can be adjoined by two dielectric layers 208 on both sides, or each dielectric layer 208 can be adjoined by two conductor layers 206 on both sides. Conductor layers 206 can each have the same thickness or different thicknesses. Similarly, dielectric layers 208 can each have the same thickness or different thicknesses. By way of example and not limitation, the thickness of each conductor layer 206 can range from about 25 nm to about 40 nm, and the thickness of each dielectric layer 208 can range from about 20 nm to about 35 nm.

[0045] By way of example and not limitation, conductor layers 206 can include conductive materials such as tungsten (W), cobalt (Co), copper (Cu), aluminum (Al), doped polycrystalline Si (polysilicon), doped single crystalline Si, silicides, or any combination thereof. Dielectric layers 208 can include dielectric materials including, but not limited to, silicon oxide (Si_xO_y , thereafter “ SiO_2 ”), silicon nitride (Si_xN_y , thereafter “ SiN ”), silicon oxynitride (SiON), or any combination thereof. In some embodiments, conductor layers 206 include metal layers, such as W, and dielectric layers 208 include SiO_2 .

[0046] As shown in FIG. 2, at least on one side in the lateral direction (e.g., along the x-axis), alternating conductor/dielectric stack 210 can include a staircase structure 212. Each “level” or “step” 214 of staircase structure 212 can include one or more conductor/dielectric layer pairs on stacked top of each other. Each conductor/dielectric layer pair includes a conductor layer 206 and dielectric layer 208 respectively. The top layer in each level 214 of staircase structure 212 is a conductor layer 206 available for interconnection in the vertical direction (e.g., along the z-axis). In some embodiments, levels 214 in staircase structure 212 have the same height. Further, adjacent levels 214 of staircase structure 212 are being offset with one another by a nominally same distance in the x-direction. More specifically, for each two adjacent levels 214 of staircase structure 212, the first level that is closer to substrate 202 can extend laterally further than the second level, thereby forming a “landing area” or a “connection point” on the first level for interconnection in the vertical direction (e.g., along the z-axis).

[0047] As shown in FIG. 2, each NAND string 204 includes a channel structure 216 that extends through alternating conductor/dielectric stack 210. Channel structure 216 is filled with semiconductor materials (e.g., as a semiconductor channel 218) and dielectric materials (e.g., as a memory film 220). In some embodiments, semiconductor channel 218 includes Si, such as amorphous Si, polysilicon, single crystalline Si, etc. In some embodiments, memory film 220 is a composite stack of layers that includes a tunneling layer, a storage layer (also known as “charge trap/storage layer”), and a blocking layer. Each NAND string 204 can have a cylindrical shape (e.g., a pillar shape). Semiconductor channel 218, the tunneling layer, the storage layer, and the blocking layer are arranged along a direction from the center toward the outer surface of the pillar in this order, according to some embodiments. The tunneling layer can include SiO₂, SiN, or any combination thereof. The storage layer can include SiN, SiON, silicon, or any combination thereof. The blocking layer can include SiO₂, SiN, high dielectric constant (high-k) dielectrics (e.g., with a dielectric constant greater than 3.9), or any combination thereof.

[0048] In some embodiments, NAND strings 204 include a plurality of control gates (each being part of a WL). Conductor layer 206 in alternating conductor/dielectric stack 210 can act as the control gate for memory cells in NAND strings 204. Additionally, each conductor layer 206 can act as the control gate for multiple NAND strings 204 that can extend laterally (e.g., along the x-y plane) as a WL ending in staircase structure 212.

[0049] In some embodiments, each NAND string 204 includes an epitaxial layer 222 and an etch stop plug 224 at the respective bottom and top of NAND string 204, as shown in FIG. 2. For each NAND string 204, epitaxial layer 222 is referred to herein as an “epitaxial plug.” Each of epitaxial plug 222 and etch stop plug 224 can be in contact with a respective end of channel structure 216. Epitaxial plug 222 can include, for example, a semiconductor material (e.g., single crystalline Si) that is epitaxially grown from substrate 202. Etch stop plug 224 can include semiconductor materials (e.g., polysilicon) or conductor materials (e.g., metals). In some embodiments, etch stop plug 224 includes an opening filled with a titanium/titanium nitride stack (barrier and adhesion layer) and W (conductor). As the name suggests, etch stop plug 224 is an etch stop layer that prevents etching of dielectrics in channel structure 216, such as SiO₂ and SiN, during subsequent etch operations. In some embodiments, etch stop plug 224 acts as the drain of NAND string 204.

[0050] In some embodiments, the array device further includes slit structures 226. Each slit structure 226 can extend vertically (e.g., along the z-axis) through alternating

conductor/dielectric stack 210. Slit structures 226 also extend along the y-axis to separate alternating conductor/dielectric stack 210 into multiple blocks as discussed earlier for FIGs 1A-1C. Slit structures 226 are filled with conductor materials including, but not limited to, W, Co, Cu, Al, a silicide, or any combination thereof. Slit structures 226 further include a dielectric layer interposed between the conductor in slit structure 226 and alternating conductor/dielectric stack 210 to electrically insulate the conductor materials in the slit structure from the surrounding conductor layers in alternating conductor/dielectric stack 210. In some embodiments, slit structure 226 acts as the source contact for NAND strings 204 located in the same memory block. Consequently, a slit structure 226 can function as the “common source contact” of multiple NAND strings 204 within a memory block.

[0051] In some embodiments, substrate 202 includes doped regions 228 with p-type or n-type dopants at a desired doping level. Each doped region 228 is in contact with a respective slit structure 226, as shown in FIG. 2. In some embodiments, slit structures 226 are electrically coupled to NAND strings 204 through doped regions 228.

[0052] It has to be noted that NAND strings 204 and slit structures 226 are partially formed in a dielectric layer 230 that is disposed over alternating conductor/dielectric stack 210. In some embodiments, dielectric layer 230 can be a layer stack made of a single dielectric material—as opposed to being a stack of alternating dielectric layers. By way of example and not limitation, dielectric layer 230 is an oxide layer, such as SiO₂. In other words, dielectric layer 230 can be the same as dielectric layer 208. Further, and as shown in FIG. 2, dielectric layer 230 can extend over staircase structure 212.

[0053] As shown in FIG. 2, dielectric conductor/dielectric stack 210 is “disrupted” by single-material dielectric structure 232 (hereafter “dielectric structure 232”) along the x-direction (and along the y-direction—not shown from FIG.2). In some embodiments, dielectric structure 232 defines the boundaries, the shape, and the size of TAC region 120 (e.g., shown in FIGS. 1A-1C). Consequently, as shown in the plan-views of FIGS. 1A-1C, dielectric structure 232 can be surrounded by conductor/dielectric stack 210. Further, dielectric structure 232 can extend in the x-y plane and be coplanar with dielectric layer 230 (e.g., the top surfaces of dielectric structure 232 and dielectric layer 230 are flushed). In some embodiments, dielectric structure 232 is formed so that it is aligned to or covers at least a portion of an underlying isolation structure or region 233 (hereafter “shallow trench isolation (STI) structure 233”). Please note that, STI structure 233 is exemplary and is not limiting. As such, other isolation structures can be used.

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Further, dielectric structure 232 is in contact with STI structure 233. By way of example and not limitation, STI structure 233 is formed on a top portion of substrate 202 and is filled with a dielectric material, including but not limited to SiO₂, for example. In some embodiments, the footprint of dielectric structure 232 is smaller or equal to the footprint of STI structure 233. For example, in some embodiments, dielectric structure 232 can cover only portion of STI structure 233.

[0054] In some embodiments, dielectric structure 232 includes the same material with dielectric layer 230, and/or dielectric layer 208. For example, dielectric structure 232 can include SiO₂. However, this is not limiting and therefore dielectric structure 232 can include a different material than dielectric layer 208 or dielectric layer 230. In some embodiments, dielectric structure 232 can have different shapes. For example, as shown in the plan-views of FIGS. 1A-1C, TAC region 120 can have a rectangle or square shape. However, these shapes are not limiting and dielectric structures 232 can have any shape according to a design layout. Further, multiple dielectric structures, like dielectric structure 232, are possible across substrate 202.

[0055] As shown in FIG. 2, 3D memory device 200 further includes TACs 234, which extend vertically through dielectric structure 232. According to some embodiments, etching through dielectric structure 232 can be advantageous (e.g., involve fewer etch operations) compared to etching through a stack of alternating layers having the same overall thickness. For example, the formation of TACs 234 in an alternating layer stack with a thickness of about 6 μm or more (e.g., for a 64 tier 3D memory device) requires multiple etch and fill operations—therefore, increases the fabrication cost. Each TAC 234 can extend through the entire thickness of dielectric structure 232 and extend through at least a portion of STI structure 233 in substrate 202.

[0056] TACs 234 can carry electrical signals from and/or to 3D memory device 200, such as part of the power bus, with shorten interconnect routing. In some embodiments, TACs 234 can provide electrical connections between 3D memory device 200 and the peripheral device (e.g., on a CMOS chip; not shown in FIG. 2) and/or between BEOL interconnects (not shown in FIG. 2) and the peripheral device. Each TAC 234 is filled with conductor materials, including, but not limited to, W, Co, Cu, Al, doped Si, silicides, or any combination thereof. Since TACs 234 are embedded in dielectric structure 232, additional layers of dielectric are not required to insulate the conductor material.

[0057] In some embodiments, 3D memory device 200 includes a plurality of “local contacts” in physical and electrical contact with the various memory array structures disclosed herein, such as NAND strings 204, slit structures 226, and conductor layers or WL 206 in staircase structure 212. The contacts are referred to herein as “local contacts” because they are in direct contact with the memory array structures, and further because they are formed within dielectric layer 230. As shown in FIG. 2, local contacts can include NAND string contacts 236, slit structure contacts 238, and WL contacts 240. In some embodiments, TACs 234 are also considered local contacts. As used herein, the term “contact” can broadly include any suitable types of interconnects including vertical interconnect access (via) lines and lateral lines (interconnect lines).

[0058] In some embodiments, each local contact is coplanar with one another, e.g., on the top surface of a dielectric layer 230 (and dielectric structure 232 for TACs 234) in which the local contacts are formed. The lower end of each local contact can be in direct contact with the respective memory array structure. For example, the lower end of NAND string contact 236 can be in contact with etch stop plug 224 of NAND string 204, and the lower end of slit structure contact 238 can be in contact with the upper end of slit structure 226. The lower end of each WL contact 240 can be in contact with top conductor layer or WL 206 in a respective level of staircase structure 212. Each local contact is filled with conductor materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. Some or all of the local contacts can be formed simultaneously in a single contact forming process as described below in detail.

[0059] As shown in FIG. 2, in addition to the local contacts, 3D memory device 200 can further include a contact layer 242 and an interconnect layer 244 as part of its interconnect structures. Contact layer 242 can include a dielectric layer and a plurality of contacts 246 (e.g., vias) in the dielectric layer. Interconnect layer 244 can be formed on contact layer 242 and can include another dielectric layer and a plurality of interconnect contacts 248 (e.g., interconnect lines) in the dielectric layer. The local contacts, contacts 246 in contact layer 242, and interconnect contacts 248 in interconnect layer 244 can be collectively referred to herein as the interconnect structures of 3D memory device 200.

[0060] In some embodiments, each contact 246 can be filled with conductor materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. All contacts 246 can be formed simultaneously in a single contact forming process as described below in detail.

[0061] In some embodiments, each interconnect contact 248 can be filled with conductor materials including, but not limited to, W, Co, Cu, Al, silicides, or any combination thereof. All interconnect contacts 248 can be formed simultaneously in a single contact formation process as described below in detail.

[0062] In some embodiments, interconnect contacts 248 in interconnect layer 244 can include bit lines 250, which are electrically connected to NAND strings 204, respectively, by corresponding contacts 246 and NAND string contacts 236. Bit lines 250 can be used to individually address a corresponding NAND string 204. Interconnect contacts 248 can further include source lines that are electrically connected to slit structures 226 (source contacts). Further, interconnect lines can be electrically connected to TACs 234 and to WL 206 in staircase structure 212 through respective contacts 246 and WL contacts 240. It is to be understood that the number of interconnect layers in 3D memory device 200 is not limited by the example in FIG. 2. Additional interconnect layer(s) with contacts can be formed to provide an interconnect network of structures for 3D memory device 200.

[0063] FIG. 3 is a flowchart of an exemplary method 300 for forming a 3D memory device similar to 3D memory device 200, according to some embodiments of the present disclosure. FIGs. 4-13 will be used to describe the exemplary fabrication process for forming a 3D memory device using method 300. By way of example and not limitation, the 3D memory device fabricated with method 300 can be the 3D memory device 200 depicted in FIG. 2. It should be understood that the operations shown in method 300 are not exhaustive and that other operations can be performed before, after, or between any of the operations. For example, other operations may include wet clean operations, dry etch operations, photolithography operations, etc. Further, the sequence of the operations in method 300 is not limiting, and some operations may be performed concurrently or in a different order.

[0064] Referring to FIG. 3 and FIG. 4, method 300 begins with operation 302, where an alternating dielectric stack 400 is disposed, or otherwise deposited, on a substrate 202. For example purposes, substrate 202 in method 300 will be described in the context of single crystalline Si. Based on the disclosure herein, other materials, as discussed above, can be used. These materials are within the spirit and scope of this disclosure. A plurality of first dielectric layer 208 and second dielectric layer 402 pairs can be formed on substrate 202 to form alternating dielectric stack 400. In some embodiments, each dielectric layer pair includes a SiO₂ layer and a SiN layer. For example, first dielectric layer 208 can be made of SiO₂ (same as

dielectric layer 230 of alternating conductor/dielectric stack 210 of FIG. 2) and second dielectric layer 402 can be made of SiN. Alternating dielectric stack 400 can be formed by one or more thin-film deposition processes including, but not limited to, chemical vapor deposition (CVD), plasma-enhanced CVD (PECVD), physical vapor deposition (PVD), atomic layer deposition (ALD), plasma-enhanced ALD (PEALD), or any combination thereof. By way of example and not limitation, the height of dielectric stack 400 can range from about 4 μm to about 30 μm . In some embodiments, second dielectric layer 402 can be a sacrificial layer that will be replaced with a conductor in a subsequent operation so that alternating dielectric stack 400 can be converted to an alternating conductor/dielectric stack, similar to alternating conductor/dielectric stack 210 of FIG. 2.

[0065] According to some embodiments, substrate 202 includes isolation regions or structures, like STI structure 233 shown in FIG. 4. STI structure 233 in FIG. 4 can be formed on a top portion of substrate 202. By way of example, STI structure 233 can be formed prior to the formation of alternating dielectric stack 400. STI structures can be filled with a dielectric material, such as for example SiO_2 .

[0066] Method 300 continues with operation 304, as illustrated in FIG 3, in which a staircase structure (like staircase structure 212 of FIG. 2) is formed from a portion of alternating dielectric stack 400. In some embodiments, a “trim-etch” process can be used on at least one side (in the lateral direction, x-direction) of alternating dielectric stack 400 to form a staircase structure with multiple levels (e.g., steps). By way of example and not limitation, a trim-etch process can be a multi-cycle process, where each cycle includes one or more photolithography operations followed by an etch operation. During the photolithography operations, a patterned photoresist (PR) layer masks a portion of dielectric stack 400. A subsequent first etch process removes a predetermined number of dielectric pairs from the exposed portion of dielectric stack 400 to form a first step (e.g., first level) in dielectric stack 400. The PR is then laterally trimmed (e.g., recessed in the x-direction) to expose an additional portion of dielectric stack 400. A subsequent second etch removes a predetermined number of dielectric pairs from the newly exposed dielectric stack 400 and the first step. Hence, a second step (e.g., second level) in dielectric stack 400 is formed. This step formation process continues in this fashion (e.g., a PR trim followed by an etch operation) until the desired number of steps in dielectric stack 400 is formed and the staircase structure is complete. As a result of this process, each level can include any desired number of dielectric layer pairs with alternating first dielectric layer 208 and second dielectric

layer 402. After the staircase structure formation, the PR layer is removed (stripped) with a wet etch process. FIG. 5 shows the resulting staircase structure 500 made from alternating dielectric stack 400 according to the description of operation 304 of method 300.

[0067] In some embodiments, the etch process used in operation 304 can be a dry etch process that uses a single etch gas chemistry for both dielectric layers 208 and 402. Alternatively, the etch process used in operation 304 can use different etch chemistries for each dielectric layer. Further, depending on the selectivity of the etch chemistry, the etch process can be timed, end-pointed, or a combination thereof.

[0068] After the staircase structure formation, dielectric layer 230 is deposited over staircase structure 500 and dielectric stack 400. In some embodiments, a CMP or a dry etch process can be used to planarize the top surface of dielectric layer 230, as shown in FIG. 5. By way of example and not limitation, dielectric layer 230 can be SiO₂ deposited by PECVD, CVD, or another suitable deposition process. The thickness of dielectric layer 230 over alternating dielectric stack 400 can range from about 10 to about 1000 nm. In some embodiments, dielectric layer 230 is the same as dielectric layer 208 of dielectric stack 400, e.g., SiO₂.

[0069] Method 300 continues with operation 306, as illustrated in FIG. 3, where a channel structure can be formed over substrate 202. However, this is not limiting and additional channel structures can be formed. Each channel structure can extend vertically through the alternating dielectric stack 400, as discussed earlier. Fabrication of each channel structure begins by etching a channel hole through dielectric layer 230 and alternating dielectric stack 400 until substrate 202 is exposed through the channel hole. Prior to filling the channel hole, an epitaxial plug 222 can be grown through the channel hole from substrate 202, as shown in FIG. 6. By way of example and not limitation, epitaxial plug 222 can be single crystalline Si. The height of epitaxial plug 222 can be controlled through the epitaxial growth process conditions. Channel structure 216 can be subsequently formed on epitaxial plug 222 by filling the channel hole.

[0070] By way of example and not limitation, a dry etch process can be used to form the channel hole. In some embodiments, the fabrication process of channel structure 216 further includes depositing memory film 220 and semiconductor channel 218 so that memory film 220 can be interposed between semiconductor channel 218 and the dielectric layer pairs 402 and 402 of alternating dielectric stack 400. Semiconductor channel 218 can include semiconductor materials, such as polysilicon. Memory film 220 can be a composite stack of dielectric layers

including a combination of a tunneling layer, a storage layer, and a blocking layer (not individually shown in FIG. 6).

[0071] By way of example and not limitation, the tunneling layer can include dielectric materials such as SiO₂, SiN, SiON, or a combination thereof. Electrons or holes from the semiconductor channel can tunnel into a storage layer through the tunneling layer. The storage layer can include materials for storing charge. The storage layer materials include, but are not limited to, SiN, SiON, a combination of SiO₂ and SiN, or a combination thereof. The blocking layer can include a single dielectric material, such as SiO₂, or a stack of dielectric materials, such as SiO₂/SiN/SiO₂ (ONO). The blocking layer can further include a high-k dielectric, such as aluminum oxide (Al₂O₃). Semiconductor channel 218 and memory film 220 can be formed by one or more thin-film deposition processes, such as ALD, CVD, PEALD, PECVD, any other suitable deposition processes, or a combination thereof.

[0072] In some embodiments, dummy channel structures (not shown in FIGs. 4-13; e.g., dummy channel structures 122 in FIGs. 1A-1B) are formed simultaneously with channel structures 216. The dummy channel structures can extend vertically through the alternating layer stack and can be filled with the same materials as those in channel structures 216. However, local contacts are not formed on the dummy channel structures to provide electrical connections with other components of the 3D memory device. Thus, the dummy channel structures cannot be used for forming memory cells in the 3D memory device, i.e., they are not electrically functional or otherwise operational. In some embodiments, the dummy channel structures are used as structural elements.

[0073] Referring to FIG. 3, method 300 continues with operation 308 and the formation of an opening in the alternating dielectric layer stack. Formation of the opening involves etching portions of dielectric layer 230 and dielectric stack 400 until STI structure 233 of substrate 202 is exposed (e.g., through the etched portions of dielectric layer 230 and dielectric stack 400), as shown in FIG. 6. In other words, the opening can be formed so that it is aligned to STI structure 233. In some embodiments, the opening cannot expose an area beyond the STI structure 233. For example, the opening cannot expose STI structure 233 and a portion of substrate 202. However, the opening can expose a portion of STI structure 233. This can be accomplished via photolithography and etch methods (patterning). For example, photolithography can be used to form a patterned PR structure or a patterned hard mask (HM) (not shown in FIG. 6) over dielectric layer 230. The patterned PR structure or patterned HM can have an opening that

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exposes an area of dielectric layer 230. The opening in the patterned PR structure or patterned HM can be positioned so that it is over an area of the underlying STI structure 233. Areas of dielectric layer 230, where the formation of a dielectric structure is not desired, are covered by the patterned PR structure or patterned HM. A subsequent dry etch process removes the exposed portions of dielectric layer 230 and dielectric stack 400—e.g., through the openings in the patterned PR structure or patterned HM—until STI structure 233 of substrate 202 is exposed. In some embodiments, the dry etch process can be a multi-step, anisotropic etch that can be terminated (e.g., stopped) when STI structure 233 is exposed. By way of example and not limitation, the dry etch process can include the same or different etch chemistry for each layer (e.g., dielectric layer 230 and alternating dielectric stack 400). As a result of operation 308, an opening 600 with width 600w is formed in dielectric stack 400 over STI structure 233, as shown in FIG. 6. As discussed above, width 600w of opening 600 can be equal or shorter than width 233w of STI structure 233 (e.g., $600w \leq 233w$). In some embodiments, opening 600 may extend partially into STI structure 233. In other words, the etch process used to form opening 600 may also remove (recess) portion of the top surface of STI structure 233. It is noted that opening 600 shown in FIG. 6 can also extend in the y-direction (not shown in the view of FIG. 6) and its size can be defined by the patterned PR structure or patterned HM and the process conditions during the etch process. In any direction, the area of opening 600 can be equal or smaller than the area of STI structure 233, according to some embodiments. Additionally, multiple openings, like opening 600, can be formed concurrently during operation 306 of method 300 in other areas of dielectric stack 400. Further, each opening 600 can be formed over an STI structure 233. In some embodiments, the aspect ratio of opening 600 can range from about 0.1 to about 10.

[0074] In some embodiments, opening 600 can be formed concurrently with channel structure 216. In an alternative embodiment, opening 600 can be formed after the formation of channel structure 216, or before the formation of channel structure 216. Each of the aforementioned sequence of operations may require additional number of photolithography, etch, or deposition operations. After the formation of opening 600, the patterned PR structure or patterned HM can be removed (stripped) with a wet etch process.

[0075] In referring to FIGs. 3 and 7, method 300 continues with operation 310, where opening 600 can be filled with a dielectric layer 702. In some embodiments, dielectric layer 702 includes a SiO₂ layer that can be deposited by a CVD, flowable CVD (FCVD), a PECVD process, or any other suitable process that can fill a high aspect ratio structure. By way of example and not

limitation, dielectric layer 702 can be the same as dielectric layer 230, and/or first dielectric layer 208. A CMP process or a dry etch process can be used to planarize dielectric layer 702 so that the top surfaces of dielectric layer 230 and dielectric layer 702 are coplanar as shown in FIG. 7. As a result, dielectric structure 232 is formed in dielectric stack 400. In some embodiments, dielectric structure 232 defines the borders of TAC region 120 shown in FIGS. 1A-1C.

[0076] In some embodiments an etch stop layer is formed on the channel structures 216. For example a dielectric layer 704 can be deposited over dielectric layers 230 and 232 and be subsequently patterned to form plug openings 706 as shown in FIG. 7. Etch stop plug 224 can be subsequently formed on channel structures 216 by filling plug openings 708 using one or more thin-film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof, as shown in FIG. 8. In some embodiments, polysilicon can be used to fill plug opening 706 followed by a CMP process to remove the excess polysilicon so that etch stop plug 224 can be coplanar with dielectric layer 704. In some embodiments, a metallic stack, such as Ti/ TiN/W, can be deposited to fill plug opening 706, followed by a CMP process to make the top surface of etch stop plug 224 and dielectric layer 704 coplanar. In some embodiments, etch stop plug 224 can be sacrificial so that it can be replaced in a subsequent operation. For example, a sacrificial etch stop plug 224 can include an oxide instead of polysilicon or a metallic stack. A sacrificial etch stop plug 224 can be removed at a later operation and replaced with a “permanent” etch stop plug made of polysilicon or a metallic stack.

[0077] In operation 312 of method 300, as illustrated in FIG. 3, one or more slit openings can be formed in alternating dielectric stack 400. For example, slit opening 900 can be formed by dry etching dielectric layers 208 and 402 (e.g., SiO₂ and SiN) in dielectric stack 400, as shown in FIG. 9. In some embodiments, doped regions 228 can be subsequently formed in substrate 202 under each slit by, for example, ion implantation and thermal diffusion through the slits. Alternatively doped regions 228 can be formed during an earlier fabrication stage, for example, prior to the formation of dielectric stack 400, according to some embodiments.

[0078] In operation 314 of method 300, slit openings 900, shown in FIG. 9, can be used for a “gate replacement” process (also known as the “WL replacement” process) in which second dielectric layers 402 (shown in FIG. 9; e.g., SiN) in stack 400 are replaced with conductor layers 206 (shown in FIG. 10; e.g., W). As a result, alternating dielectric stack 400 is converted to alternating conductor/dielectric stack 210 shown in FIG. 2.

[0079] The replacement of second dielectric layers 402 with conductor layers 206 can be achieved with the use of a wet etch process that is highly selective (e.g., with selectivity equal to, or greater than, 500:1) towards second dielectric layer 402 (e.g., SiN), in comparison to first dielectric layer 208 (e.g., SiO₂). By way of example and not limitation, the wet etch chemistry can include hot phosphoric acid (H₃PO₄). Since the wet etch chemistry is highly selective towards SiN, any layers or structures (including first dielectric layer 208 and dielectric structure 702) made of oxide (e.g., SiO₂) will not be etched or removed (i.e., will not be affected by the wet etch process).

[0080] Once second dielectric layers 402 are fully removed (e.g., etched), a conductive layer can be deposited by CVD, PECVD, ALD, PEALD, or combinations thereof to fill the space between first dielectric layers 208 through slit openings 900. As a result, conductor layers 206 can be formed between first dielectric layers 208 as shown in FIG. 10. By way of example and not limitation, the conductor materials can include W, Co, Cu, Al, polysilicon, silicides, or a combination thereof. In some embodiments, adhesion layers or barrier layers (not shown in FIG. 10) may also be deposited prior to the deposition of the conductor material. In some embodiments, conductive layers 206 can be deposited with a deposition–etch–deposition process to avoid partially filling slit openings 900 with the conductor material.

[0081] In operation 316 of method 300 shown in FIG. 3, the slit openings can be filled with a conductor material 1004 to form slit structures 226 as shown in FIG. 10. In some embodiments, conductor material 1004 can be the same as the conductor material in conductor layers 206. For example, slit structures 226 can be filled with W, Co, Cu, Al, polysilicon, silicides, or a combination thereof. In some embodiments, to electrically isolate conductor material 1004 of slit structure 226 from conductor layers 206, a dielectric layer 1008 (e.g., SiO₂) can be deposited therebetween. A CMP process can subsequently remove excess conductor material over dielectric layer 704 as shown in FIG. 10. The lower end of slit structure 226 can be in contact with doped region 228. In some embodiments, slit structure 226 can function as a source contact that is electrically connected to NAND string 204 through doped region 228 of substrate 202.

[0082] Referring to Fig. 11, a dielectric layer 1100 can be blanket deposited over dielectric layer 704 across substrate 202 so that local contacts can be formed in dielectric layer 1100. In some embodiments, the contact formation process can be divided into two separate photolithography/etch operations to accommodate the formation of contacts with different depths or heights. For example, the shortest local contacts (e.g., the NAND string contacts, the slit

structure contacts, and the upper WL contacts of the staircase structure) can be formed first, and the tallest local contacts (e.g., the TACs and the lower WL contacts of the staircase structure) can be formed second. Merely for simplicity, the aforementioned shorter local contacts can be collectively referred to as first local contacts, and the aforementioned tallest local contacts can be collectively referred to as second local contacts.

[0083] Dielectric layer 1100 can be formed by one or more thin-film deposition processes, including ALD, CVD, PVD, any other suitable processes, or any combination thereof. Dielectric layer 1100 can include dielectric materials, including, but not limited to, SiO₂, SiN, SiON, or any combination thereof. First local contacts—such as NAND string contacts 236, slit structure contacts 238, and upper WL contacts 240-1—can be formed through dielectric layer 1100 by first etching vertical openings (e.g., with a dry etch), followed by filling the openings with conductor materials using ALD, CVD, PVD, any other suitable processes, or any combination thereof. By way of example and not limitation, the conductor materials used to fill the local contacts can include W, Co, Cu, Al, polysilicon, silicides, or a combination thereof. In some embodiments, prior to the conductor material fill, the openings can be filled with a barrier layer, an adhesion layer, and/or a seed layer. In some embodiments, prior to filling the openings, the oxide sacrificial etch stop plugs 224 can be replaced with permanent etch stop plugs made of polysilicon or a metallic stack, as discussed above.

[0084] Etching of dielectric layers to form the openings of first local contacts can be controlled via the “inherent” etch selectivity between the etched layer (e.g., a dielectric layer) and the underlying layer (a conductor, a nitride or oxide, etc.). For example, in the case of NAND string contacts 236, etch stop plug 224 filled with an oxide different from dielectric layer 1100 or a nitride can prevent further etching into NAND strings 204 during the formation of the first local contact openings. In the case of slit structure contacts 238 and upper WL contacts 240-1, further etching can be prevented due to the presence of conductor material 1004 and conductor layer 206, which can act as an etch stop layer for the dry etch process. As a result, formation of first local contacts with different heights can be possible.

[0085] As discussed earlier, first local contacts—such as NAND string contacts 236, slit structure contacts 238, and upper WL contacts 240-1—can be concurrently formed in the same contact forming process. The first local contact forming process can include multiple processes, for example, photolithography, etch, thin-film deposition, and CMP. In some embodiments, each process in the contact forming process can be performed only once for all the first local contacts.

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For example, a single lithography and etch process can be used to form all the openings of NAND string contacts 236, slit structure contacts 238, and upper WL contacts 240-1 and a single deposition process can be performed to fill all the openings of NAND string contacts 236, slit structure contacts 238, and upper WL contacts 240-1 with the same conductor materials. In some embodiments, a CMP process can remove excess deposited material from the top surface of dielectric layer 1100.

[0086] In Referring to FIG. 3 and method 300, the formation of the TAC structures (and the rest of the second local contacts) can be formed in operation 318. Referring to FIG. 12, and according to some embodiments, after forming the first set of local contacts (e.g., NAND string contacts 236, slit structure contacts 238, and upper WL contacts 240-1) a second set of local contacts can be formed, including TACs 234 and lower WL contacts 240-2 that are close to substrate 202. TACs 234 can be formed in dielectric layers 1100, 704, and 232—and lower WL contacts 240-2 can be formed in dielectric layers 1100, 704, and 230—by first etching vertical openings (e.g., by dry etching), followed by filling the openings with conductor materials using ALD, CVD, PVD, any other suitable processes, or any combination thereof. The conductor materials used for filling the local contacts can include, but are not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. In some embodiments, prior to the conductor material deposition, a barrier layer, an adhesion layer, and/or a seed layer can be formed.

[0087] TACs 234 can be formed by etching through the entire thickness of dielectric structure 702. Since both TACs 234 and lower WL contacts 240-2 are formed in oxide layers (e.g., dielectric layers 1100, 704, 232, and 230) the overall etching process can be simplified in terms of etching chemistry, etching process tooling, overall process integration, and cost. By way of example and not limitation, the openings for TACs 234 and lower WL contacts 240-2 can be formed by a deep reactive-ion etching (DRIE) process or with any other suitable anisotropic etch process. Forming TACs 234 in dielectric structure 232 can simplify the fabrication process and reduce the fabrication cost. This is because TACs 234 can be easily formed even after the gate replacement process together with the other local contacts in a common contact forming process.

[0088] In some embodiments, the lower end of TACs 234 can be formed in STI structure 233 and in contact with substrate 202, as shown in FIG. 12. For example, TACs 234 can extend through STI structure 233 and stop on substrate 202. The lower end of each lower WL contacts 240-2 can be in contact with the corresponding top conductor layer 206 (WL) of a corresponding level in the staircase structure, as shown in FIG. 12. The upper ends of all the local contacts

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(including both the first and second sets of local contacts) can be coplanar with one another at the top surface of dielectric layer 1100. The second set of local contacts (including TACs 234 and lower WL contacts 240-2) can be simultaneously formed in the same contact forming process after the formation of the first set of local contacts. That is, all the local contacts (including both the first and second sets of local contacts) can be formed in two contact forming processes as illustrated in FIGs. 11 and 12.

[0089] It is understood that in some embodiments, all the local contacts (including both the first and second sets of local contacts) can be simultaneously formed in a single contact forming process. That is, the two contact forming processes illustrated in FIGs. 11 and 12 can be combined into a single contact forming process. In some embodiments, each process in the contact forming process can be performed once for all of NAND string contacts 236, slit structure contacts 238, TACs 234, upper WL contacts 240-1, and lower WL contacts 240-2. For example, a single lithography process can be performed followed by a single etch process and a single deposition process.

[0090] In some embodiments, an additional contact layer with a plurality of contacts can be formed over the local contacts. As illustrated in FIG. 13, contact layer 242 (including a dielectric layer 1302 and contacts 246) can be formed over dielectric layer 1100. Dielectric layer 1302 can be formed by one or more thin-film deposition processes, including ALD, CVD, PVD, any other suitable processes, or any combination thereof. Dielectric layer 1302 can include dielectric materials, including, but not limited to, SiO₂, SiN, SiON, or any combination thereof. Contacts 246 can be formed through dielectric layer 1302 by first etching vertical openings (e.g., using dry etch), followed by filling the openings with conductor materials using ALD, CVD, PVD, any other suitable processes, or any combination thereof. The conductor materials used to fill contacts 246 can include, but are not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. In some embodiments, prior to the conductor material deposition, a barrier layer, an adhesion layer, and/or a seed layer can be deposited in the contact opening.

[0091] As shown in FIG. 13, the lower end of each contact 246 can be in contact with the upper end of a corresponding local contact, for example, NAND string contact 236, slit structure contact 238, TAC 1200, or WL contacts 240-1 and 240-2. In some embodiments, all contacts 246 in contact layer 242 can be simultaneously formed in the same contact forming process. In some embodiments, each contact 246 of contact layer 242 is a via. Further, contact layer 242 can be

referred to as the “Via0 (V0)” level/ bottom level of the interconnect structures of 3D memory device 200.

[0092] Subsequently, a plurality of third contacts in an interconnect layer can be formed. As illustrated in FIG. 13, interconnect layer 244 (including a dielectric layer 1308 and interconnect contacts 248) can be formed above contact layer 242. Dielectric layer 1308 can be formed by one or more thin-film deposition processes, such as ALD, CVD, PVD, any other suitable processes, or any combination thereof. Dielectric layer 1308 can include dielectric materials, including, but not limited to, SiO₂, SiN, SiON, or any combination thereof. By way of example and not limitation, interconnect contacts 248 can be formed through dielectric layer 1308 by first etching vertical openings (e.g., with a dry etch process), followed by filling the openings with conductor materials using ALD, CVD, PVD, any other suitable processes, or any combination thereof. The conductor materials used to fill interconnect contacts 248 can include, but are not limited to, W, Co, Cu, Al, polysilicon, silicides, or any combination thereof. In some embodiments, prior to the conductor material deposition, a barrier layer, an adhesion layer, and/or a seed layer is formed.

[0093] As shown in FIG. 13, the lower end of each interconnect contact 248 can be in contact with the upper end of corresponding contact 246 in contact layer 242, so that each interconnect contact 248 can be electrically connected to a corresponding memory array structure, such as NAND strings 204, slit structures 226, and WLS 240-1 and 240-2. In some embodiments, all interconnect contacts 248 in interconnect layer 244 can be concurrently formed in the same contact forming process. In some embodiments, each interconnect contact 248 can be an interconnect line, and interconnect layer 244 can be referred to as the “Metal0 (M0)” level/ bottom level of the interconnect structures of 3D memory device 200.

[0094] According to some embodiments, contacts 246 and interconnect contacts 248 can be formed in a single contact forming process, such as in a dual damascene process for forming Cu contacts. Nevertheless, as illustrated in FIG. 13, the interconnect structures including local contacts and contacts 246 and 248 can be formed in a limited number of fabrication steps to reduce the fabrication complexity and cost.

[0095] Various embodiments in accordance with the present disclosure provide a 3D memory device with interconnect structures for a memory array. The interconnect structures allow contacts for various memory array structures (e.g., NAND strings, gate line slits, WLS, etc.) to be fabricated in a limited number of operations (e.g., in a single operation or in two operations),

thereby reducing the process complexity and manufacturing cost. In some embodiments, the interconnect structures disclosed herein can include bit lines in the top interconnect layer. These bit lines are suitable for 3D memory architectures in which the array device and the peripheral device are formed on different substrates and are subsequently joined by hybrid bonding in a face-to-face configuration.

[0096] Moreover, the interconnect structures disclosed herein include TACs for providing vertical interconnects between the stacked array device and peripheral device (e.g., for power bus and metal routing), thereby reducing the metal levels, improving the packing density and decrease the die size. In some embodiments, the TACs in the interconnect structures disclosed herein are formed in a dielectric structure that can be easily etched to form through holes therein compared to a stack of alternating dielectric layers or a stack of alternating conductor/dielectric layers. Therefore, fabrication complexity and cost can be reduced. The dielectric structure can be formed prior to the conversion of alternating layer stack of dielectrics to a conductor/dielectric layer stack.

[0097] In some embodiments, a 3D memory device includes a semiconductor substrate, an alternating layer stack disposed on the semiconductor substrate, and a dielectric structure, extending vertically through the alternating layer stack, on an isolation region of the substrate. Further, the alternating layer stack can abut a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material. The 3D memory device additionally can include one or more TACs that extend vertically through the dielectric and isolation region, and one or more channel structures that extend vertically through the alternating layer stack.

[0098] The 3D memory device further includes an epitaxial layer formed between each of the one or more channel structures and the semiconductor substrate, an etch stop plug disposed on each of the one or more channel structures, a staircase structure disposed in the alternating layer, and one or more contact layers disposed on the one or more TACs, channel structures, and slit structures.

[0099] In some embodiments, the dielectric structure abuts a sidewall surface of the TACs.

[0100] In some embodiments, the 3D memory device is a NAND 3D memory device.

[0101] In some embodiments, the alternating layer stack includes alternating pairs of a dielectric and conductor layers.

[0102] In some embodiments, the dielectric layer comprises silicon oxide and the conductor layer includes a metal.

[0103] In some embodiments, the conductor layers include a word line.

[0104] In some embodiments, the dielectric material is silicon oxide.

[0105] In some embodiment, the dielectric structure includes an oxide.

[0106] In some embodiment, the dielectric structure defines a through array contact region within the 3D memory device.

[0107] In some embodiments, an area of the dielectric structure is equal to or smaller than an area of the isolation region.

[0108] In some embodiments a method for forming 3D memory device includes forming an isolation structure on a substrate, disposing an alternating dielectric layer stack on the substrate, where the alternating dielectric layer stack includes pairs of a first dielectric layer and a second dielectric layer different from the first dielectric layer. The method further includes forming a channel structure extending vertically in the alternating dielectric layer, forming an opening in the alternating dielectric layer stack, where the opening exposes the isolation structure. The method also includes filling the opening with a dielectric layer to form a dielectric structure as a TAC region of the 3D memory device, removing portions of the dielectric structure and the isolation structure until the substrate is exposed to form a TAC opening that vertically extends through the dielectric structure and the isolation structure, and filling the TAC opening with a conductor to form a TAC structure in the TAC region, wherein the TAC structure is in contact with the substrate.

[0109] In some embodiments, before forming the TAC opening the method further includes forming slit openings that expose a doped region of the substrate by extending vertically in the alternating dielectric layer, replacing the second dielectric layer through the one or more slit openings with a conductor layer to convert the alternating dielectric layer stack to an alternating dielectric/conductor layer stack, and filling the one or more slit openings with a conductor to form one or more slit structures extending vertically in the alternating dielectric/conductor layer stack.

[0110] In some embodiments, before forming a channel structure, performing a trim-etch process to form a staircase structure in the alternating dielectric layer stack.

[0111] In some embodiment, removing portions of the alternating dielectric layer stack includes performing a dry etch process.

[0112] In some embodiments, filling the opening with the dielectric layer includes depositing the dielectric layer with a chemical vapor deposition, a plasma-enhanced chemical vapor deposition, or a physical vapor deposition process.

[0113] In some embodiments, filling the opening with the dielectric layer includes forming an oxide.

[0114] In some embodiments, filling the opening with the dielectric layer includes forming a silicon oxide.

[0115] In some embodiments, the first dielectric layer includes an oxide and the second dielectric layer comprises a nitride.

[0116] In some embodiments, the first dielectric layer includes a silicon oxide and the second dielectric layer comprises a silicon nitride.

[0117] In some embodiments a method for forming a 3D memory device includes disposing an alternating dielectric layer stack on a substrate, where the alternating dielectric layer stack includes pairs of a first dielectric layer and a second dielectric layer different from the first dielectric layer; forming channel structures extending vertically through the alternating dielectric layer; etching the alternating dielectric layer stack to form an opening, where the opening exposes an isolation region in the substrate; filling the opening with a dielectric layer to form a dielectric structure as a TAC region that is equal or smaller than the isolation region; etching through the dielectric structure and the isolation region to form TAC openings that expose the substrate; and filling the TAC openings with a conductor to form TAC structures in the TAC region.

[0118] In some embodiments a method for forming a 3D memory device further includes forming slit openings extending vertically through the alternating dielectric layer, where the slit openings expose a doped region of the substrate. The method further includes replacing the second dielectric layer through the slit openings with a conductor layer to convert the alternating dielectric layer stack to an alternating dielectric/conductor layer stack, filling the slit openings with a conductor to form slit structures, forming a staircase structure in the alternating dielectric layer stack, where the staircase structure comprises levels. Further the method includes, forming

a word line contact on each of the levels of the staircase structure, forming local contacts over the channel and slit structures, and forming one or more contact layers over the local contacts, each word line, and each TAC structure.

[0119] In some embodiments, forming the opening in the alternating dielectric layer stack includes performing a dry etch process.

[0120] In some embodiments, the alternating dielectric/conductor layer stack abuts a sidewall of the dielectric structure.

[0121] In some embodiments, the dielectric structure abuts a sidewall surface of each TAC structure.

[0122] In some embodiments, a 3D memory device includes a substrate with an isolation structure; an alternating conductor/dielectric layer stack disposed on the substrate; a dielectric structure extending vertically through the alternating conductor/dielectric layer stack over the isolation structure, where the alternating conductor/dielectric layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material; channel structures extending vertically through the alternating conductor/dielectric layer stack; and through array contacts extending vertically through the dielectric and the isolation structures.

[0123] In some embodiments, a 3D memory device further includes a staircase structure disposed in the alternating conductor/dielectric layer stack, where the staircase structures includes levels with each level having a conductor layer thereon; a word line contact disposed on each conductor layer of the staircase structure; and a local contact disposed on each channel structure and slit structure.

[0124] In some embodiments, the dielectric structure abuts a sidewall of the each TAC.

[0125] In some embodiments, the dielectric structure includes a through array contact region of the 3D memory device.

[0126] The foregoing description of the specific embodiments will so fully reveal the general nature of the present disclosure that others can, by applying knowledge within the skill of the art, readily modify and/or adapt for various applications such specific embodiments, without undue experimentation, without departing from the general concept of the present disclosure. Therefore, such adaptations and modifications are intended to be within the meaning and range of equivalents of the disclosed embodiments, based on the teaching and guidance presented herein.

It is to be understood that the phraseology or terminology herein is for the purpose of description and not of limitation, such that the terminology or phraseology of the present specification is to be interpreted by the skilled artisan in light of the teachings and guidance.

[0127] Embodiments of the present disclosure have been described above with the aid of functional building blocks illustrating the implementation of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed.

[0128] The Summary and Abstract sections may set forth one or more but not all exemplary embodiments of the present disclosure as contemplated by the inventor(s), and thus, are not intended to limit the present disclosure and the appended claims in any way.

[0129] The breadth and scope of the present disclosure should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.

WHAT IS CLAIMED IS:

1. A three-dimensional (3D) memory device, comprising:
 - an alternating layer stack;
 - a dielectric structure extending vertically through the alternating layer stack;
 - a through array contact (TAC) extending vertically through the dielectric structure;
 - a channel structure extending vertically through the alternating layer stack;
 - an epitaxial layer under the channel structure;
 - an etch stop plug on the channel structure;
 - a staircase structure in the alternating layer stack;
 - slit structures extending vertically in the alternating layer stack; and
 - a contact layer on the TAC, the channel structure, and the slit structures.
2. The 3D memory device of claim 1, wherein the dielectric structure abuts a sidewall surface of the TAC.
3. The 3D memory device claim 1, wherein the 3D memory device is a NAND 3D memory device.
4. The 3D memory device of claim 1, wherein the alternating layer stack comprises alternating pairs of a dielectric and a conductor layer.
5. The 3D memory device of claim 1, wherein the dielectric structure comprises silicon oxide.
6. The 3D memory device of claim 1, wherein the dielectric structure comprises an oxide material.
7. The 3D memory device of claim 1, wherein the dielectric structure defines a through array contact region within the 3D memory device.
8. The 3D memory device of claim 1, further comprising an isolation region on a semiconductor substrate and the dielectric structure has a footprint equal to or smaller than the isolation region.
9. A three-dimensional (3D) memory device, comprising:
 - an alternating conductor/dielectric layer stack;

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a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;

channel structures and slit structures extending vertically through the alternating conductor/dielectric layer stack;

a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

local contacts disposed on the channel structures and the slit structures; and

through array contacts (TACs) extending vertically through the dielectric structure.

10. The 3D memory device of claim 9, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.

11. The 3D memory device of claim 9, wherein the dielectric structure comprises a through array contact region of the 3D memory device.

12. The 3D memory device of claim 9, further comprising:

an etch stop plug interposed between each local contact of the local contacts and each channel structure of the channel structures; and

an epitaxial layer disposed between the channel structure structures and the substrate.

13. The 3D memory device of claim 9, wherein the dielectric material comprises silicon oxide.

14. The 3D memory device of claim 9, wherein the TACs comprise a conductive material.

15. A method for forming a 3D memory device, the method comprising:

disposing an alternating dielectric layer stack on a substrate;

disposing a staircase structure in the alternating dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

forming a channel structure extending vertically in the alternating dielectric layer stack;

forming a first opening in the alternating dielectric layer stack;

filling the first opening with a dielectric layer;

removing portions of the dielectric structure until the substrate is exposed to form a second opening that vertically extends through the dielectric structure;

filling the second opening with a conductor to form a through array contact (TAC) structure in contact with the substrate; and
disposing a local contact on the channel structure and the TAC structure.

16. The method of claim 15, further comprising:

forming slit openings extending vertically in the alternating dielectric layer stack, wherein the slit openings expose a doped region of the substrate;

replacing a dielectric layer of the alternating dielectric layer stack through the slit openings with the conductor layer to convert the alternating dielectric layer stack to an alternating dielectric/conductor layer stack; and

filling the slit openings with a conductor.

17. The method of claim 15, wherein disposing the staircase structure comprises performing a trim-etch process in the alternating dielectric layer stack before forming the channel structure.

18. The method of claim 15, wherein filling the first opening with the dielectric layer comprises depositing the dielectric layer with a chemical vapor deposition, a plasma-enhanced chemical vapor deposition, or a physical vapor deposition process.

19. The method of claim 15, wherein filling the first opening with the dielectric layer comprises depositing an oxide material.

20. The method of claim 15, wherein disposing the alternating dielectric layer stack comprises alternately disposing a first dielectric layer comprising an oxide material and a second dielectric layer comprising a nitride material.

ABSTRACT

Embodiments of interconnect structures of a three-dimensional (3D) memory device and method for forming the interconnect structures are disclosed. In an example, a 3D NAND memory device includes a semiconductor substrate, an alternating layer stack disposed on the semiconductor substrate, and a dielectric structure, which extends vertically through the alternating layer stack, on an isolation region of the substrate. Further, the alternating layer stack abuts a sidewall surface of the dielectric structure and the dielectric structure is formed of a dielectric material. The 3D memory device additionally includes one or more through array contacts that extend vertically through the dielectric structure and the isolation region, and one or more channel structures that extend vertically through the alternating layer stack.

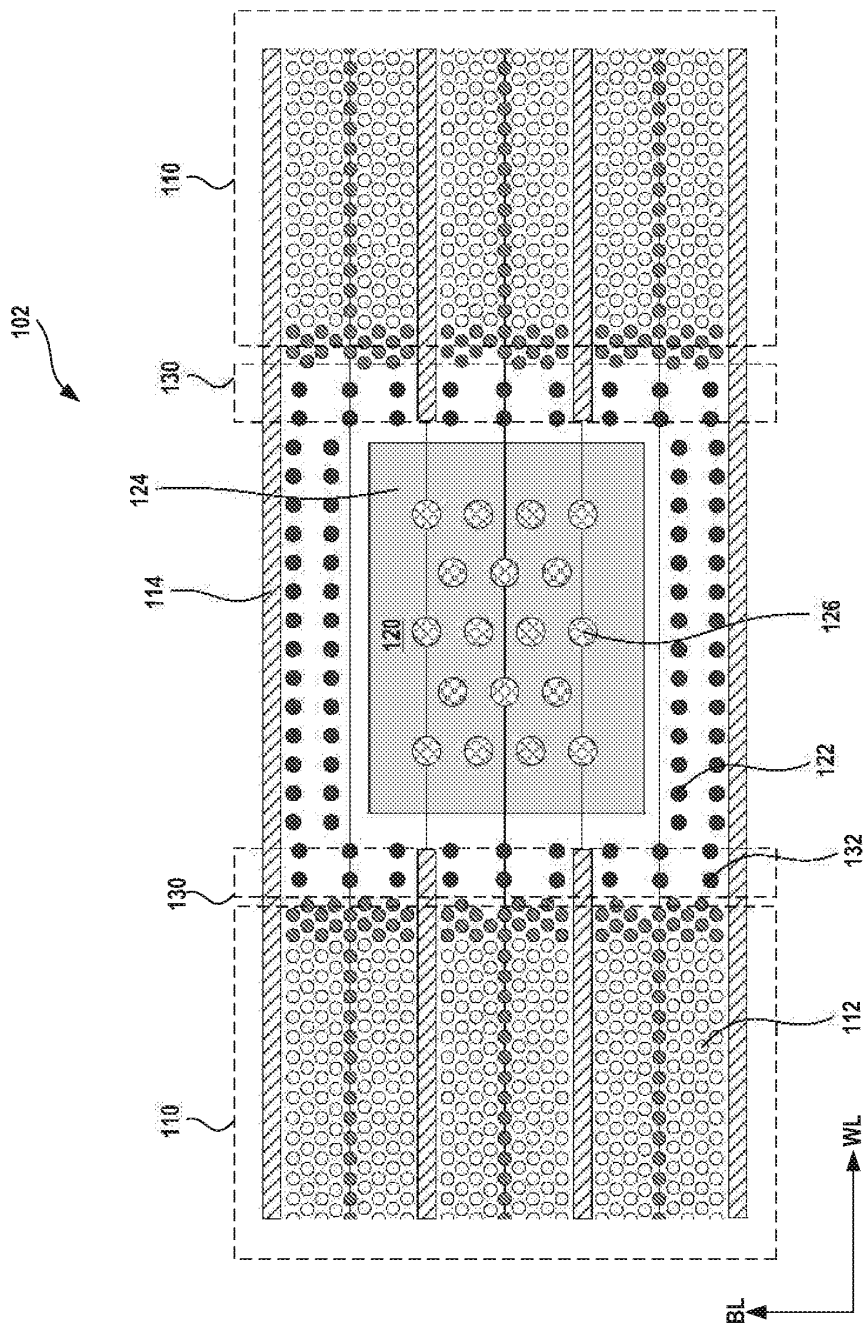


FIG. 1A

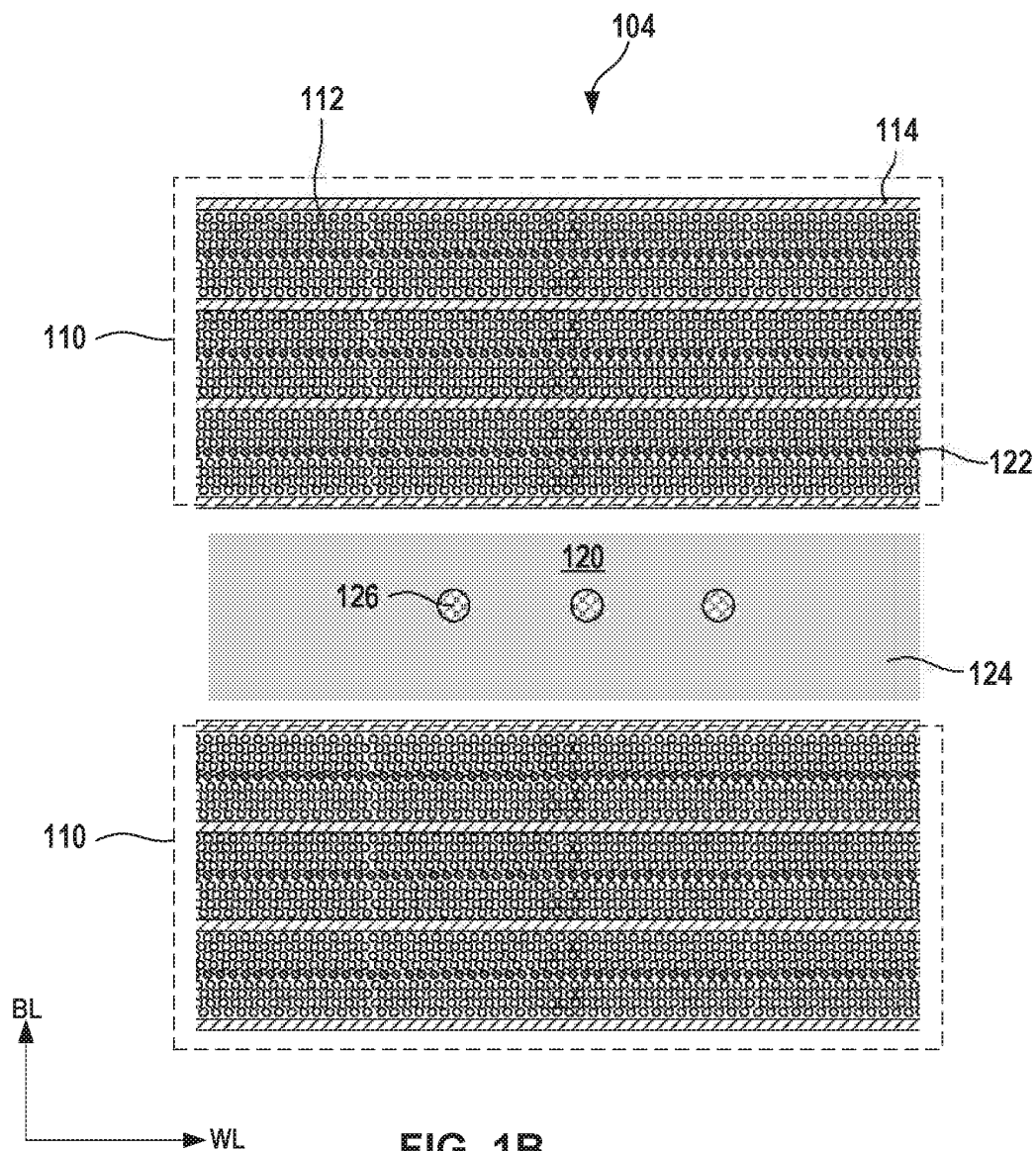
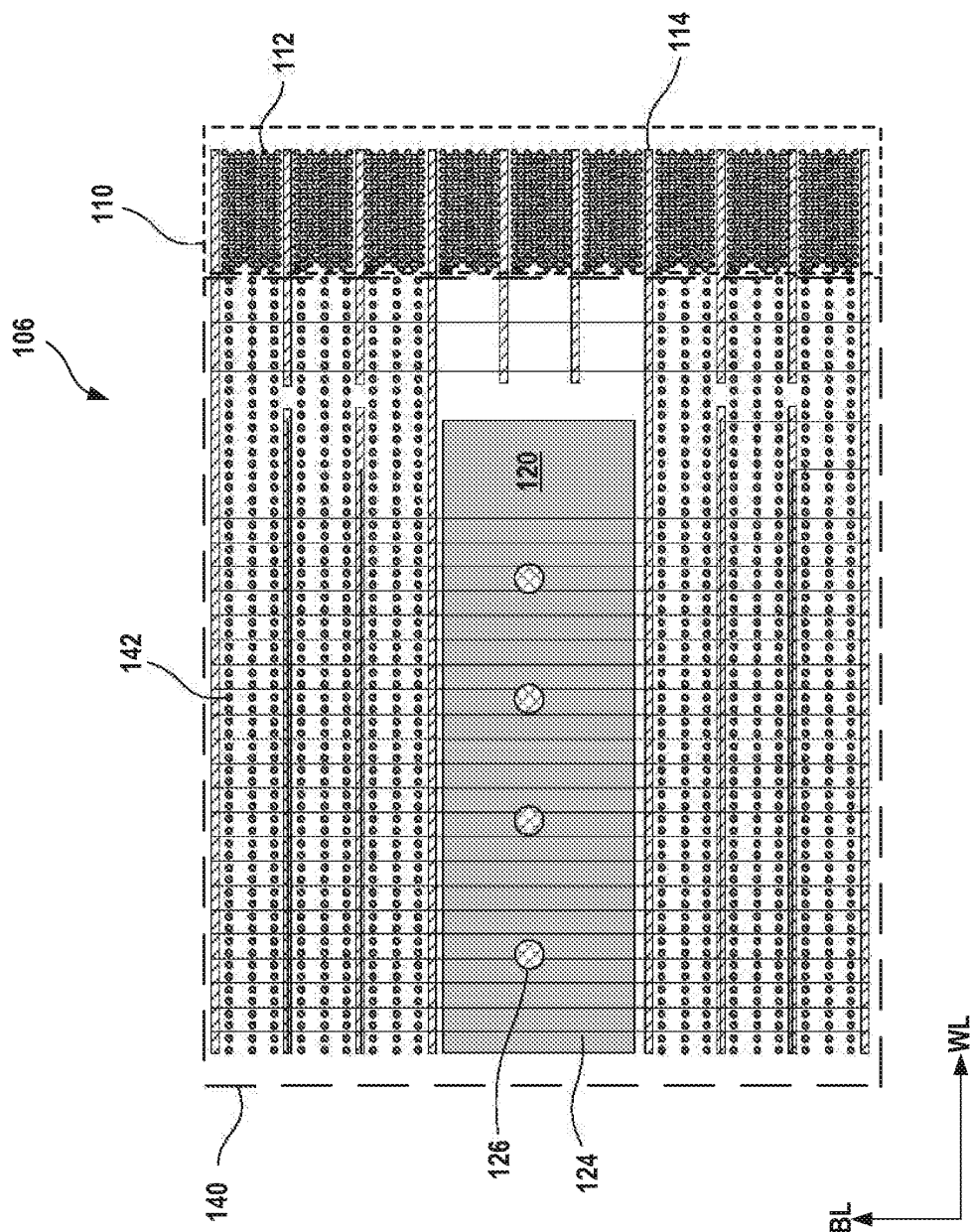


FIG. 1B



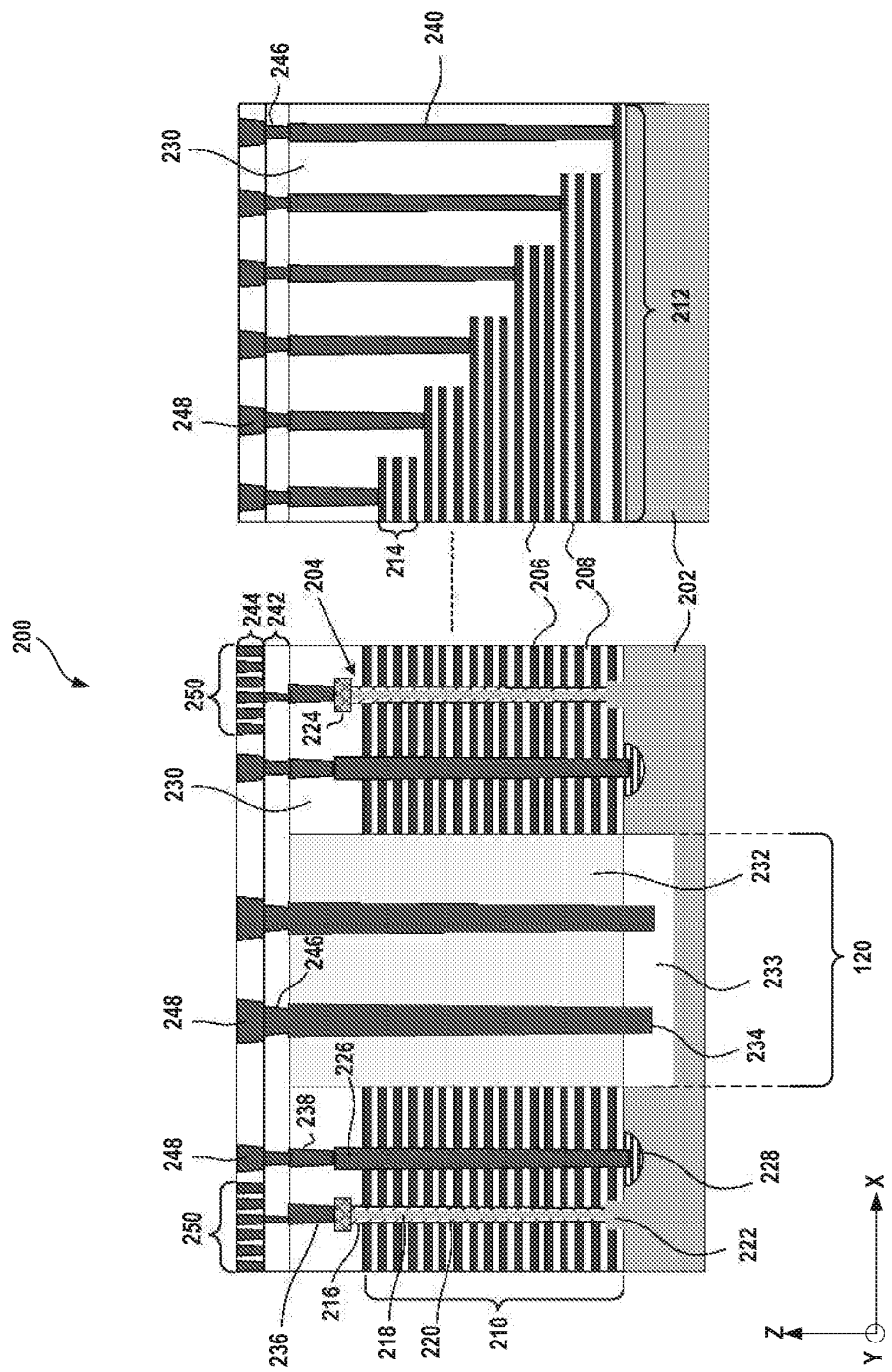


FIG. 2

300

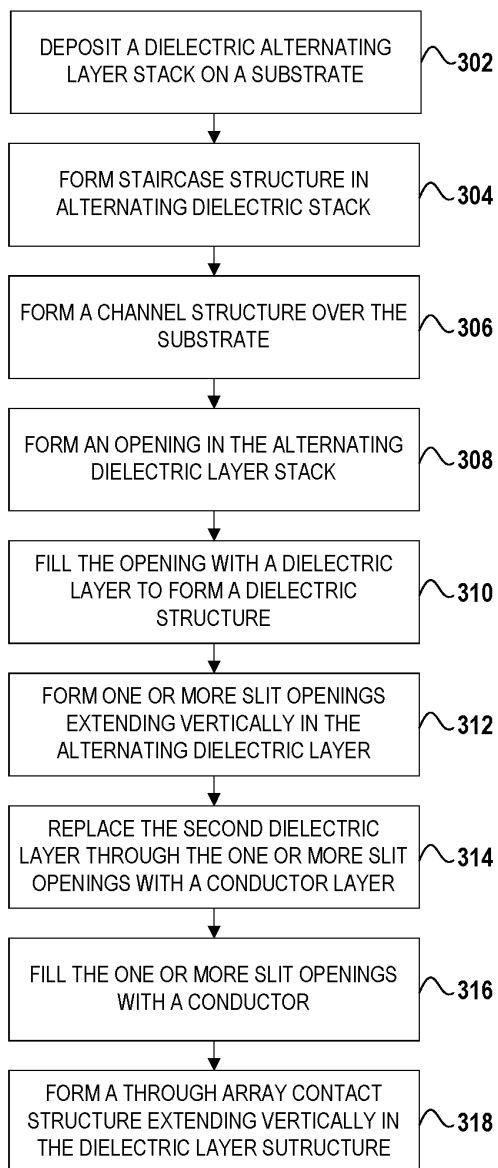


FIG. 3

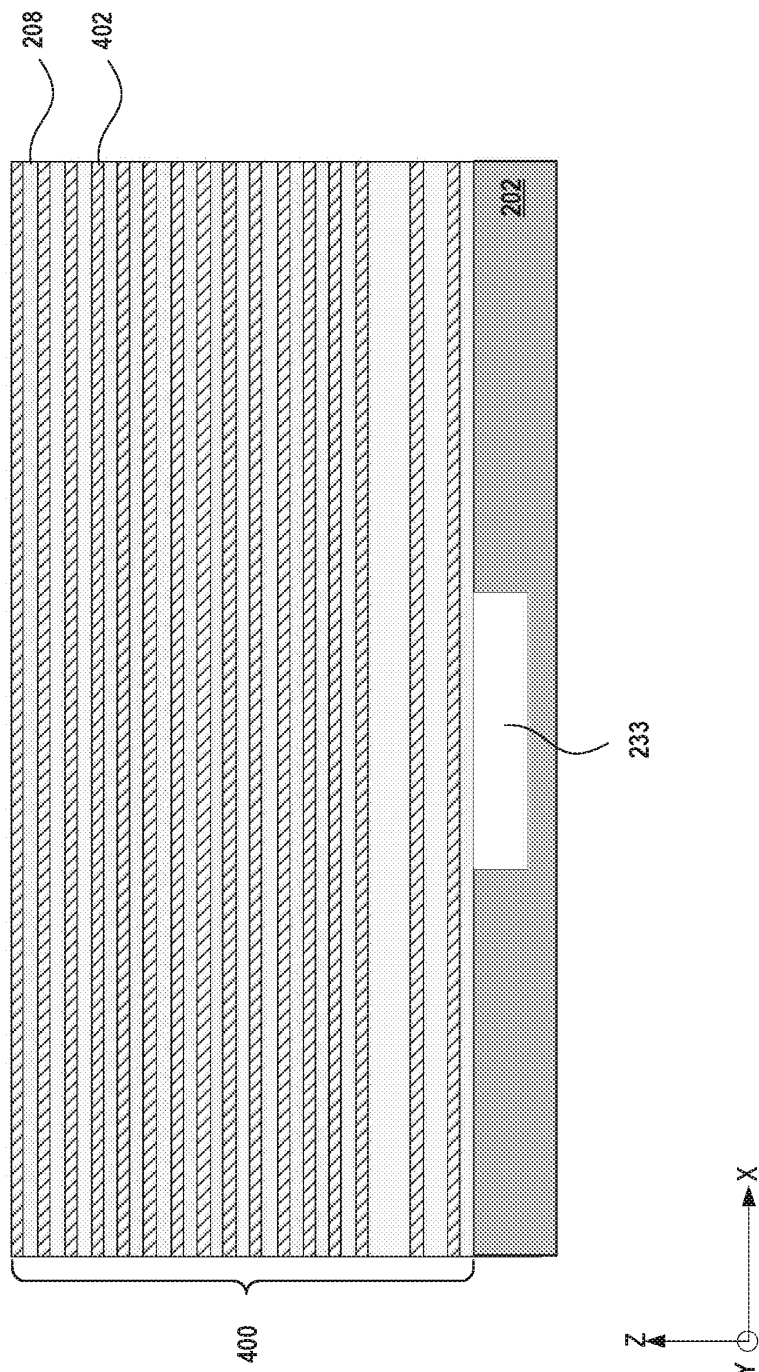


FIG. 4

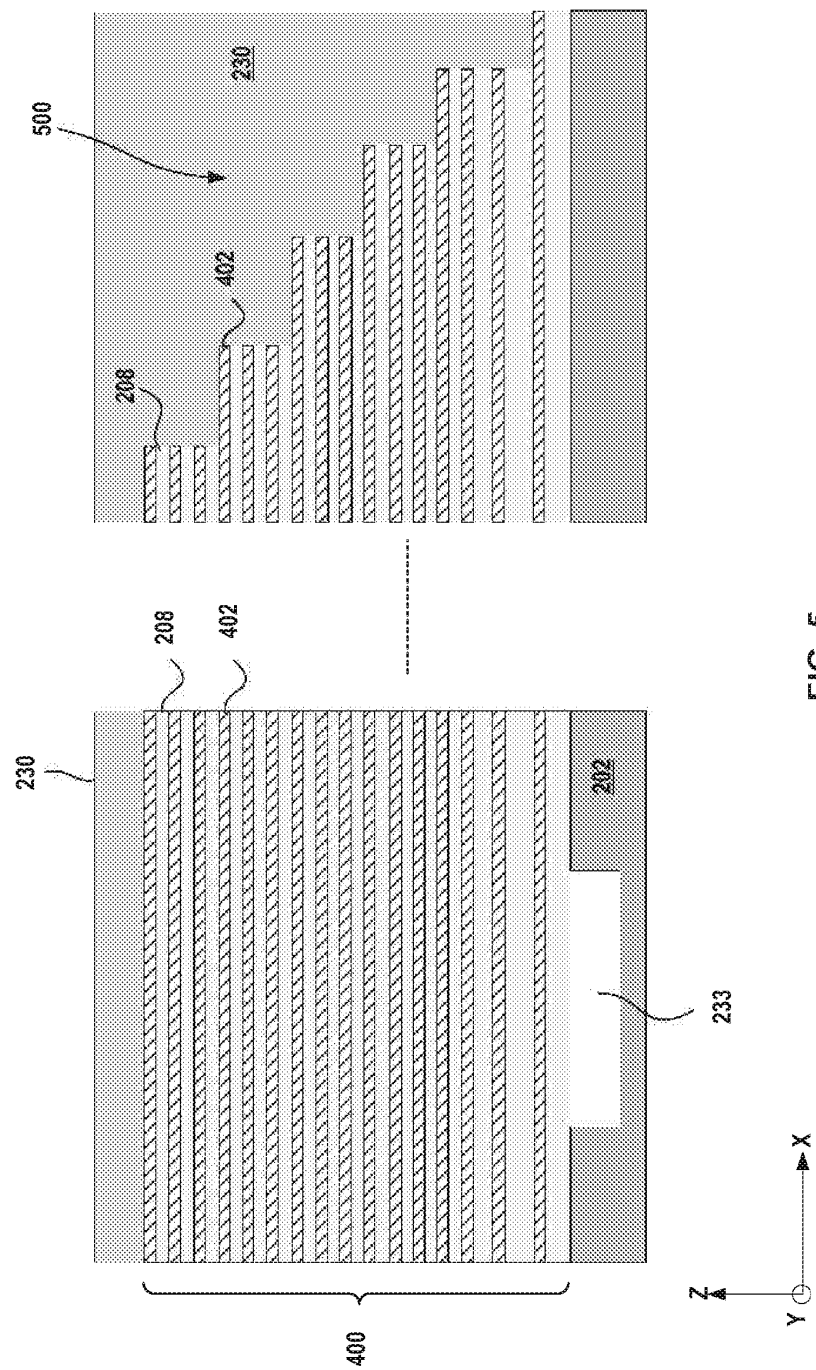


FIG. 5

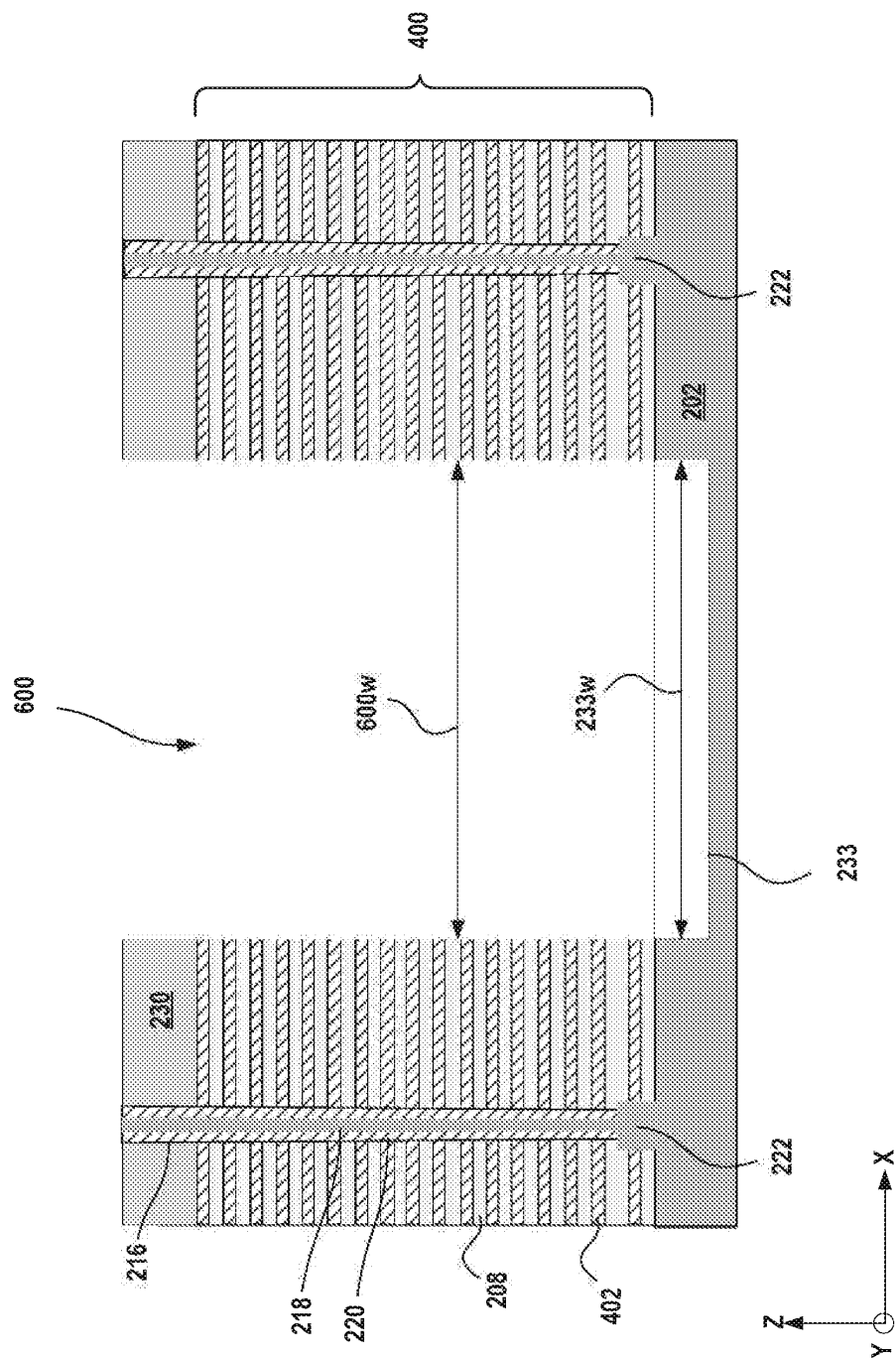


FIG. 6

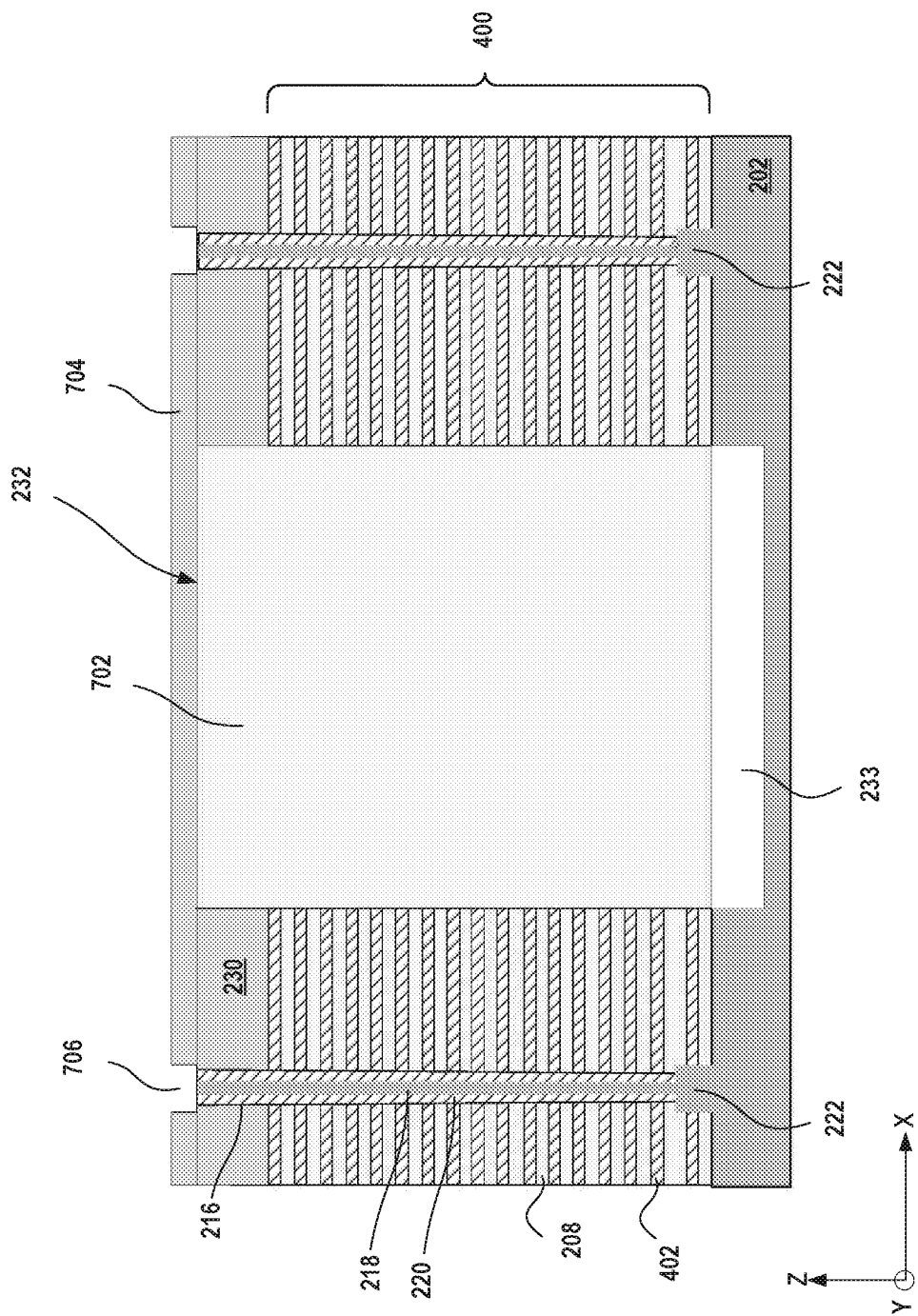


FIG. 7

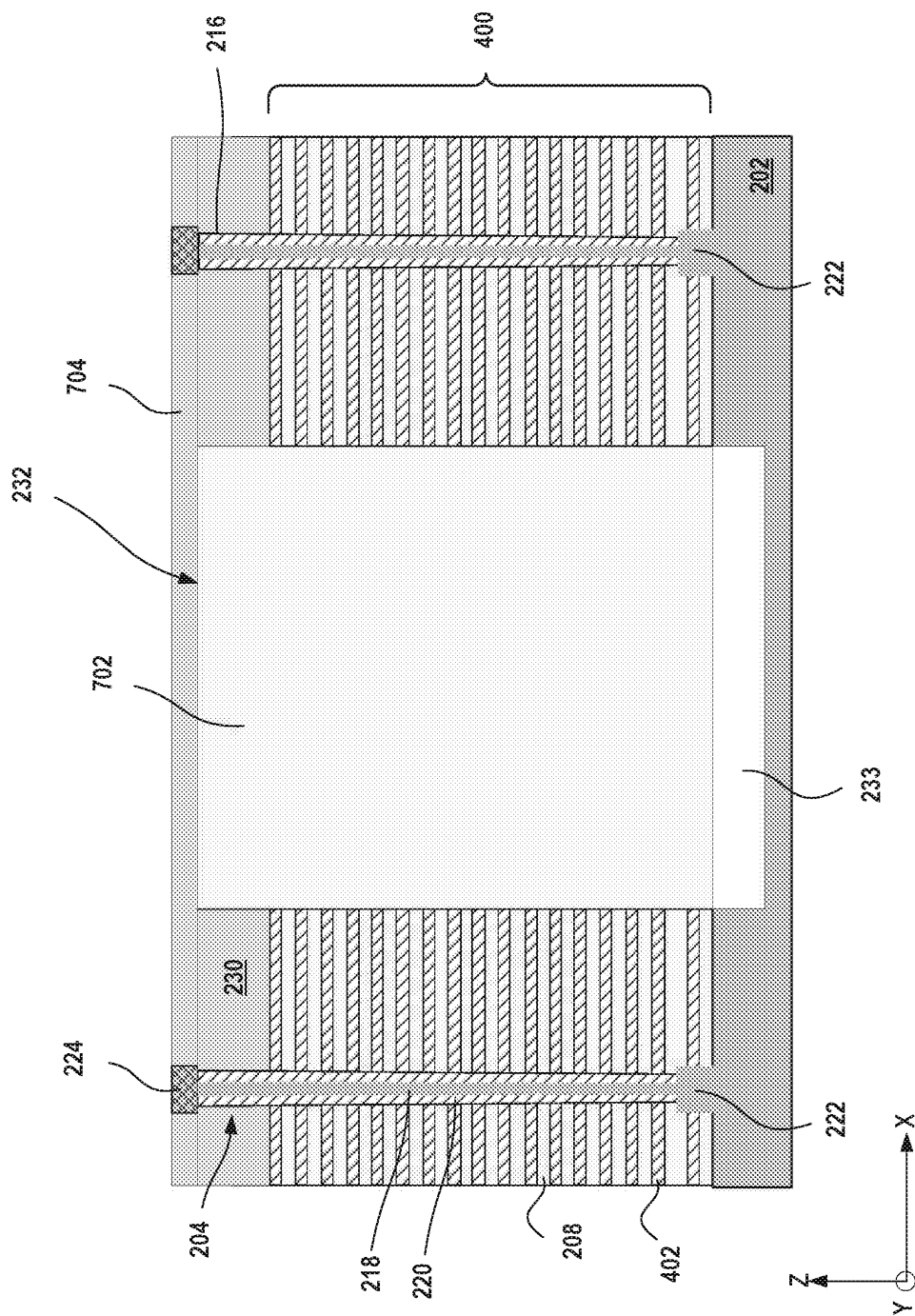


FIG. 8

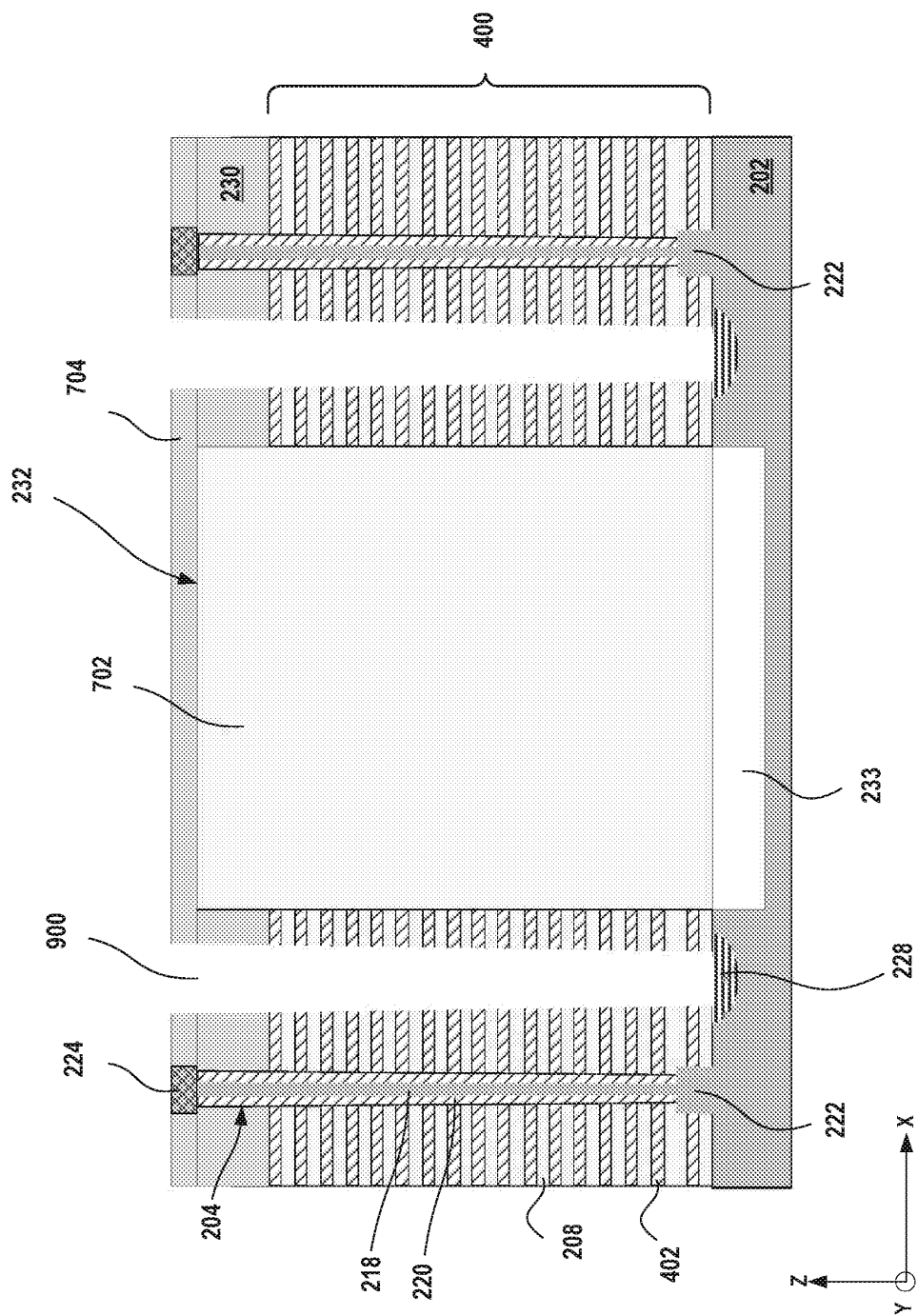


FIG. 9

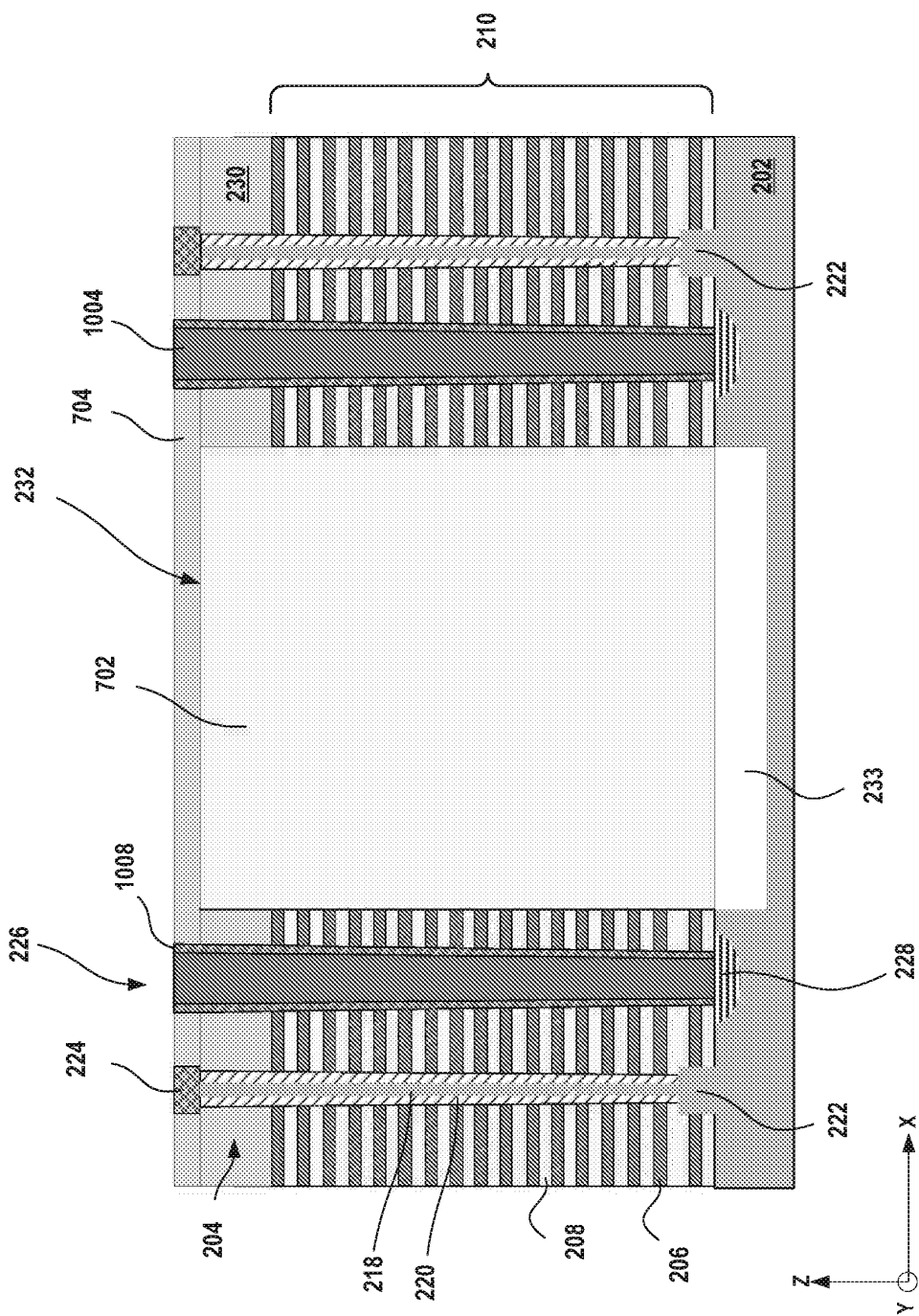
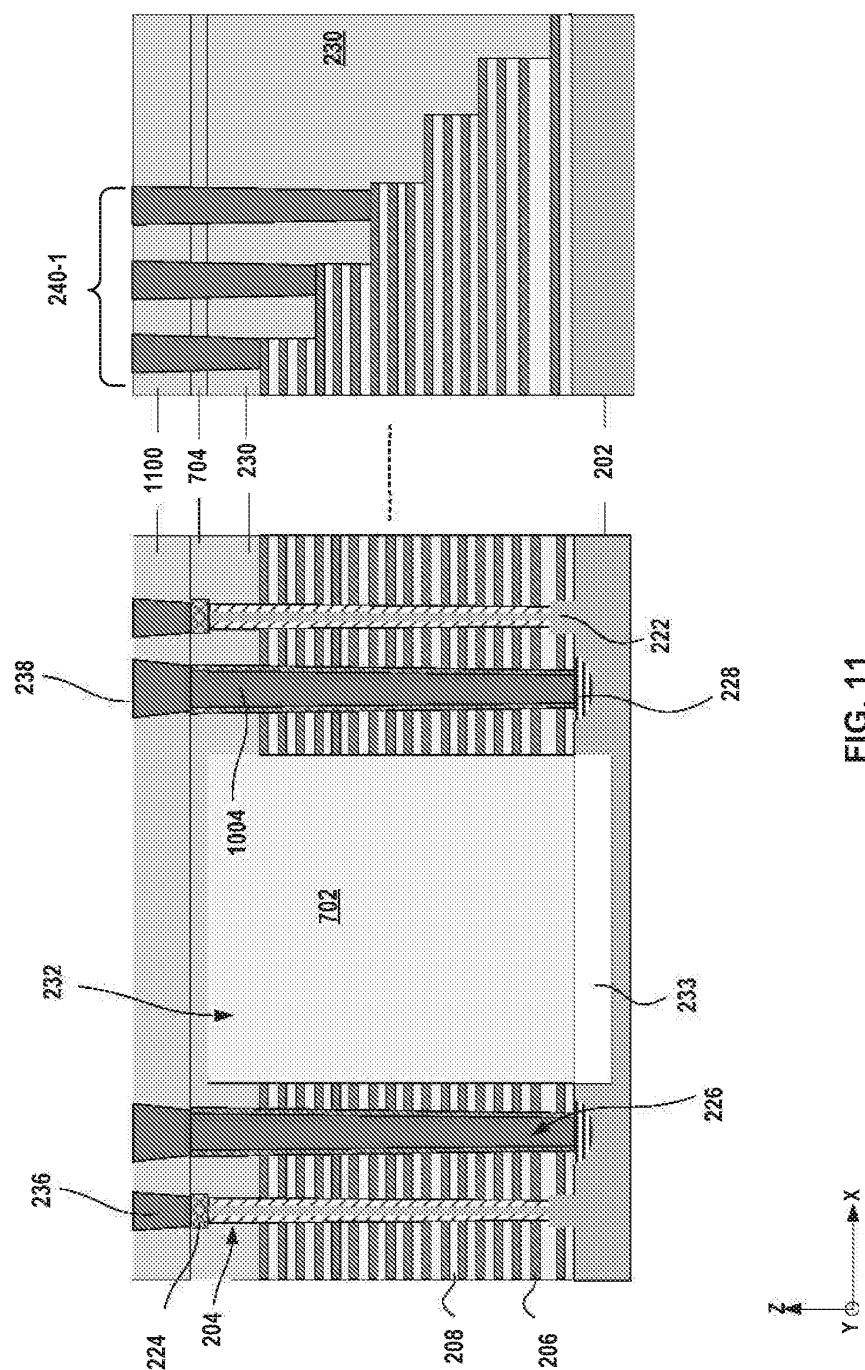


FIG. 10



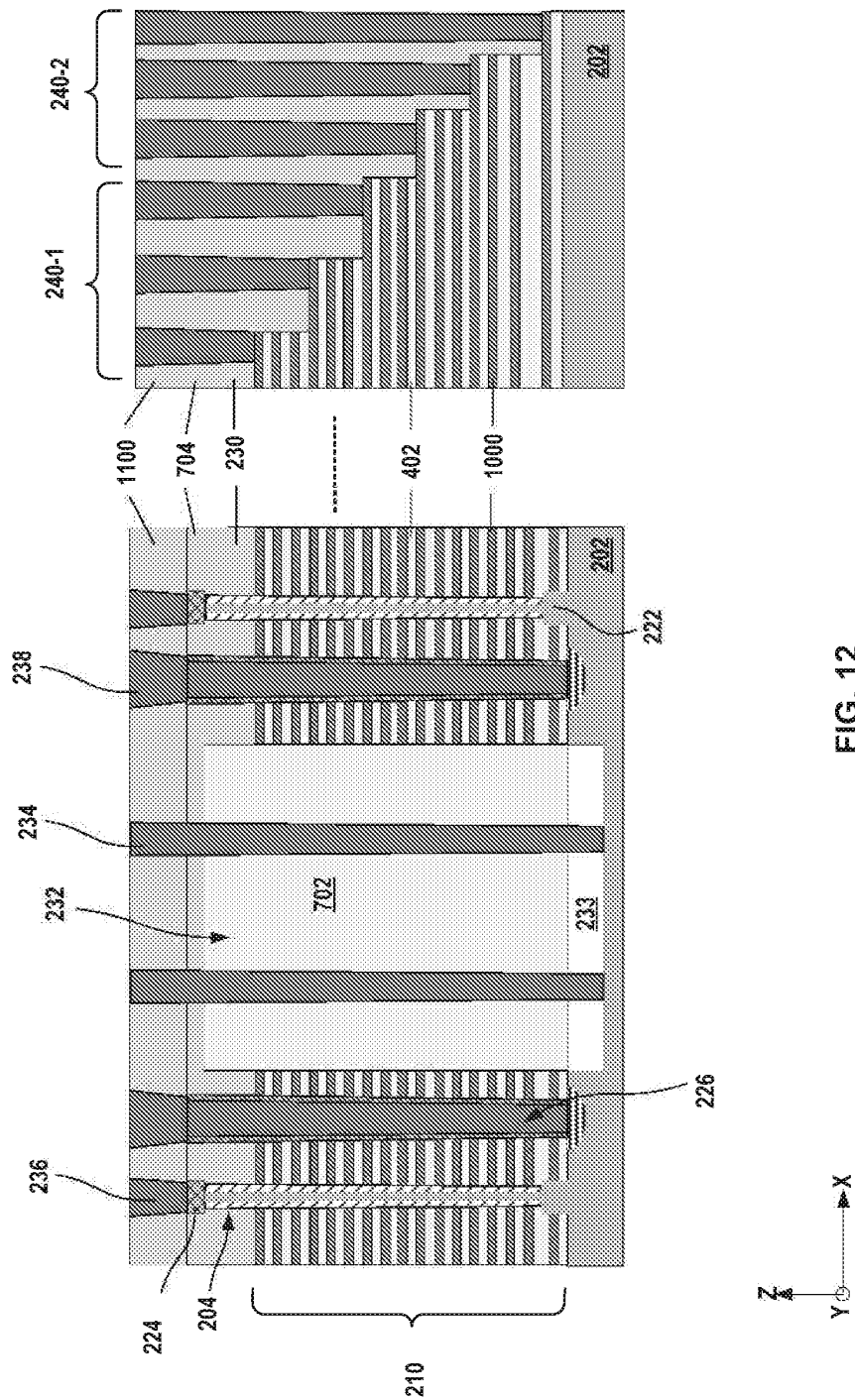


FIG. 12

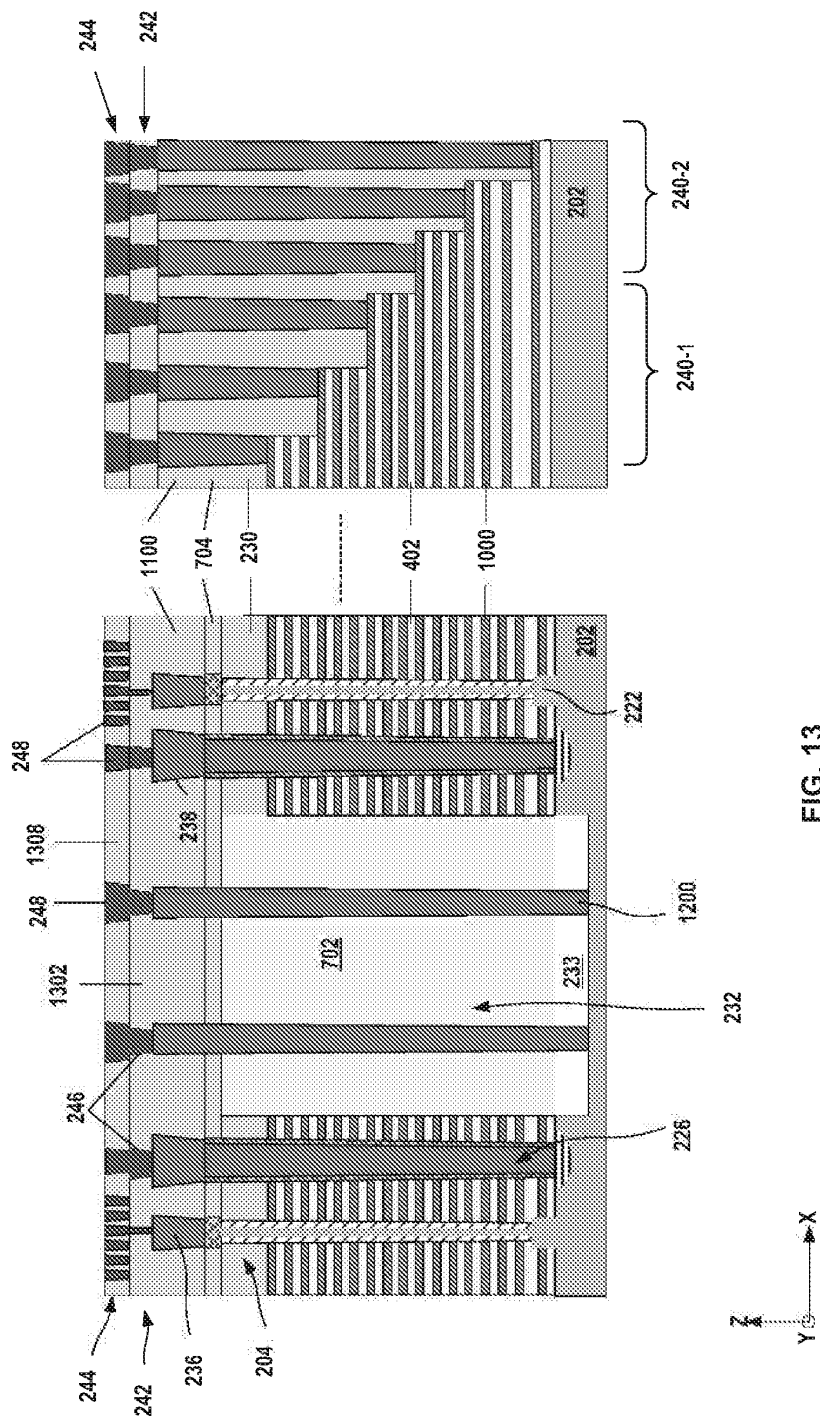


FIG. 13

TRANSMITTAL FOR POWER OF ATTORNEY TO ONE OR MORE REGISTERED PRACTITIONERS

NOTE: This form is to be submitted with the Power of Attorney by Applicant form (PTO/AIA/82B) to identify the application to which the Power of Attorney is directed, in accordance with 37 CFR 1.5, unless the application number and filing date are identified in the Power of Attorney by Applicant form. If neither form PTO/AIA/82A nor form PTO/AIA/82B identifies the application to which the Power of Attorney is directed, the Power of Attorney will not be recognized in the application.

Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Qian TAO
Title	Through Array Contact (TAC) for Three-Dimensional Memory Devices
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123.0190002

SIGNATURE of Applicant or Patent Practitioner

Signature	/Donald J. Featherstone/	Date (Optional)	
Name	Donald J. Featherstone	Registration Number	33,876
Title (if Applicant is a juristic entity)	Attorney for Applicant		
Applicant Name (if Applicant is a juristic entity)		Yangtze Memory Technologies Co., Ltd.	

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.



*Total of 1 (one) forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Doc Code: PA..

Document Description: Power of Attorney

Approved for use through 01/31/2018. GMB 0651-0036
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☒ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above.

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

26111

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☒ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number

26111

OR

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the Applicant (If the Applicant is a juristic entity, list the Applicant name in the box):

Yangtze Memory Technologies Co., Ltd.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

☒ SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

Name

Simon Shi-Ning Yang

Title

CEO

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: TAO *et al.*

Applicant: Yangtze Memory Technologies Co., Ltd.

Application No.: *To Be Assigned*

(Continuation of Appl. No. 16/047,182;
Filed: July 27, 2018)

Filed: *Herewith*

Confirmation No.: *To Be Assigned*

Art Unit: *To Be Assigned*

Examiner: *To Be Assigned*

Atty. Docket: 4123.0190002

Title: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY
DEVICES**

Information Disclosure Statement

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

Listed on accompanying IDS Forms PTO/SB/08a and PTO/SB/08b are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Applicant has checked the appropriate boxes below.

- ☐ 1. Statement under 37 C.F.R. 1.704(d). Each item of information contained in this Information Disclosure Statement: (i) was first cited in any communication from a patent office in a counterpart¹ foreign or international application or from the Office; and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of this information disclosure statement; OR (ii) is a communication that was issued by a patent office in a counterpart foreign or international application or by the Office, and this communication was not received by any individual designated in Sec. 1.56(c) more than thirty days prior to the filing of the information disclosure statement.
- ☒ 2. Filing under 37 C.F.R. § 1.97(b). This Information Disclosure Statement is being filed within three months of the date of filing of a national application other than a continued prosecution application (CPA), OR within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, OR before the mailing date of a first Office Action on the merits OR before the mailing of a first Office Action after the filing of a request for continued examination under 37 C.F.R. § 1.114. No statement or fee is required.
- ☐ 3. Filing under 37 C.F.R. § 1.97(c). This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office

¹ The term counterpart foreign patent application means that a claim for priority has been made in either the U.S. application or a foreign application based on the other, or that the disclosures of the U.S. and foreign patent applications are substantively identical (e.g., an application filed in the European Patent Office claiming the same U.K. priority as claimed in the U.S. application).

Action on the merits, but before the mailing date of a Final Rejection, or Notice of Allowance, or an action that otherwise closes prosecution in the application.

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☐ c. The required fee is provided through online credit card payment authorization in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p).
- ☐ 4. Filing under 37 C.F.R. § 1.97(d) This Information Disclosure Statement is being filed more than three months after the U.S. filing date and after the mailing date of a Final Rejection or Notice of Allowance, but on or before payment of the Issue Fee. The required fee is provided through online credit card payment authorization in the amount of \$240.00 in payment of the fee under 37 C.F.R. § 1.17(p); in addition:

Atty. Dkt. No. 4123.0190002

- ☐ a. Statement under 37 C.F.R. § 1.97(e)(1). I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(1).
- ☐ b. Statement under 37 C.F.R. § 1.97(e)(2). I hereby state that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application and, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 C.F.R. § 1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 C.F.R. § 1.97(e)(2).
- ☒ 5. The patent family for one or more foreign language documents submitted herewith includes a United States patent, and other patent, in the English language. Copies of both the particular foreign patent(s) or published foreign patent applications cited in the foreign patent office communication, and that are not already of record in this application, are enclosed. Copies of the related United States or other English language patent or published application from the family list, if not already of record, are listed on the accompanying SB/08A form. For the purposes of a statement under 37 CFR 1.97(e)(1), the United States or other English language patent or published application are to be construed as being cited by the foreign patent office. MPEP 609.04(b)(V).

Atty. Dkt. No. 4123.0190002

☐ 6. The document(s) was/were cited in a search report by a foreign patent office in a counterpart foreign application. Submission of an English language version of the search report that indicates the degree of relevance found by the foreign office is provided in satisfaction of the requirement for a concise explanation of relevance. MPEP 609.04(a)(III).

☒ 7. A concise explanation of the relevance of the non-English language document(s) appears below in accordance with 37 C.F.R. § 1.98(a)(3).

Document **FP3** (TW 201721921 A) appears to describe a “three dimensional memory device,” as noted in the attached English-language translation of the abstract.

Document **FP5** (CN 105826323 A) appears to describe a “memory element and making method thereof,” as noted in the attached English-language translation of the abstract.

Document **FP7** (CN 106920794 A) appears to describe a “3D NAND memory device and manufacturing method therefor,” as noted in the attached English-language translation of the abstract.

Document **US6** (2019/0057974 A1) is submitted herewith as the English-language counterpart of document **FP6** (CN 106910746 A).

Document **US9** (9,530,789 B2) is submitted herewith as the English-language counterpart of document **FP4** (CN 105047668 A).

Document **US10** (9,595,531 B2) is submitted herewith as the English-language counterpart of document **FP2** (TW 201606388 A).

Document **US11** (9,595,667 B2) is submitted herewith as the English-language counterpart of document **FP1** (TW 201419449 A).

Atty. Dkt. No. 4123.0190002

Document **FP9** (WO 2019/104896 A1) is submitted herewith as the English-language counterpart of document **FP8** (CN 107887395 A).

- ☒ 8. In accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of the U.S. patents and patent application publications cited as documents **US1-US12** on the attached IDS Forms are submitted.
- ☒ 9. Copies of the documents **FP1-FP9** and **NPL1** were cited by or submitted to the Office in an IDS that complies with 37 C.F.R. § 1.98(a)-(c) in Application No. 16/047,182, filed July 27, 2018 (now pending), which is relied upon for an earlier filing date under 35 U.S.C. § 120. Thus, copies of these documents are not attached. 37 C.F.R. § 1.98(d).
- ☒ 10. It is expected that the examiner will review the prosecution and cited art in the parent Application No. 16/047,182, filed July 27, 2018 (now pending), in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.
- ☐ 11. Applicants submit herewith Office Actions from the co-pending U.S. Patent Application No. _____, filed _____, as documents _____ to _____.
The identification of these Office Actions is not to be construed as a waiver of secrecy as to those applications now or upon issuance of the present application as a patent. The Examiner is respectfully requested to consider the cited applications and the art cited therein during examination.

Atty. Dkt. No. 4123.0190002

It is respectfully requested that the Examiner initial and return a copy of the enclosed IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 5/5/2020

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

14933571_1

Atty. Dkt. No. 4123.0190002

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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Sheet	1	of	2	Application Number	To Be Assigned
				Filing Date	Herewith
				First Named Inventor	Qian TAO
				Art Unit	To Be Assigned
				Examiner Name	To Be Assigned
				Attorney Docket Number	4123.0190002

U. S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	US1	US- 2016/0056188 A1	02-25-2016	Lee et al.	
	US2	US- 2016/0071861 A1	03-10-2016	Serov et al.	
	US3	US- 2017/0179026 A1	06-22-2017	Toyama et al.	
	US4	US- 2017/0186758 A1	06-29-2017	Lee et al.	
	US5	US- 2017/0358593 A1	12-14-2017	Yu et al.	
	US6	US- 2019/0057974 A1	02-21-2019	Lu et al.	
	US7	US- 2019/0341399 A1	11-07-2019	Qian Tao	
	US8	US- 8,247,895 B2	08-21-2012	Haensch et al.	
	US9	US- 9,530,789 B2	12-27-2016	Lee et al.	
	US10	US- 9,595,531 B2	03-14-2017	Zhu et al.	
	US11	US- 9,595,667 B2	03-14-2017	Pio	
	US12	US- 9,620,512 B1	04-11-2017	Nishikawa et al.	
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			
		US-			

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	FP1	TW 201419449 A	05-16-2014	MICRON TECHNOLOGY INC		
	FP2	TW 201606388 A	02-16-2016	INTEL CORP		
	FP3	TW 201721921 A	06-16-2017	MACRONIX INT CO LTD		✓
	FP4	CN 105047668 A	11-11-2015	SAMSUNG ELECTRONICS CO LT		
	FP5	CN 105826323 A	08-03-2016	MACRONIX INT CO LTD		✓
	FP6	CN 106910746 A	06-30-2017	YANGTZE MEMORY TECH CO LT		

Examiner
SignatureDate
Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Qian TAO
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123.0190002

IPR2024-00911

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known			
		Application Number	To Be Assigned		
		Filing Date	Herewith		
		First Named Inventor	Qian TAO		
		Art Unit	To Be Assigned		
		Examiner Name	To Be Assigned		
Sheet	1	of	1	Attorney Docket Number	4123.0190002

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2018/085421, mailed January 30, 2019; 9 pages.	

Examiner Signature		Date Considered	
-----------------------	--	--------------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.
1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.
This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO:
Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		
First Named Inventor/Applicant Name:		Qian TAO		
Filer:		Donald J. Featherstone/Catherine Saunders		
Attorney Docket Number:		4123.0190002		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1720

Electronic Acknowledgement Receipt	
EFS ID:	39359737
Application Number:	16867404
International Application Number:	
Confirmation Number:	7018
Title of Invention:	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
First Named Inventor/Applicant Name:	Qian TAO
Customer Number:	26111
Filer:	Donald J. Featherstone/Kim Perry
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0190002
Receipt Date:	05-MAY-2020
Filing Date:	
Time Stamp:	18:59:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1720
RAM confirmation Number	E202055J00245182
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Filing-4123-0190002.pdf	1526145	yes	84
			90cdeab744b73c7f1f55070f49b3dfc9600b08ad6		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Miscellaneous Incoming Letter		1	2	
	Transmittal of New Application		3	3	
	Authorization for Extension of Time all replies		4	4	
	Application Data Sheet		5	17	
	Oath or Declaration filed		18	22	
	Specification		23	53	
	Claims		54	56	
	Abstract		57	57	
	Drawings-other than black and white line drawings		58	72	
	Power of Attorney		73	74	
	Transmittal Letter		75	81	
	Information Disclosure Statement (IDS) Form (SB08)		82	84	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	34942	no	2
			b101f407f5e9e9168e5c7b159054f5d058e27ab		

Warnings:	
Information:	
Total Files Size (in bytes):	1561087
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.	

DONALD J. FEATHERSTONE
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(202) 772-8629
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May 5, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Re: U.S. Non-Provisional Patent Application under 37 C.F.R. § 1.53(b)
(Continuation of Appl. No. 16/047,182; Filed: July 27, 2018)
Appl. No. To Be Assigned; Filed: Herewith)
For: **THROUGH ARRAY CONTACT (TAC) FOR THREE-
DIMENSIONAL MEMORY DEVICES**
Inventors: TAO *et al.*
Our Ref.: 4123.0190002

Commissioner:

The following documents are transmitted herewith for appropriate action by the U.S.
Patent and Trademark Office:

1. Payment made electronically for **\$1,720.00** to cover Patent Application fees (*including basic filing, search, and examination fees*);
2. Utility Patent Application Transmittal Form (PTO/AIA/15);
3. Authorization to Treat a Reply As Incorporating An Extension of Time Under 37 C.F.R. § 1.136(a)(3);
4. U.S. Utility Patent Application entitled:
**THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL
MEMORY DEVICES**

and naming as inventors:

Qian TAO
Yushi HU

Zhenyu LU

Li Hong XIAO
Xiaowang DAI
Yu Ting ZHOU
Zhao Hui TANG
Mei Lan GUO
ZhiWu TANG
Qinxiang WEI

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Commissioner for Patents
May 5, 2020
Page 2

Qianbing XU
Sha Sha LIU
Jian Hua SUN
EnBo WANG

the application consisting of:

- a. An Application Data Sheet (37 C.F.R. § 1.76)(PTO/AIA/14);
- b. A copy of the signed Inventors' Declaration, as originally filed in prior U.S. Appl. No. 16/047,182;
- c. A specification containing:
 - i. 31 pages of description prior to the claims;
 - ii. 3 pages of claims (20 claims);
 - iii. a one (1) page abstract;
- d. 15 sheets of drawings: (*Figures 1A-1C and 2-13*);
5. An executed Power of Attorney by Applicant (PTO/AIA/82B) and the Transmittal for Power of Attorney form (PTO/AIA/82A);
6. An Information Disclosure Statement (IDS); and
7. IDS Forms (3 pages) listing 22 document (**US1-US12, FP1-FP9 and NPL1**).

The above-listed documents are filed electronically.

Fee payment is provided via electronic filing. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/Y-G/cms
Enclosures

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PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

EPAS ID: PAT6096830

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
QIAN TAO	09/12/2018
YUSHI HU	09/12/2018
ZHENYU LU	09/12/2018
LI HONG XIAO	09/12/2018
XIAOWANG DAI	09/12/2018
YU TING ZHOU	09/12/2018
ZHAO HUI TANG	09/12/2018
MEI LAN GUO	09/12/2018
ZHIWU TANG	09/12/2018
QINXIANG WEI	09/12/2018
QIANBING XU	09/12/2018
SHA SHA LIU	09/12/2018
JIAN HUA SUN	09/12/2018
ENBO WANG	09/12/2018
RECEIVING PARTY DATA	
Name:	YANGTZE MEMORY TECHNOLOGIES CO., LTD.
Street Address:	NO. 88 WEILAI 3RD ROAD
Internal Address:	EAST LAKE HIGH-TECH DEVELOPMENT ZONE
City:	WUHAN, HUBEI
State/Country:	CHINA
PROPERTY NUMBERS Total: 1	
Property Type	Number
Application Number:	16867404
CORRESPONDENCE DATA	
Fax Number:	(202)371-2540
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
Phone:	2023712600
Email:	ttopssecretary1@sternekessler.com, ygao@sternekessler.com

Correspondent Name:	STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C
Address Line 1:	1100 NEW YORK AVENUE, N.W.
Address Line 4:	WASHINGTON, D.C. 20005
ATTORNEY DOCKET NUMBER:	4123.0190002
NAME OF SUBMITTER:	DONALD J. FEATHERSTONE
SIGNATURE:	/DONALD J. FEATHERSTONE/
DATE SIGNED:	05/07/2020
	This document serves as an Oath/Declaration (37 CFR 1.63).
Total Attachments: 5 source=2020-05-06-Combined-Declaration-Assignment-4123-0190002#page1.tif source=2020-05-06-Combined-Declaration-Assignment-4123-0190002#page2.tif source=2020-05-06-Combined-Declaration-Assignment-4123-0190002#page3.tif source=2020-05-06-Combined-Declaration-Assignment-4123-0190002#page4.tif source=2020-05-06-Combined-Declaration-Assignment-4123-0190002#page5.tif	

COMBINED DECLARATION AND ASSIGNMENT**DECLARATION**

As the below named inventors, I hereby declare that:

This declaration is directed to:

- ☐ The attached application, or
- ☒ United States application or PCT international application
number 16/047,182
filed on July 27, 2018

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. § 1001 by fine or imprisonment of not more than five (5) years, or both.

ASSIGNMENT

In consideration of the sum of One Dollar (\$1.00) or equivalent and other good and valuable consideration paid to each of the below named inventors, each of the below named inventors, hereby sell and assign to **Yangtze Memory Technologies Co., Ltd.**, a corporation formed under the laws of China, whose mailing address is 18 Gaoxin 4th Road, East Lake High-Tech Development Zone, Wuhan, Hubei, China (hereafter referred to as the Assignee), his/her entire right, title and interest, including the right to sue for past infringement and to collect for all past, present and future damages, for the United States of America (as defined in 35 U.S.C. § 100) and throughout the world,

(a) in the invention(s) known as **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES** for which application(s) for patent in the United States of America is identified above, in any and all applications thereon, in any and all Letters Patent(s) therefor, and

(b) in any and all applications that claim the benefit of the patent application identified above in part (a), including non-provisional applications, continuing (continuation, divisional, or continuation-in-part) applications, reissues, extensions, renewals and reexaminations of the patent application or Letters Patent therefor listed above in part (a), to the full extent of the term or terms for which Letters Patents issue, and

(c) in any and all inventions described in the patent application identified above in part (a), and in any and all forms of intellectual and industrial property protection derivable from such patent application, and that are derivable from any and all continuing applications, reissues, extensions, renewals and reexaminations of such patent application, including, without limitation, patents, applications, utility models, inventor's certificates, and designs together with the right to file applications therefor; and including the right to claim the same priority rights from any previously filed applications under the International Agreement for the Protection of Industrial Property, or any other international agreement, or the domestic laws of the country in which any such application is filed, as may be applicable;

all such rights, title and interest to be held and enjoyed by the above-named Assignee, its successors, legal representatives and assigns to the same extent as all such rights, title and interest would have been held and enjoyed by the Assignor had this assignment and sale not been made.

The below named inventors agree to execute all papers necessary in connection with the application(s) and any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue, reexamination or corresponding application(s) thereof and also to execute separate assignments in connection with such application(s) as the Assignee may deem necessary or expedient.

The below named inventors agree to execute all papers necessary in connection with any patent enforcement action (judicial or otherwise) related to the application(s) or any non-provisional, continuing (continuation, divisional, or continuation-in-part), reissue or reexamination application(s) thereof and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such patent enforcement action.

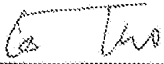
The below named inventors hereby represent that he/she has full right to convey the entire interest herein assigned, and that he/she has not executed, and will not execute, any agreement in conflict therewith.

The below named inventors hereby represent that he/she understands that the patent practitioners associated with **CUSTOMER NUMBER 26111** are the legal representatives of, and attorneys for, the assignee, and are NOT the legal representatives of, and attorneys for, the inventors.

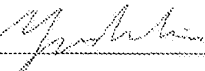
Appl. No. 16/047,182
Atty. Docket No. 4123.0190001

IN WITNESS WHEREOF, executed by the below named inventors on the date opposite his/her name.

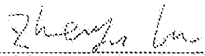
LEGAL NAME OF INVENTOR

Inventor: Qian TAO Date: 2018.9.12Signature of Inventor: 

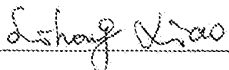
LEGAL NAME OF INVENTOR

Inventor: Yushi HU Date: 2018.9.12Signature of Inventor: 

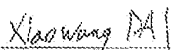
LEGAL NAME OF INVENTOR

Inventor: Zhenyu LU Date: 2018.09.12Signature of Inventor: 

LEGAL NAME OF INVENTOR

Inventor: Li Hong XIAO Date: 2018.09.12Signature of Inventor: 

LEGAL NAME OF INVENTOR

Inventor: Xiaowang DAI Date: 2018.9.12Signature of Inventor: 

Appl. No. 16/047,182
Atty. Docket No. 4123.0190001

LEGAL NAME OF INVENTOR

Inventor: Yu Ting ZHOU Date: 2018.09.12

Signature of Inventor: Yu Ting ZHOU 2018.09.12

LEGAL NAME OF INVENTOR

Inventor: Zhao Hui TANG Date: 2018.09.12

Signature of Inventor: Zhao Hui TANG

LEGAL NAME OF INVENTOR

Inventor: Mei Lan GUO Date: 2018.9.12

Signature of Inventor: [Signature]

LEGAL NAME OF INVENTOR

Inventor: Zhi Wu TANG Date: 2018.09.12

Signature of Inventor: Zhi Wu TANG 2018.09.12

LEGAL NAME OF INVENTOR

Inventor: Qinxiang WEI Date: 2018.09.12

Signature of Inventor: Qinxiang WEI

Appl. No. 16/047,182
Atty. Docket No. 4123.0190001

LEGAL NAME OF INVENTOR

Inventor: Qianbing XU Date: 2018.9.12

Signature of Inventor: Qianbing XU

LEGAL NAME OF INVENTOR

Inventor: Sha Sha LIU Date: 2018.9.12

Signature of Inventor: Sha Sha LIU

LEGAL NAME OF INVENTOR

Inventor: Jian Hua SUN Date: 2018/9/12

Signature of Inventor: Jian Hua Sun

LEGAL NAME OF INVENTOR

Inventor: EnBo WANG Date: 2018.9.12

Signature of Inventor: Wang Enbo

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/867,404	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 = *				x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 460 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1720
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)
	Total (37 CFR 1.16(i))	*	Minus **	=	x =		x =
	Independent (37 CFR 1.16(h))	*	Minus ***	=	x =		x =
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
			TOTAL ADD'L FEE			TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO.	TOT CLAIMS	IND CLAIMS
16/867,404	05/05/2020	2872	1720	4123.0190002	20	3

CONFIRMATION NO. 7018

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

FILING RECEIPT



0000000116923798

Date Mailed: 05/12/2020

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Qian TAO, Wuhan, CHINA;
Yushi Hu, Wuhan, CHINA;
Zhenyu Lu, Wuhan, CHINA;
Li Hong Xiao, Wuhan, CHINA;
Xiaowang Dai, Wuhan, CHINA;
Yu Ting Zhou, Wuhan, CHINA;
Zhao Hui Tang, Wuhan, CHINA;
Mei Lan Guo, Wuhan, CHINA;
ZhiWu Tang, Wuhan, CHINA;
Qinxiang Wei, Wuhan, CHINA;
Qianbing Xu, Wuhan, CHINA;
Sha Sha Liu, Wuhan, CHINA;
Jian Hua Sun, Wuhan, CHINA;
EnBo Wang, Wuhan, CHINA;

Applicant(s)

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA;

Assignment For Published Patent Application

Yangtze Memory Technologies Co., Ltd., Wuhan, CHINA

Power of Attorney: The patent practitioners associated with Customer Number 26111

Domestic Priority data as claimed by applicant

This application is a CON of 16/047,182 07/27/2018 PAT 10658378

page 1 of 4

which is a CON of PCT/CN2018/085421 05/03/2018

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 05/11/2020

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/867,404**

Projected Publication Date: 08/20/2020

Non-Publication Request: No

Early Publication Request: No

Title

THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

Preliminary Class

359

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/867,404	05/05/2020	Qian TAO	4123.0190002	7018
26111	7590	06/23/2020		
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER CHOI, CALVIN Y	
			ART UNIT	PAPER NUMBER
			2812	
			NOTIFICATION DATE	DELIVERY MODE
			06/23/2020	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

e-office@sternekessler.com

DETAILED ACTION

1. This Office Action is in response to the application filed on 05 May 2020.

Notice of Pre-AIA or AIA Status

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Objections

3. Claim 12 objected to because of the following informalities: claim 12 recites the limitation of “the substrate” without apparent antecedent basis. For the purpose of Examination, the limitation will be read as “a substrate”. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.
5. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claim(s) 1-16 and 18-20 is/are rejected under 35 U.S.C. 103 as being unpatentable over Pachamuthu et al. (US 9,659,956 B1; hereinafter *Pachamuthu*), in view of Lee et al. (US 2017/0186758 A1; hereinafter *Lee*).**

7. In regards to claim 1, *Pachamuthu* teaches a three-dimensional (3D) memory device, comprising:

- an alternating layer stack (32/42) (col. 22/lns. 49-50);
- a dielectric structure (74) extending vertically through the alternating layer stack (fig. 11; col. 24/lns. 20-25);
- a through array contact (TAC) (76) extending vertically through the dielectric structure (fig. 11; col. 24/lns. 18-25);
- a channel structure (11/55) extending vertically through the alternating layer stack (fig. 8; col. 16/lns. 17-30);
- an epitaxial layer (10) under the channel structure (col. 5/lns. 17-23);
- an etch stop plug (71) on the channel structure (fig. 6; col. 12/lns. 56-58);
- a staircase structure (evidenced by (300)) in the alternating layer stack (fig. 6; col. 5/lns. 4-8); and
- slit structures (e.g. (7P)) extending vertically in the alternating layer stack (fig. 11).

8. *Pachamuthu* appears to be silent as to, but does not preclude, the elements of a contact layer on the TAC, the channel structure, and the slit structures. *Lee* teaches the elements of a contact layer (e.g. (BL) over (113/118)) on the TAC, the channel structure, and the slit structures (e.g. figs. 2-3; [0081], [0087-0088]). It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the device taught by *Pachamuthu* with the aforementioned elements taught by *Lee* to improve integration of a 3D memory device (*Lee* [0005]).

9. **In regards to claim 2**, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 1. *Pachamuthu* further teaches the elements wherein the dielectric structure abuts a sidewall surface of the TAC (fig. 11: e.g. (74) abuts (76); col. 24/lns. 20-25, 48-50).

10. **In regards to claim 3**, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 1. *Pachamuthu* further teaches the elements wherein the 3D memory device is a NAND 3D memory device (col. 24/lns. 43-45).

11. In regards to claim 4, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 1. *Pachamuthu* further teaches, e.g. in figs. 9B-9D, the elements wherein the alternating layer stack comprises alternating pairs of a dielectric (32) (col. 22/lns. 49-50) and a conductor layer (46) (col. 18/lns. 55-67).

12. In regards to claim 5, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 1. *Pachamuthu* further teaches the elements wherein the dielectric structure (74) (col. 19/lns. 16-20) comprises silicon oxide (32) (col. 22/lns. 49-50).

13. In regards to claim 6, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 1. *Pachamuthu* further teaches the elements wherein the dielectric structure comprises an oxide material (fig. 11: (74); col. 24/lns. 20-25).

14. In regards to claim 7, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 1. *Pachamuthu* further teaches the elements wherein the dielectric structure defines a through array contact region within the 3D memory device (fig. 11: (76); col. 24/lns. 18-25).

15. In regards to claim 8, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 1. *Pachamuthu* further teaches the elements further comprising an isolation region (120) (col. 4/lns. 11-14) on a semiconductor substrate and the dielectric structure (74) has a footprint equal to or smaller than the isolation region (fig. 11: (74) appears to be smaller in the x-direction compared to (120)).

16. In regards to claim 9, *Pachamuthu* teaches a three-dimensional (3D) memory device, comprising:

- an alternating conductor (46)/dielectric layer (32) stack (figs. 9B-9D: col. 18/lns. 55-67, col. 22/lns. 49-50);
- a dielectric structure (74) extending vertically through the alternating conductor/dielectric layer stack (fig. 11; col. 24/lns. 20-25);

- channel structures (11/55) and slit structures (e.g. (7P)) extending vertically through the alternating conductor/dielectric layer stack (figs. 8 and 11; col. 16/lns. 17-30);
- a staircase structure (evidenced by (300)) disposed in the alternating conductor/dielectric layer stack (fig. 6; col. 5/lns. 4-8), wherein the staircase structure comprises levels with each level having a conductor layer thereon (fig. 11: (8C); col. 23/lns. 30-33); and
- through array contacts (TACs) (76) extending vertically through the dielectric structure (fig. 11; col. 24/lns. 18-25).

17. *Pachamuthu* appears to be silent as to, but does not preclude, the elements of local contacts disposed on the channel structures and the slit structures. *Lee* teaches the elements of local contacts (e.g. (BL) over (113/118)) disposed on the channel structures and the slit structures (e.g. figs. 2-3; [0081], [0087-0088]). It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the device taught by *Pachamuthu* with the aforementioned elements taught by *Lee* to improve integration of a 3D memory device (*Lee* [0005]).

18. In regards to claim 10, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 9. *Pachamuthu* further teaches the elements wherein the dielectric structure abuts a sidewall of each TAC of the TACs (fig. 11: e.g. (74) abuts (76); col. 24/lns. 20-25, 48-50).

19. In regards to claim 11, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 9. *Pachamuthu* further teaches the elements wherein the dielectric structure (74) comprises a through array contact region (76) of the 3D memory device (fig. 11; col. 24/lns. 18-25, 43-45).

20. In regards to claim 12, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 9. *Pachamuthu* further teaches the elements further comprising: an etch stop plug (71) over each channel structure of the channel structures (fig. 6; col. 12/lns. 56-58); and an epitaxial layer (10) (col. 5/lns. 17-23) disposed between the channel structure structures and a substrate

(9) (col. 5/lns. 17-23). *Lee* further teaches the elements of local contacts (e.g. (BL) over (113/118)) disposed on the channel structures (e.g. figs. 2-3; [0081], [0087-0088]). It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the device taught by *Pachamuthu* with the aforementioned elements taught by *Lee* to improve integration of a 3D memory device (*Lee* [0005]).

21. In regards to claim 13, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 9. *Pachamuthu* further teaches the elements wherein the dielectric material (74) (col. 19/lns. 16-20) comprises silicon oxide (32) (col. 22/lns. 49-50).

22. In regards to claim 14, the combination of *Pachamuthu* and *Lee* teaches the device discussed above in addressing claim 9. *Pachamuthu* further teaches the elements wherein the TACs comprise a conductive material (fig. 11: (76); col. 24/lns. 18-25).

23. In regards to claim 15, *Pachamuthu* teaches a method for forming a 3D memory device, the method comprising:

- disposing an alternating dielectric layer stack (32/42) (col. 22/lns. 49-50) on a substrate (9) (col. 5/lns. 17-20);
- disposing a staircase structure (evidenced by (300)) in the alternating dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon; (fig. 11: (8C); col. 23/lns. 30-33)
- forming a channel structure (e.g. (11/55)) extending vertically in the alternating dielectric layer stack (figs. 8; col. 16/lns. 17-30);
- forming a first opening (e.g. (76)) in the alternating dielectric layer stack (figs. 9; col. 19/lns. 46-52);
- filling the first opening with a dielectric layer (74) (fig. 11; col. 24/lns. 20-25);

- removing portions of the dielectric structure until the substrate is exposed to form a second opening that vertically extends through the dielectric structure (fig. 11: evidenced by (76); col. 24/lns. 48-50); and
- filling the second opening with a conductor to form a through array contact (TAC) structure in contact with the substrate (fig. 11: evidenced by (76); col. 24/lns. 18-25).

24. *Pachamuthu* appears to be silent as to, but does not preclude, the steps of disposing a local contact on the channel structure and the TAC structure. *Lee* teaches the steps of disposing a local contact (e.g. (BL) over (113/118)) on the channel structure and the TAC structure (e.g. figs. 2-3; [0081], [0087-0088]). It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the method taught by *Pachamuthu* with the aforementioned steps taught by *Lee* to improve integration of a 3D memory device (*Lee* [0005]).

25. In regards to claim 16, the combination of *Pachamuthu* and *Lee* teaches the method discussed above in addressing claim 15. *Pachamuthu* further teaches the steps further comprising: forming slit openings (79) (figs. 8) extending vertically in the alternating dielectric layer stack, wherein the slit openings expose a doped region (61) of the substrate (fig. 8C); replacing a dielectric layer (e.g. (42), evidenced by (143)) of the alternating dielectric layer stack through the slit openings with the conductor layer (46) to convert the alternating dielectric layer stack to an alternating dielectric/conductor layer stack (figs. 9B-9D; col. 18/lns. 55-67); and filling the slit openings with a conductor (76) (fig. 8D).

26. In regards to claim 18, the combination of *Pachamuthu* and *Lee* teaches the method discussed above in addressing claim 15. *Pachamuthu* further teaches the steps wherein filling the first opening with the dielectric layer comprises depositing the dielectric layer (74L) with a chemical vapor deposition, a plasma-enhanced chemical vapor deposition, or a physical vapor deposition process (fig. 9F; col. 20/lns. 17-20).

27. In regards to claim 19, the combination of *Pachamuthu* and *Lee* teaches the method discussed above in addressing claim 15. *Pachamuthu* further teaches the steps wherein filling the first opening with the dielectric layer comprises depositing an oxide material (74) (fig. 11; col. 24/lns. 20-25).

28. In regards to claim 20, the combination of *Pachamuthu* and *Lee* teaches the method discussed above in addressing claim 15. *Pachamuthu* further teaches the steps wherein disposing the alternating dielectric layer stack comprises alternately disposing a first dielectric layer comprising an oxide material (32) and a second dielectric layer comprising a nitride material (42) (figs. 8; col. 15/lns. 15-16).

29. Claim(s) 17 is/are rejected under 35 U.S.C. 103 as being unpatentable over the combination of *Pachamuthu* and *Lee* as applied to claim 15 above, and further in view of Gunji-Yoneoka et al. (US 2017/0365613 A1; hereinafter *Gunji-Yoneoka*).

30. In regards to claim 17, the combination of *Pachamuthu* and *Lee* teaches the method discussed above in addressing claim 15. The combination of *Pachamuthu* and *Lee* appears to be silent as to, but does not preclude, the steps wherein disposing the staircase structure comprises performing a trim-etch process in the alternating dielectric layer stack before forming the channel structure. *Gunji-Yoneoka* teaches the steps wherein disposing the staircase structure comprises performing a trim-etch process in the alternating dielectric layer stack before forming the channel structure (figs. 2-4). It would have been obvious to one having ordinary skill in the art at the time the application at hand was filed to modify the method taught by the combination of *Pachamuthu* and *Lee* with the aforementioned steps taught by *Gunji-Yoneoka* to minimize the use of masks in a lithographic process.

Conclusion

31. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CALVIN Y CHOI whose telephone number is (571)270-7882. The examiner can normally be reached on M-F 9-5.

32. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

33. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

34. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CALVIN Y. CHOI
Primary Examiner
Art Unit 2812

/CALVIN Y CHOI/
Primary Examiner, Art Unit 2812

Notice of References Cited	Application/Control No. 16/867,404		Applicant(s)/Patent Under Reexamination TAO et al.	
	Examiner CALVIN Y CHOI		Art Unit 2812	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-9659956-B1	05-2017	Pachamuthu; Jayavel	H01L27/11529	1/1
*	B	US-20170186758-A1	06-2017	LEE; Changhyun	G11C16/10	1/1
*	C	US-20170365613-A1	12-2017	GUNJI-YONEOKA; Marika	H01L27/11524	1/1
	D					
	E					
	F					
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	I					
	J					
	K					
	L					
	M					

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
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	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 16/867,404	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

CPC - Searched*		
Symbol	Date	Examiner
H01L27/11524,11529,11578-11582,1157,11551-11556.cpc. or H01L29/40114,40117.cpc. or H01L21/0223.cpc.	06/06/2020	CYC
H01L27/11582,1157,11573.cpc. or H01L29/40117.cpc. or H01L21/76802,76877.cpc. or H01L23/5226.cpc.	06/06/2020	CYC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
257	324.ccls.	06/06/2020	CYC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
H01L27/11524,11529,11578-11582,1157,11551-11556.cpc. or H01L29/40114,40117.cpc. or H01L21/0223.cpc.	06/06/2020	CYC
H01L27/11582,1157,11573.cpc. or H01L29/40117.cpc. or H01L21/76802,76877.cpc. or H01L23/5226.cpc.	06/06/2020	CYC
257/324.ccls.	06/06/2020	CYC
Inventor, assignee, and text search using EAST - please refer to search history.	06/06/2020	CYC

/CALVIN Y CHOI/ Primary Examiner, Art Unit 2812	
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<i>Search Notes</i> 	Application/Control No. 16/867,404	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/CALVIN Y CHOI/ Primary Examiner, Art Unit 2812	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	3,233	(Yangtze Memory Technologies).as. or Yao-Lan.in. or Xue-Lei.in.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/06 17:03
S2	56,151	257/324.ccls. or H01L27/11524,11529,11578-11582,1157,11551-11556.cpc. or H01L29/40114,40117.cpc. or H01L21/0223.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/06 17:05
S3	621	S1 and S2	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/06 17:05
S5	3,233	(Yangtze Memory Technologies).as. or Yao-Lan.in. or Xue-Lei.in.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/06 18:54
S6	56,151	257/324.ccls. or H01L27/11524,11529,11578-11582,1157,11551-11556.cpc. or H01L29/40114,40117.cpc. or H01L21/0223.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/06 18:54
S7	85	S5 and S6 and alternat\$5 near2 (dielectric or insulat\$5) near2 stack	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/06 18:54
S8	29	S5 and S6 and alternat\$5 near2 (dielectric or insulat\$5) near2 stack and epitaxial near2 (layer or film)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/06 19:10

S9	254	S6 and alternat\$5 near2 (dielectric or insulat\$5) near2 stack and epitaxial near2 (layer or film)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/06 19:33
S10	20	S6 and alternat\$5 near2 (dielectric or insulat\$5) near2 stack same epitaxial near2 (layer or film)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/06 19:36
S11	59	S6 and alternat\$5 near2 (dielectric or insulat\$5) near2 stack same2 epitaxial near2 (layer or film)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/06 20:30
S12	3	("20170365612" "20190067322" "20180337195").PN.	US-PGPUB; USPAT	ADJ	ON	2020/06/06 23:41
S13	56,154	257/324.ccls. or H01L27/11524,11529,11578- 11582,1157,11551-11556.cpc. or H01L29/40114,40117.cpc. or H01L21/0223.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 02:02
S14	137	S13 and vertical near2 structure same storage near2 layer and vertical near2 structure with (etch\$4 or remov\$4)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 02:02
S15	138	S13 and vertical near2 structure same storage near2 layer and (storage near2 layer) with (etch\$4 or remov\$4)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 02:21
S16	10	S13 and vertical near2 structure same storage near2 layer and (storage near2 layer) with (etch\$4 or remov\$4) same epitaxial near2 (layer or film)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 02:22
S17	3,627	(YANGTZE MEMORY TECHNOLOGIES).as. or Wei-Qinxiang.in. or Sun-Jianhua.in. or Xia-Ji.in.	US-PGPUB; USPAT; FPRS; EPO; JPO;	ADJ	ON	2020/06/07 17:01

			DERWENT; IBM_TDB			
S18	56,154	257/324.ccls. or H01L27/11524,11529,11578- 11582,1157,11551-11556.cpc. or H01L29/40114,40117.cpc. or H01L21/0223.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 17:02
S19	87,330	257/324.ccls. or H01L27/11582,1157,11573.cpc. or H01L29/40117.cpc. or H01L21/76802,76877.cpc. or H01L23/5226.cpc.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 17:02
S20	1	("9087790").PN.	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:02
S21	98	S17 and S18	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:12
S22	100	S17 and S19	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:12
S23	4	S21 and (dummy or sacrificial) near2 (hole or opening or trench or via) same spacer with (hollow or hole or empty)	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:24
S24	42	(3D or three\$1dimension\$4) near2 (memory) and (dummy or sacrificial) near2 (hole or opening or trench or via) same spacer with (hollow or hole or empty)	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:32
S25	10	(3D or three\$1dimension\$4) near2 (memory) and (dummy or sacrificial) near2 (hole or opening or trench or via) same spacer with (hollow or empty or void or gap)	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:34
S26	10	(3D or three\$1dimension\$4) near2 (memory) and (dummy or sacrificial) near2 (hole or opening or trench or via) same spacer with (hollow\$4 or empty or void or gap)	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:34
S27	28	(3D or three\$1dimension\$4) near2 (memory) and (dummy or sacrificial) with (hole or opening or trench or via) same spacer with (hollow\$4 or empty or void or gap)	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:36
S28	0	(3D or three\$1dimension\$4) near2 (memory) and through\$1stair\$1contact	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:39
S29	3,131	(3D or three\$1dimension\$4) near2 (memory) and through near2 contact	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:39

S30	4,403	S18 and through near2 contact	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:40
S31	8,781	(S18 or S19) and through near2 contact	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:41
S32	27	(S18 or S19) and through near2 contact and (dummy or sacrificial) with (hole or opening or trench or via) same spacer with (hollow\$4 or empty or void or gap)	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:41
S33	0	(S18 or S19) and through near2 contact and (dummy or sacrificial) near2 channel same (hole or opening or trench or via) same spacer with (hollow\$4 or empty or void or gap)	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:47
S34	1	(S18 or S19) and through near2 contact and (dummy or sacrificial) near2 channel same spacer with (hollow\$4 or empty or void or gap)	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:48
S35	2	(3D or three\$1dimension\$4) near2 (memory) and (dummy or sacrificial) near2 channel same spacer with (hollow\$4 or empty or void or gap)	US-PGPUB; USPAT	ADJ	ON	2020/06/07 17:49
S36	2	(3D or three\$1dimension\$4) near2 (memory) and (dummy or sacrificial) near2 channel same spacer with (hollow\$4 or empty or void or gap)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 17:49
S37	4	(3D or three\$1dimension\$4) near2 (memory) and (dummy or sacrificial) with channel same spacer with (hollow\$4 or empty or void or gap)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 18:21
S38	68	(dummy or sacrificial) with channel same (via or trench) same spacer with (hollow\$4 or empty or void or gap)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 18:23
S39	17	(dummy or sacrificial) with channel same (via or trench) same spacer with (hollow\$4 or empty or void or gap) and memory	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 18:24
S40	64	(dummy or sacrificial) with channel same (via or trench) same (spacer or fill\$4 or	US-PGPUB; USPAT; FPRS; EPO;	ADJ	ON	2020/06/07 18:34

		liner or lining) with (hollow\$4 or empty or void or gap) and memory	JPO; DERWENT; IBM_TDB			
S41	21	(dummy or sacrificial) with channel same (via or trench) same (spacer or fill\$4 or liner or lining) with (hollow\$4 or empty or void or gap) and (3D or three\$1dimension\$4) near2 (memory)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 18:34
S42	44	(dummy or sacrificial) with channel same (via or trench) same (spacer or fill\$4 or liner or lining) with (hollow\$4 or empty or void or gap) and (S18 or S19)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 18:34
S43	38	through near2 (silicon or semiconductor) near2 via and dummy near2 spacer	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 19:16
S44	5	through near2 (silicon or semiconductor) near2 via and (dummy or sacrificial) near2 spacer with (void or gap)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 19:16
S45	0	through near2 (silicon or semiconductor) near2 via same (dummy or sacrificial) near2 spacer with (void or gap)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/07 19:16
S46	1	(15/279959).APP.	USPAT; USOCR	ADJ	ON	2020/06/07 19:53
S47	3,028	(Yangtze Memory Technologies).as. or TAO-Qian.in. or Hu-Yushi.in. or Lu-Zhenyu.in. or Xiao-Li-Hong.in. or Dai-Xiaowang.in. or Zhou-Yu-Ting.in. or Tang-Zhao-Hui.in. or Guo-Mei-Lan.in. or Tang-ZhiWu.in. or Wei-Qinxiang.in. or Xu-Qianbing.in. or Liu-Sha-Sha.in. or Sun-Jian-Hua.in. or Wang-EnBo.in.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/13 14:12
S48	11	(TAC or through\$1array\$1contact or TSC or through\$1stair\$1contact) same (channel or memory) same local near2 contact	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/13 17:02

S49	12	("20160056188" "20160071861" "20170179026" "20170186758" "20170358593" "20190057974" "20190341399" "8247895" "9530789" "9595531" "9595667" "9620512").PN.	US-PGPUB; USPAT	ADJ	ON	2020/06/13 17:03
S50	157	(TAC or through\$1array\$1contact or TSC or through\$1stair\$1contact) same (channel or memory) same ((local near2 contact) or interconnect\$4 or inter\$1connect\$4 or trace)	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/13 17:09
S51	34	("20160056188" "20160071861" "20170179026" "20170186758" "20170358593" "20190057974" "20190341399" "8247895" "9530789" "9595531" "9595667" "9620512").PN.	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/13 17:09
S52	19	S51 and contact	US-PGPUB; USPAT; FPRS; EPO; JPO; DERWENT; IBM_TDB	ADJ	ON	2020/06/13 17:09
S53	0	(15/458273).APP.	USPAT; USOCR	ADJ	ON	2020/06/13 18:27

EAST Search History (Interference)

<This search history is empty>

6/19/2020 2:55:01 AM

C:\Users\cchoi2\Documents\EAST\Workspaces\16867404 - Tao et al.wsp

Bibliographic Data

Application No: 16/867,404

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged: /CALVIN Y CHOI/

Examiner's Signature

Initials

Title:

THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
05/05/2020	257	2812	4123.0190002
RULE			

APPLICANTS

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CONTINUING DATA

This application is a CON of 16047182 07/27/2018 PAT 10658378

16047182 is a CON of PCT/CN2018/085421 05/03/2018

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

05/11/2020

STATE OR COUNTRY

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WASHINGTON, DC 20005

UNITED STATES

FILING FEE RECEIVED

\$1,720

PTO/SB/08a (07-09)

Approved for use through 11/30/2020. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known	
		Application Number	To Be Assigned
		Filing Date	Herewith
		First Named Inventor	Qian TAO
		Art Unit	To Be Assigned
		Examiner Name	To Be Assigned
Sheet 1 of 2	Attorney Docket Number	4123.0190002	

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code ² (if known)			
	US1	US- 2016/0056188 A1	02-25-2016	Lee et al.	
	US2	US- 2016/0071861 A1	03-10-2016	Serov et al.	
	US3	US- 2017/0179026 A1	06-22-2017	Toyama et al.	
	US4	US- 2017/0186758 A1	06-29-2017	Lee et al.	
	US5	US- 2017/0358593 A1	12-14-2017	Yu et al.	
	US6	US- 2019/0057974 A1	02-21-2019	Lu et al.	
	US7	US- 2019/0341399 A1	11-07-2019	Qian Tao	
	US8	US- 8,247,895 B2	08-21-2012	Haensch et al.	
	US9	US- 9,530,789 B2	12-27-2016	Lee et al.	
	US10	US- 9,595,531 B2	03-14-2017	Zhu et al.	
	US11	US- 9,595,667 B2	03-14-2017	Pio	
	US12	US- 9,620,512 B1	04-11-2017	Nishikawa et al.	
		US-			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
		Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)				
	FP1	TW 201419449 A	05-16-2014	MICRON TECHNOLOGY INC		
	FP2	TW 201606388 A	02-16-2016	INTEL CORP		
	FP3	TW 201721921 A	06-16-2017	MACRONIX INT CO LTD		✓
	FP4	CN 105047668 A	11-11-2015	SAMSUNG ELECTRONICS CO LT		
	FP5	CN 105826323 A	08-03-2016	MACRONIX INT CO LTD		✓
	FP6	CN 106910746 A	06-30-2017	YANGTZE MEMORY TECH CO LT		

Examiner Signature	Date Considered
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Micron Ex. 1002, p. 124
Micron v. YMT
IPR2024-00911

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Complete if Known

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Sheet	2	of	2
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Application Number	To Be Assigned
Filing Date	Herewith
First Named Inventor	Qian TAO
Art Unit	To Be Assigned
Examiner Name	To Be Assigned
Attorney Docket Number	4123 0190002

[illegible]

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ²
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
	FP7	CN 106920794 A	07-04-2017	YANGTZE MEMORY TECH CO LT		✓
	FP8	CN 107887395 A	04-06-2018	YANGTZE MEMORY TECH CO LT		
	FP9	WO 2019/104896 A1	06-06-2019	YANGTZE MEMORY TECH CO LT		

Examiner
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IPR2024-00911

PTO/SB/08b (07-09)

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Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Complete if Known			
		Application Number	To Be Assigned		
		Filing Date	Herewith		
		First Named Inventor	Qian TAO		
		Art Unit	To Be Assigned		
		Examiner Name	To Be Assigned		
Sheet	1	of	1	Attorney Docket Number	4123.0190002

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	NPL1	International Search Report and Written Opinion of the International Searching Authority directed to related International Patent Application No. PCT/CN2018/085421, mailed January 30, 2019; 9 pages.	

Examiner Signature	/CALVIN Y CHOI/	Date Considered	06/19/2020
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Micron Ex. 1002, p. 126

Micron v. YMTC

IPR2024-00911



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/867,404	05/05/2020	Qian TAO	4123.0190002

CONFIRMATION NO. 7018

26111

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

PUBLICATION NOTICE



OC000000119368432

Title:THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

Publication No.US-2020-0266211-A1

Publication Date:08/20/2020

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: TAO *et al.*

Applicant: Yangtze Memory Technologies
Co., Ltd.

Application No.: 16/867,404

Filing Date: May 5, 2020

Confirmation No.: 7018

Art Unit: 2812

Examiner: CHOI, Calvin Y.

Atty. Docket: 4123.0190002

Title: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY
DEVICES**

Amendment and Reply Under 37 C.F.R. § 1.111

Mail Stop Amendment

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Commissioner:

In reply to the Office Action dated June 23, 2020 (the “Office Action”), Applicant submits the following Amendment and Remarks.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 19-0036.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A three-dimensional (3D) memory device, comprising:
an isolation structure formed in a substrate;
an alternating layer stack on the substrate;
a dielectric structure extending vertically through the alternating layer stack and in contact with a top surface of the isolation structure;
a through array contact (TAC) extending vertically through the dielectric structure, wherein a bottom surface of the TAC is in contact with the isolation structure;
a channel structure extending vertically through the alternating layer stack;
an epitaxial layer under the channel structure;
an etch stop plug on the channel structure;
a staircase structure in the alternating layer stack;
slit structures extending vertically in the alternating layer stack; and
a contact layer on the TAC, the channel structure, and the slit structures.
2. (Original) The 3D memory device of claim 1, wherein the dielectric structure abuts a sidewall surface of the TAC.
3. (Cancelled)
4. (Original) The 3D memory device of claim 1, wherein the alternating layer stack comprises alternating pairs of a dielectric and a conductor layer.
5. (Original) The 3D memory device of claim 1, wherein the dielectric structure comprises silicon oxide.
6. (Original) The 3D memory device of claim 1, wherein the dielectric structure comprises an oxide material.

Atty. Dkt. No. 4123.0190002

7. (Original) The 3D memory device of claim 1, wherein the dielectric structure defines a through array contact region within the 3D memory device.
8. (Currently Amended) The 3D memory device of claim 1, ~~further comprising an isolation region on a semiconductor substrate and~~ wherein a width of the dielectric structure has a footprint is equal to or smaller than a width of the isolation region structure.
9. (Currently Amended) A three-dimensional (3D) memory device, comprising:
an alternating conductor/dielectric layer stack;
a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;
~~channel structures and~~ first and second channel regions comprising first and second pluralities of channel structures, respectively;
slit structures extending vertically through the alternating conductor/dielectric layer stack;
a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;
local contacts disposed on the first and second channel structures and the slit structures;
[[and]]
a through array ~~contacts (TACs)~~ contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and
a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.
10. (Original) The 3D memory device of claim 9, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.
11. (Cancelled)
12. (Currently Amended) The 3D memory device of claim 9, further comprising:
a substrate;

an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and

an epitaxial layer disposed between ~~the channel structure structures~~ and the substrate and the first or second channel structures.

13. (Original) The 3D memory device of claim 9, wherein the dielectric material comprises silicon oxide.

14. (Original) The 3D memory device of claim 9, wherein the TACs comprise a conductive material.

15. (Currently Amended) A method for forming a 3D memory device, the method comprising:
disposing an isolation structure in a substrate;
disposing an alternating dielectric layer stack on ~~[[a]]~~ the substrate;
disposing a staircase structure in the alternating dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;
forming a channel structure extending vertically in the alternating dielectric layer stack;
forming a first opening in the alternating dielectric layer stack, wherein the first opening exposes a top surface of the isolation structure;
filling the first opening with a dielectric layer;
removing portions of the dielectric structure ~~until the substrate is exposed~~ to form a second opening that vertically extends through the dielectric structure, wherein the second opening exposes a portion of the isolation structure;
filling the second opening with a conductor to form a through array contact (TAC) structure in contact with ~~the substrate~~ the portion of the isolation structure; and
disposing a local contact on the channel structure and the TAC structure.

16. (Original) The method of claim 15, further comprising:
forming slit openings extending vertically in the alternating dielectric layer stack, wherein the slit openings expose a doped region of the substrate;

replacing a dielectric layer of the alternating dielectric layer stack through the slit openings with the conductor layer to convert the alternating dielectric layer stack to an alternating dielectric/conductor layer stack; and
filling the slit openings with a conductor.

17. (Cancelled)

18. (Original) The method of claim 15, wherein filling the first opening with the dielectric layer comprises depositing the dielectric layer with a chemical vapor deposition, a plasma-enhanced chemical vapor deposition, or a physical vapor deposition process.

19. (Original) The method of claim 15, wherein filling the first opening with the dielectric layer comprises depositing an oxide material.

20. (Original) The method of claim 15, wherein disposing the alternating dielectric layer stack comprises alternately disposing a first dielectric layer comprising an oxide material and a second dielectric layer comprising a nitride material.

21. (New) The 3D memory device of claim 1, further comprising a non-electrically functional channel structure between the channel structure and the TAC.

22. (New) The 3D memory device of claim 9, further comprising an isolation structure, wherein bottom surfaces of the plurality of TACs are in contact with a top surface of the isolation structure.

23. (New) The method of claim 15, further comprising forming a non-electrically functional channel structure between the channel structure and the TAC structure.

Remarks

Upon entry of the foregoing amendment, claims 1, 2, 4-10, 12-16, and 18-23 are pending in the application, with claims 1, 9, and 15 being the independent claims. Claims 1, 8, 9, and 15 are sought to be amended. Claims 3, 11, and 17 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein. New claims 21-23 are sought to be added. Exemplary support for the amended claims and the new claims can be found, *inter alia*, in ¶¶ [0036]-[0038] and [0055]-[0063], as well as in Figs. 1A, 2, 3, and 13 of the originally filed application. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the following remarks, Applicant respectfully requests that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn. Throughout the arguments, Applicant reminds the Examiner that the claims are given their broadest reasonable meaning in view of the specification, and any paraphrasing of the claim features is not to be interpreted as reading any features into, or characterizing of, the claims.

Claim Objection

Claim 12 objected to for allegedly lacking antecedent basis. Without acquiescing to the propriety of the objection, claim 12 has been amended. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the objection.

Rejections under 35 U.S.C. § 103

Claims 1-16 and 18-20 are rejected under 35 U.S.C. § 103 as allegedly being unpatentable over U.S. Patent No. 9,659,956 to Pachamuthu *et al.* (“Pachamuthu”), in view of U.S. Patent Application Publication No. 2017/0186758 to Lee *et al.* (“Lee”).

Claims 17 is rejected under 35 U.S.C. § 103 as allegedly being unpatentable over the combination of Pachamuthu and Lee and further in view of U.S. Patent Application Publication No. 2017/0365613 to Gunji-Yoneoka *et al.* (“Gunji-Yoneoka”).

Claims 3, 11, and 17 are sought to be cancelled, without prejudice to or disclaimer of the subject matter therein, rendering their rejection moot. Applicant respectfully traverses the rejections directed to the remaining claims and provides the following to support patentability.

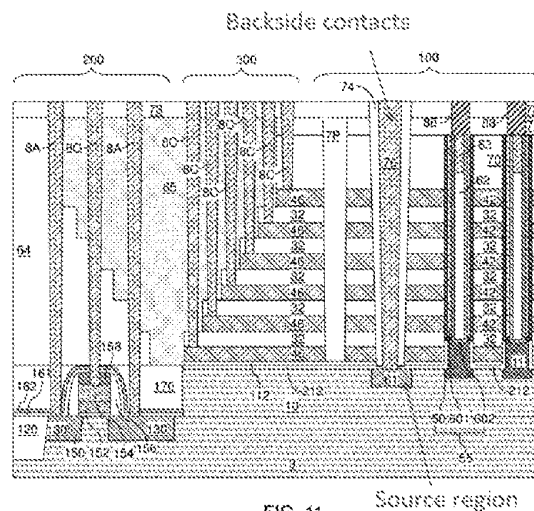
Independent claims 1, 9, and 15

Without acquiescing to the propriety of the rejection, independent claims 1, 9, and 15 have been amended to recite features that further distinguish itself from the applied references. For example, claim 1 recites, *inter alia*,

an isolation structure formed in a substrate;
an alternating layer stack on the substrate;
a dielectric structure extending vertically through the alternating layer stack and ***in contact with a top surface of the isolation structure;***
a through array contact (TAC) extending vertically through the dielectric structure, wherein ***a bottom surface of the TAC is in contact with the isolation structure.***

Pachamuthu does not disclose or suggest at least the above-noted distinguishing features. For example, the bottom surface of Pachamuthu's backside contact structures 76 (the alleged "through array contact") are in contact with a conductive structure rather than an isolation structure. As shown in annotated Fig. 11 of Pachamuthu, the bottom surface of backside contact structures 76 is in contact with the top surface of source region 61. Pachamuthu discloses that source region 61 is a conductive structure.

Specifically, Pachamuthu states "[e]ach source region 61 can be formed by implanting electrical dopants of the same conductivity type as the doping type of the drain regions 63." (Pachamuthu, 16:10-12, emphasis added.)



Claim 9 has been amended to recite features that further distinguishes itself from the applied references. For example, claim 9 recites, *inter alia*, "a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions." Pachmuthu is completely silent regarding a non-electrically functional channel structure,

let alone disclosing a plurality of non-electrically functional channel structures that surrounds the TAC region.

Claim 15 has also been amended to recite features that further distinguishes itself from the applied references. For example, claim 15 recites, *inter alia*,

disposing an isolation structure in a substrate...

forming a first opening in the alternating dielectric layer stack, wherein ***the first opening exposes a top surface of the isolation structure***;

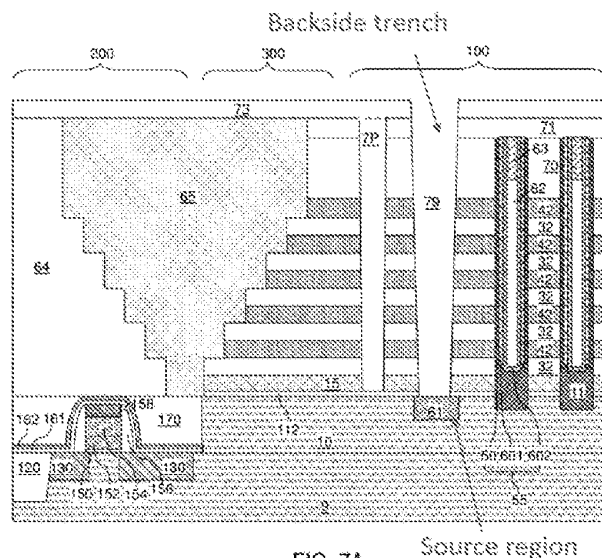
filling the first opening with a dielectric layer;

removing portions of the dielectric structure to form a second opening that vertically extends through the dielectric structure, wherein ***the second opening exposes a portion of the isolation structure***;

filling the second opening with a conductor to ***form a through array contact (TAC) structure in contact with the portion of the isolation structure***; and

disposing a local contact on the channel structure and the TAC structure.

As discussed above with reference to claim 1, Pachamuthu does not disclose or suggest at least “a through array contact (TAC) structure in contact with the portion of the isolation structure.” In addition, Pachamuthu does not disclose at least “the second opening exposes a portion of the isolation structure.” For example, Pachamuthu’s backside contact trench 79 (the alleged “second opening”) exposes a conductive structure (i.e., source region 61) rather than an isolation structure. Specifically, Pachamuthu discloses that its backside contact structure 76 is formed by first forming a backside contact trench 79 that



Annotated Fig. 7A of Pachamuthu

“can include a source contact opening in which a source contact via structure can be subsequently formed.” (Pachamuthu, 14:51-53.) Fig. 7A of Pachamuthu (annotated and reproduced) illustrates that backside contact trench 79 exposes source region 61.

Therefore, Pachamuthu does not disclose at least the above-noted distinguishing features of claims 1, 9, and 15. Further, Lee does not cure the deficiencies of Pachamuthu nor does it disclose or suggest these distinguishing features of claims 1, 9, and 15. Therefore, the Pachamuthu-Lee combination cannot establish a *prima facie* case of obviousness for at least claims 1, 9, and 15. Applicant respectfully requests that the Office reconsider and withdraw the rejection of claims 1, 9, and 15, and pass them to allowance.

Dependent claims 2-8, 10-14, and 16-20

Claims 3, 11, and 17 are sought to be cancelled without prejudice to or disclaimer of the subject matter therein, rendering their rejection moot.

As discussed above with respect to claims 1, 9, and 15, the combination of Pachamuthu and Lee does not establish a *prima facie* case for obviousness. Further, Gunji-Yoneoka does not cure the deficiencies of Pachamuthu or Lee, nor does Gunji-Yoneoka disclose these distinguishing features. Dependent claims 2, 4-8, 10, 12-14, 16, and 18-20 are patentable at least because they recite all of the features of independent claims 1, 9, and 15 from which they depend, as well as for their additional distinguishing features.

Accordingly, Applicant respectfully requests the Examiner to reconsider and withdraw the rejections under 35 U.S.C. §103 and to pass claims 1, 2, 4-10, 12-16, and 18-20 to allowance.

New Claims 21-23

New claims 21-23 have been added. At least based on their dependency from claims 1, 9, and 15, claims 21-23 are distinguishable over the applied references for the reasons above, as well as for their own distinguishing features. Accordingly, Applicant respectfully requests that claims 21-23 be passed to allowance.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicant believes that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 10/21/2020

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600

15220342_1.docx

Electronic Patent Application Fee Transmittal				
Application Number:		16867404		
Filing Date:		05-May-2020		
Title of Invention:		THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		
First Named Inventor/Applicant Name:		Qian TAO		
Filer:		Donald J. Featherstone/Catherine Saunders		
Attorney Docket Number:		4123.0190002		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 1 month with \$0 paid	1251	1	220	220
Miscellaneous:				
Total in USD (\$)				220

Electronic Acknowledgement Receipt	
EFS ID:	40905433
Application Number:	16867404
International Application Number:	
Confirmation Number:	7018
Title of Invention:	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
First Named Inventor/Applicant Name:	Qian TAO
Customer Number:	26111
Filer:	Donald J. Featherstone/Catherine Saunders
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0190002
Receipt Date:	21-OCT-2020
Filing Date:	05-MAY-2020
Time Stamp:	15:01:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 220
RAM confirmation Number	E20200KF04173867
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2020-10-21-Filing-Bundle-4123-0190002.PDF	1399536	yes	13
			a092ddc196bb66fabd22f25d6c8ee0418ae9f06c		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Miscellaneous Incoming Letter		1	2	
	Extension of Time		3	3	
	Amendment/Req. Reconsideration-After Non-Final Reject		4	4	
	Claims		5	8	
	Applicant Arguments/Remarks Made in an Amendment		9	13	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30988	no	2
			117ab5615fb2f9710d6764a08f50e0847f8f9dbc		
Warnings:					
Information:					
Total Files Size (in bytes):			1430524		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

October 21, 2020

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 7018
Art Unit 2812
Mail Stop Amendment

Re: U.S. Utility Patent Application
Appl. No. 16/867,404; Filing Date: May 5, 2020
For: **THROUGH ARRAY CONTACT (TAC) FOR THREE-
DIMENSIONAL MEMORY DEVICES**
Inventors: TAO *et al.*
Our Ref.: 4123.0190002

Commissioner:

Transmitted herewith for appropriate action are the following documents:

1. Online Credit Card Payment Authorization in the amount of **\$220.00** to cover extension of time fee;
2. Petition for Extension of Time Under 37 C.F.R. § 1.136(a)(3); and
3. Amendment and Reply Under 37 C.F.R. § 1.111.

The above-listed documents are filed electronically.

In the event that extensions of time are necessary to prevent abandonment of this patent application, then such extensions of time are hereby petitioned.

Commissioner for Patents
October 21, 2020
Page 2

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) or credit any overpayment to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/Y-G/cms
Enclosures
15220440_1.docx

PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)		Docket Number (Optional) 4123.0190002																														
Application Number 16/867,404	Filed May 5, 2020																															
For THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES																																
Art Unit 2812	Examiner CHOI, Calvin Y.																															
This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application. The requested extension and fee are as follows (check time period desired and enter the appropriate fee below): <table style="width: 100%; border-collapse: collapse;"><thead><tr><th></th><th style="text-align: center;"><u>Fee</u></th><th style="text-align: center;"><u>Small Entity Fee</u></th><th style="text-align: center;"><u>Micro Entity Fee</u></th><th></th></tr></thead><tbody><tr><td>☒ One month (37 CFR 1.17(a)(1))</td><td style="text-align: right;">\$220</td><td style="text-align: right;">\$110</td><td style="text-align: right;">\$55</td><td style="text-align: right;">\$ <u>220.00</u></td></tr><tr><td>☐ Two months (37 CFR 1.17(a)(2))</td><td style="text-align: right;">\$640</td><td style="text-align: right;">\$320</td><td style="text-align: right;">\$160</td><td style="text-align: right;">\$ _____</td></tr><tr><td>☐ Three months (37 CFR 1.17(a)(3))</td><td style="text-align: right;">\$1,480</td><td style="text-align: right;">\$740</td><td style="text-align: right;">\$370</td><td style="text-align: right;">\$ _____</td></tr><tr><td>☐ Four months (37 CFR 1.17(a)(4))</td><td style="text-align: right;">\$2,320</td><td style="text-align: right;">\$1,160</td><td style="text-align: right;">\$580</td><td style="text-align: right;">\$ _____</td></tr><tr><td>☐ Five months (37 CFR 1.17(a)(5))</td><td style="text-align: right;">\$3,160</td><td style="text-align: right;">\$1,580</td><td style="text-align: right;">\$790</td><td style="text-align: right;">\$ _____</td></tr></tbody></table> ☐ Applicant asserts small entity status. See 37 CFR 1.27. ☐ Applicant certifies micro entity status. See 37 CFR 1.29. Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously. ☐ A check in the amount of the fee is enclosed. ☐ Payment by credit card. Form PTO-2038 is attached. ☐ The Director has already been authorized to charge fees in this application to a Deposit Account. ☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number <u>19-0036</u>. ☒ Payment made via EFS-Web. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. I am the ☐ applicant. ☒ attorney or agent of record. Registration number <u>33,876</u>. ☐ attorney or agent acting under 37 CFR 1.34. Registration number _____. <u>/Donald J. Featherstone/</u> <u>10/21/2020</u> Signature Date <u>Donald J. Featherstone</u> <u>(202) 371-2600</u> Typed or printed name Telephone Number NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.				<u>Fee</u>	<u>Small Entity Fee</u>	<u>Micro Entity Fee</u>		☒ One month (37 CFR 1.17(a)(1))	\$220	\$110	\$55	\$ <u>220.00</u>	☐ Two months (37 CFR 1.17(a)(2))	\$640	\$320	\$160	\$ _____	☐ Three months (37 CFR 1.17(a)(3))	\$1,480	\$740	\$370	\$ _____	☐ Four months (37 CFR 1.17(a)(4))	\$2,320	\$1,160	\$580	\$ _____	☐ Five months (37 CFR 1.17(a)(5))	\$3,160	\$1,580	\$790	\$ _____
	<u>Fee</u>	<u>Small Entity Fee</u>	<u>Micro Entity Fee</u>																													
☒ One month (37 CFR 1.17(a)(1))	\$220	\$110	\$55	\$ <u>220.00</u>																												
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☐ Three months (37 CFR 1.17(a)(3))	\$1,480	\$740	\$370	\$ _____																												
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☐ Five months (37 CFR 1.17(a)(5))	\$3,160	\$1,580	\$790	\$ _____																												
☒ * Total of <u>1 (one)</u> forms are submitted.																																

This collection of information is required by 37 CFR 1.136(a). The information is required to obtain or retain a benefit by the public, which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 6 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop PCT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 16/867,404		Filing Date 05/05/2020		☐ To be Mailed					
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO													
APPLICATION AS FILED - PART I													
		(Column 1)		(Column 2)									
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)					
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A							
☐ SEARCH FEE (37 CFR 1.16(k), (l), or (m))		N/A		N/A		N/A							
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A							
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 = *				x \$100 =							
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 = *				x \$460 =							
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).											
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))													
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL							
APPLICATION AS AMENDED - PART II													
		(Column 1)		(Column 2)		(Column 3)							
AMENDMENT	10/21/2020	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)			
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0			x \$100 =		0			
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0			x \$480 =		0			
	☐ Application Size Fee (37 CFR 1.16(s))												
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))												
										TOTAL ADD'L FEE		0	
AMENDMENT			(Column 1)		(Column 2)		(Column 3)						
			CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)		
	Total (37 CFR 1.16(i))		*		Minus		**		=		x \$0 =		
	Independent (37 CFR 1.16(h))		*		Minus		***		=		x \$0 =		
	☐ Application Size Fee (37 CFR 1.16(s))												
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))													
										TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.										LIE			
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".										/JASON B EADDY/			
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".													
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.													

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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NOTICE OF ALLOWANCE AND FEE(S) DUE

26111 7590 12/16/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
CHOI, CALVIN Y	
ART UNIT	PAPER NUMBER

2812

DATE MAILED: 12/16/2020

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/867,404	05/05/2020	Qian TAO	4123.0190002	7018

TITLE OF INVENTION: THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	03/16/2021

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 12/16/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/867,404	05/05/2020	Qian TAO	4123.0190002	7018

TITLE OF INVENTION: THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	03/16/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOI, CALVIN Y	2812	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



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Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/867,404	05/05/2020	Qian TAO	4123.0190002	7018
26111 7590 12/16/2020 STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C. 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			EXAMINER CHOI, CALVIN Y	
			ART UNIT 2812	PAPER NUMBER
DATE MAILED: 12/16/2020				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b) (2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 16/867,404	Applicant(s) TAO et al.	
	Examiner CALVIN Y CHOI	Art Unit 2812	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the Remarks and Amendments filed on 21 October 2020.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are See Continuation Sheet. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/CALVIN Y CHOI/ Primary Examiner, Art Unit 2812	
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Continuation of 3. The allowed claim(s) is/are: 1-2,4-10,12-16 and 18-23

DETAILED ACTION

1. This Office Action is in response to the Remarks and Amendments filed on 21 October 2020.

Notice of Pre-AIA or AIA Status

2. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Allowable Subject Matter

3. **Claims 1, 2, 4-10, 12-16, and 18-23 are allowed.**

4. The following is an examiner's statement of reasons for allowance: independent claim(s) 1, 9, and 15 is/are allowable because the closest prior art does not appear to disclose, alone or in combination, the limitations of the sequential steps of: forming an isolation structure in a substrate; forming a staircase structure from an alternating dielectric/conductor layer stack on the substrate over the isolation structure; forming a channel structure through the staircase structure; forming an opening in the staircase structure to expose the isolation structure; filling the first opening with a dielectric layer; removing portions of the dielectric structure; to form a second opening that vertically extends through the dielectric structure, wherein the second opening exposes a portion of the isolation structure; filling the second opening with a conductor to form a through array contact (TAC) structure in contact with the portion of the isolation structure. Specifically, the aforementioned limitations appear to be material to the inventive concept of the application at hand to have a higher density 3D memory device.

5. The dependent claims of the application at hand are allowable because they respectively depend, directly or indirectly, from the allowable independent claims of the application at hand. Therefore, the dependent claims incorporate the allowable limitations of the independent claims.

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to CALVIN Y CHOI whose telephone number is (571)270-7882. The examiner can normally be reached on M-F 9-5 (Pacific Time).
8. Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.
9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Garber can be reached on (571) 272-2194. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

CALVIN Y. CHOI
Primary Examiner
Art Unit 2812

/CALVIN Y CHOI/
Primary Examiner, Art Unit 2812

Issue Classification 	Application/Control No. 16/867,404	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

CPC						
Symbol					Type	Version
H01L	/	27	/	11582	F	2013-01-01
H01L	/	21	/	76802	I	2013-01-01
H01L	/	21	/	76831	I	2013-01-01
H01L	/	21	/	76877	I	2013-01-01
H01L	/	23	/	5226	I	2013-01-01
H01L	/	27	/	11565	I	2013-01-01
H01L	/	27	/	1157	I	2013-01-01

CPC Combination Sets						
Symbol				Type	Set	Ranking
	/		/			

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/CALVIN Y CHOI/	05 December 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	13	13

U.S. Patent and Trademark Office

Part of Paper No.: 20201205

Issue Classification 	Application/Control No. 16/867,404	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

INTERNATIONAL CLASSIFICATION			
CLAIMED			
H01L		29	792
NON-CLAIMED			

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/CALVIN Y CHOI/ Primary Examiner, Art Unit 2812	05 December 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	13	13

U.S. Patent and Trademark Office

Part of Paper No.: 20201205

Issue Classification 	Application/Control No. 16/867,404	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	9	10	16	19										
2	2		11	17	20										
	3	10	12	18	21										
3	4	11	13	19	22										
4	5	12	14	20	23										
5	6	13	15												
6	7	14	16												
7	8		17												
8	9	15	18												

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/CALVIN Y CHOI/	05 December 2020	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	13	13

U.S. Patent and Trademark Office

Part of Paper No.: 20201205

Search Notes 	Application/Control No. 16/867,404	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

CPC - Searched*		
Symbol	Date	Examiner
H01L27/11524,11529,11578-11582,1157,11551-11556.cpc. or H01L29/40114,40117.cpc. or H01L21/0223.cpc.	06/06/2020	CYC
H01L27/11582,1157,11573.cpc. or H01L29/40117.cpc. or H01L21/76802,76877.cpc. or H01L23/5226.cpc.	06/06/2020	CYC

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
257	324.ccls.	06/06/2020	CYC

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
H01L27/11524,11529,11578-11582,1157,11551-11556.cpc. or H01L29/40114,40117.cpc. or H01L21/0223.cpc.	06/06/2020	CYC
H01L27/11582,1157,11573.cpc. or H01L29/40117.cpc. or H01L21/76802,76877.cpc. or H01L23/5226.cpc.	06/06/2020	CYC
257/324.ccls.	06/06/2020	CYC
Inventor, assignee, and text search using EAST - please refer to search history.	06/06/2020	CYC
Updated text search using EAST - please refer to updated search history.	12/05/2020	CYC

/CALVIN Y CHOI/ Primary Examiner, Art Unit 2812	
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<i>Search Notes</i> 	Application/Control No. 16/867,404	Applicant(s)/Patent Under Reexamination TAO et al.
	Examiner CALVIN Y CHOI	Art Unit 2812

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
	H01L27/11524,11529,11578-11582,1157,11551-11556.cpc. or H01L29/40114,40117.cpc. or H01L21/0223.cpc.	12/05/2020	CYC
	H01L27/11582,1157,11573.cpc. or H01L29/40117.cpc. or H01L21/76802,76877.cpc. or H01L23/5226.cpc.	12/05/2020	CYC
257	324.ccls.	12/05/2020	CYC

/CALVIN Y CHOI/ Primary Examiner, Art Unit 2812	
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EAST Search History

EAST Search History (Prior Art)

<This search history is empty>

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	41,597	257/324.ccls. or H01L27/11582,1157,11573.cpc. or H01L29/40117.cpc. or H01L21/76802,76877.cpc. or H01L23/5226.cpc.	US- PGPUB; USPAT	ADJ	ON	2020/12/05 23:41
L2	28,175	257/324.ccls. or H01L27/11524,11529,11578- 11582,1157,11551-11556.cpc. or H01L29/40114,40117.cpc. or H01L21/0223.cpc.	US- PGPUB; USPAT	ADJ	ON	2020/12/05 23:41
L3	171	(TAC or through\$1array\$1contact or TSC or through\$1stair\$1contact) same (channel or memory) same ((local near2 contact) or interconnect\$4 or inter\$1connect\$4 or trace)	US- PGPUB; USPAT	ADJ	ON	2020/12/05 23:42
L4	17	(TAC or through\$1array\$1contact or TSC or through\$1stair\$1contact) same (channel or memory) same local near2 contact	US- PGPUB; USPAT	ADJ	ON	2020/12/05 23:42
L5	52,920	(L1 or L2)	US- PGPUB; USPAT	ADJ	ON	2020/12/05 23:43
L6	171	(L3 or L4)	US- PGPUB; USPAT	ADJ	ON	2020/12/05 23:44
L7	61	L5 and L6	US- PGPUB; USPAT	ADJ	ON	2020/12/05 23:44

12/5/2020 11:44:18 PM

C:\Users\cchoi2\Documents\EAST\Workspaces\16867404 - Tao et al.wsp

DONALD J. FEATHERSTONE
DIRECTOR
(202) 772-8629
DONF@STERNEKESSLER.COM

January 22, 2021

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Confirmation No. 7018
Mail Stop Issue Fee

Re: Allowed U.S. Utility Patent Application
Appl. No. 16/867,404; Filed: May 5, 2020
For: **THROUGH ARRAY CONTACT (TAC) FOR THREE-
DIMENSIONAL MEMORY DEVICES**
Inventors: TAO *et al.*
Our Ref: 4123.0190002

Commissioner:

In response to the **Notice of Allowance and Fee(s) Due** dated December 16, 2020, the following documents are transmitted for appropriate action by the U.S. Patent and Trademark Office:

1. Online Credit Card Payment Authorization for **\$1,200.00** to cover the Issue Fee;
2. Issue Fee Transmittal (Form PTOL-85); and
3. Comments on Statement of Reasons for Allowance.

The above-listed documents are filed electronically.

Fee payment is provided through online credit card payment. The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 19-0036.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

DJF/Y-G/rtl
Enclosures

16073786_1.docx

Sterne, Kessler, Goldstein & Fox P.L.L.C. | 1100 New York Avenue, NW | Washington, D.C. 20005

P 202.371.2500 | F 202.371.2540 | sternekessler.com

Electronic Patent Application Fee Transmittal				
Application Number:		16867404		
Filing Date:		05-May-2020		
Title of Invention:		THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES		
First Named Inventor/Applicant Name:		Qian TAO		
Filer:		Donald J. Featherstone/Tonyia Skinner		
Attorney Docket Number:		4123.0190002		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1200

Electronic Acknowledgement Receipt

EFS ID:	41714338
Application Number:	16867404
International Application Number:	
Confirmation Number:	7018
Title of Invention:	THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES
First Named Inventor/Applicant Name:	Qian TAO
Customer Number:	26111
Filer:	Donald J. Featherstone/Tonyia Skinner
Filer Authorized By:	Donald J. Featherstone
Attorney Docket Number:	4123.0190002
Receipt Date:	22-JAN-2021
Filing Date:	05-MAY-2020
Time Stamp:	10:29:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	E20211LA29397533
Deposit Account	
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		2021-01-22-Filing-Bundle-4123-0190002.PDF	661983	yes	3
			04b8228d852b47c94d31964d4e44d3f9f5abfec		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Post Allowance Communication - Incoming		3	3	
	Issue Fee Payment (PTO-85B)		2	2	
	Transmittal Letter		1	1	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30464	no	2
			6ebad23b7967d43150817c9f8f4eca11236c2b5e		
Warnings:					
Information:					
Total Files Size (in bytes):			692447		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventors: TAO *et al.*

Applicant: Yangtze Memory Technologies
Co., Ltd.

Application No.: 16/867,404

Filing Date: May 5, 2020

Confirmation No.: 7018

Art Unit: 2812

Examiner: CHOI, Calvin Y.

Atty. Docket: 4123.0190002

Title: **THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY
DEVICES**

Comments on Statement of Reasons for Allowance

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Mail Stop: Issue Fee

Commissioner:

Applicant thanks the Examiner for indicating the allowability of claims 1, 2, 4–10, 12–16 and 18–23 in the Notice of Allowance dated December 16, 2020.

Comments on Statement of Reasons for Allowance

Applicant notes the Examiner's Statement of Reasons for Allowance presented on page 2 of the Notice of Allowance. Applicant reserves the right to demonstrate claims 1, 2, 4–10, 12–16 and 18–23 are allowable over the art made of record for further reasons related to any of their recited features. Applicant further contends that reservation of this right does not give rise to any implication regarding whether the Applicant agrees with or acquiesces in the reasoning provided by the Examiner.

Respectfully submitted,

STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.

/Donald J. Featherstone/

Donald J. Featherstone
Attorney for Applicant
Registration No. 33,876

Date: 1/22/21

1100 New York Avenue, N.W.
Washington, D.C. 20005-3934
(202) 371-2600
16168975.1

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

26111 7590 12/16/2020
STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/867,404	05/05/2020	Qian TAO	4123.0190002	7018

TITLE OF INVENTION: THROUGH ARRAY CONTACT (TAC) FOR THREE-DIMENSIONAL MEMORY DEVICES

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	03/16/2021

EXAMINER	ART UNIT	CLASS-SUBCLASS
CHOI, CALVIN Y	2812	257-314000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Sterne, Kessler, Goldstein & Fox
P.L.L.C.
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

Yangtze Memory Technologies Co., Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Wuhan, China

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☒ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 19-0036

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29☐ Applicant asserting small entity status. See 37 CFR 1.27☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Donald J. Featherstone/Date 1/22/21Typed or printed name Donald J. FeatherstoneRegistration No. 33,876



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/867,404	03/02/2021	10937806	4123.0190002	7018

26111 7590 02/10/2021
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WASHINGTON, DC 20005

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

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IR103 (Rev. 10/09)