

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00911
U.S. Patent No. 10,937,806
Issue Date: March 2, 2021

Title: THROUGH ARRAY CONTACT (TAC) FOR
THREE-DIMENSIONAL MEMORY DEVICES

DECLARATION OF DR. JACK C. LEE

TABLE OF CONTENTS

I. INTRODUCTION	4
II. BACKGROUND AND EXPERT QUALIFICATIONS	5
III. ASSIGNMENT AND MATERIALS CONSIDERED	7
IV. UNDERSTANDING OF THE LAW	10
V. LEVEL OF SKILL IN THE ART	14
VI. TECHNOLOGY BACKGROUND AND STATE OF THE ART	16
A. 3D NAND Flash Memories.....	16
B. Epitaxy.....	30
C. Etching.....	32
VII. THE '806 PATENT	37
A. Effective Filing Date	37
B. Overview	37
C. Prosecution History	42
D. Claims.....	44
VIII. CLAIM CONSTRUCTION.....	45
IX. UNPATENTABILITY ANALYSIS.....	46
A. Overview of the Prior Art - Toyama	46
B. <i>Ground 1</i> : Toyama's Second Modification in View of the Knowledge of a POSITA.....	53
1. Claim 8.....	53
2. Claim 10.....	83

Petition for *Inter Partes* Review of U.S. Patent No. 10,937,806
Declaration of Dr. Jack C. Lee

C.	<i>Ground 2: Toyama’s First Exemplary Structure in View of the Knowledge of a POSITA</i>	92
1.	Claim 8.....	93
2.	Claim 10.....	134
D.	<i>Ground 3: Toyama’s First Exemplary Structure and Second Modification to Its Fourth Exemplary Structure in View of the Knowledge of a POSITA</i>	143
1.	It would have been obvious to a POSITA to form the Second Modification’s “through-memory-level via structures” in a unitary dielectric fill material.....	144
2.	Claim 8.....	157
3.	Claim 10.....	168
E.	Secondary Considerations of Non-Obviousness.....	169

I, Dr. Jack C. Lee, declare as follows:

I. INTRODUCTION

1. I have been retained by Micron Technology, Inc. (“Micron”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”). I am not an employee of Micron or any affiliate or subsidiary of Micron.

2. I have been asked to consider whether certain references disclose or teach the features recited in claim 10 of U.S. Patent No. 10,937,806, which I refer to herein as the ’806 patent.

3. My opinions and the bases for my opinions are set forth below.

4. On May 2, 2024, I signed a declaration relating to the ’806 patent in connection with IPR2024-00791. That declaration addressed claims 8-9 and 11-12, while this declaration addresses claim 10. Claim 10 depends from claim 8, so my discussion of claim 8 here parallels my discussion of claim 8 in my prior declaration.

5. I am being compensated at my standard consulting rate of \$680 per hour for my time. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding.

II. BACKGROUND AND EXPERT QUALIFICATIONS

6. My curriculum vitae (“CV”) is attached hereto as Ex. 1004 and provides an accurate identification of my background, experience, and qualifications as an expert in electronics and NAND memory technology.

7. I received a B.S. degree in Electrical Engineering, with highest honors, in 1980, and an M.S. degree in Electrical Engineering in 1981, both from University of California, Los Angeles. I received a Ph.D. degree in Electrical Engineering in 1988 from University of California, Berkeley (“UC Berkeley”).

8. From 1979 to 1984, I was a Member of Technical Staff at the TRW Microelectronics Center, in the High-Speed Bipolar Device Program. I worked on bipolar device/circuit design, fabrication, and testing. I was promoted to Engineering Group Leader level in 1983.

9. I received several academic honors while at UC Berkeley. For example, I won the Best Paper Award from the Institute of Electrical and Electronics Engineers (“IEEE”) International Reliability Physics Symposium in 1988. I was also awarded a Lectureship with my own teaching assistant from UC Berkeley.

10. After receiving my Ph.D. in August 1988, I joined the faculty at The University of Texas at Austin (“UT Austin”). As a faculty member, I have taught numerous courses in semiconductor device fabrication and design, at both the undergraduate and graduate levels. This includes classes relating to, among other

things, 3D NAND technology. I have supervised over 40 students who received their doctoral degrees under my guidance. Since September 2000, I have held the Cullen Trust for Higher Education Endowed Professorship in Engineering in the Department of Electrical and Computer Engineering at UT Austin. In September 2023, I was promoted to the Professor Emeritus level.

11. My current research and teaching interests include semiconductor devices, semiconductor memory applications (including non-volatile memory), fabrication processes, silicon-on-insulator technologies, electrical and material characterization, reliability and modeling, packaging technologies, dielectric and passivation processes, display technologies, photovoltaic and solar cell technologies, high-K gate dielectrics and electrode, and alternative channel materials. I routinely encounter and address topics relating to NAND flash memory, and more specifically 3D NAND flash memory, in my research. My research has been partially supported by grants from the National Science Foundation, the Texas Advanced Research Program, the Semiconductor Research Corporation (SRC), SEMATECH, Texas Emerging Technology Funds, and others.

12. I have authored over 600 journal publications and conference proceeding papers and have coauthored 8 books and book chapters on semiconductor technologies. Many of these relate to the structure and operation of memory devices, including non-volatile memory such as NAND flash memory and

3D NAND flash memory. I am a named inventor of 9 U.S. patents. I have also received numerous teaching and research awards, e.g., inventor recognition and best paper awards.

13. In 2002, I became an IEEE fellow for my “contributions to the understanding and development of ultra-thin dielectrics and their application to silicon devices.” I was also an IEEE Electron Devices Society Distinguished Lecturer from 2004 to 2016.

14. I have served in various technology consulting and business advisor roles. For example, I have taught short courses on semiconductor device physics and technologies at various semiconductor companies and consortiums (e.g., SEMATECH). I have also organized several international conferences and have given lectures at numerous conferences and symposia, including the International Symposium on VLSI Technologies, the IEEE Symposia on VLSI Technology, and the IEEE International Electron Devices Meeting. These conferences are some of the most prestigious in the field.

III. ASSIGNMENT AND MATERIALS CONSIDERED

15. I have been asked to provide analysis and explain the subject matter of the '806 patent, including the state of the art when the application underlying the '806 patent was filed. I have also been asked to consider, analyze, and explain certain prior art to the '806 patent including how that art relates to claim 10 (which

I refer to as the “Challenged Claim”) of the ’806 patent and to provide my opinions regarding whether that art invalidates the Challenged Claim.

16. The opinions expressed in this declaration are not exhaustive of opinions I may offer in the future regarding the unpatentability of the Challenged Claim of the ’806 patent. Therefore, the fact that I do not address a particular point should not be understood to indicate an agreement on my part that any claim complies with the requirements of any other applicable rule.

17. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during this IPR or related proceedings on the ’806 patent.

18. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the ’806 patent (Ex. 1001), its prosecution history (Ex. 1002), and the following additional materials:

Exhibit	Description
1005	U.S. Patent Publ. No. 2017/0179026 A1 (“Toyama”)
1009	CN109075169A Office Action, dated November 14, 2019
1010	Certified Translation of CN109075169A Office Action, dated November 14, 2019

Petition for *Inter Partes* Review of U.S. Patent No. 10,937,806
Declaration of Dr. Jack C. Lee

Exhibit	Description
1011	CN109075169A Reexamination Decision, dated November 25, 2021
1012	Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021
1013	Micheloni, “3D Flash Memories” (2016)
1014	Aritome, “NAND Flash Memory Technologies” (2016)
1015	U.S. Patent Publ. No. 2018/0108671 A1 to Yu et al.
1016	U.S. Patent Publ. No. 2019/0229125 A1 to Zhou et al.
1017	U.S. Patent No. 10,354,980 B1 to Mushiga et al.
1018	U.S. Patent No. 9,293,348 B2 to Lai et al.
1019	U.S. Patent No. 8,598,643 B2 to Kawasaki et al.
1020	U.S. Patent No. 8,697,519 B2 to Jee et al.
1021	Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
1022	Print out of https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides
1023	Micheloni et al., “Inside Solid State Drives (SSDs)” (1 st Ed. 2013)
1024	U.S. Patent No. 10,043,558 to Shah et al.
1025	Micheloni et al., “Inside NAND Flash Memories” (2010)
1026	Lau, “Ball Grid Array Technology” (1995)
1027	U.S. Patent No. 10,103,169 to Ge et al.
1028	U.S. Patent No. 9,935,050 to Dunga et al.
1029	Chang, “ULSI Technology” (1996)

Exhibit	Description
1030	Chen, “CMS Devices & Technology for VLSI” (1988)
1031	Jaeger, “Volume V: Introduction to Microelectronic Fabrication” (1988)
1032	U.S. Patent No. 5,776,808 to Muller et al.
1033	U.S. Patent No. 9,236,393 to Cernea
1034	Capogreco et al., “Integration and electrical evaluation of epitaxially grown Si and SiGe channels for vertical NAND Memory applications,” 2015 IEEE International Memory Workshop, 2015
1035	Kim et al., “Three-Dimensional NAND Flash Architecture Design Based on Single-Crystalline Stacked Array,” IEEE Transactions on Electron Devices, Vol. 59, No. 1, Jan. 2012, pp. 35-45
1036	Wagner, “The Use of HBr in Polysilicon Etching,” Gases & Instrumentation International, Vol. 7, Issue 4, July/August (2013) printed from https://www.pall.com/content/dam/pall/microelectronics/literature-library/non-gated/HBr_Polysilicon.pdf
1037	Baker, “CMOS Circuit Design, Layout, and Simulation,” Third Ed. (2010)

IV. UNDERSTANDING OF THE LAW

19. I am not an attorney, but have been instructed in and applied the law as described in this section.

20. I understand that the first step in comparing a Challenged Claim to the prior art is for the claim to be properly construed. I address how a person of ordinary

skill in the art (POSITA) would have understood the Challenged Claim of the alleged invention in Section VIII below.

21. I have been further instructed and understand that a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a POSITA of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of ordinary skill in the art at the time the patent was filed.

22. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for a POSITA to combine the prior art references to arrive at the claimed subject matter.

23. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a POSITA at the time of the invention, one must consider the references in their entirety to

ascertain whether the disclosures in those references render the combination obvious to such a person.

24. I have been informed and understand that, while not required, the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine. The motivation linking two or more prior art references can also come from other sources, including, for instance, economic or market demand or the common sense of a POSITA at the time of the invention.

25. I understand that a particular combination may be proven obvious by showing that it was obvious to try the combination. I have been informed that, if a technique has been used to improve one device, and a POSITA would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

26. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a POSITA has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

27. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

28. Additionally, I understand that a patent is likely to be invalid for obviousness if a POSITA can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

29. I further understand that combining embodiments related to each other in a single prior art reference would not ordinarily require a leap of inventiveness.

30. I also understand that a POSITA must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

31. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but

unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

32. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a “nexus,” between any such secondary indicia and the claimed invention.

33. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

34. I provide my opinions in this declaration based on the guidelines set forth above.

V. LEVEL OF SKILL IN THE ART

35. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons a POSITA may have for combining references.

36. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of

the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art (POSITA) is also a person of ordinary creativity.

37. In my opinion, a POSITA in the field of the '806 patent would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

38. In my opinion, this POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND's structure, its component parts, how it operates, and how it is controlled.

39. In view of my educational background and decades of experience working with semiconductor memory—including non-volatile 3D NAND flash memory—I was a person of more than the ordinary level of skill in the art as of May 2018. In forming my opinion, I have drawn on my academic background and professional experiences. My opinions herein, however, were formed taking into account the perspective of an ordinarily skilled artisan.

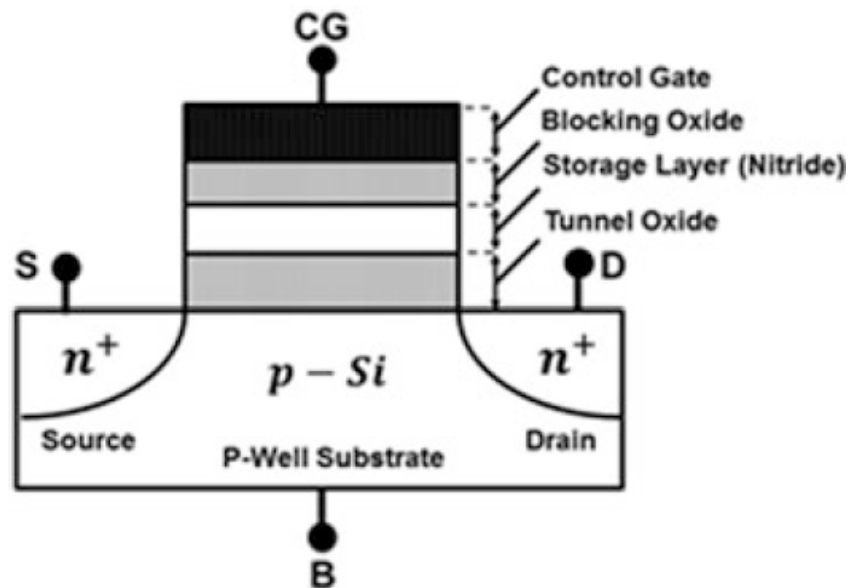
VI. TECHNOLOGY BACKGROUND AND STATE OF THE ART

A. 3D NAND Flash Memories

40. I have been asked to provide a brief overview of the technology relevant to the '806 patent and the state of the art when the '806 priority application was filed.

41. The '806 patent (and the prior art I discuss herein) relate to three-dimensional (3D) NAND flash memory. “Flash memory” has been known for many decades and is a type of memory that stores information even when power is removed (*viz.*, when the device is turned off).

42. At the heart of flash memory is the “memory cell,” which stores information as electrical charge. An example memory cell is below:



Ex. 1013 (3D Flash Memories Textbook), 41. In a memory cell, current flows from the “drain” of the device to the “source” of the device, which is typically connected

to a low voltage, such as ground. *Id.*, 150 (“[T]he Source Line ... plays the role of the ‘local ground’ for each memory cell.”).

43. The acronym “NAND” refers to a “not-AND” logic gate, and NAND flash memory is a particular type of flash memory where the memory cells form a structure similar to that of a NAND gate. Ex. 1013 (3D Flash Memories Textbook), at 14. The other most common type of flash memory is NOR flash, but NAND offers a higher integration density and occupies a larger market than NOR flash.

44. A NAND flash memory device, like most flash memory devices, has an associated memory controller that controls the read, write, and erase operations on a memory cell by applying a voltage to that cell’s “control gate,” labeled as “CG” in the above figures. *Id.*

45. For many years, a NAND flash memory was “planar,” that is, two-dimensional (2D). In 2D NAND flash memory, all memory cells lie on a 2D plane (*i.e.*, the x-y plane) on the surface of a memory chip as shown below:

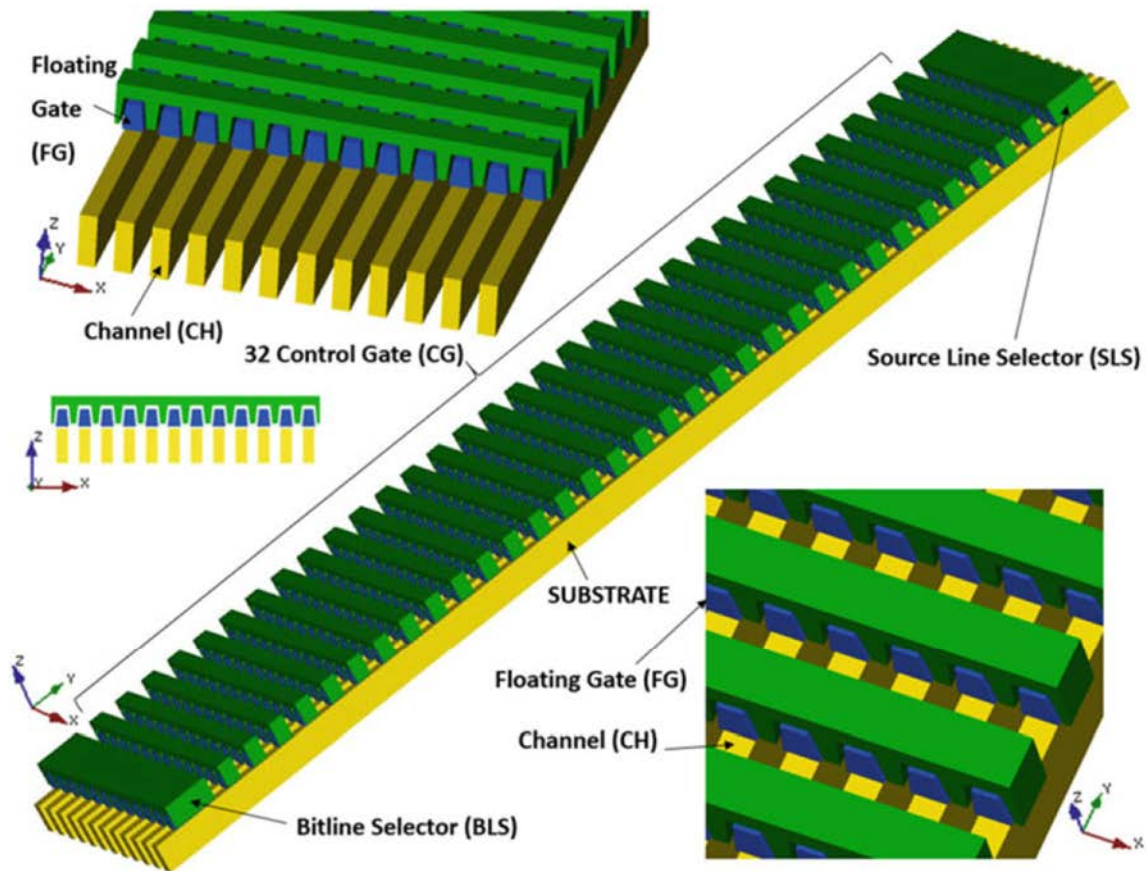


Fig. 3.9 Bird's-eye view of a planar NAND string

Ex. 1013 (3D Flash Memories Textbook), at 86.

46. To boost data storage densities and reduce cost per gigabit, the art developed so-called “three-dimensional (3D) NAND flash cells” starting in about 2006. Ex. 1014 (Aritome Textbook), 292. Unlike planar 2D NAND flash memory, in 3D NAND flash memory the memory cells are arranged in vertical, cylindrical NAND flash columns, often referred to as “memory strings.” Conceptually, a modern 3D NAND structure could be conceived by starting from the 2D NAND

string building block and turning the 2D NAND string on its side, resulting in a 3D structure with a vertical channel. The following image provides an example:

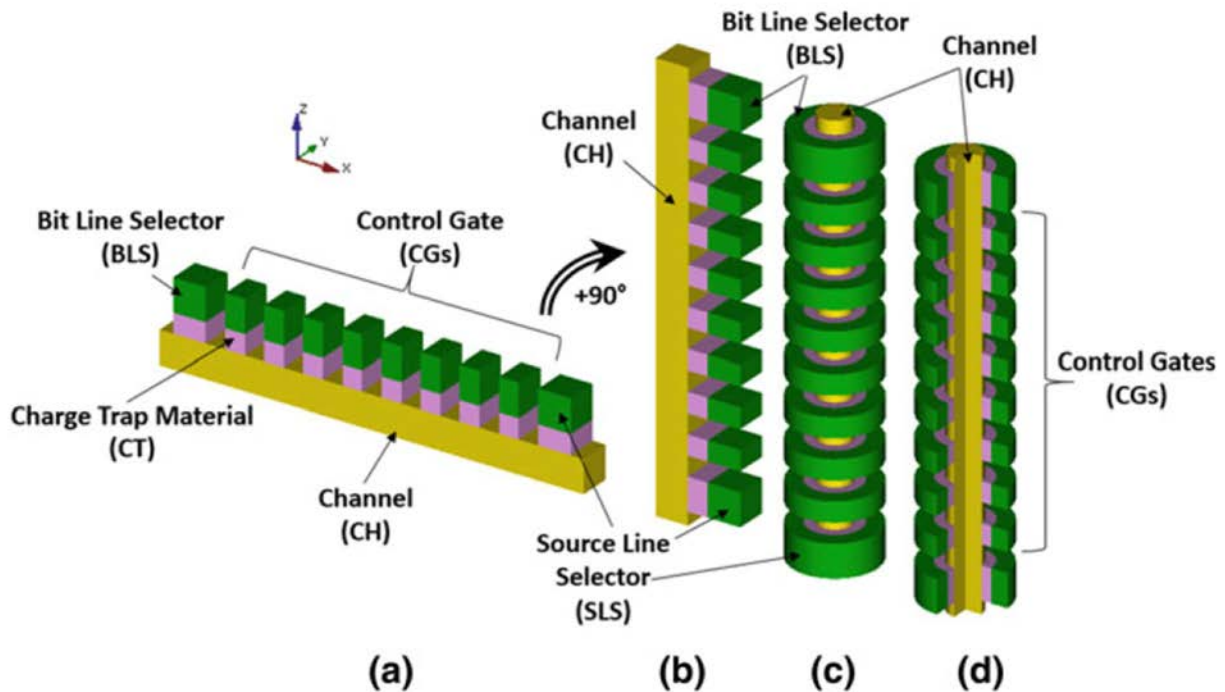


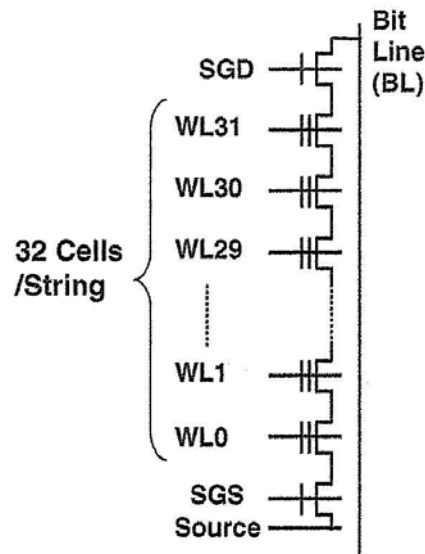
Fig. 4.1 NAND Flash string with horizontal gate and vertical channel: **a** planar, **b** planar rotated by 90°, **c** vertical channel with cylindrical shape and **d** its cross section

Ex. 1013 (3D Flash Memories Textbook), 102. As labeled in Fig. 4.1, above, each NAND string includes a “cylindrical channel.” *Id.*, 58. The concept of a “channel” was well-known in semiconductor devices and refers to a thin and layer of charge that is formed between the source and drain of a transistor when a voltage is applied to the gate. The “channel” is highly conductive and allows current to easily flow between the source and drain. The “cylindrical channel” in 3D NAND devices also provides the means for current to flow in a memory string.

47. Multiple of such vertical channels are then repeated in a three-dimensional array. Ex. 1014 (Aritome Textbook), 296.

48. As can be seen above, the NAND flash memory “strings” each contain multiple cells “connected in series.” Ex. 1014 (Aritome Textbook), 38. The source of one cell is connected to the drain of the next one. Depending on the technology, typically a string consists of 32 to 128 NAND cells.

49. Each end of a string is terminated with a “select transistor.” One is often called the “SGD” (drain-end select gate transistor) and the other one is often called “SGS” (source-end select gate transistor). The “SGD connects” at the string’s drain side “to isolate it from the bit line (BL).” Ex. 1014 (Aritome Textbook), 38. Hence, the SGD is also known as the “bit line select transistor” or the “upper select gate.” The SGS connects at the string’s source side “to isolate it from a source line (SL).” *Id.* Since the source line is commonly connected to the ground terminal, SGS is also known as the “ground select transistor” or the “lower select gate.” Word lines are connected to each memory cell control gate. *Id.*, 38-39. A schematic representation of a memory string is shown below:



Ex. 1014 (Aritome Textbook), 39.

50. Various architectures for constructing 3D NAND flash memory were known in the art. One such example is the well-known BiCS (Bit Cost Scalable) architecture, where various “contacts” (electrical connections) are formed on top of the memory array. Below are two illustrations of the BiCS architecture show top and bottom perspective views.

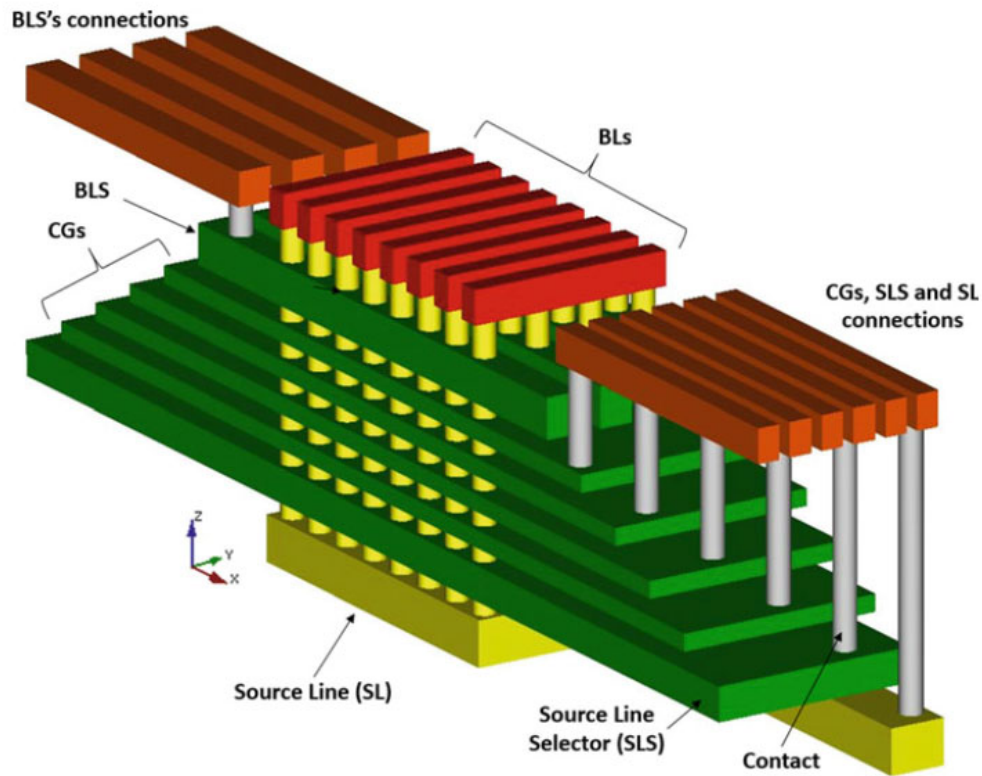


Fig. 4.13 Top bird's eye view of BiCS with gate connections

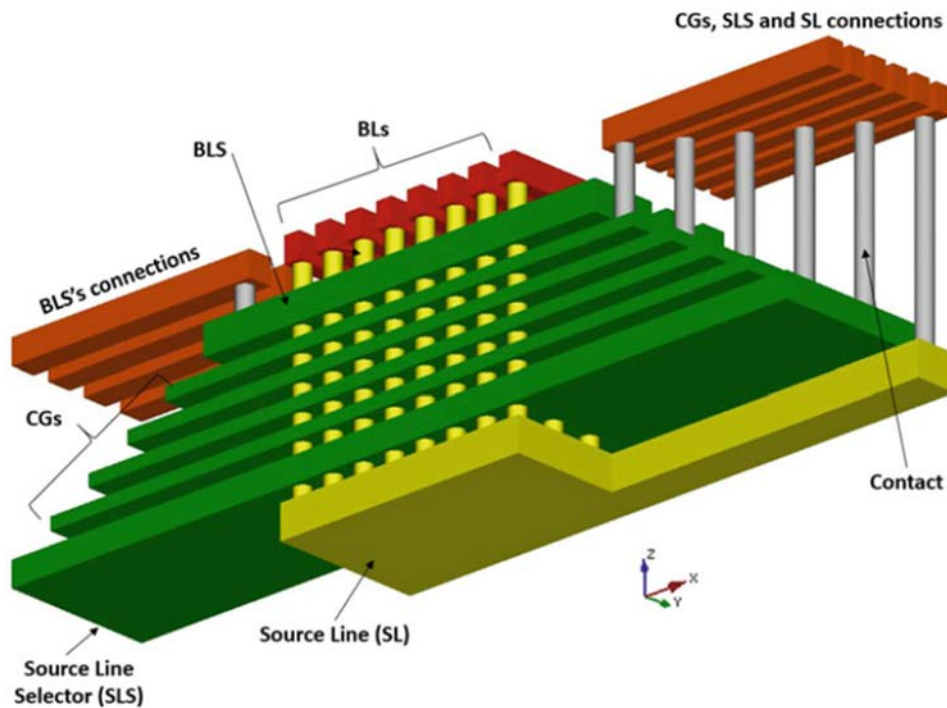


Fig. 4.14 Bottom bird's-eye view of BiCS with gate connections

Ex. 1013 (3D Flash Memories Textbook), 109-110. As is traditional in MOSFET transistors, the “source” terminal connects to a low voltage, such as ground. The same holds true in 3D NAND design, and the BiCS architecture includes source line contacts for providing a low voltage (*e.g.*, ground) connection to the memory strings. This is shown in yellow in the figures above.

51. The individual memory cells in a memory string are accessed by word lines that typically extend horizontally and connect to a control gate for a given cell on each memory string. On the periphery of the 3D NAND device, the word lines form a staircase structure, where each subsequent word line protrudes a short distance beyond the word line above it, like a staircase, as shown below in green.

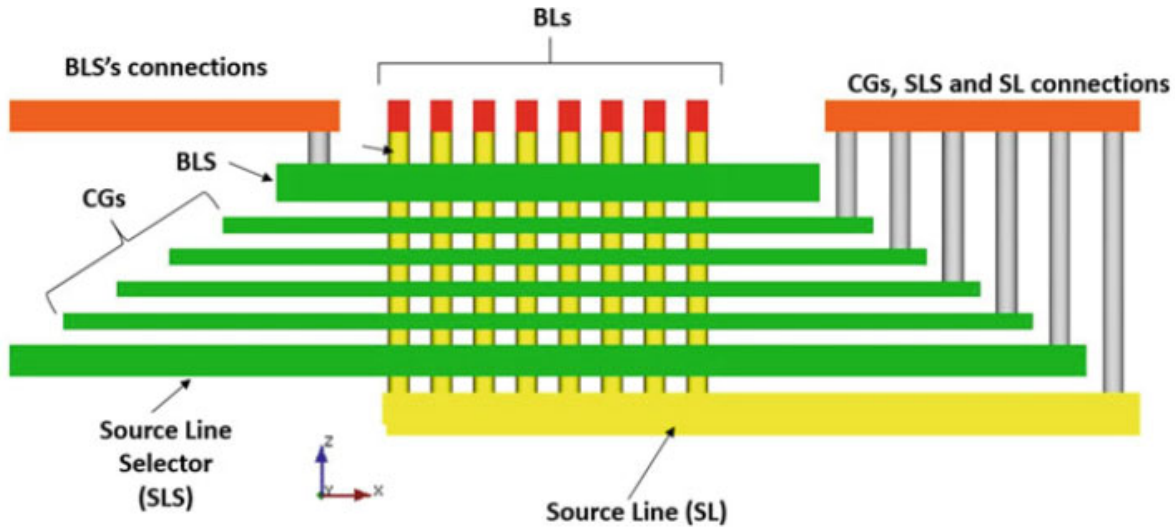


Fig. 4.12 Vertical cross section of BiCS with gate connections

Ex. 1013 (3D Flash Memories Textbook), 109 (green control gates forming a staircase). As noted, each word line delivers a control signal to a number of memory cells at the same horizontal level in the 3D NAND memory device.

52. The collection of memory cells controlled by a common signal together constitute a “word,” and the control gate is a “word line.” *Id.*; Ex. 1014 (Aritome Textbook), 41. The grey columns in the figure above, often referred to as “local contacts,” show how the word lines can be controlled by signals on the top surface of the 3D NAND device. In the context of 3D NAND chips, “local contacts” refer to the electrical connections made within the memory device to link various components such as the word lines and source lines. In facts, local contacts are also often referred to as “vias,” which have been widely known and used in all sorts of semiconductor devices for many decades. These vias create vertical electrical

connections between the different layers within the 3D NAND stack. They are integral to the architecture of semiconductor devices generally, including 3D NAND technology where they enable the functional linkage of stacked memory cells across multiple layers. Note that these local contacts can be of various lengths – some long and some very short. For example, the local contacts (the grey columns in the figure above) that connect to the word lines located near the top of the memory stack are very short while the grey column that connect to the source line is much longer. Where local contacts are connecting an existing vertical structure, such as a memory string or slit, the local contacts tend to be relative short. I note in this regard that the '806 patent gives examples of long local contacts (*e.g.*, an entire TAC) and short local contacts (*e.g.*, atop channel structures and slits). *See* Ex. 1001, 11:20-34.

53. A variety of modifications to the BiCS architecture were known, including the use of slit structures to serve as source line contacts for the NAND strings. Exemplary slit structures are shown in purple below. These particular slit structures function as contacts for connecting to the source (which may be shared by some, or all, memory strings) located on the bottom of the 3D NAND device.

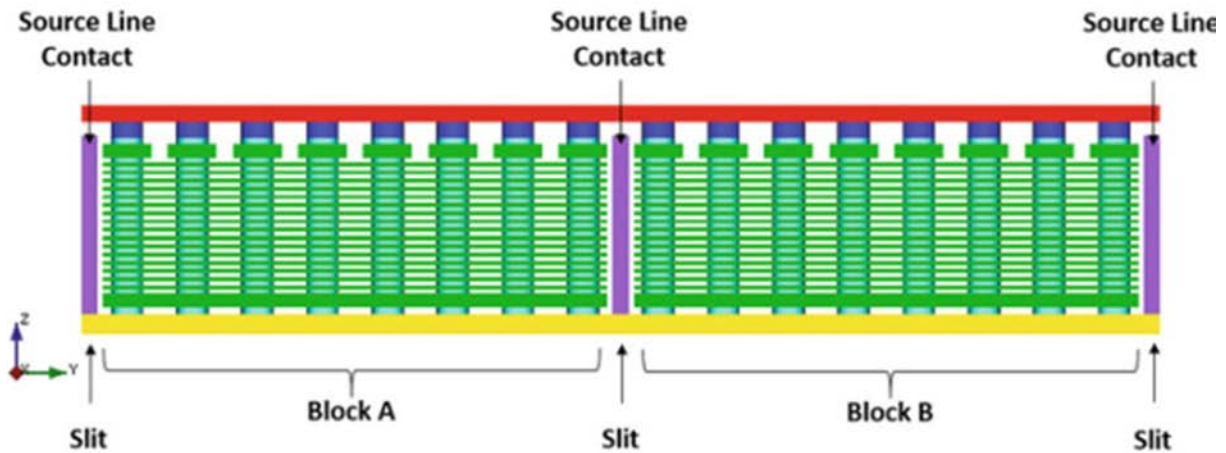


Fig. 6.8 Side view of Fig. 6.7

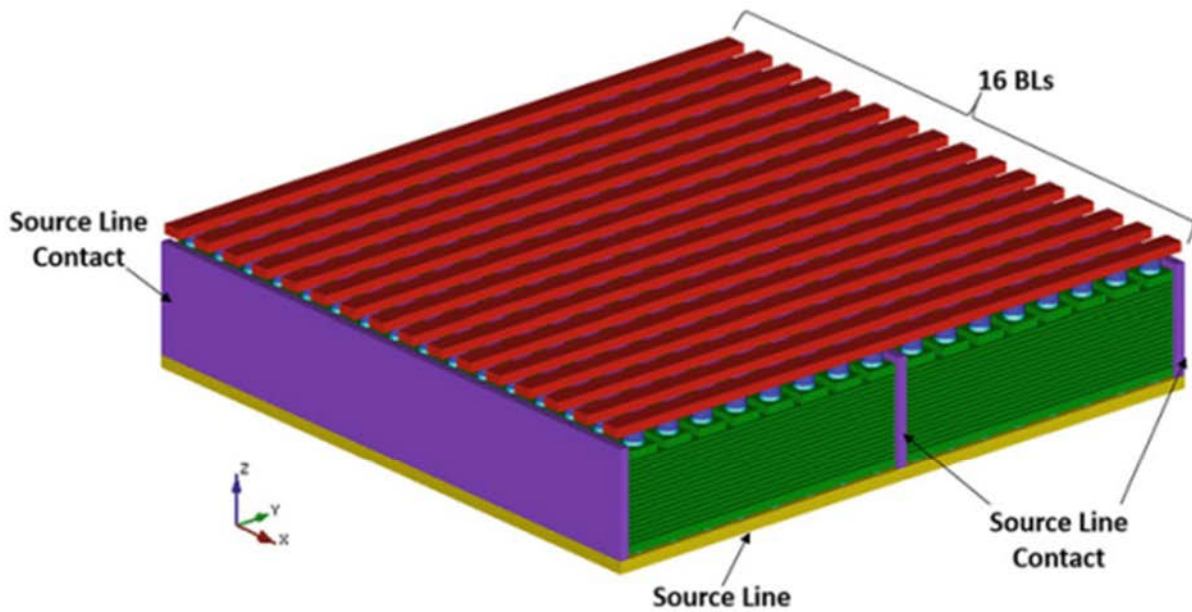


Fig. 6.7 Array slits

Ex. 1013 (3D Flash Memories Textbook), 185.

54. In both figures above, gaps are shown between the various structures. In actual 3D NAND memory devices, these “gaps” are not empty space; rather, they are filled with insulating material (known as “dielectric” material). Among other

things, dielectrics serve to isolate electrical signals and prevent one conductive structure from interfering with another other. Another function performed by the dielectric is mechanical support to prevent the other structures from collapsing.

55. Three-dimensional NAND memory devices commonly used support pillars to maintain the device's structural integrity, particularly when etching away sacrificial gate layers. Ex. 1015 (U.S. Pat. Publ. No. 2018/010867), [0051]. Because the etching away of sacrificial gate layers causes numerous voids (that is, empty spaces) in the device, the support pillars are used to maintain the device's structural integrity. A number of techniques were known for forming support pillars, e.g., using a dummy memory string. E.g., *id.*, Fig. 19A (support pillar structure 20); Ex. 1016 (U.S. Pat. Publ. No. 2019/0229125, Fig. 8 (same); Ex. 1017 (U.S. Pat. No. 10,354,980), 10:10-13 (same). These "dummy" strings have the benefit of being formed by the same process steps as the (functioning) memory strings. In addition to providing structural support and maintaining the integrity of the memory cell arrays during the manufacturing process, the dummy (non-functional) memory strings aid in achieving more uniform deposition of materials during layering process of 3D NAND fabrication. Furthermore, during device operation, dummy strings assist in heat distribution within the memory array, thereby reducing local hotspots that can affect device reliability. By having dummy strings separating blocks of active memory cells and TAC's, they help in isolating and protecting the

functional cells from electrical interference and thereby improving overall memory performance.

56. Well before the effective filing date of the '806 patent, companies (including Micron) had developed various techniques for manufacturing 3D NAND flash memory, many of which leveraged fabrication principles and materials that had been in use generally in the semiconductor manufacturing industry for decades.

57. The fabrication of 3D NAND memory chips involves etching techniques to construct vertical, high-density storage architectures. These etching processes, fundamental to semiconductor manufacturing, have been well established prior to 2018 but have been adapted for 3D NAND. Here are just a few examples of etching processes used for 3D NAND. Channel hole etching which typically makes use of a dry etching process, e.g., deep reactive ion etching (DRIE) to create vertical channels through the NAND stack. DRIE was developed in the mid-1990s, allows for etching with high aspect ratios, essential for the vertical structures in 3D NAND. Staircase etching involves sequential etching steps to create a staircase-like structure for accessing word lines across each memory layer. This process leverages standard lithographic and etching techniques known long before 2018, adapted to create the precise, repetitive structures needed for multi-layer access. Hard-mask etching process, well-known long before 2018, involves depositing a durable material like nitrides which is then patterned using photolithography to serve as a

mask. The hard mask protects underlying layers during subsequent etching. Selective etching is used to remove specific materials without damaging others by using different chemistries in plasma to target certain layers of materials, again was well-known long before 2018. Spacer etching which involves depositing and then partially removing the material developed to define narrow, uniform spacers (gaps) for cell isolation. Spacer etching processes was developed for lightly-doped drain (LDD) MOSFETs back in the 1980's and adapted for 3D NAND manufacturing process. Each of these processes originates from fundamental techniques known in semiconductor manufacturing well before 2018, adapted for the advanced architecture of 3D NAND.

58. Stacking multiple chips, also known as 3D integration, was just one of many advancements in semiconductor technology that have happened over the years. The concept of 3D integration should not be confused with 3D NAND. Although 3D integration has application to 3D NAND chips, the concept of vertically stacking multiple dies/chips predates 3D NAND by many years and has been used extensively in a variety of chip technologies. This method significantly enhances device performance and functionality while conserving space, addressing the limitations faced by traditional planar scaling methods. Naturally, when stacking multiple dies on top of one another, via structures (also called through-silicon vias (TSVs) or through-array contacts (TACs)) were implemented to provide connections

between different chips in the stack. The concept of TACs predates 2018 and was developed to meet the growing demands for increased functionality and higher performance without expanding the chip's footprint. These vertical connections are essential for shortening the path electrical signals must travel compared to traditional methods like wire bonding or flip-chip techniques. By reducing the length of interconnects, TACs enhance signal speed and reduce power consumption. Before 2018, the semiconductor industry recognized the potential of through-array contacts to mitigate the slowing pace of enhancements afforded by Moore's Law due to physical and economic limits.

59. In summary, techniques for manufacturing 3D NAND memory devices were well-known in the art before the '806 patent's effective filing date.

B. Epitaxy

60. As of 2018, a POSITA would have well understood the semiconductor manufacturing process called "epitaxy."

61. Epitaxial growth in semiconductor manufacturing processes involves depositing a crystalline layer of material onto a crystalline substrate in a way that the crystallographic orientation of the deposited material matches that of the substrate. Ex. 1029 (Chang, ULSI Technology), 132 (in epitaxy, material is "grown" on a substrate). Using an epitaxial process results in high-quality deposited layer, which can be useful for advanced integrated circuits including 3D NAND memory devices.

62. Well before 2018, use of the epitaxial growth process in 3D NAND structures was well known. For example, an epitaxial layer had been disposed between the substrate and the first channel structures primarily for enhancing the device's performance and reliability, as illustrated in the below figure:

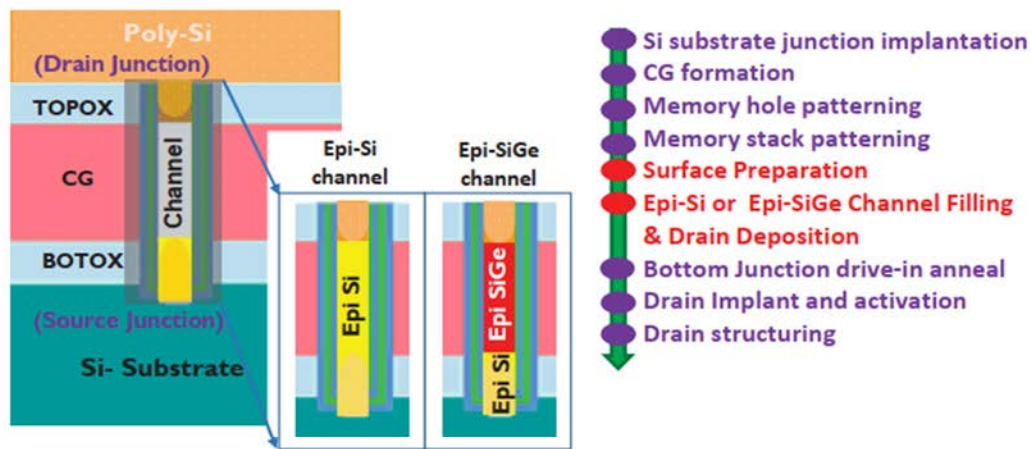


Fig. 1: Schematic view of our vertical NAND single test vehicle. Added/modified steps w.r.t. poly-Si-based process flow are highlighted in red.

Ex. 1034 (Capogreco, Integration and Electrical Evaluation), at 1.

63. This epitaxial layer serves several functions. It provides a high-quality interface between the channel structures and the underlying substrate, which can reduce device degradation over time. It also serves as a barrier, preventing impurities from the substrate from contaminating the channel materials, thus ensuring consistent device behavior and longevity. The epitaxial process provides a stable crystalline template that matches the crystal structure of the underlying

substrate. This alignment helps minimize defects that could propagate through the subsequent layers. These defects can potentially degrade the electrical performance and reliability of the 3D NAND device. The epitaxial layer also provides consistent and uniform electrical properties. The uniformity can help minimize variability of charge mobility and carrier lifetimes. See, e.g., Ex. 1035 (Kim, 3-Dimensional NAND Flash), at 2 (“Flash memory having the single-crystalline channel is expected to have the better performance such as a uniform threshold voltage distribution and stable bit-line (BL) current.”); Ex. 1034 (Capogreco, Integration and Electrical Evaluation), at 4 (epitaxially-grown silicon has superior conductivity).

64. “The success of an epitaxial growth relies heavily on the chemistry used in the process,” which may include “hydrogen and chlorosilanes, such as silicon tetrachloride (SiCl_4), trichlorosilane (SiHCl_3), and dichlorosilane (SiH_2Cl_2). In addition, silane (SiH_4) has also been used when a lower growth temperature is desired. The choice of each source gas is based on the growth conditions and layer requirements.” Ex. 1029 (Chang, ULSI Technology), 143.

C. Etching

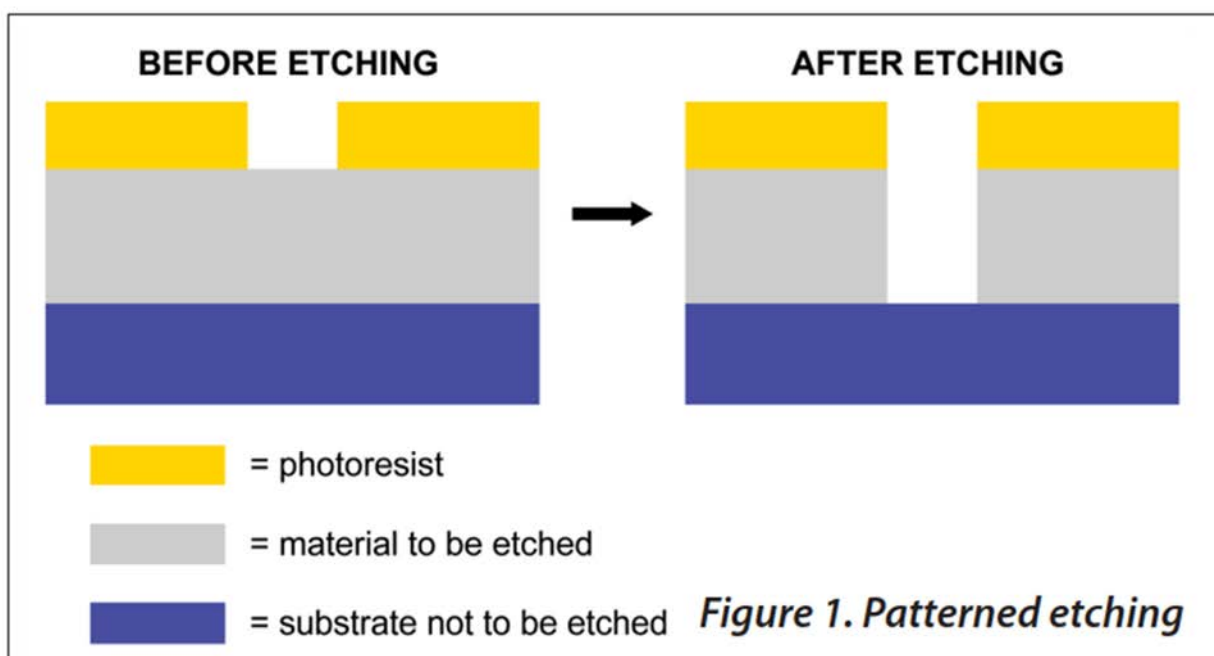
65. The fabrication of 3D NAND memory chips involves etching techniques to construct vertical, high-density storage architectures. These etching processes, fundamental to semiconductor manufacturing, have been well established prior to 2018 but have been adapted for 3D NAND. Here are just a few examples

of etching processes used for 3D NAND. Channel hole etching which typically makes use of a dry etching process, e.g., deep reactive ion etching (DRIE) to create vertical channels through the NAND stack. DRIE was developed in the mid-1990s, allows for etching with high aspect ratios, essential for the vertical structures in 3D NAND. Staircase etching involves sequential etching steps to create a staircase-like structure for accessing word lines across each memory layer. This process leverages standard lithographic and etching techniques known long before 2018, adapted to create the precise, repetitive structures needed for multi-layer access. Hard-mask etching process, well-known long before 2018, involves depositing a durable material like nitrides which is then patterned using photolithography to serve as a mask. The hard mask protects underlying layers during subsequent etching.

66. A POSITA would have well understood techniques for “etching,” a well-known semiconductor manufacturing technique used to remove material. Ex. 1029 (Chang, ULSI Technology), 356-57; Ex. 1031 (Jaeger, Introduction to Microelectronic Fabrication), 35-36. A chemical that is used to etch material is known as an “etchant.” Well before 2018, a POSITA would have known of etchants that are “selective.” A selective etchant is one that reacts to (and thus removes) some materials preferentially to others. *Id.*, 35. For example, it has long been known that carbon tetrafluoride (CF₄), when paired with a concentration of hydrogen (H₂) greater than 40%, can selectively etch silicon dioxide over silicon, by forming

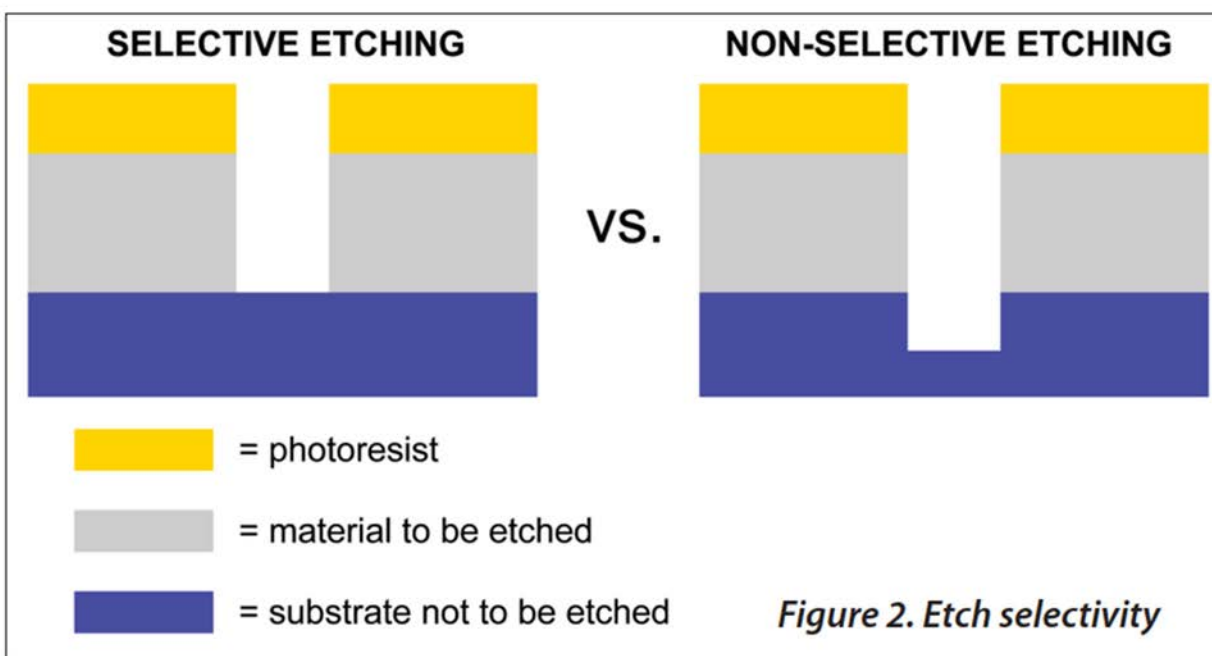
volatile compounds that can be easily removed, leaving the silicon substrate largely unaffected. Ex. 1029 (Chang, ULSI Technology), 363-64.

67. The etching process is illustrated in the following figure:



Ex. 1036 (HBr), at 1. As Figure 1, above, shows, “patterned etching” involves placing a photoresist (a material resistant to etching that is typically formed using photolithography) to shield certain material from the etching process. Then, an etchant is applied to the exposed surface. As a result, the material to be etched is removed but the material covered by the photoresist remains intact.

68. Figure 2, below, shows the difference between a selective etch and a non-selective etch:



Ex. 1036 (HBr), at 2. As Figure 2 shows, a non-selective etch may result in material being removed not only from the material to be etched but also from the substrate.

69. Selective etching, which is used to remove specific materials without damaging others by using different chemistries to target certain layers of materials, again was well-known long before 2018. Spacer etching involves depositing and then partially removing the material developed to define narrow, uniform spacers (gaps) for cell isolation. Spacer etching processes were developed for lightly-doped drain (LDD) MOSFETs back in the 1980's and adapted for 3D NAND manufacturing process. Each of these processes originates from fundamental techniques known in semiconductor manufacturing well before 2018, adapted for the advanced architecture of 3D NAND.

70. Prior to 2018, the application of selective etching in 3D NAND fabrication was already well known. This process enabled manufacturers to develop multi-layered NAND structures, significantly increasing storage capacity and efficiency. By precisely removing specific materials without damaging others, this technique allowed for the construction of vertical channels and intricate interconnects between the stacked arrays of memory cells. For example, selective etching enables the creation of very fine structures, such as the staircases for wordline connections. A POSITA would have known that any deviation in etching could lead to defects that impair the functionality of the memory chip and reduce its data retention capabilities. Thus, the accuracy of selective etching governed the uniformity and performance of the final product, directly impacting yield rates and reliability.

71. A POSITA would have known of the common use of a material to which an etchant is **not** selective as an “etch stop,” that is, to prevent the etch from removing material not intended to be removed. Ex. 1037 (Baker, CMOS Circuit Design), 48 (an “etchant stop layer is used”). For example, a POSITA would have known of the use of polysilicon to stop an etch through silicon oxide. Ex. 1032 (U.S.

Pat. No. 5,776,808), 4:25-35 (polysilicon used as “etch stop layer”);¹ Ex. 1033 (U.S. Pat. No. 9,236,393), 17:20-24 (“[t]he isotropic etch creates a trench ... that stops at the doped polysilicon layer”).

VII. THE ’806 PATENT

A. Effective Filing Date

72. I understand that the application leading to the ’806 patent was filed on May 5, 2020.

73. Based on my review of the ’806 patent, I note that it also references a PCT application on its face, which was filed May 3, 2018.

74. For purposes of this declaration, I have been asked to assume that May 3, 2018 is the effective filing date of the ’806 patent. My opinions in this declaration were formed from the perspective of a POSITA as of May 3, 2018, including both the knowledge of a POSITA at that time as well as how a POSITA would have understood the ’806 patent and the prior art.

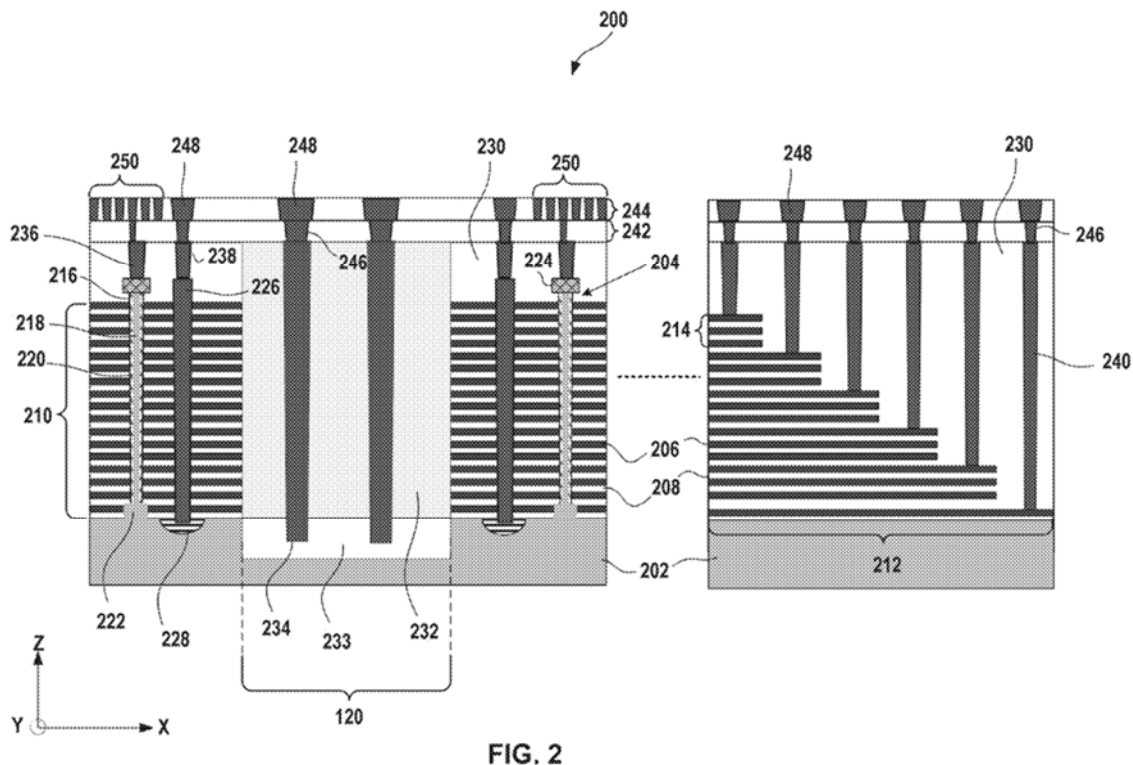
B. Overview

75. The ’806 patent relates to “three-dimensional (3D) memory devices.” Ex. 1001, 1:17-20. The title of the ’806 patent is “Through Array Contact (TAC)

¹ This prior art reference etches through a TEOS layer, which a POSITA would have understood to consist of silicon oxide.

For Three-Dimensional Memory Devices.” In particular, the specification describes and illustrates various “[e]mbodiments of interconnect structures of a three-dimensional (3D) memory device and method[s] for forming the interconnect structures.” *Id.*, Abstract.

76. To begin, as seen in Fig. 2 of the '806 patent below, the specification describes and illustrates a “3D memory device 200” with an overall 3D NAND architecture similar to that of the conventional BiCS architecture (*e.g.*, vertical memory strings, staircase region for word line access, etc.) that I discussed previously in the Technology Background.



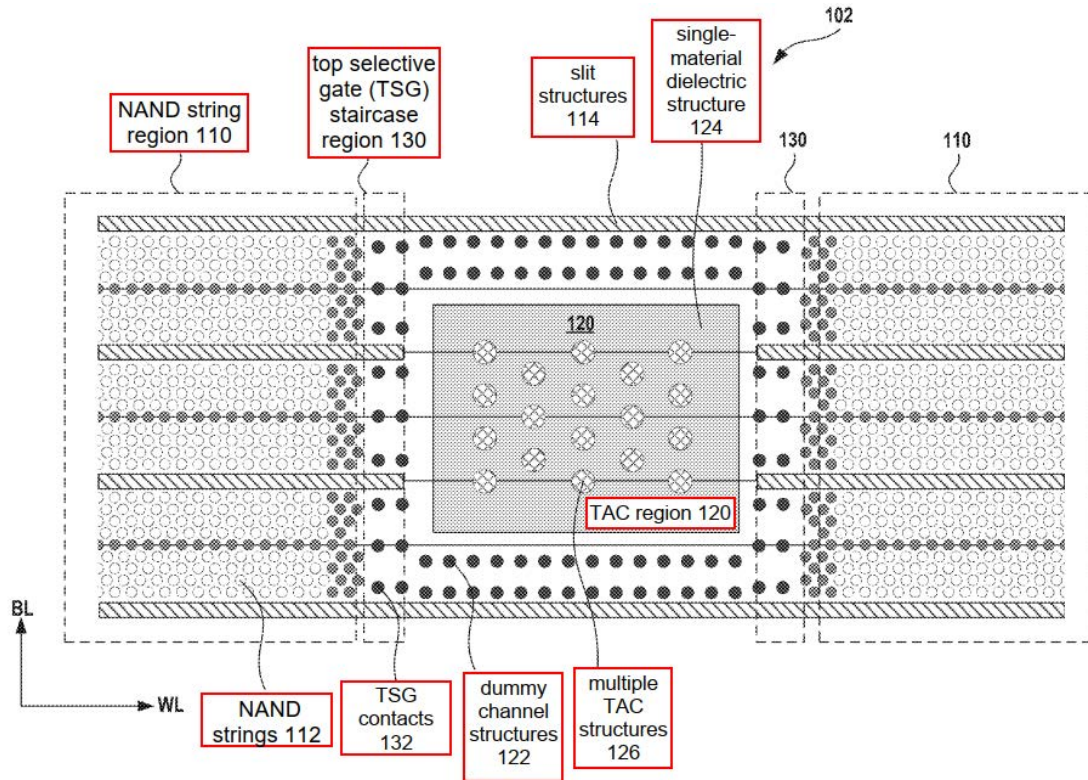
Ex. 1001, Fig. 2.

77. The “NAND strings 204” each “include[] a channel structure 216 that extends through alternating conductor/dielectric stack 210.” Ex. 1001, 9:7-9. The memory cells reside within each NAND string, and individual memory cells are formed where the word line intersects the NAND string.

78. The alleged point of novelty in the ’806 patent is a 3D memory device containing “vertical interconnects” that are located between a “stacked array device” (such as “3D memory device 200”) and a “peripheral device.” Ex. 1001, 5:38-65. In other words, the TACs may provide connections between separately fabricated chips (e.g., a memory chip and a controller chip) that are physically stacked on top of each other to form an overall 3D NAND memory device. *Id.*, 11:8-14. The ’806 patent refers to these vertical interconnects as “through array contacts” (“TACs”). *Id.*, 1:55-59; *see also id.*, Title (“Through Array Contact (TAC) For Three-Dimensional Memory Devices”). In Fig. 2 above, element 234 is a TAC. *Id.*, 10:62-64. According to the specification, “[t]he interconnect structures allow contacts to various memory array structures (e.g., NAND strings, gate line slits, word lines, etc.) to be fabricated in a limited number of steps (e.g., in a single step or in two steps), thereby reducing the process complexity and manufacturing cost.” *Id.*, 5:41-46. The cross-sectional profile of the TACs resembles that of a via and tapers slightly from top to bottom, as is common with semiconductor etch processes, which have long been well-known to POSITAs.

79. “In some embodiments, TACs 234 can provide electrical connections between 3D memory device 200 and the peripheral device (e.g., on a CMOS chip; not shown in FIG. 2).” Ex. 1001, 11:8-14. “Each TAC 234 can extend through the entire thickness of dielectric structure 232 and extend through at least a portion of STI structure 233 in a substrate 202.” *Id.*, 11:4-7. Given that the TACs may “provide electrical connections,” it is unsurprising that the specification teaches that “[e]ach TAC 234 is filled with conductor materials, including, but not limited to, W, Co, Cu, Al, doped Si, silicides, or any combination thereof.” *Id.*, 11:14-17. All of these materials were well-known to POSITAs for their conductive properties and had been used long before the ’806 patent.

80. Additionally, the ’806 specification discloses that “[m]ultiple TAC structures 126 can be formed within TAC region 120 in dielectric structure 124.” Ex. 1001, 6:20-22. An annotated version of Fig. 1A is presented below which is a top view showing a “TAC region 120” with multiple TAC structures 126 therein. Around the periphery of TAC region 120 there are various “dummy” channel structures 122 that provide structural support but serve no electrical function. *Id.*, 6:22-25.



Id., Fig. 1A (annotated). Annotated Fig. 1A above also shows the “NAND string regions” 110, among other features.

81. The ’806 patent’s 3D memory device includes an “[e]pitaxial plug” (element 222 in Figure 2) between each “channel structure” (labeled as element 216 in Figure 2) and the “substrate” (labeled as element at 202 in Figure 2). Ex. 1001, Figure 2. The ’806 patent explains that the “epitaxial plug” “can include, for example, a semiconductor material (e.g., single crystalline [silicon]) that is epitaxially grown from the substrate.” *Id.*, 9:42-44.

82. The ’806 patent’s 3D memory device also includes an “etch stop plug” (labeled as element 224 in Figure 2) between each “channel structure” 216 and

“NAND string contact” (labeled as element 236 in Figure 2). Ex. 1001, Figure 2. The ’806 patent explains that the “etch stop plug” is “an etch stop layer” made of a material such as polysilicon “that prevents etching of dielectrics,” “such as SiO₂ and SiN,” “in channel structure 216.” *Id.*, 9:49-52. “In some embodiments, etch stop plug 224 acts as the drain of NAND string 204.” *Id.*, 9:52-53.

C. Prosecution History

83. As noted above, I have reviewed the ’806 patent’s file history. I focus my discussion of the file history as it relates to the Challenged Claim. In this regard, the file history is quite short, consisting of a single Office Action, followed by a claim amendment and notice of allowance. In particular, in the first Office Action, the Examiner rejected the then-pending independent claims as obvious over U.S. Pat. No. 9,659,956 (“Pachamuthu”) in view of U.S. Pat. Publ. No. 2017/0186758 (“Lee”). I note in particular that the elements of original claim 12 (which is now challenged claim 10) were found to be known in the prior art.

84. In response to the rejection, the applicant amended what was then independent claim 9 (which subsequently issued as independent claim 8) to add the three limitations below:

- “first and second channel regions comprising first and second pluralities of channel structures, respectively”;

- “a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs)”;
- “a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.”

Ex. 1002, at 130, *see also id.*, 134-136.

85. Following the amendments above, the Examiner allowed the Challenged Claim. Ex. 1002, at 153. The notice of allowance did not specify which claim limitations of then claim 9 (now independent claim 8) distinguished the prior art.

86. I note that U.S. Pat. Publ. No. 2017/0179026 (Ex. 1005, “Toyama”) was cited in an IDS (among ***twenty-one*** other references), but was not used as the basis for a rejection or otherwise discussed by the Examiner in the file history. Ex. 1002, 81-82. As I discuss below, Toyama teaches or renders obvious each of the three claims elements that the applicant added by amendment, as well as all other elements of the Challenged Claim.

D. Claims

87. For reference, the Challenged Claim (*i.e.*, dependent claim 10) along with independent claim 8 of the '806 patent are reproduced below, with identifiers added for ease of referencing the individual claim elements:

8. A three-dimensional (3D) memory device, comprising:

[A] an alternating conductor/dielectric layer stack;

[B] a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;

[C] first and second channel regions comprising first and second pluralities of channel structures, respectively;

[D] slit structures extending vertically through the alternating conductor/dielectric layer stack;

[E] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[F] local contacts disposed on the first and second channel structures and the slit structures;

[G] a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of

through array contacts (TACs) extending vertically
through the dielectric structure; and;

[H] a plurality of non-electrically functional channel
structures surrounding the TAC region and between
the first and second channel regions.

10. The 3D memory device of claim 8, further
comprising:

[A] a substrate;

[B] an etch stop plug interposed between each local
contact of the local contacts and each channel
structure of the first and second channel structures;
and;

[C] an epitaxial layer disposed between the substrate
and the first or second channel structures.

VIII. CLAIM CONSTRUCTION

88. I am not a legal expert or an attorney and offer no opinions on the law. I understand that claim construction is a matter of law. However, I have been informed by counsel of the legal standards that apply to claim construction in an *inter partes* review, and I have applied them in forming my opinions. I understand that during an *inter partes* review, the same claim construction standard used in federal district court is applied when addressing the meaning of claim terms.

89. I have been informed that the words of a claim are generally given their plain and ordinary meaning that the term or phrase would have to POSITA at the

time of the invention in view of the surrounding claim language, the specification and the file history (collectively, the “intrinsic evidence” or “intrinsic record”).

90. I also understand that courts may consider extrinsic evidence, such as expert and inventor testimony, dictionaries, and learned treatises (collectively, the “extrinsic evidence” or the “extrinsic record”), but that such extrinsic evidence should be given less weight than the intrinsic evidence.

91. In my opinion, the Challenged Claim does not require further construction and can be afforded its plain and ordinary meaning for purposes of the analysis of the prior art that I am conducting in this declaration.

IX. UNPATENTABILITY ANALYSIS

92. For the reasons I explain in greater detail below, it is my opinion that as of the effective filing date of the ’806 patent, claim 10 of the ’806 patent is unpatentable as obvious over the prior art discussed in this declaration.

A. Overview of the Prior Art - Toyama

93. The following paragraphs provide an overview of the sole primary reference I discuss throughout this declaration.

94. Toyama (U.S. Pat. Publ. No. 2017/0179026 A1) is titled “Through-Memory-Level Via Structures for a Three-Dimensional Memory Device.” Ex. 1005, Cover. Toyama was filed September 19, 2016, and issued on June 22, 2017. *Id.* Toyama claims priority to a provisional application filed on December 22, 2015. *Id.*

I am informed that Toyama is prior art under at least 35 U.S.C. §102(a)(1) and §102(a)(2).

95. Toyama is generally directed to “[a] three dimensional NAND memory device” that includes conventional 3D NAND memory features such as “an alternating stack of word lines and insulating layers located over the word line driver devices” and “a plurality of memory stack structures extending through the alternating stack.” Ex. 1005, Abstract. Toyama also discloses “through-memory-level via structures” that “extend through a through-memory-level via region located between a staircase region of the first memory block and a staircase region of another memory block.” *Id.*

96. Toyama is a lengthy reference, including 76 figures (many with sub-parts) and over 60 columns of text. Much of Toyama describes the manufacturing processes and techniques used to form the 3D NAND memory structures it describes. I will highlight here only two of Toyama’s embodiments, which are the focus of my substantive invalidity analysis. The first is Toyama’s “first exemplary structure,” which is depicted in Figs. 1-17, and described in the accompanying text. *See generally* Ex. 1005, [0014]-[0048], [0163]-[0260]. The second is Toyama’s “second modification to fourth exemplary structure,” which I refer to hereafter as Toyama’s “Second Modification” for shorthand. Toyama’s Second Modification is depicted in Figs. 44-49, and described in the accompanying text. *Id.*, [0093]-[0103],

[0332]-[0342]. I note that other figures and text are also relevant as some of Toyama's disclosure and teachings are generally applicable to all embodiments, and certain aspects of one embodiment are simply expanded upon by other embodiments. Each of Toyama's first exemplary structure and Second Modification, alone and in combination, disclose and/or render obvious, the Challenged Claim for the reasons I discuss in Section IX.B.

97. ***First Exemplary Structure.*** Many of the features of Toyama's first exemplary structure (*e.g.*, alternating layers of conductor/dielectric, memory array region 100 containing memory strings that extend through the stack of alternating conductors 146, 246 and dielectrics 132, 232, a staircase structure, word line contacts 86 on the staircase structure, etc.) can be seen in the cross-sectional diagram of Fig. 17C below.

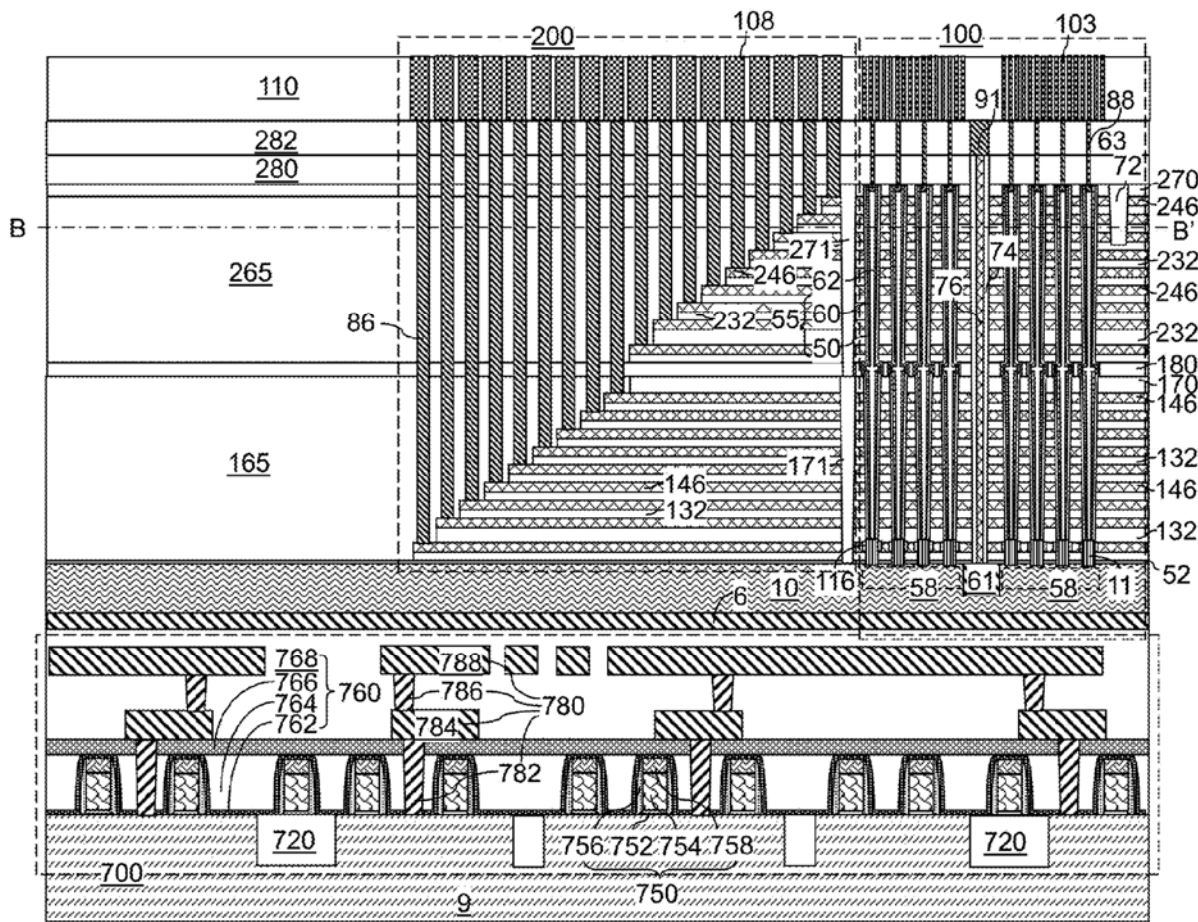


FIG. 17C

Ex. 1005, Fig. 17C.

98. And, like the '806 patent's *through array contacts*, Toyama's first exemplary embodiment discloses 3D NAND memory devices with "through-memory-level via structures," which are vias that extend through the memory array to provide electrical connection to "peripheral" devices. Ex. 1005, [0164] (discussing "peripheral device region 700" located underneath the "memory-level assembly").

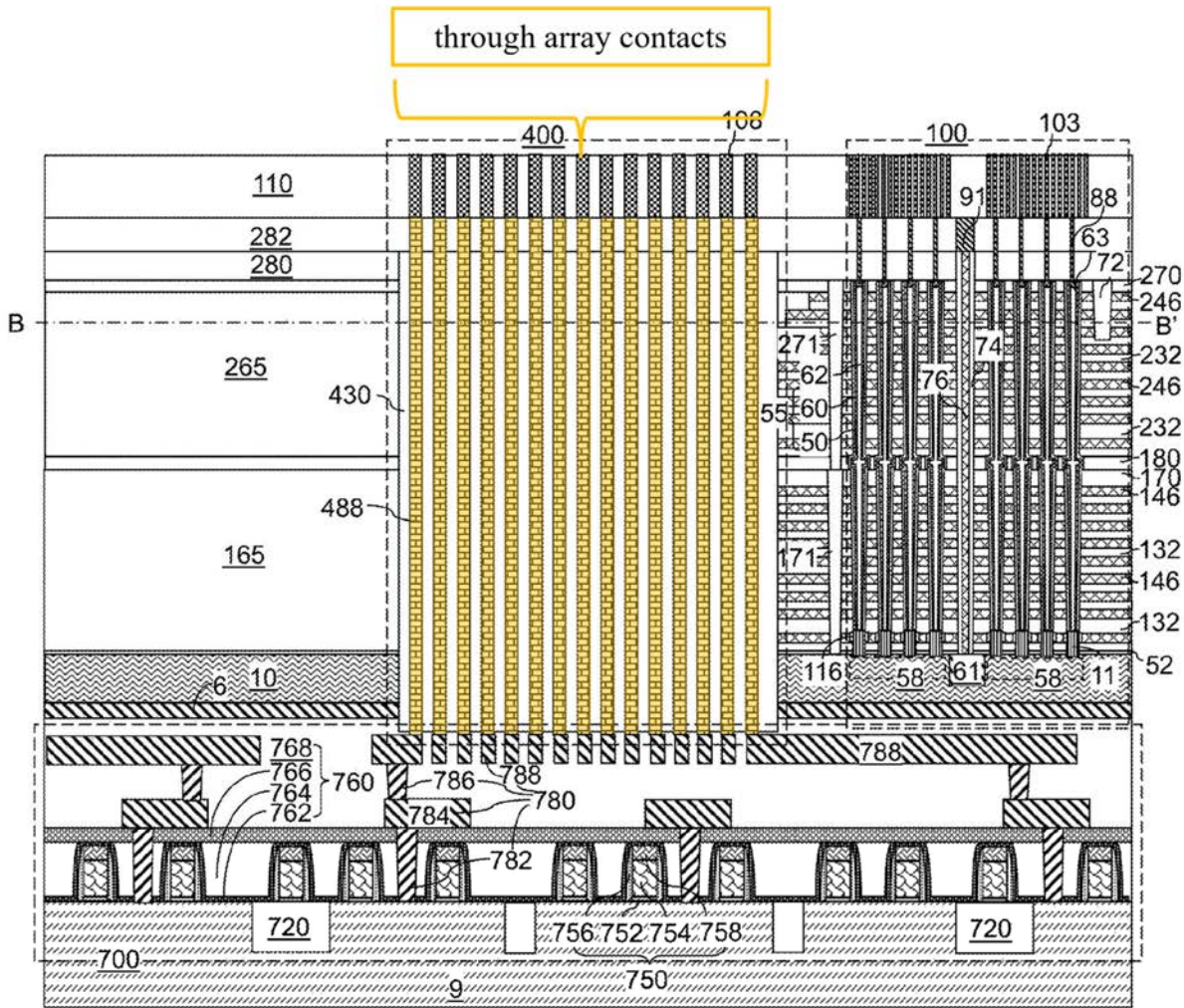


FIG. 17A

Id., Fig. 17A (annotated).

99. As I mentioned in my introduction to this declaration, this is the second declaration I have provided on the '806 patent. The claim to which this declaration pertains includes two primary limitations not discussed in my prior declaration: the “epitaxial layer” limitation, and the “etch stop plug” limitation. Toyama discloses both of these limitations.

100. Toyama discloses a layer between its substrate (“planar semiconductor material layer 10”) and its “memory stack structures 55” that it calls “pedestal channel portions 11” or “epitaxial channel portions 11.” Ex. 1005, Figures 17A, [0202], [0208]. The latter name would have confirmed to a POSITA that element 11 is formed using an epitaxial process, and that “portions 11” is an *epitaxial layer*.

101. Toyama also discloses an element between each of “memory stack structure 55” and “drain contact via structure 88” that Toyama calls a “drain region 63.” Ex. 1005, Figure 17A, [0209], [0241]. Toyama’s “drain regions 63” are made of a material such as polysilicon, and the POSITA would have recognized that they act as an etch-stop and prevent etching of dielectrics within “memory stack structure 55.” (For more detail, see my discussion of limitation [1.G].) A POSITA would have recognized that “drain regions 63” serve as the drains of “memory stack structures 55.” *Id.*, [0209], [0241], [0251]. As explained in further detail at limitation [1.G], because “drain regions 63” are plugs that stop an etch from reaching “memory stack structures 55,” they are *etch stop plugs*.

102. ***Second Embodiment.*** Many of the features of Toyama’s Second Embodiment (*e.g.*, alternating layers of conductor/dielectric, memory array region 100 containing memory strings that extend through the stack of alternating conductors, etc.) can be seen in the cross-sectional diagram of the 3D NAND memory device in Fig. 49 below. And, like the ’806 patent’s *through array contacts*,

Toyama's Second Embodiment discloses "through-memory-level via structures 676" (highlighted in yellow below) that extend through the memory array to provide electrical connection to "peripheral" devices. Ex. 1005, [0341], [0164] (discussing "peripheral device region 700" located underneath the "memory-level assembly").

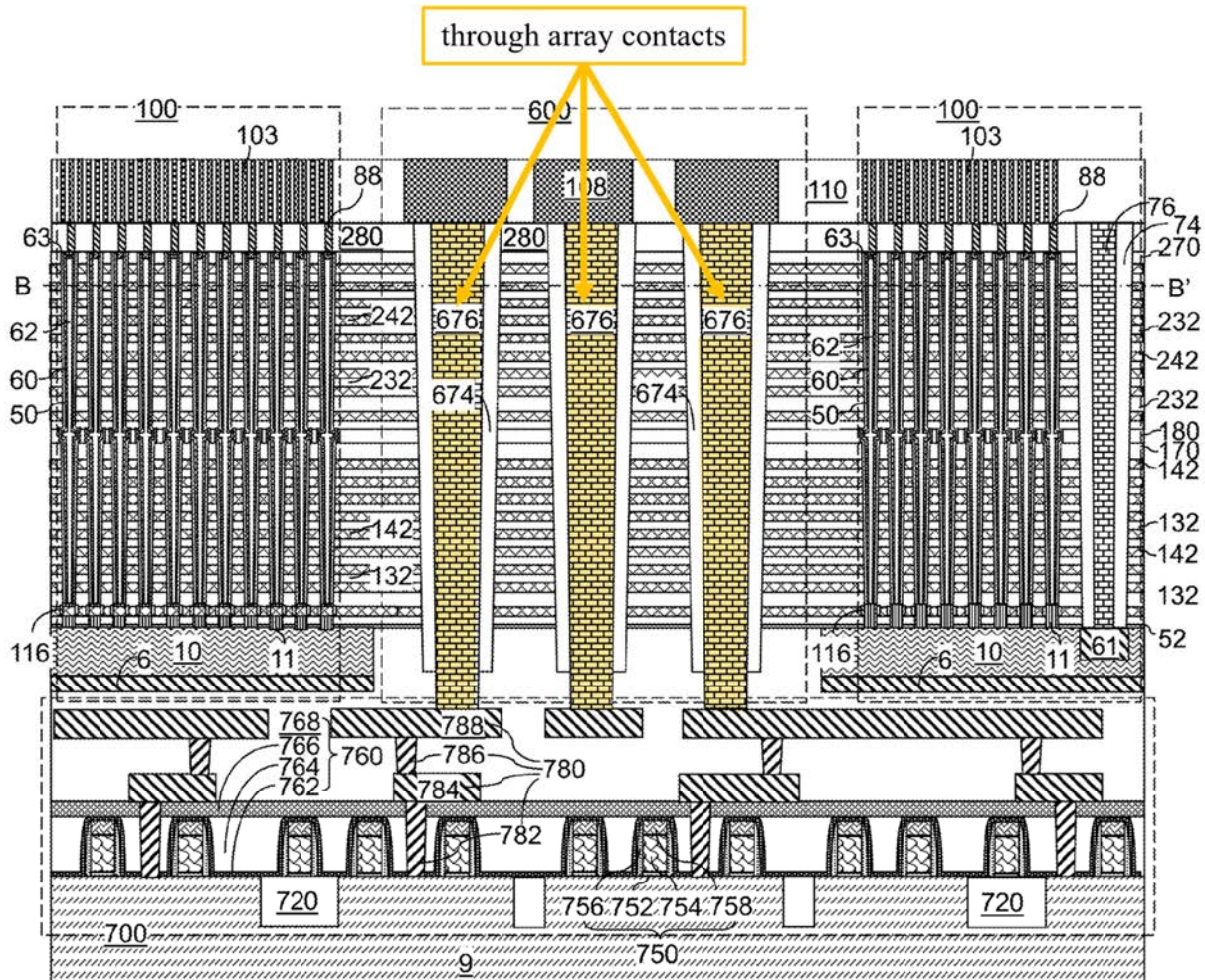


FIG. 49

Id., Fig. 49. As the above figure shows, Toyama's Second Modification—like its first exemplary structure—includes *an epitaxial layer* ("pedestal channel portions 11") and *an etch stop plug* ("drain region 63").

103. The last observation I will make here is that many of Toyama's figures build on one another to illustrate various steps in the fabrication process (*e.g.*, one figure will show an etch step to create a cavity and the next figure will show the cavity being filled with a dielectric or conductor). This is helpful to know, especially when initially reviewing Toyama.

B. Ground 1: Toyama's Second Modification in View of the Knowledge of a POSITA

104. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Toyama's "second modification of the fourth exemplary structure" (which I refer to as Toyama's "Second Modification" for shorthand) renders claim 10 of the '806 patent obvious.

1. Claim 8

[8.Pre] "A three-dimensional (3D) memory device, comprising:"

105. I offer no opinion on whether the preamble is or is not limiting. However, if the preamble is considered to be a limitation, my opinion is that Toyama discloses it. Indeed, the first sentence of Toyama's detailed description states that "the present disclosure is directed to three-dimensional non-volatile memory devices, such as vertical NAND strings and other three-dimensional devices, and methods of making the same." Ex. 1005, [0156].

[8.A] “an alternating conductor/dielectric layer stack;”

106. Toyama’s Second Embodiment discloses this limitation.

107. The “alternating stack (132, 146, 232, 246)” in Toyama is the claimed *alternating conductor/dielectric layer stack*. In what a POSITA would recognize as a clear typographical error, Figs. 47A, 48A and 49 label the alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. But, as Toyama itself explains, elements 142 and 242 are “sacrificial material layers” which were previously removed and replaced with “electrically conductive layers (146, 246).” Ex. 1005, [0337], [0340]. The same is shown in Toyama’s figures, which depict the sacrificial material layers (shaded in gray in Fig. 45A) as replaced by electrically conductive layers (cross-hatched as in Fig. 46A). A POSITA would have thus understood that elements 142 and 242 in Figs. 47A, 48A, and 49 should be labeled 146 and 246, respectively. With this understanding, Toyama Fig. 49 below illustrates the claimed *alternating conductor/dielectric layer stack*.

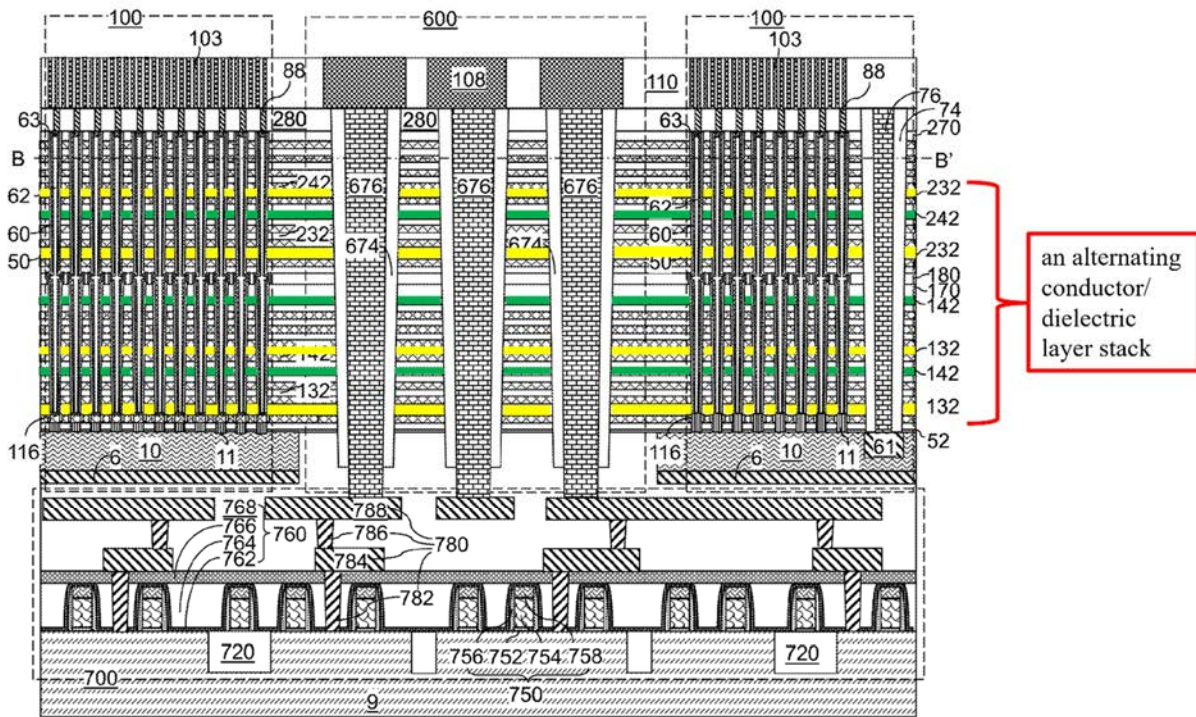


FIG. 49

Id., Fig. 49 (annotated), [0337].

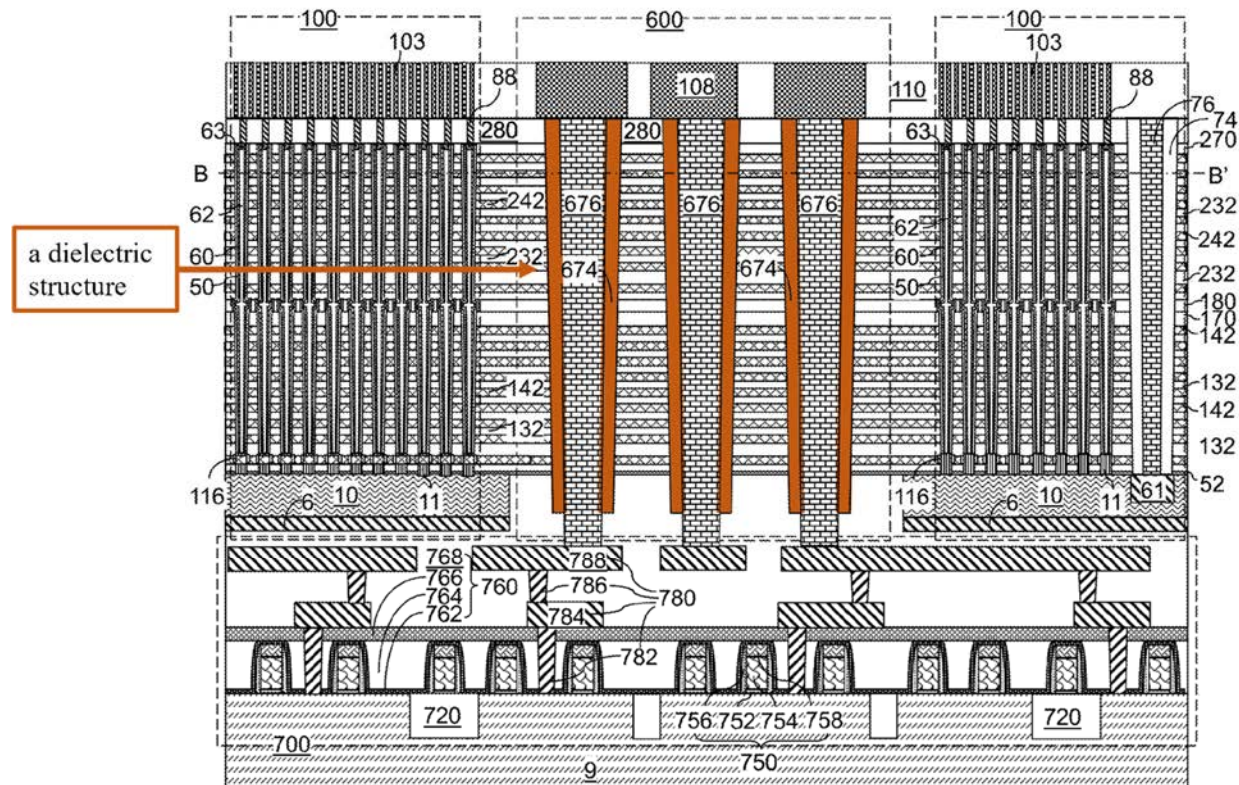
108. Toyama explains that its “alternating stack” comprises “electrically conductive layers (146, 246)” (representative layers of which are highlighted in green above), and “insulating layers (132, 232)” (representative layers of which are highlighted in yellow above). Ex. 1005, [0337].

[8.B] “a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;”

109. For ease of analysis, I separate this limitation into two sub-parts and address how Toyama’s Second Modification teaches each in turn.

[8.B.i] “a dielectric structure”

110. The “insulating liners 674” in Toyama’s Second Modification, shown below in Fig. 49, are the claimed *dielectric structure*. Ex. 1005, [0340].



Id., Fig. 49 (annotated), [0340].

111. The “insulating liners 674” are *dielectric*. Toyama forms “insulating liners 674” by depositing “a conformal insulating material layer” in “through-

memory-level openings 679.”² Ex. 1005, [0338]-[0340]. Toyama discloses that insulating liner 674 may be a “dielectric material.” *Id.*, [0233] (“[a]n insulating spacer 74 including a dielectric material”), [0381] (“insulating liner 674 having a same material composition and a same thickness as the insulating spacer 74”).

112. The Challenged Claim does not recite, or otherwise require, a “single-material” dielectric structure. This is confirmed by the ’806 patent which contemplates a “single-material” dielectric structure only “[i]n some embodiments.” Ex. 1001, 5:56-65. Regardless, Toyama contemplates that its “insulating liners 674” are made of a single material (e.g., silicon oxide). Toyama discloses that “insulating liner 674” may “hav[e] a same material composition ... as the insulating spacer 74.” Ex. 1005, [0381]. The “insulating spacer 74” in Toyama is described as including “an insulating material such as silicon oxide.” *Id.*, [0234].

113. Toyama’s “insulating liners 674” are, individually and collectively, a *structure*, which is not an art-specific term and is given its plain and ordinary meaning. See Ex. 1021, 5 (Merriam-Webster’s definition of “structure” as

² I note that Toyama [0338] refers to “through-memory-level openings 689,” but that appears to be a clear typographical error. All of the relevant figures (*e.g.*, Figs. 47A-B to 49) and the other textual description refer to the elements as “through-memory-level openings 679.”

“something (such as a building) that is constructed”). As explained above, they are constructed together, and all have the same function of insulating and electrically isolating the *through array contacts* (“through-memory-level via structures 676”) as they pass through the *alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246).” A POSITA would thus have understood that “insulating liners 674” are individually and collectively *a dielectric structure*.

114. To the extent Toyama does not expressly disclose this limitation, it would have been obvious to a POSITA. By its very terms, “insulating liner 674” is insulating, and a POSITA would have known silicon oxide to be a commonplace and suitable insulating material from which to make “insulating liner 674.” Ex. 1018 (U.S. Pat. No. 9,293,348), 2:61-65 (“dielectric structure” may comprise an “oxide” such as “silicon oxide”); Ex. 1019 (U.S. Pat. No. 8,598,643), 7:37-38 (“silicon oxide film 44 serving as an insulating film”); Ex. 1020 (U.S. Pat. No. 8,697,519), 7:30-40 (“the liner insulating layer may include a silicon oxide layer”); Ex. 1027 (U.S. Pat. No. 10,103,169), Figs. 11-12, 3:1-8 and 21:1-61 (discussing “formation of a conformal silicon oxide liner” in 3D-NAND memory devices”). And all of the “liners 674” have the same function of insulating and electrically isolating the *through array contacts* (“through-memory-level via structures 676”) as they pass through the *alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246).”

115. Thus, Toyama’s Second Modification discloses, or renders obvious, *a dielectric structure* (“insulating liners 674”).

[8.B.ii] “... extending vertically through the alternating conductor/dielectric layer stack”

116. As I discuss in the section above, Toyama’s “insulating liners 674” are individually and collectively the claimed *dielectric structure*. And, as I noted above with reference to claim element [8.A], Toyama’s “alternating stack (132, 146, 232, 246)” is *the alternating conductor/dielectric layer stack*. Accordingly, as shown in Fig. 49 below, Toyama discloses *a dielectric structure* (“insulating liners 674”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack 132, 146, 232, 246”).

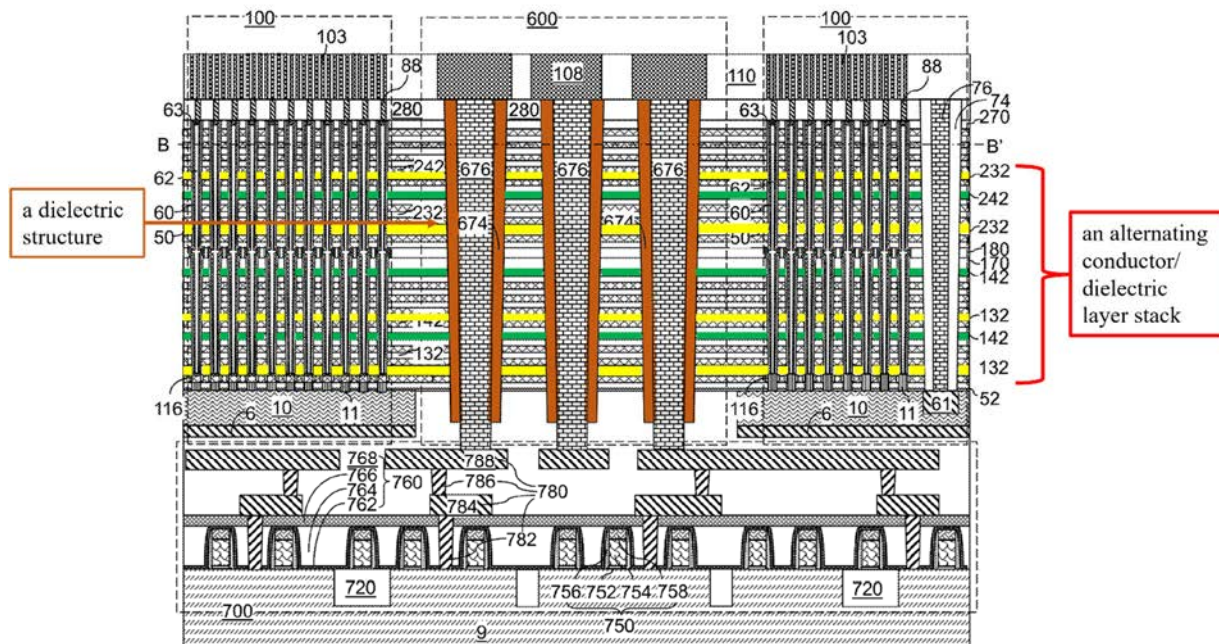


FIG. 49

Ex. 1005, Fig. 49 (annotated). As I noted previously, labels 142 and 242 are properly understood to refer to conductive material layers (146, 246).

[8.C] “first and second channel regions comprising first and second pluralities of channel structures, respectively;”

117. The “memory stack structures 55” in Toyama are each *a channel structure[]*, and portions of Toyama’s “memory array region 100” are each *a channel region* as shown below in Toyama Fig. 48B (which is a top view). The groupings of “memory stack structures 55” in the red boxes are each a *pluralit[y] of channel structures* since there are more than one channel structure 55 in each.

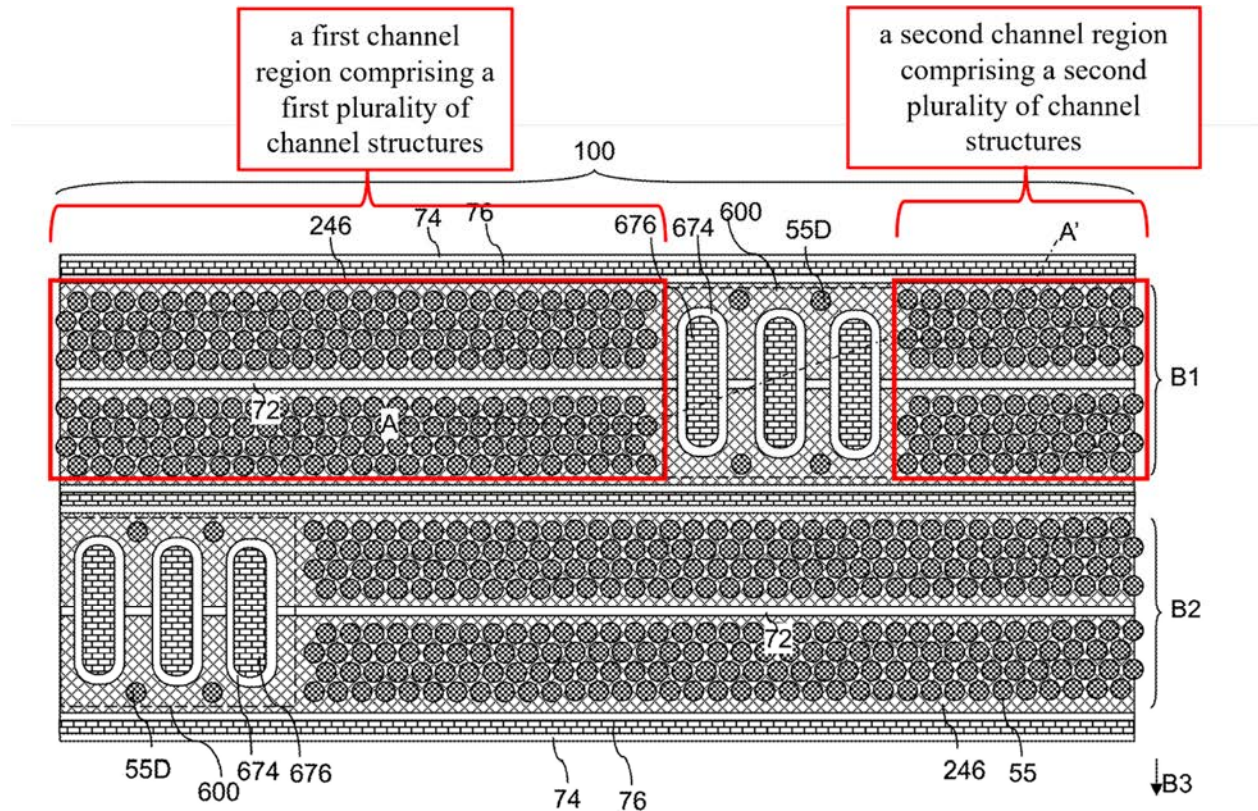


FIG. 48B

Ex. 1005, Fig. 48B (annotated), [0323], [0333].

118. Toyama also provide a cross-section view of the *first and second channel regions* (the left and right portions of “memory array region 100”). The left and right parts of the “memory array region 100” are *channel regions* because they comprise *channel structures* (“memory stack structures 55”).

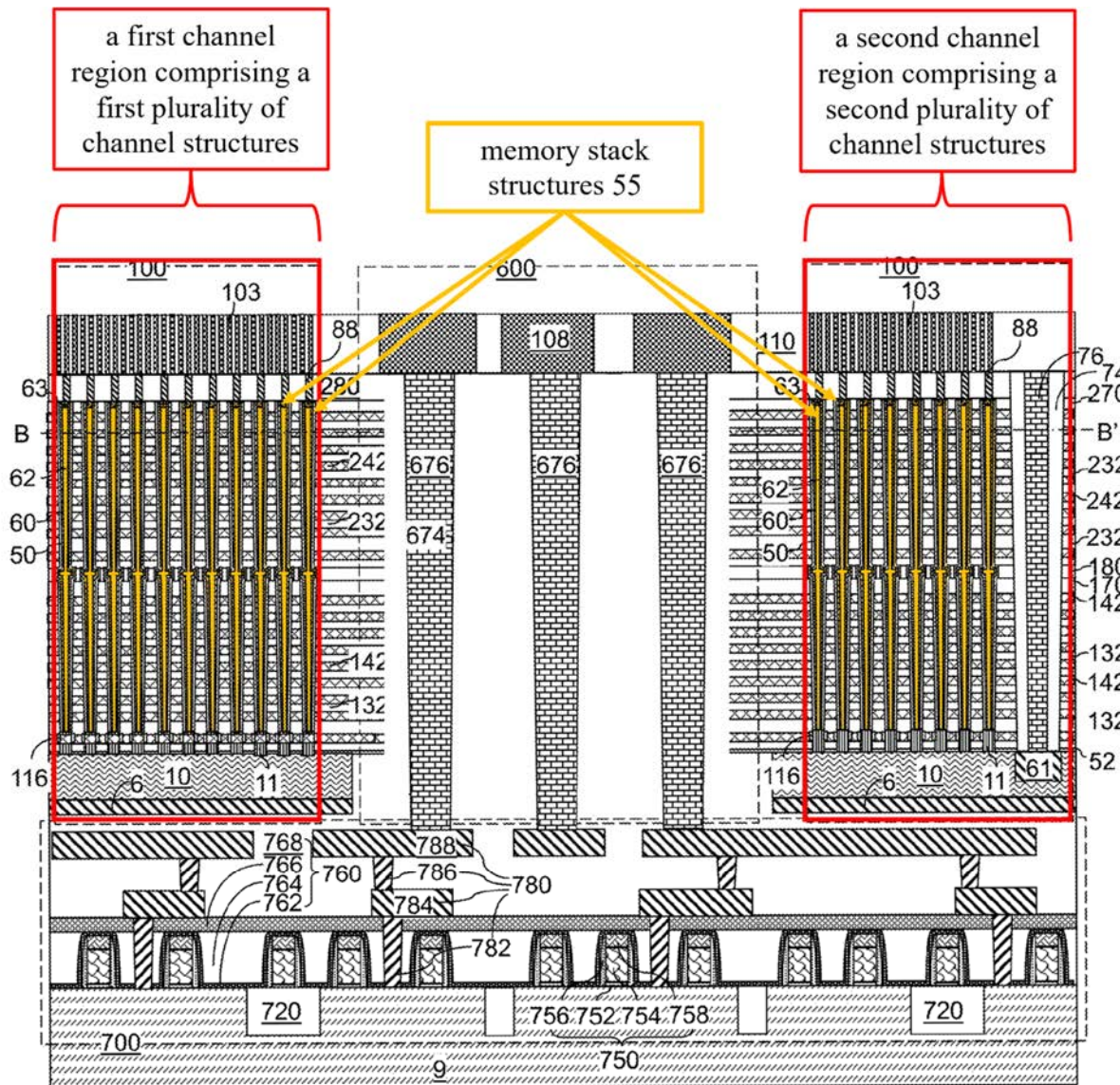


FIG. 49

Toyama, Fig. 49 (annotated). Even though memory stack structures 55 are not labelled in Fig. 49, I have highlighted them above and a POSITA would have readily recognized them.

119. Even though the claim element places no other functional or structural requirements on the claimed *channel structures*, I note that Toyama’s “memory

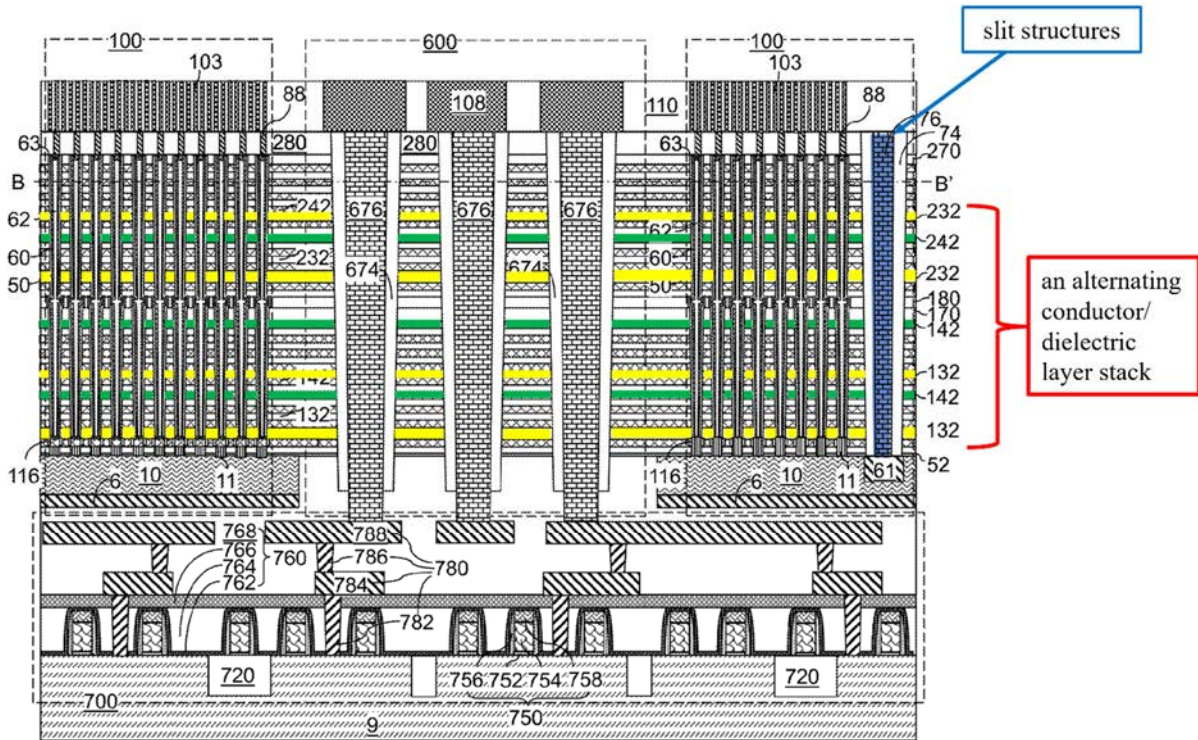
stack structures 55” perform the same function and are composed of the same components as the channel structures in the ’806 patent. With respect to function, both serves as memory elements. *Compare* Ex. 1001, 14:8-35 (“channel structure” includes a “memory film”) *with* Ex. 1005, [0388] (“The memory stack structures 55 can comprise memory elements of a vertical NAND device.”). And both are constructed from the same components. *Compare* Ex. 1001, 9:7-12 (“[c]hannel structure 216 is filled with semiconductor materials (e.g., as a semiconductor channel 218) and dielectric materials (e.g., as a memory film 220)”) *with* Ex. 1005, [0210] (“[e]ach of the memory stack structures 55 comprises a memory film 50 and a vertical semiconductor channel 60”).

120. In summary, Toyama discloses *first and second channel regions* (the left and right parts of “memory array region 100”) *comprising first and second pluralities of channel structures* (first and second pluralities of “memory stack structures 55”).

[8.D] “slit structures extending vertically through the alternating conductor/dielectric layer stack;”

121. As shown below in Fig. 49, Toyama discloses *slit structures* (“laterally-elongated contact via structures 76”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”). It is

important not to mistake the structures 676 (in the middle of the figure) for the “laterally-elongated contact via structures 76” (on the right hand side of the figure).



Ex. 1005, Fig. 49 (annotated), [0318]-[0320]. Toyama Fig. 48B also shows a top view of its *slit structures* (“laterally-elongated contact via structures 76”):

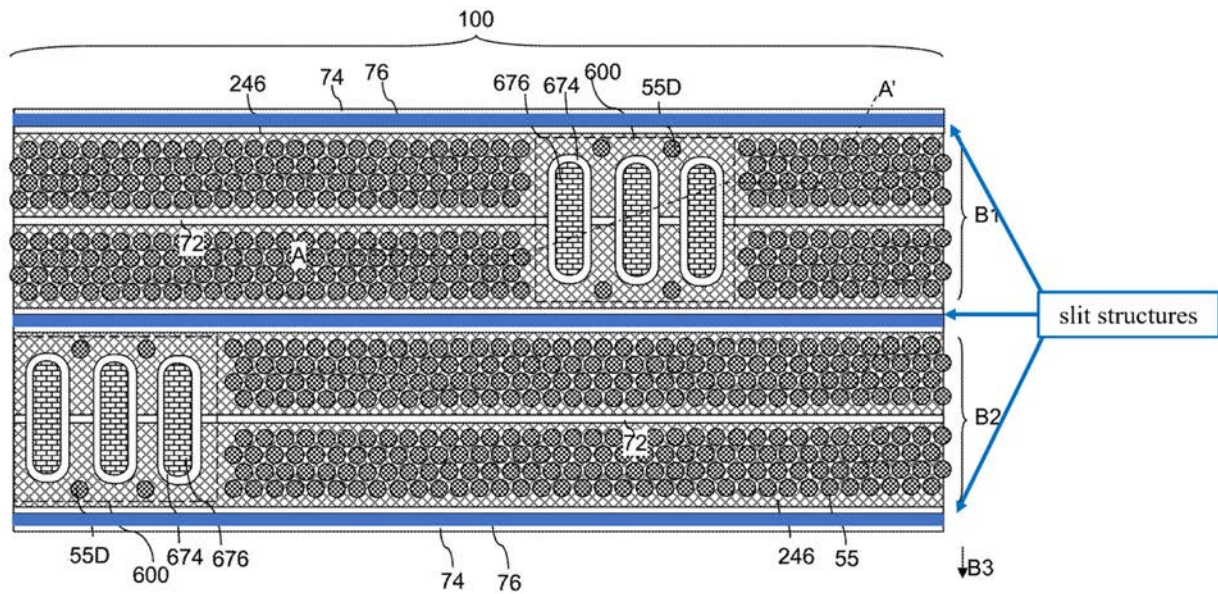


FIG. 48B

Id., Fig. 48B (annotated).

122. It is of no import that Toyama refers to the claimed *slit structures* as “laterally-elongated contact via structures 76.” Indeed, the plain meaning of “slit” is a laterally-elongated structure. See Ex. 1021, 4 (Merriam-Webster’s definition of “slit” as “a long narrow cut or opening”). As can be seen in Toyama Fig. 48B, the structure has an elongated slit shape. And, as shown in Toyama Fig. 49, above, Toyama’s “laterally-elongated contact via structure 76” *extend[] vertically in the alternating layer stack* (“alternating stack (132, 146, 232, 246)”). Accordingly, Toyama’s “laterally-elongated contact via structures 76” meets the plain language of the claims.

123. Even though the claim places no functional limitation on the “slit structure,” Toyama’s “laterally-elongated contact via structures 76” perform the same function as the ’806 patent’s “slit structures.” The ’806 specification explains that each “slit structure 226 acts as a source contact for NAND strings 204.” Ex. 1001, 9:67-10:5. Likewise, Toyama’s “laterally-elongated contact via structures 76” serves as “source connection[s].” Ex. 1005, [0241]. And the *slit structures* in Toyama and the ’806 patent both define memory “blocks” in their respective 3D memory arrays. *Compare* Ex. 1001, 9:57-59 (“[s]lit structures 226 ... extend along the y-axis to separate alternating conductor/dielectric stack 210 into multiple blocks.”) *with* Ex. 1005, [0237] (“laterally-elongated contact via structures 76 laterally extend along the first horizontal direction ... and laterally divide the at least one alternating stack ... into a plurality of laterally spaced-apart blocks.”). This reinforces my opinion that Toyama’s Second Modification meets the claim language.

[8.E] “a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;”

124. The “staircase region” highlighted in Toyama Fig. 17C below is *a staircase structure* that is *disposed in the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”). Moreover, *the staircase structure*

(“staircase region”) *comprises levels with each level having a conductor layer*
(“electrically conductive layers 146, 246”) *thereon*:

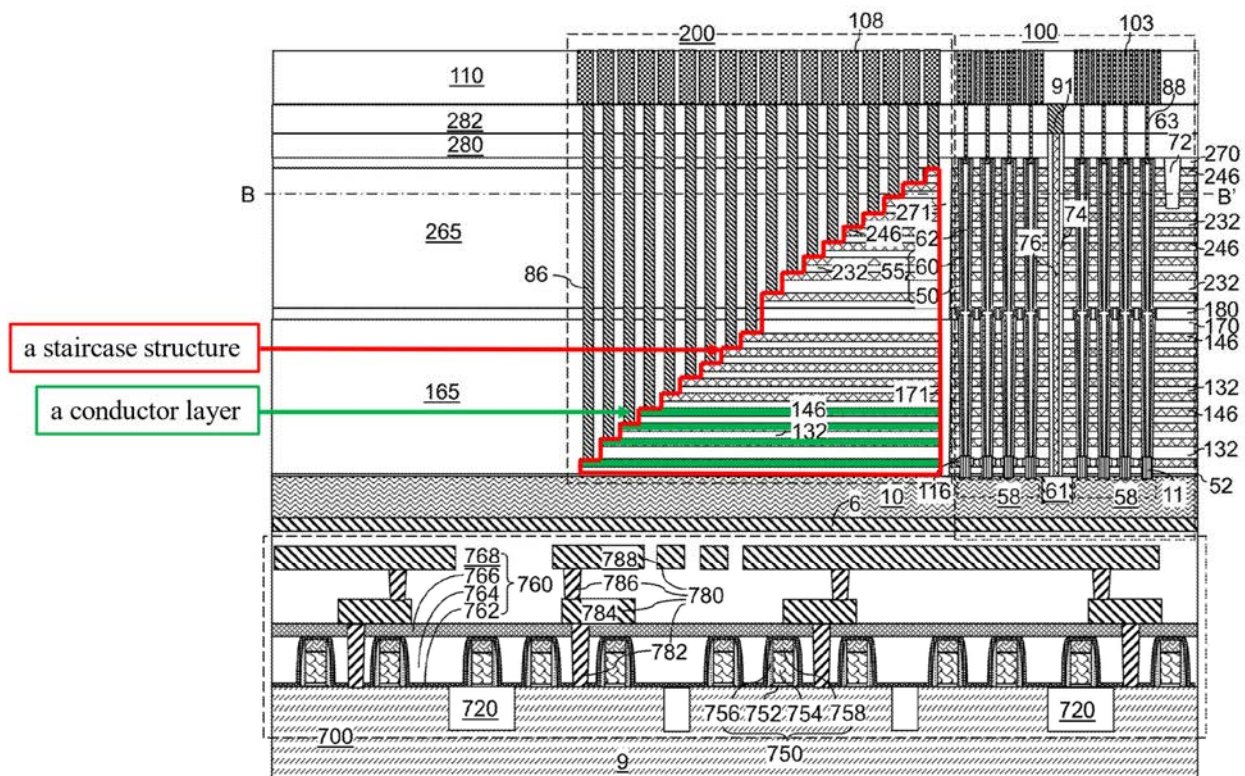


FIG. 17C

Ex. 1005, Fig. 17C (annotated). Toyama explains that “[t]he at least one alternating stack (132, 146, 232, 246) comprises staircase regions that include terraces in which each underlying electrically conductive layer (146, 246) extends farther along the first horizontal direction hd1 than any overlying electrically conductive layer (146, 246).” *Id.*, [0232].

125. While the discussion above is in the context of Toyama’s first exemplary structure, a POSITA would have understood that Toyama’s Second

Modification also teaches this limitation for substantially the same reasons. With respect to Toyama's fourth exemplary structure (to which the Second Modification pertains), Toyama notes that "word line contact via structures [86] can be formed as in the first through third embodiments." Ex. 1005, [0322]. Recall that the word line contacts are in Toyama's staircase region. *See id.*, Fig. 17C, [0243]. Thus, although not explicitly depicted in Figs. 44-49, a POSITA would therefore have understood that Toyama's fourth exemplary structure (and modifications thereof including the Second Modification) includes *a staircase structure* ("staircase regions").

126. At a minimum, it would have been obvious to a POSITA to use a staircase structure ("staircase regions") in Toyama's Second Modification. For the memory device to be functional, a POSITA would have understood that there needed to be some way to transmit signals to the "electrically conductive layers (146, 246)," because these layers serve as the word lines for accessing (*e.g.*, reading, writing, and erasing) the memory elements in the channel structures. Ex. 1005, [0323]. And it would have been obvious to a POSITA to use the well-known *staircase structure* ("staircase regions") architecture to provide access to Toyama's word lines. Not only is this true in view of the knowledge of a POSITA, but also in view of the teachings in Toyama itself regarding its first, second, and third exemplary structures, from which the Second Modification derives. *See, e.g., id.*, Fig. 17C.

[8.F] “local contacts disposed on the first and second channel structures and the slit structures;”

127. Toyama’s Second Modification discloses this element. For ease of analysis, I divide this element into two sub-parts and address each one. Before turning to my analysis, I first note that the ’806 patent teaches that “[i]n some embodiments, 3D memory device 200 includes a plurality of ‘local contacts.’” Ex. 1001, 11:20-21. “The contacts are referred to herein as ‘local contacts’ because they are in direct contact with the memory array structures, and further because they are formed within dielectric layer 230.” *Id.*, 11:24-28.

a. “local contacts disposed on the first and second channel structures”

128. Toyama’s “drain contact via structures 88” in the Second Modification are the *local contacts* that are *disposed on* (in contact with or extending above) *the first and second channel structures* (“memory stack structures 55”). Ex. 1005, Fig. 49, [0342] (“drain contact via structures 88 ... can be formed as in the first through third embodiments”).

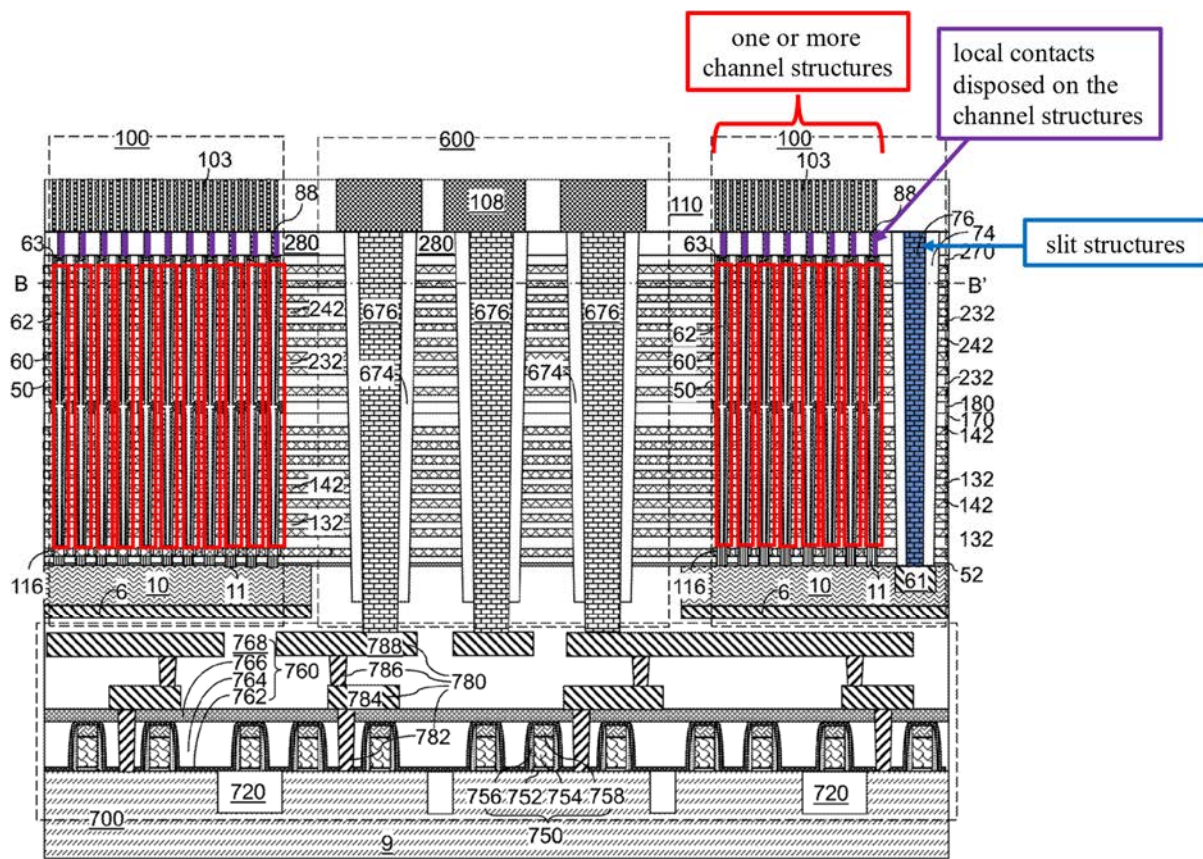


FIG. 49

Id., Fig. 49 (annotated),³ [0251] (“The bit lines 103 are formed over the memory-level assembly, and are electrically coupled to nodes (e.g., drain regions 63) of the memory stack structures 55 by the drain contact via structures 88.”).

³ Here, as in my declaration filed in IPR2024-00791, I explain that Toyama’s “memory stack structures 55” are the claimed *channel structures*. I note, however, that the red boxes drawn around the *channel structures* in my earlier declaration were drawn slightly larger than they are here, such that in the prior declaration each

b. “local contacts disposed on ... the slit structures”

129. Toyama Fig. 49 (showing the cross-section of the Second Modification) does not expressly illustrate that “source connection via structures 91” are used to connect to “laterally-elongated contact via structures 76,” but a POSITA would have understood the Second Modification to include *local contacts disposed on the slit structures* (“source connection via structures 91”). The fact that Fig. 49 does not show any connection to Toyama’s “laterally-elongated contact via structures 76” appears to merely be an artifact of where the cross-section was taken. Indeed, in describing the Second Modification, Toyama notes that “the metal interconnect structures can include ... source connection line structures (not shown).” Ex. 1005, [0342]. Because Toyama’s *slit structures* are “*laterally-elongated* contact via structures 76,” they extend some length in the horizontal direction. As such, there

box encompassed not just a “memory stack structure 55,” but arguably also other structures (e.g., “pedestal channel portion 11,” the *epitaxial layer*, and “drain region 63,” the *etch stop plug*). This overinclusive annotation was of no moment in the prior case because the challenged claims in that case did not recite *an epitaxial layer* or *an etch stop plug*. The boundaries of the box drawn here make clear that the *channel structures* include “memory stack structures 55” but **not** “pedestal channel portions 11” or “drain regions 63.”

is no need to have a single, continuous local contact that spans the entire length of the slit. Rather, a POSITA would have understood that periodic/intermittent local contacts would suffice. This explains why a particular cross-section (such as Fig. 49) does not illustrate the local contacts. But taking a cross-section at a different location would reveal such contacts.

130. As Toyama's expressly states in connection with its first exemplary structure, "source connection line structures 101 ... contact the source connection via structures 91 to provide electrically conductive paths for biasing the source region 61 through the laterally-elongated contact via structures 76." Ex. 1005, [0250]. A POSITA would thus have understood that the Second Modification, which expressly includes "source connection line structures," "source region 61," and "laterally elongated contact via structure 76," also includes "source connection via structures." Thus, Toyama discloses *local contacts* ("source connection via structures 91") *disposed on the slit structures* ("laterally-elongated contact via structures 76") in the context of the Second Modification.

131. At a minimum, it would have been obvious to a POSITA to use *local contacts* ("source connection via structures 91") *disposed on the slit structures* ("laterally elongated contact via structure 76"). To begin, a POSITA would have understood that "laterally-elongated contact via structures 76" function as the source lines for "source regions 61" in Toyama's Second Modification. Ex. 1005, [0382].

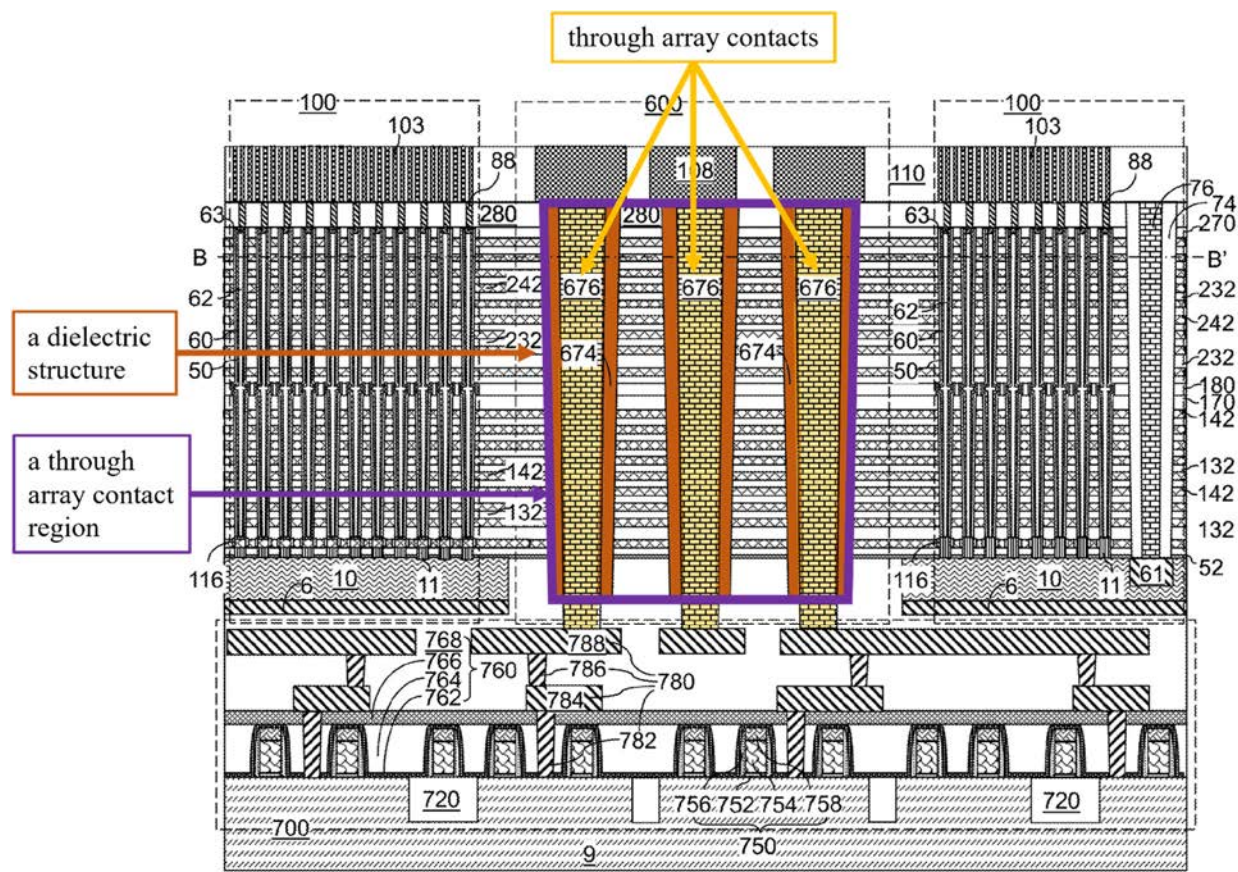
And a POSITA would have further known that “via structures 76” require a higher-level source connection to serve their purpose. Given Toyama’s express disclosure in other embodiments of “source connection via structures 91” for the same purpose, a POSITA would have been motivated to implement “source connection via structures 91” in the Second Modification (which is largely derivative of Toyama’s first, second, and third exemplary structures). Similarly, given Toyama’s express disclosure in other embodiments of using “source connection via structures 91” for the same purpose, a POSITA would have had a reasonable expectation of success in using the same (or substantially identical) manufacturing steps (which as discussed in Section VI were very well-known) to create local contacts on Toyama’s slit structures in its Second Embodiment. This is even more the case because Toyama’s Second Embodiment is largely derivative of Toyama’s first, second, and third embodiments, which expressly disclose local contacts on slit structures.

[8.G] “[i] a through array contact (TAC) region [iii] formed between the first and second channel regions, [iii] wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and”

132. Toyama’s Second Modification discloses this element. For ease of analysis, I divide this element into three sub-parts and address each one. I begin my analysis with the last sub-part, as it is helpful to understand what constitutes a *through array contact (TAC)* in Toyama before discussing the *through array contact (TAC) region* limitation.

[8.G.iii] “wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and”

133. The “through-memory-level via structures 676” in Toyama’s Second Modification are the claimed *plurality of through array contacts*. And, as can be seen in Fig. 49 below, *they extend[]vertically through the dielectric* (shown in red below). In Fig. 49 below, three “through-memory-level via structures 676” are shown, which is a *plurality*.



Ex. 1005, Fig. 49 (annotated); [0341]-[0342].

134. As discussed for claim element [8.B], “insulating liners 674” are individually and collectively *the dielectric structure*⁴ in Toyama’s Second Modification. Like water that travels *through* a hose or a pipe that extends *through* a wall, Toyama’s “through-memory-level via structures 676” extend *through* “insulating liners 674.” Thus, Toyama discloses *a plurality of through array contacts (TACs)* (“through-memory-level via structures 676”) *extending vertically through the dielectric structure* (“insulating liners 674”). Ex. 1005, [0340]-[0342]. Sub-element [8.G.iii] also refers to *the TAC region*, but I address the *through array contact (TAC) region* language in connection with sub-element [8.G.i], which I turn to now.

[8.G.i] “a through array contact (TAC) region”

135. The ’806 patent discloses that “[i]n some embodiments, dielectric structure 232 defines the boundaries, the shape, and the size of TAC region 120.” Ex. 1001, 10:26-28. Applying the same approach to Toyama, the *through array*

⁴ As previously explained (see discussion for element [8.B.i]), the claim term *a dielectric structure* is properly understood to include one **or more** dielectric structures. Thus, even if dielectric liners 674 are not considered to be a “structure” (which they are), the claim nonetheless encompasses embodiments in which each *through array contact* extends vertically through a different *dielectric structure*.

contact (TAC) region is the portion of “through-memory-level via region 600” highlighted below in Fig. 49 and is defined by the boundaries of Toyama’s *dielectric structure* (“insulating liners 674”).

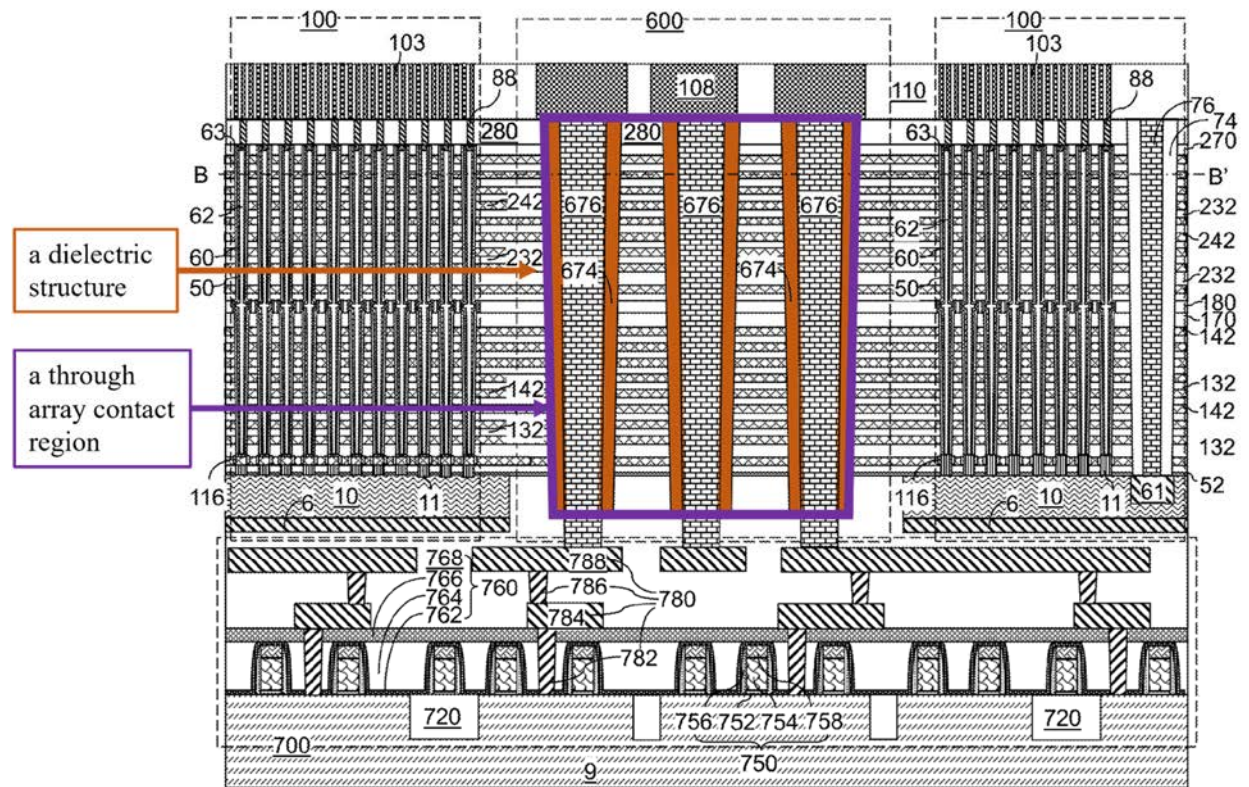


FIG. 49

Ex. 1005, Fig. 49 (annotated), [0334]. Toyama also illustrates “through-memory-level region 600” in a top view in Fig. 48B, the highlighted portion of which constitutes the claimed *through array contact (TAC) region*:

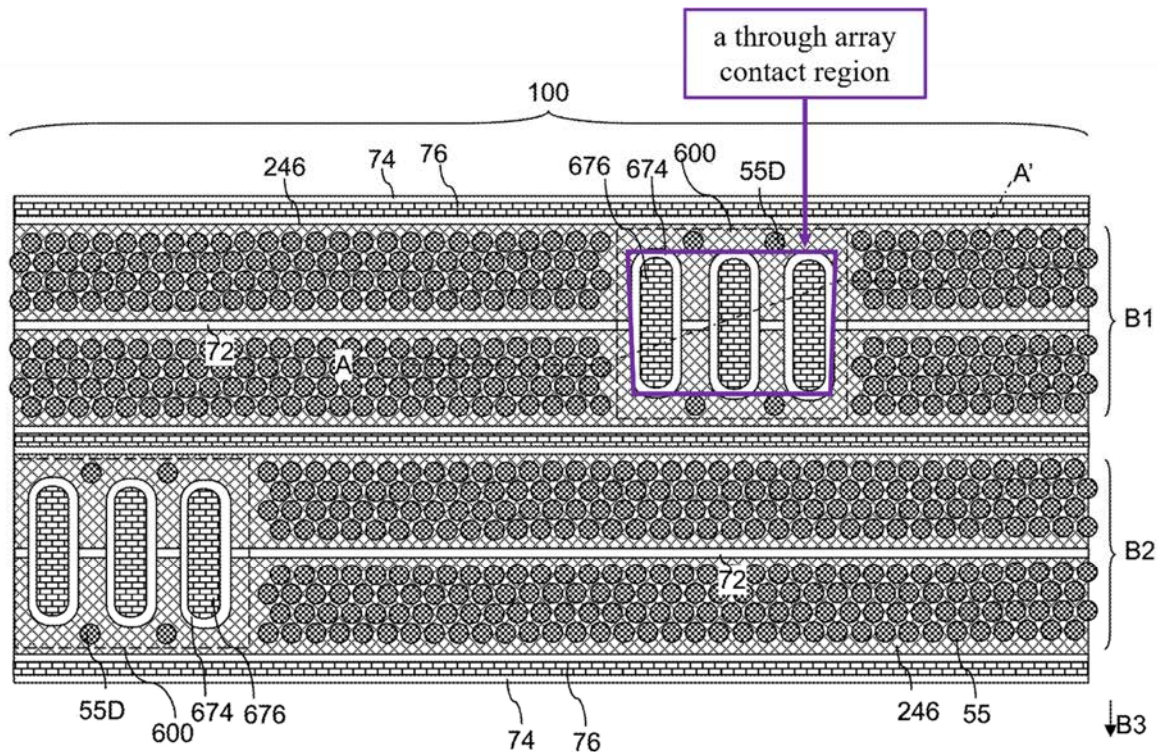


FIG. 48B

Id., Fig. 48B (annotated). As required by sub-element [8.G.iii], Toyama’s *through array contact (TAC) region* (part of “through-memory-level region 600”) *comprises a plurality of through array contacts (TACs)* (“through-memory-level via structures 676” are all within the same highlighted portion of “through-memory-level region 600”).

[8.G.ii] “... formed between the first and second channel regions”

136. I discussed how Toyama discloses *a through array contact (TAC) region* (part of “through-memory-level via region 600”) above in connection with sub-element [8.G.i]. And, I discussed Toyama’s *first and second channel regions* (first and second parts of “memory array region 100”) in connection with element

region is formed between the first and second channel regions.

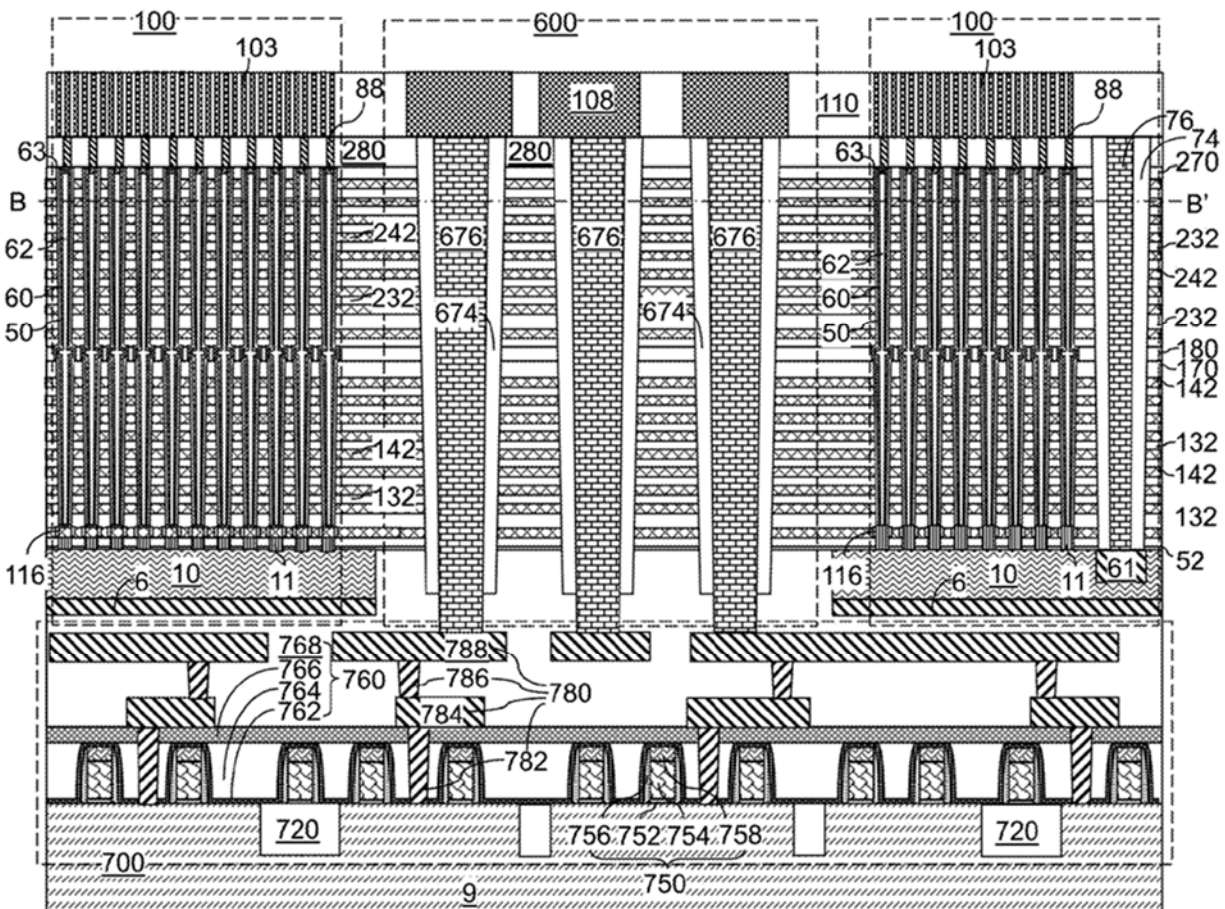


FIG. 49

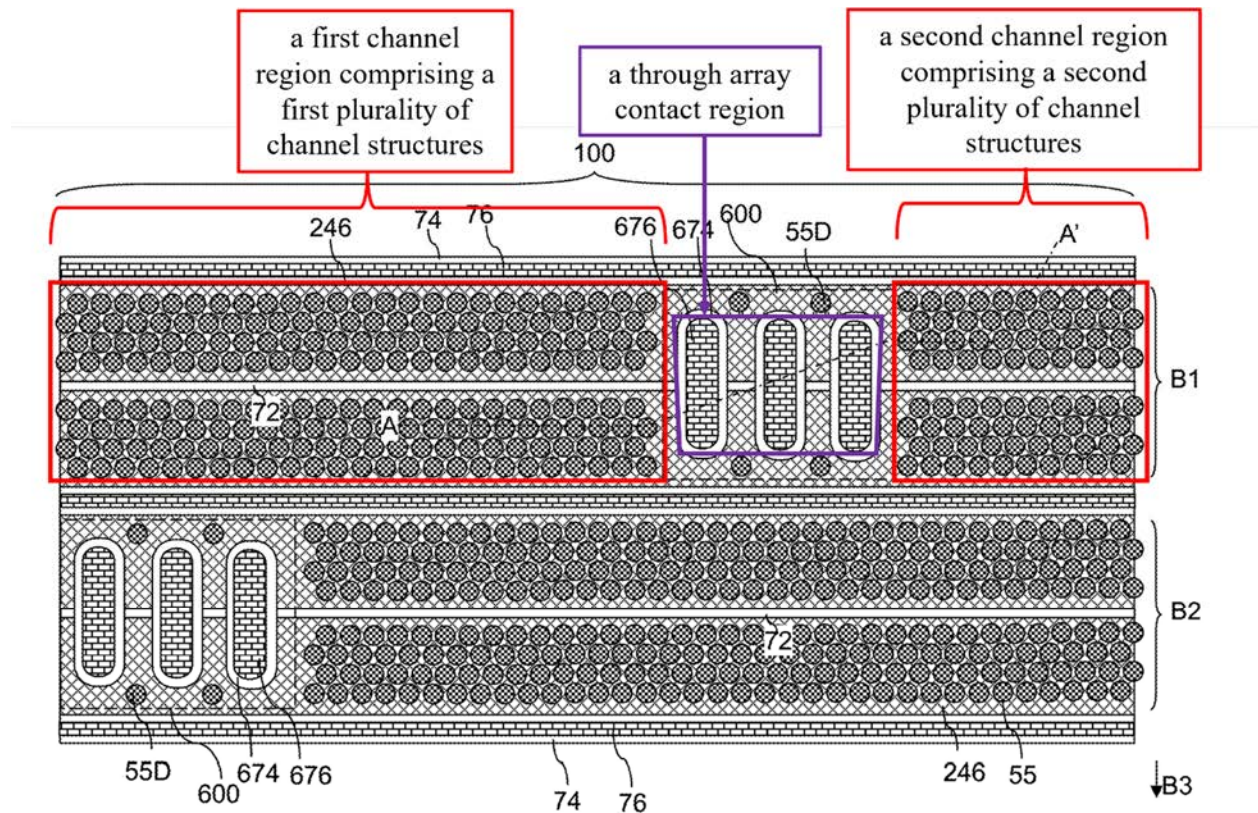
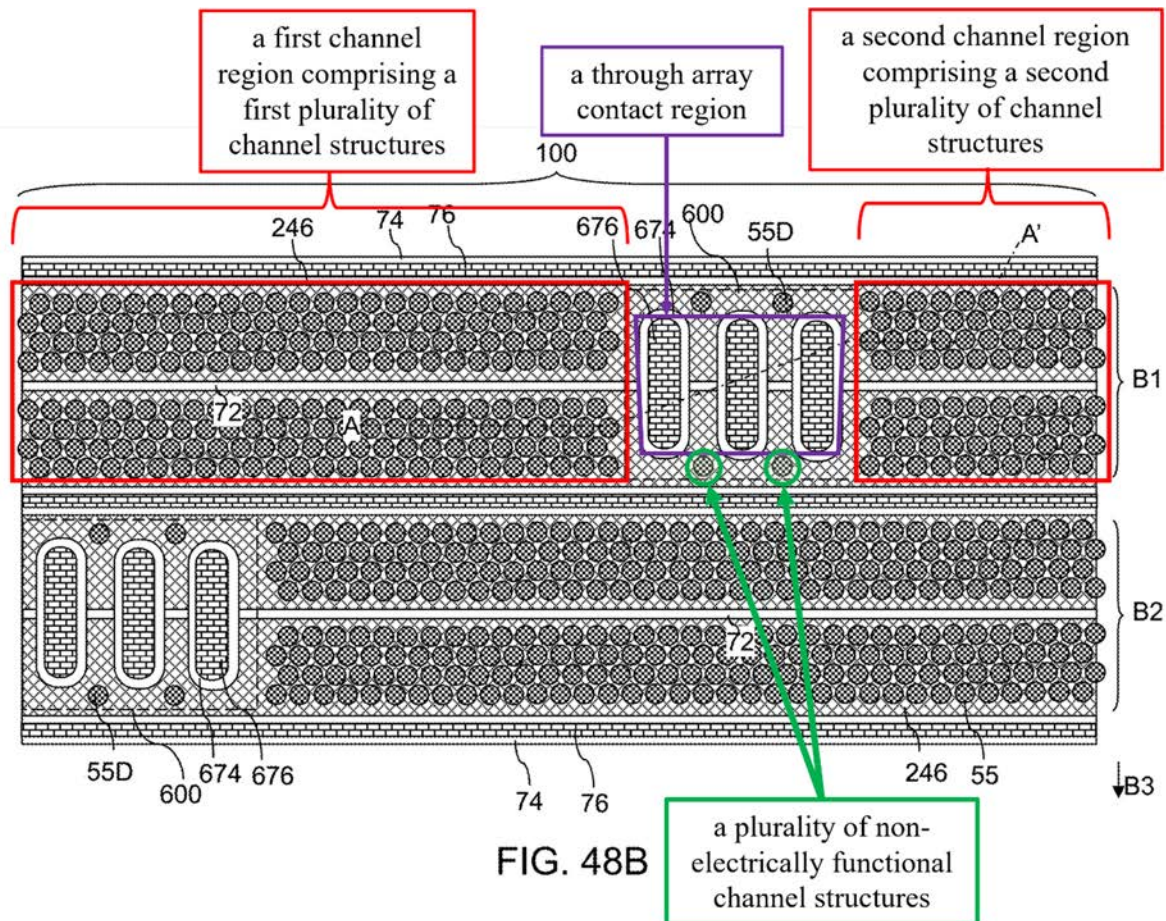


FIG. 48B

Ex. 1005, Figs. 49, 48B (annotated). Indeed, Toyama itself states that the “through-memory-level via region ... is located ... between two groups of memory stack structures 55 located in [a] block.” *Id.*, [0378]. Thus, Toyama teaches that *the through array contact (TAC) region* (part of “through-memory-level via region 600”) is *formed between the first and second channel regions* (first and second parts of “memory array region 100”).

[8.H] “a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.”

137. Toyama’s “dummy memory stack structures 55D” are the *plurality of non-electrically functional channel structures*. As the name “dummy” indicates, those memory stack structures do not perform an electrical function. In terms of location, they *surround[] the TAC region* (part of “through-memory-level via region 600”) and are *between the first and second channel regions* (first and second parts of “memory array region 100”). The location of Toyama’s “dummy memory stack structures 55D” relative to the first and second parts of “memory array region 100” and “through-memory-level via region 600” is shown in Fig. 48B below.



Ex. 1005, Fig. 48B (annotated). I note that the plain meaning of the term “surrounding” does not require *completely* surrounding. This is confirmed by everyday usage of the term and dictionaries. For instance, “[a]n isthmus is a thin strip of land surrounded by water on two sides, which connects two larger landmasses.” Ex. 1022 (<https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides>.). The same applies in the context of 3D NAND.

138. Moreover, the '806 patent itself contemplates that a first element bordered by a second element on two sides is “surrounded by” the second element.

Ex. 1001, 10:29-31 (“as shown in the plan-views of FIGS. 1A-1C, dielectric structure 232 can be **surrounded by** conductor / dielectric stack 210.”) (emphasis added). *See also id.*, 6:47-54 (with reference to Fig. 1B, dummy channel structures are formed in a NAND string regions 110, which are above and below TAC region 120); *id.*, 7:1-10 (with reference to Fig. 1C, dummy channel structures are formed in staircase regions 140, which are above and below TAC region 120). I noted that Fig. 2 uses the label 232 for the dielectric structure, but the analogous structure in Figs. 1A-1C is labelled 124. Similarly, in Figs. 1A-1C, the alternating conductor / dielectric stack that surrounds the dielectric structure is in region(s) 110.

139. Even if the claim required *non-electrically functional channel structures* on four sides of *the TAC region* (which it does not), a POSITA would have understood Toyama to disclose as much. In particular, Toyama discloses that “[d]ummy memory stack structures 55D can be provided at the periphery of the through-memory-level via regions 600.” Ex. 1005, [0333]. A POSITA would have understood the “periphery of the through-memory-level via regions 600” to include *all* sides (when viewed from the top, the “periphery” has four sides that encircle the TAC region).

140. Even if Toyama did not disclose “dummy memory stack structures 55D” bordering four sides of the *TAC region* (it does), a POSITA would nevertheless have found doing so to be obvious. Toyama Fig. 48B expressly depicts *non-*

electrically functional channel structures (“dummy memory stack structures 55D”) on two sides of *the TAC region* (part of “through-memory-level via region 600”). A POSITA would have been motivated to provide “dummy memory stack structures 55D” on all sides of the “through-memory-level via region” for additional structural support, especially where functional “memory stack structures are not formed at a sufficiently high density.” Ex. 1005, [0182]. Placing dummy stack structures on all sides of the TAC region is highly predictable and has a reasonable expectation of success because no additional processing steps are required and Toyama already discloses placing dummy stack structures in similar locations for the same purpose.

2. Claim 10

[10.Pre] “The 3D memory device of claim 8, further comprising:” [10.A] “a substrate”

141. Toyama’s Second Modification has a *substrate*. As a preliminary point, the ’806 patent explains that a “substrate” is “a material onto which subsequent material layers are added, or otherwise ‘disposed.’” Ex. 1001, 4:47-49. The ’806 patent further states that “[a] substrate can be a layer, can include one or more layers therein, and/or can have one or more layer thereupon, thereabove, and/or therebelow.” *Id.*, 5:10-12. This is reflected in certain embodiments in the ’806 patent’s specification in which “the array device and a peripheral device are formed on different substrates.” *Id.*, 5:49-51.

142. Toyama's substrate is "planar semiconductor material layer 10," which is shown below:

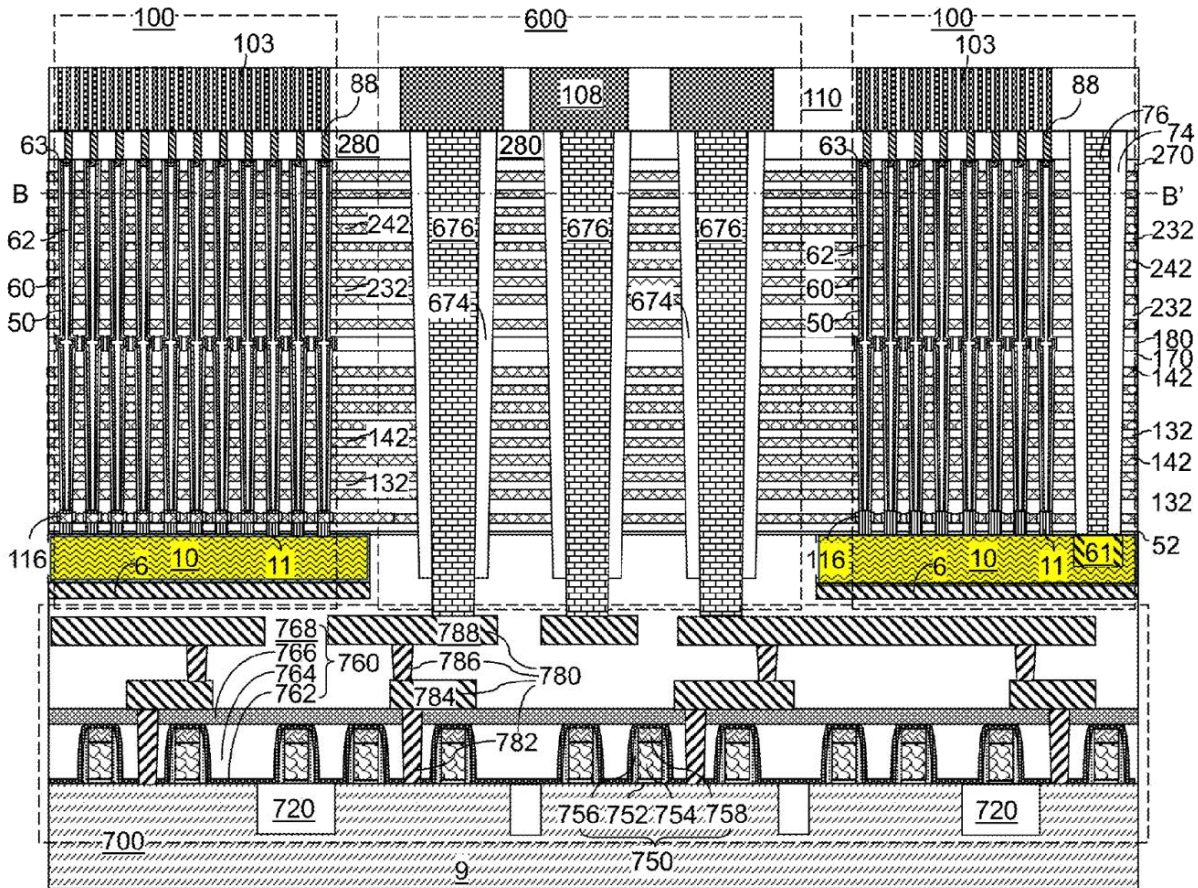


FIG. 49

Ex. 1005, Fig. 49 (annotated).

143. Toyama Figs. 2 through 17 depict how various layers are disposed on top of "planar semiconductor material layer 10." As one example, Toyama notes that "[a]n alternating plurality of the first insulating layers 132 and first sacrificial material layers 142 [are] formed over the planar semiconductor material layer 10."

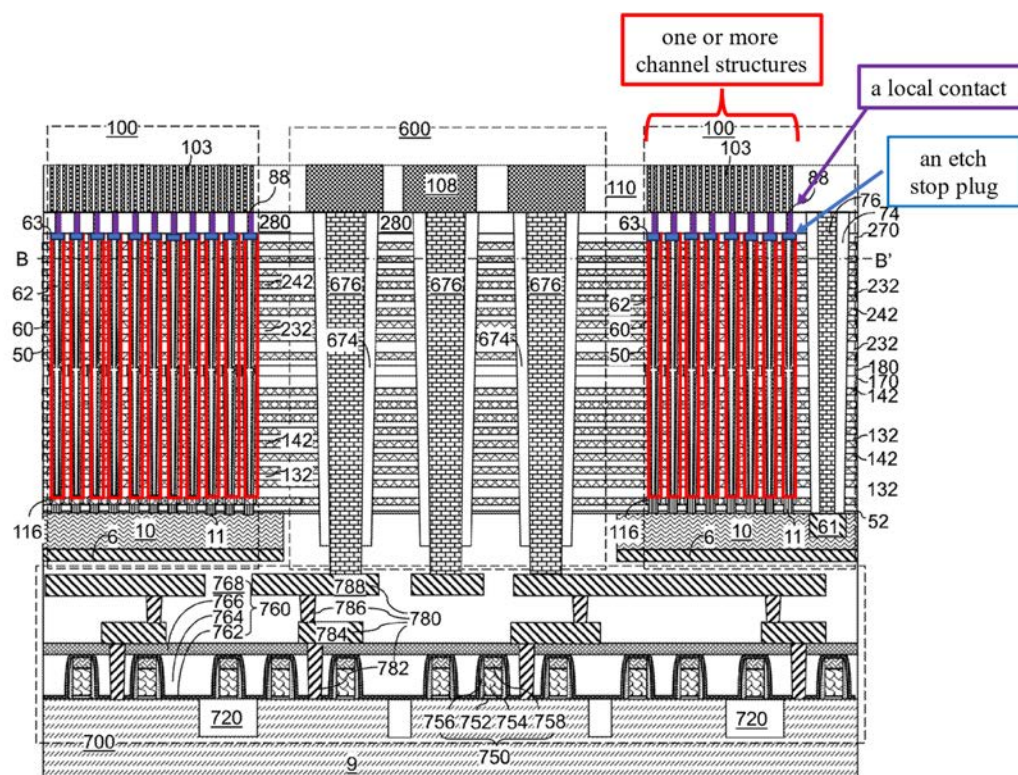
Ex. 1005, [0173]. As another example, Toyama explains that "at least one retro-

stepped dielectric material portion (165, 265) can be formed over the staircase regions on the at least one alternating stack (132, 142, 232, 242).” *Id.*, [0196].

Because the “planar semiconductor material layer 10” in Toyama is a semiconductor material onto which other materials and layers are added, it is *a substrate*.

[10.B] “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and”

144. As shown below in Fig. 49, Toyama discloses or renders obvious *an etch stop plug* (“drain region 63”) *interposed between each local contact of the local contacts* (“drain contact via structures 88”) *and each channel structure of the first and second channel structures* (“memory stack structures 55”):



Ex. 1005, Fig. 49 (annotated).

145. Toyama does not expressly describe “drain regions 63” as “etch stop plugs.” Even so, a POSITA would have understood that drain regions 63 are plugs that serve the purpose of stopping an etch and are therefore *etch stop plugs*.

146. To start, the meaning of the term *plug* in the field of flash memory is consistent with its ordinary meaning, which Merriam-Webster’s dictionary defines as “a piece used to fill a hole.” Ex. 1021, 3. In describing “drain regions 63,” Toyama explains that “[a] doped semiconductor material ... can be deposited over the dielectric cores 62 and within *the cavities in the memory openings* to form drain regions 63. The doped semiconductor material can be, for example, doped polysilicon. Excess portions of the deposited semiconductor material can be removed from above the top of the second insulating tier cap layer 270 ... to form the drain regions 63.” Ex. 1005, [0209]. Toyama’s “drain regions 63” are thus plugs because they fill the “cavities in the memory openings.” *Id.*

147. For the reasons I explain below, a POSITA would have appreciated that Toyama’s “drain regions 63” are etch stops because they have an *etch stop* function.

148. As Figure 49 shows below, Toyama forms *local contacts* (“drain contact via structures 88”) on the (“memory stack structures 55”) by etching through dielectric layer 280, and then filling the etched opening with a conductor:

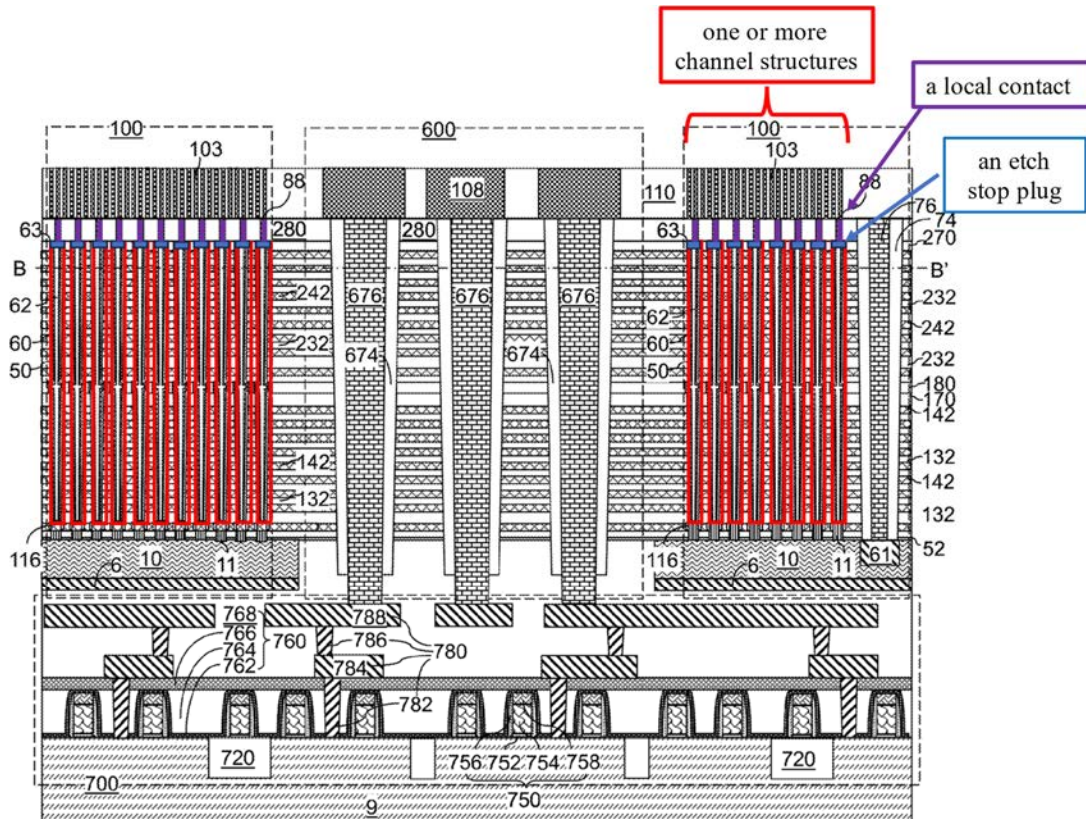


FIG. 49

Ex. 1005, Figure 49 (annotated). Toyama explains that “drain contact via structures 88 ... can be formed as in the first through third embodiments.” *Id.*, [0342]. Toyama explains in the context of its first exemplary structure that “[d]rain contact via structures 88 contacting the drain regions 63 can extend through the contact level dielectric layers,” here “first contact level dielectric layer 280.” *Id.*, [0241], [0342]. Toyama further explains that “drain contact via structures 88” “may be formed employing a respective set of patterning processes and fill processes.” *Id.*, [0241]-[0242].

149. As explained in the background section, above, the process of “patterning” generally involves forming a photoresist layer to protect certain material from etching, etching the exposed material, and then removing the photoresist.

150. A POSITA would thus have understood from Toyama’s disclosure that part of the “patterning” process includes a step of etching an opening in dielectric layer 280. Ex. 1005, [0241]-[0242]. And a POSITA would have understood from Toyama’s disclosure (or at least would have found it obvious) that the dielectric layer 280 would be formed of a dielectric material such as silicon oxide.⁵ Whether

⁵ Toyama does not expressly state that “dielectric layer 280” is made of silicon oxide, but a POSITA would have understood Toyama to contemplate doing so. At the very least, forming layer 280 of silicon oxide would have been obvious to a POSITA. Toyama expressly notes that “dielectric layer 180” could be made of “a dielectric material such as silicon oxide.” Ex. 1005, [0183]. Toyama similarly states that “second contact level dielectric layer 282 includes a dielectric material such as silicon oxide.” *Id.*, [0238]. A POSITA would have understood from Toyama’s disclosure that “dielectric layer 280” would similarly be made of silicon oxide, which was a well-known dielectric material with recognized advantages such as

or not dielectric layer 280 is formed of silicon oxide, however, Toyama contemplates (and a POSITA would certainly have found it obvious, given Toyama's express disclosure of patterning) that a dielectric-selective etchant would be used to form the opening that is ultimately filled by "drain contact via structures 88." As the textbooks and other materials I cite in the background section indicate, such selective etches were well-known and routine to implement.

151. With that context (which a POSITA would have known) in mind, the reason that the "drain regions 63" serve as *an etch stop* is evident. Namely, without "drain regions 63," the etch to form "drain contact via structures 88" may risk damaging elements of "memory stack structures 55." That is because "memory stack structures 55" may include dielectric elements (e.g., "blocking dielectric layer 51") that are formed of the same materials (e.g., silicon oxide) as layer 280. Ex. 1005, [0204]. Thus, if the etchant that is used to etch through the dielectric layer 280 were to contact the memory stack structures, the etchant may damage the dielectric elements in the memory stack structures.

being formed easily and using well-practice to techniques. And a POSITA would have found it desirable to form "dielectric layer 280" out of silicon oxide, which was a well-known and desirable dielectric material.

152. “Drain regions 63,” which are between the opening that is filled to form “drain contact via structures 88” and the “memory stack structures 55,” thus protect “memory stack structures 55” from damage. “Drain regions 63” function as an etch stop because they are made of a material like doped polysilicon, which a POSITA would have understood would **not** react significantly with the etchant used to selectively etch the dielectric layer 280. Carbon tetrafluoride (with hydrogen) is one such etchant that etches silicon oxide but does not appreciably etch polysilicon. Ex. 1029 (Chang, ULSI Technology), 363-364. Even if the etchant were to remove a portion of “drain regions 63,” the thickness of “regions 63” acts as a buffer, so that the etchant might partially etch and stop before etching through to the memory elements. Thus, “drain regions 63” serve to protect the dielectric materials in the memory stack from the etching process used to form “drain contact via structures 88.” In other words, because “drain regions 63” effectively stop the etch that ultimately forms the holes for “drain contact via structures 88,” each of “drain regions 63” is **an etch stop plug** that beneficially protects the channel structure.

[10.C] “an epitaxial layer disposed between the substrate and the first or second channel structures.”

153. As I explained above in limitations [8.C] and [10.A], respectively, Toyama discloses **channel structures** (“memory stack structures 55”) and **a substrate** (“planar semiconductor material layer 10”).

154. Toyama further discloses or renders obvious *an epitaxial layer* (“pedestal channel portions 11”) *disposed between the substrate* (“planar semiconductor material layer 10”) *and the first or second channel structures* (“memory stack structures 55”), as shown in Figure 49 below:

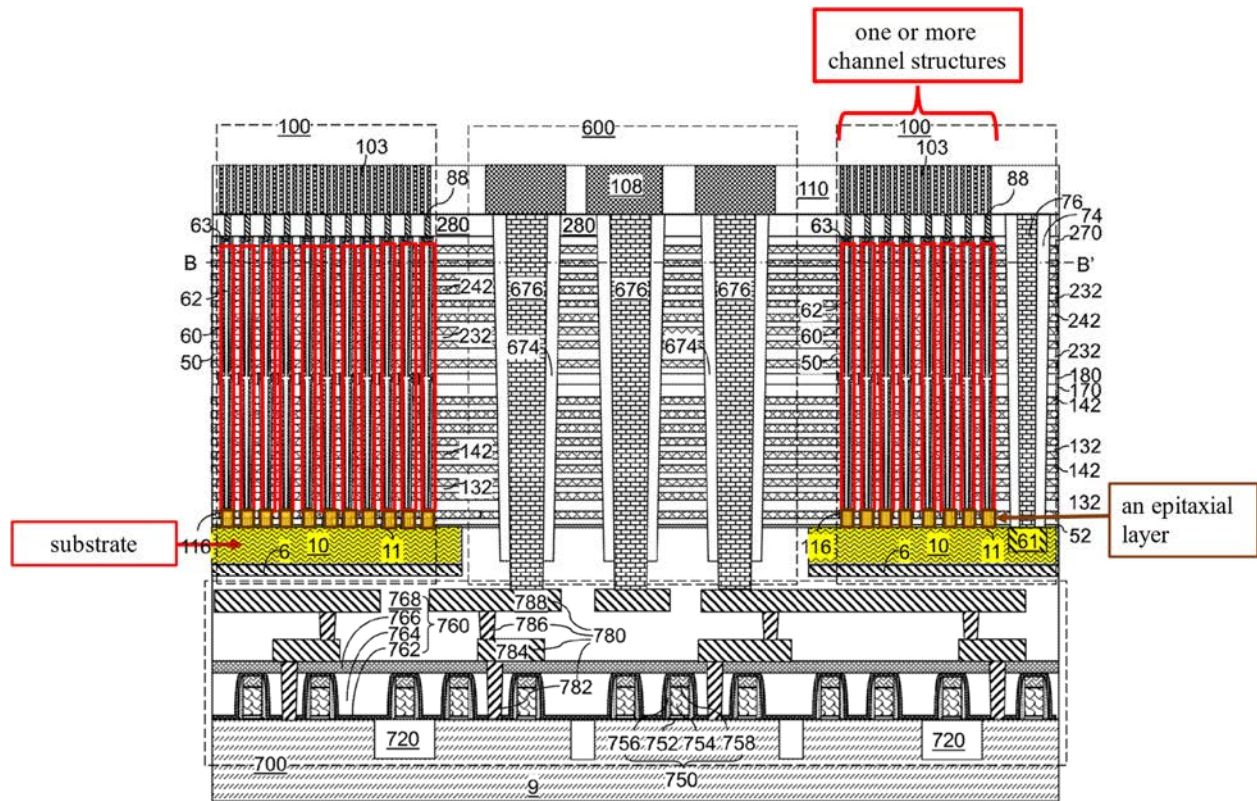


FIG. 49

Ex. 1005, Figure 49, [0208].

155. Toyama also refers to “pedestal channel portions 11” as “epitaxial channel portions 11,” which a POSITA would understand to mean that “pedestal channel portions 11” are formed epitaxially. Ex. 1005, [0202], [0208]. Indeed, a POSITA would have found Toyama’s description of how it forms “portions 11” to

be consistent with an epitaxial process. *Id.*, [0202] (“The selective semiconductor deposition **grows a semiconductor material**. ... During a selective semiconductor deposition process, a reactant (such as silane, dichlorosilane, trichlorosilane, disilane, etc.) can be flowed into a deposition chamber simultaneously with, or, alternatively with, an etchant (such as hydrogen chloride).”) (emphasis added).

156. At the very least, a POSITA would have found it obvious to form “pedestal channel portions 11” epitaxially, thus rendering obvious the claimed *epitaxial layer*. As I explained in the background section, above, techniques for epitaxy in 3D NAND flash memories were well-known and within the skill of a POSITA. And a POSITA would have known of the benefits of an epitaxial pedestal including improved performance and reliability characteristics. Thus, implementing “pedestal channel portions 11” using epitaxy would be nothing more than applying a known technique (“epitaxy”) to a known device (Toyama) to yield predictable results (e.g., performance and reliability characteristics).

C. Ground 2: Toyama’s First Exemplary Structure in View of the Knowledge of a POSITA

157. In my opinion, when viewed and considered in light of the knowledge of a POSITA, Toyama’s first exemplary structure renders claim 10 of the ’806 patent obvious.

1. Claim 8

[8.Pre] “A three-dimensional (3D) memory device, comprising:”

158. I offer no opinion on whether the preamble is or is not limiting. However, if the preamble is considered to be a limitation, my opinion is that Toyama discloses it. Indeed, the first sentence of Toyama’s detailed description states that “the present disclosure is directed to three-dimensional non-volatile memory devices, such as vertical NAND strings and other three-dimensional devices, and methods of making the same.” Ex. 1005, [0156].

[8.A] “an alternating conductor/dielectric layer stack;”

159. Toyama’s first exemplary structure discloses this element. As can be seen in Fig. 17A below, Toyama’s “alternating stack (132, 146, 232, 246)” is the claimed *alternating conductor/dielectric layer stack*. I note that only some of the alternating conductors (green) and dielectric (yellow) layers are highlighted to avoid cluttering the figure.

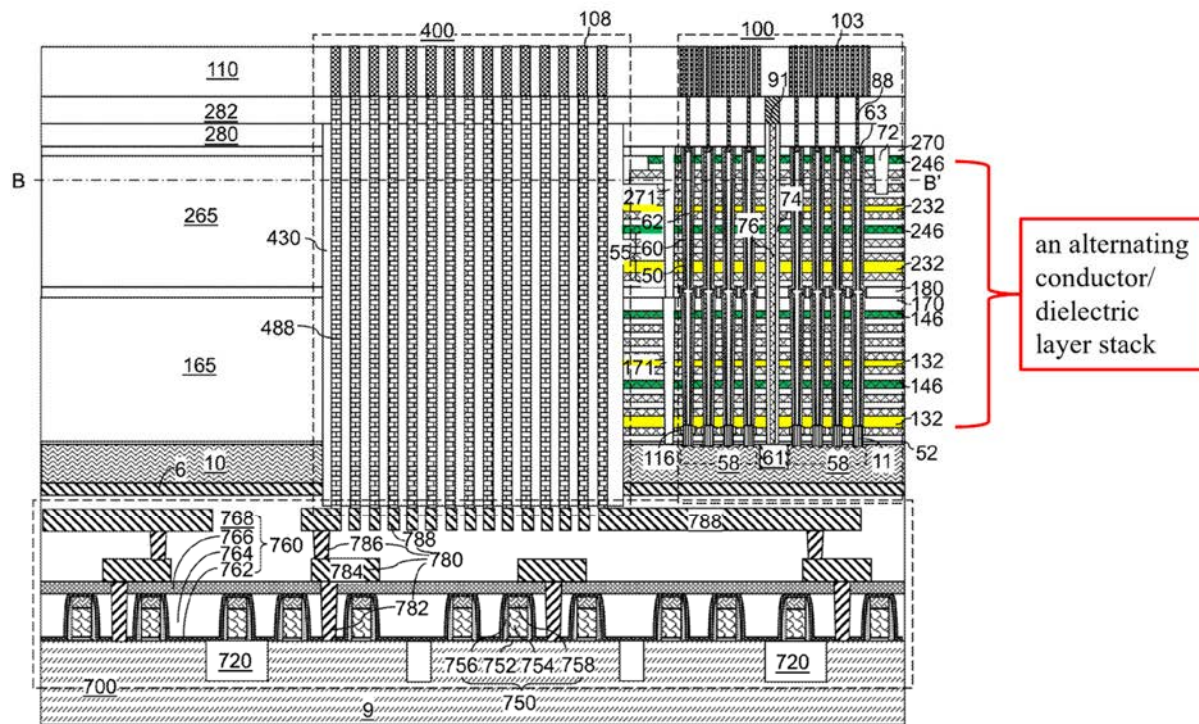


FIG. 17A

Ex. 1005, Fig. 17A (annotated). Toyama “alternating stack” comprises “first and second conductive material layers (146, 246),” “first insulating layers 132,” and “second insulating layers 232.” *Id.*, [0172], [0190], [0228], [0232].

[8.B] “a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;”

160. For ease of analysis, I separate this limitation into two sub-parts and address how Toyama’s first exemplary structure teaches each in turn.

[8.B.i] “a dielectric structure”

161. As shown below in Fig. 15A, in Toyama’s first exemplary structure the upper part of “dielectric fill material portion 430” (viz., above the top of substrate 10) is the claimed *dielectric structure*:

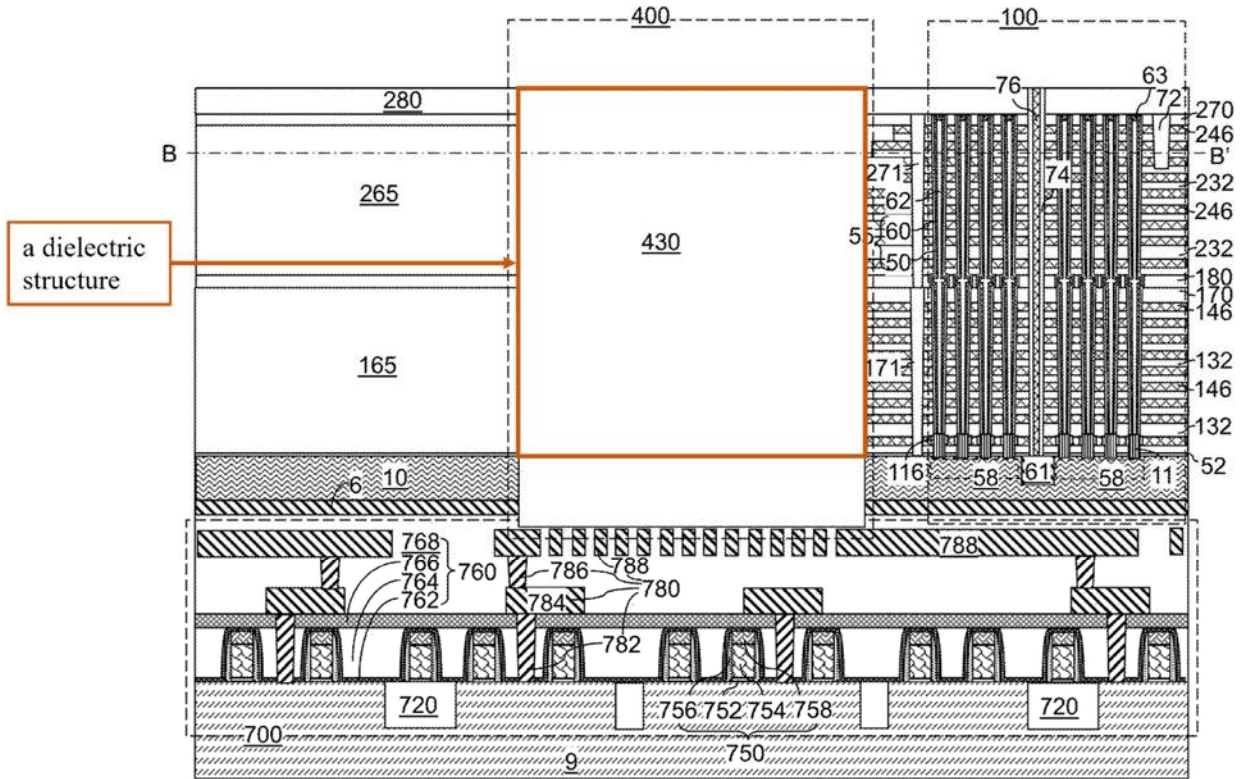
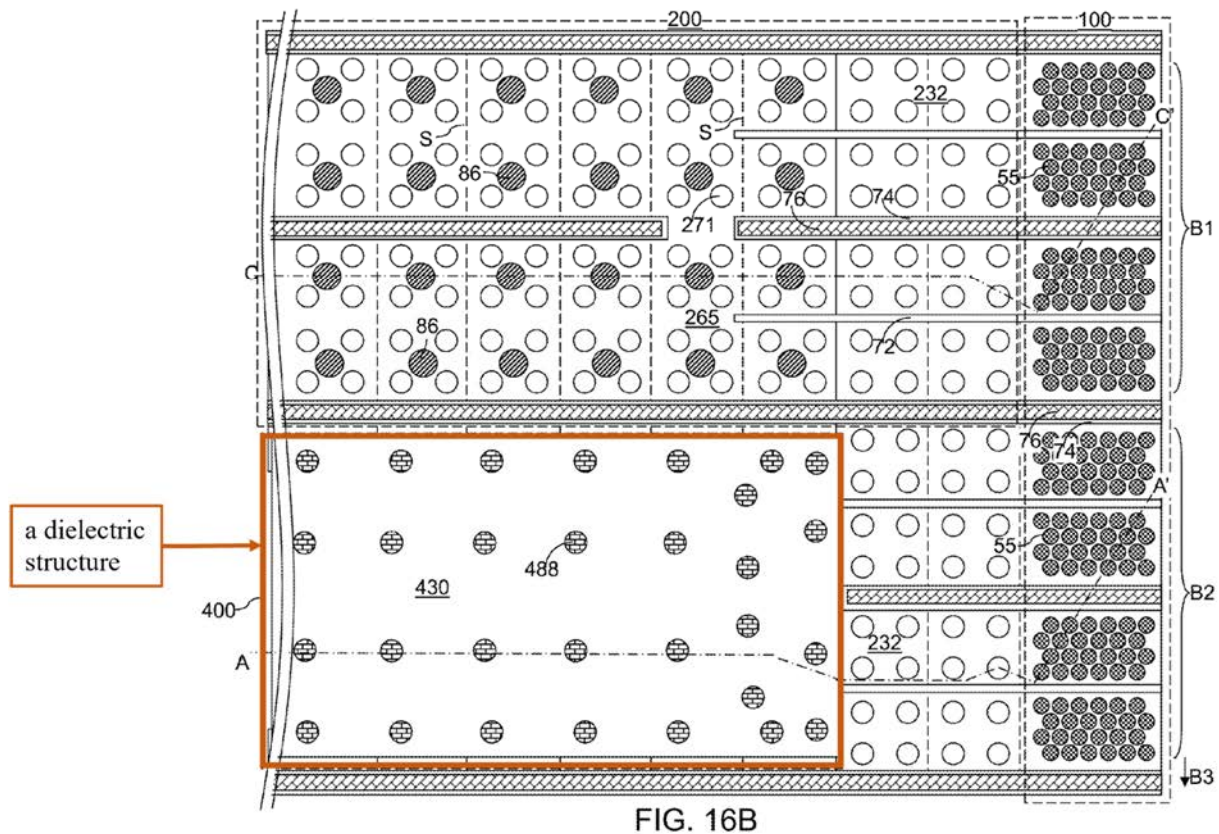


FIG. 15A

Ex. 1005, Fig. 15A (annotated). Toyama Fig. 16B also provides a top view of the *dielectric structure* (“dielectric fill material portion 430”):



Id., Fig. 16B (annotated). Toyama explains that “a dielectric fill material portion 430 is formed within each through-memory-level opening 769, for example, by deposition of a dielectric fill material.” *Id.*, [0216]. Thus, the upper section of the “dielectric fill material portion 430” is *a dielectric structure* because it is composed of “a dielectric fill material.” *Id.*

[8.B.ii] “... extending vertically through the alternating conductor/dielectric layer stack”

162. As I discussed in the previous section, the upper part of Toyama’s “dielectric fill material portion 430” is the claimed *dielectric structure*. And, as I discussed in connection with element [8.A], Toyama’s “alternating stack (132, 146,

232, 246)” is *the alternating conductor/dielectric layer stack*. Accordingly, as shown in Fig.15A below, Toyama discloses *a dielectric structure* (upper part of “dielectric fill material portion 430”) *extending vertically through the alternating conductor/dielectric layer stack* (“alternating stack 132, 146, 232, 246”):

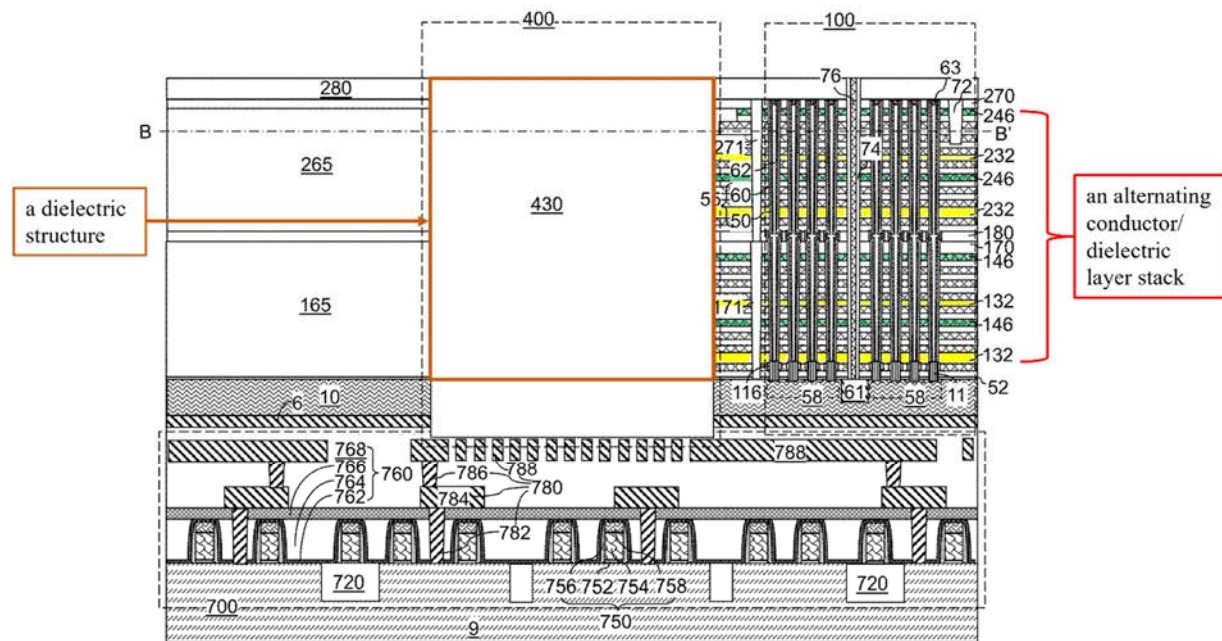


FIG. 15A

Ex. 1005, Fig. 15A (annotated).

163. I note here that Toyama’s first exemplary structure satisfies this limitation in substantially the same way as one of the embodiments in the ’806 patent. In particular, the ’806 specification shows an embodiment where dielectric structure 124 is surrounded on three sides by an alternating conductor/dielectric layer stack. This can be seen in Fig. 1C below, which is a top view of a 3D NAND device (with memory region 110 on the right and staircase region on the left):

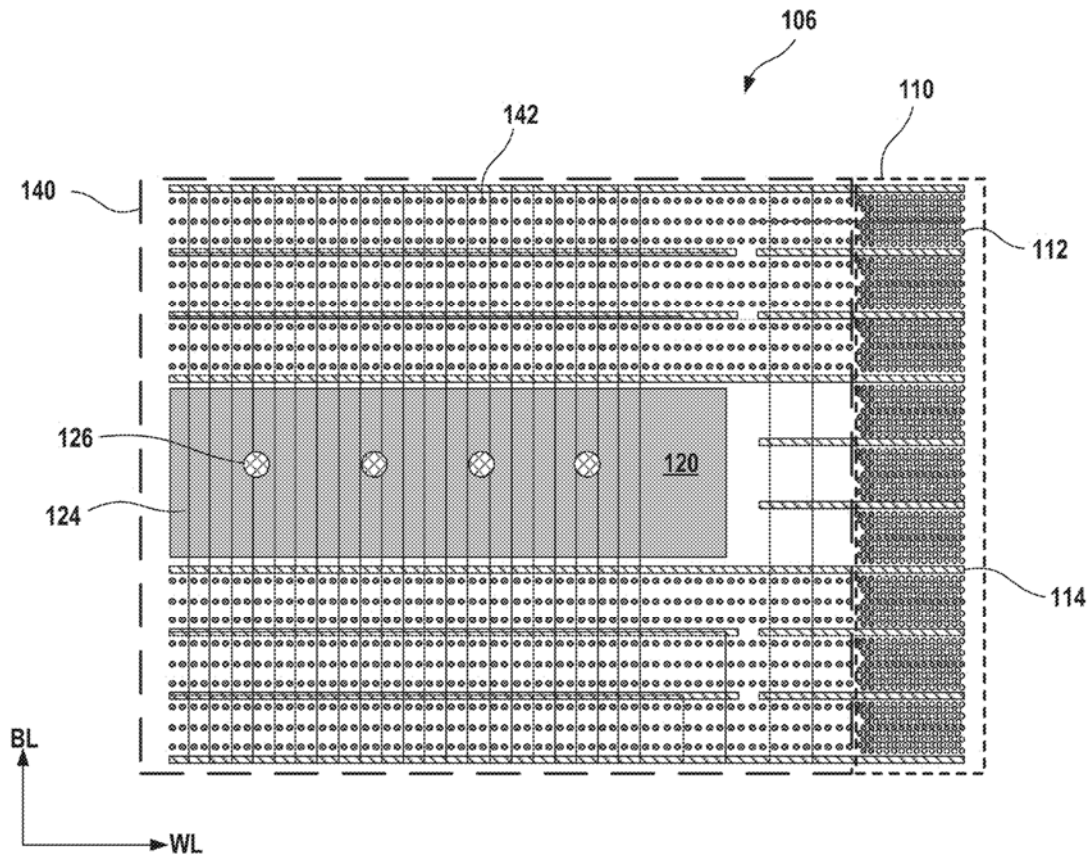


FIG. 1C

Ex. 1001, Fig. 1C.

164. Toyama's first exemplary structure is similar: the *dielectric structure* (upper part of "dielectric fill material portion 430") borders three regions including an alternating conductor/dielectric layer stack. This is shown in Toyama Fig. 16B below, which is a top view of a 3D NAND device (with "memory array region 100" on the right and staircase regions ("word line contact via region 200") on the left). Although not illustrated in Fig. 16B, I note that region 200 extends on the bottom of the figure as well.

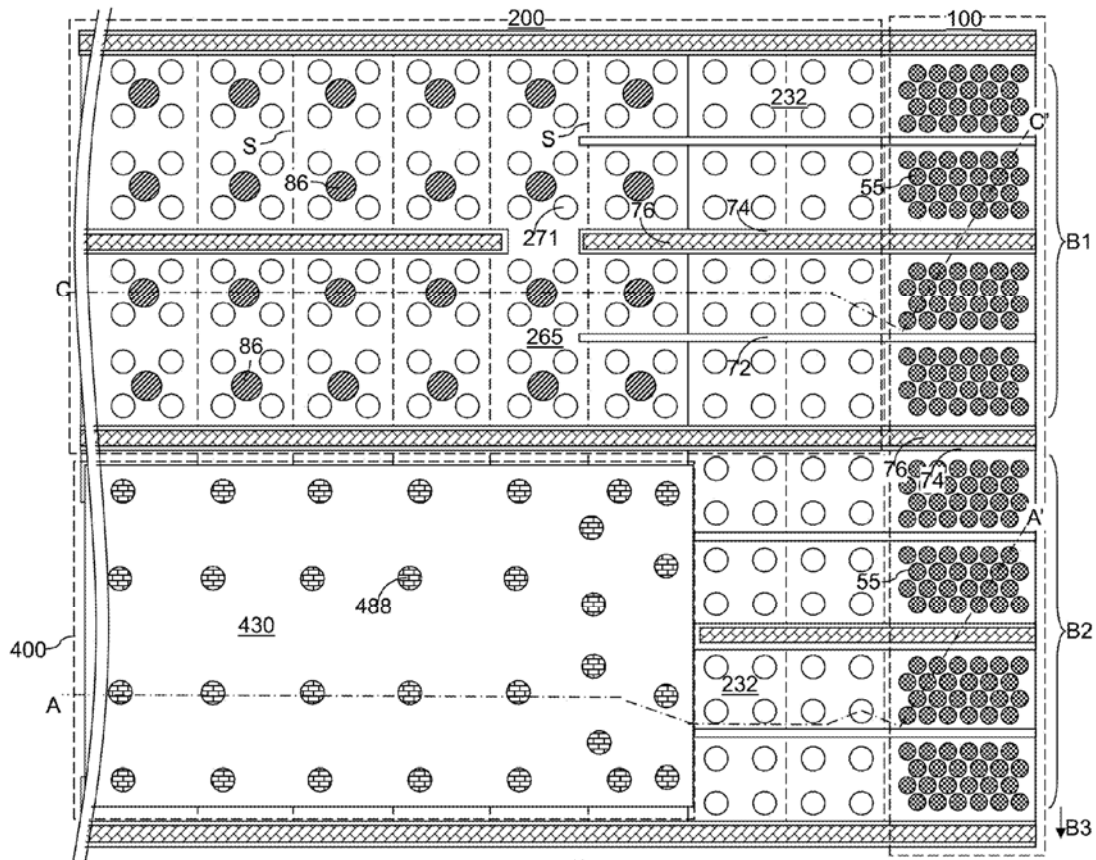


FIG. 16B

Ex. 1005, Fig. 16B.

165. Toyama forms its *dielectric structure* (upper part of “dielectric fill material portion 430”) in the same way as the ’806 patent forms its dielectric layer 702. The “dielectric fill material portion 430” in Toyama and “dielectric layer 702” in the ’806 specification are both formed by removing part of the dielectric stack before replacing the sacrificial layers with electrically conductive layers. In particular, the ’806 patent removes part of “dielectric stack 400” to form “opening 600”:

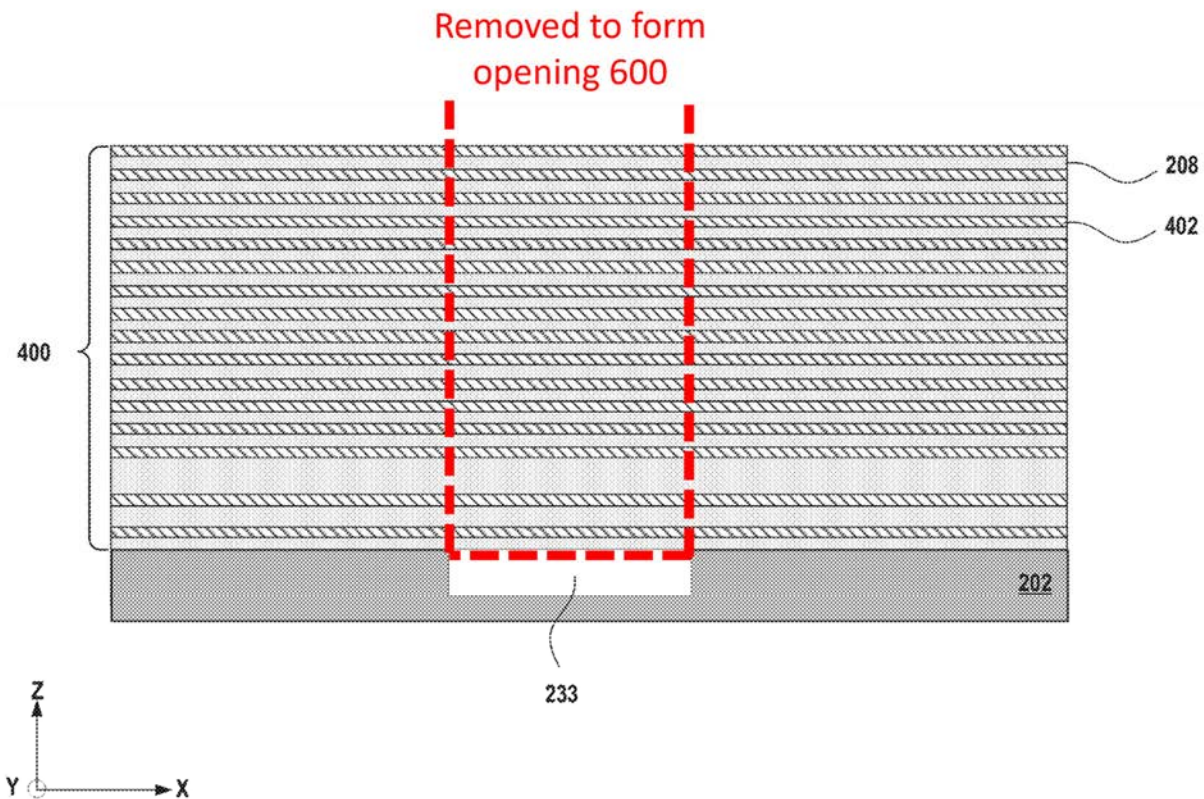


FIG. 4

Ex. 1001, Fig. 4 (annotated); *see also id.*, Fig. 6, 15:16-18. The '806 patent then fills “opening 600” with “dielectric layer 702.” *Id.*, 15:46-48.

166. In like manner, Toyama’s first exemplary structure removes “insulating layers” 132, 232 and “sacrificial material layers” 142, 242 to form “opening 769,” as shown below in Fig. 10A:

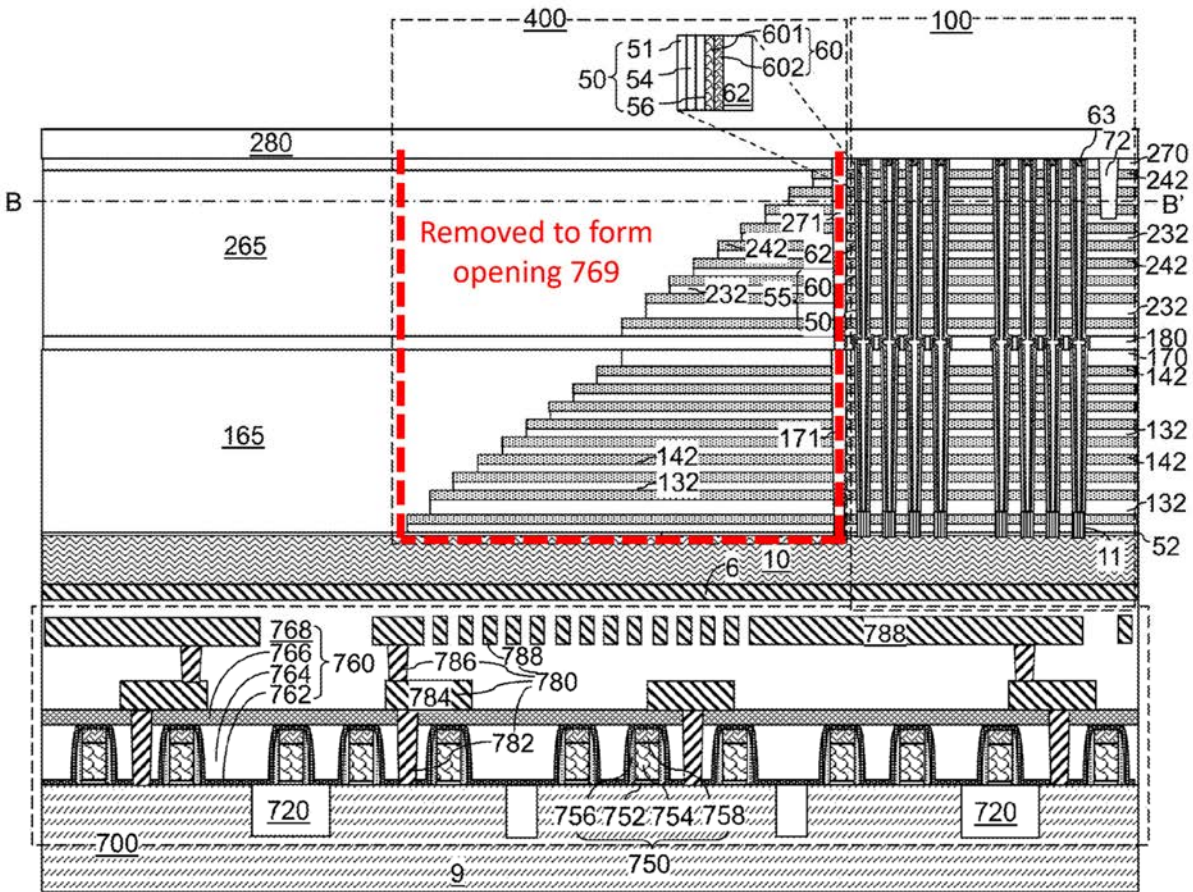


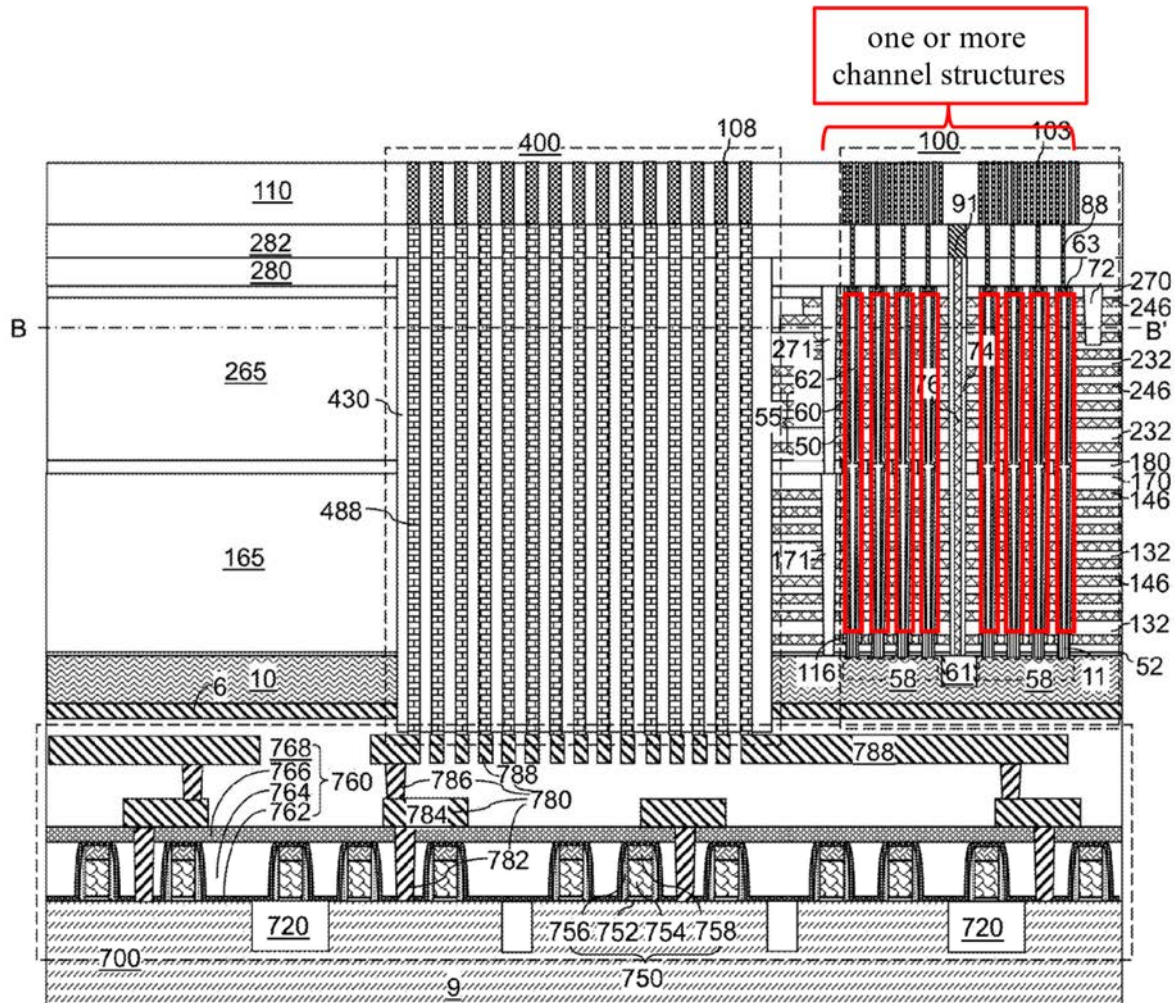
FIG. 10A

Ex. 1005, Fig. 10A (annotated), [0173], [0189]. Toyama then fills “opening 769” with “dielectric fill material portion 430.” Thus, Toyama’s first exemplary structure discloses this limitation.

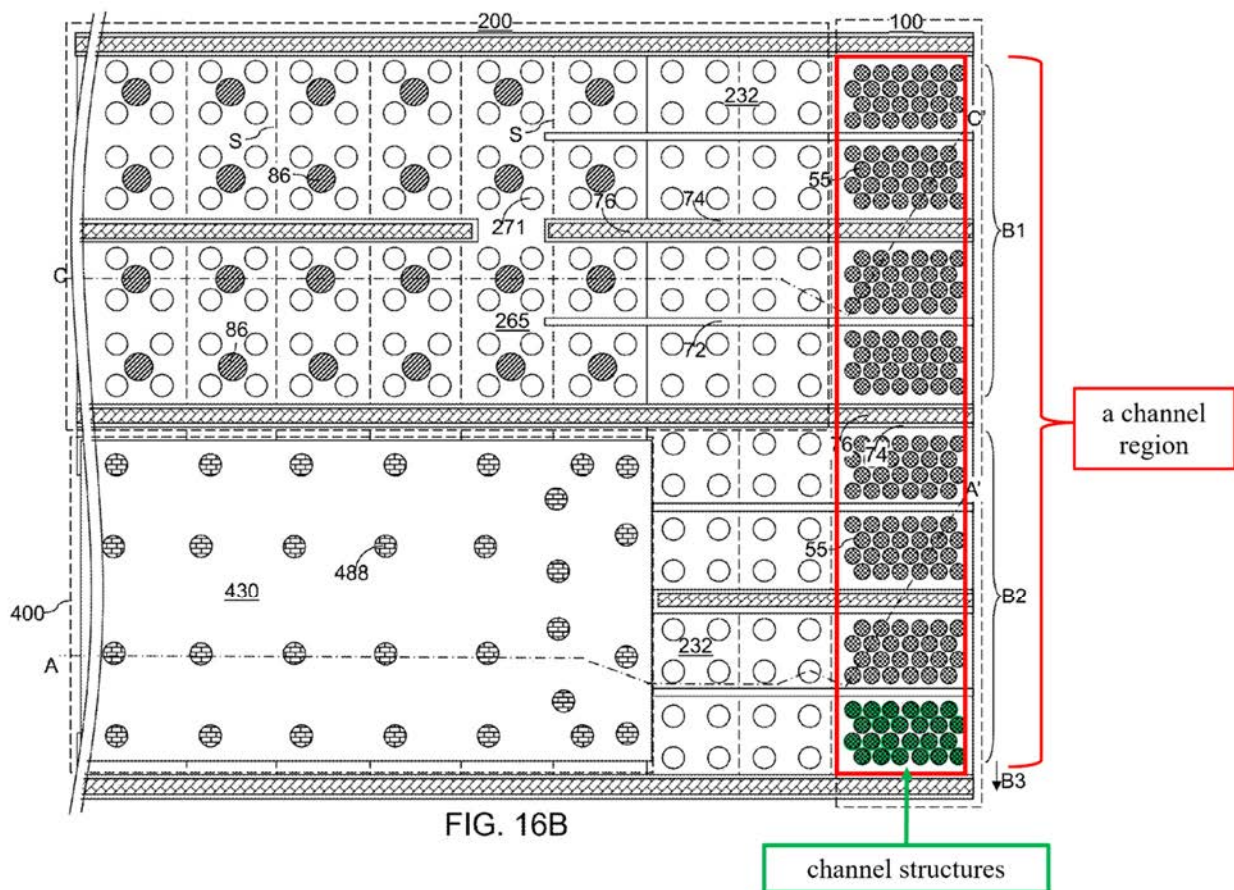
[8.C] “first and second channel regions comprising first and second pluralities of channel structures, respectively;”

167. The “memory stack structures 55” in Toyama are each *a channel structure[]*, as illustrated below in Fig. 17A. As can be seen, multiple “memory stack structures 55” are grouped together, thus forming a *pluralit[y] of channel*

structures. I will discuss further below why Toyama discloses and renders obvious *first and second pluralities*.

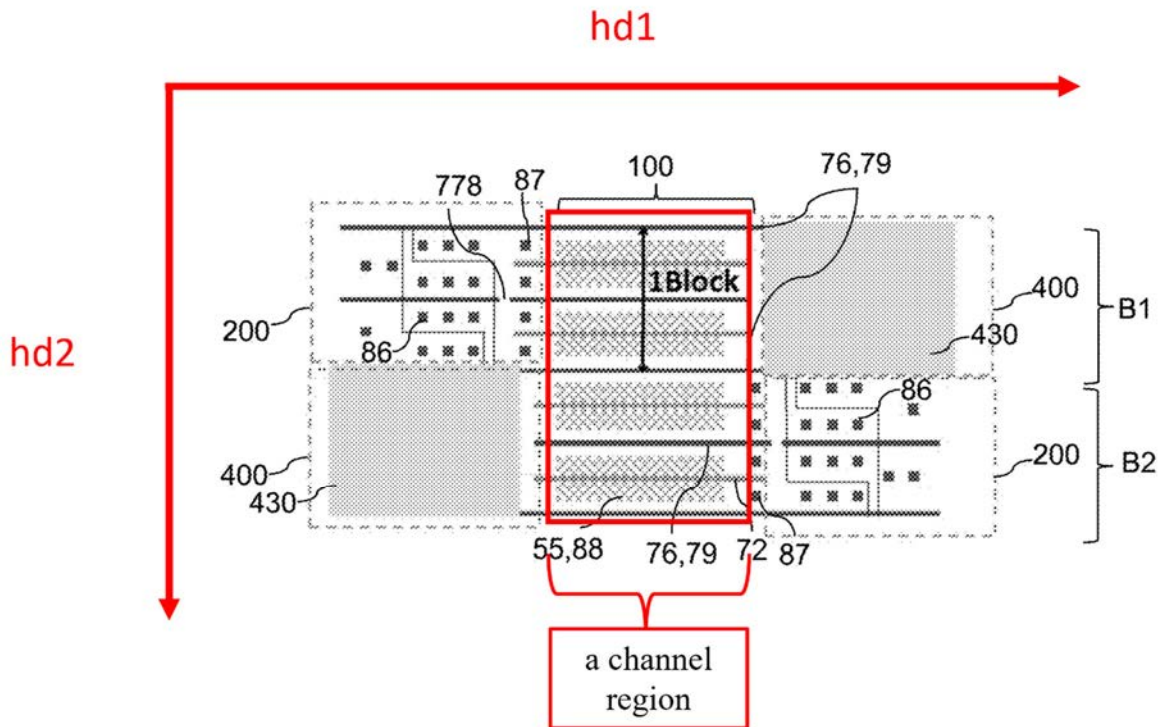


Ex. 1005, Fig. 17A (annotated), [0203]. Toyama Fig. 16B also provides a top view of the *channel structures* (“memory stack structures 55”) in Toyama’s first exemplary structure.



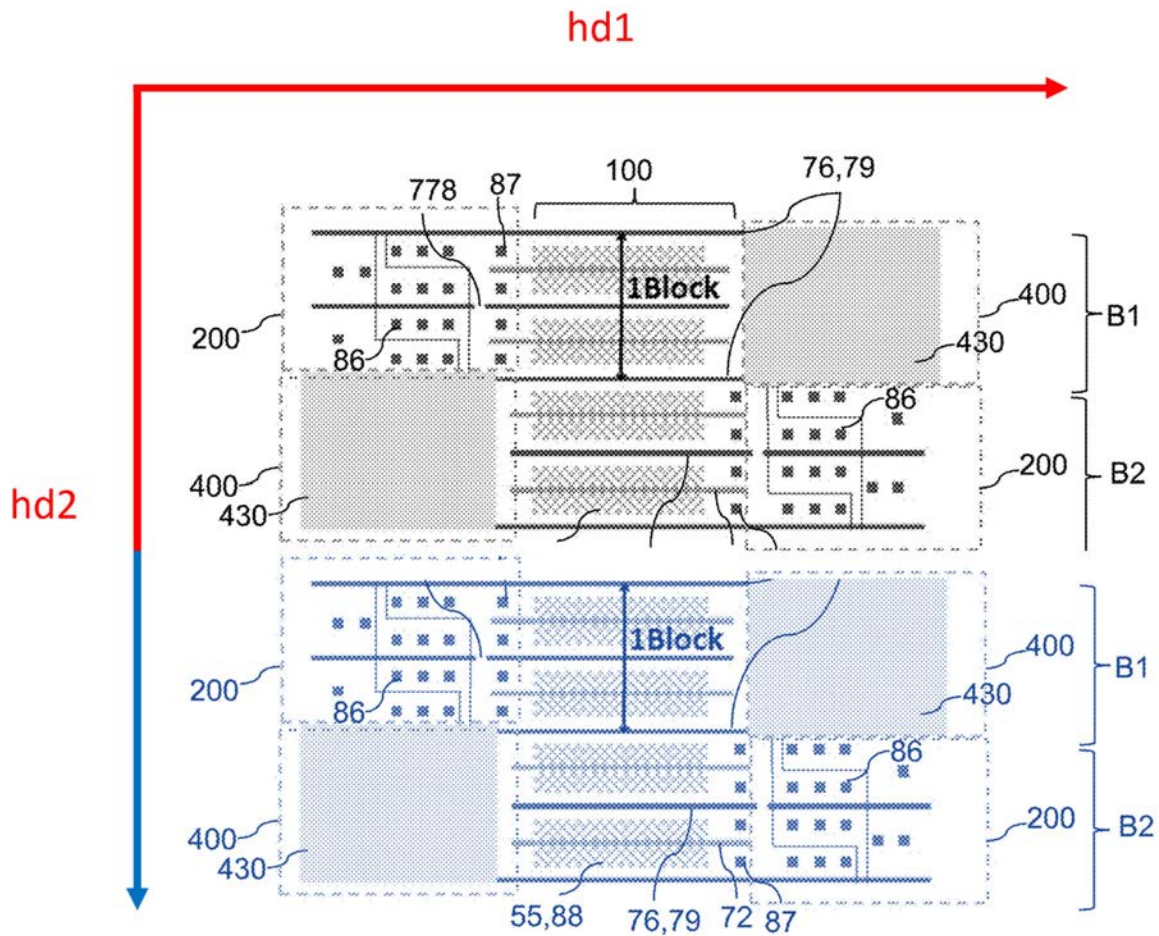
Id., Fig. 16B (annotated).

168. The area in which Toyama’s *channel structures* (“memory stack structures 55”) are located constitutes *a channel region* (part of “memory array region 100”). This area is identified in Fig. 16B above. It is also identified in Toyama Fig. 17E below, which Toyama teaches for use with Toyama’s other teachings of its first exemplary structure. Ex. 1005, [0049] (“FIGS. 17E and 17F are top-down views of an alternative exemplary structure according to the first embodiment of the present disclosure.”).



Id., Fig. 17E (annotated).

169. Toyama expressly discloses that “a neighboring pair of an odd-numbered block and an even-numbered block (such as B1 and B2) can be periodically repeated along the second horizontal direction,” which is labeled hd2 in the figure above. Ex. 1005, [0220]. Repeating the layout of Fig. 17E as Toyama teaches results in the exemplary formation shown below.

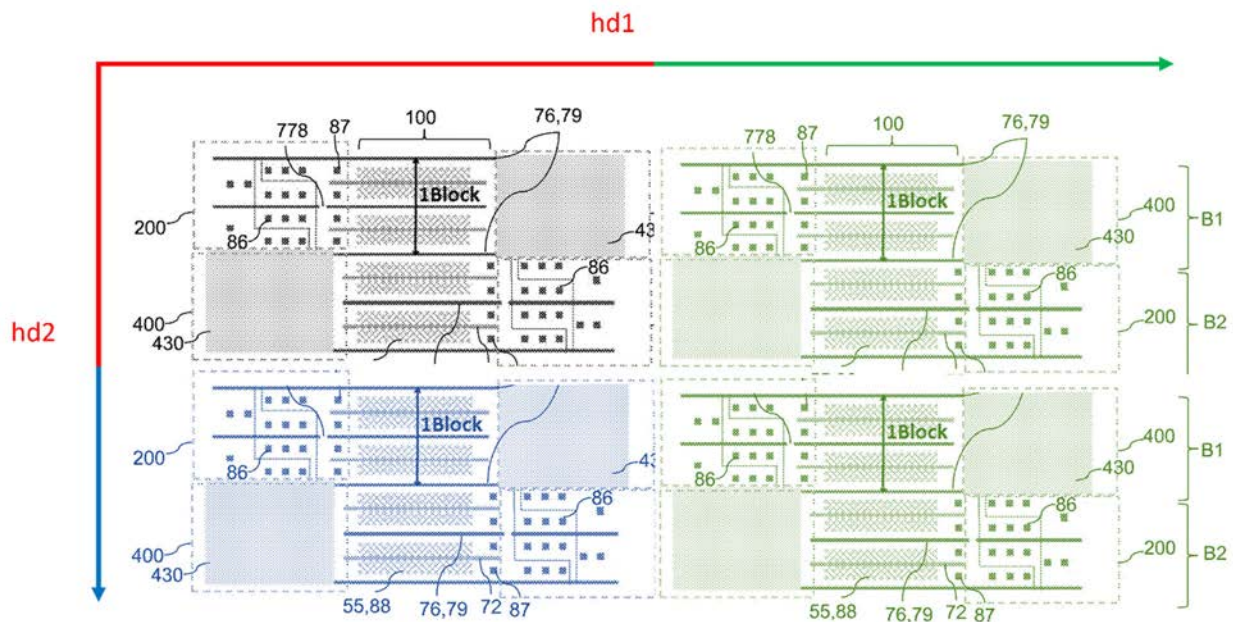


Id., Fig. 17E (modified).

170. Although Toyama does not expressly teach repeating the layout in the h1 (left-right direction), a POSITA would have found doing so obvious as I explain in the next sub-section.

a. Repeating Toyama's layout in both the x- and y-directions would have been obvious to a POSITA to implement multiple memory planes

171. It would have been obvious to a POSITA to repeat Toyama's first exemplary structure to implement multiple memory *planes* in a 3D memory device, resulting in the exemplary configuration below.



Ex. 1005, Fig. 17E (modified).

i. A POSITA would have been well aware of how to implement multiple flash memory planes in a NAND flash memory device and motivated to do so

172. Flash architectures utilizing memory planes were well-known to POSITAs long before the 2018 priority date of the '806 patent. Memory planes are simply higher-level organizational paradigms that group together multiple memory blocks and which facilitate operation of the memory device. Memory blocks are

discussed extensively throughout Toyama. *See, e.g.*, Ex. 1005, [0004]-[0009] and [0220]-[0221]. A POSITA would have known to implement a flash memory device with multiple memory planes, each including a distinct memory array region and staircase structure. For example, Chapter 6 (titled NAND Flash Design) of Micheloni's text on SSDs from 2013 teaches that "[w]ith reference to Fig. 6.1, the memory array has been split in ***two independent planes***." Ex. 1023 (Micheloni, Inside SSDs (2013)), 144 (emphasis added).

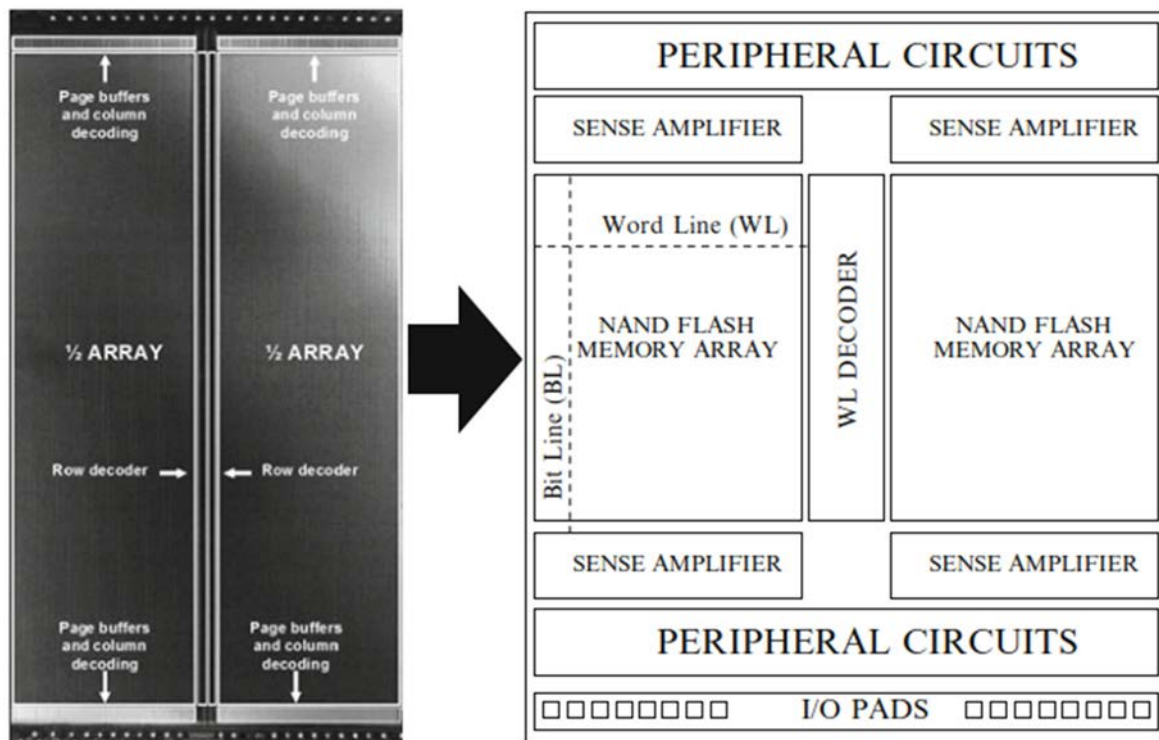
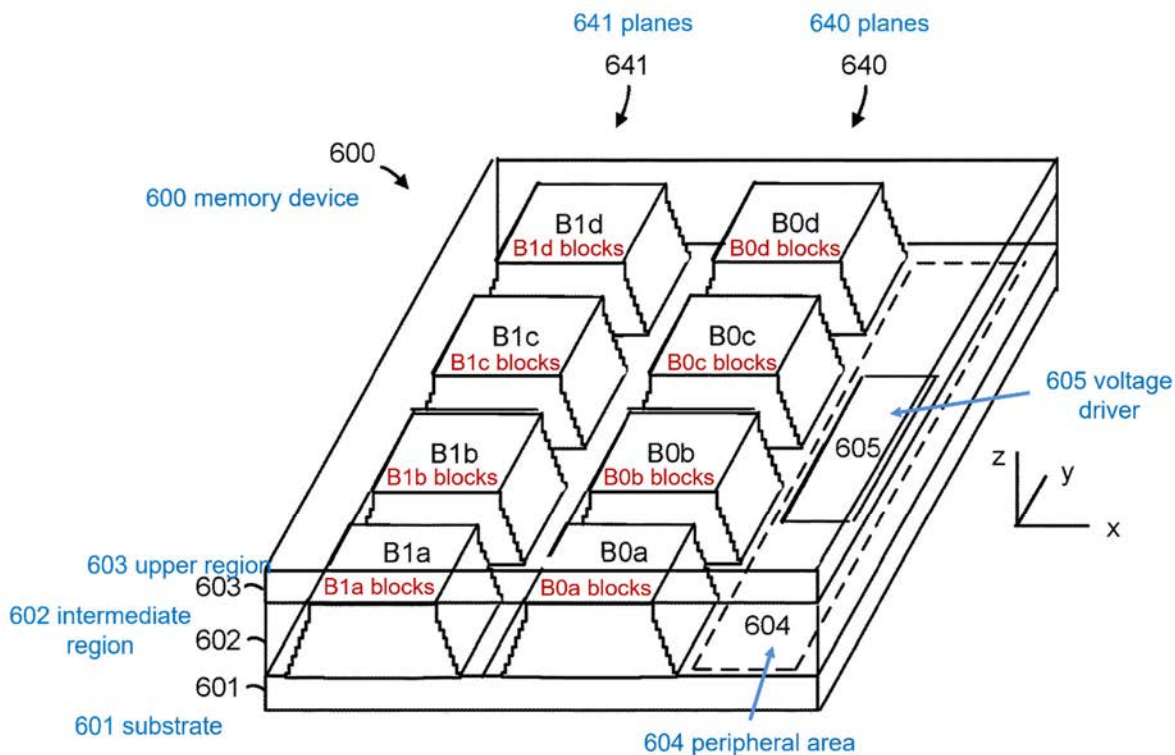


Fig. 6.1 A typical NAND Flash floorplan [1]

173. A POSITA would have known that a “NAND flash storage device or storage system, e.g., a solid-state disk (SSD) and flash cards, may be associated with

multiple chips. Each chip is composed of one or more sub-chips or dies. Each sub-chip might have multiple planes. Each plane is organized in terms of blocks that are the basic unit for erase operations.” Ex. 1023 (Michelsoni, Inside SSDs (2013)), 247.

174. A POSITA would have known how to implement a flash memory device with multiple planes by placing the planes beside each other. For example, the below figure illustrates a flash memory device with two planes and four blocks:



Ex. 1024 (U.S. Pat. No. 10,043,558), 13:37-44 (“Two planes 640 and 641 of blocks of memory cells (storage elements) are formed on a substrate 601. ... The plane 640 includes blocks B0a, B0b, B0c and B0d. The plane 641 includes blocks B1a, B1b, B1c and B1d.”).

175. A POSITA’s knowledge of flash memory devices with multiple side-by-side planes is further demonstrated by numerous devices with multiple memory planes that had already been designed and manufactured before the priority date. I present below some examples that illustrate such devices:

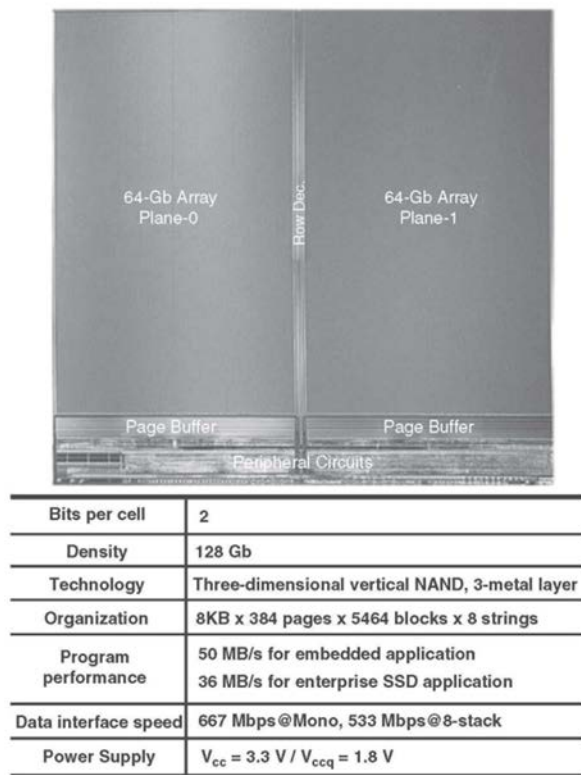


FIGURE 7.35 Die micrograph and main feature of 128-Gb 2-bit/cell 3D V-NAND flash. Die size is 133 mm².

Ex. 1014 (Aritome Textbook), 313-314 (“This memory chip has 24 stacked WL layers and consists of two planes each containing 64-Gb arrays (2732 of 3-MB blocks with 8-KB pages).”).

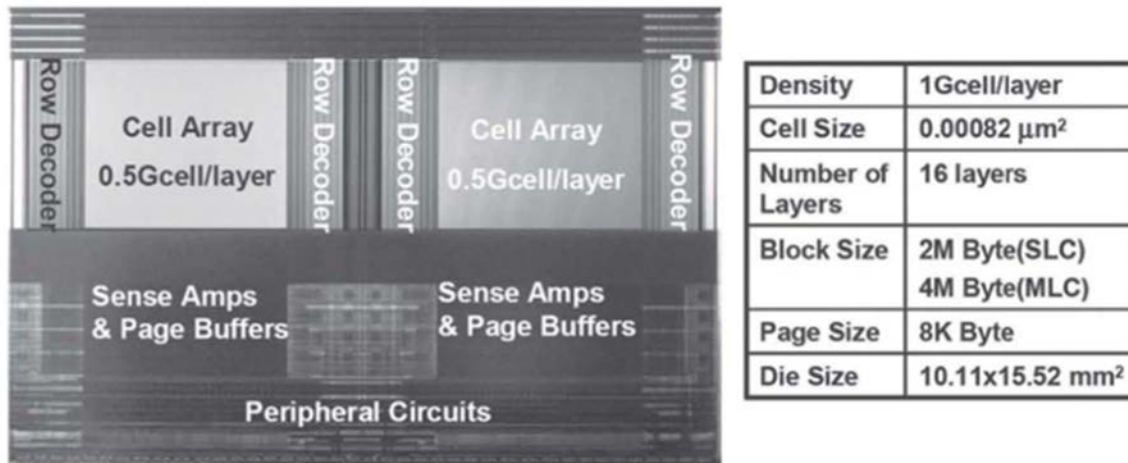


FIGURE 7.26 Image of 16-Gb pipe-shaped BiCS test chip.

Id., 308.

176. By the priority date of the '806 patent, a POSITA would have understood numerous benefits associated with utilizing a multi-plane flash memory architecture. For example, one benefit a POSITA would have been aware of is the ability “to issue a read command on multiple planes simultaneously.” Ex. 1025 (Micheloni, *Inside NAND Flash Memories* (2010)), 42. The figure below, read from left to right, illustrates various page read options. The “double-plane page read” technique is highlighted.

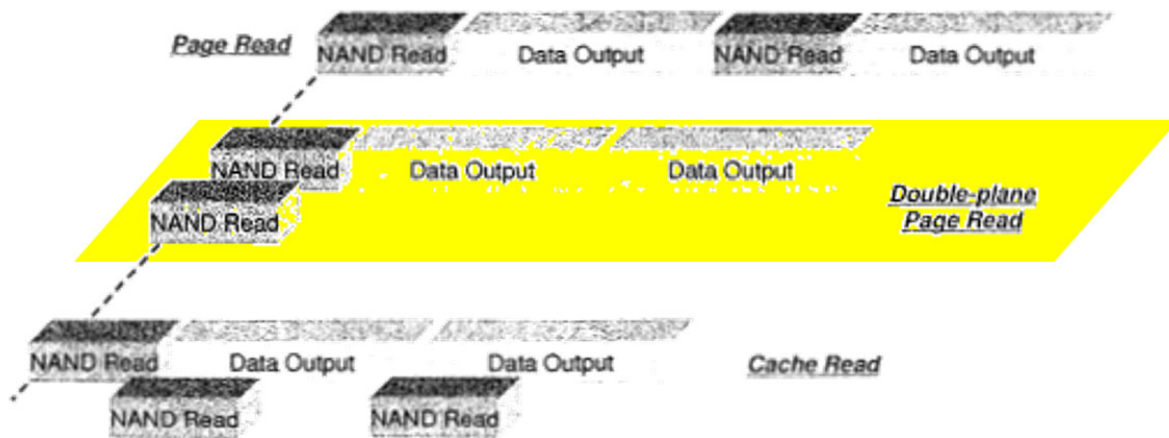


Fig. 2.19. Performance comparison among Read, Double-plane Read and Cache Read

Id.

177. A POSITA would also have known that using multiple planes improves not only read throughput, but the “double-plane program [is] used to increase write throughput,” as highlighted below. Ex. 1025 (Micheloni, Inside NAND Flash Memories (2010)), 44-45.

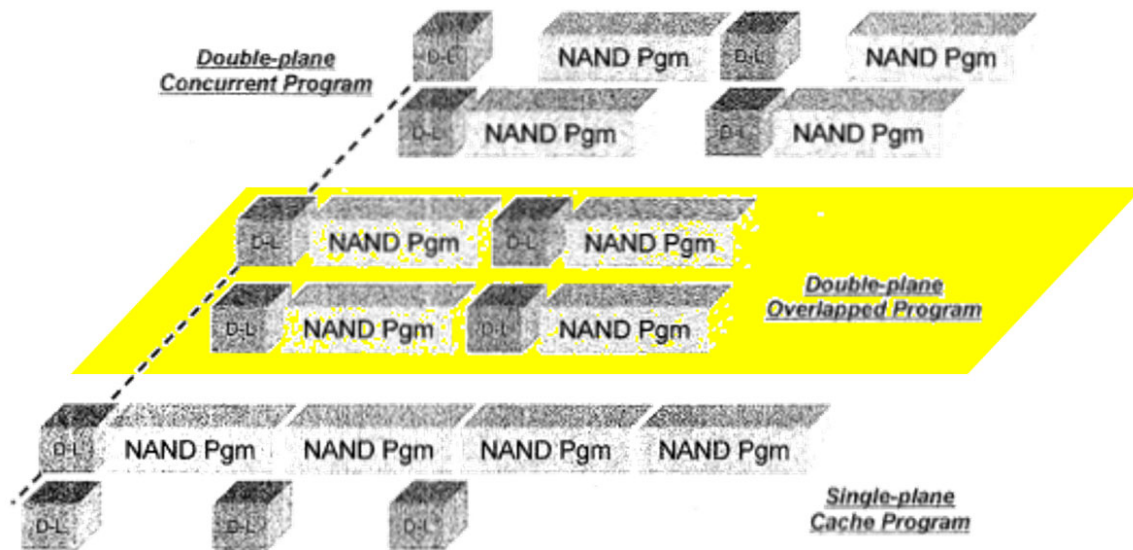


Fig. 2.24. Performance comparison among Cache Program, Overlapped Double Plane program and Concurrent Double Plane Program

Id., 44-45.

178. Thus, it was within a POSITA's knowledge that that "having two internal planes working interleaved" would "improve the performance of NAND based systems." Ex. 1025 (Michelsoni, Inside NAND Flash Memories (2010)), 171. And a POSITA would have known that "[t]his solution [was] quite common because the power issues related to this kind of solution are still manageable inside the chip and optimized versus two separate NAND devices active at the same time." *Id.*

ii. A POSITA would have had a motivation to implement, and would have had a reasonable expectation of success in implementing, multiple planes of Toyama's first exemplary structure in the hd1 direction

179. Although Toyama does not expressly disclose repeating the Fig. 17E layout in the hd1 (horizontal left-right) direction, a POSITA would have been motivated to do so. One reason for doing so is to achieve the benefits of the multiple plane architecture I just discussed. As explained above, a POSITA would have known how to implement multiple planes in a flash memory device like Toyama's. An obvious technique for implementing multiple planes in a flash memory device is to repeat them laterally across the device, the same approach taken by the commercial flash memory products discussed in the previous section.

180. While memory planes could theoretically be implemented in the hd2 (i.e., up-down direction), a POSITA would have found that less desirable because Toyama already contemplates using the hd2 direction to implement multiple blocks (within a single plane). Ex. 1005, Fig. 17E, [0220]. Thus, the more natural option would be to arrange the memory planes side-by-side in the horizontal x-direction (left-right). In any event, it is a simple design choice as to whether to implement planes in the x- or y-direction, and the x-direction is preferable in view of Toyama's teaching about arranging block in the y-direction. Thus, a POSITA would have been

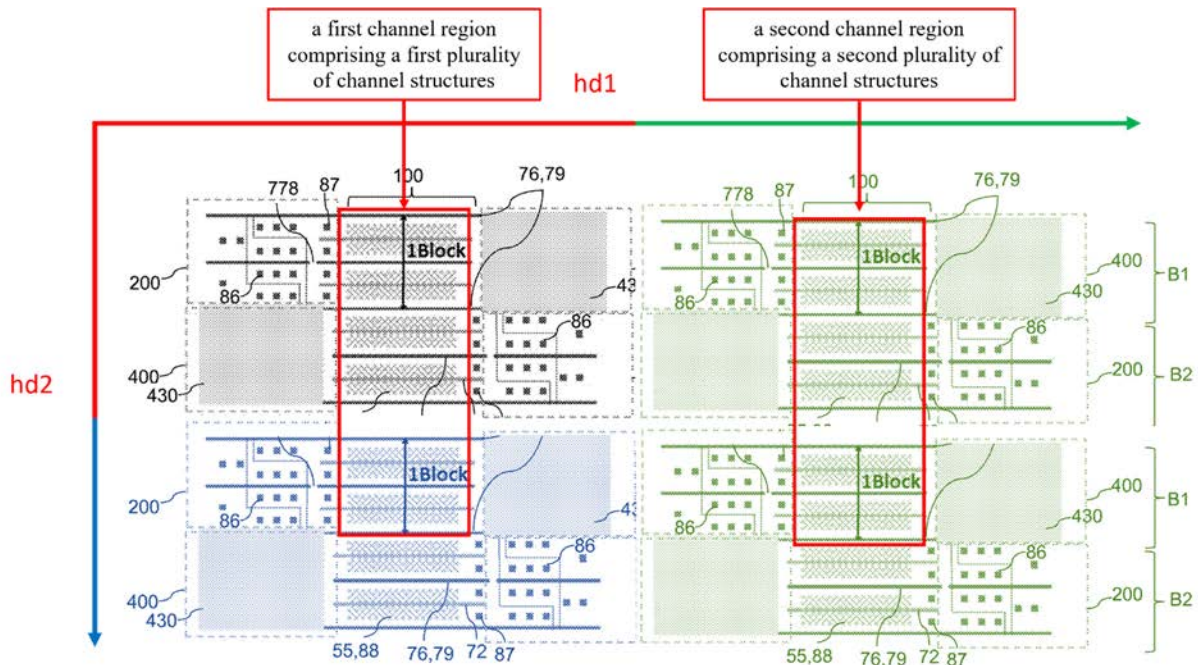
motivated to implement multiple planes of Toyama's first exemplary structure in the hd1 direction.

181. A POSITA also would have had a reasonable expectation of success in implementing multiple planes of Toyama's first exemplary structure in the hd1 direction. As I discussed above, NAND flash memory devices with multiple planes -existed many years before the '806 patent priority date. Using the layout of Toyama's Fig. 17E as the blueprint for a plane, and repeating that layout for each plane, would have been straightforward exercise for a POSITA with predictable results.

182. This obvious modification is nothing more than applying a known technique (implementing multiple planes of a NAND flash memory array) to a known device (Toyama's first exemplary structure) to yield predictable results (a NAND flash device with improved performance).

b. Toyama's modified first exemplary structure with multiple planes satisfies the element [8.C]

183. As discussed in detail in the preceding sections, a POSITA would have found it obvious to implement multiple planes of Toyama's first exemplary structure in the hd1 direction, resulting in the figure below:



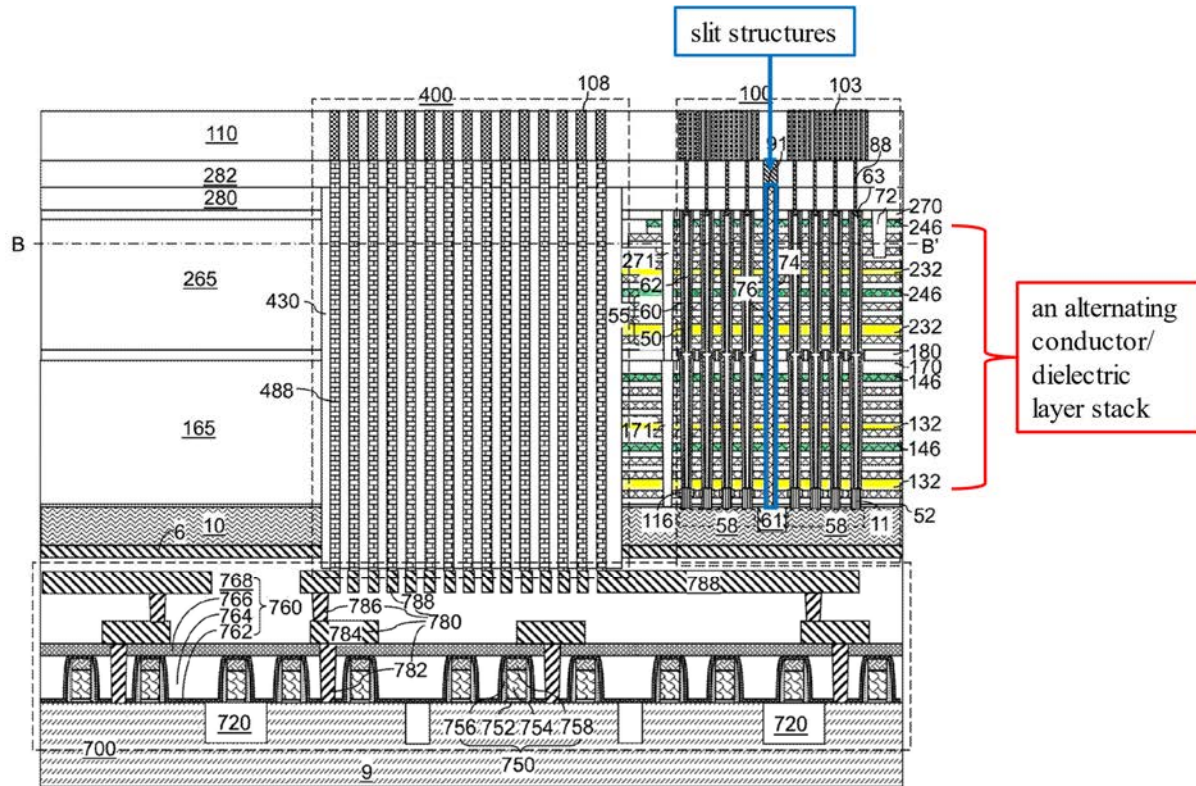
Ex. 1005, Fig. 17E (modified). As shown above, there are *first and second channel regions* (parts of the first and second “memory array regions 100”). Each of these *channel regions* comprise *a plurality of channel structures* (“memory stack structures 55”). *Id.*, Figs. 16B and 17A.

184. In summary, the obvious multi-plane modification to Toyama teaches *first and second channel regions* (first and second parts of “memory array regions 100”) *comprising first and second pluralities of channel structures* (first and second pluralities of “memory stack structures 55”).

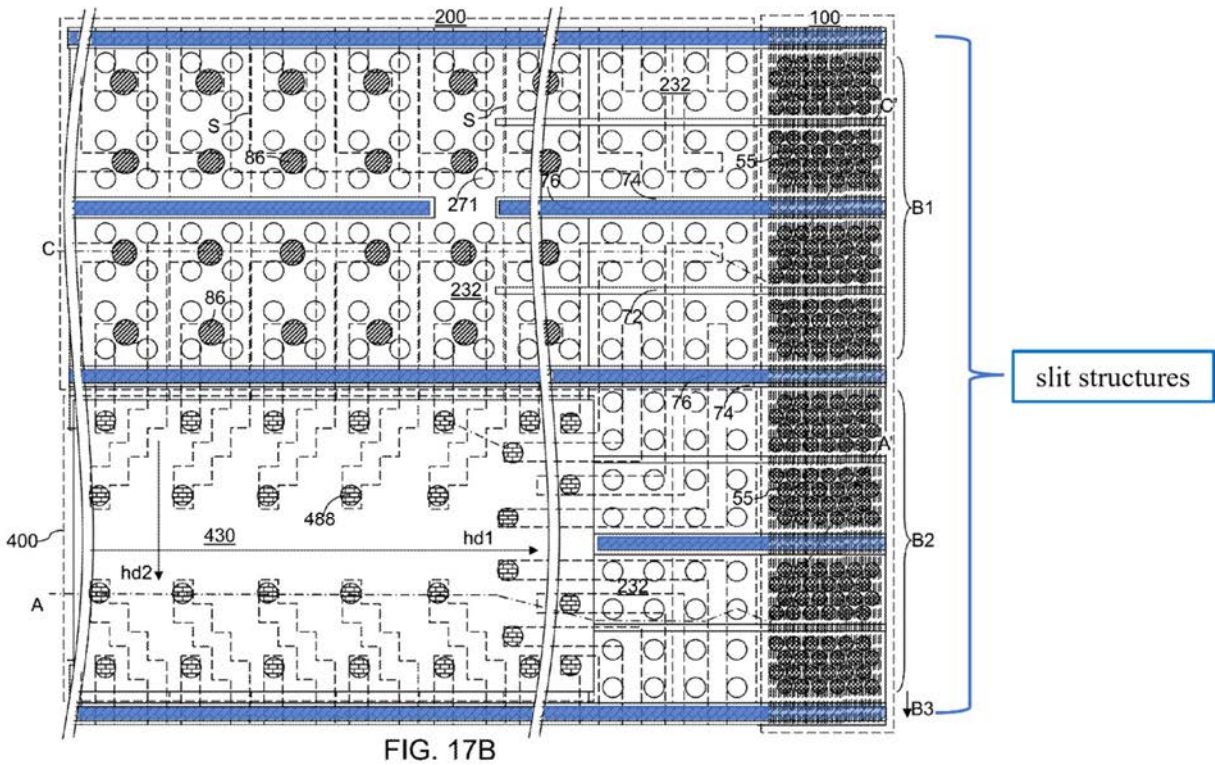
[8.D] “slit structures extending vertically through the alternating conductor/dielectric layer stack;”

185. The claimed *slit structures* in Toyama’s first exemplary structure are the “laterally-elongated contact via structures 76,” and they *extend[] vertically*

through the alternating conductor/dielectric layer stack (“alternating stack (132, 146, 232, 246)”) as shown in Fig. 17A below:



Ex. 1005, Fig. 17A (annotated). The lateral elongated shape of the “laterally-elongated contact via structures 76” *slit structures* is most easily observed in the top view of Fig. 17B:



Id., Fig. 17B (annotated). It is of no import that Toyama refers to the claimed *slit structures* as “laterally-elongated contact via structures 76.” Indeed, the plain meaning of “slit” is a laterally-elongated structure. See Ex. 1021, 4 (Merriam-Webster’s definition of “slit” as “a long narrow cut or opening”).

186. And, as can be seen in Toyama Fig. 17A above, Toyama “laterally-elongated contact via structure 76” *extend[s] vertically in the alternating layer stack* (“alternating stack (132, 146, 232, 246)”), as required by the claim.

187. Even though the claim places no functional limitation on the “slit structure,” Toyama’s “laterally-elongated contact via structures 76” perform the same function as the ’806 patent’s “slit structures.” The ’806 specification explains

that each “slit structure 226 acts as a source contact for NAND strings 204.” Ex. 1001, 10:1-2. Likewise, Toyama’s “laterally-elongated contact via structures 76” serves as “source connection[s].” Ex. 1005, [0241]. And the *slit structures* in Toyama and the ’806 patent both define memory “blocks” in their respective 3D memory arrays. *Compare* Ex. 1001, 9:57-60 (“[s]lit structures 226 ... extend along the y-axis to separate alternating conductor/dielectric stack 210 into multiple blocks.”) *with* Ex. 1005, [0237] (“laterally-elongated contact via structures 76 laterally extend along the first horizontal direction ... and laterally divide the at least one alternating stack ... into a plurality of laterally spaced-apart blocks.”). This reinforces my opinion that Toyama’s first exemplary embodiment meets the claim language.

[8.E] “a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;”

188. The “staircase region” highlighted in Toyama Fig. 17C below is *a staircase structure* that is *disposed in the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”). Moreover, *the staircase structure* (“staircase region”) *comprises levels with each level having a conductor layer* (“electrically conductive layers 146, 246”) *thereon*:

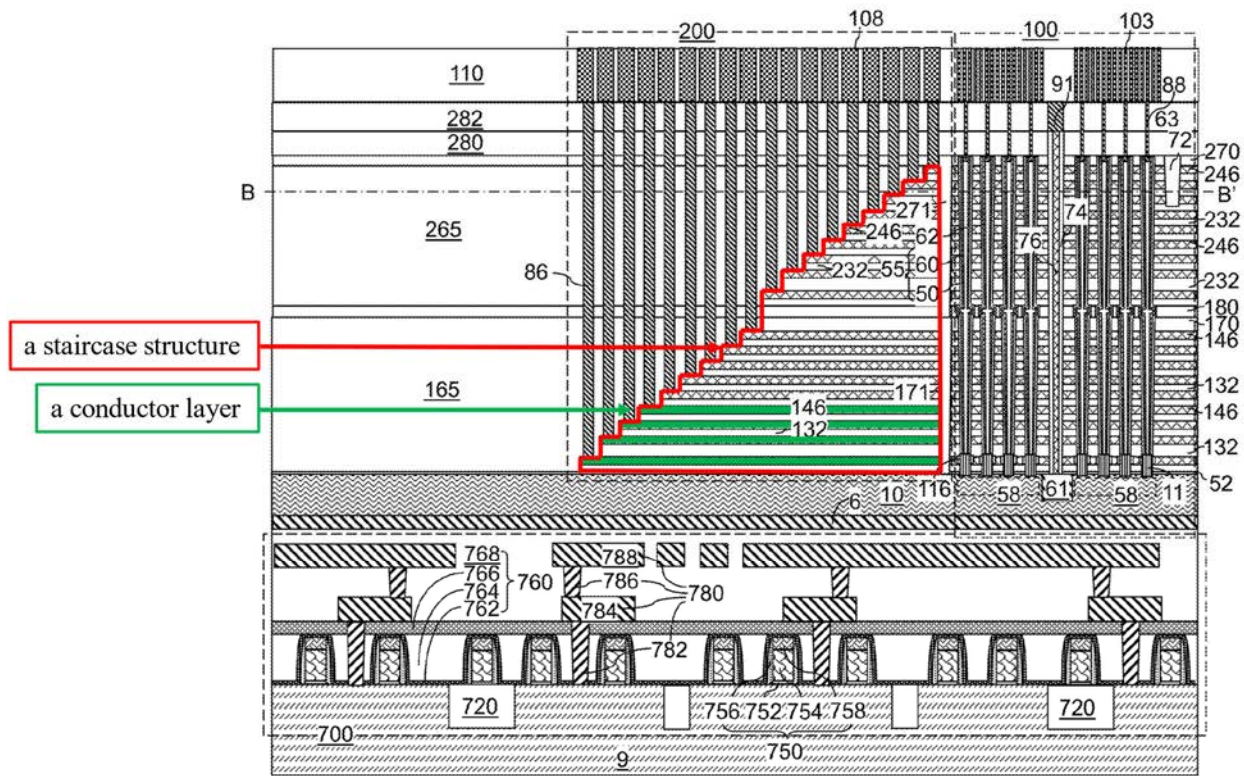


FIG. 17C

Ex. 1005, Fig. 17C (annotated). Toyama explains that “[t]he at least one alternating stack (132, 146, 232, 246) comprises staircase regions that include terraces in which each underlying electrically conductive layer (146, 246) extends farther along the first horizontal direction hd1 than any overlying electrically conductive layer (146, 246).” *Id.*, [0232].

[8.F] “local contacts disposed on the first and second channel structures and the slit structures;”

189. The “drain contact via structures 88” in Toyama’s first exemplary structure are the claimed *local contacts*, that are *disposed on* (in contact with or extending above) *the first and second channel structures* (“memory stack structures

55”), and Toyama’s “source connection via structures 91” are the *local contacts* that are *disposed on* (in contact with or extending above) *the slit structures* (“laterally-elongated contact via structures 76”), as shown in Fig. 17A below:

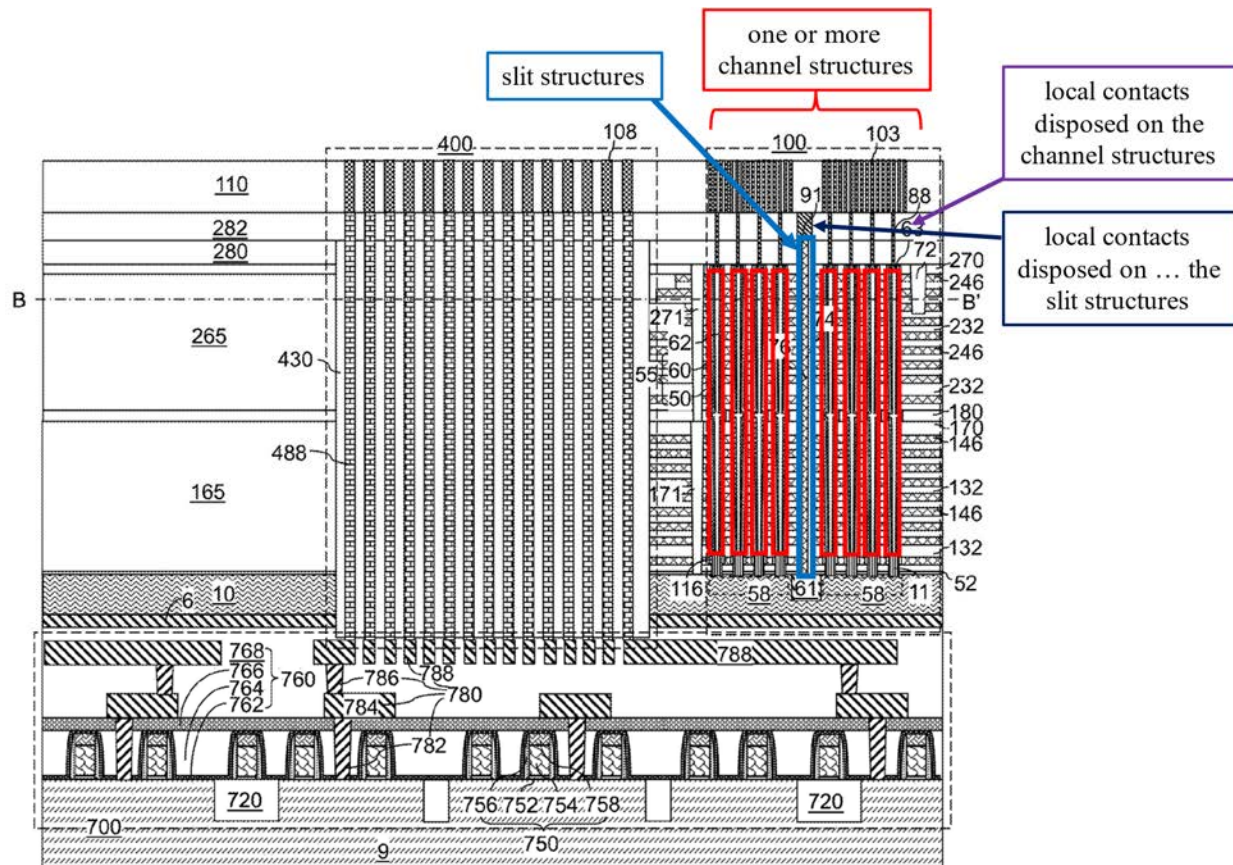


FIG. 17A

Ex. 1005, Fig. 17A (annotated); *id.*, [0251] (“The bit lines 103 are formed over the memory-level assembly, and are electrically coupled to nodes (e.g., drain regions 63) of the memory stack structures 55 by the drain contact via structures 88.”); *id.*, [0241] (“A source connection via structure 91 can extend through the contact level dielectric layers (280, 282) to provide electrical connection to the laterally-elongated

contact via structures 76.”). Toyama’s *local contacts* (“drain contact via structures 88” for the *channel structures*) are *disposed on the first and second [pluralities of] channel structures* because the “drain contact via structures 88” are the same across all of the “memory stack structures 55,” regardless of where or how many times the channel regions in Fig. 17E are repeated or in what direction(s) they are repeated. The same is true for Toyama’s local contacts atop the *slit structures* (“laterally-elongated contact via structures 76”).

190. Additionally, Toyama’s “drain contact via structures 88” are *local contacts disposed on the first and second channel structures*, and Toyama’s “source connection via structures 91” are *local contacts disposed on ... the slit structures*, for the reasons explained above for Ground 1, limitation [8.F].

[8.G] “a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and”

191. Toyama’s first exemplary structure (with the obvious multi-plane modification) discloses this element. For ease of analysis, I divide this element into three sub-parts and address each one. I begin my analysis with the last sub-part, as it is helpful to understand what constitutes a *through array contact (TAC)* in Toyama before discussing the *through array contact (TAC) region* limitation.

[8.G] “[i] a through array contact (TAC) region [ii] formed between the first and second channel regions, [iii] wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and”

192. Toyama’s first exemplary structure (with the obvious multi-plane modification) discloses this element. For ease of analysis, I divide this element into three sub-parts and address each one. I begin my analysis with the last sub-part, as it is helpful to understand what constitutes a *through array contact (TAC)* in Toyama before discussing the *through array contact (TAC) region* limitation.

[8.G.iii] “wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and”

193. In Toyama’s first exemplary structure (and its obvious multi-plane modification), “through-memory-level via structures 488” are the *through array contacts (TACs)*, as shown in Fig. 17A below.

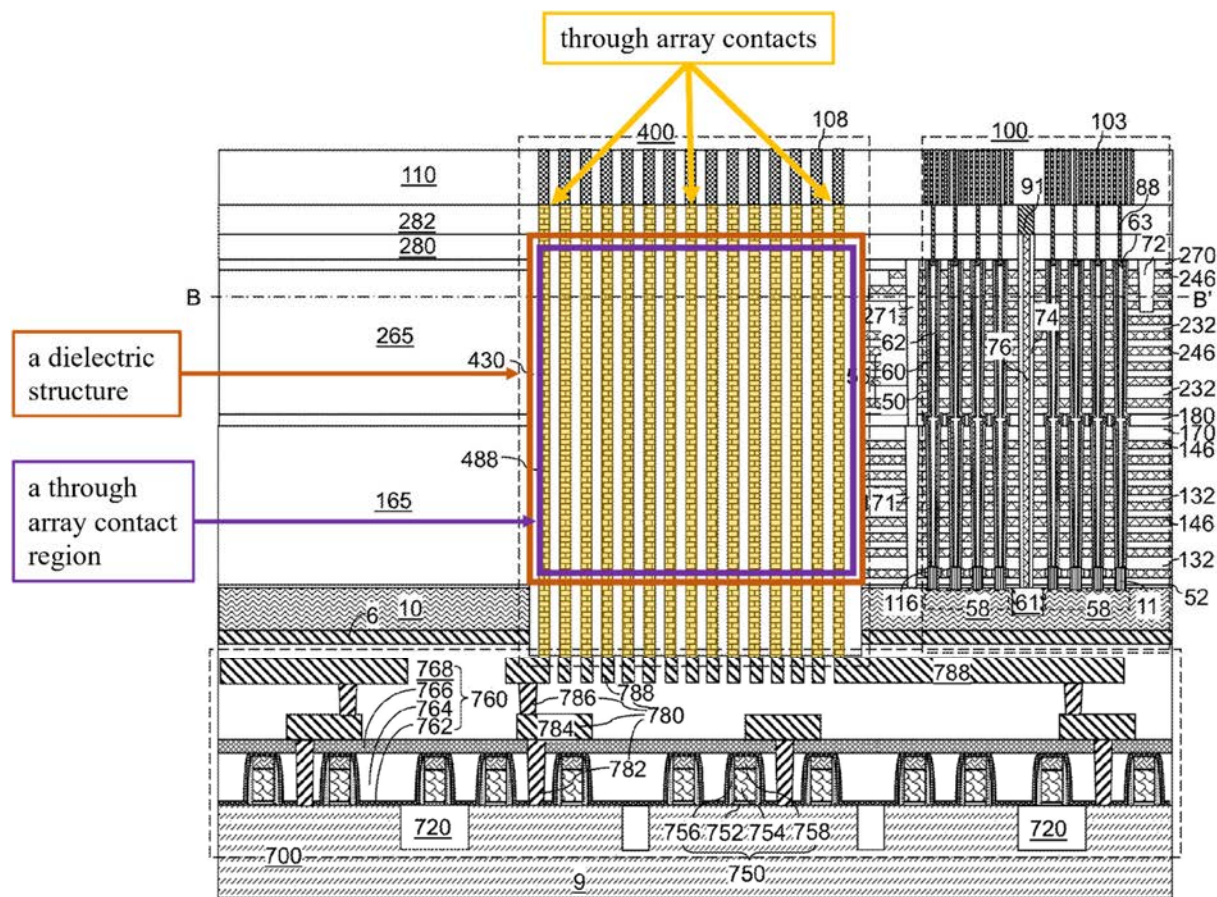


FIG. 17A

Ex. 1005, Fig. 17A (annotated), [0239].

194. As I discussed for element [8.B], in Toyama’s first exemplary structure the upper part of “dielectric fill material portion 430” is *the dielectric structure*. Thus, Toyama discloses *a plurality of through array contacts (TACs)* (“through-memory-level via structures 488”) *extending vertically through the dielectric structure* (upper part of “dielectric fill material portion 430”). Sub-element [8.G.iii] also refers to *the TAC region*, but I address the *through array contact (TAC) region* language in connection with sub-element [8.G.i], which I turn to now.

[8.G.i] “a *through array contact (TAC) region*”

195. The '806 patent discloses that “[i]n some embodiments, dielectric structure 232 defines the boundaries, the shape, and the size of TAC region 120.” Ex. 1001, 10:26-28. Applying the same approach to Toyama’s first exemplary structure (and its obvious multi-plane modification), the *through array contact (TAC) region* is the portion of “through-memory-level via region 400” highlighted below in Fig. 17A. Toyama’s *dielectric structure* (upper part of “dielectric fill material portion 430”) is also identified for reference.

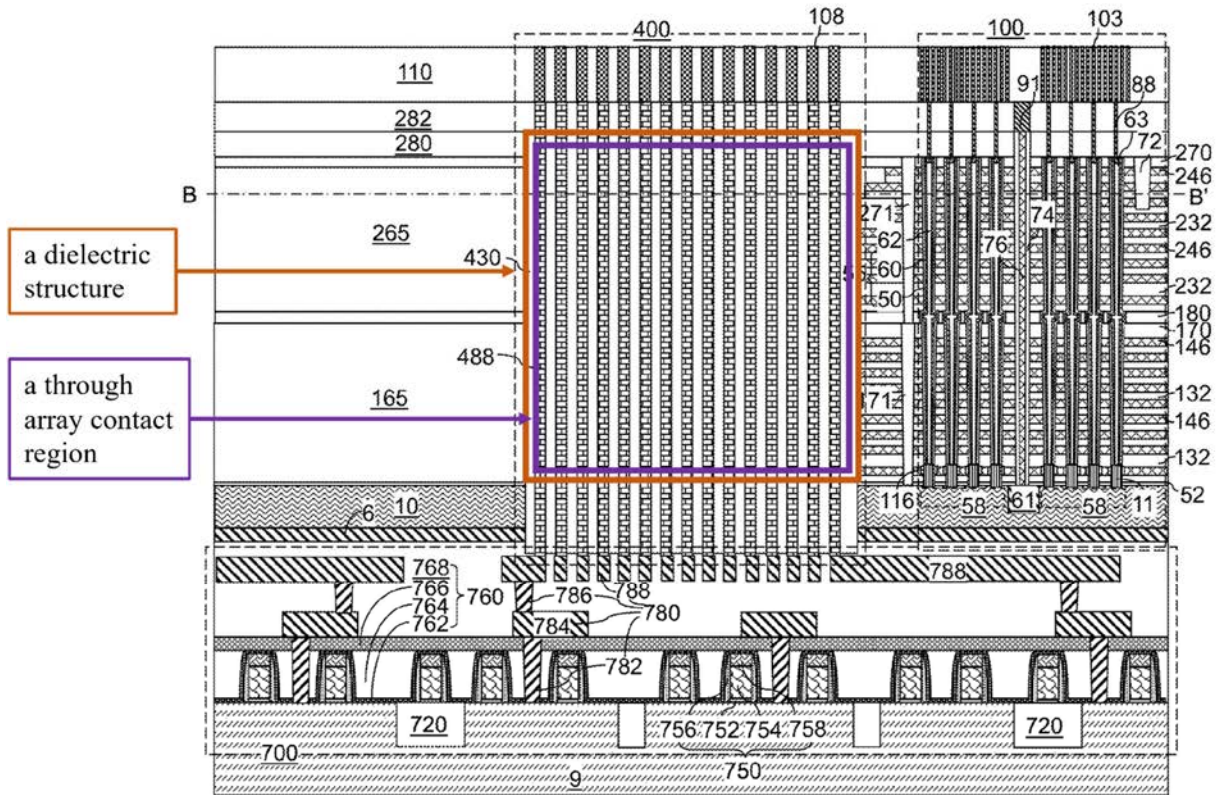
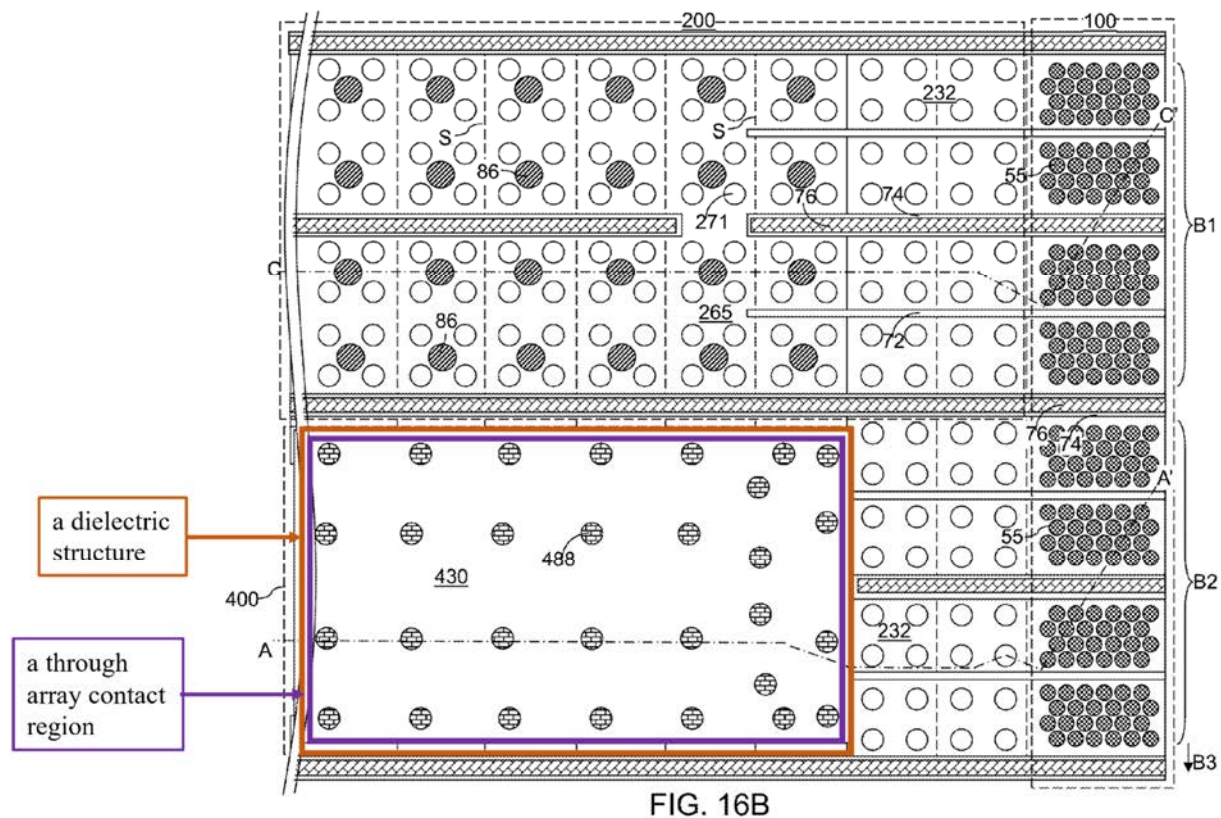


FIG. 17A

Ex. 1005, Fig. 17A (annotated), [0165]-[0167]. Toyama also illustrates depicts “through-memory-level region 400” in a top view in Fig. 16B, the highlighted portion of which constitutes the claims *through array contact (TAC) region* :



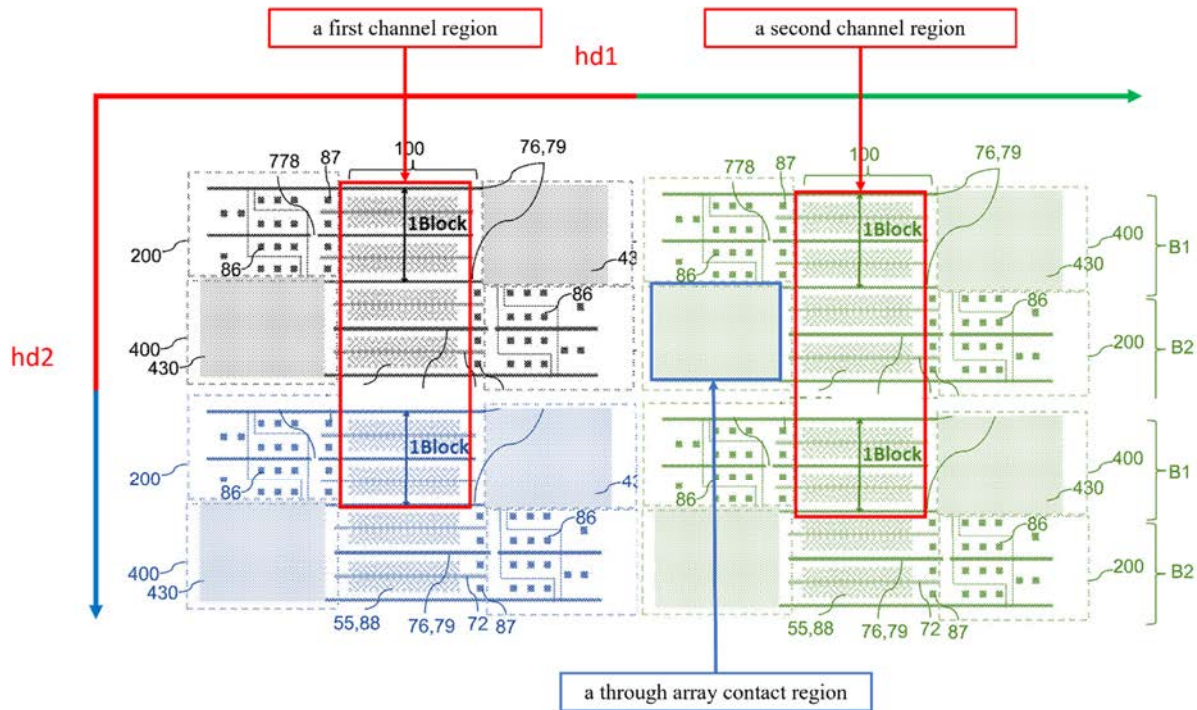
Id., Fig. 16B (annotated).

[8.G.ii] “... formed between the first and second channel regions stack”

196. The first exemplary structure does not expressly disclose that it’s *through array contact (TAC) region* (part of “through-memory-level via region 400”) is *formed between the first and second channel regions*. However, the obvious multi-plane modification to Toyama’s first exemplary structures satisfies the *formed between* requirement.

197. As I discussed in connection with element [8.C], a POSITA would have found it obvious to implement multiple planes of Toyama’s first exemplary structure in the hd1 direction, resulting in the configuration shown below. As identified in the

modified figure below, Toyama’s multi-plane modification has *a through array contact (TAC) region* (part of “through-memory-level via region 400”) *formed between the first and second channel regions* (first and second “memory array regions 100”):



Ex. 1005, Fig. 17E (modified).

[8.H] “a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.”

198. For ease of analysis, I separate this limitation into two sub-parts and address how Toyama’s first exemplary structure teaches each in turn.

a. “a plurality of non-electrically functional channel structures”

199. In Toyama’s first exemplary embodiment (including its obvious multi-plane modification), the “first-tier support pillar structures 171” and “second-tier

support pillar structures 271” disclose, or at least render obvious, *a plurality of non-electrically functional channel structures*, as shown in the cross section of Fig. 17A and top view of Fig. 16B.

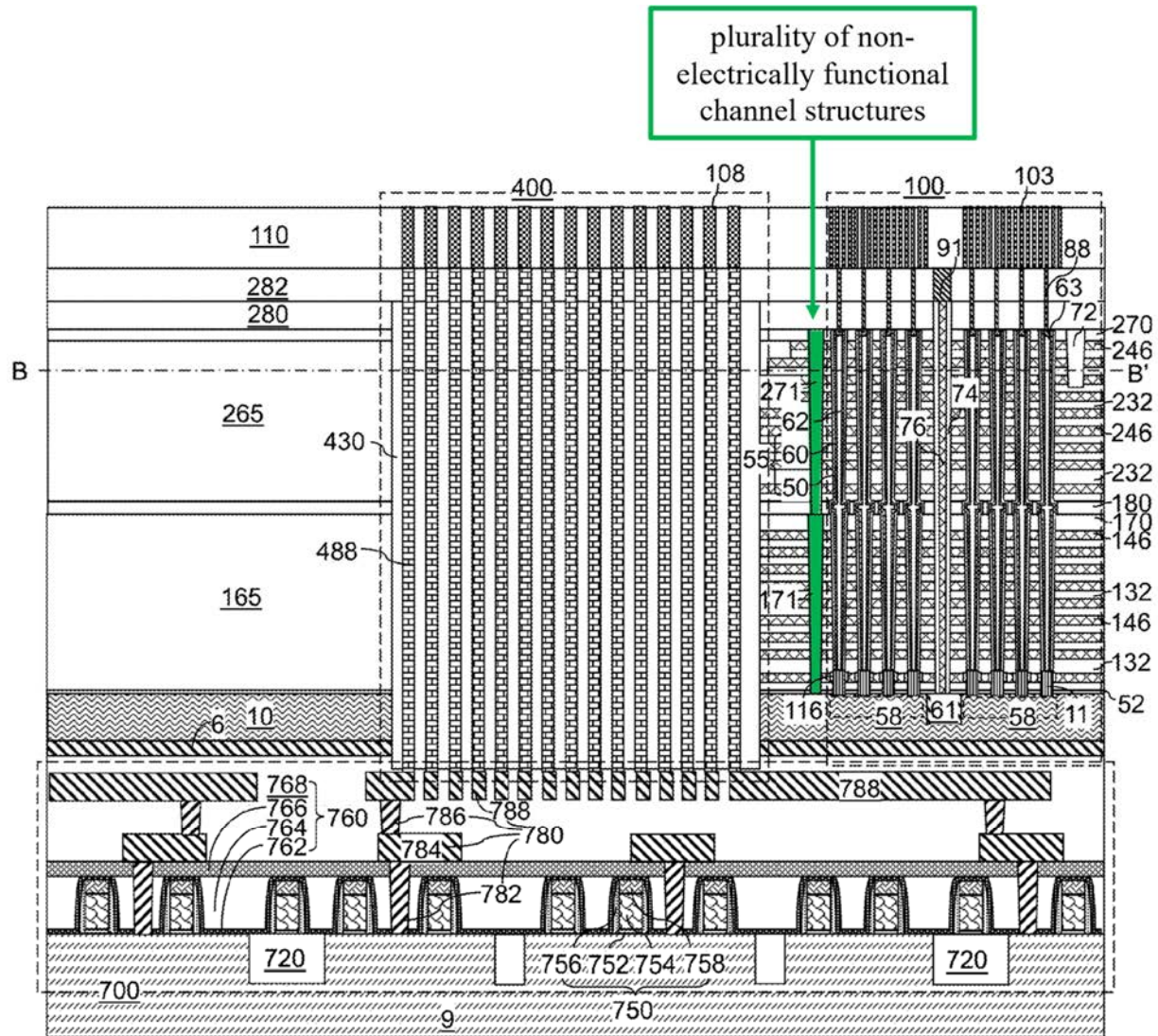
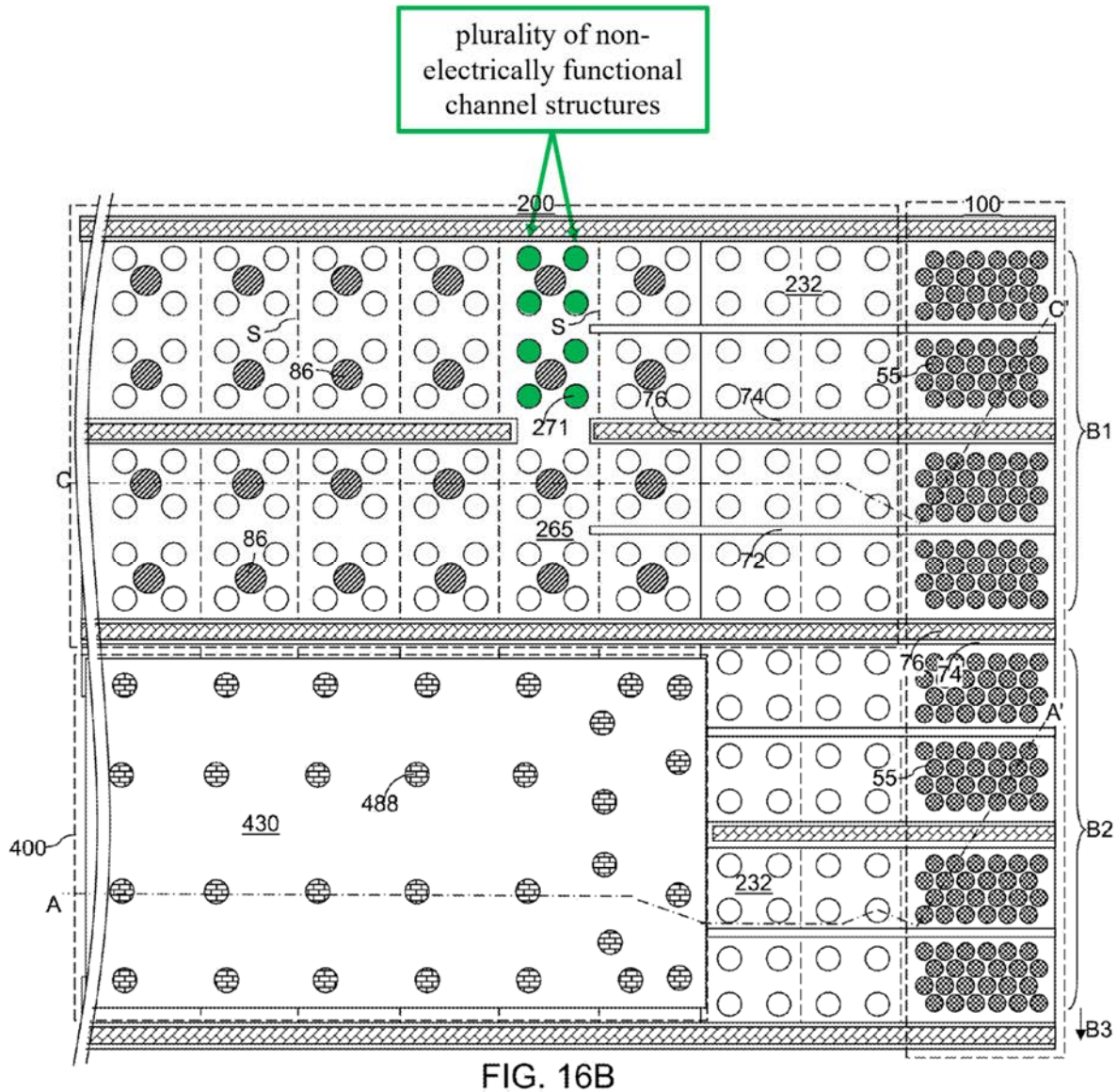


FIG. 17A



Ex. 1005, Figs. 17A, 16B (annotated), [0182], [0197].

200. Toyama discloses that “first-tier support pillar structures 171 are formed ... at the same time [that] the memory stack structures 55 are formed in the memory openings 49.” Ex. 1005, [0203]. “In this embodiment, the first-tier support pillar structures 171 ... comprise dummy memory stack structures which are not electrically connected to bit lines.” *Id.* A POSITA would have understood that

Toyama’s “dummy memory stack structures” are *non-electrically functional channel structures*.

201. Claim 8 is an apparatus claim, not a method claim. As such, it places no restriction on *how* or *when* the *non-electrically functional channel structures* are formed. Nevertheless, I note that the ’806 patent forms its non-electrically functional channel structures 122 in the same way as Toyama’s “dummy memory stack structures” (*i.e.* using the same process step as for the functional channel structures, except no local contacts are formed on top of the dummy channel structures). See Ex. 1001, 6:22-23, 14:36-49. Moreover, the ’806 patent’s “dummy channel structures” provide “mechanical support” to the device, just like Toyama’s “dummy memory stack structures.” *Id.*

202. While Toyama’s “second-tier support pillar structures 271” are not expressly stated to be “dummy memory stack structures,” a POSITA would have understood them to be so. A POSITA would have understood that Toyama forms its first and second tiers of “support pillar structures” 171, 271 as “dummy memory stack structures” at the same time and using the same process steps as Toyama’s “memory stack structures 55.” Indeed, forming the structures separately using different process steps would make little sense and be inefficient.

203. At a minimum, forming Toyama’s “support pillar structures” 171, 271 as dummy memory stack structures would have been obvious to a POSITA, not just

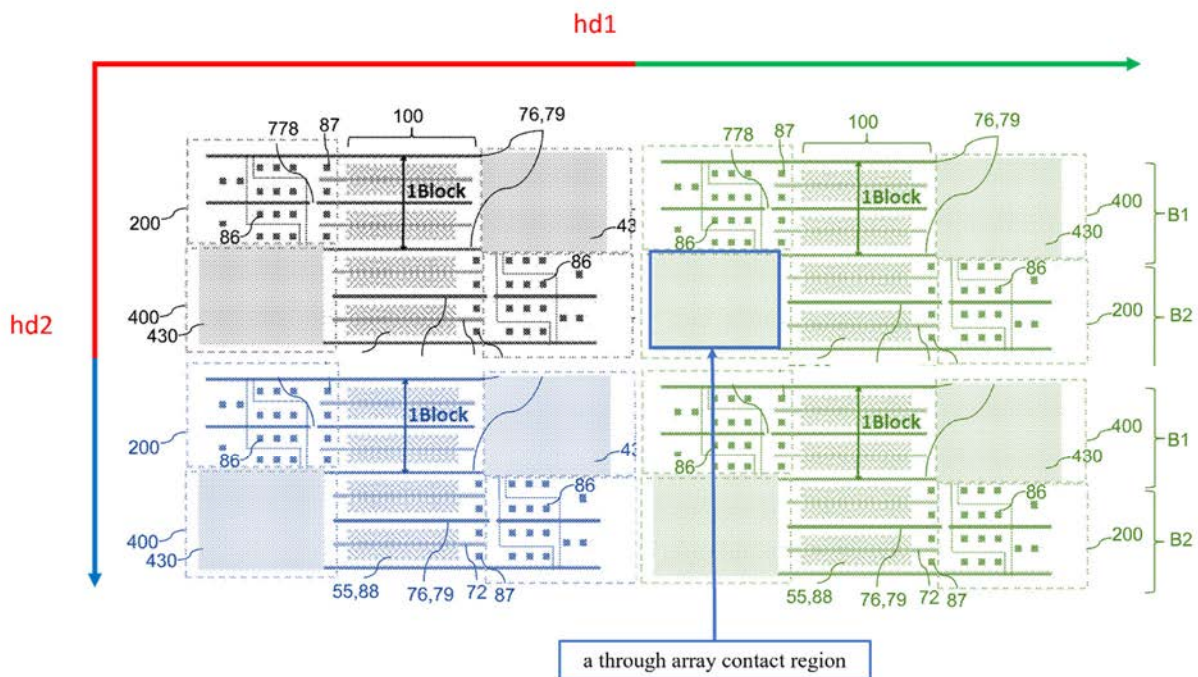
from Toyama, but also from the general knowledge of a POSITA. A POSITA would have known how to create support pillar structures by depositing the components of memory stack structures and how to make them *non-electrically functional* simply by not connecting those structures to anything. *See, e.g.*, Ex. 1005, [0311] (“dummy memory stack structures” can be formed “for structural support”); Ex. 1016 (U.S. Pat. Publ. No. 2019/0229125), [0162] (“support pillar structure” includes same components as “memory stack structure”); Ex. 1017 (U.S. Pat. No. 10,354,980), 9:50-67 (“support pillar structures” includes same components as “memory stack structures”); Ex. 1015 (U.S. Pat. Publ. No. 2018/0108671), [0073]-[0081] (“memory openings 49” and “support openings 19” are filled with the same materials).

204. The motivation to form *non-electrically functional channel structures* (“dummy memory stack structures”) comes from the structural support they provide to the surrounding regions and the fact they the dummy structures can be formed using the same process steps which are already necessary to form the functional *channel structures* (“memory stack structures”). And a POSITA would have had a reasonable expectation of success because of the numerous references (including Toyama itself) that disclose techniques for forming dummy memory stack structures.

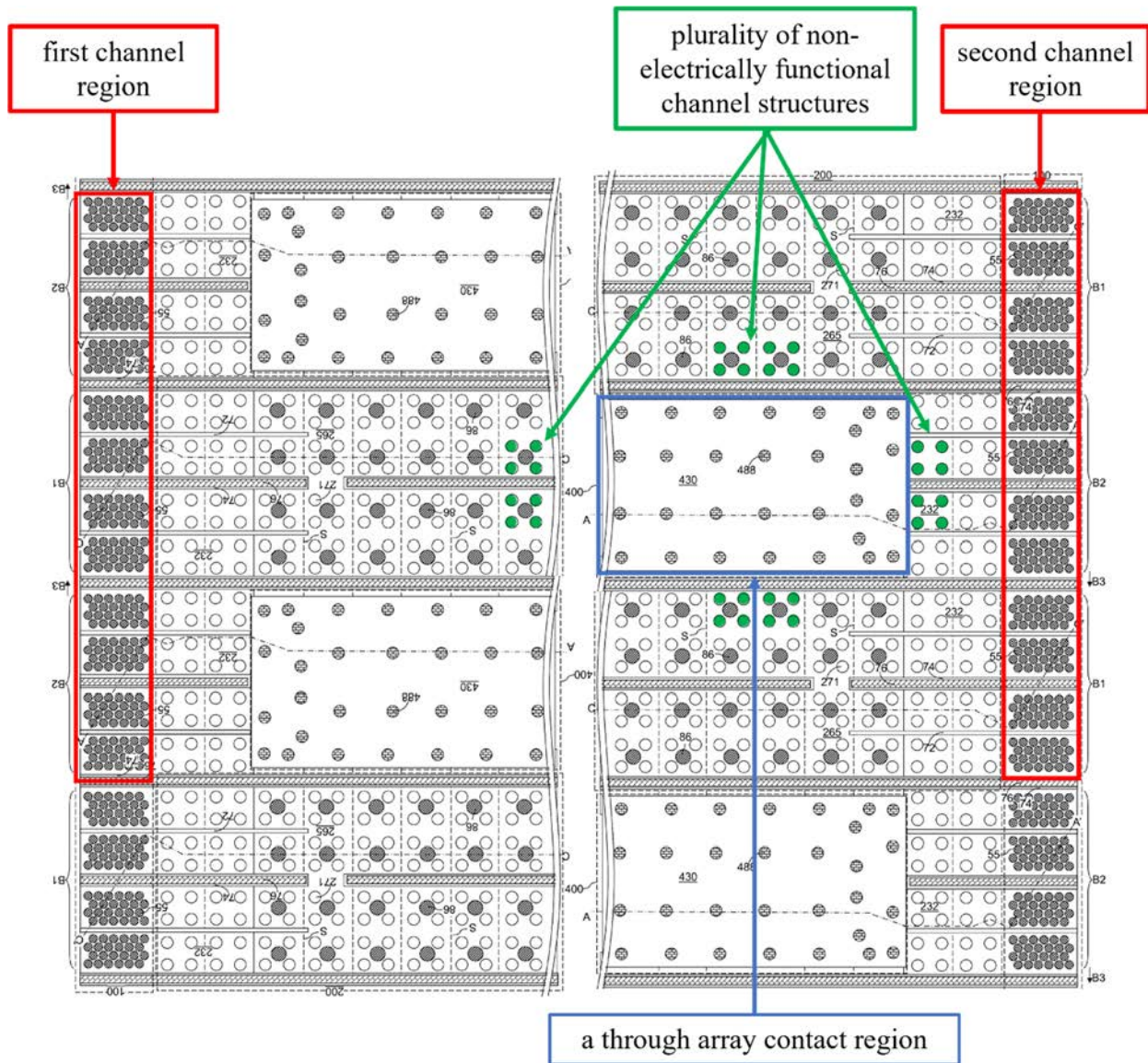
205. Toyama thus discloses (or at least renders obvious) this limitation.

b. “... surrounding the TAC region and between the first and second channel regions”

206. The obvious multi-plane modification to Toyama’s first exemplary structure satisfies this limitation. As I discussed in my analysis for element [8.C], a POSITA would have found it obvious to implement multiple planes of Toyama’s first exemplary structure by adding more instances of Fig. 17E in the hd1 direction, as shown in the modified figure below:



Ex. 1005, Fig. 17E (modified). Reflecting this same multi-plane modification to the view shown in Fig. 16B produces the layout below. I emphasize here that this is the *same multi-plane modification*, not a new or different modification, that I have previously discussed in connection with element [8.C].



2. Claim 10

[10.Pre] “The 3D memory device of claim 8, further comprising:” [10.A] “a substrate”

207. In Toyama’s first exemplary structure, as I explained earlier for Toyama’s Second Modification, the *substrate* is the “planar semiconductor material layer” 10, highlighted in Fig. 17A below. See, e.g., Ex. 1005, [0169]-[0170].

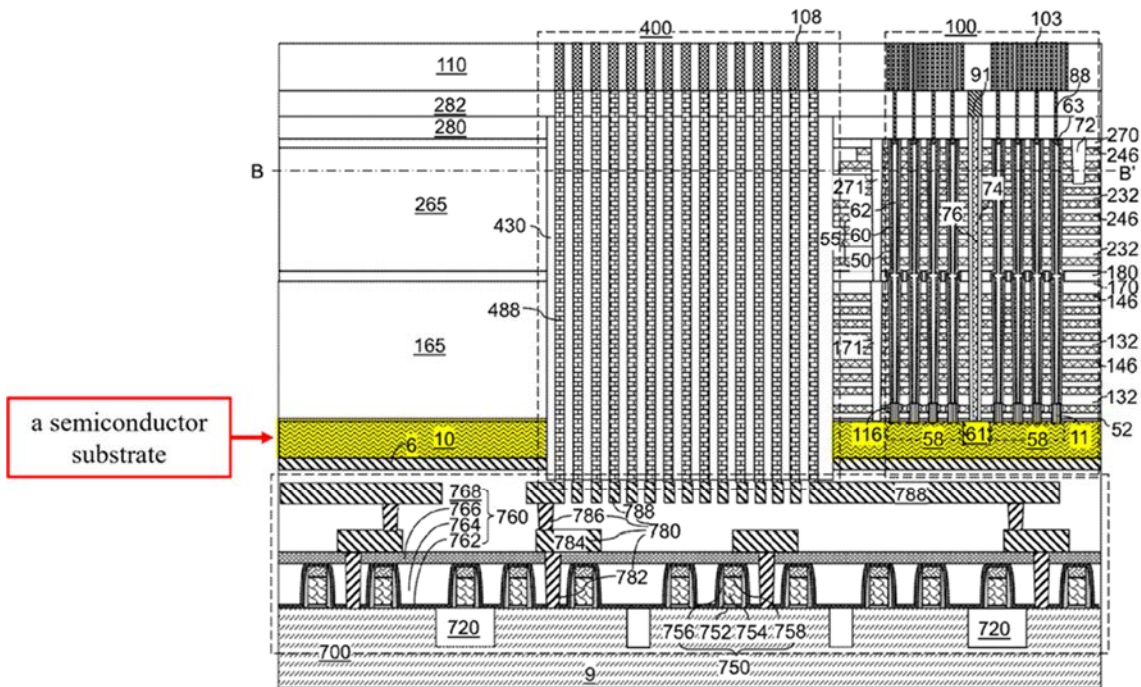


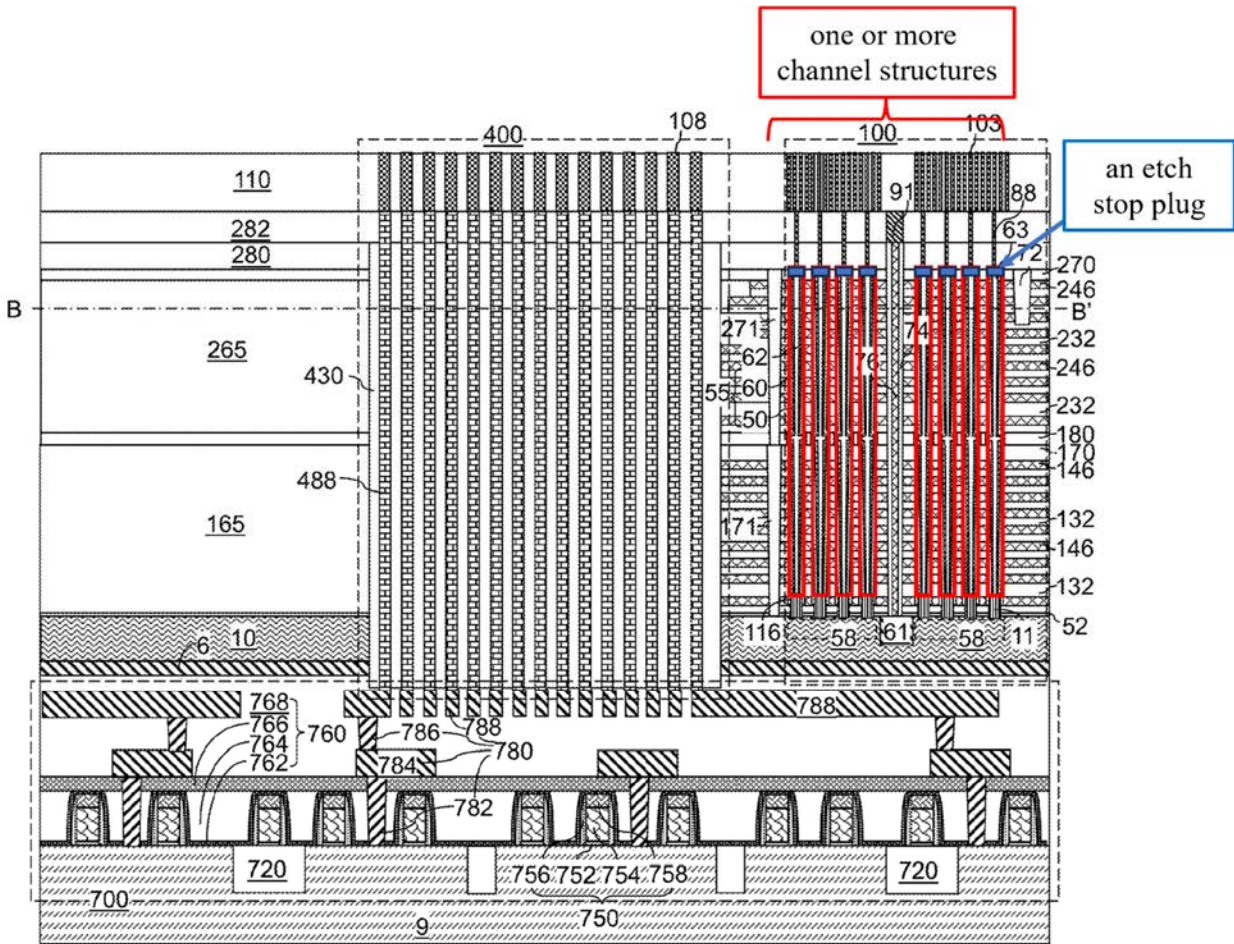
FIG. 17A

Id., Fig. 17A (annotated). Toyama Figs. 2 through 17 depict how various layers are disposed on top of “planar semiconductor material layer 10.” As one example, Toyama notes that “[a]n alternating plurality of the first insulating layers 132 and first sacrificial material layers 142 [are] formed over the planar semiconductor material layer 10.” *Id.*, [0173]. As another example, Toyama explains that “at least one retro-stepped dielectric material portion (165, 265) can be formed over the

staircase regions on the at least one alternating stack (132, 142, 232, 242).” *Id.*, [0196]. Because the “planar semiconductor material layer 10” in Toyama is a semiconductor material onto which other materials and layers are added, it is *a substrate*.

[10.B] “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and”

208. As the below figure illustrates, Toyama discloses or renders obvious *an etch stop plug* (“drain region 63”) interposed *between each local contact of the local contacts* (“drain contact via structures 88”) *and each channel structure of the first and second channel structures* (“memory stack structures 55”):



Ex. 1005, Fig. 17A; Ex. 1001, 4:26-31 (defining “on”).

209. Toyama does not expressly describe “drain regions 63” as “etch stop plugs.” Even so, a POSITA would have understood that drain regions 63 are plugs that serve the purpose of stopping an etch and are therefore *etch stop plugs*.

210. To start, the meaning of the term *plug* in the field of flash memory is consistent with its ordinary meaning, which Merriam-Webster’s dictionary defines as “a piece used to fill a hole.” Ex. 1021, 3. In describing “drain regions 63,”

Toyama explains that “[a] doped semiconductor material ... can be deposited over the dielectric cores 62 and within *the cavities in the memory openings* to form drain regions 63. The doped semiconductor material can be, for example, doped polysilicon. Excess portions of the deposited semiconductor material can be removed from above the top of the second insulating tier cap layer 270 ... to form the drain regions 63.” Ex. 1005, [0209]. Toyama’s “drain regions 63” are thus plugs because they fill the “cavities in the memory openings.” *Id.*

211. For the reasons I explain below, a POSITA would have appreciated that Toyama’s “drain regions 63” are etch stops because they have an *etch stop* function.

212. As Figure 17A shows below, Toyama forms contacts (“drain contact via structures 88”) in the *contact layers on the one or more channel structures* (“memory stack structures 55”) by etching through dielectric layers 280 and 282, and then filling the etched opening with a conductor:

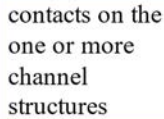


FIG. 17A

Ex. 1005, Fig. 17A. “Drain contact via structures 88 contacting the drain regions 63 can extend through the contact level dielectric layers (280, 282).” *Id.*, [0241]. Toyama further explains that “drain contact via structures 88” “may be formed by employing a respective set of patterning processes and fill processes.” *Id.*, [0241]-[0242].

213. As explained in the background section, above, the process of “patterning” generally involves forming a photoresist layer to protect certain material from etching, etching the exposed material, and then removing the photoresist.

214. A POSITA would thus have understood from Toyama's disclosure that part of the "patterning" process includes a step of etching an opening in dielectric layers 280 and 282. Ex. 1005, [0241]. And a POSITA would have understood from Toyama's disclosure (or at least would have found it obvious) that the dielectric layers 280, 282 would be formed of a dielectric material such as silicon oxide.⁶

⁶ Toyama states that "second contact level dielectric layer 282 includes a dielectric material such as silicon oxide." Ex. 1005, [0238]. Toyama does not expressly state that "dielectric layer 280" is made of silicon oxide, but a POSITA would have understood Toyama to contemplate doing so. At the very least, forming layer 280 of silicon oxide would have been obvious to a POSITA. Toyama expressly notes that "dielectric layer 180" could be made of "a dielectric material such as silicon oxide." *Id.*, [0183]. A POSITA would have understood from Toyama's disclosure that "dielectric layer 280" would similarly be made of silicon oxide, which was a well-known dielectric material with recognized advantages such as being formed easily and using well-practice to techniques. And a POSITA would have found it desirable to form "dielectric layer 280" out of silicon oxide where layer 282 is formed out of silicon dioxide because that would allow a silicon-oxide-selective etchant to etch through both layers.

Whether or not dielectric layers 280, 282 are formed of silicon oxide, however, Toyama contemplates (and a POSITA would certainly have found it obvious, given Toyama's express disclosure of patterning) that a dielectric-selective etchant would be used to form the opening that is ultimately filled by "drain contact via structures 88." As the textbooks and other materials I cite in the background section indicate, such selective etches were well-known and routine to implement.

215. With that context (which a POSITA would have known) in mind, the reason that the "drain regions 63" serve as *an etch stop* is evident. Namely, without "drain regions 63," the etch to form "drain contact via structures 88" may risk damaging elements of "memory stack structures 55." That is because "memory stack structures 55" may include dielectric elements (e.g., "blocking dielectric layer 51") that are formed of the same materials (e.g., silicon oxide) as layers 280 and 282. Ex. 1005, [0204]. Thus, if the etchant that is used to etch through the dielectric layers 280 and 282 were to contact the memory stack structures, the etchant may damage the dielectric elements in the memory stack structures.

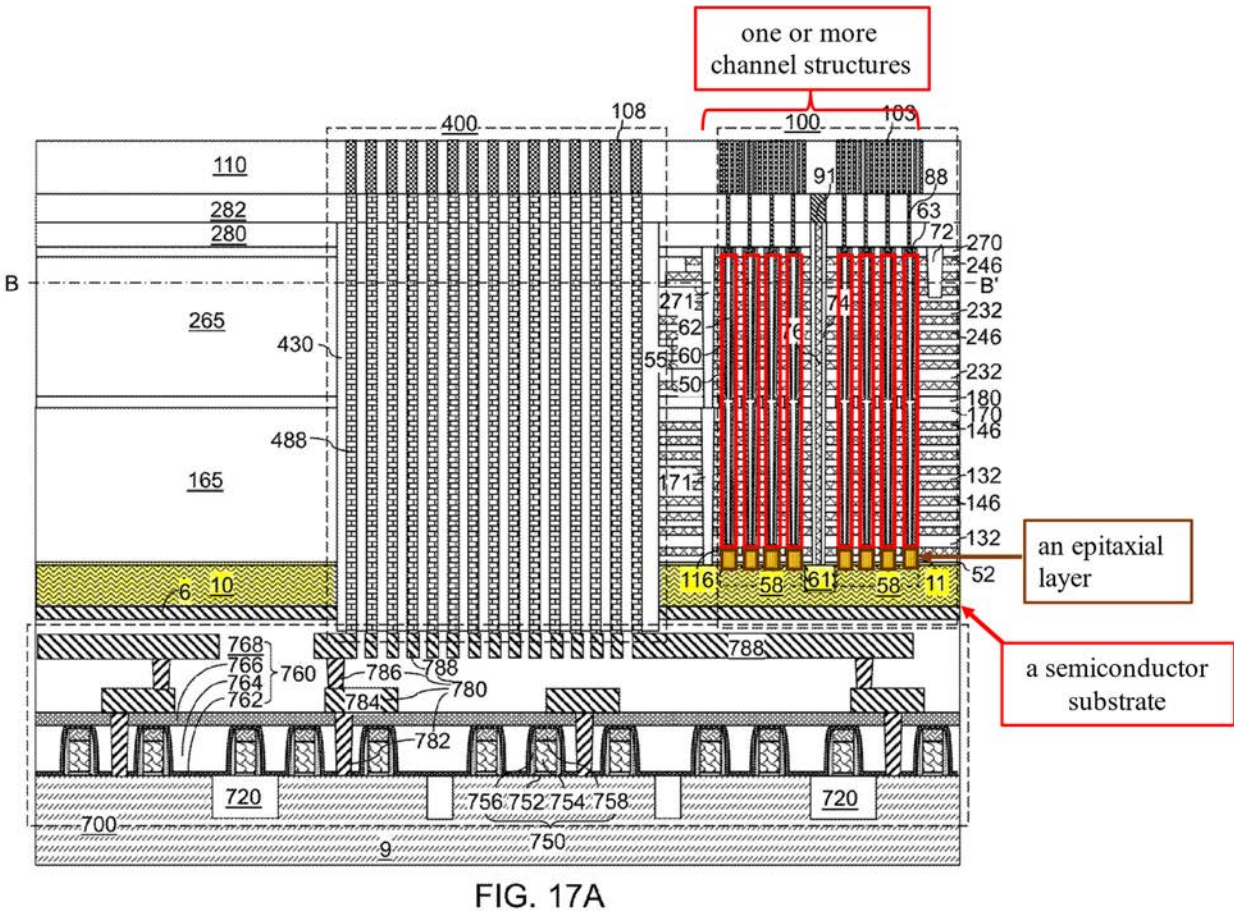
216. "Drain regions 63," which are between the opening that is filled to form "drain contact via structures 88" and the "memory stack structures 55," thus protect "memory stack structures 55" from damage. "Drain regions 63" function as an etch stop because they are made of a material like doped polysilicon, which a POSITA would have understood would **not** react significantly with the etchant used to

selectively etch the dielectric layers 280 and 282. Carbon tetrafluoride (with hydrogen) is one such etchant that etches silicon oxide but does not appreciably etch polysilicon. Ex. 1029 (Chang, ULSI Technology), 363-364. Even if the etchant were to remove a portion of “drain regions 63,” the thickness of “regions 63” acts as a buffer, so that the etchant might partially etch and stop before etching through to the memory elements. Thus, “drain regions 63” serve to protect the dielectric materials in the memory stack from the etching process used to form “drain contact via structures 88.” In other words, because “drain regions 63” effectively stop the etch that ultimately forms the holes for “drain contact via structures 88,” each of “drain regions 63” is *an etch stop plug* that beneficially protects the channel structure.

[10.C] “an epitaxial layer disposed between the substrate and the first or second channel structures.”

217. As I explained above in limitations [8.C] and [10.A], respectively, Toyama discloses *channel structures* (“memory stack structures 55”) and *a substrate* (“planar semiconductor material layer 10”).

218. Toyama further discloses or renders obvious *an epitaxial layer* (“pedestal channel portions 11”) *disposed between the substrate* (“planar semiconductor material layer 10”) *and the first or second channel structures* (“memory stack structures 55”), as shown in Fig. 17A below:



Ex. 1005, Figure 17A, [0208].

219. Toyama also refers to “pedestal channel portions 11” as “epitaxial channel portions 11,” which a POSITA would understand to mean that “pedestal channel portions 11” are formed epitaxially. Ex. 1005, [0202], [0208]. Indeed, a POSITA would have found Toyama’s description of how it forms “portions 11” to be consistent with an epitaxial process. *Id.*, [0202] (“The selective semiconductor deposition **grows a semiconductor material**. ... During a selective semiconductor deposition process, a reactant (such as silane, dichlorosilane, trichlorosilane,

disilane, etc.) can be flowed into a deposition chamber simultaneously with, or, alternatively with, an etchant (such as hydrogen chloride).”) (emphasis added).

220. At the very least, a POSITA would have found it obvious to form “pedestal channel portions 11” epitaxially, thus rendering obvious the claimed *epitaxial layer*. As I explained in the background section, above, techniques for epitaxy in 3D NAND flash memories were well-known and within the skill of a POSITA. And a POSITA would have known of the benefits of an epitaxial pedestal including improved performance and reliability characteristics. Thus, implementing “pedestal channel portions 11” using epitaxy would be nothing more than applying a known technique (“epitaxy”) to a known device (Toyama) to yield predictable results (e.g., performance and reliability characteristics).

D. Ground 3: Toyama’s First Exemplary Structure and Second Modification to Its Fourth Exemplary Structure in View of the Knowledge of a POSITA

221. In Ground 3, Toyama’s Second Modification is modified so that “through-memory-level via structures” are formed within a unitary dielectric fill material as in Toyama’s first exemplary structure, instead of using the Second Modification’s “insulating liners 674.” See discussion of element [8.G.i] for Ground 1 (Second Modification) and Ground 2 (first exemplary structure). As I discuss below, a POSITA would have been motivated to make the combination with a

reasonable expectation of success and the combination renders the Challenged Claim obvious.

1. **It would have been obvious to a POSITA to form the Second Modification’s “through-memory-level via structures” in a unitary dielectric fill material**
 - a. **Toyama’s first exemplary structure uses a unitary dielectric fill material portion to insulate “through-memory-level via structures”**

222. Toyama’s first exemplary structure expressly discloses that “through-memory-level via structures” can be electrically isolated from the “alternating stack” by a “dielectric fill material portion 430,” as shown in Fig. 17A below.

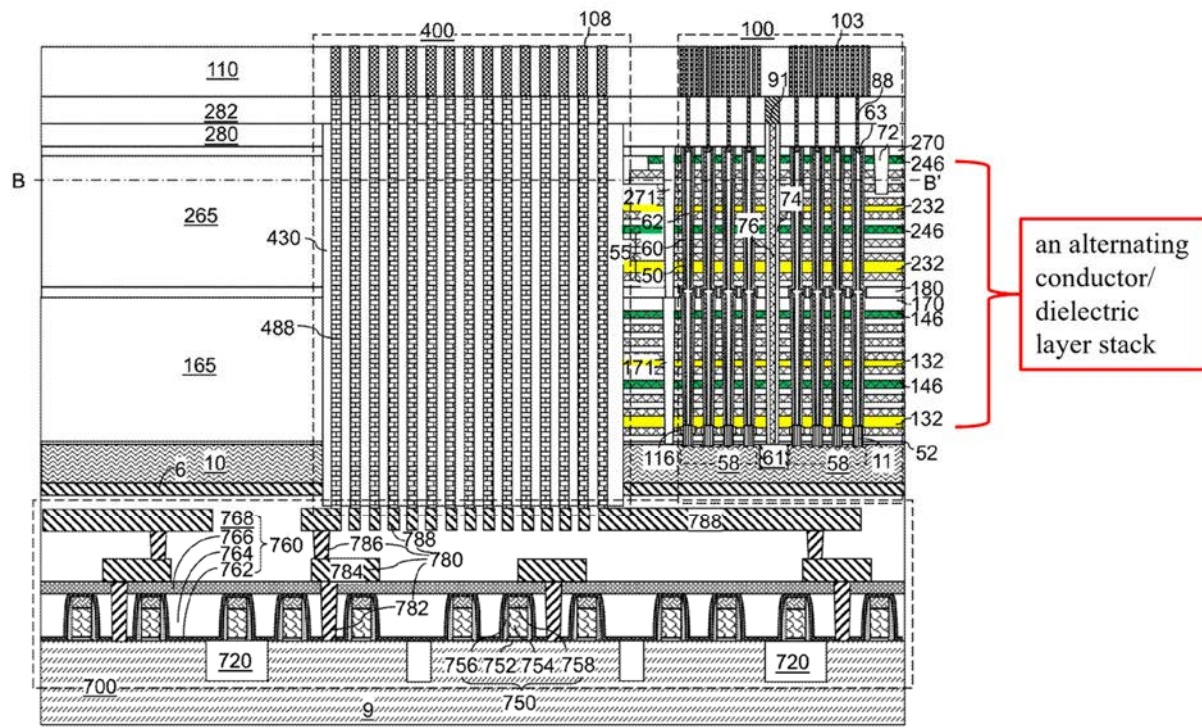


FIG. 17A

Ex. 1005, Fig. 17A (annotated). As a POSITA would have recognized from looking at Fig. 15A, which shows a process formation step prior to Fig. 17A, the “dielectric fill material portion 430” in Toyama’s first exemplary structure is a unitary dielectric fill material.

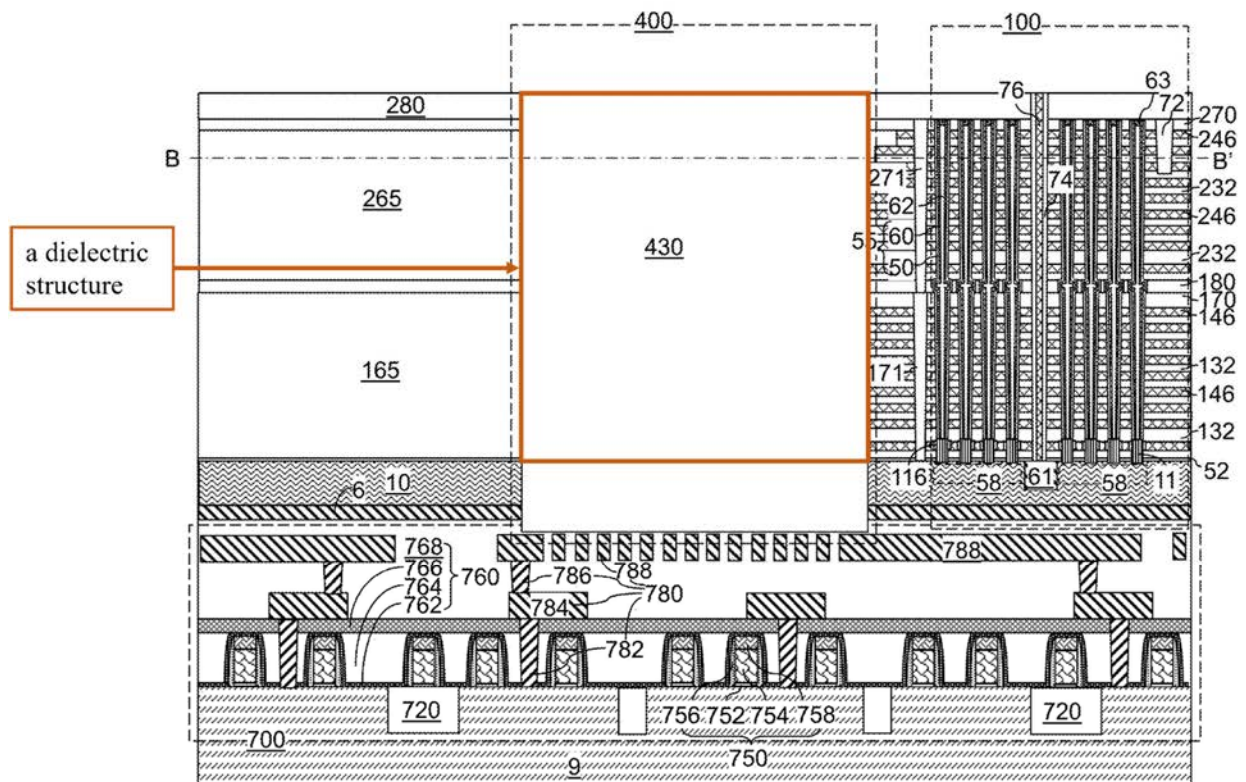


FIG. 15A

Id., Fig. 15A (annotated). Moreover, it was generally known in the art to insulate conductive elements (such as “through-memory-level via structures”) using a unitary dielectric fill material. *See, e.g.*, Ex. 1028 (U.S. Pat. No. 9,935,050), Figs. 12A, 13A, 14A.

b. The obviousness combination

223. Toyama’s Second Modification expressly discloses that its “through-memory-level via structures 676” extend vertically through the “alternating stack” and are electrically isolated from the alternating stack by “insulating liners 674,” as shown in Fig. 49 below. *See generally* Ground 1 discussion of element [8.G.iii].

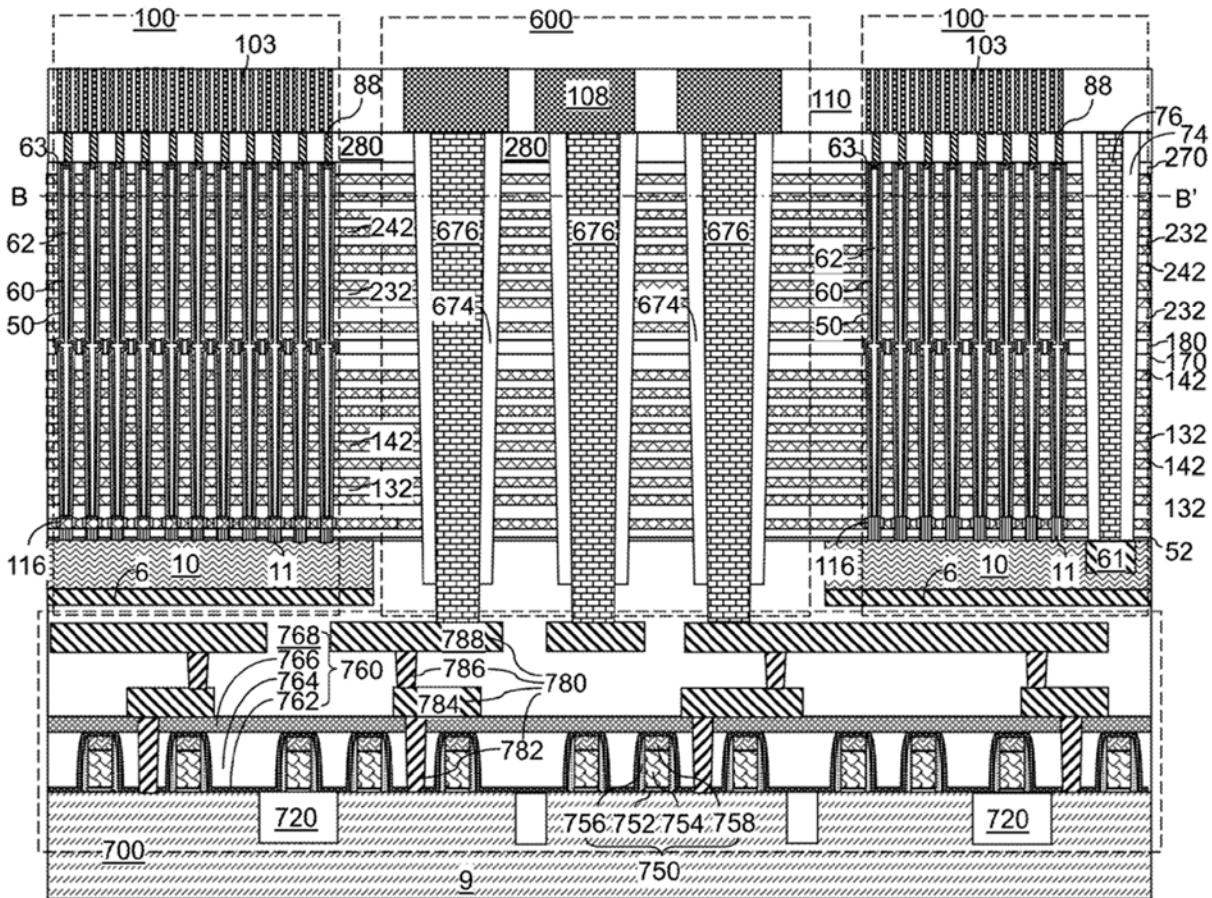


FIG. 49

Ex. 1005, Fig. 49. Toyama's Second Modification serves as the baseline structure for the obviousness combination.

224. It would have been obvious to a POSITA to modify Toyama's Second Modification to electrically isolate its "through-memory-level via structures 676" with a unitary dielectric fill material, as taught by Toyama's first exemplary structure. Below is a side-by-side comparison showing the modified and unmodified versions of Fig. 49.

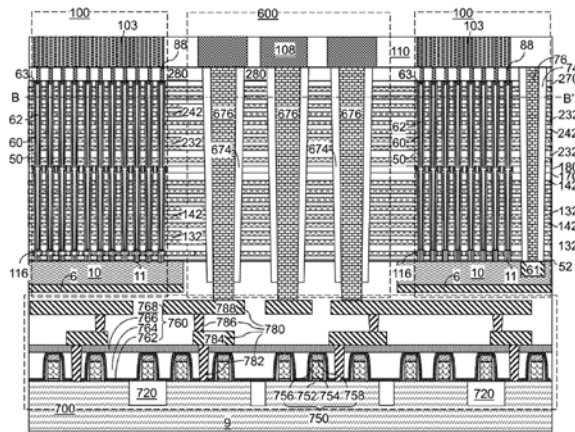


FIG. 49

Unmodified

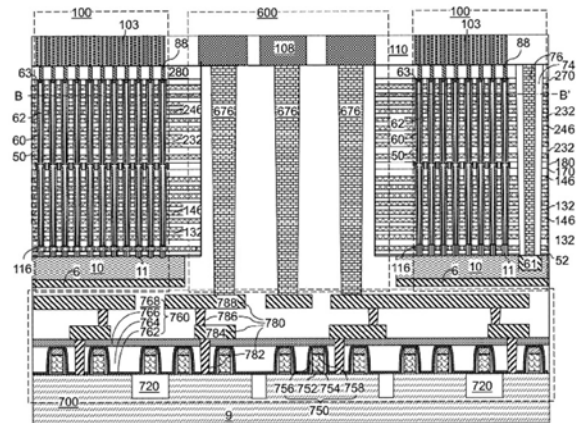


FIG. 49

Modified

Ex. 1005, Fig. 49. The modified figure also corrects the typographical error I previously discussed concerning the numbering of the alternating conductor/dielectric layer stack and the sacrificial layers. I also present below unmodified and modified versions of Fig. 48B, which is a top view of the same combination:

Unmodified

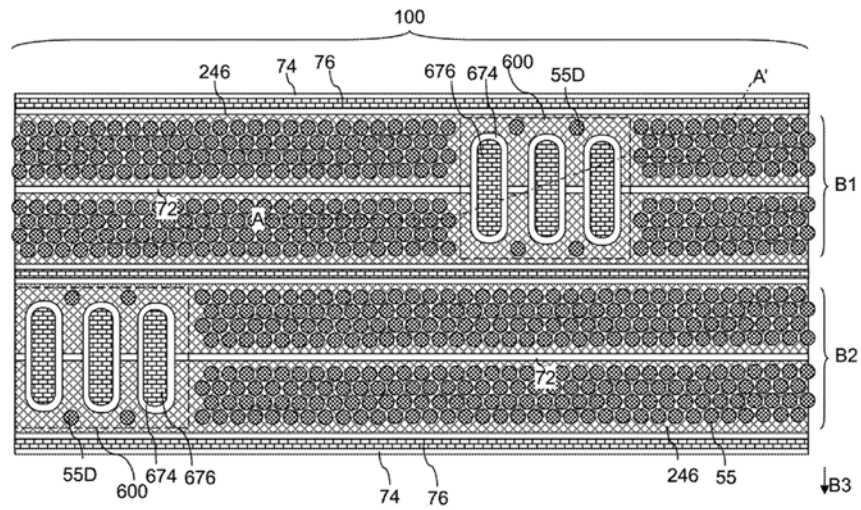


FIG. 48B

Modified

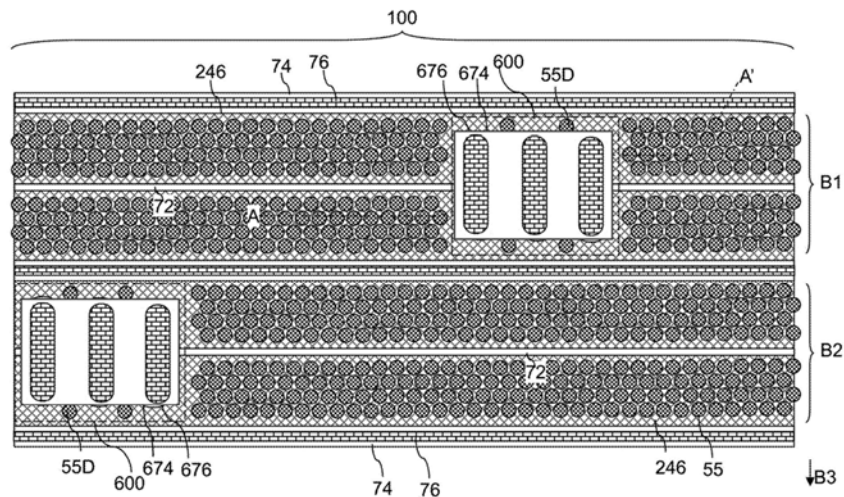


FIG. 48B

Id., Fig. 48B.

225. As I discuss in further detail below, the obviousness combination is merely the substitution of one element (*viz.*, “insulating liners 674” in the Second Modification) for another known element (the unitary dielectric fill material 430 in Toyama’s first exemplary structure) to yield an expected result (electrically isolating

the Second Modification’s “through-memory-level via structures”). Ex. 1005, Figs. 16B, 48B, [0378].

c. Motivation to combine

226. A POSITA would have been motivated to use a unitary dielectric fill material to surround “through-memory-level via structures 676.” At the outset I note that Toyama discloses that its “fourth exemplary structure,” which the Second Modification is based on, “can be formed concurrently with formation of any of the first, second, and third exemplary structures or modifications thereof,” suggesting compatibility between the embodiments. Ex. 1005, [0310]. Indeed, Toyama’s “fourth exemplary structure illustrated in FIGS. 33A and 33B can be formed employing the same processing steps as the processing steps employed to form the first exemplary structure of FIGS. 10A and 10B.” *Id.*

227. A POSITA would have understood that forming the “through-memory-level via structures” within a unitary dielectric fill material would be desirable because it performs the necessary function of electrically isolating the “through-memory-level via structures.” Otherwise, the “through-memory-level via structures” may electrically interfere with each other (or with other conductive elements of the Second Modification, such as “electrically conductive layers (146, 246)”). Ex. 1005, [0316]. I highlight two particular aspects of this benefit below.

228. **First**, a POSITA would have understood that using a unitary dielectric fill material would reduce *capacitive coupling* compared to the unmodified version of Toyama’s Second Modification. Capacitive coupling (also known as “crosstalk”) occurs where a signal in one conductive element electromagnetically induces a voltage and/or current in a different nearby conductive element. This phenomenon is well-known to POSITAs and is highly undesirable. *See* Ex. 1026 (Lau, Ball Grid Array Technology), 39-40, 64, 77. The amount of capacitive coupling is inversely proportional to the distance between the conductors. Thus, with other things being equal, a greater separation between conductive elements will result in less capacitive coupling and less cross-talk. *Id.*, 39 (“[I]ncreasing the separation of conductors reduces capacitive coupling.”).

229. In Toyama, unwanted capacitive coupling may occur between the “through-memory-level via structures” and “electrically conductive layers (146, 246),” which act as the wordlines that control the gates on the memory cells. This undesirable crosstalk creates electrical noise in both the “through-memory-level via structures” and in the “electrically conductive layers.” Ex. 1026 (Lau, Ball Grid Array Technology), 39. (noting that “electrical noise” caused by “coupling of signals between nearby conductors due to parasitic capacitance” is a “pressing issue” for electrical performance).

230. In Toyama's Second Modification the "through-memory-level via structures 676" are separated from "electrically conductive layers (146, 246)" by "insulating liners 674" and layers 180, 280. *See* Ex. 1005, Fig. 49. While this may function suitably within certain noise tolerance levels, a POSITA would have recognized it is not ideal and there is room for improvement. In this regard, Toyama's first exemplary structure separates its "through-memory-level via structures" from "electrically conductive layers (146, 246)" with a single "dielectric fill material portion 430." *Id.*, *see also id.*, Figs. 17A-B. A POSITA would have appreciated that because Toyama's first exemplary structure includes a unitary "dielectric fill material portion 430" to isolate the "through-memory-level via structures" from the "electrically conductive layers" instead of "liners 674" and layers 180, 280, the first exemplary structure's "through-memory-level via region" would be less susceptible to capacitive coupling between the "via structures" and the "electrically conductive layers" than that of Toyama's Second Modification.

231. **Second**, a POSITA would have found the obviousness modification to provide another benefit over Toyama's first exemplary structure (which expressly discloses using "dielectric fill material portion 430") because it places the "dielectric fill material portion" and "through-memory-level via structures" inside "memory array region 100." One benefit, as a POSITA would have recognized, is that "through-memory-level via structures" would then be located closer to the elements

that use the signals carried by the through-memory-level via structures, reducing signal times and shortening wires used for routing. For instance, a POSITA would have understood that “through-memory-level via structures” can connect “memory stack structures 55” to peripheral devices underneath the memory array that provide control signals to “memory stack structures 55.” Ex. 1005, [0003], [0163], Fig. 49. Additionally, a POSITA would have understood that “through-memory-level via structures” can connect “memory stack structures 55” to a “power distribution network” or to “control signals.” *Id.*, [0361], [0377]. As a POSITA would have known, placing the “through-memory-level via structures” that carry the above-mentioned signals inside of a “memory array region 100”—that is, closer to “memory stack structures 55”—has the benefits of reducing signal propagation delays and electrical losses, thus maintaining signal integrity.

d. Reasonable expectation of success

232. A POSITA would have had a reasonable expectation of success in modifying Toyama’s Second Modification to electrically isolate “through-memory-level via structures 676” with a unitary dielectric fill material. As a general matter, Toyama expressly contemplates modifications to its disclosed embodiments. *See, e.g.*, Ex. 1005, [0273] (“a modification of the second exemplary structure is illustrated,”), [0277] (“third exemplary structure can be derived from the first exemplary structure, the second exemplary structure, or modifications thereof”).

[0296] (“a modification of the third exemplary structure can be derived”), [0325] (“a first modification of the fourth exemplary structure is illustrated”).

233. Toyama’s specification begins with a “exemplary structure” and proceeds to describe various modification thereto, inviting a POSITA to take advantage of relevant teachings from one embodiment and apply them to another. As it relates to the Second Modification in particular, Toyama notes that the “second modification of the fourth exemplary structure can be formed concurrently with the formation of any of the first, second, and third exemplary structures or modifications thereof, or can be formed as a stand-alone structure.” Ex. 1005, [0332].

234. Toyama goes on to further note that “where an embodiment employing a particular structure and/or configuration as illustrated in the present disclosure, it is understood that the present disclosure may be practiced with any other compatible structures and/or configurations that are functionally equivalent provided that substitutions are not explicitly forbidden or otherwise known to be impossible to one of ordinary skill in the art.” Ex. 1005, [0390].

235. Particularly in view of Toyama’s teachings regarding manufacturing steps, a POSITA would have known how to fabricate a device implementing the combination. Toyama discloses step-by-step procedures for how to form “dielectric fill material portion 430” and the “through-memory-level via structures” within it. *See generally* Ex. 1005, Figs. 1A-17F. For instance, Toyama discloses patterning

an opening 769, filling the opening with “dielectric fill material portion 430,” and performing another patterning and fill process to create the through array contacts (“through-memory-level via structures 488”). *Id.*, [0213]-[0216], [0242]. These were run-of-the-mill semiconductor fabrication steps that were well-known processes in the art generally, and in 3D NAND manufacturing specifically.

236. Moreover, Toyama discloses—and a POSITA would have understood—that the elements of Toyama’s Second Modification and its first exemplary structure are compatible with each other. Indeed, apart the respective “through-memory-level via region,” the elements of the first exemplary structure and the Second Modification are largely the same, including, for example: *the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”); *the channel structures* (“memory stack structures 55”); *the slit structures* (“laterally elongated contact via structures 76”); *the staircase structure* (“staircase regions”); *the local contacts disposed on the channel structures* (“drain contact via structures 88”); and *the local contacts disposed on the slit structures* (“source connection via structures 91”). Compare generally claim 8 analysis for Ground 1 and Ground 2.

237. Even as it relates to the “through-memory-level via region,” a POSITA would have understood each embodiment’s structure to serve a similar purpose. The Second Modification’s *through array contacts* (“through-memory-level via

structures 676”), like the first exemplary structure’s *through array contacts* (“through-memory-level via structures 488”), provide the medium through which electrical signals vertically traverse the respective *dielectric structure* in each embodiment. And the Second Modification’s *dielectric structure* (“insulating liners 674), like the first exemplary structure’s *dielectric structure* (the upper part of “dielectric fill material portion 430”), serves to electrically isolate the *through array contacts* (“through-memory-level via structures”) from *the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246).”

238. Toyama describes patterning and filling (which, as I discussed above, are used to form the first exemplary structure’s “through-memory-level via region 400”) in the context of the fourth exemplary structure and its modifications. See, e.g., Ex. 1005, [0314]-[0315], [0318], [0324], [0326], [0334]-[0335]. Thus, a POSITA would have understood that the process steps for forming the relevant structures are compatible. In summary, it would have been straightforward for a POSITA to form a unitary dielectric fill material in Toyama’s Second Modification “through-memory-level region 600,” as well as forming thereafter “through-memory-level via structures 676” in the unitary dielectric.

239. Additionally, the results of the combination would have been predictable. In particular, a POSITA would have understood that a unitary dielectric fill material would achieve the purpose of the Second Modification’s “insulating

liners 674,” viz., to electrically isolate the “through-memory-level via structures 676.” Likewise, the impacts on crosstalk and capacitive coupling were well-understood electrical phenomena I discussed in the previous section.

2. Claim 8

[8.Pre] “A three-dimensional (3D) memory device, comprising:”

240. Toyama’s Second Modification discloses this limitation for the same reasons I discussed for the preamble in Ground 1. Thus, the combination discloses *a three-dimensional (3D) memory device*.

[8.A] “an alternating conductor/dielectric layer stack;”

241. For the same reasons I explained in connection with element [8.A] in Ground 1, the Second Modification’s “alternating stack (132, 146, 232, 246)” is *an alternating conductor/dielectric layer stack*. The combination does not change the Second Modification’s “alternating stack.” As shown below, the combination satisfies this limitation:

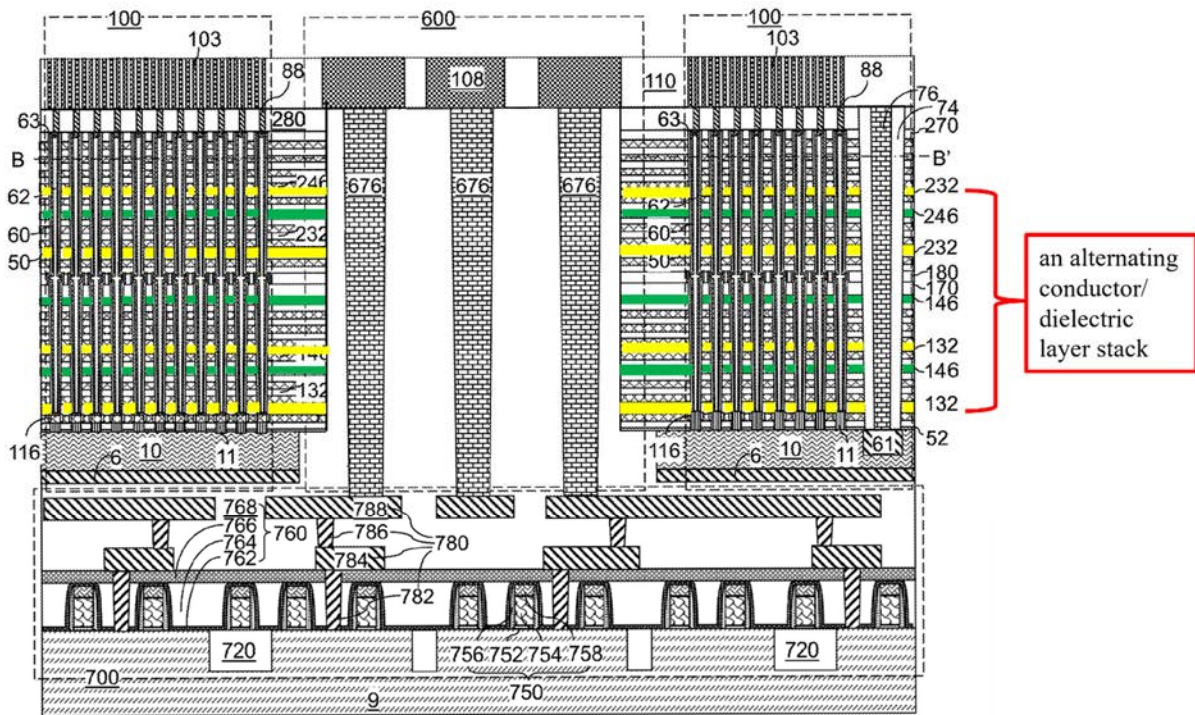


FIG. 49

Ex. 1005, Fig. 49 (modified).

[8.B] “a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;”

242. As discussed, the combination involves applying the first exemplary embodiment’s teach of a unitary dielectric fill material in lieu of the “insulating liners 674” in the Second Modification. The first exemplary embodiment’s unitary dielectric fill material remains *a dielectric structure* when applied to Toyama’s Second Modification.

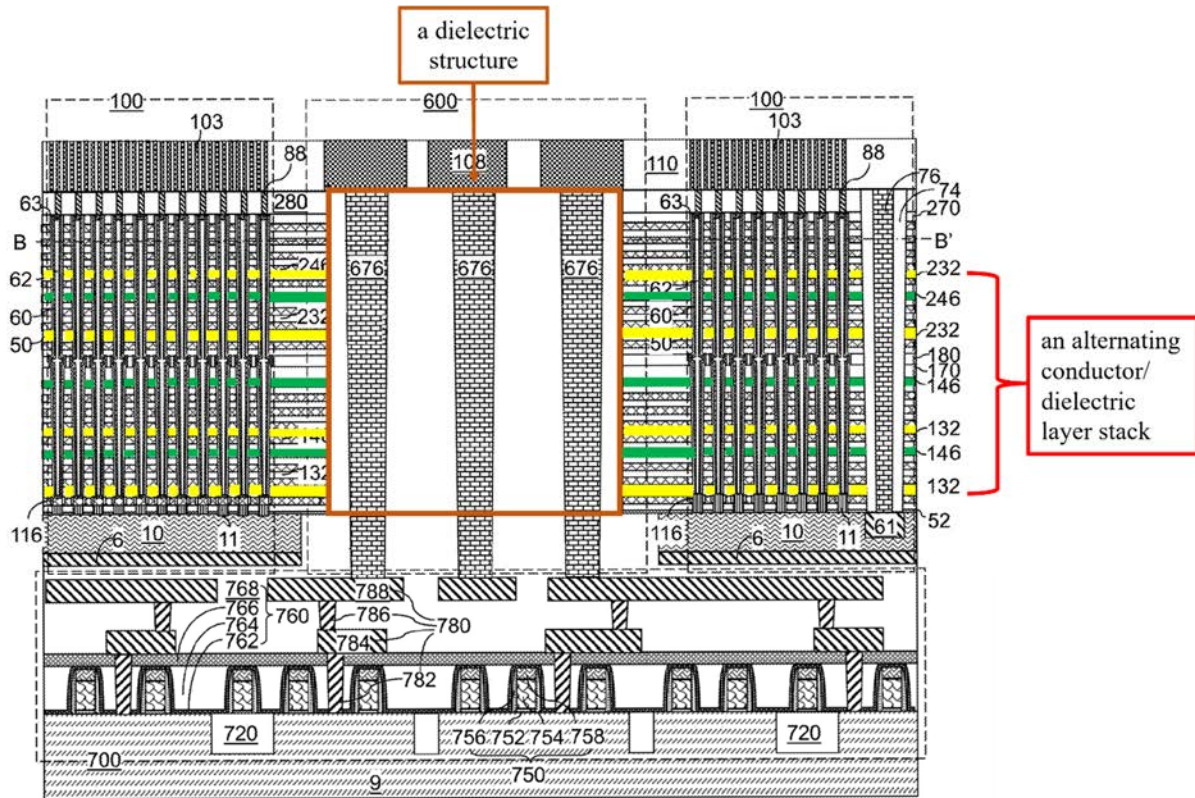


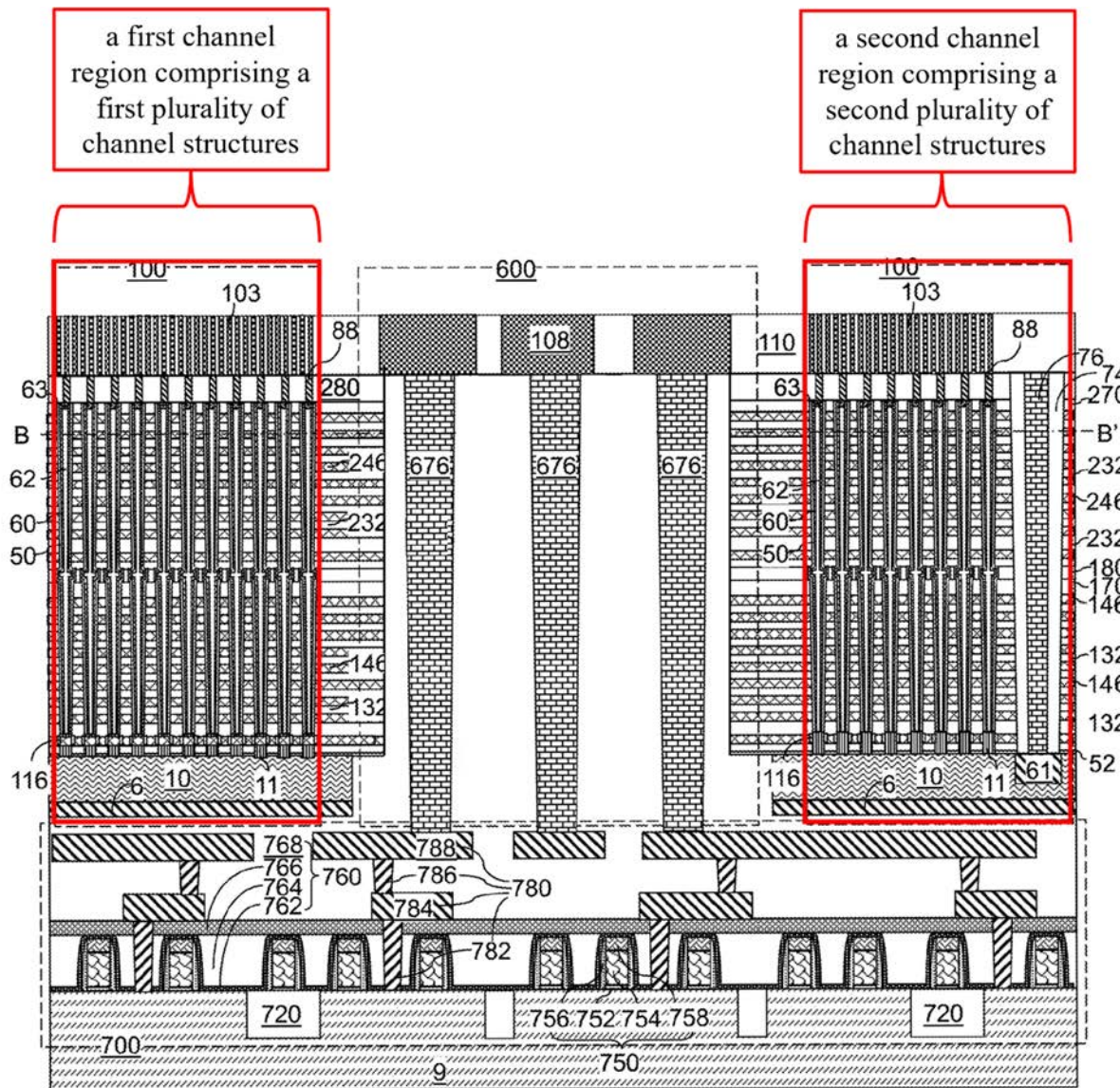
FIG. 49

Ex. 1005, Fig. 49 (modified). And it *extend[s] vertically through the alternating conductor/dielectric layer stack* for the reasons I discussed for element [8.B] in both Ground 1 and Ground 2, and as shown above in the modified version of Fig. 49. Thus, the combination discloses *a dielectric structure extending vertically through the alternating conductor/dielectric layer stack*. See also *Id.*, [0216].

[8.C] “first and second channel regions comprising first and second pluralities of channel structures, respectively;”

243. The obviousness combination does not change the Second Modification’s *first and second channel regions* (first and second parts of “memory array region 100”) *comprising first and second pluralities of channel structures*

(“memory stack structures 55”), which I discussed in connection with claim element [8.C] for Ground 1. Thus, as shown in the modified figure below, the combination satisfies this limitation.



Ex. 1005, Fig. 49 (modified).

[8.D] “slit structures extending vertically through the alternating conductor/dielectric layer stack;”

244. The combination does not change my mapping of the Second Modification’s *slit structures* (“laterally-elongated contact via structures 76”) *extend[] vertically through the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”) as discuss for element [8.D] in Ground 1. Thus, the combination satisfies this limitation for the same reasons.

[8.E] “a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;”

245. As I explained for element [8.E] in Ground 1, Toyama’s Second Modification discloses and/or renders obvious *a staircase structure* (“staircase regions”) *disposed in the alternating conductor/dielectric layer stack* (“alternating stack (132, 146, 232, 246)”), *wherein the staircase structure comprises levels with each level having a conductor layer* (“electrically conductive layers 146, 246”) *thereon*. The combination does not alter this mapping. The combination satisfies this limitation for the same reasons.

[8.F] “local contacts disposed on the first and second channel structures and the slit structures;”

246. As I explained for element [8.F] in Ground 1, Toyama’s Second Modification discloses and/or renders obvious *local contacts* (“drain contact via structures 88”) *disposed on* (above) *the channel structures* (“memory stack

structures 55”), and *local contacts* (“source connection via structures”) *disposed on* (above) *the slit structures* (“laterally-elongated contact via structures 76”). The combination does not alter this mapping. Thus, the combination satisfies this limitation for the same reasons.

[8.G] “[i] a through array contact (TAC) region [ii] formed between the first and second channel regions, [iii] wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and”

247. The combination discloses this element. For ease of analysis, I divide this element into three sub-parts and address each one. I begin my analysis with the last sub-part, as it is helpful to understand what constitutes a *through array contact (TAC)* in Toyama before discussing the *through array contact (TAC) region* limitation.

[8.G.iii] “wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and”

248. I explained in connection with element [8.G.iii] for Ground 1 that the “through-memory-level via structures 676” in Toyama’s Second Modification are the claimed *through array contacts*. And the *dielectric structure* in the combination is a unitary dielectric fill material. See discussion of element [8.B] and Section IX.D.1. Accordingly, in the combination, the *TAC region* (part of “through-memory-level region 600”) *comprises a plurality of through array contacts* (TACs) (“through-memory-level via structures 676”) that *extend[] vertically through the*

dielectric structure (the unitary dielectric fill material), as shown in modified Fig. 49 below:

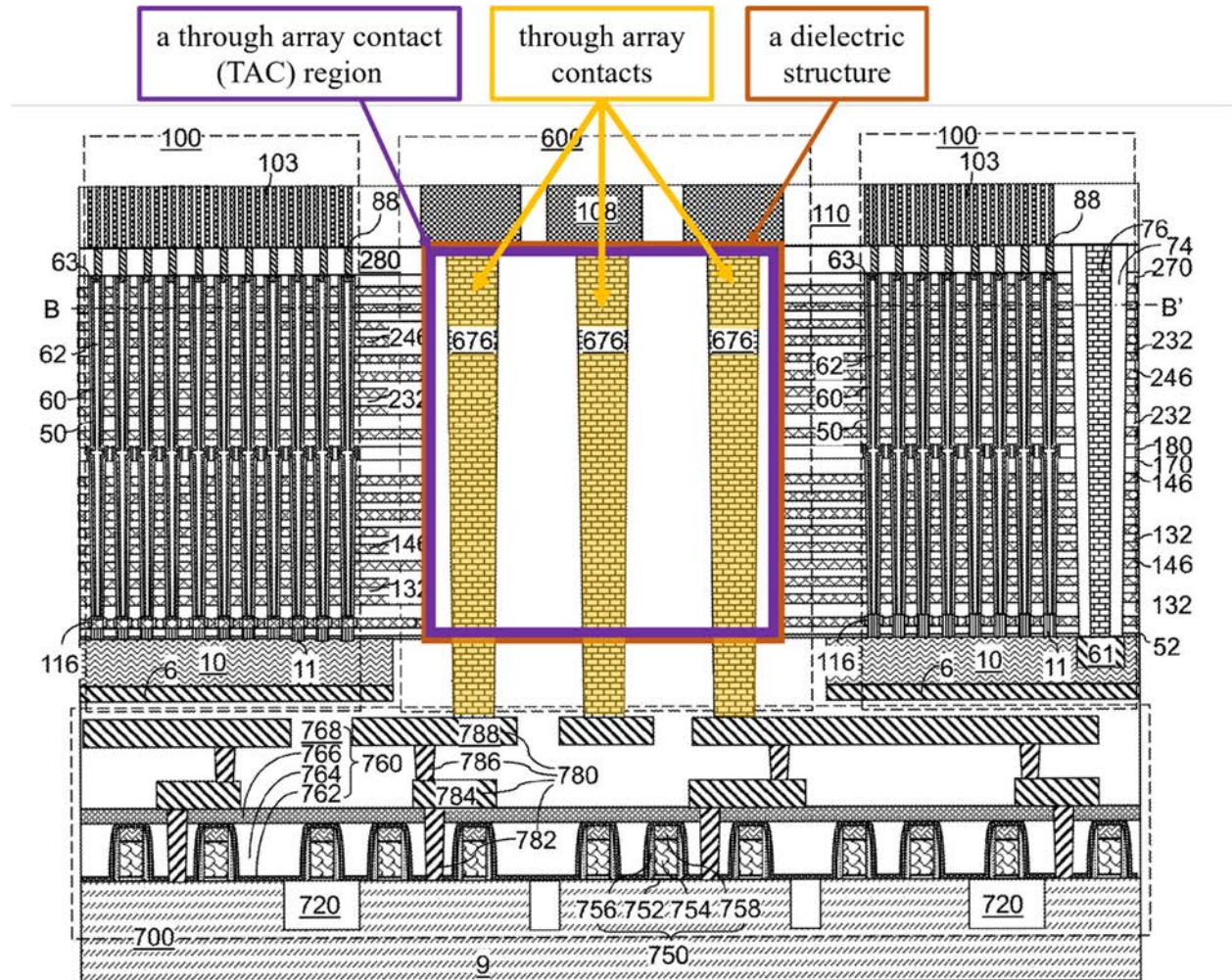


FIG. 49

Ex. 1005, Fig. 49 (modified).

[8.G.i] “a through array contact (TAC) region”

249. In summary, the combination satisfies element [8.G.i]. To being, the ’806 patent discloses that “[i]n some embodiments, dielectric structure 232 defines the boundaries, the shape, and the size of TAC region 120.” Ex. 1001, 10:26-

28. Applying the same approach to the combination, the *through array contact (TAC) region* is the portion of “through-memory-level via region 600” highlighted below in modified Fig. 49 and is defined by the boundaries of Toyama’s *dielectric structure* (unitary dielectric fill material):

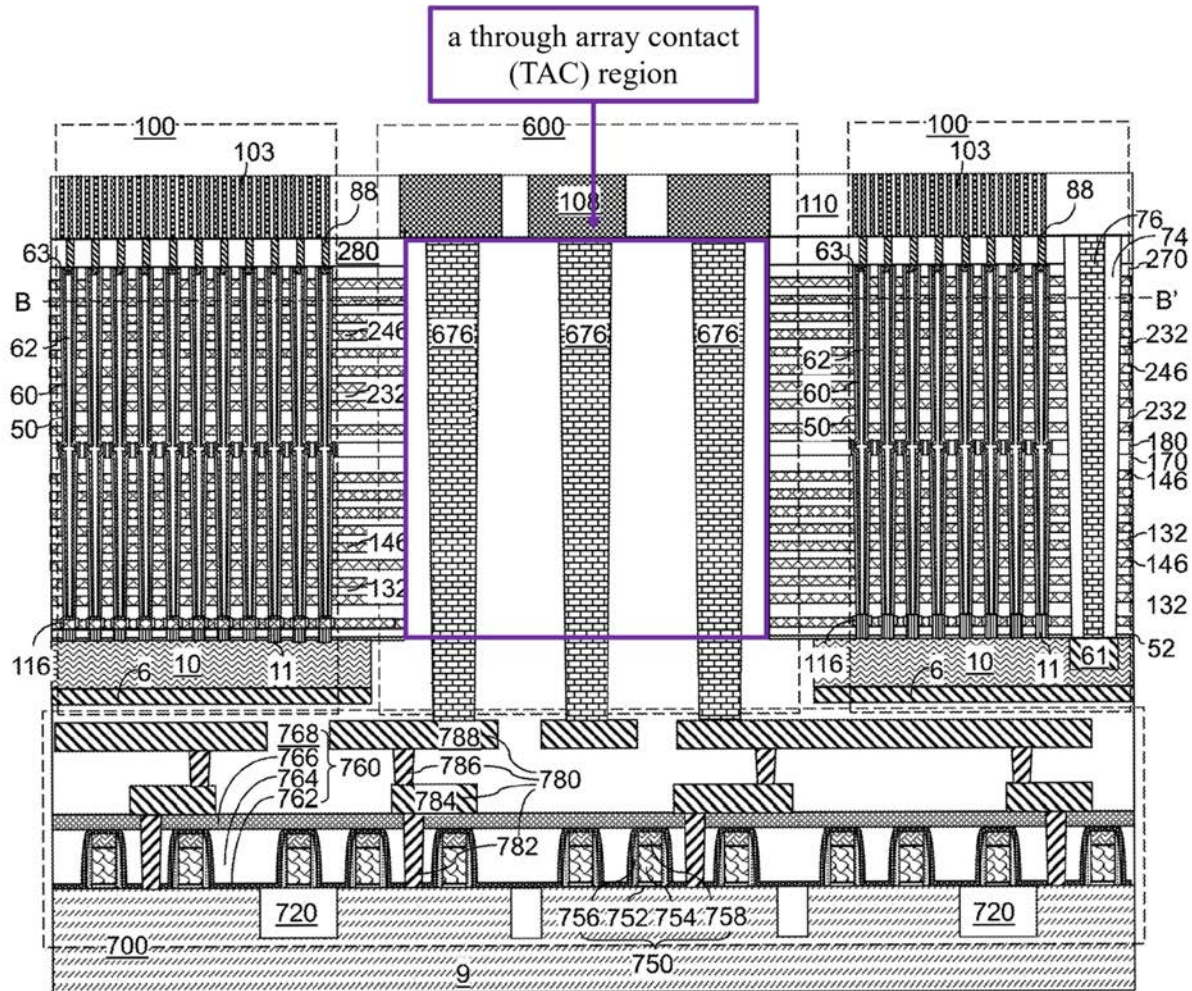


FIG. 49

Ex. 1005, Fig. 49 (modified). The combination is shown in top view below in modified Fig. 48 with the *through array contact (TAC) region* boxed in purple.

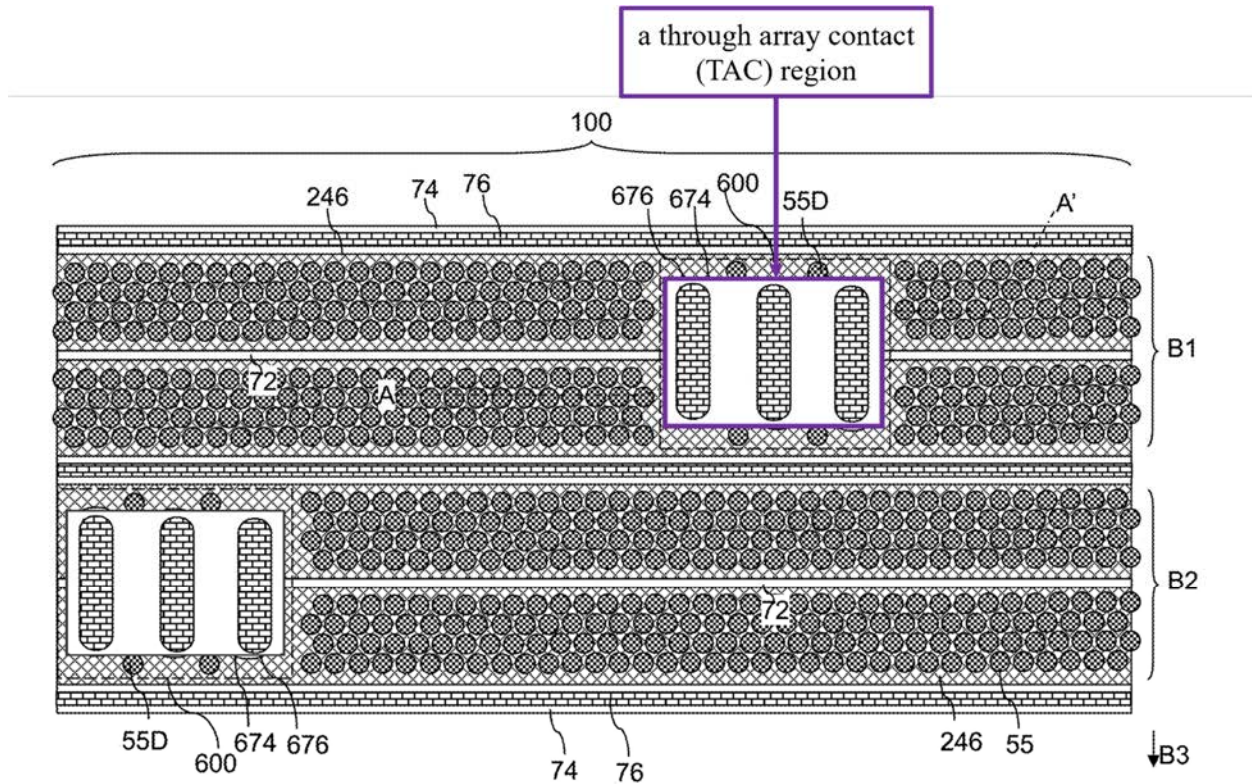


FIG. 48B

Id., Fig. 48B (modified).

[8.G.ii] “... formed between the first and second channel regions stack”

250. As discussed above for limitation [8.C], the combination discloses *first and second channel regions* (first and second parts of “memory array region 100”). Accordingly, the combination’s *TAC region* (part of “through-memory-level via region 600”) is *formed between the first and second channel regions* (first and second parts of “memory array region 100”), as shown in modified Fig. 49 below:

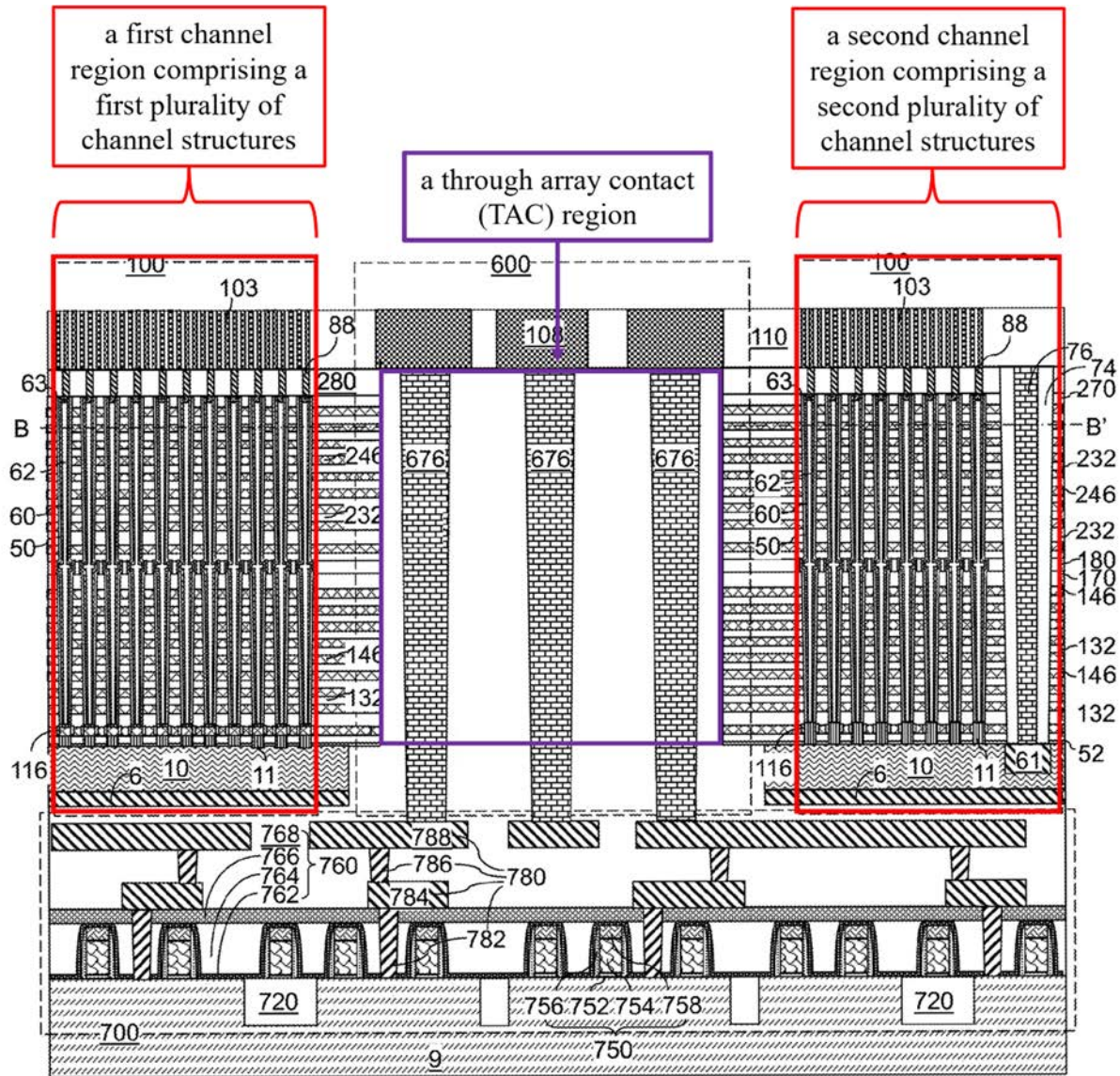


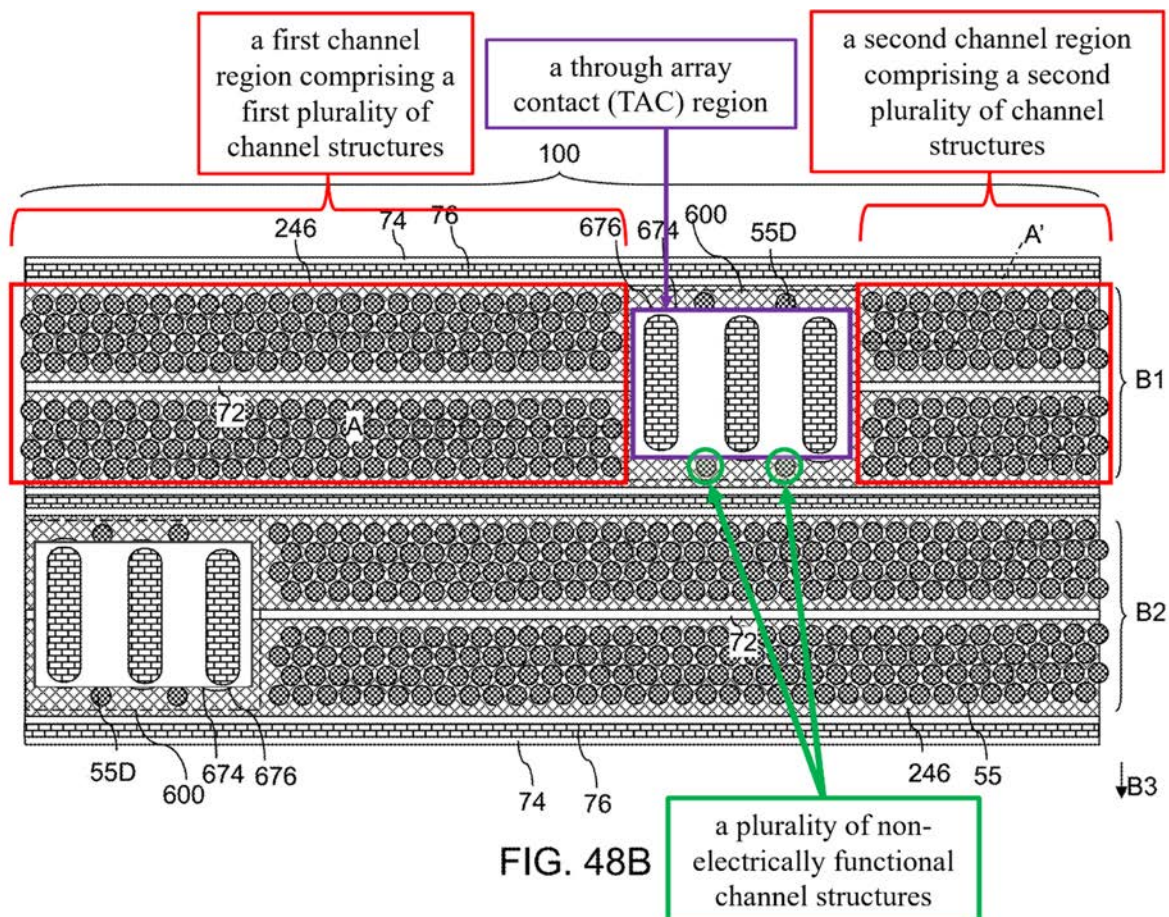
FIG. 49

Toyama, Fig. 49 (modified).

[8.H] “a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.”

251. As I discuss in connection with element [8.B] and Section IX.D.1, the combination involves using a unitary dielectric fill material in place of the Second Modification’s “insulating liners 674” for the claimed *dielectric structure*. The

combination does not change the Second Modification's "dummy memory stack structures 55D." See, e.g., Ex. 1005, Fig. 48B. Accordingly, the combination discloses and/or renders obvious *a plurality of non-electrically functional channel structures* ("dummy memory stack structures 55D") *surrounding the TAC region* (part of "through-memory-level via region 600") *and between the first and second channel regions* (first and second parts of "memory array region 100") for the same reasons I explained in connection with element [8.H] for Ground 1.



Id., Fig. 48B (modified); see also discussion of elements [8.G] (*through array contact (TAC) region*) and [8.C] (*first and second channel regions*).

3. Claim 10

[10.Pre] “The 3D memory device of claim 8, further comprising:” [10.A] “a substrate”

252. The combination does not change my mapping of the Second Modification’s *substrate* (“planar semiconductor material layer 10”) as I discuss for element [10.A] in Ground 1. Thus, the combination satisfies this limitation for the same reasons.

[10.B] “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and”

253. The combination does not change my mapping of the Second Modification’s *etch stop plug* (“drain regions 63”) *interposed between each local contact of the local contacts* (“drain contact via structures 88”) *and each channel structure of the first and second channel structures* (“dummy stack structures 55”), as I discuss for element [10.B] in Ground 1. Thus, the combination satisfies this limitation for the same reasons.

[10.C] “an epitaxial layer disposed between the substrate and the first or second channel structures.”

254. The combination does not change my mapping of the Second Modification’s *epitaxial layer* (“pedestal channel portions 11”) *disposed between the substrate* (“planar semiconductor material layer 10”) *and the first or second channel structures* (“memory stack structures 55”), as I discuss for element [10.C] in Ground 1. Thus, the combination satisfies this limitation for the same reasons.

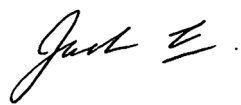
E. Secondary Considerations of Non-Obviousness

255. Based on my review of the '806 patent's file history, I note that no secondary considerations of non-obviousness were identified in connection with the patent's claims. Nor am I otherwise aware of any evidence of commercial success, skepticism, failure of others, industry praise, unexpected results, or the like relating to the '806 patent. Instead, as discussed above, it is my opinion that the subject matter embraced by the Challenged Claim was known in and obvious over the prior art.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: May 19, 2024

Location: Austin, Texas

Signature: 
DR. JACK C. LEE