National Intellectual Property Administration

100140

[redacted]

Issue Date:

November 14, 2019

Application or Patent Number: 201880000655.5 **Issue Serial Number: 2019111101704580**

Applicant or patentee: Yangtze Memory Technologies Co., Ltd.

Invention Name: Through-array Contacts (TACs) for Three-Dimensional Memory Devices

Notice of Opinion of Third Review

1. ☒ The examiner has received the Statement of Opinion submitted by the applicant on August 7, 2019, and on this basis, the examiner continued to conduct substantive examination of the aforementioned patent application.

☐ In accordance with the reexamination decision made by the National Intellectual Property Administration on _____MM _____DD _____YYYY, the examiner continued to conduct substantive review of the aforementioned patent application.

☐ _____

2. ☐ Upon review, the amended documents submitted by the applicant on _____ do not comply with the provisions of Paragraph 3 of Article 51 of the Implementation Rules of the Patent Law and are not accepted.

3. The Continuing Review was conducted on the following application documents:

☐ Amended application documents attached to the above Statement of Opinion.

☒ The application documents on which the previous Notice of Opinion of Review was based and the amended replacement of application documents attached to the above Statement of Opinion.

☐ Application documents on which the previous Notice of Opinion of Review was based.

☐ The application documents determined by the aforementioned re-examination decision.

☐ _____

4. ☐ No new Reference Documents are referenced in this notice.

☒ This notice references the following Reference Documents (its numbers are continued and will continue to be used during future reviews):

Case number	File number or name	Publication date (or date of conflicting application)
2	US 2017179026A1	20170622

5. Conclusive comments from review:

Regarding the Specification:

☐ The content of the application falls within the scope of no patent granting under Article 5 of the Patent Law.

☐ The Specifications does not comply with the provisions of Article 26, Paragraph 3 of the Patent Law.

☐ The modification of the Specifications does not comply with the provisions of Article 33 of the Patent Law.

☐ The writing of the Specifications does not comply with the provisions of Article 17 of the Implementation Rules of the Patent Law.

☐ _____

Regarding the Claims:

☐ The Claims ___do not comply with the provisions of Article 2, Paragraph 2 of the Patent Law.

☐ The Claims ___do not comply with the provisions of Article 9, Paragraph 1 of the Patent Law.

☐ The Claims ___do not possess novelty as prescribed in Article 22, Paragraph 2 of the Patent Law.

Claims 1-32 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

☐ The Claims ___do not possess the practicality specified in Paragraph 4 of Article 22 of the Patent Law.

☐ The Claims ___fall within the scope of no patent granting as stipulated in Article 25 of the Patent Law.

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☐ The Claims ___do not comply with the provisions of Article 26, Paragraph 4 of the Patent Law.
☐ The Claims ___do not comply with the provisions of Article 31, Paragraph 1 of the Patent Law.
☐ The modification _of the Claims does not comply with the provisions of Article 33 of the Patent Law.
☐ The Claims ___do not comply with the provisions of Article 19 of the Implementation Rules of the Patent Law.
☐ The Claims ___do not comply with the provisions of Article 20 of the Implementation Rules of the Patent Law.
☐ The Claims ___do not comply with the provisions of Article 21 of the Implementation Rules of the Patent Law.
☐ The Claims ___do not comply with the provisions of Article 22 of the Implementation Rules of the Patent Law.
☐_____

☐ The application does not comply with the provisions of Article 26, Paragraph 5 of the Patent Law or Article 26 of the Implementation Rules.
☐ The application does not comply with the provisions of Article 20, Paragraph 1 of the Patent Law.
☐ The sub-case application does not comply with the provisions of Paragraph 1 of Article 43 of the Implementation Rules of the Patent Law.
The specific analysis of the above conclusive comments is provided in the body of this notice.

6. Based on the above conclusive opinion, the examiner believes that:
☐ The applicant shall modify the application documents according to the requirements set forth in the body of the notice.
☐ The applicant shall demonstrate in the Statement of Opinion the reasons why its patent application can be granted patent rights and modify the non-compliant sections specified in the body of the notice, otherwise the patent rights cannot be granted.
☒ There is no substantive content in the patent application that can be granted the patent rights, and if the applicant does not state the reasons or the reasons stated are insufficient, its application will be rejected.
☐_____

7. The applicant is advised to pay attention to the following matters:

(1) According to Articles 11 and 12 of the "Administrative Measures for Patent Priority Examination": The deadline for the applicant to reply to the Notice of Opinion on Patent Review is 2 months from the date of issuance of the notice. If the applicant fails to reply within the time limit, the National Intellectual Property Administration may suspend the priority review procedure and handle it according to the ordinary procedure. That is, according to the provisions of Article 37 of the Patent Law, the applicant shall state the opinion within 2 months from the date of receipt of this notice. If the applicant fails to reply within the time limit without justifiable reasons, its application will be deemed to be withdrawn.

(2) The applicant's amendment to the application shall comply with the provisions of Article 33 of the Patent Law and shall not exceed the scope recorded in the original Specifications and Claims. At the same time, the amendment made by the applicant to the patent application documents shall comply with the provisions of Paragraph 3 of Article 51 of the Implementation Rules of the Patent Law and shall be amended in accordance with the requirements of this notice.

(3) The applicant's Statement of Opinion and/or amended text shall be mailed or submitted to the Acceptance Office, the Patent Office, the National Intellectual Property Administration. Any documents not mailed or submitted to the Acceptance Office shall not be binding.

(4) The applicant and/or agent may not come to the National Intellectual Property Administration to meet with the examiner without an appointment.

8. The body of this notice contains a total of 6 pages with the following attachment(s):
☐ A total of _____copies _ pages of the referenced Reference Documents.
☐_____

Examination Department:
Electrical Invention
Examination Department

Examiner: Wang Xiaofeng Contact number: 010-62089918

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Notice of Opinion of Third Review

Application No.: 2018800006555

The examiner has carefully reviewed the Applicant's Statement of Opinion submitted for the previous notice of opinion of review, and the revised application documents, and specifically introduced Reference Document 2. The following examination comments have been made:

1. Claim 1 does not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

Reference Document 2 (US2017/0179026A1) discloses a 3D memory device and specifically discloses (paragraphs 0005-0389 of the Specifications, Figs. 1A-76):

a semiconductor substrate 9; an alternating stacked layer disposed on the semiconductor substrate 9; a dielectric structure 430 extending perpendicularly through the alternating stacked layer, wherein the alternating stacked layer abuts a sidewall surface of the dielectric structure 430, and the dielectric structure 430 is formed of a dielectric material (paragraph 0216-0217 of the Specifications, Figs. 12A-12B); at least two through-array contacts 488, both extending perpendicularly through the dielectric structure 430; and one or more channel structures extending perpendicularly through the alternating stacked layer.

It can be understood that the distinguishing feature of this claim relative to Reference Document 2 is: a dielectric structure on an isolation area of the semiconductor substrate, at least two through-array contacts extending perpendicularly through one of a plurality of isolation areas. Based on this, the technical problem to be solved by this claim is how to set the position of the area for the through-array contacts.

However, the isolation area is a necessary component in the semiconductor device, and Reference Document 2 also discloses a shallow trench isolation area 720 on the semiconductor substrate and a lower level dielectric layer 760, where the through-array contacts 488 are connected with the lower level metal interconnect structure 780 through at least a portion of the lower level dielectric layer 760. The through-hole area of the through layer is provided on the isolation area of the substrate, which is a conventional setting easily achieved by those skilled in the art, therefore, it is common knowledge. On this basis, in order to electrically connect with the lower level metal interconnect structure and realize memory function, those skilled in the art can easily extend the through array contacts through the isolation area covering the lower level metal interconnect structure. Therefore, it is obvious to those skilled in the art to obtain the technical solution claimed by this claim based on the common knowledge

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of Reference Document 2, and there is no need for creative work. This claim does not have prominent substantive features or significant progress, and does not have the inventiveness as specified in Paragraph 3 of Article 22 of the Patent Law.

2. Claims 2-11 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

For Claim 2, Reference Document 2 discloses an epitaxial layer 11 formed between each of the one or more channel structures and semiconductor substrate 9; a ladder structure disposed in the alternating stacked layer; one or more contact layers disposed on the at least two through-array contacts 488, the one or more channel structures, and the one or more crevice structures; and at the same time, an etch stop plug is provided on the channel structure to prevent etch damage to the channel, which is common knowledge in the art.

For Claim 3, Reference Document 2 discloses that the dielectric structure abuts the sidewall surfaces of the at least two through-array contacts 488.

For Claim 4, Reference Document 2 discloses a 3D NAND memory piece.

For Claim 5, Reference Document 2 discloses alternating pairs of the alternating stacked layers comprising a dielectric layer and a conductor layer.

For Claim 6, Reference Document 2 discloses that the dielectric layer comprises silicon oxide, and it is common knowledge that the conductor layer comprises metal.

For Claim 7, Reference Document 2 discloses that the conductor layer comprises a word line.

For Claims 8-9, Reference Document 2 discloses that the dielectric material is silicon oxide.

For Claim 10, Reference Document 2 discloses that the dielectric structure 430 defines a through-array contact area within the three-dimensional memory device;

For Claim 11, setting the dielectric structure to have a footprint equal to or smaller than the isolation area is a common technical means in the art, and those skilled in the art can easily set it according to the actual situation of the device.

Therefore, where the Claims referenced do not possess creativity, Claims 2-11 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law either.

3. Therefore, Claim 12 does not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

Reference Document 2 (US2017/0179026A1) discloses a method of manufacturing a 3D memory

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device, and specifically discloses (paragraph 0005-0389 of the Specifications, Figs. 1A-76):

forming a shallow trench isolation area 720 on the semiconductor substrate 9; providing an alternating dielectric stack layer on the semiconductor substrate 9 comprising a first and a second dielectric layer pair, the second dielectric layer being different from the first dielectric layer [in the pair], specifically, forming an alternating conductor/dielectric stack layer based on the alternating dielectric stack layer; forming a channel structure extending vertically in the alternating dielectric stack layer; forming an opening 769 in the alternating dielectric stack layer, wherein the opening 769 is filled with the dielectric layer to form a dielectric structure 430 as a through-array contact area of the 3D memory device; removing the dielectric structure 430 to form a through-array contact opening extending vertically through the dielectric structure 430; filling the through-array contact opening with a conductor to form a through-array contact structure 488 in the through-array contact area.

It can be understood that the distinguishing feature of this claim relative to Reference Document 2 is: the opening exposing the isolation structure, removing portions of the isolation structure until the substrate is exposed to form a through-array contact opening extending perpendicularly through the dielectric structure and the isolation structure, the through-array contact structure contacting the substrate; Based on this, the technical problem to be solved by this claim is how to set the position of the area of the through-array contacts.

However, the isolation area is a necessary component in the semiconductor device, and Reference Document 2 also discloses a shallow trench isolation area 720 on the semiconductor substrate and a lower level dielectric layer 760, where the through-array contacts 488 are connected with the lower level metal interconnect structure 780 through at least a portion of the lower level dielectric layer 760. The through-hole area of the through layer is provided on the isolation area of the substrate, which is a conventional setting easily achieved by those skilled in the art and is common knowledge. On this basis, in order to electrically connect with the interconnected structure in the substrate and realize memory function, those skilled in the art can readily remove portions of the isolation structure to extend through-array contacts through the isolation area to contact the substrate. Therefore, it is obvious to those skilled in the art to obtain the technical solution claimed by this claim based on the common knowledge of Reference Document 2, and there is no need for creative work. This claim does not have prominent substantive features and significant progress, and does not have the inventiveness as specified in Paragraph 3 of Article 22 of the Patent Law.

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4. Therefore, Claims 13-20 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

For Claim 13, Reference Document 2 discloses: Prior to forming the through-array contact opening, the method further comprises: forming a crevice opening extending vertically in the alternating dielectric stack layer, wherein the slit opening exposes a doped area of the substrate; replacing the second dielectric layer with a conductor layer through one or more crevice openings to convert the alternating dielectric stack layer into an alternating dielectric/conductor stack layer (Reference Document 2 discloses a sacrificial layer process); and filling the one or more crevice openings with a conductor to form one or more crevice structures 76, 79 extending vertically in the alternating dielectric/conductor stack layer.

For Claims 14-15, pruning & etching processes and dry etching processes are common technical means in the art to form ladder structures in alternating dielectric stack layers.

For Claim 16, the specific process for filling the dielectric layer is common knowledge in the art.

For Claims 17-18, Reference Document 2 discloses that filling the opening 769 with a dielectric layer comprises forming silicon oxide;

For Claims 19-20, Reference Document 2 discloses that the first dielectric layer includes silicon oxide and the second dielectric layer includes silicon nitride.

Therefore, where the Claims referenced do not possess creativity, Claims 13-20 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law either.

5. Therefore, Claim 21 does not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

Reference Document 2 (US2017/0179026A1) discloses a method of manufacturing a 3D memory device, and specifically discloses (paragraph 0005-0389 of the Specifications, Figs. 1A-76):

An alternating dielectric stack layer is provided on the semiconductor substrate 9, which includes a first and a second dielectric layer pair. The second dielectric layer is different from the first dielectric layer [in the pair]. Specifically, alternating conductor/dielectric stack layers are formed based on alternating dielectric stack layers; channel structures extending vertically in the alternating dielectric stack layers are formed; opening 769 is formed in the alternating dielectric stack layer, wherein opening 769 is filled with a dielectric layer to form a dielectric structure 430 serving as a through-array contact area of the 3D memory device; remove the dielectric structure 430 to form a through-array contact opening extending vertically through the dielectric structure 430; fill the through-array contact opening

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with a conductor to form through-array contact structure 488 in the through array contact area.

It can be understood that the distinguishing feature of this claim relative to Reference Document 2 is: the opening exposing the isolation structure, the through-array contact area being equal to or smaller than the isolation area, etching through the isolation area to form a through-array contact opening exposing the substrate. Based on this, the technical problem to be solved by this claim is how to set the position of the area of the through-array contacts.

However, the isolation area is a necessary component in the semiconductor device, and Reference Document 2 also discloses a shallow trench isolation area 720 on the semiconductor substrate and a lower level dielectric layer 760, where the through-array contacts 488 are connected with the lower level metal interconnect structure 780 through at least a portion of the lower level dielectric layer 760. The through-hole area of the through layer is provided on the isolation area of the substrate, and is smaller than the isolation area, which is a conventional setting easily achieved by those skilled in the art, therefore, it is common knowledge. On this basis, in order to electrically connect with the lower level metal interconnect structure and realize memory function, those skilled in the art can easily form the through-array contact opening by etching the isolation structures to expose through-array contact opening on the substrate. Therefore, it is obvious to those skilled in the art to obtain the technical solution claimed by this claim based on the common knowledge of Reference Document 2, and there is no need for creative work. This claim does not have prominent substantive features or significant progress, and does not have the creativity as specified in Paragraph 3 of Article 22 of the Patent Law.

6. Therefore, Claims 22-27 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

For Claim 22, Reference Document 2 discloses: forming a crevice opening extending perpendicularly through the alternating dielectric layer, wherein the crevice opening exposes a doped area of the substrate (see FIG. 14C); replacing the second dielectric layer with a conductor layer through the crevice opening to convert the alternating dielectric stack layer into an alternating dielectric/conductor stack layer; filling the crevice opening with a conductor to form crevice structures 76 and 79; forming a ladder structure in the alternating dielectric stack layer, wherein the ladder structure comprises a hierarchy; forming word line contacts on each level of the hierarchy of the ladder structure; forming local contacts on the channel structure and the crevice structure; and forming one or more contact layers on the local contacts, each word line, and each through-array contact structure (see

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Figs. 17A-17C).

For Claim 23, Reference Document 2 discloses that the first dielectric layer comprises silicon oxide and the second dielectric layer comprise silicon nitride;

For Claim 24, Reference Document 2 discloses that the opening is formed by dry etching.

For Claim 25, Reference Document 2 discloses that filling the opening with a dielectric layer comprises forming silicon oxide;

For Claim 26, Reference Document 2 discloses that the alternating dielectric/conductor stack layer abuts the sidewall of the dielectric structure 430.

For Claim 27, Reference Document 2 discloses that the dielectric structure 430 abuts a sidewall surface of each through array contact structure

Therefore, where the Claims referenced do not possess creativity, Claims 22-27 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law either.

7. Claim 28 does not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

Reference Document 2 (US2017/0179026A1) discloses a 3D memory device and specifically discloses (paragraph 0005-0389 of the Specifications, Figs. 1A-76):

a semiconductor substrate 9 having a shallow trench isolation area 720; an alternating stack layer, in particular a pair of conductors/dielectric layers, disposed on the semiconductor substrate 9; a dielectric structure 430 extending vertically through the alternating stack layer, wherein the alternating stack layer abuts a sidewall surface of the dielectric structure 430 and the dielectric structure 430 is formed of a dielectric material (paragraphs 0216-0217, Figs. 12A-12B of the Specifications); at least two through-array contacts 488, both extending vertically through the dielectric structure 430; and one or more channel structures extending vertically through the alternating stack layer.

It can be understood that the distinguishing feature of this claim relative to Reference Document 2 is: a dielectric structure on an isolation area of the semiconductor substrate, at least two through-array contacts extending perpendicularly through one of a plurality of isolation areas. Based on this, the technical problem to be solved by this claim is how to set the position of the area of the through-array contacts.

However, the isolation area is a necessary component in the semiconductor device, and Reference Document 2 also discloses a shallow trench isolation area 720 on the semiconductor substrate and a

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lower level dielectric layer 760, where the through-array contacts 488 are connected with the lower level metal interconnect structure 780 through at least a portion of the lower level dielectric layer 760. The through-hole area of the through layer is provided on the isolation area of the substrate, which is a conventional setting easily achievable by those skilled in the art, therefore, it is common knowledge. On this basis, in order to electrically connect with the lower level metal interconnect structure and realize memory function, those skilled in the art can easily extend the through array contacts through the isolation area covering the lower level metal interconnect structure. Therefore, it is obvious to those skilled in the art to obtain the technical solution claimed by this claim based on the common knowledge of Reference Document 2, and there is no need for creative work. This claim does not have prominent substantive features or significant progress, and neither does it have the inventiveness specified in Article 22, Paragraph 3 of the Patent Law.

8. Therefore, Claims 29-32 do not possess creativity as prescribed in Article 22, Paragraph 3 of the Patent Law.

For Claim 29, Reference Document 2 discloses: a ladder structure disposed in an alternating conductor/dielectric stack layer, wherein the ladder structure comprises a hierarchy with a conductor layer at each level; word line contact(s) disposed on each conductor layer of the ladder structure; local contact(s) disposed on each channel structure and crevice structure.

For Claim 30, Reference Document 2 discloses that the dielectric structure abuts the side wall surface of each through-array contact 488.

3) For Claim 31, Reference Document 2 discloses that the dielectric structure includes a through-array contact area of the three-dimensional memory device;

For Claim 32, Reference Document 2 discloses an epitaxial layer 11 formed between each of the one or more channel structures and the semiconductor substrate 9; at the same time, it is common knowledge in the art to provide an etch stop plug on the channel structure to prevent the channel from being etched and damaged.

Therefore, where the Claims referenced do not have creativity, Claims 29-32 do not have creativity prescribed in Article 22, Paragraph 3 of the Patent Law either.

Based on the above reasons, neither the independent Claims nor the dependent Claims of the present application are creative, and there is no other substantive content in the Specifications that justify granting of any patent right. Therefore, even if the applicant reorganizes the Claims and/or further

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defines the content stated in the Specifications, the present application does not have the prospect of being granted a patent right. This application will be dismissed if the applicant is unable to make sufficient grounds for the creativity of this application within the time limit as specified in this notice.

Examiner Name: Wang Xiaofeng Examiner Code: 160262

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TRANSPERFECT

April 1, 2024

Certification

Translator's Declaration:

I, Meihua Shi, hereby declare:

That I possess advanced knowledge of the Chinese and English languages.

My qualifications are as follows: I have obtained master's degree from both China and United States and have been translating documents for over 20 years. I am competent to translate from Simplified Chinese to English.

The attached Chinese into English translation has been translated by me and to the best of my knowledge and belief, it is a true and accurate translation of:

Certified Translation of CN109075169A Office Action, dated November 14, 2019

I understand that willful false statement and link are punishable by fine or imprisonment, or both (18 U.S.C. 1001) and may jeopardize the validity of the application or any patent issuing thereon. I declare under the penalty of the perjury that all statements made herein of my own knowledge are true and all statements made on information and belief are believed to be true.

Meihua Shi

Sworn to before me this
April 2, 2024

Signature, Notary Public

ERICA M. KLEIN
Notary Public, State of New York
No. 01KL6382038
Qualified in Livingston County
Commission Expires 10/15/2026

Stamp, Notary Public