Chapter

19

Packaging Glossary

Ronald W. Gedney

19.1 Introduction

The idea for a packaging glossary actually arose from a conversation with Prof. Sillo, chairman of the mechanical engineering department at Binghamton University. We were discussing electronic packaging course material and he said he wished a glossary of packaging terms were available. As I had edited a packaging applications guide for IBM in 1990, I knew that it contained a partial glossary for both packaging acronyms and terminology. So I foolishly said I thought it would not be too difficult to compile such a document, and would see if I could provide it for him.

I sat down with my computer, pulled together some books along with my applications guide and set to work. Some 4 weeks later, I realized this was going to be a much lengthier task than I had planned. By that time, I was up to the "Rs," had compiled over 30 pages, and felt it was too late to quit. So I dug in, kept going, and finally, finally, arrived at the "Zs."

My goal was to include a clear, but brief, definition of as many package acronyms, types, and terminologies as possible. The glossary very thoroughly covers first-level packages (chip carriers) and second-level packages (printed circuit boards). This includes not only package types, but thermal management, process technology—including chemical terms, reliability and quality, contacts and connectors, and electrical terms. The original intent was to provide a reference document for students majoring in electronic packaging (either through the ME or EE curriculum) at universities. It should also be useful to people who are new to—or do not work every day with—the field of electronic packaging. However, electronic packaging is such a complex, interdisciplinary field, that even the experienced practitioner may find it useful to have all the terminology in one reference document.

Micron Ex. 1026, p. 70
Micron v. YMTC
IPR2024-00911

I would like to thank Dr. Donald P. Seraphim for taking the time to do a thorough review of the glossary and providing me with excellent feedback. I would also like to thank Richard J. Prosman of the Integrated Electronics Engineering Center at Binghamton University for his interest and encouragement, without which this might not have been completed at all.

19.2 Terms

accelerated (stress) testing A test meant to produce failures caused by the same wearout failure mechanism as expected in field operation but in significantly shorter time.

accelerator A chemical additive that hastens a chemical reaction under specific conditions.

acceptable quality level (1) The lowest quality level a supplier is permitted to present continually for acceptance. (2) The maximum percentage of defects or number of defective parts considered to be an acceptable average for a given process or technique.

activating A treatment that renders nonconductive material receptive to electroless deposition. Also called *seeding, catalyzing,* or *sensitizing.*

active components Electronic components, such as transistors, diodes, etc., which can operate on an applied electrical signal so as to change its basic characteristics (i.e., rectification, amplification, switching, etc.).

active trimming A method of adjusting a circuit function under operating conditions.

additive process (plating) A chemical reduction process for obtaining conductive patterns by the selective deposition of conductive material on clad or unclad base material.

adhesion The ability of a conductor or insulator material to withstand a force attempting to separate it from the substrate.

adhesion promotion The chemical process of preparing a surface to provide for a uniform, well-bonded interface.

Advanced Statistical Analysis Program (ASTAP) An IBM circuit analysis and simulation program. It performs DC, time domain, and frequency domain simulations. Statistics can be applied to all simulations to predict operating tolerances. (Also see **SPICE.**)

alloy (1) Any of a large number of substances having metallic properties and consisting of two or more elements, which are usually metallic. (2) To make or melt an alloy.

alpha particle Decay product of some radioactive isotopes. It is a high-energy (mv range) helium nucleus capable of generating electron/hole pairs in microelectronic devices and switching cells, causing soft errors in some devices.

alumina Aluminum oxide, Al_2O_3. Alumina substrates are made of formulations that are primarily alumina. Nearly all ceramic modules are manufac-

Micron Ex. 1026, p. 71
Micron v. YMTC
IPR2024-00911

tured with alumina ceramics, as alumina is easy to work with, has fairly good thermal conductivity, and, for flip chip, has a TCE of 6.5 versus 3.0 for silicon.

aluminum nitride Chemical symbol is AlN. This material has a thermal conductivity of 200 m^2/K versus 20 for alumina. Also its thermal coefficient of expansion is very close to that of silicon (3.0). This is a relatively new ceramic, which is already in use for high-power components and has potential to replace BeO as well as Al_2O_3.

aluminum oxide See **alumina.**

ambient The environment that surrounds and contacts a system or component.

anchoring spurs Extensions of the lands on printed wiring beneath a cover layer to assist in holding the lands to the base material.

angle of attack The angle between the squeegee face of a thick-film printer and the plane of the screen.

anisotropic Exhibiting different properties when tested along axes in different directions. In magnetics, capable of being magnetized more readily in one direction than in a transverse direction.

anisotropic conductive adhesive An adhesive that can be made conductive in the vertical, or z axis, while remaining an insulator in the horizontal or x and y axes.

annular ring The portion of conductive material that completely surrounds a hole.

antihalation backing The coating on the rear surface of a film or glass plate that reduces the reflection of light into the areas of the emulsion layer that are to be unexposed.

Application-Specific Integrated Circuit (ASIC) An integrated circuit chip with personalization customized for a specific product. Personalization refers to wiring on the integrated circuit chip.

aqueous In printed board manufacturing operations, water-soluble processes such as a mild sodium or potassium carbonate solution used for image development.

Area Array Tape Automated Bonding (ATAB) Tape-automated bonding in which edge-located pads and additional pads on the inner surface area of a chip are addressed in the bonding scheme.

array A group of elements (pads, pins) or circuits arranged in rows and columns on one substrate.

artwork An accurately scaled configuration that is used to produce an artwork master or production master.

artwork master An accurately scaled (usually 1:1) pattern that is used to produce the production master.

aspect ratio A ratio of the length or depth of a hole to its preplated diameter.

aspot The active areas in an electrical contact interface where asperities are highly deformed and break through any insulating film material.

Micron Ex. 1026, p. 72
Micron v. YMTC
IPR2024-00911

assembly A number of parts or subassemblies or any combination thereof joined together.

assembly/rework Terms denoting joining and replacement processes of microelectronic components. Assembly refers to the initial attachment of device and interconnections to the package. Rework refers to the removal of a device including interconnections, preparation of the joining site for a new device, and rejoining of the new device.

A-wire Term coined by IBM for area wire bond package for memory devices. Refers to particular technique of wire bonding from the middle of the semiconductor device to a lead frame resting on an insulator over the device. (See **lead on chip.**)

axial leads Leads that come out of the ends of a discrete component or device along the central axis, rather than out of the sides.

backbonding Bonding active chips to the substrate using the back of the chip, leaving the face, with its circuitry facing up. The opposite of backbonding is face-down bonding.

Back-End-of-the-Line (BEOL) That portion of the integrated circuit fabrication where the active components (transistors, resistors, etc.) are interconnected with wiring on the wafer. It includes contacts, insulator, metal levels, and bonding sites for chip-to-package connections. Dicing the wafer into individual integrated circuit chips is also a BEOL process. The front-end-of-the-line (FEOL) denotes the first portion of the fabrication where the individual devices are patterned in the semiconductor.

back panel or backplane A planar printed circuit board package holding plugged-in lower-level package components (e.g., cards) as well as discrete wires and cables interconnecting these components. (See also **mother board.**)

Backside Metallurgy (BSM) A metallization pad electrically connected to internal conductors within a multilayered ceramic package to which pins are brazed.

ball bond A bond formed when an interconnection wire with a ball-shape end is deformed by thermocompression against a metallized pad. Also called *nail head bond* from the appearance of the flattened ball.

ball grid array package For very high speed integrated circuits, a package embodying a rather novel technology in which solder-contact pads are not just around the package periphery (as with chip carriers), but cover the entire bottom surface in checkerboard fashion. Also known as *pad array carrier* (PAC), *pad array package, land grid array,* or *pad-grid array package.*

Ball Limiting Metallurgy (BLM) The solder wettable terminal metallurgy which defines the size and area of a soldered connection, such as a C-4 pad on a chip. The BLM limits the flow of the solder to the desired area, and provides adhesion and contact to the chip wiring.

ball mill A cylindrical jar filled with ceramic or metal balls that is rotated to mix and grind ceramic powders.

bare chip (die) An unpackaged silicon device. For multichip modules, manufacturers purchase bare die, tested and ready for assembly to a package.

Micron Ex. 1026, p. 73
Micron v. YMTC
IPR2024-00911

barrel-cracking One of the major reliability problems with printed boards is barrel-cracking, or the cracking of the plated through-hole copper during temperature cycling.

BAT Acronym for Bond, Assembly and Test. Usually refers to device assembly into a finished module or package.

bayonet coupling A quick-coupling device for plug and receptacle connectors, accomplished by the rotation of the two parts under pressure.

beam lead chip A chip employing electrical terminations in the form of tabs extending beyond the edge of the chip for direct bonding to a mounting substrate.

bellows contact A connector contact that is a flat spring folded to provide a uniform spring rate over the full tolerance range of the mating unit.

beryllia Beryllium oxide, BeO. A substrate material used where extremely good thermal conductivity is desired.

bifet An integrated circuit that has both bipolar and FET transistors integrated together on the same piece of silicon.

bifurcated contact A connector contact (usually a flat spring) that is slotted lengthwise to provide independently operated points of contact, or redundant or tandem operation.

bifurcated squeegee A two-part squeegee used in a screen printer so that the thick-film composition fluid can be pumped through the squeegee to provide a continuous supply of fluid. This arrangement is especially useful for a highly pseudoplastic or thixotropic fluid used for high resolution printing.

bimetal mask A mask formed by different metals combined by electroforming or cladding. Apertures are selectively etched through one metal to form an image in a second metal.

binders Materials added to thick-film compositions, unfired substrates, and so forth to give sufficient strength for prefire handling.

bipolar transistor A transistor that uses charge carriers of both polarities.

BIST See **built-in self-test.**

blade contact A flat male contact, used in multiple-contact connectors, designed to mate with a tuning fork or a flat formed female contact.

bleed The loss of acuity at the edge of a deposit due to fluidity of the deposited material.

blister (1) A localized swelling and separation between any of the layers of a base material or dielectric, or between base material/dielectric and conductive foil or fired conductor. A form of delamination. (2) Air or entrapped volatiles that rise under the solder mask during thermal shocks.

block copolymer A copolymer compound resulting from the chemical reaction between *n* number of molecules, which are a block of one monomer, and "n" number of molecules, which are a block of another monomer. Example: stearine (rigid) with silicone (elastic).

blow hole A void in a solder connection caused by outgassing or a void in a fired dielectric.

Micron Ex. 1026, p. 74
Micron v. YMTC
IPR2024-00911

board This package element can best be defined as an organic printed-circuit card or board on which smaller cards or modules can be mounted. Its connections to the next higher level involve discrete wire or cables either soldered or plugged into connector systems.

body (1) Main, or largest, portion of a connector to which other portions are attached or inserted. (2) Structural portion of a ceramic particle or the material or mixture from which it is made.

boiling Phase change and formation of bubbles in a superheated liquid.

bond strength The force per unit area required to separate two adjacent layers of a package (substrate, board, etc.) by a force perpendicular to the package surface.

bondability Those surface characteristics and conditions of cleanliness of a bonding area which must exist in order to provide a capability for successfully bonding an interconnection material by one of several methods such as ultrasonic or thermocompression wire bonding, or soldering.

bonding The joining together of two materials; for example, the attachment of wires to an integrated circuit or the mounting of an integrated circuit to a substrate.

bonding layer An adhesive layer used in bonding together other discrete layers of a multilayer printed board during lamination.

bonding pads Areas of metallization on the integrated circuit die that permit connection to the die of fine wires or circuit elements.

boot A form placed around the wire termination of a multiple-contact connector to contain a liquid potting compound. Also, a protective housing usually made from a resilient material to prevent entry of moisture into a connector.

boundary-scan A method of testing a chip whereby scannable test cells are placed at each input/output pin to allow control of the chip boundaries. The test circuitry provides a virtual electronic bed of nails by way of only a 4-wire test bus. This same test bus can also provide access to initiate or evaluate on-chip built-in self-test.

bow The deviation from flatness of a board, characterized by a roughly cylindrical or spherical curvature such that, if the board is rectangular, its four corners are in the same plane.

braze A joint formed between two different materials by formation of liquid at the interface.

brazing The joining of metals by melting a nonferrous, filler brazing metal, such as eutectic gold-tin alloy, having a melting point lower than that of the base metals. Also known as *hard soldering.*

breakaway The screen-to-substrate separation required during off-contact screen printing. Also known as the *snap-off distance.*

brown oxide An oxide layer on copper, formed intentionally by chemicals, to enhance adhesion to polymers.

B-stage resin In a thermosetting reaction, a resin that is in an intermediate state of cross-link which is capable of further flow upon heating. The cure is

Micron Ex. 1026, p. 75
Micron v. YMTC
IPR2024-00911

normally completed during the laminating cycle. (See **C-stage resin** and **prepreg.**)

bt resins Bis-maleimide-triazine-type resins are mixed with epoxies to achieve the desired laminate properties for use in printed boards. Advantages include high heat resistance, low dielectric constant and excellent electrical insulation resistance even after moisture absorption.

BTAB The acronym for Bumped Tape Automated Bonding where the raised bump for each bond site is prepared on the tape material as opposed to the bump being on the chip.

Built-In Self-Test (BIST) An electrical test scheme whereby hardware is added on the chip to allow the integrated circuit (IC) to test itself with minimal external test equipment. By embedding the test circuitry within the same silicon as the IC's normal application circuitry, BIST is not prone to the loading effects or signal limitations of an external test system. BIST also provides at-speed testing of the chip.

bulk resistance The resistance that is due to the length, cross section and material of a conductive element.

bump A means of providing connections to the terminal areas of a device. A small mound is formed on the device (or substrate) pads and is used as a contact for face-down bonding.

bump contacts Contacting pads that rise substantially above the surface level of the chip. Also, raised pads on the substrate that contact the flat land areas of the chip. Also called *ball contacts, raised pads,* or *pedestals.*

Bumped Tape (BTAB) A tape used in the tape automated bonding process where the inner-lead bond sites have been formed into raised metal bumps on the tape rather than on the chip. This ensures mechanical and electrical separation of the inner-lead bonds and the nonpad areas of the chip (die) being bonded.

burned plating Rough, dull electrodeposit caused by excessive plating current density.

burn-in The process of exposing a component part to elevated temperatures with a voltage stress applied for the purpose of screening out marginal parts.

burnishing Smoothing the conductor materials, after printing and firing, with a fiberglass brush, eraser, or other abrasive material.

burn-off Removal of unwanted materials—typically organic from greensheet or organic contaminants from substrates.

bus bar A conduit, such as a conductor on a printed board, for distributing electrical energy. (See **plating bar,** a subcategory of this term.)

butt Placing two conductors together end to end (but not overlapping) with their axes in line.

camber A term that describes the amount of overall warpage present in a substrate.

capacitance The electrostatic element that stores charge. In packaging systems, it is used: (1) in lumped equivalent circuits to represent part of a line dis-

Micron Ex. 1026, p. 76
Micron v. YMTC
IPR2024-00911

continuity; (2) in a distributed system to represent the electrostatic storage property of a transmission line; (3) to filter powering systems, because it delivers current in response to a change in voltage.

capacitive coupling The electrical interaction between two conductors caused by the capacitance between them.

card A printed-circuit panel (usually multilayer) that provides the interconnection and power distribution to the electronics on the panel, and provides interconnect capability to the next level package. It is also known as a daughter board. It plugs into a mother (printed circuit) board.

Card-on-Board (COB) Package technology in which multiple printed-circuit panels (cards) are connected to a (large) printed-circuit panel (board) at 90° angles.

case temperature The temperature measured at a specified location on the (external) case of a device.

catalyzing See **activating.**

CDIP (CERDIP) Acronym for Ceramic Dual In-line Package. The package is composed of a ceramic header and lid, a stamped-metal lead frame, and a frit glass that is used to secure the structure.

ceramic Inorganic, nonmetallic material, such as alumina, beryllia, or glass-ceramic, whose final characteristics are produced by subjection to high temperatures.

Ceramic Ball Grid Array package (CBGA) A ceramic package designed for surface mount applications. It is similar to a ceramic pin grid array except that, instead of pins, the input/output terminals are composed of solder balls. (See **ball grid array package.**)

cermet A solid homogeneous material usually consisting of a finely divided admixture of a metal and ceramic in intimate contact. Cermet thin films are normally combinations of dielectric materials and metals, usually used as resistor elements in hybrid circuits.

channel For a printed circuit board, a channel is the space between the grid of through holes (vias).

characteristic impedance (Z_0) The ratio of voltage to current in a propagating wave; that is, the impedance that is offered to this wave at any point on the line. In printed wiring, its value depends on the width of the conductor, the distance from the conductor to ground planes, and the dielectric constant of the media between them.

chemical milling The process in which metal is formed into intricate shapes by masking certain portions and then etching away the unwanted material.

Chemical Vapor Deposition (CVD) Depositing circuit elements on a substrate by chemical reduction of the vapor of a volatile chemical in contact with the substrate.

chemorheology The study of the processability or flow (rheology) and the chemistry of the polymer system. Processability parameters include, for instance, heating rates, hold temperatures, injection speeds, and compaction

Micron Ex. 1026, p. 77
Micron v. YMTC
IPR2024-00911

pressures. The chemical aspect, on the other hand, involves the rate of reaction, the mechanisms, the kinetics, and the cessation of the chemical reaction at the end of the polymerization.

chip The individual semiconductor element or integrated circuit after it has been cut or separated out of the processed semiconductor wafer, distinct from a completely packaged or encapsulated integrated circuit with leads attached. Also referred to as a *die.* Sometimes used to refer to uncased, normally leadless, passive components (e.g., chip capacitor).

chip carrier An integrated circuit package, usually square, which may have a cavity for the chip in the center. Its connections are usually on all four sides.

Chip-on-Board (COB) One of many configurations in which a chip is directly bonded to a printed circuit board or substrate. [See also **Direct Chip Attach (DCA).**]

Chip-on-Lead (COL) Refers to a package structure whereby some inner leads (of a lead frame) pass under the chip, and the tips of the leads protrude under the two short sides of the die where the bonding pads are located. This allows the ratio of the die size to package size to be substantially increased, and enhances the package thermally.

circuitization Denoting the circuit fabrication process of imaging, plating, etching, and stripping.

clearance hole A hole in the conductive pattern that is larger than, but coaxial with, a hole in the printed board base material.

clinched lead A component lead that extends through a hole in the printed board and is formed to prevent components from falling out prior to soldering.

coated metal core substrate A substrate consisting of an organic or inorganic insulation coating bonded to metal. Insulated surface or surfaces are used for circuit deposition. The metal core may be used for its thermal properties or to control the coefficient of expansion of the overall package.

coaxial A cable configuration having two cylindrical conductors with coincidental axes, such as a conductor with a tabular shield surrounding the conductor and insulated from it.

COB (1) Acronym for Chip-on-Board, which see. (2) Acronym for Card-on-Board, which see.

Coefficient of Thermal Expansion (CTE) The ratio of the change in dimensions to the change in temperature-per-unit starting length, usually expressed in cm/cm/°C.

Coffin-Manson equation Often used to relate the strain amplitude to the fatigue life. Basically the equation states that the number of cycles to failure is proportional to the reciprocal of the strain squared. In reliability testing it can be used to predict field life based on accelerated temperature cycling in the laboratory.

cofiring (1) A process in which two thick-film compositions are printed and dried one after the other and then fired at the same time. (2) Processing thick-film conductors and dielectrics through the firing cycle at the same time to form multilayer structures (e.g., multilayer ceramic substrates).

Micron Ex. 1026, p. 78
Micron v. YMTC
IPR2024-00911

coined lead A cylindrical lead that has been formed to have parallel surfaces approximating a ribbon lead configuration.

cold flow Permanent deformation of the insulation due to mechanical forces, without the aid of heat softening of the insulating material.

cold solder joint A soldered connection exhibiting poor wetting and a dull, porous appearance due to insufficient heat or inadequate cleaning prior to soldering or because of excessive impurities in the solder.

cold weld Forming a hermetic seal in a metal package by welding the lid to the frame using pressure alone.

collimated light In photoprinting, the state of all light rays traveling in parallel at the exposure plane. This is in comparison to a point source, which generates light rays at varying angles.

complementary metal-oxide semiconductor (cmos) This refers to logic in which cascaded field effect transistors (FET) of opposite polarity are used to minimize power consumption.

compliant bond A bond which uses an elastically and/or plastically deformable member to impart the required energy to the lead.

component An individual functional element in a physically independent body that cannot be further reduced or divided without destroying its stated function, for example, a resistor, capacitor, diode, or transistor.

component lead The formed conductor that extends from a component and serves as a mechanical and/or electrical connection for that component.

component side That side of the printed wiring board on which most of the components are mounted.

compression seal A seal made between an electronic package and its leads. The seal is formed as the heated metal case, upon cooling, shrinks around the glass insulator, thereby forming a tight joint.

conditioning Time-limited exposure of a test specimen to specified environment(s) prior to testing.

conductance A measure of the ability of any material to conduct an electrical charge. Conductance is the ratio of current flow to the potential difference. The reciprocal of electrical resistance.

conduction Thermal transmission of heat energy from a hotter region to a cooler region in a conducting medium.

conductive adhesive An adhesive material, usually epoxy, that has metal powder added to increase electrical conductivity. The usual conductor material added is silver.

conductive epoxy An epoxy material (polymer resin) that has been made conductive by the addition of a metal powder, usually gold or silver.

conductive foil A thin sheet of metal that may cover one or both sides of the base material and is used for forming the conductive pattern.

conductive pattern The configuration or design of the conductive material on the base material. For an organic printed board, the pattern includes conduc-

Micron Ex. 1026, p. 79
Micron v. YMTC
IPR2024-00911

tors, lands, and through connections (vias), when these connections are an integral part of the manufacturing process. When applied to flat ceramic packages, a conductive pattern is accomplished by means of screened-on metallization, forming the internal portions of leads and other conductive area.

conductivity, electrical The capability of a material to carry an electrical current; that is, conductances of a unit cube of any material. The reciprocal of resistivity.

conductor, electrical A class of materials that conduct electricity easily. They have very low resistivity which is usually expressed in micro-ohm-cm. The best conductors include silver, copper, gold, and superconducting-ceramics.

conductor spacing The observable distance between adjacent edges (not centerline to centerline) of isolated conductive patterns in a conductor layer.

conductor, thermal A class of materials, such as copper, aluminum, and beryllia, that conduct heat.

conformal coating A thin, nonconductive coating, either plastic or inorganic, applied to a circuit for environmental and/or mechanical protection.

connector Generally, all devices used to provide rapid connect/disconnect service for electrical cable and wire terminations, board to board.

connector assembly A mated plug and receptacle.

contact The element in a connector that makes the actual electrical contact. Also, the point of joining in an electrical connection.

contact alignment The overall side play of contacts within the insert cavity to permit self-alignment of mated contacts. Also called *amount of contact float.*

contact angle The angle enclosed within the fillet, between a plane tangent to the solder/base-metal surface and a plane tangent to the solder/air interface.

contact arc The electrical (current) discharge that occurs between mating contacts when a circuit is being made or broken.

contact area The common area between a conductor and a connector across which the flow of electricity takes place.

contact length Length of travel made by one contact in contact with another during assembly or disassembly of the connector. (See also **wiping action.**)

contact printing A method of screen printing in which the screen is almost (within a few mils) in contact with the substrate. Used for precision printing or with nonflexible screens. Also a method of photoprinting in which the mask is in direct contact with the photoresist on the part.

contact rating The Aerospace Industries Association of America, Inc. defines contact rating as "The maximum current for a given type of load (that is, voltage, frequency, and nature of impedance) which the relay (contacts) will make, carry, and break (unless otherwise specified) for its rated life."

contact resistance Excess electrical resistance in series with the bulk conductor resistance of two contacting electrical conductors arising from the nature of the contact geometry and surface properties of the contacting surfaces.

Micron Ex. 1026, p. 80
Micron v. YMTC
IPR2024-00911

contact retention The minimum axial load in either direction that a contact must withstand while remaining fixed in its normal position within an insert.

contact spacing The distance between centerlines of adjacent contact areas.

contact spring (1) A current-carrying spring, usually a flat-leaf type or wire member, to which the contacts are fastened. Contact-spring bearing contacts are assembled between insulators in the contact assembly, to form contact combinations. (2) A non-current-carrying spring that positions or tensions a current-carrying member.

contact (spring) tension The contact pressure developed, usually resulting from the specified adjustment of movable contacts against mating stationary springs, when the relay is unenergized.

contact weld (1) The point of attachment of a contact to its support when accomplished by resistance welding. (2) A contacting failure due to the fusing of contacting surfaces under load conditions to the point that the contacts fail to separate when expected.

contact wipe The scrubbing action between mating contacts resulting from contact overtravel or follow.

continuity An uninterrupted path for the flow of electrical current in a circuit.

Controlled Collapse Chip Connection (C4) A solder joint connecting a substrate and a flip chip, where the surface tensions force of the liquid solder supports the weight of the chip and controls the height (collapse) of the joint (the height being a function of the two contacting areas and the total volume of solder in the joint).

controlled impedance For high-speed circuits, the impedance (Z_0) is fixed by design; i.e., the line thickness, spacing, distance to a ground plane, and the dielectric constant of the base material are part of the design. The actual tolerance on the nominal design depends on manufacturing control of these parameters.

convection cooling (self-convection) Generally refers to a system component in still air. The heat actually radiates away from the component without the benefit of forced air in the system environment generating air currents.

conversion efficiency In regard to photoemissive devices, the ratio of maximum available luminous- or radiant-flux output to total input power.

coplanar leads Ribbon-type leads (flat) extending from the sides of the circuit package, all of which lie in the same plane.

copyboard The part of a process camera used to hold the artwork in place.

cordierite A crystalline ceramic material of composition 2 magnesium oxide, 2 aluminum oxide, and 5 silicon oxide that can be crystallized from glass of the same composition or sintered from powders.

core material The fully cured, inner-layer segments, with circuitizing on one or both sides, that form the multilayer circuit.

corner mark The mark at the corners of printed circuit board artwork, the inside edges of which usually locate the borders and establish the contour of the board. Also called *crop mark.*

Micron Ex. 1026, p. 81
Micron v. YMTC
IPR2024-00911

COS Acronym for Chip-on-Substrate, synonymous with Chip-on-Board, which see.

COT Acronym for Chip-on-Tape, referring to the practice of testing chips after mounted on a continuous reel of TAB tape.

coupled noise The electromagnetic and electrostatic linkages between two nearby conductors that allow one line to induce a signal on the other. (See also **crosstalk.**)

coupler A chemical agent, frequently an organosilane, used to enhance the bond between a resin and a glass reinforcement.

cover lay Outer layer(s) of insulating material applied over the conductive pattern on the surface of the printed board. Also called *cover layer* or *cover coat.*

cover seal The seal at the perimeter of the cover or lid, when joined to the package body. In hybrid fabrication, the cover-sealing operation itself. The seal my be accomplished by resistance welding, cold welding (solid-phase bond), brazing, soldering, or other means.

cracking A condition in metallic and/or nonmetallic coatings consisting of breaks that extend through to an underlying surface.

crazing A network of fine cracks on the surface or through the layers of plastic or glass materials, such as conformal coatings or glass encapsulants. This condition can manifest itself in the form of connected white spots or "crosses" below the surface of the base material and is usually related to mechanically or thermally induced stress. (See also **measling.**)

creep The dimensional change with time of a material under load.

crimp termination A connection in which a metal sleeve is secured to a conductor by mechanically crimping the sleeve with pliers, presses, or automated crimping machines. Splices, terminals, and multicontact connectors are typical terminating devices attached by crimping.

crosshatching The breaking up of large conductive areas by the use of a pattern of voids in the conductive material.

cross link Intermolecular bonds produced between long-chain molecules in a material to increase molecular size and weight by chemical or photon bombardment, resulting in a change in physical properties in the material.

crossover The transverse crossing of metallization paths without mutual electrical contact achieved by the deposition of an insulating layer between the conducting paths at the area of crossing.

cross-sectional area The area of the cut surface of an object that has been cut at right angles to the long axis of the object.

crosstalk The undesirable interference caused by the coupling of energy between signal paths.

crystallization Formation of crystalline phaseout of amorphous material during high-temperature processing. Undesirable or uncontrollable crystallization is called devitrification.

C-stage resin A resin that is fully cross-linked at room temperature. (See also **B-stage resin.**)

Micron Ex. 1026, p. 82
Micron v. YMTC
IPR2024-00911

CTE Coefficient of Thermal Expansion, which see.

CTE mismatch The difference in the coefficients of thermal expansion (CTEs) of two materials or components joined together, producing strains and stresses at the joining interfaces or in the attachment structures (solder joints, leads, and so on).

cure To change the physical properties of a material (usually from a liquid to a solid) by chemical reaction or by the action of heat and catalysts, alone or in combination, with or without pressure.

curing agent An inorganic or organic compound that initiates the polymerization of a resin.

curing cycle For a thermosetting material, commonly for a resin compound such as a bonding adhesive, it is the combination of total time-temperature profile to achieve the desired result; for example, the complete irreversible hardening of the material, resulting in a strong bond.

current-carrying capacity The maximum current that can be carried continuously, under specified conditions, by a conductor without causing objectionable degradation of electrical or mechanical properties of the conductor or the substrate on which it resides.

Current-Mode Logic (CML) Basically equivalent to emitter-coupled logic (ECL), except that it operates in the nonsaturated mode and has greater speed.

current penetration The depth that a current of a given frequency penetrates into the surface of a conductor carrying the current, commonly called *skin depth.*

curtain coating Coating process in which a fluid forced through a narrow slot creates a falling liquid film.

custom design A form of design in which the choice and arrangement of components and wiring on a package may vary arbitrarily within tolerances from a regular array.

cut and strip Method of producing artwork by cutting the pattern and stripping away the unwanted areas of a two-layer system.

cut-through resistance The ability of a material to withstand mechanical pressure, usually a sharp edge of prescribed radius, without separation.

decoupling capacitor A shunt-placed capacitor that is used to filter transients on a power distribution system.

definition The fidelity of reproduction of the printed board relative to the production master.

delamination A separation between plies within the base material, or between the base material and the conductive foil, or both.

delay time The time interval from the point at which the leading edge of the input pulse has reached 10 percent of its maximum amplitude to the point at which the leading edge of the output pulse has reached 90 percent of its maximum amplitude.

delta-I noise See **switching noise.**

Micron Ex. 1026, p. 83
Micron v. YMTC
IPR2024-00911

dendritic growth The electrolytic transfer of metal from one conductor to another similar to electroplating except that dendritic growth usually, though not always, forms from cathode to anode. The dendrite assumes the form of a stalk with branches resembling a tree. When this dendritic growth touches the opposite conductor, there is an abrupt rise in current. This phenomenon is dependent on the presence of moisture, current and the nature of the conductive surfaces. Also a "tree-like" structure in electrolytic plating. Usually the result of high current density and additives in the plating bath. (See also **whiskers** and **electromigration.**)

deposition The "laying down" of films or metal or insulators on a substrate, by evaporative deposition, sputtering or electroplating.

derating factor A factor used to reduce the current-carrying capacity of a wire when the wire is used in other environments than that for which the value was established.

device An individual electrical element usually in an independent body, that cannot be further reduced without destroying its stated function. Also, an electronic part consisting of one or more active passive elements.

devitrification The undesirable formation of crystals in glass during firing. The desirable process is called crystallization.

devitrify To deprive of glassy luster and transparency or to change from a vitreous to a crystalline condition.

dewetting (1) The development and formation of a nonwetting condition after wetting has already commenced. (2) A condition that results when molten solder has coated a surface and then receded, leaving irregularly shaped mounds of solder separated by areas covered with a thin solder film. The basis metal is not exposed, however.

dicing Separating a semiconductor wafer into individual dies.

die Integrated circuit chip as cut (diced) from finished wafer. (See **chip.**)

die bond Mechanical attachment of the silicon die or chip to the substrate usually by solder, epoxy, or gold-silicon eutectic. The die bond is made to the back (inactive) side of the chip with the circuit side (face) up.

die pick-and-place machine A die-sort system designed specifically to (1) remove (pick) previously tested semiconductor devices automatically out of a scribed, diced, or broken wafer mounted on a taut plastic tape and (2) transfer each individual good die for deposition into a consecutive cavity of a specific storage container.

dielectric Material that does not conduct electricity. Generally, *dielectric* refers to materials that are to be used as capacitors, whereas *insulators* refers to materials that are primarily used as electrical insulators. Both materials can serve as either or both and the terms are often used interchangeably.

dielectric breakdown The complete failure of a dielectric material characterized by a disruptive electrical discharge through the material due to a deterioration of material or an excessive sudden increase in voltage.

dielectric constant The ratio of the capacitance, C_x, of a given configuration of electrodes with a specified dielectric, to the capacitance, C_v, of the same electrode configuration having a vacuum (or air) as the dielectric.

Micron Ex. 1026, p. 84
Micron v. YMTC
IPR2024-00911

dielectric loss Electric energy transformed into heat in a dielectric subjected to a changing electric field.

dielectric strength The maximum voltage that a dielectric can withstand, under specified conditions, without resulting in a voltage breakdown (usually expressed as volts per unit dimension).

diffusion bonds Processes accomplished by bringing two conductors to be joined into intimate contact and inducing the atoms of one material to diffuse into the structure of the other.

digitizing Any method of reducing feature locations on a flat plane to give digital representation of x-y coordinates.

dimensional stability A measure of dimensional change caused by such factors as temperature, humidity, chemical treatment, age, or stress (usually expressed as delta units per unit).

dip soldering A process in which printed boards with attached components are brought in contact with the surface of a static pool of molten solder for the purpose of soldering the entire exposed conductive pattern and the component leads in one operation.

Direct Chip Attach (DCA) A name applied to any of the chip-to-substrate connections used to eliminate the first level of packaging. (See also **Chip-on-Board.**)

direct emulsion A sensitized liquid coating for producing stencil screens. The material is applied to the screen mesh before exposure and development.

direct emulsion screen A screen whose emulsion is applied by painting directly onto the screen, as opposed to the indirect-emulsion type.

discrete component Individual components or elements, such as resistors, capacitors, etc., that are handled discretely, as opposed to those that are made by screen printing or other deposition methods as parts of a hybrid network.

Distance to Neutral Point (DNP) The separation of a joint from the neutral point on a chip. This dimension controls the strain on the joint imposed by the expansion mismatch between chip and substrate. The neutral point is usually the geometric center of an array of pads and defines the point at which there is no relative motion of chip and substrate in the X-Y plane during thermal cycling.

distributed network A network in which the parameters of resistance, capacitance, and inductance cannot be considered localized at any one point in the network.

doctor blade A method of casting slurry into a thin sheet by the use of a knife blade placed over a moving carrier to control slurry thickness.

double-sided substrate A substrate carrying active circuitry on both its topside and bottomside, electrically connected by means of metallized through-holes, edge metallization, or both.

drag soldering A process in which supported, moving printed circuit (wiring) assemblies are brought into contact with the surface of a static pool of molten solder.

Micron Ex. 1026, p. 85
Micron v. YMTC
IPR2024-00911

drift Permanent change in value of a capacitor or resistor over a period of time because of the effects of temperature, aging, humidity, etc.

drill smear While drilling holes in printed boards, a drill's temperature may exceed the glass transition temperature (T_g) of the dielectric material, resulting in melting. The melts are smeared across the hole walls and copper interconnect surfaces by the penetration and extraction of the drill bit. The smear can be several micrometers thick and interfere with the forming of reliable internal plane connections.

driver The off-chip circuit that supplies the signal voltage and current to the package lines. Also called an *output buffer circuit.*

dross Oxide and other contaminants that form on the surface of molten solder.

dry film For printed board imaging operations, a photopolymer that is coated onto a carrier sheet, which in turn is laminated to the surface of the board.

dry pressing Pressing and compacting together of dry powdered materials with additives in rigid die molds under heat and pressure to form a solid mass, usually followed by sintering to form shapes.

Dual-in-Line Package (DIP) A package having two straight, parallel rows of leads extending at right angles from the base and having standard spacings between leads and between rows of leads.

ductility The capability of a material to deform plastically before fracturing.

duty cycle A statement of energized and deenergized time in repetitious operation; for example, x sec on and y sec off.

dynamic contact resistance A change in contact electrical resistance due to a variation in contact pressure on contacts mechanically closed.

dynamic flex A form of flexible circuitry developed for applications where continued flexure is necessary. In contrast, static flex, once installed, remains fixed.

E glass A low-alkali lime-alumina-borosilicate glass, noted for its good electrical and mechanical properties. Substantially used in making fabric for printed circuit boards.

edge connected module A functional package (containing devices) that is connected to the next level of package on one edge, usually by plugging into a connector socket (although it could also be soldered in place).

edge connector A connector designed specifically for making removable and reliable interconnections between the edge of a printed board and the next level package.

edge definition The fidelity of reproduction of a pattern edge relative to the production master.

edge metallization The metallization applied to the edge of a substrate, wraparound fashion, such that it establishes an electrical connection between circuitry on the top and bottom of the substrate.

edge spacing The distance between a pattern, component, or both, from the edges of the printed board.

Micron Ex. 1026, p. 86
Micron v. YMTC
IPR2024-00911

elastomer Any elastic, rubberlike substance, such as natural or synthetic rubber. Silicon rubber is one of the most commonly used elastomers.

electrode A conductor through which a current enters or leaves an electrolytic cell, arc furnace, vacuum tube, gas-discharge tube, or other nonmetallic conductor.

electrodeposited (ED) copper ED copper is made in one of two ways: (1) a thin layer of copper is deposited by sputtering or electroless plating on a material and then electroplated up to the final desired thickness; (2) copper is continuously electroplated on a smooth, slowly turning stainless steel (cathode) drum. The deposited-foil thickness is controlled by the speed of the drum's rotation; foil is peeled continuously from the surface of the drum as it emerges from the plating solution. The surface closest to the drum is smooth and even, but the side exposed to the electroplating bath has a pronounced roughness.

electrodeposition The deposition of a conductive material from a plating solution by the application of electrical current.

electroformed mask Usually a trimetal structure in which a core material is selectively electroplated on both sides with a dissimilar metal. The core is then etched back to form a mesh pattern on one side and a stencil cavity on the reverse.

electroless deposition The deposition of conductive material from an autocatalytic plating solution without the application of electrical current.

electroluminescence The direct conversion of electrical energy into light.

electrolysis The separation of chemical components by the passage of current through an electrolyte.

electrolyte Current-conducting solution (liquid or solid) between two electrodes or plates of a capacitor, at least one of which is covered by a dielectric film.

electrolytic cleaning Cleaning in which a current is passed through a solution; the part is set up as one of the electrodes.

electrolytic corrosion Corrosion by means of electrochemical action.

electrolytic tough pitch A term describing the method of raw copper preparation to ensure a good physical- and electrical-grade copper-finished product.

Electromagnetic Compatibility (EMC) A package that has built-in electrically conductive shielding to prevent the escape of electromagnetic radiation. Government standards are available that specify allowable radiation losses.

electromigration The electrolytic transfer of metal from one conductor to another that is separated from the first by a dielectric medium through which the ions move under d-c potential.

electron-beam bonding Bonding two conductors by means of heating with a stream of electrons in a vacuum.

electron-beam patterning E-beam, or EB, patterning of resist by evaporation of the resist material from the heat supplied by the energy of a narrowly focused electron beam.

Micron Ex. 1026, p. 87
Micron v. YMTC
IPR2024-00911

electronic packaging The technology of interconnecting semiconductor and other electronic devices to provide an electronic function. An electronic package supplies the means for interconnecting power and signal terminals, mechanical stability and protection, and a path for thermal management so that it will both survive and perform under a plurality of environmental conditions.

electronic shielding A physical barrier, usually electrically conductive, designed to reduce the interaction of electric or magnetic fields upon devices, circuits, or portions of circuits.

electroplate The application of a metallic coating on a surface by means of electrolytic action.

electrostatic discharge Discharge of static charge on a surface or body through a conductive path to ground.

element A topologically distinguishable part of a microcircuit that contributes directly to its electrical characteristics.

emitter-coupled logic A nonsaturating form of bipolar logic in which the emitters of the input logic transistors are coupled with the emitter of a reference transistor. Also known as *current-switch logic.*

emulsion The organic material used to coat and/or plug the mesh of a screen to form a circuit pattern.

encapsulate Sealing or covering an element or circuit for mechanical and environmental protection. Typical encapsulating materials are potting, glob top, and molding compounds.

encroachment Solder mask on lands or surface-mount device pads, via bleeding, smearing, or misregistration.

End of Life (EOL) The end of the useful operating life of a component or equipment determined by a "wear-out" or life-terminating mechanism measured in units of time. EOL is usually specified as an objective in reliability calculations.

Engineering Change (EC) A change in design. An electrical design change is frequently implanted by cutting out or adding an electrical path to the manufactured hardware, e.g., laser deleting a line or adding a wire on a ceramic substrate.

escape wiring See **fanout wiring.**

etch factor The ratio of the depth of etch (conductor thickness) to the amount of lateral etch (undercut).

etchant A solution used to remove, by chemical reaction, the unwanted portion of material from a printed board.

etchback A process for the controlled removal of nonmetallic materials from the sidewalls of holes to a specified depth. The process is used to remove resin smear and to expose additional internal conductor surfaces.

etched metal mask A mask formed by etching apertures through a solid metal protected by a photoresist.

Micron Ex. 1026, p. 88
Micron v. YMTC
IPR2024-00911

etched printed board A board having a conductive pattern formed by the chemical removal of unwanted portions of the conductive foil. (See also **subtractive process.**)

etching A process by which a printed pattern is formed by either chemical or chemical and electrolytic removal of the unwanted portion of conductive material bonded to a base.

eutectic The minimum melting point of a combination of two or more metals or ceramics. The eutectic temperature of a system (if one exists) is always lower than the melting point of any of the individual components of the system.

External Thermal Enhancement (ETE) The mechanical member of the package that conducts heat away from the outside case of the package. This is usually a thermally conductive material (e.g., a heat sink) that is attached to the external surface of a module and projects into an air stream.

external thermal resistance A term describing the thermal resistance from a convenient point of the outside surface of an electronic package to an ambient reference point.

exothermic Characterized by the liberation of heat.

exposure The product of light intensity and time; the total amount of light striking a given area of photographic material.

external leads Electronic package conductors for input and output signals, power and ground.

face-down bonding A method of attaching a component or circuit chip to a substrate by inverting the chip and bonding the chip contacts to the mirror image contact points on the substrate. The pads or bumps that are used at the contact points may have originally been on either the chip or the substrate. The actual bonding process may be some type of thermocompression, ultrasonic, or solder technique. Also called *face bonding.*

failure The termination of the capability of an item to perform a required function.

failure criteria The specification limits beyond which the component is defined to fail to perform its required function.

failure mechanism A structural or chemical process, such as corrosion, carbon tracking, or fatigue, that causes failure.

failure mode Failure at the macro level; that is, the observed effect of failure. Examples include a "short," an open-circuit board, and system malfunction.

failure rate The rate at which devices from a given population can be expected (or were found) to fail as a function of time (e.g., percent per 1000 hours of operation).

fatigue Used to describe a failure of any structure caused by repeated application of stress over a period of time.

fatigue life The number of loading cycles of a specified nature that a design element can sustain before failing.

Micron Ex. 1026, p. 89
Micron v. YMTC
IPR2024-00911

fanout wiring The wiring layer that directly interconnects a device or small package to the next level of packaging. This may be simply a direct interconnection, but generally is used to describe wiring that "fans out" from the device/package to the wiring or via grid of the next level package. (See also **global wiring.**)

feed-through A connector or terminal block, usually having double-ended terminals that permit simple distribution and busing of electrical circuits.

ferroelectric A crystalline dielectric that exhibits dielectric hysteresis; an electrostatic analog to ferromagnetic materials.

Field Effect Transistor (FET) A transistor in which a voltage applied to a thin conductor over a thin insulator controls current flow in a semiconductor region (gate) of one polar type. This component originates and terminates in two regions of the opposite polar type located at either end of the gate region.

Field Replaceable Unit (FRU) A component or subsystem of an electronic assembly which may be replaced at the site of installation.

filler (1) A substance, often inert, added to a compound to improve properties and/or decrease cost. (2) A material used in a cable to fill large interstices where there are no electrical components.

film Single or multiple layers or coating of thin or thick material used to form interconnections and crossovers (conductors, insulators) or various elements (resistors, capacitors). Thin films can be deposited by vacuum evaporation or sputtering and/or plating. Thick films can be deposited by screen printing. Also, a term to describe thin, plastic sheeting.

film stress The compressive or tensile forces appearing in a film. Internal film stress is the intrinsic stress of a film related to its mechanical structure and deposition parameters. Induced film stress is the component of film stress related to an external force such as mismatched mechanical properties of the substrate.

final seal The manufacturing operation that completes the enclosure of the hybrid microcircuits so that further internal processing cannot be performed without delidding or disassembling the package.

fine leak A leak in a sealed package less than 10^{-6} cm^3/sec at 1 atmosphere of differential air pressure.

fine leak test A test to establish the integrity of a given device package by measuring the leak rate of the package under specified conditions. It usually employs a tracer gas as the test medium.

fingers The short lands containing the contact pads on a substrate to which the chip is bonded. In a flip-chip arrangement, such lands will contain a solder stop—a nonwettable organic or inorganic material to which solder will not adhere—to contain the solder and provide adequate height from chip to substrate.

fire The heating of a thick-film circuit or substrate so that the resistors, conductors, etc., or ceramic body are transformed into their final form.

Micron Ex. 1026, p. 90
Micron v. YMTC
IPR2024-00911

flame-off The procedure in which the wire is severed by passing a flame across the wire, thereby melting it. The procedure is used in gold wire thermocompression bonding to form a ball for making a ball bond.

flame retardant An inorganic or organic compound added to a polymer mixture that causes the resulting plastic to be self-extinguishing after a flame is removed.

flare The widened portion of a printed circuit line as it enters a land. Also, the undesirable enlarged, tapered area of a punched hole, typical of the side through which material exits during hole formation.

flash point The temperature to which a material must be heated to give off sufficient vapor to form a flammable mixture.

flat cable A cable with two or more parallel, round, or flat conductors in the same plane encapsulated by an insulating material.

flat conductor A wire manufactured in a flattened form, as opposed to round or square.

flatness The long-range deviation from planarity of a film surface, measured in micrometers/millimeter or mils/inch.

flatpack or **flat pac** An integrated circuit package having its leads extending from all four sides and parallel to the base.

flex life The ability of a design element, such as a conductor wire, cable, or flex circuit to withstand repeated bending. (See also **fatigue life.**)

flexible printed wiring (or flex circuit) A patterned arrangement of printed wiring using a flexible base material with or without flexible cover layers.

flip chip A chip that has bumped terminations spaced around the device and is intended for facedown mounting. (See also **facedown bonding.**)

flip-chip attachment A method of attaching a device to a substrate in which the device is flipped so that the connecting conductor pads on the face of the device are set on mirror-image pads on the substrate and bonded by reflowing the solder.

flood bar A bar or other device on a screen-printing machine that will drag pastes back to the starting point after the squeegee has made a printing stroke. The flood stroke returns the paste without pushing it through the meshes, so that it does not print but returns the paste supply to be ready for the next print.

flow soldering See **wave soldering.**

flush conductor A conductor whose outer surface is in the same plane as the surface of the insulating material adjacent to the conductor.

flux In soldering, a material that chemically attacks surface oxides so that molten solder can wet the surface to be soldered, or an inert liquid which excludes oxygen during the soldering process.

footprint The area needed on a substrate for a component or element. Usually refers to specific geometric pattern of a chip. (See also **land pattern.**)

Micron Ex. 1026, p. 91
Micron v. YMTC
IPR2024-00911

FR-4 Designation of the Electronic Industries Association for a fire-retardant epoxy resin-glass cloth laminate. By common usage, the resin for such a laminate.

frit Glass composition ground up into a powder form and used in thick-film compositions as the portion of the composition that melts upon firing to give adhesion to the substrate and hold the conductive composition together.

from-to list Written wiring instructions in the form of a list indicating termination points.

functional test An electrical test on a package, performed after all component assembly operations are completed, to ensure that the electronic function of the assembly conforms to desired criteria of operation.

fusing The melting of a metallic coating (usually electrodeposited) by means of a heat-transfer medium, followed by solidification.

gas blanket An atmosphere of forming gas flowing over a heated integrated-circuit chip or a substrate during bonding that keeps the metallization from oxidizing.

gate array A semicustom product, implemented from a fully diffused or ion-implanted semiconductor wafer carrying a matrix of identical primary cells arranged into columns with routing channels between them in the x and y directions.

gate, logic Usually an electric circuit which combines information of its two inputs to form its output signal in accordance to the logic function it performs.

gate, structural Term used to designate a hinged frame which contains a number of boards and can swing out for servicing and/or access to the interior of a fixed frame.

glass A hard, brittle substance, usually transparent, made by fusing silicates with soda, lime, etc.

glass-ceramic Inorganic, nonmetallic material obtained by controlled crystallization of glass into a nonporous and fine microstructure.

glass+ceramic Inorganic, nonmetallic material obtained by admixing crystalline ceramic with glass and sintering the composite.

glass fabric Cloth woven from glass yarns which are made of filaments.

glass transition temperature (T_g) In polymer or glass chemistry, the temperature corresponding to the glass-to-liquid transition, below which the thermal expansion coefficient is low and nearly constant, and above which it is very high.

glaze The glassy coating applied to the surface of a formed article or the material or mixture from which the coating is made.

glazed substrate A glass-coated ceramic substrate that effects a smooth and nonporous surface.

glob top A glob of encapsulant material (usually epoxy or silicone or combination thereof) surrounding a chip in the chip-on-board assembly process.

Micron Ex. 1026, p. 92
Micron v. YMTC
IPR2024-00911

global wiring Wiring interconnecting components mounted on a package (as opposed to the wiring connecting the components to the package. (See also **fanout wiring.**)

golden device A semiconductor device that has been fully characterized and meets all specification requirements (e.g., a "perfect" device), usually used as a test verification tool or to establish standards for the product.

green ceramic Unsintered ceramic, usually a ceramic-loaded organic system.

green density Density of a ceramic after composite pressing.

green sheet A composite organic-inorganic, flexible sheet ready for metallization, if desired, and lamination to form green ceramic entities which upon removal of organic (by firing or sintering) results in a ceramic substrate.

grid An orthogonal network of two sets of parallel equidistant lines used for locating points on a printed board.

ground A common reference point for circuit returns, shielding or heat sinking.

ground plane A conductor layer or portion thereof used as a common reference point for circuit returns, shielding or heat sinking.

ground plane clearance The etched portion of a ground plane around a through hole that isolates the plane electrically and mechanically from the hole.

gull wing A common lead form used to interconnect surface-mounted packages to the printed-circuit board. The leads, normally 100 to 250 microns thick, are bent outward, downward, then again outward from the package body, providing feet for solder interconnection, and some degree of mechanical compliance.

halation The spreading of light outside the intended area of exposure by reflection from the rear surface of the transparent base supporting the emulsion to be exposed.

haloing Mechanically induced fracturing or delamination on or below the surface of the base material; usually evidenced by a light area ("halo") around holes, other machined areas, or both.

hand cut Artwork that has been prepared without the use of a drafting machine.

hard-drawn copper wire Copper wire that has been drawn to size and not annealed.

hard glass Glasses having a high softening temperature (>700°C), such as the borosilicate glasses used to seal feedthrough leads into metal packages.

harness A term used to describe a group of conductors laid parallel or twisted by hand, usually with many breakouts, laced together or pulled into a rubber or plastic sheath, used to interconnect electric circuits.

HASL Acronym for Hot Air Solder Leveling—a technique for controlling the amount and height of solder on a package. The hot air melts (or keeps the solder molten after emerging from a bath) the solder and the velocity of the air forces excess solder off the package pads.

Micron Ex. 1026, p. 93
Micron v. YMTC
IPR2024-00911

HAST Acronym for Highly Accelerated Stress Test; usually used to describe a test in which components are placed in a pressure chamber and subjected to steam under one atmosphere or more of pressure at correspondingly high temperatures.

header The bottom portion of a device package to which the chip is attached and from which the external leads extend.

heat sink A thermally conductive material, usually metal, to which electronic components, their substrate, or their package are attached. This material has the ability to rapidly transmit heat from the generating source (component).

heel On a wire bond, the part of the lead adjacent to the bond that has been deformed by the edge of the bonding tool used in making the bond. The back edge of the bond.

hermetic Sealed so that the object is gastight. A plastic encapsulation cannot be hermetic as it allows permeation by gases.

hertz dot An intentionally raised area on a connector to concentrate the force within a contact interface, usually used to assist in breaking through oxides on a mating interface.

hertz stress The force divided by the deformed area in a contact system.

High Density Multichip Interconnect (HDMI) A high-density multichip module approach developed by General Electric. The chips are mounted in cavities in a substrate. A polyimide film is laminated to the face of the chips and a laser is used to etch via holes for contact to the chip bonding pads. A thin-film multilevel interconnect structure is built on the polyimide overlay to interconnect the devices and input/output pads.

high pot test A high voltage applied between two terminals seperated by an insulator. The voltage (typically between 100 and 1000 volts) is designed to be lower than the breakdown voltage of the insulator, but adequate to detect any leakage paths that may ultimately cause failure of the package.

hole breakout A condition in which a hole is not completely surrounded by the land.

hole cleaning The process for cleaning conductive surfaces exposed within a hole (e.g., removal of a resin smear).

hole density The quantity of holes in a printed board per unit area.

hole location The dimensional location of the center of the hole.

hole pattern The arrangement of all holes in a printed board with respect to a reference point.

hole pull strength The force necessary to rupture a plated-through hole or its surface terminal pads when loaded or pulled in the direction of the axis of the hole.

hole void A void in the metallic deposit of a plated-through hole that exposes the base material.

horn A cone-shaped member that transmits ultrasonic energy from a transducer to a bonding tool.

Micron Ex. 1026, p. 94
Micron v. YMTC
IPR2024-00911

hot dip Covering a surface by dipping the surface to be coated into a molten bath of the coating material.

hot-gas reflow The technique in which a heated gas, including air, is impinged on a site to be solder-reflowed, usually to form a solder interconnection.

hot-knife soldering The technique in which a heated blade (electrically or conductively) is used as a heat source for melting solder during package joining. The blade may be used to force mechanical contact throughout the joining process.

hot zone The part of a continuous furnace or kiln that is held at maximum temperature. Other zones are the preheat zone and the cooling zone.

hybrid circuit A circuit that uses two or more fabrication techniques to form the circuit, such as integrated circuit chips attached to a substrate having thin-film devices and conductors.

Hybrid Integrated Circuit (HIC) In general, any integrated circuit that is not monolithic. The term *hybrid* indicates that the circuit elements are made by two or more different technologies. A typical HIC consists of semiconductor chips and capacitors attached to a ceramic substrate carrying printed resistors and interconnections that are vacuum-evaporated or screen printed/fired.

hybrid microcircuit A microcircuit consisting of elements that are a combination of the film circuit type and the semiconductor type, or a combination of one or both of the types with discrete parts.

icicle See **solder projection.**

I-lead A surface-mounted device lead that is formed such that the end of the lead contacts the board pattern at a 90° angle. Also called a butt joint.

ILB Acronym for Inner Lead Bonding, which see.

immersion plating In galvanic displacement, the chemical deposition of a thin metallic coating over certain basis metals by a partial displacement of the basis metal.

impedance The ratio of the effective value of the potential difference between two terminals to the effective value of the current flow produced by that potential difference.

impingement cooling A method of cooling in which the air is mechanically directed from the cooling fan to strike (impinge) directly on the component to be cooled. Sometimes called *jet impingement.*

impregnant A substance, usually liquid, used to saturate an organic dielectric and to replace the air between its fibers and in pinholes. Impregnation usually increases the dielectric strength and the dielectric constant of the assembly.

impregnation In printed circuit boards, the process of coating the substrate (glass cloth) with a resin solution and drying. The dried product is called *prepreg.*

inclusion A foreign particle, metallic or nonmetallic, in a conductive layer, plating or base material.

Micron Ex. 1026, p. 95
Micron v. YMTC
IPR2024-00911

indirect-direct emulsion A combination film and sensitized-liquid system for producing stencil screens. Materials are applied to the screen mesh before exposure and development.

indirect emulsion A sensitized-film coating used for producing stencil screens. Materials are exposed and developed before application to the screen mesh.

indirect-emulsion screen A screen whose emulsion is a separate sheet or film of material, attached by being pressed into the mesh of the screen (as opposed to the direct-emulsion type).

inductance The property of an electric circuit whereby it resists any change of current during the building up or decaying of a self-induced magnetic field and hence produces a delay in current change, with resulting operational delay. In packaging systems, it is: (1) used in lumped equivalent circuits to represent part of a line discontinuity; (2) used in a distributed system to represent the electromagnetic storage property of a transmission line; and (3) the cause of delta I noise because it induces an opposing voltage in response to a change in current.

inert atmosphere A gas atmosphere such as helium or nitrogen that is nonoxidizing or nonreducing to metals.

infrared light-emitting diode An optoelectronic device containing a semiconductor pn junction that emits radiant energy in the 0.78- to 100-micrometer wavelength region when forward-biased.

Infrared Reflow (IR) The technique in which primarily long wavelength light is used to heat solder joints to the melting temperature. Normally, a circuit board having prepositioned packages is transported through an IR reflow furnace.

injection laser A solid-state semiconductor device consisting of at least one pn junction capable of emitting coherent or stimulated radiation under specified conditions. The device will incorporate a resonant optical cavity.

injection molded Molding by injecting liquefied plastic into a mold of desired shape.

Injection Molded Card (IMC) Card for electronic packages made by injection molding of plastics into a molded cavity of desired shape.

ink Synonymous with composition and paste when relating to screenable thick-film materials and with solder mask when referring to screen printing.

Inner Lead Bond (ILB) Refers to the electrically interconnecting wiring from the device to the next level package. (See also **outer lead bonding.**)

in process test A set of tests (usually nonfunctional) designed to assure integrity of each individual process involved (in constructing a package) to locate defects in construction at the process step where they are created.

input/output (I/O) terminal A chip or package connector (terminal) acting to interconnect the chip to the package or one package level to the physically adjacent level in the hierarchy. Usually refers to the number of contacts necessary to wire to or interconnect an assembly. Pin out, connections, and terminals are other common words to describe the same. Care must be taken to

Micron Ex. 1026, p. 96
Micron v. YMTC
IPR2024-00911

differentiate between the total number of I/Os between levels, signal I/Os, I/Os used to distribute power and reference I/Os.

insert (1) To assemble components, manually or automatically, into a printed board. (2) A part that holds the contacts in the proper arrangement and electrically insulates them from each other and from the shell. (See also **body.**)

insertion force For a contact system, the maximum force encountered while mating a printed board to a connector.

insulation A nonconductive material usually surrounding or separating two conductive materials.

Insulation Resistance (IR) The resistance to current flow when a potential is applied. IR is measured in megohms. Usually intended to evaluate the leakage integrity between interconnections that are supposed to be electrically isolated.

Insulator Metal Substrate Technology (IMST) A substrate, such as one made of porcelainized steel, which is not subject to size limitations and may have superior thermal dissipation characteristics. IMST refers to insulated-metal substrate technology of Sanyo. It is a single-sided aluminum core with epoxy coating and etched copper wiring.

insulators A class of materials with high resistivity. Materials that do not conduct electricity.

integrated circuit A microcircuit consisting of interconnected elements inseparably associated and formed in situ on or within a single substrate to perform an electronic circuit function.

interchip wiring The conducting wiring path connecting circuits on one chip with those on another chip to perform a function.

interconnection The joining of one individual device with another.

interface The borderline region between two different materials, for example, the region where a thick-film resistor composition and its connecting conductor composition meet, intermingle, react, and so on.

interlayer connection An electrical connection (i.e., plated through holes or via holes) between conductive patterns in different layers of a multilayer printed board. (See also **through connection.**)

intermetallic compound (1) An intermediate phase (a homogeneous phase whose composition range does not include any pure metal) in an alloy system that has a narrow range of composition but has an atomic bonding that can be of several types. (2) A stoichiometric compound whose properties differ considerably from those of the metals that make up the compound in terms of strength, brittleness, and hardness.

internal layer A conductive pattern that is contained entirely within a multilayer printed board.

internal resistance A term used to represent thermal resistance from the junction of a device, inside an electronic package, to a convenient point on the outside surface of the package.

Micron Ex. 1026, p. 97
Micron v. YMTC
IPR2024-00911

Internal Thermal Enhancement (ITE) A direct thermal path from the device to the package case, usually a thermal grease or metal "finger" between the backside of a flip-chip device that provides thermal enhancement inside the first-level package.

interposer To interpose is to place or come between two objects. In packaging, an interposer usually means an interconnection scheme that allows a set of fine-pitch connections (say on a chip) to connect to a second set of connections that is further apart (say on a lead frame). TAB tape is often used in this manner. In connectors, an interposer can provide a 1:1 interconnection from say, a leadless module, to a printed board (for example, an elastomeric connector).

interstitial via hole (1) A plated-through hole connecting two or more conductor layers of a multilayer printed board but not extending fully through all the layers of base material composing the board. (2) A metallized hole connecting two or more conductor layers in a package that is placed within the normal x-y via grid of the package.

invar A trade name (International Nickel Company, Inc.) for a very low thermal expansion alloy of nickel and iron.

ion migration The movement of free ions within a material or across the boundary between two materials under the influence of an applied electric field.

ionizable (ionic) contaminants Process residues, flux activators, fingerprints, and etching and plating salts, all of which exist as ions and, when dissolved, increase electrical conductivity.

irradiation The exposure of a material to high-energy emissions. In insulations, used to alter the molecular structure favorably.

isolation A technique for electrically separating circuit elements. In dielectric isolation, components are isolated by means of insulating layers. In diode isolation, components are isolated by means of reverse-biased pn junctions.

isopak A unique pin-grid array package (trademark of General Dynamics) consisting of kovar pins sealed in a glass-to-kovar plate flush for chip bonding.

JEDEC Acronym for Joint Electron Device Engineering Council. An Electronic Industries Association body that has published numerous standards for first-level packages.

J-lead A surface-mount integrated circuit package whose leads are formed into a J pattern, folding under the device body.

job A term used to indicate a batch of componentry started through a process as a single group having the same history.

jumper wire An electrical connection that is not part of the original design, added between two points on a printed board after the intended conductive pattern has been formed.

junction (1) A contact between two dissimilar metals or materials. (2) A connection between two or more conductors or two or more sections of a transmission line. (3) In solid-state materials, a region of transition between p- and n-type semiconductor materials as in a transistor or diode.

Micron Ex. 1026, p. 98
Micron v. YMTC
IPR2024-00911

key A device designed to ensure that the coupling of two components can occur in only one position.

keying slot A slot in a printed board that permits the board to be plugged into its mating receptacle, but prevents it from being plugged into any other receptacle. Also, in manufacturing, often used for locating the printed circuit board into a desired position (x, y and z) for photoprinting or drilling operations.

kiln High-temperature furnace used for firing ceramics.

Kirkendall voids The formation of voids by diffusion across the interface between two different materials, in the material having the greater diffusion rate into the other.

kovar An alloy of 53 percent iron, 17 percent cobalt, 29 percent nickel, and trace elements, with thermal expansion matching alumina substrates and certain sealing glasses. Most commonly used lead frame and pin material. Conforms to the ASTM designation F15.

laminate A product made by bonding together two or more layers of material under heat and pressure to form a single structure.

laminate void The absence of resin in an area that normally contains resin.

lamination The process of consolidating sheets of prepreg under heat and pressure to form a solid product. Applied also to the consolidation of prepregs and precircuitized subcomposites to form a composite.

land A portion of a conductive pattern that is usually, but not exclusively, used for the connection or attachment (or both) of components.

Land Grid Array package (LGA) See **Ball Grid Array Package.**

land pattern A combination of lands intended for the mounting of a particular component.

landless hole A plated-through hole or via without a land.

Large Scale Integration (LSI) Term used to describe semiconductor chips with more than 1000 circuits.

laser bonding Effecting a metal-to-metal bond of two conductors by welding the two materials together using a laser beam for a heat source.

laser soldering The technique in which heat to reflow a solder interconnection is provided by a laser.

lay-up The process of registering and stacking layers of a multilayer structure (e.g., PC board or multilayer ceramic module) in preparation for the laminating cycle.

leaching The migration of components of a substrate into working solution.

lead (1) That portion of an electrical component used to connect it to the outside world. (2) A conductive path, usually self-supporting. (3) A soft, heavy metal (chemical symbol Pb) that is used in solder compositions and other alloys.

Micron Ex. 1026, p. 99
Micron v. YMTC
IPR2024-00911

lead frame The metallic portion of the device package that completes the electrical connection path from the die or dice and from ancillary hybrid circuit elements to the outside world.

Lead on Chip (LOC) Refers to a package structure in which the inner leads (of a lead frame) are located on the chip so that the wires can be bonded inside the chip area. Package density and performance are greatly improved as wire bond sites do not have to be fixed around the edge of the chip, and power distribution can be optimized.

leaded chip carrier A plastic or ceramic chip carrier with compliant leads for terminations.

Leadless Chip Carrier (LCC) A chip carrier with integral metallized terminations and no compliant external leads.

leaf spring contact A leaf spring contact is a connector element consisting of a conductive member configured as a cantilever beam which applies force through the displacement of the beam.

lift-off Patterning of metal by removal or "lift-off" of surrounding materials usually in a solvent.

line See **conductor.**

line discontinuity A load point, consisting of a lumped equivalent circuit or resistance, capacitance, and inductance anywhere on a transmission line that produces spurious reflections.

line loading Externally connected resistance, capacitance and inductance, or combination thereof on a transmission line.

line resistance Resistance of conductor lines in a package, measured in ohms per unit length or for a given cross section, ohms per square.

lines per channel The number of conductive lines between vias in an organic board or ceramic substrate.

Liquid Crystal Display (LCD) Display technology based on liquid crystal materials whose light transmission is changeable by the application of an electrical field. LCD devices are used in numeric readouts and for flat-screen television receivers.

Logic Service Terminal (LST) A terminal (on a package or package component) carrying logic signals as opposed to one used only for electrical power.

loss factor A factor of an insulating material that is equal to the product of its dissipation and dielectric constant. The tangent of the angle between the real and imaginary current.

lot In manufacturing, this term is similar to a "job," but more than one job may be combined to make up a "lot."

low-loss dielectric An insulating material, such as polyethylene, that has relatively low dielectric loss, making it suitable for transmission of radio frequency energy.

Micron Ex. 1026, p. 100
Micron v. YMTC
IPR2024-00911

lossy signal line Distributed energy dissipative elements in a transmission line, such as series resistance, skin effect, and dielectric conduction.

lug A term commonly used to describe a termination, usually crimped or soldered to the conductor, with provision for screwing down to a terminal.

mask The photographic negative that serves as the master for making thick-film screens and thin-film patterns.

mass spectrometer An instrument used to determine the leak rate of a hermetically sealed package by ionizing the gas outflow, permitting an analysis of the flow rate in cm^3/sec at 1 atmosphere differential pressure.

master drawing A document that shows the dimensional limits or grid locations applicable to any or all parts of a printed board (rigid or flexible), including the arrangement of conductive and nonconductive patterns or elements; the size, type, and location of holes; and any other information necessary to describe the product to be fabricated.

Mean Time to Failure (MTTF) Applicable to individual parts or devices in reliability technology. It is the arithmetic average of the lengths of time-to-failure registered for parts or devices of the same type, operated as a group under identical conditions.

measling An internal condition occurring in laminated base material in which the glass fibers are separated from the resin at the weave intersections. This condition manifests itself in the form of discrete white spots or "crosses" below the surface of the base material and is usually related to thermally induced stress or chemical attack at the interface.

melt extrude To heat a material above its crystalline melt point and extrude it through an orifice.

meniscus In a solder joint, the minimum angle at which the solder tapers from the joint to the flat area of the conductor.

mesh In a mask, number of openings per lineal inch, measured from the center of any wire.

mesh porosity The amount of open area in a mesh versus the amount of closed area. Also expressed as *percentage of open area.*

mesh size The number of openings per inch in a screen. A 200-mesh screen has 200 openings per linear inch and 40,000 openings per square inch.

metal-clad base material (metal clad laminate) Base material covered with foil on one or both of its sides.

metal migration An undesirable phenomenon whereby metal ions, notably silver, are transmitted through another metal or across an insulated surface, in the presence of moisture and an electrical potential.

Metal-Oxide Semiconductor (MOS) A method of construction distinguishes this type of integrated circuit from bipolar integrated circuits. MOS integrated circuits are slower than bipolar integrated circuits, but have the advantage of high circuit density and low cost. The metal acts as a capacitor plate which, when charged across the oxide, draws the opposite charges to the semiconductor surface (i.e. electrons or holes) and bends the conduction band into the conductive state.

Micron Ex. 1026, p. 101
Micron v. YMTC
IPR2024-00911

Metal-Oxide Semiconductor Field Effect Transistors (MOSFET) The basic element of MOS integrated circuits. An FET consists of diffused source and drain regions on either side of a p- or n-channel region, and a gate electrode insulated from the channel by silicon oxide.

metallization The process of applying a conductive metal film to the surface on an integrated circuit chip or a package base material.

Metallized Ceramic (MC) Ceramic (fired) substrate metallized with thick and/or thin metal films. (In IBM, metallized ceramic refers to a thin-film copper metallization on a fired alumina substrate).

MHO An electrical unit of conductivity that is the conductivity of a body with the resistance of one ohm.

microcircuit A small circuit having a high equivalent circuit element density that is considered to be a single part composed of interconnected elements on or within a single substrate and that performs an electronic circuit function. (This excludes printed wiring boards, circuit card assemblies, and modules composed exclusively of discrete electronic parts.)

microelectronics The area of electronic technology associated with or applied to the realization of electronic systems from extremely small electronic parts or elements.

micron An obsolete unit of length equal to a micrometer.

microsectioning The preparation of a specimen for the metallographic examination of the material to be examined (usually by cutting out a cross section, followed by encapsulation, polishing, etching, staining, and so on).

microstrip A type of transmission line configuration that consists of a conductor over a parallel ground plane, separated by a dielectric.

microstructure Structural features, such as crystal or phase boundaries, or defects or inhomogeneities within a solid, usually resolved at high magnification.

microwave A short electrical wave, usually a wavelength of less than 300 mm (12 in) or over 1000 MHz.

microwave integrated circuits Distributed passive elements (resistors, capacitors) and interconnections that are used as transmission line components at microwave frequencies and that use the convenience of the open-face nature of the microstrip structure and build them into a compact unit along with the active devices.

mill (1) A machine for grinding or mixing material, for example, a ball mill and a paint mill. (2) Grinding or mixing a material, for example, milling a thick-film composition.

minimum annular ring The minimum width of metal, at the narrowest point, between the edge of the hole and the outer edge of the land. This measurement is made to the drilled hole on internal layers of multilayer printed boards and to the edge of the plating on outside layers of multilayer boards and double-sided boards.

Micron Ex. 1026, p. 102
Micron v. YMTC
IPR2024-00911

minimum electrical spacing The minimum allowable distance between adjacent conductors that is sufficient to prevent dielectric breakdown, corona, or both between the conductors at any given voltage and altitude.

mismatch A termination having a different impedance from that for which a circuit or cable is designed.

misregistration The lack of dimensional conformity between successively produced features or patterns.

module A chip carrier on which the chip terminals are fed out by various means to terminals spaced to suit the spacing and dimensions of wires on the next higher level of package (i.e., card or board). It may also contain wiring planes and power planes interconnecting several of its chips, and thus be equivalent to a card. A separable unit in a packaging scheme.

modulus of elasticity The ratio of stress to strain in an elastic material.

mold release An organic compound added to a molding compound or powder that migrates to the mold surface to form a waxy layer between the plastic and mold metal and to allow easy removal of the part from the mold.

monolithic integrated circuit An integrated circuit consisting of elements formed on or with a semiconductor substrate with at least one of the elements formed within the substrate.

Monolithic Systems Technology (MST) A hybrid ceramic package technology manufactured in IBM by screen-printing silver palladium conductors onto alumina substrates with pins attached by swaging techniques and chips bonded with solder connections (C4).

monomer A term denoting a single property or ingredient. A molecule of low molecular weight used as a starting material for polymerization to produce molecules of larger molecular weight, called polymers.

mother board A printed board assembly used for interconnecting arrays of plug-in electronic modules or cards.

M-quad® Trademark of Olin Corp. Particular design of a quad flat pack having a metal case for improved thermal properties.

Multichip Module (MCM) A module or package capable of supporting several chips on a single package. The industry recognizes three types of multichip modules depending on their construction:

MCM-C Modules constructed on cofired ceramic substrates using thick-film (screen-printing) technologies to form the conductor patterns.

MCM-D Modules whose interconnections are formed by the thin-film deposition of metals on deposited dielectrics, which may be polymers or inorganic dielectrics.

MCM-L Modules using advanced forms of printed wiring board (PWB) technologies to form the copper conductors on plastic laminated-based dielectrics.

multichip package An electronic package that carries a number of chips and interconnects them through several layers of conductive patterns. Each one is separated by insulative layers and interconnected via holes.

Micron Ex. 1026, p. 103
Micron v. YMTC
IPR2024-00911

multifilament mesh Woven material with multiple-strand threads.

Multilayer Ceramic (MLC) Ceramic substrate consisting of multiple layers of metals and ceramics interconnected with vias. All with thick film wiring.

multilayer printed board The general term for completely processed printed circuit or printed wiring configurations consisting of alternate layers of conductive patterns and insulating materials bonded together, with conductive patterns in more than two layers, and with conductive patterns interconnected as required. The term includes both flexible and rigid organic multilayer boards and ceramic multilayer boards used to interconnect arrays of integrated circuits.

multiple-image production master A production master that is used in the process of making two or more printed boards simultaneously.

mutual capacitance Capacitance between two conductors when all other conductors, including ground, are connected together and then regarded as an ignored ground.

nail head bond See **ball bond.**

nail heading Term to describe the ductile deformation of the land pattern in a PCB where the drill bit has punched through the copper plane.

negative Artwork, artwork master, or production master in which the intended conductive pattern is transparent to light, and the areas to be free from conductive material are opaque.

negative-acting resist A resist that is polymerized (hardened) by light and that, after exposure and development, remains on the surface of a laminate in those areas that were under the transparent parts of a production master.

net A group of terminals interconnected to have a common dc electrical potential in a package.

nick A cut or a notch in a wire or conductor.

NIP A PCB with No Inner Plane, but with two surface planes of interconnections.

nonfunctional land A land on an internal or external layer that is not connected to the conductive pattern on its layer. But, it may be used for test purposes by connection through a via to the other surface of a card or NIP allowing all circuits to be tested from just one side.

nonwetting (1) The lack of metallurgical wetting between molten solder and a metallic surface due to the presence of a physical barrier on the metallic surface. (2) A condition in which a surface has contacted molten solder, but the solder has not adhered to all of the surface; basis metal remains exposed.

off-contact In printing, the opposite of contact printing in that the printer is set up with a space between the screen and the substrate.

offset land A land that is intentionally not in physical contact with its associated component hole.

ohm A unit of electrical resistance, the resistance being that of a circuit in which a potential difference of one volt produces a current of one ampere.

Micron Ex. 1026, p. 104
Micron v. YMTC
IPR2024-00911

ohmic contact A contact between two materials across which the voltage drop is the same regardless of the direction of current flow.

oil canning The movement of entry material in the "z" direction during drilling in concert with the movement of the pressure foot.

OLB See **Outer Lead Bonding.**

opaquer A material that, when added to the resin system, renders the laminate sufficiently opaque that the yarn or weave of the reinforcing material cannot be seen with the unaided eye, using either reflected or transmitted light.

optical interconnection Components and modules composed of optoelectronic devices that are used as circuit building blocks. Interconnections consist of the conversion of electrical energy to light and vice versa through optoelectronic elements.

optoelectronic device A device that detects and/or is responsive to electromagnetic radiation (light) in the visible, infrared, and/or ultraviolet spectra regions; emits or modifies noncoherent or coherent electromagnetic radiation in these same regions; or utilizes such electromagnetic radiation for its internal operation.

Outer Lead Bonding (OLB) The process of joining the outer leads of a package to the next level of assembly.

outgassing Deaeration or other gaseous emission from a printed board assembly (printed board, component, or connector) when exposed to a reduced pressure, or heat, or both.

outgrowth The increase in conductor width at one side of a conductor, caused by plating buildup over that delineated on the production master.

overcoat A thin film of insulating material, either organic or inorganic, applied over circuit elements to provide mechanical protection and/or prevent contamination.

overglaze A glass coating over another component or element, normally used to give physical or electrical protection.

overhang The sum of outgrowth and undercut. If an undercut does not occur, only the overhang is the outgrowth.

overheated solder connection A solder connection characterized by solder surfaces that are dull, chalky, grainy, and porous or pitted.

overlay One material applied over another material.

Overmolded Pad Array Carrier (OMPAC) A new type of solder ball I/O package developed by Motorola. The OMPAC is made from a BT resin substrate, with bottom side solder balls attached, typically on a 0.040- to 0.060-in grid. After device attach, the substrate is overmolded (transfer molding only on the die side of the package).

ozone test Exposure of material to a high concentration of ozone to give an accelerated indication of degradation expected in normal environments.

package In the electronics/microelectronics industry, an enclosure for a single element, an integrated circuit, or a hybrid circuit. It provides hermetic or

Micron Ex. 1026, p. 105
Micron v. YMTC
IPR2024-00911

nonhermetic protection, determines the form factor, and serves as the first-level interconnection externally for the device by means of package terminals. A package generally consists of a bottom part, called the case or header, and a top part, called the cover or lid. These are sealed into one unit. Passive parts may be enclosed in an encapsulant or molded package.

package delay Time delays associated with the interconnections between components in circuits that make up a logical function.

packaging density Quantity of functions (components, interconnection devices, mechanical devices) per unit volume, usually expressed in qualitative terms, such as high, medium, or low.

packaging level A member of a nested interconnected packaging hierarchy (e.g., chip, chip carrier, card, board in order—low to high level).

pad The metallized area on a substrate or on the face of an integrated circuit used for making electrical connections. (See also **land.**)

pad-grid array package See **ball grid array package.**

panel A rectangular or square base material of predetermined size intended for or containing one or more printed boards.

parasitic An inductive, resistive, or capacitive contribution to a circuit that arises from the circuit configuration, as opposed to the design values of deliberately introduced components. Examples are the inductance of conductors, the resistance of interconnections and contacts, and the capacitance between conductors or between regions with a component.

passivation The formation of an insulating layer directly over the semiconductor surface to protect the surface from contaminants, moisture, or particles. Usually an oxide of the semiconductor is used; however, deposition of other materials is also used.

passive chip components Resistor, resistor array, capacitor, and inductor chips, of thick- or thin-film (multilayer) construction, intended for surface mounting on printed boards or hybrid substrates, having top or back electrical contacts, or both.

passive components (elements) An electronic circuit element that displays no gain or control, such as a resistor, inductor, or capacitor.

paste Synonymous with composition and ink when relating to screenable thick-film materials.

pattern The configuration of conductive and nonconductive materials on a panel or printed board. Pattern also denotes the circuit configuration on related tools, drawings, and masters.

pattern plating The selective plating (usually electrolytic) of a conductive layer into a photoresist pattern.

peel bond Similar to lift-off of the bond, with the separation of the lead from the bonding surface proceeding along the interface of the metallization and substrate insulation rather than the bond-metal surface.

peel strength The force per unit width required to peel the conductor or foil from the base material.

Micron Ex. 1026, p. 106
Micron v. YMTC
IPR2024-00911

permanent mask A resist that is not removed after processing (for example, plating resist used in the fully additive process).

permeability The property of a material, such as solid plastic, that allows penetration by a liquid or gas.

phase diagram State of a metal alloy or ceramic over a wide temperature range. The phase diagram is used to identify phases as a function of composition and temperature.

Phosphosilicate Glass (PSG) Phosphorous-doped silicon dioxide (also known as *P-glass*). It is often used as a dielectric material for insulation between conducting layers, for inhibiting the diffusion of sodium impurities, and for planarization since it softens and flows at 1000 to 1100°C to create a smooth topography for subsequent operations.

photographic reduction dimension A dimension (for example, the distance between lines or between two specified points) on the artwork master to indicate to the photographer the extent to which the artwork master is to be photographically reduced. (The value of the dimension refers to the 1:1 scale and must be specified.)

photolithography The use of light or ultraviolet rays through a mask to define circuit conductor patterns.

photopolymer A polymer that changes characteristics when exposed to light of a given frequency.

photoresist A photosensitive coating that is applied to a laminate and subsequently exposed through a photo tool (film) and developed to create a pattern that can be either plated or etched.

photosensitive Sensitive to light.

phototransistor A transistor (bipolar or field effect) that is used to detect light or that has been optimized for light sensitivity. The base region or gate may or may not be connected to an external terminal.

physical design The mechanical layout of the package including device and circuit element placement.

pick-and-place The mechanical process of selecting and placing chips on the correct substrate site in preparation for joining (interconnecting) the chip to the substrate.

piezoelectric Electricity or electric polarization caused by stress.

pin Electrical terminal and/or mechanical support that has a round cross section.

pin density The quantity of pins on a printed circuit board per unit area.

pin-grid array A package or interconnect scheme, featuring a multiplicity of plug-in type electrical terminals arranged in a prescribed matrix format or array. Used with high input/output-count packages.

pinhole A small hole occurring as an imperfection that penetrates entirely through a layer of material.

Micron Ex. 1026, p. 107
Micron v. YMTC
IPR2024-00911

pin-in-hole mounting Method of assembly of printed boards whereby the component pins are inserted through holes in the board and mechanically secured before being soldered in place.

pink ring The change in color around a copper pattern where it has lost adhesion to a polymer due to chemical intrusion of the interface oxide layer.

Pin-Through-Hole (PTH) Refers to the class of packages or modules whereby the leads are soldered in plated through holes in the next level package (usually a printed circuit board).

pit A small hole occurring as an imperfection that does not penetrate entirely through the foil.

pitch The nominal distance from center to center of adjacent conductors. Where conductors are of equal size and spacing is uniform, the pitch is usually measured from the reference edge of the adjacent conductor.

placement The actual placing of chip circuits, chips, chip carriers and/or cards in the desired location on corresponding images for a given package level.

plain weave Mesh pattern in which the filaments are woven with one over, one under.

planar package Usually refers to a simple system having one card (sometimes two cabled together) which holds all the modules or electronics for the system. Larger systems usually use Card-on-Board (COB) packaging where several cards are plugged edgewise into a back-panel printed board.

plasma etching The action of an electrically conductive gas, or plasma (composed of ionized gas or molecules), to remove unwanted portions of conductive or insulative pattern.

plastic A polymeric material, either organic, such as epoxy and polyimide, or inorganic, such as silicone, used for conformal coating, encapsulation, or overcoating.

plastic ball grid array package A surface mount package consisting of a plastic substrate whose input/output connections consist of solder balls in an array on the bottom of the package. (See **ball grid array package.**)

plastic encapsulation Environmental protection of a completed circuit by embedding it in a plastic such as epoxy or silicone.

Plastic Dual In-line Package (PDIP) A molded plastic (over lead frame) package with leads on both sides that are all in alignment. Generally used for pin-through-hole type of assembly. (See also gullwing package.)

Plastic Leaded Chip Carrier (PLCC) A molded plastic and lead frame package designed for surface mount applications. The leads, which may be on all four sides of the package are formed in the shape of a "J."

plasticizer A chemical agent added in compounding plastics and/or ceramic "green" bodies to make them softer and more flexible.

plate finish In laminating, the finish present on the metallic surface of metal-clad base material resulting from direct contact with the laminating press plates without modification by any subsequent finishing process.

Micron Ex. 1026, p. 108
Micron v. YMTC
IPR2024-00911

plated-through hole A hole in which an electrical connection is made between internal and/or external conductive patterns, by the plating of metal on the wall of the hole.

plated-through hole structure test A visual examination of the metallic conductors and plated-through holes of a printed board after the glass-plastic laminate has been dissolved away.

plating (1) Metallic deposit on a surface, formed either chemically or electrochemically. (2) The process of the chemical or electrochemical deposition of metal on a surface.

plating bar The temporary conductive path interconnecting areas of a printed board to be electroplated, usually located on the panel outside the borders of such a board.

plating up The process consisting of the electrochemical deposition of a conductive material on the base materials (surface holes, and so on) after the base material has been made conductive.

plug The part of a connector that is normally removable from, or permanently mounted to, the other part; usually that half of a two-piece connector that contains the pin contacts.

pogo pin A pogo contact is a connector element that consists of a pin assembly containing an integral coiled spring which applies the contact force.

point-to-point wiring An interconnecting technique in which the connections between components are made by wires routed between connection points.

polar ingredient Any ingredient in a material or complex capable of ionization.

polar solvents Solvents with an electrical dipole that are capable of dissolving polar compounds and/or ionics.

polarization A technique of eliminating symmetry within a plane so that parts can be engaged in only one way in order to minimize the possibility of electrical and mechanical damage or malfunction.

polarized slot A slot at the edge of a printed board used to ensure proper insertion and location in a mating connector. (See also **keying slot.**)

polyimides A class of resin compounds containing the NH group which are derived from ammonia and are "imidized" from polyamic acid at temperatures high enough to initiate and complete the imide ring closure. Polyimides are often used as organic dielectric interlevel layers.

polymer A material having molecules of high molecular weight, formed by the polymerization of lower molecular weight molecules.

polymer thick film A class of materials, used for thick-film inks and polymer-based substrates. Also, a technology in which conductive and resistive inks of a polymer base are screen-printed onto a dielectric to create a circuit.

polymerization A chemical reaction in which the molecules of a monomer are cross-linked to form large molecules whose molecular weight is a multiple of that of the original substance.

Micron Ex. 1026, p. 109
Micron v. YMTC
IPR2024-00911

porcelain A mixture of borosilicate glass with minor quantities of zirconia and other ingredients. Often referred to as *enamel.*

positive An artwork, artwork master, or production master in which the intended conductive pattern is opaque to light and the areas intended to be free from conductive material are transparent.

positive-acting resist A resist that is decomposed (softened) by light and that, after exposure and development, is removed from those areas that were under the transparent parts of a production master.

pot life The length of time a two-part epoxy system remains useful, usually measured in hours; it can be extended by refrigeration.

potting See **encapsulate.**

power cycling Used for reliability testing of finished assemblies by the application of cyclic power to a heat-generating component in the assembly.

power distribution The network of conductors throughout the package which supplies the operating voltages and currents to the circuits.

prefire To fire one thick-film composition, for example, a conductor, before printing a second thick-film composition, for example, a resistor.

preform For soldering or adhesion functions, a form that is circular or square-shaped and is punched out of thin sheets of solder, epoxy, or eutectic alloy. The form is placed on the spot of attachment by soldering or by bonding prior to placing the object there to be heated.

prepreg Sheet material, such as glass fabric impregnated with a resin cured to an intermediate stage (B-stage resin).

pressed alumina Aluminum oxide ceramic formed by applying pressure to the ceramic powder and a binder prior to firing in a kiln.

press-fit contact An electrical contact that can be pressed into a hole in an insulator, printed board (with or without plated-through holes), or a metal plate.

pressure contact Method of interconnection whereby the electrical path is maintained by means of a continually applied force (such as a spring) to the contact points.

print-through An undesirable condition that is typical with surface-mount designs on double-sided, noninner plane, rigid printed boards or cores, in which the image on one side is printed through the substrate to the other side.

printed board A general term for completely processed printed circuit or printed wiring configurations. It includes rigid or flexible boards (organic or ceramic) and single, double, and multilayer printed boards. (This definition and the definitions below are based on ANSI/IPC-T-50C, Ref. 1.)

printed wiring board A board with printed-on point-to-point connections (only).

printed circuit board A board with printed-on components as well as point-to-point connections.

printed board assembly A general term used to denote either a printed wiring assembly or a printed circuit assembly.

Micron Ex. 1026, p. 110
Micron v. YMTC
IPR2024-00911

printed circuit A conductive pattern comprising printed components, printed wiring, or a combination thereof, all formed in a predetermined design and intended to be attached to a common base.

printed component A part, such as an inductor, resistor, capacitor, or transmission line, that is formed as part of the conductive pattern of the printed board.

printed wiring The conductive pattern intended to be formed on a common base, to provide point-to-point connection of discrete components, but not to contain printed components.

printed wiring assembly A printed wiring board on which separately manufactured components and parts have been added.

probe A pointed conductor used in making electrical contact to a circuit pad for testing.

production master A 1:1 scale pattern that is used to produce one or more printed boards (rigid or flexible) within the accuracy specified on the master drawing. See also **single-image production master** and **multiple-image production master.**

profile In reference to firing, a graph of time versus temperature or, in a continuous thick-film furnace, of position versus temperature.

profilometer An instrument for measuring surface roughness.

propagation delay The time it takes a signal to leave the output terminal of one chip, travel across the package, and enter the input terminal of another chip.

pseudoplastic A characteristic of a fluid whereby its viscosity decreases as the shear rate is increased. This does not imply a change in behavior with time. This type of behavior is often obtained when solids are dispersed in organic vehicles (for example, thick-film compositions).

pulse soldering Soldering a connection by melting the solder in the joint area by pulsing current through a high-resistance point applied to the joint area and the solder.

purple plague One of several gold-aluminum compounds formed when bonding gold to aluminum and activated by reexposure to high temperature. Compound growth is highly enhanced by the presence of silicon to form ternary compounds. The compounds, which are purplish in color, are very brittle, potentially leading to time-dependent failure of the bonds.

pyrolyzed Of a material, characterized by gaining its final form by the action of heat (burning).

q The inverse ratio of the frequency band between half-power points (bandwidth) to the resonant frequency of the oscillating system. Refers to the electromechanical system of an ultrasonic bonder, or the sensitivity of the mechanical resonance to changes in driving frequency.

Quad Flat Pack (QFP) Ceramic or plastic chip carrier with leads projecting down and away on all four sides of a square package. Commonly used to describe chip carriers with gull wing leads.

Micron Ex. 1026, p. 111
Micron v. YMTC
IPR2024-00911

Quad In-line Package (QUIP) A diplike plastic package with leads coming out in two rows. Half of the leads are bent close to the body and the other half projected out for additional 1.27 mm before being bent down.

quick disconnect A type of connector that permits rapid locking and unlocking of two connector halves.

radiation (1) The combined process of emission, transmission, and absorption of thermal energy between bodies separated by empty space. (2) The emission of electromagnetic energy from an electrical signal in a conductor.

Radio Frequency Interference (RFI) Undesired conducted or radiated electrical disturbances, including transients, that may interfere with the operation of electrical or electronic communications equipment or other electronic equipment.

random mesh registration A mask or screen in which the mesh holes are not positioned in any specific location relative to the cavity pattern.

rated voltage That voltage at which a component can operate for extended periods without undue degradation or safety hazard.

reactance That part of an impedance of an alternating current circuit that is due to capacitance or inductance.

Reaction Injection Molding (RIM) A molding process where two (or more) streams of reactants are metered into a small mixing chamber where turbulent mixing breaks up the fluids into finely interspersed striations for faster reaction. The mixture is then delivered to a mold to complete the polymerization.

real estate The surface area of an integrated circuit or substrate. The surface area required for a component or element.

receptacle Usually, the fixed or stationary half of a two-piece multiple-contact connector. Also, the connector half, usually mounted on a panel and containing socket contacts.

receiver The off-chip circuit that accepts the signal voltages and currents from the package lines. Also called an *input buffer circuit.*

reflow soldering A process for joining parts by tinning the mating surfaces, placing them together, heating until the solder fuses, and allowing them to cool in the joined position.

registration The accuracy of concentricity or relative position of all patterns on any mask with the corresponding patterns of any other mask of a given device series when properly superimposed.

registration marks The marks on a wafer or substrate that are used for aligning successive processing masks. Also known as *alignment marks* or *fiducial marks.*

reliability A collective name for those measures of quality that reflect the effect of time in storage or use of a product, as distinct from those measures that show the state of the product at the time of delivery. Generally, it is the capability of an item to perform a required function under stated conditions for a stated period of time.

Micron Ex. 1026, p. 112
Micron v. YMTC
IPR2024-00911

Rent's rule An empirical relation, first recorded by E. Rent of IBM, which states that the number of used input/output terminals on a logic package is proportional to a fractional power of the number of subpackages interconnected in the package.

repairing The act of restoring the functional capability of a defective part without necessarily restoring appearance, interchangeability, or uniformity.

resin An organic polymer that cross-links to form a thermosetting plastic when mixed with a curing agent.

resin recession The presence of voids between the barrel of a plated-through hole and the wall of the hole, seen in microsections of plated-through holes in boards that have been exposed to high temperatures.

resin-rich area A significant thickness of a nonreinforced resin layer of the same composition as that within the base material.

resin smear Resin transferred from the base material onto the wall of a drilled hole, covering the exposed edge of the conductive pattern, normally caused by drilling.

resin-starved area An area in a printed board that has an insufficient amount of resin to wet out the reinforcement completely; evidenced by low gloss, dry spots, or exposed fibers.

resist Coating material used to mask or protect selected areas of a pattern from the action of an etchant, solder, or plating.

resistance The property of a conductor that opposes the flow of current by dissipating energy as heat. In packages, it causes voltage and current losses in signal and power distribution systems.

resistance soldering A method of soldering in which a current is passed through and heats the soldering area by contact with one or more electrodes.

resistivity The ability of a material to resist the passage of electric current either through its bulk or on a surface. The unit of bulk resistivity is the ohm-centimeter. The unit of surface resistivity or line resistance is the ohm. A convenient way to express the resistivity of film conductors is in sheet resistivity, which is the electrical resistance measured across the opposite sides of a square of deposited film material. Sheet resistivity is expressed in ohms per square.

resistor A device that offers resistance to the flow of electric current in accordance with Ohm's law: $R = E/I$, where R is resistance, E is voltage, and I is current.

resistor termination A thick-film conductor pad that overlaps and makes contact with a thick-film resistor area.

resolution The fineness of detail of a screen-printed pattern. The ability of photographic materials to reproduce fine detail.

reverse image The resist pattern on a printed board that allows the exposure of conductive areas for subsequent plating.

reversion A chemical reaction in which a polymerized material degenerates at least partially to a polymeric state lower than that of the original monomer.

Micron Ex. 1026, p. 113
Micron v. YMTC
IPR2024-00911

It is usually accompanied by significant changes in physical and mechanical properties.

rheology The science dealing with the deformation and flow of matter.

rifling Spiral groove or ridge in the substrate due to filling.

right-angle edge connector A connector that terminates conductors at the edge of a printed board, while bringing the terminations out at right angles to the plane of the board conductors.

rise time The time during which the leading edge of a pulse increases from 10 to 90 percent of its maximum amplitude.

roadmap A printed pattern of nonconductive material by which the circuitry and components are delineated on a board to aid in service and repair of the board.

roller coating Coating process in which liquid is transferred to a soft, grooved roller and then to the surface of a printed board.

rosin flux A flux having a rosin base that becomes interactive after being subjected to the soldering temperature.

roughness The microscopic peak-to-valley distances of film-surface protuberances and depressions, measured in angstroms.

routing program An automatic program containing an algorithm which "routs" or places prescribed wiring within a package. Usually used with printed circuit board layout.

rupture In breaking-strength or creep tests, the point at which a material physically comes apart.

sawtooth Small projections on the edge of a screen-printed pattern caused by fillets of emulsion left in the screen mesh and by the mesh itself.

screen A network of metal or fabric strands mounted snugly on a frame and upon which the film circuit patterns and configurations are superimposed by photographic means.

screen printing A process for transferring an image to a surface by forcing suitable media through a stencil screen with a squeegee. The synonym *silk screening* is a nonpreferential term.

screen tension The tautness of a mounted woven mesh, expressed in mils per unit of weight.

sealing Joining the package carrier base with its cover or lid into a sealed unit. For hybrids, sealing connotes an important finishing operation in fabricating a hybrid microcircuit, signaling the stage when the assembly, in the form of a populated package, becomes a bona fide hermetic (or nonhermetic) entity.

seeding The use of a colloid metal or compound to form metallic nuclei, which become the activated sites for initiation of plating (either electrolytic or electroless).

semiadditive process An additive process for obtaining conductive patterns that combines an electroless metal deposition on an unclad or thin-foil sub-

Micron Ex. 1026, p. 114
Micron v. YMTC
IPR2024-00911

strate with electroplating, etching, or both. (See also **additive process** and **subtractive process.**)

semiaqueous Aqueous chemistry with the addition of an organic solvent.

semiconductor device A device whose essential characteristics are governed by the flow of charge carriers within a semiconductor.

sensitizer Material used to activate a photographic resist to create chemical changes in it.

sequentially laminated multilayer printed board A multilayer board that is formed by laminating through-hole plated double-sided or multilayer boards together. The circuitry layers are interconnected with interstitial via holes and through connections.

Seraphim's theory States that the wiring capacity of a printed board is approximated by the following equation $W_c = 2.25N_tP$, where N_t is the number of terminals per device (module) mounted on the board and P is the pitch (spacing) between them.

shear rate With regard to viscous fluids, the relative rate of flow or movement.

sheath The material, usually an extruded plastic or elastomer, applied outermost to a wire or cable. Also called a *jacket.*

sheet resistance The electrical resistance of a thin sheet of a material with a uniform thickness as measured across opposite sides of a unit square pattern. Expressed in ohms per square.

shelf life The length of time a one- or two-part epoxy system can be stored before use, usually measured in months.

shell An outside case, usually metallic, into which the insert (body) and contacts are assembled. Shells of mating connector halves usually allow proper alignment and polarization and provide protection for projecting contacts.

signal An electrical impulse of predetermined voltage, current, polarity, and pulse width.

signal conductor An individual conductor used to transmit an impressed signal.

signal distribution The network of package conductors that interconnects the drivers and receivers.

signal plane A conductor layer intended to carry signals, rather than serve as a ground or in some other fixed-voltage function.

silk screening See **screen printing.**

silver migration The growth of silver (Ag) crystals between a silver bearing or coated conductor anode and a cathode a few mils apart in a circuit when a dc voltage is applied over a long period of time under conditions of high humidity. Alloying the Ag with a small quantity of a higher melting temperature metal greatly reduces this tendency. (See also **electromigration.**)

Micron Ex. 1026, p. 115
Micron v. YMTC
IPR2024-00911

simultaneous switch Two or more driver circuits on the same chip or nearby chips changing state in unison thereby creating switching noise on package lines and drawing current simultaneously. When there are many such circuits switching, the large in-rush of current may drag down the voltage at the device terminals creating so-called delta I noise (which see).

single chip module (SCM) A package supporting one chip, as opposed to a multichip which supports several.

single-image production master A production master used in the process of making a single printed board.

Single-In-line (SIP) A plastic molded lead frame package whereby all the leads come off one edge of the package in one uniform pattern (line).

Single In-line Memory Module (SIMM) Usually a small printed circuit board with eight or nine small outline memory modules with contacts on one long edge designed to plug into the next-level package.

Single-Layer Metallization package (SLAM) Ceramic leadless package without cavity, sealed by ceramic or glass to a ceramic cap.

single-sided board A printed board with a conductive pattern on one side only.

singulated A term used to describe the separation of packages produced in multiple or reel format into a single unit to aid in further processing.

sinter To heat without melting, to cause a refractory dielectric material to become a rigid body free of binders, contaminants, and so on.

skin effect At very high frequencies, current travels only on the surface layer of a conductor, not uniformly throughout; this region of current flow is called the *skin*. The skin depth is inversely proportional to the square root of the frequency.

skived tape Tape shaved in a thin layer from a cylindrical block of material.

slip casting See **tape casting.**

slivers Portions of plating overhang (solder, tin, gold, and so on) on conductor edges that are partially or completely detached.

slump A spreading of printed thick film or solder paste after screen printing but before drying. Too much slumping results in a loss of definition.

slurry A thick mixture of liquid and solids, the solids being in suspension in the liquid.

Small Outline J lead (SOJ) Small outline package with "J" leads for surface mount.

Small Outline Package (SOP) Also called *SOIC* (small outline integrated circuit package). A plastic molded lead frame package with leads on two sides similar to a dual-in-line package but smaller with leads on 1.27-, 1.0-, or 0.85-mm spacing. It is meant for surface mounting.

smear removal See **hole cleaning.**

Micron Ex. 1026, p. 116
Micron v. YMTC
IPR2024-00911

snap-off distance The screen printer distance setting between the bottom of the screen and the top of the substrate.

soak time The length of time a ceramic material, for example, a substrate or thick-film composition, is held at the peak temperature of the firing cycle.

socket contact A female contact designed to receive and mate with a male contact. It is normally connected to the live side of a circuit.

soft error A memory state error induced by a process which produces no permanent alteration of the physical condition of the memory device. Soft errors can be created by alpha particles passing through the device.

soft glass Glasses, typical high-lead content glasses, having a low softening points that could be used to seal ceramic or metal lids to packages below about 450C. Also called solder glasses because of their ability to wet most metal surfaces.

softening point Refers to the temperature at which the log viscosity of glass is 7.6 poises, as defined and measured to ASTM specification.

solder A low melting point alloy, usually of lead(Pb)-tin(Sn), that can wet copper, conduct current, and mechanically join conductors and so on.

solder balls Small spheres of solder adhering to laminate, mask, or conductor surfaces (generally after wave or reflow soldering).

solder bumps The round solder balls bonded to a transistor contact area and used to make connection to a conductor by face-down bonding techniques.

solder coat A layer of solder applied directly to the printed board conductive path from a molten solder bath.

solder column package Devised by IBM, this first level package looks identical to a ceramic pin grid array package. However, instead of hard metal pins, the input/output terminals consist of columns of solder up to 0.150″ long. The package is surface mounted to a printed circuit board by reflowing a selected amount of solder around the base of the columns. The long solder columns provide stress relief between the ceramic package and the board. It is designed for large ceramic chip carriers (e.g., 35 mm to 64 mm on a side).

solder connection An electrical/mechanical connection that employs solder for the joining of two or more metal parts.

solder cup terminal A metallic termination device that has a hollow, cylindrical feature, open on one end, to accommodate the soldering of one or more leads or wires.

solder dam A dielectric composition screened across a conductor to keep molten solder from spreading further onto solderable conductors.

solder eye A solder-type terminal provided with a hole at its end through which a wire can be inserted prior to being soldered.

solder fillet A blended or meniscoid (rounded) configuration of solder around a component or wire lead and land.

solder hierarchy In a complex package assembly, some components have to be assembled (soldered) before others, so these usually utilize a higher melting point solder than later assembled components. Ideally, if the assembly is sol-

Micron Ex. 1026, p. 117
Micron v. YMTC
IPR2024-00911

dered to a board, the board connection is made with the lowest melting point solder so that previous solder joints are not reflowed or negatively affected by the last joining process.

solder leveling A solder coating process in which heated gas or other media level and remove excess solder after the substrate is dipped in molten solder.

Solid Logic Technology (SLT) Ceramic package technology practiced by IBM in the 1960s by firing AgPd conductors onto dry-pressed and fired alumina substrate.

solder mask coating See **resist.**

solder plugs Cores of solder in the plated-through holes of a printed board.

solder projection An undesirable protrusion of solder from a solidified solder joint or coating. Also called *icicle.*

solder side On boards with components on one side only, the side of a printed board that is opposite the component side.

solder webbing A continuous film or curtain of solder that is parallel to, but does not necessarily adhere to, a surface pattern, or that is between separate conductive patterns that should be free of solder.

solder wicking The capillary rise of solder between individual strands of stranded wire.

solderability The ability of a conductor to be wetted by solder and to form a strong bond with the solder.

soldering A process of joining metallic surfaces with solder, without melting the base material.

soldering flux See **flux.**

soldering oil (blanket) Liquid formulations used in oil-intermix wave soldering equipment. Also used as pot coverings on still and wave solder pots to eliminate dross and reduce solder surface tension.

solderless wrap See **wire wrap.**

solid state Pertaining to circuits and components using semiconductors as substrates.

space transformer A package transforming a spatially dense set of chip connections to a less dense set of connection points on the next level package.

specific mesh registration A mask or screen in which the mesh holes are carefully aligned to correspond with the apertures of the stencil cavity.

spice A simulation program for integrated circuit analysis that is the industry standard for circuit simulation.

spinning A process for coating a smooth surface with a uniform film. Usually used to coat a semiconductor wafer with a photosensitive emulsion by placing the wafer on a rotating chuck and dropping the emulsion on the surface. The combination of centrifugal acceleration and adhesion of the liquid forms a uniform film of emulsion on the surface. Also used to provide thin coatings (for example, of polyimide dielectric) on package elements.

Micron Ex. 1026, p. 118
Micron v. YMTC
IPR2024-00911

splay The tendency of a rotating drill bit to drill off-center, out-of-round, nonperpendicular holes.

sputter cleaning Bombardment of a surface with energetic argon or other noble gas ions to clean the surface of oxide films and residues that could interfere with subsequent electrical or mechanical contact layers. The bombardment knocks off (or sputters) surface atoms to render the surface clean.

sputtering The ejection of particles from the surface of a material resulting from bombardment by ions and atoms. The material may be used as a source for deposition.

squeegee The block of a screen printer that pushes the liquid composition across the screen and transfers the images through the mesh onto the substrate.

stair stepping Irregular edge definition of a screen-printed pattern caused by interference between the mesh openings and the stencil cavity.

stamped printed wiring Wiring that is produced by die stamping and is bonded to an insulating base.

static flex Flexible wiring circuit carrier, which once installed, remains fixed.

stencil The emulsion or metal layer in which the image apertures are reproduced.

step exposure A technique in which a series of exposures is made to determine the optimum amount of time and distance required for exposing a photosensitive material with any given light source.

step soldering The technique for sequentially soldering connections using solder alloys with different melting temperatures.

stitch bond A thermocompression bond in which a capillary tube is used for feeding the wire and forming the bond.

storage temperature The temperature at which a device, without any power applied, is stored. Usually a maximum storage temperature is specified.

straight-through lead A component lead that extends through a hole in a printed board without subsequent forming of the lead.

strand A single, uninsulated wire.

strand lay The distance of advance of one strand of spirally stranded conductor, in one turn, measured axially.

stress corrosion Refers to the degradation of mechanical properties of brittle materials by crack propagation due to the acceleration of applied stress in the presence of corroding atmospheres such as water. The phenomenon exists in polymers as well as metals.

stress relief The formed portion of a component lead or wire lead, providing sufficient compliancy to minimize stress between terminations. Encapsulation with polymers can provide stress relief.

strip line A type of transmission line configuration that consists of a single, narrow conductor parallel and equidistant to two parallel ground planes. Also, a microwave conductor on a substrate.

Micron Ex. 1026, p. 119
Micron v. YMTC
IPR2024-00911

substrate In the hybrid industry, that which is used as a base material, usually aluminum oxide (alumina).

subtractive process A process for obtaining conductive patterns by the selective removal of unwanted portions of a conductive foil, usually by chemical etching.

supported hole A hole in a printed board, the inside surface of which is plated or otherwise reinforced.

Surface Mount Technology (SMT) A method of electrically and mechanically connecting components to the surface of a conductive pattern (e.g., as on a printed circuit board) without using through holes.

swaged leads (1) Component lead wires that extend through the printed board and are flattened, or swaged, to secure the component to the board during manufacturing operations. (2) Leads that are inserted through a ceramic substrate and then formed (swaged) to create a lead bulge on both the top and bottom of the substrate, providing a good mechanical joint to the substrate.

swimming Lateral shifting of a thick-film conductor pattern on molten-glass cross-over patterns. Also, lateral movement of etched inner-layer features during lamination of multilayer boards as a result of excess temperature or pressure or both.

switching noise An induced voltage on the power distribution system at the circuit terminals caused by the rapidly changing current involved in the simultaneous switching of many drivers.

Tape Automated Bonding (TAB) The process where silicon chips are joined to patterned metal on polymer tape (e.g., copper on polyimide) using thermocompression bonding, and subsequently attached to a substrate or board by outer lead bonding. Intermediate processing may be carried out in strip form through operations such as testing, encapsulation, burn-in, and excising the individual packages from the tape.

tape bonding The utilization of a metal or plastic tape material as a support to and carrier of a microelectronic component in a gang bonding process.

tape cable A form of multiple conductor consisting of parallel metal strips embedded in insulating material. Also called *flat, flexible cable.*

tape casting In the hybrid industry, the thin, tapelike appearance of ceramic slurry when poured, usually through a flattening device called a "doctor blade," after drying by evaporation of the suspension medium. This method results in long (can be hundreds of feet), thin (typically 5 to 25 mils), ceramic tape that can be cut to size for optimum processing, metallized, via holes punched and filled with metal, and laminated into multilayer structures for final firing. Also called *slip casting.*

taped components Components attached to continuous tape to facilitate automatic component incoming inspection, lead forming, assembling, and testing.

Tape Pak Trademark of National Semiconductor. Particular design of a quad flat pack.

Micron Ex. 1026, p. 120
Micron v. YMTC
IPR2024-00911

taper pin A pin-type terminal having a tapered end designed to be impacted into a tapered hole to form a connection.

taper tab A flat terminal having tapered sides designed to receive a mating tapered female terminal.

tarnish A discoloration or staining of a conductor or shield wire, caused by exposure to the atmosphere.

temperature coefficient of resistance The amount of resistance change of a material per degree of temperature rise.

tensile strength The greatest longitudinal tensile stress a substance can bear without tearing apart or rupturing.

tension set The condition in which a plastic material shows permanent deformation caused by a stress, after the stress is removed.

tenting A printed board fabrication method of covering over plated-through holes and the surrounding conductive pattern with resist, usually dry film.

terminal A metallic termination device used for making electrical connections.

terminal pad See **land.**

test board A printed board suitable for determining the acceptability of the board or of a batch of boards produced with the same process.

test coupon A portion of the quality conformance test circuitry used for a specific acceptance test or group of related tests.

test pattern A pattern used for inspection or testing purposes.

thermal aging Exposure to a given thermal condition or a programmed series of conditions for prescribed periods of time.

Thermal Conduction Module (TCM) An IBM multichip (100 chips or more) module that is cooled by thermal conduction of pistons in contact with the chips.

thermal conductivity The rate with which a material is capable of transferring a given amount of heat through itself.

thermal cycling A method whereby a cyclic stress is imposed on an assembly of microelectronic components by alternately heating and cooling in a chamber. It is used to accelerated reliability testing of components and assemblies.

thermal mismatch Difference in thermal coefficients of expansion of materials which are bonded together.

thermal resistance The thermal resistance of a unit cube of material.

thermocompression bonding (TC bonding) A process involving the use of pressure and temperature to join two materials by interdiffusion across the boundary.

Thermogravimetric Analysis (TGA) A technique that measures material weight change as a function of increasing temperature.

Thermomechanical Analysis (TMA) A technique that measures the linear expansion or other deformations of a material with respect to changes in temperature.

Micron Ex. 1026, p. 121
Micron v. YMTC
IPR2024-00911

thermoplastic A resin that is set into its final shape by forcing the melted base polymer into a cooled mold or through a die, after which it is cooled. The hardened polymer can be remelted and reprocessed several times.

thermoset A resin that is cured, set, or hardened, usually by heating, into a permanent shape. The polymerization reaction is an irreversible reaction known as *cross linking*. Once set, a thermosetting plastic cannot be remelted, although most soften with the application of heat.

thermosonic bonding (T/S) A bonding process which uses a combination of thermocompression (TC) bonding and ultrasonic bonding. It is done on what amounts to a gold-wire TC bonder with ultrasonic power applied to the capillary.

thick film A film deposited by screen printing processes having between 5 and 20 micrometer thickness, and fired at high temperature to fuse into its final form.

thin film Refers to coatings that generally range from a few (2–3) atomic layers to a few (1–5) micrometers in thickness. The key distinguishing feature from thick films is that thin films are usually deposited by evaporation, sputtering or chemical vapor deposition.

thin-film packaging An electronic package in which the conductors and/or insulators are fabricated using deposition and patterning techniques similar to those used for integrated circuit chips.

Thin Small Outline Package (TSOP) A small outline package (which see) whose thickness is much less than a standard package. TSOPs can range from 1.5 down to only 0.5 mm in thickness.

thixotropic Pertaining to the tendency of a fluid to decrease in viscosity as the time to exposure to a given shear rate increases. The shear stress versus shear strain rate curve of a thixotropic material should show a hysteresis loop. A purely pseudoplastic material will not give a hysteresis loop because this property is not time-dependent. Most thick-film pastes or inks are thixotropic.

three-layer tape An interconnection medium used in tape automated bonding (TAB), where the tape is comprised of three layers: metallization (usually copper), polymer (usually polyimide), and adhesive (usually epoxy) in between.

through connection An electrical connection between conductive patterns on opposite sides of an insulating base, such as a plated-through hole or clinched jumper wire.

through-hole mounting See **pin-in-hole mounting.**

tie bar See **plating bar.**

tinned Literally, coated with tin, but commonly used to indicate coating with solder.

tinning A process for coating metallic surfaces with a thin coat of solder.

to can See **transistor outline metal can package.**

tombstoning Term used to describe the lifting of one end of a component during surface mount solder reflow.

Micron Ex. 1026, p. 122
Micron v. YMTC
IPR2024-00911

tooling feature A specified physical feature on a printed board or panel such as a marking, hole, cutout, notch, slot or edge used exclusively to position the board or panel or mount components accurately.

tooling holes A general term for holes placed in a printed board or panel and used to aid in the manufacturing, assembly, or testing process.

Top Side Metallurgy (TSM) Refers to the metallization on the top side of a substrate to which a chip is joined.

Top Surface Metallurgy (TSM) The layer of conductive metal on the top of a substrate or package.

topography The surface condition of a film; bumps, craters, etc.

torque test A test designed to ascertain the stiffness of a material under given environmental conditions.

transfer molding An automated type of compression molding in which a preform of plastic (usually an epoxy-based resin) is poured from a pot into a hot mold cavity.

transfer soldering A soldering process using a hand soldering iron and a measured amount of solder in the form of a ball, chip, or disk.

transient mismatch Thermal mismatch between elements of a structure which, because of thermal lag, varies with time until reaching a steady state value.

transistor An active semiconductor device capable of providing power amplification and having three or more terminals.

Transistor Outline (TO) package An industry standard package designation established by JEDEC of EIA.

transistor outline metal can package In integrated circuits, a type of package resembling a transistor can but generally larger and having more leads. The pins are arranged in a circle in the base.

transmission cable Two or more transmission lines. If the structure is flat, it is called flat transmission cable to differentiate it from a round structure, such as a jacketed group of coaxial cables.

transmission line A signal-carrying circuit composed of conductors and dielectric material with controlled electrical characteristics used for the transmission of high-frequency or narrow-pulse signals.

trim (1) Of resistors, to change from the as-fired value to the final desired value, usually by removing parts of the body of the resistor (with abrasive particles—"sand blasting"—or with a laser). (2) To make adjustments in resistors, coils, capacitors (often by adding or replacing) to bring electrical performance into exact agreement with specifications.

trim lines Lines that define the borders of a printed board.

triplate structure In a printed board, a signal line may be sandwiched between two reference planes. Such a design is referred to as a *shielded stripline* or a *triplate structure.*

Micron Ex. 1026, p. 123
Micron v. YMTC
IPR2024-00911

true position The theoretically exact location of a feature or hole established by basic dimensions.

tuning fork contact A U-shaped female contact, either stamped or formed, so named because it resembles a tuning fork.

twill weave Mesh pattern in which the filaments are woven with one over, two under.

two-layer tape A form of tape fabrication for tape automated bonding (TAB), whereby the copper metallurgy is directly deposited on the Kapton carrier tape (i.e., no adhesive is used in bonding the copper).

Ultra Large Scale Integration (ULSI) So far, an extreme in circuit integration, used to indicate presence of one hundred million transistors (or more) on a single semiconductor chip.

ultrasonic bonding A bond formed when a wire is pressed against a bonding pad and the pressing mechanism is ultrasonically vibrated at a frequency above 10 kHz. These high-frequency vibrations break down and disperse the oxide films that are present on the conductor surfaces. As these surface films are removed, diffusion of the conductor materials occurs at the interface. The joints formed are metallurgically sound diffusion bonds.

undercut (1) In process, the distance on one edge of a conductor measured parallel to the board surface from the outer edge of the conductor, including etch resists, to the maximum point of indentation on the copper edge. (2) After fabrication, the distance on one edge of the conductor measured parallel to the board surface from the outer edge of the conductor, excluding overplating and coatings, to the maximum point of indentation on the same edge.

unsupported hole A hole containing neither conductive material nor any other type of reinforcement.

vacuum deposition Deposition of a metal film onto a substrate in a vacuum by metal evaporation techniques.

vapor-phase reflow A technique for solder reflow to form package interconnections. The solder joint is heated by the heat of condensation of an inert vapor.

varnish The mixed and aged catalyzed resin solution used to impregnate glass cloth in the process of producing printed boards.

vehicle The organic system in a composition.

Very High Speed Integrated Circuit (VHSIC) Originally referring to devices with 1.0 micrometer ground rules.

very large scale integration (VLSI) Referring to a single semiconductor chip with more than 10,000 transistors. The upper boundary is not well-defined.

via (hole) An opening in the dielectric layer(s), of a multilayer structure, whose walls are made conductive to enable interconnections between conductive layers.

via, blind A via that does not go all the way through a multilayer structure. It may interconnect the top or bottom surfaces to one or more internal planes.

Micron Ex. 1026, p. 124
Micron v. YMTC
IPR2024-00911

via, buried A via that interconnects internal planes in a multilayer structure, but does not come out to the top or bottom surfaces.

via, fixed A via built into a package on a predetermined grid.

via, programmable A via whose location does not correspond to the same grid locations as fixed vias. The via and its location is "programmed" into a design only as needed.

via, segmented A fixed via interconnection. A predetermined subset of all wiring planes.

via, through A fixed via passing through all wiring planes.

viscosity The intrinsic property of a fluid that resists internal flow by offering counteracting forces.

vitreous Glassy. As used in ceramic technology, indicating fired characteristics approaching a glassy state but not necessarily totally glassy.

vitrification The formation of a glassy or noncrystalline material.

void The absence of substances in a localized area.

volt A unit of electromotive force.

voltage drop The amount of voltage loss from original input in a conductor of given size and length.

voltage plane A conductor or portion of a conductor layer on or in a printed board that is maintained at other than ground potential. It can also be used as a common voltage source for heat-sinking or for shielding.

voltage plane clearance The etched portion of a voltage plane around a plated-through or non-plated-through hole that isolates the voltage plane from the hole.

voltage regulation The drop in voltage due to load current, usually expressed as a percentage.

VSOP Acronym for Very Small Outline Package.

wafer Usually, a slice of semiconductor crystalline ingot used for substrate material when modified by the addition, as applicable, of impurity diffusion (doping), ion implantation, epitaxy, etc., and whose active surface has been processed into arrays of discrete devices or ICs by metallization and passivation.

warp See **bow** and **flatness.**

water absorption test A method used to determine the water penetration through an insulating material after a given water immersion period.

watt A unit of electrical power; the power of one ampere of current pushed by one volt of electromotive force.

wave soldering A process in which printed boards are brought in contact with the surface of continuously flowing and circulating solder. Also called *mass soldering.*

wavelength The distance, measured in the direction of propagation, of a repetitive electrical pulse or waveform between two successive points that are characterized by the same phase of vibration.

Micron Ex. 1026, p. 125
Micron v. YMTC
IPR2024-00911

wear track In connectors, the imprint of one contact surface on its mate caused by insertion and/or withdrawal.

weave exposure A surface condition of base material in which the unbroken fibers of woven glass cloth are not completely covered by resin.

weave texture A surface condition of base material in which a weave pattern of glass cloth is apparent although the unbroken fibers of the woven cloth are completely covered with resin.

wedge bond A thermocompression bond in which a wedge-shaped tool is used to apply pressure to the wire being attached.

welding Connections that are made by fusing two conductors, using heat, pressure, or both.

wetting The formation of a relatively uniform, smooth, unbroken, and adherent film of solder to a basis metal.

whiskers Single-crystal growths resembling fine wire, which may extend to 0.64 mm (0.025 in) high. They most frequently occur on boards or components that have been electroplated with tin. The process may be described as an electroless one in that growth requires no voltage. Growth can occur in inert-gas or vacuum environments and is reportedly induced by compressive stress and high temperatures, accelerated by—though not dependent upon—humidity. (See also **electromigration.**)

wicking Capillary adsorption of liquid along the fibers of a base material. Also, the flow of solder away from the desired area by wetting or capillary action.

wiping action The action of two electrical contacts that come in contact by sliding against each other.

wire bond A completed wire connection whose constituents provide electrical continuity between the semiconductor die (pad) and a terminal. These constituents are (1) the fine wire; (2) metal bonding surfaces like die pad and package land; and (3) metallurgical interfaces between wire, and metals on both the chip and substrate.

wire bonding The method used to attach very fine wire to semiconductor components in order to interconnect these components with each other or with package leads.

wire wrap A method of connecting a solid wire to a square, rectangular, or V-shape terminal by tightly wrapping the wire around the terminal with a special tool.

wireability The capability of a package to permit the interconnections of subpackages or chips mounted on it and terminals attached to it measured as the probability of wiring success. Wiring capacity (length), via availability, and terminal access are all considerations in determining package wireability.

wiring (also **routing**) The manual or automatic prescription of routes for wires interconnecting package components.

wiring assignment The manual or automatic prescription of particular pads, pins, connectors, or terminals to which corresponding wires are to be attached.

wiring capacity The total available length of wiring tracks in a package.

Micron Ex. 1026, p. 126
Micron v. YMTC
IPR2024-00911

wiring channel A linear region on a package wiring plane containing space for at least one wiring track.

wiring demand The product of wiring connection count and average connection length required to interconnect a given set of chips or subpackages.

yellow wire Discrete wires that are yellow in color interconnecting terminals on a package. Originally used in reference to all back panel wiring on early electronic assemblies.

yield The ratio of the number of acceptable items produced in a production run to the total number that were attempted to be produced (i.e., started in the production run).

yield strength The stress at which a material exhibits a specified strain deviation from purely elastic stress-strain behavior (often chosen at 1 percent offset).

zero-insertion-force connector A connector in which the contact surfaces do not mechanically touch or very lightly touch, thus requiring no insertion force. After mating, the contacts are actuated in some fashion to make intimate electrical contact.

19.3 Author's Note

Since putting this glossary together in August, 1993, I have already had to make several revisions to it. Some changes were terms, provided by reviewers, that I had not run across before. Each company tends to define acronyms and terms that best serve them in describing package technology. It is quite doubtful if all the of this terminology has been included in the preceding glossary. Also, several new terms had been coined since the initial compilation, another reminder of the dynamic environment in which we live and work.

19.4 References

1. *Electronic Materials Handbook: Volume 1 Packaging,* published by ASM International, 1989.
2. R. R. Tummala and E. J. Rymaszewski (eds.), *Microelectronics Packaging Handbook,* Van Nostrand Reinhold, 1989.
3. D. A. Doane and P. F. Franzon (eds.), *Multichip Module Technologies and Alternatives: The Basics,* Van Nostrand Reinhold, 1993.
4. John H. Lau (ed.), *Handbook of Tape Automated Bonding,* Van Nostrand Reinhold, 1992.
5. G. Messner, I. Turlik, J. W. Balde, and P. E. Garrou (eds.), *Thin Film Multichip Modules,* International Society for Hybrid Microelectronics, 1992.
6. D. P. Seraphim, R. Lasky, and C.-Y. Li (eds.), *Principles of Electronic Packaging,* McGraw-Hill, 1989.
7. *Low End Packaging Applications Guide,* edited by R. W. Gedney, March, 1990; 160-page guide to package technology used internal to IBM.

Micron Ex. 1026, p. 127
Micron v. YMTC
IPR2024-00911

Author Biographies

John H. Lau is a senior engineer of Hewlett-Packard Company located in Palo Alto, California. His research activities cover a broad range of electronics packaging and manufacturing technology.

He received the B.E. degree in civil engineering from National Taiwan University, the M.A.Sc. degree in structural engineering from University of British Columbia, the M.S. degree in engineering mechanics from University of Wisconsin, the M.S. degree in management science from Fairleigh Dickinson University, and the Ph.D. degree in theoretical and applied mechanics from University of Illinois.

Prior to joining Hewlett-Packard Laboratories in 1984, he worked for Exxon Production and Research Company and Sandia National Laboratory. He has more than 24 years of research and development experience in applying the principles of engineering and science to the electronic, petroleum, nuclear, and defense industries. He has authored and coauthored over 100 technical publications in these areas and is the author and editor of the books, *Solder Joint Reliability: Theory and Applications, Handbook of Tape Automated Bonding, Thermal Stress and Strain in Microelectronics Packaging, The Mechanics of Solder Alloy Interconnects, Handbook of Fine Pitch Surface Mount Technology,* and *Chip On Board Technologies for Multichip Modules.*

He is an associate editor of the *ASME Transactions, Journal of Electronic Packaging,* and the *IEEE Transactions on Components, Packaging, and Manufacturing Technology.* He has also served as session chairman, program chairman, general chairman, and invited speaker

Micron Ex. 1026, p. 128
Micron v. YMTC
IPR2024-00911

of several IEEE, ASME, ASM, ISHM, and NEPCON conferences and symposiums. He is an IEEE fellow, a registered professional engineer, and is listed in the American Men and Women of Science.

Richard E. Sigliano received his B.S. in Biological Sciences/Chemistry from Fullerton State. He worked for 5 years at Beckman Instruments as a Material Development Engineer in the areas of liquid crystal materials and displays, thin film microcircuits, and thick film materials and microcircuits.

He has been with KYOCERA AMERICA for the past 15 years, and is currently the New Product Development and Marketing Manager.

He is a member of IEPS, IEEE, ISHM, and is currently the company representative at the JEDEC JC-11 Committee for package standardization.

Osamu Fujikawa is Director, Research and Development Group of Ibiden, Ogaki, Japan. He received his B.S. degree in chemistry from Shizuoka University, Japan in 1970 and joined Ibiden in the same year. Since then he has played a key role in developing PCB, COB, and plastic package material and process technology. Currently, his R&D management assignment covers the developing DCA, MCM, plastic package technologies, and other nonelectronics products at Ibiden.

Motoji Kato is Sales and Marketing Manager of Ibiden U.S.A., Santa Clara, California. He received his B.S. degree in nuclear engineering from Nagoya University, Japan in 1983. He joined Ibiden in the same year and as an engineer of material and process development. He has been involved in technical marketing activities at the U.S. subsidiary of Ibiden since 1988.

Patrick Hession is Component Engineer, Compaq Computer Corporation, Houston, Texas. Mr. Hession received his B.S. degree in chemical engineering from the University of Rochester, New York, in 1982. He has over 12 years of experience in the electronics industry dealing with electronic packaging. His experience includes over 6 years at Texas Instruments in Dallas holding various engineering and engineering management positions in their PCB fabrication organization. While at TI, Mr. Hession worked on development of high-density, sequential multilayer PCBs using laser drilled buried and blind vias. Mr. Hession worked for 5 years at Apple Computer in Cupertino, California, managing their packaging and process development organization. His responsibilities included TAB and BGA package and process

Micron Ex. 1026, p. 129
Micron v. YMTC
IPR2024-00911

development, as well as responsibility for Apple's PCB design technology. For the past year, Mr. Hession has been with Compaq Computer Corporation in Houston. He is currently responsible for Compaq's PCB and IC packaging technology, working in Compaq's PCA-Components Engineering organization. His activity includes managing Compaq's PCB technology roadmap, and design and development of IC packaging, including BGAs.

Thomas Caulfield, a senior engineering manager in MLC Packaging Applications at IBM Microelectronics, has an Eng.Sc.D. degree in Metallurgy from Columbia University. Since 1990, he has been both a team leader and engineering manager during the qualification and implementation of CBGA technology within IBM. His current responsibilities include managing New Business Development and New Product Application in the Ceramic Chip Carrier Business Unit.

Marie Cole, an advisory engineer in MLC Packaging Applications at IBM Microelectronics, has a B.S.Ch.E. from Rensselaer Polytechnic Institute and an M.S. in Materials Science from Columbia University. She has worked on the development of CBGA and CCGA packaging since 1988. Her current role is in New Product Applications in the Ceramic Chip Carrier Business Unit.

Frank Cappo has nearly 30 years of experience in packaging process, tooling, and product development. These activities include support for System 360, 370, and 390. His current assignment is in the MLC Electrical Design and Analysis area of the Ceramic Chip Carrier Business Unit of IBM Microelectronics.

Jeffrey Zitz is the lead thermal engineer for the Advanced Thermal Technology department in the Ceramic Chip Carrier Business Unit of IBM Microelectronics. He received his B.S.M.E. and M.S.M.E. from Rensselaer Polytechnic Institute, concentrating in air and immersion cooling, and has more than 8 years experience in the module and system-level packaging of personal, workstation, mini- and mainframe computers. Jeff is a licensed Professional Engineer in the state of New York.

Joseph Benenati has over 30 years of experience in application, design, and fabrication of electronic modules. He currently is a senior

Micron Ex. 1026, p. 130
Micron v. YMTC
IPR2024-00911

technical staff member in the IBM Microelectronics Division, playing a major role in packaging menu selection to fill product application needs for both single and multichip modules. He is also the program manager for ball grid array modules.

Donald R. Banks received a B.S. in Metallurgical Engineering from the Montana College of Mineral Science and Technology in 1984 and an M.S. in Materials Science and Metallurgical Engineering from the University of Notre Dame in 1986. Mr. Banks has published on intermetallic compound growth, solder corrosion, assembly processes, reliability, and array packaging. He has 5 years experience with ball grid array and column grid array technologies. The author worked in IBM's Assembly Process Design Group from 1988 to 1993 in Austin, Texas and Endicott, New York. Mr. Banks is currently employed by Motorola, Inc., in the Advanced Packaging and Assembly Manufacturing group in Austin, concentrating on both plastic and ceramic BGA and CGA packaging.

Karl Hoebener is an Advisory Scientist in the IBM PC Company Austin. He is at present involved in the Advanced Laminate Technology Development in the panel manufacturing facility. Prior to joining the ALT development group Karl was the project leader of the Solder Ball Connect process development and qualification effort. He was a member of the Austin second-level packaging development laboratory and was associated with several projects that included surface mount technology, SMT/PIH hybrid processes. Prior to joining the Austin facility he was involved in first-level packaging projects such as direct chip attachment on ceramic substrates, and chip dicing and picking.

Karl Hoebener is the recipient of five patents and has authored six technical disclosure bulletins. He received the First and Second Invention Achievement Awards, and an Outstanding Technical Achievement Award for Solder Ball Connect Development and Qualification. He has authored a number of internal and external technical papers.

Puligandla Viswanadham is an Advisory Scientist in the IBM PC Company, Austin. He is currently involved in the Advanced Laminate Technology Development in the Panel Manufacturing Facility. Prior to joining the panel plant he was involved in the process development and reliability assessments of fine pitch assemblies that included fine pitch Quad Flat packs and Thin Small Outline Packages in IBM Systems Technology Division in Endicott, New York. He has an M.Sc., degree

Micron Ex. 1026, p. 131
Micron v. YMTC
IPR2024-00911

from Saugor University, India, and a Ph.D. degree in chemistry from the University of Toledo, Toledo, Ohio. Dr. Viswanadham joined IBM, Rochester, Minnesota in 1979. As a member of the Materials and Process Engineering group he was involved in corrosion studies, analytical methods development, plating, and contamination control. He joined IBM, Austin development laboratories in 1986 and has been involved with solderable surface evaluations, Tape Automated Bonding (TAB), and Fine Pitch Quad Flat Pack second-level assembly process development and reliability evaluations. He was Site Materials Engineering/Analytical Labs Manager at Austin during 1989 to 1990. Prior to Joining IBM, his research activities included high-temperature chemistry and thermodynamics of binary and ternary chalcogenides, atomic absorption, slag seed equilibria in coal-fired magnetohydrodynamic energy generation, and astrophysics. He has authored or coauthored over 65 publications in various technical journals, symposium proceedings, and trade magazines and books. He is a Fellow of the American Institute of Chemists and a member of American Chemical Society, National Association of Corrosion Engineers, New York Academy of Sciences, and Scientific Research Society of North America. He received the IBM First and Second Invention Achievement Awards, and Fourth-level Technical Author Recognition Award. Dr. Viswanadham is the author of two patents and 14 Invention Disclosures.

Yung-Cheng Lee received his B.S.M.E. degree from the National Taiwan University in 1978, and the M.S. and Ph.D. degrees from the University of Minnesota, in 1982 and 1984, respectively. He is an Associate Professor of Mechanical Engineering and the Associate Director of the Center for Advanced Manufacturing and Packaging for Microwave, Optical and Digital Electronics, University of Colorado—Boulder. Prior to joining the University in 1989, he was a Member of Technical Staff at AT&T Bell Laboratories, Murray Hill, New Jersey.

His research interests include low-cost prototyping and thermal management of multichip modules, 3-D packaging, self-aligning soldering, thermosonic bonding, optoelectronics packaging, and fuzzy logic modeling and control. He received the Presidential Young Investigator Award from National Science Foundation in 1990, and the Outstanding Young Manufacturing Engineer Award from SME in 1992.

Jay Jui-Hsiang Liu received the B.S. degree in Physics from National Taiwan University in 1977, the M.S. degree in Materials Science from National Tsing Hua University in 1979, and the Ph.D. degree in Materials Science from Cornell University in 1986.

Micron Ex. 1026, p. 132
Micron v. YMTC
IPR2024-00911

Currently, he is a Senior Staff Engineer with the Advanced Packaging Development Center of Motorola at Chandler, Arizona, where he works on all issues related to high-performance single-chip and MCM package designs. Prior to joining Motorola, Jay was a member of technical staff with AT&T—Bell Labs, Princeton and worked on material and assembly issues associated with surface mount technologies and MCMs.

Chi-Taou Tsai received the B.S. degree in Physics from National Central University in ChungLi, Taiwan, in 1976 and the M.S. and the Ph.D. degrees in Electrical Engineering from University of Utah, Salt Lake City, Utah in 1982 and 1984, respectively.

He joined Motorola at Phoenix, AZ after graduation to work on electronic packaging R/D. Currently, he is with the Advanced Packaging Design and Automation Center of Motorola at Chandler, AZ, where he works on all issues related to the IC packaging electrical performance and signal integrity. His research interests include electrical modeling, simulation, measurement, design, and development of high-speed and high-performance packages, MCMs, and systems.

Yifan Guo is currently with IBM Microelectronic Division. Dr. Guo received his Ph.D. degree in Engineering Mechanics from Virginia Polytechnic Institute and State University in 1989. After graduation, he was appointed as Assistant Professor in the Engineering Science and Mechanics Department at VPI&SU. He taught courses in mechanics and continued his research in the area of experimental mechanics and mechanics of composite materials. He jointed IBM Corporation in 1990 and began his research in the field of microelectronic packaging. He was heavily involved in the development of the ceramic BGA package in IBM. He has received an IBM Division Award for his contributions in the development and applications of moiré interferometry in electronic packaging.

Dr. Guo has published more than 20 technical papers in journals and conference proceedings, and received a best-paper award for his paper published in the *Journal of Experimental Techniques.*

John S. Corbin, Senior Engineer, IBM RISC Systems 6000 Division, Austin, Texas received his B.S. and M.S. degrees in mechanical engineering from the University of Texas at Austin in 1972 and 1974, respectively. He joined IBM in 1974 and spent 10 years in printer development, working primarily in the area of motion control. This was followed by 6 years in the Systems Technology Division Packaging Laboratory in Austin, applying finite element modeling techniques in the area of mechanical packaging reliability. He is currently a Senior

Micron Ex. 1026, p. 133
Micron v. YMTC
IPR2024-00911

Engineer in the IBM RISC System 6000 Division where his interests relate to system packaging reliability. Mr. Corbin is a registered professional engineer in the state of Texas.

Robert C. Marrs is Vice President & General Manager, MicroSystems Division, Amkor Electronics, Inc., Chandler, Arizona. His responsibilities in this position include strategic and tactical marketing, design, development, and profit/loss management of newly developed technologies. He directs all advanced-technology product groups and design teams. Mr. Marrs has been with Amkor Electronics since 1989 and founded the advanced packaging division for Amkor Electronics in 1991. He is credited with the design and development of numerous new packaging technologies including PowerQuad, low-cost flip chip, ICR, MCM BGAs, and SuperBGAs. He has more than 20 years of experience in IC packaging and assembly and holds numerous packaging technology patents. Prior to his position with Amkor, Mr. Marrs was founder and president of another subcontract manufacturer, and has held a variety of other packaging positions during his career in the IC industry. Prior affiliations include VLSI Technology, National Semiconductor, Siliconix, and TRW. Mr. Marrs received his Bachelor of Science degree cum laude in 1974 from California State University at Long Beach in Industrial Technology.

William B. Mullen is Senior Member of the Technical Staff and Manager of the Advanced Manufacturing Technology Interconnect Technologies Laboratories in the Land Mobile Products Sector of Motorola, Inc., Fort Lauderdale, Florida. The Interconnect Technology laboratories are responsible for the development and characterization of strategic assembly and integrated circuit packaging technologies for their products. During the last 7 years Mr. Mullen has taken the initiative to introduce both CBGA and PBGA technologies into the portable products produced by Motorola. His expertise in interconnect and process design has provided the foundation for the introduction of surface mount technology to Motorola's portable products. Mr. Mullen received his B.S. in Physics from Florida Institute of Technology in 1970 and has since remained focused in the field of electronics manufacturing processes and electronic materials. Included among his 17 issued patents are several related to OMPAC™ and BGA technologies. He is credited with numerous internal publications on interconnect technology and is currently exploring the attributes of DCA.

Robert Darveaux is Senior Staff Engineer in the Land Mobile Products Sector of Motorola in Plantation, Florida. Dr. Darveaux

Micron Ex. 1026, p. 134
Micron v. YMTC
IPR2024-00911

received his B.S. in Nuclear Engineering from Iowa State University and his Ph.D. in Materials Science and Engineering from North Carolina State University. His research and development activities have been in the areas of thermal performance of multichip modules, mechanical characterization of solders, finite element modeling, power device packaging, failure analysis, and reliability prediction. His modeling and fatigue analysis work have been integral to Motorola's BGA implementation process. He has authored over 20 technical articles and has three patents.

Barry M. Miles is Senior Staff Engineer and Manager of the Advanced Manufacturing Technology IC Packaging Lab, Motorola, Plantation, Florida. Barry is responsible for semiconductor package development and the implementation of these packages into the manufacturing environment, specific to portable and mobile electronic communications products. He was one of the original members of the PBGA package development team at Motorola in Florida, with responsibility for package-level reliability testing and moisture-sensitivity studies. Employed by Motorola since 1983, he has also done work in the areas of thin film hybrids, flex and printed circuit board fabrication, and surface mount assembly. Barry received his B.S. degree in Chemical Engineering from the University of South Florida, Tampa, Florida. He has written numerous papers for publishing in technical conference proceedings, and currently holds 10 issued patents.

Allen Hertz is Staff Process Engineer of Paging Products Group of Motorola, Boynton Beach, Florida. Mr. Hertz is responsible for the development and introduction of production processes and overseeing designs for manufacturability of new paging products. Mr. Hertz is best known for his work on plastic ball grid array packages and 1005 (20×40) chip components; he holds patents that apply to both of these areas. In 1989 Mr. Hertz was the first to implement PBGA technology into a commercial product and has been instrumental in the success of this technology in Motorola. Mr. Hertz received his B.S. in Ocean Engineering from Florida Atlantic University; he has authored over 10 technical publications and has four issued patents.

Philip E. Rogren is Vice President of Marketing and Sales, Hestia Technologies Inc., Sunnyvale, California. Mr. Rogren has been involved in semiconductor packaging and interface technology since 1974. His involvement in the industry has included both engineering and marketing and sales responsibilities. He has published numerous technical

Micron Ex. 1026, p. 135
Micron v. YMTC
IPR2024-00911

papers in refereed journals and participated as speaker and panelist in several industry workshops. He received a B.S. degree in Ceramic Engineering from the University of Washington in 1974.

Seyed Hassan Hashemi is a Member of the Technical Staff and a project manager in MCC's High Value Electronics (HVE) Division. He has worked at MCC since January 1985. His work includes high-frequency electrical characterization and thermomechanical modeling of single and multichip packaging and interconnect problems. He has also been a technical lead for the power distribution project, where he worked on experimental and simulation of switching-noise problems in high-speed packaging and interconnect applications. He is currently managing two multiclient projects; the Single and Few Chip Packaging (SFCP) project and the Ball Grid Array (BGA) Package Reliability project.

Mr. Hashemi received a B.S. in Electrical Engineering from the University of Houston in 1982, and an M.S. in Electrical Engineering from the University of Texas at Austin in 1984. He holds four U.S. patents, and is the principle author or co-author of over 30 MCC internal reports, 3 book chapters, and over 25 journal and technical publications in the areas of single and few chip packaging, power distribution, electrical characterization, and modeling of packaging and interconnect problems. He is a member of Eta Kappa Nu, Tau Beta Pi, IEEE, ISHM, and IEPS.

David B. Walshak, Jr., is a member of the technical staff in MCC's High Value Electronics Division. He joined MCC in April 1984. He obtained his B.S. in Mechanical Engineering from the University of Texas at Austin in 1982 and an M.S. in Mechanical Engineering from UT in 1988. His primary area of concentration at MCC has been in the fine-pitch assembly process development. Over the last several years he has developed tape automated bonding (TAB) assembly processes for both inner- and outer-lead bonding using thermocompression, thermosonic, and laser energy techniques.

Mr. Walshak was the project leader for the first sets of multichip modules that were assembled at MCC. He developed cost models for various assembly techniques for use in prototype-sized assembly requests. Recently, he has used finite element modeling to conduct parametric studies of various package components to optimize thermal performance for various package types, including BGAs.

He has written and presented several papers relating to fine-pitch assembly and thermal modeling, including a chapter on inner-lead

Micron Ex. 1026, p. 136
Micron v. YMTC
IPR2024-00911

bonding for John Lau's *Handbook of Tape Automated Bonding*. Mr. Walshak is a member of Pi Tau Sigma, Tau Beta Pi, Phi Kappa Phi, IEPS, and SMTA.

Kingshuk Banerji is Senior Staff Engineer in the Advanced Manufacturing Technology Labs of the Land Mobile Product Sector of Motorola in Plantation, Florida. He received his B.S. and M.S. degrees from Indian Institute of Technology and his Ph.D. in materials engineering from Georgia Tech. He works in the areas of process development and interconnect reliability for board assembly and flip chip packaging.

Andrew J. Mawer is a packaging engineer with Motorola Semiconductor Products Sector's Advanced Packaging Technology Department in Austin, Texas. He received his B.S. in Mechanical Engineering from the University of Texas at Austin in 1987 and his Master of Mechanical Engineering from Rice University in 1989. His primary area of interest is Plastic Ball Grid Array (PBGA) solder joint reliability characterization, improvement, and application lifetime prediction. He has also been involved with PBGA assembly process development (concentrating on solder bump attachment), package design, and all aspects of surface mount assembly, including inspection and rework. Prior to joining Motorola, Andrew spent 4 years at Compaq Computer Corporation in the Component Reliability, Materials Analysis, and Advanced Manufacturing Technology Departments working on various levels of packaging and interconnect, such as surface mount devices, PBGA, TAB, PGA, printed circuit boards, keyboards, laptop/desktop PC enclosures, sockets, connectors, and cables. His main areas of responsibility there were component/interconnect reliability, surface mount assembly process analysis, and thermal/mechanical finite element modeling. He was part of the team that implemented PBGA technology to Compaq. Andrew has authored or coauthored several technical articles on PBGA and has also presented at several industry symposiums.

Glenn Dody is Manager, Surface Mount Application Lab and Reliability Test Center in the Semiconductor Products Sector of Motorola in Austin, Texas. He has 20 years experience with the U.S. Air Force in Aviation Electronics, 7 years as Printed Circuit Board Assembly Manager, 2 years in surface mount package development, and 9 years in surface mount technology research and development. Glenn is a member of ISHM, and the Testing subcommittee of the IEEE Compliant Lead Task Force.

Micron Ex. 1026, p. 137
Micron v. YMTC
IPR2024-00911

Chin-Ching Huang is Manager, Package Characterization, at VLSI Technology, Inc. Since joining the company in 1989, he has been responsible for the development of measurement techniques, modeling, and simulation of thermal, mechanical stress, and electrical characteristics of packages, TAB and MCM. He has five U.S. patents related to package technology at VLSI Technology, Inc. Dr. Huang received a B.S. (Physics) from Soochow University, Taiwan, M.S. (Physics) and M.S.E.E. from Florida Institute of Technology, and a Ph.D. degree in Materials Science from the University of Virginia. Prior to joining VLSI Technology, Inc., he held the position of Principal Engineer at Digital Equipment Corporation, where he was responsible for conducting research on heat dissipation for MCM. Dr. Huang started his career in the industry as a Senior Engineer at National Semiconductor/Fairchild Camera & Instruments Gate Array Division, where he was involved in package characterization with emphasis on ceramic and plastic package development for ECL and CMOS gate arrays.

Ahmad Hamzehdoost is Senior Packaging Engineer, VLSI Technology, Inc., San Jose. His fields of expertise include thermal and stress analysis of microelectronic packages. He received a B.S. degree in Electrical Engineering from University of Arizona and M.S. degree in Mechanical Engineering from Manhattan College. He has authored several papers on the topic of heat transfer in IC packaging.

John A. Adams has over 19 years experience in the development of Automated Inspection and Measurements systems, using both vision and discrete gauging technologies. He has extensive experience in developing vision inspection computer algorithms. He has patented x-ray and x-ray laminography vision systems. He has expertise in system software design, automated systems hardware design, project planning, equipment acceptance test methodology, calibration methodology, statistical process control, capability studies of automated instrumentation, specification generation, technical documentation, manuals, and trade journal papers. He has presented papers at many national and international technical conferences. He has a B.S. degree in Physics from the University of San Diego and Ph.D. degree in Experimental Nuclear Physics from Arizona State University. He is a member of IEPS. He has received IR-100 award in 1984, is named in *Who's Who in Finance and Industry 1994,* and *Who's Who Worldwide 1995.*

Tom C. Chung is Tandem Computers' Visiting Representative at Microelectronics and Computer Technology Corporation (MCC) in

Micron Ex. 1026, p. 138
Micron v. YMTC
IPR2024-00911

Austin, Texas. Dr. Chung has more than 14 years of experience in the field of advanced computer packaging and interconnect technologies, including surface mount, tape automated bonding, flip-chip, advanced single-chip packaging, multichip module technologies, etc. He worked on semiconductor assembly, test, packaging, and interconnect-related technology developments for United Technologies Corporation and MCC for 5 years, respectively, before joining Tandem Computers, Inc., in 1989 as a Development Engineering Manager in the advanced computer packaging and interconnect department. Since early 1993, he has taken the responsibility as Tandem's technical representative at MCC to lead a group to develop flip-chip-based MCM technology for the next generation of computer workstations. He has a B.S.E. from NCKU in Taiwan, an M.S.M.E. from Texas Tech University, and an M.S. in engineering management and a Ph.D. in engineering from Southern Methodist University, Dallas, Texas. He owns four U.S. patents and has published more than 20 technical papers. He is also a coauthor of two technical books, *Handbook of Tape Automated Bonding* (published in 1992) and *Chip on Board Technologies for Multichip Modules* (published in 1994).

Paul Mescher is a process development engineer in IBM's Assembly Process Design group. Mr. Mescher received his B.S. degree from Arizona State University in Materials Science Engineering and joined IBM Endicott in 1988. He has been working exclusively on BGA process development issues for IBM since 1991, and continues to be a key member of the TBGA package development team. Prior to 1991, he worked in materials support, splitting time between TAB product and PTFE card process development issues.

Christopher A. Schmolze is Senior Technical Service Engineer, 3M Company, Semiconductor Products Business, Austin, Texas. Mr. Schmolze received his B.S.M.E. from the University of Minnesota. Employed by 3M since 1984, he has held positions in sustaining engineering, product development, and technical service. His areas of interest are static dissipative thermoplastics, IC packages, IC sockets, and IC trays and carriers. This work has led to two patents, one for a "Semiconducting Polymeric Composite" and the other for a "Contactless Multipurpose TAB Socket." He currently represents 3M on industry standards committees for IC sockets and IC package mechanical outlines and chairs the JEDEC JC11.13 Quality Subcommittee. Professional affiliations have included ASME and currently include ISHM and IEPS and CTEA.

Micron Ex. 1026, p. 139
Micron v. YMTC
IPR2024-00911

E. Jan Vardaman, President, TechSearch International, Inc. received her B.A. in Economics and Business in 1979 from Mercer University, and her M.S. in Economics from the University of Texas in 1981. After working as a government computer industry analyst, she joined Microelectronics and Computer Technology Corporation in 1984, where she analyzed developments in semiconductor packaging/interconnect. In 1987, she founded TechSearch International, Inc., a company involved in licensing electronics technology and providing technical information on international developments in the electronics industry. She is a member of the IEEE, CHMT, ISHM, and the International Electronics Packaging Society. She has made presentations on developments in tape automated bonding and multichip modules in Japan, the United States, and Europe and has authored publications in numerous countries. She is also the editor of the recently released book published by IEEE titled, *Surface Mount Technology—Recent Japanese Developments.*

Ronald W. Gedney is a consultant in electronic packaging since retiring from IBM in 1992. Mr. Gedney received the B.S.E.E. degree from Tufts University, and subsequently joined IBM while undertaking part-time postgraduate studies at Syracuse University. At IBM he first developed reliability test techniques and specifications for passive components and ferrite memory cores. With the formation of IBM's Components Division, he become involved with the development of single- and multichip electronic packages. In 1974 he became Program Manager of IBM's Metallized Ceramic program, a thin film, single- and multichip package technology based in Endicott, New York. He has been manager of Packaging Development in IBM's General Technology Division, Burlington, Vermont, and a consultant at the IBM plant in Havant, England. In 1984 he returned to Endicott, where he has held a number of management and engineering assignments in the packaging development laboratory, including the development of TAB tape. He has published a number of papers and holds several patents in electronic packaging. A past president of the IEEE Components, Packaging and Manufacturing Technology Society, he was elected a Fellow of the IEEE in recognition for contributions to the field of electronic packaging.

Micron Ex. 1026, p. 140
Micron v. YMTC
IPR2024-00911

Index

ABAQUS, 393–396
Absolute temperature, 380–382
Accelerated stress test, 446–447
Accelerated thermal cycling (ATC), 175, 224–225, 258–261
Acceleration factor (AF), 160–161
Acoustic microscopy, 325–328
  (*See also* C-SAM; SLAM)
Activation energy, 380–381
Additive process, 107–108
Advanced packages, 22–33
Alluvial fan effect, 67
Alumina
  production of, 70–77
  (*See also* Aluminum oxide)
Alumina ceramic, 69–70, 136
Alumina-silica (Al_2O_3-SiO_2), 78
Aluminum nitride (AlN), 79–82
Aluminum oxide, 68, 69
Anorthite, 78–79
ANSYS®, 231, 263, 392–396
AOI (*see* Automatic optical inspection)
Application-specific integrated circuits (*see* ASIC)
Applications for PBGA, 285–287
Applied stress, 380–382
Aramide, 99, 101–103
Area tape automated bonding BGA (*see* ATAB BGA)
ARIES inspection system, 471
ASIC, 15
Aspect ratio, 226–228
Asperities, 533–534
Assembly yields as performance measurement, 332
ATAB BGA, 32–33, 443–464
  assembly of, 445–446
  reliability of, 446–447
  structure of, 443–444
ATC (*see* Accelerated thermal cycling)
Autoclave test (*see* Pressure-cooker test)
Automated x-ray inspection, 471–473
Automatic optical inspection (AOI), 470
AX1024R, 50

Bakeout, 320–323
Ball and column attach, 139–141
Ball grid array (*see* BGA)
Ball measurements and SPC, 479–486
Bathtub curve, 518
Beam-splitter vision system, 495, 497–498
Beryllium copper, 525, 536
BGA:
  classes of, 543–546
  introduction to, 1–64
  next-generation, 38–51
  and PQFP comparisons, 34–38
BGA industry, 543–554
  existing infrastructure, 546–548
  and IC design trends, 15–16
  production equipment, 548–551
  standards, 551-552
BGA inspection (*see* Inspection of BGA)
BGA package classifications, 543
BGA package configurations, 544–545
BGA rework process (*see* Rework process)
BGA routing:
  1.0-mm-pitch, 124–125
  1.27-mm-pitch, 122–124
  1.5-mm-pitch, 119–121
Binders, 71
Bipolar technology, 7
Bismaleimide triazene, (*see* BT)
Board design, 368–369
Boltzmann's constant, 380–381

Micron Ex. 1026, p. 142
Micron v. YMTC
IPR2024-00911

Bonding methods:
flip chip bonding, 66, 68
tape automated bonding (TAB), 66–67
wire bonding, 66
Bridging, 475
BT, 29, 101, 109, 351, 362, 365, 550
Bubble test, 317
Build-up process, 108
Bulk versus joint behavior, 396–398
Burn-in:
defined, 517–518
at module level, 139
types of, 518–520
(*See also* Burn-in socket)
Burn-in board, 522
Burn-in socket, 517–541
attributes, 522–538
contacts, 531–536
electrical performance of, 536–538
materials used for, 523–526
operation of, 526–531

CAEDS®, 231, 263
Calcia, 69
Capacitance, 346–349, 352–354, 459–460
(*See also RLC* equations)
Card assembly and wireability, 141–149
Card pad diameter, 255–258
Carrier geometries, 172–173
Cavity-down package, 94, 154–155, 195
Cavity-up package, 94, 195
CBGA, 23–29, 171–192
advantages of, 90, 165–167
assembly process, 175–177
and carrier geometries, 172–173
cleanability, 177–178
defects in, 475–478
environment, 172–173
future trends, 188–189
inspection of, 178–179, 478–487
thermal and electrical characteristics of, 193–221
CBGA assembly reliability, 223–265
optimization of, 255–261
rework and repair, 179–182
strain distribution in, 224–228
CBGA experimental study, 197–203
CBGA modeling study, 204–208
CBGA package, 174
CBGA rework and repair, 179–182
CBGA verus PBGA, 90
CBGA/CCGA, 131–169
card assembly, 141–146
electrical attributes, 149–152
example applications, 163–167
interconnection reliability, 157–163
module assembly, 136–141
product performance of, 154
thermal attributes, 153–157
wireability, 146–148
CCGA, 131–169, 185–187
(*See also* CBGA/CCGA)
Ceracom, 104
Ceramic ball grid array (*see* CBGA)
Ceramic column grid array (*see* CCGA)
Ceramic core substrate, 104
Ceramic material processing, 68–83
Ceramic materials, 65–92
and BGA substrate circuit density, 86–90
glass, 83–85
history of, 65–68
introduction to, 65–68
processing, 68–83
Ceramic substrate circuit density, 86–90
Ceramic substrates, 65–92
C5 packages, 75, 383
C4 packages (*see* Controlled collapse chip connection)
Chip encapsulation, 137–138
Chip-level interconnects
and ceramic chip carriers, 136–137
Chip-level interconnects
common methods of, 2
CIH (*see* Condensation inert heating)
CISC, 15
Classification of BGA packages, 543
Clock frequency, 15
Closed-form formulas, 458–460
C-mode scanning acoustic microscopy (C-SAM), 327–328
CMOS, 6–8
COB (chips on board) technology, 2
Coefficient of thermal expansion (CTE), 184
Coffin-Manson relationship, 158–161, 228, 244, 261
Cofiring, 74–75

Micron Ex. 1026, p. 143
Micron v. YMTC
IPR2024-00911

Complementary metal-oxide semiconductor (*see* CMOS)
Complex instruction-set computing (*see* CISC)
Component reliability equations, 413–414
Component reliability estimation procedure, 433–436
Condensation inert heating (CIH), 501–502
Conductance, 335–339, 346–349, 450–455
Conduction, 195–196, 448, 450–455
Conductive heat transfer, 336–337
Configurations of BGA packages, 544–546
Connector resistance, 534
Constitutive relations, 380–382
Constriction resistance, 534–535
Contact resistance, 534
Controlled collapse chip connection (C4), 66, 135, 151–152
Convection, 196, 335, 448, 455–456
Conventional packages, 20–22
Cooling methods, 368–369
Copper, 83, 105, 111, 196, 278–279, 341–343, 350–351, 365
Corrosion of bond pad, 283–284, 313–314
Corrosion-resistant materials, 525
Coupled transient analysis, 372
CQFP, 20–21
Crack growth rate, 421–426
Crack initiation and growth, 417–426
Crack-length correlations, 420–426
Cracking (*see* Popcorn effect)
Creep rupture, 399
Creep strain, 381
Cross-sectional acoustic microscope (*see* CSAM)
Cross-sectional x-ray, 474–475
Crosstalk, 346, 371–372
C-SAM, 316–317, 327–328, 471
CSP, 42–43, 48, 49, 50
CTE (*see* Coefficient of thermal expansion)
Cyanate ester, 101, 109

Damage integral function, 418
Definitions of packaging terms, 555–612
Deformation constants, 391–396
Delamination, 100, 283–284, 298, 312–314
Delta temperature, 162–164, 337
Delta-I noise (*see* Switching noise)
Depopulated arrays, 125–127
Die-attach material, 361–362
Dielectric constant, 85, 86, 95–96, 346
Diffusional creep, 380
Direct bond copper (DBC), 81–82
Dislocation climb processes, 380, 390
Dislocation glide-controlled kinetics, 380, 390, 398
Displacement fields, 237–244, 245–247
Dissipation factor, 96
Distance from the neutral point (DNP), 175, 238, 240, 250–251, 502
Distribution function for failures, 413
DNP (*see* Distance from the neutral point)
Dog-bone design, 141–142, 173
DRAM, 7–11
Dry packaging, 314–315
Dry pressing, 75–76
Dual-in-line package (DIP), 65
Ductility, 389–391, 400, 407
Dynamic burn-in, 519
Dynamic random access memory (*see* DRAM)

EBGA, 360, 366–367
Elastic modulus, 231–234
Electrical advantages of BGAs vs. other surface mount packages, 353–354
Electrical analysis methodology, 370–373
Electrical attributes of CBGA/CCGA packages, 149–152
Electrical management of CBGA, 208–219
Electrical management of PBGA, 280–283, 334, 345–355, 369–376
Electrical management of TBGA, 457–460
Electrical modeling and high-performance design, 354–355
Electrical parasitic comparison, 208–211
Electrical properties of laminate materials, 350
Electron microscopy, 185
Electronic package functions, 1

Micron Ex. 1026, p. 144
Micron v. YMTC
IPR2024-00911

Electronic package heirarchy, 1–5
Electronics packaging:
  BGA update, 17–56
  functions of, 1
Electrostatic discharge (*see* ESD)
Emitter coupled logic (ECL), 7
Encapsulation, 137–138, 446
End-line effects, 460
Engineering change requests, 503
Engineering stress, 385–386
Enhanced BGA (*see* EBGA)
Environmental stress screening (ESS), 519–520
Environmental variables, 368–369
Epoxy resin, 98
  characteristics of, 100
Equivalent beam, 231–235
ESD, 15
Etchback, 299–302
External augmentation, 344–345
External board design, 368–369
External resistance, 455–456
External thermal design, 196–197
Extrinsic failures, 520–522

Failure analysis of solder joints, 184–185
Failure statistics, 413–414
Fanout vias, 116
Fatigue life, 431–437
Fatigue model correlation, 431–437
Fatigue strength, 535
FEM (*see* Finite element method)
Fiducials, 303–304
Field cycles as function of CTE, 184
Film coefficient, 455–456
Film resistance, 534–535
Finite element method (FEM), 230–234, 241–244, 252–255
Finite element modeling, 182–183, 230–234, 241–244, 252–255, 414–416
First-level interconnect concerns, 373
First-level packages, 2–4
Flip chip bonding, 110, 136–137
Flip chip soldering enhancement, 68
Forming and sintering, 76
FPIC, 50–51, 52
Frequency response, 281–282
Fringe, 235–238, 246–247
FTC, 546
Functional electrical test, 284

Geometric variables, 362–367
Glass ceramics, 83–85
Glass cloth, 99
Glob top BGAs, 545
Global deformations (*see* Macro deformations)
Global-local analysis (*see* Macro-micro analysis)
Glossary of terms, 555–612
Gold embrittlement, 75, 400–410
Gold in PBGA manufacture, 276
Grain boundary sliding, 380, 397–398
Grating, 234–237
Green sheets, 70–71, 136
Ground bounce, 347

HASL, 299
Heat dissipation in PBGA structure, 278–280
Heat-flow paths, 360
Heat transfer, 194–208, 336–339, 448–449
Heat transfer coefficient, 199, 204–207
Height-to-radius ratio, 398–399
Hermetic encapsulation, 138
Heterogeneous coarsening, 419
High I/O CBGA, 216–219
High-performance solder grid array, 342–343
High-temperature resistivity, 94–95
HLOOP2, 395
Horizontal flow control (HFC) nozzle, 495–496
Hot air solder level (*see* HASL)
Hot press method, 76

IC (*see* Integrated circuit)
IC chips, 1–4
ILB, 446
Imide resin, 98
Impedance, 346–349, 350, 355, 459–460
Impedance mismatches, 347–348
Inductance, 346–349, 351–355, 458–460
  (*See also RLC* equations)
Inductance comparisons, 150–151
Inductance, package-effective, 151–152
Inductance and PBGA, 280
Industry infrastructure for BGAs, 543–554
  (*See also* BGA industry)

Micron Ex. 1026, p. 145
Micron v. YMTC
IPR2024-00911

Inelastic strain, 381, 396
Infant mortalities, 518, 520
Infrared inspection, 470
Inner lead bonding (*see* ILB)
Inorganic BGAs, 543
Inspection of BGA, 465–489
  history of, 465–466
  methods of, 468–473
  problems of, 466–468
  visual, 466–467
Inspection of CBGA, 178–179, 478–487
Inspection equipment suppliers, 551
Institute for Interconnecting and Packaging Electronic Circuits, 314–315
Integrated circuit:
  and chip size, 9
  and density, 7–8
  and design cycles, 15–16
  and feature size, 11
  and operating voltage, 12–15
  and performance, 12, 13
  power supply of, 12–15
  and process technology, 6–7
  trends, 5–16
Interconnections:
  chip-level, 2, 136–137
  comparisons of, 150–151
  reliability of, 157–163
  techniques for, 136–137
Interfacial adhesion, 312–314
Interfacial fracture, 412
Intergranular cracking, 412
Internal thermal design, 194–195
Intrinsic failures, 520–522
Ionics, 284–285
IPC-SM-786, 315
IR process, 446

Joint Electron Device Engineering Council (JEDEC), 133–134, 174, 268, 274, 545, 551–552
Joint failure, 413–414
Joint versus bulk behavior, 396–398
Junction-to-ambient thermal resistance, 363–364
Junction temperature, 450, 456

Kapton, 98
Kerimide, 98

Laminates, 93–99
Lamination, 74
Land grid array (*see* LGA)
Large-size PBGA rework problems, 500–502
Layer factor, 118
Learning curves, 311–312
LGA, 331, 546
Linear elastic constants table, 415
Local deformations (*see* Micro deformations)
Lognormal distribution, 413, 422
Loss function, 18–19
Low-temperature-cofired ceramics, 83–85
LTCC (*see* Low-temperature-cofired ceramics)

Macro-CTE mismatch, 230
Macro deformations, 237–244
Macro-micro analysis, 229–230
Magnesia, 69
Manufacturers, 545–551
Manufacturing issues, 331–357
Materials commonly used in microelectronic packaging, 451
Materials set, electrical properties, 350–351
Materials variables, 361–362
mBGA, 40, 45, 46
MCC, 546
MCM, 51–56
MCM applications, 285–287
MCM-Cs, 51–52
MCM-Ds, 52
MCM-Ls, 52
MCM PBGA, 269–271
MCM yield, 55
Mechanical characterization of BGA solder joints, 383–410
Mechanical pressing, 76
Melting points, 69–70
Metal cap BGAs, 545
Metallurgy in PBGA manufacture, 275–278
μBGA, 40–42, 46–47
Micro deformations, 244–255
Micro-CTE mismatch, 230
Microprocessor packaging example, 154–157

Micron Ex. 1026, p. 146
Micron v. YMTC
IPR2024-00911

MIPS, 17, 18
Misregistration, 478
Mixed BGA, 48–51
MLC carrier performance, 151–152
MLC carriers, 135–136
Module-level burn-in, 139
Module pad diameter, 255–258
Moiré interferometry, 185, 224, 234–237
Moisture desorption (*see* Bakeout)
Moisture sensitivity, 37–39, 283, 312, 323
Molding compounds, 361–362, 550
Molding methods, 29–30
Motherboard design and PBGA thermal performance, 278–279
Motherboards for PBGA use, 272–275
Mullite, 78–79
Multichip module (*see* MCM)
Multilayer capability, 216
Multilayer ceramic carriers (*see* MLC carriers)
Multilayer cofiring, 70–75

Net rotation, 242–244
Next-generation BGAs, 38–51
No-clean flux assembly, 178, 274
Noise problems, 346–348, 372
Nonhermetic encapsulation, 138
Nonnormal forces, 526, 529
Normal deformation, 238–244
Normal force, 526, 528
Normal strain, 246–249
Normalized card-side solder volume, 255–258
Normalized module-size solder volume, 255–258
Norris-Landzberg, 244, 261
Numerical simulation modeling, 204–208
Nusselt number, 205

Octals, 436
Oil-canning, 181
OLB, 446
OMPAC™, 29, 295–298, 339–341, 351–352, 362
On/off cycles, 161–164
One-and-one-half-level packages, 2
Opens, 311, 475
Operating speed of IC, 15
Organic BGAs, 543–546
Outer lead bonding (*see* OLB)
Overmolded BGAs, 545
Overmolded Pad Array Carrier (*see* OMPAC)
Overmolding, 29–30

PAC, 295, 299, 546
Package configurations, 339–345
Package construction, electrical, 351–353
Package construction, thermal, 339–345
Package encapsulation, 137–138
Packaging glossary, 555–612
Pad carrier array (*see* PAC)
Pad metallization and creep behavior, 388–390
PBGA, 29–32
  advantages of, 90, 268–271
  failure analysis, 325–329
  future trends, 287–289
  for MCM applications, 269–271
  mechanical outline, 285–286
  package construction, 339–345, 351–353
  repair, 323–325
  surface mount advantages of, 268–269
  surface mount attach process, 274–275
  trends and future developments, 287–289
  weaknesses of, 271–272
PBGA assembly, 295–330
  failure analysis, 325–329
  methods of, 309–310
  placement considerations, 298–306
  process compliance, 306–308
PBGA design, 331–357
PBGA electrical considerations, 280–283
PBGA factory handling requirements, 312–323
PBGA manufacturing process, 275–278
PBGA packaging technology, 267–294
PBGA reliability, 283–285, 379–442
PBGA repair, 323–325
PBGA soldering yields, 310–312
PBGA thermal considerations, 278–280
PBGA versus CBGA, 90, 272
PBGA versus QFP, 373–376
PCB (*see* Printed circuit board)

Micron Ex. 1026, p. 147
Micron v. YMTC
IPR2024-00911

PCB and pin density, 117–119
PCB real estate, 115–116
PCB routing (*see* Printed circuit board)
PCMCIA, 1
Penetrating radiation inspection:
  infrared, 470
  ultrasound, 470–471
  x-ray, 471
PGA, 23, 25, 65
Photo via process, 108
Pin fins, 206
Pinouts, maximum, 299
Planarization, 509–510
Plastic ball grid array (*see* PBGA)
Plastic materials, 93–113
  fabrication of, 105–108
  overview, 93–100
Plastic pin grid array (*see* PPGA)
Plastic quad flat pack (*see* PQFP)
Plastic substrate, 93–113
  as BGA substrate, 111
  for direct chip attach, 108–110
Plastic substrate for direct chip attach, 108–110
  flip chip bonding and, 110
  wire bonding and, 109
Plating, 75
PLCC, 20
PMCM®, 269
Poisson's ratio, 231, 414
Polyethersulfone, 524–525
Polyimide resin, 98, 362
Polyvinyl butyryl (PVB) as binder, 71
Popcorn effect, 37–38, 283, 298, 312–314
Power distribution integrity, 371
Power and ground (P/G) inductance, 214–216
PPGA, 359
PQFP, 20, 194, 208–216, 268–269
Preforms, 309, 511–512
Pressure-cooker test (PCT), 103, 104–105, 284–285
Pressure-sensitive adhesive, 199, 203
Printed circuit board (PCB), 115–129
  BGA impact on fabrication of, 127–128
  and PBGA manufacture, 275–278
  routing complexity of, 117–125
  surface area requirements for, 115–116
Printed wiring board (PWB), 93–94
Process capability index, 304–305
Process compliance in PBGA technology, 306–308
Process variations in PBGA technology, 305
Production equipment, 548–551
Propagation delay, 371
PSA (*see* Pressure-sensitive adhesive)
Punching, 72

QFP, 190, 268, 311–312
Quad flat pack (*see* QFP)
Quartz fiber, 99

Racheting effect, 185, 188
Radiation, 448
Radiation inspection (*see* Penetrating radiation inspection)
Random failure, 518
Reduced instruction set computing (*see* RISC)
Registration markings, 302
Reinforced fiber, 99
Reliability of CBGA assembly, 223–265
Reliability of PBGA assembly, 379–442
Reliability testing, 283–285
Resin materials, 98
Resistance, 333–340, 345–349, 458, 460 (*See also RLC* equations)
Rework equipment vendors, 493–497
Rework process, 491–516
  of CBGA assemblies, 503–514
  definition of, 493
  of PBGA assemblies, 499–502
  of TBGA assemblies, 503–514
Rework process steps:
  cleaning and inspection, 513–514
  component removal, 507–508
  component replacement and reflow, 512–513
  site preparation, 508–510
  solder replenishment, 510–512
Rework/repair of CBGA modules, 179–182
RISC, 16
RLC equations, 195–196, 279–282, 449–460
Route factor, 118–119

Micron Ex. 1026, p. 148
Micron v. YMTC
IPR2024-00911

Sapphire, 68–69
SATT, 446
SBGA (*see* *Super*BGA™)
Scanning laser acoustic microscopy (*see* SLAM)
Screen printing, 72–74
Second-level packages, 2, 4–5
Semiconductor Industry Association (*see* SIA)
Semiconductor market, 5–8
Semiconductor packages, electrical requirements, 345–346
Semiconductor packages, noise problems, 346–348
Sequential process, 108
Shear deformation, 240–244
Shear modulus, 380–382
Shear strain, 227–228, 249–252
Shipping and scribing, 74
Shorts, 311
SIA, 8, 10
Signal delay, 214
Signal escape, 147–148
Signal fidelity, 371
Signal inductance, 212–213
Signal loading capacitance, 213–214
Signal-to-power ratios, 151–152
Silica, 69, 78
Silicon carbide (SiC), 83
SLAM, 316–317, 326–327, 470
SLICC, 38, 43, 189, 288
SMA, 546
Socket (*see* Burn-in socket)
Soft error, 535
Soft tooling, 72
Solder, 23–29
Solder alloy deformation constants, 394
Solder alloys, 383, 394
Solder defects, typical, 179, 180, 309–312
Solder joint:
  characteristics of, 383–386
  cracking of, 417–426
  failure, 184–185, 328–329
  reliability, 183–184, 379–442
Solder joint strain, 223–265
Solder joint test samples, 383–410
Solder mask material, 112
Solder replenishment, 510–512
Solder temperature resistivity test, 95
Soldering yields, 310–312
Solid logic technology (SLD), 65
Solid solder deposition (*see* SSD)
SPC, 478–480
SRAM, 8, 10
SSD, 309
Staggered-grid BGA, 125–126
Static burn-in, 519
Static random access memory (*see* SRAM)
Statistical process control (*see* SPC)
Steady-state burn-in, 519
Steady-state creep, 380–382, 386–391
Steady-state strain rate, 380–382
Stiffener, 446
Strain analysis, 229–263
Strain distribution, 223–265
Strain energy density, 423, 425
Strain-hardening law, 381
Stress exponent, 380, 392
Stress relaxation, 524, 536
Stress and strain equations, 384–386
Substrate characteristics, 100–104
Substrate dielectric material, 361–362
Substrate fabrication process, 105–108
Substrate materials/suppliers, 550
Substrate stability, 111–112
Subtractive process, 105–107
*Super*BGA™, 43, 45, 48, 288–289
Superplasticity, 380
Suppliers, 545–551
Surface illumination inspection, 469–470
Surface laser acoustic microscope (*see* SLAM)
Surface mount advantages of PBGA, 268–269
Surface mount attach process, 274–275
Switching noise, 372

TAB, 66–67, 137
  (*See also* ATAB BGA)
TBGA (*see* ATAB BGA)
TBGA assembly, 445–446
TBGA reliability, 446–447
TBGA structure, 443–445
Tape automated bonding (*see* ATAB BGA)
Tape-based BGAs, 545

Micron Ex. 1026, p. 149
Micron v. YMTC
IPR2024-00911

Tape casting, 72
TBGA, 32–33
  (*See also* ATAB BGA)
TCP, 22–23
TDBI (*see* Test during burn-in)
Temperature cycle, 284
Tensile stress, 385–386, 392–399
Test during burn-in (TDBI), 519
Test socket suppliers, 551
Testing to failure, 284
Thermal attributes of CBGA/CCGA packages, 153–157
Thermal coefficient of expansion (TCE), 68, 97, 136
Thermal conductivity of various materials, 366, 451
Thermal cycle performance, 426–430
Thermal cycle reliability studies, 426–430
Thermal cycling, 184–187
Thermal design:
  experimental study, 197–208
  external, 196–197
  internal, 194–195
Thermal dissipation, 89–90, 111, 278–280
Thermal fatigue, 158–163, 410–436
Thermal management of ATAB BGA, 447–457
Thermal management of CBGA, 194–208
Thermal management of PBGA, 333–345, 359–369
Thermal management of TBGA, 447–457
Thermal measurement, 456–457
Thermal performance:
  improvement of, 341–345
  materials affecting, 335
  and package size, 362–365
  and package substrate design, 365–366
  variables affecting, 361–369
Thermal planes, 341–342
Thermal profiling, 500–501
Thermal resistance, 194–208, 279, 449–450, 457
Thermal transfer basics, 334–339
Thermal transfer equations, 336–337
Thermal vias, 206–207, 279, 341, 365–366
Thermocouple, 501
Third-level packages, 2
Three-dimensional modeling (*see* Finite element modeling)
Through-hole reliability, 106–107
Time-dependent deformations, 393–395
Time of flight, 371
Time-independent deformations, 393–395
Trace length, 211–212
Transfer function, 282
Transfer tape method, 76–77
Transgranular cracking, 412
Transient creep, 381
Transient creep coefficient, 381
T-Sam test, 284
TSOP, 21–22, 23
Tungsten, 78, 80, 82, 353

ULSI, 12
Ultrasound inspection, 470–471
Ultrathin TCP, 22–24
Unit marking, 277
Unit of work, 30
Upilex, 445
User's perspective of PBGA, 359–377

Variables:
  environmental, 368–369
  geometric, 362–367
  materials, 361–362
Variables, nomenclature, 438–439
Vendor-related packaging failures, 521–522
Vendors, 545–551
Vendor's perspective of PBGA, 331–357
  and electrical performance, 345–355
  and thermal performance, 334–345
Via hole filling, 72
Via pad diameter, 121–122
Via-in-pad geometry, 173
Viscoplastic strain energy density, 418, 423, 425
VLSI, 12
Voiding, 475
Voltage bounce, 347
Voltage, IC operating, 12–15

Micron Ex. 1026, p. 150
Micron v. YMTC
IPR2024-00911

Voltage potential equation, 347
Von Mises relation, 382, 392–393

Warpage, 475, 485–486
Water absorption, 97
Weibull distribution, 413
Wire bonding (Figs. 1.2, 1.3), 3
Wire bonding, 109–110, 137, 288
Wiring density, 86–88

X-ray, cross-sectional, 474–475
X-ray diffraction intensities, 78–79
X-ray inspection, 179, 275, 471–475
X-Y placement, 303–306

Young's modulus, 415

Zero-level packages, 2

Micron Ex. 1026, p. 151
Micron v. YMTC
IPR2024-00911

ABOUT THE EDITOR

John H. Lau is a senior engineer of Hewlett-Packard Company in Palo Alto, California. His research activities cover a broad range of electronics packaging and manufacturing technology. He has more than 24 years of research and development experience in applying the principles of engineering and science to the electronic, petroleum, nuclear, and defense industries. He has authored and coauthored over 100 technical publications in these areas and is the author and editor of the books *Solder Joint Reliability: Theory and Applications, Handbook of Tape Automated Bonding, Thermal Stress and Strain in Microelectronics Packaging, Handbook of Fine Pitch Surface Mount Technology, The Mechanics of Solder Alloy Interconnects,* and *Chip On Board Technologies for Multichip Modules.* He is an associate editor of the *ASME Transactions,* the *Journal of Electronic Packaging,* and the *IEEE Transactions on Components, Packaging, and Manufacturing Technology.*

Micron Ex. 1026, p. 152
Micron v. YMTC
IPR2024-00911

TK7870.16/.B21/1995
Ball grid array technology / John H. Lau, editor.

ddoz c. 1 SVO

Micron Ex. 1026, p. 153
Micron v. YMTC
IPR2024-00911