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THIRD EDITION

CMOS

Circuit Design, Layout, and Simulation

R. JACOB BAKER

IEEE Series on Microelectronic Systems

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Multipliers

Name	Symbol	Value
terra	T	10^{12}
giga	G	10^{9}
mega	M (MEG in SPICE)	10^{6}
kilo	k	10^{3}
milli	m	10^{-3}
micro	μ (or u)	10^{-6}
nano	n	10^{-9}
pico	p	10^{-12}
femto	f	10^{-15}
atto	a (not used in SPICE)	10^{-18}

Physical Constants

Name	Symbol	Value/Units
Vacuum dielectric constant	ε_0	8.85 aF/μm
Silicon dielectric constant	ε_{si}	$11.7\varepsilon_0$
SiO_2 dielectric constant	ε_{ox}	$3.97\varepsilon_0$
SiN_3 dielectric constant	ε_{Ni}	$16\varepsilon_0$
Boltzmann's constant	k	1.38×10^{-23} J/K
Electronic charge	q	1.6×10^{-19} C
Temperature	T	Kelvin
Thermal voltage	V_T	$kT/q = 26$ mV @ 300K

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To my wife Julie

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Preface

CMOS (complementary metal oxide semiconductor) technology continues to be the dominant technology for fabricating integrated circuits (ICs or chips). This dominance will likely continue for the next 25 years and perhaps even longer. Why? CMOS technology is reliable, manufacturable, low power, low cost, and, perhaps most importantly, scalable. The fact that silicon integrated circuit technology is scalable was observed and described in 1965 by Intel founder Gordon Moore. His observations are now referred to as *Moore's law* and state that the number of devices on a chip will double every 18 to 24 months. While originally not specific to CMOS, Moore's law has been fulfilled over the years by scaling down the feature size in CMOS technology. Whereas the gate lengths of early CMOS transistors were in the micrometer range (long-channel devices) the feature sizes of current CMOS devices are in the nanometer range (short-channel devices).

To encompass both the long- and short-channel CMOS technologies in this book, a two-path approach to custom CMOS integrated circuit design is adopted. Design techniques are developed for both and then compared. This comparison gives readers deep insight into the circuit design process. While the square-law equations used to describe MOSFET operation that students learn in an introductory course in microelectronics can be used for analog design in a long-channel CMOS process they are not useful when designing in short-channel, or nanometer, CMOS technology. The behavior of the devices in a nanometer CMOS process is quite complex. Simple equations to describe the devices' behavior are not possible. Rather electrical plots are used to estimate biasing points and operating behavior. It is still useful, however, for the student to use mathematical rigor when learning circuit analysis and design and, hence, the reason for the two-path approach. Hand calculations can be performed using a long-channel CMOS technology with the results then used to describe how to design in a nano-CMOS process.

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What's new in the third edition of CMOS? The information discussing computer-aided design (CAD) tools (e.g., Cadence, Electric, HSPICE, LASI, LTspice, and WinSpice) has been moved to the book's webpage, **http://CMOSedu.com**. In addition, chapters were added covering the implementation of data converters and feedback amplifiers. This additional, practical, information should make the book even more useful as an academic text and companion for the working design engineer. As in the earlier editions, the book is filled with practical design examples, discussions, and problems. The solutions to the end-of-chapter problems (for self-study) and the netlists used when simulating the circuits are found at CMOSedu.com. Additional problems are also found at this website. Those interested in gaining an in-depth knowledge of CMOS analog and digital design will be greatly aided by downloading, modifying, and simulating the design examples found in the book.

The assumed background of the reader is a knowledge of linear circuits (e.g., RC and RLC circuits, Bode plots, Laplace transforms, AC analysis, etc.), microelectronics (e.g., diodes, transistors, small-signal analysis, amplifiers, switching behavior, etc.), and digital logic design. Several courses can be taught using this book including VLSI or CMOS digital IC design (chapters 1–7 and 10–19), CMOS analog IC design (chapters 9 and 20–24), and advanced analog IC design (chapters 8 and 25–31).

How will this book be useful to the student, researcher, or practicing engineer?

A great deal of effort has gone into making this book useful to an eclectic audience. For the student, the book is filled with hundreds of examples, problems, and practical discussions (according to one student there can never be too many examples in a textbook). The layout discussions build a knowledge foundation important for troubleshooting and precision or high-speed design. Layout expertise is gained in a step-by-step fashion by including circuit design details, process steps, and simulation concerns (parasitics). Covering layout in a single chapter and decoupling the discussions from design and simulation was avoided. The digital design chapters emphasize real-world process parameters (e.g., I_{off} , I_{on} , t_{ox} , VDD). The analog chapters provide coherent discussions about selecting device sizes and design considerations. Likewise "cookbook" design procedures for selecting the widths/lengths of MOSFETs and design using long-channel equations in a short-channel process are not present. The focus is on preparing the student to "hit the ground running" when they become a custom CMOS IC designer or product engineer.

For the researcher, topics in circuit design such as noise considerations and sensing using delta-sigma modulation (DSM) continue to be important in nanometer CMOS. For example, in Ch. 17 the use of DSM has been applied to CMOS image sensors, Flash memory, and memory using thin oxides (direct tunneling). Sensing using DSM is important because it makes use of the fact that as CMOS clock speeds are going up, the gain and matching of transistors is deteriorating. Further, Ch. 8 discusses noise-limited design issues such as, "Why can't I improve the signal-to-noise ratio in my imaging chip?" or "Why is integrating thermal or flicker noise harmful?"

For the working engineer, the book provides design and layout examples that will be immediately useful in products. At the risk of stating the obvious, matching, power, speed, process shifts, power supply voltage variations, and temperature behavior are extremely important in practical design. The discussions and examples found in this book

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are focused on these topics. Phase-locked loops, charge pumps, low-voltage references, single and fully-differential op-amp designs, continuous-time and clocked comparators, memory circuits, etc., are covered in detail with numerous examples. To ensure the most practical computer validation of the designs, the simulations for the nanometer designs (a 50 nm process) use the BSIM4 SPICE models. Again, all of the book's simulation examples are available at CMOSedu.com.

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R. Jacob (Jake) Baker

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Chapter

4

The Active and Poly Layers

The active, n-select, p-select, and poly layers are used to form n-channel and p-channel MOSFETs (NMOS and PMOS respectively) and so metal1 can make an ohmic contact to the substrate or well. The active layer, in a layout program, defines openings in the silicon dioxide covering the substrate (see Figs. 2.3 and 2.4). The n-select and p-select layers indicate where to implant n-type or p-type atoms, respectively. The active and select layers are always used together. The active defines an opening in the oxide and the select then dopes the semiconductor in the opening either n-type or p-type.

The poly layer forms the gate of the MOSFETs. Poly is a short name for polysilicon (not to be confused with the poly, or polygon, object in a layout program). Polysilicon is made up of small crystalline regions of silicon. Therefore, in the strictest sense, poly is not amorphous silicon (randomly organized atoms), and it is not crystalline silicon (an orderly arrangement of atoms in the material) such as the wafer.

4.1 Layout using the Active and Poly Layers

We've covered the following fabrication layers in Chs. 2 and 3: n-well, metal1, via1, metal2, and overglass. In this section we cover the following additional fabrication layers: active, n-select, p-select, poly1, silicide block, and contact.

The Active Layer

Examine the layout of a box and the corresponding angled view (the fabrication results) seen in Fig. 4.1. The box is drawn on the active layer and indicates where to open a hole in the field oxide (FOX). These openings are called active areas. The field area (the area that isn't the active area, which is the area where the FOX is grown) is used for routing wires (connecting the circuit together). The MOSFETs are fabricated in the bulk (the p-substrate or the n-well) in these active openings. The FOX is used to isolate the devices from one another (the active areas are isolated by the FOX). Note that there will be some resistive connection between active areas (either through the substrate or the n-well). However, the FOX is grown thick enough to keep the interactions between adjacent active areas to a minimum.

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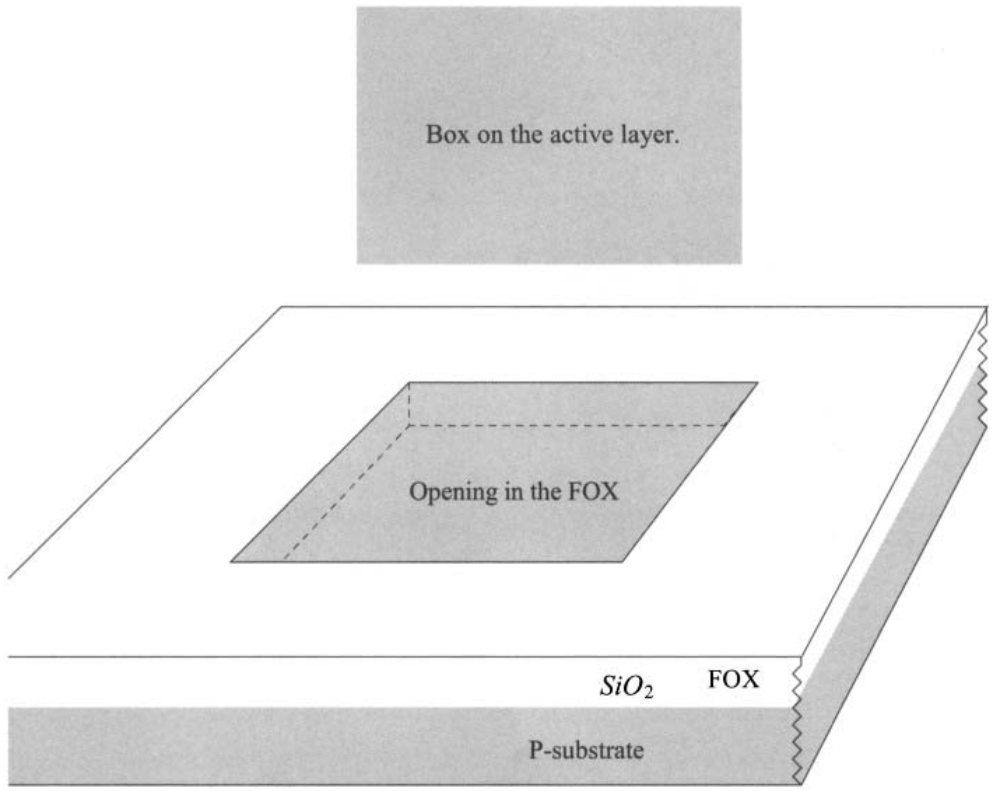

Figure 4.1 How the active layer specifies where to open holes in the field oxide (FOX).

The P- and N-Select Layers

Surrounding the active layer with either the n-select or p-select layers dopes the semiconductor n- or p-type. Figure 4.2 shows several combinations of selects, n-well, and active layers. In (a) and (b) for example, the opening in the FOX is implanted p-type (in the location determined by the p-select mask). When learning to do design and layout, it's important to be able to see a layout and then visualize the corresponding cross-sectional views.

Also seen in this figure (see 4.2i and j) is how a single layer (called the n+ layer) can be used instead of two layers (the active and n-select layers). The n+ layer in (j) is used directly for the active mask (openings in the FOX) in (i). The n-select in (i) is a *derived* mask. It is derived by bloating the size of the n+ layer. The n-select mask must be larger than the active mask due to misalignment. If the implant (select) isn't aligned directly over the active opening in the FOX, then the semiconductor exposed in the active opening won't get doped. If the select and active masks could be aligned perfectly, the select layers wouldn't need to be larger than the active layer. Also note that using a select without active causes the implant to bombard the FOX. Since the FOX is thick, it keeps the implanted atoms from reaching the substrate.

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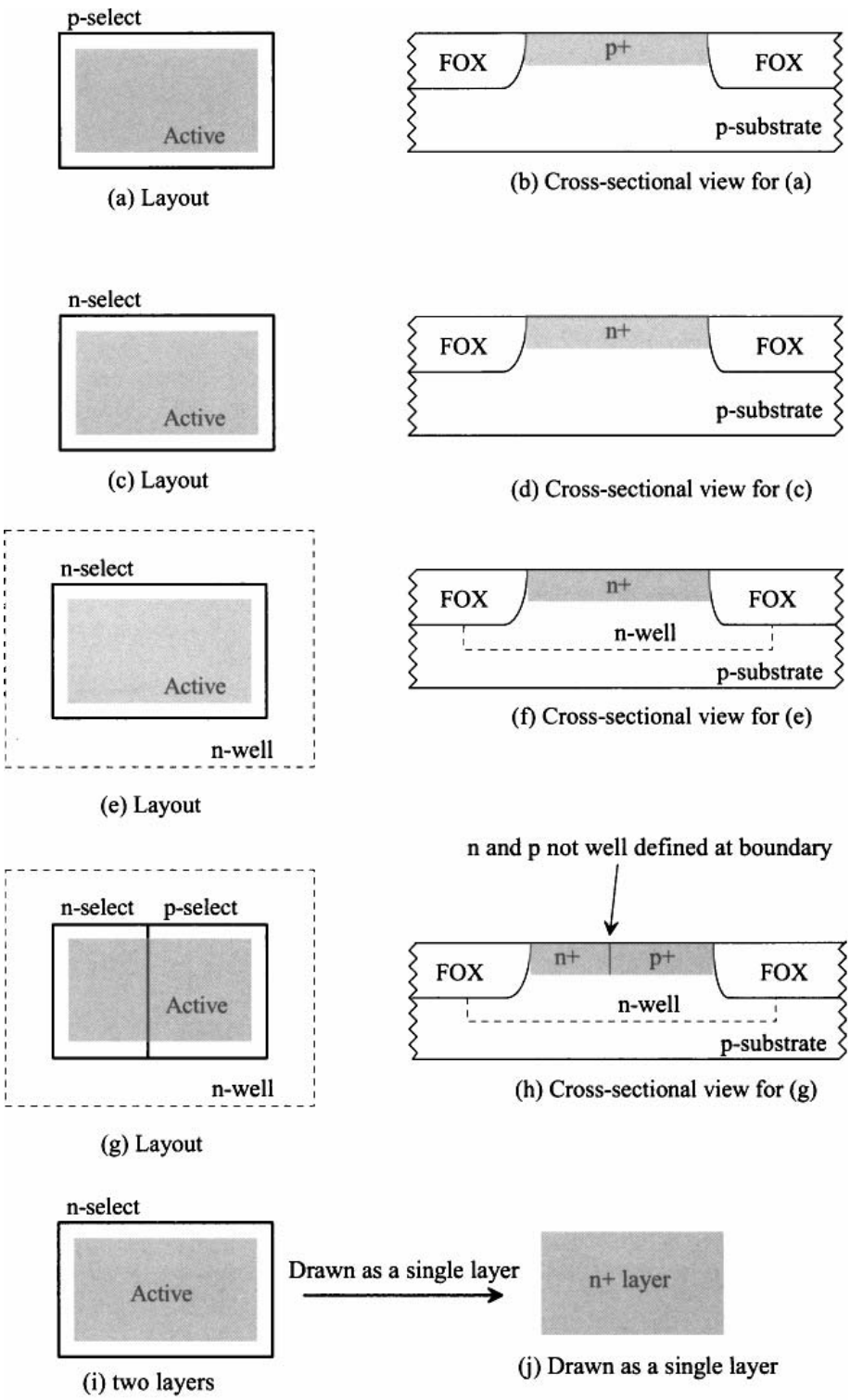

Figure 4.2 Combinations of active, selects, and n-wells.

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The Poly Layer

The poly layer is used for MOSFET formation. Consider the layout seen in Fig. 4.3a. Drawing poly over active produces a MOSFET layout. If we see a complicated layout, it is straightforward to determine the number of MOSFETs in the layout simply by counting how many times poly crosses active. Note that the gate of the MOSFET is formed with the polysilicon, and the source and drain of the MOSFET are formed with the n+ implant. Further note that the source and drain of an integrated MOSFET (in a general CMOS process) are interchangeable. We are not showing the (required) contact to the substrate (the body of the MOSFET). The body connection will be covered in a moment (the MOSFET is a four-terminal device).

Self-Aligned Gate

Notice how, Fig. 4.3b or c, the area under the poly gate isn't doped n+. After the opening in the FOX is formed with the active mask, a thin insulating oxide is grown over the opening. This is the MOSFET's gate oxide (GOX), Fig. 4.3b. Next, the poly mask specifies where to deposit the polysilicon gate material. This is followed by applying the implant in the areas specified by the n-select mask. The implant easily penetrates through the thin GOX into the source and drain areas. However, the polysilicon gate acts like a mask to keep the n+ atoms from penetrating under the MOSFET's gate (the poly is made thick enough to ensure the implant doesn't reach the GOX). Also, the drain and gate become self-aligned to the source/drain of the MOSFET. This is important because we know we can't perfectly align the poly mask to the active masks.

Example 4.1
Comment on the problems with the MOSFET layout seen in Fig. Ex4.1.

In Fig. Ex4.1a the active layer defines an opening in the field oxide. The select masks are placed exactly where the desired n+ implants will occur, as seen in Fig. 4.3. However, due to shifts in the select mask, relative to the poly mask, the area directly next to the gate will not get implanted. (Redraw Fig. Ex. 4.1b with the poly layer shifted left or right.) Notice how the incorrect layout in Fig. Ex4.1b looks exactly the same as the correct layout in Fig. 4.3a. ■

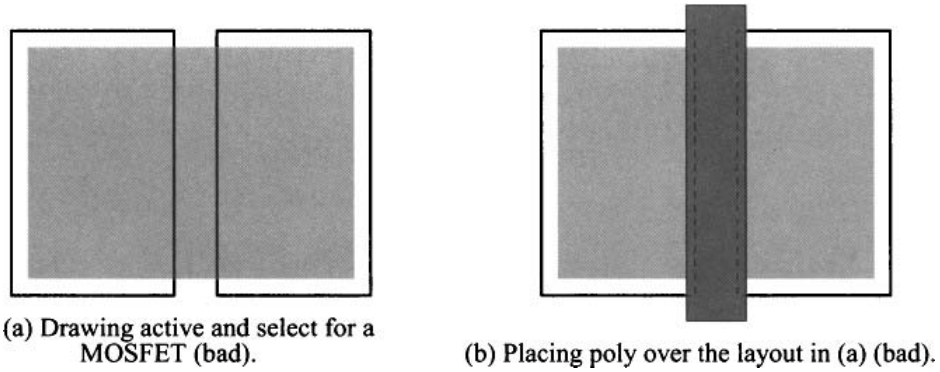

Figure Ex4.1 Bad layout examples (what NOT to do).

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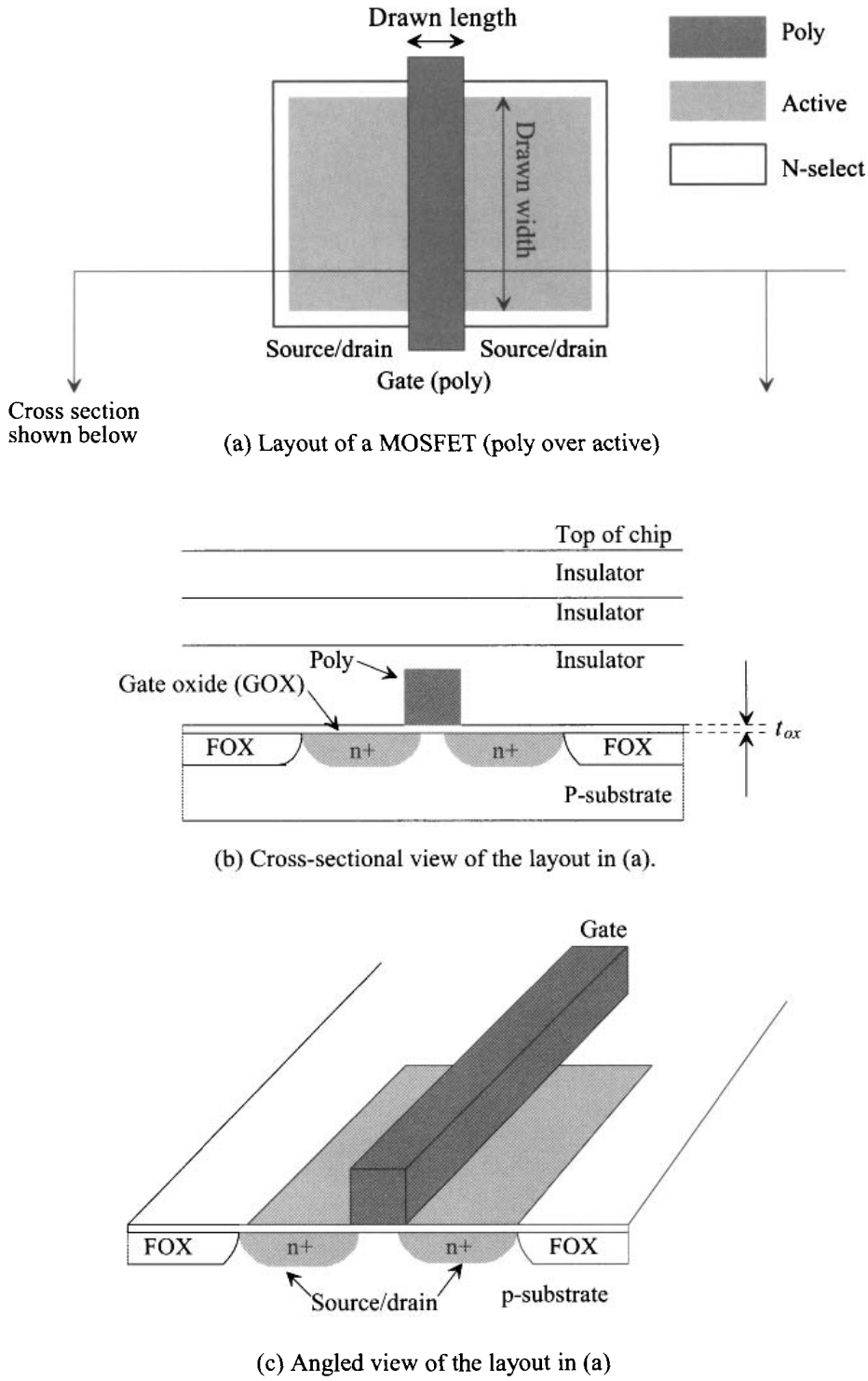

Figure 4.3 Layout and cross-sectional views of a MOSFET.

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The Poly Wire

The poly layer can also be used, like metal1, as a wire. Poly is routed on top of the FOX. The main limitation when using the poly layer for interconnection is its sheet resistance. As we saw in the last chapter, the sheet resistance of the metal layers is approximately 0.1 Ω/square. The sheet resistance of the doped poly can be on the order of 200 Ω/square. The capacitance to substrate is also larger for poly simply because it is closer to the substrate (see Table 3.1). Therefore, the delay through a poly line can be considerably longer than the delay through a metal line. To reduce the sheet resistance of poly (and of the implanted active regions), a silicide (a material that is a mixture of silicon and a refractory metal like tungsten) is deposited over the MOSFET and field region, Fig. 4.4. The silicide and poly gate sandwich is called a polycide.

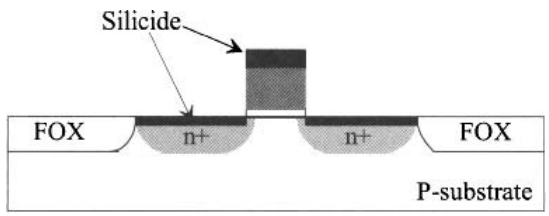

Figure 4.4 How the gate and drain/source of a MOSFET are silicided to reduce sheet resistance.

Table 4.1 gives some typical values of sheet resistance, R_{square}, for well, poly, n+, and p+ in a nm CMOS process. When we use the poly as a mask to self-align the source and drain regions of the MOSFET to the gate, Fig. 4.3, we dope the poly either n-type (for an NMOS device) or p-type (for a PMOS device). Silicide is then used to avoid forming a pn-junction (diode) when the PMOS and NMOS polysilicon gates are connected together in the field region (the silicide electrically shorts the n- and p-type poly gates together). The other specifications seen in the table will be discussed in the next chapter.

Table 4.1 Typical properties of resistive materials in a nm CMOS process.

Silicide	Resistor type	R_{square} (ohms/sq) AVG.	*TCR*1 (ppm/C) AVG.	*TCR*2 (ppm/C^2) AVG.	*VCR*1 (ppm/V) AVG.	*VCR*2 (ppm/V^2) AVG.	Mismatch % $\Delta R/R$
N/A	well	500 ± 10	2400 ± 50	7 ± 0.5	8000 ± 200	500 ± 50	< 0.1
No	n+ poly	200 ± 1	20 ± 10	0.6 ± 0.03	700 ± 50	150 ± 15	< 0.5
No	p+ poly	400 ± 5	160 ± 10	0.8 ± 0.03	600 ± 50	150 ± 15	< 0.2
No	n+	100 ± 2	1500 ± 10	0.04 ± 0.1	2500 ± 50	350 ± 20	< 0.4
No	p+	125 ± 3	1400 ± 20	0.4 ± 0.1	80 ± 80	100 ± 25	< 0.6
Yes	n+ poly	5 ± 0.3	3300 ± 90	1.0 ± 0.2	2500 ± 125	3800 ± 400	< 0.4
Yes	p+ poly	7 ± 0.1	3600 ± 50	1.0 ± 0.2	2500 ± 400	5500 ± 250	< 0.7
Yes	n+	10 ± 0.1	3700 ± 50	1.0 ± 0.2	350 ± 150	600 ± 60	< 1.0
Yes	p+	20 ± 0.1	3800 ± 40	1.0 ± 0.2	150 ± 50	800 ± 40	< 1.0

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Silicide Block

In some situations (as in making a resistor), it is desirable to keep from depositing the silicide on the gate poly or source/drain regions. A layer called the silicide block can be used for this purpose. Consider the following example.

Example 4.2
Estimate the delay through the poly wire in Fig. 4.5 with and without silicide. The width of the wire is 1 and the length is 1,000. Use a scale factor of 50 nm and the values for capacitance in Table 3.1. Simulate the delay using SPICE.

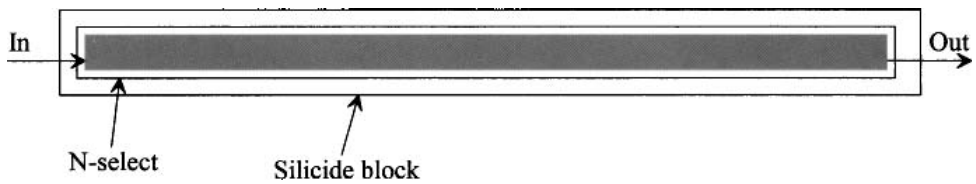

Figure 4.5 Estimating the delay through a polysilicon line with and without a silicide.

The capacitance of the poly wire to substrate doesn't depend on the presence or absence of the silicide. Using the data from Table 3.1, we can estimate the capacitance of the poly wire to substrate as

$$C_{poly} = C_{plate} \cdot area_{drawn} \cdot (scale)^2 + C_{fringe} \cdot perimeter_{drawn} \cdot scale \qquad (4.1)$$

or

$$C_{poly} = (58\ aF) \cdot (1,000) \cdot (0.05)^2 + (88\ aF) \cdot (2,002) \cdot (0.05) \approx 9\ fF$$

The resistance of the poly wire is calculated using

$$R = R_{square} \cdot \frac{L}{W} \qquad (4.2)$$

From the data in Table 4.1, the resistance of the wire is either 200k (no silicide) or 5k (with silicide). The delays are then calculated as

$$t_d = 0.35 \cdot 9\ fF \cdot 200k = 630\ ps \text{ and } t_d = 0.35 \cdot 9\ fF \cdot 5k = 16\ ps$$

The simulation results are seen in Fig. 4.6. In the simulation netlist we divided the line up into 1,000 squares. The capacitance/square is 9 aF (remembering SPICE doesn't recognize "a" so we use e-18). The resistance/square is either 200 Ω (no silicide) or 5 Ω (with a silicide). ■

Note that the silicide block layer should not be placed under (surround) a contact to polysilicon or active else a rectifying contact may form (this is important).

4.1.1 Process Flow

A generic CMOS process flow is seen in Fig. 4.7. The fabrication of both PMOS and NMOS devices is detailed in this figure. This figure doesn't show the initial steps taken to fabricate the n-well (and/or p-well) but rather starts with the wells already fabricated.

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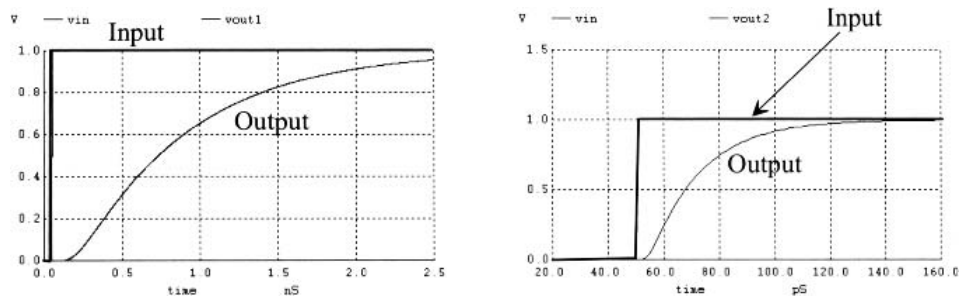

(a) Poly without silicide (b) Silicided poly

Figure 4.6 Simulated delay through poly wires.

The first step, Fig. 4.7a, is to grow a thin pad oxide on top of the entire wafer. This is followed by depositing nitride (the pad oxide is used as a cushion for the nitride) and photoresist layers. The photoresist is then patterned using the active mask. The remaining photoresist, seen in Fig. 4.7a, ultimately defines the openings in the FOX.

In Fig. 4.7b the areas not covered by the photoresist are etched. The etching extends down into the wafer so that *shallow trenches* are formed. In (c) the shallow trenches are filled with SiO_2. These trenches isolate the active areas and form the field regions (FOX). This type of device isolation is called shallow trench isolation (STI).

In (d) two separate implants are performed to adjust the threshold voltages of the devices. A photoresist is patterned (twice) to select the areas for threshold voltage adjust.

Figure 4.7e shows the results after the deposition and patterning of polysilicon (for the MOSFET gate material). This is followed by several implants. In (f) we see a shallow implant to form the MOSFET's lightly doped drains (LDD). The LDD implants prevent the electric field directly next to the source/drain regions from becoming too high (this is discussed further in Ch. 6). Note that the poly gate is used as a mask during this step.

The next step is to grow a spacer oxide on the sides of the gate poly, Fig. 4.7g. After the spacer is grown, the n+/p+ implants are performed. This implant dopes the areas used for the source/drain of the MOSFETs as well as the gate poly. The last step is to silicide the source and drain regions of the MOSFET. This is important for reducing the sheet resistances of the polysilicon and n+/p+ materials, as indicated in Table 4.1.

Finally, note that the process sequence seen in Fig. 4.7 is often called, in the manufacturing process, the front-end of the line (FEOL). The fabrication of the metal layers and associated contacts/vias is called the back-end of the line (BEOL).

Damascene Process Steps

The process of: 1) making a trench, 2) (over) filling the trench with a material, and 3) grinding the material down until the top of the wafer is flat is called a Damascene process (a technique used, and invented, by craftsman in the city of Damascus to inlay gold or silver in swords). The STI process just described is a Damascene process. More often, though, the Damascene process is associated with the metal layers in a CMOS process. Trenches are formed in the insulators. Copper, for example, is then deposited in the trenches. The top of the wafer is then ground down until it is flat.

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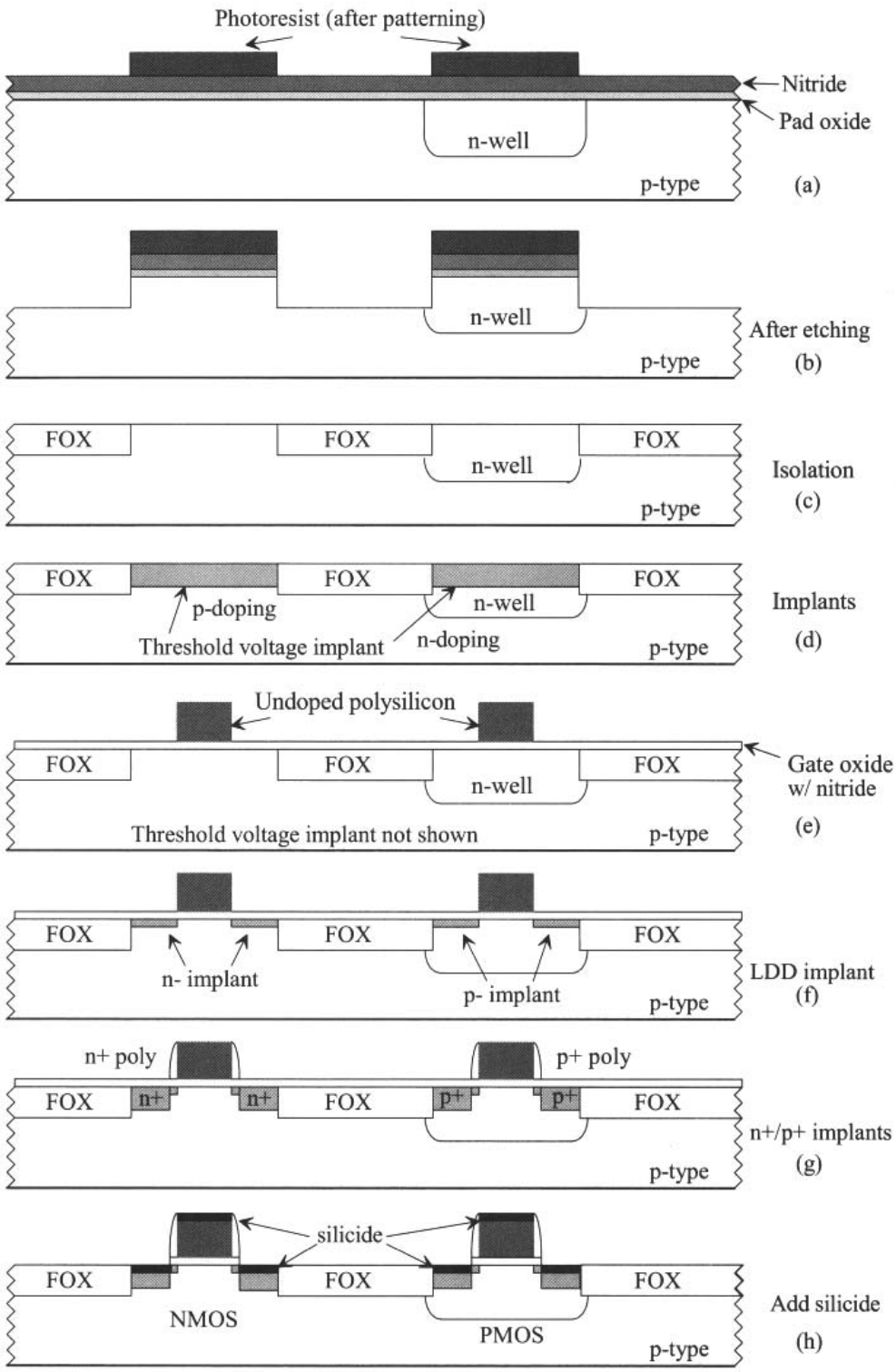
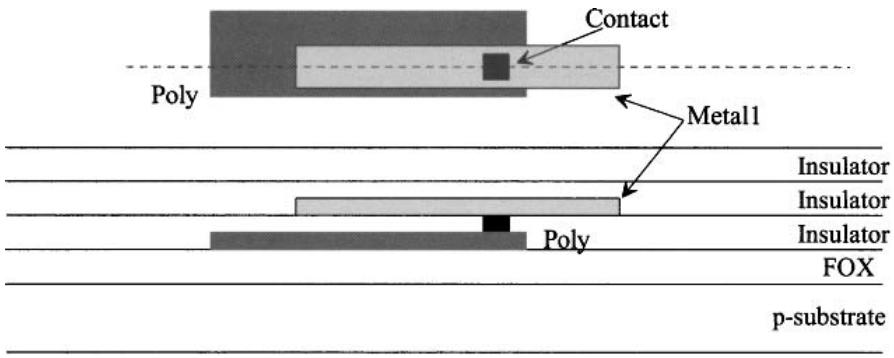


Figure 4.7 General CMOS process flow.

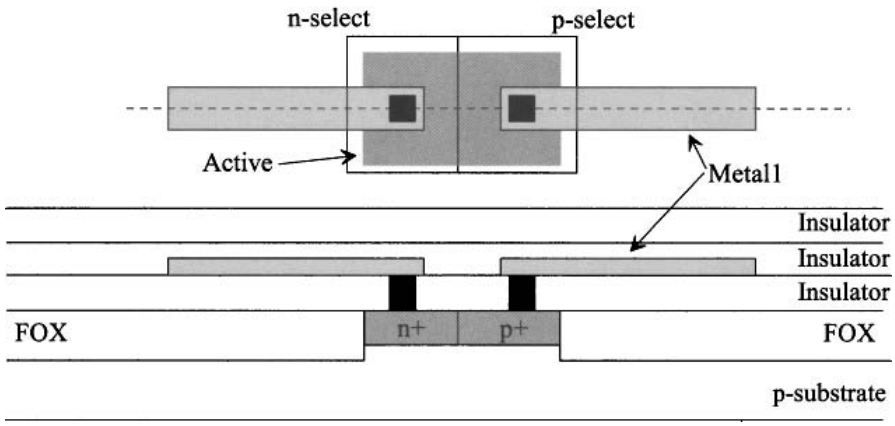
4.2 Connecting Wires to Poly and Active

In the last section we discussed how to lay out active areas and polysilicon. Here, in this section, let's discuss how to connect metal wires to poly and active. The contact layer connects metal1 to either active (n+/p+) or poly. Unless we want to form a rectifying contact (a Schottky diode), *we never connect metal directly to the substrate or well.* Further, we won't connect metal to poly without having the silicide in place. Never put a silicide block around a contact to poly.

Figure 4.8a shows a layout and corresponding cross-sectional view of the layers metal1, contact, and poly (a contact to poly). Figure 4.8b shows a connection to n+ and p+. Note that, like we did with the via cell in Fig. 3.13, we can layout contact cells to poly, n+, and p+. Further note that metal1 is connected to either metal2 (through via1) or poly/active. Metal2 can't be connected to active/poly without first connecting to metal1 and a contact.



(a) Metal1 connecting to poly through a contact.



(b) Contacts to active.

Figure 4.8 How metal1 is connected to poly and active.

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When etching an opening for a contact to poly or active, an etchant stop layer is used. The etchant stop is put down directly on top of the FOX prior to depositing the insulator.

Connecting the P-Substrate to Ground

So far, throughout the book, we've said that the p-substrate is at ground potential. However, we haven't actually said how we connect the substrate to ground (the substrate must be connected to the ground pad through a wire). The substrate, as seen in Fig. 4.4, is the body of the NMOS devices and is common to all NMOS devices fabricated on the chip (assuming an n-well process, see Fig. 2.24). Towards connecting the substrate to ground, consider the layout seen in Fig. 4.9. Again note that we only connect metal1 to p+ (or n+/poly) and not directly to the substrate. Further notice that poly sits on the FOX while metal1 sits on the insulator above FOX.

An important consideration when "tying down the substrate" is the number of places, around the chip, the substrate is tied to ground. We don't just connect the substrate to ground with one connection, like the one seen in Fig. 4.9, and assume that the entire chip's substrate is grounded. The reason for this is that the substrate is a resistive material. The circuitry fabricated in the substrate (in the bulk) has leakage currents (DC and AC) that flow in the p-type semiconductor of the substrate. The result is an increase in the substrate's potential above ground in localized regions of the chip. Ideally, the current flowing in the substrate is zero. In reality it won't be zero but will have some value that depends on the location and the activity of the on-chip circuitry. A substrate connection provides a place to remove this substrate current (a point of exit), keeping the substrate potential at ground. In practice, substrate connections are used wherever possible (more on this topic when we cover standard cell frames later in the chapter).

The body for the PMOS devices is the n-well. The n-well must also be tied to a known voltage through n+ and metal1. For the PMOS's body connection, an n+ region is placed in the n-well and connected with a metal1 wire to (for digital design) *VDD*. If an n-well is laid out and used to make a resistor or for the body of a PMOS device, then there must be n+ in the n-well.

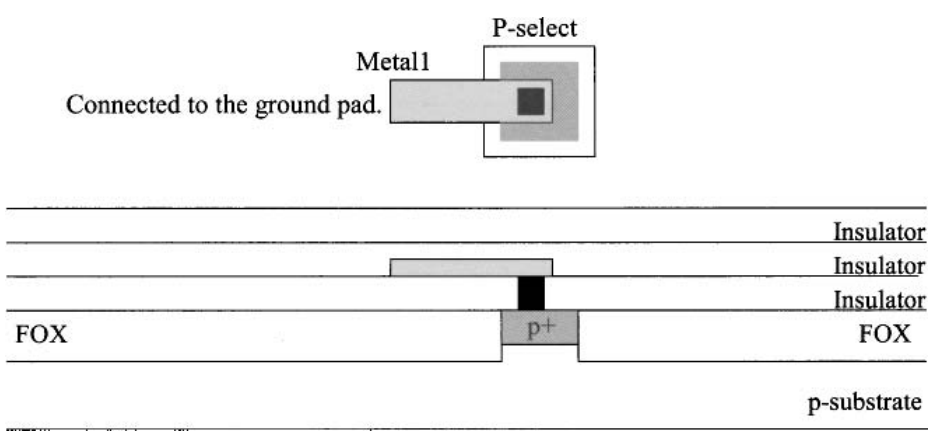

Figure 4.9 Connecting the substrate to ground.

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Layout of an N-Well Resistor

The layout of an n-well resistor is seen in Fig. 4.10. On each side of the resistor, n+ regions are implanted so that we can drop metal1 down and make a connection. We aren't showing the silicide in the cross-sectional view (Fig. 4.4). Further, after reviewing Table 4.1, we see that the sheet resistance of the n+ regions is small compared to the sheet resistance of the n-well. When we calculate the number of squares, we measure between edges of active as seen in the figure. This results in a small error in the measured resistance compared to the actual resistance. The variation in the sheet resistance with process shifts (say 20%) makes this error insignificant. The next chapter will discuss the layout of resistors in more detail.

Notice that if the substrate is at ground, we can't apply a potential on either side of the wire less than, say, –0.5 V for fear of turning on the n-well to substrate parasitic diode. These parasitics, as discussed in Ch. 2, are an important concern when laying out resistors.

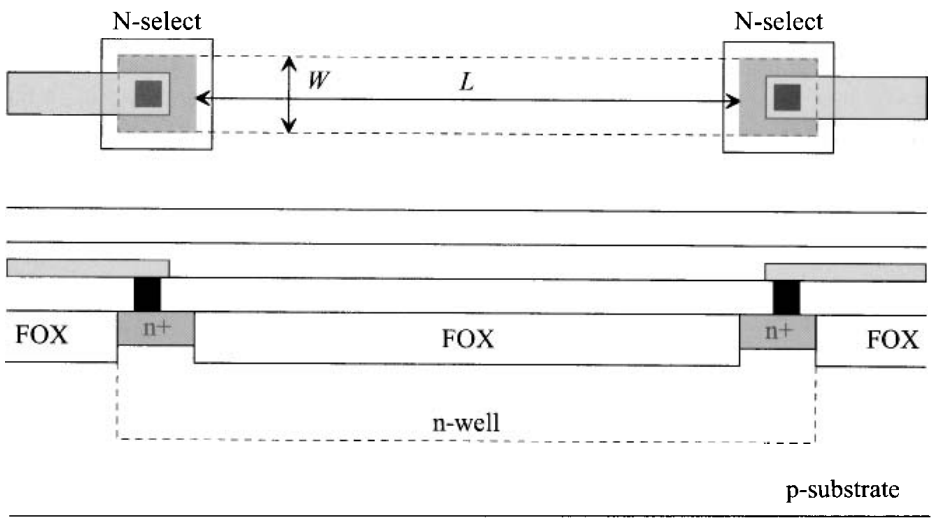

Figure 4.10 Layout of an n-well resistor and the corresponding cross-sectional view.

Example 4.3

Consider the layout for a metal1 connection to an n-well resistor seen in Fig. 4.11. Will the extension of the n+ beyond the n-well affect the resistor's operation? Why or why not?

The cross-sectional view along the dotted line in the layout is also seen in the figure. The n+ active forms a diode with the p-substrate. As long as this diode doesn't forward bias, the connection to the n-well works just like the connection in Fig. 4.10. There is additional junction (depletion) capacitance with this connection (between the n+ and substrate). When the resistor in Fig. 4.10 is fabricated, the active mask won't be perfectly aligned with the n-well. As this example illustrates, it doesn't have to be perfectly aligned for a proper connection to the resistor. ■

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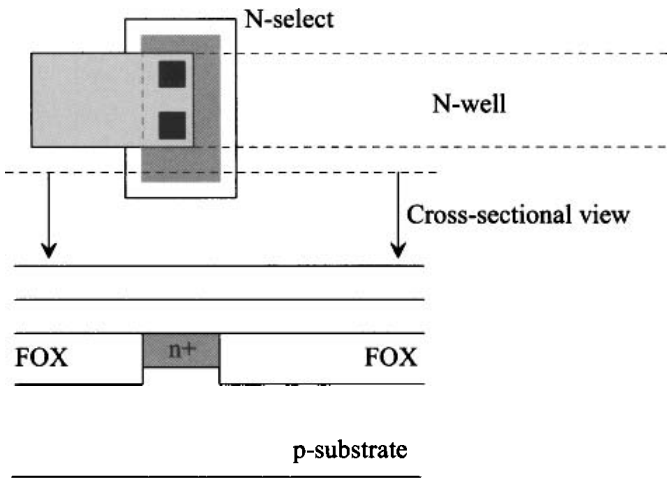

Figure 4.11 Active extending beyond the edges of the n-well.

Layout of an NMOS Device

Figure 4.12 shows the layout, schematic representation, and cross-sectional views of an NMOS device. As seen in Fig. 4.3 and the associated discussion, **poly over active** forms a MOSFET. It's important to remember that the MOSFET is a four-terminal device. In

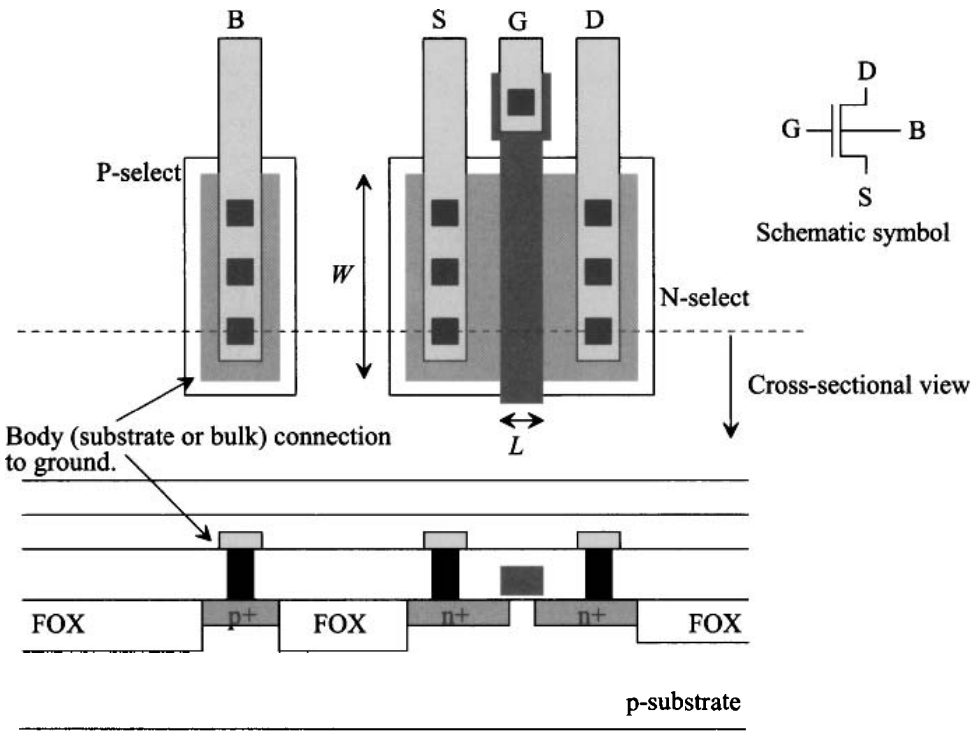

Figure 4.12 Layout and cross-sectional views of an NMOS device.

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Fig. 4.12 we show the bulk connection in the layout and in the schematic. In an n-well process, the bulk is tied to ground so the bulk (or body) connection is normally not shown in the schematic symbol. Also note, again, that the source and drain are interchangeable.

Layout of a PMOS Device

Figure 4.13 shows the layout of a PMOS device. Note how we lay the device out in an n-well. Also seen in the figure is the schematic symbol for the PMOS device. Again, the source and drain of the MOSFET are interchangeable. The n-well is normally tied to the highest potential, *VDD*, in the circuit to keep the parasitic n-well/p-substrate diode from forward biasing.

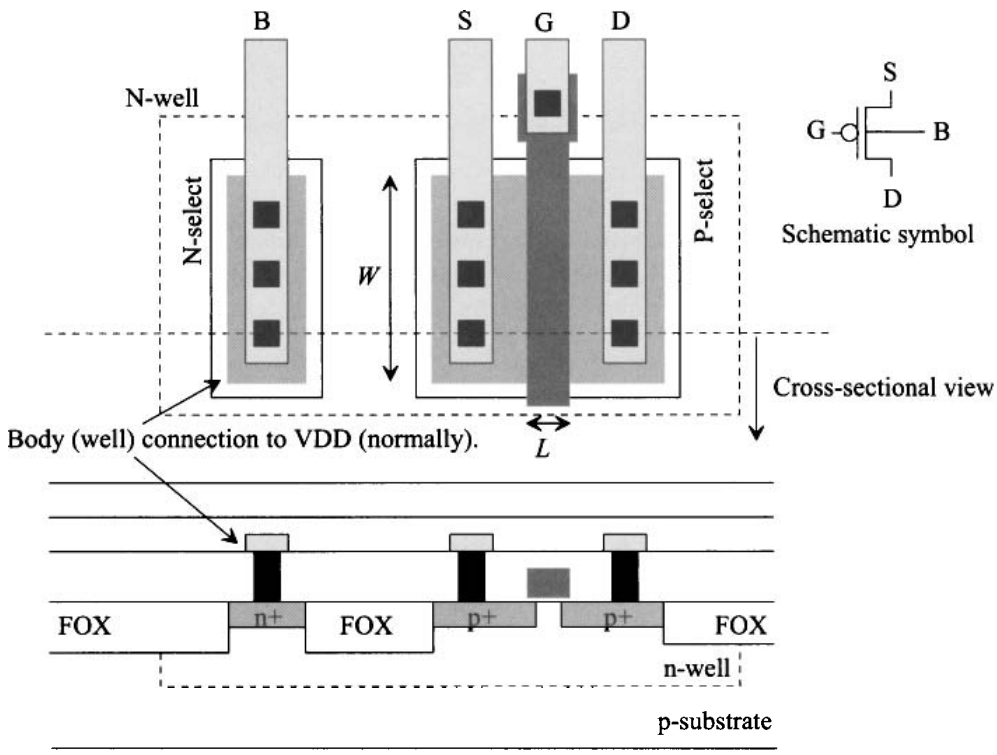

Figure 4.13 Layout and cross-sectional views of an PMOS device.

A Comment Concerning MOSFET Symbols

We'll use the symbols shown in Figs. 4.14a and b to represent NMOS and PMOS devices. Because the bulk terminals aren't drawn in these symbols, it's assumed they are connected to ground (NMOS device) or *VDD* (PMOS device). Notice that the drain and source in this symbol, like the actual layout, are interchangeable. The symbols seen in (c) and (d) are the bipolar-derived symbols where the arrow on the MOSFET's source represents the direction of drain current flow (derived from a bipolar junction transistor symbol). Since, for an integrated circuit MOSFET, the current can flow in either direction through the MOSFET, we'll avoid using the bipolar-derived symbols. Finally, the

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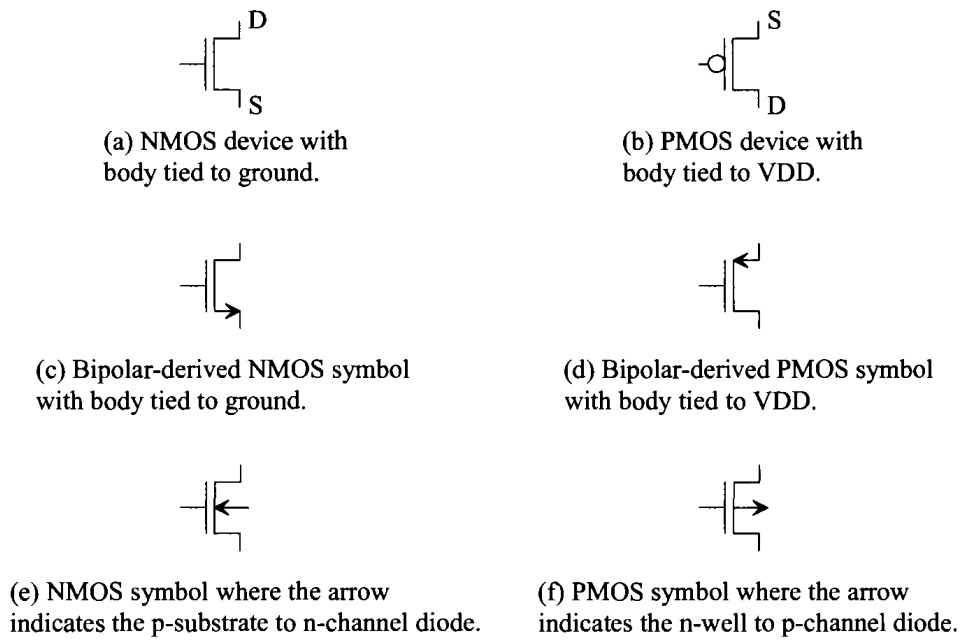

(a) NMOS device with body tied to ground.

(b) PMOS device with body tied to VDD.

(c) Bipolar-derived NMOS symbol with body tied to ground.

(d) Bipolar-derived PMOS symbol with body tied to VDD.

(e) NMOS symbol where the arrow indicates the p-substrate to n-channel diode.

(f) PMOS symbol where the arrow indicates the n-well to p-channel diode.

Figure 4.14 Symbols commonly found in schematics to represent a MOSFET.

symbols seen in (e) and (f) are also used to draw schematics. The arrow in the bulk terminal represents the p-substrate (or p-well) to n-channel diode (NMOS) or the p-channel to n-well diode (PMOS).

Standard Cell Frame

When doing layout, it can be convenient to route power and ground as well as substrate and well connections in a fashion that makes connecting the MOSFETs together simpler. We don't have to worry about the substrate and well connections or the routing of power. Towards this goal, consider the layout seen in Fig. 4.15a. The top half of the layout is an n-well. This n-well is where PMOS devices are placed, as indicated in the figure. The top of the n-well is tied to *VDD* through an n+ implant. In other words, the metal on the top of the layout has n+ underneath it and is routed to the *VDD* pad. Below this layout of the n+ well tie-down, and still in the n-well, is a p-select region. We can draw one or more PMOS devices with active, poly, contacts, and metal1 and place them in this area. The NMOS devices are laid out in the area below this, that is, the area of the n-select layer. Below the NMOS area is the substrate connection, p+, to ground. The metal, at the bottom of the layout, connects the p+ substrate contacts to the ground pad.

Figure 4.15b shows how the standard cell frames can be laid out end-to-end to increase the area available for the layout of the MOSFETs. Notice that the layout area is increased horizontally and not vertically. Standard cell frames have a standard height. Also notice how power, ground, well, and substrate connections are routed through the cell. Finally, note that overlapping layout layers, like the n-well, is fine. It simply indicates a larger layout area (of course the design rule check must be passed).

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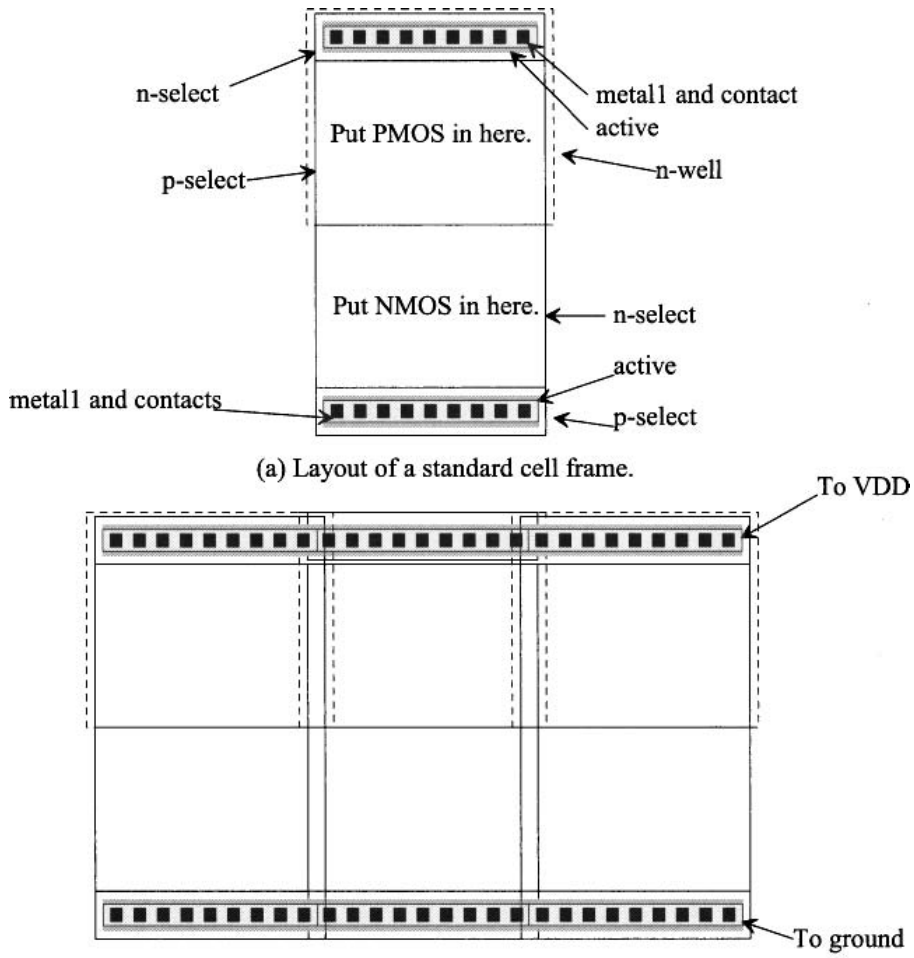

(a) Layout of a standard cell frame.

(b) Increasing the area available for layout of MOSFETs.

Figure 4.15 Layout of standard cell frames.

Design Rules

Figure 4.16 shows the design rules for the active, contact, poly, and select layers. More detailed information on the design rules can be found at MOSIS (http://mosis.org). Seen at the bottom of Fig. 4.16 is an alternative method of laying out an NMOS device. The same active area is used for both the MOSFET formation and the contact to the MOSFET's body (either p-substrate for NMOS or n-well for PMOS). In Fig. 4.12, for example, we laid out the substrate connection a distance away from the source and drain. (The source and drain of the MOSFET are interchangeable.) In the layout seen in Fig. 4.16, we *abut* the n-select directly next to the p-select. This minimizes the layout area. However, as seen in Figs. 4.2g and 4.2h, the n+ and p+ aren't well defined at the boundary between the two materials (the select masks can shift). The p+/n+ can, for all intents and purposes, be thought of as being shorted together. Since the substrate is tied to ground, the layout of the MOSFET in this way (to minimize area) **isn't symmetrical** and the source must also be tied to ground (the source and drain are not interchangeable).

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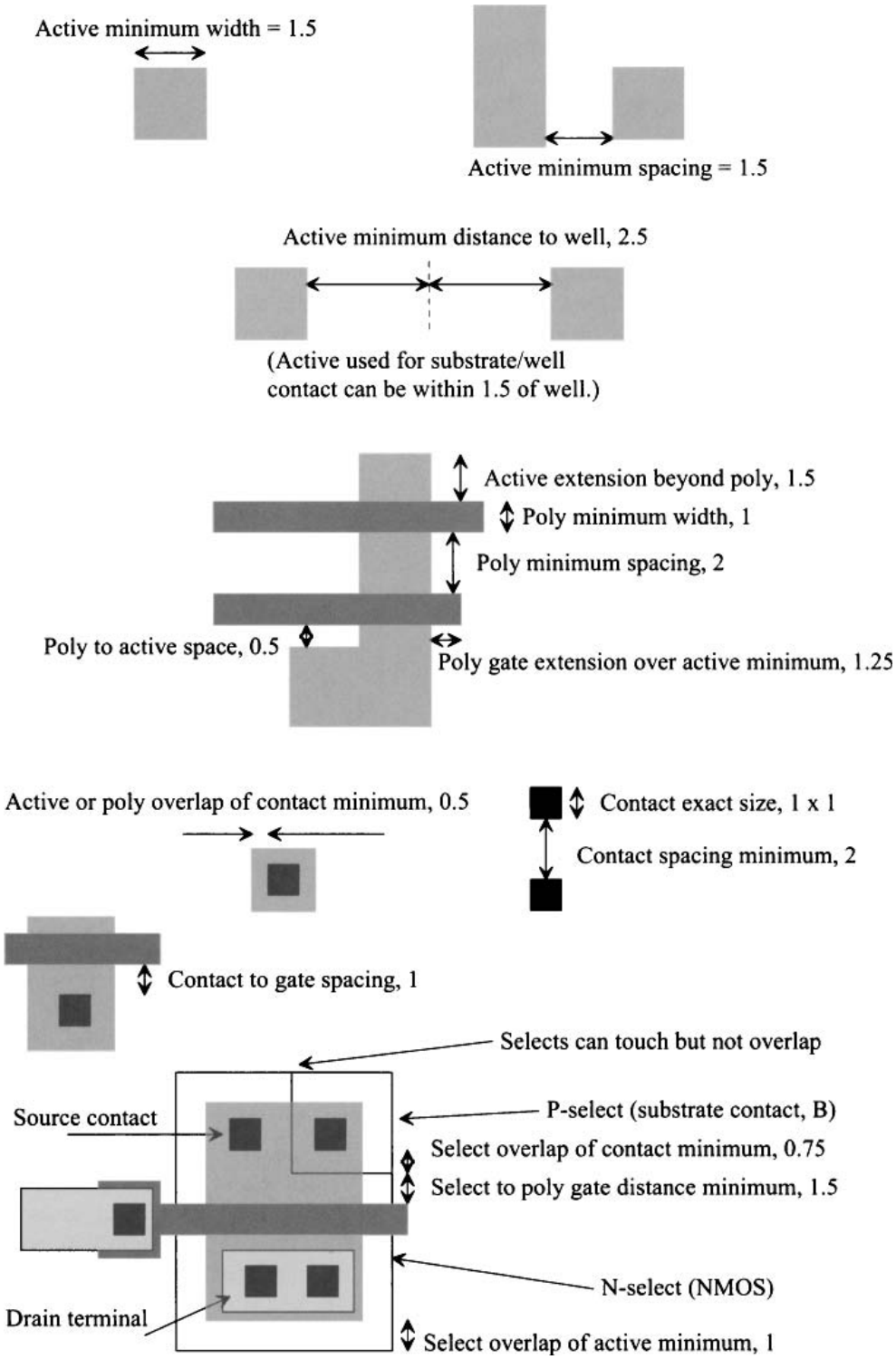

Figure 4.16 Design rules for active, selects, poly, and contacts.

4.3 Electrostatic Discharge (ESD) Protection

A major concern in CMOS technology is the protection of the thin gate oxides, Fig. 4.3b, from electrostatic discharge (ESD). While an in-depth presentation of techniques for preventing ESD damage are outside the scope of this book, here we briefly show how the active layers can be used to form a simple diode-protection structure.

Where does ESD come from? Walking across the floor, for example, causes the buildup of charge on the human body. Touching a conducting object can result in a transfer of charge or a static "shock." If the transfer of this charge (the discharge of the electrostatic charge buildup on the human body) is through the thin gate oxide (GOX) of a MOSFET, it is likely that the GOX will be damaged. While we use the human body as the location of the buildup of electrostatic charge, just about any object can build up charge. To keep from damaging the GOX, consider the circuit seen in Fig. 4.17. Here we connect two diodes to the input pad. If the signals applied to the pad are within ground and *VDD*, neither diode turns on. However, if the voltage on the pad starts to increase above *VDD* + 0.5 V or decrease below – 0.5 V, one of the diodes turns on and provides a low impedance "clamp" to keep the voltage on the GOX from becoming excessive.

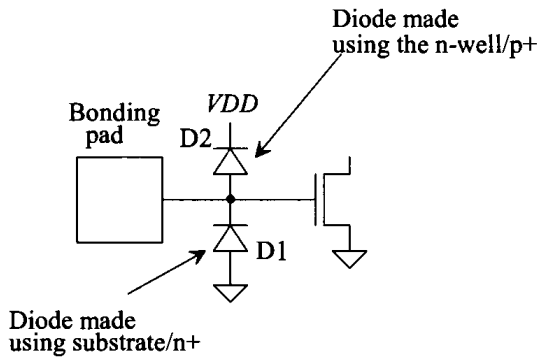

Figure 4.17 Adding diodes to the pads to protect the MOSFET gates from ESD damage.

Layout of the Diodes

Examine the layout seen in Fig. 4.18. This layout shows a conceptual implementation of the diode protection circuitry seen in Fig. 4.17. Diode, D1, is implemented using p-substrate (for the anode) and n+ (for the cathode). The substrate is connected to ground through a metal1 ground bus as seen in the figure. It is desirable to place the substrate connection and n+ as close together as possible to minimize the resistance in series with the diode. Further, it is desirable to increase the size of this n+/p+ diode to both reduce the resistance of the diode and increase its current handling capability. The drawback of increasing the size is the larger capacitive loading on the pad (the depletion capacitances of the diodes). Diode D2 is implemented using p+ in the n-well (for the anode) and the n-well (for the cathode). An n+ implant is needed in the n-well to provide a connection to a wire that is connected to *VDD*. Again, the *VDD* is run through the pad on a bus (the horizontal metal line connected to *VDD* at the bottom of the layout). Again, it's desirable

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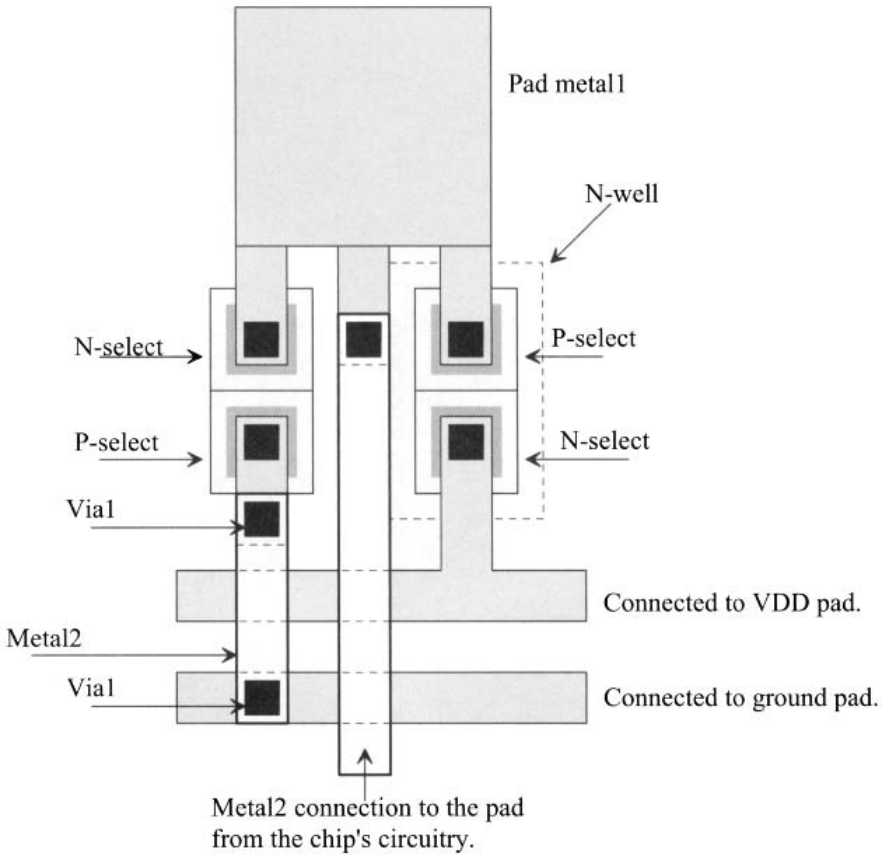

Figure 4.18 Conceptual layout of a pad ESD protection circuit.

to minimize the series resistance between the p+ and n+/n-well. Normally, the ground bus at the bottom of the pad ties the substrate to ground (p+ is implanted under the bus and tied, with contacts, to the metal) and the *VDD* bus is connected to n+/n-well directly beneath it.

Figure 4.19 shows a more realistic view of an I/O (input/output) pad with ESD protection diodes. We've laid the implants directly next to each other to minimize parasitic resistance. We've also staggered the diodes, that is, D1, D2, D1, and D2 to increase their areas. In a real pad layout, the top layer of metal must be used (not metal1 as we've used in the figure, see Figs. 3.20 to 3.23). An example padframe layout is seen in Fig. 4.20. Two of the pads must be connected (separately) to the *VDD* and ground buses.

An important addition to most pads is a buffer to drive the large off-chip capacitances, which are relatively large compared to the on-chip capacitances. We briefly talked about output buffers in Sec. 3.3.2. The circuit design for I/O buffers is covered in Ch. 11 where we talk about inverters. While it's possible to design custom pads for a project, it's generally a better idea to get pads directly from the CMOS vendor where the chips will be fabricated (pads can be downloaded from MOSIS too).

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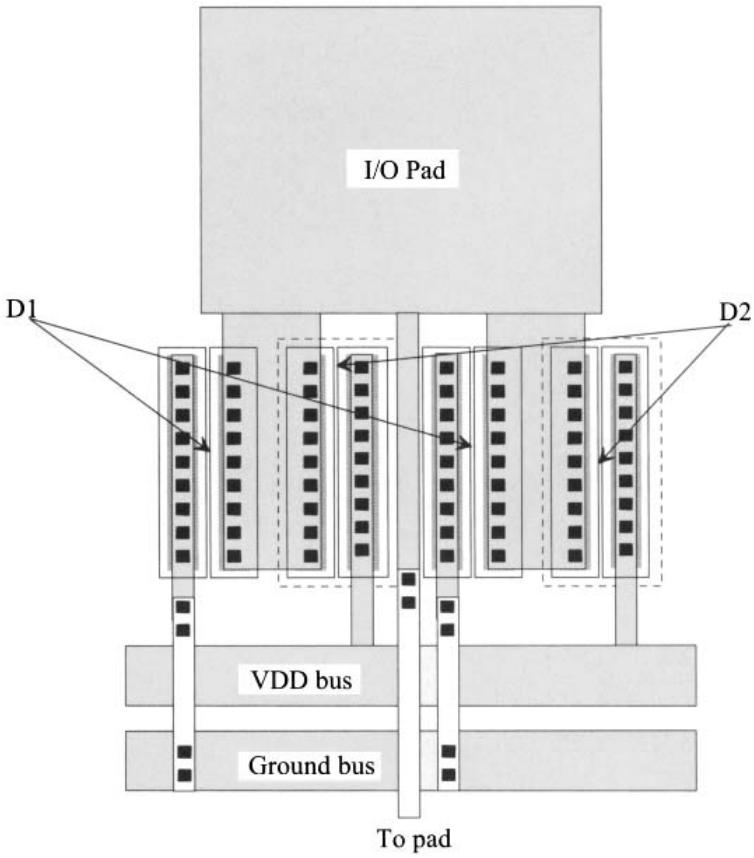

Figure 4.19 More detailed implementation of a pad with ESD protection.

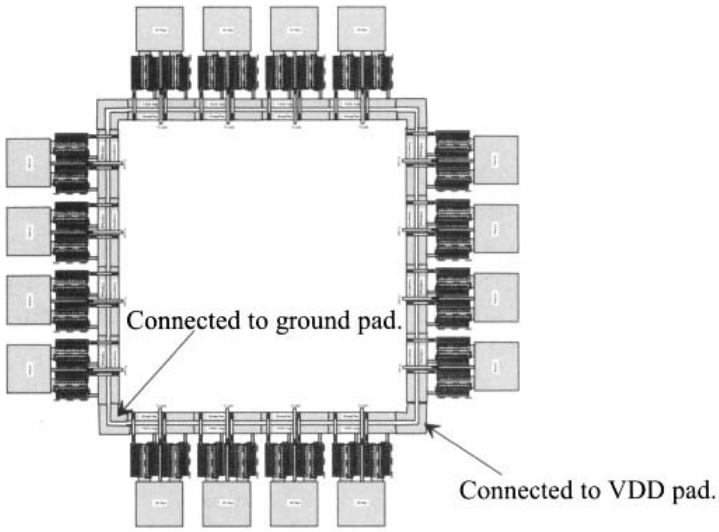

Figure 4.20 Layout of a padframe using pads with ESD diodes.

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ADDITIONAL READING

[1] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*, Second Edition, Cambridge University Press, 2010. ISBN 978-0521832946

[2] A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, John Wiley and Sons Publishers, 2002. ISBN 0-471-49871-8

[3] D. Clein, *CMOS IC Layout: Concepts, Methodologies, and Tools*, Newnes Publishers, 2000. ISBN 0-750-67194-7

[4] S. Dabral and T. J. Maloney, *Basic ESD and I/O Design*, John Wiley and Sons Publishers, 1999. ISBN 0-471-25359-6

PROBLEMS

4.1 Lay out a nominally 200 kΩ resistor with metal1 wire connections. DRC your layout. What would happen if the layout did not include n+ under the contacts? Use the sheet resistances from Table 4.1.

4.2 Sketch the cross-sectional view along the line indicated in Fig. 4.21.

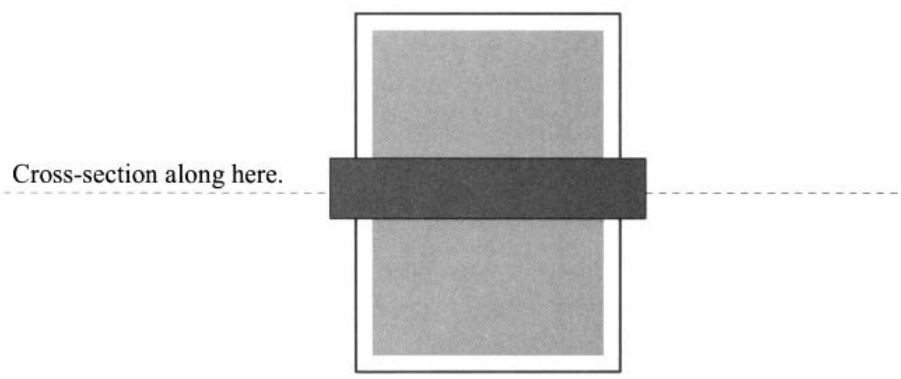

Figure 4.21 Layout used in Problem 4.2.

4.3 Sketch the cross-sectional views across the *VDD* and ground power buses in the standard cell frame of Fig. 4.15.

4.4 Suppose the "bad" layout seen in Fig. Ex4.1 is used to fabricate an NMOS device. Will the poly be doped? Why or why not?

4.5 Why is polysilicon's parasitic capacitance larger than metal1's?

4.6 Lay out an NMOS device with an length of 1 and width of 10. Label all four of the MOSFET terminals.

4.7 Lay out an PMOS device with a length of 1 and width of 20. Label all four of the MOSFET terminals.

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4.8 Using the standard cell frame, lay out 10 (length) by 10 (width) NMOS and PMOS transistors. Sketch several cross-sectional views of the resulting layouts showing all four terminals of the MOSFETs.

4.9 Repeat Ex. 4.2 for a poly wire that is 5 wide.

4.10 Sketch the cross-sectional view at the line indicated in Fig. 4.22.

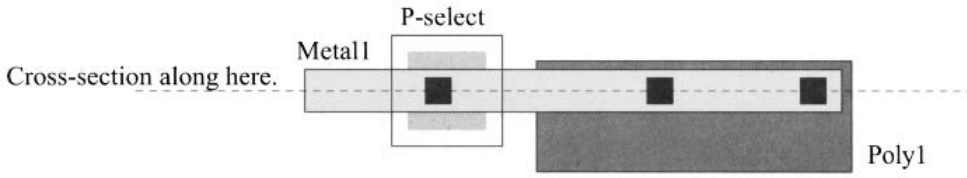

Figure 4.22 Layout used in Problem 4.10.

4.11 Sketch the cross-sectional views across the lines shown in Fig. 4.23.

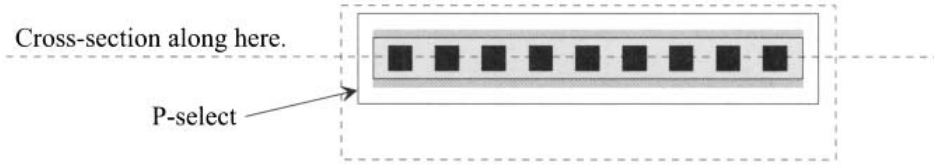

Figure 4.23 Layout used in Problem 4.11.

4.12 The layout of a PMOS device is seen in Fig. 4.24 is incorrect. What is the (fatal) problem?

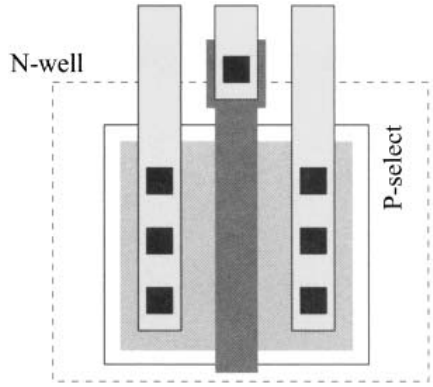

Figure 4.24 Flawed layout of a PMOS device. What is the error?

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About the Author

R. Jacob (Jake) Baker is an engineer, educator, and inventor. He has more than 20 years of engineering experience and holds over 200 granted or pending patents in integrated circuit design. Jake is the author of several circuit design books. For a detailed biography see: http://cmosedu.com/jbaker/jbaker.htm