

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case No.: IPR2024-00911
U.S. Patent No. 10,937,806

**PATENT OWNER'S PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107**

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LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Joint Claim Construction Statement
Ex. 2002	File History of U.S. Pat. No. 10,658,378

LIST OF ABBREVIATIONS

Abbreviation	Term
'806	U.S. Pat. No. 10,937,806
'806FH	File History of U.S. Pat. No. 10,937,806
'378	U.S. Pat. No. 10,658,378
Challenged Claim	Ex. 1001, Claim 10
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00911, Paper 1)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Toyama	U.S. Patent Publication No. 2017/0179026

Pursuant to § 42.107,¹ Patent Owner submits this Preliminary Response to the above-captioned Petition, which should be denied in its entirety based on Petitioner's failure to show a reasonable likelihood of prevailing on any asserted ground as to the Challenged Claim.

I. INTRODUCTION

This proceeding relates to the second of two *inter partes* review petitions filed by Petitioner concerning U.S. Patent No. 10,937,806 ("the '806") and should be denied institution for at least the same reasons identified in Patent Owner's prior Preliminary Response in IPR2024-00791.² Petitioner's second IPR challenges dependent claim 10 ("Challenged Claim") and raises the same grounds based on the Toyama reference for independent claim 8, on which the Challenged Claim depends, as the first IPR. This Preliminary Response presents the same arguments that were

¹ All emphasis and color annotations herein are added, and all statutory and regulatory citations are to either 35 U.S.C. or 37 C.F.R., as the context indicates, unless otherwise stated.

² PO does not oppose Petitioner's claim that it needed a second petition (Paper 3), but disputes Petitioner's assertions that PO's identification of asserted claims was belated, that PO's infringement allegations are without merit and could not have been credibly alleged, and that PO has asserted a large number of '806 claims.

raised in the first proceeding for independent claim 8 as well as additional arguments that address the Challenged Claim specifically.

As set forth in Patent Owner's earlier Preliminary Response, Petitioner's previously filed petition in IPR2024-00791 (Pap. 1) challenging claims 8-9 and 11-12 should be denied institution. IPR2024-00791, Pap. 10. The Challenged Claim in this IPR (claim 10) depends from the previously challenged independent claim 8, and Petitioner relies on the same Toyama grounds again here. Pet. 1. Accordingly, Patent Owner presents the same arguments here as to the limitations of claim 8, which are required by dependent claim 10. In addition, Patent Owner presents additional arguments as to the further limitations recited by dependent claim 10. The previously-filed Preliminary Response in IPR2024-00791 did not address dependent claim 10 because Petitioner had not challenged dependent claim 10. Thus, any decision by the Board to institute IPR2024-00791 does not mean that a reasonable likelihood of success also exists in this proceeding.

The '806 is directed to a novel three-dimensional (3D) memory device having through array contacts and methods related to manufacturing such a device. As memory cells are scaled down and the density of memory cells increases, it becomes challenging to collect and route signals to the peripheral circuitry efficiently. The '806 provides a solution by forming through array contacts (TACs) in a dedicated region where they provide vertical interconnects to the peripheral

devices. '806, 1:24-36, 2:24-26, 5:52-56, 11:8-14, 19:59-64. By forming this TAC region within a dedicated dielectric structure, the '806 simplifies the fabrication process, improving yield and lowering costs. The '806 also improves performance by locating the TAC region between regions of memory channels. '806, Figs. 1A-B, 2, Claim 8.

The '806 introduced a 3D memory device in which TACs “extend vertically through” the “dielectric structure,” which hosts a “TAC region” that is between “first and second channel regions” of the memory device. '806, Abstract, 10:62-64, Figs. 1A-B, 2, Claim 8. The claimed invention recites “a dielectric structure extending vertically through the alternating conductor/dielectric layer stack,” “first and second channel regions comprising first and second pluralities of channel structures, respectively,” and “a through array contact (TAC) region formed between the first and second channel regions.” See '806, Claim 8. As a result, the claimed invention avoids the issues arising from forming TACs through alternating dielectric/conductor stacks and “simplif[ies] the fabrication process and reduce[s] the fabrication cost.” '806, 18:41-46. The '806 also includes an etch stop plug between channels and the contacts above, which “prevents etching of dielectrics in channel structure 216, such as SiO₂ and SiN, during subsequent etch operations.” '806, 9:49-52, Claim 10.

As an initial matter, as set forth in Patent Owner’s earlier Preliminary Response, the Board should exercise its discretion to deny institution under § 325(d) because the same art (Toyama) was expressly considered during prosecution and Petitioner has not shown Examiner error. IPR2024-00791, Pap. 10.

In addition, institution should be denied because the Petition fails to establish a reasonable likelihood of prevailing with respect to the Challenged Claim. Petitioner does not assert that any of the cited references anticipates the Challenged Claim. Instead, Petitioner argues obviousness ignoring binding Federal Circuit law and applying faulty analysis that attempts to mold the prior art into claim 10 based solely on hindsight.

Petitioner’s arguments under Ground 1, which rely on Toyama’s “second modification of the fourth exemplary structure” (“Second Modification”), directly contradict binding Federal Circuit precedent. Claim 10 requires “a **plurality** of through array contacts (TACs) extending vertically through **the dielectric structure**,” but Petitioners arguments instead rely on multiple dielectric structures—each with its own TAC. Consistent with the Federal Circuit’s recent decision in *Finjan LLC v. SonicWall, Inc.*, multiple TACs must extend through the same dielectric structure—not one or more different structures. 84 F.4th 963, 974-975 (Fed. Cir. 2023). Petitioner also fails to present a mapping that includes an etch stop plug between “each” local contact and each channel structure. Petitioner’s mapping does not even

discuss one of structures that it mapped to the claimed local contacts of independent claim 8, and in fact there is no such alleged etch stop plug present in that location.

Petitioner's Ground 2 relies on Toyama's "First Exemplary Structure," which lacks the claimed TAC region between two channel regions because the alleged TAC region is placed on one side of the device. Realizing the deficiencies of Toyama's First Exemplary Structure, Petitioner proposes putting two devices next to each other in a repeating pattern but forgets that such a modification would eliminate the peripheral circuitry that is in that location according to Toyama. In addition, for similar reasons as for Ground 1, Petitioner fails to present a mapping that includes an etch stop plug between "each" local contact and each channel structure.

Finally, Ground 3 relies on a modification of Toyama's Second Modification based on Toyama's First Exemplary Structure's unitary dielectric fill material. Petitioner's proposed modification replaces a path used for current flow with a large insulator (a block of dielectric fill material). No POSITA would have made this proposed modification. Moreover, the modification proposed by Petitioner fails to show the etch stop plug limitation for the same reasons as for Ground 1.

For each of its grounds, Petitioner fails to establish how these hindsight-based modifications would have been obvious to a POSITA. Because the asserted

prior art fails to disclose or render obvious at least one limitation of each of the Challenged Claim, the Board should deny institution.

II. THE CLAIMED INVENTION OF THE '806 PATENT

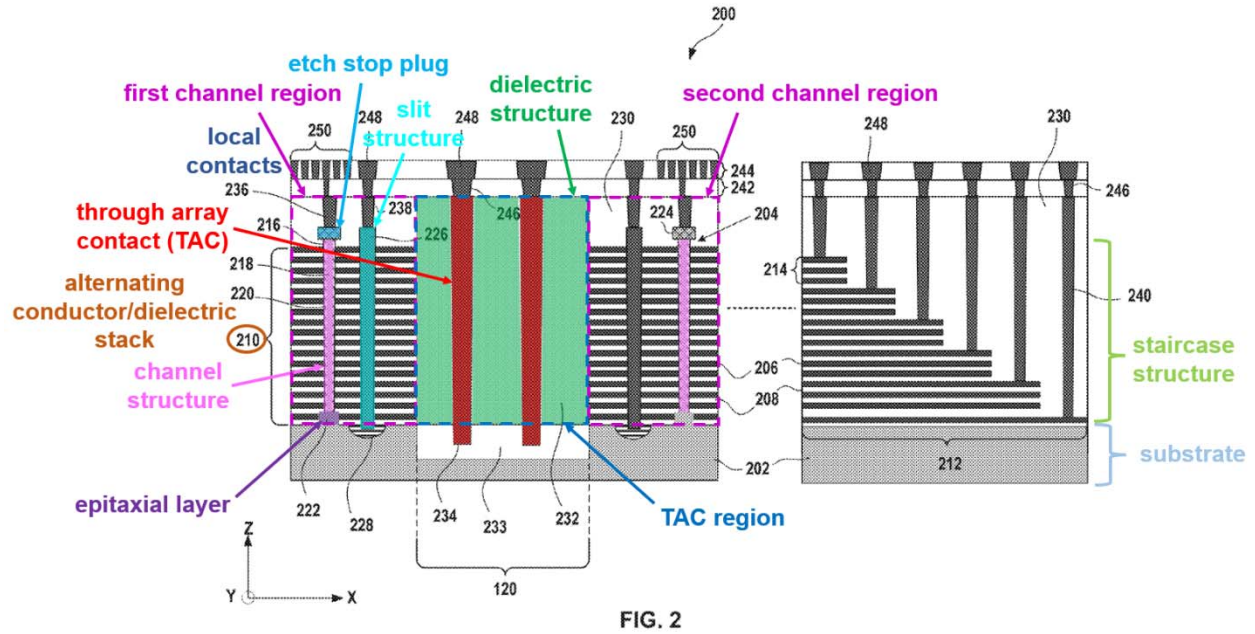
The claimed invention of the '806 is directed to a “three-dimensional (3D) memory device” and related methods that addresses issues arising from the fabrication techniques known in the prior art and, as a result, “simplif[ies] the fabrication process and reduce[s] the fabrication cost.” '806, Abstract, 18:41-46.

Specifically, the '806 is directed to an improved 3D memory device and methods for forming such a device in which “through array contacts (TACs)” “extend vertically through” the “dielectric structure,” which hosts a “TAC region.” '806, Abstract, 6:17-20, 10:61-63, 21:20-28. 3D memory devices in the prior art at the earliest claimed priority date of the '806 involved through array vias that form connections between various components of the device in order to reduce the size and increase density. '806, 1:24-36. These vias were placed within the alternating dielectric and conductive layers, which required a complex etching process and “increase[d] the fabrication cost.” '806, 10:61-11:4.

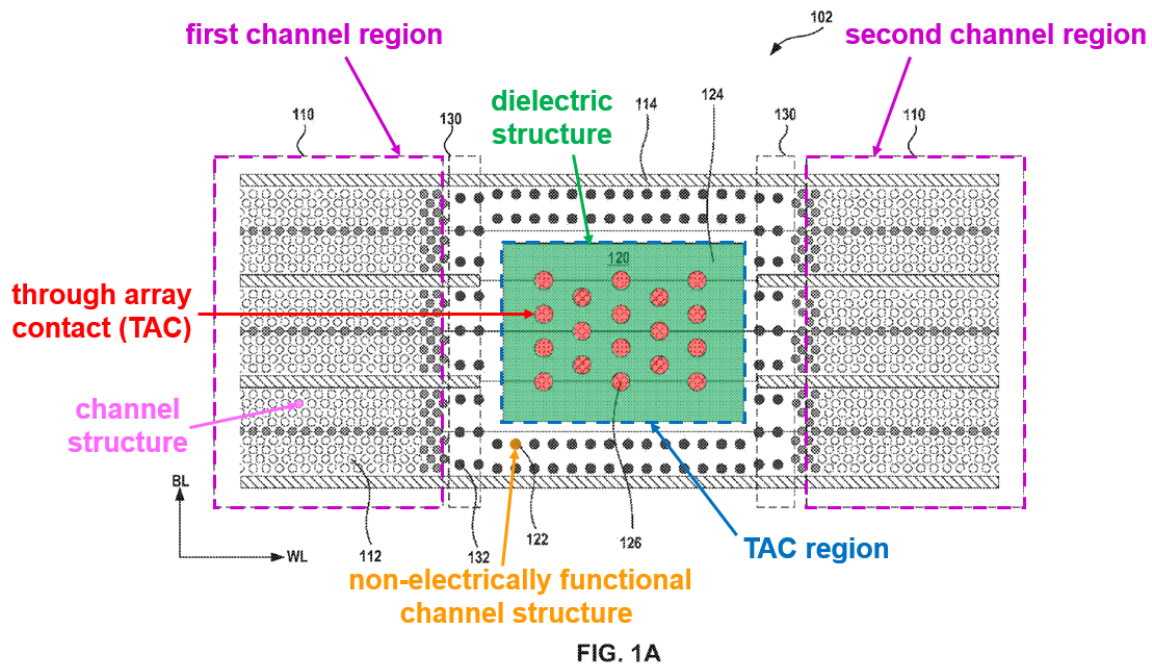
The novel device and methods the '806 teaches and recites in the claims is characterized by **TACs** that “extend vertically through” the “**dielectric structure**” of a “**TAC region**” that can be between “**first and second channel regions**” comprising “**channel structures**.” '806, Abstract, 6:17-20, 10:61-63, 21:20-28,

Claim 8. This novel configuration of elements allows for easier and less costly manufacture of 3D memory devices and achieves shorter interconnect routing. '806, 5:61-65, 11:8-10, 18:32-38, 20:33-41.

A representative embodiment of the '806's memory device includes: (1) **“alternating conductor/dielectric layer stack 210”** ('806, 8:23-31); (2) **“dielectric structure 232”** ('806, 10:23-34); (3) **“channel structures 216”** and **“slit structures 226”** extending vertically through **“alternating conductor/dielectric layer stack 210”** ('806, 9:7-12, 10:6-11); (4) **“staircase structure 212”** ('806, 8:54-61); (5) **“local contacts”** on **“channel structures 216”** and **“slit structures 226”** ('806, 11:28-30); (6) **“TACs 234”** extending vertically through **“dielectric structure 232”** ('806, 10:62-64, 20:49-52); (7) **“first and second channel regions”** and a **“TAC region 120”** between them ('806, 6:4-11, Fig. 2, Claim 8); (8) **“non-electrically functional channel structures 122”** surrounding the **“TAC region 120”** and between **“first and second channel regions”** ('806, 6:22-29, Fig. 1A, Claim 8); (9) a **“substrate 202”** ('806, 7:13-35, Fig. 2); (10) an **“etch stop plug 224”** between each **“local contact”** and each **“channel structure 216”** ('806, 9:36-53, Fig.2); and (11) an **“epitaxial layer 222”** between **“substrate 202”** and **“channel structures 216”** ('806, 9:36-40, Fig.2). Vertical and horizontal cross-section views of the memory device are below.



'806, Fig. 2 (annotated).



'806, Fig. 1A (annotated).

The Challenged Claim (claim 10) depends from claim 8, and is directed to aspects of the above-described invention:

[8.pre] A three-dimensional (3D) memory device, comprising:

[8.a] an alternating conductor/dielectric layer stack;

[8.b] a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;

[8.c] first and second channel regions comprising first and second pluralities of channel structures, respectively;

[8.d] slit structures extending vertically through the alternating conductor/dielectric layer stack;

[8.e] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[8.f] local contacts disposed on the first and second channel structures and the slit structures;

[8.g] a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and

[8.h] a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.

[10.pre] The 3D memory device of claim 8, further comprising:

[10.a] a substrate;

[10.b] an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and

[10.c] an epitaxial layer disposed between the substrate and the first or second channel structures.

III. FILE HISTORY

The claims of the '806 remain patentable over the prior art for at least the same reason identified during prosecution. As discussed further below in § VII, the prior art does not disclose or render obvious, *inter alia*, the '806 claim elements “a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure.” Claims directed to these elements were allowed after thorough prosecution and consideration of numerous prior art references.

The '806 was filed on May 5, 2020, as a continuation of application no. 16/047,182, filed on July 27, 2018, which was issued as U.S. Patent No. 10,658,378 (“the '378”). The application included 3 independent claims (pending claims 1, 9, and 15) and 17 dependent claims (pending claims 2-8 which depend from pending claim 1, pending claims 10-14 which depend from pending claim 9, and pending

claims 16-20 which depend from pending claim 15). Ex. 1002, 53-55 (05/05/2020 Claims).

In a non-final office action, the Examiner rejected pending claims 1-16 and 18-20 under 35 U.S.C. § 103 as being allegedly obvious over U.S. Patent No. 9,659,956 (“Pachamuthu”) in view of U.S. Patent Publication No. 2017/0186758 (“Lee”), and rejected pending claim 17 under 35 U.S.C. § 103 as being allegedly obvious over these two references in further view of U.S. Patent Publication No. 2017/0365613 (“Gunji-Yoneoka”). Ex. 1002, 104-112 (06/23/2020 Office Action).

In a response, Applicant amended pending independent claims 1, 9, and 15 “[w]ithout acquiescing to the propriety of the rejection” to “recite features that further distinguish itself from the applied references.” Ex. 1002, 128-137 (10/21/2020 Amendment and Reply). Applicant also canceled pending dependent claims 3, 11, and 17. *Id.* Having placed the independent claims in allowable form, Applicant requested that their respective dependent claims also be allowed. *Id.* Applicant further added three new claims that depend from the three pending independent claims. Ex. 1002, 128-137 (10/21/2020 Amendment and Reply). The Examiner subsequently allowed all pending claims. Ex. 1002, 147-154 (12/16/2020 Notice of Allowance). The ’806 issued on March 2, 2021 with twenty claims, including the renumbered independent claims 1, 8, and 13. Ex. 1002, 169 (02/10/2021 Issue Notification).

With the original filing of the '806, Applicant filed an information disclosure statement (IDS) that notified the Examiner of U.S. Patent Publication No. 2017/0179026 ("Toyama"). Ex. 1002, 81 (05/05/2020 Information Disclosure Statement). The Examiner considered Toyama and explicitly cited it as a "reference[] considered." Ex. 1002, 124 (06/23/2020 List of References Cited by Applicant and Considered by Examiner). In addition, the '806 and its parent, the '378, share the same Examiner (Calvin Y. Choi), who was presented Toyama during the prosecution of the '378 in an IDS with Toyama alone (Ex. 2002, 555 (12/03/2019 Information Disclosure Statement)) and considered it (Ex. 2002, 593 (01/13/2020 List of References Cited by Applicant and Considered by Examiner)). Petitioner's assertion that "Patent Owner only gave Examiner a haystack" is belied by the fact that Applicant submitted an IDS solely to cite Toyama during the application of the parent, which was then explicitly considered by the Examiner, who was already familiar with Toyama even before the '806 was filed. Petitioner is aware of the prosecution history of the '378 (*see generally* IPR2024-00788, Pet. 9-15) and yet omitted these relevant facts.

Moreover, the '806 was issued with only nineteen references (twelve U.S. patent documents and seven foreign patent documents)—one of which is Toyama. '806, (56). Thus, the Examiner duly considered Toyama twice—once for

the '378 and again when subsequently examining the '806 at issue here—but found it lacking.

IV. CLAIM CONSTRUCTION

The Board construes claim terms “using the same claim construction standard that would be used to construe the claim in a civil action.” § 42.100(b). Under this standard, claim terms are “generally given their ordinary and customary meaning” to a person of ordinary skill in the art. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). A POSITA ascertains the meaning of the claims based on the claim language, specification, prosecution history, and relevant extrinsic evidence, although the claims and patent specification are the primary sources for construing claims. *Id.* at 1314-16.

The Petition asserts that “the terms of the 806 Patent’s claims do not require further construction and should receive their plain and ordinary meaning.” Pet. 27. Patent Owner reserves the right to modify its proposed construction and to raise further claim construction issues if the Board institutes IPR, and to raise claim construction issues in the underlying district court proceedings.

The parties recently exchanged proposed claim constructions and filed a joint claim construction statement in the parallel district court proceeding. Ex. 2001 (“Joint Claim Construction and Prehearing Statement”). The claim construction disputes in district court do not impact the issues raised in this Preliminary Response.

V. BACKGROUND OF THE ASSERTED PRIOR ART

A. U.S. Patent Publication No. 2017/0179026 (“Toyama”) (Ex. 1005)

Petitioner does not contend that Toyama anticipates the Challenged Claim, and instead argues only that it renders obvious the Challenged Claim in view of the knowledge of a POSITA. Pet. 7, 27-122.

Toyama teaches a 3D NAND memory device with four exemplary structures and their modifications. Ex. 1005, [0004]. Only two of these exemplary structures are relied on by Petitioner: (1) Toyama’s “first exemplary structure,” illustrated in Figures 1A-B to 17A-F, and (2) Toyama’s “second modification of the fourth exemplary structure,” illustrated in Figures 44A-B to 49. Pet. 15, 25.

Toyama’s first exemplary structure includes, among other elements:

“**semiconductor substrate 9**” (Ex. 1005, [0163]); “**planar semiconductor material layer 10**” (Ex. 1005, [0170]); “**alternating stack (132, 146, 232, 246)**” (Ex. 1005, [0232]); “**channels**” (Ex. 1005, [0211]); “**laterally-elongated contact via structures 76**” (Ex. 1005, [0236]); “**drain contact via structures 88**” (Ex. 1005, [0241]); “**source connection via structures 91**” (Ex. 1005, [0250]); “**dielectric fill material portion 430**” (Ex. 1005, [0216]); and “**through-memory-level via structures 488**” (Ex. 1005, [0244]). A cross-section view of Toyama’s first exemplary structure is below.

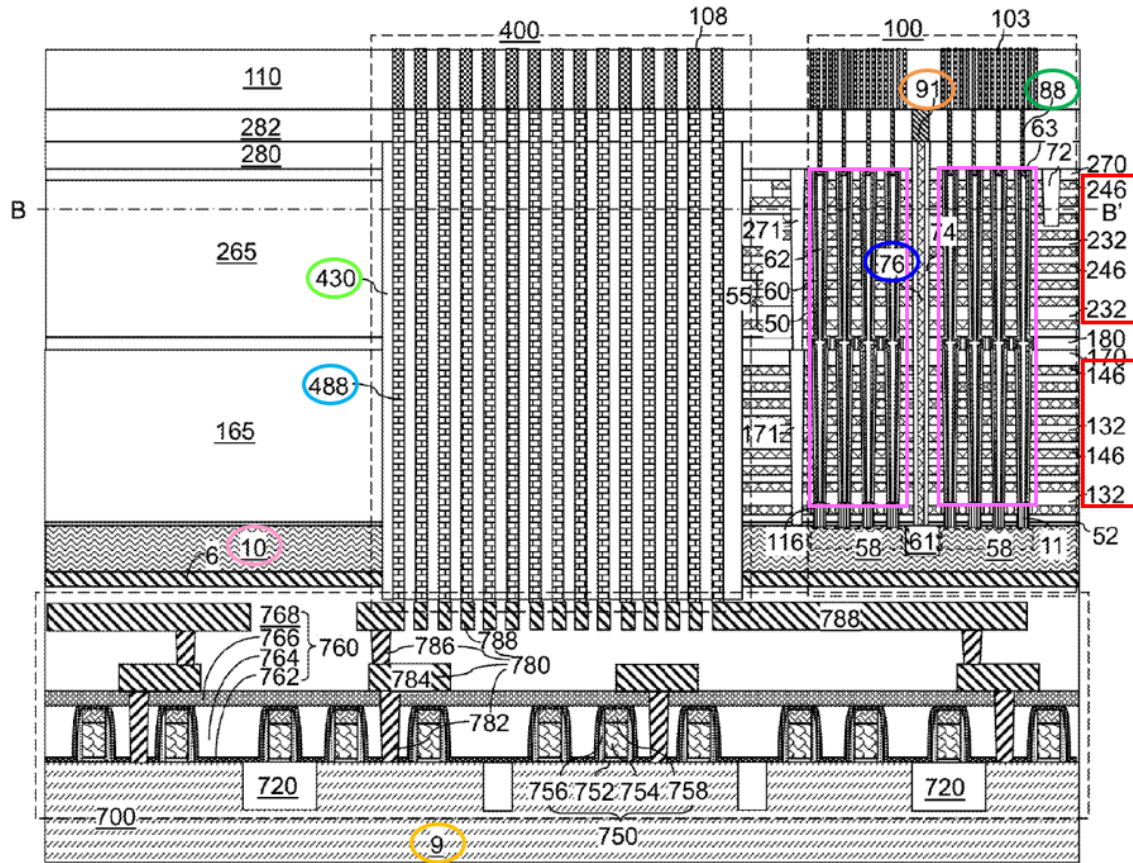


FIG. 17A

Ex. 1005, Fig. 17A (annotated).

In Toyama’s first exemplary structure, **dielectric fill material portion 430** hosts **through-memory-level via structures 488** to form vertical interconnects; however, Toyama’s first exemplary structure lacks two regions with channel structures on opposite sides. Instead, **dielectric fill material portion 430** is formed in a staircase region and therefore has **channels** on one side only. As Toyama explains, the through-memory-level via region 400 (in which the through-memory-level via structures 488 are formed) “is located on a *lengthwise end* of the

second block B2 and between a staircase region of the first block B1 and a staircase region of the third block B3.” Ex. 1005, [0252], Fig. 17B.

Toyama’s second modification of the fourth exemplary structure includes, among other elements: “**semiconductor substrate 9**” (Ex. 1005, [0163]); “**planar semiconductor material layer 10**” (Ex. 1005, [0170]); “**alternating stack (132, 146, 232, 246)**” (Ex. 1005, [0232]); “**channels**” (Ex. 1005, [0211]); “**laterally-elongated contact via structures 76**” (Ex. 1005, [0236]); “**drain contact via structures 88**” (Ex. 1005, [0241]); “**insulating liners 674**” (Ex. 1005, [0340]); and “**through-memory-level via structure 676**” (Ex. 1005, [0341]). A cross-section view of Toyama’s second modification of the fourth exemplary structure is below.

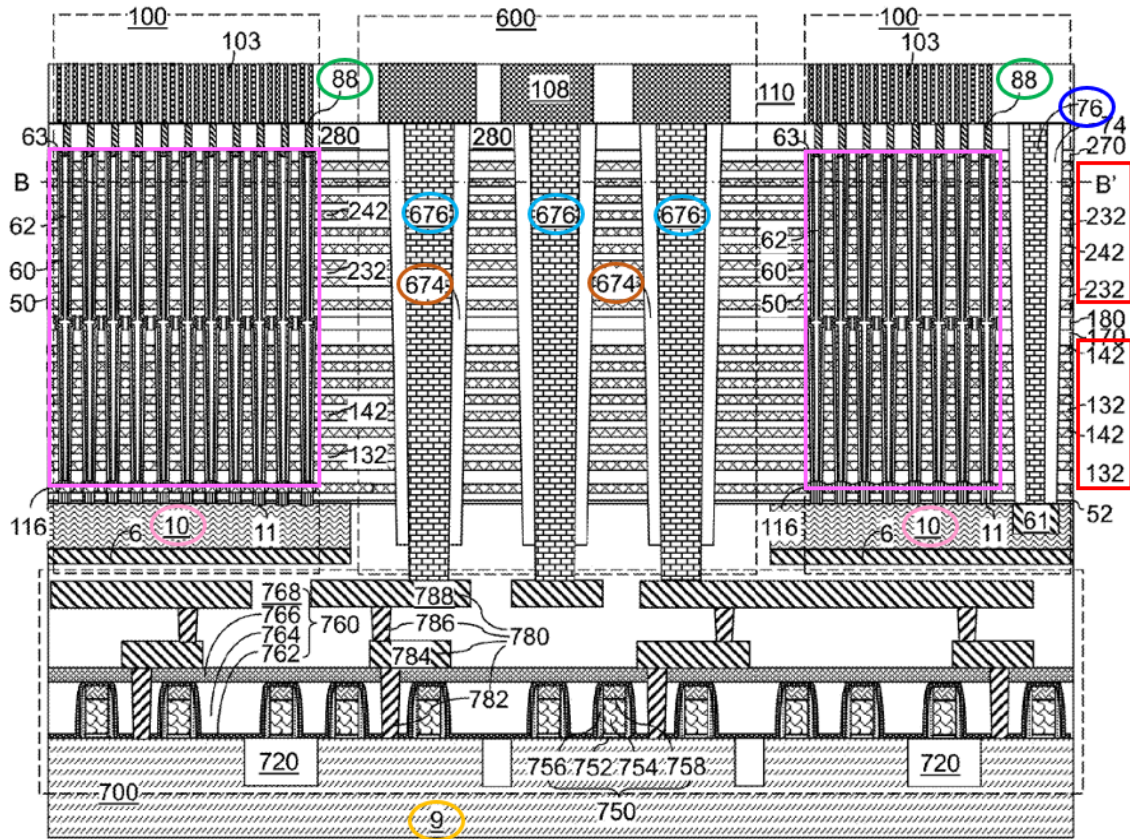


FIG. 49

Ex. 1005, Fig. 49 (annotated).³

³ Petitioner states: “In a clear typographical error, Fig. 49 (as well as Figs. 47A and 48A) labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142 and 242 are ‘sacrificial material layers’ which, in a previous process step, were removed and replaced with ‘electrically conductive layers (146, 246).’ Toyama, [0337], [0340].” Pet. 28. Patent Owner does not challenge this assertion for purposes of the POPR.

In Toyama's second modification of the fourth exemplary structure, **through-memory-level via structures 676** are not formed through a dielectric structure; instead, they are formed through **alternating stack (132, 146, 232, 246)**, where layers 146 and 246 are conductive, and as a result, they require separate **insulating liners 674** around each individual **through-memory-level via structure 676**.

VI. THE BOARD SHOULD EXERCISE ITS DISCRETION UNDER § 325(D) TO DENY INSTITUTION

The Board has statutory discretion to deny *inter partes* review when the petition relies on the same or substantially the same prior art or arguments that were previously presented to the Office. *See* 35 U.S.C. § 325(d). The two-part framework established in *Advanced Bionics* considers (A) whether the same or substantially the same art was previously presented to the Office or whether the same or substantially the same arguments were previously presented to the Office, and (B) if either condition is satisfied in the first part, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of the challenged claim. *See Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Pap. 6 at *8-9 (precedential) (“If a condition in the first part of the framework is satisfied and the petitioner fails to make a showing of material error, the Director generally will exercise discretion not to institute *inter partes* review.”). The PTAB has used the six factors set forth in *Becton, Dickinson*

to evaluate the two-part *Advanced Bionics* framework. *Advanced Bionics*, IPR2019-01469, Pap. 6 at 7, n.8 citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Pap. 8 (Dec. 15, 2017) (precedential as to §III.C.5, first paragraph). *Becton, Dickson* factors (a) “the similarities and material differences between the asserted art and the prior art involved during examination,” (b) “the cumulative nature of the asserted art and the prior art evaluated during examination,” and (d) “the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art” relate to the first part of the *Advanced Bionics* framework (whether the art or arguments presented in the Petition are the same or substantially the same as those previously presented to the Office). *Becton, Dickson* factors (c) “the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection,” (e) “whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art,” and (f) “the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments” relate to the second part of the framework (whether the petitioner has demonstrated a material error by the Office in its prior consideration of the prior art or arguments).

Applying the *Advanced Bionics* framework to this proceeding, the Board

should exercise its discretion and deny institution because, as discussed below, (A) Petitioner relies on the same art (Toyama) that was previously presented to the Office, and (B) Petitioner fails to demonstrate that the Office erred in a manner material to the patentability of the Challenged Claim.

A. All Grounds Rely on the Same Prior Art That Was Previously Presented to the Office

In all grounds, Petitioner relies solely on Toyama. As discussed in § III, Toyama was presented to the Examiner in an information disclosure statement (IDS). Ex. 1002, 81 (05/05/2020 Information Disclosure Statement). The Examiner considered Toyama and explicitly signed the IDS to indicate that Toyama was a “reference[] considered.” Ex. 1002, 124 (06/23/2020 List of References Cited by Applicant and Considered by Examiner). In addition, the ’806 and its parent, the ’378, share the same Examiner, who was also previously presented Toyama during the prosecution of the parent ’378 in an IDS identifying Toyama alone (Ex. 2002, 555 (12/19/2019 Information Disclosure Statement)), and the Examiner signed that IDS as well to indicate that Toyama was considered (Ex. 2002, 593 (01/13/2020 List of References Cited by Applicant and Considered by Examiner)). Therefore, the reference was previously presented to the Office for purposes of § 325(d). *See, e.g., Advanced Bionics*, IPR2019-01469, Pap. 6 at 7-8 (precedential) (“Previously presented art includes ... art provided to the Office by an applicant, such as on an Information Disclosure Statement (IDS),

in the prosecution history of the challenged patent.”). Petitioner argues that the record is silent as to what, if any, substantive consideration the Examiner gave Toyama (Pet. 10), but as explained above, the Examiner expressly confirmed that Toyama was considered, and this is not a situation where the reference was presented along with hundreds of other references. The ’806 issued with only nineteen references, one of which is Toyama (’806, (56)), and again, previously during prosecution of the parent ’378, Toyama was submitted by itself in an IDS to the same Examiner.

B. The Office Did Not Err in a Manner Material to Patentability of the Challenged Claim

Petitioner has not shown that the Examiner erred in its consideration of Toyama during prosecution, and its arguments are contradicted by the record.

As an initial matter, Petitioner’s substantive arguments for Examiner error are focused on ***only*** elements that were incorporated into the pending independent claim 9 by Applicant in the October 21, 2020, Reply to Office Action. Pet. 11-13; Ex. 1002, 130. But those particular elements were incorporated into the pending independent claim 9 (issued as independent claim 8) following rejections based on different references than Toyama. Thus, Petitioner has no basis for limiting its § 325(d) analysis of Toyama to those particular elements. Indeed, in its incomplete analysis, Petitioner is entirely silent as to the last phrase (emphasized) of limitation [8.g] “...a plurality of through array contacts (TACs) ***extending vertically through***

the dielectric structure” (*see* Pet. 12)—it is this element of independent claim 8 that Petitioner’s cited embodiment plainly fails to teach (*see* Pet. 13). In addition, Petitioner’s § 325(d) analysis does not address the additional limitations of dependent claim 10 (the Challenged Claim). As explained below and in § VII, there are multiple elements that are missing from Toyama, which Petitioner fails to discuss in its § 325(d) analysis. Thus, Petitioner has not met its burden of showing Examiner error.

Indeed, the Examiner did not err as Toyama discloses the fabrication technique that the ’806 criticizes and improves upon. For example, a key feature of the ’806 missing from Toyama is that the TACs are formed in a dedicated TAC region hosted by a dielectric structure between two channel regions. This configuration results in a less complex and less costly fabrication technique. ’806, 5:41-45, 10:64-11:4, 18:32-46, 20:13-20. Further, the ’806 emphasizes the importance of “shorten[ing] interconnect routing” in the placement of the TACs (’806, 11:8-10), which is further achieved by placing the TAC region between two channel regions. ’806, 6:17-20, Fig. 2.

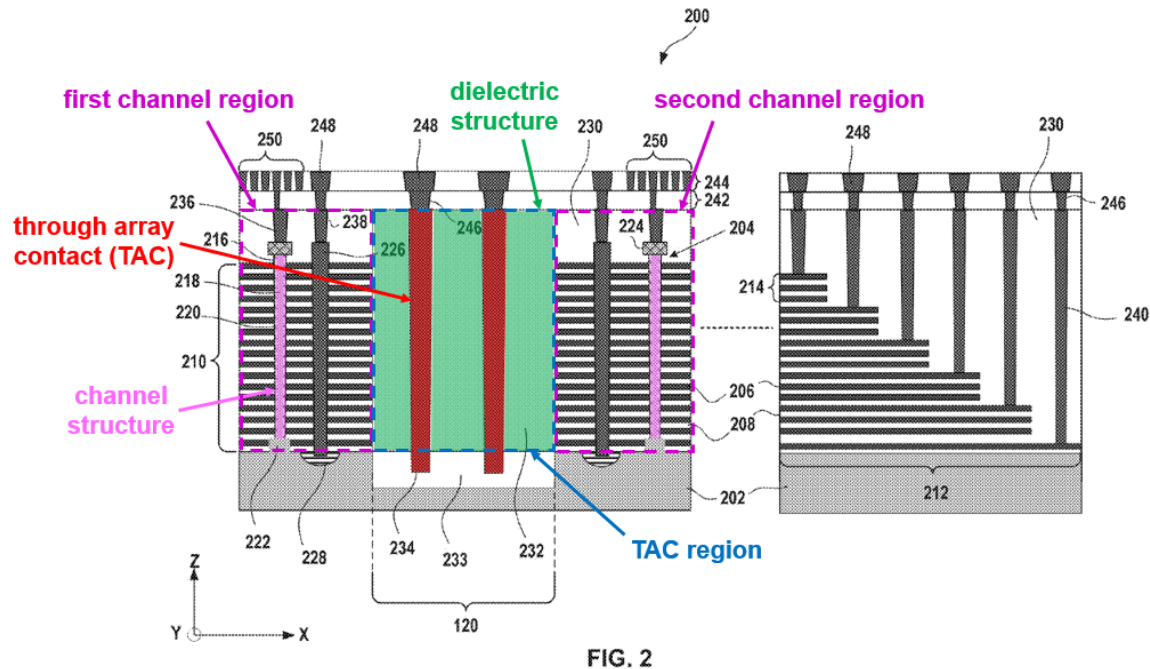


FIG. 2

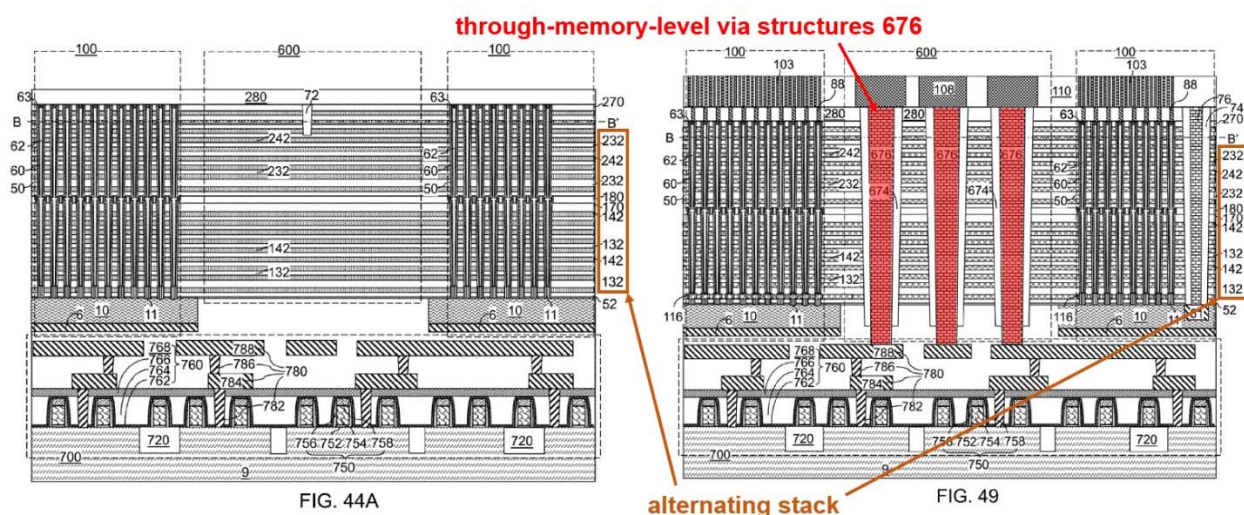
'806, Fig. 2 (annotated).

The prior art at the time of the priority date of the '806 formed vertical vias (such as TACs) through the alternating dielectric and conductive layers without first forming a dielectric structure, thus “increase[ing] the fabrication cost.” '806, 10:64-11:4, 18:32-46. The '806 simplifies the fabrication process of TACs by forming them in a dedicated dielectric structure and avoiding the need to etch through the multiple dielectric/conductor layers stack to form the openings for TACs. '806, 10:64-11:4, 18:32-46. As a result, the dielectric structure can be formed with ease using various patterning techniques, and the TACs can be formed via a significantly simplified process. '806, 18:32-46, 21:20-28. Further, '806 teaches placing the dielectric structure and the TACs hosted by them within the

array region in order to shorten the interconnect routes the TACs provide. '806, 6:17-20, 11:8-10.

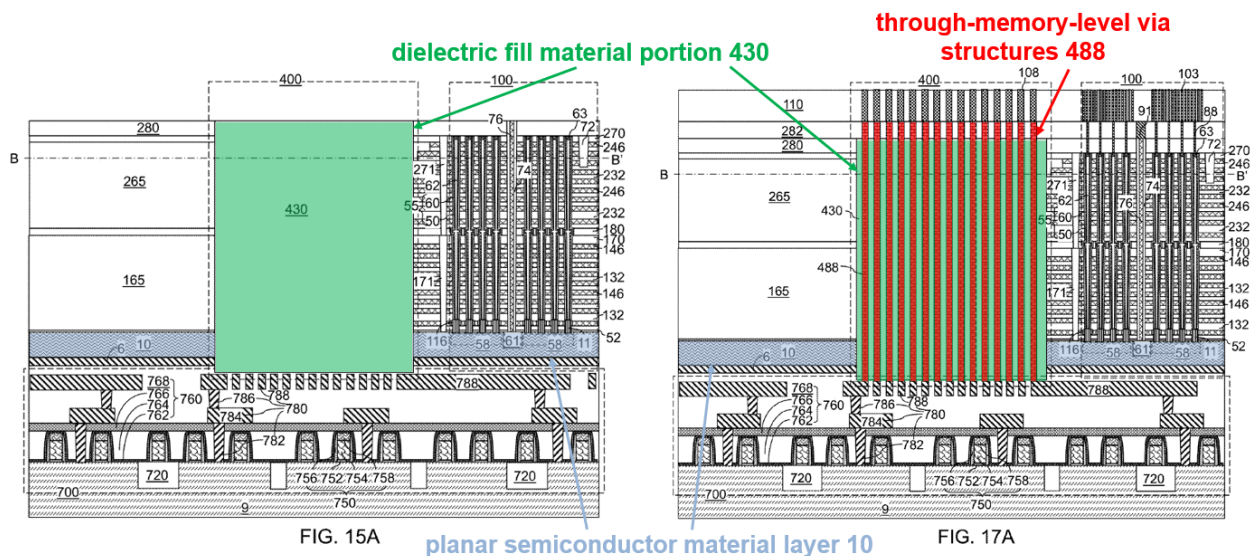
Toyama discloses multiple embodiments, but none of them teaches the structure claimed in the '806. Regarding the placement of “through-memory-level via structures,” Petitioner relies on two of Toyama’s teachings.

First, in Ground 1, Petitioner relies on placing “through-memory-level via structures 676” through an alternating stack of dielectric and conductive materials as in the second modification of the fourth exemplary structure (Ex. 1005, Fig. 49). As explained further in § VII.A, this embodiment lacks the claimed dielectric structure through which multiple TACs extend because only one TAC can extend through any individual liner. Rather, forming the TACs through an alternating stack of dielectric and conductive materials is exactly what the '806 aimed to avoid due to its complexity. '806, 5:41-45, 10:64-11:4, 18:32-46, 20:13-20.



Ex. 1005, Figs. 44A, 49 (annotated).

Second, in Ground 2, Petitioner relies on Toyama's placement of "through-memory-level via structures 488" in "dielectric fill material portion 430" as in the "first exemplary structure." Ex. 1005, Fig. 17A. As further explained in § VII.B, this structure lacks first and second channel regions such that a TAC region is between the first and second channel regions. Rather, the dielectric fill material is formed "on a lengthwise end of the ... block," in a staircase region, and therefore only has channels on one side. Ex. 1005, [0252], Fig. 17A.



Ex. 1005, Figs. 15A, 17A (annotated). In an attempt to overcome this deficiency, Petitioner copy-pastes Toyama's device such that it repeats in both horizontal directions (hd1 and hd2 below):

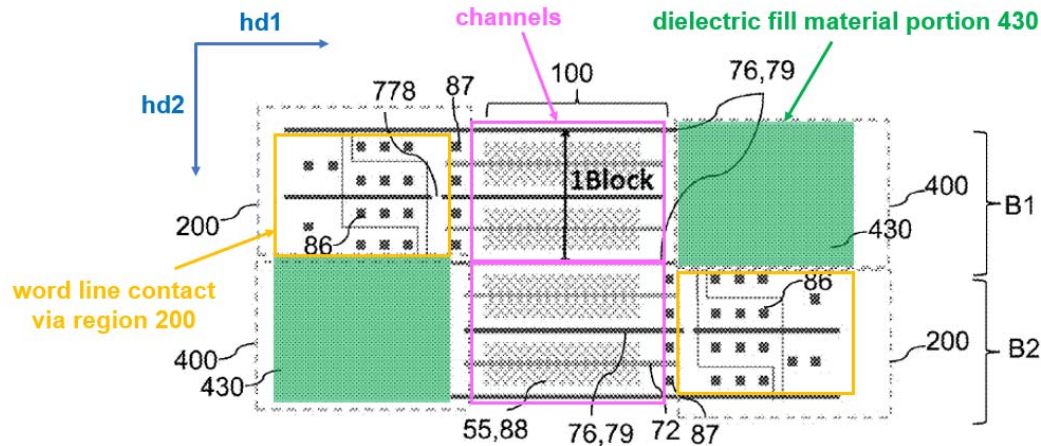
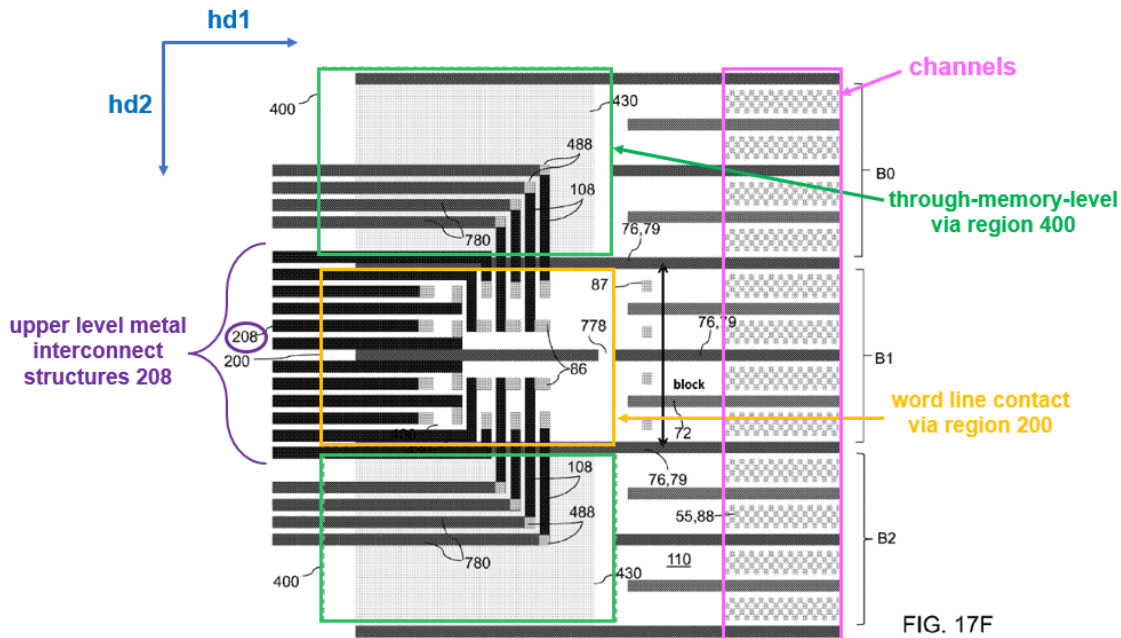


FIG. 17E

Ex. 1005, Fig. 17E (annotated). Although Toyama teaches that the blocks shown above can be repeated along the hd2 (bit line) direction, such repetition does not result in the claimed arrangement. Toyama also quite intentionally does not teach repeating the blocks in the hd1 (word line) direction because the inactive staircase regions are on the sides of Toyama's device—doubling up these regions back-to-back such that the inactive space is multiplied, as Petitioner proposes, rather than making the active channel region longer, is non-sensical. Toyama also requires additional circuitry elements on both the left and right of the word line contact via regions of Figure 17E, which Petitioner ignores. As shown in Toyama's Figure 17F below (illustrating the left side of exemplary blocks B0-B2), each staircase region has “upper level metal interconnect structures 208” extending into the hd1 direction to couple to circuitry such as “driver circuit devices.” Ex. 1005, [0251].



Ex, 1005, Fig. 17F (annotated). By simply copy-pasting the structures of Fig. 17E to repeat in the hd1 direction, Petitioner eliminates this necessary circuitry on the sides of the array. Finally, even if the proposed modification could work, Petitioner provides no motivation to make this change other than its hindsight-based attempt to match claim 10.

Third, in Ground 3, Petitioner again proposes a hindsight-based modification to the embodiments disclosed in Toyama by combining separate embodiments. In addition to failing to provide sufficient motivation for a POSITA to attempt this modification, Petitioner's proposal is again non-sensical. In an effort to try to match claim 10, Petitioner proposed replacing a region of Toyama's word lines, which are used to conduct current and control the memory cells, with a large insulating dielectric block from another portion of an embodiment. As explained

in § VII.C, a POSITA would not have replaced Toyama's conductive word lines used to control memory cells with a large insulating block that would eliminate or at least severely inhibit that control.

Moreover, in every ground, Petitioner fails to propose a mapping in accordance with the plain language of claim 10, which requires each of the local contacts to have etch stop plugs interposed between it and a channel structure. In Petitioner's faulty mapping, only some of the local contacts satisfy this condition.

Finally, Petitioner incorrectly argues that a rejection by the Chinese Patent Office in a proceeding involving a foreign counterpart is evidence of the U.S. Examiner "overlooking" Toyama's teachings. Pet. 2, 9, 11. Tellingly, as Federal Circuit precedent notes, "it is the reference itself, not the information generated in prosecuting foreign counterparts, that is material to prosecution in the United States. The details of foreign prosecution are not an additional category of material information." *See ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 547 (Fed. Cir. 1998). Indeed, Petitioner's faulty and conclusory analysis only highlights some of the reasons why prosecution history of a foreign counterpart is irrelevant here. First, the claims in the Chinese application are distinct from the Challenged Claim and do not recite analogous elements to the '806 claim elements such as "a through array contact (TAC) region formed between the first and second channel regions." Exs. 1010, 1012. Second, Petitioner ignores that the Chinese Patent Office found

that each of the independent claims (and by extension, all claims) in the Chinese application in fact had “distinguishing features” from Toyama, but only found them unpatentable by applying a legal standard different from the U.S. patent law (i.e., they did not “possess creativity” as prescribed in Chinese law). Exs. 1010, 1012. Third, Petitioner’s analysis is conclusory and, tellingly, makes no attempt to discuss the substance or applicability of the Chinese Patent Office’s analysis to the U.S. examination. Instead, Petitioner simply speculates that the Examiner must have overlooked Toyama’s teachings. All the evidence in the record points to the opposite: that Toyama’s teachings lack key inventive features of the ’806 application, and the Examiner recognized this fact.

Therefore, the Office did not err in a manner material to patentability of the Challenged Claim. The Board should exercise its discretion under § 325(d) and deny institution.

**VII. PETITIONER FAILS TO ESTABLISH A REASONABLE
LIKELIHOOD THAT IT WOULD PREVAIL WITH RESPECT TO
THE CHALLENGED CLAIM**

Petitioner fails to establish a reasonable likelihood that it would prevail with respect to the Challenged Claim because Petitioner has failed to show that prior art discloses or renders obvious at least the elements of the Challenged Claim relating to “a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array

contacts (TACs) extending vertically through the dielectric structure” and “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures.” As explained below, Petitioner cites a single primary reference—Toyama—and asserts that its various embodiments disclose or render obvious these features. But each of Petitioner’s grounds instead relies either on erroneous mappings or on making changes to Toyama solely due to the benefit of hindsight. Each of Petitioner’s arguments fails.

Ground 1 relies on Toyama’s “second modification of the fourth exemplary structure” (hereinafter “Second Modification”) that does not disclose or render obvious “a plurality of through array contacts (TACs) extending vertically through the dielectric structure.” Petitioner improperly attempts to rely on multiple separate dielectric structures, each with a single TAC extending through it—directly contradicting Federal Circuit precedent requiring that the TACs extend through a single dielectric structure to satisfy the claim language. Toyama’s Second Modification also does not disclose or render obvious “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures” because Petitioner presents a mapping in which there is no etch stop plug between some of the purported local contacts and channel structures.

Ground 2 relies on Toyama’s “First Exemplary Structure,” which similarly does not disclose or render obvious the aforementioned “TAC region” limitation. Realizing the deficiencies of Toyama’s First Exemplary Structure, Petitioner resorts to altering the device in ways that are not taught by Toyama and instead conflict with its teachings. Petitioner’s hindsight-driven obviousness arguments fail. Similar to Ground 1, Toyama’s First Exemplary Structure also does not disclose or render obvious the “etch stop plug” limitation because Petitioner presents a mapping in which there is no etch stop plug between some of the purported local contacts and channel structures.

Ground 3 relies on a modification of Toyama’s Second Modification based on Toyama’s First Exemplary Structure’s unitary dielectric fill material. Petitioner’s sole argument relies on trying to use the ’806 claims as a roadmap for obviousness and thus again fails. In addition, the erroneous modification proposed by Petitioner still fails to show the “etch stop plug” limitation for the same reasons as in Ground 1.

Therefore, Petitioner’s assertions as to claim 10 (which incorporates all the limitations of independent claim 8), the only Challenged Claim, fail with respect to all the grounds proposed by Petitioner.

A. Ground 1: Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious Limitations [8.g] and [10.b]

In Ground 1, Petitioner relies on Toyama’s Second Modification as allegedly rendering obvious the Challenged Claim (Pet. 26-61), but Petitioner fails to show that Toyama’s Second Modification discloses or renders obvious two separate limitations of the Challenged Claim: [8.g] (“... *a plurality of through array contacts (TACs) extending vertically through the dielectric structure*”) and [10.b] (“*an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures*”).

1. Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious “... a plurality of through array contacts (TACs) extending vertically through the dielectric structure” (Limitation [8.g])

Toyama’s Second Modification does not disclose or render obvious “*a plurality of through array contacts (TACs) extending vertically through the dielectric structure*” as required by limitation [8.g] because Toyama’s alleged plurality of TACs do not extend vertically through any one purported dielectric structure. Petitioner’s mapping directly conflicts with Federal Circuit precedent holding that multiple alleged occurrences of a claim element (here, Toyama’s multiple physically separated dielectric liners) cannot be used satisfy a limitation that must be satisfied by a single occurrence of the element (here, the claimed

plurality of TACs must extend through “***the dielectric structure***”). See *Finjan LLC v. SonicWall, Inc.*, 84 F.4th 963, 974-975 (Fed. Cir. 2023).

As illustrated below in Fig. 49, Petitioner maps Toyama’s three “**through-memory-level via structures 676**” to the claimed “plurality of through array contacts (TACs)” and attempts to map Toyama’s three separate “**insulating liners 674**” that line each separate “through-memory-level via structures 676” to the claimed “dielectric structure”:

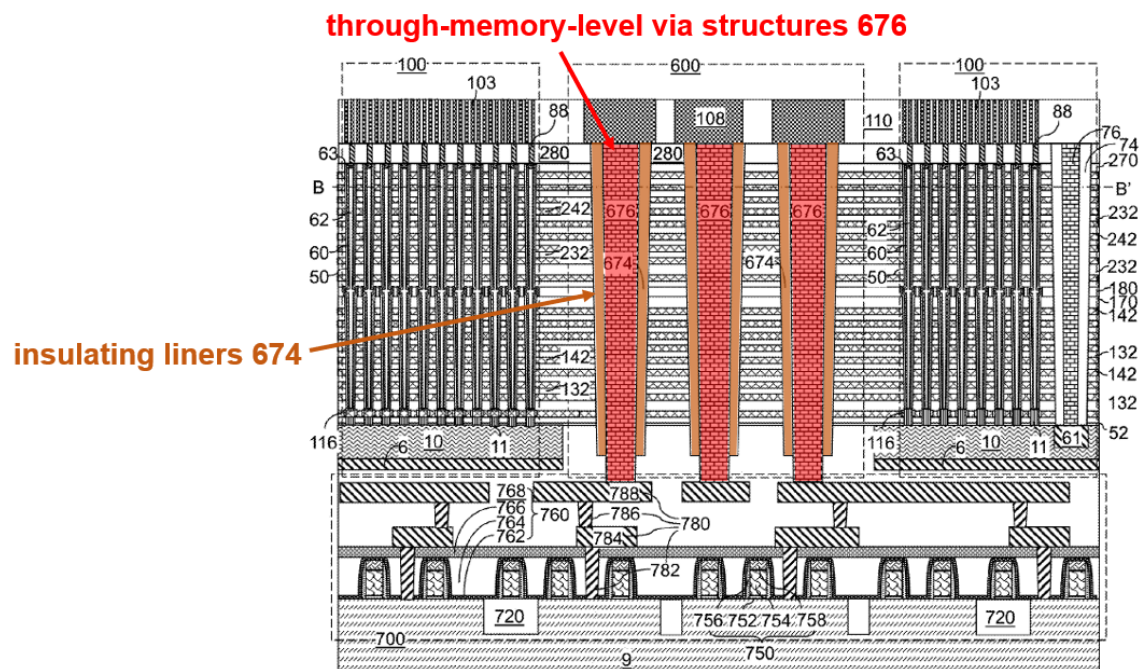


FIG. 49

Ex. 1005, Fig. 49 (annotated by Patent Owner to show Petitioner’s mapping); *see* Pet. 49 (using similar annotations but also adding a purple box over the image), 31-32. Toyama explains that one “through-memory-level cavity 679’ is present within each insulating liner 674” and that the “the through-memory-level via structures 676

can be formed ... within the through-memory-level openings 679.” Ex. 1005, [0340]-[0341].

The Challenged Claim, however, requires “a **plurality** of through array contacts (TACs) extending vertically through **the dielectric structure**,”—i.e., the same dielectric structure—which configuration is absent from Toyama's Second Modification. Even assuming that a TAC with a “liner” qualifies as a TAC extending through a “dielectric structure,” in Toyama’s Second Modification only a single alleged TAC extends through any given “insulating liner 674.” Realizing this problem, Petitioner erroneously attempts to map multiple insulating liners 674 to a single “dielectric structure.” Pet. 30-31.

Petitioner’s mapping directly conflicts with Federal Circuit law. The Federal Circuit has made clear that multiple occurrences of a claim element cannot be used satisfy a limitation that must be satisfied by a single occurrence of the element. *Finjan LLC v. SonicWall, Inc.*, 84 F.4th 963, 975 (Fed. Cir. 2023) (“Even if an infringing system can use ‘one or more computers,’ the plain language of the claims requires at least one of those computers to perform all the functions listed in the claims of the ARB Patent.”). Here, the claim requires that a single “dielectric structure” must have “a **plurality** of through array contacts (TACs) extend[] vertically through” it, which any of Toyama’s “insulating liner 674” fails to show.

In its attempt to map multiple separate liners to a single structure (Pet. 30-31), Petitioner misinterprets the Federal Circuit decision *KCJ Corp. v. Kinetic Concepts* in which the Court found that “an indefinite article ‘a’ or ‘an’ in patent parlance carries the meaning of ‘one or more’ in open-ended claims containing the transitional phrase ‘comprising.’” 223 F.3d 1351, 1356 (Fed. Cir. 2000). This principle merely means that in a memory structure that reads on claim 10 there could be more than one dielectric structures in the memory structure, and does **not** mean that more than one dielectric structures can be combined together for any requirements imposed on “the dielectric structure” (singular) in claim 10. *See Finjan*, 84 F.4th at 974-975 (“‘[T]he indefinite article a means one or more in open-ended claims containing the transitional phrase comprising.’ But that is a separate issue from whether the claims require the same component to perform multiple functions or satisfy multiple limitations of a claim. ... Claim 1 of the ARB Patent requires that the same computer perform each of the claimed steps.”). Petitioner ignores this distinction, and its misapplication of this fundamental principle means there is no basis for its improper mapping.

Therefore, Petitioner has failed to show that Toyama’s Second Modification discloses or renders obvious limitation [8.g].

2. Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures” (Limitation [10.b])

Toyama’s Second Modification does not disclose or render obvious “*an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures*” as required by limitation [10.b] because Toyama’s alleged etch stop plugs are not interposed between “**each**” of the local contacts and channel structures. Indeed, Petitioner’s analysis for dependent claim 10 entirely ignores one of the structures that Petitioner mapped to the local contacts of independent claim 8. This is because Toyama’s alleged etch stop plugs are plainly not interposed between that purported local contact and the purported channel structures.

The ’806 limitation [8.c] recites “first and second channel regions comprising first and second pluralities of channel structures,” which form the antecedent basis for the “each channel structure of the first and second channel structures” of limitation [10.b]. In addition, limitation [8.f] recites “local contacts disposed on the first and second channel structures and the slit structures,” which form the antecedent basis for “each local contact of the local contacts” of limitation [10.b]. In relevant part, claim 10 requires an etch stop plug “interposed between each local

contact of the local contacts and each channel structure of the first and second channel structures.”

Petitioner’s mapping for claim 10 does not even attempt to address “each local contact.” For independent claim 8, Petitioner contends that Toyama’s “**memory stack structures 55**” are the claimed “first and second channel structures” and that Toyama’s “**drain contact via structures 88**” and “**source connection via structures 91**” are the claimed “local contacts disposed on the first and second channel structures and the slit structures.” Pet. 32-38, 40-44.

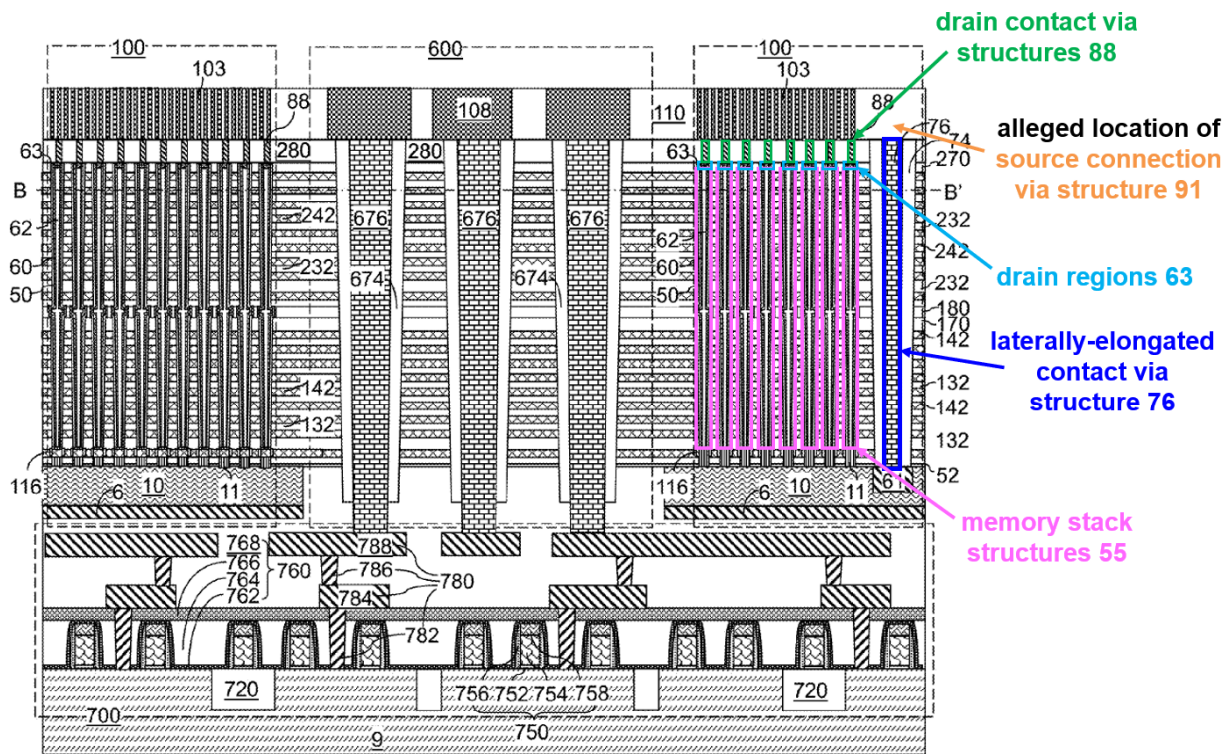


FIG. 49

Ex. 1005, Fig. 49 (annotated by Patent Owner). Although the Petition does not annotate the location of **source connection via structures 91** in Figure 49,

Petitioner argues that a POSITA would have understood **source connection via structures 91** to be disposed on the **laterally-elongated contact via structures 76**, as shown above.⁴ Pet. 40-44. With regards to claim 10, Petitioner argues that Toyama’s “**drain regions 63**” meet the limitation of “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures.”⁵ Pet. 54-59. Petitioner’s analysis, however, discusses only **drain contact via structures 88** (a subset of the purported local contacts)—not **source connection via structures 91**, which Petitioner mapped to one of the claimed local contacts to meet limitation [8.f].

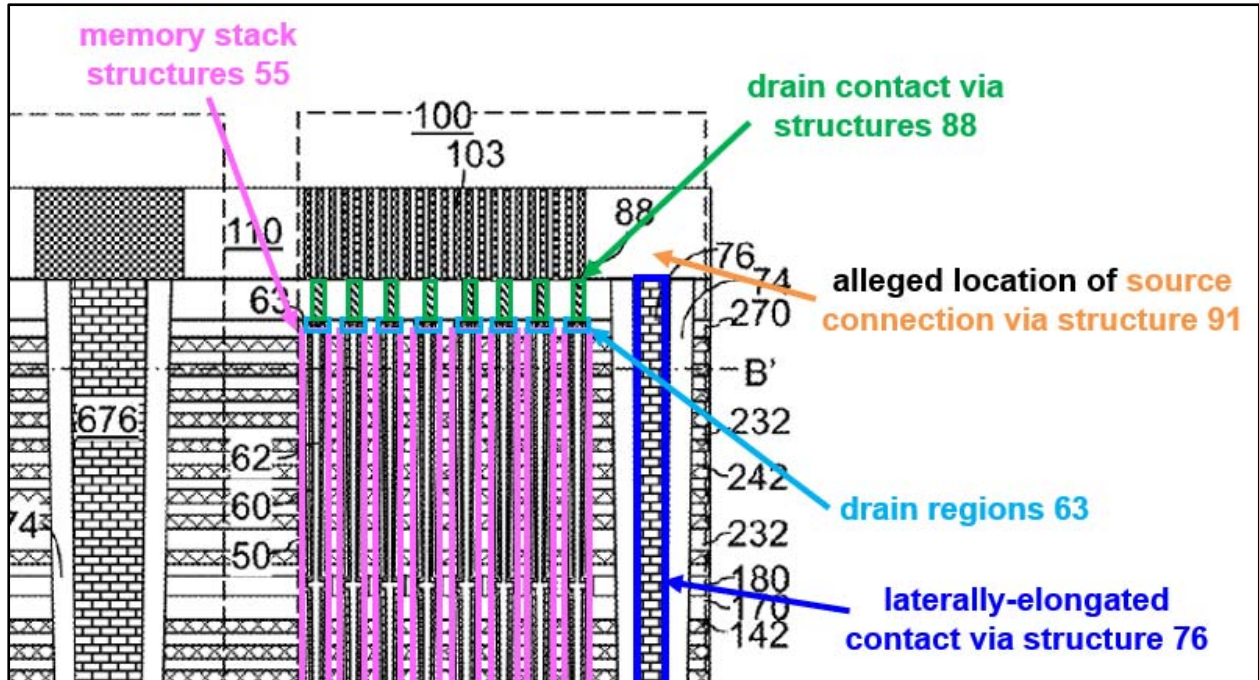
Because claim 10 requires an etch stop plug interposed between **each local contact of the local contacts** and each channel structure of the first and second channel structures, Petitioner was required to identify an etch stop plug that is

⁴ For the purposes of this POPR, Patent Owner does not dispute Petitioner’s claim that Toyama’s “Second Modification ... would also include ‘source connection via structures’” or that a “POSITA would have found the use of local contacts disposed on the slit structures (‘source connection via structures 91’) obvious.”

⁵ For the purposes of this POPR, Patent Owner does not dispute Petitioner’s claim that “a POSITA would have understood, or at least found obvious, that ‘drain regions 63’ are plugs that serve the purpose of stopping an etch.” Pet. 55.

interposed between the **source connection via structures** and **memory stack structures**—but failed to do so. As previously explained, Petitioner maps the antecedent for “the local contacts” to both the **drain contact via structures** and the **source connection via structures**, and therefore needs to identify etch stop plugs between both of these structures and the purported channel structures, respectively. While Petitioner’s mapping discusses **drain contact via structures** and **memory stack structures**, Petitioner does not even attempt to address **source connection via structures** and **memory stack structures**. Arguing that Toyama discloses an etch stop plug interposed between the channel structures and some of the purported local contacts that Petitioner mapped to the claimed local contacts is not sufficient. Petitioner simply failed to show that Toyama’s Second Modification teaches each element of limitation [10.b] and fails as a result.

Toyama’s alleged etch stop plug, **drain regions 63**, is **not** interposed between **source connection via structures 91** (one of the purported local contacts) and **memory stack structures 55** (the alleged channel structures) as required by claim 10. As shown in Fig. 49 of Toyama annotated below, the **drain regions 63** are, at most, “interposed between” the **drain contact via structures 88** and **memory stack structures 55**. None of the **drain regions 63**, however, is “interposed between” the **source connection via structures 91** and **memory stack structures 55** as required by limitation [10.b]:



Ex. 1005, Fig. 49 (excerpted and annotated by Patent Owner). As a result, the alleged etch stop plug of Toyama is not interposed between “each” local contact of the local contacts and each channel structure of the first and second channel structures as required by limitation [10.b].

Therefore, Petitioner has failed to show that Toyama's Second Modification discloses or renders obvious limitation [10.b].

B. Ground 2: Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious Limitations [8.g] and [10.b]

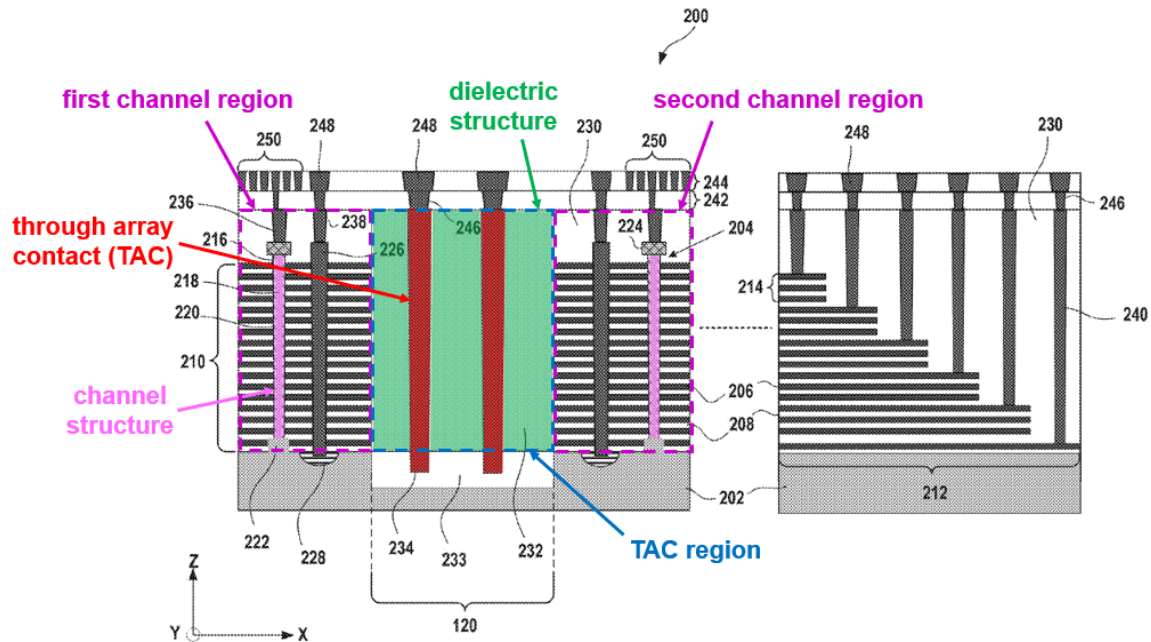
In Ground 1, Petitioner relies on Toyama’s First Exemplary Structure as allegedly rendering obvious the Challenged Claim (Pet. 61-100), but Petitioner fails to show that Toyama’s First Exemplary Structure discloses or renders obvious two separate limitations of the Challenged Claim: [8.g] (“... ***a plurality of through array***

contacts (TACs) extending vertically through the dielectric structure”) and [10.b] (*“an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures”*).

1. Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious “... a plurality of through array contacts (TACs) extending vertically through the dielectric structure” (Limitation [8.g])

Toyama’s First Exemplary Structure does not disclose or render obvious “*a plurality of through array contacts (TACs) extending vertically through the dielectric structure*” as required by limitation [8.g] because the alleged TAC region is not formed between a first channel region and a second channel region. Instead, it has a channel region on only one side. While Petitioner proposes altering the First Exemplary Structure to repeat portions of the device and add a second channel region, its modification cannot and would not be made because it omits necessary neighboring structures, including the driver circuit that connects to the memory structure on the second side.

The ’806 claim 8 requires “a **through array contact (TAC) region** formed **between the first and second channel regions,**” which Toyama’s First Exemplary Structure fails to teach.



Ex. 1001, Fig. 2 (annotated). As illustrated in Figure 2 of the '806, above, the through array contacts (TACs) are formed in a **TAC region** that is formed in the active region between the **first and second channel regions**. As a result of this improvement, interconnect routing may be shortened.

In contrast to the '806 Patent, the channels in Toyama's First Exemplary Structure are present only on one side of each alleged TAC region (i.e., the alleged region containing dielectric fill material portion 430 and through-memory-level via structures 488):

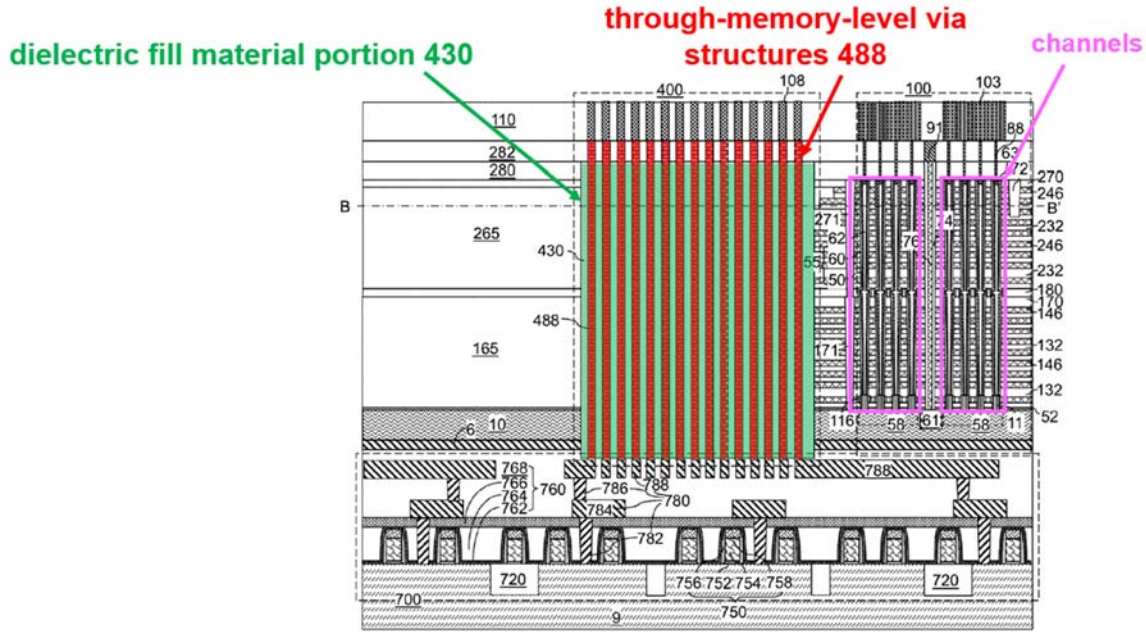


FIG. 17A

Ex. 1005, Fig. 17A (annotated by Patent Owner to show Petitioner's mapping); see Pet. 65, 85-87. Toyama never contemplates forming channels on both sides of the alleged TAC region of Toyama's First Exemplary Structure.

In a hindsight-based attempt to overcome this deficiency, Petitioner alters Toyama's device to repeat in both horizontal directions (hd1 and hd2). Pet. 69. Figure 17E of Toyama shows a top-down view of the structures that Petitioner proposes repeating in the hd1 and hd2 directions:

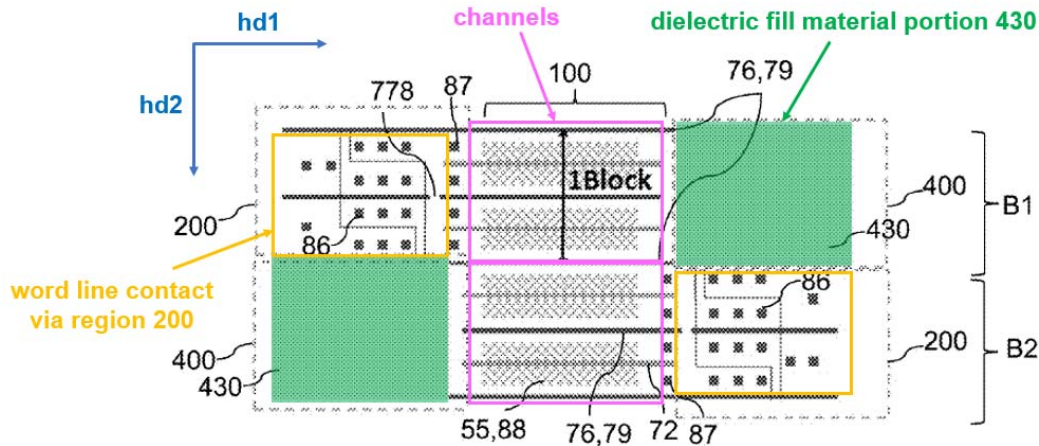
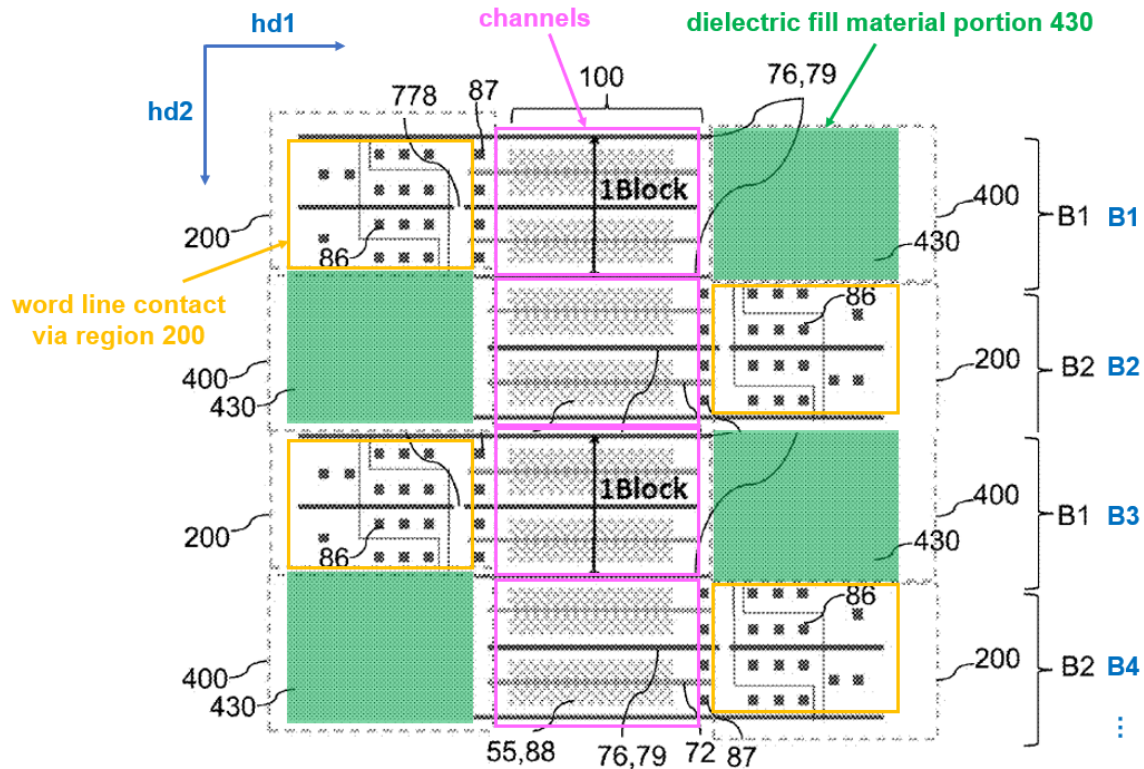


FIG. 17E

Ex. 1005, Fig. 17E (annotated). As discussed above, Petitioner maps the region containing dielectric fill material portion 430 to the claimed TAC region. Pet. 85-86. While Toyama does suggest repeating this layout in the hd2 direction (bit line direction), repeating in the hd2 direction merely creates a row of adjacent channels and does not result in the claimed configuration of a TAC region with channel regions on both sides. Moreover, Toyama never suggests that this layout may be repeated in the hd1 direction (word line direction) because other circuitry that Petitioner ignores, including driver circuits, is required beyond the staircase regions in the hd1 direction.

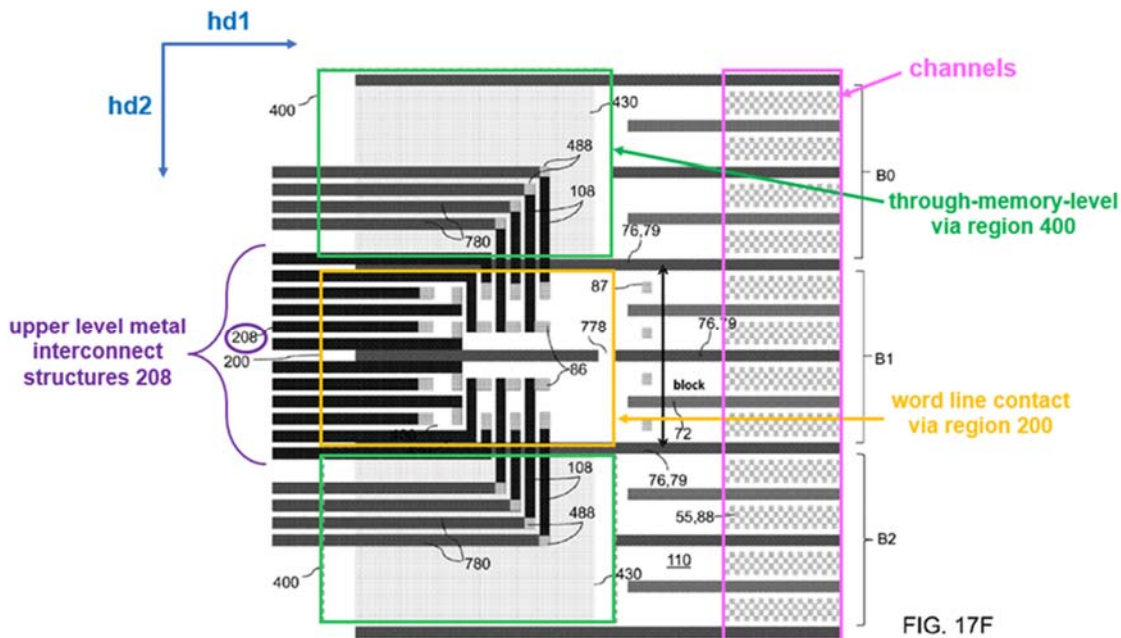
First, repeating Toyama's layout along the bit line direction (hd2) does not alter the basic configuration of Toyama's memory device: an alleged channel region on only one side of each alleged TAC region. As shown below, the alleged channel regions simply repeat in a row, as a contiguous set of channel regions:



Ex. 1005, Fig. 17E (annotated and modified). Thus, this proposed modification does not result in a TAC region formed between first and second channel regions as required by the Challenged Claim.

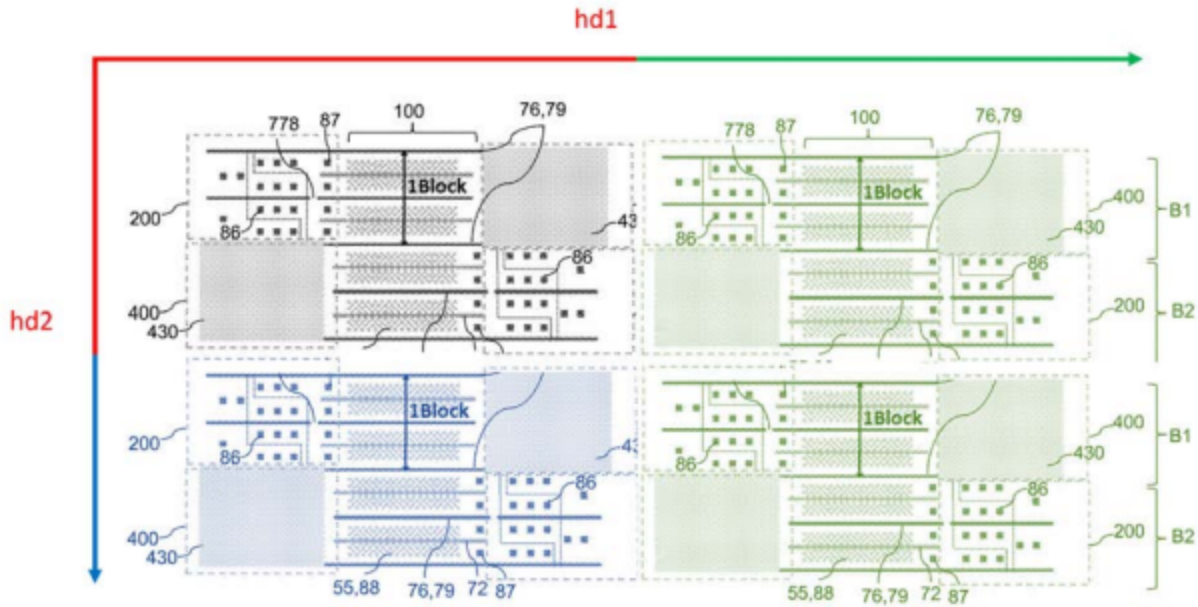
Second, repeating the layout along the word line direction (hd1) is not taught by Toyama, and the layout **cannot** be repeated in that direction as proposed by Petitioner because Toyama includes “peripheral circuitry” beyond the alleged TAC region. Ex. 1005, [0163]. Such peripheral circuitry, such as “driver circuitry,” “supports[s] the operation of [the] memory structure.” *Id.* For example, Toyama teaches “upper level metal interconnect structures 208” to connect to the driver circuits. Ex. 1005, [0251]. Indeed, Figure 17F—which is part of the First Exemplary

Structure relied upon by Petitioner in this ground—shows these interconnect structures, which extend to the left of the alleged TAC region for connecting to the driver circuit.



Ex, 1005, Fig. 17F (annotated). Moreover, because Toyama’s blocks have “word line contact via regions 200” on the left and on the right of the channels, the interconnects and driver circuits are present on **both sides** of the layout in the hd1 direction.

Petition’s proposed modification completely ignores the peripheral circuitry, including the driver circuit, and therefore would not work. As shown below, Petitioner’s alteration of Toyama to repeat in the hd1 direction does not account for the necessary driver circuitry:



Ex. 1005, Fig. 17E (modified and annotated by Petitioner, Pet. 69). It is unsurprising that the layout of Figure 17E is not repeatable in the hd1 direction—Toyama is designed to instead repeat in the hd2 direction, with peripheral circuitry on either side in the hd1 direction. But none of the circuitry needed to operate each memory array is included in Petitioner’s analysis. Petitioner relies on hindsight to blindly copy and paste elements of Toyama, in a way not taught by Toyama, and in a way that lacks the necessary support circuitry for a functioning memory device.

Therefore, Petitioner has failed to show that Toyama’s First Exemplary Structure discloses or renders obvious limitation [8.g].

2. Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures” (Limitation [10.b])

Toyama’s First Exemplary Structure does not disclose or render obvious “*an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures*” as required by limitation [10.b] because Toyama’s alleged etch stop plugs are not interposed between “**each**” of the purported local contacts and channel structures. As with Ground 1, Petitioner’s analysis of Ground 2 for dependent claim 10 entirely ignores one of the structures that Petitioner mapped to the local contacts of independent claim 8. This again is because Toyama’s alleged etch stop plugs are plainly not interposed between that purported local contact and the purported channel structures.

Petitioner’s mapping for claim 10 does not even attempt to address “each local contact.” For independent claim 8, Petitioner once again contends that Toyama’s “**memory stack structures 55**” are the claimed “first and second channel structures” and that Toyama’s “**drain contact via structures 88**” and “**source connection via structures 91**” are the claimed “local contacts disposed on the first and second channel structures and the slit structures.” Pet. 70-85, 86-87.

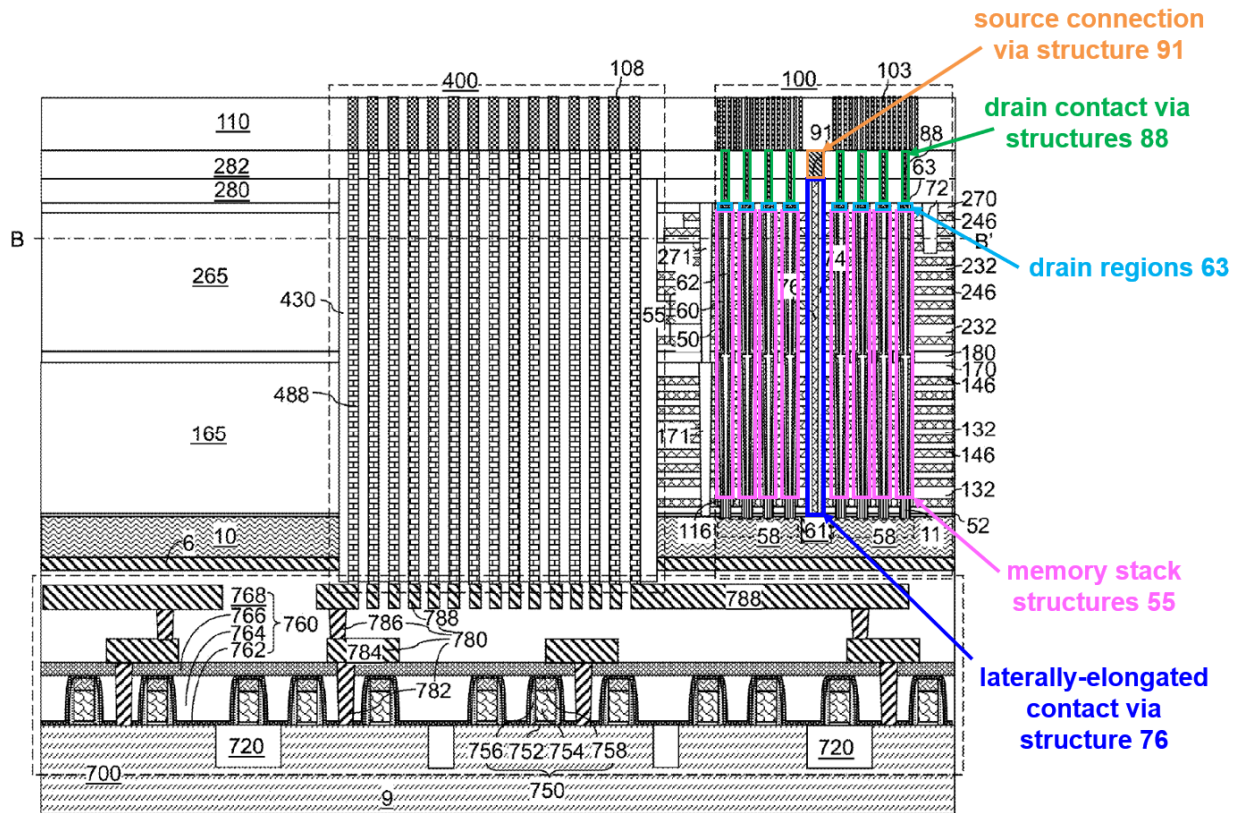


FIG. 17A

Ex. 1005, Fig. 17A (annotated by Patent Owner). Specifically, to meet limitation [8.F], Petitioner argues that Toyama’s **drain contact via structures 88** are local contacts disposed on **memory stack structures 55** and that **source connection via structures 91** are local contacts disposed on “**laterally-elongated contact via structures 76.**” Pet. 86-87. With regards to claim 10, Petitioner argues that Toyama’s “**drain regions 63**” meet the limitation of “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the

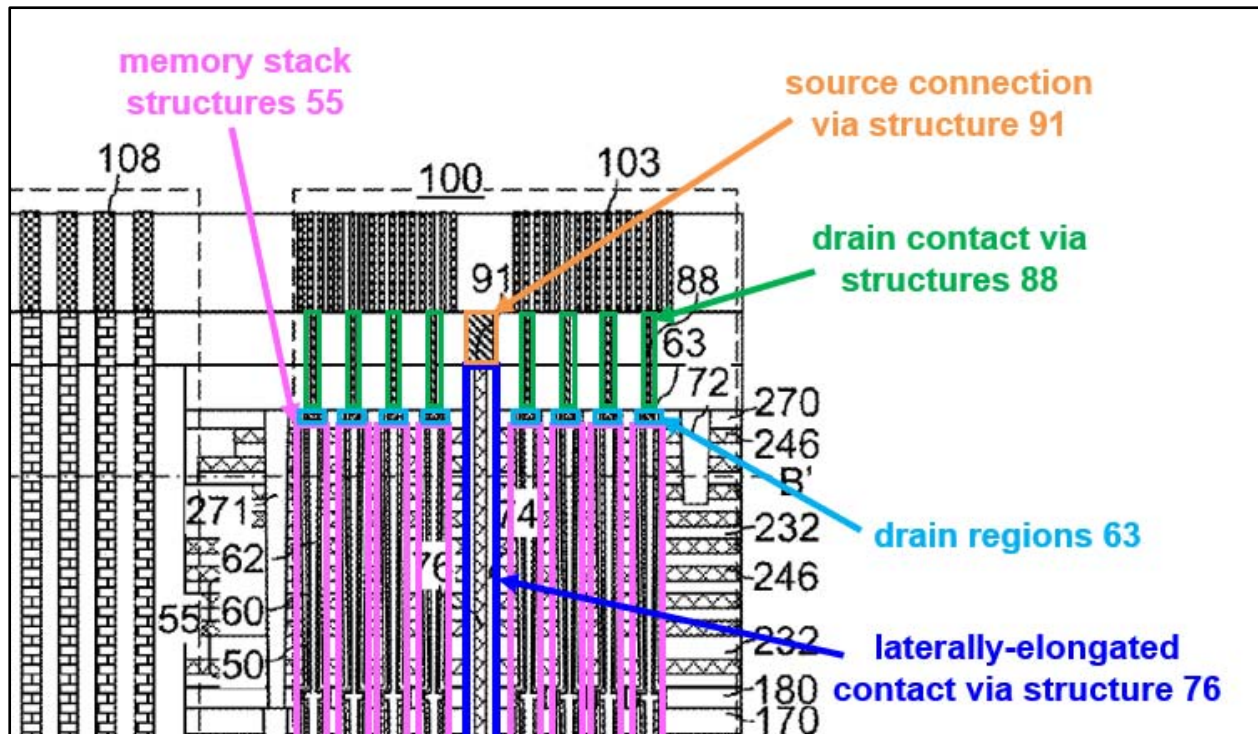
first and second channel structures.”⁶ Pet. 98-99. Petitioner’s analysis, however, discusses only **drain contact via structures 88** (a subset of the purported local contacts)—not **source connection via structures 91**, which Petitioner mapped to one of the claimed local contacts to meet limitation [8.f].

Because claim 10 requires an etch stop plug interposed between **each local contact of the local contacts** and each channel structure of the first and second channel structures, Petitioner was required to identify an etch stop plug that is also interposed between the **source connection via structures** and **memory stack structures**—but failed to do so. As previously explained, Petitioner maps the antecedent for “the local contacts” to **both** the **drain contact via structures** and the **source connection via structures**, and therefore needs to identify etch stop plugs between both of these structures and the purported channel structures, respectively. While Petitioner’s mapping discusses **drain contact via structures** and **memory stack structures**, Petitioner does not even attempt to address **source connection via structures** and **memory stack structures**. Arguing that Toyama discloses an etch stop plug interposed between the channel structures and **some** of the purported local

⁶ For the purposes of this POPR, Patent Owner does not dispute Petitioner’s claim that “a POSITA would have understood, or at least found obvious, that ‘drain regions 63’ are plugs that serve the purpose of stopping an etch.” Pet. 55.

contacts that Petitioner mapped to the claimed local contacts is not sufficient. Petitioner simply failed to show that Toyama's First Exemplary Structure teaches each element of limitation [10.b] and this Ground fails as a result.

Toyama's alleged etch stop plug, **drain regions 63**, is **not** interposed between **source connection via structures 91** (one of the alleged local contacts) and **memory stack structures 55** (the alleged channel structures) as required by claim 10. As shown in Fig. 17A of Toyama annotated below, the **drain regions 63** are, at most, "interposed between" the **drain contact via structures 88** and **memory stack structures 55**. None of the **drain regions 63**, however, is "interposed between" the **source connection via structures 91** and **memory stack structures 55** as required by limitation [10.b]:



Ex. 1005, Fig. 17A (excerpted and annotated by Patent Owner). As a result, the alleged etch stop plug of Toyama is not interposed between “each” purported local contact of the local contacts and each purported channel structure of the first and second channel structures as required by limitation [10.b].

Therefore, Petitioner has failed to show that Toyama’s First Exemplary Structure discloses or renders obvious limitation [10.b].

C. Ground 3: Petitioner Fails to Show That a POSITA Would Have Found It Obvious to Modify Toyama or That the Proposed Modification Discloses or Renders Obvious Limitation [10.b]

In Ground 3, Petitioner relies on a modification of Toyama’s Second Modification based on Toyama’s First Exemplary Structure (hereinafter, following Petitioner’s terminology for convenience, “Obviousness Combination”) as allegedly

rendering obvious the Challenged Claim (Pet. 100-125), but Petitioner (1) fails to show that a POSITA would have found it obvious to modify Toyama in the proposed manner and (2) fails to show that the proposed modification renders obvious limitation [10.b] (“*an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures*”).

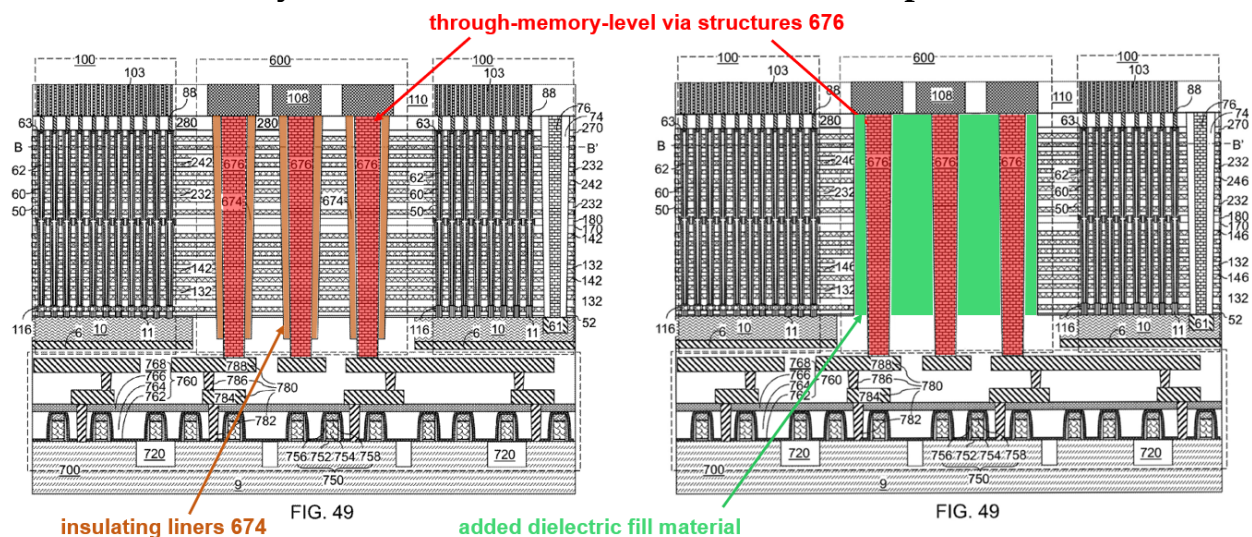
1. Petitioner Fails to Show That a POSITA Would Have Found It Obvious to Modify Toyama’s Second Modification in the Proposed Manner

Petitioner’s modification of Toyama’s Second Modification based on Toyama’s First Exemplary Structure (“Obviousness Combination”) fails because a POSITA would not have made Petitioner’s hindsight-based modification as it replaces conductive material used to conduct current to control memory with a large dielectric (an insulator), and Petitioner does not even attempt to address the impact that these changes would have had on Toyama’s memory structure.

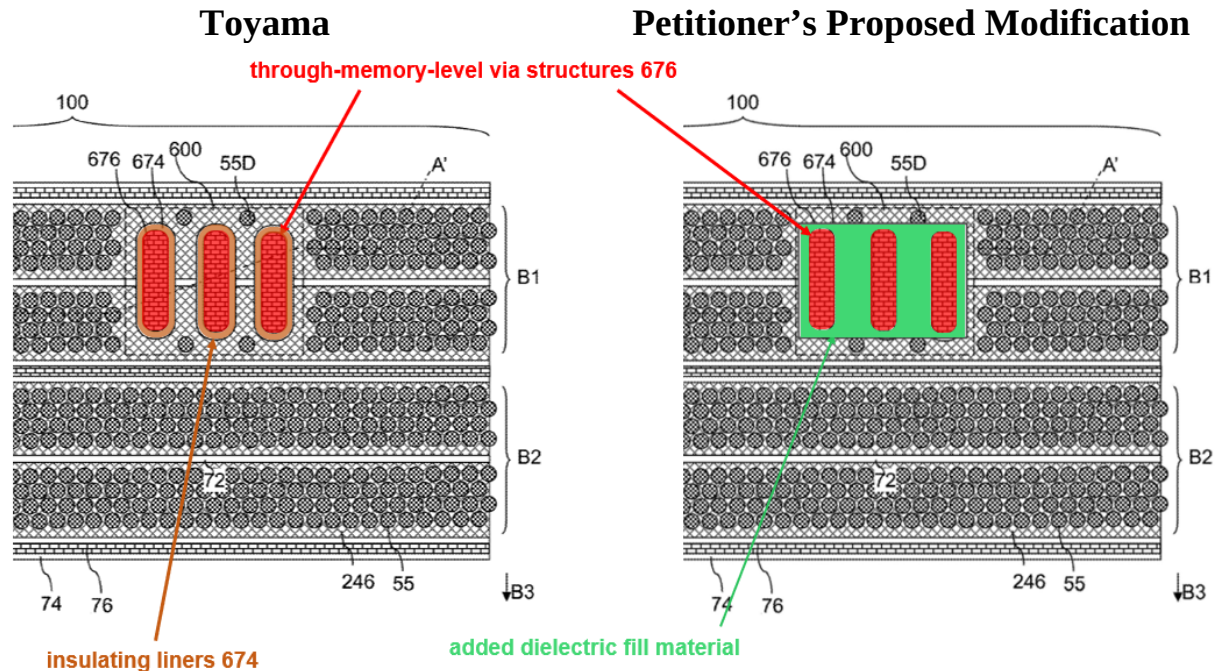
Petitioner fails to show that a POSITA would have been motivated to make its proposed modification of Toyama’s Second Modification based on Toyama’s First Exemplary Structure. As discussed in § VII.A.1, Toyama’s Second Modification does not disclose or render obvious “*a plurality of through array contacts (TACs) extending vertically through the dielectric structure*” as required by limitation [8.g] because Toyama’s alleged TACs do not extend through the same

structure (the claimed “dielectric structure”). With the hope of overcoming this deficiency, in Ground 3, Petitioner puts forth a modification of Toyama’s Second Modification based on Toyama’s First Exemplary Structure, wherein the physically separated insulating liners around the alleged TACs are replaced with a unitary dielectric filling material around all the alleged TACs, as shown:

Petitioner's Proposed Modification



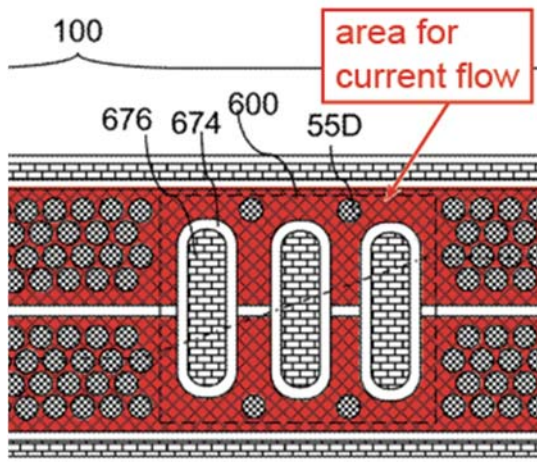
Ex. 1005, Fig. 49 (left: annotated by Patent Owner; right: modified by Petitioner at Pet. 104 and annotated by Patent Owner).



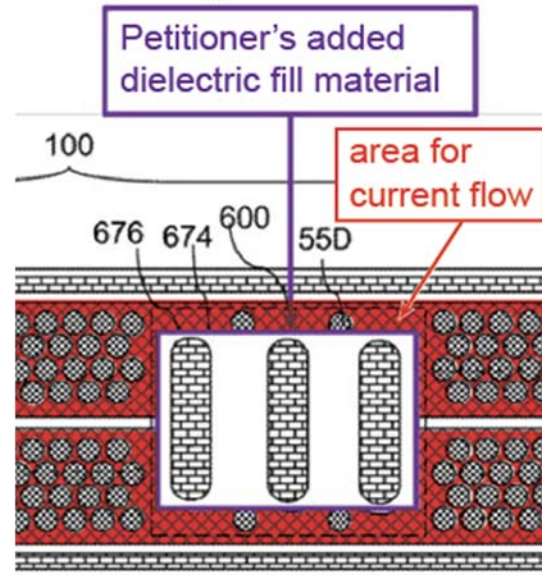
Ex. 1005, Fig. 48B (left: annotated and excerpted by Patent Owner; right: modified by Petitioner at Pet. 105 and annotated and excerpted by Patent Owner).

A POSITA would not have added a unitary dielectric fill material to Toyama's Second Modification because this modification removes large portions of the conductive layers in the active region that form the word lines and replaces them with an insulator. Importantly, these word lines are conductive and used to conduct current to control the memory—replacing them with a large insulator would eliminate that capability in those areas. As illustrated below, Petitioner's proposed modification (enlarged and annotated below) would add an insulating dielectric fill material that has a much larger area than the original insulating liners, and extends all the way to dummy memory stack structures 55D:

Toyama



Petitioner's Proposed Modification



Ex. 1005, Fig. 48B (left: annotated and excerpted by Patent Owner; right: modified by Petitioner at Pet. 105 and annotated and excerpted by Patent Owner). As such, this would eliminate any current flow in these areas of the current flow in the word lines. Petitioner does not even attempt to address this issue, including the adverse impact the restriction of current flow would have on the operability of the device. A POSITA would not have made this alteration to eliminate critical current flow in these areas.

To overcome these difficulties, the '806 has a different arrangement of features in the relevant regions, which does not create the restrictions present in Petitioner's proposed Obviousness Combination:

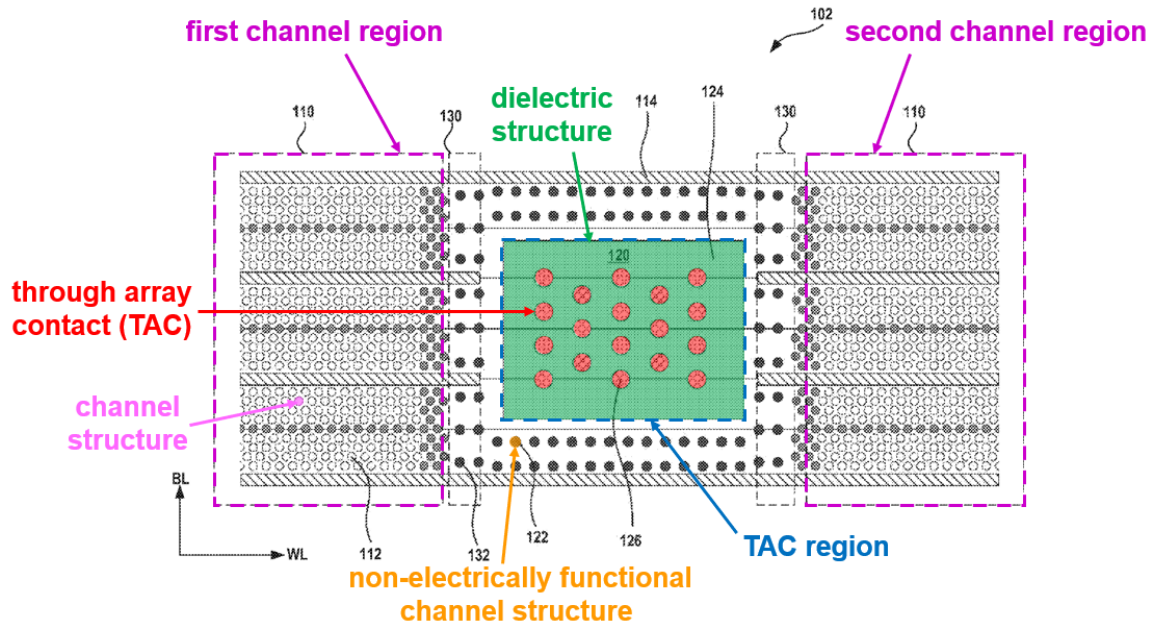


FIG. 1A

'806, Fig. 1A (annotated). In addition, the '806 uses an isolation structure onto which the dielectric structure is deposited with a high level of control using various patterning techniques. '806, 10:35-38, 14:63-15:30, 21:20-28. Forming a unitary dielectric fill material portion in a crowded memory array region with several other structures in its vicinity presents challenges that would have deterred a POSITA and are overcome by the novel teachings of the '806. Petitioner fails to address these considerations and simply asserts that the Obviousness Combination "is nothing more than the mere substitution of one element ... for another ... to yield a predictable result." Pet. 105. The only thing predictable about Petitioner's proposed alteration is that replacing the conductive material in the word lines used to control the memory with an insulator would cause the device to fail.

Notably, Toyama alone teaches more than a dozen embodiments with various configuration of elements, but none of these embodiments teach forming a unitary dielectric block in the memory array region between two channel regions because it eliminates the conductive material in the word lines.

Petitioner's argument that a POSITA would have been motivated to make the combination because it "would reduce capacitive coupling as compared to Toyama's Second Modification" (Pet. 107-108) is misplaced. Petitioner argues that its modification addresses capacitive coupling between the through-memory-level vias (the alleged TACs) and the electrically conductive layers in that region, but Toyama's Second Modification already "minimizes" capacitive coupling by placing the through-memory-level via structures in the memory array region with dielectric liners. Ex. 1005, [0377]. As Toyama explains, these through-memory-level via structures "provide various control signals for a three-dimensional memory device in a manner that shortens the signal path, and thus, minimizes ... capacitive coupling." *Id.* Petitioner's expert, Dr. Lee, explains that there is a relation between capacitive coupling and distance between conductive elements (Ex. 1003 ¶ 228), but he fails to address that capacitive coupling is also a function of the length (or area) of overlap. *See* Ex. 1026 at 64 ("Crosstalk increases as the ... ***length of their close proximity*** (coupled length) increases"). In Toyama, the through-memory-level via structures and the "electrically conductive layers (146, 246)" run perpendicular to one

another—i.e., vertical vias passing through horizontal layers—and thus the length or area of their proximity is de minimis. Thus, Petitioner has not shown that replacing Toyama’s insulating liners with a dielectric fill material portion would reduce capacitive coupling, particularly where Toyama expressly “minimizes” it already.

Petitioner further argues that a POSITA would have recognized that placing the through-memory-level via structures (the alleged TACs) in the memory array region 100 has certain benefits (Pet. 108-109), but Toyama’s Second Modification—the embodiment that Petitioner proposes modifying—already has through-memory-level via structures (the alleged TACs) in the memory array region 100. Petitioner is not proposing moving the alleged TACs. Thus, any benefits of having the alleged TACs in that particular location are irrelevant to whether a POSITA would make a different modification, i.e. adding a unitary dielectric fill material as proposed by Petitioner.

Petitioner asserts that “elements of the [F]irst [E]xemplary [S]tructure and the Second Modification are compatible with each other” (Pet. 111; Ex. 1003, ¶¶ 226-239), but Toyama does not teach such compatibility or substitution between its embodiments. Rather, Petitioner’s argument is based on nothing more than the conclusory testimony of Petitioner’s expert. *See* Pet. 111 (citing Ex. 1003, ¶¶ 236-239). That a limited set of other, **different** structures may have the same name in both embodiments (*id.*) is irrelevant.

Petitioner's assertion that a POSITA would have found the combination straightforward (Pet. 109-113, citing Ex. 1003, ¶¶ 226-239) relates to whether a POSITA could **manufacture** the device, and do not address the lack of motivation to make the proposed combination, let alone the adverse impact that replacing the conductive word lines with an insulator would have.

Therefore, Petitioner fails to show that a POSITA would have found it obvious to modify Toyama's Second Modification in the alleged manner.

2. Petitioner Fails to Show That the Obviousness Combination Discloses or Renders Obvious “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures” (Limitation [10.b])

Even if a POSITA would have found Petitioner's Obviousness Combination obvious (which is not the case), the Obviousness Combination still does not disclose or render obvious “*an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures*” as required by limitation [10.b] because, as with Grounds 1 and 2, Toyama's alleged etch stop plugs are not interposed between each purported local contact of the local contacts and the channel structures.

In Ground 3, Petitioner relies on the Ground 1 arguments regarding Toyama's Second Modification to allegedly meet the etch stop plug limitation [10.b]. Pet. 125 (“The obviousness combination does not alter any of the foregoing components in

the Second Modification”). As explained in § VII.A.2, Petitioner’s Ground 1 arguments with respect to limitation [10.b] fail.

Therefore, Petitioner has failed to show that the Obviousness Combination discloses or renders obvious limitation [10.b] for the same reasons discussed for Ground 1.

VIII. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests that the Board deny institution.

Dated: October 10, 2024

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 10,187 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: October 10, 2024

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CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

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