

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00911
Patent 10,937,806

**DECLARATION OF WOODWARD YANG, PH.D. IN SUPPORT OF
PATENT OWNER'S RESPONSE**

Executed this 3rd day of April, 2025 in Milan, Italy (GMT + 2).

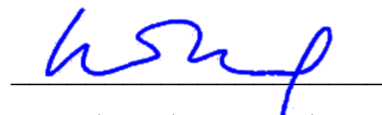

Woodward Yang, Ph.D.

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I, Woodward Yang, Ph.D., hereby declare as follows:

I. INTRODUCTION

1. I have been retained by counsel for Yangtze Memory Technologies Company, LTD (“YMTC”) in the above captioned *inter partes* review of U.S. Patent No. 10,937,806 (Ex. 1001, “’806 patent”). I have been asked to consider the scope and content of the prior art, and respond to certain allegations regarding the prior art, presented by Micron Technology, Inc., (“Petitioner”) in its petition for *inter partes* review of the ’806 patent (“Petition”) and the May 2, 2024 Declaration of Dr. Jack Lee (Ex. 1003). The arguments raised in Dr. Lee’s declaration are similar to those raised in the Petition. Unless otherwise noted, my opinions with respect to the Petition also apply to the corresponding section of Dr. Lee’s declaration, and vice-versa. As explained in Sections X-XII (discussing the Grounds raised in the Petition), the invalidity arguments raised in the Petition do not show that the prior art anticipates or renders obvious the Challenged Claim, and the arguments raised in Dr. Lee’s declaration are insufficient for similar reasons.

2. I am being compensated for my time at my usual consulting rate of \$900 per hour, plus reimbursement for any actual expenses. No part of my compensation depends on the content of the opinions that I herein render or on the outcome of this review proceeding. I have no expectation or promise of additional business with

Patent Owner (“PO”) in exchange for the positions explained herein. I do not have any direct financial interest in any of the parties.

3. Unless otherwise noted, the statements made herein are based on my personal knowledge, and if called to testify about this declaration, I could and would do so competently and truthfully.

II. QUALIFICATIONS

4. My qualifications including cases in which I was an expert are stated more fully in my curriculum vitae which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

5. I am presently the Gordon McKay Professor of Electrical Engineering and Computer Science in the Paulson School of Engineering and Applied Science at Harvard University, where I have taught and pursued research endeavors since 1990. I have taught classes related generally to the design and analysis of microelectronic circuits and Very Large Scale Integration (“VLSI”) systems: the process of creating integrated circuits by combining thousands of transistors into a single chip. The microprocessors and graphics processors found in personal computers and smartphones are examples of VLSI devices. I have also taught graduate and undergraduate level courses in computer architecture, computing hardware, digital logic design, mixed signal circuit design, circuit theory, and engineering design. My research pursuits have been directed to the development of advanced computing and

memory systems for high performance image processing and computer vision applications, data encryption, error correcting codes, and integrated sensor and computing systems.

6. In 2008, I was appointed as the Harvard Business School (“HBS”) University Fellow and have taught courses at HBS as a Visiting Professor. In this capacity, I have conducted research and taught business school courses on the commercialization of new technologies, technological innovation, and industry architecture.

7. I have over 30 years of experience in semiconductor design and manufacturing technology. I graduated with a Bachelor of Science degree in Electrical Engineering and Computer Science from the University of California, Berkeley in 1984. I received a Master’s of Science degree in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology in 1987. I then received a Ph.D. in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology in 1990. My doctoral thesis dealt with the architecture and design of charge-coupled device (“CCD”) processors for computer vision. In the 1990’s and early 2000’s, I developed and successfully commercialized two disruptive technologies, complementary metal oxide semiconductor (“CMOS”) image sensors and pseudo-SRAM (Static Random Access Memory), which were based on advanced DRAM manufacturing technology and are now found in almost

every cell phone and other mobile devices. In addition, I am a named inventor on nine U.S. patents pertaining to semiconductor devices and related technology, which are listed in my curriculum vitae, a true and correct copy of which is attached as Appendix A.

8. My research has focused on the design and implementation of integrated circuits and systems, including dynamic random access memory (“DRAM”), CMOS image sensors, mixed-signal circuitry, and high performance image processing systems. Over the course of my work, I have developed and become familiar with a wide range semiconductor manufacturing technology.

9. In addition, I have received numerous honors and awards for my contributions to the electrical engineering industry, including the National Science Foundation Young Investigator Award, Army Young Investigator Award, Hertz Foundation Fellowship, and National Science Foundation Fellowship. I have given numerous presentations and invited lectures, including at the Consumer Electronics Show as Keynote Speaker, at the U.S. Science and Technology Symposium in Computing and Telecommunication, at the National Research Council Workshop on the Electronics Industry, and before the Institute of Electrical and Electronics Engineers (“IEEE”) Laser and Electro Optical Society. I have also been named an IEEE Distinguished Lecturer. In addition, I have been interviewed three times by The EE Times and once by The Weekly Economist.

10. I have also served as a consultant throughout my career. From 1991 to 1993, I advised on the research and development of advanced Complementary-metal-oxide-semiconductor (“CMOS”)/charge-coupled device (“CCD”) technology and circuitry at the Istituto per la Ricerca Scientifica e Tecnologica (IRST), in Trento, Italy. From 1993 to 1998, I served as a consultant for Hamamatsu Photonics, K.K. in Hamamatsu City, Japan, where I helped develop smart image sensors and CMOS/CCD analog charge-domain circuitry.

11. From 1995 to 2000, I worked as a consultant and Senior Fellow at Hyundai Electronics Industries, in Ichon, Korea. At Hyundai, I developed and commercialized high performance CMOS image sensor technology for embedded image sensing and processing applications and researched advanced Dynamic Random Access Memory (“DRAM”) design and merged memory logic (MML) technology for advanced computer systems. From 1998 to 2001, I served as a member of the Science and Technology Board for Polaroid Corporation, where I evaluated Polaroid’s research and technology developments.

12. In 2000 I founded a company called Silicon7, Inc. Silicon7 was located in Seongnam-si, Kyoungki-do, Korea, and developed application-specific memory products for mobile communications and computing platforms. For example, we developed 4-Mbit and 8-Mbit pseudo SRAMs which featured a 70-nanosecond access time and ultra low power consumption that were targeted for mobile

applications such as handsets and personal digital assistant. These advanced memory components and systems were optimized for the distinct requirements of mobile communication devices.

13. I am also an author (or co-author) of many publications, including:

- “The New Economics of Semiconductor Manufacturing,” IEEE Spectrum, vol. 45, issue 5, pp. 24-29 (May 2008);
- “A Low-Power 256-Mb SDRAM with an On-Chip Thermometer and Biased Reference Line Sensing Scheme,” IEEE Journal of Solid-State Circuits, vol. 38, no. 2, pp. 329-337 (February 2003);
- “An Antifuse EPROM Circuitry Scheme for Field-Programmable Repair in DRAM,” IEEE Journal of Solid-State Circuits, vol. 35, no. 10, pp. 1408-1414, (October 2000);
- “An Improved Digital CMOS Imager,” IEEE Workshop on Charged-Coupled Devices and Advanced Image Sensors, Nagano, Japan (June 1999);
- “A Linear-Response, High-Dynamic Range CMOS Imager Suitable for Spectroscopic Applications,” IEEE Workshop on Charged-Coupled Devices and Advanced Image Sensors, Nagano, Japan (June 1999);

- “An Integrated 800 x 600 CMOS Imaging System,” Digest of Technical Papers of IEEE International Solid-State Circuits Conference, pp. 304-305 (February 1999);
- “A CCD/CMOS Image Sensor Array with Integrated A/D Conversion,” Proceedings of the IEEE International Symposium on Circuits and Systems, vol. 3, pp. 1908-1911 (June 1997);
- “Neuromorphic CMOS Circuitry for Active Bidirectional Delay Lines,” Proceedings of IEEE International Symposium on Circuits and Systems, vol. 3, pp. 473-476 (May 1996);
- “A CCD/CMOS Image Motion Sensor,” Digest of Technical Papers of IEEE International Solid—State Circuits Conference, pp. 194-195 (February 1993);
- “The MIT Vision Chip Project: Analog VLSI Systems for Fast Image Acquisition and Early Vision Processing,” Proceedings of the International Conference on Robotics and Automation, vol. 2, pp. 1330-1335 (April 1991);

- “Optimization of Low Pressure Nitridation/Oxidation of SiO₂ for Scaled MOS Devices,” IEEE Transactions on Electron Devices, vol. ED-35, no. 7, pp. 935-944 (July 1988);
- “MOS Electrical Characteristics of Low Pressure Re—oxidized Nitrided Oxide,” Technical Digest of International Electron Devices Conference, pp. 668-671 (December 1986); and
- “Hot Carriers Induced Degradation in Thin Gate Oxide MOSFETs,” Technical Digest of International Electron Devices Conference, pp. 186-189, (December 1983).

III. MY ASSIGNMENT AND BASES OF OPINIONS

14. I have been asked to provide my opinions as to the scope and content of the '806 patent as well as the prior art presented by Petitioner in the Petition and Dr. Lee. Specifically, I have been asked to opine on what a person of ordinary skill in the art would have understood the '806 patent to disclose, and I have been asked to provide my opinions concerning whether Toyama (Ex. 1005) discloses or renders obvious claim 10 of the '806 patent.

15. In the course of conducting my analysis and forming my opinions, I have reviewed the references and materials cited in the Petition, Preliminary Response, and herein including those listed below:

Exhibit No.	Reference
N/A	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00791, Paper 1)
Ex. 1001	U.S. Patent No. 10,937,806 B2 to Tao et al.
Ex. 1002	File History of U.S. Patent No. 10,937,806 B2 to Tao et al.
Ex. 1003	Declaration of Dr. Jack Lee (“Lee”)
Ex. 1004	<i>Curriculum Vitae</i> of Dr. Jack C. Lee
Ex. 1005	U.S. Patent Publ. No. 2017/0179026 A1 (“Toyama”)
Ex. 1009	CN109075169A Office Action, dated November 14, 2019
Ex. 1010	Certified Translation of CN109075169A Office Action, dated November 14, 2019
Ex. 1011	CN109075169A Reexamination Decision, dated November 25, 2021
Ex. 1012	Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021
Ex. 1013	Michelsoni, “3D Flash Memories” (2016)
Ex. 1014	Aritome, “NAND Flash Memory Technologies” (2016)
Ex. 1015	U.S. Patent Publ. No. 2018/0108671 A1 to Yu et al.
Ex. 1016	U.S. Patent Publ. No. 2019/0229125 A1 to Zhou et al.
Ex. 1017	U.S. Patent No. 10,354,980 B1 to Mushiga et al.
Ex. 1018	U.S. Patent No. 9,293,348 to Lai et al.
Ex. 1019	U.S. Patent No. 8,598,643 B2 to Kawasaki et al.
Ex. 1020	U.S. Patent No. 8,697,519 to Jee et al.
Ex. 1021	Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)
Ex. 1022	Print out of https://www.studycountry.com/wiki/what-is-a-piece-ofland-surrounded-by-water-on-2-sides
Ex. 1023	Michelsoni et al., “Inside Solid State Drives (SSDs)” (1st Ed. 2013)
Ex. 1024	U.S. Patent No. 10,043,558 to Shah et al.
Ex. 1025	Michelsoni et al., “Inside NAND Flash Memories” (2010)
Ex. 1026	Lau, “Ball Grid Array Technology” (1995)
Ex. 1027	U.S. Patent No. 10,103,169 to Ge et al.
Ex. 1028	U.S. Patent No. 9,935,050 to Dunga et al.
Ex. 1029	Chang, “ULSI Technology” (1996)
Ex. 1030	Chen, “CMS Devices & Technology for VLSI” (1988)
Ex. 1031	Jaeger, “Volume V: Introduction to Microelectronic Fabrication” (1988)
Ex. 1032	U.S. Patent No. 5,776,808 to Muller et al.
Ex. 1033	U.S. Patent No. 9,236,393 to Cernea

Ex. 1034	Capogreco et al., “Integration and electrical evaluation of epitaxially grown Si and SiGe channels for vertical NAND Memory applications,” 2015 IEEE International Memory Workshop, 2015
Ex. 1035	Kim et al., “Three-Dimensional NAND Flash Architecture Design Based on Single-Crystalline Stacked Array,” IEEE Transactions on Electron Devices, Vol. 59, No. 1, Jan. 2012, pp. 35-45
Ex. 1036	Wagner, “The Use of HBr in Polysilicon Etching,” Gases & Instrumentation International, Vol. 7, Issue 4, July/August (2013) printed from https://www.pall.com/content/dam/pall/microelectronics/literaturelibrary/non-gated/HBr_Polysilicon.pdf
Ex. 1037	Baker, “CMOS Circuit Design, Layout, and Simulation,” Third Ed. (2010)
N/A	Patent Owner’s Preliminary Response (IPR2024-00911, Paper 9)
Ex. 2001	Joint Claim Construction Statement
N/A	Decision Granting Institution of <i>Inter Partes Review</i> of U.S. Patent No. 10,937,806 (IPR2024-00911, Paper 12)
Ex. 2002	File History of U.S. Patent No. 10,658,378 B2 to Tao et al.
Ex. 2003	Micron’s Preliminary Claim Constructions
Ex. 2004	YMTC’s Proposed Claim Constructions
Ex. 2006	Deposition Transcript of Dr. Lee
Ex. 2007	U.S. Patent No. 10,559,583 B2 to Park et al. (“Park”)
Ex. 2008	Deposition Transcript of Dr. Lee Regarding U.S. Patent No. 10,658,378 (IPR2024-00788, -00909)

16. My opinions in this declaration are based on my review of these documents, as well as upon my education, training, research, knowledge, and experience.

17. All emphases (such as bolding, underlying, or italics) appearing in quotations and citations cited herein have been added by me, unless otherwise stated.

IV. SUMMARY OF MY OPINIONS

18. It is my opinion that Toyama's second modification of the fourth exemplary structure ("Second Modification") does not disclose or render obvious claim 10 of the '806 patent at least because:

- Toyama's Second Modification does not disclose or render obvious "a plurality of through array contacts (TACs) extending vertically through the dielectric structure," as required by independent claim 8 (from which claim 10 depends).
- Toyama's Second Modification does not disclose or render obvious "a plurality of non-electrically functional channel structures surrounding the TAC region," as required by independent claim 8 (from which claim 10 depends).
- Toyama's Second Modification does not disclose or render obvious "an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures," as required by dependent claim 10.

19. It is my opinion that Toyama's First Exemplary Structure does not disclose or render obvious claim 10 of the '806 patent at least because:

- Toyama's First Exemplary Structure does not disclose or render obvious "a through array contact (TAC) region formed between the first and second channel regions," as required by independent claim 8 (from which claims 9, 11-12 depend).
- Toyama's First Exemplary Structure does not disclose or render obvious "an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures," as required by dependent claim 10.

20. It is my opinion that Toyama's Second Modification in combination with Toyama's First Exemplary Structure does not disclose or render obvious claim 10 of the '806 patent at least because:

- A person of ordinary skill in the art would not have found it obvious to modify Toyama's Second Modification in the proposed manner.
- Toyama's Second Modification in combination with Toyama's First Exemplary Structure does not disclose or render obvious "a plurality of non-electrically functional channel structures surrounding the TAC region," as required by independent claim 8 (from which claim 10 depends).

- Toyama’s Second Modification in combination with Toyama’s First Exemplary Structure does not disclose or render obvious “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures,” as required by dependent claim 10.

V. APPLICABLE LEGAL STANDARDS

21. I am not a legal expert and offer no opinions on the law. However, I have been informed by counsel of the various legal standards that apply, and I have applied those standards in arriving at my conclusions.

A. Claim Construction

22. I was informed, unless otherwise noted, I should give claim terms their ordinary and customary meaning as understood by a person of skill in the art at the time of the invention. I was informed and I understand that the words of the patent’s claims and the context in which the term is used in the claims can be highly instructive in ascertaining the term’s meaning. I further understand that the terms of a claim are to be interpreted in the context of the entire patent, including the patent’s other claims, its specification and its figures.

23. I have been further instructed that a patent’s “prosecution history” may often provide helpful evidence about how the Patent Office and the applicant understood the patent and its claims. Therefore, I have been instructed that claim

terms should also be interpreted in light of the patent's prosecution history. In addition to the claims, the specification, the figures, and the prosecution history, I have been instructed that certain "extrinsic evidence" such as scientific or technical references may also help inform the way in which the person of ordinary skill in the art might understand the claim term. I have been instructed that extrinsic evidence must always be considered in the context of the intrinsic evidence.

B. Anticipation

24. I have been informed by counsel that a patent claim is invalid as anticipated if each element of that claim is present either explicitly or inherently in a single prior art reference. I have also been informed that, to be an inherent disclosure, the prior art reference must necessarily disclose the limitation, and the fact that the reference might possibly practice or possibly contain a claimed limitation is insufficient to establish that the reference inherently teaches the limitation.

C. Obviousness

25. I understand that a claim is unpatentable if it would have been obvious to a person of ordinary skill in the art at the time the invention was made. I understand that a claim could have been obvious from a single prior art reference or from a combination of two or more prior art references. I understand that an obviousness analysis requires an understanding of the scope and content of the prior

art, any differences between the invention and the prior art, and the level of ordinary skill in evaluating the pertinent art.

26. I further understand that a claim would have been obvious if it unites old elements with no change to their respective functions or alters prior art by mere substitution of one element for another known in the field, and that combination yields predictable results. Also, I understand that obviousness does not require physical combination or bodily incorporation, but rather consideration of what the combined teachings would have suggested to persons of ordinary skill in the art at the time of the invention.

27. While it may be helpful to identify a reason for this combination, I understand that there is no rigid requirement of finding an express teaching, suggestion, or motivation to combine within the references. When a product is available, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation, obviousness likely bars its patentability. For the same reason, if a technique has been used to improve one device and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious. I understand that a claim would have been obvious if a person of ordinary skill in the art would have had

reason to combine multiple prior art references or add missing features to reproduce the invention recited in the claims.

28. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the invention, the failure of others to make the invention, praise of the invention by those having ordinary skill in the art, and copying of the invention by others in the field. I understand that there must be a nexus, that is, a connection, between any such secondary considerations and the invention.

29. I understand that in considering obviousness, it is important not to determine obviousness using the benefit of hindsight derived from the patent being considered.

D. Claim Dependency

30. I understand that a patent may include two types of claims, independent claims and dependent claims. An independent claim stands alone and includes only the limitations it recites. A dependent claim can depend from an independent claim or another dependent claim. I understand that a dependent claim includes all the

limitations that it recites in addition to all of the limitations recited in the claim from which it depends.

VI. THE '806 PATENT

A. Overview of the '806 Patent

31. The claimed invention of the '806 is directed to a “three-dimensional (3D) memory device” and related methods that address issues arising from the fabrication techniques known in the prior art and, as a result, “simplif[y] the fabrication process and reduce[] the fabrication cost.” '806, Abstract, 18:41-46.

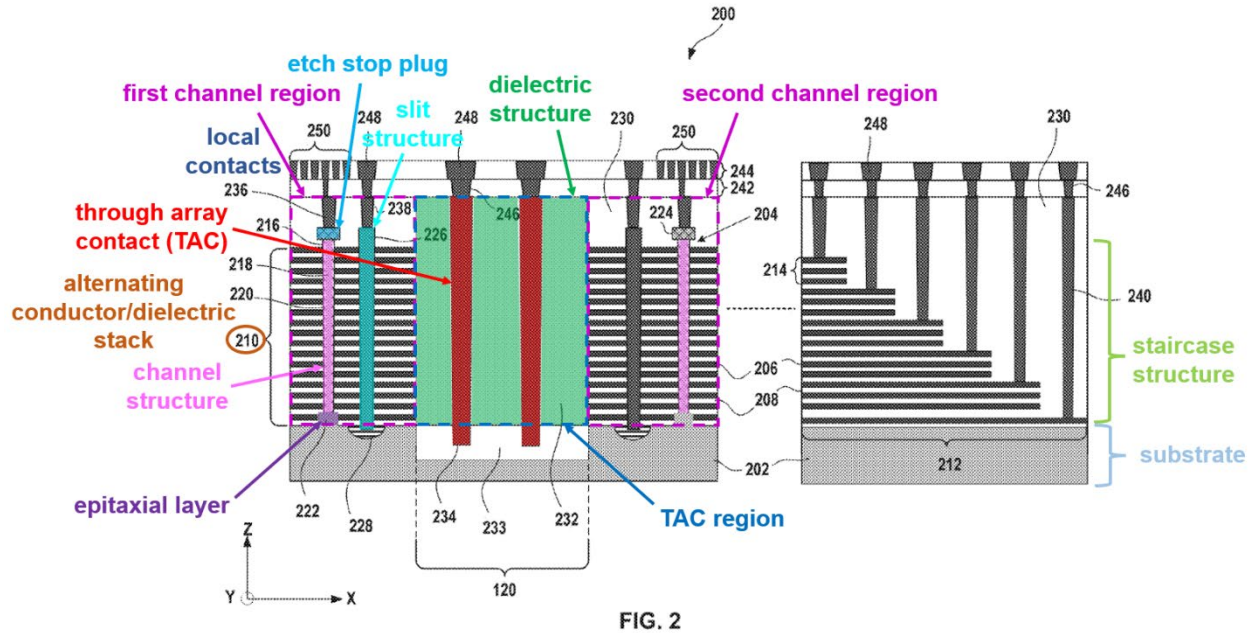
32. Specifically, the '806 is directed to an improved 3D memory device and methods for forming such a device in which a plurality of “through array contacts (TACs)” “extend vertically through” the “dielectric structure,” which hosts a “TAC region.” '806, Abstract, 6:17-20, 10:61-63, 21:20-28. 3D memory devices in the prior art at the earliest claimed priority date of the '806 involved through array vias that form connections between various components of the device to reduce size and increase density. '806, 1:24-36. These vias were placed within the alternating dielectric and conductive layers, which required a complex etching process and “increase[d] the fabrication cost.” '806, 10:61-11:4.

33. The novel device the '806 teaches and recites in the Challenged Claim is characterized by a plurality of **TACs** that “extend vertically through” the “**dielectric structure**” and are positioned within a “**TAC region.**” '806, Abstract,

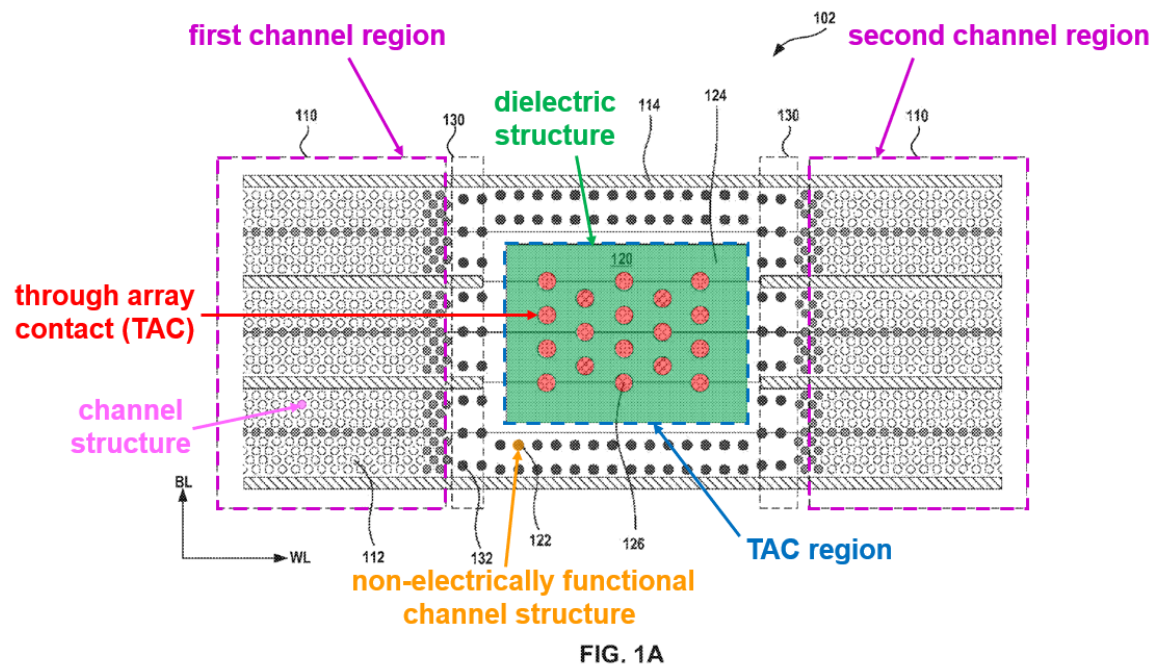
6:17-20, 10:61-63, 21:20-28, Claim 8. The **TAC region** can be between “**first and second channel regions**” comprising “**channel structures**.” *Id.* This novel configuration of elements allows for easier and less costly manufacture of 3D memory devices and achieves shorter interconnect routing. ’806, 5:61-65, 11:8-10, 18:32-38, 20:33-41.

34. A representative embodiment of the ’806’s memory device includes: (1) “**alternating conductor/dielectric layer stack 210**” (’806, 8:23-31); (2) “**dielectric structure 232**” (’806, 10:23-34); (3) “**channel structures 216**” and “**slit structures 226**” extending vertically through “**alternating conductor/dielectric layer stack 210**” (’806, 9:7-12, 10:6-11); (4) “**staircase structure 212**” (’806, 8:54-61); (5) “**local contacts**” on “**channel structures 216**” and “**slit structures 226**” (’806, 11:28-30); (6) “**TACs 234**” extending vertically through “**dielectric structure 232**” (’806, 10:62-64, 20:49-52); (7) “**first and second channel regions**” and a “**TAC region 120**” between them (’806, 6:4-11, Fig. 2, Claim 8); (8) “**non-electrically functional channel structures 122**” surrounding the “**TAC region 120**” and between “**first and second channel regions**” (’806, 6:22-29, Fig. 1A, Claim 8); (9) a “**substrate 202**” (’806, 7:13-35, Fig. 2); (10) an “**etch stop plug 224**” between each “**local contact**” and each “**channel structure 216**” (’806, 9:36-53, Fig. 2); and (11) an “**epitaxial layer 222**” between “**substrate 202**” and “**channel structures**”

216" ('806, 9:36-40, Fig.2). Vertical and horizontal cross-section views of the memory device are below.



'806, Fig. 2 (annotated).



'806, Fig. 1A (annotated).

B. Listing of the Challenged Claims

35. For reference, claim 10 (“Challenged Claim”) of the ’806 Patent and claim 8, from which it depends, are reproduced below:

[8.pre] A three-dimensional (3D) memory device, comprising:

[8.a] an alternating conductor/dielectric layer stack;

[8.b] a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;

[8.c] first and second channel regions comprising first and second pluralities of channel structures, respectively;

[8.d] slit structures extending vertically through the alternating conductor/dielectric layer stack;

[8.e] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[8.f] local contacts disposed on the first and second channel structures and the slit structures;

[8.g] a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and

[8.h] a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.

[10.pre] The 3D memory device of claim 8, further comprising:

[10.a] a substrate;

[10.b] an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and

[10.c] an epitaxial layer disposed between the substrate and the first or second channel structures.

C. File History of the '806 Patent

36. The '806 was filed on May 5, 2020, as a continuation of application no. 16/047,182, filed on July 27, 2018, which was issued as U.S. Patent No. 10,658,378 ("the '378"). The application included 3 independent claims (pending claims 1, 9, and 15) and 17 dependent claims (pending claims 2-8 that depended from pending claim 1, pending claims 10-14 that depended from pending claim 9, and pending claims 16-20 that depended from pending claim 15). Ex. 1002, 53-55 (05/05/2020 Claims).

37. In a non-final office action, the Examiner rejected pending claims 1-16 and 18-20 under 35 U.S.C. §103 as being allegedly obvious over U.S. Patent No. 9,659,956 ("Pachamuthu") in view of U.S. Patent Publication No. 2017/0186758 ("Lee"), and rejected pending claim 17 under 35 U.S.C. §103 as being allegedly obvious over these two references in further view of U.S. Patent Publication No. 2017/0365613 ("Gunji-Yoneoka"). Ex. 1002, 104-112 (06/23/2020 Office Action).

38. In a response, Applicant amended pending independent claims 1, 9, and 15 "[w]ithout acquiescing to the propriety of the rejection" to "recite features that further distinguish itself from the applied references." Ex. 1002, 128-137 (10/21/2020 Amendment and Reply). Applicant also canceled pending dependent claims 3, 11, and 17. *Id.* Having placed the independent claims in allowable form,

Applicant requested that their respective dependent claims also be allowed. *Id.* Applicant further added three new claims that depend from the three pending independent claims. Ex. 1002, 128-137 (10/21/2020 Amendment and Reply). The Examiner subsequently allowed all pending claims. Ex. 1002, 147-154 (12/16/2020 Notice of Allowance). The '806 issued on March 2, 2021 with twenty claims, including the renumbered independent claims 1, 8, and 13. Ex. 1002, 169 (02/10/2021 Issue Notification).

39. With the original filing of the '806, Applicant filed an information disclosure statement (IDS) that notified the Examiner of U.S. Patent Publication No. 2017/0179026 ("Toyama"). Ex. 1002, 81 (05/05/2020 Information Disclosure Statement). The Examiner considered Toyama and explicitly cited it as a "reference[] considered." Ex. 1002, 124 (06/23/2020 List of References Cited by Applicant and Considered by Examiner). In addition, the '806 and its parent, the '378, share the same Examiner (Calvin Y. Choi), who was presented with Toyama during the prosecution of the '378 in an IDS with Toyama alone (Ex. 2005, 555 (12/03/2019 Information Disclosure Statement)) and considered it (Ex. 2005, 593 (01/13/2020 List of References Cited by Applicant and Considered by Examiner)). I disagree with Petitioner's assertion that "Patent Owner only gave Examiner a haystack" because Applicant submitted an IDS solely to cite Toyama during the application of the parent, which was then explicitly considered by the Examiner, then submitted an

IDS citing Toyama again during the application of the '806. The Examiner, who was already familiar with Toyama even before the '806 was filed, explicitly considered Toyama again during the prosecution of the '806 application.

40. Moreover, the '806 was issued with nineteen references (twelve U.S. patent documents and seven foreign patent documents)—one of which is Toyama. '806, (56). Thus, the Examiner considered Toyama twice—once for the '378 and again when subsequently examining the '806 at issue here—but found it lacking.

VII. LEVEL OF ORDINARY SKILL IN THE ART

41. My opinions in this declaration are based on the understandings of a person of ordinary skill in the art, which I understand is sometimes referred to as an “ordinary artisan” or by the acronyms “POSITA” (person of ordinary skill in the art) or “POSA,” as of the time of the invention.

42. I have been asked to consider the level of ordinary skill that someone in the field of technology of the '806 patent would have had at the time the claimed invention disclosed in the '806 patent was made. In determining the level of ordinary skill in the art, I considered the following: (1) the levels of education and experience of persons working in the field; (2) the types of problems encountered in the field; and (3) the sophistication of the technology.

43. In my opinion, a person of ordinary skill in the art capable of reading and understanding the claims of the '806 patent at the time of the invention would have had at least a bachelor's degree in electrical engineering, materials science, or a similar discipline, along with at least 2 years of professional experience in semiconductor fabrication process integration for memory devices or an equivalent level of knowledge and experience. For example, an advanced degree may replace some of the professional experience, or extensive experience may replace some of the educational requirements.

44. In this case, Dr. Lee has asserted in his declaration that a person of ordinary skill in the art at the time of the invention described in the '806 patent:

would have had a bachelor of science degree in electrical engineering or a similar discipline, along with 2-3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).

Lee, ¶37.

45. In view of my educational background and years of experience, including my many years of experience designing high performance integrated circuits and developing advanced semiconductor manufacturing process technology for advanced DRAM, CMOS image sensors, and NAND flash, I both met and exceeded the qualifications of a person of ordinary skill in the art as of the earliest possible priority date of the '806 Patent in May 2018. That is true under both my

own definition of a person of ordinary skill in the art, as well as under Dr. Lee's definition, and my opinions as set forth herein are the same regardless of which definition of a person of ordinary skill in the art is applied.

VIII. CLAIM CONSTRUCTION FOR THE '806 PATENT

46. I have been asked to opine on the scope and content of the '806 patent and what a person of ordinary skill in the art would have understood the '806 patent to disclose and teach as it relates to the term "each local contact of the local contacts."

A. "each local contact of the local contacts" (Claim 10)

47. The term "each local contact of the local contacts" of claim 10 should be construed, according to its plain and ordinary meaning, as referring to the "local contacts disposed on the first and second channel structures *and the slit structures*" as recited in independent claim 8, from which claim 10 depends. In my opinion, the Board should reject Petitioner's attempt to limit "each local contact of the local contacts" to only some of the claimed local contacts—those disposed on the channel structures.

48. My opinion is that Patent Owner's proposed construction is the only one consistent with the claim language. Claim 10 recites "each local contact of the local contacts" (limitation [10.b]), and the antecedent basis for this term is independent claim 8's recitation of "local contacts disposed on the first and second channel structures and the slit structures" (limitation [8.f]). Moreover, there is

nothing in the phrase “each local contact of the local contacts” to limit it to merely a subset of the previously recited local contacts. Thus, “**each** local contact of the local contacts” refers to **all** of the local contacts that are mapped to satisfy the “local contacts” of limitation [8.f], including those above the slit structures as well as those above the channel structures.

49. Petitioner’s argument that “each local contact of the local contacts” as recited in limitation [10.b] refers to only the “local contacts disposed on the first and second channel structures” and not the “local contacts disposed on ... the slit structures” (Prelim. Reply, 1) is contrary to the express language of the claim and ignores the antecedent basis for the term. To satisfy claim 10, which recites “***an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures,***” it is not sufficient to show an etch stop plug interposed between “***some*** local contacts” of the local contacts and each channel structure of the first and second channel structures—rather claim 10 recites “**each** local contact.” Petitioner’s interpretation, therefore, improperly reads out the term “each.”

50. In arguing for its construction, Petitioner mischaracterizes Patent Owner’s position as requiring “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures ***[and each of the slit structures]***.” Prelim. Reply, 3-4. Patent

Owner proposes no such additional limitation. Claim 10 requires an etch stop plug located between two things: (1) each local contact of the local contacts and (2) each channel structure of the first and second channel structures. The parties are in agreement regarding the scope of (2)—i.e., the channel structures. Instead, it is the scope of “each local contact of the local contacts” that is at issue. The antecedent for this term supports Patent Owner’s construction, and so no modification of the claim language of claim 10 is necessary (unlike Petitioner’s construction).

51. Petitioner argues that the claim language supports its construction because the etch stop plug of claim 10 is “between” the local contacts and the channel structures, which is “referring to an area for the etch stop that is above the channel structure and beneath the local contact” (Prelim. Reply, 4), but this argument is based on an incorrect assumption that it is not possible to have an etch stop plug between the channel structures and the local contacts disposed on the slit structures. Similarly, Petitioner incorrectly argues that the claims require that “[o]nly the local contacts for the channel structures are above the channel structures.” Prelim. Reply, 4. The claims never recite this limitation—nor is there any support for reading such a negative limitation into the claims. There is nothing precluding a local contact from being above both the channel structures and the slit structures.

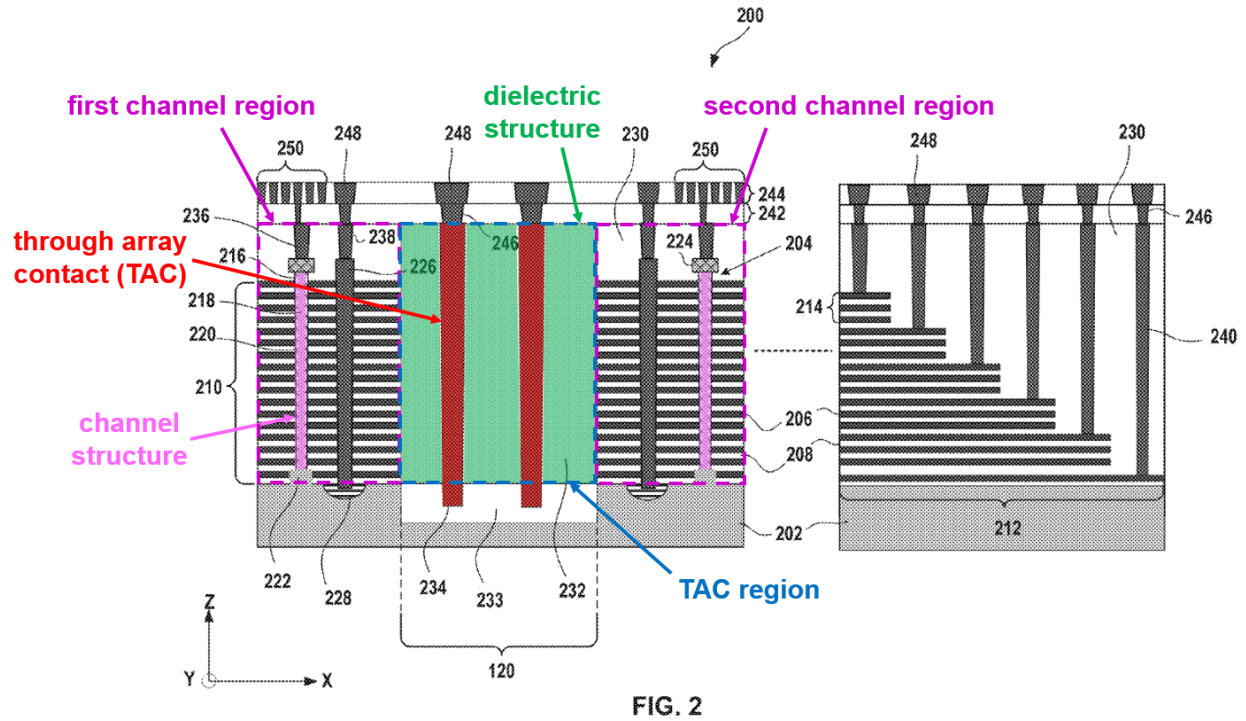
52. As one example of a structure that would be consistent with claim 10 as properly construed, a “local contact” may be disposed on both a channel structure

and a slit structure, with an etch stop plug in between the local contact and the channel structure. Limitation [8.f], which introduces the term “local contact,” recites “local contacts disposed on the first and second channel structures and the slit structures,” which does not require a local contact to be disposed *only* on a channel structure or *only* a slit structure—it may be disposed on both.

53. The ’806 specification provides such examples (discussed below), and does not limit the meaning of the term “local contact” to exclude local contacts that are disposed on both a channel structure and a slit structure. The ’806 does not expressly define the term “local contact,” but provides several examples of local contacts. ’806, 11:24-28, 11:31-34. The closest the ’806 comes to a definition of “local contact” is as follows:

The contacts are referred to herein as “local contacts” because they are in direct contact with the memory array structures, and further because they are formed within dielectric layer 230. ... As used herein, the term “contact” can broadly include any suitable types of interconnects including vertical interconnect access (via) lines and lateral lines (interconnect lines).

’806, 11:24-34. However, this passage does not define the outer boundaries of the term “local contact” because the ’806 also describes **TACs 234** as local contacts (’806, 11:30-31) even though they are formed in **dielectric structure 232** instead of dielectric layer 230.



'806, Fig. 2 (annotated). Furthermore, as the above quote indicates, “contacts” can be “lateral lines (interconnect lines)” and thus a local contact may be disposed on two or more “memory array structures” such as channel structures and slit structures. For example, the '806 discloses such lateral contacts in the form of “interconnect contacts 248,” e.g., “bit lines 250, which are electrically connected to NAND strings” (channel structures) in the NAND string region. '806, 12:7-12. As illustrated in the figure below, which has been annotated to show an example bit line, a bit line extends along the “bit line (BL) direction” in the NAND string region 110 and therefore is disposed on channel structures as well as slit structures. (The precise placement of the bit line in the NAND string region does not matter because the

location of the slit structures and channel structures means that the bit lines will be disposed over both.) '806, 5:66-6:4.

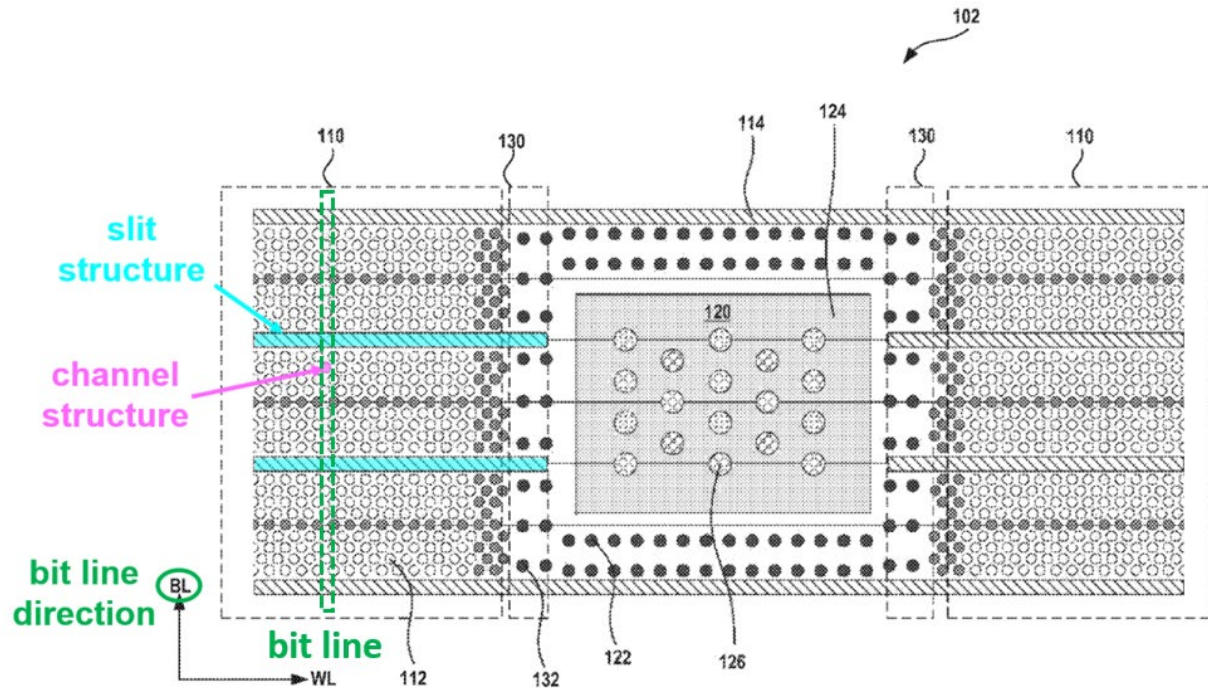


FIG. 1A

'806, Fig. 1A (annotated).

54. Dr. Lee's testimony regarding the related '378, which shares the same specification, also confirms that an interconnect such as a bit line is a local contact in the context of the specification:

So in column 11 line 15, around 15, it says that *local contact is essentially provide [sic] a conducting layer with memory array structures*, such as the NAND string 204, S-T-R-I-N-G-S, 204, slit structures 226, conductive layer

or word line 206, and the staircase structure 212. So *the local contact basically is an interconnect to connect the memory array structure to, for example, external – external input, outputs.*

Ex. 2008, 66:11-14 (emphasis added).

55. For all of these reasons, the Board’s preliminary conclusion in its Decision on Institution that “the plain and ordinary meaning of ‘each local contact’ recited in claim 10 ... refer[s] to each channel structure local contact and not to each slit structure local contact” (DI, 12) is inconsistent with the claims and specification. Specifically, the Board repeatedly assumed that there must be two separate types of local contacts—“slit structure local contacts” and “channel structure local contacts” (DI, 12)—even though those terms are not recited in the claims, and the Board did not consider that the above-described lateral local contacts located above *both* the slit and channel structures, as disclosed in the specification, would be consistent with the claims. Similarly, the Board incorrectly concluded that “the slit structure local contact is not located above a channel structure,” which again wrongly assumes that there must be separate “slit structure local contacts” and “channel structure local contacts.” A local contact located on a slit structure may also be located on a channel structure, as illustrated above.

56. Accordingly, the term “each local contact of the local contacts” of claim 10 should be construed, according to its plain and ordinary meaning, as referring to

the “local contacts disposed on the first and second channel structures and the slit structures,” as recited in claim 8.

IX. THE ASSERTED PRIOR ART

A. U.S. Patent Publication No. 2017/0179026 (“Toyama”) (Ex. 1005)

57. Petitioner does not argue that Toyama anticipates the Challenged Claim, and instead argues only that it renders obvious the Challenged Claim in view of the knowledge of a person of ordinary skill in the art. Pet. 7, 27-122.

58. Toyama teaches a 3D NAND memory device with four exemplary structures and their modifications. Ex. 1005, [0004]. Only two of these exemplary structures are relied on by Petitioner: (1) Toyama’s “second modification of the fourth exemplary structure,” illustrated in Figures 44A-B to 49, and (2) Toyama’s “first exemplary structure,” illustrated in Figures 1A-B to 17A-F. Pet. 7.

59. Toyama’s second modification of the fourth exemplary structure includes, among other elements: “**semiconductor substrate 9**” (Ex. 1005, [0163]); “**planar semiconductor material layer 10**” (Ex. 1005, [0170]); “**alternating stack (132, 146, 232, 246)**” (Ex. 1005, [0232]); “**channels**” (Ex. 1005, [0211]); “**laterally-elongated contact via structures 76**” (Ex. 1005, [0236]); “**drain contact via structures 88**” (Ex. 1005, [0241]); “**insulating liners 674**” (Ex. 1005, [0340]); and “**through-memory-level via structure 676**” (Ex. 1005, [0341]). A cross-section view of Toyama’s second modification of the fourth exemplary structure is below.

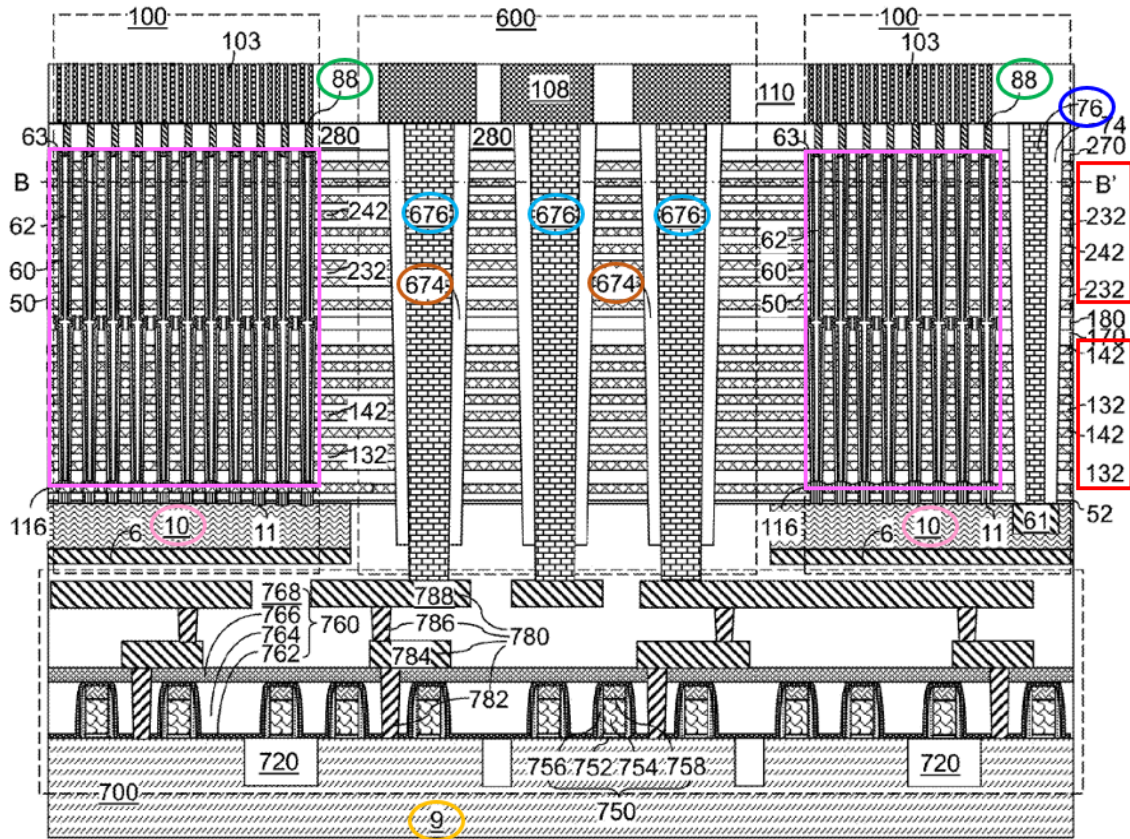


FIG. 49

Ex. 1005, Fig. 49 (annotated). (Note that Petitioner states: “In a clear typographical error, Figure 49 labels its alternating conductor/dielectric layer stack as elements 132, 142, 232, 242. Elements 142, 242 are ‘sacrificial material layers’ which, in a process step prior to Figure 49, were removed and replaced with ‘electrically conductive layers (146, 246).’ Toyama, [0337], [0340].” Pet. 39. I do not challenge this statement for purposes of this declaration.)

60. In Toyama's second modification of the fourth exemplary structure, **through-memory-level via structures 676** are not formed through a dielectric structure; instead, they are formed through **alternating stack (132, 146, 232, 246)**.

where layers 146 and 246 are conductive, and as a result, they require separate **insulating liners 674** around each individual **through-memory-level via structure 676**. Before the **through-memory-level via structures 676** are deposited, the through-memory-level openings 679 (which are formed in dense portions of the alternating stack in the memory region) and backside contact trenches 79 are used to introduce etchants that etch the sacrificial material layers (142, 242) and conductive material to form electrically conductive layers (146, 246). Ex. 1005, [0337].

61. Toyama's first exemplary structure includes, among other elements: "**semiconductor substrate 9**" (Ex. 1005, [0163]); "**planar semiconductor material layer 10**" (Ex. 1005, [0170]); "**alternating stack (132, 146, 232, 246)**" (Ex. 1005, [0232]); "**channels**" (Ex. 1005, [0211]); "**laterally-elongated contact via structures 76**" (Ex. 1005, [0236]); "**drain contact via structures 88**" (Ex. 1005, [0241]); "**source connection via structures 91**" (Ex. 1005, [0250]); "**dielectric fill material portion 430**" (Ex. 1005, [0216]); and "**through-memory-level via structures 488**" (Ex. 1005, [0244]). A cross-section view of Toyama's first exemplary structure is below.

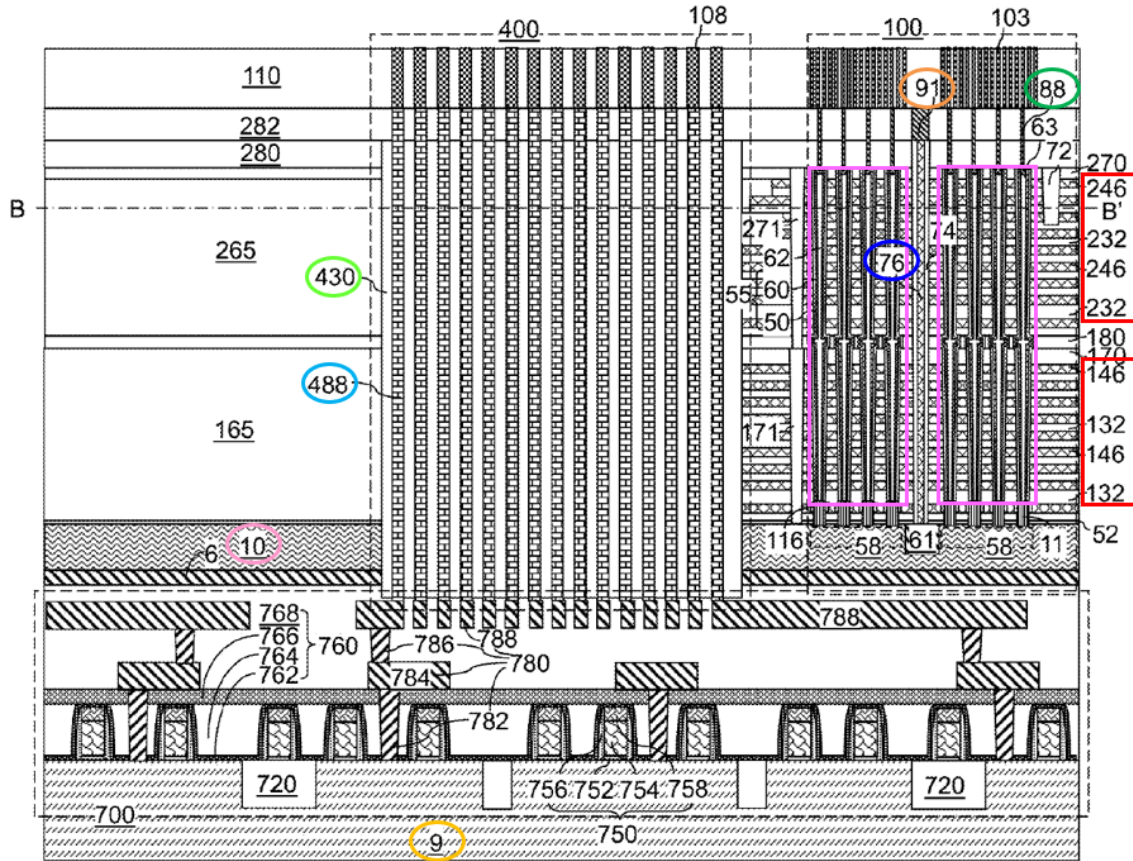


FIG. 17A

Ex. 1005, Fig. 17A (annotated).

62. In Toyama's first exemplary structure, **dielectric fill material portion 430** hosts **through-memory-level via structures 488** to form vertical interconnects; however, Toyama's first exemplary structure lacks two regions with channel structures on opposite sides. Instead, **dielectric fill material portion 430** is formed in a staircase region and therefore has **channels** on one side only. As Toyama explains, the through-memory-level via region 400 (in which the through-memory-level via structures 488 are formed) "is located on a *lengthwise end* of the second block B2 and between a staircase region of the first block B1 and a staircase region

of the third block B3.” Ex. 1005, [0252], Fig. 17B. Figure 17A likewise shows that the **dielectric fill material portion 430** is located at the end of the staircase region of the device. In this location, the openings for **through-memory-level via structures 488** are not used in the replacement process to form electrically conductive layers (146, 246).

X. PETITIONER’S GROUND 1: TOYAMA’S SECOND MODIFICATION DOES NOT DISCLOSE OR RENDER OBVIOUS CLAIM 10

63. For the reasons explained below, it is my opinion that Toyama’s Second Modification does not disclose or render obvious the Challenged Claim at least because Toyama’s Second Modification does not disclose or render obvious multiple elements of claim 8 (from which claim 10 depends) and claim 10. For example, Toyama’s Second Modification does not disclose or render obvious “*a plurality of through array contacts (TACs) extending vertically through the dielectric structure*” as required by limitation [8.g] because Toyama’s alleged plurality of TACs does not extend vertically through any one purported dielectric structure. I have been informed and understand that multiple alleged occurrences of a claim element (here, Toyama’s multiple separate dielectric liners) cannot be used to satisfy a limitation that must be satisfied by the same occurrence of the element (here, the claimed plurality of TACs must extend through “the dielectric structure” meaning one specific dielectric structure). Toyama’s Second Modification also does not

disclose or render obvious “*a plurality of non-electrically functional channel structures surrounding the TAC region*” as required by limitation [8.h] because Toyama’s alleged non-electrically functional channel structures do not surround the alleged TAC region. Finally, Toyama’s Second Modification does not disclose or render obvious “*an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures*” as required by limitation [10.b] because the alleged etch stop plugs are not interposed between “each” of the local contacts Petitioner mapped to limitation [8.f] and the alleged channel structures.

A. Independent Claim 8: Toyama’s Second Modification Does Not Disclose or Render Obvious “a Plurality of Through Array Contacts (TACs) Extending Vertically Through the Dielectric Structure” (Limitation [8.g])

64. Toyama’s Second Modification does not disclose or render obvious “*a plurality of through array contacts (TACs) extending vertically through the dielectric structure*” as required by limitation [8.g] because Toyama’s alleged TACs do not extend through the same structure (the claimed “dielectric structure”).

65. The Challenged Claim requires “a *plurality* of through array contacts (TACs) extending vertically through *the dielectric structure*”—i.e., the same dielectric structure—but this configuration is not disclosed or rendered obvious by Toyama’s Second Modification. As illustrated below in Toyama’s Fig. 49, Petitioner maps “**insulating liners 674**” of “**through-memory-level via structures**

676” to the claimed “dielectric structure” of the ’806 (Pet. 28-31, 48-50), but this mapping relies on a separate insulating liner (i.e., a separate alleged dielectric structure) for each TAC.

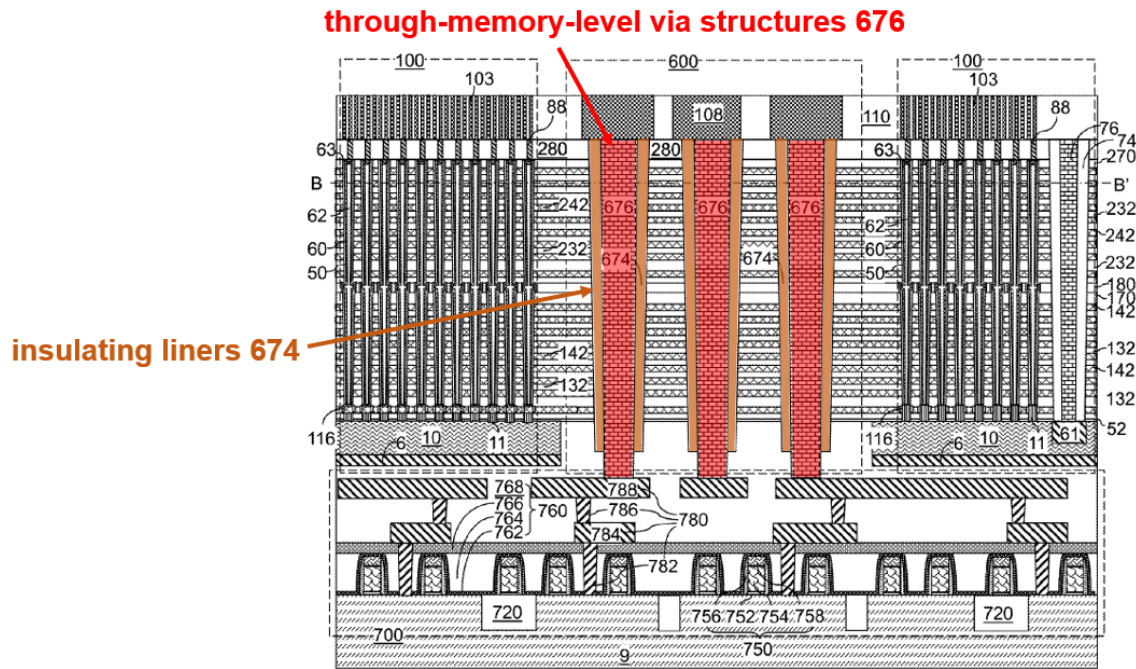


FIG. 49

Ex. 1005, Fig. 49 (annotated by Patent Owner to show Petitioner’s mapping); *see* Pet. 48-50 (using similar annotations but also adding a purple box over the image); Ex. 1005, [0340]-[0341] (explaining that one “through-memory-level cavity 679” is present within each insulating liner 674” for the through-memory-level via structure 676). In other words, only a single “**through-memory-level via structure 676**” (the alleged TAC)—not the claimed plurality of TACs—extends through a given “**insulating liner 674**.” Realizing this problem, Petitioner erroneously attempts to

map multiple insulating liners 674 to a single “dielectric structure.” Pet. 30 (alleging that “these components together are ... a structure”).

66. I disagree with Petitioner’s attempt to rely on separate dielectric structures as a single claimed “dielectric structure.” Specifically, the ’806 claims require that the same “dielectric structure” must have “a *plurality* of through array contacts (TACs) extend[] vertically through” it, which cannot be met by aggregating multiple separate instances of Toyama’s “insulating liner 674.” Thus, I agree with the Board’s preliminary conclusion in its Institution Decision that Toyama’s Second Modification does not show “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” because “Petitioner has not sufficiently shown that Toyama’s three insulating liners are a single dielectric structure.” Pap. 12 (“DI”), 23. In my opinion, Toyama’s Second Modification is akin to the 3D memory devices in the prior art at the earliest claimed priority date of the ’806, which involved through array vias that form connections between various components of the device to reduce size and increase density. ’806, 1:24-36. These vias were placed within the alternating dielectric and conductive layers, which required a complex etching process and “increase[d] the fabrication cost.” ’806, 10:61-11:4.

67. The claim language “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” allows for there to be more than one dielectric structure, but it does *not* mean that more than one dielectric structure

can be combined or otherwise pieced together for any claimed requirements imposed on the claimed “dielectric structure” (singular). Petitioner’s mapping of claim 8 to Toyama ignores this distinction. (To be clear, the claim does not preclude multiple dielectric structures. But the limitation “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” requires that the plurality of TACs extend through at least one particular dielectric structure, regardless of whether additional dielectric structures are also present in the device.)

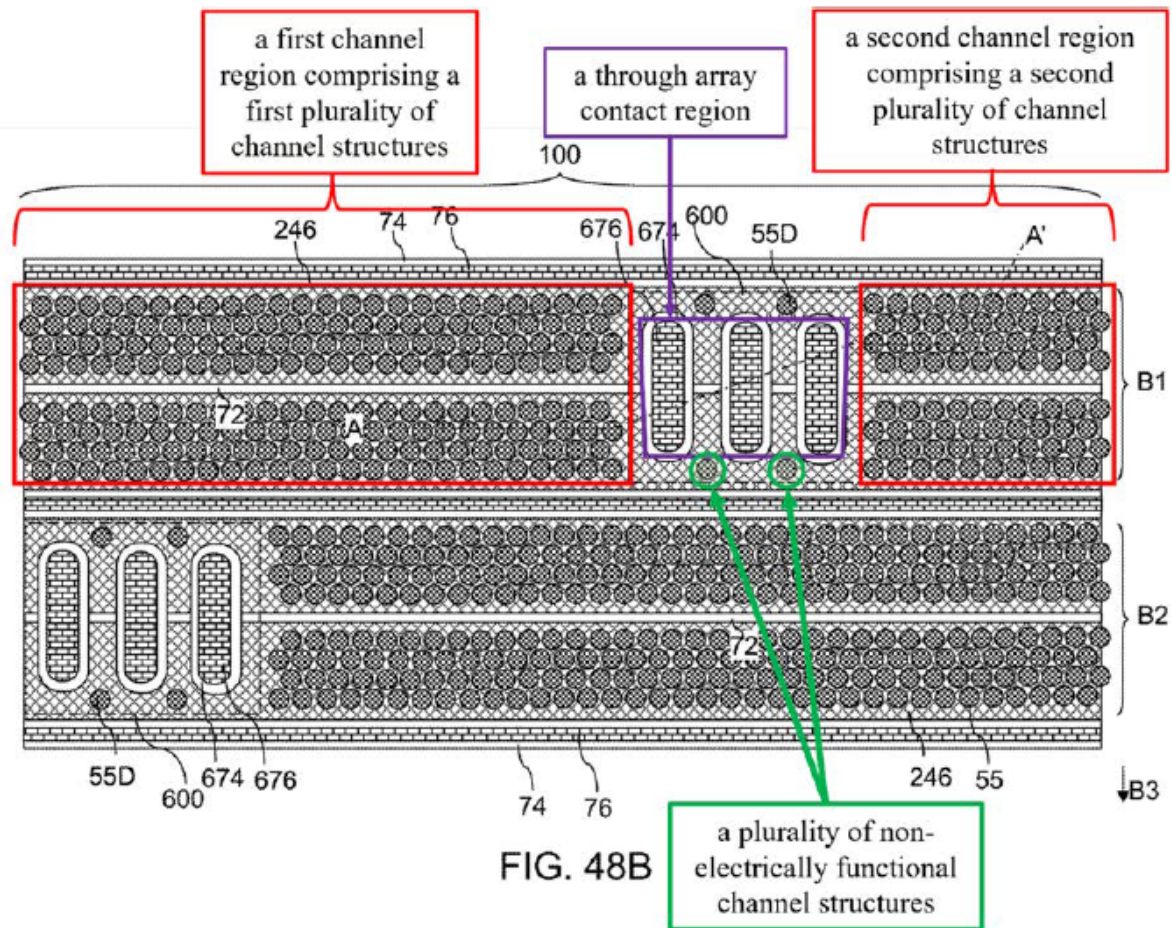
68. Therefore, Petitioner has not shown that Toyama’s Second Modification discloses or renders obvious “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” as required by limitation [8.g].

B. Independent Claim 8: Toyama’s Second Modification Does Not Disclose or Render Obvious “a Plurality of Non-Electrically Functional Channel Structures Surrounding the TAC Region” (Limitation [8.h])

69. Toyama’s Second Modification also does not disclose or render obvious “*a plurality of non-electrically functional channel structures surrounding the TAC region*” as required by limitation [8.h] because Toyama’s alleged non-electrically functional channel structures do not surround the alleged TAC region.

70. As shown below in Figure 48B of Toyama, Petitioner maps Toyama’s “**dummy memory stack structures 55D**” to the claimed non-electrically functional channel structures, but Toyama’s **dummy memory stack structures 55D** do not

“surround” the alleged **TAC region**. While there are two dummy memory stack structures 55D above the alleged TAC region and two below the alleged TAC region, they are positioned in such a way that they, at most, surround one TAC within the alleged TAC region—they do not surround the alleged **TAC region** itself, which is a larger area that extends beyond a single TAC and includes “a plurality of through array contacts (TACs).”



Ex. 1005, Fig. 48B (annotated by Petitioner, Pet. 51).

71. I have not opined on the precise scope of “surrounding” in the claims because under no possible interpretation do Toyama’s dummy memory stack structures 55D surround the alleged TAC region. As discussed, at most they surround one single TAC instead of the claimed “region” that comprises a plurality of TACs.

72. Therefore, Petitioner has not shown that Toyama’s Second Modification discloses or renders obvious “a plurality of non-electrically functional channel structures surrounding the TAC region” as required by limitation [8.h].

C. Claim 10: Toyama’s Second Modification Does Not Disclose or Render Obvious “an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the First and Second Channel Structures” (Limitation [10.b])

73. Toyama’s Second Modification also does not disclose or render obvious “*an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures*” as required by limitation [10.b] because Toyama’s alleged etch stop plugs are not interposed between “**each**” of the alleged local contacts and the alleged channel structures. Indeed, Petitioner’s analysis for dependent claim 10 omits one of the types of structures that Petitioner mapped to the “local contacts” of independent claim 8. This is because those alleged etch stop plugs are plainly not interposed between that purported local contact and the purported channel structures.

74. As I explain in §VIII.A, the plain meaning of the term “each local contact of the local contacts” refers to each of the “local contacts disposed on the first and second channel structures and the slit structures” as recited in limitation [8.f].

75. Petitioner’s mapping for claim 10 in the Petition does not even attempt to address “each local contact.” For independent claim 8, Petitioner contends that Toyama’s “**memory stack structures 55**” are the claimed “first and second channel structures” and “**laterally-elongated contact via structures 76**” are the claimed “slit structures.” Pet. 32-38. Petitioner further alleges that Toyama’s “**drain contact via structures 88**” *and* “**source connection via structures 91**” are the claimed “local contacts disposed on the first and second channel structures and the slit structures.” Pet. 40-44.

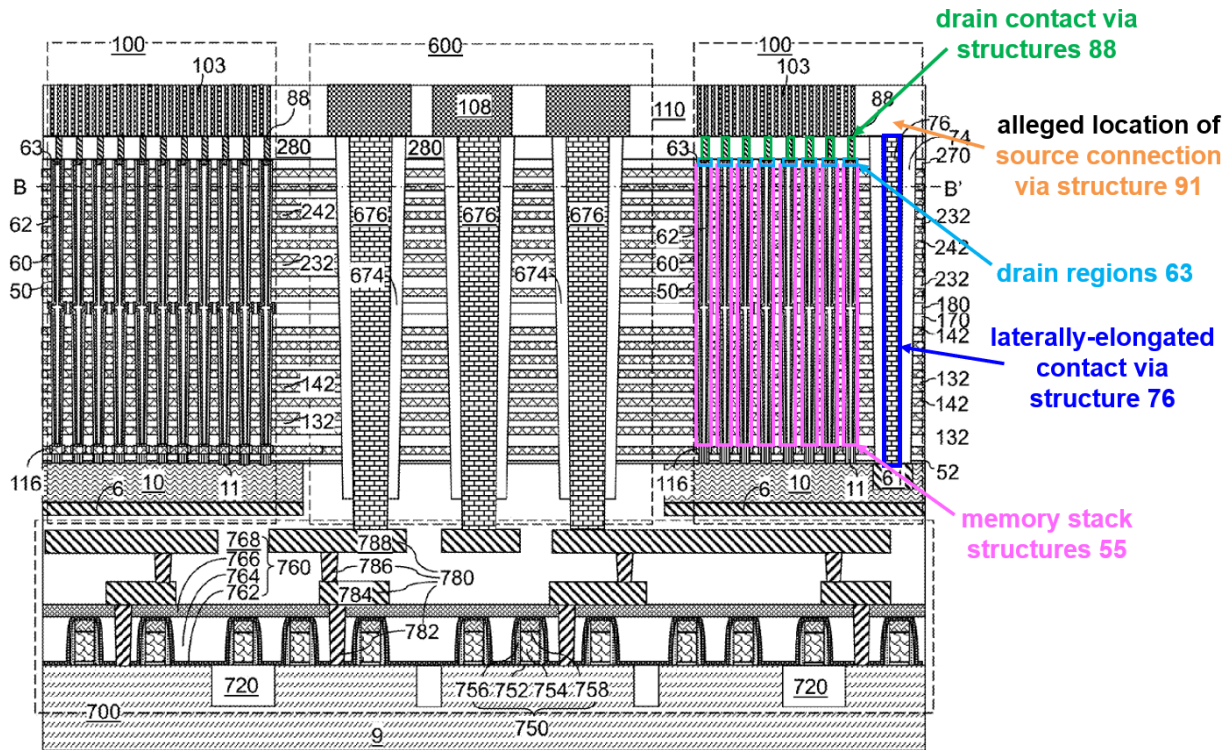


FIG. 49

Ex. 1005, Fig. 49 (annotated by Patent Owner). Although the Petition does not annotate the location of **source connection via structures 91** in Figure 49, Petitioner argues that a person of ordinary skill in the art would have understood **source connection via structures 91** to be disposed on the **laterally-elongated contact via structures 76**, as shown above. Pet. 40-44. (For the purposes of this declaration, I do not dispute Petitioner’s claim that Toyama’s “Second Modification ... would also include ‘source connection via structures’” or that a “POSITA would have found the use of local contacts disposed on the slit structures (‘source connection via structures 91’) obvious.”) Thus, Petitioner has alleged that “**drain contact via structures 88**” are local contacts disposed on the alleged first

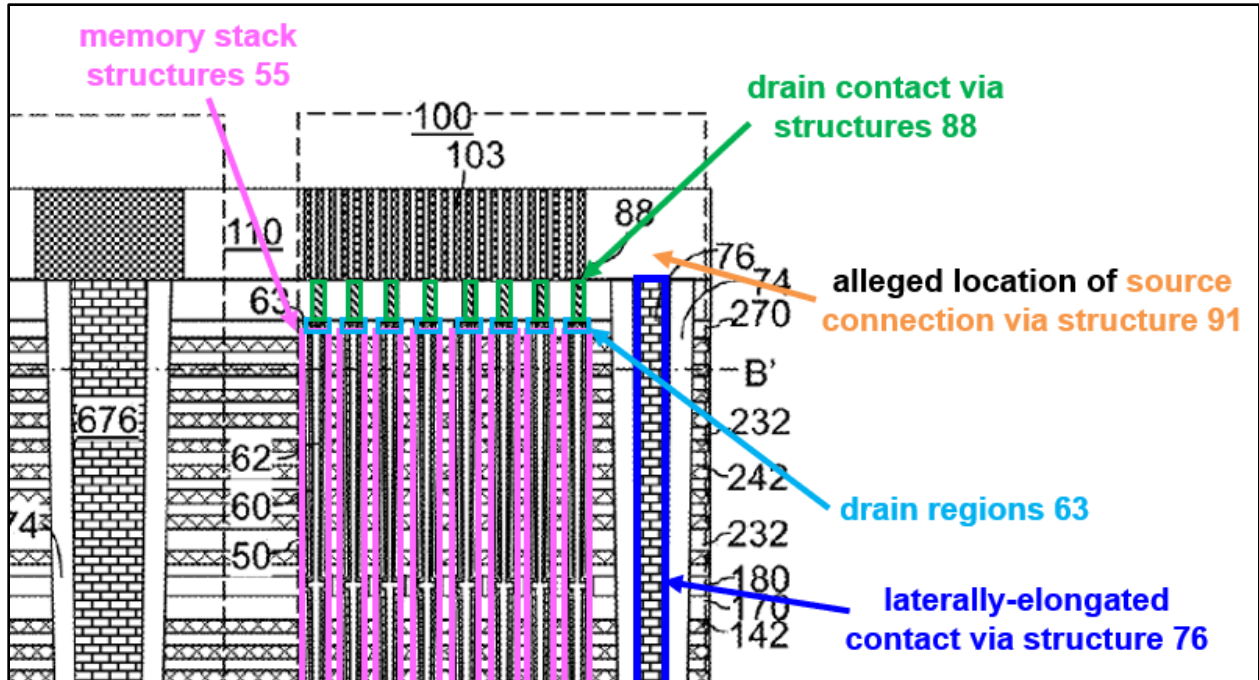
and second channel structures (“**memory stack structures 55**”) and “**source connection via structures 91**” are local contacts disposed on the alleged slit structures (“**laterally-elongated contact via structures 76**”).

76. With regards to claim 10, Petitioner argues that Toyama’s “**drain regions 63**” meet the limitation of “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures” (Pet. 54-59), but Petitioner’s analysis discusses only **drain contact via structures 88** (a subset of the purported local contacts). (For the purposes of this declaration, I do not dispute Petitioner’s claim that “a POSITA would have understood, or at least found obvious, that ‘drain regions 63’ are plugs that serve the purpose of stopping an etch.” Pet. 55.) Petitioner entirely ignores **source connection via structures 91**, which Petitioner mapped to one of the claimed local contacts to meet limitation [8.f].

77. Because claim 10 requires an etch stop plug interposed between **each local contact of the local contacts** and each channel structure of the first and second channel structures, Petitioner was required to identify an etch stop plug that is interposed between the **source connection via structures** (alleged local contacts) and **memory stack structures** (alleged channel structures)—but failed to do so. While Petitioner’s mapping discusses whether there is an etch stop plug interposed between the **drain contact via structures** and the **memory stack structures**,

Petitioner does not even attempt to address whether there is an etch stop plug interposed between the **source connection via structures** and **memory stack structures**. Arguing that Toyama discloses an etch stop plug interposed between the channel structures and some of the purported local contacts that Petitioner mapped to the claimed local contacts is not sufficient. Petitioner simply failed to show that Toyama's Second Modification teaches each element of limitation [10.b].

78. Toyama's alleged etch stop plug, **drain regions 63**, is **not** interposed between **source connection via structures 91** (one of the purported local contacts) and **memory stack structures 55** (the alleged channel structures) as required by claim 10. Indeed, Petitioner has not even alleged that the alleged etch stop plug is between those structures. As shown in Fig. 49 of Toyama annotated below, the **drain regions 63** are, at most, "interposed between" the **drain contact via structures 88** and **memory stack structures 55**. None of the **drain regions 63**, however, is "interposed between" the **source connection via structures 91** and **memory stack structures 55** as required by limitation [10.b]:



Ex. 1005, Fig. 49 (excerpted and annotated by Patent Owner). For limitation [8.f], Petitioner relies on both **drain contact via structures 88** (“local contacts disposed on the first and second channel structures”) and **source connection via structures 91** (“local contacts disposed on...the slit structures”), and *cannot* meet this limitation without relying on both structures. As a result, the alleged etch stop plug of Toyama is not interposed between “each” purported local contact of the local contacts and each purported channel structure of the first and second channel structures as required by limitation [10.b].

79. Therefore, Petitioner has not shown that Toyama's Second Modification discloses or renders obvious limitation [10.b].

**XI. PETITIONER’S GROUND 2: TOYAMA’S SECOND
MODIFICATION DOES NOT DISCLOSE OR RENDER OBVIOUS
CLAIM 10**

80. For the reasons explained below, it is my opinion that Toyama’s First Exemplary Structure does not disclose or render obvious the Challenged Claim at least because Toyama’s First Exemplary Structure does not disclose or render obvious claim 8—the sole challenged independent claim. For example, Toyama’s First Exemplary Structure does not disclose or render obvious “*a through array contact (TAC) region formed between the first and second channel regions*” as required by claim limitation [8.g]. In addition, Petitioner has not shown that Toyama’s First Exemplary Structure discloses or renders obvious “*an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures*” as required by limitation [10.b] because, once again, the alleged etch stop plugs are not interposed between “each” of the local contacts Petitioner mapped to limitation [8.f] and the alleged channel structures.

A. Independent Claim 8: Toyama’s First Exemplary Structure Does Not Disclose or Render Obvious “a Through Array Contact (TAC) Region Formed Between the First and Second Channel Regions” (Limitation [8.g])

81. Toyama’s First Exemplary Structure does not disclose or render obvious “*a through array contact (TAC) region formed between the first and second channel regions*” as required by limitation [8.g] because the alleged TAC

region is not formed between a first channel region and a second channel region. Instead, it has a channel region on only one side. While Petitioner proposes altering the First Exemplary Structure to repeat portions of the device and add a second channel region, its proposed modification adds a second memory device with a second channel region rather than the claimed memory device comprising a TAC region between two channel regions. In addition, its modification cannot and would not be made because it removes necessary neighboring structures (e.g., the driver circuit that connects to the memory structure on the second side) that would result in the Toyama memory structure failing to function as intended.

82. The '806 claim 8 requires “a **through array contact (TAC) region** formed **between the first and second channel regions**,” which Toyama’s First Exemplary Structure fails to teach.

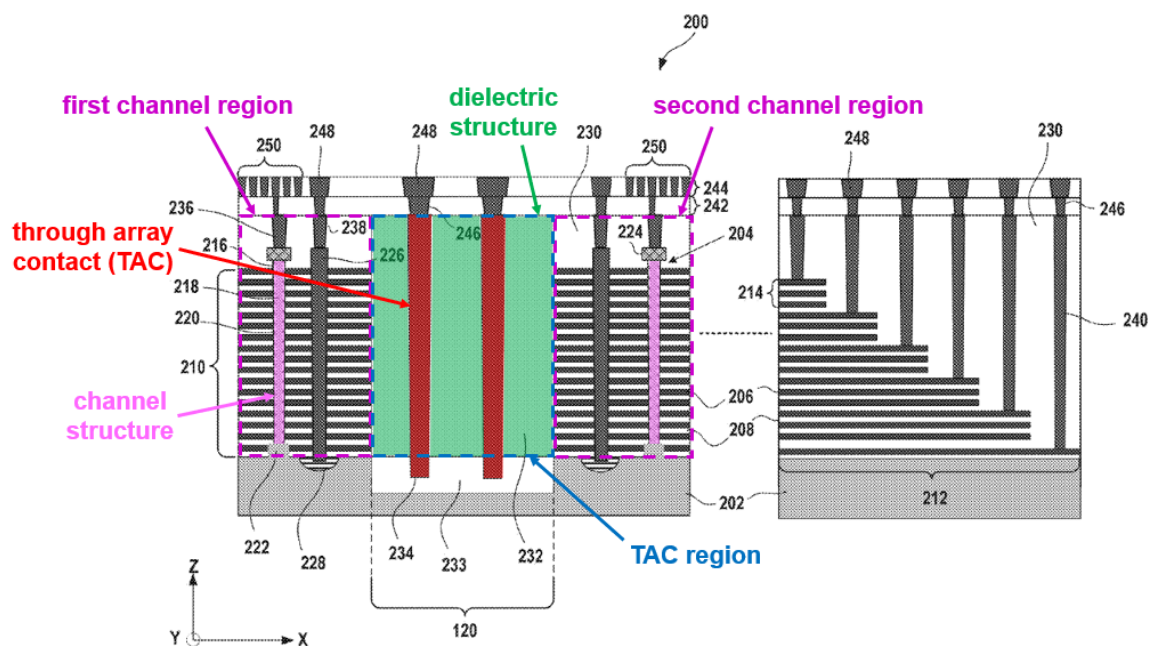


FIG. 2

'806, Fig. 2 (annotated).

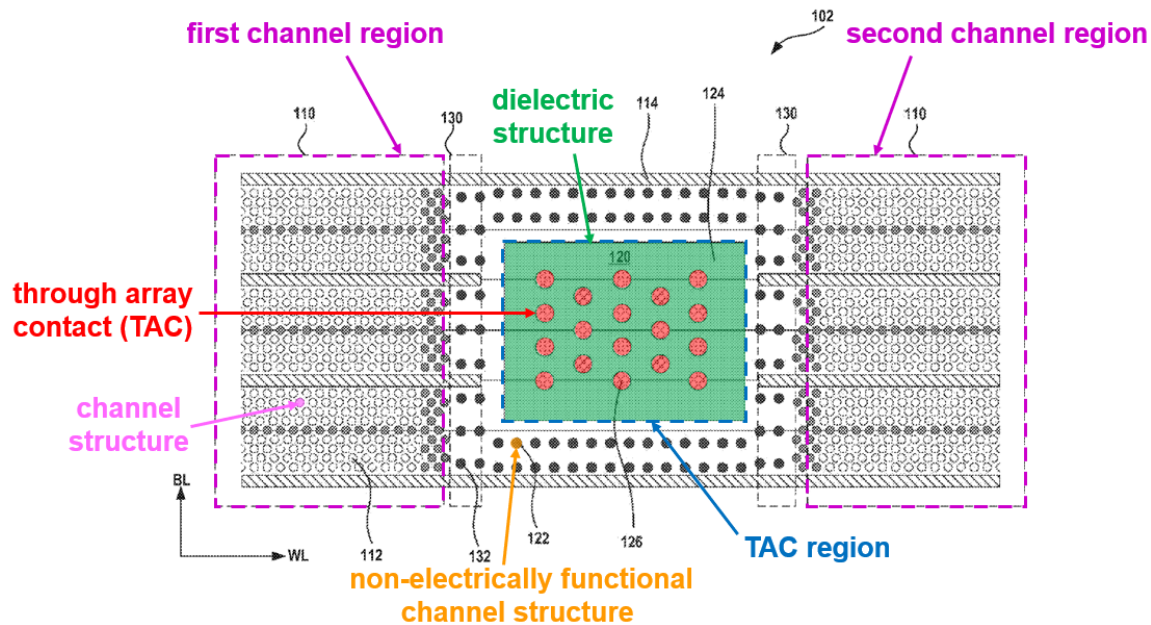


FIG. 1A

'806, Fig. 1A (annotated). As illustrated in Figures 2 and 1A, the claimed through array contacts (TACs) are formed in a **TAC region** that is formed in the array region between the **first and second channel regions**. As a result of this placement, TACs are formed closer to memory device components, and interconnect routing may be shortened. '806, 11:8-14.

83. In contrast to the '806, the channels in Toyama's First Exemplary Structure are positioned on only one side of each alleged TAC region (i.e., the alleged region containing dielectric fill material portion 430 and through-memory-level via structures 488):

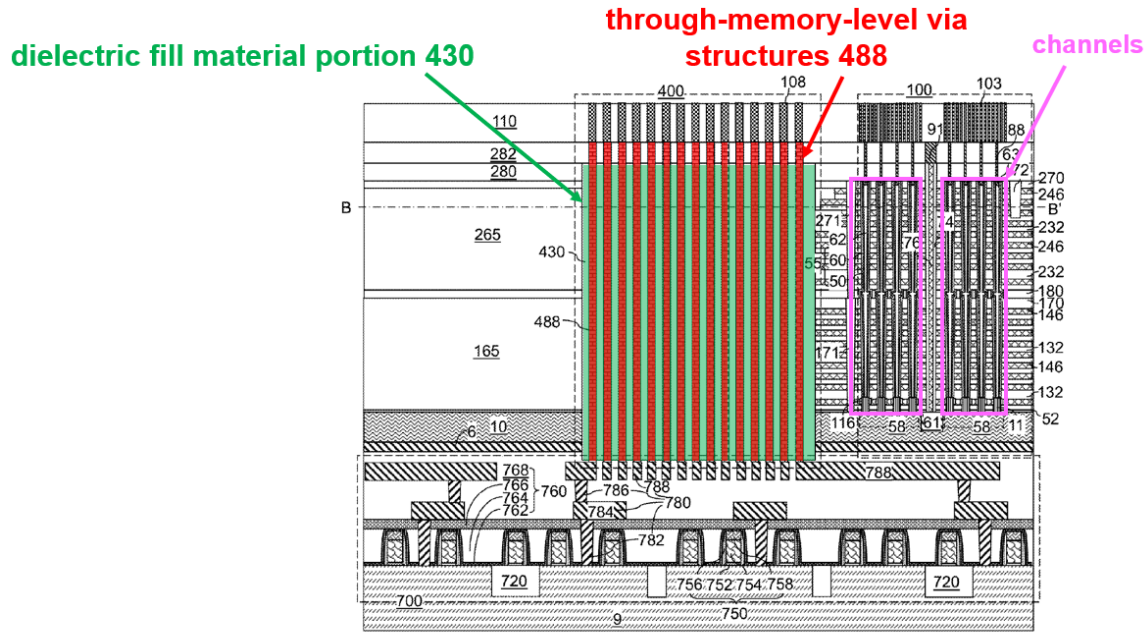


FIG. 17A

Ex. 1005, Fig. 17A (annotated by Patent Owner to show Petitioner's mapping); *see* Pet. 70, 89-91. Toyama never contemplates forming channels on both sides of the alleged TAC region of Toyama's First Exemplary Structure.

84. In a hindsight-based attempt to overcome this deficiency, Petitioner alters Toyama's device to repeat a "layout" from one of Toyama's figures in both horizontal directions (hd1 and hd2) so that the alleged TAC region would purportedly have channel structures on two sides. Pet. 69. Specifically, Figure 17E of Toyama shows a top-down view of the disclosed "layout" that Petitioner proposes repeating in the hd1 and hd2 directions:

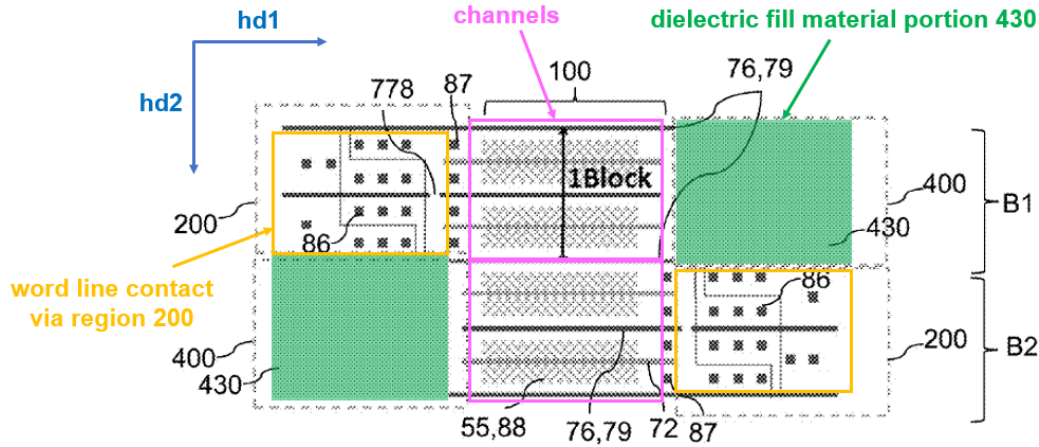


FIG. 17E

Ex. 1005, Fig. 17E (annotated). As discussed above, Petitioner maps the region containing dielectric fill material portion 430 to the claimed TAC region. Pet. 85-86. According to Petitioner, it would have been obvious to repeat this layout to create “multiple flash memory planes” “each including a distinct memory array region and staircase structure.” Pet. 74-75.

85. Petitioner’s proposed modification does not result in the claimed “memory device” comprising “a through array contact (TAC) region formed between the first and second channel regions” because, by introducing a distinct “plane” for the second channel region, Petitioner is instead adding a second memory device with a second channel region. As discussed above, the ’806 is directed to a TAC region that is formed in a single array between the first and second channel regions, which provides the benefit that TACs are closer to memory device components, and interconnect routing may be shortened. ’806, 11:8-14. In other

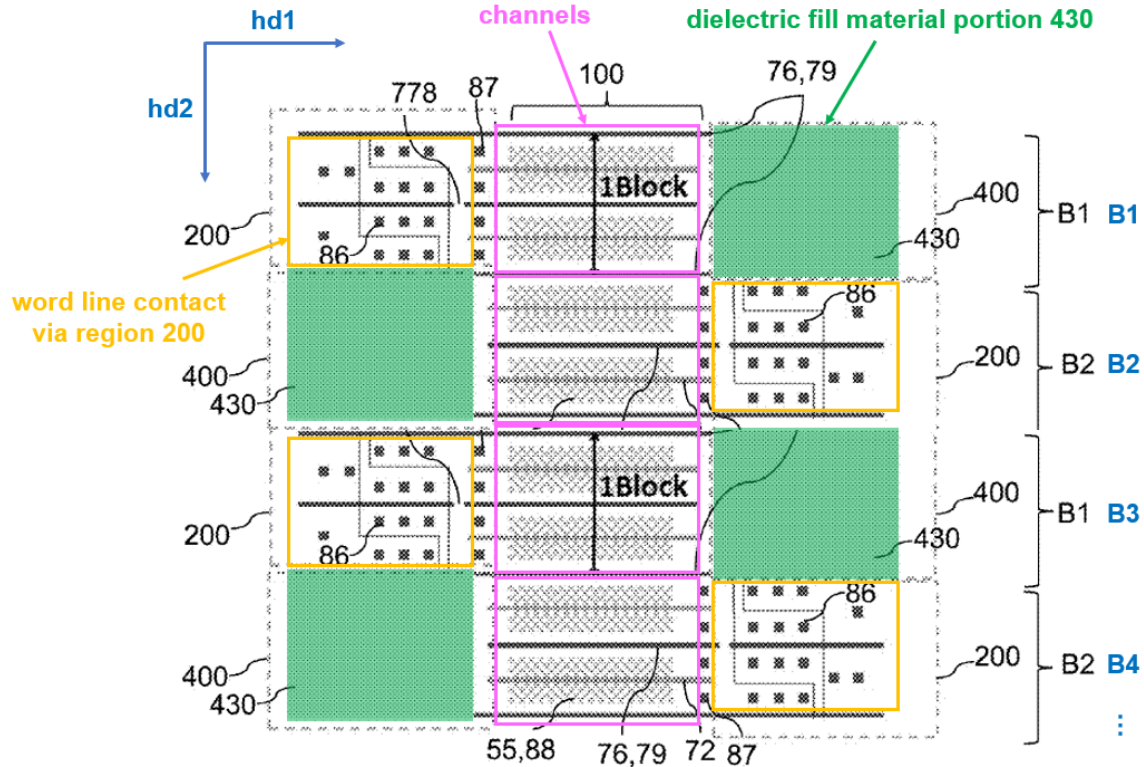
words, the claimed geometry having channel regions on both sides of the TAC region provides the disclosed benefit because *both channel regions* serve the same alternating conductor/dielectric stack as part of the same claimed “*memory device*” as claimed in the ’806. Petitioner tries to circumvent this requirement with its proposed modification of Toyama by adding a “distinct” memory plane for the second channel region (Pet. 74), but that channel region is part of a second, “distinct” memory device, and thus does not meet the Challenged Claim.

86. A person of ordinary skill in the art would have understood from the ’806 disclosures that the TAC region of the ’806 passes through an alternating conductor/dielectric stack that hosts both the first channel region and the second channel region. This is clearly shown in Figs. 1A-B and 2. The configuration that Petitioner has proposed results in two separate NAND planes that function independently and have two distinct conductor/dielectric stacks that are not physically or directly electrically connected. Therefore, since the two NAND planes operate independently, a person of ordinary skill in the art would not have considered the two channel regions from different planes to be a “first channel region” and a “second channel region” of the claimed memory device, but rather a “channel region in a first plane” and a “channel region in a second plane.” Furthermore, in Petitioner’s proposed modification, there are at least two separate alternating conductor/dielectric stacks through which different sets of alleged TACs extend

within two different alleged dielectric structures. This is in contrast to the '806 specification which consistently teaches that the first and second channel regions in Figs. 1A-B and 2 are within the same conductor/dielectric stack which is penetrated by the same TAC region within the same dielectric structure. It is only this TAC region between two channel regions in the same alternating conductor/dielectric stack (the same memory device) that would satisfy the claim language.

87. In addition, a person of ordinary skill in the art could not and would not have made the proposed modification. As an initial matter, while Toyama does suggest repeating this layout in the hd2 direction (bit line direction), repeating in the hd2 direction merely creates a row of adjacent channels and does not result in the claimed configuration of a TAC region with channel regions on both sides.

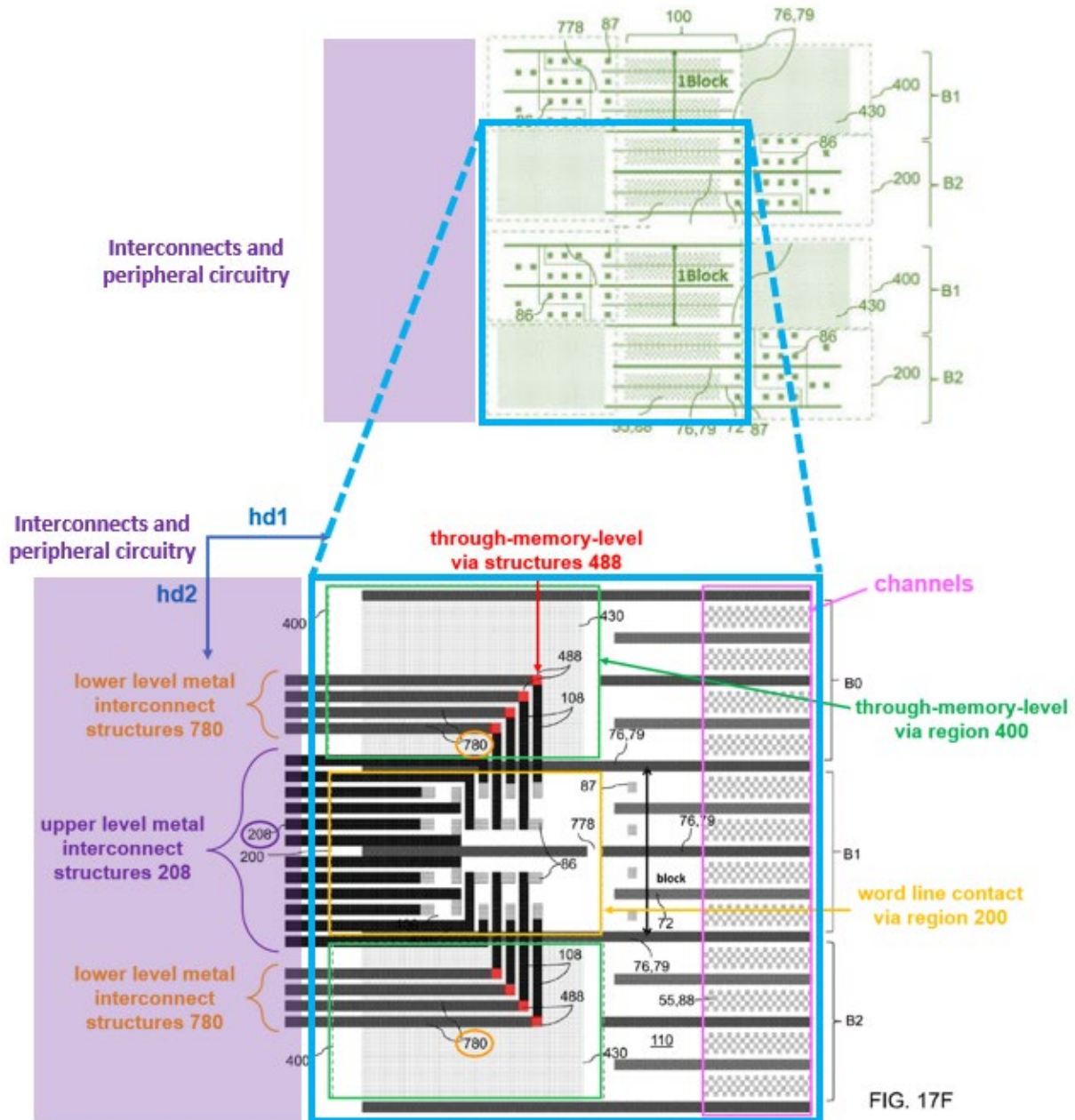
88. Specifically, repeating Toyama's layout along the bit line direction (hd2) does not alter the basic configuration of Toyama's memory device: an alleged channel region on only one side of each alleged TAC region. As shown below, the alleged channel regions simply repeat in a row, as a contiguous set of channel regions:



Ex. 1005, Fig. 17E (modified by Petitioner and annotated by Patent Owner); Pet. 73. Thus, this proposed modification does not result in a TAC region formed between first and second channel regions as required by the Challenged Claim. Petitioner's only proposal to arguably read on limitation [8.g] is to repeat in the hd1 direction.

89. But, Toyama never suggests that this layout may be repeated in the hd1 direction (word line direction). In fact, this proposed modification ignores other circuitry, including driver circuits, that is in the hd1 direction—i.e., in the location where Petition proposes instead adding additional layouts. Driver circuits, such as word line decoders, are essential components used to control the read and write operations in a memory device, and, as I explain below, are placed beyond the

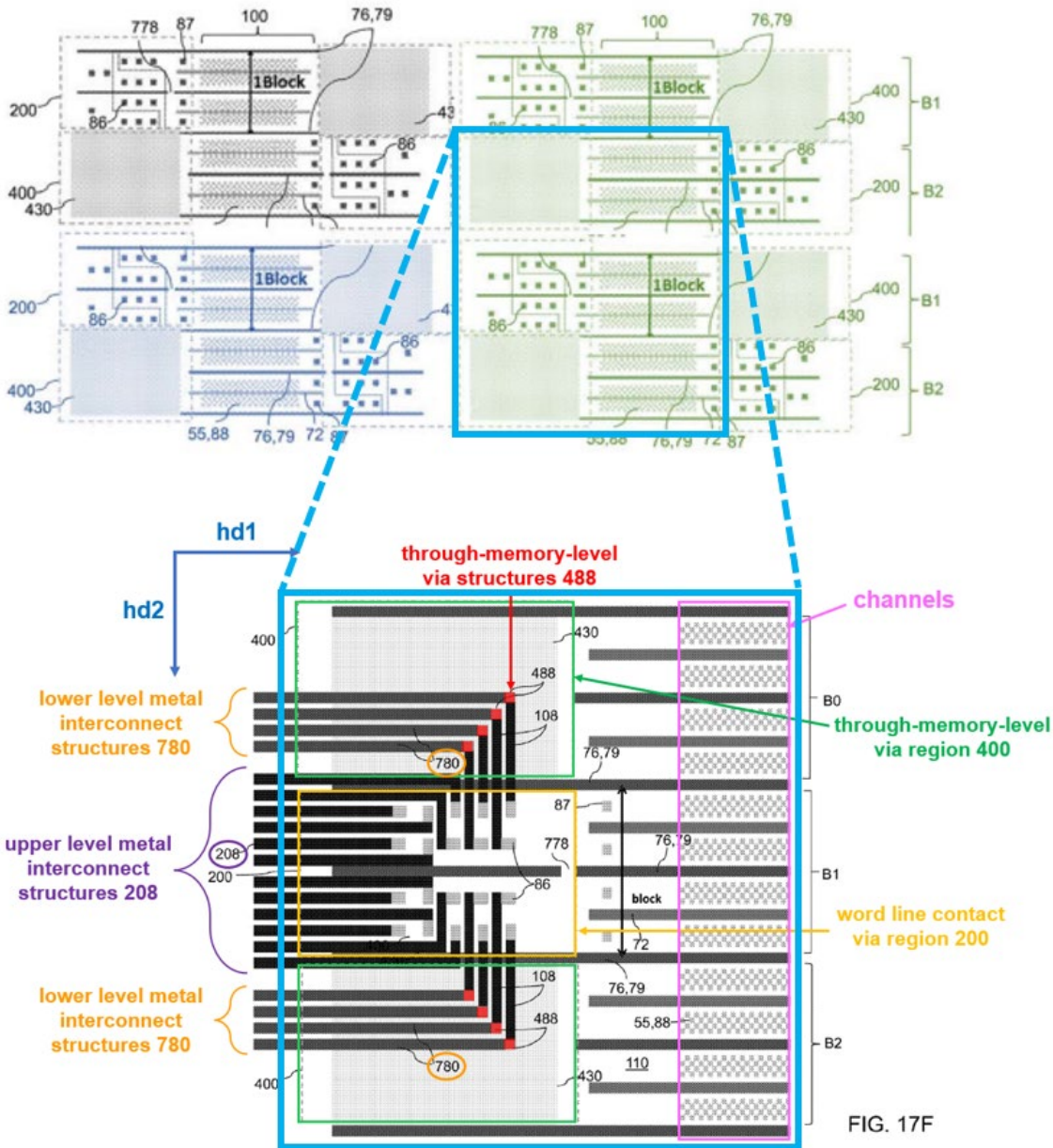
staircase region in the hd1 direction in Toyama. Specifically, Toyama includes “peripheral circuitry” to the left (and the right) of the alleged TAC region. Ex. 1005, [0163]. Such peripheral circuitry, such as “driver circuitry,” “supports[s] the operation of [the] memory structure.” *Id.* Critically, Toyama teaches that “upper level metal interconnect structures 208” connect to the driver circuits “at a location other than region 400” (the alleged TAC region) (Ex. 1005, [0251]) and Figure 17F—which is part of the First Exemplary Structure relied upon by Petitioner in this ground—shows these interconnect structures extending to the left of the alleged TAC region in the hd1 direction. The annotated figure below shows the location of these interconnects and peripheral circuitry relative to the “layouts” that are disclosed by Toyama:



Ex, 1005, Fig. 17F (annotated) and Fig. 17E (modified by Petitioner and annotated by Patent owner); Pet. 73. As shown, the driver circuits and the interconnects that connect to them are located to the left of the “layout” that Petitioner proposes repeating in the hd1 direction—i.e., precisely where Petitioner proposes adding the additional memory plane. Moreover, because Toyama’s blocks have “word line

contact via regions 200” on the left and on the right of the channels, the interconnects and driver circuits are present on ***both sides*** of the layout in the hd1 direction.

90. Petitioner’s proposed modification completely ignores the interconnects and peripheral circuitry, including the driver circuit, and therefore would not work. As shown below, Petitioner’s alteration of Toyama—to repeat in the hd1 direction—adds additional “layouts” in the location of necessary interconnects and driver circuitry:



Ex. 1005, Fig. 17E (modified and annotated by Petitioner, Pet. 74) (top) and Fig. 17F (annotated by Patent Owner) (bottom). It is unsurprising that the layout of Figure 17E is not repeatable in the hd1 direction—Toyama is designed to instead repeat in the hd2 direction, with interconnects and peripheral circuitry on either side in the hd1 direction. But none of the circuitry needed to operate each memory array

and discussed in Toyama is included in Petitioner's modification. Petitioner relies on hindsight to blindly copy and paste elements of Toyama, in a way not taught by Toyama, and in a way that lacks the necessary interconnects and support circuitry for a functioning memory device.

91. By completely ignoring the interconnects and driver circuitry, Petitioner and Dr. Lee have failed to address many additional complications that would have arisen from simply repeating Toyama's device in the hd1 direction. First and foremost, the combination eliminates the peripheral circuitry and interconnects entirely, which are necessary for the device to operate. Even if Petitioner and Dr. Lee try to propose an alternative arrangement that does not eliminate the interconnects and peripheral circuitry, the particular arrangement would introduce other complications that Petitioner and Dr. Lee have not even attempted to address, such as routing congestion and complications, resistance-capacitance delays, impacts on performance, power consumption, heat dissipation, device size, among many other issues. All of these complications would have not only motivated a person of skill in the art to make these hindsight-based alterations, but they are also left unaddressed by Petitioner and Dr. Lee. And the particular impact of the complications would depend significantly on the particular arrangement proposed by Petitioner and Dr. Lee, which was not included in the Petition or the opening declaration.

92. To the extent it is argued that the interconnects and driver circuits in Toyama are only on one side, and that additional planes could be created on the other side in the hd1 direction, this would not resolve the issue. As discussed, Toyama shows in Figure 17F that the memory array has interconnects and driver circuits on at least the left side, and thus in the modification adding additional planes, each plane would likewise include the required interconnects and driver circuitry on the left side. In other words, a new plane cannot be added on the right in the proposed location because that new plane would need to include interconnects and driver circuits to its left.

93. Petitioner makes a series of arguments regarding why a person of ordinary skill in the art allegedly would have been motivated and found it obvious to make the proposed modification (Pet. 74-83), but none of the analysis addresses the issue discussed above. Again, this is because Petitioner's analysis and proposed modification do not consider how Toyama's device would function as a workable memory device, and instead blindly copies and pastes elements of Toyama. Petitioner first argues that "[a] POSITA would have known how to implement a flash memory device with multiple planes by placing the planes beside each other" (Pet. 75), but this provides no motivation to modify Toyama, and also does not establish that a person of ordinary skill in the art would have known how to modify the specific device taught by Toyama to include multiple planes in the manner proposed.

Indeed, the very fact that Petitioner's expert, Dr. Lee, did not consider the necessary adjacent circuitry shows that Petitioner's generalized citations to other references (Pet. 75-80) are not directly applicable to Toyama.

94. Petitioner asserts that “a POSITA understood numerous benefits of a multi-plane flash memory device,” which Petitioner lumps together as “improve[d] ... performance of NAND based systems” (Pet. 79-80), but again, these purported benefits cannot be achieved with Petitioner's proposed modification because Toyama's device does not allow the proposed modification. Moreover, even assuming, *arguendo*, that there are workable ways to introduce multiple planes in Toyama's device (i.e., layouts other than the one Petitioner has proposed), the Petition does not present any such alternatives and therefore has not shown that any such alternatives would result in “a through array contact (TAC) region formed between the first and second channel regions” as required by limitation [8.g].

95. Finally, for the same reasons, Petitioner has not established that “the obviousness combination is nothing more than applying a known technique (implementing multiple planes of a NAND flash memory array) to a known device (Toyama's first exemplary structure) to yield predictable results (a NAND flash device with improved performance).” Pet. 82.

96. Therefore, Petitioner has not shown that Toyama’s First Exemplary Structure discloses or renders obvious “a through array contact (TAC) region formed between the first and second channel regions” as required by limitation [8.g].

B. Claim 10: Toyama’s First Exemplary Structure Does Not Disclose or Render Obvious “an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the First and Second Channel Structures” (Limitation [10.b])

97. As with Toyama’s Second Modification, Toyama’s First Exemplary Structure also does not disclose or render obvious “*an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures*” as required by limitation [10.b] because Toyama’s alleged etch stop plugs are not interposed between “**each**” of the alleged local contacts and the alleged channel structures. Indeed, Petitioner’s analysis for dependent claim 10 omits one of the types of structures that Petitioner mapped to the “local contacts” of independent claim 8. This is because those alleged etch stop plugs are plainly not interposed between that purported local contact and the purported channel structures.

98. As I explain in §VIII.A, the plain meaning of the term “each local contact of the local contacts” refers to each of the “local contacts disposed on the first and second channel structures and the slit structures” as recited in limitation [8.f].

99. Petitioner’s mapping for claim 10 in the Petition does not even attempt to address “each local contact.” For independent claim 8, Petitioner contends that Toyama’s “**memory stack structures 55**” are the claimed “first and second channel structures” and “**laterally-elongated contact via structures 76**” are the claimed “slit structures.” Pet. 70-85. Petitioner further alleges that Toyama’s “**drain contact via structures 88**” and “**source connection via structures 91**” are the claimed “local contacts disposed on the first and second channel structures and the slit structures.” Pet. 86-87.

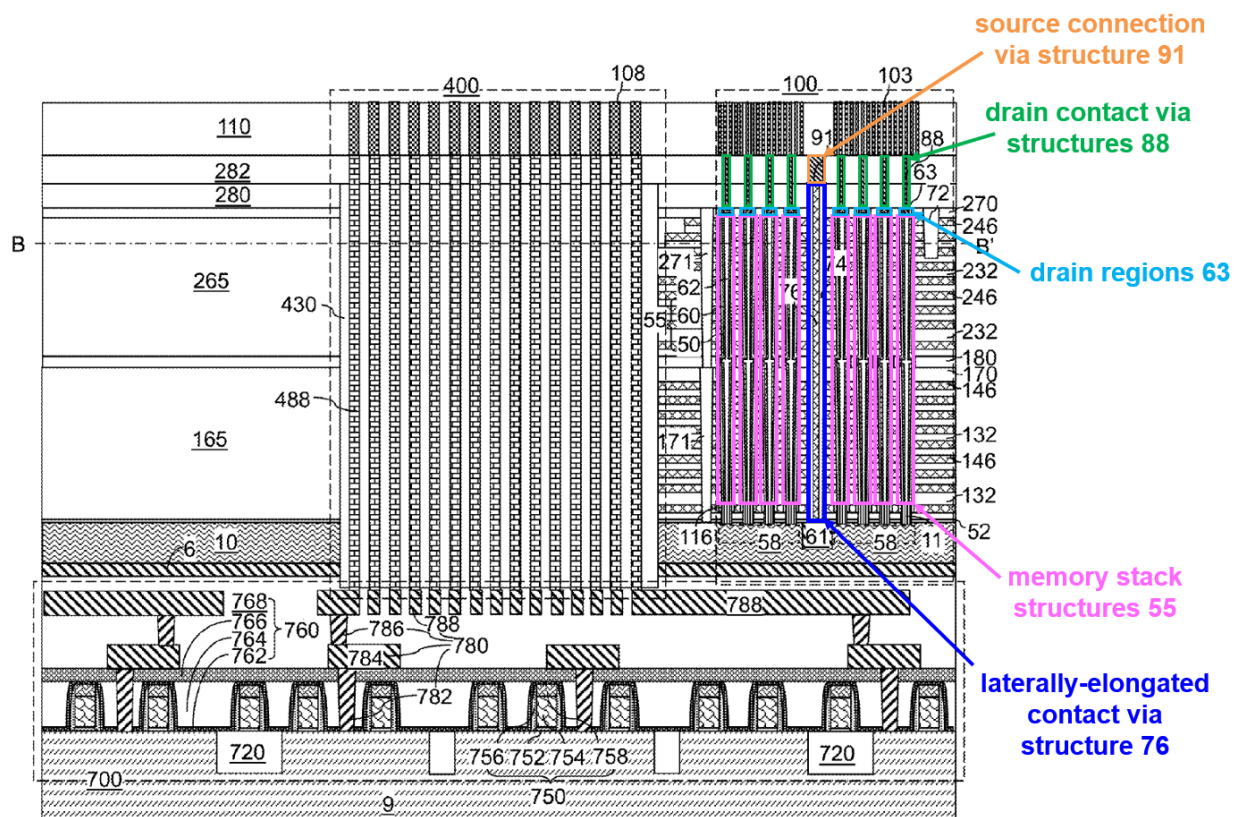


FIG. 17A

Ex. 1005, Fig. 17A (annotated by Patent Owner). Specifically, to meet limitation [8.f], Petitioner argues that Toyama’s “**drain contact via structures 88**” are local

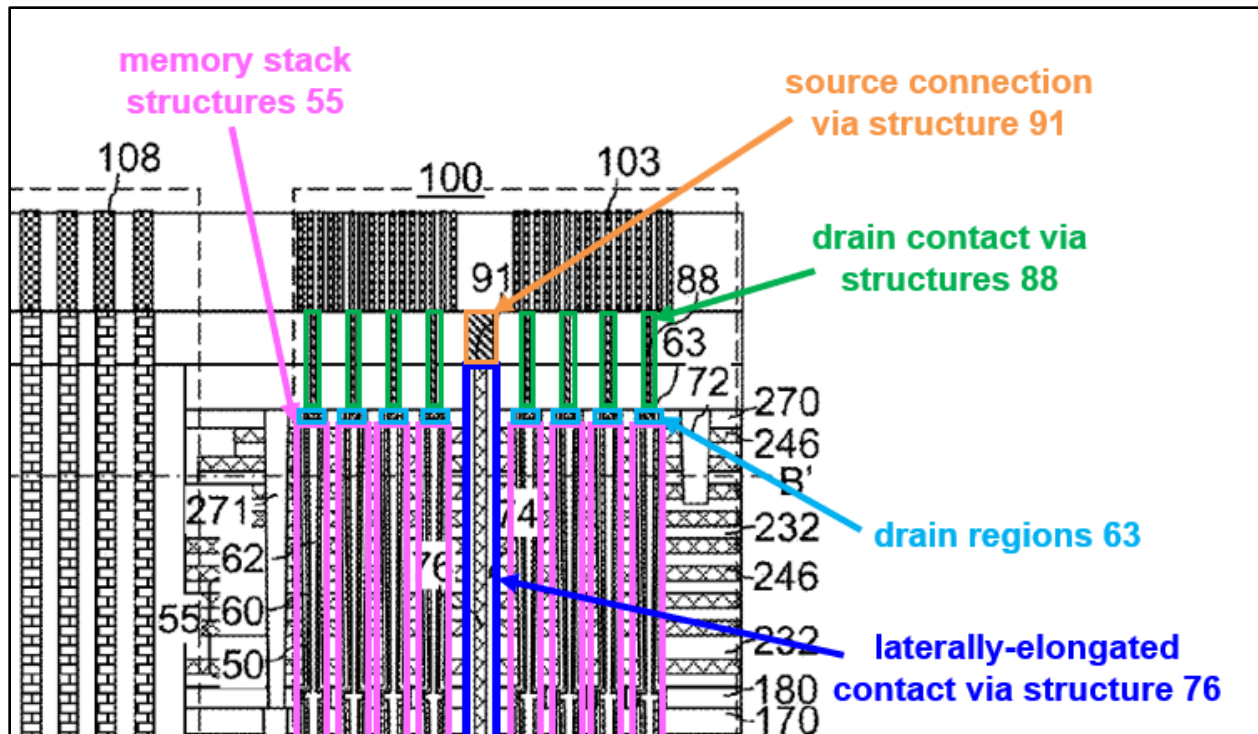
contacts disposed on the alleged first and second channel structures (“**memory stack structures 55**”) and “**source connection via structures 91**” are local contacts disposed on the alleged slit structures (“**laterally-elongated contact via structures 76**”). Pet. 86-87.

100. With regards to claim 10, Petitioner argues that Toyama’s “**drain regions 63**” meet the limitation of “an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures” (Pet. 98-99), but Petitioner’s analysis discusses only **drain contact via structures 88** (a subset of the purported local contacts). (For the purposes of this declaration, I do not dispute Petitioner’s assertion that “a POSITA would have understood, or at least found obvious, that ‘drain regions 63’ are plugs that serve the purpose of stopping an etch.” Pet. 55.) Petitioner entirely ignores **source connection via structures 91**, which Petitioner mapped to one of the claimed local contacts to meet limitation [8.f].

101. Because claim 10 requires an etch stop plug interposed between **each local contact of the local contacts** and each channel structure of the first and second channel structures, Petitioner was required to identify an etch stop plug that is also interposed between the **source connection via structures** (alleged local contacts) and **memory stack structures** (alleged channel structures)—but failed to do so. While Petitioner’s mapping discusses whether there is an etch stop plug interposed

between the **drain contact via structures** and **memory stack structures**, Petitioner does not even attempt to address whether there is an etch stop plug interposed between the **source connection via structures** and **memory stack structures**. Arguing that Toyama discloses an etch stop plug interposed between the channel structures and some of the purported local contacts that Petitioner mapped to the claimed local contacts is not sufficient. Petitioner simply failed to show that Toyama's First Exemplary Structure teaches each element of limitation [10.b].

102. Toyama's alleged etch stop plug, **drain regions 63**, is **not** interposed between **source connection via structures 91** (one of the alleged local contacts) and **memory stack structures 55** (the alleged channel structures) as required by claim 10. Indeed, Petitioner has not even alleged that the alleged etch stop plug is between those structures. As shown in Fig. 17A of Toyama annotated below, the **drain regions 63** are, at most, "interposed between" the **drain contact via structures 88** and **memory stack structures 55**. None of the **drain regions 63**, however, is "interposed between" the **source connection via structures 91** and **memory stack structures 55** as required by limitation [10.b]:



Ex. 1005, Fig. 17A (excerpted and annotated by Patent Owner). For limitation [8.f], Petitioner relies on both **drain contact via structures 88** (“local contacts disposed on the first and second channel structures”) and **source connection via structures 91** (“local contacts disposed on...the slit structures”), and *cannot* meet this limitation without relying on both structures. As a result, the alleged etch stop plug of Toyama is not interposed between “each” purported local contact of the local contacts and each purported channel structure of the first and second channel structures as required by limitation [10.b].

103. Therefore, Petitioner has not shown that Toyama’s First Exemplary Structure discloses or renders obvious limitation [10.b].

**XII. PETITIONER’S GROUND 3: TOYAMA’S SECOND MODIFICATION
IN COMBINATION WITH TOYAMA’S FIRST EXEMPLARY
STRUCTURE DOES NOT DISCLOSE OR RENDER OBVIOUS
CLAIM 10**

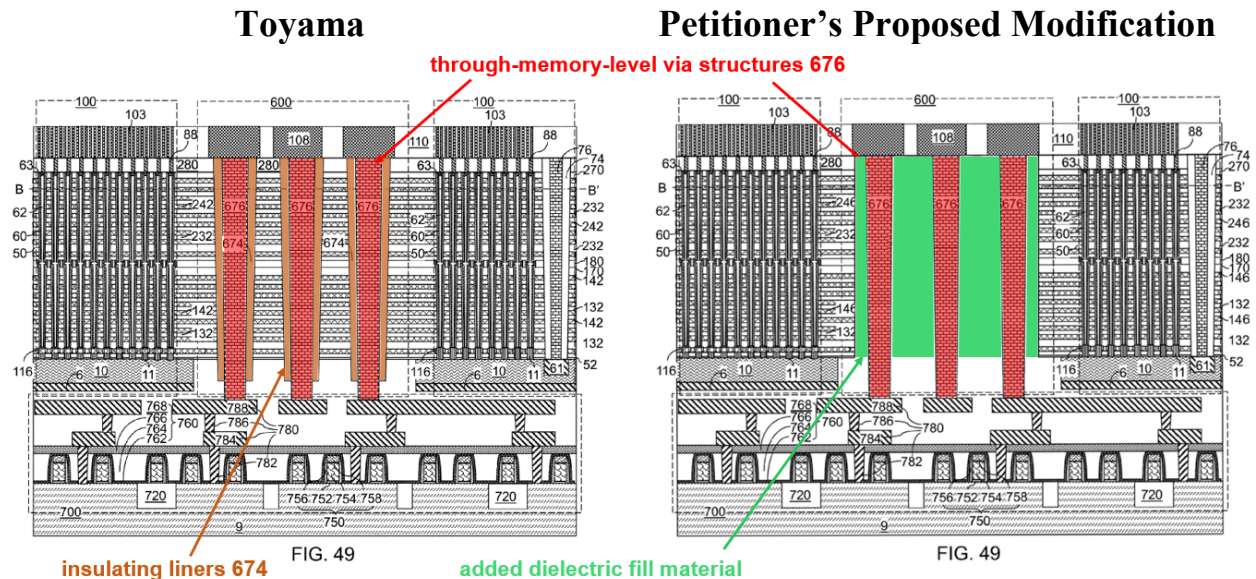
104. In Ground 3, Petitioner relies on a modification of Toyama’s Second Modification based on Toyama’s First Exemplary Structure (which Petitioner refers to as “Obviousness Combination”) as allegedly rendering obvious the Challenged Claim. Pet. 100-125. For the reasons explained below, it is my opinion that the Obviousness Combination does not disclose or render obvious the Challenged Claim at least because a person of ordinary skill in the art would not have made Petitioner’s hindsight-based modification. In addition, Petitioner’s Obviousness Combination does not disclose or render obvious *“a plurality of non-electrically functional channel structures surrounding the TAC region”* as required by limitation [8.h] because Toyama’s alleged non-electrically functional channel structures do not surround the alleged TAC region. Finally, Petitioner fails to show that the Obviousness Combination renders obvious limitation [10.b] (*“an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures”*) for the same reasons as discussed for Ground 1.

A. A Person of Ordinary Skill in the Art Would Not Have Found It Obvious to Modify Toyama’s Second Modification in the Proposed Manner

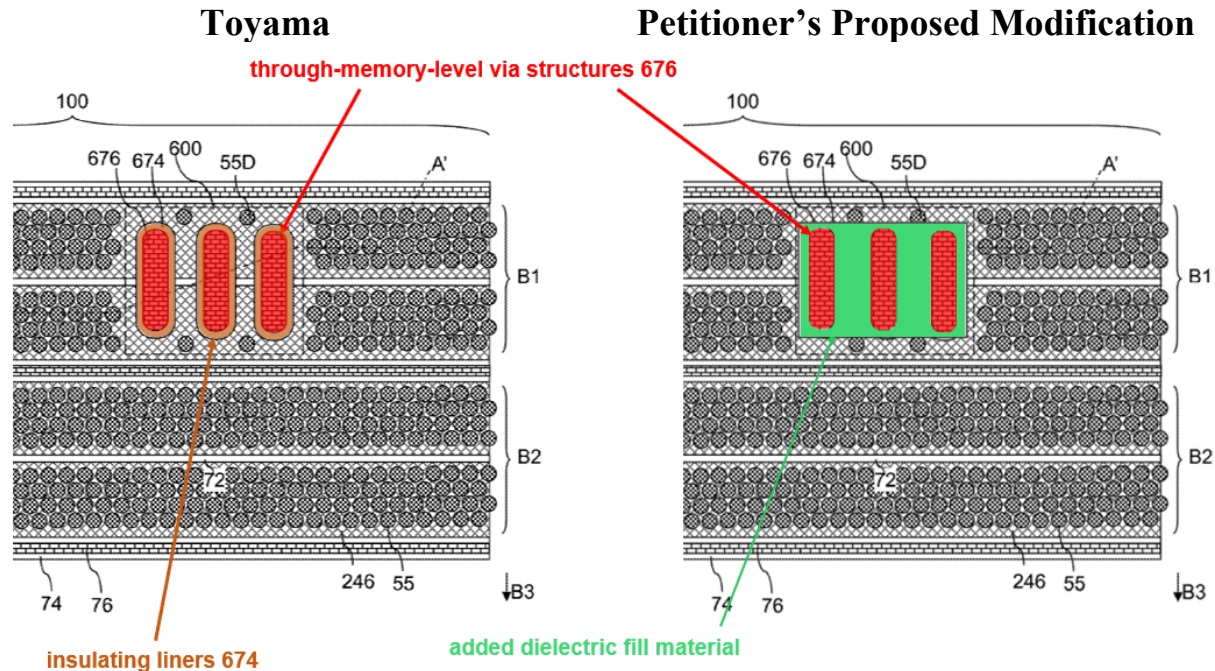
105. Petitioner’s proposed modification of Toyama’s Second Modification based on Toyama’s First Exemplary Structure (Pet. 100-125) does not render obvious the Challenged Claim because a person of ordinary skill in the art would not have made Petitioner’s hindsight-based modification. Toyama uses the TAC openings for depositing etchant and conductive material during the gate replacement process, and the proposed unitary dielectric blocks that access. In addition, the proposed modification replaces conductive material used to conduct current to control memory with a large dielectric (an insulator), and Petitioner does not even attempt to address the impact that these changes would have had on Toyama’s memory structure.

106. Petitioner has not shown that a person of ordinary skill in the art would have been motivated to make its proposed modification of Toyama’s Second Modification based on Toyama’s First Exemplary Structure. As I discuss in §X.A, Toyama’s Second Modification does not disclose or render obvious “*a plurality of through array contacts (TACs) extending vertically through the dielectric structure*” as required by limitation [8.g] because Toyama’s alleged TACs do not extend through the same structure (the claimed “dielectric structure”). With the hope of overcoming this deficiency, in Ground 3, Petitioner puts forth a modification of

Toyama's Second Modification based on Toyama's First Exemplary Structure, wherein the physically separated insulating liners around the alleged TACs are replaced with a unitary dielectric filling material around all the alleged TACs, as shown:



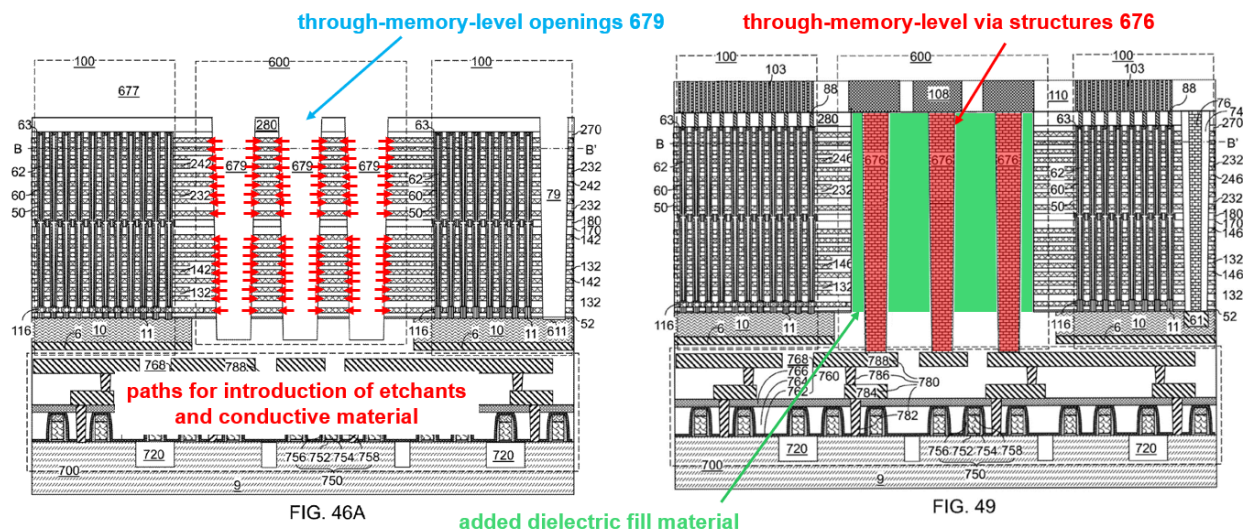
Ex. 1005, Fig. 49 (left: annotated by Patent Owner; right: modified by Petitioner at Pet. 104 and annotated by Patent Owner).



Ex. 1005, Fig. 48B (left: annotated and excerpted by Patent Owner; right: modified by Petitioner at Pet. 105 and annotated and excerpted by Patent Owner).

107. A person of ordinary skill in the art would not have added a unitary dielectric fill material to Toyama's Second Modification for multiple reasons. First, adding the unitary dielectric fill material would have gone against Toyama's express teachings of using the alleged TAC openings for depositing etchant and conductive material during the gate replacement process—the proposed unitary dielectric completely blocks access to the alternating stack through the alleged TAC openings. For example, Toyama teaches forming “through-memory-level via structures 676” (the alleged TACs) by forming conductive material in “through-memory-level openings 679.” Ex. 1005, [0341]. Prior to the formation of the via structures 676, the openings 679 are “employed to introduce etchants that etch the sacrificial

material layers (142, 242) selective to the insulating layers (132, 232)” as well as to introduce “conductive material” to form “electrically conductive layers (146, 246).” Ex. 1005, [0337]. This process is possible because, as shown in unmodified Figure 46A, below, the alleged TAC openings (through-memory-level openings 679) directly abut sacrificial material layers (142, 242) of the alternating stack, allowing the alleged TAC openings to be used for introduction of etchants and conductive material.



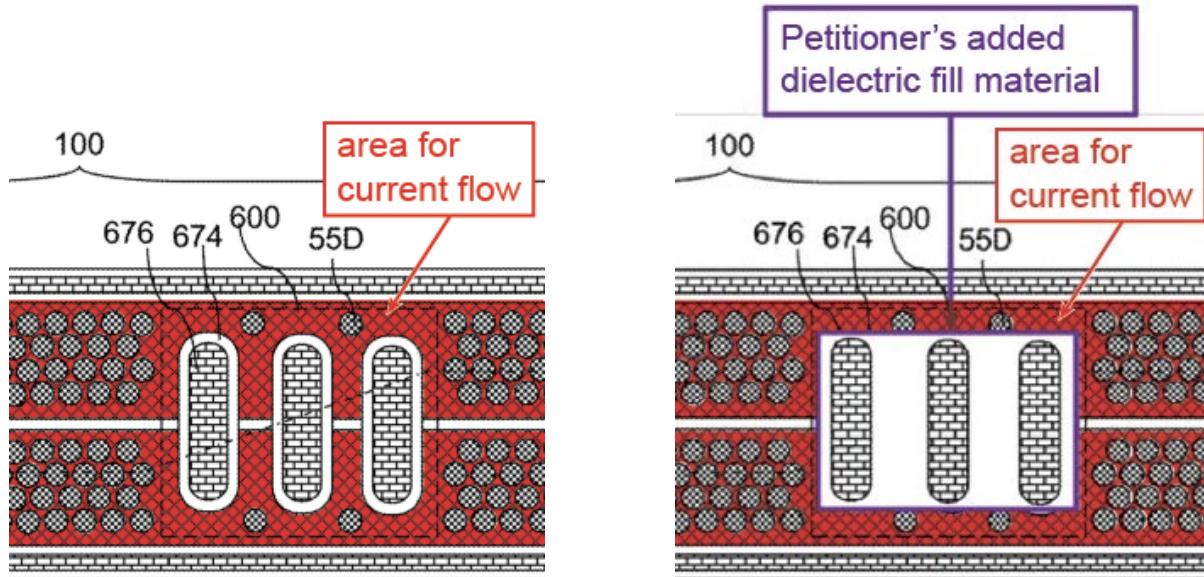
Ex. 1005, Fig. 46A (annotated by Patent Owner), Fig. 49 (modified by Petitioner at Pet. 104 and annotated by Patent Owner). In contrast, Petitioner’s proposed modification (modified Fig. 49, above) cuts off this access. By using Petitioner’s proposed method of “form[ing] a unitary dielectric fill material in ‘through-memory-level region 600’ and subsequently forming ‘through-memory-level via structures 676’ within the unitary dielectric” using Toyama’s First Exemplary Structure’s

teachings (Pet. 107), the openings 679 are formed within the unitary dielectric fill material instead of the alternating stack, thereby blocking access to the alternating stack and eliminating a critical path for the introduction of etchants and conductive materials. In other words, in Petitioner's proposed modification, the unitary dielectric fill material blocks the alleged TAC openings from being utilized for their intended purpose.

108. Second, Petitioner's proposed modification removes large portions of the conductive layers in the array region that form the word lines and replaces them with an insulator. Importantly, these word lines are electrically conductive and are used to control the memory—replacing them with a large insulator would eliminate that capability in those areas. As illustrated below, Petitioner's proposed modification (enlarged and annotated below) would add an insulating dielectric fill material that has a much larger area than the original insulating liners, and extends all the way to dummy memory stack structures 55D:

Toyama

Petitioner's Proposed Modification



Ex. 1005, Fig. 48B (left: annotated and excerpted by Patent Owner; right: modified by Petitioner at Pet. 105 and annotated and excerpted by Patent Owner). As such, this would eliminate current flow through these areas of the word lines that Petitioner proposed converting into dielectric fill material, thereby causing current to flow through a much narrower region. A person of ordinary skill in the art would have understood that, at minimum, this modification would introduce reliability and manufacturing issues, and therefore the device would not operate as intended.

109. I note that Dr. Lee agrees that higher current density causes undesirable hot spots that “degrade” the device. *See* Ex. 2006, 36:16-37:1 (“assuming that everything remained the same” in comparison a wire “carrying less current density, [] a person of ordinary skill in the art would - - likely to conclude that the temperature of the high current density [wire] will be higher”), 32:9-10 (“local hot spot[s] ... can degrade your device reliability”). Petitioner does not address this issue, including

the adverse impact the restriction of current flow would have on the operability of the device. A person of ordinary skill in the art would not have made this alteration to eliminate critical current flow in these areas.

110. To overcome these difficulties, the '806 has a different arrangement of features in the relevant regions, which does not create the restrictions present in Petitioner's proposed Obviousness Combination and allows for wide areas around the dielectric structure for current flow through the word lines:

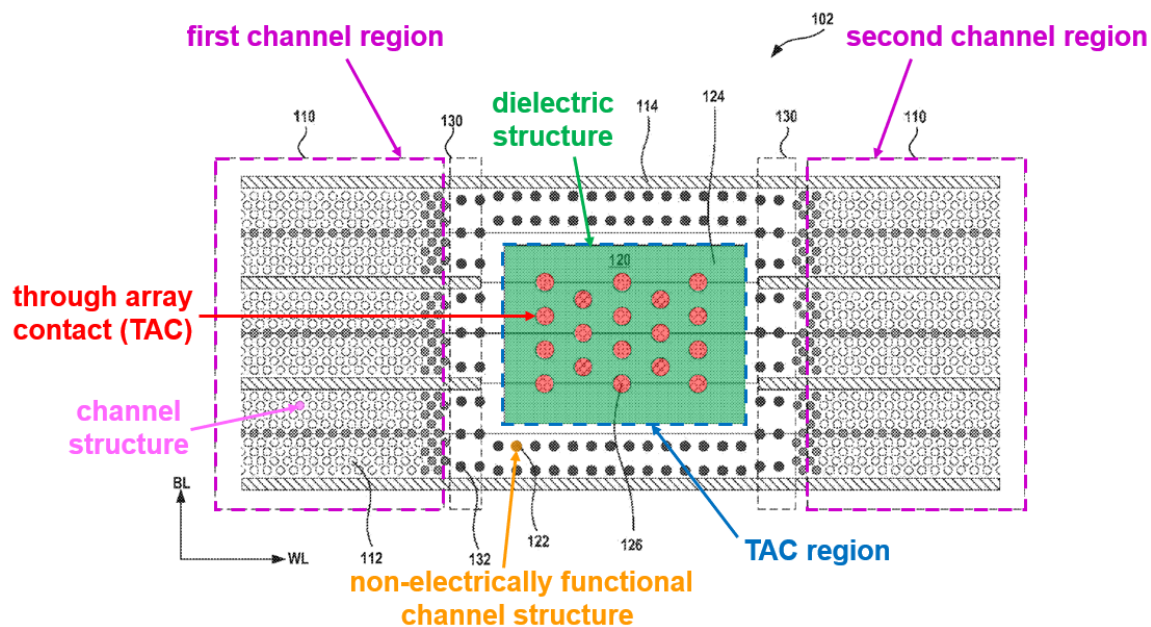


FIG. 1A

'806, Fig. 1A (annotated). In addition, the '806 uses an isolation structure onto which the dielectric structure is deposited with a high level of control using various patterning techniques, which Toyama does not teach. '806, 10:35-38, 14:63-15:30, 21:20-28. Forming a unitary dielectric fill material portion in a crowded memory array region with several other structures in its vicinity presents challenges that

would have deterred a person of ordinary skill in the art and are overcome by the novel teachings of the '806. Toyama does not teach placing multiple through-memory-level vias within a dielectric structure in the memory region, because this solution was not known. For example, if the dielectric structure is too small, the vias, which are significantly bigger than the channels, would not fit. If the dielectric structure is too large, the current flow through the word lines is blocked. Increasing the distance between the “laterally-elongated contact via structures 76” to solve the latter problem was not feasible (and regardless, is not proposed by Petitioner), because the gate replacement process requires these structures not to be too distant from each other.

111. In particular, Toyama’s “laterally-elongated contact via structures 76” are formed by filling the “backside contact trenches 79.” Ex. 1005, [0236]. The backside contact trenches 79 are used in the gate replacement process for supplying the etchant to remove the sacrificial layers and then supplying the metal to form the conductive layers. Ex. 1005, [0223] (“The isotropic etch process can be a wet etch process employing a wet etch solution, or can be a gas phase (dry) etch process in which *the etchant is introduced in a vapor phase into the backside contact trench 79.*”) [0227-0228] (“At least one conductive material can be deposited in the plurality of backside recesses (143, 243), on the sidewalls of the backside contact trench 79, and over the first contact level dielectric layer 280. ... ¶ A plurality of

first electrically conductive layers 146 can be formed in the plurality of first backside recesses 143, a plurality of second electrically conductive layers 246 can be formed in the plurality of second backside recesses 243, and a continuous metallic material layer (not shown) can be formed on the sidewalls of each backside contact trench 79 and over the first contact level dielectric layer 280.”). For the gate replacement process to succeed, these trenches must not be too distant from each other.

112. For example, U.S. Patent No. 10,559,583 (“Park”) (Ex. 2007), filed on 01/25/2017, taught that when “inflow passages,” i.e., paths through which the etchant and conductive material reaches given locations, are too long, “defects” may form at those locations. Ex. 2007, 9:44-48 (“Thus, the connecting electrodes 129f to 129i may have a zigzag form to thus *shorten the inflow passages for the phosphoric acid and the conductive material and prevent a defect from occurring* in the process of forming the gate electrode layer 120.”), 15:56-59 (“Thus, when an inflow passage of the phosphoric acid is not properly secured, *a portion of the sacrificial layers SL may remain without being removed.*”). Park taught various ways of shortening the inflow passages to reduce the likelihood of defects. Ex. 2007, 10:14-17 (“Thus, the word line cuts provided to form the first and second lines 103 and 104 may allow the inflow passages for the phosphoric acid and the conductive material to be shortened.”), 11:52-59 (“The second dummy channel structures DCH2 may serve to shorten inflow passages of phosphoric acid and a conductive material

that are required to flow therethrough in a process of forming the gate electrode layers. Thus, degradation of the characteristics of the memory device 100A due to a void formed within the gate electrode layers in the process of forming the gate electrode layer may be prevented.”), 12:30-38, 12:47-52, 16:38-49. Therefore, in Petitioner’s Obviousness Combination, increasing the distance between Toyama’s backside contact trenches in order to overcome the issue of shrinking current flow paths due to the introduction of a large dielectric fill material portion would have caused the exact problem Park warns against. In other words, a person of ordinary skill in the art would not simply have been able to place laterally-elongated contact via structures 76 farther from each other without causing serious problems with the gate replacement process.

113. In contrast to Toyama’s Second Modification, Toyama’s First Exemplary Structure was able to teach a dielectric fill material portion large enough to fit multiple vias at the end of the stack opposite to the staircase region because there is no need for the current to flow there through the word lines in that location, which is at the end of the stack without word line contacts. Petitioner does not address these considerations and simply asserts that the Obviousness Combination “is nothing more than the mere substitution of one element ... for another ... to yield a predictable result.” Pet. 100. Results of replacing the conductive material in the word lines used to control the memory with an insulator are far from predictable,

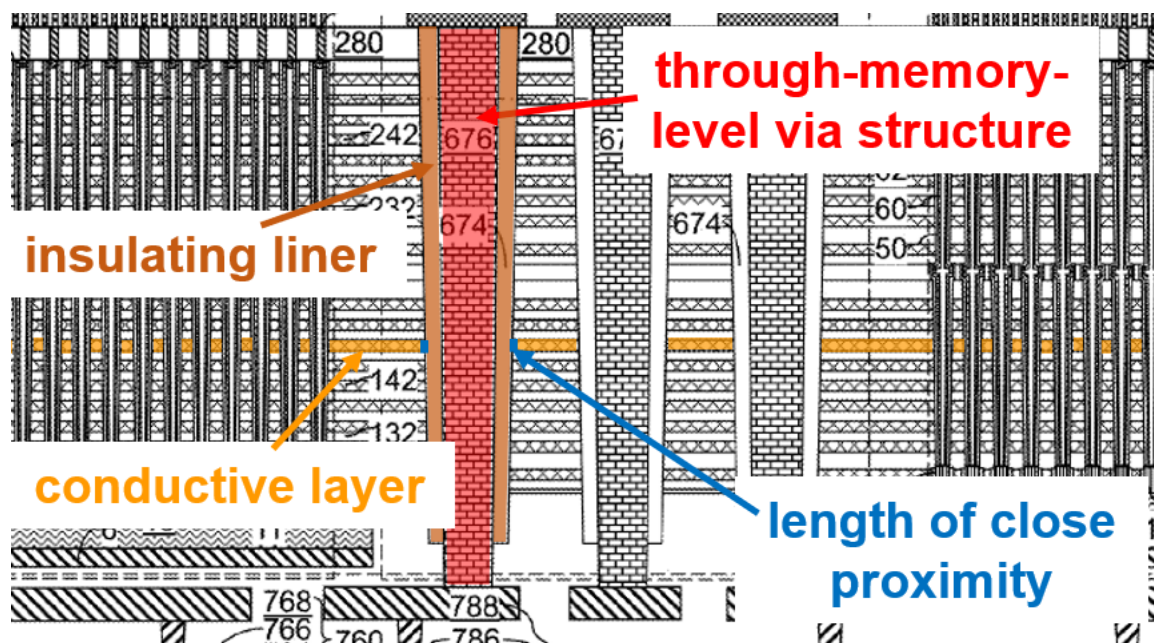
and would cause the device to not operate as intended, including by introducing severe reliability and manufacturing issues, as I explained above.

114. Notably, Toyama teaches more than a dozen embodiments with various configuration of elements, but none of these embodiments teaches forming a unitary dielectric block in the memory array region between two channel regions because it eliminates the conductive material in the word lines.

115. Thus, I agree with the Board’s conclusion in its institution decision, “[a]s Patent Owner points out, based on the present record, Petitioner does not appear to address the impact of replacing the region containing conductive word lines with dielectric fill material. Based on the preliminary record, it appears that replacing the conductive word lines with insulating material would eliminate the current that controls the memory, resulting in a non-functioning device.” DI, 43-44.

116. Petitioner’s argument that a person of ordinary skill in the art would have been motivated to make the combination because it “would reduce capacitive coupling as compared to Toyama’s Second Modification” (Pet. 107-108) is misplaced. As a preliminary matter, this purported motivation does not address the issue discussed above. In addition, while Petitioner argues that its modification addresses capacitive coupling between the through-memory-level vias (the alleged TACs) and the electrically conductive layers in that region, Toyama’s Second Modification already “minimizes” capacitive coupling by placing the through-

memory-level via structures in the memory array region with dielectric liners. Ex. 1005, [0377]. As Toyama explains, these through-memory-level via structures “provide various control signals for a three-dimensional memory device in a manner that shortens the signal path, and thus, minimizes ... capacitive coupling.” *Id.* Petitioner’s expert, Dr. Lee, explains that there is a relation between capacitive coupling and distance between conductive elements (Ex. 1003 ¶ 186), but he does not address that capacitive coupling is also a function of the length (or area) of overlap. *See* Ex. 1026 at 64 (“Crosstalk increases as the ... *length of their close proximity* (coupled length) increases”). In Toyama, the through-memory-level via structures and the “electrically conductive layers (146, 246)” run perpendicular to one another—i.e., vertical vias passing through horizontal layers—and thus the length or area of their proximity is de minimis.



Ex. 1005, Fig. 49 (excerpted and annotated to show the length of close proximity between a through-memory-level via structure and a conductive layer). Thus, Petitioner has not shown that replacing Toyama’s insulating liners with a dielectric fill material portion would reduce capacitive coupling, particularly where Toyama expressly “minimizes” it already. Furthermore, Dr. Lee and Petitioner have not explained why this particular capacitance is important for improving NAND performance, in light of the fact that this capacitive coupling is relatively very small when compared to the capacitive coupling between two adjacent word lines within a NAND stack.

117. Petitioner further argues that a person of ordinary skill in the art would have recognized that placing the through-memory-level via structures (the alleged TACs) in the memory array region 100 has certain benefits (Pet. 108-109), but Toyama’s Second Modification—the embodiment that Petitioner proposes modifying—already has through-memory-level via structures (the alleged TACs) in the memory array region 100. Petitioner is not proposing moving the alleged TACs. Thus, any benefits of having the alleged TACs in that particular location are irrelevant to whether a person of ordinary skill in the art would make a different modification, i.e., adding a unitary dielectric fill material as proposed by Petitioner.

118. Petitioner asserts that “elements of the [F]irst [E]xemplary [S]tructure and the Second Modification are compatible with each other” (Pet. 111; Ex. 1003,

¶¶236-239), but Toyama does not teach such compatibility or substitution between its embodiments. Rather, Petitioner's argument is based on nothing more than the conclusory testimony of Petitioner's expert. *See* Pet. 111 (citing Ex. 1003, ¶¶236-239). That a limited set of other, *different* structures may have the same name in both embodiments (*id.*) is irrelevant. Indeed, the issues discussed above demonstrate that the embodiments are not compatible. At the very least, they are not combinable in the way proposed by Petitioner.

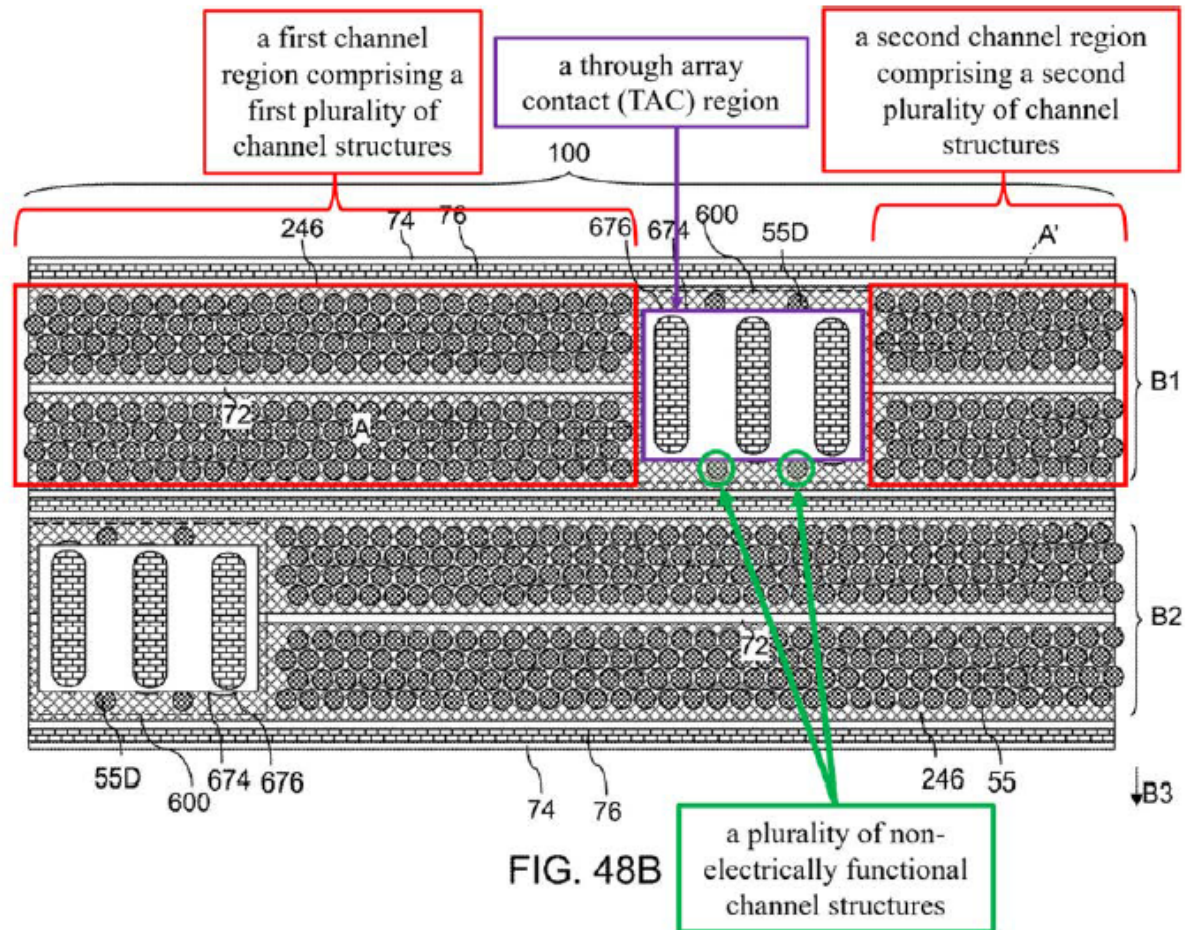
119. Petitioner's assertion that a person of ordinary skill in the art would have found the combination straightforward (Pet. 112-113, citing Ex. 1003, ¶¶184-197) relates to whether a person of ordinary skill in the art could *manufacture* the device, and do not address the lack of motivation to make the proposed combination, let alone the adverse impact that replacing the conductive word lines with an insulator would have. *See* Pet. 110 ("A POSITA also would have understood how to manufacture a device implementing the obviousness combination.").

120. Therefore, Petitioner has not shown that a person of ordinary skill in the art would have found it obvious to modify Toyama's Second Modification in the alleged manner.

B. Independent Claim 8: Petitioner’s Obviousness Combination Does Not Disclose or Render Obvious “a plurality of non-electrically functional channel structures surrounding the TAC region” (Limitation [8.h])

121. Petitioner’s Obviousness Combination also does not disclose or render obvious “*a plurality of non-electrically functional channel structures surrounding the TAC region*” as required by limitation [8.h] because Toyama’s alleged non-electrically functional channel structures do not surround the alleged TAC region.

122. For Ground 3, Petitioner relies on the teachings of only Toyama’s Second Modification (Ground 1) for the alleged plurality of non-electrically functional channel structures, and cross-references its analysis from Ground 1 in the Petition. *See* Pet. 123 (“The obviousness combination does not alter the Second Modification’s ‘dummy memory stack structures 55D.’ ... Thus, for the reasons explained in Ground 1, the obviousness combination renders obvious [Limitation [8.h]].”). Thus, for the same reasons discussed for Ground 1 (*see* §X.B) and as shown below, Toyama’s **dummy memory stack structures 55D** do not “surround” the alleged **TAC region**.



Ex. 1005, Fig. 48B (annotated by Petitioner, Pet. 120).

123. Therefore, Petitioner has not shown that the Obviousness Combination discloses or renders obvious “a plurality of non-electrically functional channel structures surrounding the TAC region” as required by limitation [8.h].

C. Claim 10: Petitioner’s Obviousness Combination Does Not Disclose or Render Obvious “an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the First and Second Channel Structures” (Limitation [10.b])

124. Petitioner’s Obviousness Combination does not disclose or render obvious “*an etch stop plug interposed between each local contact of the local*

contacts and each channel structure of the first and second channel structures”

as required by limitation [10.b] because, as with Grounds 1 and 2, Toyama’s alleged etch stop plugs are not interposed between each purported local contact of the local contacts and the channel structures.

125. In Ground 3, Petitioner relies on the Ground 1 arguments regarding Toyama’s Second Modification to attempt to meet the etch stop plug limitation [10.b]. Pet. 125 (“The obviousness combination does not alter any of the foregoing components in the Second Modification”). As I explain in §X.C, Petitioner’s Ground 1 arguments with respect to limitation [10.b] fail.

126. Therefore, Petitioner has not shown that the Obviousness Combination discloses or renders obvious limitation [10.b] for the same reasons I discuss for Ground 1.

II. CONCLUSION

127. For at least the reasons discussed above, it is my opinion that Petitioner has not demonstrated that the Challenged Claim of the ’806 patent are anticipated or obvious.

128. This declaration represents my opinions that I have formed to date on the specific issues for which I have been asked to opine and based on the material currently available to me. I reserve the right to supplement this declaration to address any new information offered by Petitioner or provided by the Board. Also,

I reserve the right to supplement this declaration insofar as Petitioner is permitted to supplement the record with any additional opinions or arguments.

129. I hereby declare that all statements made herein of my own knowledge are true and all statements made herein on information and belief were and are believed by me to be true, and that all statements herein were and are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code and that any such willful false statements may jeopardize the validity of the application or any patents issued thereon.

APPENDIX A

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University of California, Berkeley May 1984
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Professor of Electrical Engineering and Computer Science
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Gordon McKay Professor September 1997 - present
Associate Professor September 1994 - 1997
Assistant Professor September 1990 - 1994

Analysis, design and implementation of microelectronic circuits and VLSI systems.
Teaching and curriculum planning in electrical engineering and computer science.

Founder and Program Director September 2015 - May 2020
Master in Design Engineering at Harvard University
Collaborative 2-year degree program at Harvard Graduate School of Design and School of Engineering and Applied Sciences

HBS University Fellow and Visiting Professor September 2008 – May 2012
Harvard Business School
Research and teaching in disruptive innovation, technology transfer, and industry evolution.

Founder and CEO March 2000 – March 2008
Silicon7, Incorporated
Seongnam-si, Kyoungki-do, KOREA
Application Specific Memory products for mobile communications and computing platforms.

Science and Technology Board Member June 1998 – June 2001
Polaroid Corporation, Cambridge, Massachusetts
Evaluation of research and technology developments.

Consultant and Senior Fellow Hyundai Electronics Industries, Ichon, Korea Development of high performance CMOS image sensor technology for embedded image sensing and processing applications. Research on advanced DRAM design and merged memory logic (MML) technology for advanced computer systems.	August 1995 – March 2000
Consultant Hamamatsu Photonics K.K., Hamamatsu City, Japan Development of smart image sensors and CCD/CMOS analog charge-domain circuitry.	December 1993 - June 1998
Consultant Istituto per la Ricerca Scientifica e Tecnologica (IRST), Trento, Italy Research and development of advanced CMOS/CCD technology and circuitry.	June 1991 - December 1993
Consultant M.I.T. Lincoln Laboratory, Dr. Alice M. Chiang, Advisor Design and implementation of CCD image sensors and analog signal processors.	June 1988 - August 1990
Research Assistant M.I.T. Artificial Intelligence Laboratory, Professor Tomaso Poggio, Advisor Implementation of analog VLSI hardware for computer vision.	September 1987 - August 1990
Research Assistant M.I.T. Microsystems Technology Laboratory, Professor Charles G. Sodini, Advisor Development and characterization of low pressure ammonia and oxygen annealing process for improved reliability of scaled MOS transistors.	September 1984 - August 1987
Research Assistant U.C. Berkeley Electronic Research Laboratory, Professor Chenming Hu, Advisor Measurement and analysis of hot electron degradation in MOS transistors.	January 1983 - May 1984

Honors and Awards:

National Science Foundation Young Investigator Award	1992
Army Research Office Young Investigator Award	1992
Hertz Foundation Fellowship	1984 – 1990
National Science Foundation Fellowship	1984
University of California Alumni Scholarship	1980 - 1984
Phi Beta Kappa, Eta Kappa Nu, Tau Beta Pi	1984

Patents:

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In the matter of CERTAIN CONSUMER ELECTRONICS WITH DISPLAY AND PROCESSING CAPABILITIES, (ITC, Investigation No. 337-TA-885, deposition and trial) – retained by Toshiba

In the matter of CERTAIN GRAPHICS PROCESSING CHIPS, SYSTEMS ON A CHIP, AND THE PRODUCTS CONTAINING THE SAME, (ITC, Investigation No. 337-TA-941, deposition and trial) – retained by Nvidia

In the matter of US Patent 6,418,310 (US Patent and Trademark Office, Patent Trial and Appeal Board, IPR2015-05183, deposition) – retained by Ericsson Inc.

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