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Transcript of Jack Lee, Ph.D.

Date: January 30, 2025

Case: Micron Technology, Inc. -v- Yangtze Memory Technologies Company, LTD.,
(PTAB)

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

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Transcript of Jack Lee, Ph.D.
Conducted on January 30, 2025

1 (1 to 4)

1 UNITED STATES PATENT AND TRADEMARK OFFICE 2 BEFORE THE PATENT TRIAL AND APPEAL BOARD 3 MICRON TECHNOLOGY, INC.,) 4) 5 Petitioner,) 6) 7 vs.) Case No. 8) IPR2024-00791 9 YANGTZE MEMORY TECHNOLOGIES) 10 COMPANY, LTD.,) Patent 10,937,806 11) 12 Patent Owner.) 13 -----) 14 VIDEOTAPED DEPOSITION OF JACK LEE, PH.D. 15 VIA VIDEOCONFERENCE 16 THURSDAY, JANUARY 30, 2025 17 8:04 A.M. 18 19 20 21 22 23 Stenographically reported by: 24 Kayla Lotstein 25 California CSR No. 13916, CRR, RPR, CRC	3 1 APPEARANCES OF COUNSEL: 2 FOR PETITIONER: 3 ORRICK HERRINGTON & SUTCLIFFE LLP 4 BY: PARTH SAGDEO, ESQ. 5 Psagdeo@orrick.com 6 51 West 52nd Street 7 New York, New York 10019 8 (212) 506-5000 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 Also Present: 25 Parker Simpson, Videographer
2 1 UNITED STATES PATENT AND TRADEMARK OFFICE 2 BEFORE THE PATENT TRIAL AND APPEAL BOARD 3 4 MICRON TECHNOLOGY, INC.,) 5) 6 Petitioner,) 7 vs.) Case No. 8) IPR2024-00791 9 YANGTZE MEMORY TECHNOLOGIES) 10 COMPANY, LTD.,) Patent 10,937,806 11) 12 Patent Owner.) 13 -----) 14 15 16 17 18 19 20 21 22 23 24 25 13 VIDEOTAPED DEPOSITION OF JACK LEE, PH.D. taken 14 on behalf of Patent Owner, at 8:04 a.m., 15 Thursday, January 30, 2025, Via 16 Videoconference, before Kayla Lotstein, 17 Certified Shorthand Reporter No. 13916 of the 18 State of California, pursuant to Notice.	4 1 INDEX 2 WITNESS: JACK LEE, Ph.D. 3 EXAMINATIONS 4 Page 5 By Mr. Cross 8 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25

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EXHIBITS				VIA VIDEOCONFERENCE; THURSDAY, JANUARY 30, 2025			
No.	Description	Page		8:04 A.M.			
Exhibit A	United States Patent No. US 10,658,378 B2; Date of Patent: May 19, 2020	14		* * *			
				THE VIDEOGRAPHER: Here begins the videotaped			
				deposition of Jack Lee, Ph.D., in the matter of Micron			
				Technology, Incorporated, versus Yangtze Memory			
				Technologies Company, Limited, in the United States			
				Patent and Trademark Office, before patent and trial			
				appeal board, Case Numbers IPR2024-00791 and			
				PR2024-000911.			
				Today's date is 1/30/2025. The time on the			
				video monitor is 8:05 Pacific time.			
				The remote videographer for today is Parker			
				Simpson representing Planet Depos.			
				All parties of this video deposition are			
				attending remotely.			
				Would counsel please voice-identify themselves			
				and state whom they represent.			
				MR. CROSS: Allen Cross, Ropes & Gray, for patent			
				owner, YMTC.			
				MR. SAGDEO: Parth Sagdeo with Orrick Herrington			
				for Petitioner, Micron.			
				THE VIDEOGRAPHER: The court reporter today is			
				Kayla Lotstein representing Planet Depos. The witness			
				will now be sworn.			
6				8			
INDEX (CONTINUED)				THE STENOGRAPHER: Hello. My name is Kayla			
				Lotstein. My CSR number is 13916.			
PREVIOUSLY MARKED EXHIBITS				Jack Lee, Ph.D.,			
No.	Description			called as a witness on behalf of the Patent Owner, and			
Exhibit 1001	United States Patent No. US 10,937,806 B2; Date of Patent: March 2, 2021			having been duly sworn, was examined and testified as			
Exhibit 1003	Declaration of Jack C. Lee, Ph.D.			follows:			
Exhibit 1005	United States Patent Application Publication No. US 2017/0179026 A1; Pub. Date: June 22, 2017			EXAMINATION			
INFORMATION TO BE SUPPLIED				BY MR. CROSS:			
	Page	Line		Q Good morning, Dr. Lee. Could you please state			
	(None)			your name.			
QUESTIONS INSTRUCTED NOT TO ANSWER				A Jack Lee.			
	Page	Line		Q And what address are you currently located at?			
	(None)			A 5803 Westslope Cove, Austin, Texas 78731.			
				Q And can you provide us with what materials you			
				have in front of you, if any.			
				A Just a laptop.			
				Q Okay. And do you have any programs opened up			
				on the laptop?			
				A No.			
				Q Do you have any other screens in -- in your			
				room that you're in?			
				A Yeah. I have a monitor -- two monitors.			
				Q Okay. Connected to your laptop?			
				A Yes. Yes.			
				Q You understand that you are under oath today?			

9 1 A Yes. 2 Q And you understand that I'll be asking 3 questions, and you'll be answering them? 4 A Yes. 5 Q Okay. And I ask that you please wait for me 6 to finish, and then I'll try and wait for you to do the 7 same. 8 A Yes. 9 Q Is there any reason why you cannot testify 10 truthfully and fully today? 11 A No. 12 Q And if I ask you a question that you don't 13 understand, do you agree to ask for clarification? 14 A Yes. 15 Q If you don't ask for clarification, I'll 16 assume that you understand the question. 17 Is that fair? 18 A Yes. 19 Q Before we proceed, I'd like to go through a 20 couple of terms that we'll be using today throughout. 21 Did you file a declaration in IPR2024-00791 22 labeled Exhibit 1003? 23 A Can you -- is it possible that you upload 24 the -- my declaration? Because I don't remember the 25 page number or details at all.	11 1 A Yeah. Would you upload that, please. 2 Q I can upload that. 3 And, finally, are you familiar with US Patent 4 Publication Number 2017/0179026, which was filed by a 5 Mr. Toyama? 6 A Yes. 7 Would you mind uploading that too? 8 Q It's a larger file. It's -- should be there 9 now. 10 A Still uploading. 11 Okay. I have downloaded it. 12 Q Great. 13 And I'll be referring to this as the Toyama 14 reference. 15 Do you agree? 16 A Yes. 17 Q Great. 18 Can you please state what your consulting rate 19 for this IPR is? 20 A It's \$680 an hour. 21 Q Thank you. 22 And is that the same rate for all of your work 23 on these YMTC matters? 24 A Yes. 25 Q Dr. Lee, what did you do to prepare for
10 1 Q Sure. 2 Did you receive the document, Dr. Lee? 3 A Yes. 4 Q Great. 5 A Yes. I received it. 6 Q Great. 7 If I refer to this one as your first 8 declaration, you'll understand what I mean? 9 A Yes. 10 Q Great. 11 You also filed a -- what I refer to as a 12 second declaration in IPR2024-00911 also marked as 13 Exhibit 1003; is that correct? 14 A Yeah. 15 Q And I'll upload -- 16 A Yes. 17 Q I'll upload that one as well. 18 A Thank you, sir. Thank you. 19 I've received it. 20 Q Great. 21 And are you familiar with US Patent 22 10,937,806? 23 A Is this the one that we say is '806 patent? 24 Q That's correct. So I'll refer to that as the 25 '806 patent going forward.	12 1 today's deposition? 2 A I reviewed the four documents that you just 3 uploaded and I just downloaded, and I also review the 4 materials that I cited in each of the declarations in -- 5 in the sections "Assignment and Materials Considered." 6 I have also discussed with counsel about some 7 of the details of the four documents and the materials 8 cited in each of the declarations. 9 Q And about how long did you discuss these 10 materials with counsel? 11 A I don't recall the exact time -- length of 12 time. In the last few weeks, we have number -- several 13 meetings via Zoom, and -- but this is for both the 14 depositions -- in preparation for the deposition of the 15 '378 patent that took place on Tuesday of this week and 16 in preparation of the deposition of the '806 patent that 17 take place -- that are taking place right now. 18 Q When you reviewed your first declaration, did 19 you find any inaccuracies? 20 A No. 21 Q When you reviewed your second declaration, did 22 you find any inaccuracies? 23 A No, not that I can recall. 24 Q So these declarations reflect the opinions 25 you've formulated in these matters?

13 1 A Yes. 2 Q What materials did you consider in formulating 3 your opinions? 4 A As I mentioned, that -- the materials that I 5 have considered are listed in both of the declarations 6 in these sections of "Assignment and Materials 7 Considered." 8 Q You didn't consider anything outside of those 9 lists? 10 A The list -- the -- the table listed all the 11 exhibit, and as I discuss in the sections, I also review 12 and considered the '806 patent, Exhibit 1001, and its 13 prosecution history, Exhibit 1002, and the materials 14 listed in the table in the sections of "Assignment and 15 Materials Considered." 16 Q And that's true of both declarations; correct? 17 A That is correct. 18 Q And before you signed your declaration, did 19 you review either of the petitions? 20 A No, I did not. 21 Q Turning to the '806 patent, if you have that 22 up in front of you -- 23 A Yes. 24 Q -- on the cover at Code 63, it reads, 25 "Continuation of Application No. 16/047,182, filed on	15 1 the same specification? 2 A I had not compare side by side, but I believe 3 that the written descriptions and the drawing are very 4 similar, if not the same. 5 Q Thank you. 6 You filed declarations in IPRs challenging the 7 '378 patent; correct? 8 A Those are the IPRs that we discussed on 9 Tuesday; is that correct? Yes. 10 Q I believe so. 11 A Thank you, sir. 12 Q For terms that appear in both the challenged 13 '378 claims and the '806 claims, did you use the same 14 definitions? 15 A Can you repeat that, please. 16 Q For terms that appear in both the challenged 17 '378 claims and the '806 claims, did you use the same 18 definitions for those terms? 19 A I'm sorry. I'm not sure what you mean by 20 "definition." 21 Do you mean the claim construction? 22 Q Let me rephrase. 23 Are there any claim terms in which you applied 24 a different meaning in analyzing the '378 claims than 25 you applied in analyzing the '806 claims?
14 1 July 27, 2018, now Patent No. 10,658,378." 2 Did I read that correctly? 3 A Yes. 4 Q Do you understand what a "continuation" means? 5 A I might have discussed this in my declaration. 6 Can you hold on one second. 7 Let's see. I don't know if I have discussed 8 that. 9 Q Are you familiar with US Patent 10 Number 10,658,378? 11 A Yes. Hold on one second. Let me make sure 12 that's the number. 13 Can you upload that patent, please. 14 Q Sure. 15 A I'm pretty sure that's the one that we discuss 16 on Tuesday, but I just want to make sure. 17 MR. CROSS: I'm uploading what I've labeled as -- 18 or titled Exhibit A - US 10,658,378. 19 If I could have that marked as Exhibit A. 20 (Whereupon Exhibit A was marked for 21 identification.) 22 THE WITNESS: Yes. That's the '378 patent that we 23 discussed on Tuesday. 24 BY MR. CROSS: 25 Q Does the '378 patent and the '806 patent share	16 1 A As I explain in the "Claim Construction" 2 section of my declarations, in paragraph 72 to 74, that, 3 first of all, I'm not an attorney, and so I offer no 4 opinions on the law, but I understand the claim 5 construction is a matter of law. 6 And I have been informed that the words of the 7 claim are generally given plain and ordinary meaning 8 that the term or the phrase would have to a person of 9 ordinary skill in the art at the time of the invention 10 in view of the surrounding claim language, 11 specification, and file history. Those collectively 12 called intrinsic evidence or intrinsic record. 13 I also understand that the courts may consider 14 what is called the extrinsic evidence, such as expert 15 and inventor's testimony, dictionary, and other learned 16 treatises, collectively called extrinsic evidence or 17 extrinsic record, but that in my -- that those extrinsic 18 evidence are given less weight than the intrinsic 19 evidence. 20 So, in my opinion, the challenged terms or the 21 challenged claims do not require further construction 22 and can be afforded the plain and ordinary meaning for 23 the purpose of analyzing the prior art that I'm 24 conducting in both of those declarations. 25 Q So, to confirm, in both the '378 declarations

17 1 you filed and the '806 declarations you filed -- that 2 were filed, you applied the plain and ordinary meaning 3 of the terms that appear in the claims? 4 MR. SAGDEO: Objection. Form. 5 THE WITNESS: As I explained in this section, that 6 the challenged claim do not require further construction 7 and can be afford -- afforded the plain and ordinary 8 meaning for the purpose of the analysis of the prior 9 art. 10 And -- and, of course, as I discuss in this 11 section that the plain and ordinary meaning that the 12 terms would have to a person of ordinary skill in the 13 art at the time of the invention in viewed of the 14 intrinsic evidence and extrinsic evidence. 15 BY MR. CROSS: 16 Q Okay. I don't think the -- that answered my 17 question, which was whether or not you're applying a 18 different meaning to any of the terms that are in the 19 '378 declaration than in the '806 declaration when they 20 are using the same language. 21 MR. SAGDEO: Objection. Form. 22 BY MR. CROSS: 23 Q So can you please -- 24 A Is -- sorry. I was going to ask you the 25 question.	19 1 meaning in the '378 declarations versus '806 2 declarations. I don't recall, but -- there might be, 3 but I don't recall. I have not consider that question. 4 But the claim construction, or what you say, 5 the definitions, how I -- how I define the terms in 6 the -- in the claims are described in my declarations, 7 for example, the Declaration 1 in paragraph 72 to 75. 8 Q Thank you. 9 Dr. Lee, have you ever designed memory 10 devices? 11 A Yes. 12 Q Is density an important aspect of designing 13 memory devices? 14 A I believe that I have discussed that in my 15 declarations in the -- in the "Technology Background and 16 State of the Art." 17 For example, in Declaration 1, at various 18 places, I discuss that NAND offer a higher integration 19 density than NOR flash, and the construction and the 20 fabrication of the 3D NAND memory chips involves various 21 technique in order to construct a high-density storage 22 architecture. 23 So a person of ordinary skill in the art would 24 understand that memory density, or what is called the 25 integration density, is an important consideration in
18 1 Q Oh, go ahead. 2 A Is there a particular term that you're 3 thinking that I'm applying a different meaning? If so, 4 can you -- can you refer where it was -- where it is in 5 my declarations. 6 Q Right now, I'm asking if you're aware of any 7 terms where you applied a different meaning in one set 8 of declarations than the other set of declarations. 9 MR. SAGDEO: Objection. Form. 10 THE WITNESS: Do you mean Declaration 1 and 11 Declaration 2 for the '806 patent, or do you mean the 12 declarations of the '806 versus the declarations of the 13 '378 patent? 14 BY MR. CROSS: 15 Q Let's start with any differences between the 16 declarations of the '806 versus the declarations of the 17 '38 -- the '378 patent. 18 A As I mention, that the claim -- the claims do 19 not require further construction, can be afforded their 20 plain and ordinary meaning for the purpose of this 21 analysis of the prior art and also given -- in view of 22 the intrinsic and extrinsic evidence to a person of 23 ordinary skill in the art at the time of invention. 24 Having said that, I don't recall that -- I 25 don't recall the -- any terms that is given different	20 1 designing memory devices. 2 Q Can you tell me what affects integration 3 density in memory devices? 4 A Well, as I discuss in the sections of the 5 background -- "Technology Background and State of the 6 Art" in both of my declarations for the '806 patent, 7 that the memory density depends on various features of 8 the memory chip. 9 So, for example, it depends on the 10 architecture. There's mainly two types, the most common 11 types of so-called flash memory, NOR flash and NAND 12 flash. 13 NOR flash, commonly referred to as the 14 parallel architecture, whereas NAND flash are commonly 15 referred to as the series architecture. 16 As I mentioned just now, that -- and I discuss 17 here in the sections of "Technology Background and State 18 of the Art," that NAND flash offers a higher integration 19 density than NOR flash. So that's one thing that affect 20 the density of the -- of the memory chip. 21 And I also discuss other things that affect 22 your density. For example, in the old days, the NAND 23 flash is of two-dimensional, so-called planar 24 architecture. Planar means only an xy-plane. And 25 devices are fabricated -- devices, meaning the memory

21 1 cells, are fabricated on the surface of the memory chip. 2 So one of the ways to improve and increase the 3 integration density is to move from two-dimensional to 4 three-dimensional NAND flashes and -- so that the memory 5 flash -- memory cells arranged in a vertical, 6 cylindrical columns. 7 So those are some of the examples of how 8 density of memory chips can be increased. 9 Of course, another important attribute is -- 10 and I discuss that in the section, is the technology 11 itself, the fabrication technology that involve 12 patterning and etching. 13 And the etching technique, that's being 14 improved significantly over the years. For example, as 15 I discuss in my declarations, that the advent of dry 16 etching process, for example, so-called deep reactive 17 ion etching, have been used to allow etching with 18 high-aspect ratio and, therefore, increase the etching 19 capability as well, therefore, increase the integration 20 density. 21 So those are some of the effect -- that affect 22 the integration density of a memory chip. Of course, 23 there are a lot more than what I just discuss now, and 24 some of the details can be found in my -- in the 25 discussion sections of "Technology Background and State	23 1 per unit area. The larger the memory cells means that 2 for a given area of the chip, the lower the number of 3 memory cells you can pack into the area and, therefore, 4 the lower the integration density. 5 Is that what you were thinking related to 6 feature size? 7 Q That is. Thank you very much, Dr. Lee. 8 A Thank you. 9 Q When designing memory devices, is operation 10 speed an important aspect to consider? 11 A Yes. As I discuss also in the "Technology 12 Background," the signal speed is -- is an important 13 factors. 14 So, for example, as I discuss in the section, 15 that by reducing the length of the interconnects, the 16 through array contacts enhance the signal speed and 17 reduce the power consumption. So that is one of the 18 important considerations. 19 Another consideration is -- that affect your 20 speed of the device is the parasitic capacitance. Not 21 only parasitic capacitance affect the noise but also 22 affect the speed as well. 23 Q Why does the length of an interconnect affect 24 the signal speed? 25 A Well, the speed of a single transmission, you
22 1 of the Art." 2 Q Would feature size and the distances between 3 those structures affect integration density? 4 MR. SAGDEO: Objection. Form. 5 THE WITNESS: I believe -- when you say "feature 6 size," do you mean in -- in semiconductor field, feature 7 size means the equivalent of what is the smallest 8 dimension defined in a technology node? 9 Is that what you're referring to? 10 BY MR. CROSS: 11 Q I think I was referring to something more 12 general, as just the -- the sizes of the cells or the 13 sizes of particular structures within the memory device, 14 as those shrink, does that affect integration density? 15 A Yes. Obviously, that the size of the memory 16 cell depends on your capability -- the fabrication 17 capability that involve, as I mentioned, etching, 18 patterning, the use of hard mask, the use of what is 19 called a spacer etching, selective etching. And all 20 those are -- affect the size of the memory cells. 21 Now, obviously, the larger the size of each 22 memory cell, the lower the integration density of the 23 memory chip, because integration density, in the 24 simplest terms, is not exactly how it's defined, but you 25 can see that it's related to the number of memory cells	24 1 can think of it as how long does it take for an electron 2 to go from one place to another. The longer the 3 interconnects, meaning a wire, given everything else is 4 the same, one can imagine that it will take longer for 5 electron to go from input to output. 6 So by reducing the length of the interconnect, 7 for example, interconnects such as through array 8 contacts would enhance signal speed, is to -- is 9 described and discussed in my declarations in the 10 section that I mention, "Technology Background and State 11 of the Art." 12 Q And why would parasitic capacitance affect 13 signal speed? 14 A Have you heard of RC time constant? 15 Q I have, but if you could elucidate. 16 A Okay. So, in general, the speed of the chip 17 is also related to what is called the RC time constant. 18 R represent resistance, and C represent capacitance. 19 So within the chip, there's a lot of 20 capacitance between different electrodes, okay, that 21 basically give you a so-called capacitive -- capacitive 22 coupling. And as I discuss in the declarations, this 23 capacitive coupling not only can cause cross talk 24 between one conductive element to another conductive 25 element nearby, but because of the RC time constant,

25 1 that the speed of the chip can also inadvertently be 2 affected by this parasitic capacitance, "parasitic" 3 meaning "unwanted," capacitance. 4 Q So does this parasitic capacitance affect the 5 interconnects? 6 A I'm not sure I understand what you mean by 7 that. You mean did the interconnect affect the 8 parasitic capacitance? 9 Interconnect, depending on how they are 10 arranged, would result in very different value of 11 parasitic capacitance, not the other way around. 12 Q Sorry. 13 For clarification, you mentioned that there's 14 capacitive coupling between one conductive element and 15 another conductive element. 16 Is an example of these conductive elements 17 interconnects? 18 A Yes. Any conductive element, such as 19 interconnects, can have a signal, electromagnetically 20 induced voltage or current, in a different nearby 21 conductive element, such as interconnects. 22 So if your question is whether what I refer to 23 as conductive element can be interconnects, yes. 24 Interconnects are conductive elements; so, therefore, 25 capacitive coupling can occur between two neighboring or	27 1 It's describing the same phenomena. It's just 2 that the -- it's just that one is the -- when you talk 3 about capacitive coupling between two conductor, you can 4 think of it as the -- as proportional to the overlap 5 area and inversely proportional to the distance between 6 the two conductors. And so that's the net value of the 7 capacitive coupling, or sometimes they simply say the 8 total capacity and value. 9 But if you divide it by the area, then that's 10 the capacitive coupling per unit area, but they are both 11 describing the same phenomena. 12 BY MR. CROSS: 13 Q So we were talking about signal speed, and to 14 confirm, it's the total capacitive coupling that affects 15 signal speed; correct? 16 A When you say the "signal speed," do you mean 17 the signal speed of the transmission -- 18 Q Yes. 19 A -- or the signal speed of the memory device? 20 What do you -- what do you mean by "signal 21 speed"? 22 Do you mean the signal speed of the 23 transmission through the conductive layer or the signal 24 speed -- the net signal speed of the memory elements? 25 Q So when we started this conversation, you
26 1 nearby conductive element -- elements; and, therefore, 2 the capacitive coupling can also occur between 3 neighboring or nearby interconnects because 4 interconnects are conductive elements. 5 Q The longer the two interconnects are 6 neighboring each other lengthwise, would that increase 7 the parasitic capacitance? 8 A Well, the amount of capacitive coupling 9 depends on the distance between the two conductors. 10 Obviously, the closer the two conductors are, the higher 11 the capacitive coupling. In other words, the amount of 12 capacitive coupling is inversely proportional to the 13 distance between the conductors. 14 Now, obviously, if the conductors are very 15 short, okay, the amount of capacitive coupling will be 16 reduced, but the capacitive coupling per unit length is 17 only inversely proportional to the distance between 18 conductors, and the permittivity of the ambient, or the 19 dielectrics, separate the two conductors. 20 Q For clarification, capacitive coupling and 21 capacitive coupling per unit length are different terms; 22 correct? 23 MR. SAGDEO: Object to form. 24 THE WITNESS: I'm not sure what you mean by 25 "different terms."	28 1 mentioned that reducing the length of the interconnects 2 would reduce -- or would affect the signal speed of the 3 transmission, and that's what I'm referring to in my 4 question. 5 So to rephrase or to restate, is it the total 6 capacitive coupling that affects the signal speed? 7 MR. SAGDEO: Object to form. 8 THE WITNESS: Again, I have to clarify what -- when 9 I talk about "signal speed" earlier, I was referring 10 to -- you were asking me about the length of the 11 interconnect; and I said, yeah, by reducing the length 12 of the interconnect, for example, the through array 13 contact enhanced signal speed, as I describe in my 14 declarations, what I referred there is the signal speed 15 transmission through the -- through the wire. 16 And so if that's what you're referring to, 17 yes, it does. 18 BY MR. CROSS: 19 Q Does operating temperature affect the 20 operation speed of a memory device? 21 A I don't think I discussed that in my 22 declarations. 23 Is there something in my declaration that you 24 specifically want to ask? 25 Q No. My question is directed towards your

29 1 expertise in designing memory devices more generally. 2 A Well, in general, believe it or not, the -- 3 you would think that the higher the temperature, the 4 faster the electron would go. No. 5 Actually, because we're dealing with solid 6 state, due to various phenomena, the mobility of the 7 charge carrier, such as electrons, which is negative 8 charge, or holes, which is positive charge, reduces when 9 the operating temperature increase. So, therefore, when 10 the chip become hot, that the operating speed of the 11 circuit will degrade. 12 And that is why that -- if you notice, that 13 your laptop, your desktop all have cooling system, a fan 14 or sometimes even put it -- put some kind of 15 refrigerations, to make sure that the chip does not heat 16 up. And that's one of the reasons why -- that such 17 techniques, using heat sink, fan, refrigerations, to 18 make sure that the chips do not get too high of the 19 temperature. 20 So in answer to your question, that 21 semiconductor chips, the operation, including speed, 22 would degrade as temperature goes up. 23 Q What causes the operating temperature to go 24 up? 25 MR. SAGDEO: Objection. Form.	31 1 geometry and you increase the current current, which 2 means the current density increases, under the same 3 operation remain, everything the same, you just crank up 4 the current through a very -- through the same cross 5 section, then the current -- then the temperature would 6 likely to go up. 7 Does that make sense? 8 Q That makes sense. 9 But to rephrase, if you maintain the same 10 current but change the geometry so that the cross 11 section was smaller, temperature would also go up; 12 correct? 13 A It -- essentially, it depends on the current 14 density, not the current itself. 15 Q Okay. 16 A Again, simplifies it significantly. The 17 temperature of the chip not only depends on the current 18 density but also depends on what kind of dielectric is 19 surrounding the -- the interconnects, what kind of heat 20 sink do you have, and so on and so forth. 21 Q Understood. 22 When designing memory devices, is reliability 23 an important aspect? 24 A So, obviously, it is important. In fact, 25 related to -- to your temperature questions, that have
30 1 THE WITNESS: So this is what I teach in short 2 courses in -- in -- in industry as well as what I taught 3 at University of Texas for 35 years. 4 And so your question is, what causes the 5 temperature of the chip to go up? 6 Well, in general, silicon is what is called an 7 indirect bandgap material. So when electron are 8 conducting through the silicon, that the -- when 9 electron -- this is very detailed. But, in short, that 10 when electrons move around in the semiconductor, such as 11 silicon or germanium or silicon-germanium, temperature 12 would go up due to that indirect bandgap features of 13 silicon. 14 BY MR. CROSS: 15 Q Could increase in current density through the 16 conductive elements in the semiconductor cause 17 temperatures to go up? 18 A Well, it depends. It depends on many things. 19 It depends on if you increase the temperature -- 20 increasing the current. But if you increase the line 21 width or the thickness of the interconnects, then the 22 current density per unit area -- per unit area, the 23 cross section of the wire, remain the same, then the 24 temperature unlikely to go up. 25 However, if you maintain the same interconnect	32 1 high temperature, not only that affect your operations 2 of the memory chip; it also affects your reliability. 3 So, for example, on page 26, I discuss that -- 4 at the bottom of page 26 of my first declaration, that 5 during the device operation, dummy strings assist in 6 heat distributions within the memory array, thereby 7 reducing the local hot spots that can affect device 8 reliability. 9 Local hot spot means that the temperature 10 become hot locally. Okay? 11 And -- and, therefore, when you have local hot 12 spot, that can degrade your device reliability; and, 13 therefore, that -- the reason why I talk about that is 14 because reliability is an important considerations. And 15 that's part of my research and -- and studies and 16 teaching at University of Texas at Austin and also in 17 short course environment in industry. 18 Q Can you give me some examples of what causes 19 local hot spots. 20 A Well, as I discuss, that when you have -- for 21 example, when you don't use a dummy string in your 22 memory chip, that can cause -- you know, that can cause 23 a local hot spot. 24 And another example, as we discuss earlier, if 25 you apply high -- high current density through a

33 1 interconnect, you could -- you could have -- create a 2 local hot spot situation. 3 Those are the obvious examples of causes for 4 local hot spot. And there are various example, and I 5 talk about that in my classes, that if you have 6 nonuniform depositions of -- of devices, you know, such 7 as dielectric or metal wire, you could cause a increase 8 in -- in temperature. And if you don't apply enough 9 heat sink, that can cause local hot spot. And in case 10 of memory devices, you can have inadvertent 11 overprogramming of a cell that can cause local hot spot. 12 So there's various -- there -- I mean, if -- 13 if you like, you can come and take my course, and you 14 can learn all the -- all the things that I talk about 15 which can cause increase in local -- temperature 16 locally, also called a local hot spot. 17 Q Thank you, Dr. Lee. 18 If you have a conductor that suddenly gets 19 thin, where it gets thin, that's where you would expect 20 a local hot spot to form? 21 MR. SAGDEO: Objection. Form. 22 THE WITNESS: Would it -- how does it low -- 23 suddenly get thin? What do you mean by that? 24 BY MR. CROSS: 25 Q If the geometry is such that it's wide in some	35 1 give me the entire questions in details. 2 What is the cross-sectional area, what is it 3 made of, what is the surrounding regions, and so and so 4 forth. 5 BY MR. CROSS: 6 Q Okay. For a conductor, all things being 7 equal, would the local hot spot form where the current 8 density is greatest? 9 MR. SAGDEO: Objection. Form. 10 THE WITNESS: Again, it really depends on the 11 particular problems you're dealing -- you're working 12 with: What is the geometry of the -- of the device, the 13 cross section, the voltage that you apply, the 14 dielectric material that you use, and the conductive 15 material that you use, and the placement of these 16 materials? 17 And in order to answer your questions of would 18 the hot spot occurs at a spot where the local current 19 density is higher, it's not as simple as that. 20 That's -- that's why thermal management engineers -- 21 it's not just one engineers, but a team of engineers 22 to -- to deal with that. 23 BY MR. CROSS: 24 Q So I prefaced my question as, all other 25 aspects being equal, would the current density -- strike
34 1 spots and narrower in other spots, you would expect 2 local hot spots to form where it's narrower; correct? 3 MR. SAGDEO: Objection. Form. 4 THE WITNESS: Well, not necessarily. I mean, 5 that's such a general -- such a general statement that 6 that is not -- that's not always true, because when you 7 talk about a wire that is not uniform cross-sectional 8 area or a chip that is not uniform metal layer, it is 9 not a -- simple as you think it is, because when you 10 have a conductor buyer -- lines, whether it's a 11 conductive word lines or conductive bit line, if that 12 line has a smaller area, it's -- that's what you're 13 referring to -- the resistance is really -- depends on 14 various things. 15 For example, is the bottleneck remain the same 16 before you suddenly narrow the interconnect or -- and 17 after you -- you said suddenly narrow the wire? 18 It really -- it's not a -- a person of 19 ordinary skill in the art would understand that, you 20 know, if the bottleneck is -- remained about the same, 21 meaning that the part of conductor to which the current 22 is most concentrated or most restricted, then the 23 current density's about the same; and, therefore, you 24 might not have a local hot spot anyway. 25 So to answer your question, you really have to	36 1 that. 2 So I prefaced the question as, where all 3 things being equal, would the hot spot form where the 4 current density is greatest? 5 MR. SAGDEO: Objection. Form. 6 THE WITNESS: And I think at -- at the beginning of 7 this discussion, I already discuss that and I talk about 8 that in the -- in the -- in the discussions in my 9 declarations, that if you have two wires and one -- and 10 both wire are the same, same length, same cross section, 11 if you have -- pump more current through one wire, wire 12 number one, and pump less current to wire number two, 13 and assuming everything else remain the same, then the 14 temperature of the wire that carry higher current 15 density would likely be higher. 16 But, again, you really have to consider all 17 the details that you discuss, that we discuss, and so it 18 is -- it is not as simple as you imagine. But assuming 19 that everything remained the same, then, yeah, sure. 20 Two wire, one carry high current density, one 21 carrying less current density, then a person of ordinary 22 skill in the art would -- likely to conclude that the 23 temperature of the high current density will be higher. 24 But how much higher, it really -- it really depends on 25 the -- many things, including the surrounding ambient,

37 1 surrounding materials. 2 MR. CROSS: Dr. Lee, we've been going for a little 3 bit over an hour. 4 Would you like a short break, or we can 5 continue? 6 THE WITNESS: Sure. Let's take a short break. 7 MR. CROSS: Okay. 8 THE VIDEOGRAPHER: We are going off the record. 9 The time is 9:22. 10 (Recess was taken at 9:22 a.m. until 11 9:34 a.m.) 12 THE VIDEOGRAPHER: We are back on the record. The 13 time is 9:34. 14 BY MR. CROSS: 15 Q Hi, Dr. Lee. 16 Could you please turn to page 17 of your first 17 declaration. 18 A Page 17? 19 Q That's right. 20 A Paragraph 44? 21 Q That's right. 22 A Yes. 23 Q Can you see the top leftmost image, it labels 24 the yellow structure there as "channel (CH)"? 25 Is that correct?	39 1 components, where the yellow part is referred to as 2 "substrate," whether that's correct or not -- 3 That was your question; right? 4 Q That's right. Was that correctly labeled? 5 A Well, this is extracted from a textbook, "3D 6 Flash Memories Textbook." 7 And depending on how substrate are defined in 8 the textbook, which I don't recall -- I don't have it in 9 front of me, unless you have it -- that I'm sure that 10 the author would label it accordingly. 11 And if -- based on '806 explanation what a 12 substrate is, that a substrate is a material on which -- 13 onto which subsequent materials -- material layers are 14 added, or otherwise disposed. So -- and a substrate can 15 be a layer -- can include one or more layers therein 16 and/or can have one or more layer thereupon, thereabove, 17 and/or therebelow. 18 So I would think that here's the substrate, 19 that subsequent material layers are added and disposed, 20 and it can be a layer. So I don't have any reason why 21 it is not labeled correctly, but, again, it really 22 depends on what the textbook define a substrate is. 23 Does that make sense? 24 Q Do you agree that the structure labeled 25 "substrate" is also a channel?
38 1 A Yes. 2 Q Are all of those yellow structures different 3 channels? 4 A Yes. 5 Q In the next figure that's diagonal, is that 6 label of "substrate" correct? 7 A I have discussed what is a substrate, I 8 believe, in my declarations. Let's see. Apologize. 9 So in '806 patent, they explain what a 10 substrate is, in column 4, line 47 or so, that substrate 11 is a material that -- "onto which subsequent material 12 layers are added, or otherwise 'disposed.'" Right? 13 And then -- and then in column 5, '806, 14 row 10, '806 further say, "Substrate can be a layer, can 15 include one or more layers" -- "one or more layers 16 therein, and/or can" be -- "can have one or more layer 17 thereupon, thereabove, and/or therebelow." 18 And then further down, I believe in, yeah, row 19 49, in certain example, it says that, where array -- 20 "where the array device and a peripheral device are 21 formed on different substrates." 22 So the question you have -- 23 What page is that again? On page -- 24 Q 17? 25 A -- 17 -- sorry -- whether the diagonal	40 1 A This is a non-NAND gate -- NAND memory devices 2 or planar memory devices. So when the -- when the word 3 lines, which is the control gates, are turned on, it 4 will induce a channel near the surface of the substrate. 5 So the substrate is not -- the question is not 6 really a -- is not really a precise question because the 7 substrate is not a channel, but the channel, which is 8 the electrons that carry the current, is located near 9 the surface of the substrate. 10 So I'm not sure what you mean by, is the 11 substrate the channel? 12 The channel -- the channel is -- occurs within 13 a substrate near the surface, between the oxide and the 14 silicons near the surface, close to the oxide interface. 15 Q Previously, you agreed with me that the yellow 16 structures are different channels. 17 Are you saying that the yellow structures are 18 not channels? 19 MR. SAGDEO: Objection. Form 20 THE WITNESS: You mean the upper corner, left-hand 21 corner? 22 BY MR. CROSS: 23 Q That's correct. 24 A Well, I think that when I say that, yeah, 25 that's -- that's where the channel is, the channel is

41 1 occurring in the yellow regions near the silicon 2 dioxide/silicon interface. So, you know, roughly 3 speaking, you could say, well, that's -- that's the 4 channel. 5 To be more precise is where the channel 6 located. It's inside the yellow region near the 7 silicon/silicon dioxide interface. 8 Does that make sense to you? 9 Q Yeah, that makes sense. 10 Let's turn to page 21 of your declaration. 11 A 21. Okay. 12 Q Are you there? 13 A Yeah. 14 Q Okay. Sorry. 15 A No. I was waiting for your question. 16 Q You refer to this 3D NAND architecture as Bit 17 Cost Scalable architecture, BiCS; correct? 18 A Well, that's what it is known as. It's not my 19 reference. It is the -- what is known as the I -- Bit 20 Cost Scalable 3D NAND. 21 Q So can you explain what the meaning of "Bit 22 Cost Scalable" is. 23 A You mean why it is call "Bit Cost Scalable"? 24 Is that what you mean? 25 Q That's right.	43 1 green. 2 A Yeah. I don't recall exactly what it refers 3 to. It's been a while that I look at this. 4 And you said it's bit line select? Is that 5 what you're saying? 6 Q That is what I said, but why don't you tell me 7 what you think the top green feature is. 8 MR. SAGDEO: Objection. Form. 9 THE WITNESS: I -- it makes sense that -- it makes 10 sense that that might be that -- what it stand for, but 11 I'm not sure because maybe -- let me see. I think I 12 might have -- let me see if I talk about that. I'm 13 trying to see if -- oh, I probably have discussed that 14 in my declaration. Let me -- give me a minute. 15 Yeah. If you look at -- sorry. If you look 16 at page 18, that -- in Figure A, in fact, in Figure B 17 also, BLS stand for "Bitline Selector." Not bit line 18 select. "Bitline Selector." 19 BY MR. CROSS: 20 Q Can you explain to me what the functionality 21 of a bit line selector is. 22 A Well, bit line select -- selector is 23 responding -- is responsible for selecting and enable 24 the appropriate bit line within the NAND array. 25 So, therefore, it basically helps to control
42 1 A Well, if you -- I believe this is term by the 2 inventors of this architecture. 3 The primary goal of this architecture is to 4 deduce the Bit Cost while scaling the storage density. 5 So -- so, therefore, unlike planar devices, you have 6 stack memory that stacks vertically, and, therefore, it 7 increases the bit -- the bit density without stringing 8 the feature size, so that reduced the cost per bit. 9 And there are many other features of this 10 architecture, but I think that the reason why they call 11 it Bit Cost Scalable is kind of art they -- I know what 12 you mean, but -- but I think that it's related to reduce 13 the Bit Cost while scaling the density -- the storage 14 density. 15 Does that make sense? 16 I think that's what -- why they call that, but 17 I'm not quite sure. That's what it's known for, but I 18 believe that's what is -- the reason behind it is the 19 Bit Cost is reduced, meaning the cost per bit is 20 reduced, and the density is scale. 21 Q Thank you. 22 So the top green element is labeled the "Bit 23 Line Selector (BLS)"; correct? 24 A BLS -- the green part or the red part? 25 Q Capital B, capital L, capital S. So the top	44 1 which memory cell are access during -- during data 2 operations, such as read, program, and so on. 3 Q So returning to the figure at page 21, do you 4 agree that the bit line selector is divided into four in 5 the Y direction, one for each row of channels in the Y 6 direction? 7 A Yeah. So your individual line -- is that what 8 you mean? 9 Yeah. Sure. 10 Q Then in red, there are eight bit lines in the 11 X direction that connect to each of the rows of channels 12 in the X direction, respectively; correct? 13 A Eight bit lines. 14 So if you count the number of red lines on 15 the -- on the top in the Y directions, there are eight 16 bit lines. Eight separate bit lines. So, yeah, there's 17 eight of them. 18 Q And just for clarification, those eight are 19 lined up in the X direction; correct? 20 A Well, each bit line is in the Y direction, and 21 they are lined up in the X direction. 22 Q You see that there are multiple channel gates, 23 CGs, for selecting the cells at a particular layer in 24 the Z direction; correct? 25 A Yes.

45 1 Q Each of these channels -- strike that. 2 Each of these channel gates is a word line; 3 correct? 4 A I think you have the -- you use the wrong 5 terminology. CG does not stand for "channel gate." 6 Q Control gate. 7 A Yeah. If you look at page 18, CG stand for 8 "control gate." 9 So can you repeat your question, please. 10 Q Yes. I'll start over. 11 So there are multiple control gates, CGs, for 12 selecting the cells at a particular layer in the 13 Z direction; correct? 14 A That is correct. You can see that there's 15 number of layers -- of green layers in the Z direction. 16 Those are what is called the control gate or word lines. 17 Q These control gates are not divided in the 18 xy-plane; correct? 19 A What do you mean by "divided"? 20 Q So the top layer, the bit line selector is 21 divided into four; correct? 22 MR. SAGDEO: Object to form. 23 THE WITNESS: You mean the top bit line select -- 24 bit line selectors have discrete lines or, according to 25 you, there are four bit line selector, the green lines;	47 1 basically turn on the -- in the -- turn on the cells on 2 that plane. Right? 3 But you don't want to access all the -- all 4 the bit lines -- all the cells on that -- on the same 5 plane. You just want to access whether you want to do 6 the read or programming, that particular intersection 7 between the word lines and the bit line. Right? 8 If you want to access row 1, column 1 only, 9 right, then you turn on the word line of the first row, 10 but the turn ons all the -- basically apply voltage to 11 all the memory cells at the control gate of that -- on 12 that same plane. But you only want to access 13 column 1 -- row 1, column 1 in the -- the memory cell in 14 row 1, column 1; so, therefore, that the bit line has to 15 be discrete rather than on the same plane so that you 16 can individually access a particular column or, in other 17 words, a particular bit line. 18 Does that make sense? 19 If you don't -- if you do not have separate, 20 discrete word line -- bit lines for the bit line 21 selector, then you can individually select a particular 22 memory cells that you want to program or read or 23 whatnot, or erase. 24 Q Thank you. That was helpful. 25 Can you tell me typically what is -- what are
46 1 is that right? 2 BY MR. CROSS: 3 Q Right. 4 A That's your question? 5 Yeah, that there's four discrete bit line 6 selector lines. 7 Q And my question now is that the control gates 8 are not similarly divided; right? 9 A So your question is that -- whether the 10 control gates, or the word lines, in each of the four 11 word lines that showed, right, are just one plane 12 instead of individual discrete line. 13 That's your question; right? 14 Q That's correct. 15 A Yeah. That -- that is correct, that word 16 lines are just one plane. 17 Q So can you tell me the purpose of this 18 configuration, where the bit line selector is divided in 19 the Y direction, the bit lines themselves are divided in 20 the X direction, and the control gates are divided in 21 the Z direction? 22 A I don't understand. What do you mean by -- 23 you want me to explain how this works? Is that what 24 you -- you're asking? 25 So the bit line basic -- the word line	48 1 the thicknesses of these layers? 2 MR. SAGDEO: Object to form. 3 THE WITNESS: What do you mean? It really depends 4 on the technology node you're talking about. 5 BY MR. CROSS: 6 Q Okay. 7 A But what technology node are you talking 8 about? Are you talking about -- what year are you 9 referring to -- so -- 10 Q Generally -- oh. 11 A I mean, it really depends on what are the -- 12 you mean each individual gate -- control gate, the 13 green, and typical bit line selector control thickness? 14 Q So -- 15 A Is that what you mean? 16 Q -- looking at just the control gate layer, 17 what would be a typical thickness? Are we talking 18 millimeters? Microns? Nanometers? 19 MR. SAGDEO: Object to form. 20 THE WITNESS: What technology node are you talking 21 about? 22 BY MR. CROSS: 23 Q The technology node available at the time of 24 this publication. 25 A What publications?

49 1 Q Where you got this figure. 2 A Where I got the figures. So this is Aritome, 3 which is -- 2000- -- 2016. 4 I would have to look at a particular road map 5 that -- what it is, but I can tell you that typical 6 thickness, for example, word lines, not in millimeters, 7 in nanometers. 8 Typically, individual control gate material, 9 let's say made of tungstens, are in that -- you know, 10 less than -- again, it depends on the technology node. 11 I would say around 5 to 20 nanometer. I don't know. 12 I -- I -- you know, all these numbers can 13 really pinpoint a certain year, and so -- sorry. Let me 14 quiet the -- let me close the door so that the cat 15 doesn't cause too much trouble. 16 I apologize. Sorry. 17 So 2016, I would say closer to a little bit 18 higher than -- higher end of the 5 to 20 nanometer. 19 Q Thank you. 20 Moving on -- 21 A Again, I mean, I don't remember all those 22 number on top of my head. These are -- you can look up 23 quite easily, looking at the -- if I have -- if you -- 24 do you have the Exhibit 1014? I can -- I can look at 25 it? Because I -- I don't have it. If you can	51 1 BY MR. CROSS: 2 Q Okay. In your first and second declarations, 3 you included three grounds, all based on obviousness 4 over the Toyama reference; correct? 5 A As you can see in my declaration, in -- in the 6 table of context -- contents, that all three ground in 7 each declaration are based on Toyama's prior art. 8 Q Okay. Just to get some definitions aside, for 9 ground 1, you rely on the second modification to the 10 fourth exemplary structure. 11 Is it okay if I refer to this as the "second 12 modification"? 13 A Are you referring to the first exhibit -- the 14 first declaration? 15 Q I believe it's true in both declarations, but 16 we can focus on the first declaration. 17 A As I explain in paragraph 85 in the first 18 declaration, that Toyama's second modification of the 19 fourth exemplary structure, which I refer to as Toyama 20 second modifications. And, similarly, in paragraph 104, 21 said the same thing. So yeah. Since I did that in -- 22 in my declarations, so let's refer that as "second 23 modification" for shorthand. 24 Q And for ground 2, this is reliant on the first 25 exemplary structure depicted in Figures 1 through 17.
50 1 download -- upload it, I can look at it and tell you 2 what the thickness is. 3 Do you think that's necessary? 4 Q I think we can maybe leave that for later. 5 But it's fair to say that you wouldn't expect 6 the control gate to be less than 1 nanometer or greater 7 than 100 nanometers? 8 MR. SAGDEO: Object to form. 9 THE WITNESS: Again, I -- without looking at the 10 exhibit, I would not be able to tell you, but I would 11 say that it's likely to be 20 nanometer or less, but I 12 don't know because I was told that this is not a memory 13 test and you -- you know, I don't think -- you know, 14 this is almost like memory test. Right? 15 Unless I write -- have written it, the 16 thickness of different layers, I would have to have a -- 17 have the prior art in front of me to tell you what it 18 is. 19 So I would hesitate to tell you what it is at 20 a specific year at a specific time. It's specific 21 depending on the number of layers that is used in -- 22 in -- in the 3D NAND and -- so, in general, I can tell 23 you that, in general, they're not in millimeter range, 24 like you said; they're in nanometer range. And the more 25 advanced chip, in general, the smaller the dimension.	52 1 Okay if I refer to this as "Toyama's first 2 exemplary structure"? 3 A Sure. That's what I was -- that -- that's 4 what I refer to as -- in my declaration also. 5 Q And for ground 3, it's an obviousness 6 combination of Toyama's second modification and first 7 exemplary structure; correct? 8 A That is correct. 9 Q You don't argue that Toyama anticipates any of 10 the claims; correct? 11 A So as I explain in paragraph 85, for example, 12 that, in my opinion, when viewed and considered in light 13 of the knowledge of a POSITA, Toyama's second 14 modification renders claims 8 to 9 and 11 to 12 of the 15 '806 patent obvious. So I apply obviousness to 16 invalidate those claims, and I did not argue 17 anticipation in both of my declarations. 18 Q Focusing on Toyama's first exemplary 19 structure, is this a Bit Cost Scalable architecture? 20 MR. SAGDEO: Object to form. 21 (Reporter clarification.) 22 THE WITNESS: Oh, I -- sorry. I just -- I didn't 23 say anything. 24 I'm not sure it is your -- whether one can say 25 the Toyama is Bit Cost Scalable because Bit Cost

53 1 Scalable is a trademark. It's a trademarked term and -- 2 by Toshiba. So Toyama, looking at the '026 patent, is 3 SanDisk, but I believe that -- so your question is 4 that -- is Toyama's NAND structure a Bit Cost Scalable 5 structure? 6 Well, Bit Cost Scalable is a trademark term by 7 Toshiba and -- if I recall correctly, and Western 8 Digital, I believe. 9 So whether SanDisk -- even though Western 10 Digital acquired SanDisk at certain time, I don't know 11 whether SanDisk or Toyama will call this a Bit Cost 12 Scalable. 13 But in the background of Toyama, it does say 14 that ultra -- ultra high-density storage devices have 15 been proposed using three-dimensional (3D) stacked 16 memory stack structure, sometimes referred to as Bit 17 Cost Scalable (BiCS) architecture. 18 And this is a 3D NAND structure, but I don't 19 know what the trademark law is, whether at that time 20 Toyama would call this a Bit Cost Scalable device or 21 not, so -- but it is a 3D NAND stack memory cells -- 22 memory devices that Toyama describe in his '026 patent. 23 Not sure if I answered your question. 24 BY MR. CROSS: 25 Q So like the Bit Cost Scalable architecture in	55 1 paragraph -- for example, paragraph 52, a variety of 2 modification to Bit Cost Scalable architecture were 3 known, for example, the use of slit structure and -- and 4 perhaps dummy string structure and so on and so forth. 5 So I believe that the device -- that Toyama 6 describe 3D NAND flash memory, but whether it can be 7 call Bit Cost Scalable, I think, is more a business 8 term, a trademark. So I cannot answer you directly 9 whether they can be called Bit Cost Scalable because I 10 don't know the legal boundary between SanDisk and 11 Western Digital, and so -- but no matter what you call 12 it, it is a 3D NAND memory cells -- memory chips. 13 Q And is it fair to say that the Bit Cost 14 Scalable architecture in your background section and 15 Toyama's first exemplary structure would both have a bit 16 line selector that is divided in the Y direction? 17 A Yeah. As Toyama -- in paragraph 163, it talk 18 about bit line sensing, bit line -- and bit line decoder 19 circuits, and that the bit lines are overlaying the 20 array of memory stack structure as connected to the 21 drain-side end of the vertical semiconductor channels. 22 So -- yeah. So the first exemplary structure 23 has a number of bit line layers overlaying the memory 24 chip. 25 Q Turning to Toyama's second modification, like
54 1 your background section of your declaration, does 2 Toyama's first exemplary structure have a bit line 3 selector that's divided in the Y direction, bit lines 4 that are divided in the X direction, and channel gates 5 divided in the Z direction? 6 MR. SAGDEO: Object to form. 7 THE WITNESS: Where are you reading? 8 BY MR. CROSS: 9 Q I'm not reading. 10 I'm simply asking, do we have the same kind of 11 division of structures as what we discussed regarding 12 the Bit Cost Scalable architecture that was in your 13 background section? 14 A Yeah. They're very similar. But, once again, 15 they both are 3D NAND architecture. They both had 16 electrical contacts or an electrical connection formed 17 on top of the memory; and they both have source terminal 18 connected to low voltage, for example, ground; and 19 individual memory accessed by word line, typically 20 horizontal extensioned; and the word lines form 21 staircase structure and -- to be able to access to the 22 external peripheral circuit. 23 So in many ways, the device of Toyama are very 24 similar to Bit Cost Scalable architecture, but, as I 25 mention, that -- in my -- in my declarations, in	56 1 the Bit Cost Scalable architecture in your background, 2 does Toyama's second modification have a similar bit 3 line selector that is divided in the Y direction? 4 MR. SAGDEO: Objection. Form. 5 THE WITNESS: So as I describe in the section of 6 "Overview of the Prior Art - Toyama," first, again, we 7 have to remember that Toyama is a very lengthy 8 reference. It has 70 figures, and many have subparts, 9 and over 60 columns of text, and -- but I focus on two 10 structure, which is, like I said, that first exemplary 11 structure and second modification to the fourth 12 exemplary structure, which I refer to as the second 13 modifications. 14 And as I describe in paragraph 81 at 15 Figure 17C, right, represent the -- the first -- is one 16 of the figure that describe the first exemplar. 17 BY MR. CROSS: 18 Q Sorry. I -- 19 A And then Figure 49 is one of the key figures 20 that describe the second modifications. 21 Q So turning to Figure 49 of Toyama, can you 22 identify the bit line selector? 23 MR. SAGDEO: Objection. Form. 24 THE WITNESS: So the bit lines are labeled 103, the 25 bit lines that extend along the second horizontal

57 1 direction, which is perpendicular to the first 2 horizontal direction, hd1. Right? 3 So 103 is the -- the bit line -- the bit lines 4 and -- so yeah. So that's -- that's what a bit line is. 5 I don't think it shows the bit line selectors in these 6 figures. 7 BY MR. CROSS: 8 Q Is a bit line selector required? 9 MR. SAGDEO: Objection. Form 10 THE WITNESS: I don't understand what you mean, is 11 it required. 12 Required in what sense? 13 BY MR. CROSS: 14 Q For a functional memory device of this 15 structure, do you need a bit line selector? 16 A In Figure 49, for the Bit Cost Scalable device 17 by Toshiba, I believe they use the bit line selector as 18 we show in the figures before, and -- but not all the 3D 19 NAND architecture would require 3D NAND -- would require 20 bit line selector. So yeah. Some -- some require; some 21 don't. 22 Q So my question is more specific to what's 23 illustrated in Figure 49. 24 Does Toshiba's second modification need a bit 25 line selector in order to operate?	59 1 end is to isolate it from the bit line. Okay? 2 And SG- -- SGD is also known as bit line 3 select transistors, or upper select gate. And so, yeah, 4 the SGD, in general, could also mean -- is also known as 5 the bit line selector. 6 Q And this is the same thing as an upper select 7 gate; correct? 8 A What is the same as upper select -- you said 9 upper select gate? 10 Q Yeah. I'm looking at paragraph 48 of your 11 declaration. I think what you're saying is that the 12 drain-end select gate transistor is the same thing as a 13 bit line select transistor and an upper select gate. 14 A Yeah. It's also known as the upper select 15 gate. 16 Q So turning back to Toyama Figure 49, would the 17 upper select gate just be the topmost conductive layer, 18 270? 19 MR. SAGDEO: Object to form. 20 THE WITNESS: Say it again. I'm sorry. 21 BY MR. CROSS: 22 Q No, that's fine. Let me know when you're at 23 Figure 49. 24 A Are you looking at page 49 -- 43? 25 Q This is page 92, Figure 49 of Toyama.
58 1 MR. SAGDEO: Objection. Form. 2 THE WITNESS: Well, in general, 3D NAND memory 3 cells -- memory chips do not explicitly require a bit 4 line selector if, for example, it is a floating-gate -- 5 floating-gate-based devices. So the -- I believe that 6 the 3 -- the Toyama make use of floating-gate materials. 7 So if -- if that's the case, then it does not 8 need -- does not need a dedicated bit line selectors, 9 but it is selected by, you know, bit line routing, and 10 so it does not need a separate BLS transistor alone. 11 BY MR. CROSS: 12 Q If you turn to paragraph 48 of your 13 declaration. 14 A 48? 15 Okay. 16 Q You explain that the drain-end select gate 17 transistor, SGD, is also known as the bit line select 18 transistor. 19 Is this all the same as the bit line selector? 20 A Well, it's this -- different terminology. 21 Q Different terminology for the same function 22 and structure? 23 A So as I explained in the -- in that paragraph, 24 that -- that SGD, which is drain-end select transistors, 25 or S- -- SGC, is connected -- that at the string drain	60 1 A Oh, okay. Yeah. Which is, by my declaration, 2 page 43. 3 Is that right? 4 Q That's right. Yeah. Same figure. 5 So is the upper select gate the uppermost 6 conductive layer, 270, in Figure 49? 7 MR. SAGDEO: Object to form. 8 BY MR. CROSS: 9 Q Sorry. I think I got -- it's hard to see 10 these small numbers, but -- so let me rephrase the 11 question because the 270 is an insulating layer. 12 Would the topmost conductive layer in 13 Figure 49 be the upper select gate? 14 MR. SAGDEO: Object to form. 15 THE WITNESS: Wait. I don't understand. 270 is 16 insulated. 17 BY MR. CROSS: 18 Q Right. 19 So just beneath that is a conductive layer; 20 correct? 21 MR. SAGDEO: Object to form. 22 THE WITNESS: I -- what layer is that? 23 BY MR. CROSS: 24 Q I think it's a 242 layer -- or no. That's 25 a -- if we go to page 45 of your declaration --

61 1 A 45. 2 Okay. 3 Q -- you see that you've identified a number of 4 layers as an alternating conductor/dielectric layer 5 stack? 6 A Right. 7 Q Above that, what are those conductive layers? 8 A You mean the conductive layer 246 and 146? 9 Q I don't think that these layers are 10 specifically labeled, but you can see that you bracketed 11 a number of layers from 232 down to 132 as an 12 alternating conductor/dielectric layer stack; right? 13 A Yes. 14 MR. SAGDEO: Object to form. 15 BY MR. CROSS: 16 Q Do you see that above layer 232 are additional 17 conductor layers? 18 MR. SAGDEO: Object to form. 19 THE WITNESS: Yeah. I'm not sure if Toyama 20 described what they are. It might be -- it's just one 21 of space. It might be just word line. I don't know. 22 MR. CROSS: Okay. I think we can go off the 23 record. 24 THE WITNESS: Okay. 25 THE VIDEOGRAPHER: We are going off the record.	63 1 CERTIFICATE OF SHORTHAND REPORTER - NOTARY PUBLIC 2 3 I, Kayla Lotstein, Certified Shorthand 4 Reporter Number 13916 within the State of California, do 5 hereby certify; 6 That JACK LEE, Ph.D., the witness whose 7 deposition is hereinbefore set forth, was duly sworn by 8 me before the commencement of such deposition and that 9 such deposition was taken before me and is a true record 10 of the testimony given by such witness. 11 I further certify that the adverse party was 12 represented by counsel at the deposition. 13 I further certify that the deposition of JACK 14 LEE, Ph.D. occurred via videoconference on January 30, 15 2025, commencing at 8:04 a.m. PST and ending at 11:15 16 a.m. PST. 17 18 IN WITNESS WHEREOF, I have hereunto set my hand this 6th 19 day of February, 2025. 20 21  22 _____ 23 Kayla Lotstein, CA CSR, 13916 24 25
62 1 The time is 10:57. 2 (Recess was taken at 10:57 a.m. until 3 11:07 a.m.) 4 THE VIDEOGRAPHER: And we are back on the record. 5 The time is 11:07. 6 MR. CROSS: Hi, Dr. Lee. I -- thank you very much. 7 I have no further questions for you. 8 THE WITNESS: Thank you. 9 MR. SAGDEO: No redirect. 10 MR. CROSS: Great. 11 THE VIDEOGRAPHER: Okay. If there's nothing 12 further, this concludes the deposition of Jack Lee, 13 M.D. -- or Ph.D. The time is 11:07. 14 (A discussion was held off the record.) 15 THE STENOGRAPHER: Counsel, would you like to order 16 a certified copy? 17 MR. SAGDEO: For this transcript, just the sort of 18 standard final transcript. 19 (Proceedings concluded at 11:15 a.m.) 20 21 22 23 24 25	

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