

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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MICRON TECHNOLOGY, INC.,  
Micron  
v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,  
Patent Owner

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Case No.: IPR2024-00911  
U.S. Patent No. 10,937,806  
Issue Date: March 2, 2021

Title: THROUGH ARRAY CONTACT (TAC) FOR  
THREE-DIMENSIONAL MEMORY DEVICES

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**REPLY DECLARATION OF DR. JACK C. LEE**

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I, Dr. Jack C. Lee, declare as follows:

## **I. INTRODUCTION**

1. My name is Jack Lee. I have been retained on behalf of Micron Technology, Inc. (“Micron”) as an independent consultant in this proceeding before the United States Patent and Trademark Office (“USPTO”).

2. I have already submitted a declaration in this proceeding, which I understand to be Exhibit 1003. I refer to that declaration as my “Initial Declaration” and also cite simply as “Lee.” My Initial Declaration opined on claim 10 (“Challenged Claim”) of U.S. Pat. No. 10,137,806 (“the ’806 patent”).

3. A summary of my education, professional experience, and other qualifications is included within paragraphs 5-13 of my Initial Declaration, and in my CV (Exhibit 1004).

4. I have been asked to review the Patent Trial and Appeal Board’s Institution Decision (“ID”) (Paper 12), which instituted this IPR proceeding. I have also been asked to review the Patent Owner Response (“POR”) (Paper 15) filed by Yangtze Memory Technology Co. Ltd. (“Patent Owner” or “YMTC”), and the accompanying exhibits and declarations, and provide my opinions on some of the statements and arguments offered in YMTC’s materials. My opinions and the bases for my opinions are set forth below.

5. I am being compensated for my time at my standard consulting rate of \$680 per hour. My compensation is based solely on the amount of time that I devote to activity related to this case and is no way contingent on the nature of my findings, the presentation of my findings and testimony, or the outcome of this or any proceeding. I have no other financial interest in this proceeding.

6. In this declaration, which I may refer to as my “Reply Declaration,” I do not address every argument or opinion that appears in YMTC’s Patent Owner Response or in Dr. Yang’s declaration (Exhibit 2005, “Yang Decl.”) with which I disagree. Instead, I focus on arguments and opinions that are most likely to be relevant to the outcome of this proceeding. For this reason, the opinions that are expressed in this Reply Declaration are not exhaustive of my opinions regarding the unpatentability of the Challenged Claims. My opinions should be understood to be from the perspective of a person of ordinary skill in the art (“POSITA”) as defined in my Initial Declaration.

## **II. MATERIALS CONSIDERED**

7. In preparing this Reply Declaration, I reviewed and considered the following materials, along with any other materials referenced in the body of my Initial Declaration and this Reply Declaration:

| <b>Exhibit</b> | <b>Description</b>                                                                                                                                                                                           |
|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1001           | U.S. Patent No. 10,937,806 B2 to Tao et al.                                                                                                                                                                  |
| 1002           | File History of U.S. Patent No. 10,937,806 B2 to Tao et al.                                                                                                                                                  |
| 1005           | U.S. Patent Publ. No. 2017/0179026 A1 to Toyama et al. (“Toyama”).                                                                                                                                           |
| 1009           | CN109075169A Office Action, dated November 14, 2019                                                                                                                                                          |
| 1010           | Certified Translation of CN109075169A Office Action, dated November 14, 2019                                                                                                                                 |
| 1011           | CN109075169A Reexamination Decision, dated November 25, 2021                                                                                                                                                 |
| 1012           | Certified Translation of CN109075169A Reexamination Decision, dated November 25, 2021                                                                                                                        |
| 1013           | Michelsoni, “3D Flash Memories” (2016)                                                                                                                                                                       |
| 1014           | Aritome, “NAND Flash Memory Technologies” (2016)                                                                                                                                                             |
| 1015           | U.S. Patent Publ. No. 2018/0108671 A1 to Yu et al.                                                                                                                                                           |
| 1016           | U.S. Patent Publ. No. 2019/0229125 A1 to Zhou et al.                                                                                                                                                         |
| 1017           | U.S. Patent No. 10,354,980 B1 to Mushiga et al.                                                                                                                                                              |
| 1018           | U.S. Patent No. 9,293,348 B2 to Lai et al.                                                                                                                                                                   |
| 1019           | U.S. Patent No. 8,598,643 B2 to Kawasaki et al.                                                                                                                                                              |
| 1020           | U.S. Patent No. 8,697,519 B2 to Jee et al.                                                                                                                                                                   |
| 1021           | Excerpts from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)                                                                                                                             |
| 1022           | Print out of <a href="https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides">https://www.studycountry.com/wiki/what-is-a-piece-of-land-surrounded-by-water-on-2-sides</a> |

| <b>Exhibit</b> | <b>Description</b>                                                                                                                                                                    |
|----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1023           | Michelsoni et al., “Inside Solid State Drives (SSDs)” (1 <sup>st</sup> Ed. 2013)                                                                                                      |
| 1024           | U.S. Patent No. 10,043,558 to Shah et al.                                                                                                                                             |
| 1025           | Michelsoni et al., “Inside NAND Flash Memories” (2010)                                                                                                                                |
| 1026           | Lau, “Ball Grid Array Technology” (1995)                                                                                                                                              |
| 1027           | U.S. Patent No. 10,103,169 to Ge et al.                                                                                                                                               |
| 1028           | U.S. Patent No. 9,935,050 to Dunga et al.                                                                                                                                             |
| 1044           | Transcript of the Deposition of Woodward Yang, dated April 22, 2025, in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , Case Nos. IPR2024-00788, -00909 |
| 1045           | Woodward Yang, Deposition Exhibit 4, in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , Case Nos. IPR2024-00788, -00909                                 |
| 1046           | Woodward Yang, Deposition Exhibit 5, in <i>Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.</i> , Case Nos. IPR2024-00788, -00909                                 |
| 1047           | Transcript of the Deposition of Woodward Yang, dated April 24, 2025, in Case Nos. IPR2024-00791, -00911                                                                               |
| 1048           | Woodward Yang, Deposition Exhibit 2, in Case Nos. IPR2024-00791, -00911                                                                                                               |
| 1049           | Michelsoni et al., “Inside Solid State Drives (SSDs)” (2 <sup>nd</sup> Ed. 2018)                                                                                                      |
| 1050           | PCT Publication No. WO 2009/079014 A1 to Yang et al.                                                                                                                                  |
| 1051           | Additional excerpt from “Merriam-Webster’s Collegiate Dictionary,” Eleventh Edition (2014)                                                                                            |

| Exhibit | Description                                                                                                                                                                    |
|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1052    | Print out of <a href="https://gf.com/about-us/gf-in-the-community/stem-at-gf/glossary-of-terms/">https://gf.com/about-us/gf-in-the-community/stem-at-gf/glossary-of-terms/</a> |

8. As stated above, I also reviewed and considered the Board’s Institution Decision (Paper 12), issued on January 7, 2025; YMTC’s Patent Owner Response (Paper 15), filed on April 2, 2025; and the exhibits that YMTC submitted with its Patent Owner Response, including Dr. Yang’s declaration (Ex. 2005).

### III. UNDERSTANDING OF THE GOVERNING LAW

9. I am not an attorney but I have been instructed on and applied the law as described in my Initial Declaration.

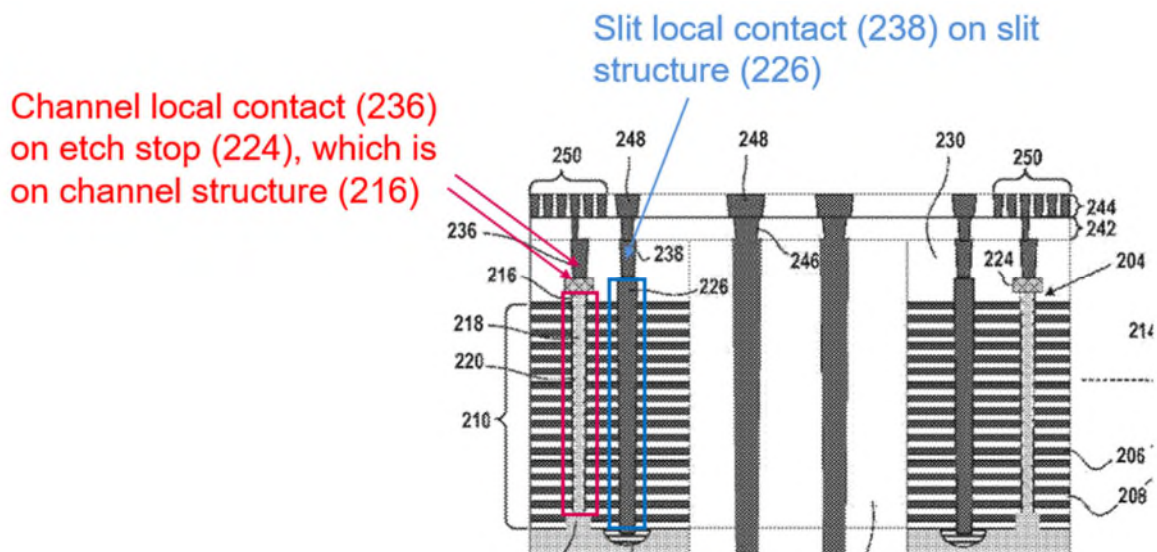
### IV. CLAIM CONSTRUCTION

#### A. “an etch stop plug interposed between each local contact of the local contacts, and each channel structure of the channel structures” (claim 10)

10. As I understand, Micron and YMTC’s dispute with respect to this limitation is whether the term “each local contact” refers to local contacts on the channel structures (Micron’s position) or refers to local contacts on the channel structures **and** on the slit structures (YMTC’s position). I agree with Micron’s position. A POSITA reading the limitation in the context of the claim as a whole and the specification would have understood that the claim requires etch stop plugs

between channel structures and the channel structure local contacts, and does not require etch stop plugs between channel structures and slit structure local contacts.

11. Before discussing the claim construction issue, I place the relevant claim terms in context. As shown below, the '806 patent discloses local contacts (236) for channel structures (216) and local contacts (238) for the slit structures (226). There are etch stops (224) only between the channel local contacts and the channel structures.



'806 patent, Figure 2 (partial), 11:28-30 (“As shown in FIG. 2, local contacts can include NAND string contacts 236, slit structure contacts 238, and WL contacts 240.”), 9:36-39 (“In some embodiments, each NAND string 204 includes an epitaxial layer 222 and an etch stop plug 224 at the respective bottom and top of NAND string 204, as shown in FIG. 2.”).

12. Notably, the '806 patent never discloses an etch stop on the slit structures. In fact, the Patent distinguishes the channels that have etch stops and slit structures that do not. '806 patent, 11:40-43 (local contacts connecting to channel etch stops and connecting directly to slits), 2:38-56 (only channels have etch stops), 9:36-53 (same), 15:61-16:15 (same), 17:53-62 (same). This is unsurprising, because the '806 patent defines the function of the “etch stop plug” as protecting the channel and serving as the channel’s drain: “As the name suggests, etch stop plug 224 is an etch stop layer that prevents etching of dielectrics in channel structure 216, such as SiO<sub>2</sub> and SiN, during subsequent etch operations. In some embodiments, etch stop plug 224 acts as the drain of NAND string 204.” *Id.*, 9:40-53.

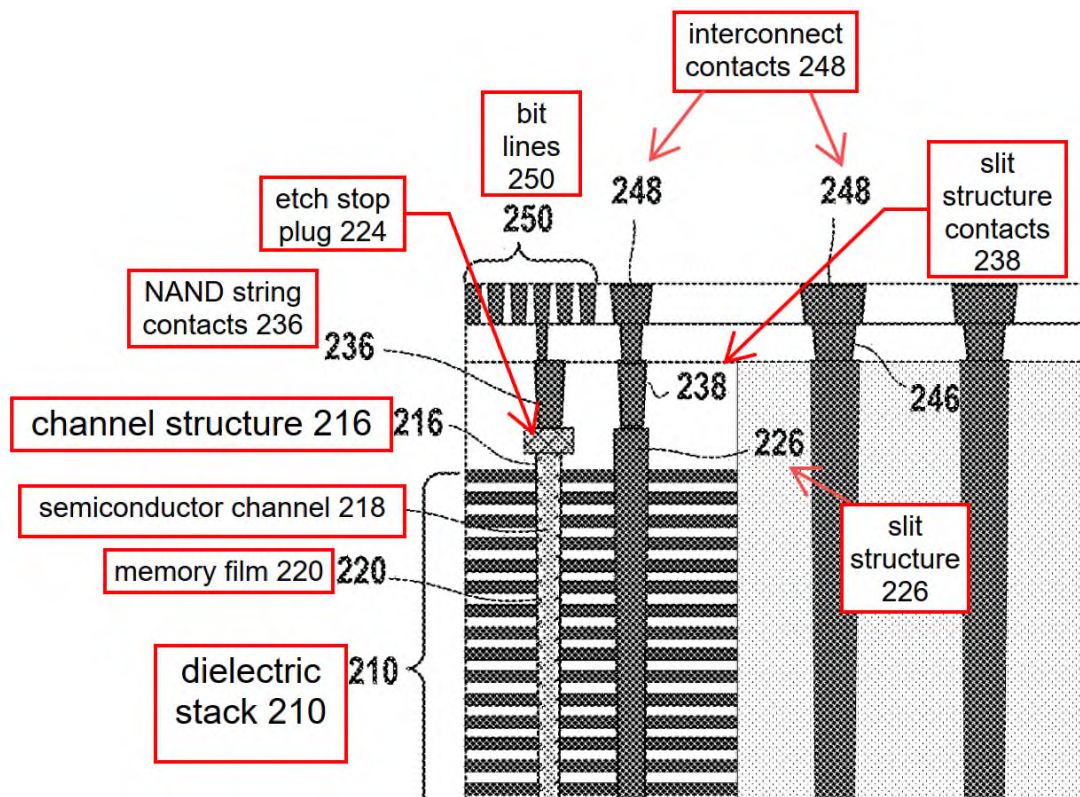
13. YMTC’s construction, which would require “etch stop plugs” between slit structure local contacts (“local contacts disposed on ... the slit structures”) and the “channel structures” is contrary to a POSITA’s understanding.

14. **First**, not a single embodiment of the '806 patent meets YMTC’s construction. The '806 patent repeatedly, consistently, and exclusively describes “NAND string contacts” (236) as the “local contacts” for the “channel structures” (216), and “slit structure contacts” (238) as the “local contacts” for the “slit structures” (226). '806 patent, 11:27-29, 11:38-43. The '806 patent’s “etch stop plugs” (224) are ***always*** described as being between the channel structure local

contacts (236) and the channel structures (216). *Id.*, 11:40-42. Indeed, the point of an “etch stop” is to protect **channel** structures; I agree with Dr. Yang that an etch stop plug on a **slit** structure is unnecessary because “the material composition of [slit structure] 226 in and of itself can stop the etch that required for the formation of [slit structure contacts] 238.” Ex. 1044 (4/22/25 Yang Dep.) 121:14-16; ’806 patent, 9:40-53 And the ’806 patent **never** identifies any “etch stop plugs” that are interposed between slit structure local contacts (238) and channel structures (216). YMTC’s construction, therefore, cannot be correct.

15. **Second**, YMTC’s assertion that there is ’806 patent embodiment meeting its construction is incorrect. YMTC’s argument is premised on its nonsensical assertion that “bit lines 250” are “local contacts disposed on ... the slit structures.”

16. As an initial matter, “bit lines 250” are not “local” contacts. Consistent with a POSITA’s general understanding, the ’806 patent explains that “local contacts” are “in physical and electrical contact with the various memory array structures disclosed herein, such as ... slit structures 226.” ’806 patent, 11:20-24. Thus, “the lower end of slit structure contacts 238 [i.e., the slit structure local contacts] can be in contact with the upper end of slit structures 226.” *Id.*, 11:38-43. As Figure 2 shows, “bit lines 250,” in contrast, are not in **physical** contact with “slit structures 226”:



*Id.*, Figure 2 (cropped, annotated). Nor are “bit lines 250” in **electrical** contact with slit structures 226; instead, they are in (indirect) electrical contact with channel structure 216. *Id.*, 12:7-10. That “bit lines 250” are not “local” contacts is confirmed by the ‘806 patent’s description of them as “interconnect contacts.” *Id.*, 12:7-10. The patent describes “local contacts” as distinct from “interconnect contacts.” *Id.*, 11:59-62. Indeed, bit lines are the very opposite of local to the slit structures: they are “in the top interconnect layer.” *Id.*, 5:46-48.

17. My deposition testimony is consistent with this understanding. I was asked: “And what is the function of the local contact recited in line 15 of the ’378 patent?” Ex. 2008, 66:1-3. I answered: “So in column 11 line 15, around 15, it

says that local contact is essentially provide a conducting layer with memory array structures, such as the NAND string 204, S-T-R-I-N-G-S, 204, slit structures 226, conductive layer or word line 206, and the staircase structure 212. So the local contact basically is an interconnect to connect the memory array structure to, for example, external -- external input, outputs.” *Id.*, 66:4-14

18. I was not asked for, nor did not I provide, a definition of the term “local contact.” And I did not state that every component electrically connected to a “memory array structure,” no matter how indirectly connected, is a local contact. On the contrary, the ’806 patent itself defines “local” contacts in relevant part as contacts that are “in direct contact with the memory array structures.” ’806 patent, 11:24-28.

19. **Third**, the plain claim language undermines PO’s interpretation. Independent claim 15 requires two sets of local contacts: (1) local contacts on channel structures, and (2) local contacts on slit structures. Dependent claim 18 then recites that there is “an etch stop plug interposed between each local contact of the local contacts and each channel structure.” Plainly, dependent claim 18 refers to the local contacts on the channel structures, not those on the slit structures, because it positions the etch stop above the channel structure and beneath the local contact (by its use of “interposed between”). A POSITA would

not have read the limitation at issue divorced from the rest of the claim and the specification, as YMTC seems to suggest.

**V. GROUND 1: TOYAMA’S SECOND MODIFICATION RENDERS THE CHALLENGED CLAIMS OBVIOUS**

**A. Limitation [8.G]: “a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure”**

**1. YMTC’s Implicit Claim Construction Requiring Multiple TACs To Extend Through A Single Dielectric Structure Is Incorrect**

20. A POSITA would have understood that, in the context of claim 8, the phrase “through array contacts” may refer to contacts that extend vertically through multiple dielectric structures. YMTC in effect asserts that claim 8 requires that multiple “through array contacts” extend through a single dielectric structure. POR 26-30. I disagree with YMTC’s position.

21. As I understand, in patent law “a” generally means “one or more” unless a POSITA would have understood a clear intent to limit the word “a” to a singular usage. In my opinion, a POSITA considering the intrinsic and extrinsic evidence of the ’806 patent would not find any clear evidence of intent to limit “a” to a singular dielectric structure. Instead, a POSITA would have understood that a

device according to the '806 patent might include multiple dielectric structures, each of which includes one through array contact.

22. The specification expressly provides that “terms, such as ‘a,’ ‘an,’ or ‘the,’ ... may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context.” ’806 patent, 4:17-25. A POSITA would have understood this passage to define “a” in such a way as to include plurals, reinforcing what I understand to be the general rule of patent law that “a” means “one or more.”

23. There is nothing about the context of the “dielectric structure” in the ’806 patent that would require multiple TACs extend through a single dielectric structure. As explained in my Initial Declaration, the purpose of the dielectric structure is to electrically isolate the through array contacts from each other and the alternating conductor/dielectric layer stack, through which the through array contacts extend. That purpose can be served by a unitary block of material (as disclosed expressly in the ’806 patent), and can also be served by multiple noncontiguous liners, each electrically isolating one through array contact.

24. Indeed, as explained above, a POSITA would have understood that the ’806 patent contemplates embodiments with multiple dielectric structures (each of which includes a single TAC), i.e., each TAC is isolated by its own dielectric structure. ’806 patent, 21:11-28.

25. I understand that Dr. Yang and YMTC contend that using a unitary block as a dielectric structure may offer some cost savings. Yang Decl. ¶ 66 (quoting '806 patent, 10:61-11:4). Dr. Yang, however, overlooks that forming a large unitary dielectric block typically involves depositing significantly more dielectric material than conformal liners and may require longer overall processing time — including deposition and planarization — compared to liner-based approaches. Dr. Yang also ignores the benefit of thin liners, which occupy less space and preserve more of the gate layers, offering advantages in layout density and electrical performance. Even accepting that assertion, a POSITA would have recognized that liner-based insulation is also a well-known, effective and desirable method for insulating through array contacts. Indeed, the '806 patent discloses the use of dielectric liners for this exact purpose, e.g., slit structures 226 are insulated with dielectric layer 1008. '806 patent, 16:66-17:4.

26. A person of ordinary skill in the art would have recognized that both liner-based and block-based dielectric insulation methods were well-known and viable techniques for electrically isolating through-array contacts (TACs) in 3D NAND structures. The Patent Owner argues in the context of Ground 3 that replacing Toyama's liner-based approach with a block-based dielectric fill is hindsight-driven and would eliminate a path used for current flow (POR 5, 58–60). That argument ignores the fact that the choice between these two insulation

approaches involves routine engineering trade-offs, not a rigid rule. As explained in my Opening Declaration (Lee, ¶¶ 160–166), a block dielectric structure offers the benefit of uniform and predictable isolation, particularly valuable in layouts where many TACs pass adjacent to vertically stacked wordlines, creating significant potential for cumulative parasitic coupling. A POSITA would have appreciated this trade-off and understood how to implement the block-based structure—by adjusting TAC placement, conductor routing, or via strategies—without compromising operability.

27. At the same time, a POSITA would have understood that liner-based insulation offers certain advantages, such as layout compactness and reduced material usage, which may be beneficial in scenarios where isolation requirements are less stringent. However, in the context of Toyama’s proposed combination—where multiple TACs are concentrated within a shared TAC region extending through an alternating conductor/dielectric stack—a unitary dielectric fill would serve the desirable function of electrically isolating the TACs in a predictable and process-compatible manner. This is not a hindsight reconstruction but rather a predictable design substitution, consistent with longstanding engineering practices and well within the capabilities of a POSITA. As with any engineering problem, each approach carries its own set of advantages and disadvantages, and the decision between them depends on how trade-offs are balanced to meet the

design's performance, manufacturability, and reliability goals. Accordingly, the motivation to implement a block-based dielectric structure in Ground 3's proposed modification is both reasonable and technically sound.

## **2. Under Micron's Construction, Toyama Renders Limitation [8.G] Obvious**

28. As I understand, YMTC's arguments regarding this limitation depend on its contention that multiple *through array contacts* must extend through a "singular" *dielectric structure*. POR 29. However, as I explained above, YMTC's implicit construction is improperly narrow. §V.A.1. If limitation [8.G] permits the *through array contacts* to extend through multiple *dielectric structures* (as the limitation should be interpreted), then Toyama's Second Modification teaches limitation [8.H]. Lee ¶¶ 132-136.

## **3. Limitation [8.G] Would Have Been Obvious Even under YMTC's Construction**

29. Even accepting YMTC's incorrect construction that multiple *through array contacts* must extend through a "single" *dielectric structure*, Toyama's Second Modification renders limitation [8.G] obvious. As I explained in my Initial Declaration, the "insulating liners 674" in Toyama function together and are

collectively understood by a POSITA to form a single *dielectric structure*.<sup>1</sup> Lee ¶ 113.

30. Importantly, the term “structure” does not require all its elements to be contiguous. For example, Merriam-Webster’s defines a structure as “something arranged in a definite pattern of organization.” Ex. 1021, 5.<sup>2</sup> Consistently with that definition, as YMTC’s own expert agreed, a structure such as the wall (pictured below) can consist of spaced-apart elements, i.e. its components are not all touching each other, and still be considered a structure:

---

<sup>1</sup> My opinion here is consistent with my view that each of the “insulating liners 674” is individually a structure, as Dr. Yang acknowledged when he stated that, “a structure ... can be composed of other structures.” Ex. 1044 (4/22/25 Yang Dep.), 43:25-44:2.

<sup>2</sup> Although my Initial Declaration focused on a different Merriam-Webster definition -- “something (as a building) that is constructed” -- I reference this additional definition because, in light of the parties’ arguments, it has become apparent that the earlier definition alone does not fully resolve the dispute.



Ex. 1045 (4/22/25 Yang Dep., Ex. 4); Ex. 1044 (4/22/25 Yang Dep.), 45:3-4, 47:3-6. Identifying the “wooden posts” as a “wall structure”). Similarly, the staircase below is considered a structure even though the stairs do not contact each other:



Micron Ex. 1043, p. 21  
Micron v. YMTC  
IPR2025-00911

Ex. 1046 (4/22/25 Yang Dep., Ex. 5). I understand Dr. Yang’s position is that there may be anchors embedded within the wall that are also form part of the staircase structure. But the point remains, even if those anchoring structures did not touch each other, this would still be a staircase **structure**. The definition of a structure focuses on functional arrangement, not physical continuity. In other words, a POSITA would understand that what qualifies something as a “structure” is not necessarily physical continuity, but rather functional arrangement and organization toward a common purpose—just as the steps collectively enable vertical movement despite being spaced apart.

31. As explained in my Initial Declaration, a POSITA would have understood “insulating liners 674” in Toyama’s Second Modification to be individually **and collectively** a dielectric structure:

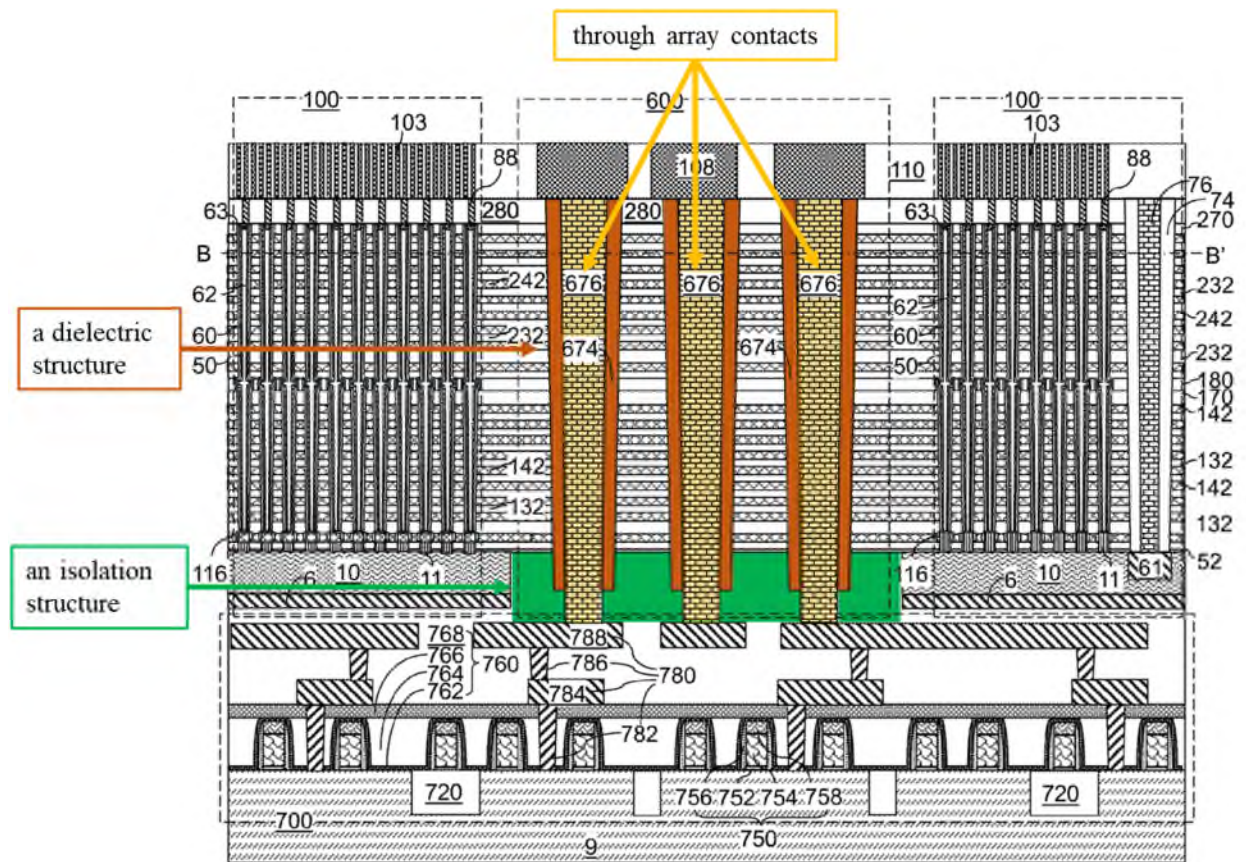


FIG. 49

Toyama, Figure 49 (annotated); Lee ¶¶ 132-136. Like the wall posts and staircase steps discussed above, each of “insulating liners 674” is arranged and organized in a definite and purposeful pattern. Importantly, all the liners perform the same function: insulating the *TACs* as they pass through the *alternating ... layer stack*. Lee ¶ 113. Thus, a POSITA would have understood that the “insulating liners 674” are collectively a (single) *dielectric structure* even though they may be physically separated. *Id.*

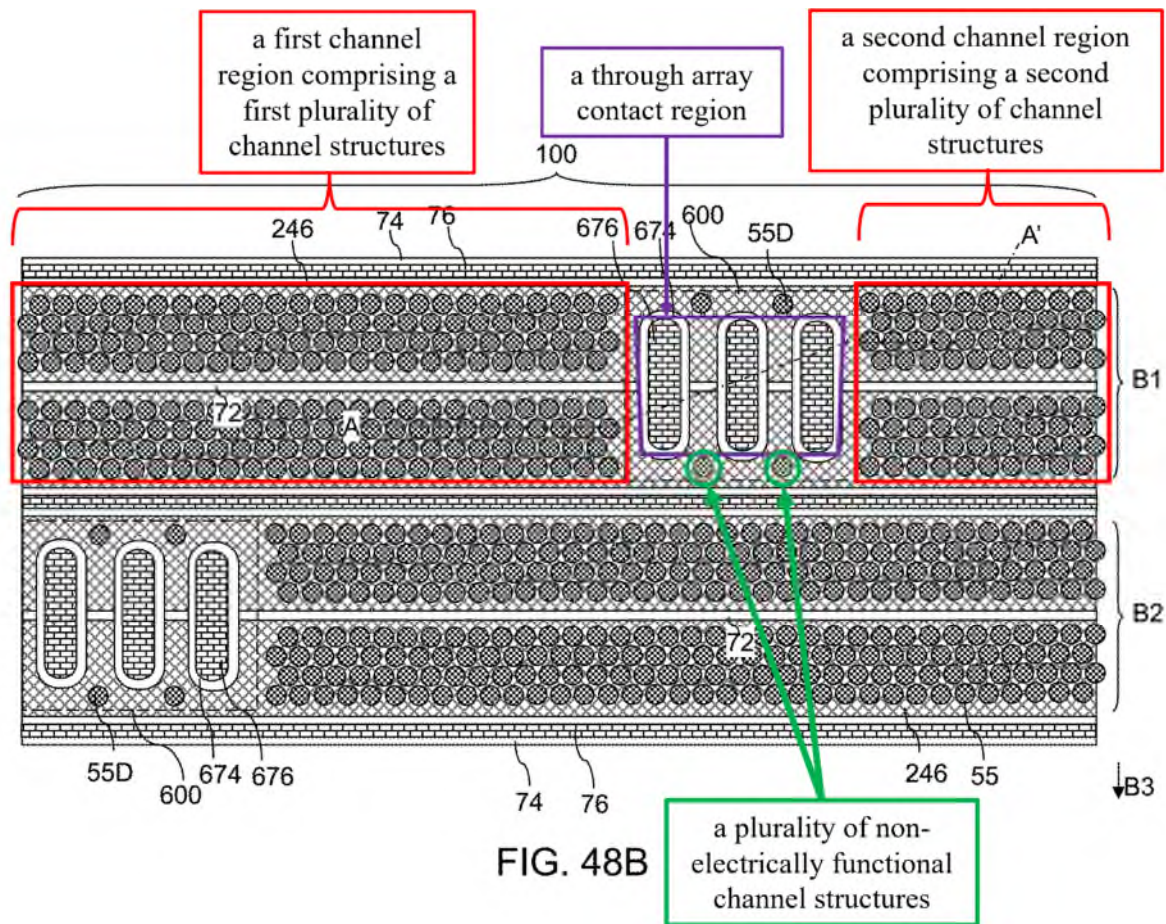
**B. Limitation [8.H]: “a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions”**

32. As I understand, YMTC’s only argument with respect to this limitation is that Toyama’s “dummy memory stack structures 55D” are not *surrounding* the indicated part of “through-memory-level region 600.” POR 31-

33. I disagree with YMTC’s position for several reasons.

**1. YMTC’s Argument Relies on a Construction of “Surrounding” Contrary to Its Plain Meaning**

33. In the mapping for Limitation [8.H] in my Initial Declaration, I annotated Toyama’s Figure 48B to show that a plurality of non-electrically functional channel structures (indicated in green) surrounding a through array contact region (indicated in purple)—even if one were to interpret the Figure literally and ignore the broader specification context (*see below*):



Lee ¶¶ 137-140, 251.

34. YMTC’s assertion that Figure 48B fails to teach the “surrounding” limitation [8.H] is inconsistent with the plain meaning of “surrounding.” YMTC asserts that because Figure 48B only shows *non-electrically functional channel structures* on only two sides of the *TAC region*, and therefore do not meet the limitation, i.e. YMTC contends that the structures are not *surrounding* the TAC region. POR 31-33. But the plain meaning of “surrounding” is not so limited. The term “surrounding” does not require enclosure on all four sides. Indeed, YMTC ignores intrinsic and extrinsic evidence establishing that one structure may

surround another even if it is situated on just two sides. Lee ¶ 137. A POSITA would have understood this broader, conventional usage of the term “surrounding.”

**2. YMTC Ignores Toyama’s Disclosure That Its Non-Electrically Functional Channel Structures Are “Provided at the Periphery” of Its TAC Region**

35. As my Initial Declaration explained, Toyama’s statement that “[d]ummy memory stack structures 55D can be provided at the periphery of the through-memory-level via region 600,” which a POSITA would have understood to mean to mean these *non-electrically functional channel structures* may be located on four sides of the *TAC region*. Lee ¶ 139. YMTC fails to respond to this point. I agree with Dr. Yang, who testified that the periphery of a rectangle, such as the *TAC region* shown, is “the four sides of the rectangle.” Thus, Toyama’s disclosure supports the conclusion that the dummy memory stack structures surround the TAC region, even under YMTC’s unduly narrow interpretation of “surrounding”: Ex. 1047 (4/24/25 Yang Dep.) 24:7-10. I also note that a POSITA would have understood the dummy channels (i.e., non-electrically functional channels structures) would be located to on the left and right of the purple box shown above. Due to well-known edge effects in semiconductor processing, it is prudent to end an array of channels with rows or columns of dummy channels, ensuring that the functional channels are, in fact, functional. It was standard practice to include dummy channels at the boundaries of functional channel arrays

to mitigate edge-related non-uniformities—such as etch distortion, implant variability, or lithography irregularities—and to protect the electrical performance of the interior functional channels. This understanding is consistent with Toyama’s disclosure of dummy channels being placed along the peripheral of the TAC region.

### **3. YMTC Ignores My Alternative Obviousness Argument**

36. As I explained in my Initial Declaration, even if a POSITA did not understand Toyama’s disclosure to contemplate placing *non-electrically functional channel structures* on four sides of the *TAC region*, a POSITA would have found it doing so an obvious and “highly predictable” use of prior art elements according to their established functions. Lee ¶ 140. Again, an additional benefit is to mitigate the well-known edge effect, which I discuss immediately above.

## **VI. GROUND 2: TOYAMA’S FIRST EXEMPLARY STRUCTURE RENDERS THE CHALLENGED CLAIMS OBVIOUS**

37. In my Initial Declaration, I explained that a POSITA would have arrived at limitation [8.G] by implementing multiple planes of Toyama’s first exemplary structure. Lee ¶¶ 167-184, 192-197. I disagree with YMTC’s arguments against this obvious modification for the reasons explained below.

**A. Limitation [8.G]: “a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure”**

38. My Initial Declaration explained that a POSITA would have found it obvious to implement a device including multiple planes of Toyama’s first exemplary structure, in part because of the common use of planes in flash memory devices and the well-recognized performance benefits of doing so. Lee ¶¶ 179-182. I further explained that a device implementing two planes of Toyama’s first exemplary structure meets each limitation of every Challenged Claim (including limitation [8.G]). *E.g.*, Lee ¶¶ 183-184, 192-197.

39. As I understand, YMTC raised two counterarguments in response. First, YMTC asserts that the proposed modification would result in two devices, and YMTC contends that the claim requires a single device. POR 39-40. Second, YMTC asserts that the proposed modification would result in a nonfunctional apparatus. POR 40. I disagree with both arguments for the reasons discussed below.

**1. YMTC’s Argument That an Apparatus with Two Planes Is Not “a Device” Is Meritless.**

40. YMTC’s argument that the proposed modification would not be “a device” rests on a flawed interpretation of the term “device” from the perspective of a POSITA.

**a. A flash memory device with two planes is still a “device.”**

41. The preamble of claim 8 recites “[a] three-dimensional (3D) memory device, comprising” a number of recited elements. The proposed modification that are discussed in my Initial Declaration is “to implement multiple memory planes in *a 3D memory device.*” Lee ¶ 171. YMTC does not dispute that a POSITA could implement multiple planes of Toyama’s first exemplary structure. Instead, YMTC asserts that such a configuration is not “a device.” POR 43-44. I disagree.

YMTC’s understanding of “device” lacks support from the claim, the specification, or the extrinsic record.

42. The ’806 patent’s definition of “3D memory device” is “a semiconductor device with vertically-oriented strings of memory cell transistors (referred to herein as ‘memory strings,’ such as NAND strings) on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate.” ’806 patent, 5:30-37. The proposed modification meets this definition.

43. As an initial matter, Toyama’s first exemplary structure meets the ’806 patent’s definition of “3D memory device.” Indeed, Toyama’s title is “Through-Memory-Level Via Structures for a Three-Dimensional Memory Device.” Toyama expressly states that its “embodiments ... can be employed to form various semiconductor devices such as three-dimensional monolithic memory array devices comprising a plurality of NAND memory strings.” Toyama, [0156]. And Toyama states that its disclosure is “directed to three-dimensional non-volatile memory devices, such as vertical NAND strings.” *Id.*; *see also* Toyama, Figure 17A (showing “memory stack structures 55” extending in a vertical direction with respect to the substrate).

44. The proposed modification retains these defining characteristics and nothing about the proposed modification takes it outside of the ’806 patent’s definition. Each individual plane is fabricated in exactly the same way as in Toyama’s first exemplary structure, resulting in “vertically-oriented strings of memory cell transistors” “on a laterally-oriented substrate.” And the proposed modified structure remains a 3D “semiconductor-based” memory device, as defined by the ’806 patent. That is true for all the same reasons as explained above and in my initial declaration, which discussed these components of Toyama’s first exemplary structure in detail. *See generally* Lee § IX.C (Ground 2).

45. YMTC’s argument that the proposed modification is not a (singular) “device” is mistaken. Under the plain meaning of “device,” which a POSITA would have understood to apply in the context of the ’806 patent, it is “a piece of equipment or a mechanism designed to serve a special purpose or perform a special function.” Ex. 1051, 3 (MW definition of “device”). Thus, a device can comprise other devices.

46. The ’806 specification uses the term “device” consistent with its plain meaning. It contemplates that one “device” can be part of another “device,” and that a device can even include multiple substrates.<sup>3</sup> ’806 patent, 7:53-57 (“3D

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<sup>3</sup> If YMTC were to argue that the proposed modification is not a “device” because it involves a different substrate, that would be incorrect. First, the ’806 patent explicitly contemplates a “device” comprising multiple substrates. ’806 patent, 7:53-57. Moreover, a POSITA would have understood how to fabricate a 3D NAND flash device with multiple planes on a single substrate -- e.g., on a single die formed from a single wafer. Ex. 1023 (Micheloni 2013), at p. 247 (describing a “die” containing multiple planes); Ex. 1052 (<https://gf.com/about-us/gf-in-the-community/stem-at-gf/glossary-of-terms/>) (single wafer comprises multiple dies); Lee ¶¶ 141-144 (collecting examples).

memory device” includes an “array device” and a “peripheral device,” and a device may comprise multiple substrates).

47. That a NAND flash memory with two planes remains a single “device” is confirmed by extrinsic evidence. For example, the Micheloni 2013 textbook notes that a “NAND flash storage **device**” may comprise “multiple chips,” each “chip” comprising multiple “sub-chips or dies,” and each “sub-chip might have **multiple planes**.” Ex. 1023 (Micheloni 2013), at p. 247 (emphasis added); Ex. 1049 (Micheloni 2018), at p. 357; *see also* Ex. 1014, at p. 313 (“3D V-NAND flash memory device” comprises “two planes”).

48. Micheloni also describes a “memory array” that has been “split in two independent planes.” Ex. 1023, at p. 144. Recall from the ’806 patent that the “memory array” (“also referred to herein as an ‘array device’”) is a “component[]” of the “3D memory device.” ’806 patent, 5:38-41, 7:53-57. It thus follows that “independent planes” are part of a single “3D memory device.”

49. Further, a patent from Dr. Yang describes a NAND flash device as having multiple planes. Ex. 1050 (WO 2009/079014), [038] (“[I]t may be possible to increase the writing throughput up to 60 MB/s (or more) with **3 devices** of SLC NAND flash (**six planes** ...).”) (emphasis added); *id.*, Figure 5 (showing two planes per device). The additional planes simply allow access operations to occur in parallel. It would make little sense to consider the planes as separate “devices,”

because there is a single flash device that executes a unified access operation by coordinating parallel activity across its planes—each plane performing a portion of that operation. The operation is initiated and completed by the device, not independently by each plane. Thus, a POSITA would not describe each plane as a separate device, consistent with the extrinsic evidence discussed above.

50. What’s more, at deposition, Dr. Yang acknowledged—and I agree—that the following “solid-state drive” (SSD) is a “device”:



Ex. 1048 (4/24/25 Yang Dep., Ex. 2); Ex. 1047 (4/24/25 Yang Dep.), 11:24-12:10. It was well-understood that an SSD may include multiple planes. Lee ¶¶ 172-178. It follows that a single “device” may include multiple flash memory planes.

51. Although YMTC asserts that forming a TAC region “between the first and second channel regions ... provides the benefit that [the] TACs are closer to

[the] memory device components, and interconnect routing may be shortened,”

YMTC’s assertion is both incorrect and irrelevant. POR 43-44.

52. **First**, the passage of the specification on which YMTC relies does not describe, nor would a POSITA understand, the benefit of “shorten[ing] interconnect routing” to be limited to placing a TAC region between channel structures in a single plane. That passage of the ’806 patent states that “TACs 234 can carry electrical signals from and/or to 3D memory device 200, such as part of the power bus, with shorten[ed] interconnect routing.” ’806 patent, 11:8-10. A POSITA would have understood that these benefits could be achieved whether the TACs are in a memory region, a word line region, or another region. In other words, neither the claims nor the cited specification passages suggest that this benefit is a required feature of the invention. In fact, the ’806 patent includes embodiments in which the TACs are not between channel regions. *See, e.g., id.*, Figure 1C. Moreover, a POSITA would not have understood the claims to expressly recite this purported benefit. Nor would a POSITA have seen any clear statement in the specification or prosecution history that that would justify requiring the word “device” to be narrowed to a single-plane device.

53. **Second**, YMTC does not dispute that the use of multiple planes improves performance, which would have independently motivated a POSITA to implement multiple planes in Toyama’s first exemplary structure. This

performance benefit is distinct from, and additive to, any advantages associated with shortening interconnect routing.

**b. The Claim Is Not Limited to a Single “3D Memory Device”**

54. Even if the word “device” were understood to exclude multi-plane devices, the combination still renders claim 8 obvious because it is not limited to a single “device” for two different and independent reasons.

55. **First**, a POSITA would have understood that the claim’s preamble is not limiting. I have been instructed that, under patent law, a preamble is not limiting when the body of the claim recites a structurally complete invention and the preamble merely state a purpose or intended use. In this case, claim 8 recites a structurally complete memory architecture that does not rely on the preamble for completeness. A POSITA would have recognized this and therefore would not interpret the preamble as limiting the claim to a single device.

56. **Second**, a POSITA would not have understood that “a” here must be limited to the singular. As I understand, “a” is construed in patent law to mean “one or more” absent some clear intent to limit the word to the singular. But, here, there is no lexicography, disclaimer, or anything about the structure or purpose of the claimed device that would require it to consist only of a single plane. On the contrary, as I explained in my Initial Declaration, a POSITA would have known

that there would be benefit in using Toyama's first exemplary structure to implement a multi-plane device. Lee ¶¶ 172-182.

**2. A POSITA Would Have Been Able to Make the Proposed Combination Functional**

57. A POSITA would have been able to make the proposed combination functional in view of the longstanding use of planes in flash memory devices (which had peripheral circuitry) well before the '806 patent. My Initial Declaration included a lengthy discussion, supported by extrinsic evidence, demonstrating that a POSITA would have understood how to implement a flash memory device (like Toyama's first exemplary structure) with multiple planes. Lee ¶¶ 172-182.

58. As summarized in the Institution Decision, "a POSITA would have had a reasonable expectation of success in implementing multiple planes of Toyama's First Exemplary Structure in the hd1 direction because NAND devices having multiple planes existed for many years before the priority date of the '806 patent and that implementation of such a structure would have been straightforward as it merely applies a known technique (implementing multiple planes of [a] NAND flash memory array) to a known device (Toyama's first exemplary structure) to yield predictable results (a NAND flash device with improved performance)." ID, 30.

59. A POSITA would have been motivated to implement multiple planes of Toyama’s first exemplary structure for the well-known performance and reliability benefits. Lee ¶¶ 172-182. And a POSITA would have had a reasonable expectation of success in doing so. *Id.* I should note as an initial matter that “peripheral circuitry” has been a fundamental aspect of memory design since the inception of semiconductor memory, referring to the supporting circuitry – such as row and column decoders – needed to access and control the memory array. Implementing peripheral circuitry was highly routine and has been standard in memory design for many decades prior to the ’806 patent. A POSITA would not have been dissuaded in any way by the issue of placing peripheral circuitry. That a POSITA would have been able to, and would have had a reasonable expectation of success in, implementing multiple planes of Toyama’s first exemplary structure is illustrated by the numerous prior art examples of the use of multiple planes in devices that expressly discuss peripheral circuitry.

60. **First**, as mentioned in my Initial Declaration, a figure from the Micheloni 2013 textbook (reproduced below) shares peripheral circuitry in a two-plane memory device:

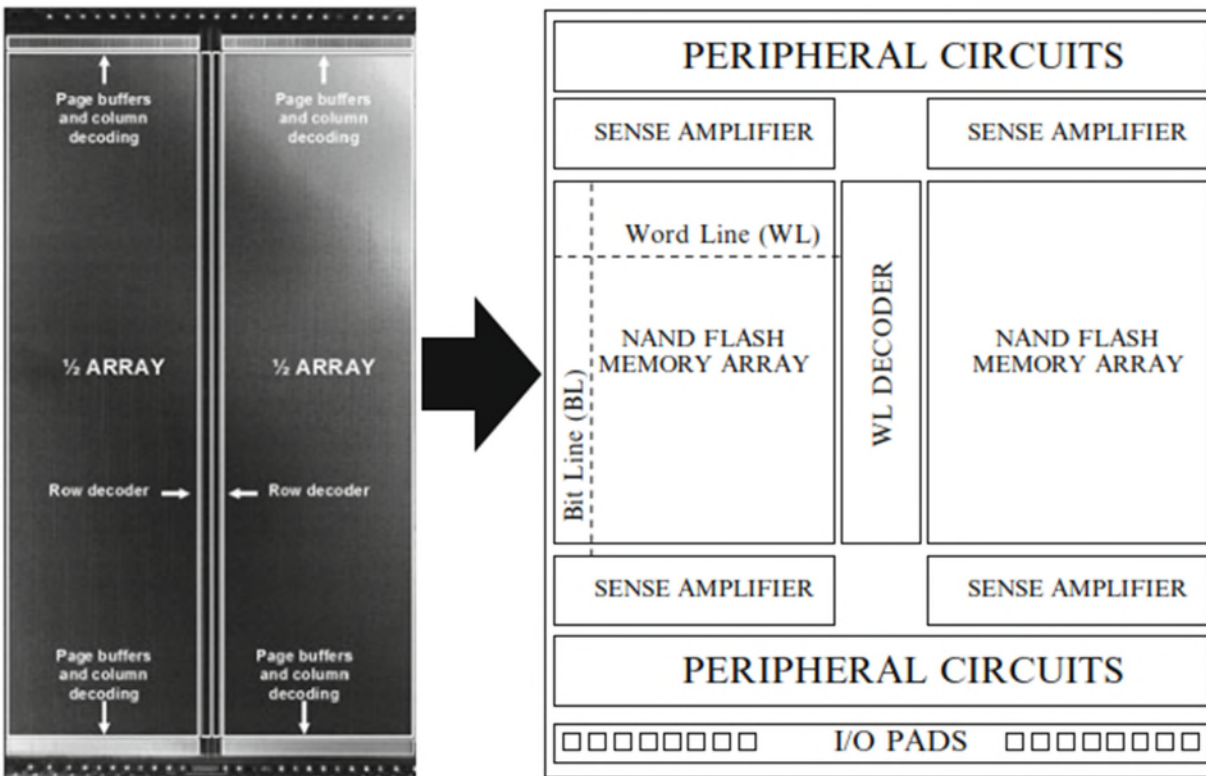


**Fig. 6.1** A typical NAND Flash floorplan [1]

Lee ¶ 172 (reproducing figure from Ex. 1023, at p. 144). As this figure shows, a POSITA would have recognized that peripheral circuitry may be placed above and below the NAND flash planes (when viewing the planes from above).

61. **Second**, a figure from the Aritome textbook discussing a two-plane 3D NAND device (which I mentioned in my Initial Declaration) shows its placement of peripheral circuitry:

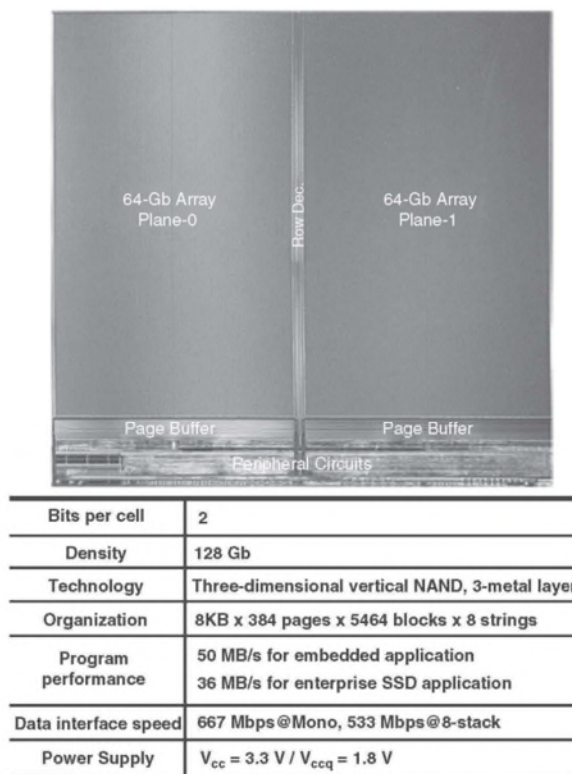


FIGURE 7.35 Die micrograph and main feature of 128-Gb 2-bit/cell 3D V-NAND flash. Die size is 133 mm<sup>2</sup>.

62.

Lee ¶ 175 (reproducing figure from Ex. 1014, at pp. 313-314). As this figure shows, a POSITA would have recognized that peripheral circuitry may all be placed below (from a top-view perspective) the memory planes.

63. **Third**, another figure from Aritome discussing a different two-plane 3D NAND device (which I also discussed in my Initial Declaration) shows its placement of peripheral circuitry:

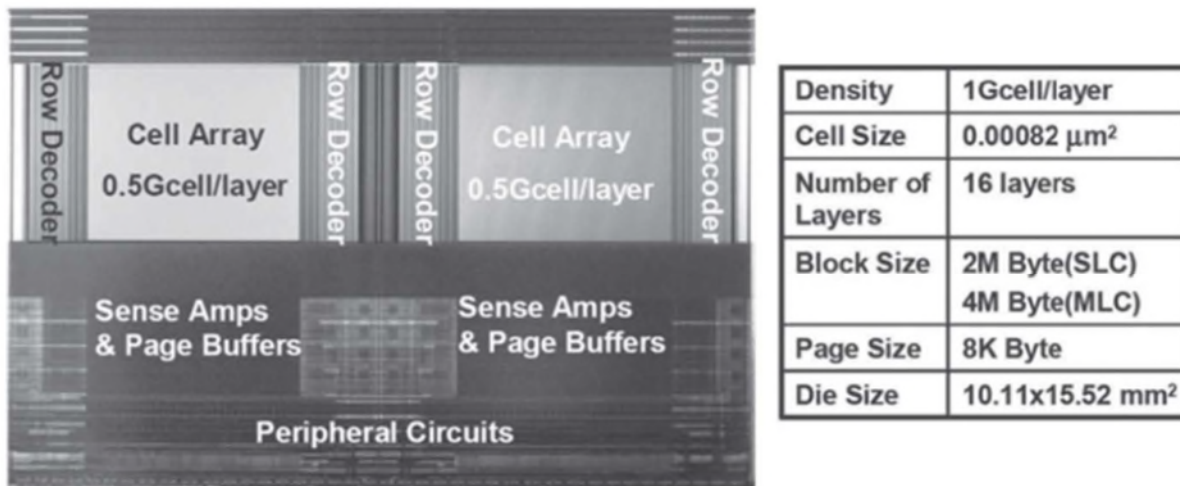
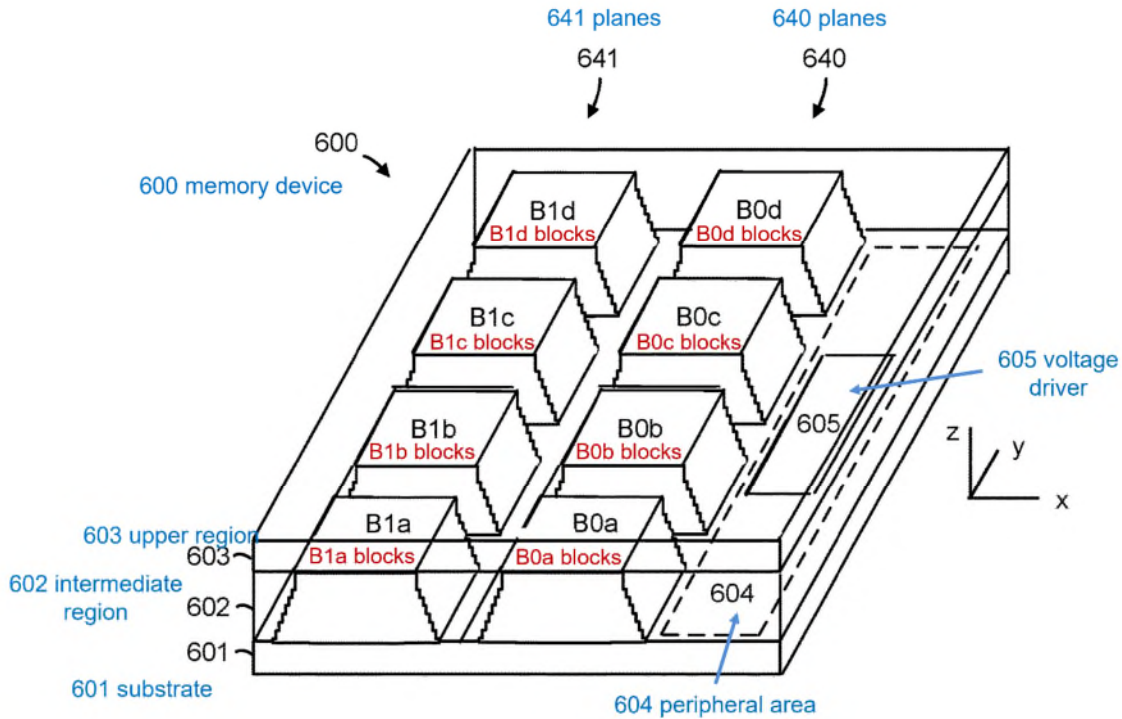


**FIGURE 7.26** Image of 16-Gb pipe-shaped BiCS test chip.

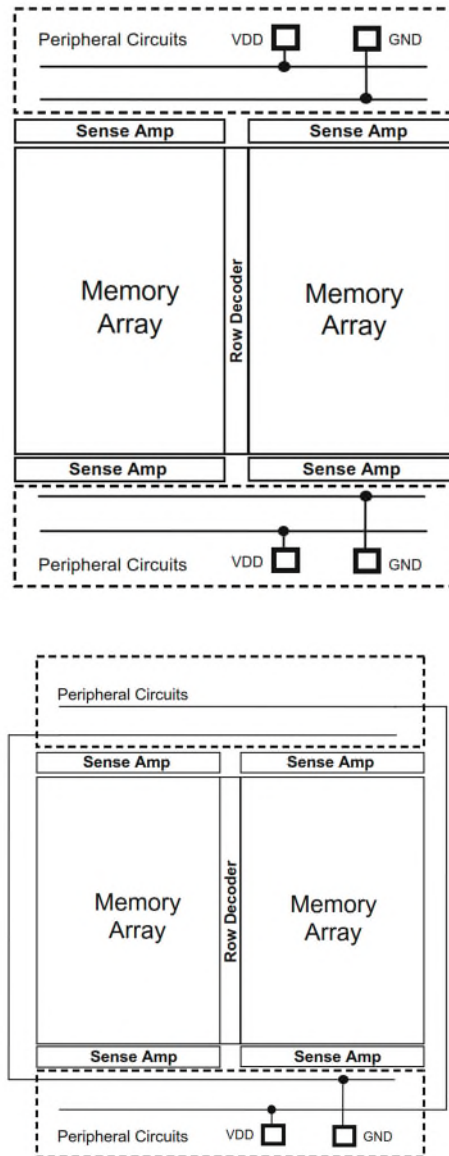
Lee ¶ 175 (reproducing figure from Ex. 1014, at p. 308). As with the previous Aritome figure, this figure demonstrates that a POSITA would have known how to place the peripheral circuitry below (from a top-view perspective) the memory planes.

64. **Fourth**, the Shah reference (which I also discussed in my Initial Declaration) shows two planes side-by-side and labels “a peripheral area 604 of the substrate includes circuitry for use by the blocks”:



Lee ¶ 174 (reproducing figure from Ex. 1024); Ex. 1024, 13:45-46. As the above figure shows, Shah places its “peripheral area 604” on one side of memory planes 640 and 641.

65. Fifth, although not expressly discussed in my Initial Declaration, Micheloni further discusses the placement of peripheral circuitry in a multiplane (indeed, die-stacked) device as shown below:



Ex. 1013, at pp. 286-287.

66. **Sixth**, even beyond the disclosures that specifically discuss peripheral circuitry, the fact that numerous (functional) flash memory devices by 2018 included multiple planes further supports that placing peripheral circuitry in a multi-plane device was within the skill of a POSITA. That is because, as a POSITA would have understood, any flash memory device needs peripheral

circuitry. As Micheloni 2016 put it, “a NAND Flash device is mainly a memory array but, in order to perform read, program, and erase, there is a need for additional [peripheral] circuits.” Ex. 1013, at p. 82. Indeed, Micheloni (2016) states that one of its “lesson[s]” is “how to connect wordlines, bitlines, NAND string selectors, and source line[s] to the peripheral circuits, such as decoders and sense amplifiers.” *Id.* at pp. 178-179. In addition to the strategies discussed above, Micheloni identifies -- citing to a conference paper -- an approach in which peripheral circuits are laid out “under the memory array.” *Id.* at p. 175. I note that in the context of 3D devices, designers have greater flexibility in the peripheral circuitry placement. As Micheloni recognizes, these circuits can be located beneath the memory array, although they are often still placed alongside it. the array. When located under the array, peripheral circuits are typically separated from the substrate by metal interconnect layers that provide routing channels. Likewise, routing layers above the array allow vertical and lateral connectivity, enabling access to the 3D memory stack wherever necessary.

67. The fact that numerous multi-plane devices existed demonstrates that techniques for placing peripheral circuitry in such devices were well known.

68. In summary, a POSITA would not have encountered any problems or difficulties in placing peripheral circuitry when modifying Toyama’s first exemplary structure to include multiple memory planes. By the priority date of

the '806 patent, it was well known in the semiconductor industry that peripheral circuitry, such as decoders, sense amplifiers, and control logic, could be placed in a variety of locations relative to the memory array, depending on design and integration requirements. As industry-standard texts like Micheloni (*Inside NAND Flash Memories*, 2010) (Ex. 1025) and Aritome (*NAND Flash Memory Technologies*, 2016) (Ex. 1014) explain, peripheral circuits could be placed beneath the memory array using CMOS-under-array (CUA) integration, alongside the array for ease of routing, or even in vertically stacked layers using 3D integration techniques such as wafer bonding or TSVs. Multiplane NAND architectures with shared or distributed peripheral circuitry were common in commercial devices well before 2020, and the placement of such circuits was a routine aspect of memory layout design.

69. Thus, a POSITA would have understood that implementing multiple planes within Toyama's structure did not preclude or complicate peripheral circuit integration, and would have had a reasonable expectation of success in designing around any physical constraints using well-established placement strategies. As the above examples further demonstrate, a POSITA would have understood that the peripheral circuitry of the modified device could be placed, from a top-down perspective, above and below the memory array, entirely beneath the memory array, or alongside the memory array.

70. YMTC argues that a POSITA would not have been able to make the proposed combination because Toyama's Figure 17F shows peripheral circuitry on both sides of each plane and, therefore, that a POSITA would not have been able to implement multiple planes. POR 45-52. I disagree.

71. A POSITA would have known that Toyama's disclosure is not limited to Figure 17F; indeed, Toyama describes Figure 17F as an "alternative exemplary structure." Toyama, [0049]. In contrast, Toyama describes Figures 17A-D as being view of the "first exemplary structure." Thus, a POSITA would have understood that, from how Toyama describes Figure 17F, it is not even part of—and, certainly, not a required part of—Toyama's "first exemplary structure." And even if it were part of Toyama's first exemplary structure, a POSITA would have recognized that alternative peripheral circuitry could be used. *E.g.*, Toyama, [0390].

72. Here, the record evidence—including the numerous prior art 3D NAND flash memory devices that have implemented multiple planes, the specific prior art disclosures of the locations of peripheral circuitry in multi-plane flash memory devices, and YMTC's failure to rebut any of this evidence—compels the conclusion that a POSITA would have been motivated to implement multiple planes of Toyama's first exemplary structure in a functional device with a reasonable expectation of success.

**VII. GROUND 3: TOYAMA’S FIRST EXEMPLARY STRUCTURE AND SECOND MODIFICATION RENDER THE CHALLENGED CLAIMS OBVIOUS**

**A. A POSITA Would Have Been Motivated To Combine Toyama’s First Exemplary Structure and Its Second Modification**

**1. A POSITA Would Have Known How to Use Slit Structures (Toyama’s “Laterally Elongated Contact Via Structures 76”) to Perform Gate Replacement In the Proposed Combination**

73. YMTC asserts that the proposed modification would have resulted in an inoperable device because, to YMTC, the use of a unitary dielectric to house the TACs would remove access for depositing conductive material during the gate replacement process. POR 58-59. But Toyama discloses gate replacement in exactly the same way as the ’806 patent: using the *slit structures* (“laterally elongated contact via structures 76”) for access. A POSITA would have known how to perform the gate replacement process in the proposed combination using slit structures alone.

74. As background, a POSITA would have known by the patent’s priority date the conventional process of “gate replacement.” Each memory cell in the NAND memory device includes a “control gate,” which is a means for controlling the operation of the cell. Lee ¶¶ 44, 50-52. In 3D NAND memory, the device includes conductive layers (sometimes known as “gate layers”) that serve as the

control gates for a number of memory cells. *Id.* (These layers are also sometimes called “word lines.”) Toyama, [0232]. In part for ease of manufacturing, the stack through which the 3D NAND strings are ultimately placed is first manufactured as an alternating series of layers, at least one of which is designed to be “sacrificial”—that is, it will later be removed. *Id.*, Figure 2, [0173] (describing “insulating layers 132” and “sacrificial material layers 142”). Then, as part of the gate replacement process, those sacrificial layers are removed and replaced with conductive layers serving as the control gates for the memory cells. Lee ¶¶ 50-52; Toyama, Figures 13-15, 44-46 (showing the gate replacement process).

75. This approach was not only disclosed in Toyama—it was also standard practice in the art. As described in Micheloni (Ex. 1013, at pp. 131-132) and Aritome (Ex. 1014, at pp. 308-313), slit-based gate replacement was a conventional fabrication step for 3D NAND devices at the time. These references explain how the gate replacement process involved etching sacrificial layers using slit structures and then depositing control gate materials via those same openings, without requiring additional access structures. The ’806 patent itself confirms this practice: it performs gate replacement using slit structures alone and is silent on any additional openings or unconventional mechanisms. See ’806 patent, 16:27-34.

76. A POSITA would have understood that a conventional approach to gate replacement was to use openings that ultimately become slit structures (e.g., Toyama’s “laterally elongated contact via structures 76”). For example, Toyama discloses in the context of its first exemplary structure that vertical “backside contact trenches 79” are formed in the alternating stack. Toyama, Figures 12-13, [0217], [0221]. Using “trenches 79,” an etchant is introduced to selectively remove the sacrificial layers. *Id.*, Figures 13-14, [0222]-[0224]. The etching process results in “backside recesses (143, 243),” that is, openings. *Id.*, [0222]-[0224]. Toyama fills in these “recesses (143, 243)” with conductive material in the form of “electrically conductive layers (146, 246),” which serve as the device’s gate layers. *Id.*, [0231]-[0232]. Toyama’s use of slit structures in this manner was conventional; textbooks described this typical approach to gate replacement. *See, e.g.*, Ex. 1013, at pp. 131-132; Ex. 1014, at pp. 308-313. Importantly, this prior art approach did not require the use of any other openings to perform gate replacement—just the openings that ultimately become the slit structures.

77. In view of the widespread use of slit structures as the sole access points for gate replacement, I disagree with YMTC’s assertion that a POSITA would have been “discouraged” from making the proposed combination. YMTC asserts that, unlike Toyama’s Second Modification, the proposed combination cannot use “through-memory-level openings 679” as access points for gate

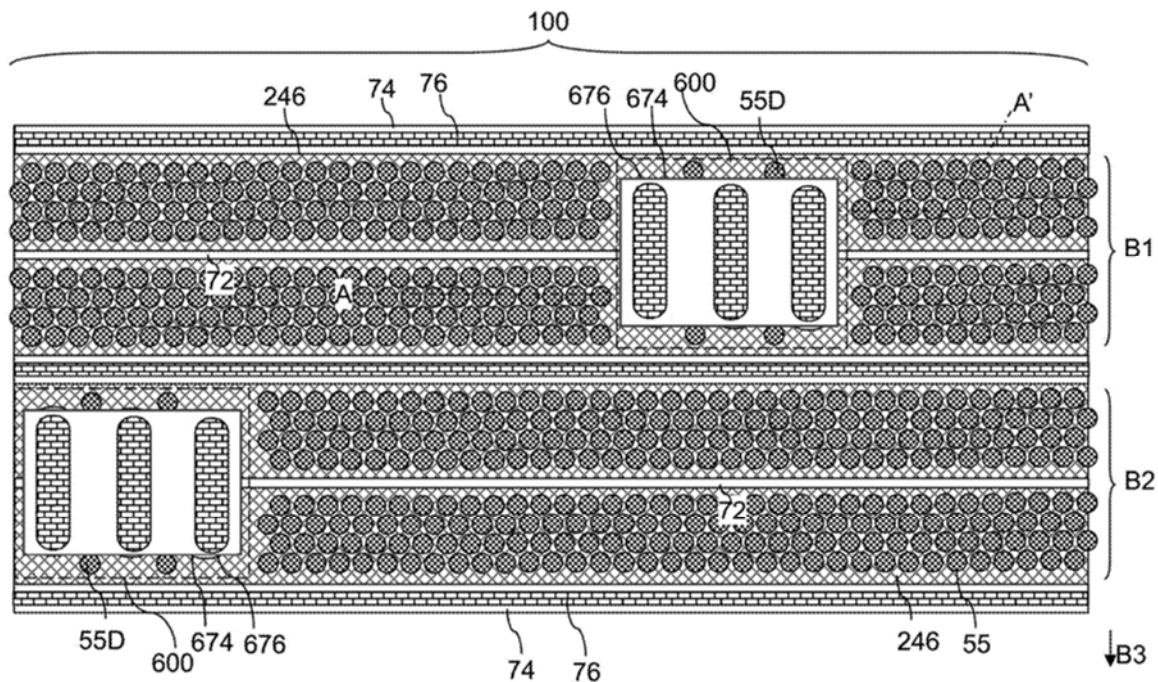
replacement. POR 60-61. But YMTC cannot dispute that the Second Modification **also** uses “backside contact trenches 79” as access points for gate replacement, and the proposed modification continues to allow these trenches to be used. Indeed, both embodiments being combined expressly describe the use of “trenches 79” for gate replacement. Toyama, [0217] (first exemplary structure), [0337] (Second Modification). Indeed, Toyama’s fourth exemplary structure (on which the Second Modification is based) exclusively uses slit structures for gate replacement. *Id.*, Figures 36A-37A. And Toyama’s disclosure confirms that a POSITA would have been able to mix and match the relevant elements of Toyama’s exemplary structures—here the gate replacement processes. Lee ¶¶ 232-239 (citing Toyama, [0332], [0390]. To the extent that not using “openings 679” reduces access for gate replacement, a POSITA would have known how to adjust the sizing and spacing of “trenches 79” so as to achieve a successful gate replacement in light of the numerous prior art devices, discussed above, that exclusively use slit structures for gate replacement. A POSITA would have had a reasonable expectation of success in manufacturing the proposed modification with slit structures alone being used for gate replacement.

78. Indeed, POSITA would have found that Toyama encourages the combination because both combined structures use the exact same conventional element for gate replacement.

79. The '806 patent's disclosure further supports that a POSITA would have been able to make the proposed combination. Just like the proposed modification, the '806 patent uses slit structures alone to perform gate replacement. '806 patent, 16:27-34. And far from disclosing any unconventional means for doing so, the '806 patent simply notes in a single sentence that this conventional process is performed. Because the '806 patent is entirely silent on how to perform gate replacement using only slit structures, it suggests that a person of ordinary skill in the art was more than capable of doing so.

**2. A POSITA Would Have Known How To Design The Proposed Combination's Dielectric Structure So As To Allow The Device To Operate**

80. As explained in my Initial Declaration, a POSITA would have found it obvious "to modify Toyama's Second Modification to electrically isolate 'through-memory-level via structures 676' with a unitary dielectric fill material, as taught by Toyama's first exemplary structure." Lee ¶¶ 224, 232. For illustrative purposes, the Petition showed a modified version of Figure 48B illustrating the proposed modification:



Lee ¶ 224 (including a modified version of Toyama, Figure 48B).

81. YMTC asserts that a POSITA would have been discouraged from making the proposed combination because, according to YMTC, the proposed combination's *dielectric structure* (akin to “dielectric fill material portion 430”) reduces the area for current flow between channel regions in a way that would render the device inoperable. POR 63-64. But Toyama’s conductive layers are made out of metal (as it uses a gate replacement process, and thus would typically replace the sacrificial gates with tungsten gates), and a POSITA would have understood that metal (which is highly conductive) has very little resistance.

82. Moreover, the amount of conductive-layer resistance in the proposed modification (low as it is), is not materially higher than in the Second Modification because, as a POSITA knew, resistivity is in large part dependent on the “bottleneck”—that is, the part of the current path with the smallest cross-sectional area.

83. Indeed, resistance ( $R$ ) is often expressed using the formula  $R = \rho L/A$ , where  $\rho$  is resistivity,  $L$  is length, and  $A$  is cross-sectional area. Moreover, it is well known that the resistance of a length of conductor can be modeled as the sum of the resistances of that conductor’s components in series. In other words,  $R_{\text{total}} = R_1 + R_2$ .

84. So, for example, let’s say that an unrestricted section of a conductor is  $1\ \Omega$  per unit length and a restricted section of a conductor is  $1000\ \Omega$ . Now let’s compare three conductors with a unit length of 5: (conductor A) that is unrestricted the whole length, (conductor B) that is restricted for just one of the five units, and (conductor C) that is restricted for its entire length. The resistances of each of these conductors would be (A)  $5\ \Omega$ , (B)  $1005\ \Omega$ , and (C)  $5000\ \Omega$ . In terms of relative resistance (which is in this context the more material measure), the resistance of conductors B and C are much closer to each other (within a factor of 5) than to conductor A, which differs by a factor of 200 (from B) and 1000 (from

C). Although the real-world resistances of conductor layers will vary from this example, it illustrates how the bottleneck dictates overall resistance.

85. A POSITA would have been able to design the proposed combination—e.g., adjusting the size of the dielectric fill, TACs, and surrounding circuitry — so as to preserve current flow and device functionality.

86. As I understand, YMTC draws conclusions based on the relative sizes of the '806 patent's Figure 1A-C, and Toyama's figures. That's contrary to the understanding of a POSITA. Both documents expressly state that their drawing are not to scale. Toyama says "[t]he drawings are not drawn to scale." Toyama, [0156]. And the '806 patent says, "unless otherwise indicated"—and it is never otherwise indicated) — "the disclosure should not be interpreted as to-scale drawings." '806 patent, 3:57-59.

87. In fact, there is no material difference in components between the '806 patent and the proposed modification—only the relative sizes at which those components are drawn. And a POSITA would have understood that the components are design choice, made based on various design criteria, and would not treat figure proportions in the '806 patent or in Toyama as fixed and limiting.

88. The '806 patent itself confirms that a POSITA would have been able to size and scale the dielectric structure and the conductive layers so as to design a functional device. Not only are the '806 patent's figures expressly not to scale, but

the '806 patent does not provide any guidance as to the relative sizes of its *dielectric structures* and its *conductive layers*. The '806 patent's silence on how to size the dielectric structure and the conductor layer so as to preserve current flow through the conductor layer from one side of the dielectric structure to the other, confirms that a person of ordinary skill in the art was more than capable of doing so.

89. Moreover, Toyama itself contradicts YMTC's assertion that a POSITA would be discouraged from placing unitary dielectric structures in a memory region. POR 63-64. As shown below, Toyama discloses embodiments that do just that:

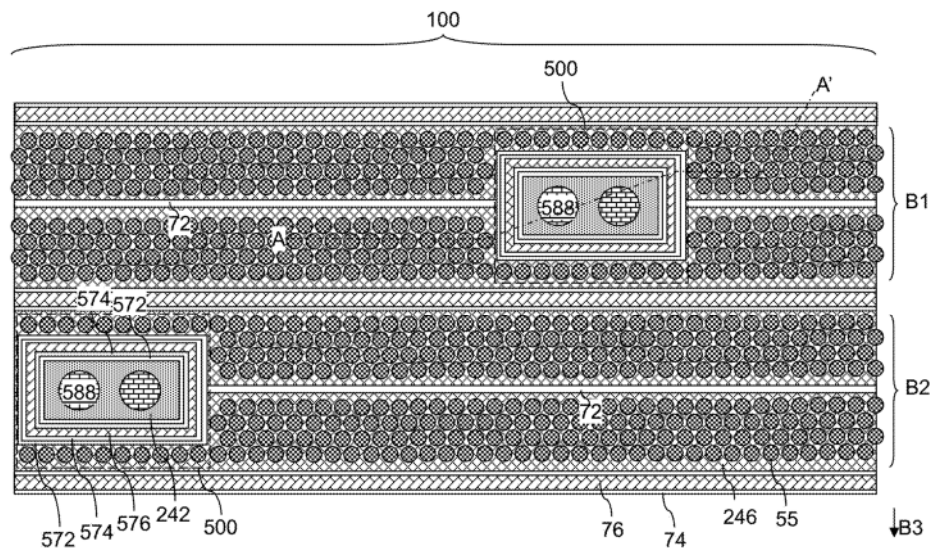


FIG. 39B

Toyama, Figures 39B, 69B. These devices, which also require current to flow around a dielectric block of material, would be equally vulnerable to the purported

problems that YMTC raises—increased resistance, “hot spots,” etc. That Toyama itself shows devices overcoming these purported problems illustrates that a POSITA would not have been dissuaded from the proposed combination. On the contrary, a POSITA would have recognized that dielectric blocks could desirably be formed within the memory region 100.

90. Even assuming that there was any material restriction of current flow in the proposed modification (there would not have been for the reasons above), a POSITA would have known of alternative techniques for propagating the conductive layers’ signals to the channel structures that are intended to receive them. For example, a POSITA would have known to use vias (vertical interconnects) to convey an electrical signal to each side of the dielectric structure. YMTC presumes that the control gate’s electrical signal travel in one direction (e.g., from left to right), such that the signal would need to flow around the dielectric structure to propagate to the channel structures on the other side. However, as shown below, a POSITA would have known that each channel region can be provided a separate electrical signal through separate word line vias. This is illustrated, for example, in the Micheloni 2016 textbook:

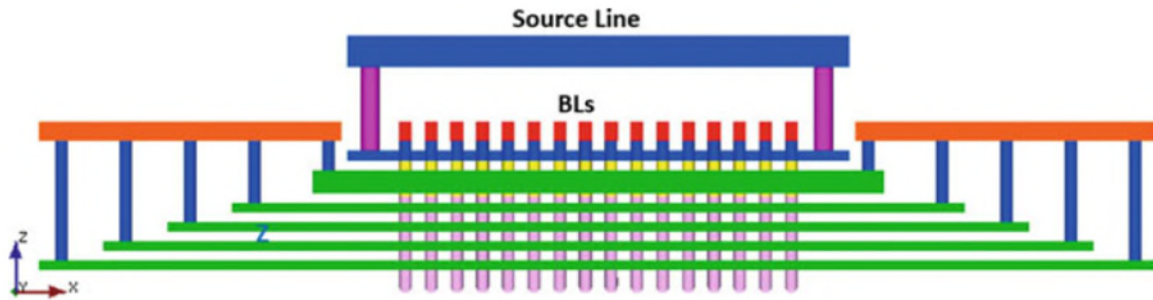


**Fig. 4.33** X-Z cross section of Fig. 4.32

Ex. 1013, at p. 120. As the above figure shows, each conductive gate layer (the horizontal green lines) is supplied an electrical signal using vias (the vertical blue lines) on each end of the device. Thus, even if a dielectric structure with TACs is placed between the channel structures (the pink and yellow structures below the bit lines (BLs)), such that the gate layer is interrupted, a POSITA would have known to supply each side of the dielectric structure using a separate via.

91. An annotated, modified version of Figure 48B, below, illustrates this conventional approach:

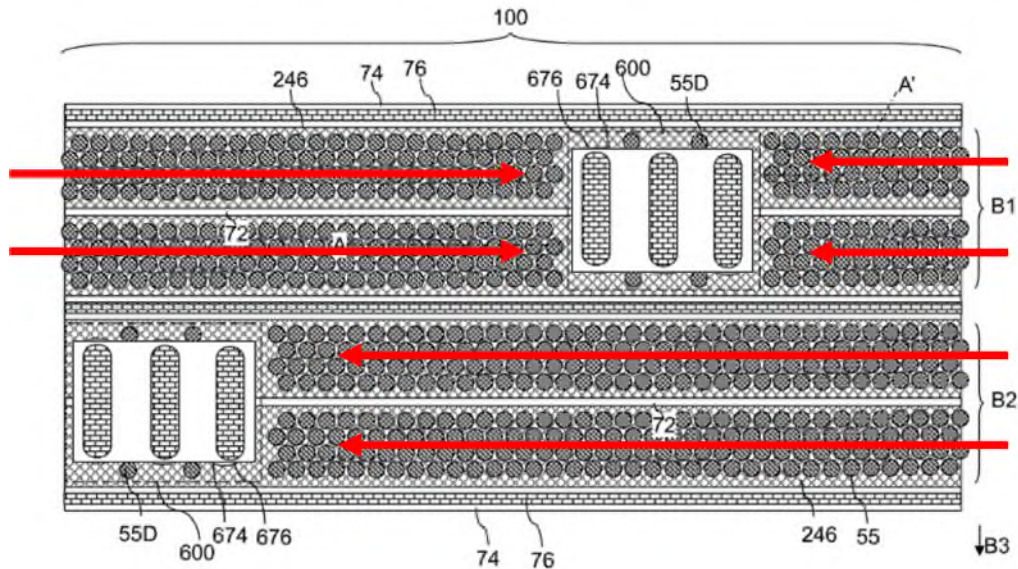


FIG. 48B

Toyama, Figure 48B (modified and annotated). As the annotated figure shows, the conventional approach of word line vias on both sides of the memory array, as applied to the proposed combination, would obviate any need for there to be current flow past the dielectric structure. A POSITA would have known how to apply this technique to Toyama at least because Toyama itself discloses the use of word line vias (“contact via structure[s] 86”). *Id.*, [0329]. Thus, even if YMTC’s purported current restriction problem posed any issue to a POSITA, a POSITA would have known alternative ways of solving the problem.

**3. YMTC’s Arguments against Motivation To Combine Are Incorrect**

**a. YMTC’s Capacitive-Coupling And TAC-Placement Objections Are Beside The Point**

92. My Initial Declaration explained that forming the “through-memory-level via structures” inside a unitary dielectric fill material, as in the obviousness combination, would be desirable—and, indeed, serve a necessary function—because the dielectric fill material electrically isolates the “through-memory-level via structures.” Lee ¶ 227. Putting aside YMTC’s meritless arguments regarding the gate replacement process (addressed in §VII.A.1) and the resistance of the conductive layers (addressed in §VII.A.2), YMTC does not dispute that a unitary dielectric fill material would serve the desirable function of electrically isolating the proposed combination’s “through-memory-level via structures.” Lee ¶ 227. At bottom, using a unitary dielectric fill (as in Toyama’s first exemplary structure) in place of dielectric liners (as in Toyama’s Second Modification) would be nothing more than a simple substitution of known elements with predictable results (e.g., the unitary block would insulate the TACs just as the liners did).

93. YMTC’s assertion that capacitive coupling was already “minimiz[ed]” in Toyama’s Second Modification is incorrect and beside the point. POR 67. Toyama states that:

The various through-memory-level via structures (588, 676) of the fourth exemplary structure or modifications thereof can be employed to provide vertical electrically conductive path inside the selected areas of a memory array region 100. The through-memory-level via structures (588, 676) may be employed as a portion of a power distribution network, or can be employed to provide various control signals for a three-dimensional memory device in a manner that shortens the signal path, and thus, minimizes signal loss and capacitive coupling.

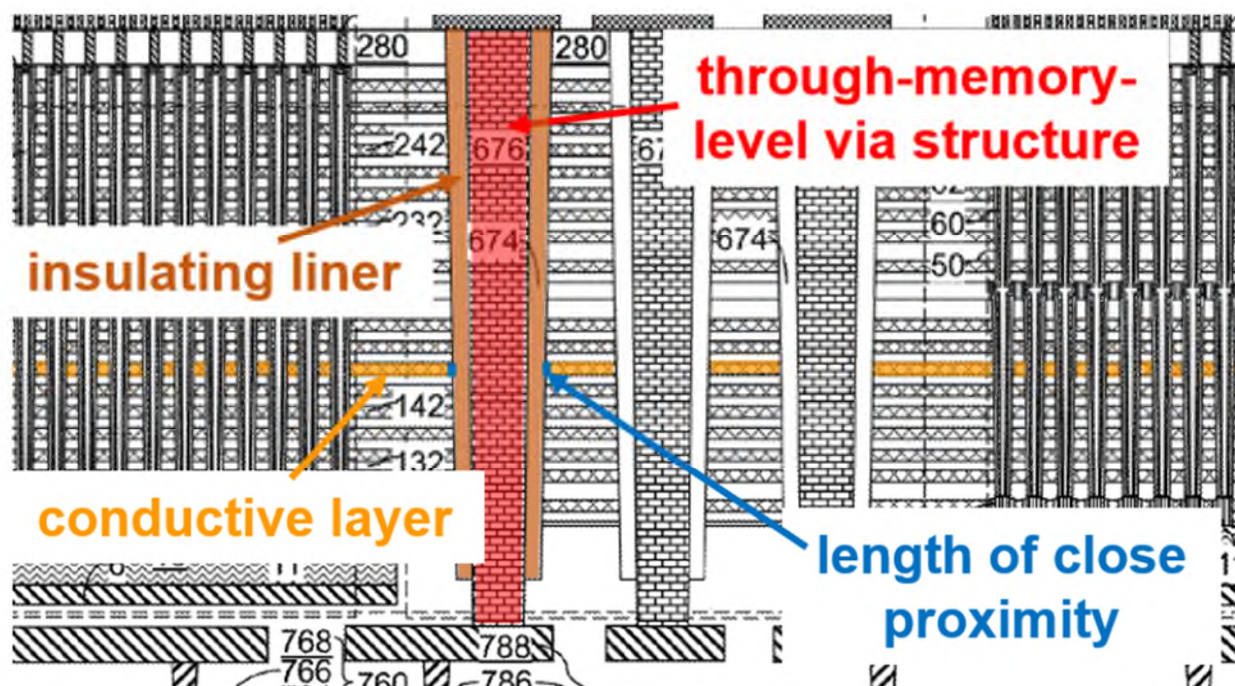
Toyama, [0377].

94. A POSITA would understand from Toyama's disclosure that capacitive coupling is a real concern for devices flash memory devices like Toyama's (and the '806 patent's). Indeed, Toyama would not have mentioned "capacitive coupling" if it was not a significant concern in device design and operation.

95. PO seems to contend that because Toyama describes the fourth exemplary structure (and modification) to "minimize[]" capacitive coupling, that these embodiments have no problem with capacitive coupling whatsoever. But Toyama's use of the word "minimize" does not mean that there is *no* capacitive coupling, just as a construction project that minimizes cost will still cost something. As with the construction project's cost, capacitive coupling in 3D NAND memory device is a factor that must be managed and reduced to the

greatest extent practicable. Indeed, as a POSITA understood, “[c]apacitance is the primary cause of delays in packaging and interconnect systems.” Ex. 1026, at pp. 63-64. What’s more, capacitive coupling may interfere with program, read, and erase operations in a 3D memory device. Thus, a POSITA reading Toyama would understand that the fourth exemplary structure reduces capacitive coupling but would also understand that further reductions would be beneficial. Lee ¶¶ 228-230 (discussing the problems caused by capacitive coupling).

96. Moreover, YMTC’s argument dramatically understates the degree of capacitive coupling because it overlooks a key aspect of the modified device’s structure. YMTC highlights a single conductive layer and asserts that capacitive coupling between that conductive layer and the through-memory-level via structure is minimal because the “length of close proximity” is small:



POR 68. But YMTC ignores that there are over a dozen conductive layers 146, 246 shown in Figure 49, which YMTC annotates (there may be many dozens in a real device), and each of them can capacitively couple to the through-memory-level via structure. Thus, the degree of capacitive coupling is far greater than what YMTC suggests, and a POSITA would have seen a benefit in reducing it.

**b. A POSITA Would Have Recognized a Benefit to Placing TACs In The Memory Region**

97. As explained in my Initial Declaration, a POSITA would have recognized a benefit to the proposed combination because, as compared to one of the combined embodiments (namely, Toyama's first exemplary structure), the proposed design locates its through array contacts ("through-memory-level via structures") within the memory array, thereby reducing signal propagation delays and electrical losses. Lee ¶ 231. YMTC apparently contends that these benefits are irrelevant because Toyama's Second Modification already places its TACs in the memory array. POR 68-69. But the point is that a POSITA starting with Toyama's first exemplary structure would have viewed the Second Modification's TAC placement as an improvement and would have been motivated to incorporate that feature, along with its accompanying benefits, into the first exemplary structure, consistent with my analysis in my Initial Declaration. Lee ¶ 231.

98. In summary, the proposed combination is nothing more than the mere substitution of one element for another known in the field to yield a predictable and beneficial result, well within the skill of a POSITA. Lee ¶¶ 232-239.

**B. Limitation [8.H]”**

99. YMTC’s argument that Ground 3 fails to render limitation [8.H] obvious fails for all the reasons explained above for Ground 1. §V.B .

**VIII. LIMITATION [10.B]: “AN ETCH STOP PLUG INTERPOSED BETWEEN EACH LOCAL CONTACT OF THE LOCAL CONTACTS AND EACH CHANNEL STRUCTURE OF THE CHANNEL STRUCTURES” (ALL GROUNDS)**

**A. Under Micron’s Construction, Limitation [10.B] Would Have Been Obvious**

100. YMTC argues that limitation [10.B] requires an *etch stop plug* interposed between each slit structure local contacts (that is, the *local contacts disposed on ... the slit structures*) and the *channel structures*. For the reasons explained above (§ IV.A), I disagree. If claim 10 is understood to only require etch stop plugs between the channel structure local contacts (that is, the *local contacts disposed on the channel structures*) and the channel structures, then Toyama renders claim 10 obvious for the reasons explained in my initial declaration. Lee ¶¶ 144-152, 208-216, 253.

**B. Toyama Discloses Claim 10 Even Under YMTC's Construction**

101. Toyama's First Exemplary Structure and Second Modification render the claim 18 obvious even accepting PO's construction. That is because Toyama discloses the claim in exactly the same way that, under PO's erroneous theory, the '806 discloses it. In other words, the faulty logic underlying YMTC's proposed construction would similarly require concluding that Toyama discloses the limitation.

102. PO asserts (POR 18-19) that the '806 patent's "bit lines 250" are *local contacts disposed on the channel structures and the slit structures* (limitation [15.G]), such that the '806 discloses *an etch stop plug* ("etch stop plug 224") *interposed between each local contact of the local contacts* ("bit lines 250") *and each channel structure of the channel structures* ("channel structure 216"). POR 18-19. PO annotates Figure 1A with its apparent theory:

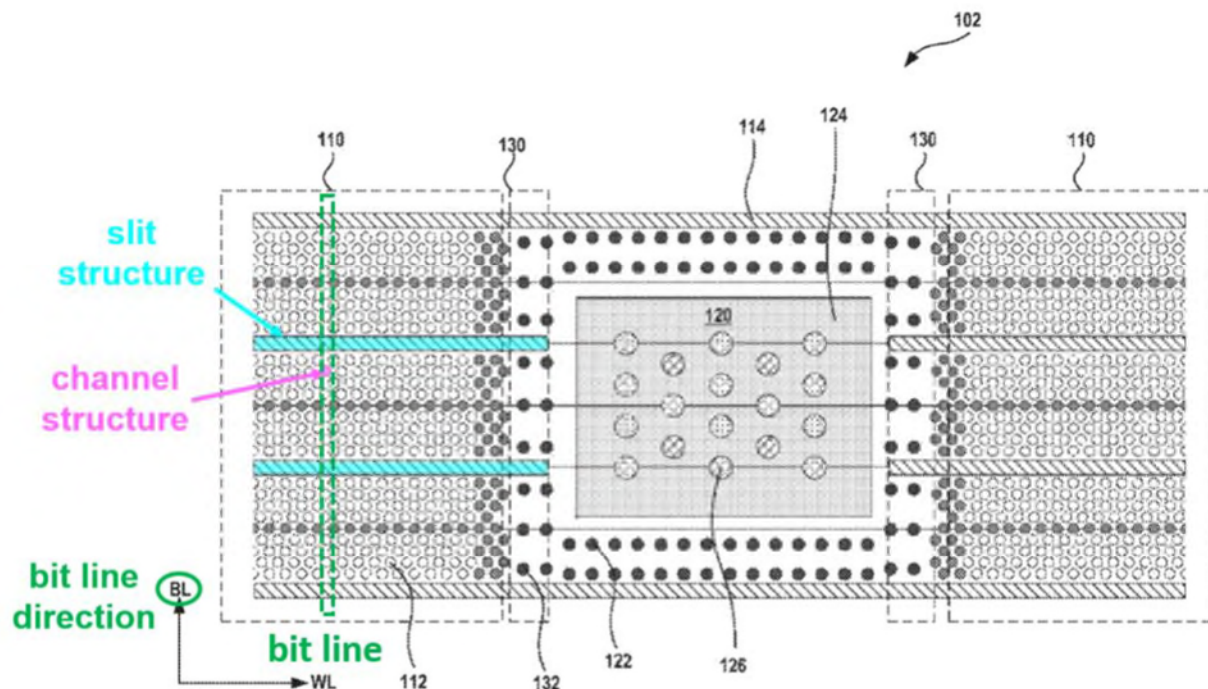
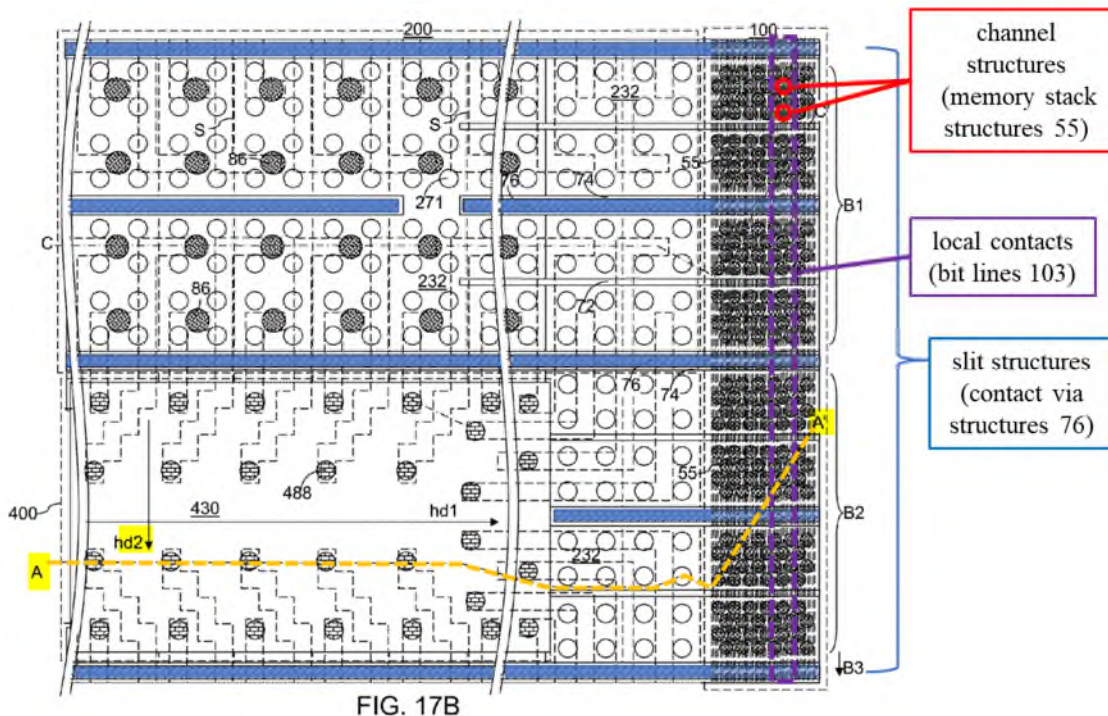


FIG. 1A

POR 19 (annotating '806 patent, Figure 1A).

103. By the same logic, Toyama discloses limitations [8.F] and [10.B]. Specifically, each of Toyama's embodiments discloses *local contacts* ("bit lines 103") *disposed on the channel structures* ("memory stack structures 55") *and the slit structures* ("laterally elongated contact via structures 76"), such that Toyama discloses *an etch stop plug* ("drain region 63") *interposed between each local contact of the local contacts* ("bit lines 103") *and each channel structure of the channel structures* ("memory stack structures 55"). Pet. 102-103. Figure 17B illustrates this disclosure in Toyama's First Exemplary Structure:



Toyama, Figure 17B (annotated). Although “bit lines 103” are not expressly labeled in Figure 17B, a POSITA would have understood that Toyama’s First Exemplary Structure includes bit lines as indicated in the annotated figure. For example, Toyama states (at [0250]) that “bit lines 103 extend along at the second horizontal direction hd2.” Figure 17B depicts the second horizontal direction (hd2), as is highlighted in the annotated figure. Confirming this, Toyama states (at [0251]) that “bit lines 103 are illustrated in dotted lines” in Figure 17B. Further confirming this, Figure 17D expressly labels “bit lines 103” where they are indicated in the annotated version of Figure 17B.

104. As the annotated version of Figure 17B shows, “bit lines 103” (in purple) are above “memory stack structures 55” (in red), and Toyama explains

(and a POSITA would have understood) that in between “memory stack structures 55” and “bit lines 103” are “drain regions 63.” Toyama, [0251], Figure 17A.

105. Figure 48B similarly depicts this disclosure in Toyama’s Second Modification:

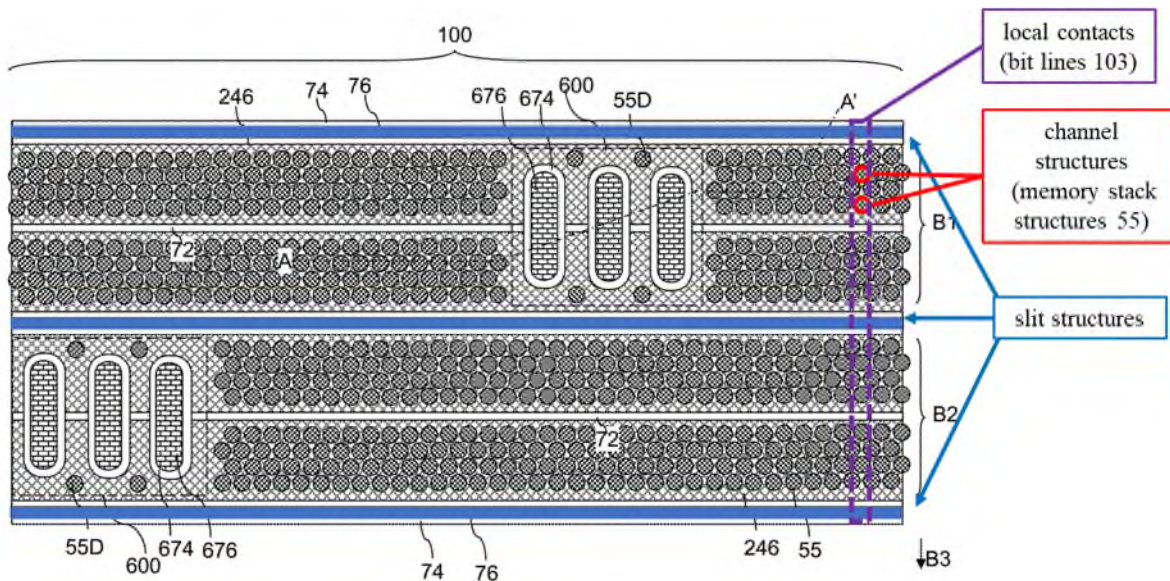


FIG. 48B

Toyama, Figure 48B (annotated).

106. Although Figure 48B does not expressly label “bit lines 103,” a POSITA would have understood that Toyama’s Second Modification includes bit lines 103 as indicated in the annotated figure. For example, Toyama (at [0342]) explains that “bit lines 103 ... extend along the second horizontal direction hd2.” A POSITA would have understood that the second horizontal direction is the direction indicated by the purple annotation at least in part because the “laterally-elongated contact via structures 76” (that is, the “slit structures” labeled above in

blue) are described as “extending along the first horizontal direction hd1,” and “the second horizontal direction hd2” is described as “perpendicular to the first horizontal direction hd1.” Toyama, [0329], [0331].

107. A POSITA would have further understood that the etch stop plugs (“drain regions 63”) are interposed between “bit lines 103” and “memory stack structures 55.” Toyama, [0251], Figure 49.

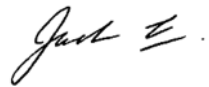
## **IX. CONCLUSION**

108. The Board should hold all Challenged Claims unpatentable.

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willfully false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1101 of Title 18 of the United States Code.

Date: 6/25/2025

Location: Austin TX

Signature: 

DR. JACK C. LEE