

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00911

Patent 10,937,806

PATENT OWNER'S SUR-REPLY

TABLE OF CONTENTS

LIST OF EXHIBITS	v
LIST OF ABBREVIATIONS	vi
I. INTRODUCTION	1
II. CLAIM CONSTRUCTION	2
A. “a dielectric structure” and “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” (Claim 8).....	2
B. “each local contact of the local contacts” (Claim 10).....	5
III. TOYAMA FAILS TO DISCLOSE OR RENDER OBVIOUS CLAIM 8, FROM WHICH THE CHALLENGED CLAIM DEPENDS	8
A. Ground 1: Toyama’s Second Modification.....	8
1. Toyama’s Second Modification Does Not Disclose or Render Obvious “a Plurality of Through Array Contacts (TACs) Extending Vertically Through the Dielectric Structure”	8
2. Toyama’s Second Modification Does Not Disclose or Render Obvious “a Plurality of Non-Electrically Functional Channel Structures Surrounding the TAC Region”	11
B. Ground 2: Toyama’s First Exemplary Structure.....	17
1. Petitioner’s Modification Results in Multiple Devices, None of Which Meet the Claimed Configuration.....	17
2. Petitioner’s Modification Results in an Inoperable Device	20
C. Ground 3: Toyama’s Second Modification in Combination with Toyama’s First Exemplary Structure	24
1. A POSITA Would Not Have Found It Obvious to Modify Toyama’s Second Modification in the Proposed Manner	24
(a) Petitioner’s Obviousness Combination Would Fail with Respect to Gate Replacement	24
(b) Petitioner’s Obviousness Combination Would Block Current and Render the Device Inoperable.....	26

(c)	Petitioner’s Proposed Motivations for the Obviousness Combination are Flawed	29
2.	Petitioner’s Obviousness Combination Does Not Disclose or Render Obvious “a Plurality of Non- Electrically Functional Channel Structures Surrounding the TAC Region”	31
IV.	TOYAMA FAILS TO DISCLOSE OR RENDER OBVIOUS THE ADDITIONAL LIMITATION OF CHALLENGED CLAIM 10 (ALL GROUNDS).....	31
V.	CONCLUSION.....	36

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>ABS Glob., Inc. v. Cytonome/St, LLC</i> , 84 F.4th 1034 (Fed. Cir. 2023)	5
<i>Baldwin Graphic Sys., Inc. v. Siebert, Inc.</i> , 512 F.3d 1338 (Fed. Cir. 2008)	5
<i>Carrum Techs., LLC v. Ford Motor Co.</i> , No. CV 18-1647-RGA, 2023 WL 7407778 (D. Del. Nov. 9, 2023)	5
<i>Commscope, Inc. v. Tq Delta, LLC</i> , 2023 WL 7491181 (P.T.A.B. Nov. 13, 2023)	29
<i>Finjan LLC v. SonicWall, Inc.</i> , 84 F.4th 963 (Fed. Cir. 2023)	<i>passim</i>
<i>Henny Penny Corp. v. Frymaster LLC</i> , 938 F.3d 1324 (Fed. Cir. 2019)	1
<i>KCJ Corp. v. Kinetic Concepts, Inc.</i> , 223 F.3d 1351 (Fed. Cir. 2000)	4, 5
<i>Merck & Co. v. Teva Pharms. USA, Inc.</i> , 395 F.3d 1364 (Fed. Cir. 2005)	6
<i>ResONet.com, Inc. v. Lansa, Inc.</i> , 346 F.3d 1374 (Fed. Cir. 2003)	6
<i>Salazar v. AT&T Mobility LLC</i> , 64 F.4th 1311 (Fed. Cir. 2023)	4, 19
Other Authorities	
37 C.F.R. § 42.23(b)	1

LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	Joint Claim Construction Statement
Ex. 2002	File History of U.S. Patent No. 10,658,378 B2 to Tao et al.
Ex. 2003	Micron’s Preliminary Claim Constructions
Ex. 2004	YMTC’s Proposed Claim Constructions
Ex. 2005	Declaration of Dr. Yang (“Yang”)
Ex. 2006	Deposition Transcript of Dr. Lee
Ex. 2007	U.S. Patent No. 10,559,583 B2 to Park et al. (“Park”)
Ex. 2008	Deposition Transcript of Dr. Lee Regarding U.S. Patent No. 10,658,378 (IPR2024-00788, -00909)
Ex. 2009	Declaration of Andrew Radsch
Ex. 2010 ¹	Transcript of June 13, 2025 Deposition of Dr. Jack Lee Regarding IPR2024-00791

¹ The deposition transcript from IPR2024-00791, which relates to the same patent as this proceeding (U.S. Patent No. 10,937,806) is being filed with permission from Petitioner.

LIST OF ABBREVIATIONS

Abbreviation	Term
'806 or '806 patent	U.S. Pat. No. 10,937,806
'806FH	File History of U.S. Pat. No. 10,937,806
Board or PTAB	Patent Trial and Appeal Board
Challenged Claim	'806 patent, claim 10
DI	Decision Granting Institution for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00911, Paper 12)
Lee(I)	May 19, 2024, Declaration of Dr. Jack C. Lee (Ex. 1003)
Lee(II)	June 25, 2025, Reply Declaration of Dr. Jack C. Lee (Ex. 1043)
Office or USPTO	U.S. Patent and Trademark Office
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner or PO	Yangtze Memory Technologies Company, Ltd.
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00911, Paper 1)
Petitioner	Micron Technology, Inc.
POR	Patent Owner Response for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00911, Paper 15)
POSITA	Person of ordinary skill in the art
Reply	Petitioner's Reply for <i>Inter Partes</i> Review of U.S. Patent No. 10,937,806 (IPR2024-00911, Paper 17)
Toyama	U.S. Patent Publication No. 2017/0179026

I. INTRODUCTION

Petitioner's Reply fails to address the issues raised in the POR, misunderstands the prior art, and misrepresents PO's positions. In addition, the Reply introduces new arguments, which the Board should disregard, as Petitioner needed to make its entire case in the Petition. 37 C.F.R. § 42.23(b); *Henny Penny Corp. v. Frymaster LLC*, 938 F.3d 1324, 1330-31 (Fed. Cir. 2019) (rejecting attempts to broaden the petition's ground in its reply). Because Petitioner has not been able to remedy the deficiencies in its Petition, the Board should uphold the validity of claim 10 (the sole Challenged Claim).

Ground 1 (Toyama's Second Modification) fails to teach "a plurality of through array contacts (TACs) extending vertically through the dielectric structure" as required by Claim 8 (from which Challenged Claim 10 depends) because the purported TACs each extend through separate insulating liners and not through the same dielectric structure. Petitioner's counterarguments contravene well-established Federal Circuit precedent that one instance of an element must meet all requirements of the claim for that element. Additionally, Toyama's Second Modification does not teach "a plurality of non-electrically functional channel structures surrounding the TAC region," as its structures are only on opposite sides of the alleged TAC region, and do not surround it.

For Ground 2 (Toyama’s First Exemplary Structure), the placement of the TAC region is to one side of the channel region—not “formed between the first and second channel regions” as required. Petitioner’s proposed modification—adding a second memory device—does not create a memory device with two channel regions and a TAC region between them, and would eliminate peripheral circuitry and interconnects.

For Ground 3 (Toyama’s Second Modification using Toyama’s First Exemplary Structure’s unitary dielectric fill material), Petitioner fails to show the combination would have been obvious as it not only eliminates a critical aspect of Toyama’s gate replacement process but also drastically restricts current flow in each of the gate layers. Petitioner’s purported motivations are belied by its own expert.

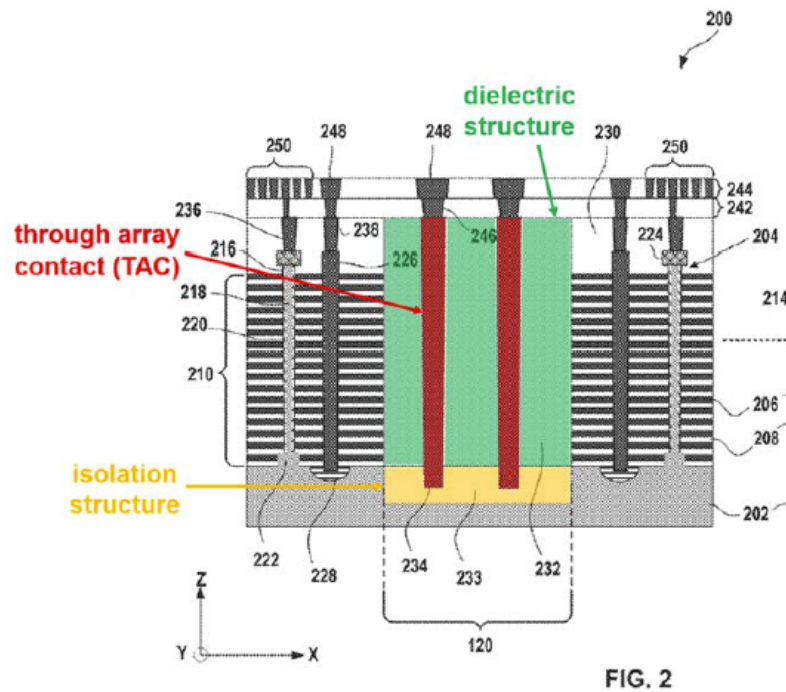
Finally, all grounds fail to meet the “etch stop plug” limitation of claim 10 because the alleged etch stop plugs are not between *each* local contact and each channel structure, as required by the plain meaning.

II. CLAIM CONSTRUCTION

A. “a dielectric structure” and “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” (Claim 8)

This limitation requires multiple “through array contacts (TACs)” to extend through the same dielectric structure.

First, consistent with the claims, the disclosed embodiments with multiple TACs in the '806 depict the TACs extending through the same dielectric, e.g., as shown in Figure 2:



Petitioner’s mischaracterization of the '806 as “contemplat[ing] embodiments with multiple dielectric structures (each of which includes a single TAC)” is wrong. The passage in question ('806, 21:11-28) simply describes the formation of a single TAC within “the dielectric structure” rather than the claimed plurality of TACs just as it describes the formation of a single “channel structure” in the “alternating dielectric layer stack.” There is no suggestion of using multiple dielectric structures, much less using a single TAC in each of the multiple dielectric structures. Using a separate dielectric structure for each TAC would contravene the '806 objective to reduce

fabrication complexity and cost. See POR 5-6; Yang ¶¶ 32-33; '806, 10:64-11:7, 20:33-41. Petitioner offers no response other than the unsupported assertion that such an embodiment is claimed. Reply, 6-7.

Second, Petitioner's understanding of Federal Circuit precedent is flawed. While an indefinite article "a" does not preclude more than one, there must still be at least one instance of the element that meets all the requirements of the claim applicable to that element. See *Finjan LLC v. SonicWall, Inc.*, 84 F.4th 963, 974-75 (Fed. Cir. 2023) ("Even if an infringing system can use 'one or more computers,' the plain language of the claims requires at least one of those computers to perform all the functions listed in the claims....."); *Salazar v. AT&T Mobility LLC*, 64 F.4th 1311, 1317 (Fed. Cir. 2023) (similar but regarding "microprocessors"). Thus, here one dielectric structure must meet all the requirements applicable to it, i.e., having TACs (plural) extending through it. The Board correctly concluded as much in its institution decision: "[w]hile the open-ended language may permit the claimed memory device to have more than one dielectric structure, this does not change the claim language that requires multiple TACs to extend vertically through a single dielectric structure." DI, 23-24; see also POR, 28-30.

Petitioner's cited cases (Reply 7-9) are inapposite, as they were not addressing the *Finjan* issue applicable here. *KCJ* merely addressed whether "a ... continuous ... chamber" encompasses one or more chambers, and not whether the same chamber

must satisfy each reference to the chamber throughout the claim. *KCJ Corp. v. Kinetic Concepts, Inc.*, 223 F.3d 1351, 1355-57 (Fed. Cir. 2000). Similarly, *ABS* addresses whether the claimed flow channel’s focusing region must be “configured for only a single sample stream” (i.e., whether the term excludes a second stream), which is a separate issue from whether the same sample stream must meet all the claimed requirements. *ABS Glob., Inc. v. Cytonome/St, LLC*, 84 F.4th 1034, 1040-43 (Fed. Cir. 2023); *Carrum Techs., LLC v. Ford Motor Co.*, No. CV 18-1647-RGA, 2023 WL 7407778, at *5 (D. Del. Nov. 9, 2023) (“Plaintiff’s reliance on *ABS Global* is misplaced because the Federal Circuit addressed a different issue there.”).

Petitioner’s reliance on *Baldwin* (Reply, 7-8) fares no better, and indeed the Federal Circuit in *Finjan* expressly distinguished *Baldwin* as merely addressing the principle that the indefinite article a means one or more, the decision was “***not addressing whether the use of a definite article to refer to the initial antecedent phrase requires the same component to perform the later limitation.***” *Finjan*, 84 F.4th at 974 (citing *Baldwin Graphic Sys., Inc. v. Siebert, Inc.*, 512 F.3d 1338, 1342 (Fed. Cir. 2008)).

B. “each local contact of the local contacts” (Claim 10)

The term “each local contact of the local contacts” of claim 10 should be afforded its plain and ordinary meaning: the term refers to the same antecedent “local

contacts disposed on the channel structures **and the slit structures**” recited in independent claim 8, from which claim 10 depends.

Contrary to Federal Circuit precedent defining “each” as “each and every,” *ResONet.com, Inc. v. Lansa, Inc.*, 346 F.3d 1374, 1379 (Fed. Cir. 2003), Petitioner seeks to reinterpret “**each** local contact of the local contacts” to mean only **some** of the claimed local contacts. Reply 1-5. Petitioner does not and cannot dispute that the antecedent basis for “**the** local contacts” is claim 8’s “local contacts disposed on the channel structures **and** the slit structures.” *See id.* Nonetheless, Petitioner improperly ignores this antecedent basis by contending that claim 10’s “**each** local contact of the local contacts” is limited to the subset of local contacts—i.e., only those on the channel structures. Reply, 5. This interpretation improperly reads the word “each” out of the claim. *See Merck & Co. v. Teva Pharms. USA, Inc.*, 395 F.3d 1364, 1372 (Fed. Cir. 2005) (“A claim construction that gives meaning to all the terms of the claim is preferred over one that does not do so.”).

Petitioner’s position rests on a mischaracterization of the specification and its embodiments. Petitioner incorrectly assumes that a local contact must be either on a channel structure or on a slit structure, but not both. Reply, 2-3. As PO has explained (POR 16), nothing precludes a local contact from being above both the channel structures and the slit structures. Indeed, the bit lines are local contacts disposed on both the channel structures and the slit structures (POR 16-19).

Petitioner asserts that “‘bit lines 250’ are not ‘local’ contacts” because they are not “in physical and electrical contact with the various memory array structures” as the ’806 requires. Reply 3-4. But the specification explains that the bit lines are “electrically connected to NAND strings 204, respectively, by corresponding contacts 246 and NAND string contacts 236.” ’806, 12:7-10. Therefore, at a minimum, the bit lines are physically and electrically connected to memory array structures—namely “contacts 246”—which Petitioner ignores. Petitioner does not, and cannot, dispute that contacts 246 are themselves “memory array structures” because they are structures within the memory array, just like the “NAND strings, gate line slits, [and] word lines.” ’806, 5:41-46, 20:16-21.

Petitioner’s argument that “bit lines” are not “local contacts” because bit lines are in an interconnect layer and the ’806 allegedly “describes ‘local contacts’ as distinct from ‘interconnect contacts’” (Reply 4-5 (citing ’806, 11:59-62, 12:7-10)) is directly contradicted by the specification. The ’806 defines the term “contact” as including interconnects: “the term ‘contact’ can broadly include any suitable types of interconnects including vertical interconnect access (via) lines and lateral lines (interconnect lines).” ’806, 11:31-34. Dr. Lee agreed with this broad understanding (Ex. 2008, 66:11-14), and his subsequent attempts to retreat from that opinion (Ex. Lee(II) ¶¶17-18) should be dismissed. The specification nowhere suggests that local contacts cannot reside within a labeled contact layer (e.g., layers 242 or 244).

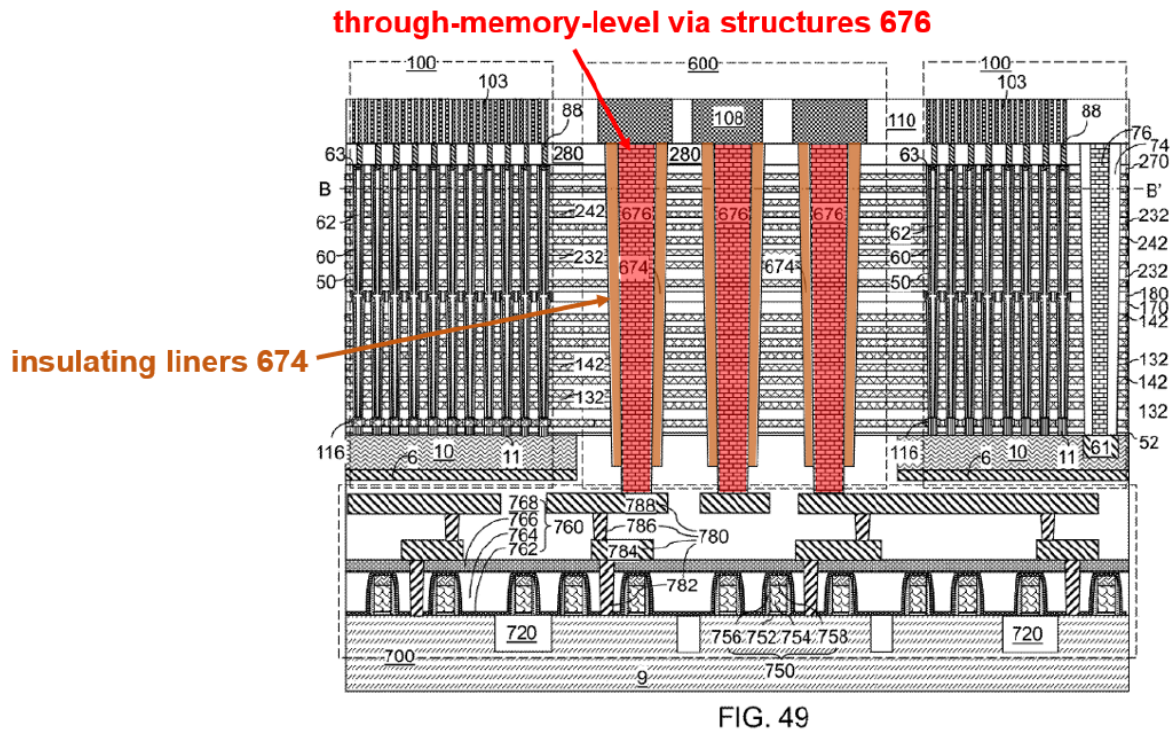
**III. TOYAMA FAILS TO DISCLOSE OR RENDER OBVIOUS CLAIM 8,
FROM WHICH THE CHALLENGED CLAIM DEPENDS**

A. Ground 1: Toyama’s Second Modification

Toyama’s Second Modification fails to teach multiple elements of claim 8, from which Challenged Claim 10 depends.

1. Toyama’s Second Modification Does Not Disclose or Render Obvious “a Plurality of Through Array Contacts (TACs) Extending Vertically Through the Dielectric Structure”

Toyama’s Second Modification neither discloses nor renders obvious this limitation. POR, 26-30. Toyama shows only a single through-memory-level via structure 676 (purported TAC)—extending through any one insulating liner 674 (purported dielectric structures), so no “plurality” of TACs traverses a given dielectric structure:



Toyama, Fig. 49 (annotated by PO).

Petitioner's claim construction arguments (Reply, 6-9) conflict with controlling precedent. *See* §II.A. *Finjan* requires that at least one recited element—here, a dielectric structure—to contain all claimed features.

Petitioner's fallback argument that Toyama's discrete liners collectively form a dielectric structure (Reply, 9-13) also misses the mark. The Board already rejected this theory when Petitioner could not “sufficiently explain how multiple constructed items can be considered...a single structure” under the very definition of “structure” (as “something...that is constructed”) that Petitioner advanced. DI, 23; *cf.* Pet. 31-32. Switching definitions (Reply, 10)—now quoting “something arranged in a definite pattern of organization” (Ex. 1021, 5) does not fix the problem. Every

component in a semiconductor is patterned with photolithography, yet that does not collapse distinct items into one “structure.”

Unable to ground its position in intrinsic evidence, Petitioner cites the below photographs, which are inapposite:



Ex. 1045



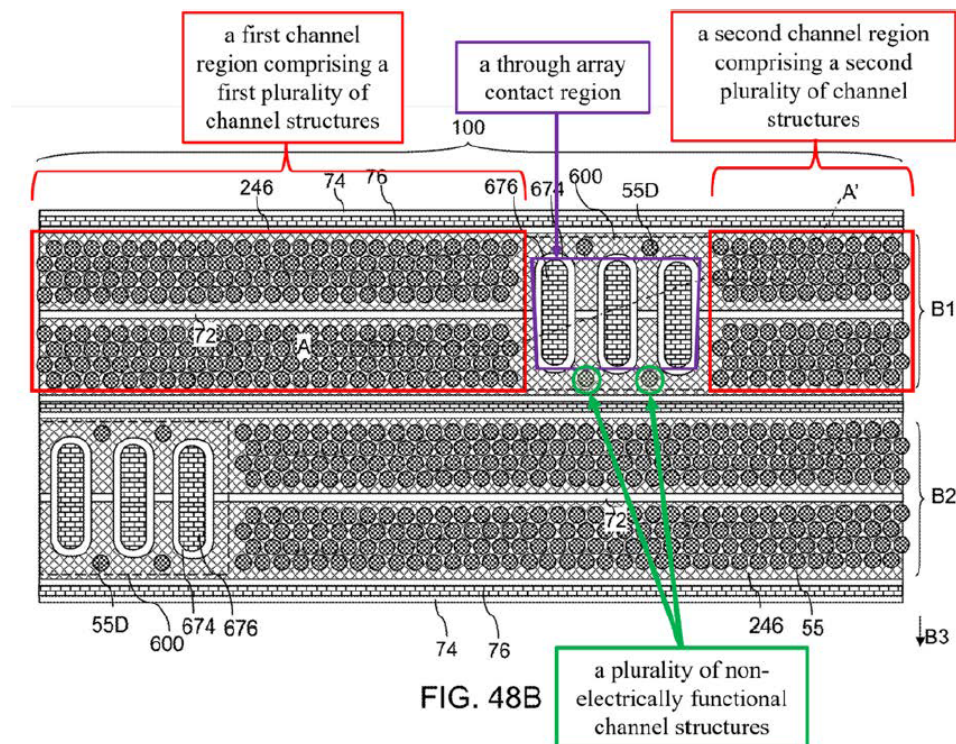
Ex. 1046

Unlike Toyama’s liner, which independently serves as a dielectric isolating the TAC, a single post or step cannot function as a wall or staircase structure, respectively. Also, Petitioner claims the wall’s “components [] are not all touching each other,” but the posts visibly do touch; moreover as Dr. Yang testified, a wall would include additional material binding the posts together. Ex. 1044, 47:23-25, 52:7-53:8. Likewise, Dr. Yang explained that “integral to the staircase structure” above is anchoring in the wall connecting the steps. Ex. 1044, 48:2-50:16. Petitioner’s expert agrees. See Ex. 2009, 86:5-90:2 (admitting a staircase structure requires “provid[ing]...intended function”), 94:11-97:9 (admitting that without the

additional anchoring mechanism of the wall the steps would “no longer exist as a functional unit”). The cited structures therefore consist of contiguous, integrated elements, and Petitioner’s reliance on them is misplaced.

2. Toyama’s Second Modification Does Not Disclose or Render Obvious “a Plurality of Non-Electrically Functional Channel Structures Surrounding the TAC Region”

Toyama’s Second Modification neither discloses nor renders obvious this limitation. POR, 30-33. Petitioner’s annotation of Fig. 48B below shows the purported non-electrically functional channel structures (green) flank the alleged TAC region (purple) on two sides; they do not surround it.



Pet. 51.

The structures fail to surround the region under any reasonable reading; therefore, construing “surrounding” is unnecessary. POR, 32. Rejecting Petitioner’s attempts to stretch “surrounding” to cover “features...on just two sides” is not contrary to the term’s plain meaning. *Contra* Reply 13. Petitioner’s “isthmus” analogy (Pet. 50-51; Ex. 1022), while misplaced, also does not support Petitioner’s argument. An isthmus is bordered by water ***along its full length*** on two sides, which in no way resembles Toyama.

Nor does the ’806 support Petitioner. *Contra* Reply 13. Rather, the ’806 states that dielectric structures of Figs. 1A-C are “surrounded by conductor/dielectric stack 210”—which confirms that the conductor/dielectric stack is on more than just two sides of the dielectric structures. ’806, 10:29-31. Contrary to Petitioner’s arguments (Pet. 50-52), the figures show the conductor/dielectric stack beyond two sides of each dielectric structure. Figure 1A illustrates the stack (lavender) on all four sides of the dielectric structure (pink) (indicated by regions of non-electrically functional channels 122 and contacts 132 (black circles) on all four sides):

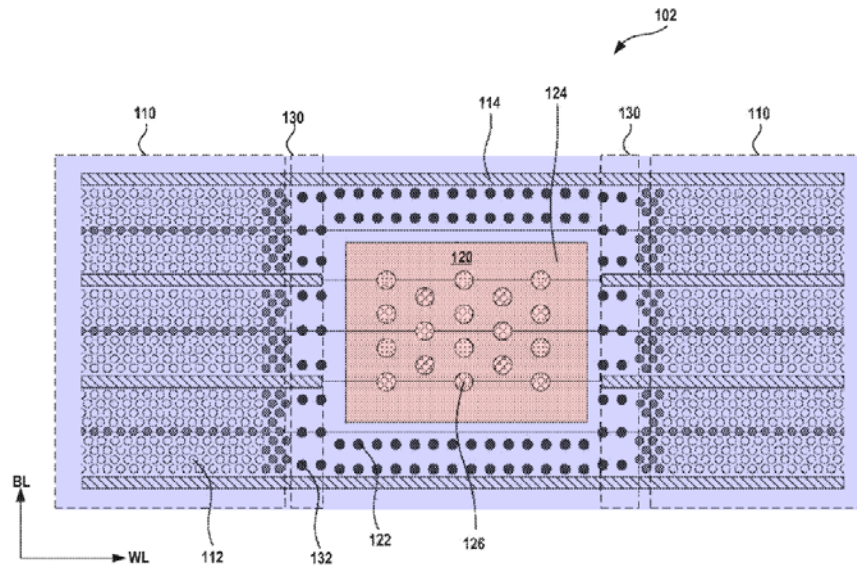
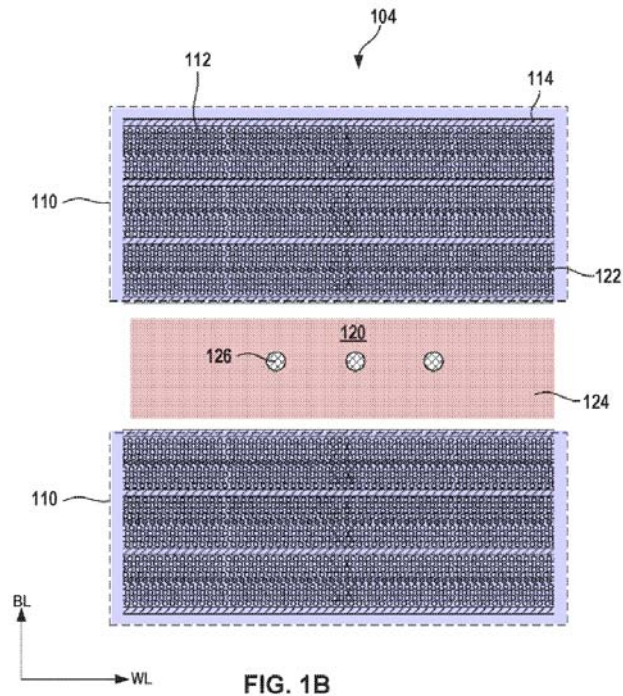


FIG. 1A

'806, Fig. 1A. Figure 1B shows conductor/dielectric stack (lavender) of the NAND string regions 110 extending beyond just the two sides of the dielectric structure 124 (pink):



'806 Fig. 1B (annotated). And Figure 1C (below) illustrates the conductor/dielectric stack (lavender) that forms the staircase region on more than just two sides of the dielectric structure 124 (pink):

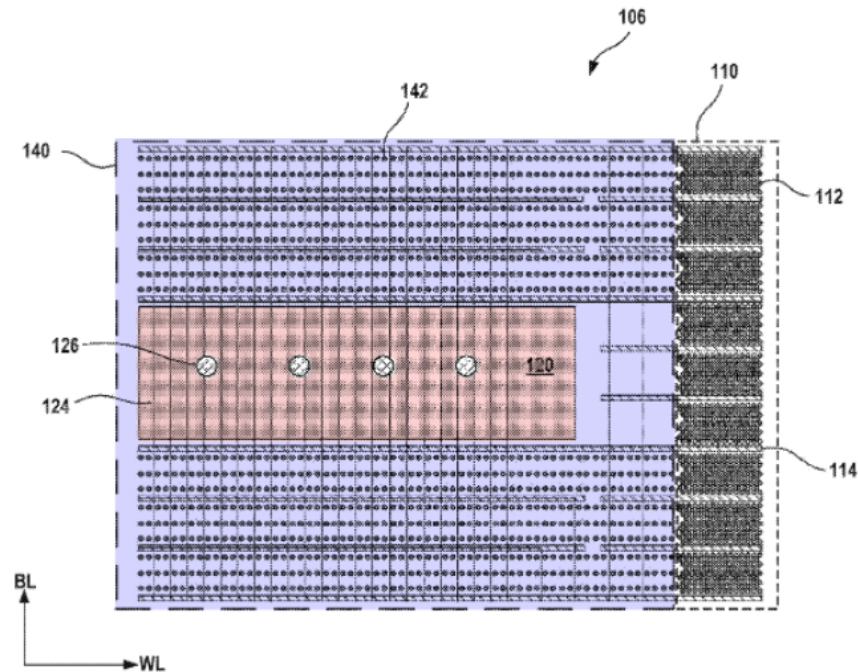


FIG. 1C

'806 Fig. 1C (annotated); *contra* Pet. 65 (incorrectly stating “dielectric structure 124 borders...staircase (i.e. word line) regions 140” “above and below” only), 51-52 (same).

Petitioner’s attempt to stretch Toyama’s disclosure—that dummy structures 55D are “provided at the periphery” of TAC region 600—fails. Reply 13 (citing Pet. 52, which cites Toyama, [0333]). “[A]t a periphery” does not mean the dummy structures are present along any more of the periphery than is shown and described. Toyama simply describes what Fig. 48B shows—a couple of dummy structures 55D at the top and bottom edges (i.e., at the periphery, not the center) of

the TAC region 600.² Dr. Lee’s new assertion that a POSITA would add dummy channels to the other sides of region 600 (Lee(II) ¶35) due to “edge effects” is untimely and should have been raised in the Petition. Further, this assertion is conclusory and lacks evidence that such “edge effects” were “well known,” would occur at the sides of region 600, or that dummy structures would mitigate these effects. Thus, Petitioner’s argument is improperly based on alleged general knowledge to supply a missing claim limitation.

Petitioner also has not shown that a POSITA would have found it obvious to “[p]lac[e] dummy stack structures on all sides of the TAC region” (Pet. 52-53; Reply 13). Petitioner’s assertion that this would provide additional “structural support” where “memory stack structures are not formed at a sufficiently high density” lacks evidentiary support. Pet. 23-53; Lee(I) ¶121 (quoting Toyama, [0182]); Lee(II) ¶36. Toyama contemplates “support pillar structures” near the staircase region, where memory stack structures are sparse (Toyama, Figs. 4A-4B; [0182]), but Petitioner has not shown that the periphery of the “through-memory-level via region” where channel structures are present, is similarly sparse. In fact, the left and right sides of

² Dr. Yang’s statement that a rectangle’s periphery is “the four sides of the rectangle” does not support Petitioner’s interpretation (Reply 13). Any location on one side of the rectangle is “at a periphery.”

the through-memory-level via region 600, where Petitioner proposes adding dummy stack structures, border memory stack structures (Toyama, Fig. 48B). Replacing them with dummy stack structures would only reduce memory capacity without adding mechanical support, since the memory stack structure already provides it.

B. Ground 2: Toyama’s First Exemplary Structure

Toyama’s First Exemplary Structure does not disclose or render obvious the Challenged Claim at least because it fails to teach “*a through array contact (TAC) region formed between the first and second channel regions*” (claim 8). Specifically, the purported TAC region in Toyama is located to the side of a single, centralized channel region, not between two channel regions. POR 41-42. Furthermore, Petitioner’s attempt to address this deficiency using multiple 3D memory devices contradicts relevant case law and renders the Toyama’s memory structure inoperable.

1. Petitioner’s Modification Results in Multiple Devices, None of Which Meet the Claimed Configuration

Petitioner’s modification would yield multiple memory devices—not a single device that satisfies the elements of claim 8. POR 43-44.

Petitioner’s modification duplicates elements of Toyama into several independent memory planes (i.e., multiple memory devices), but this fragments the claim’s requirements of its “three-dimensional (3D) memory device.” Even if

multiple devices are permitted, at least one device must meet all claim limitations, which Petitioner’s modification does not provide.

Petitioner does not dispute that its “modification adds a second memory device.” POR, 39-40; Reply, 14-16. Petitioner’s argument that “one ‘device’ can be part of another ‘device’” (Reply 14-15) is irrelevant to the meaning of “3D memory device,” as these limitations cannot be satisfied by features spread across different devices. Petitioner’s interpretation would unreasonably mean that any device containing one or more 3D memory devices—such as a hard drive, backup server, a server farm, or any plane, ship, or car with 3D flash memory used to store navigation data—would itself be a 3D memory device regardless of whether there is a single functional unit that meets every claim limitation.³ These claims are not directed to all memory devices everywhere or even multiple 3D memory devices within a larger device; they are directed a single “three-dimensional (3D) memory device” that must meet each of the claimed requirements.

Petitioner’s selective citation to the specification does not support its interpretation. *Cf.* Reply, 14 (citing ’806, 5:30-37). The referenced passage does

³ Dr. Lee’s examples from the extrinsic evidence about the usage of the term “device” (Lee(II) ¶¶47-49) and Dr. Yang’s acknowledgement that a solid-state drive is a device (Lee(II) ¶50) are equally irrelevant.

not define “3D memory device” as encompassing multiple 3D memory devices, and both the claims and specification are directed to a single device’s fabrication and configuration.

Petitioner also misinterprets another ’806 passage, claiming a 3D memory device can include both an array device and a peripheral device on different substrates.⁴ Reply, 14-15 (citing ’806, 7:53-57); Lee(II) ¶46. This passage does not describe channel regions on different substrates or suggest that claim limitations can be met by features on different planes. Instead, the ’806 requires both channel regions to be part of the same memory device. POR, 43-44 (citing ’806, 11:8-14); Yang, ¶¶85-86 (citing ’806 Figs. 1A-B, 2). Toyama neither discloses nor suggests this arrangement.

Petitioner next argues that the “a” in “a three-dimensional (3D) memory device” may be plural. Reply, 16. However, the dispute is whether a single device must satisfy all limitations, regardless of additional devices present. Petitioner’s position—that different devices can collectively meet the claim—contradicts Federal Circuit precedent such as *Finjan* and *Salazar* (see §II.A) and leads to

⁴ Dr. Lee incorrectly equates the term “substrate” with “wafer” (Lee(II) at 31 n.3). The specification defines “substrate” as “material onto which subsequent material layers are added” (’806 4:47-49), which is not synonymous with “wafer.”

unreasonable results, e.g., a collection of devices where one has a dielectric structure, another has a staircase structure, and yet another has slit structures, could collectively meet the claim. Such a collection of devices is outside the claim's scope. Petitioner's reliance on *Catalina Mktg. Int'l, Inc. v. Coolsavings.com, Inc.* is misplaced. Reply 16. As Petitioner's flawed interpretation demonstrates, the preamble's "three-dimensional (3D) memory device" is necessary to "define[] a structurally complete invention." 289 F.3d 801, 808 (Fed. Cir. 2002).

Petitioner incorrectly claims that PO limits the benefit to placing a TAC region between channel structures. Reply, 15-16; Lee(II) ¶¶51-53. This is not the case. The claims only require that at least one TAC region be between a first and second channel region of the same device. The presence of a TAC region elsewhere (e.g., in the staircase region as Fig. 1C shows), does not change that the **same** "3D memory device" includes a TAC region between two channel regions (as Fig. 1A shows).

2. Petitioner's Modification Results in an Inoperable Device

Petitioner's proposed modification results in a configuration missing the essential interconnects and support circuitry for an operable device. POR, 44-52. Specifically, duplicating memory-cell structures of Figure 17E next to one another along the hd1 axis (*see* Pet. 74) causes the left memory structure to overlap with the right memory cell's peripheral circuitry (shown in Fig. 17F, purple)—making one or both memory structures inoperable:

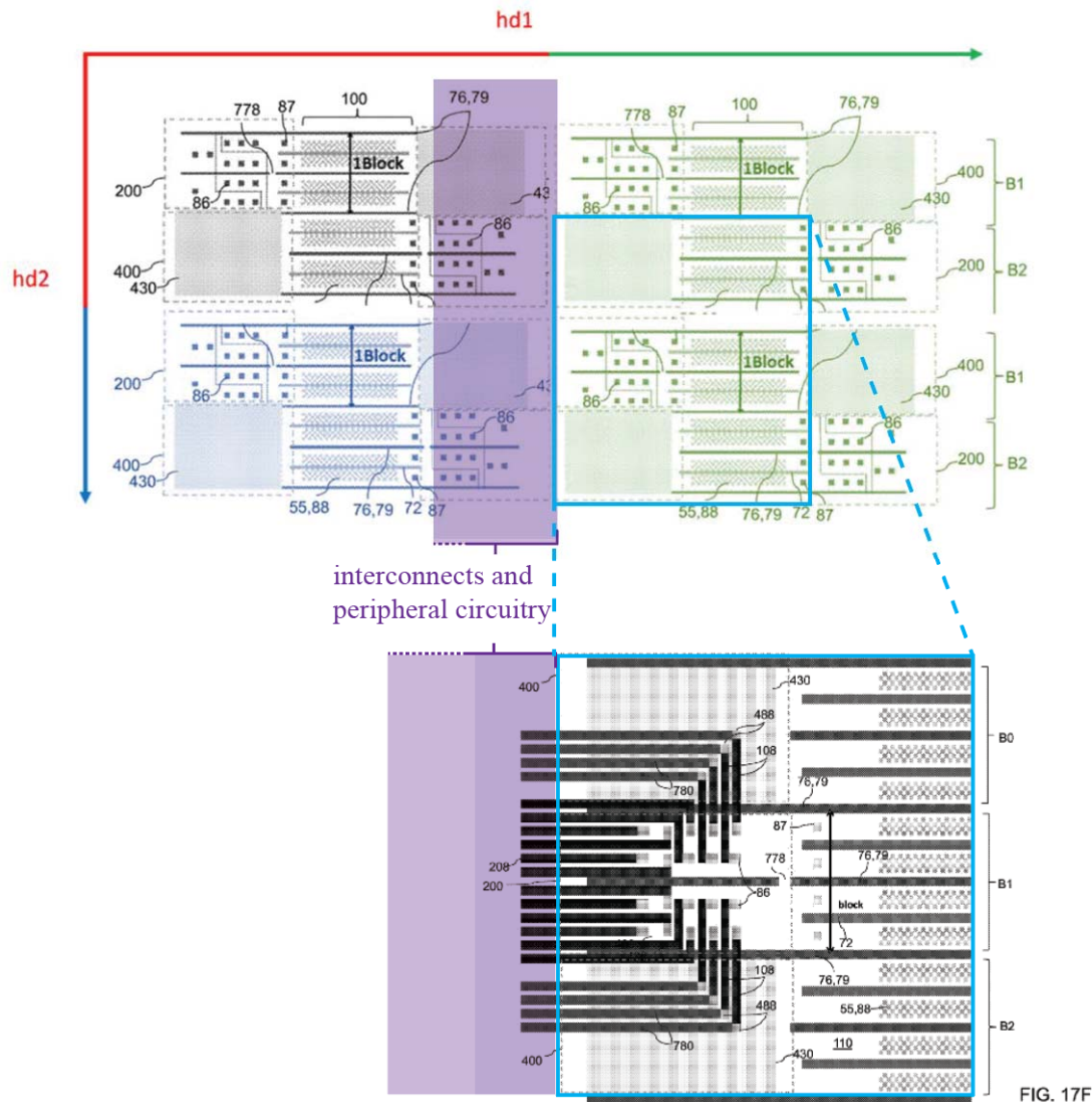


FIG. 17F

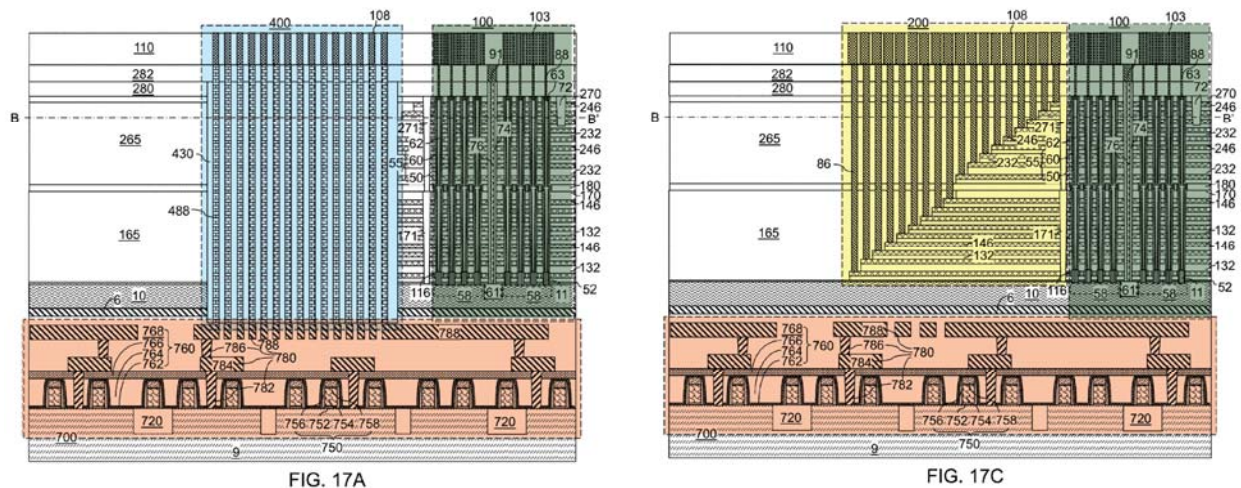
Pet. 74 (top, modifying Toyama, Fig. 17E with PO’s purple and blue annotations) and Fig. 17F (annotated by PO) (bottom); *see also* POR, 45-50; Yang, ¶¶89-92. Petitioner’s attempt to dismiss Toyama’s Fig. 17F as merely an “alternative” or optional, “exemplary structure” (Reply, 17) is incorrect. Toyama states that “FIGS. 17E and 17F are top-down views of” the same structure (Toyama, [0049]), and the “repeat[ed] layout shown in Fig. 17E in the hd1 and hd2 directions, **as shown** in the

modified figure [above]” is the trial ground (Pet. 74 (emphasis added)). Petitioner cannot just ignore critical elements of the structure that forms the trial ground depicted in Fig. 17F.

Petitioner’s suggestion that PO’s argument relies on “bodily incorporation” is incorrect. Reply, 18-19. The POR addresses the modification exactly as set forth in the Petition (Pet. 74), where Petitioner illustrated its proposal to “repeat the layout shown in Fig. 17E.” Under the mapping as depicted, Petitioner failed to address that Toyama’s full structure includes necessary adjacent structures that Petition’s mapping omits. Attempts in the Reply to cure this deficiency are untimely. Petitioner’s argument that upper-level interconnects may be omitted because Toyama uses permissive language is unpersuasive; Toyama frequently uses “may,” but this does not suggest undisclosed configurations. Toyama is designed to repeat only in the hd2 direction, with interconnects and peripheral circuitry on either side in the hd1 direction. POR, 48-50; Yang ¶¶90-91. Moreover, the general existence of multiple-plane devices in the art does not change the fact that the proposed modification of Toyama would render one or more planes inoperable by omitting critical elements. *Contra* Reply, 18.

Petitioner’s late assertions that interconnects can be placed under, alongside, or above the array (Reply 18, Lee(II) ¶69) do not address Toyama’s disclosures of interconnects and circuits already under, alongside, and above the arrays, leaving no

room for Petitioner’s new modifications. For example, Toyama at [0251] describes the “upper level metal interconnect structures 208...coupled to the driver circuit devices” depicted in Figure 17F (above) to the left of the staircase region. And Figures 17A and 17C (below) illustrate the “underlying peripheral device region 700” (orange) to the left and beneath the TAC region (blue), staircase region (yellow), active region (green):



See also Toyama, [0164]-[0165].

Dr. Lee’s assertion that “YMTC does not dispute that [using]...multiple planes improves performance” (Lee(II) ¶53) is misplaced. As the POR states, the Petition did not present workable alternatives for introducing multiple planes in Toyama’s device. POR, 51. Without such alternatives, Dr. Lee’s claims of a “performance benefit” (Lee(II) ¶53) are speculative at best.

In conclusion, Petitioner has not shown that a POSITA would have disregarded Toyama’s teachings by duplicating its device in the hd1 direction, as

this would create significant interconnect issues. The Board’s preliminary opinion was issued without the benefit of the full record, including Dr. Yang’s testimony. The Board should revise its preliminary finding and reject Petitioner’s modification as non-obvious.

C. Ground 3: Toyama’s Second Modification in Combination with Toyama’s First Exemplary Structure

Petitioner’s modification (“Obviousness Combination”) fails to disclose or render obvious the Challenged Claim because (1) Petitioner fails to show that a POSITA would have made the hindsight-based modification and (2) it does not disclose or render obvious *“a plurality of non-electrically functional channel structures surrounding the TAC region”* (claim 8).

1. A POSITA Would Not Have Found It Obvious to Modify Toyama’s Second Modification in the Proposed Manner

(a) Petitioner’s Obviousness Combination Would Fail with Respect to Gate Replacement

Toyama teaches using the openings of the alleged TACs of the Second Modification to deposit etchant and conductive material during gate replacement; however, as explained in the POR, a POSITA would not have been motivated to add the First Exemplary Structure’s unitary dielectric fill around these TAC openings, as this would curtail a critical step in forming the memory gates. POR, 61-62.

The Petition overlooked this function and now Petitioner downplays the issue by claiming that the “backside contact trenches 79” (the alleged slits) would serve

the same purpose. Reply, 20. Yet, even if these slit structures were used for gate replacement, large areas would remain inaccessible to etchant and replacement metal, as Dr. Yang explained (Ex. 2004, ¶¶108-109, citing Ex. 2006). Petitioner leaves these issues entirely unaddressed.

Petitioner’s reliance on Toyama’s First Exemplary Structure, which uses “trenches 79” for gate replacement (Reply, 20), is misplaced because this structure lacks the claimed dielectric block within the memory cell array of Toyama’s Second Modification, which narrows the etchant and metal deposition flow paths and complicates gate replacement. In the First Exemplary Structure, the dielectric is present only in the staircase region, where the flow path is not restricted, and gate uniformity is less critical. Petitioner’s textbook exhibits (Exs. 1013-1014) likewise do not address dielectric blocks in the array region.

Contrary to Petitioner’s arguments, *Uber Techs., Inc. v. X One, Inc.* is inapposite—the ’806 is not “‘entirely silent on how to’ perform gate replacement using only slit structure openings.” *Contra* Reply, 20-21 (quoting 957 F.3d 1334, 1339 (Fed. Cir. 2020)). The ’806 describes the process for gate replacement using slit structures (’806, 16:27-34) and specifies the etching process and etchant used (’806, 16:35-46). Furthermore, the ’806 geometry provides more open flow paths than Toyama’s as shown by comparing ’806 Fig. 1A (where the slits do not face dielectric trenches, which would obstruct etchant flow) *with* Toyama Fig. 47B

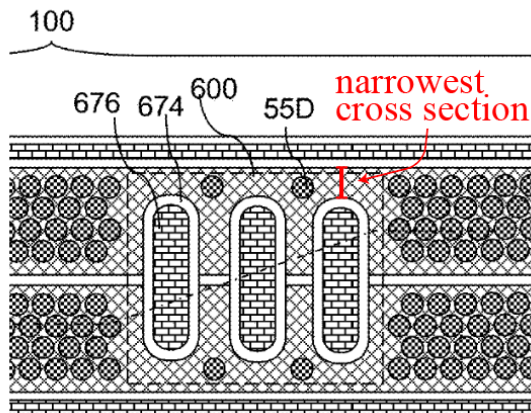
(where trenches 72 run the length of the array and obstruct etchant flow). See Toyama [0198] (explaining trenches 72 are formed in the “sacrificial layer” before gate replacement), [0343] (same).

(b) Petitioner’s Obviousness Combination Would Block Current and Render the Device Inoperable

As the Board recognized at institution, “replacing the conductive word lines with insulating material would eliminate the current that controls the memory, resulting in a non-functioning device.” DI, 44. PO’s further explanation (POR, 63-67) is un rebutted.

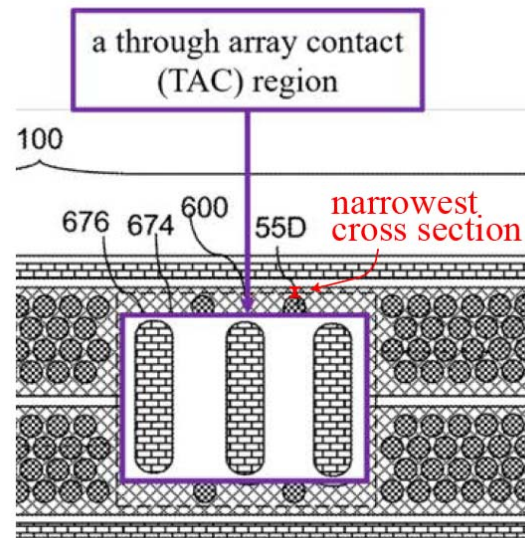
Petitioner’s assertion that word-line resistance is not a concern because the lines are “made out of metal” (Reply, 21-22) is belied by Dr. Lee’s testimony that “*nonuniform depositions of...metal* wire [can] increase...temperature[, and] cause *[a] local hot spot.*” Ex. 2006, 32:18-33:16 (emphasis added). Here, using metals does not negate the concern regarding resistance, because the layers are very thin. As Dr. Lee points out, resistance is inversely proportional to the cross-sectional area through which current flows. Lee(II) ¶83. Because the gate layers are very thin, the width of the passage (perpendicular to current flow) is critical to the resistance. As shown below, Petitioner’s modification drastically decreases the narrowest cross section (width × thickness) in Toyama’s gate layers:

Toyama



Toyama, Fig. 48B
(excerpt, PO annotation in red)

Petitioner's Proposed Modification



Pet. 116
(excerpt, PO annotation in red)

A smaller cross-sectional area at the bottleneck results in increased current density, which, as Dr. Lee admits, causes undesirable hot spots that “degrade” the device. See Ex. 2006, 36:16-37:1, 32:9-10; POR, 63-64.

Petitioner’s new argument based on a different Toyama embodiment (Reply, 22, citing Fig. 39B) improperly introduces new features requiring new analysis. Regardless, this embodiment’s unitary dielectric structure is irrelevant because its gates have a larger cross-section, and the memory array does not use dummy structures 55D.

The Reply's argument that a POSITA would have used staircase contacts on both sides to access the memory cells should be rejected as untimely. Even so, such changes would have been undesirable.

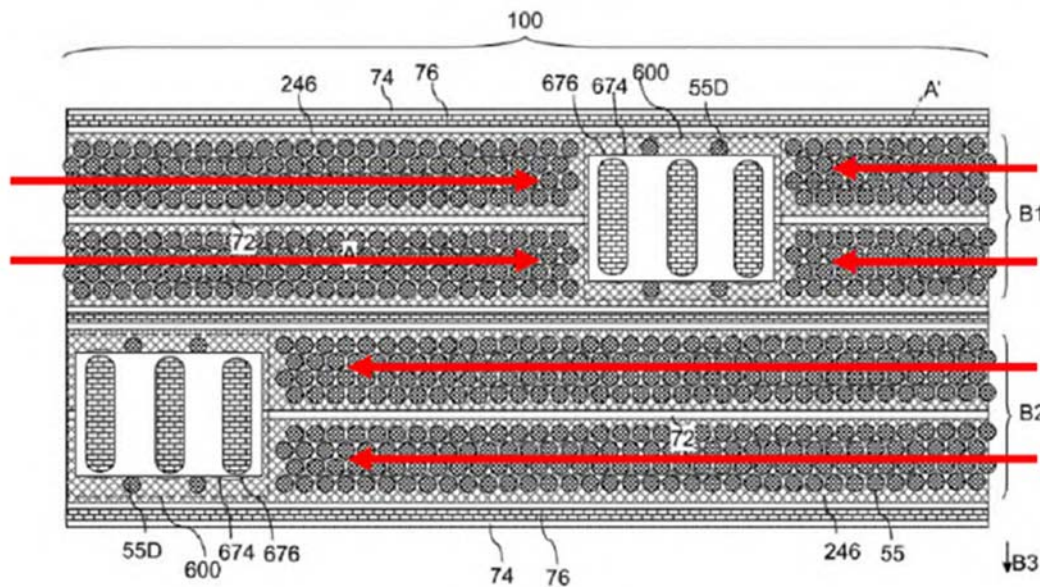


FIG. 48B

Lee(II) ¶91. **First**, adding staircases on both sides increases the device size, contrary to Toyama's goal of "decreas[ing]...device size/footprint." Toyama, [0389]. **Second**, the new modification would limit each memory block to one through-memory-level via region, eliminating critical interconnect capabilities. **Third**, Petitioner does not address the impact adding a second staircase has on peripheral devices and interconnects. Petitioner fails to explain why a POSITA would have been motivated to make these disadvantageous changes.

Petitioner's reliance on *Uber Techs.* again fails. Reply 23-24. The '806 teaches how to size the dielectric structure with the help of the isolation structure. *See e.g.*, '806, 10:35-48, 14:63-15:36, 21:20-28. And the '806 geometry (discussed above) provides larger current paths. *See* '806, Fig. 1A. Petitioner disregards these enabling teachings and incorrectly claims PO's arguments are based on the figures drawn to scale (Reply, 23-24). In fact, PO's arguments are based on the '806's teachings of a novel configuration using a dielectric structure, formed to the desired size with the help of an isolation structure. *See, e.g.*, POR, 64-66.

Lastly, *Intel Corp. v. PACT XPP Schweiz AG* is inapposite. Reply 26 (quoting 61 F.4th 1373, 1380 (Fed. Cir. 2023)). While showing "an 'improvement' in the categorical sense" is not required, Petitioner must show that a unitary dielectric fill material is a "suitable option" for Toyama's Second Modification. *See Commscope, Inc. v. Tq Delta, LLC*, 2023 WL 7491181, at *9 (P.T.A.B. Nov. 13, 2023) (distinguishing *Intel*). Petitioner has not done so, and as explained, a dielectric fill material is not a suitable replacement for Toyama's dielectric liner in the array region.

(c) Petitioner's Proposed Motivations for the Obviousness Combination are Flawed

For the reasons discussed above and in the POR (POR, 58-70), a POSITA would not have been motivated to make the proposed modification or have had a reasonable expectation of success. Petitioner incorrectly claims that PO's arguments

require the Obviousness Combination to be “superior to Toyama’s expressly disclosed embodiments” (Reply, 26). In fact, Toyama does not disclose the proposed modification, and Petitioner has not identified a viable motivation for a POSITA to have made the proposed changes or addressed the several reasons a POSITA would have lacked a reasonable expectation of success. The purported advantages cited by Petitioner are **not** actual advantages (POR, 67-69). Without a motivation, a POSITA would not have made Petitioner’s proposed changes, especially given the disadvantages, such as faulty gate replacement and blocked word line current.

Petitioner’s only alleged benefit to modify Toyama’s Second Modification—lower capacitive coupling—is contradicted by Dr. Lee repeatedly testifying that a thin liner offers better electrical performance than a solid dielectric block. Ex. 2009, 100:17-101:6, 97:15-100:13; Lee(II) ¶25. Dr. Lee also explained the physical advantages of a liner over a dielectric structure. Ex. 2009, 97:16-99:21.

Dr. Yang’s un rebutted testimony (Yang ¶116) further establishes that Toyama’s Second Modification already minimizes capacitive coupling by “shorten[ing] the signal path” (Toyama, [0377]). Petitioner also misrepresents PO’s position as “ignor[ing]” conductive layers in discussing the length of close proximity. Reply, 27. In fact, PO used an exemplary conductive layer to show that capacitive coupling between conductive layers and the alleged TACs is minimal compared to

the much larger capacitive coupling between neighboring conductive layers. POR, 67-68; Ex. 2006, 27:2-6. Petitioner does not address these arguments.

Finally, the alleged benefits of Toyama’s Second Modification TAC placement are irrelevant to the proposed combination. The trial ground is to “**modify Toyama’s Second Modification** to electrically isolate ‘through-memory-level via structures 676’ **with a unitary dielectric fill material**, as taught by Toyama’s first exemplary structure.” Pet. 103-104, 101-113; *contra* Reply 26-28. Petitioner fails to explain how the benefits of TACs in the memory array region are relevant to “modify[ing] Toyama’s Second Modification” when it already includes TACs in that region.

2. Petitioner’s Obviousness Combination Does Not Disclose or Render Obvious “a Plurality of Non-Electrically Functional Channel Structures Surrounding the TAC Region”

Petitioner’s Obviousness Combination neither discloses nor renders obvious this limitation (POR, 70-71). Petitioner’s Reply arguments fail for the same reasons as Ground 1 (§III.A.2).

IV. TOYAMA FAILS TO DISCLOSE OR RENDER OBVIOUS THE ADDITIONAL LIMITATION OF CHALLENGED CLAIM 10 (ALL GROUNDS)

Petitioner does not dispute that its Petition mappings fail to meet the requirement in dependent claim 10 of an etch stop between **each** local contact and each channel structure (*see* §II.B).

Instead, Petitioner introduces improper new claim mappings relying on a bit line as the purported local contact (Reply, 29-32), which also fail to meet the claim. Petitioner argues that its new mappings should be permitted (Reply, 29 n.6 (citing *Apple*, 2024 WL 3084509, at *5)), but the cited case is inapposite because PO has not proposed a new claim construction—PO is relying on the plain language of the claim. Instead, Petitioner is belatedly and improperly trying to correct its failure of proof.

Regardless, in relying on bit lines to address dependent claim 10, Petitioner fails to show that the bit line is “disposed on ... the slit structures” as required by independent claim 8. For both the First Exemplary Structure (Ground 2) and Second Modification (Ground 1) (and therefore also for the combination (Ground 3)), Toyama makes clear that there are no **bit lines 103** on the purported **slit structures 76**:

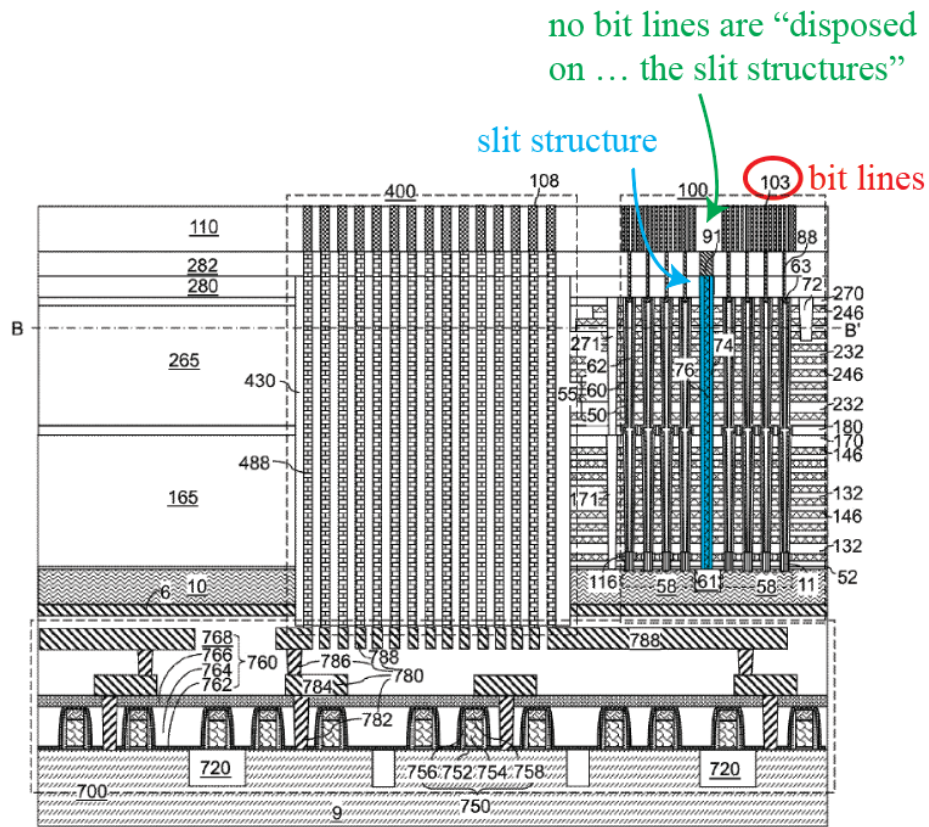


FIG. 17A

Toyama, Fig. 17A (first exemplary structure); *see also* Pet. 86-87.

bit lines

slit
structure

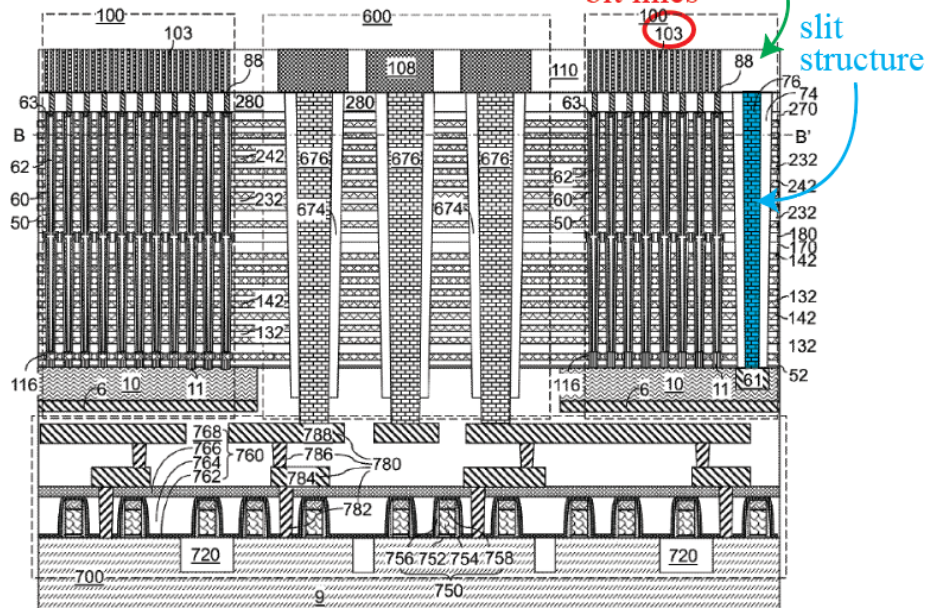
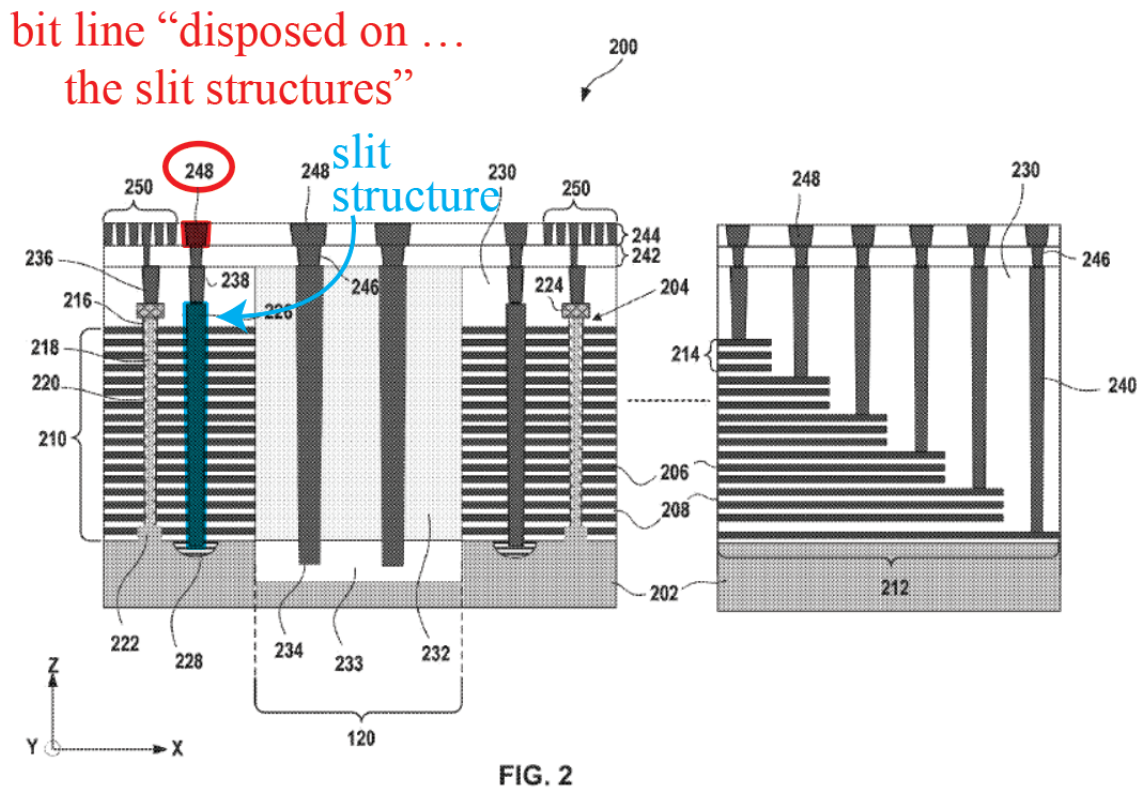


FIG. 49

Toyama, Fig. 49 (second modification); *see also* Pet. 40-42. Petitioner’s conjecture about the path of the bit lines in Fig. 17B and Fig. 48B (Reply 31-32) contradicts Fig. 17A and Fig. 49, which as depicted above, confirm that there are no bit lines on the purported slit structures. For the same reason, that bit lines 103 “extend along...direction hd2” (perpendicular to the figures above) (Reply 31-32) does not mean they extend in that direction so far as to cross over the slit structures. To the extent Petitioner is suggesting that Figs. 17A and 49 are inaccurate, it has provided no evidence of the purported inaccuracy and thus has failed to meet its burden of proof.

Petitioner's attempt to compare Toyama to the '806's bit lines is unavailing—in contrast to Toyama, the '806 expressly states that the “interconnect contacts 248 can include bit lines 250,” and the interconnect contact is disposed on the slit structure as depicted in Figure 2:



'806, 12:7-8, Fig. 2. See also POR 16-21; Yang ¶¶52-56.

Finally, to the extent Petitioner relies on obviousness, no motivation has been provided to run bit lines over slit structures. See Reply 29-32; Lee ¶¶101-107.

V. CONCLUSION

For the reasons above, Petitioner has failed to demonstrate by a preponderance of the evidence that the Challenged Claim of the '806 is anticipated or obvious. Accordingly, the Board should uphold the validity of the Challenged Claim.

Dated: August 6, 2025

Respectfully submitted,

By: /James L. Davis, Jr./

James L. Davis, Jr.
Reg. No. 57,325
ROPES & GRAY LLP
525 University Avenue, 8th Floor
Palo Alto, CA 94301
Telephone: +1-650-617-4794
James.L.Davis@ropesgray.com

Andrew T. Radsch
(*pro hac vice*)
ROPES & GRAY LLP
525 University Avenue, 8th Floor
Palo Alto, CA 94301
Telephone: +1-650-617-4011
Andrew.Radsch@ropesgray.com

Christopher M. Bonny
Reg. No. 63,307
ROPES & GRAY LLP
525 University Avenue, 8th Floor
Palo Alto, CA 94301
Telephone: +1-650-617-4011
Christopher.Bonny@ropesgray.com

Allen S. Cross
Reg. No. 74,729
ROPES & GRAY LLP
2099 Pennsylvania Avenue, NW
Washington, D.C. 20006-6807
Phone: +1-202-508-4708
Allen.Cross@ropesgray.com

*Attorneys for Patent Owner, Yangtze
Memory Technologies Co. Ltd.*

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S SUR-REPLY under 37 C.F.R. § 42.23 complies with the type-volume limitation in 37 C.F.R. § 42.24(c). According to the word-processing system's word count, the brief contains 5,598 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(c).

Dated: August 6, 2025

Respectfully submitted,

By: /James L. Davis, Jr./
James L. Davis, Jr.
Reg. No. 57,325
ROPES & GRAY LLP

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S SUR-REPLY UNDER was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

Lead Counsel	Back-up Counsel
Jeremy Jason Lang Registration No. 73,604 (jjlang@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 51 West 52nd Street New York, NY 10019 T: 212-506-5000; F: 212-506-5151 P52PTABDocket@orrick.com PTABDocketJL2@orrick.com PTABDocketJ3B3@orrick.com T61PTABDocket@orrick.com PTABDocketP2S7@orrick.com micron-ymtc_ohs@orrick.com	Travis Jensen Registration No. 60,087 (tjensen@orrick.com) K. Patrick Herman Registration No. 75,018 (pherman@orrick.com) Jared Bobrow <i>Pro Hac Vice</i> (jbobrow@orrick.com) Parth Sagdeo Registration No. 71,275 (psagdeo@orrick.com)
<i>Counsel for Petitioner Micron Technology, Inc.</i>	

Dated: August 6, 2025

By: /Jonathan Bradford/
Name: Jonathan Bradford

ROPES & GRAY LLP