

Patent Owner's Demonstrative Slides

Micron Technology, Inc. v. Yangtze Memory Technologies Company, Ltd.
Inter Partes Review of
U.S. Patent No. 10,937,806
September 4, 2025

IPR2024-00791 and IPR2024-00911
Patent Trial and Appeal Board
United States Patent and Trademark Office

I. Introduction

Table of Abbreviations

Abbreviation	Description
'806	U.S. Pat. No. 10,937,806
'806FH	File History of U.S. Pat. No. 10,937,806
Challenged Claims	'806, Claims 8-12
Patent Owner or PO	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
Board	USPTO Patent Trial and Appeal Board
IPR-791	IPR2024-00791 (<i>Inter Partes</i> Review of U.S. Patent No. 10,937,806), challenging Claims 8-9, 11-12
IPR-911	IPR2024-00911 (<i>Inter Partes</i> Review of U.S. Patent No. 10,937,806), challenging Claim 10
Pet-791	Petition for IPR791 (IPR2024-00791, Paper 1)
Pet-911	Petition for IPR911 (IPR2024-00911, Paper 1)
ID-791	Decision Granting Institution for IPR791 (IPR2024-00791, Paper 11)
ID-911	Decision Granting Institution for IPR911 (IPR2024-00911, Paper 12)
POR-791	Patent Owner's Response for IPR791 (IPR2024-00791, Paper 14)
POR-911	Patent Owner's Response for IPR911 (IPR2024-00911, Paper 15)
Reply-791	Petitioner's Reply for IPR791 (IPR2024-00791, Paper 16)
Reply-911	Petitioner's Reply for IPR911 (IPR2024-00911, Paper 17)
Sur-Reply-791	Patent Owner's Sur-Reply for IPR791 (IPR2024-00791, Paper 18)
Sur-Reply-911	Patent Owner's Sur-Reply for IPR911 (IPR2024-00911, Paper 22)
Lee(I)-791	Original Declaration of Dr. Jack C. Lee for IPR791 (IPR2024-00791, Ex. 1003)
Lee(II)-791	Reply Declaration of Dr. Jack C. Lee for IPR791 (IPR2024-00791, Ex. 1043)
Lee(I)-911	Original Declaration of Dr. Jack C. Lee for IPR911 (IPR2024-00911, Ex. 1003)
Lee(II)-911	Reply Declaration of Dr. Jack C. Lee for IPR911 (IPR2024-00911, Ex. 1043)
Yang-791	Declaration of Dr. Woodward Yang for IPR791 (IPR2024-00791, Ex. 2004)
Yang-911	Declaration of Dr. Woodward Yang for IPR911 (IPR2024-00911, Ex. 2005)
Toyama	U.S. Patent Publication No. 2017/0179026
Lee 1/30/25 Tr.	Transcript of January 30, 2025 Deposition of Dr. Lee for IPR791 and IPR911 (IPR2024-00791, Ex. 2006 and IPR2024-00911, Ex. 2006)
Lee 6/13/25 Tr.	Transcript of June 13, 2025 Deposition of Dr. Lee for IPR791 and IPR911 (IPR2024-00791, Ex. 2008 and IPR2024-00911, Ex. 2010)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
POSITA	Person of ordinary skill in the art

All citations within quotations omitted herein, and emphasis added unless otherwise indicated

'806, Claims 8-12

- Claim 8 of the '806 recites:

[8.pre] A three-dimensional (3D) memory device, comprising:

[8.a] an alternating conductor/dielectric layer stack;

[8.b] a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;

[8.c] first and second channel regions comprising first and second pluralities of channel structures, respectively;

[8.d] slit structures extending vertically through the alternating conductor/dielectric layer stack;

[8.e] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;

[8.f] local contacts disposed on the first and second channel structures and the slit structures;

[8.g] a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and

[8.h] a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.

- Claim 9 of the '806 recites:

The 3D memory device of claim 8, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.

- Claim 10 of the '806 recites:

[10.pre] The 3D memory device of claim 8, further comprising:

[10.a] a substrate;

[10.b] an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and

[10.c] an epitaxial layer disposed between the substrate and the first or second channel structures.

- Claim 11 of the '806 recites:

The 3D memory device of claim 8, wherein the dielectric material comprises silicon oxide.

- Claim 12 of the '806 recites:

The 3D memory device of claim 8, wherein the TACs comprise a conductive material.

Grounds

Claims	Ground	IPR
'806, claims 8-12	(1) Toyama's Second Modification Obviousness	IPR-791 (claims 8-11, 11-12) and IPR-911 (claim 10)
'806, claims 8-12	(2) Toyama's First Exemplary Structure Obviousness	IPR-791 (claims 8-11, 11-12) and IPR-911 (claim 10)
'806, claims 8-12	(3) Toyama's Second Modification in view of Toyama's First Exemplary Structure Obviousness	IPR-791 (claims 8-11, 11-12) and IPR-911 (claim 10)

Pet-791, 7; Pet-911, 15.

Disputed Issues

Issue	Slides
CLAIM CONSTRUCTION: “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” (Limitation [8.g]) “each local contact of the local contacts” (Limitation [10.b])	Slides 7-13
GROUND 1: TOYAMA’S SECOND MODIFICATION - Independent Claim 8: Toyama’s Second Modification Does Not Disclose or Render Obvious “a plurality of through array contacts (TACs) extending vertically through the dielectric structure” (Limitation [8.g]) - Independent Claim 8: Toyama’s Second Modification Does Not Disclose or Render Obvious “a plurality of non-electrically functional channel structures surrounding the TAC region” (Limitation [8.h]) - Petitioner Fails to Show That Toyama’s Second Modification Discloses or Renders Obvious “an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the First and Second Channel Structures” (Limitation [10.b])	Slides 14-24
GROUND 2: TOYAMA’S FIRST EXEMPLARY STRUCTURE - Independent Claim 8: Toyama’s First Exemplary Structure Does Not Disclose or Render Obvious “a through array contact (TAC) region formed between the first and second channel regions” (Limitation [8.g]) - Petitioner Fails to Show That Toyama’s First Exemplary Structure Discloses or Renders Obvious “an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the First and Second Channel Structures” (Limitation [10.b])	Slides 25-34
GROUND 3: TOYAMA’S SECOND MODIFICATION IN COMBINATION WITH TOYAMA’S FIRST EXEMPLARY STRUCTURE - A POSITA Would Not Have Found It Obvious to Modify Toyama’s Second Modification in the Proposed Manner - Independent Claim 8: Petitioner’s Obviousness Combination Does Not Disclose or Render Obvious “a plurality of non-electrically functional channel structures surrounding the TAC region” (Limitation [8.h]) - Petitioner Fails to Show That the Obviousness Combination Discloses or Renders Obvious “an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the First and Second Channel Structures” (Limitation [10.b])	Slides 35-43

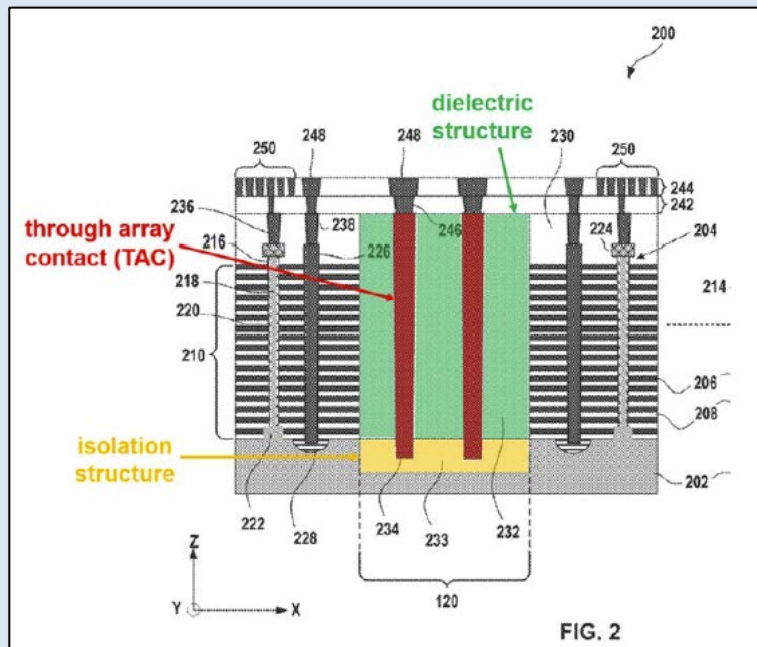
II. Claim Construction

Claim 8 Requires Multiple Through Array Contacts (TACs) Extending Through the Same Dielectric Structure

- Claim 8 of the '806 recites:

[8.g] a plurality of through array contacts (TACs) extending vertically through the dielectric structure

- The disclosed embodiments with multiple TACs depict the *TACs extending through the same dielectric structure*:
- The embodiment with a single TAC is irrelevant to claim 8
- The '806 patent explains that the dielectric structure avoids the complex etching process of etching vias through the alternating stack:



'806, Figure 2.

'806 patent: “[E]tching through dielectric structure 232 can be advantageous (e.g., involve fewer etch operations) compared to etching through a stack of alternating layers having the same overall thickness. For example, the formation of TACs 234 in an alternating layer stack with a thickness of about 6 μm or more (e.g., for a 64 tier 3D memory device) requires multiple etch and fill operations—therefore, increases the fabrication cost.”

'806, 10:62-11:4; Yang-791, ¶¶32; Yang-911, ¶32.

Claim 8 Requires Multiple Through Array Contacts (TACs) Extending Through the Same Dielectric Structure

- Federal Circuit precedent requires at least one instance of the element (here, the claimed “a dielectric structure”) that meets *all* of the requirements applicable to that element:

Federal Circuit: “Even if an infringing system can use “one or more computers,” **the plain language of the claims requires at least one of those computers to perform all the functions listed in the claims of the ARB Patent.**”

Finjan LLC v. SonicWall, Inc., 84 F.4th 963, 974-975 (Fed. Cir. 2023).

Federal Circuit: “Here, it does not suffice to have multiple microprocessors, each able to perform just one of the recited functions; **the claim language requires at least one microprocessor capable of performing each of the recited functions.**”

Salazar v. AT&T Mobility LLC, 64 F.4th 1311, 1317 (Fed. Cir. 2023).

Claim 10 Refers to the Local Contacts Disposed on the Channel Structures and the Slit Structures

- Claim 10 of the '806 recites:

[10.b] an etch stop plug interposed between **each local contact of the local contacts** and each channel structure of the first and second channel structures

- The antecedent term is “local contacts disposed on the first *and* second channel structures and the slit structures”:

[8.f] **local contacts disposed on** the first and second **channel structures and the slit structures**;

Petitioner Reads the Word “Each” Out of the Claim

Term	Patent Owner’s Construction	Petitioner’s Construction
“each local contact of the local contacts” '806, C1. 10	Plain and ordinary meaning: refers to the same antecedent “local contacts disposed on the first and second channel structures and the slit structures” recited in independent claim 8 POR 9-11-14; Sur-Reply 911, 5-6.	Refers to local contacts on the channel structures Reply-911, 1-2.

Petitioner argues: “The parties’ dispute with respect to this limitation is whether *the term ‘each local contact’ refers to local contacts on the channel structures* (Petitioner’s position, Lee-Reply ¶¶10-19) or refers to local contacts on the channel structures and on the slit structures (PO’s position).¹ *PO’s construction, which excludes every embodiment of the specification, cannot be correct.*”

Reply-911, 1-2.

- Petitioner’s construction contradicts the plain meaning in view of the applicable antecedent basis
- Petitioner’s construction ignores Federal Circuit precedent:

Federal Circuit: “In the phrase immediately following the functional language, the claim recites, ‘said ID being generated as a function of the number, location, and length of **each** field in said first image.’ ‘961 patent, col. 8, ll. 23-25 (emphasis added). **This language shows that the claimed algorithm evaluates attributes of each (and every) field in the information to be displayed, i.e., the first image.**”

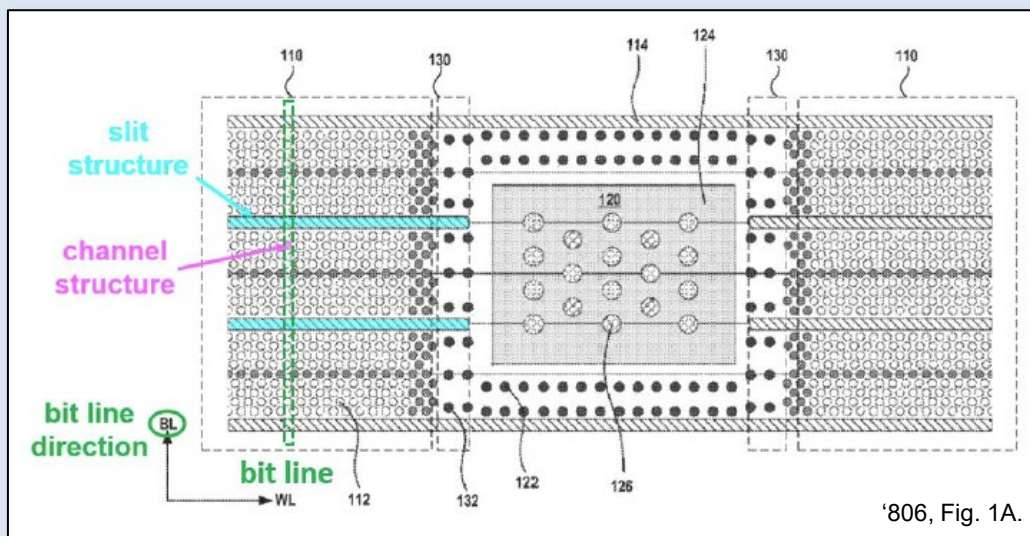
ResONet.com, Inc. v. Lansa, Inc., 346 F.3d 1374, 1379 (Fed. Cir. 2003); POR-911, 14; Sur-Reply-911, 6.

Petitioner Mischaracterizes the Specification and Its Embodiments

Petitioner argues: “[N]ot a single embodiment of the ‘806 meets PO’s construction.”

Reply-911, 2-3.

- But the specification discloses bit lines that are local contacts disposed on both the channel structures and the slit structures:



‘806 Patent: “In some embodiments, interconnect contacts 248 in interconnect layer 244 can include **bit lines 250, which are electrically connected to NAND strings 204**, respectively, by corresponding contacts 246 and NAND string contacts 236.”

‘806, 12:7-10.

‘806 Patent: “According to some embodiments, FIGS. 1A-1C are plan-views of various exemplary regions of a 3D memory device along **a bit line (BL) and a word line (WL) direction as denoted by respective axes labeled BL and WL**. For example, FIG. 1A is a plan-view of an exemplary TAC region 102 of the 3D memory device.”

‘806, 5:66-6:4; see also ‘806, 5:66-7:10.

Petitioner Mischaracterizes the Specification and Its Embodiments

Petitioner argues: “As an initial matter, ‘bit lines 250’ are not ‘local’ contacts. ... [A]s Figure 2 shows, ‘bit lines 250’ ... are not in physical contact with ‘slit structures 226’.”

Reply-911, 3.

- But the specification explains that (i) local contacts include contacts “in direct contact with the memory array structures” and (ii) bit lines are connected to memory array structures—contacts 246:

'806 Patent: “The contacts are referred to herein as ‘local contacts’ because they **are in direct contact with the memory array structures**....”

'806, 11:24-26.

'806 Patent: “In some embodiments, interconnect contacts 248 in interconnect layer 244 can include **bit lines 250, which are electrically connected to NAND strings 204, respectively, by corresponding contacts 246** and NAND string contacts 236.”

'806, 12:7-10.

Petitioner argues: “The patent describes ‘local contacts’ as distinct from ‘interconnect contacts.’”

Reply-911, 4.

- But the specification defines “contact” broadly to include any suitable type of interconnect:

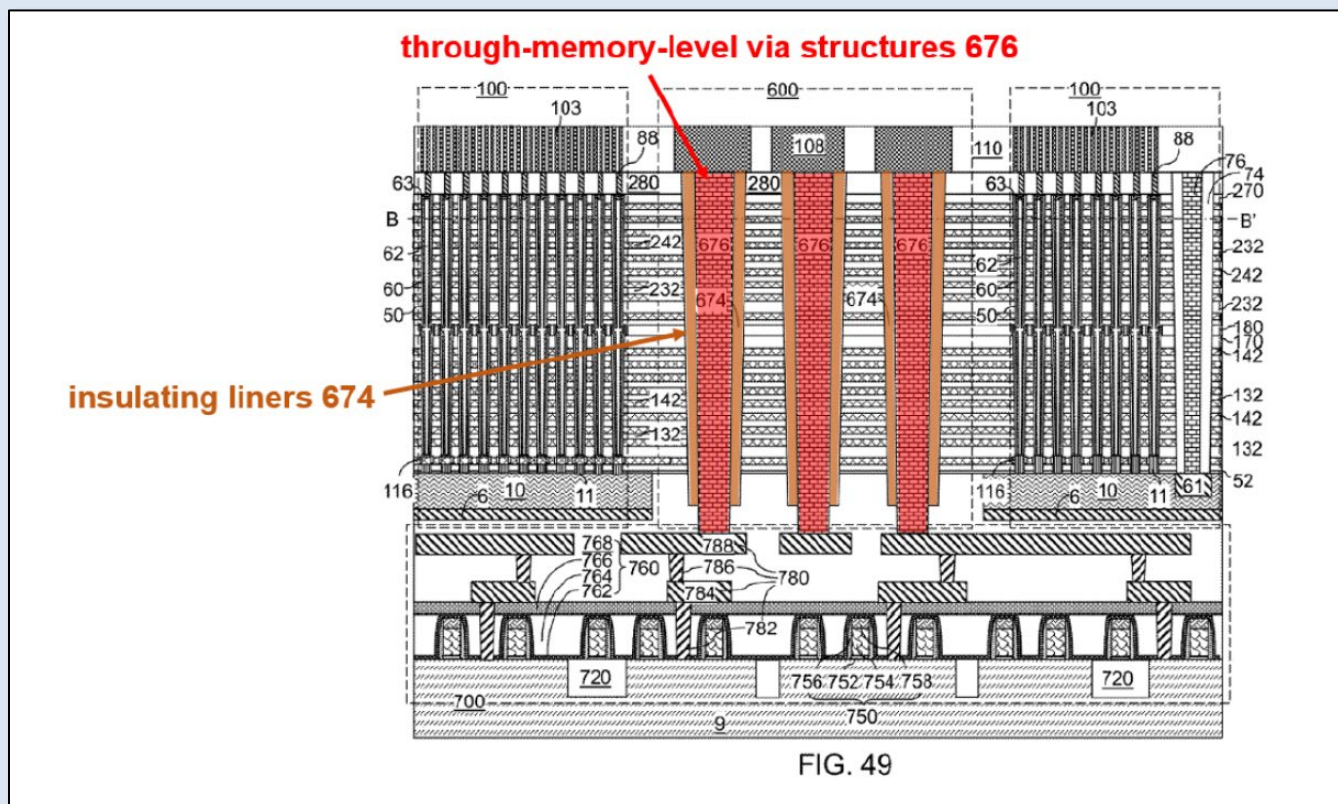
'806 Patent: “As used herein, **the term ‘contact’ can broadly include any suitable types of interconnects including vertical interconnect access (via) lines and lateral lines (interconnect lines).**”

'806, 11:31-34.

III. GROUND 1 (TOYAMA'S SECOND MODIFICATION): CLAIMS 8-12

Toyama's Second Modification Does Not Disclose or Render Obvious "a plurality of through array contacts (TACs) extending vertically through the dielectric structure" (Limitation [8.g])

- Only a single **through-memory-level via structure** extends through any one **insulating liner**



Toyama, Fig. 49 (annotated by PO showing Petitioner's mapping).

Toyama's Second Modification Does Not Disclose or Render Obvious "a plurality of through array contacts (TACs) extending vertically through the dielectric structure" (Limitation [8.g])

Petitioner argues: "PO does not dispute that *the same one or more dielectric structures* ('insulating liners 674') *satisfy all claim limitations*."

Reply-791, 7; Reply-911, 5.

- Petitioner's argument contravenes case law (*see* Slide 9)
- Petitioner failed to show that at least one purported dielectric structure satisfies all claim limitations

Toyama's Second Modification Does Not Disclose or Render Obvious "a plurality of through array contacts (TACs) extending vertically through the dielectric structure" (Limitation [8.g])

Petitioner argues: "[T]he combination of Toyama's 'insulating liners 674' are collectively a single dielectric structure."

Reply-791, 7-11; Reply-911, 9-13.

- The claimed dielectric structure simplifies etching process by avoiding etching multiple vias through the alternating metal/insulator stack (*see* Slide 8)
- Insulating liners are complete, functional, and separate structures—they do not work together to form a dielectric structure
- Lacking intrinsic evidence, Petitioner relies on irrelevant extrinsic examples of posts and steps, which are not individually complete and functional structures:



Reply-791, 9-10; Reply-911, 10-12.

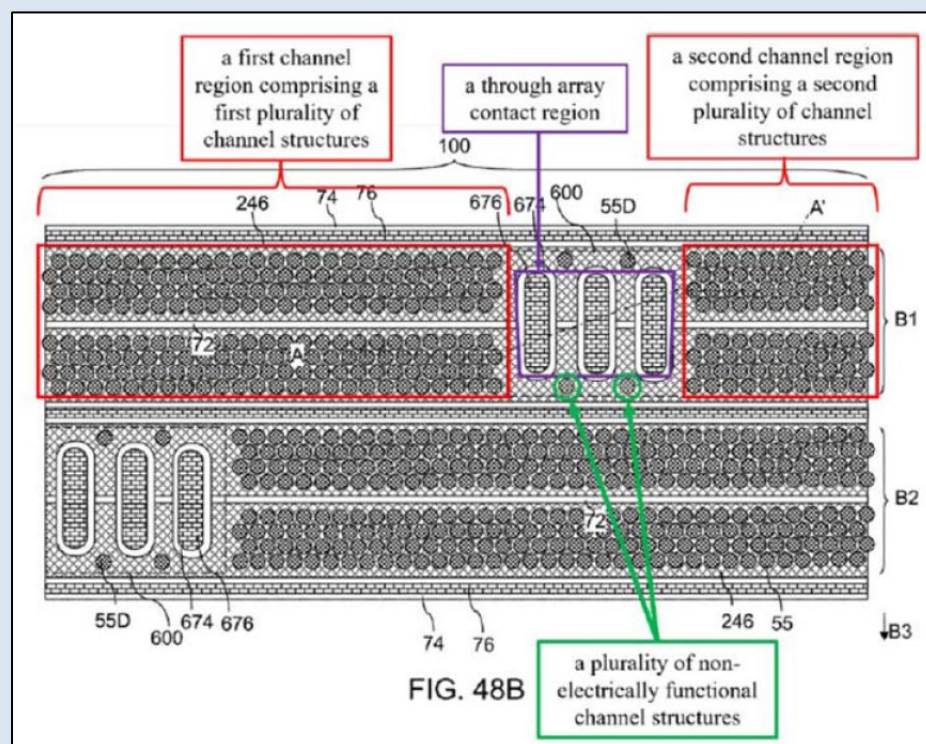
- Petitioner's expert admitted that without the additional anchoring mechanism of the wall, the steps would "no longer exist as a functional unit"

Lee 6/13/25 Tr., 94:11-97:9, 86:5-90:2.

POR-791, 18-22; Yang-791, ¶¶54-58; Sur-Reply-791, 7-10;
POR-911, 26-30; Yang-911, ¶¶64-68; Sur-Reply-911, 8-11.

Toyama's Second Modification Does Not Disclose or Render Obvious "a plurality of non-electrically functional channel structures surrounding the TAC region" (Limitation [8.h])

- Toyama's **dummy structures 55D** are sparsely disposed along two sides of the purported **TAC region** only, they do not surround the **TAC region** because these dummy structures do not extend beyond these two sides



Pet-791, 52 (Petitioner's annotations of Toyama, Fig. 48B); Pet-911, 51 (same).

Toyama's Second Modification Does Not Disclose or Render Obvious "a plurality of non-electrically functional channel structures surrounding the TAC region" (Limitation [8.h])

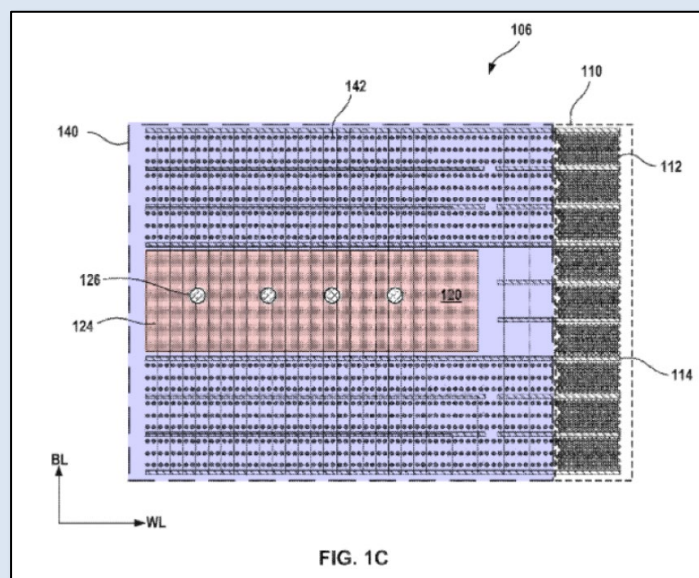
Petitioner argues: "But the PO ignores the Petition's *intrinsic* and extrinsic *evidence showing that a first feature may surround another on just two sides.*"

Reply-791, 12; Reply-911, 13.

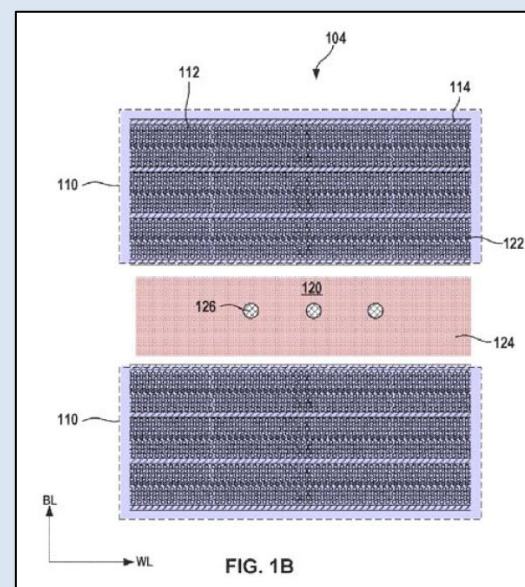
- The specification's use of "surrounding" does not cover "features ... on just two sides":

'806 patent: "In some embodiments, *dielectric structure 232 defines* the boundaries, the shape, and the size of **TAC region 120** (e.g., shown in FIGS. 1A-1C). Consequently, *as shown in the plan-views of FIGS. 1A-1C*, dielectric structure 232 can be *surrounded by conductor/dielectric stack 210.*"

'806, 10:29-31.



The **conductor/dielectric stack** on more than two sides of the **dielectric structure**



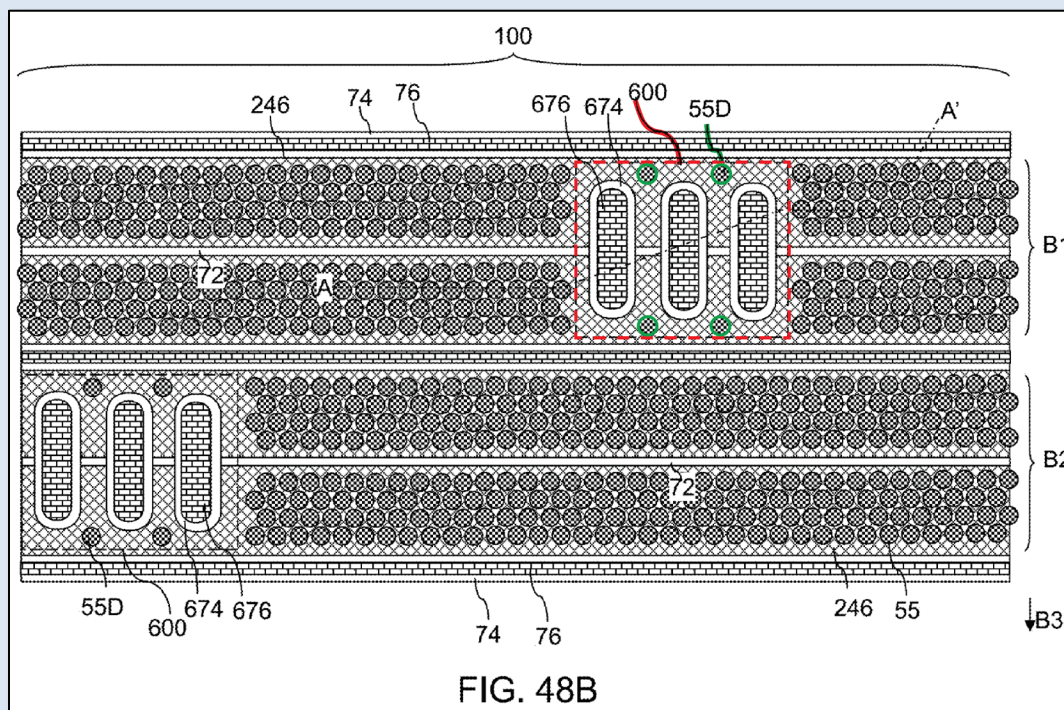
The **conductor/dielectric stack** extending beyond just two sides of **dielectric structure**

Toyama's Second Modification Does Not Disclose or Render Obvious "a plurality of non-electrically functional channel structures surrounding the TAC region" (Limitation [8.h])

Petitioner argues: "[A] POSITA would have understood *Toyama's statement that '[d]ummy memory stack structures 55D can be provided at the periphery of the through-memory-level via region 600' to disclose placing these non-electrically functional channel structures on four sides of the TAC region.*"

Pet-791, 53-54 (citing Toyama [0183]); Pet-911, 52-53 (same).

- But "at the periphery" teaches no more than what Toyama already illustrates, **dummy structures 55D** sparsely disposed along two sides of the purported TAC region:



Toyama's Second Modification Does Not Disclose or Render Obvious "a plurality of non-electrically functional channel structures surrounding the TAC region" (Limitation [8.h])

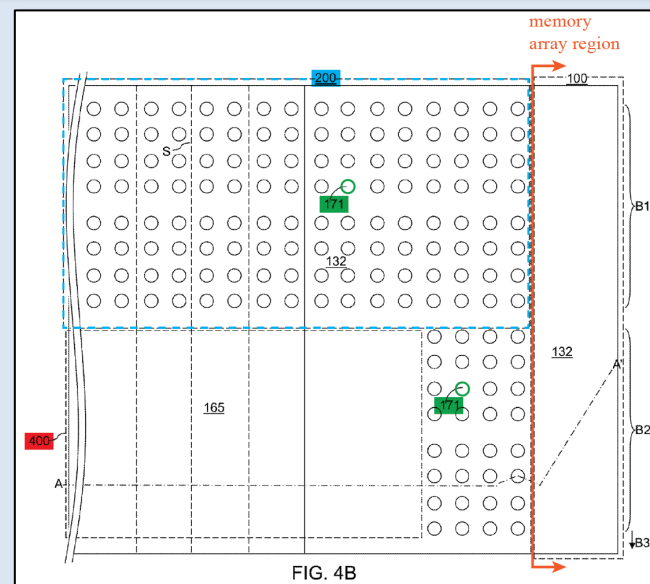
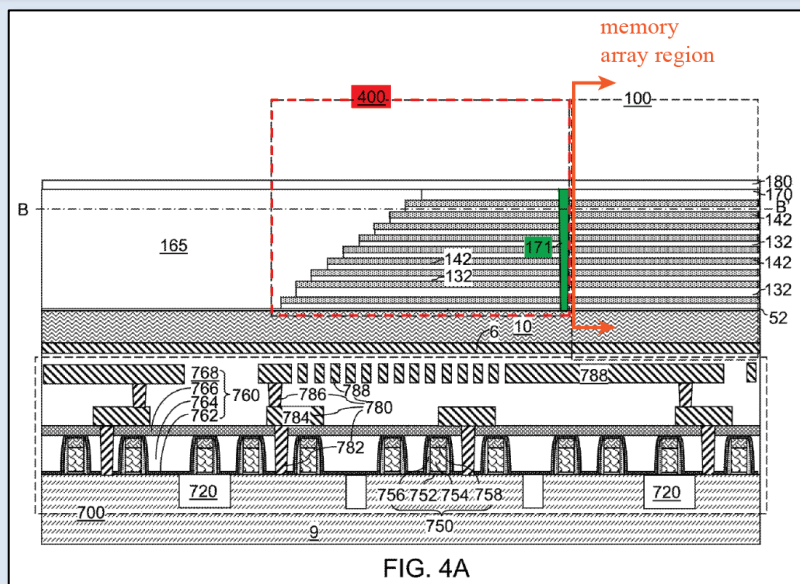
Petitioner argues: "A POSITA would have found it desirable to form 'dummy memory stack structures 55D' for structural support in regions (e.g., the **left and right periphery of the 'through-memory-level via region'**) where functional 'memory stack structures are not formed at a sufficiently high density.'"

Pet-791, 53-54 (citing Toyama [0183]); Pet-911, 52-53 (same).
Lee(I)-791 ¶121; Lee(I)-911 ¶140.

- Petitioner's argument is unsupported and mischaracterizes Toyama, which is directed to regions outside **memory array region 100**:

Sur-Reply-791, 15-16; Sur-Reply-911, 16-17.

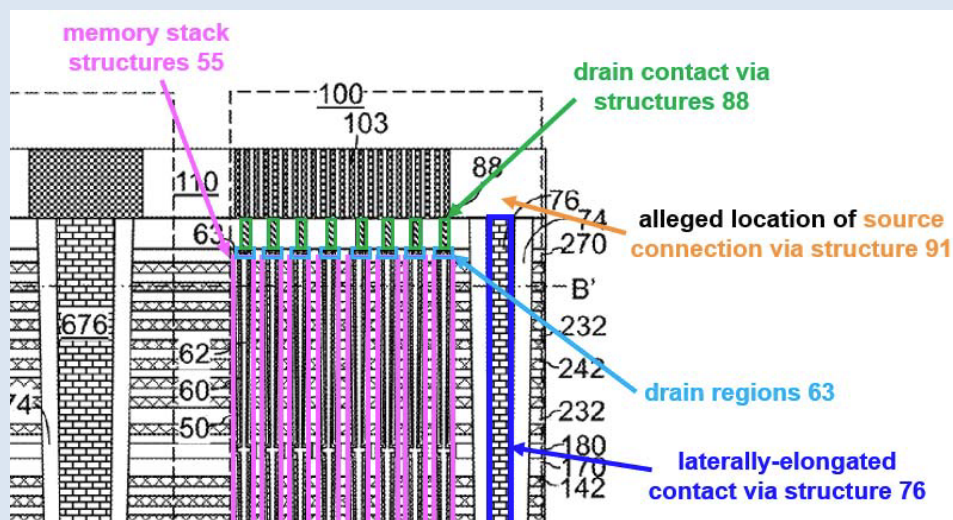
Toyama: "Referring to FIGS. 4A and 4B, first-tier support pillar structures 171 can be formed in portions of the first-tier alternating stack (132, 142) in which memory stack structures are not formed at a sufficiently high density in subsequent processing steps. For example, the **first-tier support pillar structures 171 can be formed in the through-memory-level via regions 400 and the word line contact via regions 200.**"



POR-791, 22-25; Yang-791, ¶¶59-62; Sur-Reply-791, 10-16;
POR-911, 30-33; Yang-911, ¶¶69-72; Sur-Reply-911, 11-17.

Toyama's Second Modification Fails to Disclose or Render Obvious “an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the First and Second Channel Structures” (Limitation [10.b])

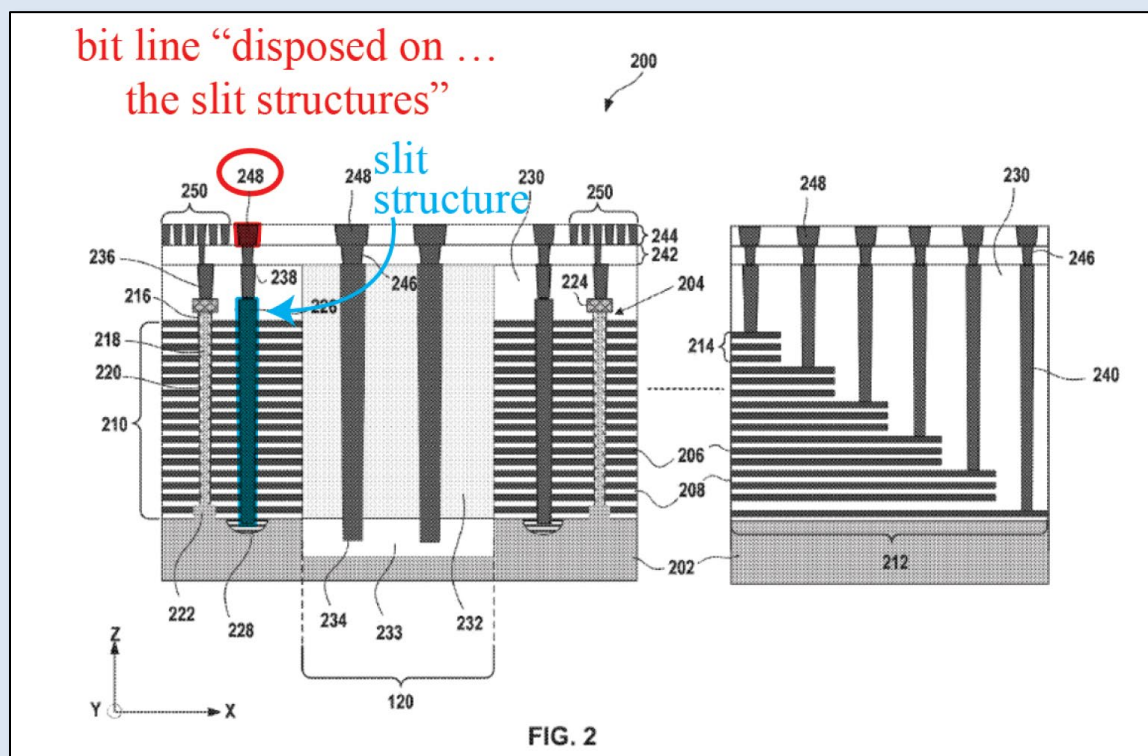
- “each local contact of the local contacts” refers to the “local contacts disposed on the first and second channel structures and the slit structures” (see Slides 10-13)
- *The Petition’s mapping does not satisfy limitation [10.b] under PO’s construction*
 - The **drain regions 63** (alleged etch stop plug) is not interposed between **source connection via structures 91** (one of the alleged local contacts) and **memory stack structures 55** (the alleged channel structures)



Toyama, Fig. 49.

Toyama's Second Modification Fails to Disclose or Render Obvious “an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the First and Second Channel Structures” (Limitation [10.b])

- '806 patent's cross-section, on the other hand, discloses the **bit line** above the **slit structure**



'806 patent: “In some embodiments, **interconnect contacts 248** in interconnect layer 244 **can include bit lines 250**....”

'806, 12:7-8.

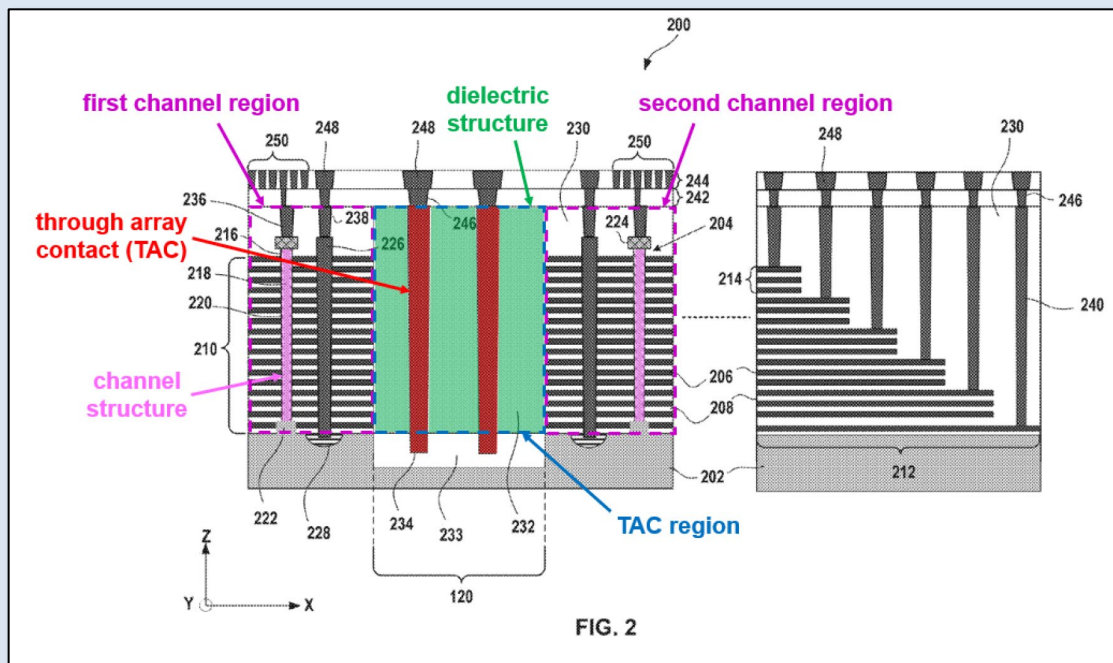
IV. GROUND 2 (TOYAMA'S FIRST EXEMPLARY STRUCTURE): CLAIMS 8-12

Petitioner's Modification of Toyama's First Exemplary Structure Does Not Disclose or Render Obvious "a through array contact (TAC) region formed between the first and second channel regions" (Limitation [8.g])

- By placing the **TAC region** between two **channel regions** of the same memory device, interconnect routing may be shortened

'806 patent: "**TACs 234 can** carry electrical signals from and/or to 3D memory device 200, such as part of the power bus, with **shorten interconnect routing**."

'806, 11:8-10; Yang-791, ¶¶65.



Dr. Yang: "A person of ordinary skill in the art would have understood from the '806 disclosures that **the TAC region** of the '806 passes through an alternating conductor/dielectric stack that **hosts both the first channel region and the second channel region**. This is clearly shown in Figs. 1A-B and 2."

Yang-791, ¶¶69.

Petitioner's Modification of Toyama's First Exemplary Structure Does Not Disclose or Render Obvious "a through array contact (TAC) region formed between the first and second channel regions" (Limitation [8.g])

- In contrast, Toyama's First Exemplary Structure positions a **channel region** on only one side of the alleged **TAC region**:

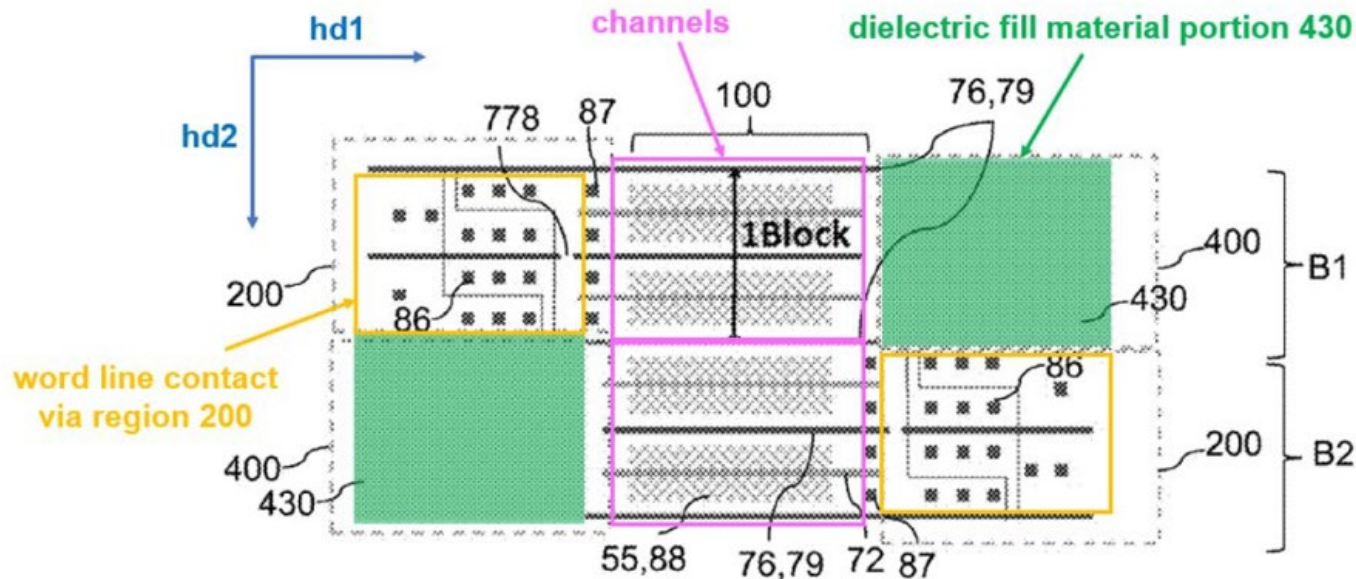


FIG. 17E

Petitioner's Modification of Toyama's First Exemplary Structure Does Not Disclose or Render Obvious "a through array contact (TAC) region formed between the first and second channel regions" (Limitation [8.g])

- In contrast, Toyama's First Exemplary Structure positions a **channel region** on only one side of the alleged **TAC region**:

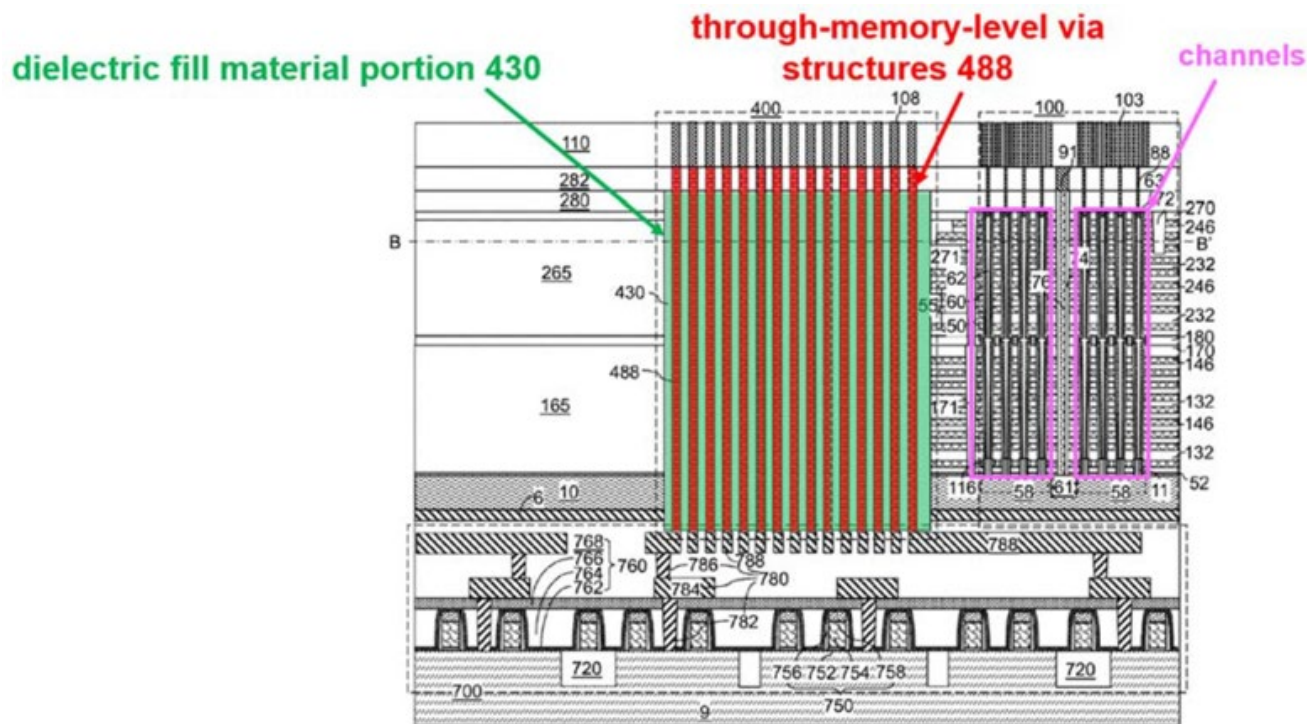


FIG. 17A

Petitioner's Modification of Toyama's First Exemplary Structure Does Not Disclose or Render Obvious "a through array contact (TAC) region formed between the first and second channel regions" (Limitation [8.g])

- Duplicating memory devices next to each does not cure the deficiency of Toyama's memory device
- It is undisputed that Petitioner's proposed modification adds a second, independent memory device

Cf. POR-791, 25-26, 28-29; Reply-791, 14-17.

Dr. Yang: "Petitioner's proposed modification does not result in the claimed 'memory device' comprising 'a through array contact (TAC) region formed between the first and second channel regions' because, by **introducing a distinct 'plane'** for the second channel region, **Petitioner is** instead **adding a second memory device** with a second channel region."

Yang-791, ¶¶68; Yang-911, ¶¶85.

Dr. Yang: "**The configuration** that Petitioner has **proposed results in two separate NAND planes that function independently** and have two distinct conductor/dielectric stacks that are not physically or directly electrically connected."

Yang-791, ¶¶69; Yang-911, ¶¶86.

Petitioner's Modification of Toyama's First Exemplary Structure Does Not Disclose or Render Obvious "a through array contact (TAC) region formed between the first and second channel regions" (Limitation [8.g])

Petitioner argues: "PO has not shown that 'a' here must be limited to the singular. As has been discussed at length in this Reply, **the word 'a' means 'one or more'** absent a clear intent to the contrary."

Reply-791, 17; Reply-911, 16.

- But the real issue here is whether at least one of the memory devices of the proposed modification can individually meet all claimed limitations, not whether several memory devices of the proposed modification may collectively meet all claimed limitations
- Petitioner failed to show that at least one of the memory devices satisfies all the requisite limitations

Federal Circuit: "Even if an infringing system can use 'one or more computers,' the plain language of the claims requires at least one of those computers to perform all the functions listed in the claims of the ARB Patent."

Finjan LLC v. SonicWall, Inc., 84 F.4th 963, 974-75 (Fed. Cir. 2023).

Federal Circuit: "Here, it does not suffice to have multiple microprocessors, each able to perform just one of the recited functions; the claim language requires at least one microprocessor capable of performing each of the recited function."

Salazar v. AT&T Mobility LLC, 64 F.4th 1311, 1317 (Fed. Cir. 2023).

Petitioner's Modification of Toyama's First Exemplary Structure Does Not Disclose or Render Obvious "a through array contact (TAC) region formed between the first and second channel regions" (Limitation [8.g])

- Toyama suggests repeating the structure of 17E in the **hd2** direction only because it would not alter the basic configuration of device
- Repeating in the **hd1** direction, as proposed, conflicts with the placement of other circuitry

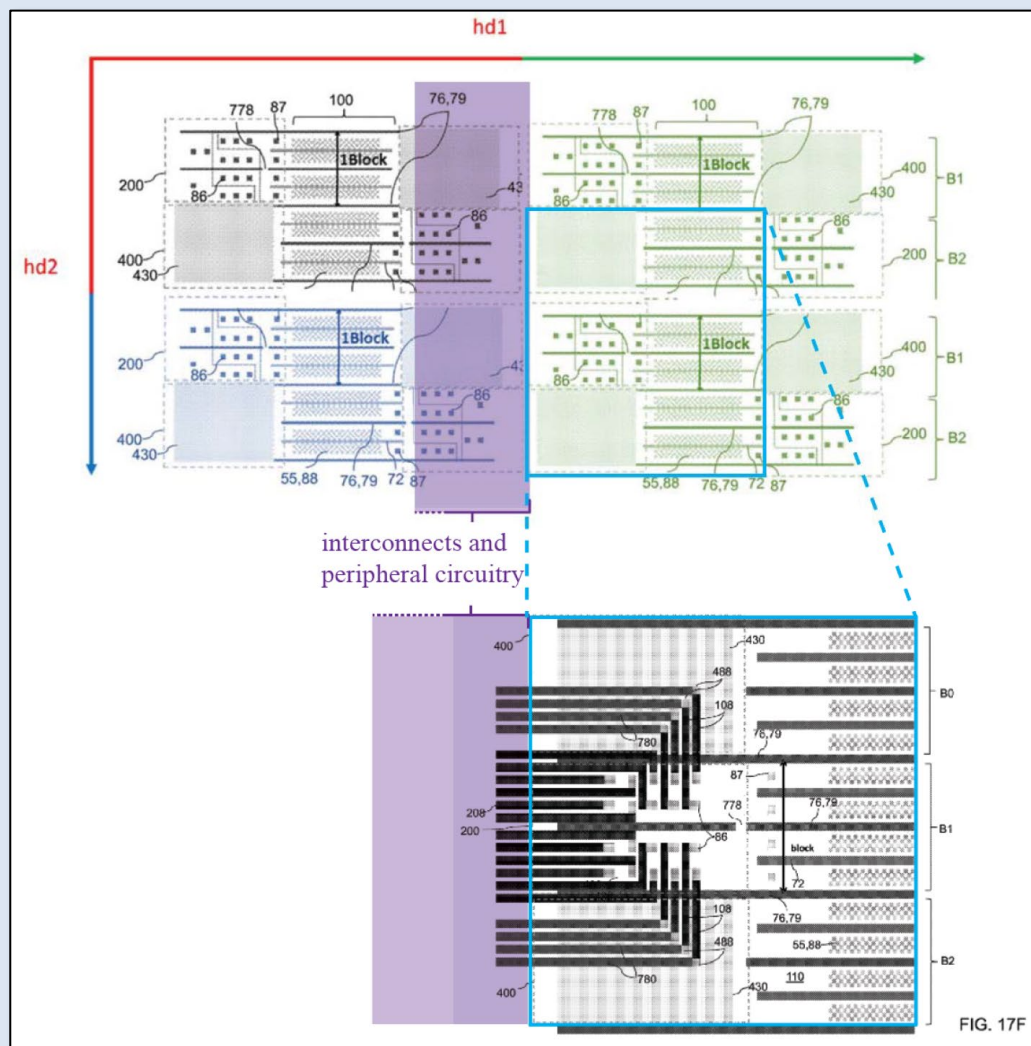


FIG. 17F

Petitioner's Modification of Toyama's First Exemplary Structure Does Not Disclose or Render Obvious "a through array contact (TAC) region formed between the first and second channel regions" (Limitation [8.g])

- A POSITA would not have considered Petitioner's proposed modification

Dr. Yang: "It is unsurprising that the layout of Figure 17E is not repeatable in the hd1 direction—***Toyama is designed to instead repeat in the hd2 direction, with interconnects and peripheral circuitry on either side in the hd1 direction.***"

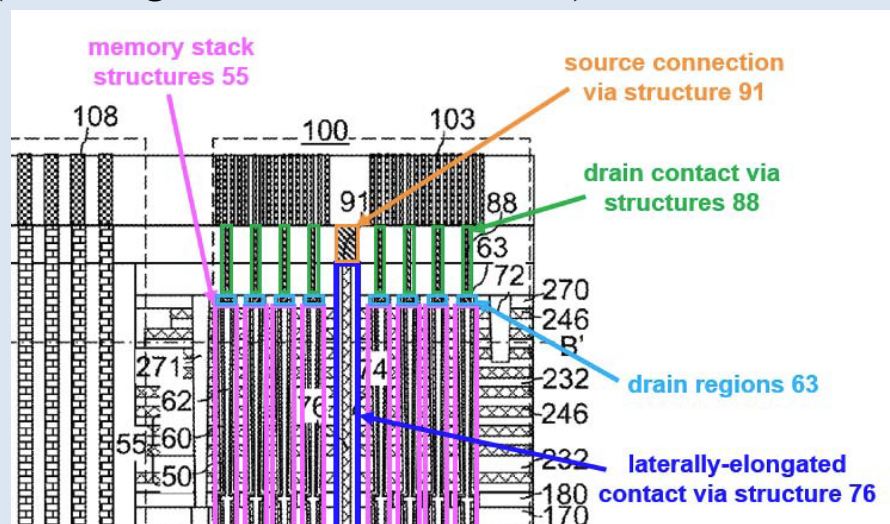
Yang-791, ¶63.

Dr. Yang: "[T]he combination eliminates the peripheral circuitry and interconnects entirely, which are ***necessary for the device to operate***. Even if Petitioner and Dr. Lee try to propose an alternative arrangement that does not eliminate the interconnects and peripheral circuitry, the particular arrangement would introduce other complications that ***Petitioner and Dr. Lee have not even attempted to address***, such as ***routing congestion and complications, resistance-capacitance delays, impacts on performance, power consumption, heat dissipation, device size***, among many other issues."

Yang-791, ¶79.

Petitioner's Modification of Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the First and Second Channel Structures" (Limitation [10.b])

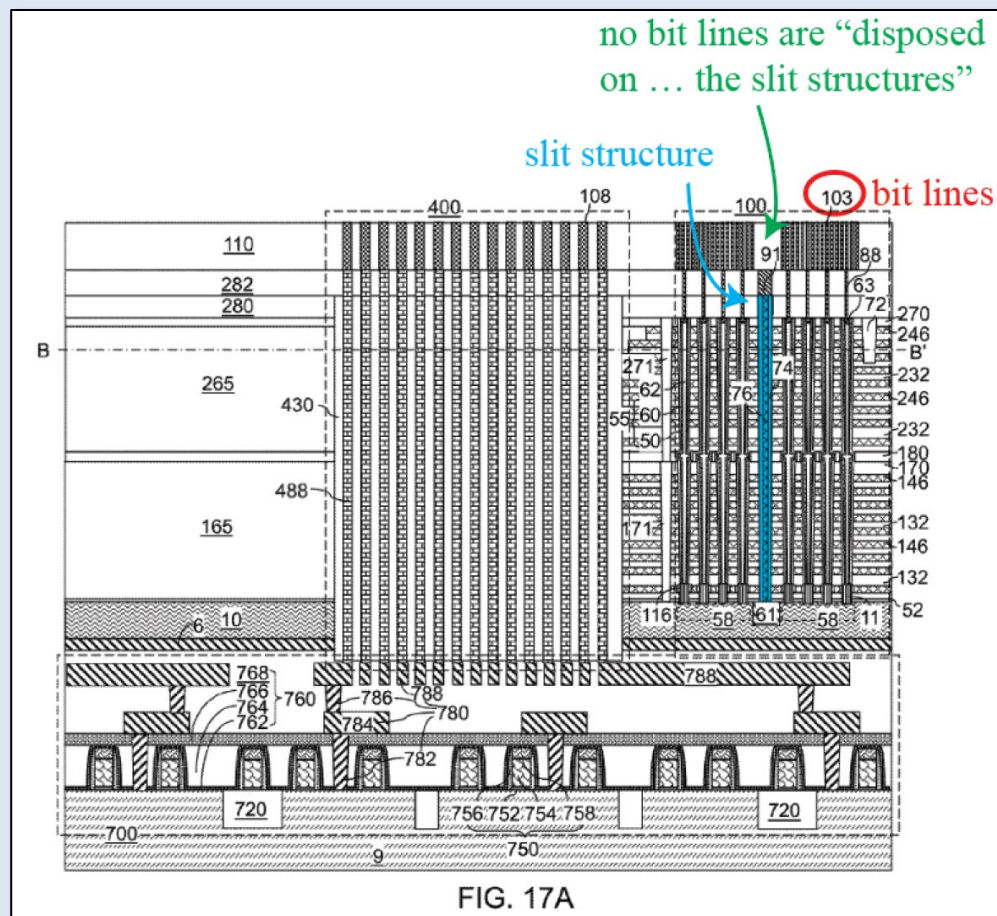
- "each local contact of the local contacts" refers to the "local contacts disposed on the first and second channel structures and the slit structures" (see Slides 10-13)
- *The Petition's mapping does not satisfy limitation [10.b] under PO's construction*
- The **drain regions 63** (alleged etch stop plug) is not interposed between **source connection via structures 91** (one of the alleged local contacts) and **memory stack structures 55** (the alleged channel structures)



Toyama, Fig. 17.

Petitioner's Modification of Toyama's First Exemplary Structure Fails to Disclose or Render Obvious "an Etch Stop Plug Interposed Between Each Local Contact of the Local Contacts and Each Channel Structure of the First and Second Channel Structures" (Limitation [10.b])

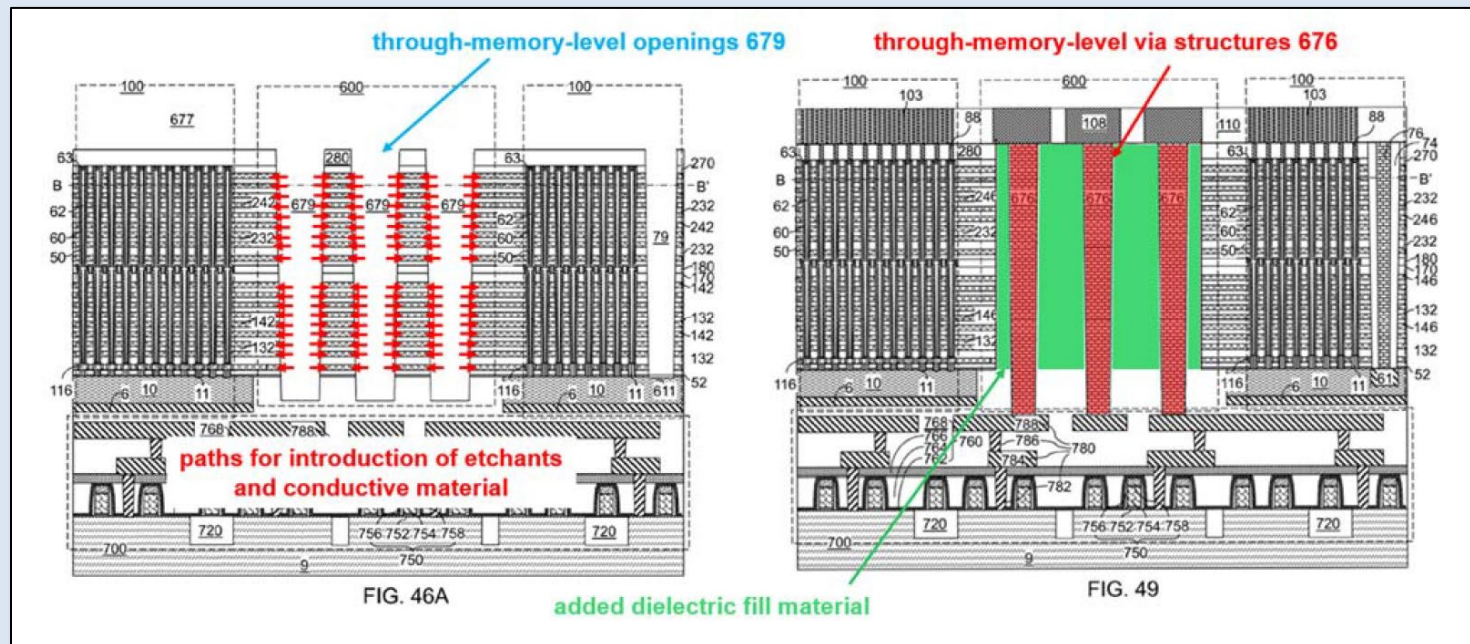
- Petitioner's new mapping on reply is deficient
- Toyama's cross-section shows that there is no **bit line** above the **slit structure**
- Petitioner makes no obviousness argument, nor provides any motivation to run bit lines over slit structures



V. GROUND 3 (COMBINATION OF TOYAMA'S SECOND MODIFICATION AND FIRST EXEMPLARY STRUCTURE): CLAIMS 8-12

No Motivation to Combine Toyama's Second Modification and First Exemplary Structure

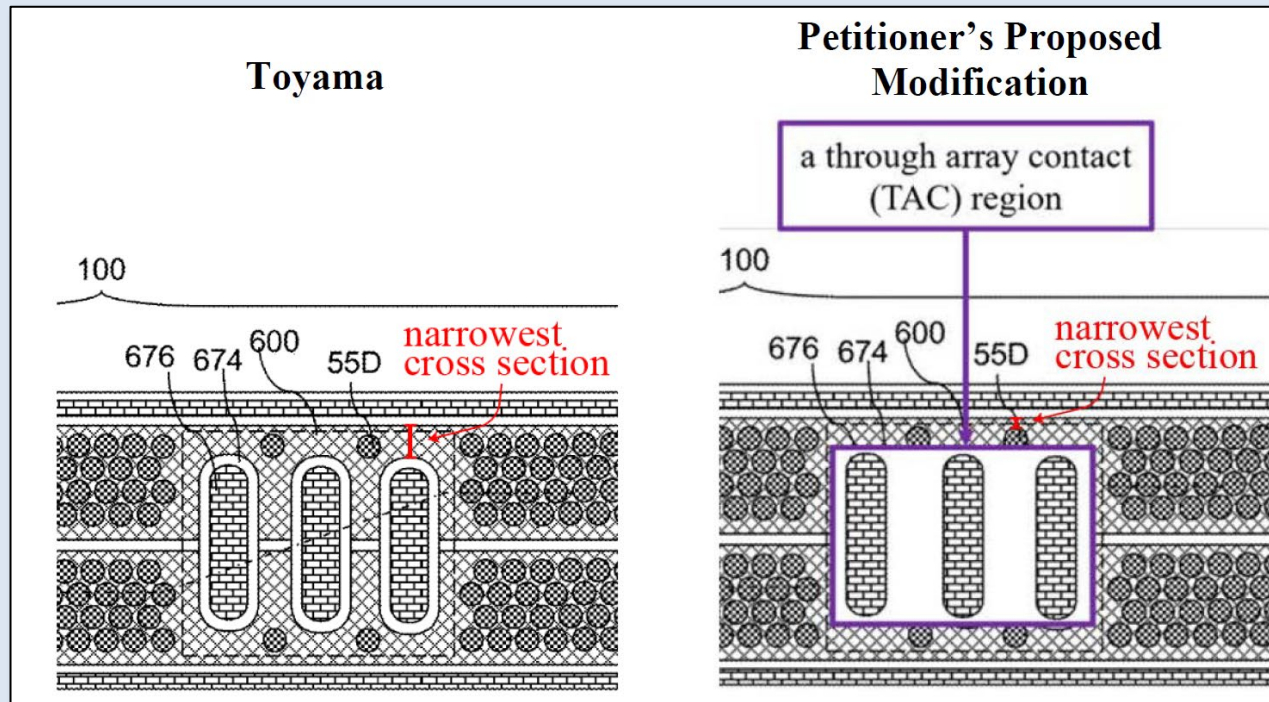
- Proposed modification eliminates sources for gate replacement etchant and conductive materials



Ex. 1005, Fig. 46A (annotated by Patent Owner), Fig. 49 (modified by Petitioner at Pet. 99 and annotated by Patent Owner)

No Motivation to Combine Toyama's Second Modification and First Exemplary Structure

- Petitioner's modification would block current and render device inoperable



Dr. Yang: “**Petitioner’s proposed modification** ... would eliminate current flow through these areas of the word lines that Petitioner proposed converting into dielectric fill material, thereby **causing current to flow through a much narrower region**. A person of ordinary skill in the art would have understood that, at minimum, this modification **would introduce reliability and manufacturing issues**, and therefore the device would not operate as intended.”

Yang-791, ¶84.

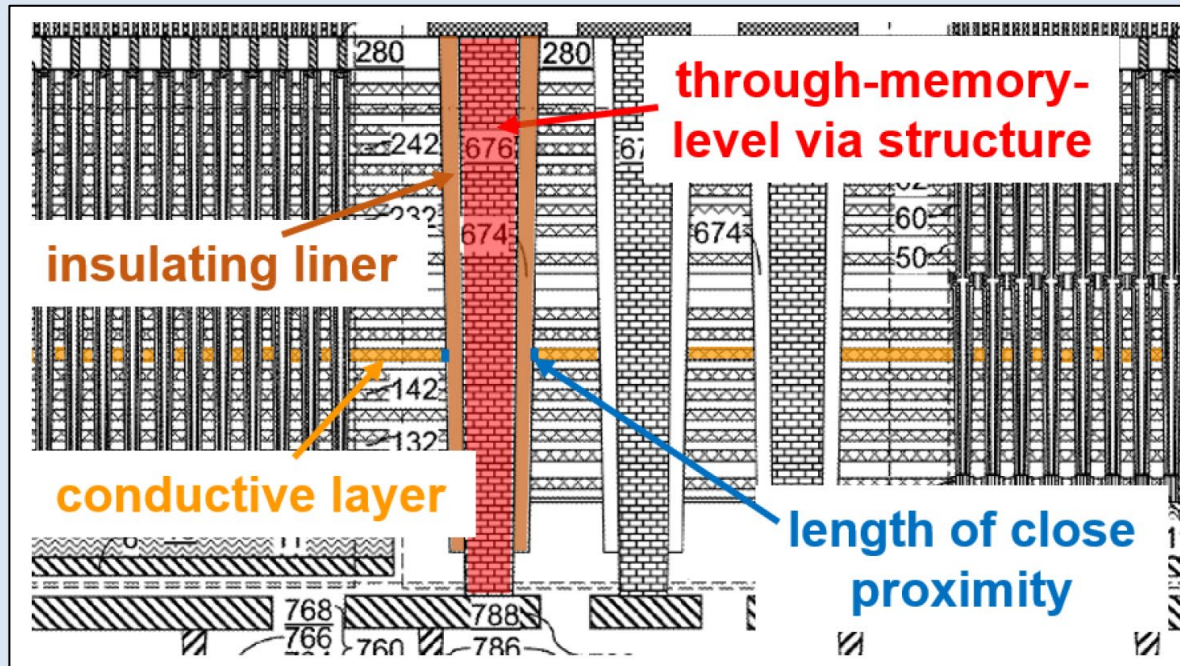
Dr. Lee admits: “**Local hot spot** means that the temperature become hot locally. Okay? And -- and, therefore, when you have local hot spot, that can **degrade your device reliability**....”

See 1/30/25 Lee Tr., 36:16-37:1, 32:9-10.

POR-791, 42-46; Yang-791, ¶¶85-91; Sur-Reply-791, 26-30;
 POR-911, 63-67; Yang-911, ¶¶109-115; Sur-Reply-911, 26-29.

No Motivation to Combine Toyama's Second Modification and First Exemplary Structure

- Petitioner's modification would not meaningfully reduce capacitive coupling



Toyama, Fig. 49 (excerpted and annotated PO).

Dr. Lee admits: “when you talk about **capacitive coupling between two conductor[s]**, you can think of it ... as **proportional to the overlap area**.”

See 1/30/25 Lee Tr., 27:2-6; Sur-Reply-791, 32.

No Motivation to Combine Toyama's Second Modification and First Exemplary Structure

- Testimony by Petitioner's own expert belies their motivation to use a dielectric structure instead of thin dielectric liners:

Dr. Lee admits: “Dr. Yang, however, overlooks that **forming a large unitary dielectric block typically involves depositing significantly more dielectric material than conformal liners** and may require longer overall processing time — including deposition and planarization — compared to liner-based approaches. Dr. Yang also ignores the benefit of **thin liners, which occupy less space and preserve more of the gate layers, offering advantages in** layout density and **electrical performance**.”

Lee(II)-791, ¶15.

Dr. Lee admits: “Q. ... [H]ow does a liner have advantages in [] electrical performance over [a] dielectric structure? ... THE WITNESS: I explained earlier that the -- **this liner** base **would provide** electrical – **better electrical characteristics, including lower parasitic capacitance**, more uniform gate control, **and better channel coupling**.”

Lee 06/13/25 Tr. at 100:17-101:6; See also *id.* at 97:15-100:13.

Petitioner's New Arguments in the Reply Are Unavailing

Petitioner argues: “*Toyama itself discloses embodiments that place unitary dielectric structures in a memory region.*”

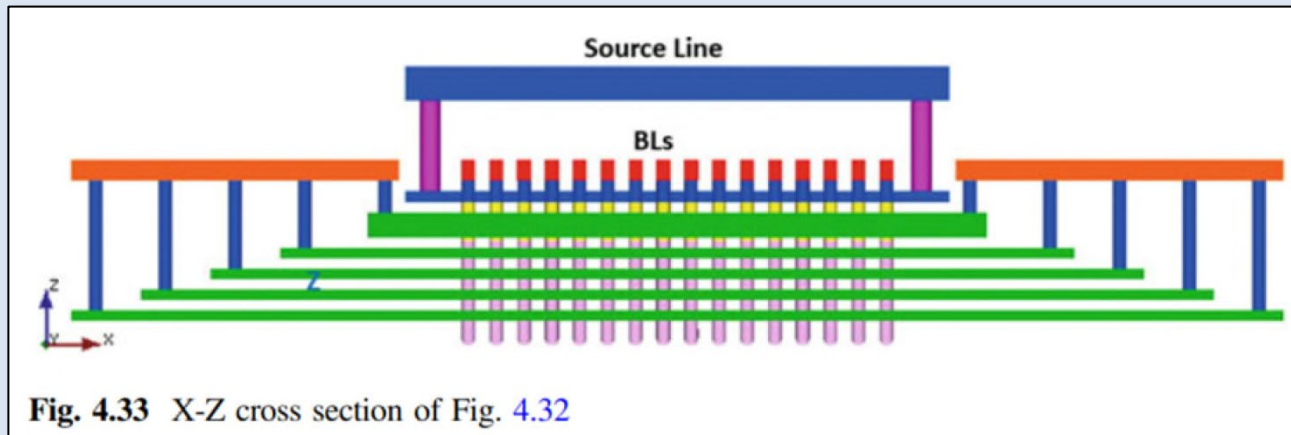
Reply-791, 24 (citing Toyama Figs. 39B and 69B).

- These two embodiments were not mentioned, much less relied upon, in the trial grounds
- The new embodiments have entirely different configurations from the trial grounds—neither of which use dummy structures 55D, which Petitioner relies upon to satisfy other limitations

Petitioner's New Arguments in the Reply Are Unavailing

Petitioner argues: “[A] POSITA would have known to *use vias* (vertical interconnects) *to convey an electrical signal to each side of the dielectric structure*.”

Reply-791, 24-25 (citing Ex. 1013, Fig. 4.33).

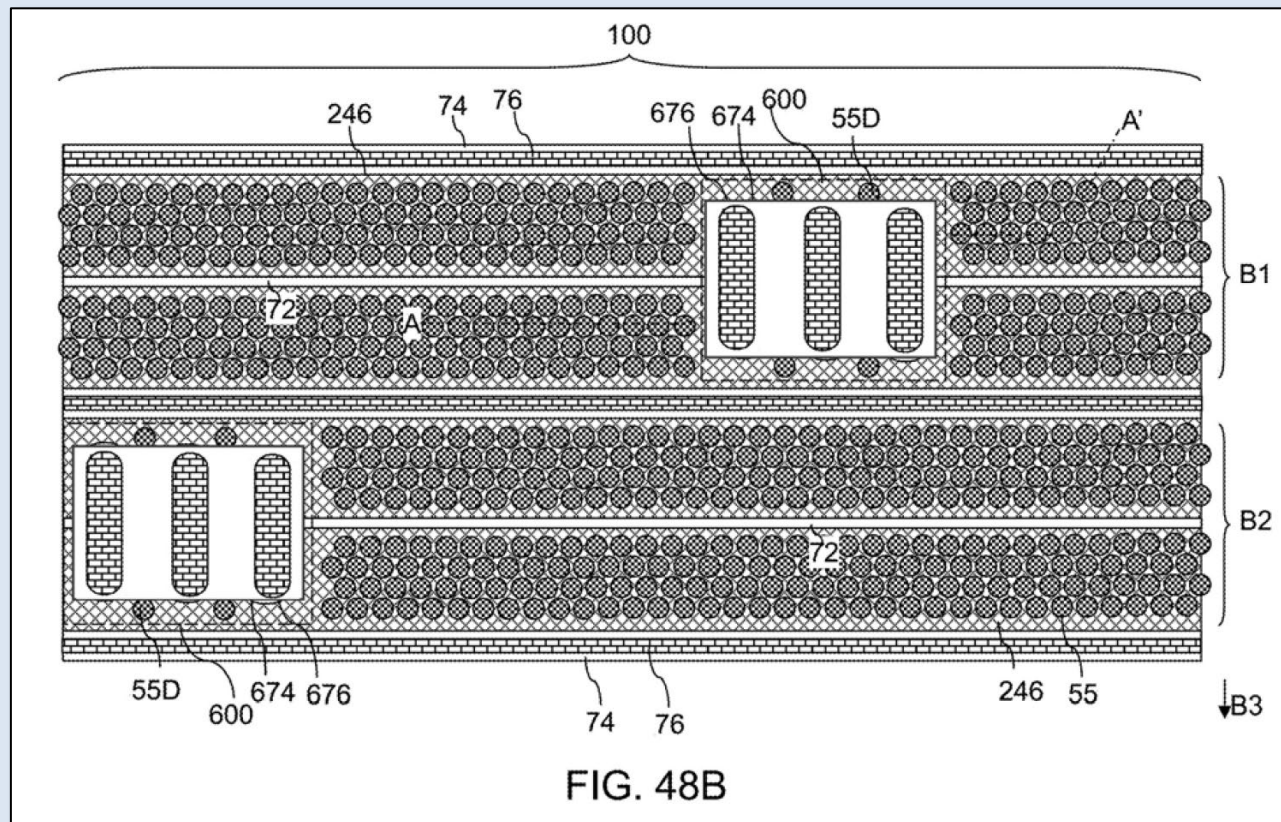


-00791 Ex. 1013, 120.

- Adding second staircase for vias is a new modification
- Requires increases the device size or reducing memory capacity
- Limits each memory block to a single through-memory-level via region—eliminating interconnect capabilities
- Fails to consider impact of second staircase on peripheral devices, interconnects, and power consumption

Petitioner's Obviousness Combination Does Not Disclose or Render Obvious “a plurality of non-electrically functional channel structures surrounding the TAC region” (Limitation [8.h])

- Petitioner's modification does cure failure to meet the “surrounding” limitation (*see* Slides 18-21)



Pet-791, 99 (modifying Toyama Fig. 48B); Pet-911, 120.

**Petitioner's Obviousness Combination Does Not Disclose or Render Obvious
"an Etch Stop Plug Interposed Between Each Local Contact of the Local
Contacts and Each Channel Structure of the First and Second Channel
Structures" (Limitation [10.b])**

- Petitioner's modification does not cure Toyama's failure to meet the "etch stop plug" limitation as the ground relies on Toyama's Second Modification alone for this limitation (*see* Slides 22-24)

Pet-911, 125.