

Micron Technology, Inc.
Petitioner
v.
Yangtze Memory Technologies Company, Ltd.
Patent Owner

IPR2024-00791 & IPR2024-00911
U.S. Patent No. 10,937,806

Micron's Hearing Demonstratives

September 4, 2025

Hearing Roadmap

1. Overview
2. Ground 2: A Multi-Plane Implementation Of Toyama's First Exemplary Structure
3. Ground 3: A Combination Of Toyama's First Exemplary Structure And Its Second Modification
4. Ground 1: Toyama's Second Modification

Hearing Roadmap

1. Overview
 - The 806-1 and 806-2 IPRs
 - Grounds
 - Overlap with the 378 IPRs
 - The '806 Patent
2. Ground 2: A Multi-Plane Implementation Of Toyama's First Exemplary Structure
3. Ground 3: A Combination Of Toyama's First Exemplary Structure And Its Second Modification
4. Ground 1: Toyama's Second Modification

Overview > The 806-1 and 806-2 IPRs

Summary

IPR	Challenged Claims	Grounds		
		1	2	3
IPR2024-00791 (806-1 IPR)	8-9 and 11-12	✓	✓	✓
IPR2024-00911 (806-2 IPR)	10	✓	✓	✓

Overview > The 806-1 and 806-2 IPRs

Grounds

- Ground 1: Claims 8-12 are obvious in view of Toyama's second modification to its fourth exemplary structure ("Second Modification") and the knowledge of a POSITA.
 - PO contests limitations [8.G.iii] (TACs extending vertically through the dielectric structure), [8.H] (non-electrically functional channel structures surrounding the TAC region), and [10.B] (etch stop plug).
- Ground 2: Claims 8-12 are obvious in view of Toyama's first exemplary structure and the knowledge of a POSITA.
 - PO contests limitations [8.PRE] (a device) and [10.B] (etch stop plug), and contends that the proposed modification results in an inoperable device.
- Ground 3: Claims 8-12 are obvious in view of Toyama's first exemplary structure, Toyama's Second Modification, and the knowledge of a POSITA.
 - PO contests limitation [8.H] (non-electrically functional channel structures surrounding the TAC region) and [10.B] (etch stop plug), and contends that a POSITA would lack motivation to combine Toyama's embodiments.

Overview > The 806-1 and 806-2 IPRs Overlap With The 378 IPRs

- Two issues overlap between the 806 IPRs and the 378 IPRs:
 - The “TACs extending vertically through the dielectric structure” limitation (limitation [8.G.iii], Ground 1).
 - The “etch stop plug” limitation (limitation [10.B], all Grounds).

Overview > The 806-1 and 806-2 IPRs

Purported Invention

- The '806 patent purports to invent a three-dimensional NAND memory device, e.g., as shown in Figure 1A:

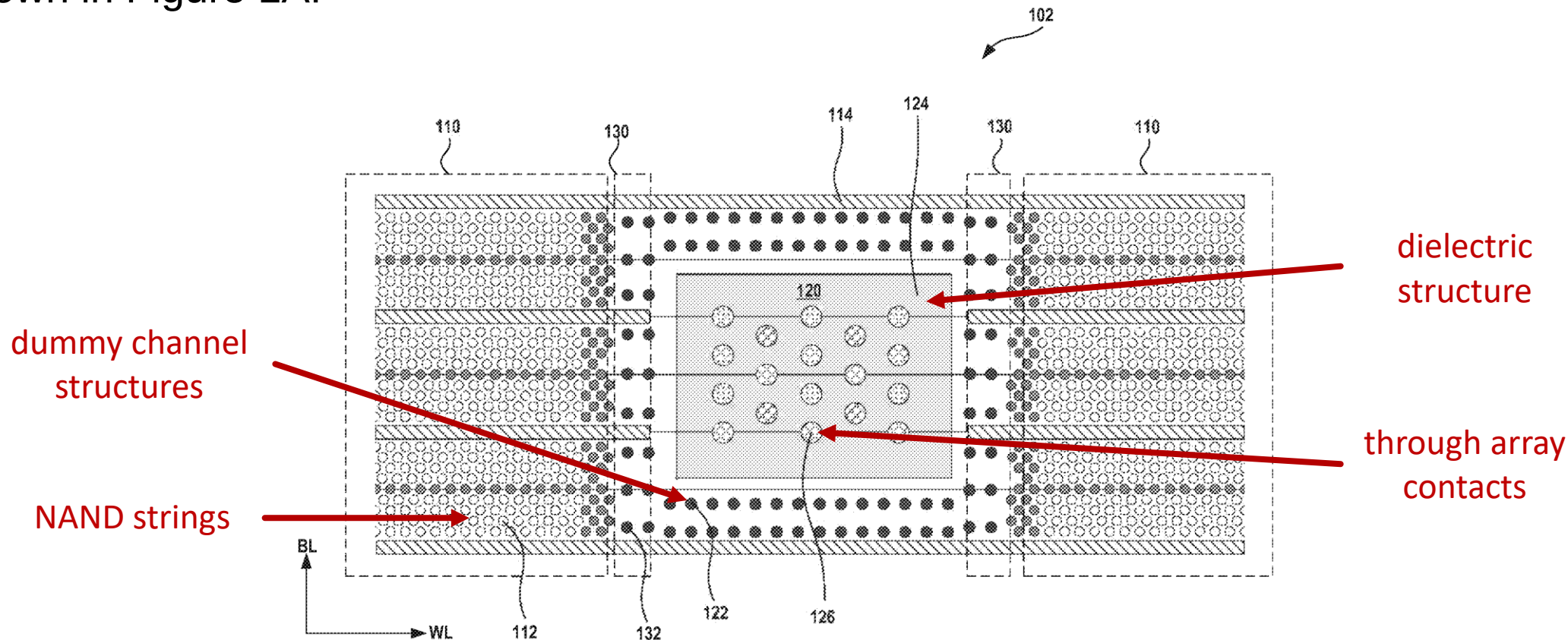


FIG. 1A

'806 patent, Figure 1A; 806-1 Petition at 15-25;
806-2 Petition at 15-25.

Micron Ex. 1053, Micron v. YMTC
IPR2024-00791, -00911

Hearing Roadmap

1. Overview
2. Ground 2: A Multi-Plane Implementation Of Toyama's First Exemplary Structure
 - Reasonable Expectation Of Success
 - [8.PRE]: "A ... Device"
 - [10.B]: "Etch Stop Plug" Limitation
3. Ground 3: A Combination Of Toyama's First Exemplary Structure And Its Second Modification
4. Ground 1: Toyama's Second Modification

Ground 2 > Reasonable Expectation Of Success > The Petitions' Showing The Ground 2 Obviousness Theory

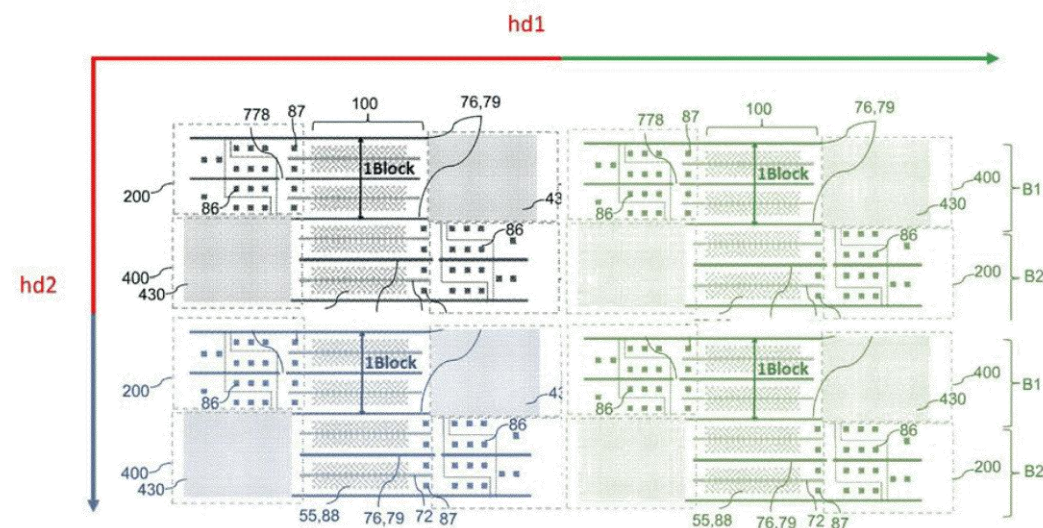
- The Petitions demonstrated that a POSITA would have found it obvious to implement multiple planes of Toyama's first exemplary structure, and that the resulting device would render all Challenged Claims obvious.

806-1 Petition at 69-77; 806-1 Lee ¶ 140;
806-2 Petition at 74-82; 806-2 Lee ¶¶ 172-178.

Toyama, Figure 17E (modified); 806-1 Petition at 69;
806-2 Petition at 74.

- a. A POSITA would have found it obvious to implement multiple planes of Toyama's first exemplary structure in the hd1 direction.

A POSITA would have found it obvious to implement Toyama's first exemplary structure in a 3D memory device with multiple *planes*. Thus, a POSITA would have found it obvious to repeat the layout shown in Fig. 17E in the hd1 *and* hd2 directions, as shown in the modified figure below:



Toyama, Fig. 17E (modified).

Ground 2 > Reasonable Expectation Of Success > The Petitions' Showing Reasonable Expectation of Success

- Further supported by Dr. Lee’s testimony and prior art publications, the Petitions demonstrated that “a POSITA would have known how to implement a flash memory device with multiple planes by placing the planes beside each other.”

806-1 Petition at 69-75 (citing figures on right);
806-2 Petition at 74-75 (same).

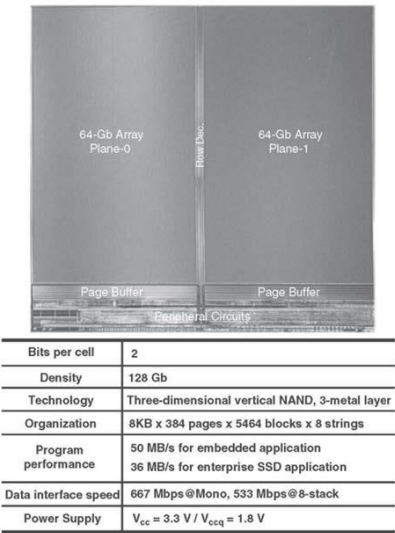


FIGURE 7.35 Die micrograph and main feature of 128-Gb 2-bit/cell 3D V-NAND flash. Die size is 133 mm².

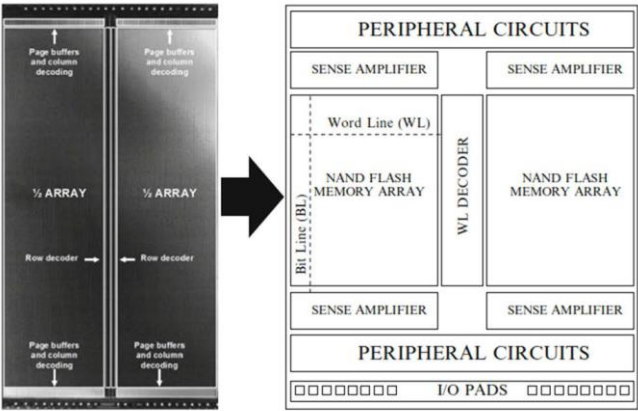


Fig. 6.1 A typical NAND Flash floorplan [1]

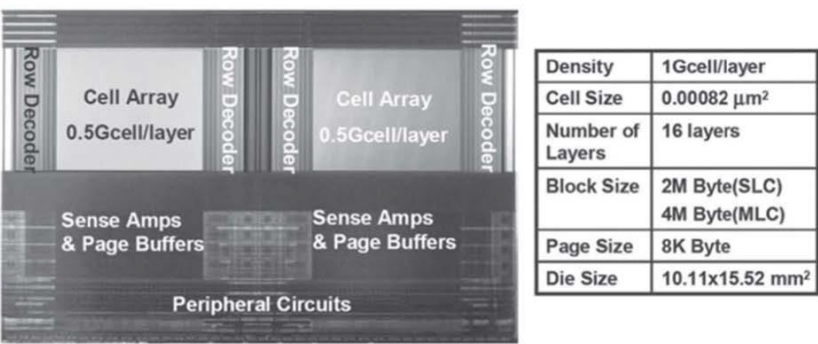
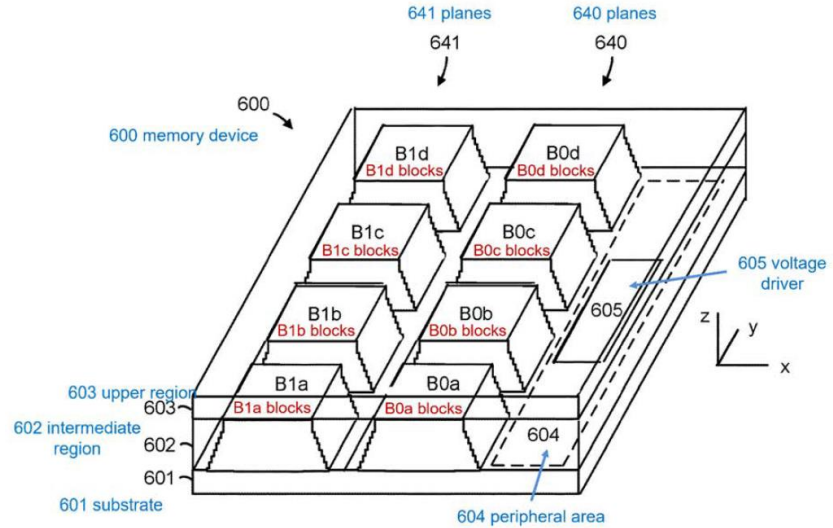


FIGURE 7.26 Image of 16-Gb pipe-shaped BiCS test chip.

Ex. 1014 at 313-314, 308.



Ex. 1023 at 144.

Ex. 1024, 13:37-44.
Micron Ex. 1053, Micron v. YMTC
IPR2024-00791, -00911 10

Ground 2 > Reasonable Expectation Of Success > The Petitions' Showing Motivation to Combine

- Supported by Dr. Lee's detailed testimony and prior art textbooks, the Petition explained that a POSITA would have been motivated to implement multiple planes of Toyama's first exemplary structure due to the well-known performance and reliability benefits of doing so.
- PO does not dispute these recognized advantages of a multi-plane device.

By the priority date, a POSITA understood numerous benefits of a multi-plane flash memory device. Lee ¶¶ 144-146. A POSITA would have known, for example, that “[o]n multi-plane device, it is possible to issue a read command on multiple planes simultaneously,” as illustrated below (see “double-plane page read”):

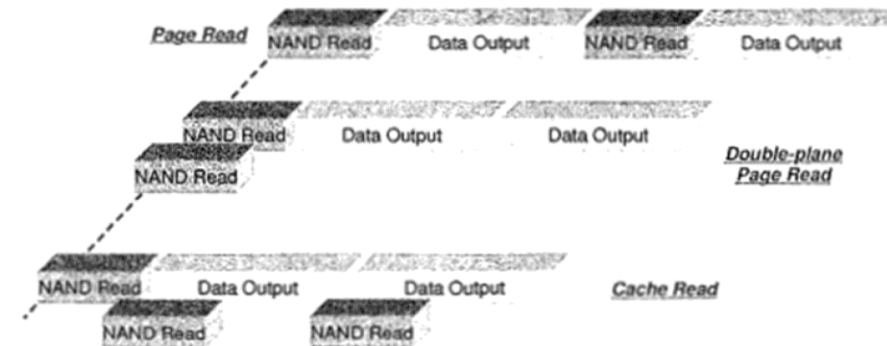


Fig. 2.19. Performance comparison among Read, Double-plane Read and Cache Read

Ex. 1025, 42.

806-1 Petition at 74; 806-1 Lee ¶¶ 144-149;
806-1 Lee-Reply ¶ 47; 806-2 Petition at 75;
806-2 Lee ¶¶ 141-147; 806-2 Lee-Reply ¶ 59.

The ID Preliminarily Rejected The Same Inoperability Argument That PO Now Makes

- PO asserts that implementing multiple planes of Toyama’s first exemplary structure would not leave room for necessary “peripheral circuitry,” rendering the proposed combination inoperable.

806-1 POPR at 32-33, 36-38; 806-2 POPR at 45-46.

- The Institution Decision preliminarily rejected that inoperability argument, finding that “NAND devices having multiple planes [had] existed for many years”:

Petitioner also provides sufficient argument and evidence that a POSITA would have had a reasonable expectation of success in implementing multiple planes of Toyama’s First Exemplary Structure in the hd1 direction because NAND devices having multiple planes existed for many years before the priority date of the ’806 patent and that implementation of such a structure would have been straightforward as it merely applies a known technique (implementing multiple planes of NAND flash memory array) to a known device (Toyama’s first exemplary structure) to yield predictable results (a NAND flash device with improved performance). Pet. 69–77 (citing, *inter alia*, Ex. 1003 ¶¶ 148–151); *see also*

806-1 ID at 29 (citing 806-1 Petition at 69-77); 806-2 ID at 29-30.

PO Ignores That The Petition's Theory Is Not Limited To Figure 17F

- PO's inoperability argument is based on Figure 17F, which according to PO requires peripheral circuitry extending past the sides of the TAC regions.

806-1 POR at 30; 806-2 POR at 46.

- PO's reliance on Figure 17F for its inoperability argument misses the mark because Petitioner's theory is not limited to—indeed, does not even mention—that figure.

806-1 Petition at 69-77; 806-2 Petition at 74-80.

- PO's argument that Figure 17F must be used with Figure 17E is meritless:

- Toyama's description of Figure 17F notes that the layout it depicts is not mandatory.

806-1 Petition at 17 (citing Toyama, [0251]);

806-2 Petition at 87 (same).

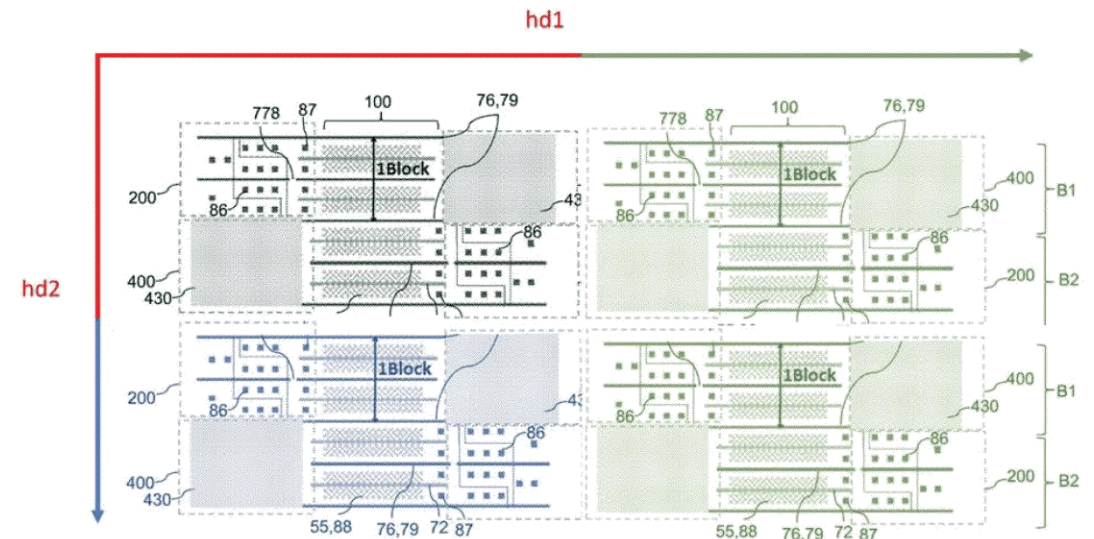
- Regardless, the Petition merely uses Figure 17E as an "exemplary configuration."

806-1 Lee ¶ 140; 806-2 Lee ¶ 171.

- a. **A POSITA would have found it obvious to implement multiple planes of Toyama's first exemplary structure in the hd1 direction.**

806-1 Petition at 69; see also 806-2 Petition at 74.

140. It would have been obvious to a POSITA to repeat Toyama's first exemplary structure to implement multiple memory *planes* in a 3D memory device, resulting in the exemplary configuration below.



Ex. 1005, Fig. 17E (modified).

806-1 Lee, ¶140; see also 806-2 Lee ¶ 171.

Micron Ex. 1053, Micron v. YMTC

IPR2024-00791, -00911 13

PO Ignores That Toyama Expressly Contemplates Modifications to Its Embodiments

- PO's reliance on Figure 17F also misses the mark because Toyama's first exemplary structure is not limited to that figure.
 - Toyama describes Figure 17F as “an **alternative exemplary structure** according to the first embodiment of the present disclosure.”

Toyama, [0049]; 806-1 Reply at 17 (quoting same); 806-2 Reply at 17 (same).
 - Moreover, Toyama contemplates that its expressly disclosed structures may be modified, reinforcing Dr. Lee's testimony that a POSITA could and would make the proposed modification:

[0390] Although the foregoing refers to particular embodiments, it will be understood that the disclosure is not so limited. It will occur to those of ordinary skill in the art that various modifications may be made to the disclosed embodiments and that such modifications are intended to be within the scope of the disclosure. Where an embodiment employ-

Toyama, [0390]; 806-1 Lee-Reply ¶ 59 (citing same); 806-2 Lee-Reply ¶ 71.

Ground 2 > Reasonable Expectation Of Success

PO Does Not Rebut That Implementing Peripheral Circuitry Was Highly Routine In The Art

- Even if the peripheral circuitry arrangement in Figure 17F were a required part of Toyama's first exemplary structure (it is not), PO does not rebut Petitioner's evidence that a POSITA would have been able to rearrange the peripheral circuitry to enable a multi-plane implementation.
 - PO has not rebutted the numerous prior art devices implementing peripheral circuitry, including in side-by-side multi-plane configurations just like the proposed modification.

806-1 Petition at 69-77; 806-1 Lee ¶¶ 140-151; 806-1 Reply at 17-19.

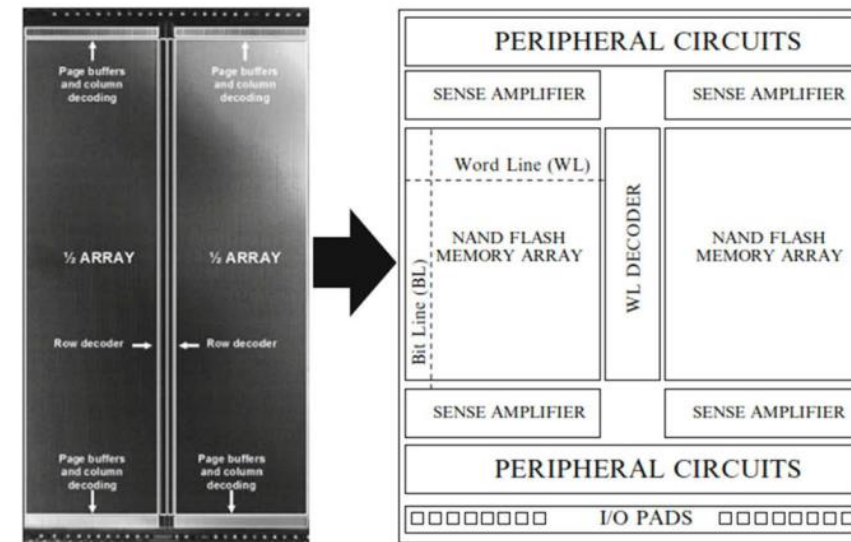
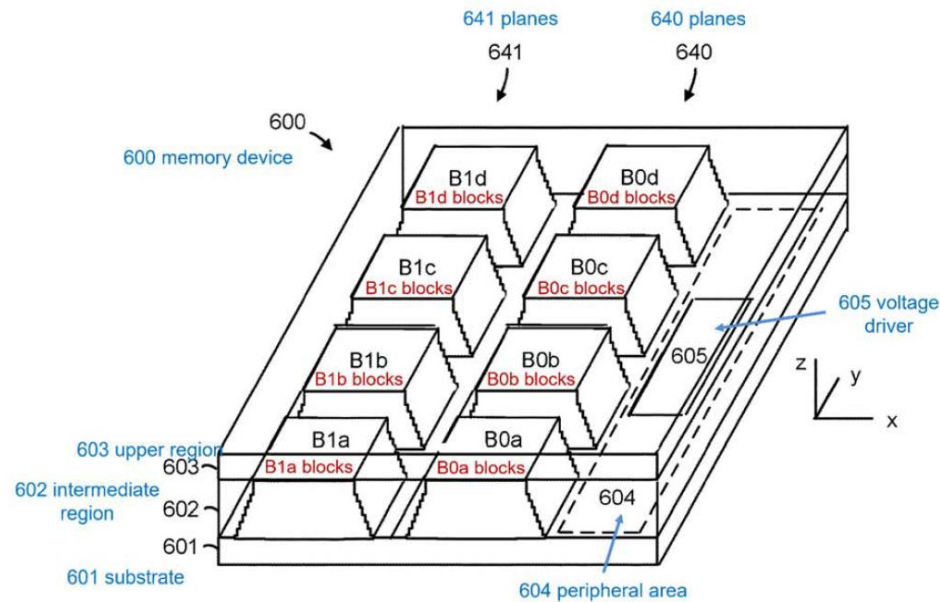


Fig. 6.1 A typical NAND Flash floorplan [1]

Ex. 1024, Figure 5 (annotated); 806-1 Petition at 71 (citing same);
806-2 Petition at 76 (same).

Ex. 1023 at 144; 806-1 Petition at 72 (citing
same); 806-2 Petition at 77 (same).

Micron Ex. 1053, Micron v. YMTC
IPR2024-00791, -00911 15

PO's Inoperability Objection Is An Improper "Bodily Incorporation" Argument

- PO does not attempt to distinguish *Elbrus*, which rejected an argument—just like PO's argument here—that the bodily incorporation of a proposed combination would lead to an "inoperable circuit":

The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference, but rather whether a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention. Therefore, Elbrus's argument that combining Sukegawa and Lu could lead to an unworkable circuit is basically irrelevant.

Elbrus Int'l Ltd. v. Samsung Elecs. Co., 738 F. App'x 694, 698-699 (Fed. Cir. 2018) (cleaned up and emphasis added); 806-1 Reply at 19 (also citing other "bodily incorporation" cases that PO does not distinguish); 806-2 Reply at 18 (same).

PO's Timeliness Objection To Petitioner's Reply Is Meritless

- PO's sur-reply asserts that Petitioner's reply positions are untimely.

806-1 Sur-reply at 22; 806-2 Sur-reply at 22.

- Petitioner's reply arguments rebut PO's attacks on the Petition's position (on the right) that a POSITA would have had a reasonable expectation of success due to the commonplace implementation of flash memory planes before the priority date.

806-1 Petition at 77; 806-2 Petition at 81-82.

A POSITA also would have had a reasonable expectation of success in implementing multiple planes of Toyama's first exemplary structure in the hdl direction. As noted above, NAND flash memory devices with multiple planes existed for many years before the priority date of the 806 Patent. Lee ¶ 150. §X.A.4.a.i. Taking the layout shown in Toyama's Fig. 17E as the blueprint for a plane, and repeating that layout for each plane, would have been straightforward for a POSITA and a POSITA could have done so with predictable results. Lee ¶ 150.

Thus, the obviousness combination is nothing more than applying a known technique (implementing multiple planes of a NAND flash memory array) to a known device (Toyama's first exemplary structure) to yield predictable results (a NAND flash device with improved performance). Lee ¶ 151.

806-1 Petition at 77; 806-2 Petition at 81-82.

Ground 2 > “A ... Device”

The “Device” Limitation

Claim Element	Claim Language	806-1 IPR	806-2 IPR
[8.PRE]	“A three-dimensional (3D) memory device comprising:”		

- Although PO frames its challenge as a deficiency in Petitioner’s mapping for limitation [8.G], PO’s challenge actually relates to the preamble language “[a] ... device.”.

806-1 POR at 25; 806-2 POR at 39.

Ground 2 > “A ... Device”

The Petition’s Showing

- Contrary to PO’s assertion, the Petition consistently described the proposed combination as a multi-plane “**device**” (singular).

806-1 Sur-reply at 17; 806-2 Sur-reply at 17.

A POSITA would have found it obvious to implement Toyama’s first exemplary structure in a 3D memory device with multiple *planes*. Thus, a POSITA

806-1 Petition at 69; 806-2 Petition at 74.

Thus, the obviousness combination is nothing more than applying a known technique (implementing multiple planes of a NAND flash memory array) to a known device (Toyama’s first exemplary structure) to yield predictable results (a NAND flash device with improved performance). Lee ¶ 151.

806-1 Petition at 77; 806-2 Petition at 82.

In Its ID, The Board Understood Petitioner’s Theory To Relate To A Single Device

- In the Institution Decision, the Board consistently and correctly understood Petitioner’s obviousness theory to relate to a single device.

regions, Petitioner provides sufficient argument with supporting evidence that a POSITA would have reason to modify Toyama First Exemplary Structure, which has a channel region (memory array region 100) on only one side of the TAC region (part of “through-memory-level via region 400”), to extend the device in the hd1 region and that such a modified device, having multiple planes, would have a TAC region formed between the first and second channel regions as required by claim element [8.G].
Pet. 66–78, 83–87.

806-1 ID at 27-28; see also id. at 28 (“Petitioner provides sufficient argument and evidence ... that a POSITA would have modified Toyama to provide a multi-plane flash memory device.”) (emphasis added); 806-2 ID at 33-34.

PO Ignores the Extrinsic Evidence Showing That a Multi-Plane Device Is Still a Device

- Although PO asserts that a multi-plane memory is multiple devices, Dr. Lee testified (supported by textbook evidence) that the ordinary meaning of “device” encompasses a NAND flash memory with two planes.

806-1 Reply at 15; 806-1 Lee-Reply ¶¶ 34-38; 806-2 Lee-Reply ¶¶ 41-53.

A NAND flash storage device or storage system, e.g., a solid-state disk (SSD) and flash cards, may be associated with multiple chips. Each chip is composed of one or more sub-chips or dies. Each sub-chip might have multiple planes. Each plane is

Ex. 1023 (Micheloni 2013 Textbook) at p. 247; 806-1 Lee-Reply ¶ 35; 806-2 Lee-Reply ¶ 46.

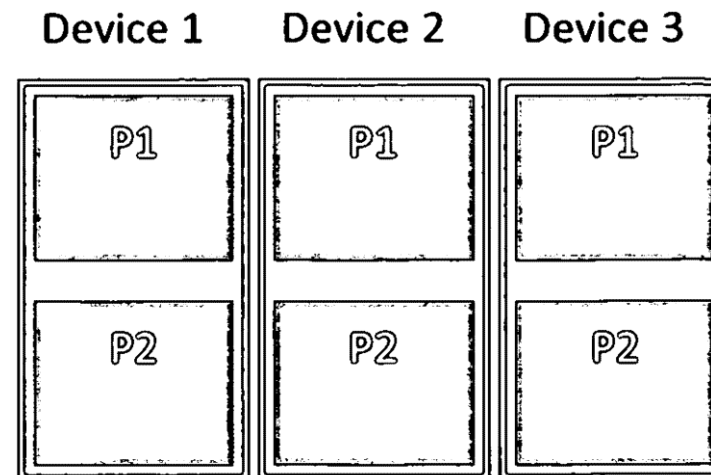
uct with the V-NAND cell was implemented [39, 40]. Figure 7.35 shows the die micrograph of the 128-Gb MLC (2-bit/cell) 3D V-NAND flash memory device as the first generation of the V-NAND cell array technology. This memory chip has 24 stacked WL layers and consists of two planes each containing 64-Gb arrays (2732 of 3-MB blocks with 8-KB pages). The shared-WL-block scheme for the row circuit

Ex. 1014 (Aritome Textbook) at p. 313; 806-1 Lee-Reply ¶ 35; 806-2 Lee-Reply ¶ 46.

Dr. Yang’s “Device” Opinion Is Contradicted by His Own Patent

- Dr. Yang’s testimony that a flash memory with multiple planes is not “a device” is unsupported by any evidence and, in fact, is contradicted by his own prior art patent, which contemplates a multi-plane NAND flash device.

[038] In the embodiment illustrated in FIG. 5, throughput may be increased by cascading devices. For example, it may be possible to increase the writing throughput up to 60 MB/s (or more) with 3 devices of SLC NAND flash (six planes with 4 kB of a page) running an internal 1 bit shift register at 1 GHz.



Ex. 1050, [038], Figure 5 (two planes per device); 806-1 Lee-Reply ¶ 37 (citing same); 806-1 Reply at 15; 806-2 Lee-Reply ¶ 49 (same); 806-2 Reply at 15.

The Specification Does Not Disavow Or Disclaim A Multi-Plane “Device”

- Dr. Lee explained, and PO has not rebutted, the specification’s definition of “3D memory device” is met by a multi-plane device.

806-1 Reply at 14; 806-2 Reply at 14.

- The specification defines “3D memory device” as “a semiconductor device with vertically-oriented strings of memory cell transistors ... on a laterally-oriented substrate so that the memory strings extend in the vertical direction with respect to the substrate.”

’806 patent, 5:30-37.

- PO does not dispute Dr. Lee’s testimony that the proposed combination includes (1) vertically-oriented strings of memory cell transistors on a laterally-oriented substrate, (2) so that the memory strings extend in the vertical direction with respect to the substrate.

806-1 Lee-Reply ¶¶ 30-33; 806-2 Lee-Reply ¶¶ 42-46.

- PO fails to identify any disclaimer that would warrant narrowing “device” to a single-plane device.

806-1 Reply at 16; 806-2 Reply at 16.

- A purported benefit of the patent, shortening interconnect routing, is not a basis for narrowing “device” to a single-plane device.

806-1 Reply at 15-16; 806-2 Reply at 15-16.

PO’s “Unreasonable Results” Are A Red Herring

- PO contends that Petitioner’s understanding of “device” leads to “unreasonable results,” such as that “a server farm, or any plane, ship, or car with 3D flash memory” would be a 3D memory device.

806-1 Sur-reply at 17, 19.

- But PO ignores Dr. Lee’s testimony explaining why a POSITA would have understood a multi-plane flash memory, in which the planes operate together, to be a single “device”:

in parallel. It would make little sense to consider the planes as separate “devices,” because there is a single flash device that executes a unified access operation by coordinating parallel activity across its planes—each plane performing a portion of that operation. The operation is initiated and completed by the device, not independently by each plane. Thus, a POSITA would not describe each plane as a

806-1 Lee-Reply ¶ 37; 806-2 Lee-Reply ¶ 49.

The Preamble Is Not Limiting

- PO has not shown any basis to depart from the principle that “a preamble is generally not limiting.”

Moreover, clear reliance on the preamble during prosecution to distinguish the claimed invention from the prior art transforms the preamble into a claim limitation because such reliance indicates use of the preamble to define, in part, the claimed invention. ... Without such reliance, however, a preamble generally is not limiting when the claim body describes a structurally complete invention such that deletion of the preamble phrase does not affect the structure or steps of the claimed invention.

Catalina Mktg. Int’l, Inc. v. Coolsavings.com, Inc., 289 F.3d 801, 809 (Fed. Cir. 2002);
806-1 Reply at 16 (citing same); 806-2 Reply at 16 (same).

Ground 2 > “Etch Stop Plug” Limitation

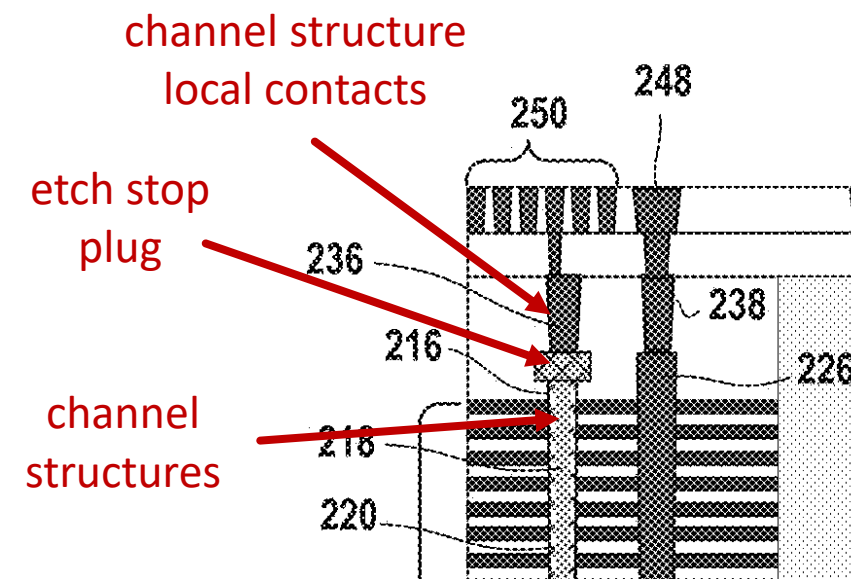
The Limitation at Issue

Claim Element	Claim Language	806-1 IPR	806-2 IPR
[10.B]	“an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures”		

Ground 2 > “Etch Stop Plug” Limitation > Claim Construction

The Parties’ Claim Construction Dispute

- The parties’ dispute centers on the meaning of “each local contact of the local contacts.”
 - Petitioner contends that the limitation requires an etch stop plug between (1) each channel structure local contact and (2) each channel structure.
806-2 Reply at 1-5.
 - PO contends that the limitation requires an etch stop plug between (1) each channel structure local contact **and** each slit structure local contact, and (2) each channel structure.
806-2 POR at 14.
- PO’s proposal, which reads out every embodiment of the specification, cannot be correct.
806-2 Reply at 2-3.



806 patent, Figure 2 (partial).

Ground 2 > “Etch Stop Plug” Limitation > Claim Construction

The Board Preliminarily Adopted Petitioner’s Construction

- In the Institution Decision, the Board addressed—and preliminarily rejected—the exact arguments that PO now advances.
 - The Board found that Petitioner’s construction is the only construction that makes logical sense:

at 24:13–20. At this stage of the proceeding, Petitioner persuasively explains that the only way for an etch stop plug to be interposed between a local contact and a channel structure is if the local contact is located on the channel structure, i.e., the local contact is a channel structure local contact. *See, e.g.,* Pet. Reply 4–5. Thus, we understand the plain and ordinary

*806-2 ID at 12-13;
806-2 Reply at 1-2.*

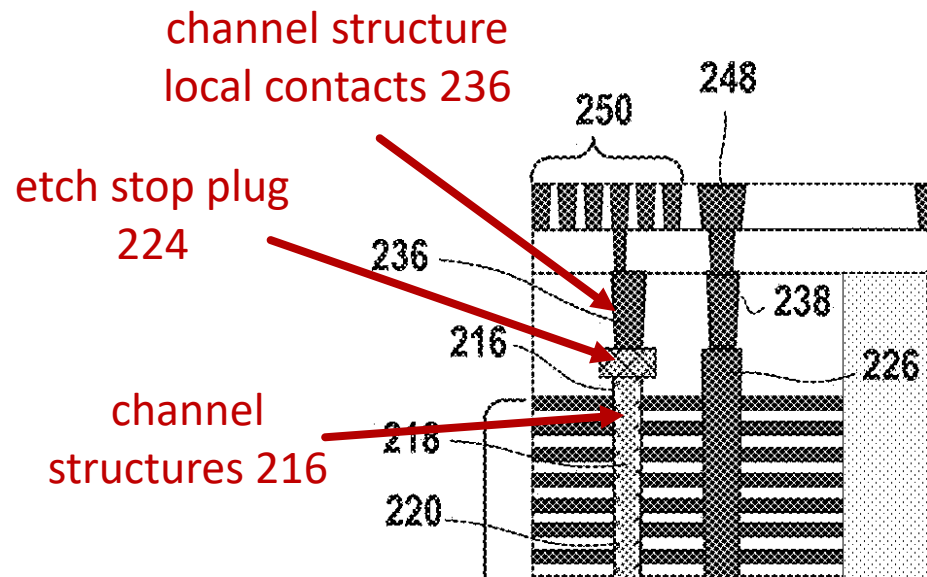
- The Board noted that during prosecution the Examiner did not adopt the construction that PO now urges:

Thus, the Examiner did not consider the claim to require an etch stop plug disposed between a *slit structure local contact* and a channel structure.

*806-2 ID at 12-13;
806-2 Reply at 1-2.*

- PO fails to rebut the Board’s reasoning.

The '806 Patent Exclusively Describes Etch Stop Plugs Between the Channel Structure Local Contacts and Channel Structures



'806 patent, Figure 2 (partial).

- The '806 patent describes “NAND string contacts” (236) as the “local contacts” for the “channel structures” (216), and “slit structure contacts” (238) as the “local contacts” for the “slit structures” (226).

806-2 Reply at 2-3.

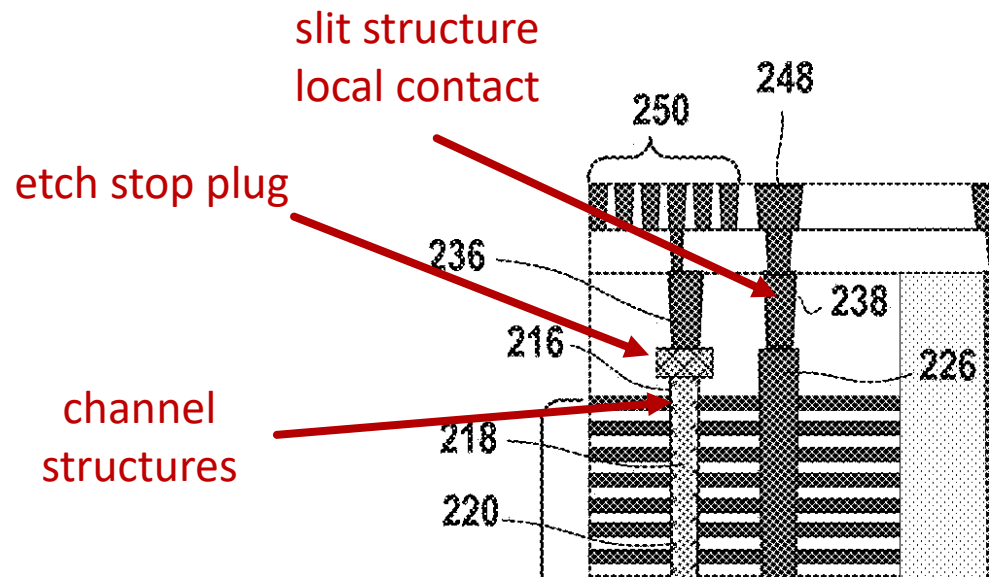
- The '806 patent exclusively describes the “etch stop plugs” (224) as being between the channel structure local contacts (236) and the channel structures (216).

806-2 Reply at 2.

- The etch stop plugs' purpose is to protect the channel structures from etching operations, which might otherwise damage the dielectric material in the channel structures.

806-2 Lee-Reply ¶¶ 10-14.

The Experts Agree That Slit Structures Do Not Have, Nor Do They Need, Etch Stop Plugs



'806 patent, Figure 2 (partial).

- The '806 patent never states or suggests that there is an etch stop plug between a slit structure local contact (238) and a channel structure (216).

806-2 Reply at 2-3.

- Both parties' experts agree that slit structures do not need etch stop plugs because the slit structures are made of a conductive material that naturally stops etches.

806-2 Lee-Reply ¶ 14.

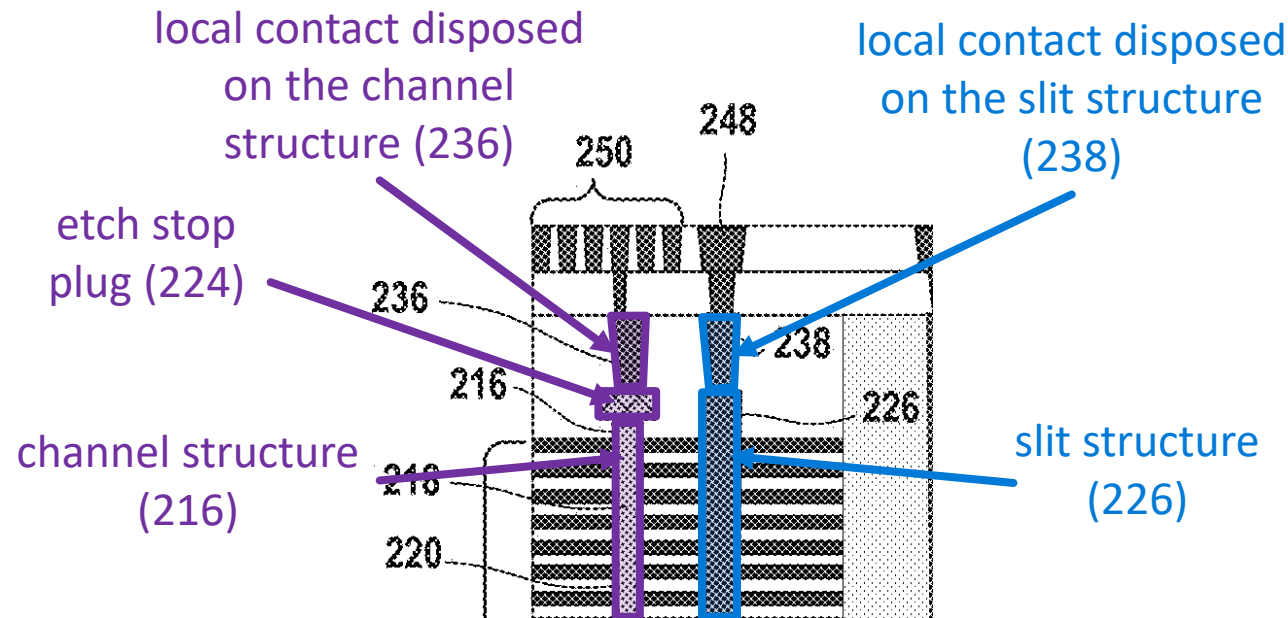
- Even if slit structures did have etch stop plugs, they wouldn't be interposed between the slit structure local contacts and the **channel** structures as allegedly claimed.

806-2 Reply at 2.

Ground 2 > “Etch Stop Plug” Limitation > Claim Construction > PO’s Construction Is Incorrect PO’s Construction Would Exclude All Disclosed Embodiments

- By requiring etch stop plugs (224) between the slit structure local contacts (238) and the channel structures (216), PO’s construction would exclude **every** disclosed embodiment.

806-2 Reply at 1-3.



'806 patent, Figure 2 (partial).

- Etch stop plug (224):
 - IS “interposed between” the channel structure local contact (238) and the channel structure (216).
 - IS **NOT** “interposed between” the slit structure local contact (238) and the channel structure (216).

PO Asserts That “Bit Lines 250” Are the Claimed “Each Local Contact of the Local Contacts”

- After Petitioner pointed out in its Preliminary Reply that PO’s construction excludes every disclosed embodiment, PO responded by asserting that the ’806 patent’s “bit lines 250” are the claimed “each local contact of the local contacts.”

806-2 POR at 18.

- PO’s reliance on “bit lines 250” fails for at least the following three reasons:
 - “Bit lines 250” are not “local contacts disposed on ... the slit structures.”
 - PO’s construction would excludes every embodiment.
 - PO’s reliance on “interconnect structures 248” as local contacts is untimely and meritless.

806-2 Reply at 1-5.

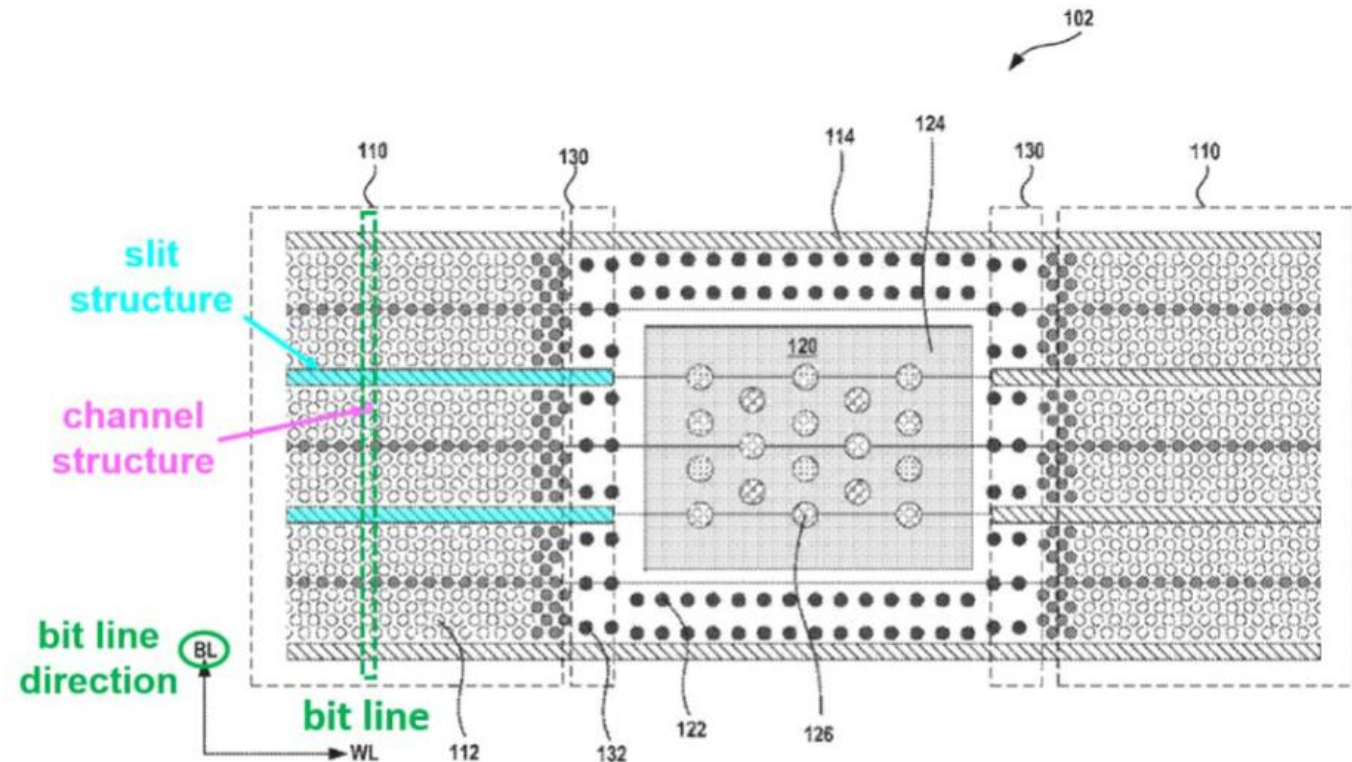


FIG. 1A

POR 32 (annotating ’806 patent, Figure 1A).

Ground 2 > “Etch Stop Plug” Limitation > Claim Construction > PO’s Construction Is Incorrect

1. “Bit Lines 250” Are Not “Local Contacts Disposed On ... The Slit Structures”

“Bit lines 250” are not “local contacts disposed on ... the slit structures” because:

1. The specification defines “local contacts” as “in direct contact with the memory array structures,” “such as ... slit structures.”

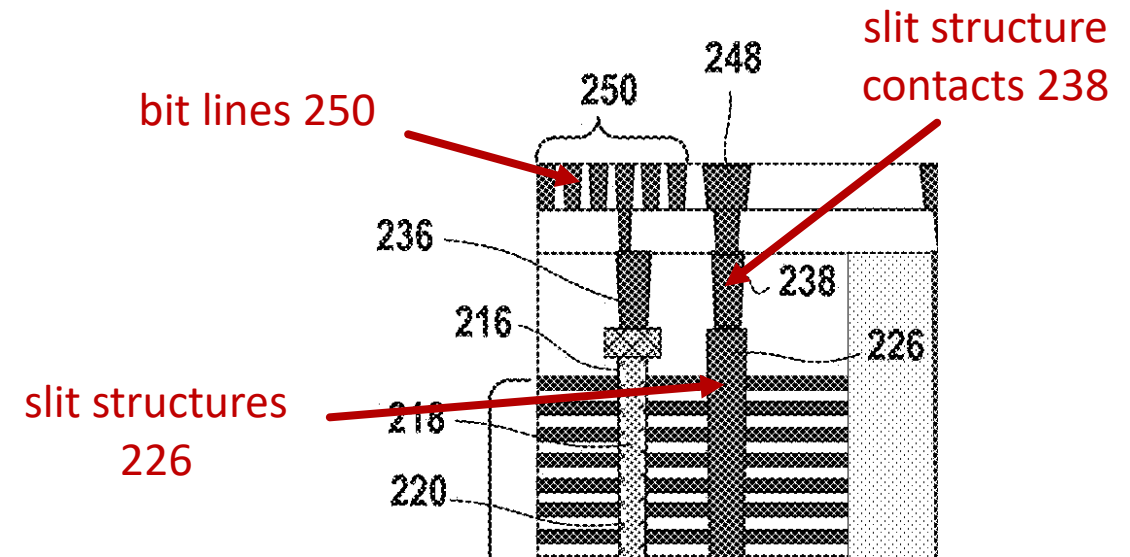
'806 patent, 11:24-28; 806-2 Lee-Reply ¶ 18.

- “Bit lines 250” are **not** in direct contact with slit structures 226.

806-2 Reply at 1-3 (citing 806-2 Lee-Reply ¶¶ 10-19).

2. The specification distinguishes between “local contacts” and “bit lines 250” (which it describes as “interconnect contacts”).

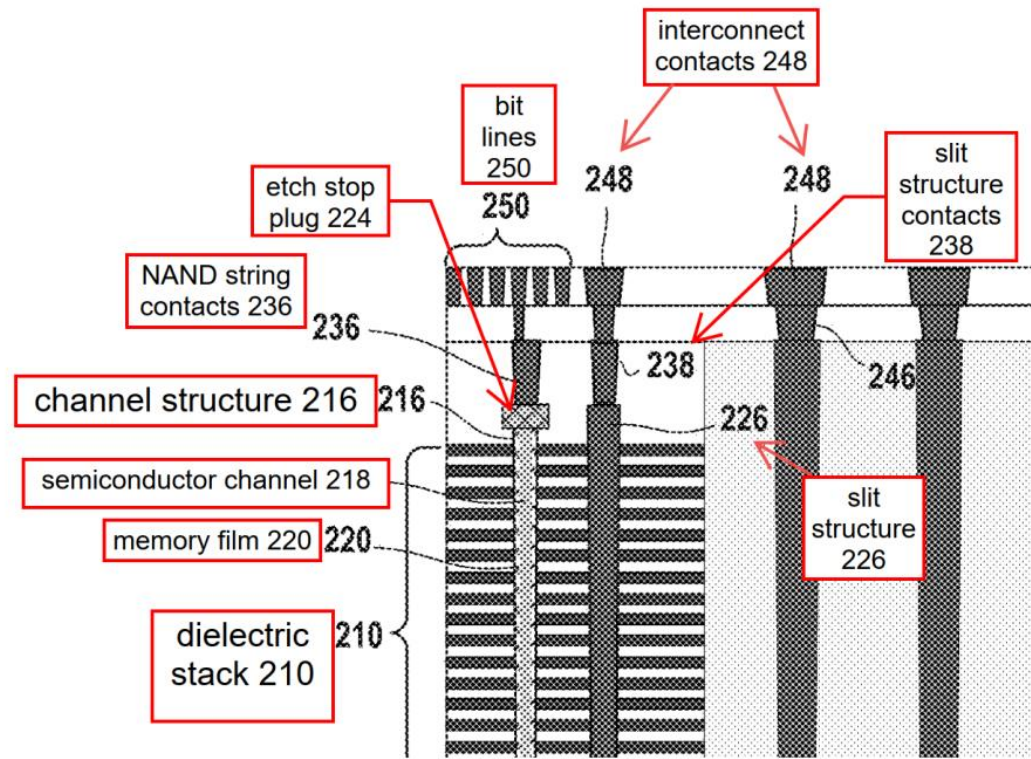
'806 patent, 5:46-48, 11:59-62, 12:7-10; 806-2 Lee-Reply ¶ 16; 806-2 Reply at 4-5.



'806 patent, Figure 2 (partial).

Ground 2 > “Etch Stop Plug” Limitation > Claim Construction > PO’s Construction Is Incorrect

2. PO’s Construction Excludes Every Embodiment



- Each of the '806 patent embodiments requires “slit structure contacts” (238) in order to provide an electrical connection to the “slit structures” (226).

806-2 Reply at 2.

- The '806 patent expressly provides that “slit structure contacts” are “local contacts.”

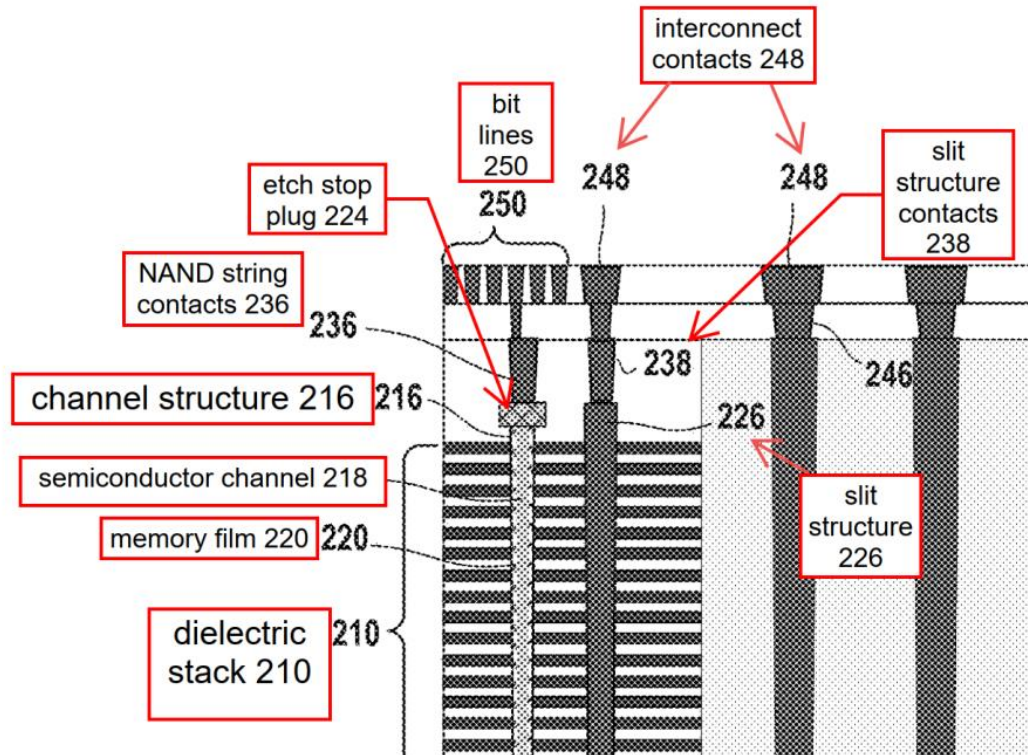
'806 patent, 11:20-24, 11:38-41; 806-2 Reply at 2.

- PO’s construction excludes every embodiment because there is no etch stop structure between the slit structure local contacts and the channel structures.

806-2 Lee-Reply ¶¶ 14, 19; 806-2 Reply at 2-3.

'378 patent, Figure 2 (cropped, annotated); 378-2 Reply at 12.

3. PO’s Reliance on “Interconnect Structures 248” Is Untimely and Meritless



- PO’s assertion that element 248 is a “local contact,” raised for the first time in its sur-reply, is improper. *806-2 Sur-reply at 35.*

- The POR relied exclusively on “bit lines 250” as the claimed “local contacts.” *806-2 POR at 19.*

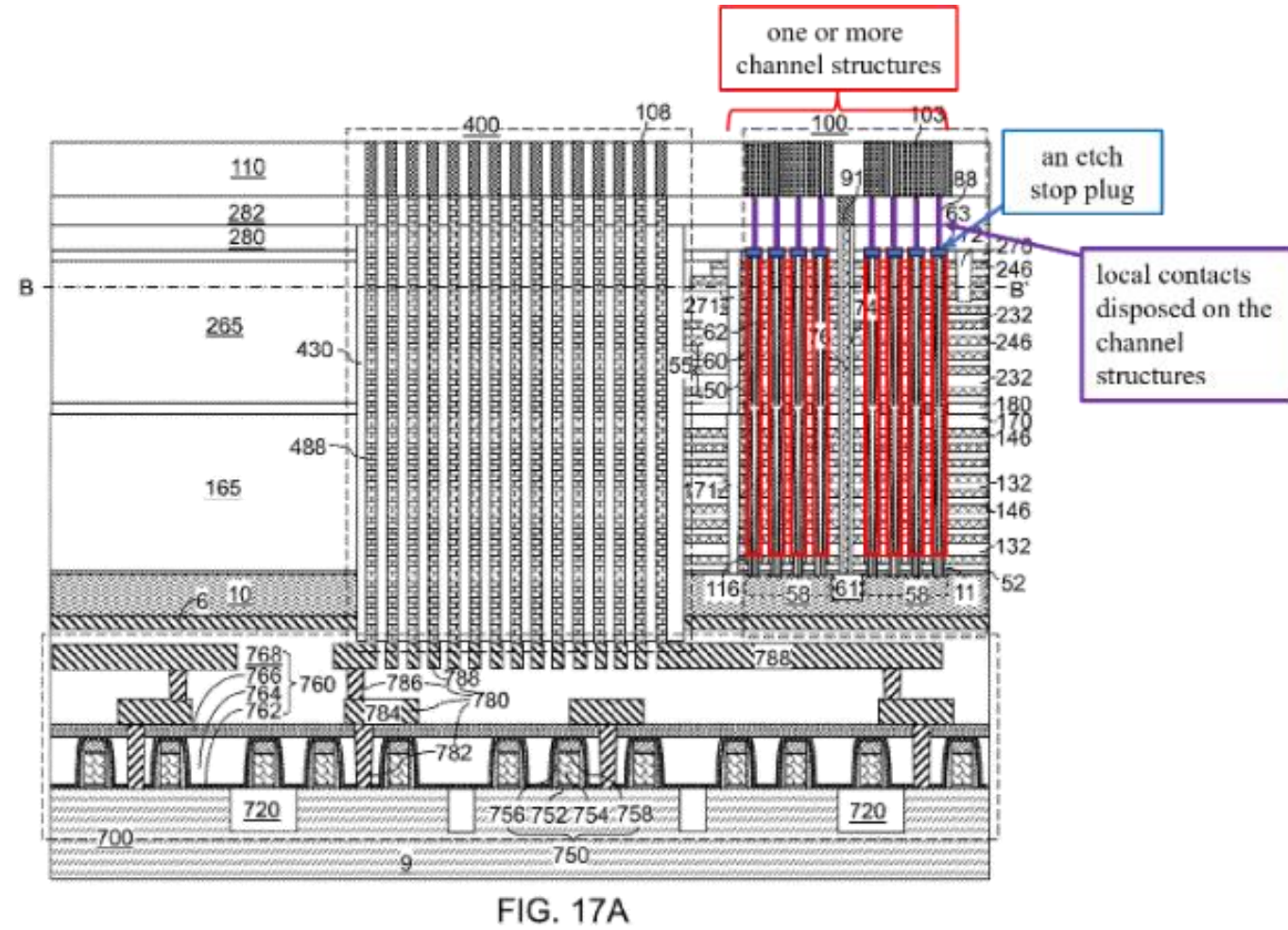
- PO’s reliance on element 248 in its sur-reply is untimely. *37 C.F.R. § 42.23(b).*

- PO asserts that there must an etch stop plug interposed between a channel structure and “**each and every**” local contact. *806-2 Sur-Reply at 6.*

’378 patent, Figure 2 (cropped, annotated); 378-2 Reply at 12.

Ground 2 > “Etch Stop Plug” Limitation > Obviousness Under Petitioner’s Construction PO Does Not Dispute That the Claims Would Have Been Obvious Under Petitioner’s Construction

- The Petition demonstrated that Ground 2’s “drain regions 63” are etch stop plugs as claimed.
806-2 Petition at 54-59, 98-99.
- The Institution Decision agreed. It held that the claim only requires etch stop plugs between channel structure local contacts and channel structures.
806-2 ID at 37-40.
- PO does not dispute that Toyama’s etch stop plugs (63) are interposed between channel structure local contacts (88) and channel structures (55).
806-2 Reply at 29.
- Thus, if the Board maintains its preliminary construction, Ground 2 renders the “etch stop plug” limitation obvious.
806-2 Reply at 29.



Toyama, Figure 17A (annotated); 806-2 Petition at 98-99.

Ground 2 > “Etch Stop Plug” Limitation > Obviousness Under PO’s Construction PO’s Attempt to Distinguish Toyama’s “Bit Lines 103” Is Misguided

- PO relies on the absence of bit lines over the slit structures in Toyama Figures 17A and 49.

806-2 Sur-reply at 35.

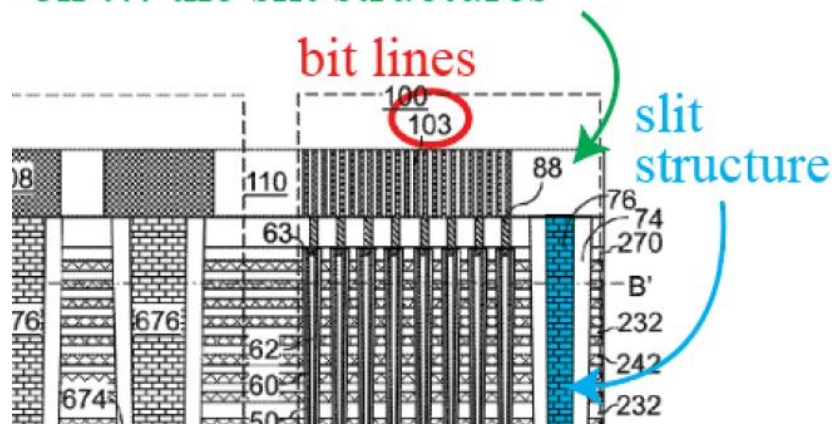
- As Dr. Lee explained, a POSITA would have understood from Toyama’s disclosure (including Figures 17B and 48B, and its text) that Toyama’s bit lines overlies its slit structures.

806-2 Lee-Reply ¶¶ 103-107.

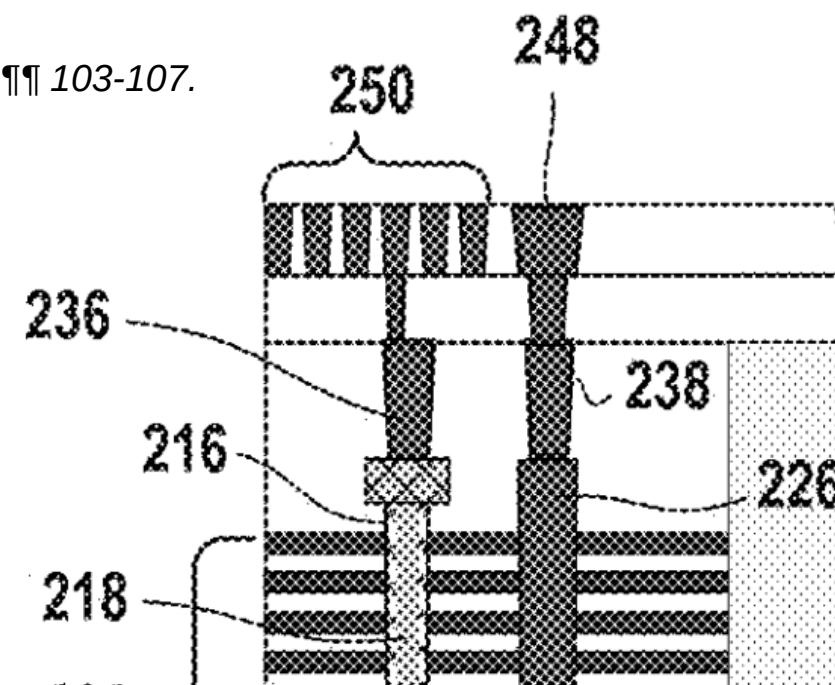
- PO’s argument is contrary to Figure 2 of the ’378 patent.

806-2 Lee-Reply ¶¶ 103-107.

no bit lines are “disposed on ... the slit structures”



806-2 Sur-reply at 35 (annotating Toyama, Figure 49).



'806 patent, Figure 2 (annotated)

Micron Ex. 1053, Micron v. YMT

IPR2024-00791, -00911 38

Ground 2 > “Etch Stop Plug” Limitation > Obviousness Under PO’s Construction

PO’s “New Mapping” Objection Is Meritless

- PO asserts that Petitioner’s mapping of the claim to Toyama’s bit lines under PO’s “etch stop plug” construction is untimely.

806-2 Sur-reply at 32.

- But, under the Federal Circuit’s decision in *Apple*, Petitioner must be permitted to respond to PO’s construction.

[W]here a patent owner in an IPR first proposes a claim construction in a patent owner response, a petitioner must be given the opportunity in its reply to argue and present evidence of anticipation or obviousness under the new construction.

Apple Inc. v. Omni MedSci, Inc., No. 2023-1034, 2024 WL 3084509, at *5 (Fed. Cir. June 21, 2024) (cited in 806-2 Reply at 29 n.6).

Ground 2 > “Etch Stop Plug” Limitation > Obviousness Under PO’s Construction

PO’s Attempts to Distinguish *Apple* Fall Flat

- PO asserts that Apple is inapposite because “PO has not proposed a new claim construction.”

806-2 Sur-reply at 32.

- But PO ***did*** propose a construction for this limitation in its POR:

A. “each local contact of the local contacts” (Claim 10)

The term “each local contact of the local contacts” of claim 10 should be construed, according to its plain and ordinary meaning, as referring to the “local contacts disposed on the first and second channel structures ***and the slit structures***” as recited in independent claim 8, from which claim 10 depends. The Board should

806-2 POR at 14 (claim construction section).

- The APA requires that Petitioner be able to respond to PO’s construction, which Petitioner could not have reasonably foreseen in its Petition.

*Apple, 2024 WL3084509 at *5 (“[U]nder the APA, the Board cannot adopt a new claim construction without giving the petitioner an opportunity to respond.”); 806-2 Reply at 29 n.6.*

Hearing Roadmap

1. Overview
2. Ground 2: A Multi-Plane Implementation Of Toyama's First Exemplary Structure
3. Ground 3: A Combination Of Toyama's First Exemplary Structure And Its Second Modification
 1. The Petitions' Obviousness Theory
 2. PO's Gate-Replacement Inoperability Argument
 3. PO's Current-Elimination Inoperability Argument
 4. Petitioner's Motivation To Combine
 5. Limitation [8.H]: Dummy Channel Structures "Surrounding" TAC Region
 6. "Etch Stop Plug" Limitation
4. Ground 1: Toyama's Second Modification

The Proposed Combination Of Two Toyama Embodiments

- The Petitions demonstrated that a POSITA would have found it obvious to form Toyama's Second Modification's "through-memory-level via structures" in a unitary material, as in Toyama's first exemplary structure.

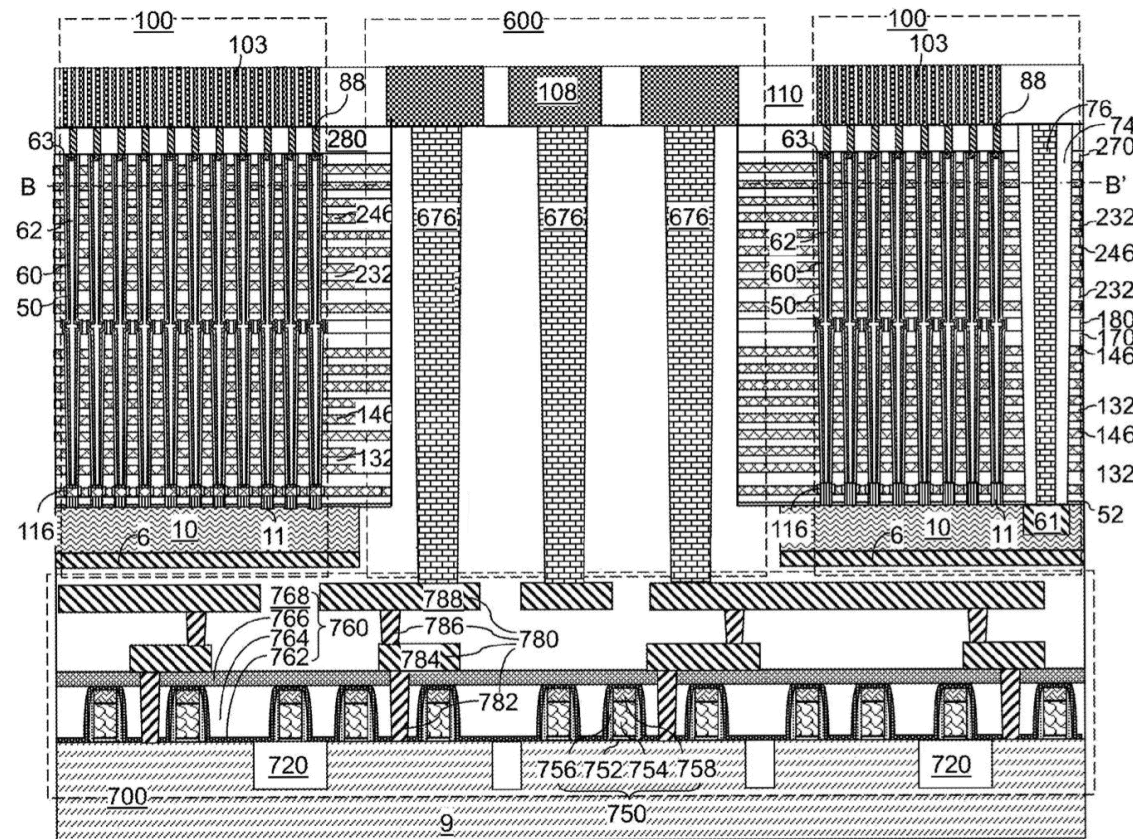


FIG. 49

*Toyama, Figure 49 (modified);
806-1 Petition at 96-108; 806-2
Petition at 100-113.*

The Proposed Combination Is A Simple Substitution

- The Petitions explained that the proposed combination would have been nothing more than a simple substitution of known elements with predictable results.

As the Petition explains in further detail below, the obviousness combination is nothing more than the mere substitution of one element (the Second Modification's "insulating liners 674") for another known in the field (a unitary dielectric fill material, as in the first exemplary structure's "dielectric fill material portion 430") to yield a predictable result (e.g., electrically isolating the Second Modification's "through-memory-level via structures"). Toyama, Figs. 16B, 48B, [0378]; Lee ¶ 183; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

806-1 Petition at 100; 806-2 Petition at 105.

Ground 3 > 2. PO's Gate-Replacement Inoperability Argument Technology Background

- A “control gate,” sometimes called a “word line,” is an electrically conductive layer used to control the operation of a flash memory cell.

806-1 Lee-Reply ¶ 62; 806-2 Lee-Reply ¶ 74.

- Gate replacement is the conventional part of a 3D NAND flash memory manufacturing process in which the memory strings' control gates are formed.

806-1 Lee-Reply ¶ 63; 806-2 Lee-Reply ¶ 75.

- Conventionally, etchant is applied to slit openings (the openings subsequently filled in to form slit structures 76) to etch away sacrificial layers that are then replaced with control gates.

806-1 Lee-Reply ¶¶ 65-66; 806-2 Lee-Reply ¶¶ 73-79.

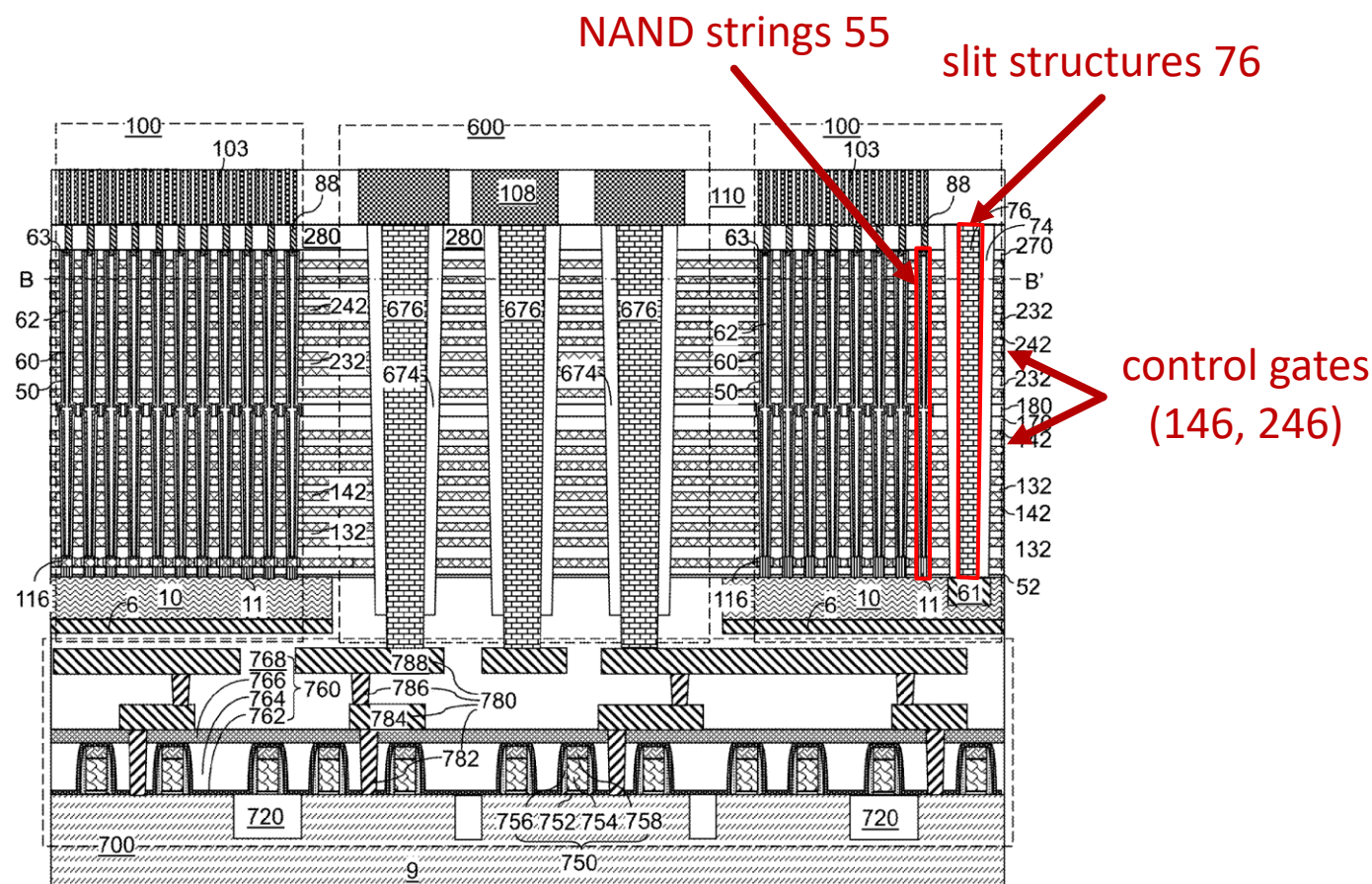


FIG. 49

*Toyama, Figure 49 (annotated); 806-1
Petition at 18-20; 806-2 Petition at 17-19.*

Ground 3 > 2. PO's Gate-Replacement Inoperability Argument

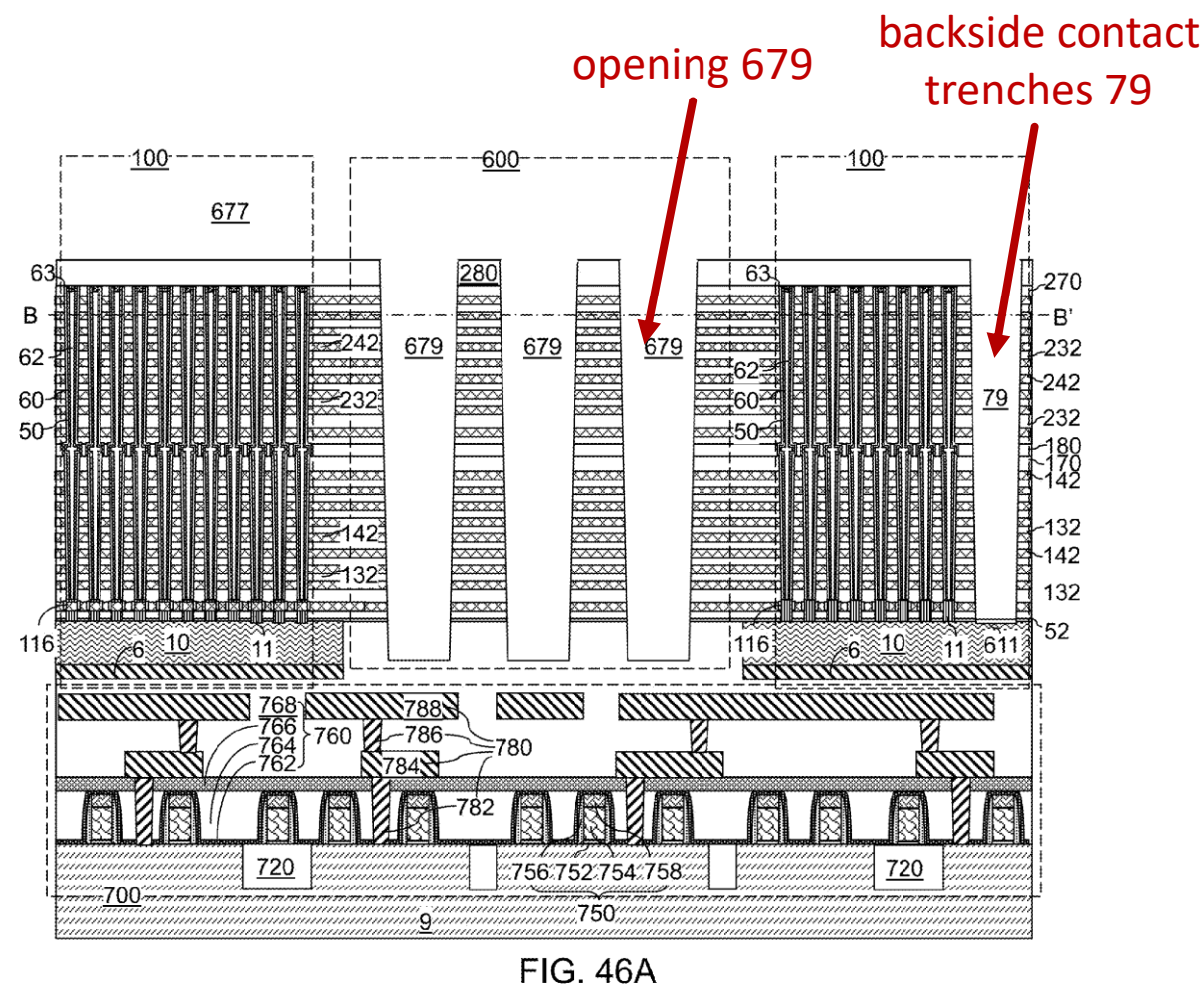
The Dispute

- PO contends that the combination would fail during the gate-replacement step of manufacturing because it replaces “openings 679” with a unitary dielectric structure.

806-1 POR at 40-41; 806-1 Sur-reply at 24-25; 806-2 POR at 58-62; 806-2 Sur-reply at 24-26.

- Petitioner has shown, however, that a POSITA would have been able to use Toyama's slit structure openings (“trenches 79”), which remain unchanged by the proposed modification, for gate replacement.

806-1 Reply at 21-23; 806-1 Lee-Reply ¶¶ 61-67; 806-2 Reply at 19-21; 806-2 Lee-Reply ¶¶ 73-79.



Toyama, Figure 46A.

Toyama's Embodiments All Use Slit Structure Openings For Gate Replacement

Toyama's Embodiments All Use Slit Structure Openings For Gate Replacement

- Contrary to PO's inoperability argument, both of the Toyama embodiments in the combination use slit structure openings—"backside contact trenches 79"—to allow access for gate replacement (red arrows).

- Even if the proposed combination would not use “openings 679,” it would continue to use “trenches 79.”

806-1 Reply at 21-22; 806-2 Reply at 20.

- PO does not dispute that many of Toyama's other embodiments, such as its first exemplary structure, ***exclusively*** use “trenches 79” for gate replacement.

806-1 Reply at 20; 806-1 Lee-Reply ¶ 65; 806-2 Reply at 20; 806-2 Lee-Reply ¶ 76.

- PO's arguments that "trenches 79" are insufficient for gate replacement are pure attorney argument unsupported by Dr. Yang, and contradicted by Dr. Lee's testimony.

806-1 Reply at 21-22; 806-1 Lee-Reply ¶¶ 62, 65-66.

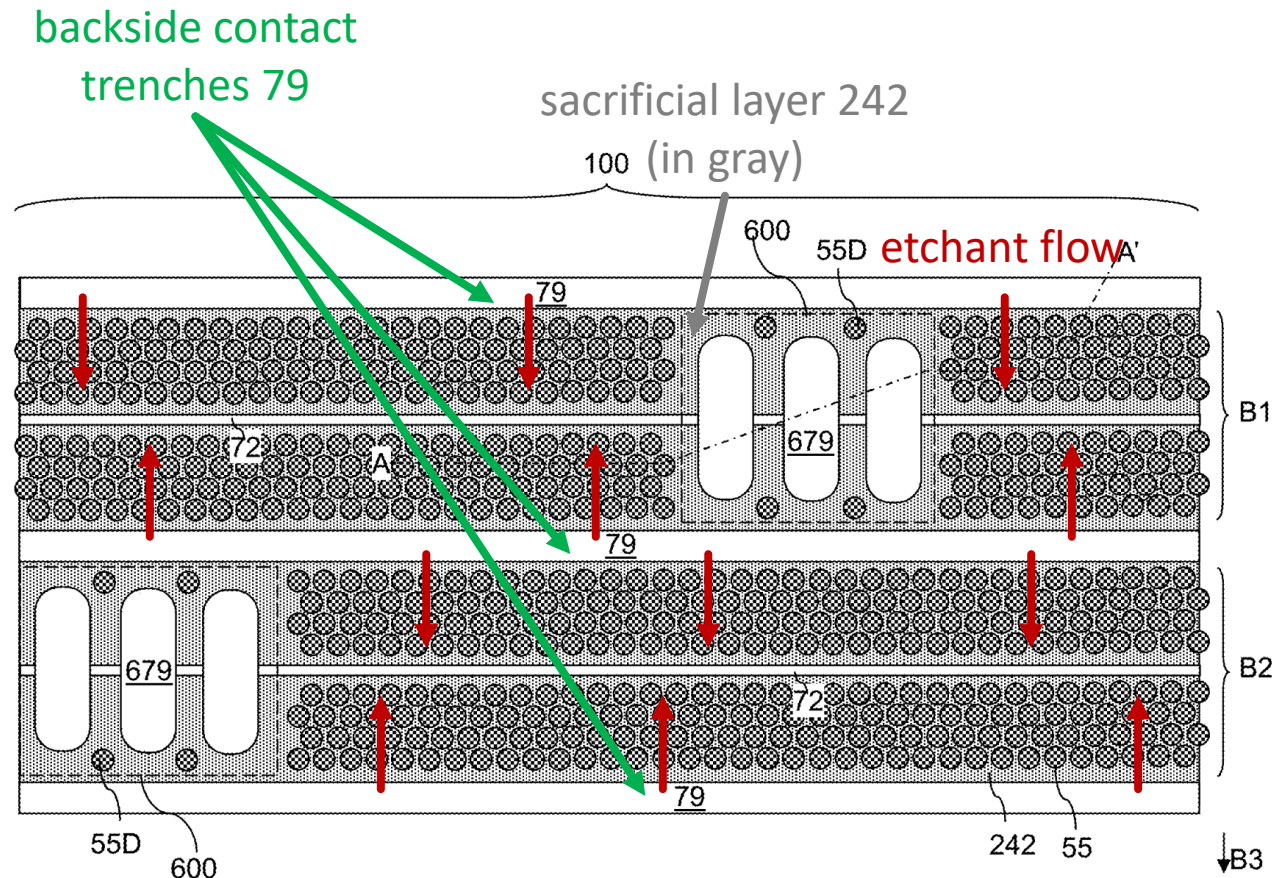


FIG. 45B

Toyama, Figure 45B.

Ground 3 > 2. PO's Gate-Replacement Inoperability Argument

Toyama Teaches Using Only “Trenches 79” For Gate Replacement In Materially Identical Embodiments

- PO asserts that a “dielectric block within the memory cell array” would prevent exclusive use of “trenches 79” for gate replacement.

806-1 Sur-reply at 25-26; 806-2 Sur-reply at 24-25.

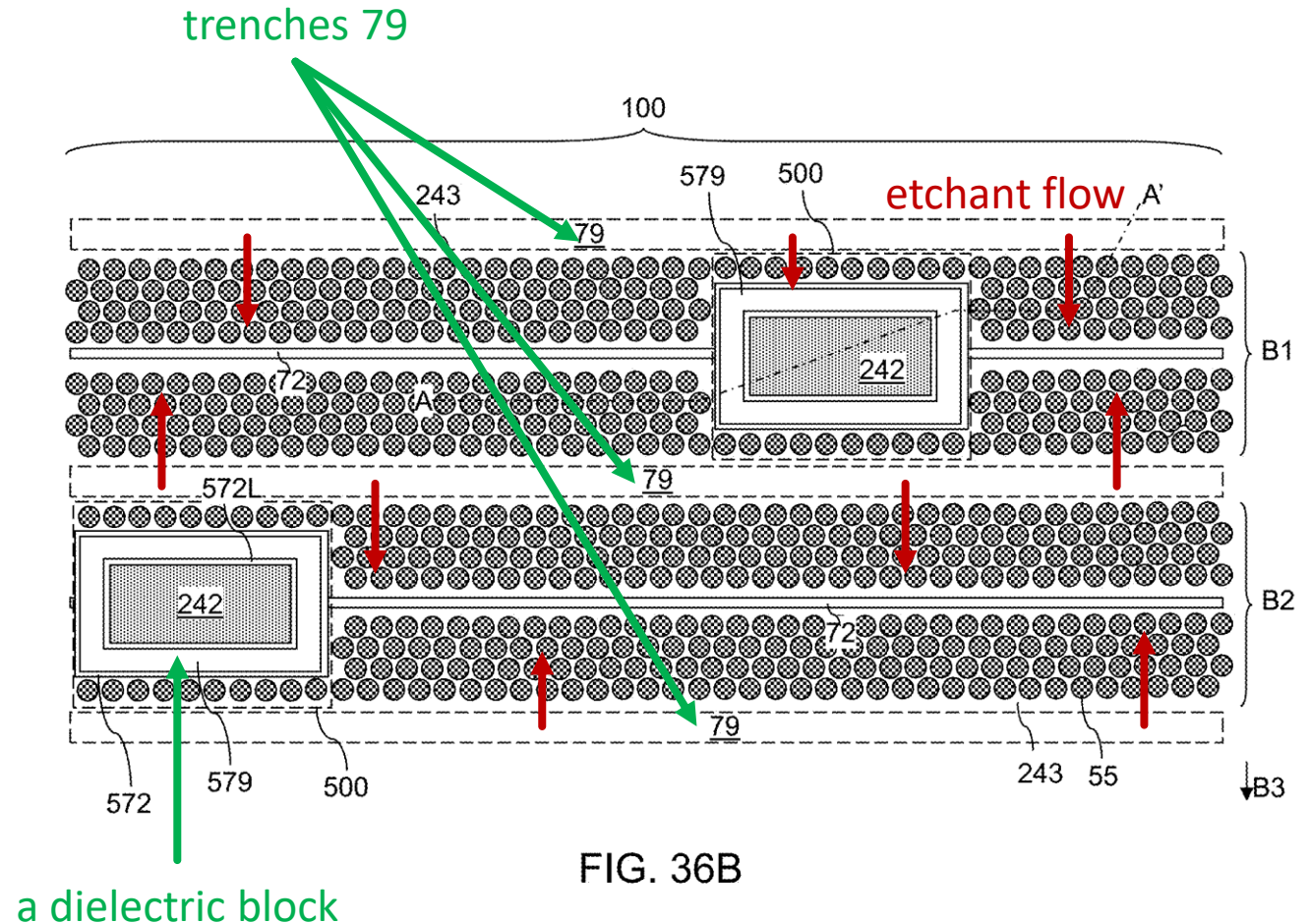
- Toyama describes embodiments (shown in, e.g., Figure 36B) with a dielectric block in the memory array. 806-1 Reply at 24; 806-2 Reply at 20; Toyama, Figures 12-13, 36B, 69B.

- PO asserts that the '806 patent has “more open flow paths” than Toyama.

806-1 Sur-reply at 25-26; 806-2 Sur-reply at 25.

- It is improper to compare of the scale of Toyama and '806 patent figures.

806-1 Reply at 27-28 (citing *Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l, Inc.*, 222 F.3d 951, 956 (Fed. Cir. 2000));
806-2 Reply at 23-25.



Toyama, Figure 36B (annotated); 806-1 Lee-Reply ¶ 65 (discussing Toyama's fourth exemplary structure); 806-2 Lee-Reply ¶ 77 (same).

PO's Teaching Away Argument Must Fail

- PO's teaching away argument fails as a matter of law because PO has not identified anything in Toyama or another reference that "criticizes, discredits, or otherwise discourages the solution claimed."

In re Meza, 780 F. App'x 895, 902 (Fed. Cir. 2019); 806-1 Reply at 23; 806-2 Reply at 21.

- As Dr. Lee testified, and PO does not rebut, a POSITA with knowledge of Toyama and the substantial use in the art of slit structures for gate replacement would have known how to adjust relevant design parameters to have a functional and manufacturable device:

92 (citing Toyama, [0332], [0390]. To the extent that not using "openings 679" reduces access for gate replacement, a POSITA would have known how to adjust the sizing and spacing of "trenches 79" so as to achieve a successful gate replacement in light of the numerous prior art devices, discussed above, that exclusively use slit structures for gate replacement. A POSITA would have had a reasonable expectation of success in manufacturing the proposed modification with slit structures alone being used for gate replacement.

806-1 Lee-Reply ¶ 65;
806-2 Lee-Reply ¶ 77.

The '806 Patent Presumes That A POSITA Knew Slit-Structure-Based Gate Replacement

- PO's argument that gate replacement using slit structures (as in the proposed combination) was outside of a POSITA's skill is contradicted by the '806 patent's own disclosure, which instructs performing gate replacement using slit openings in a single sentence without any elaboration.

In operation 314 of method 300, slit openings 900, shown in FIG. 9, can be used for a “gate replacement” process (also known as the “WL replacement” process) in which second dielectric layers 402 (shown in FIG. 9; e.g., SiN) in stack 400 are replaced with conductor layers 206 (shown in FIG. 10; e.g., W). As a result, alternating dielectric stack 400 is

'806 patent, 16:27-34; 806-1 Reply at 22-23; 806-2 Reply at 20-21.

- The '806 patent's silence on how to use only slit structures for gate replacement “suggest[s] that a person of ordinary skill in the art was more than capable of” doing so.

806-1 Reply at 22-23 (citing Uber Techs., Inc. v. X One, Inc., 957 F.3d 1334, 1339 (Fed. Cir. 2020)); 806-2 Reply at 20-21 (same).

Micron Ex. 1053, Micron v. YMTC
IPR2024-00791, -00911 49

The Dispute

- PO contends that the proposed combination, by replacing Toyama's Second Modification's dielectric liners with a unitary dielectric structure as in the first exemplary structure, would "block current and render the device "inoperable."

806-1 Sur-reply at 26; 806-2 Sur-reply at 26.

- Dr. Lee, supported by voluminous prior art evidence, testified that a POSITA would have been able to size the relevant components (e.g., the dielectric structure, the gate layers, and the TACs) to design a functional device.

806-1 Reply at 23-28; 806-2 Reply at 21-25.

73. A POSITA would have been able to design the proposed combination—e.g., adjusting the size of the dielectric fill, TACs, and surrounding circuitry — so as to preserve current flow and device functionality.

806-1 Lee-Reply ¶¶ 73-79 (citing Toyama, [0156], [0329], Figures 39B, 69B, '806 patent, 3:57-59, Ex. 1013, at p.120); 806-2 Lee-Reply ¶¶ 80-91 (same).

Ground 3 > 3. PO's Current-Elimination Inoperability Argument

Toyama Expressly Contradicts PO's Current-Elimination Argument

- Toyama's express disclosure of embodiments with a dielectric block in the memory array region contradicts PO's assertion that doing so in Ground 3 would render the device inoperable.

806-1 Reply at 24 (rebutting 806-1 POR at 42-43); 806-1 Lee-Reply ¶ 77; 806-2 Reply at 22; 806-2 Lee-Reply ¶ 89.

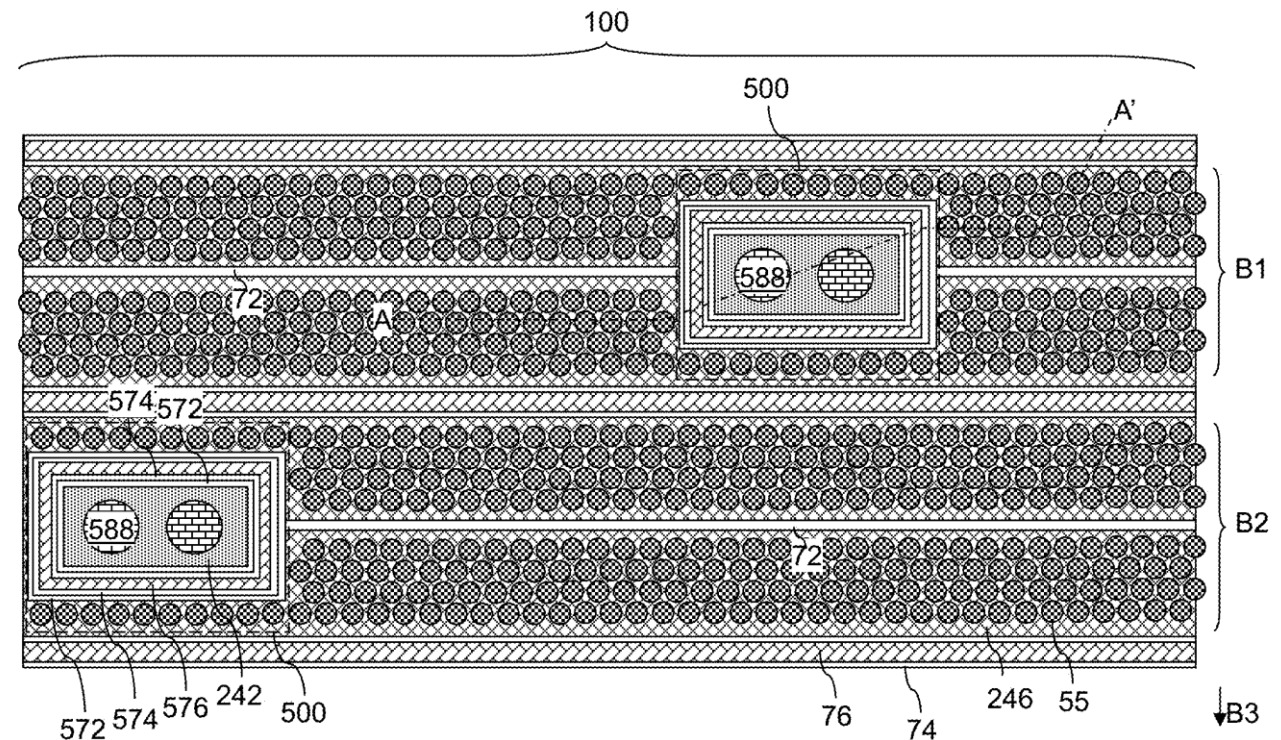


FIG. 39B

Toyama, Figure 39B; 806-1 Reply at 24; 806-2 Reply at 22.

Ground 3 > 3. PO's Current-Elimination Inoperability Argument

The '806 Patent Itself Contradicts PO's Current-Restriction Argument

- PO does not dispute that the '806 patent's own gate layers narrow around the dielectric structure, just like the proposed combination.

806-1 Reply at 26-28; 806-1 Lee-Reply ¶¶ 74-76;
806-2 Reply at 23-25; 806-2 Lee-Reply ¶¶ 86-88.

- Yet the '806 patent does not teach how to avoid PO's alleged current-restriction issue. This "suggest[s] that a person of ordinary skill in the art was more than capable of" sizing a device's components to accommodate the dielectric structure.

806-1 Reply at 26 (quoting *Uber Techs., Inc. v. X One, Inc.*, 957 F.3d 1334, 1339 (Fed. Cir. 2020));
806-2 Reply at 24 (same).

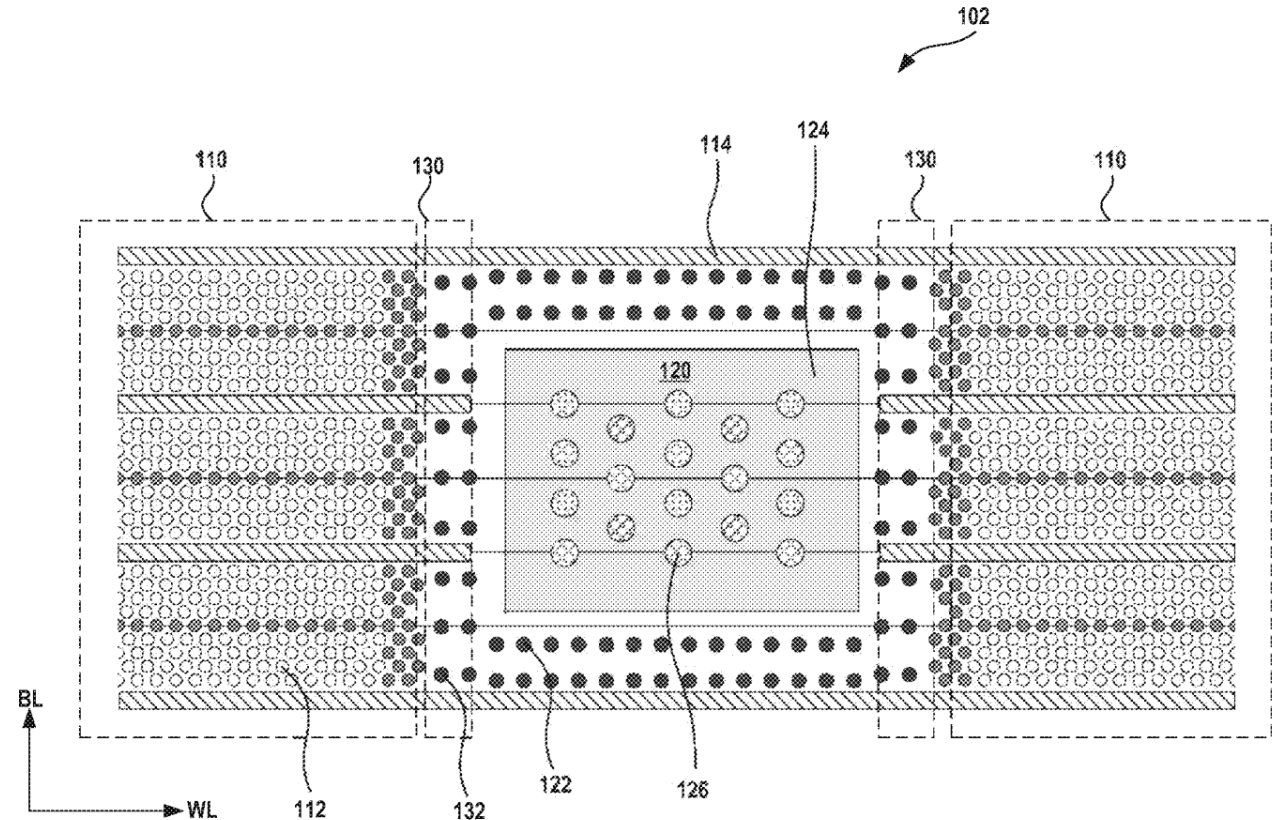


FIG. 1A '806 patent, Figure 1A (annotated);
806-1 Reply at 26-28; 806-2 Reply at 23-25.

Micron Ex. 1053, Micron v. YMTC
IPR2024-00791, -00911 52

Ground 3 > 3. PO's Current-Elimination Inoperability Argument

PO Improperly Relies On The Scale Of Figures

- To support its argument, PO repeatedly relies on a comparison between the relative sizes of features in '806 patent's Figure 1A and Toyama's Figure 48B.

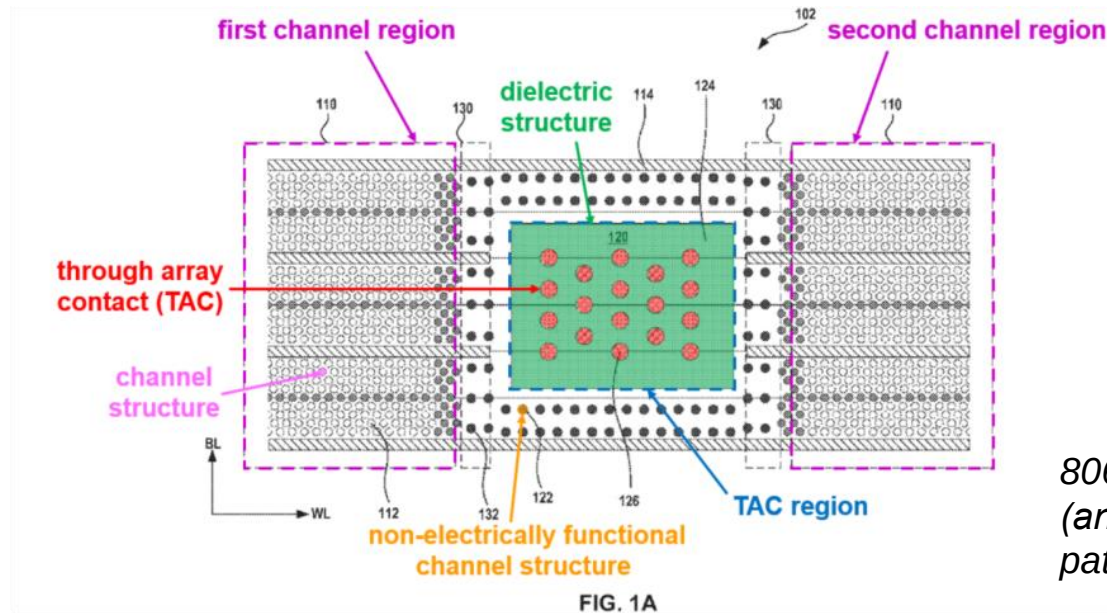
806-1 POR at 26-27; 806-1 Sur-reply at 27; 806-2 POR at 62; 806-2 Sur-reply at 27.

- But PO's comparison of figures runs afoul of the legal principle that figures are presumed to be not to scale.

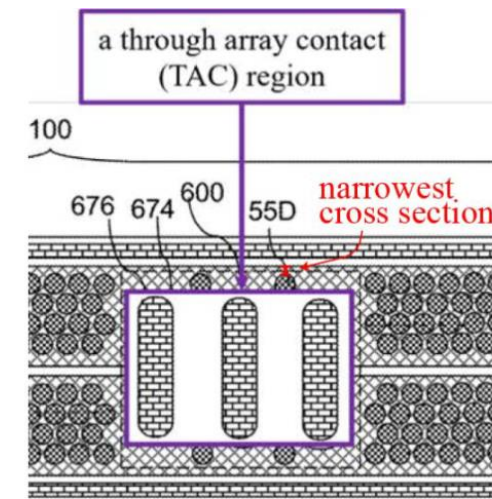
806-1 Reply at 27-28 (citing Hockerson-Halberstadt, Inc. v. Avia Grp. Int'l, Inc., 222 F.3d 951, 956 (Fed. Cir. 2000)); 806-2 Reply at 28 (same).

- That legal presumption is buttressed by the '806 patent and Toyama's express statements that their figures are not to scale.

Id. (citing Toyama, [0156]; '806 patent, 3:57-59).



*806-1 POR at 44
(annotating '806
patent, Figure 1A).*



*Pet. 116
(excerpt, PO annotation in red)*

*806-1 Sur-reply at 27
(annotating a
modified version of
Toyama, Figure 48B);
806-2 Sur-reply at 27
(same)*

A POSITA Would Have Known Of Techniques To Mitigate Any Current Restriction

- Even assuming the proposed combination materially restricted gate-layer current (it does not), a POSITA would have known to use vertical interconnects to solve this alleged problem.

806-1 Reply at 24-25; 806-1 Lee-Reply ¶¶ 78-79; 806-2 Reply at 23; 806-2 Lee-Reply ¶¶ 90-91.

- PO asserts that adding staircases on both sides would “increase device size,” “eliminat[e] critical interconnect capabilities,” and “impact ... peripheral devices.”

806-1 Sur-reply at 28-29; 806-2 Sur-reply at 28.

- But Dr. Lee’s testified (supported by textbook evidence) that this approach was a standard design in the prior art and a POSITA would have viewed it as a suitable option.

806-1 Lee-Reply ¶¶ 78-79; 806-2 Lee-Reply ¶¶ 90-91.

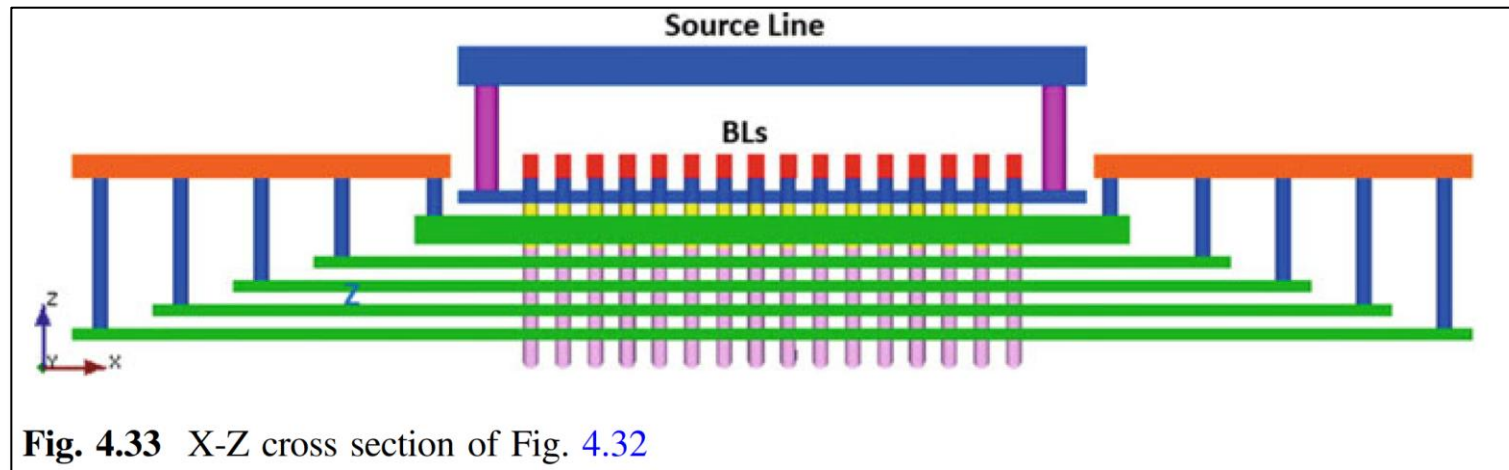


Fig. 4.33 X-Z cross section of Fig. 4.32

Ex. 1013 (Micheloni 2013 Textbook), at p. 120; 806-1 Lee-Reply ¶ 78 (discussing same); 806-2 Lee-Reply ¶ 90 (same).

Micron Ex. 1053, Micron v. YMTC
IPR2024-00791, -00911 54

Ground 3 > 4. Motivation to Combine The Dispute

- The Petitions explained that using a unitary dielectric block (as in Toyama's first exemplary structure) in place of insulating liners (as in Toyama's Second Modification) would have been a simple substitution with predictable results.

806-1 Petition at 100; 806-1 Lee ¶ 183; 806-2 Petition at 105; 806-2 Lee ¶ 220.

- In addition, the Petitions identified two specific motivations to combine:
 - Using a unitary dielectric block would reduce capacitive coupling compared to the dielectric liners of Toyama's Second Modification.

806-1 Petition at 101-103; 806-2 Petition at 106-108.

- Placing a unitary block like that of Toyama's first exemplary structure within a memory region allows the TACs to be closer to the memory stack structures.

806-1 Petition at 103-104; 806-2 Petition at 108-109.

Ground 3 > 4. Motivation to Combine

Petitioner's Mere-Substitution Rationale Is Unrebutted

- The Petitions explained that the proposed combination (i.e., using a unitary dielectric block in place of insulating liners) is a mere substitution of one known element for another to yield a predictable result.

As the Petition explains in further detail below, the obviousness combination is nothing more than the mere substitution of one element (the Second Modification's "insulating liners 674") for another known in the field (a unitary dielectric fill material, as in the first exemplary structure's "dielectric fill material portion 430") to yield a predictable result (e.g., electrically isolating the Second Modification's "through-memory-level via structures"). Toyama, Figs. 16B, 48B, [0378]; Lee ¶ 183; *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007).

806-1 Petition at 100;
806-2 Petition at 105.

- PO does not dispute that the base element (insulating liners) and the substituting element (a unitary dielectric fill) were "known in the field."
- PO does not dispute that substituting in a unitary dielectric fill would have the predictable result of electrically isolating the proposed combination's TACs.

Petitioner's Mere-Substitution Rationale Is Sufficient To Establish Obviousness

- *KSR* reiterates an age-old principle: where a proposed combination is a mere substitution of known elements with predictable results, a separate motivation to combine is not required.

[I]n *Sakraida v. Ag Pro, Inc.*, 425 U.S. 273 (1976), the Court derived from the precedents the conclusion that when a patent “simply arranges old elements with each performing the same function it had been known to perform” and yields no more than one would expect from such an arrangement, the combination is obvious. *Id.*, at 282, 96 S.Ct. 1532. ... *Sakraida* and *Anderson's–Black Rock* are illustrative—a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions.

KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 425-26 (2007); 806-1 Petition at 108; 806-1 Reply at 28-29; 806-2 Petition at 105; 806-2 Reply at 25-26.

- That principle is directly applicable here, where individual dielectric liners and a unitary dielectric block were known elements with established functions.

PO's Objections To Petitioner's Capacitive-Coupling And TAC-Placement Rationales Are Legally Irrelevant

- PO's objections to Petitioner's capacitive-coupling and TAC-placement rationales cannot defeat obviousness because neither contradicts that the use of a dielectric block in place of liners is a "suitable option."

Intel Corp. v. Qualcomm Inc., 21 F.4th 784, 800 (Fed. Cir. 2021); 806-1 Petition at 101 (citing *Intel*).

- For example, PO's contention that liners already minimize capacitive coupling does **not** mean that a unitary dielectric block (as in the proposed combination) would unsuitably increase capacitive coupling.

806-1 Reply at 28-29; 806-2 Reply at 25-28.

- PO contends that the Second Modification's placement of the dielectric liners within the memory array is already advantageous. But that does **not** contradict the critical point—that using a unitary dielectric block would also be desirable because it has that advantage.

Id.

- PO's objections are no different from the patentee's arguments in *Intel* that the proposed combination was "less effective" than one of the primary references by itself. *Intel* rejected that argument as improperly requiring that the combination be the "best" option.

Intel, 21 F.4th at 800.

Ground 3 > 5. Dummy Channel Structures “Surrounding” TAC Region

The Limitation At Issue

Claim Element	Claim Language	806-1 IPR	806-2 IPR
[8.H]	“a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions”		

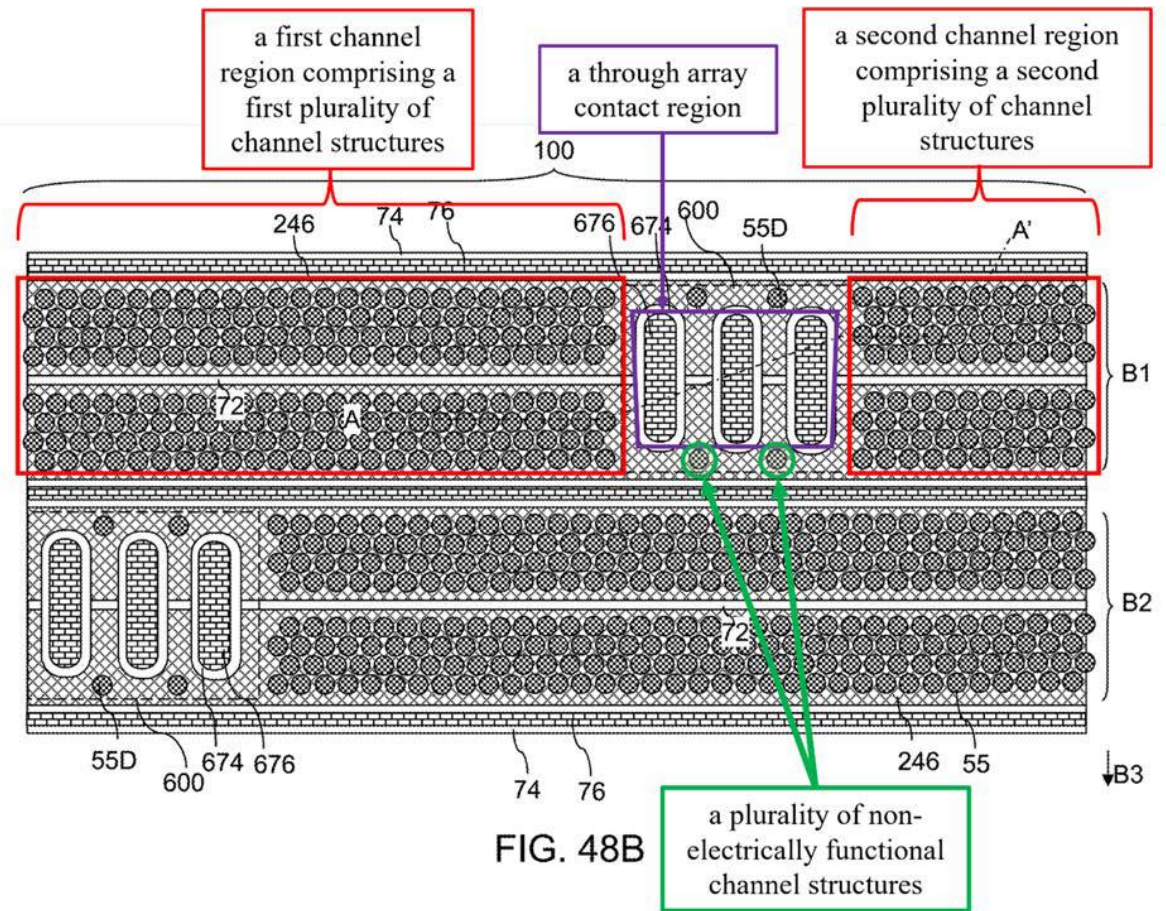
Ground 3 > 5. Dummy Channel Structures “Surrounding” TAC Region

Toyama’s Figure 48B Discloses Dummy Structures “Surrounding” A TAC Region

- The Petition explained that Toyama discloses a plurality of non-electrically functional channel structures (“dummy memory stack structures 55D”) meeting the limitation.

806-1 Petition at 52; 806-2 Petition at 50-53.

- PO does not dispute that “dummy memory stack structures 55D are a plurality of non-electrically functional channel structures, or that the part of region 600 indicated in purple is a TAC region.
- PO’s **only** dispute is the limitation’s requirement that the dummy structures are “surrounding” the TAC region.



Toyama Figure 48B; 806-1 Petition at 13; 806-2 Petition at 51.

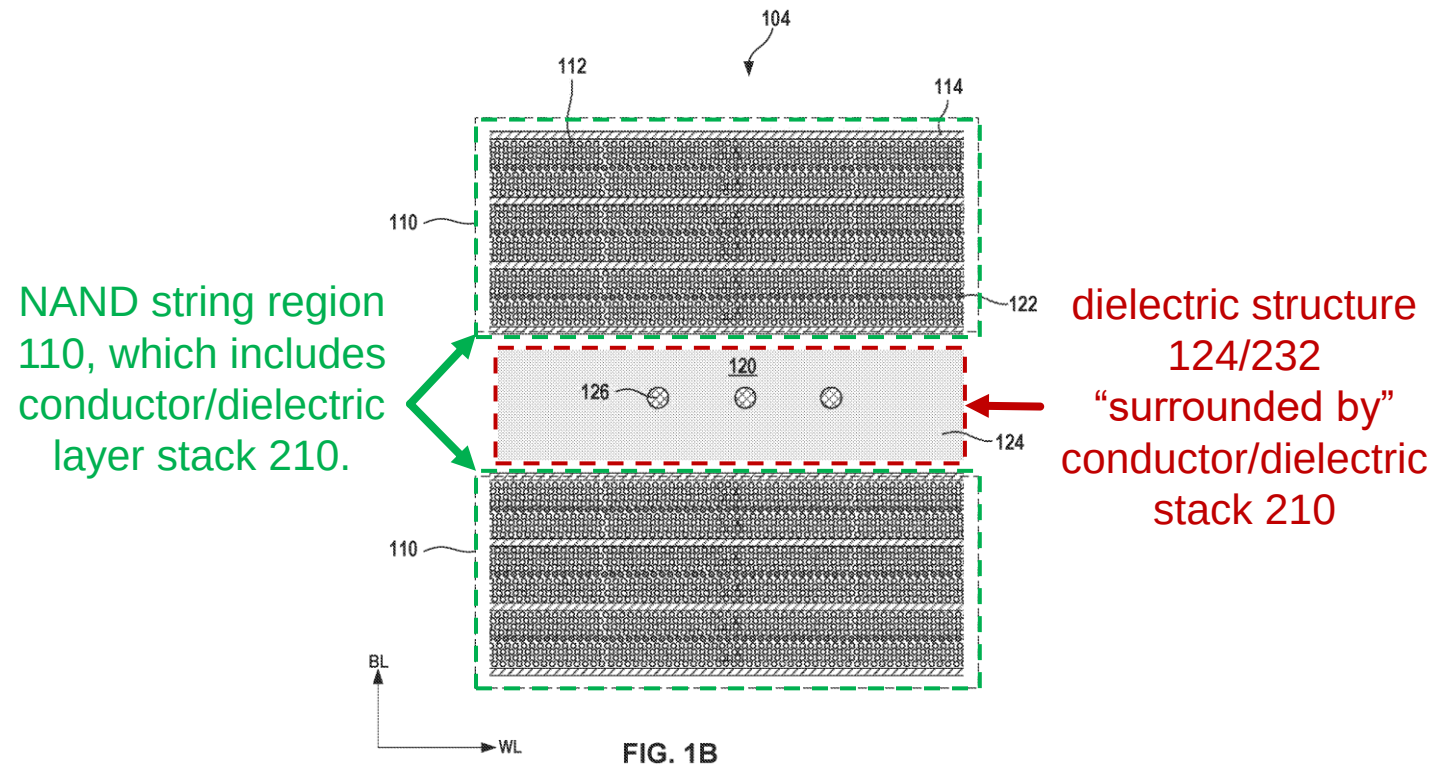
Ground 3 > 5. Dummy Channel Structures “Surrounding” TAC Region PO’s Distinction of Figure 48B Uses An Unduly Narrow Construction Of “Surrounding”

- PO asserts that because Figure 48B shows dummy structures 55D on only two sides of the TAC region, dummy structures 55D are not “surrounding” the TAC region.

806-1 POR at 30-31; 806-2 POR at 30-33.

- PO’s construction of “surrounding” is inconsistent with the ’806 patent, which expressly describes bordering on two sides as “surrounded by.”

*806-1 Petition at 52 n.9; 806-1 Lee ¶ 119;
806-2 Petition at 50 n.13; 806-2 Lee ¶ 137.*



shown in FIGS. 1A-1C). Consequently, as shown in the plan-views of FIGS. 1A-1C, dielectric structure 232 can be surrounded by conductor/dielectric stack 210. Further,

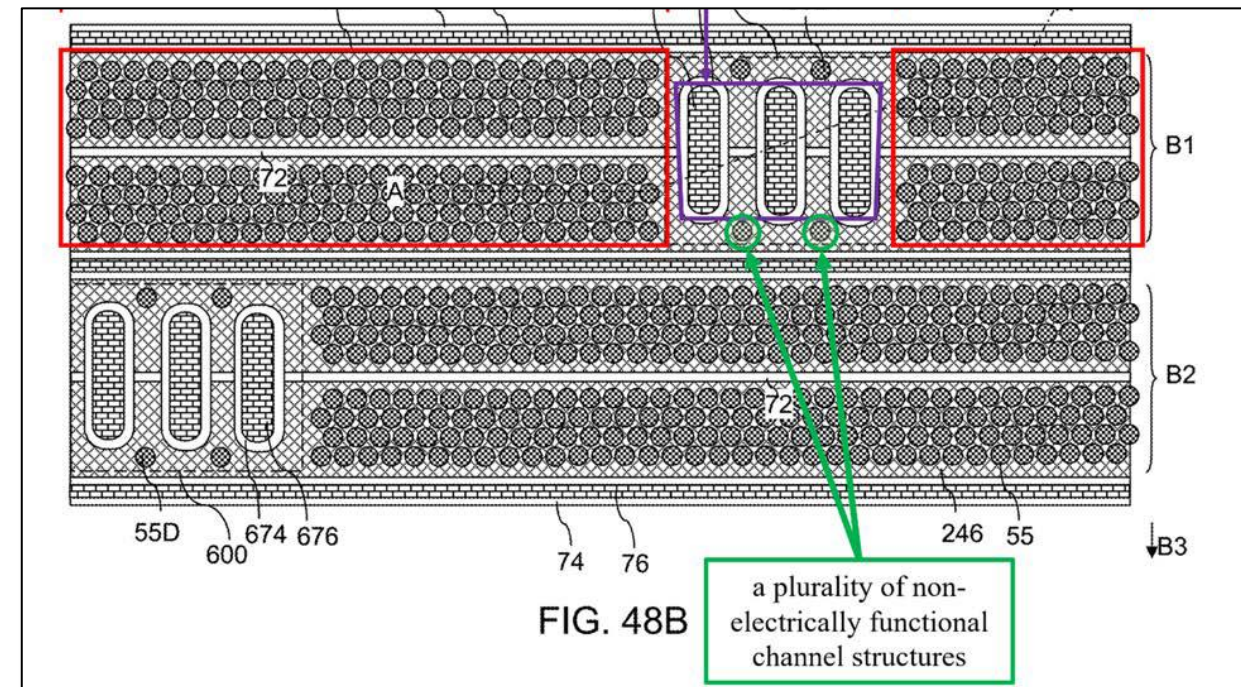
Ground 3 > 5. Dummy Channel Structures “Surrounding” TAC Region Toyama Discloses The “Surrounding” Requirement Even Under PO’s Interpretation

- Toyama discloses the “surrounding” limitation even under PO’s erroneous requirement that dummy structures are on all sides of the TAC region.
- Specifically, the Petition demonstrated that because Toyama describes its dummy stack structures 55D as “provided at the periphery” of Toyama’s TAC region, a POSITA would have understood from Toyama’s description that dummy structures 55D are on “all sides” of Toyama’s TAC region.

806-1 Petition at 54 (citing 806-1 Lee ¶ 120).

entirely within a block (B1, B2, etc.). Dummy memory stack structures 55D can be provided at a periphery of the through-memory-level via regions 600. The dummy memory stack

*Toyama, [0333]; 806-1 Petition at 53 (citing same);
806-2 Petition at 52 (same).*



Toyama, Figure 48B; 806-1 Petition at 120; 806-2 Petition at 51.

Micron Ex. 1053, Micron v. YMTC

IPR2024-00791, -00911 62

Ground 3 > 5. Dummy Channel Structures “Surrounding” TAC Region

PO’s Argument Misunderstands The Meaning Of “Periphery”

- PO asserts that by “provid[ing]” dummy structures 55D “at the periphery,” Toyama merely indicates that structures 55D are “at the top and bottom edges.”

806-1 Sur-reply at 14-15; 806-2 Sur-reply at 15-17.

- PO’s assertion is untimely because it was raised for the first time in sur-reply; the POR ignored Toyama’s “provided at the periphery” disclosure.

806-1 POR at 22-25; 806-2 POR at 30-33.

- Dr. Lee’s testified that a POSITA would have understood Toyama’s disclosure to include placing such structures on “all sides” of the TAC region.

806-1 Lee ¶ 120; 806-2 Lee ¶ 139.

- Dr. Yang testified at deposition (at right) that the “periphery” of a rectangle is “the four sides of the rectangle.”



*Yang Depo.
Ex. 7.*

Q. Well, let's take, I guess, the second framing that you mentioned, which is a gray object on a white background. If we take that context, what would you say the periphery is?

A. Assuming that that black border is a piece of the gray object, it appears to be the outer edge of that black border going around the four sides of the rectangle -- of the gray rectangle.

Ex. 1047 (4/24 Yang deposition) at 24:3-10; 806-1 Reply at 12 (discussing same); 806-2 Reply at 13.

Micron Ex. 1053, Micron v. YMTC
IPR2024-00791, -00911

A POSITA Would Have Found Providing Dummy Channel Structures on All Sides of the TAC Region Obvious

- The Petition showed that even if Toyama does not expressly disclose this limitation (it does), a POSITA would have found it to be a predictable use of prior art elements according to their established functions.

806-1 Petition at 53-54 (citing KSR Int’l Co. v. Teleflex Inc., 550 U.S. 398, 401 (2007));

806-1 Lee ¶ 121; 806-2 Petition at 52-53; 806-2 Lee ¶ 140.

- Toyama discloses non-electrically functional channel structures (Toyama’s “dummy memory stack structures 55D”).

806-1 Petition at 51-52; 806-2 Petition at 50-51.

- Toyama discloses that “dummy ... structures 55D” have the purpose of providing structural support.

806-1 Petition at 53; 806-2 Petition at 51-52.

- The use of dummy channel structures to provide structural support was well-known in the art.

806-1 Petition at 20-21; 806-2 Petition at 19.

- Thus, a POSITA would have found that placing dummy stack structures on all sides of the TAC region was a predictable use of prior art elements.

806-1 Petition at 53-54; 806-2 Petition at 52-53.

Ground 3 > 5. Dummy Channel Structures “Surrounding” TAC Region

PO’s Arguments Against Obviousness Are Untimely and Meritless

- PO argues in sur-reply that a POSITA would not have been motivated to surround the TAC region with dummy channel structures 55D because, to PO, these regions would not have needed additional structural support.
806-1 Sur-reply at 15-16; 806-2 Sur-reply at 16-17.
- PO’s argument is untimely and forfeited. The PORs entirely ignored the Petition’s obviousness theory. It is improper for PO to respond in sur-reply by introducing new arguments, which should have been made in the POR.
806-1 POR at 22-25; 806-2 POR at 30-33; 37 C.F.R. § 42.23(b).
- Simple substitutions with predictable results, as here, do not need a separately articulated motivation to combine.
806-1 Petition at 53-54; 806-2 Petition at 52-53.
- Dr. Lee testified that a POSITA would have been motivated to place dummy structures 55D around the TAC region based on the well-known structural-support and heat-dissipation benefits of dummy structures 55D--benefits that are amplified when dummy structures surround the TAC region.
806-1 Lee ¶¶ 54, 121; 806-2 Lee ¶¶ 55, 140.
- Dr. Lee explained that this motivation is reinforced by a POSITA’s understanding of edge effects, which counsel against placing functional channels (55) directly adjacent to a TAC region.
806-1 Lee-Reply ¶ 23; 806-2 Lee-Reply ¶ 35.

Ground 3 > 6. “Etch Stop Plug” Limitation

PO’s “Etch Stop Plug” Arguments Must Fail

- The Petition explained that Toyama’s “drain regions 63” are “etch stop plugs” as claimed.

806-2 Petition at 125; 806-2 Lee-Reply ¶ 253; supra slide 36.

- As previously explained, PO’s construction of the “etch stop plug” limitation is nonsensical and would exclude every disclosed embodiment.

See supra, slides 27-35 (Ground 1 > “Etch Stop Plug” Limitation > Claim Construction).

- Even under PO’s meritless construction, Toyama’s “bit lines 103” meet the “etch stop plugs” limitation for the same reason as PO contends “bit lines 250” the limitation.

See supra, slides 37-40 (Ground 1 > “Etch Stop Plug” Limitation > Obviousness Under PO’s Construction).

Hearing Roadmap

1. Overview
2. Ground 2: A Multi-Plane Implementation Of Toyama's First Exemplary Structure
3. Ground 3: A Combination Of Toyama's First Exemplary Structure And Its Second Modification
4. Ground 1: Toyama's Second Modification
 - Limitation [8.G.iii]: TACs Extending Vertically through the Dielectric Structure
 - Limitation [8.H]: Dummy Channel Structures "Surrounding" TAC Region
 - Limitation [10.B]: "Etch Stop Plug" Limitation

Ground 1 > TACs Extending Vertically Through A Dielectric Structure

The Limitation at Issue

Claim Element	Claim Language	806-1 IPR	806-2 IPR
[8.G.iii]	“a plurality of through array contacts (TACs) extending vertically through the dielectric structure”		

Ground 1 > TACs Extending Vertically Through A Dielectric Structure > Claim Construction

The Parties' Claim Construction Dispute

- Claim 8 recites “a dielectric structure” and “through array contacts (TACs) extending vertically through the dielectric structure.”
- The parties' dispute centers on whether:
 - the claimed device's “through array contacts” may extend vertically through multiple dielectric structures (as Petitioner contends); or whether
 - the claim requires that multiple “through array contacts” extend through a “single dielectric structure” (as PO contends).

806-1 Reply at 2-6; 806-2 Reply at 6-9.

806-1 POR at 18; 806-2 POR at 26.

Ground 1 > TACs Extending Vertically Through A Dielectric Structure > Claim Construction

Petitioner's Construction Complies with Antecedent Basis Principles

- The antecedent basis for the claimed “the dielectric structure” is “a dielectric structure.”
806-1 Reply at 4; 806-2 Reply at 7.
- PO does not dispute that “a” means “one or more,” absent exceptions that PO agrees do not apply.
Id.
- In *Baldwin*, the Federal Circuit explained that “the” takes its numerosity from the element’s antecedent basis:

The use of a definite article (“said” or “the”) to refer back to an initial indefinite article does not implicate, let alone mandate the singular. Because the initial indefinite article (“a”) carries either a singular or plural meaning, any later reference to that same claim element merely reflects the same potential plurality.

Baldwin Graphic Sys., Inc. v. Siebert, Inc., 512 F.3d 1338, 1343 (Fed. Cir. 2008).

- It follows that the limitation “the dielectric structure” has a “plural-allowing meaning.”
806-1 Reply at 4 (quoting Baldwin); 806-2 Reply at 7 (same).

Ground 1 > TACs Extending Vertically Through A Dielectric Structure > Claim Construction

The Specification Reinforces the General Rule That “A” Is Plural-Allowing

- The '806 patent specification expressly provides that “a” and “the” can convey a plural usage:

Similarly, terms, such as “a,” “an,” or “the,” again, may be understood to convey a singular usage or to convey a plural usage, depending at least in part upon context.

'806 patent, 4:17-25.

- The Federal Circuit has held that similar language “reinforces” the “general rule” that “a” and “the” are plural-allowing:

That definition reinforces, rather than negates, the applicability here of the “one or more” general rule concerning “a” or “an.” It also brings into play the lexicography principle—that, with narrow exceptions, “[w]here the specification instructs as to the meaning of a claim term, ‘the inventor’s lexicography governs.’”

ABS Glob., Inc. v. Cytonome/St, LLC, 84 F.4th 1034, 1041 (Fed. Cir. 2023); 806-1 Reply at 4 (quoting ABS); 806-2 Reply at 6-7 (same).

- PO does not respond to Dr. Lee’s testimony that the context of the '806 patent supports a plural-allowing meaning of “a” and “the” dielectric structure.

806-1 Reply at 3 (806-1 Lee-Reply ¶¶ 12-15); 806-2 Reply at 6 (806-2 Lee-Reply ¶¶ 20-27).

Micron Ex. 1053, Micron v. YMTC
IPR2024-00791, -00911 71

Ground 1 > TACs Extending Vertically Through A Dielectric Structure > Claim Construction

Baldwin Supports Petitioner's Construction

- *Baldwin* involved a claim to “**a pre-soaked fabric roll** saturated to equilibrium with cleaning solvent disposed around a core, **said fabric roll having a sealed sleeve.**”

Baldwin Graphic Sys., Inc. v. Siebert, Inc., 512 F.3d 1338, 1340 (Fed. Cir. 2008); 806-1 Reply at 4-5; 806-2 Reply at 7-8.

- The district court interpreted the phrase “said fabric roll” as suggesting “a singular fabric roll,” such that multiple fabric rolls collectively having a single sleeve did not meet the limitation.
- The Federal Circuit reversed. It held that because the antecedent for “said fabric roll” was “a fabric roll,” the word “said” encompassed “one or more” fabric rolls. Thus, the claim covered an arrangement where several fabric rolls collectively had a single sleeve, even though no single fabric roll had its own sleeve.
- Here, like the district court in *Baldwin*, PO errs in reading the requirement that TACs extend through “the dielectric structure” to require a single dielectric structure. Instead, under *Baldwin*, “the” refers back to “a dielectric structure,” which covers “one or more,” and the claims cover an arrangement where the TACs extend through **one or more** dielectric structures.

806-1 Reply at 4-5 (quoting *Baldwin*); 806-2 Reply at 7-8 (same).

Ground 1 > TACs Extending Vertically Through A Dielectric Structure > Claim Construction

PO's Reliance on *Finjan* Is Misplaced

- *Finjan* is inapposite.

806-1 Sur-reply at 5.

- Here, unlike in *Finjan*, the '806 patent specification expressly contemplates that “a” and “the” may be used “to convey a plural usage.”

806-1 Reply at 5; 806-2 Reply at 8.

- In *Finjan*, different computers in the accused system performed different of the relevant claim's limitations.

806-1 Reply at 5-6 (quoting *Finjan*, 84 F.4th at 974); 806-2 Reply at 8-9 (same).

- Here, unlike in *Finjan*, it is undisputed that the “**same** ‘one or more’” dielectric structures in Toyama (here, “insulating liners 674”) satisfy **every** requirement of the claimed dielectric structures.

Id.

Ground 1 > TACs Extending Vertically Through A Dielectric Structure > Obvious Under PO's Construction

The Plain Meaning of “Structure” Does Not Include a Contiguosness Requirement

- Ground 1 renders the limitation obvious even under PO's construction.
- The plain meaning of “structure”—“something arranged in a definite pattern of organization”—does not impose a requirement that its components are contiguous.

806-1 Reply at 8 (quoting Ex. 1021, at 4); 806-2 Reply at 10 (same).

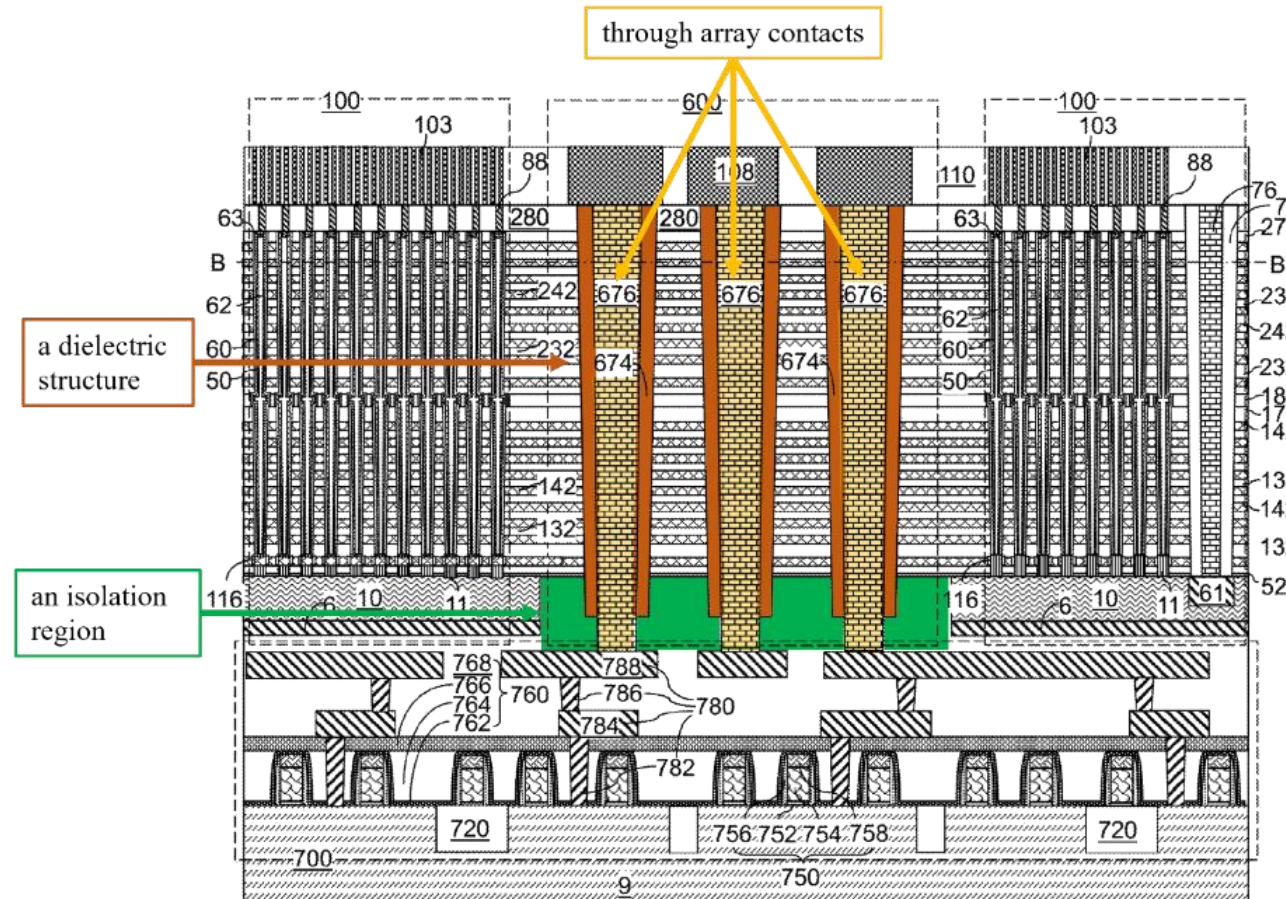
- Consistent with the plain meaning, both experts agree that the wall in the adjacent photo is a “structure” even though its components are not contiguous.

*806-1 Reply at 9 (Exs. 1044, 1045);
806-2 Reply at 10-12 (same).*



Ground 1 > TACs Extending Vertically Through A Dielectric Structure > POs Construction Toyama's "Insulating Liners 674" Are Individually and Collectively a Single Structure

- PO does not dispute that "insulating liners 674" (below) are arranged in a definite pattern of organization, e.g., the liners all have the same function of insulating the TACs from the alternating layer stack:



Toyama, Figure 49
(annotated); 806-1 Petition at
49-50; 806-2 Petition at 48-50.

FIG. 49

Ground 1 > Dummy Channel Structures “Surrounding” TAC Region

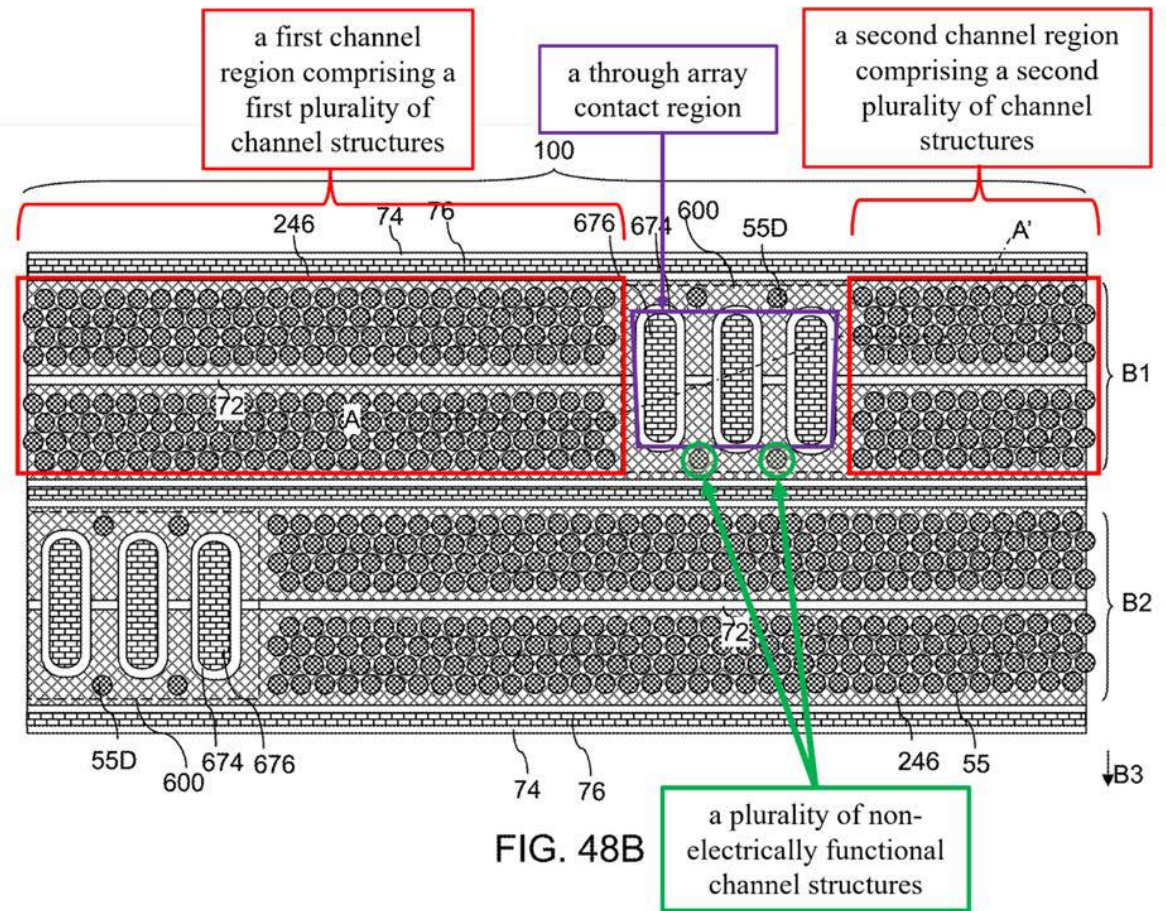
Ground 1 Discloses And Renders Obvious The “Surrounding” Limitation

- The Petition demonstrated that Ground 1’s “dummy memory stack structures 55D” disclose and render obvious non-electrically functional channel structures surrounding Ground 1’s TAC region (part of “through-memory-level via region 600”).

806-1 Petition at 52.

- PO’s arguments against Ground 1’s mapping for this limitation must fail for the same reasons as explained above for Ground 3.

See supra, slides 59-65 (Ground 3 > 5. Dummy Channel Structures Are “Surrounding” TAC Region).



Toyama Figure 48B (annotated).

Ground 1 > “Etch Stop Plug” Limitation

PO’s “Etch Stop Plug” Arguments Must Fail

- The Petition explained that Toyama’s “drain regions 63” are “etch stop plugs” as claimed.

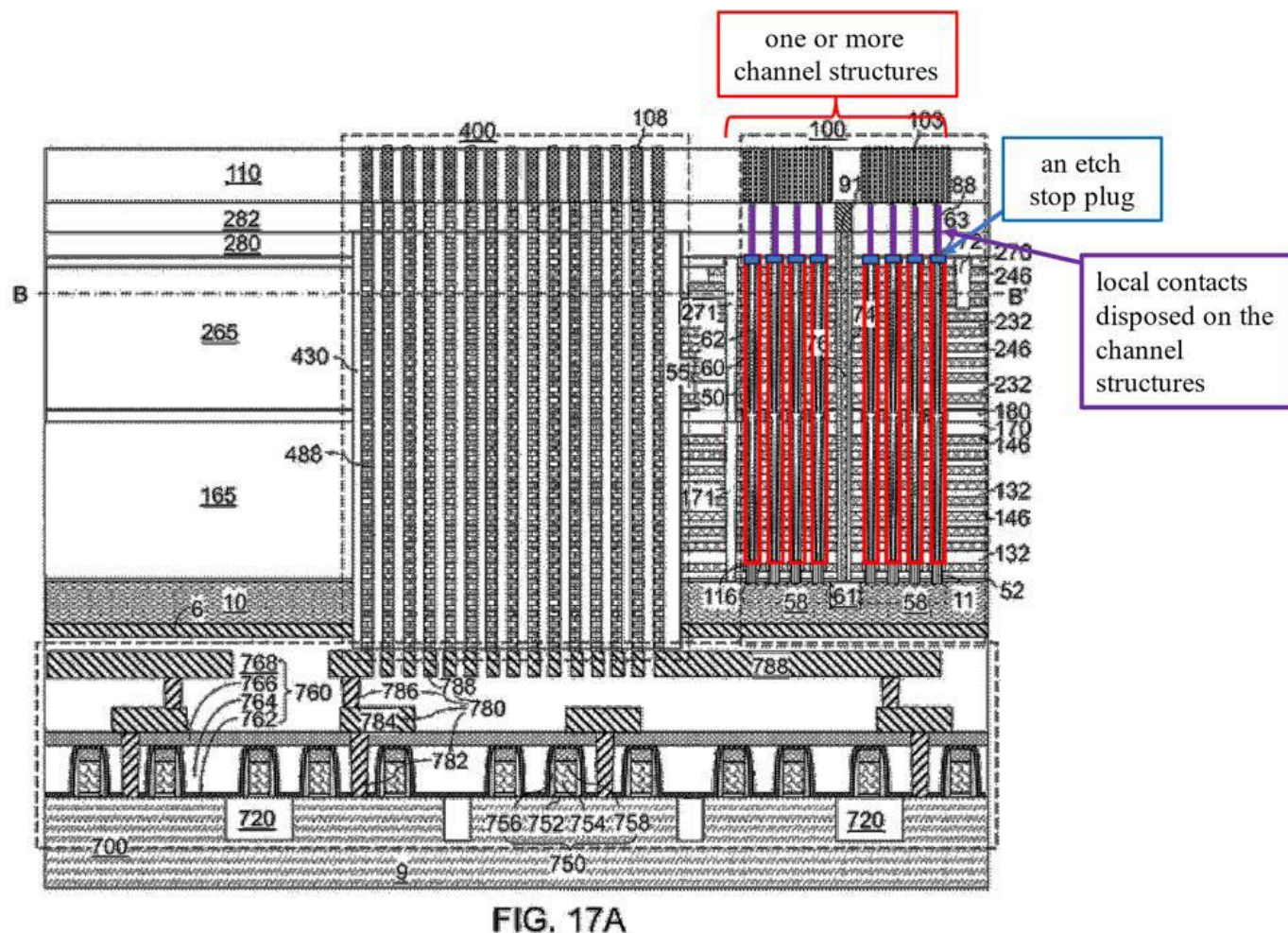
806-2 Petition at 125; 806-2 Lee-Reply ¶ 253.

- As previously explained, PO’s construction of the “etch stop plug” limitation is nonsensical and would exclude every disclosed embodiment.

See supra, slides 27-35 (Ground 1 > “Etch Stop Plug” Limitation > Claim Construction).

- Even under PO’s meritless construction, Toyama’s “bit lines 103” meet the “etch stop plugs” limitation for the same reason as PO contends “bit lines 250” the limitation.

See supra, slides 37-40 (Ground 1 > “Etch Stop Plug” Limitation > Obviousness Under PO’s Construction).



Toyama Figure 17A (annotated).

'806 Patent, Independent Claim 8

8. A three-dimensional (3D) memory device, comprising:

- an alternating conductor/dielectric layer stack;
- a dielectric structure extending vertically through the alternating conductor/dielectric layer stack;
- first and second channel regions comprising first and second pluralities of channel structures, respectively;
- slit structures extending vertically through the alternating conductor/dielectric layer stack;
- a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;
- local contacts disposed on the first and second channel structures and the slit structures;
- a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and
- a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.

'806 Patent, Dependent Claims 9-12

9. The 3D memory device of claim 8, wherein the dielectric structure abuts a sidewall of each TAC of the TACs.

10. The 3D memory device of claim 8, further comprising:
a substrate;
an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and
an epitaxial layer disposed between the substrate and the first or second channel structures.

11. The 3D memory device of claim 8, wherein the dielectric material comprises silicon oxide.

12. The 3D memory device of claim 8, wherein the TACs comprise a conductive material.