

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner.

IPR2024-00911
Patent 10,937,806 B2

Before JO-ANNE M. KOKOSKI, KIMBERLY McGRAW, and
MICHAEL T. CYGAN, *Administrative Patent Judges*.

McGRAW, *Administrative Patent Judge*.

JUDGMENT
Final Written Decision
Determining No Challenged Claim Unpatentable
35 U.S.C. § 318; 37 C.F.R. § 42.64

I. INTRODUCTION

Micron Technology, Inc. (“Petitioner”) filed a Petition to institute an *inter partes* review of claim 10 of U.S. Patent No. 10,937,806 B2 (“the ’806 patent,” Ex. 1001). Paper 1 (“Pet.”). Petitioner also filed a paper explaining why it filed multiple petitions challenging the ’806 patent and ranking the petitions. Paper 3 (“Ranking”); *see also Micron Technology, Inc. v. Yangtze Memory Technologies Co., Ltd.*, IPR2024-00791, Paper 1 (“791-Petition”)(challenging claims 8, 9, 11, and 12 of the ’806 patent). Yangtze Memory Technologies Company, Ltd. (“Patent Owner”) filed a Preliminary Response. Paper 10 (“Prelim. Resp.”). With prior approval from the Board, Petitioner filed a Preliminary Reply brief to address claim construction issues (Paper 9, “Prelim. Reply”), to which Patent Owner filed a Preliminary Sur-reply (Paper 11, “Prelim. Sur-reply”).

On November 27, 2024 we instituted an *inter partes* review of the claims challenged in the 791-Petition. *See Micron Technology, Inc. v. Yangtze Memory Technologies Co., Ltd.*, IPR2024-00791, Paper 11 (PTAB Nov. 27, 2024). On January 7, 2025, we instituted an *inter partes* review of the challenged claim based on all arguments identified in the present Petition. Paper 12 (“Inst. Dec.” or “Institution Decision”). Patent Owner filed a Response to the Petition (Paper 15, “PO Resp.”), Petitioner filed a Reply (Paper 17, “Reply”), and Patent Owner filed a Sur-reply (Paper 22, “Sur-reply”). We held a consolidated oral hearing for this proceeding and IPR2024-00791 on September 4, 2025, and a transcript of the hearing has been entered into the record. Paper 29 (“Tr.”). On November 24, 2025, a Good Cause Extension was issued in IPR2024-00791 to permit alignment with the schedule in this proceeding.

We have jurisdiction under 35 U.S.C. § 6. We issue this Final Written Decision pursuant to 35 U.S.C. § 318(a). Concurrently with this Decision, we issue a Final Written Decision in IPR2024-00791 (Ex. 3001) determining that none of the claims of the '806 patent challenged in that proceeding were shown to be unpatentable. Based on the record before us, we conclude that Petitioner has not shown by a preponderance of the evidence that claim 10 of the '806 patent is unpatentable.

A. Real Parties in Interest

Petitioner identifies itself and its subsidiaries, including Micron Consumer Products Group LLC, as the real parties in interest. Pet. 5. Patent Owner identifies itself as the real party in interest. Paper 4 (Mandatory Notice), 2.

B. Related Matters

The parties state that the '806 patent is asserted in *Yangtze Memory Techs. Co., Ltd. v. Micron Tech. Inc.*, Case No. 3:23-cv-05792-RFL (N.D. Cal.) (“the District Court Litigation”). Pet. 5; Paper 4, 2.

As noted above, claims 8, 9, 11, and 12 of the '806 patent are challenged in the 791-Petition. Claim 10, which is challenged in this proceeding, depends upon independent claim 8 challenged in the 791-IPR.

Petitioner also states it filed IPRs challenging other patents asserted in the District Court Litigation, namely U.S. Patent Nos. 10,950,623 (IPR2024-00794), 10,658,378 (IPR2024-00788, IPR2024-00909), 10,861,872 (IPR2024-00789, IPR2024-00910), 10,868,031 (IPR2024-00790), 11,501,822 (IPR2024-00795), 11,468,957 (IPR2024-00792), and 11,600,342 (IPR2024-00793, IPR2024-00912). Pet. 5–6.

C. The '806 Patent

The '806 patent, titled “Through Array Contact (TAC) for Three-Dimensional Memory Devices” relates to “a channel hole plug structure of three-dimensional (3D) memory devices and a method for forming the same.” Ex. 1001, code (54), 1:18–20. An embodiment of the 3D memory device is illustrated in Figure 2 of the '806 patent and is reproduced below.

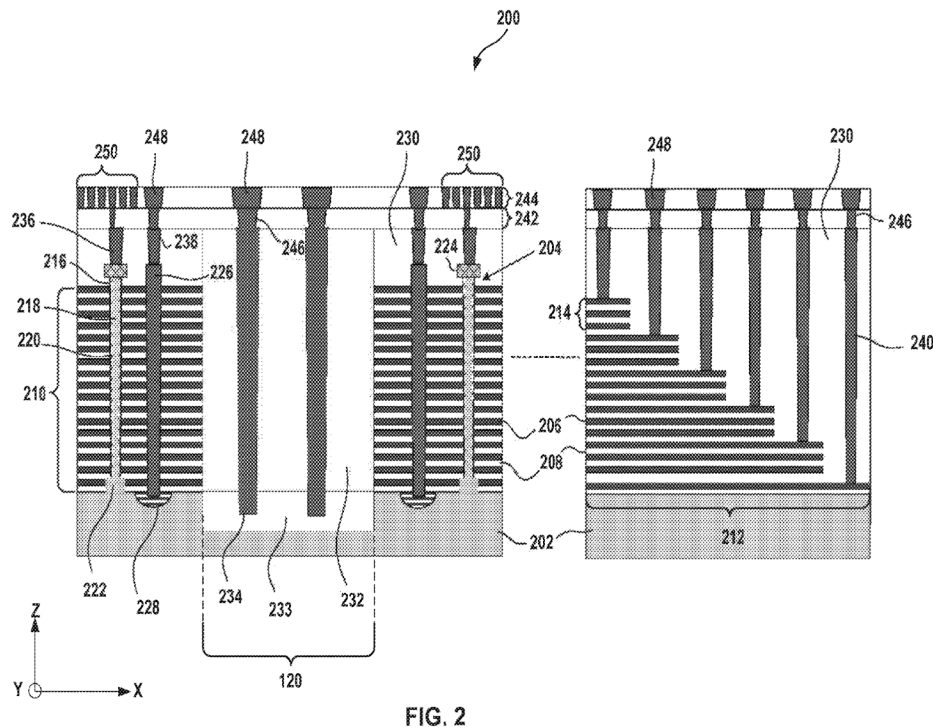


Figure 2 “is a cross-sectional view of an exemplary 3D memory device 200” disclosed in the '806 patent. Ex. 1001, 3:41–42.

Memory device 200 can be a “NAND Flash memory device^[1] in which memory cells are provided in the form of an array of NAND strings

¹ Though not explicitly defined in the specification, Petitioner’s declarant states that “[t]he acronym ‘NAND’ refers to a ‘not-AND’ logic gate, and NAND flash memory is a particular type of flash memory where the memory cells form a structure similar to that of a NAND gate.” Ex. 1003 ¶ 43.

204 extending vertically above substrate 202.” *Id.* at 8:17–20. “The array device can include a plurality of NAND strings 204 that extend through a plurality of conductor layer 206 and dielectric layer 208 pairs” that alternate in the vertical direction, also referred to as “‘alternating conductor/dielectric stack’ 210.” *Id.* at 8:20–31. Alternating conductor/dielectric stack 210 can include staircase structure 212, where each “level” or “step” 214 can include one or more conductor/dielectric layer pairs stacked. *Id.* at 8:54–59. “The top layer in each level 214 of staircase structure 212 is a conductor layer 206 available for interconnection in the vertical direction (e.g., along the z-axis).” *Id.* at 8:61–63. Figure 2 also shows “channel structure 216 that extends through alternating conductor/dielectric stack 210” that is filled with semiconductor materials and dielectric materials. *Id.* at 9:7–12. The embodiment illustrated in Figure 2 also includes slit structures 226 that also extend through alternating conductor/dielectric stack 210 and may extend along the y-axis to separate alternating conductor/dielectric stack into multiple blocks. *Id.* at 9:54–58.

Figure 2 also illustrates through array contacts (“TACs”) 234, extending vertically through dielectric structure 232, which are within a TAC region 120 that can have, but are not limited to, a rectangle or square shape. *Id.* at 10:55–64. “TACs 234 can carry electrical signals from and/or to 3D memory device 200” and “can provide electrical connections between the 3D memory device 200 and the peripheral device.” *Id.* at 11:8–14.

D. Illustrative Claim

Petitioner challenges dependent claim 10 in this proceeding. Claim 10 depends upon independent claim 8, which is challenged in IPR2024-00791. Claims 8 and 10 are reproduced below.

8. [1.PRE] A three-dimensional (3D) memory device, comprising:

- [8.A] an alternating conductor/dielectric layer stack;
- [8.B.i] a dielectric structure [8.B.ii] extending vertically through the alternating conductor/dielectric layer stack;
- [8.C] first and second channel regions comprising first and second pluralities of channel structures, respectively;
- [8.D] slit structures extending vertically through the alternating conductor/dielectric layer stack;
- [8.E] a staircase structure disposed in the alternating conductor/dielectric layer stack, wherein the staircase structure comprises levels with each level having a conductor layer thereon;
- [8.F] local contacts disposed on the first and second channel structures and the slit structures;
- [8.G] a through array contact (TAC) region formed between the first and second channel regions, wherein the TAC region comprises a plurality of through array contacts (TACs) extending vertically through the dielectric structure; and
- [8.H] a plurality of non-electrically functional channel structures surrounding the TAC region and between the first and second channel regions.

Ex. 1001, 23:54–24:8 (bracketed material added).

10. [10.PRE] The 3D memory device of claim 8, further comprising:

- [10.A] a substrate;
- [10.B] an etch stop plug interposed between each local contact of the local contacts and each channel structure of the first and second channel structures; and
- [10.C] an epitaxial layer disposed between the substrate and the first or second channel structures.

Id. at 24:13–20 (bracketed material added).

E. Asserted Ground

Petitioner asserts that claim 10 would have been unpatentable on the following ground:

Claim Challenged	35 U.S.C. §	Reference(s)/Basis
10	103 ²	Toyama ³

Pet. 15⁴. Petitioner states that it maintains the same three alternative arguments that independent claim 8 would have been obvious over various embodiments of Toyama that it presented in the 791-IPR and presents additional arguments and evidence that claim 10, which depends from claim 8, would have been obvious over those embodiments addressed in the 791-IPR. Pet. 1, 27–61 (alternative argument 1 relying on Toyama’s Second Modification), 61–100 (alternative argument 2 relying on Toyama’s First Exemplary Structure), 101–125 (alternative argument 3 relying on Toyama’s First Exemplary Structure in combination with the Second Modification).

Petitioner relies on the Declaration of Jack C. Lee, Ph. D. (Ex. 1003) and the Reply Declaration of Jack C. Lee, Ph.D. (Ex. 1043) in support of its

² The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112–29, 125 Stat. 284 (2011), revised 35 U.S.C. §§ 102 and 103 effective March 16, 2013. Because the ’806 patent has an effective filing date after March 16, 2013 (Ex. 1001, codes (22), (63)), we refer to the AIA version of Sections 102 and 103.

³ Toyama, US Pub. No. 2017/0179026 A1, published June 22, 2017 (Ex. 1005).

⁴ Petitioner characterizes its alternative arguments of unpatentability of claim 10 as based on three “grounds.” *See* Pet. 15. Because each of Petitioner’s arguments are based on the same reference, albeit different embodiments, we characterize Petitioner’s challenges as three alternative arguments based on a single ground because each argument relies on the same reference.

contentions. Patent Owner relies on the Declaration of Woodward Yang Ph.D. (Ex. 2005). Transcripts of the depositions of Dr. Lee (Exs. 2006, 2010) and of Dr. Yang (Ex. 1044) have also been submitted into the record.

II. ANALYSIS

A. *Level of Ordinary Skill in the Art*

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had “a bachelor of science degree in electrical engineering or a similar discipline” with “2–3 years of professional experience working with (e.g., researching, designing, or teaching) NAND flash memory devices, or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience).” Pet. 26 (citing Ex. 1003 ¶¶ 35–39). Petitioner further contends that a “POSITA would also have been aware of and generally knowledgeable about semiconductor manufacturing and 3D NAND’s structure, its component parts, how it operates, and how it is controlled.” *Id.*

Patent Owner does not object to Petitioner’s proposed definition (PO Resp. 13), but Patent Owner’s declarant Dr. Yang provides a slightly different definition, stating a POSITA:

would have had at least a bachelor’s degree in electrical engineering, materials science, or a similar discipline, along with at least 2 years of professional experience in semiconductor fabrication process integration for memory devices or an equivalent level of knowledge and experience. For example, an advanced degree may replace some of the professional experience, or extensive experience may replace some of the educational requirements.

Ex. 2005 ¶ 43.

Petitioner’s proposed definition appears to be consistent with the cited prior art and the disclosure of the ’806 patent, and we adopt it for purposes

of this Decision. We note that our Decision would be the same under either definition of a POSITA.

B. Claim Construction

We construe claims challenged in an *inter partes* review proceeding, “using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. [§] 282(b),” including construing the claims “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b). Under this standard, claim terms are generally given their plain and ordinary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). Only those terms in controversy need to be construed, and only to the extent necessary to resolve the controversy. *Realtime Data LLC v. Iancu*, 912 F.3d 1348, 1375 (Fed. Cir. 2019).

In our Decision on Institution, we noted that the parties disputed construction of “each local contact” found in dependent claim 10, and “dielectric structure” recited in independent claim 8. Inst. Dec. 8–9. We determine that no express construction of “each local contact” recited in claim 10, or any other claim term, is required to resolve the issues in dispute in this proceeding.

C. Obviousness over Toyama

Petitioner presents three alternative arguments that challenged claim 10 would have been obvious over Toyama. *See* Pet. 26–61 (alternative argument 1), 61–100 (alternative argument 2), 101–125 (alternative argument 3). For the following reasons, we determine that Petitioner has not

shown by a preponderance of the evidence that claim 10 would have been obvious over Toyama under any of the alternative arguments.

1. Toyama

Toyama is titled “Through-Memory-Level Via Structures for a Three-Dimensional Memory Device.” Ex. 1005, code (54). Toyama relates to three-dimensional NAND memory devices, such as vertical NAND strings, and describes four exemplary structures and modifications thereof. *Id.* ¶¶ 4, 14–155 (describing figures depicting first, second, third, and fourth exemplary structures as well as various modifications of those structures).

Embodiments of Toyama’s “first exemplary structure” are illustrated in Figures 1 through 17. *See* Ex. 1005 ¶¶ 14–49, 163–260, Figs. 1–17. Figure 15A is shown below. *Id.* ¶ 39.

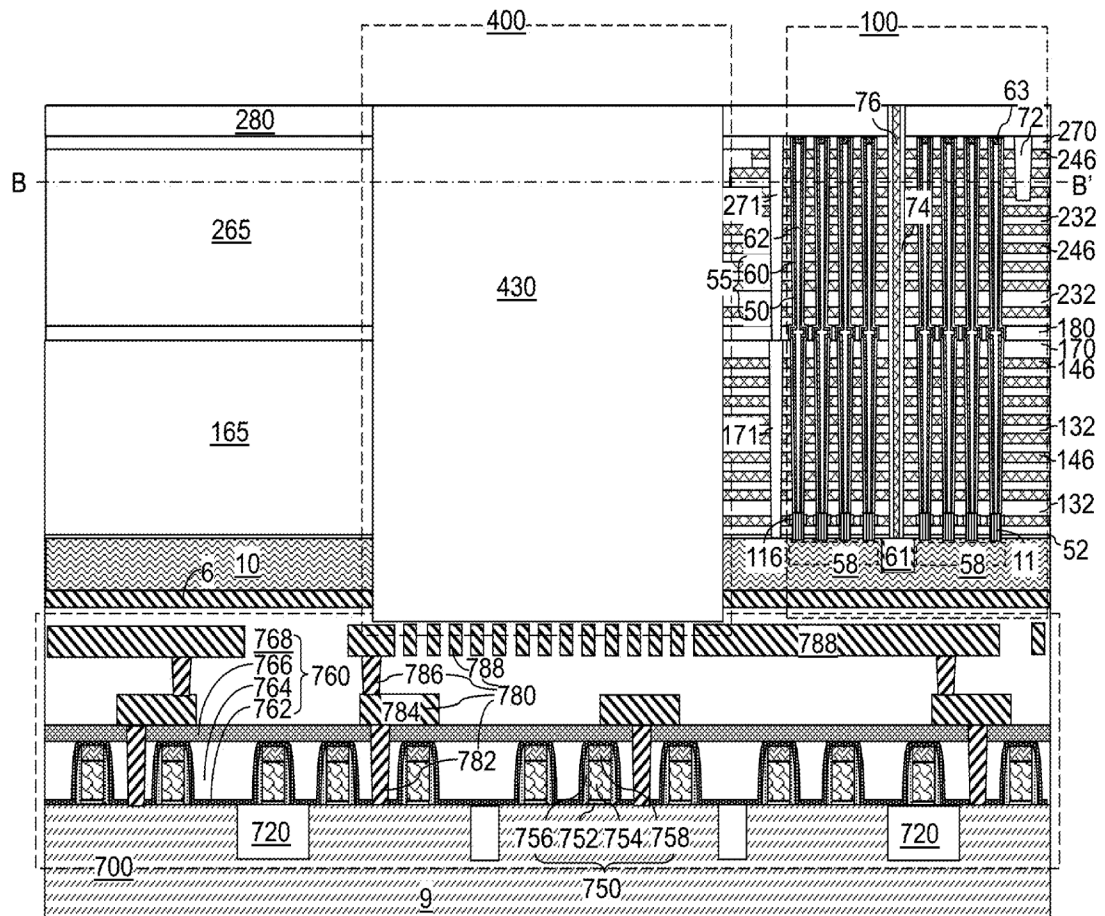


FIG. 15A

Figure 15A is a vertical cross-sectional view of the first exemplary structure of the first embodiment after formation of, *inter alia*, electrically conductive layers. Ex. 1005 ¶ 39.

At least one dielectric layer 760 is formed over the semiconductor devices, and lower level metal interconnect structures 780 formed thereon to function as landing pads for through-memory-level via structures. Ex. 1005 ¶ 164. Upon these structures in underlying peripheral region 700 (those having numbers in the 700s), a planar semiconductor layer 10 is formed. On semiconductor layer 10 is an alternating stack of conductive layers 146, 246

(replacing sacrificial material layers 142, 242) and insulating layers 132, 232. *Id.* ¶¶ 172, 196, 228. In portions of the alternating stack, supporting pillar structures 171 are formed, and other portions of the dielectric stack appear as a stepped region. *Id.* ¶ 182, Fig. 4B. In the stepped region, a through-memory-level opening 769 can extend from the top of the device down to the lower level metal interconnect structures 780 in peripheral region 700. *Id.* ¶ 213. A dielectric fill material portion 430 is formed within each through-memory-level opening 769. *Id.* ¶ 216.

Figures 17E and 17F illustrate an exemplary layout of the upper level metal interconnect structures. Ex. 1005 ¶ 251. In this embodiment, some upper level metal interconnect structures 108 are electrically coupled to the lower level metal interconnect structures 780 by the through-memory-level via structures 488 located in region 400 and are electrically coupled to the word lines 46 by the word line contact via structures 86 in region 200. *Id.*

Toyama also describes a “second modification of [a] fourth exemplary structure” (“Second Modification”) illustrated in Figures 44A through 49. Ex. 1005 ¶¶ 93–103. Figure 49 is shown below:

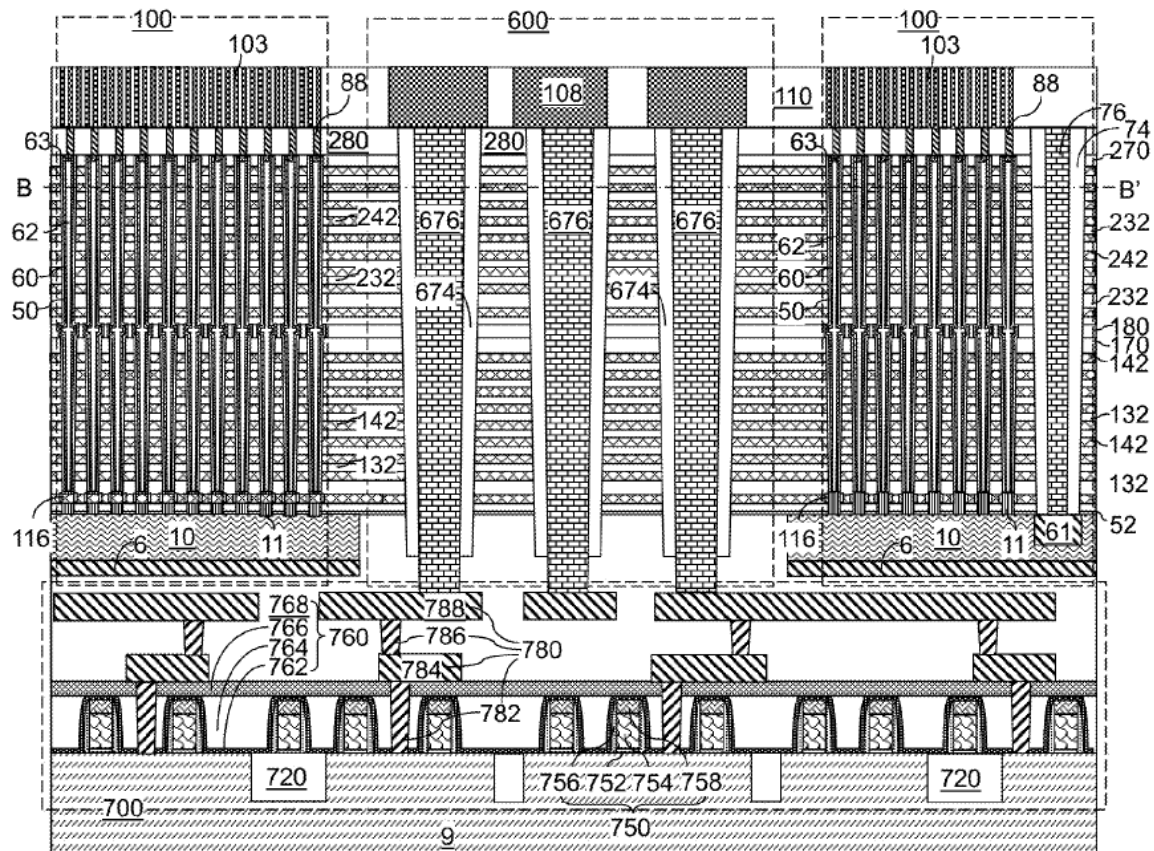


FIG. 49

Figure 49 is a vertical cross-sectional view of Toyama's second modification of its fourth exemplary structure after formation of upper level metal interconnect structures. Ex. 1005 ¶ 103. Figure 49 depicts semiconductor substrate 9 having peripheral region 700, upon which planar semiconductive layer 10 is formed having an alternating stack of conductive layers 146, 246 (replacing sacrificial material layers 142, 242) and insulating layers 132, 232. *Id.* ¶¶ 310–311, 332. Multiple through-memory-level openings 676, surrounded by insulating liners 674, are created within the alternating stack. *Id.* ¶¶ 339–341.

2. *Asserted Obviousness of Claim 10 over Toyama*

Petitioner presents three arguments that claim 10, which depends from claim 8, would have been obvious over Toyama. Pet. 26–125. Patent

Owner opposes. For each of these arguments, Petitioner asserts that independent claim 8 would have been obvious for the reasons set forth in its petition in the 791-IPR. *See id.* at 1 (stating the present Petition maintains the same grounds set forth in IPR2024-00791). As explained in our Final Written Decision (Ex. 3001) in the 791-IPR issued concurrently, Petitioner did not show by a preponderance of the evidence that independent claim 8 would have been obvious over Toyama under any of Petitioner’s three alternative arguments.

None of Petitioner’s arguments set forth in the present Petition, including the arguments directed to claim 10, remedy the deficiencies regarding its base claim 8. *See* Pet. 53–31, 98–101, 124–125; *see also* Reply. Accordingly, for the same reasons set forth in the Final Written Decision in the 791-IPR issued concurrently, Petitioner has not shown by a preponderance of the evidence that independent claim 8, and therefore dependent claim 10, would have been obvious over Toyama. *See In re Fine*, 837 F.2d 1071, 1076 (Fed. Cir. 1988) (“Dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious.”); Ex. 3001.

III. CONCLUSION

After reviewing the record and weighing the evidence offered by both parties, we determine that Petitioner fails to show, by a preponderance of the evidence, that claim 10 of the ’806 patent is unpatentable.

Claim	35 U.S.C. §	Reference(s)/ Basis	Claims Shown Unpatentable	Claims Not Shown Unpatentable
10	103	Toyama		10

IV. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that Petitioner has not established by a preponderance of the evidence that claim 10 of the '806 patent is unpatentable;
and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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