

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
Petitioner

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,
Patent Owner

Case No.: IPR2024-00912
U.S. Patent No. 11,600,342
Issue Date: March 7, 2023

Title: METHOD FOR READING THREE-DIMENSIONAL FLASH MEMORY

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 11,600,342
PURSUANT TO 35 U.S.C. §§311-319 AND 37 C.F.R. §42**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	MANDATORY NOTICES	5
A.	Real Party-in-Interest	5
B.	Related Matters.....	5
C.	Counsel, Service, and Fee Information	6
III.	REQUIREMENTS FOR IPR.....	8
A.	Grounds for Standing	8
B.	Identification of Challenged Claims and Statement of Precise Relief Requested	8
IV.	INSTITUTION SHOULD BE GRANTED	9
A.	There Are No Grounds for a §314 Discretionary Denial.....	9
1.	Possibility of a Stay	10
2.	Proximity of the Court’s Trial Date.....	10
3.	Investment in the Parallel Proceeding	10
4.	Issue Overlap.....	11
5.	Party Overlap	12
6.	Other Circumstances	12
B.	Denial Under §325(d) Would Be Inappropriate.....	12
V.	THE ’342 PATENT	13
A.	Technology Background	13
1.	NAND Flash Structure.....	13
2.	3D NAND Flash Operation	17

B.	Overview of the Patent.....	22
C.	Prosecution History	26
VI.	CLAIM CONSTRUCTION.....	27
VII.	LEVEL OF ORDINARY SKILL IN THE ART	28
VIII.	PRIOR ART OVERVIEW	29
A.	Seo	29
B.	Nam	31
C.	Choi	32
IX.	THE '342 PATENT'S CLAIMS ARE OBVIOUS.....	35
A.	<i>Ground 1</i> : Claim 7 Is Obvious Over Seo in View of Choi.....	35
1.	Claim 1	35
2.	Claim 7	45
3.	Motivation to Combine	50
B.	<i>Ground 2</i> : Claim 7 Is Obvious Over Nam in View of Choi.....	53
1.	Explanation of Figures	53
2.	Claim 1	56
3.	Claim 7	68
4.	Motivation to Combine	71
X.	SECONDARY CONSIDERATIONS	73
XI.	CONCLUSION	73

TABLE OF AUTHORITIES

	Page(s)
 Cases	
<i>Apple Inc. v. Fintiv, Inc.</i> , Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020).....	9, 10, 11
<i>Geo. M. Martin Co. v. All. Mach. Sys. Int’l LLC</i> , 618 F.3d 1294 (Fed. Cir. 2010)	49, 71
<i>Nanya Tech. Corp. v. Lone Star Silicon Innovations, LLC</i> , IPR2018-00062, Paper 7 (PTAB Apr. 25, 2018)	33
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005) (<i>en banc</i>)	27
<i>Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC</i> , IPR2019-01393, Paper 24 (PTAB June 16, 2020)	10, 11
<i>Unwired Planet, LLC v. Google Inc.</i> , 841 F.3d 995 (Fed. Cir. 2016)	48, 71
<i>Yangtze Memory Technologies Co., Ltd. V. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL (N.D. Cal., filed Nov. 9, 2023)	5, 6, 11
 Statutes	
35 U.S.C. §102(a)	29, 31, 33
35 U.S.C. §314(a)	6
35 U.S.C. §325(d)	6, 12
 Other Authorities	
37 C.F.R. §42.10(b)	8
37 C.F.R. §42.108(a).....	6

LISTING OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 11,600,342 to Chen et al.
1002	File History of U.S. Patent No. 11,600,342 to Chen et al.
1003	Declaration of David Kuan-Yu Liu, Ph.D. (“Liu”)
1004	<i>Curriculum Vitae</i> of David Kuan-Yu Liu, Ph.D.
1005	U.S. Patent Publ. No. 2021/0027848 A1 to Seo (“Seo”)
1006	U.S. Patent Publ. No. 2015/0003169 A1 to Nam et al. (“Nam”)
1007	Choi et al., “Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory,” 2016 Symposium on VLSI Technology, Digest of Technical Papers, 78-79 (“Choi”)
1008	<i>Intentionally Omitted</i>
1009	Minute Order, Dkt. No. 42, dated February 22, 2024 in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1010	Combined Civil and Criminal Federal Court Management Statistics (December 31, 2023), available at https://www.uscourts.gov/sites/default/files/data_tables/fcms_na_distcomparison1231.2023.pdf
1011	Docket from <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1012	U.S. Patent No. 9,589,978 to Yip
1013	Aritome, “NAND Flash Memory Technologies” (2016)
1014	Silvagni, “3D NAND Flash Based on Planar Cells,” Computers 2017

Petition for *Inter Partes* Review of U.S. Patent No. 11,600,342

Exhibit	Description
1015	U.S. Patent Publ. No. 2020/0168276 A1 to Yang
1016	U.S. Patent No. 9,620,233 to Dong et al.
1017	Michelsoni, “3D Flash Memories” (2016)
1018	U.S Patent No. 10,276,251 B1 to Lobana et al.
1019	U.S Patent No. 9,361,993 B1 to Chen et al.
1020	Affidavit of Nathaniel E. Frank-White (Internet Archive) re Choi Reference (Ex. 1007)
1021	Declaration of Gordon MacPherson (IEEE) re Choi Reference (Ex. 1007)
1022	Certified File History of U.S. Patent No. 10,403,637 to Lue
1023	Wu et al., “Multiscale simulation of lateral charge loss in Si ₃ N ₄ 3D NAND flash based on density functional theory,” Journal of Physics D: Applied Physics, vol. 52, no. 39, 395103, 2019
1024	U.S. Patent Publ. No. 2019/0198117 A1 to Yu et al.
1025	U.S. Patent No. 10,121,529 B2 to Lee
1026	Michelsoni et al., “Inside Solid State Drives (SSDs)” (2 nd Ed. 2018)
1027	U.S. Patent Publ. No. 2020/0395372 A1 to Seo et al.
1028	U.S. Patent Publ. No. 2019/0348122 A1 to Ko et al.
1029	U.S. Patent Publ. No. 2016/0293271 A1 to Won et al.
1030	U.S. Patent No. 8,873,288 to Sharon et al.
1031	U.S. Patent Publ. No. 2016/0300620 A1 to Dutta et al.
1032	U.S. Patent No. 10,438,671 to Chen et al.
1033	U.S. Patent Publ. No. 2016/0372185 A1 to Shim et al.

Exhibit	Description
1034	U.S. Pat. No. 8,400,839 to Li
1035	Complaint for Patent Infringement, Dkt. No. 1, filed Nov. 9, 2023, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1036	First Amended Complaint for Patent Infringement, Dkt. No. 29, filed Feb. 2, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL
1037	Plaintiff and Counterclaim Defendant Yangtze Memory Technologies Company, Ltd.’s Disclosure of Asserted Claims and Infringement Contentions, dated May 6, 2024, in <i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc. and Micron Consumer Products Group, LLC</i> , Case No. 3:23-cv-05792-RFL

I. INTRODUCTION

Petitioner Micron Technology, Inc. (“Petitioner”) respectfully requests *inter partes* review of claim 7 (the “Challenged Claim”) of U.S. Patent No. 11,600,342 (the “’342 patent”) assigned to Yangtze Memory Technologies Co., Ltd (“Patent Owner” or “PO”). There is more than a reasonable likelihood that Petitioner will prevail with respect to the Challenged Claim. Micron previously filed IPR2024-00793, which challenges other claims of the ’342 patent. *See* §II.B. Concurrently filed herewith, Micron’s Explanation for and Ranking of Two Petitions explains the basis for filing this second Petition. Challenged Claim 7 depends from claim 1. This Petition relies on Grounds 1 and 3 from IPR2024-00793 and the knowledge of a POSITA to demonstrate that the elements of claim 7 are disclosed or rendered obvious.

The ’342 patent relates to a charge-trap 3D NAND memory device. The ’342 patent purports to address a fast-charge loss problem. Fast-charge loss involves—over time—the escape of shallowly-trapped particles from the charge-trap layer of a memory cell. Because of fast-charge loss, a read operation after a program operation may produce different results depending on *when* the read operation occurs. The ’342 patent purports to address this problem by removing fast charges during a “read-prepare” period before a read. Specifically, as shown below, the ’342 patent teaches (1) applying a voltage on an unselected word line, (2) grounding the selected

word line, and (3) applying a voltage on an unselected string. The '342 patent alleges that this creates an electrical field that causes the fast charges to de-trap. The Examiner allowed the claims because of (1) above.

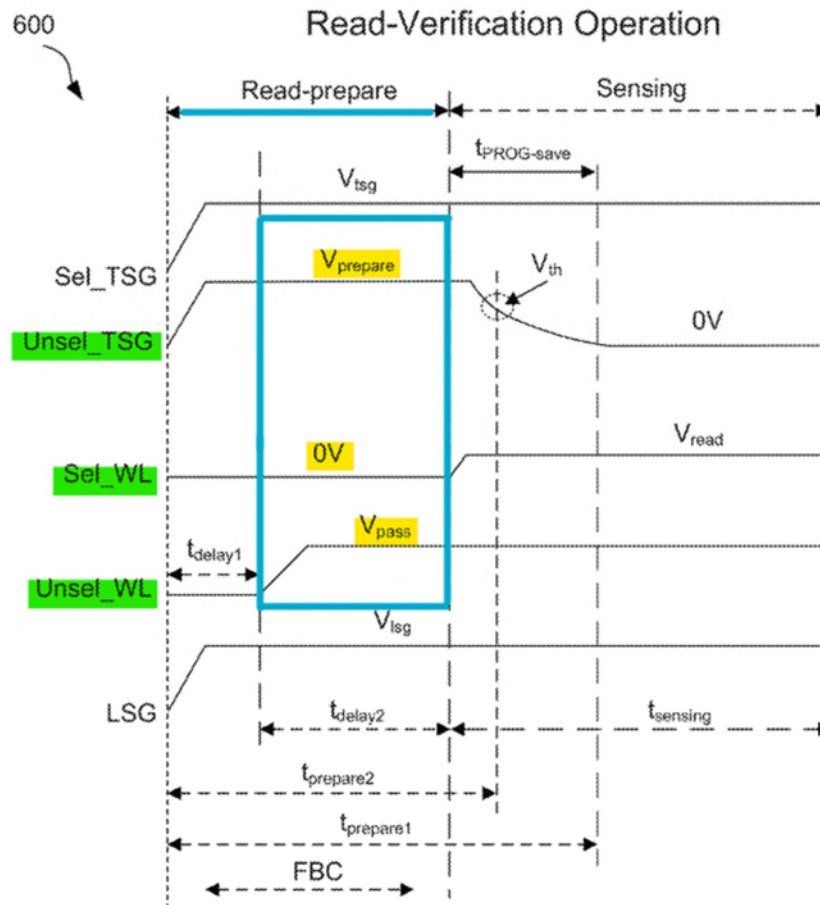


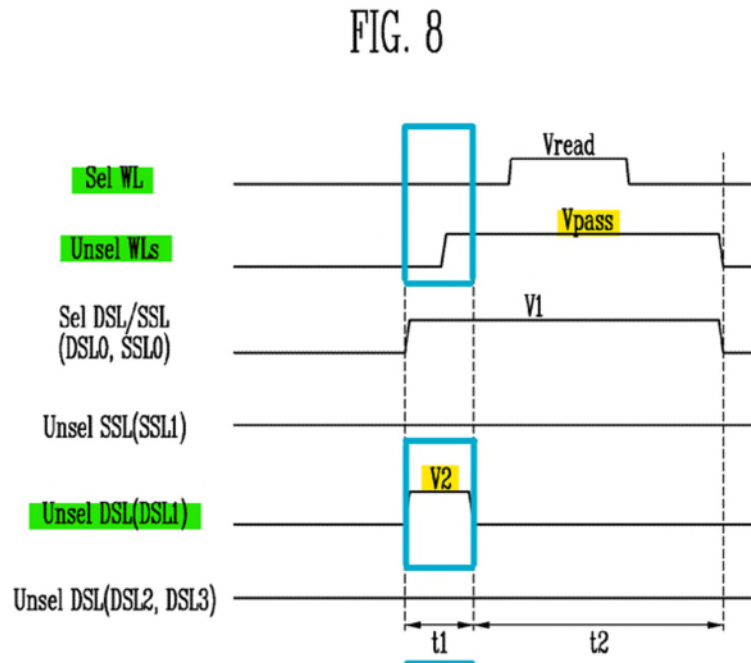
Fig. 6

Ex. 1001, FIG. 6 (annotated).

The Petition focuses on three references: Seo, Nam, and Choi. Seo and Nam disclose the heart of the '342 patent: the creation of an electrical field during a pre-

read period. Choi explains that this electric field removes fast charges. These references were not cited or discussed during prosecution.

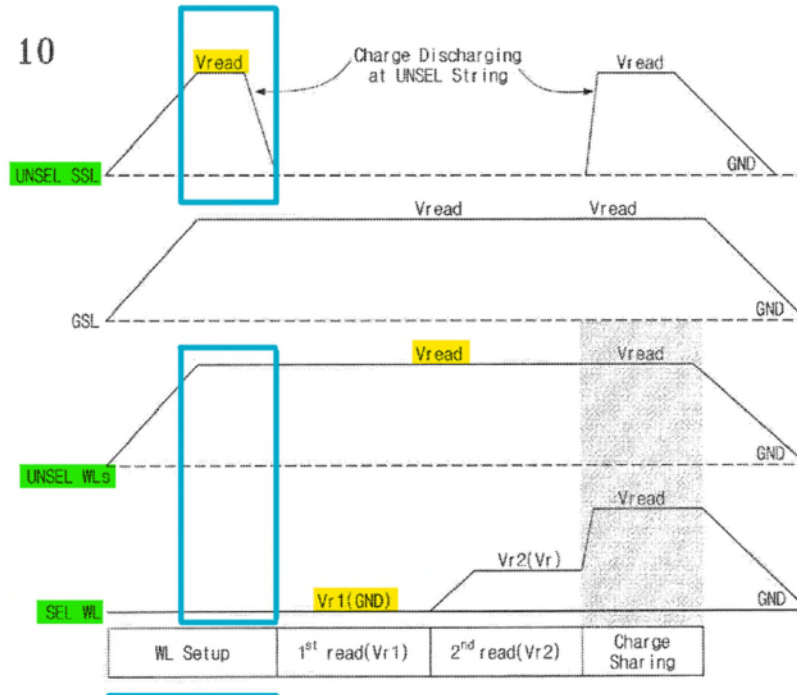
Just like the '342 patent, Seo creates an electric field before a read operation using the unselected word lines, selected word line, and unselected string:



Seo, FIG. 8 (annotated).

Nam discloses the same:

Fig. 10



Nam, FIG. 10 (annotated).

Choi teaches what removes fast charges: “a large lateral electric field.” Choi, 2:16-18. To the extent PO argues that a reference must expressly describe fast-charge removal (which is incorrect), this Petition combines each of Seo and Nam with Choi.

Challenged claim 7 requires that “a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell” “when” “applying the read voltage during the second time period.” Ex. 1001, 15:23-37. The “when” condition corresponds to when the sensing (or read) operation occurs. And when this condition occurs, the “voltage of the unselected top select gate” is typically zero (as in the prior art herein). Thus, all that claim 7 effectively adds is that an unselected

cell, i.e., an erased or programmed cell, has a zero threshold voltage at this time. While it is more common that an erased cell has a negative threshold voltage, an erased cell with a zero threshold voltage was well known in the prior art. Moreover, using such a threshold voltage on an erased cell was a simple design choice among a finite number of choices. This is because the selection of the erase threshold voltage must be within the finite threshold window of the memory cell.

Petitioner requests that the Board institute trial and find the Challenged Claim unpatentable as obvious under §103.

II. MANDATORY NOTICES

A. Real Party-in-Interest

Petitioner Micron Technology, Inc. and its subsidiaries, including Micron Consumer Products Group LLC, are the real parties-in-interest.

B. Related Matters

According to USPTO assignment records, the '342 patent is currently assigned to Yangtze Memory Technologies, Co., Ltd. ("YMTC" or "Patent Owner"). YMTC has asserted the '342 patent and U.S. Patent Nos. 10,658,378, 10,861,872, 10,868,031, 10,937,806, 10,950,623, 11,468,957, and 11,501,822 in a co-pending litigation, *Yangtze Memory Technologies Co., Ltd. V. Micron Technology, Inc. and Micron Consumer Products Group, LLC*, Case No. 3:23-cv-05792-RFL (N.D. Cal., filed Nov. 9, 2023) ("Co-Pending Litigation").

Petition for *Inter Partes* Review of U.S. Patent No. 11,600,342

In addition to this Petition, Petitioner is filing (or has filed) petitions for *inter partes* review of each asserted patent in the Co-Pending Litigation.

Patent	PTAB Proceeding	Wave 1/Wave 2
10,658,378 (claims 15-17 and 19-20)	IPR2024-00788	Wave 1 Petitions
10,861,872 (claims 1-6 and 11-13)	IPR2024-00789	
10,868,031	IPR2024-00790	
10,937,806 (claims 8-9 and 11-12)	IPR2024-00791	
10,950,623	IPR2024-00794	
11,468,957	IPR2024-00792	
11,501,822	IPR2024-00795	
11,600,342 (claims 1-6 and 8-20)	IPR2024-00793	
10,658,378 (claims 1-7 & 18)	IPR2024-00909	Wave 2 Petitions
10,861,872 (claims 7-10)	IPR2024-00910	
10,937,806 (claim 10)	IPR2024-00911	
11,600,342 (claim 7)	IPR2024-00912	

The Director and the Board should allow this Petition under 35 U.S.C. §314(a), 35 U.S.C. §325(d), and/or 37 C.F.R. §42.108(a). Concurrently filed herewith, Micron’s Explanation for and Ranking of Two Petitions explains the basis for filing this second Petition challenging a different claim of the ’342 Patent.

C. Counsel, Service, and Fee Information

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ymtc_ohs@orrick.com. Pursuant to 37 C.F.R. §42.10(b), Petitioner's Power of Attorney is attached.

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

III. REQUIREMENTS FOR IPR

A. Grounds for Standing

Petitioner certifies that the '342 patent is available for IPR, and that Petitioner is not barred or estopped from requesting this IPR. Micron was served with a Complaint alleging infringement of the '342 patent on November 14, 2023.

B. Identification of Challenged Claims and Statement of Precise Relief Requested

This Petition assumes that the '342 patent is entitled to the earliest priority date that it lists: October 23, 2019.

Petitioner relies on the following references: (1) U.S. Publ. 2021/0027848A1 (Ex. 1005, "Seo"), (2) U.S. Publ. 2015/0003169A1 (Ex. 1006, "Nam"), and (3) *Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory*, 2016 Symposium on VLSI Technology, Digest of Technical Papers, 78-79 (Ex. 1007, "Choi"). These references are all prior art. *See* §VIII.

Petitioner challenges claim 7 on the following grounds:

Ground 1: Claim 7 is obvious over Seo in view of Choi and the knowledge of a POSITA; and

Ground 2: Claim 7 is obvious over Nam in view of Choi and the knowledge of a POSITA.

IV. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits. All other requirements for IPR have been met. The Board should institute IPR.

A. There Are No Grounds for a §314 Discretionary Denial

There is a pending district court action involving the '342 Patent. The PTAB has explained that it “will not ... discretionarily deny institution in view of a parallel district court litigation where a petition presents compelling evidence of unpatentability.” 6/21/22 Interim Procedure, 2, 4-5. Petitioner submits that it presents a compelling case here: claim 7 of the '342 Patent are unambiguously unpatentable.

Petitioner also notes that the factors considered by the Board when assessing whether to institute IPR in light of a parallel proceeding collectively weigh in favor of institution. *See Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) (precedential) (“*Fintiv*”). In particular: the district court may stay the case, any potential trial will occur after the deadline for a final written decision,

little district court work has occurred, petitioner diligently prepared this petition, and the petition is substantively strong.

1. Possibility of a Stay

Petitioner intends to seek a stay if the Board institutes IPR. Until this issue is adjudicated, any attempt to predict the outcome would require speculation. This factor is neutral. *See Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (PTAB June 16, 2020) (informative) (“*Sand Revolution*”); *Fintiv* at 12 (similar).

2. Proximity of the Court’s Trial Date

On February 22, 2024, the district court entered a scheduling order which set a trial date of December 1, 2025. *See* Ex. 1009. As a result, if IPR proceedings are instituted, they should be completed well before the scheduled trial date. *See also* Ex. 1010 (statistics indicating that it takes on average 48.9 months to reach trial in district). This weighs strongly in favor of institution.

3. Investment in the Parallel Proceeding

To date, the parties and the district court have invested very little in the parallel proceeding. Indeed, beyond engaging in some motion practice regarding the pleadings, no substantive progress has been made. The parties are over a month away from completing the exchange of contentions and have not taken any depositions. Fact discovery is in its infancy. No claim construction positions have been exchanged, no claim construction order has issued, no infringement or

invalidity expert discovery has occurred, and no summary judgment motions have been filed. This weighs in favor of institution. *See Sand Revolution* at 11.

The Board also has explained that institution is appropriate where “the petitioner filed the petition expeditiously....” *Fintiv* at 11. Here, Patent Owner asserted eight different patents against Petitioner. Ex. 1011. Petitioner proceeded with diligence, filing eight petitions approximately six months after being served with the original complaint and approximately three months after the filing of an amended complaint. *Id.*, Exs. 1035-36. After Petitioner filed these eight petitions, Patent Owner asserted new claims against Petitioner in district court on May 6, 2024. Ex. 1037. Petitioner has filed petitions on these new claims—claims that Petitioner could not have foreseen would be asserted—within two weeks. This also weighs strongly in favor of institution.

4. Issue Overlap

The wave 1 and wave 2 Petitions challenge all asserted claims in the Co-Pending Litigation. Should the Board institute, Micron stipulates that it will not advance in District Court any invalidity defense that formed the basis of any of the grounds in this Petition. Micron submits that this eliminates any potential overlap in issues between the proceedings here and in District Court. The Board has found that such stipulations weigh in favor of institution. *Sand Revolution* at 11-12.

5. Party Overlap

Both Petitioner and Patent Owner are parties in the parallel proceeding. This, however, is of little moment as there is often party overlap when there is a parallel proceeding.

6. Other Circumstances

Here, Petitioner submits that its petition has significant substantive merit. It is premised on clear, understandable prior art that the Patent Office did not previously consider. Thus, this factor also weighs in favor of institution.

B. Denial Under §325(d) Would Be Inappropriate

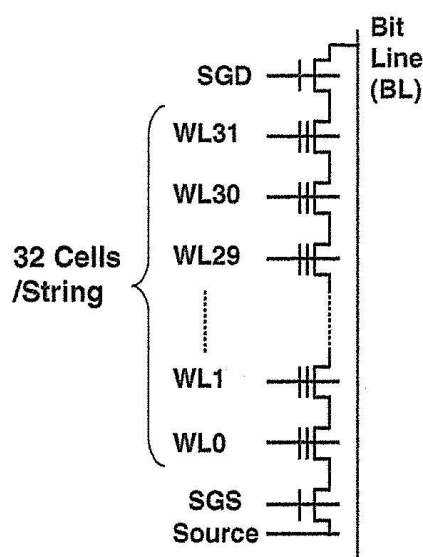
Neither Patent Owner nor the Examiner cited or discussed Seo, Nam, or Choi during prosecution of the '342 patent. *See generally* Ex. 1002. Further, these references present noncumulative invalidity arguments, because each discloses applying a voltage on the unselected word lines during a pre-read period, unlike the prior art on which the Examiner relied. §V.C.

V. THE '342 PATENT

A. Technology Background

1. NAND Flash Structure

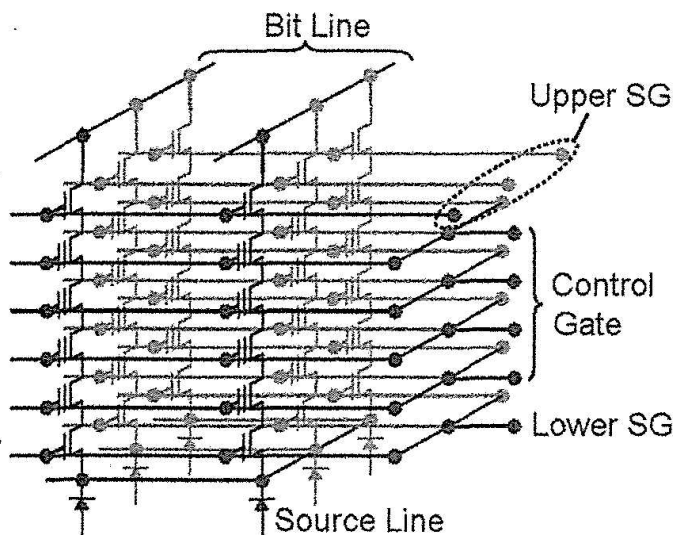
“Flash memory” is a form of “non-volatile memory.” Ex. 1012, 1:24-26; *see also* Ex. 1003 (“Liu”¹), ¶¶ 41-63. Flash memory cells, e.g., NAND cells, are arranged in “strings” with multiple cells “connected in series.” Ex. 1013, 38. The cells are surrounded by “select transistors (SGD, SGS),” one on the top (usually, drain side) and one on the bottom (usually, source side). *Id.*, 38-39. One such string is shown below:



Id., 39.

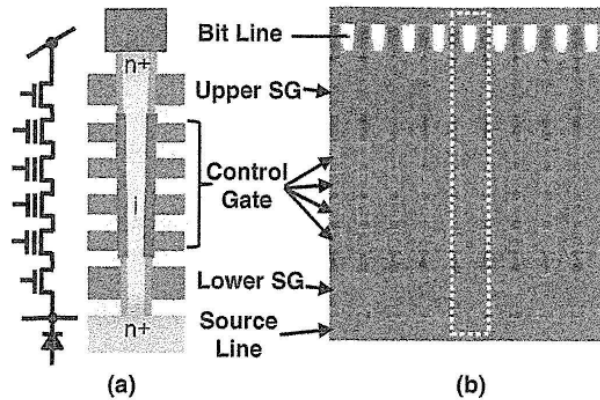
¹ David Kuan-Yu Liu, Ph.D. is a leading expert in the physics of read and interference issues in memories.

Early NAND devices were formed as two-dimensional arrays of cells on a substrate surface. Ex. 1013, 38. But “three-dimensional (3D) NAND flash cells” were developed. *Id.*, 292. 3D NAND structure is like “turning the 2D NAND string upside,” “resulting” in a “vertical channel.” Ex. 1014, 3. Memory cells (comprising transistors) are formed vertically by stacking alternating layers of metal and dielectric (e.g., oxide such as SiO₂) around a cylindrical pillar. Ex. 1013, 294-95. Each metal layer acts as the control gate (gate terminal) of a transistor. *Id.*, 295. Multiple such vertical pillars/channels are then repeated in a three-dimensional array:

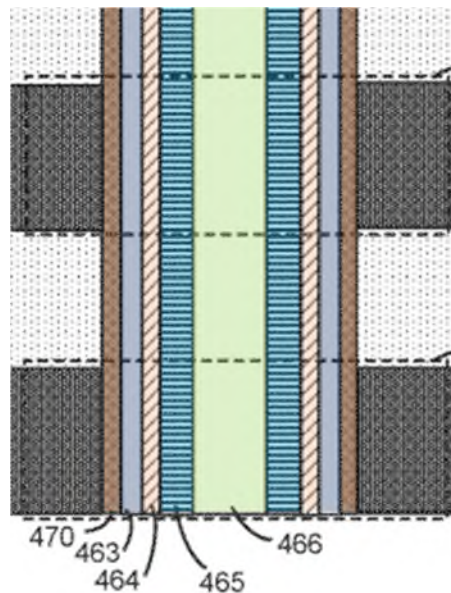


Id., 296. A particular vertical memory cell is selected using a word line and bit line, along with the select gates. *Id.*, 295-97.

An example 3D NAND vertical memory cell string with a charge-trapping layer is shown below:



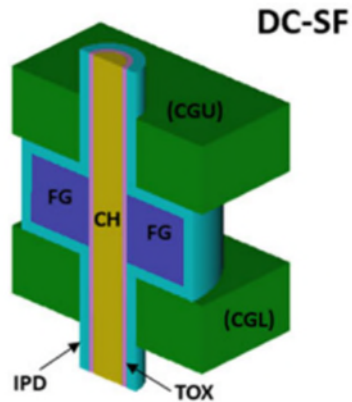
Ex. 1013, 296. The ONO (oxide-nitride-oxide) sidewall of a memory-string pillar can comprise an oxide blocking layer (e.g., 470 below), a nitride charge-trapping or storage layer (463), and an oxide tunneling layer (464). Ex. 1015, [0083], Ex. 1016, 13:19-26.



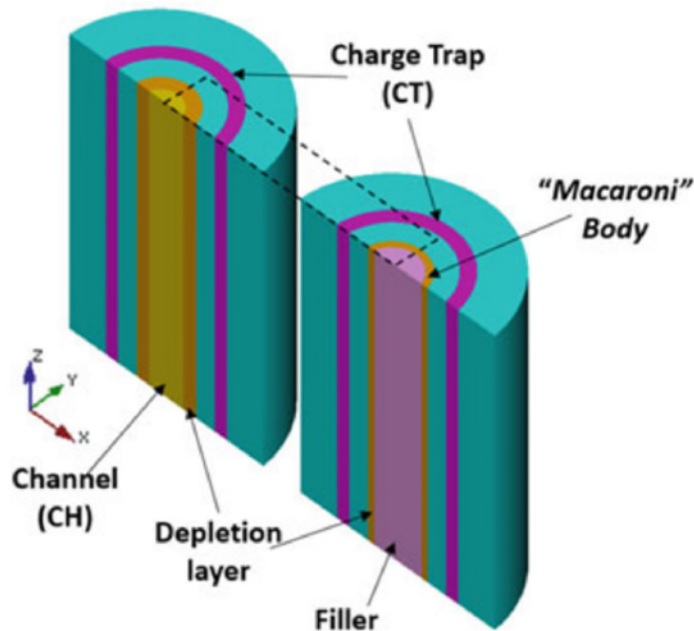
Ex. 1015, FIG. 4E (partial) (annotated).

The two most common types of 3D Flash memory cells are conductive floating gate memory cells and charge-trap memory cells. Because of the conductive

floating gates, the vertical memory string for this type is made with separated floating gates:



Ex. 1017, 145. Charge-trap technology, however, employs a non-conductive data storage portion, e.g., silicon nitride, and thus the charge-trap layer is not separated and merely extends through the entire vertical string:



Id., 106.

2. 3D NAND Flash Operation

A NAND memory cell stores charge in its charge-storage material, and the amount of charge that the cell stores corresponds to a threshold voltage (V_{th}). Ex. 1016, 13:43-49. There is a range of charge that such a cell can store, which gives rise to a corresponding range of threshold voltages. This range is known as the threshold voltage window. Ex. 1030, 1:61-2:5; Liu, ¶ 64 (establishing the same is true for both floating gate and charge-trap cells). This threshold voltage window typically spans a low negative and low positive voltage. Ex. 1013, 312; Liu, ¶ 64.

Within this threshold voltage window, the designer must arrange nonoverlapping data state windows (1) with each data state spanning a threshold distribution within the overall threshold voltage window and (2) with each data state corresponding to either the erased state or a particular data state. An example is shown below. Here, the “threshold window ... ranges from -2.5 V to 4 V.” Ex. 1034, 35:45-56. As can be seen, the erased state has a threshold distribution -2.5 to approximately -2 V.

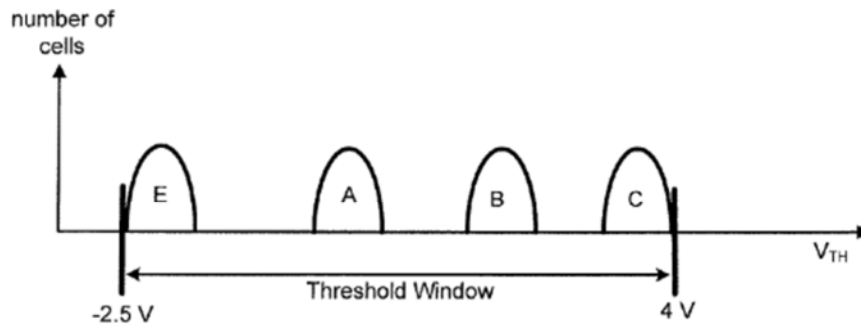
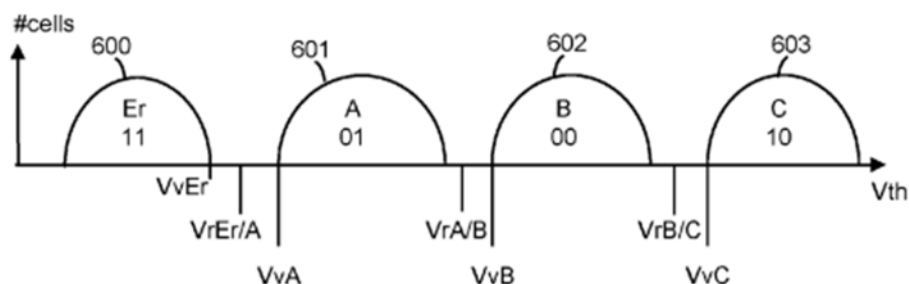


FIG. 36A

Ex. 1034, Fig. 36A, Liu, ¶ 65.

Programmed data states allow the device to distinguish the states from one another via read operations. For example, taking a threshold voltage window below (while this reference provides no specific values, along the horizontal axis, the threshold voltage increases from the lowest value to the highest value), the designer selects the data states (and corresponding threshold distributions) as shown below. Specifically, for a two-bit-per-cell memory device, there is an erased state E_r and programmed data states A, B, and C. The erase and program operations remove or inject charge into the memory cell to place the cell in the appropriate state, i.e., cause the memory cell to have the appropriate threshold voltage for the state. For example, an erase will cause the memory cell to have a threshold voltage within the E_r state shown below.



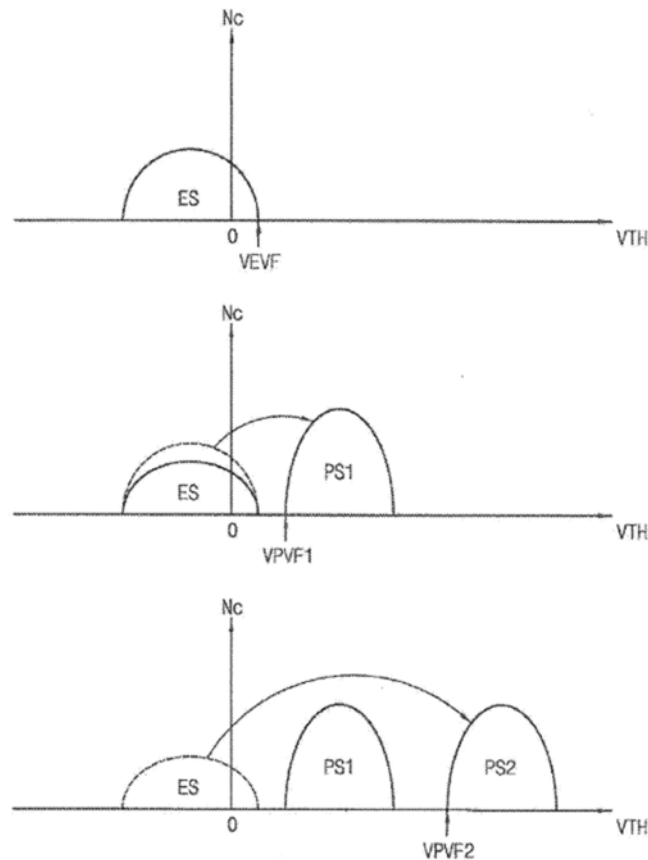
Ex. 1016, FIG. 6. A read (verify) operation, for example, reads the memory cell using a read voltage of $V_{rEr/A}$. That operation will determine whether the memory cell's threshold voltage is greater or less than $V_{rEr/A}$. If the memory cell's threshold voltage is less than $V_{rEr/A}$, the memory cell is in the erased state. Otherwise, the memory cell is either in the data state of A, B, or C. Subsequent reads (verifies) further distinguish the specific state. Liu, ¶ 66.

Note that in the immediately above example (Ex. 1016), the figure does not expressly state the voltage range of the threshold voltage window. And in both of the above examples (Ex. 1034 and Ex. 1016), the figures do not specify the voltage distribution values for the data states. This is because what is critical to the above read operation is that the individual voltage distributions do not overlap. Liu, ¶ 67.

While the threshold voltage of the erased state is typically a negative value (Ex. 1013, 312), the threshold voltage of the erased state may be zero. Indeed, well-known memory manufacturers employ such a state. For example, Hong-yan Chen, a SanDisk patent, describes a memory cell “in the erased state with $V_{th}=0$ V.” Ex.

1032, 20:21-22. By way of another example, Young-Seop Shim, a Samsung patent, discloses an erased state that includes a zero threshold voltage:

FIG. 6



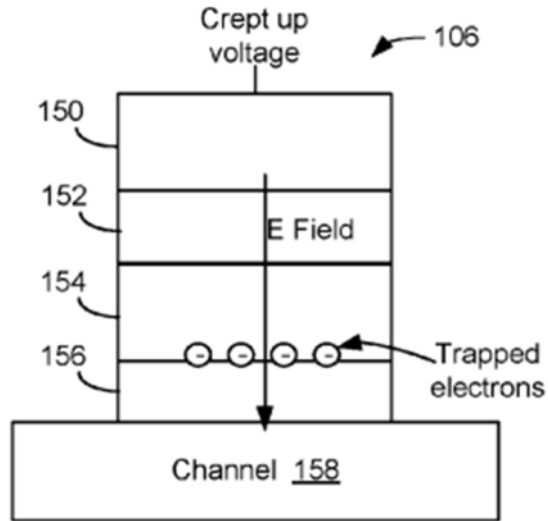
Ex. 1033, Fig. 6. Deepanshu Dutta, another SanDisk patent, discloses the same. Ex. 1031, [0090] (“In some embodiments, erased threshold voltage E is below zero volts. In other embodiments, *erased threshold voltage distribution E* is above zero volts, *or partially above zero volts.*”) (emphasis added). Note that “partially above zero volts,” as Deepanshu Dutta discloses, refers to the threshold voltage window for the erased state’s threshold voltage range including negative values, zero, and positive

values, as shown in Ex. 1033, Fig. 6, above. Liu, ¶ 68. As shown above, these data state windows are windows, i.e., a range of values, because programming a memory cell will result in a distribution of threshold voltage values within the window. Liu, ¶ 69. There is a finite number of choices in configuring the voltage ranges of these data state windows. Liu, ¶ 70.

During read operations, all cell transistors on a selected memory string except the selected cell to be read are given a pass voltage that is higher than the highest V_{th} of all possible data states. Ex. 1016, 3:21-27, 3:33-37. A read voltage between two data states is applied to the control gate of the selected cell to determine its state. *Id.*, 3:10-29, 9:66-10:15, 14:31-37; Liu, ¶ 71.

NAND device programming involves a cycle: a programming pulse, a read operation to verify programming success, and then if necessary, repeating the process until reaching the correct data state. Ex. 1018, 10:43-47; Ex. 1019, 11:50-52. This verify operation can be identical to the read operation described above (using a verify voltage). Ex. 1018, 16:16-21; Ex. 1019, 17:10-13; Liu, ¶ 72.

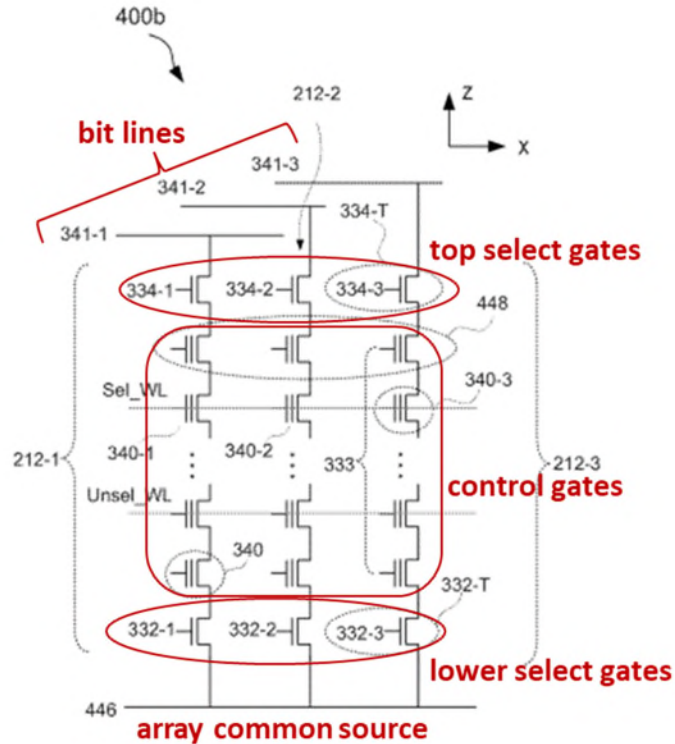
Data storage using charge trap technology has a drawback in that charges may escape (i.e., de-trap) over time. Ex. 1013, 327. Electric fields can cause de-trapping which, over time, can alter the intended data state. *Id.*, Ex. 1016, 3:52-59, 17:12-17.



Ex. 1016, FIG. 1A; Liu, ¶ 73.

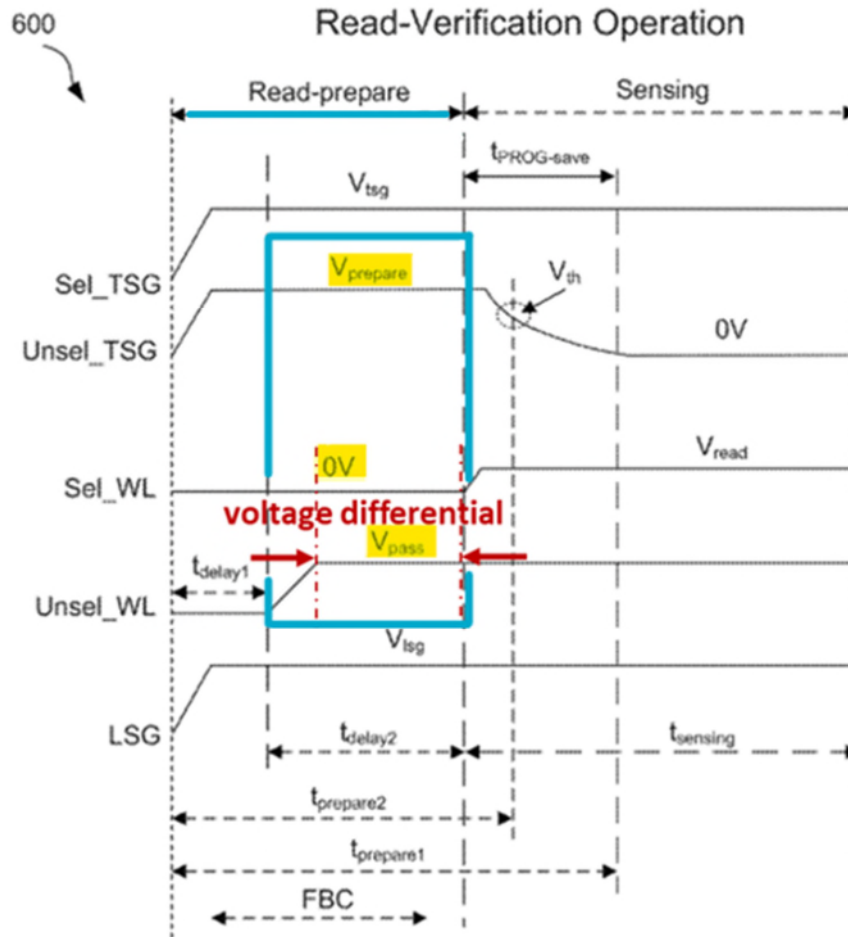
B. Overview of the Patent

The '342 patent relates to a read-verification operation for charge-trapping 3D NAND. Ex. 1001, Abstract, 1:29-32, 7:15-22. The 3D NAND has a conventional structure:



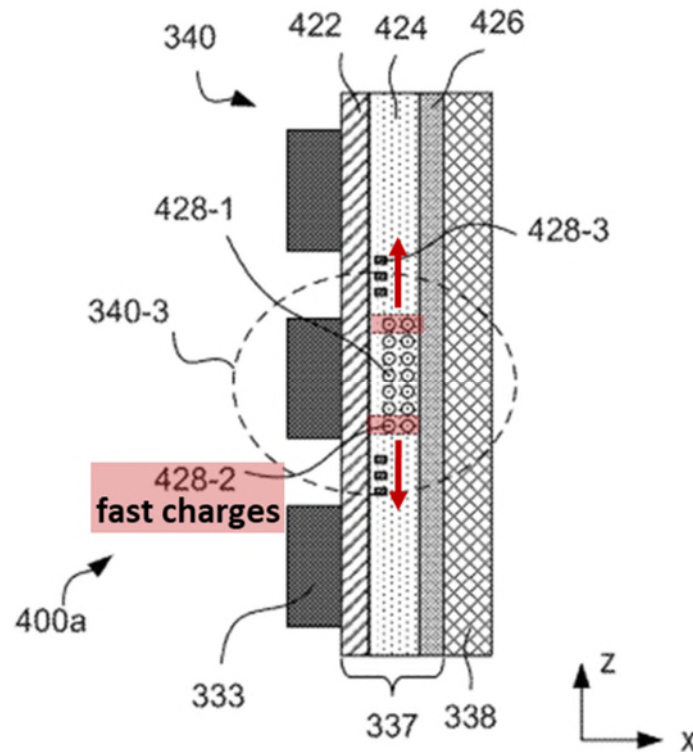
Id., FIG. 4B (annotated); 7:51-8:4.

The '342 patent acknowledges the problem of de-trapping in charge-trap memories, i.e., the de-trapping after a program can create read errors. Ex. 1001, 1:29-36. It purports to address this drawback by “removing fast charges of the target memory cell at a read-prepare step” before a read/sensing operation. *Id.*, Abstract, FIGs. 6-8. “Removing the fast charges of the target memory cell includes applying a prepare voltage ($V_{prepare}$) on an unselected top select gate (Unsel_TSG) of an unselected memory string, applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell, and applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL).” *Id.*



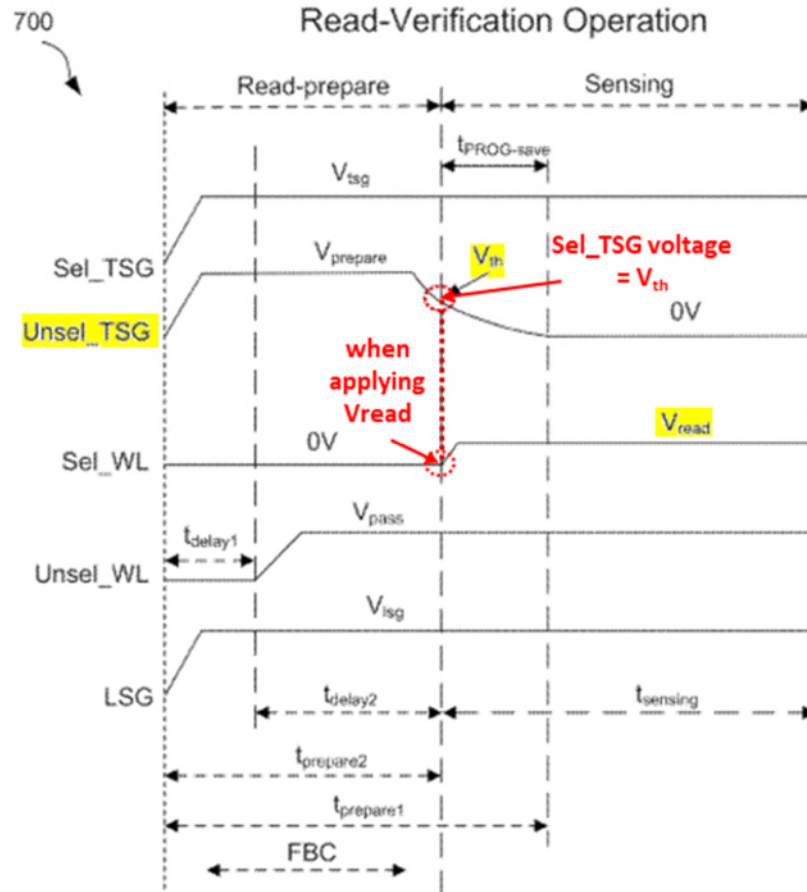
Id., FIG. 6 (annotations added). The prepare voltage turns on the unselected top select gate (Unsel_TSG), i.e., the unselected string. *Id.*, 8:67, 12:56-62. The pass voltage, which is applied to Unsel_WL during the read-prepare and sensing periods, is a term of art and turns on the unselected word lines (Unsel_WL). Liu, ¶¶ 76-80.

The differential between V_{off} on a selected word line and V_{pass} on neighboring, unselected word lines generates an electric field, which exerts a force to “de-trap the fast charges 428-2 from the shallow traps, pull[ing] them towards the neighboring unselected memory cells.” Ex. 1001, 12:24-34.



Id., FIG. 4A (annotated); Liu, ¶ 81.

As relevant here, claim 7 relates to “a voltage of the unselected top select gate” being “a threshold voltage of an unselected memory cell” “when” “applying the read voltage during the second time period.” Ex. 1001, 15:23-37. The “when” condition corresponds to when the sensing (or read) operation occurs, i.e., the read voltage is applied to measure the threshold voltage of the selected memory cell. *Id.*, 13:18-22. This point of time is shown below:



Id., Fig. 7 (annotated); Liu, ¶ 82.

Accordingly, claim 7 requires determining the level of the “voltage of the unselected top select gate” at this time. And whatever the “voltage of the unselected top select gate” is at this time, “a threshold voltage of an unselected memory cell” must be equal to that voltage. Liu, ¶ 83.

C. Prosecution History

During prosecution, the claims were rejected as anticipated by U.S. Publication 2019/0371394 (to Yang). Ex. 1002, 271-274. Applicant successfully

distinguished Yang by arguing that during the first time period, zero volts is “applied” to the “unselected word lines.” *Id.*, 311-312, 321-323.

VI. CLAIM CONSTRUCTION

The Board applies the same *Phillips* claim construction standard used by district courts. *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (*en banc*). For purposes of this petition, Petitioner submits that the ’342 patent’s claim terms do not require further construction and can be afforded their plain and ordinary meaning.

This Petition, however, addresses the claims’ use of “applying” voltages “during” particular “time period[s].” The ’342 patent makes clear that the claims do not require applying these voltages throughout a given time period. For example, claim 1 recites “applying, on an unselected word line, a pass voltage during the first time period....” Ex. 1001, Claim 1. As recited in dependent claim 4 and as can be seen below, the pass voltage V_{pass} is not applied throughout the first (“Read-prepare”) time period:

Id., FIG. 6; *see also id.*, Claim 4 (reciting the corresponding “delay period”); Liu, ¶¶ 87-93.

A POSITA in the field of the '342 patent would have had a master's degree in electrical engineering or a similar discipline, along with 4-5 years of professional experience working with (e.g., researching, designing, or developing) NAND flash memory devices (including issues relating to the operation, e.g., reading of said

devices), or an equivalent level of skill, knowledge, and experience (e.g., an advanced degree may replace some of the professional experience). Liu, ¶¶ 35-39.

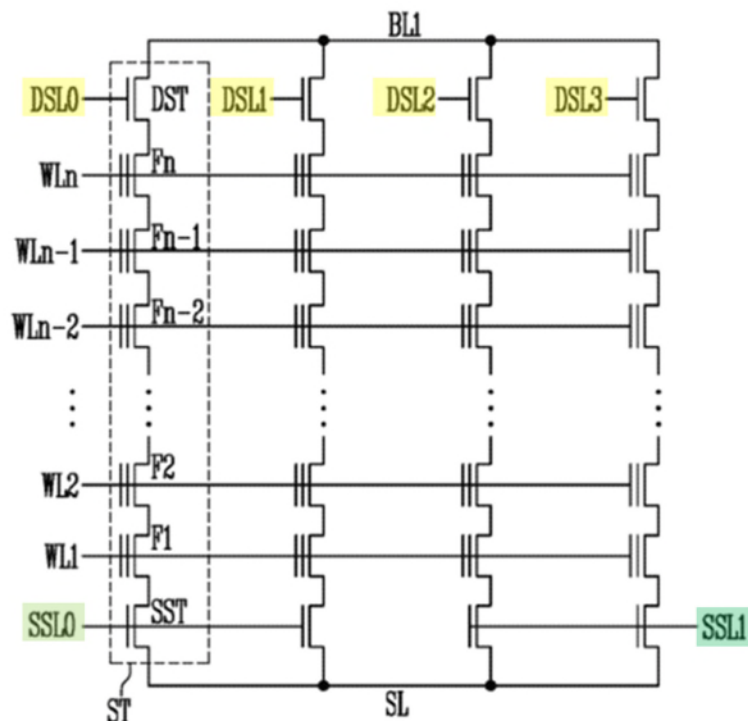
VIII. PRIOR ART OVERVIEW

A. Seo

Seo was filed on October 18, 2019, and was published on January 28, 2021.

Seo, Cover. Seo is prior art under 35 U.S.C. §§102(a)(1)-(2) (AIA).

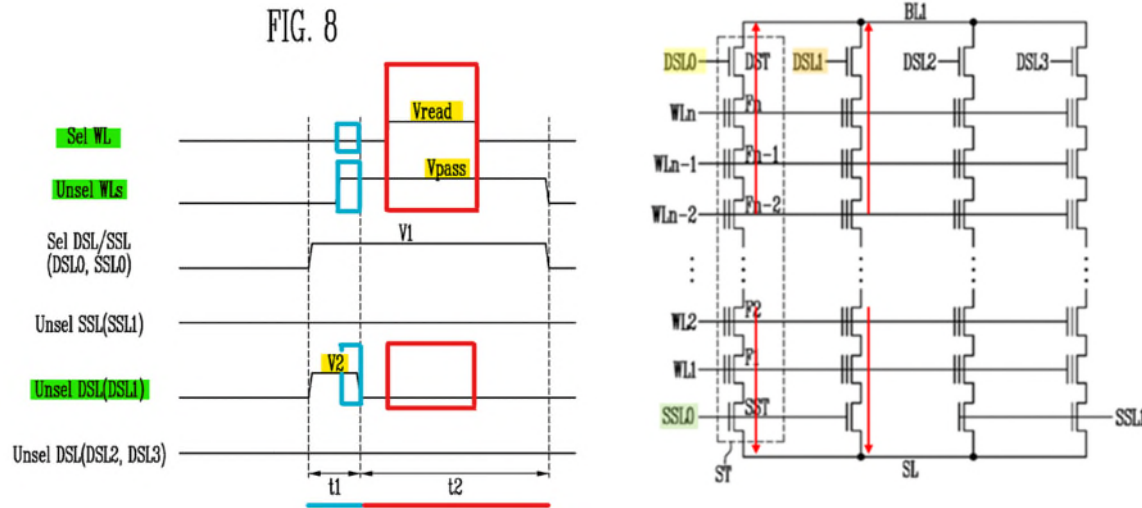
Seo is directed to read operations of nonvolatile memory devices such as 3D NAND flash memory. Seo, Abstract, [0004]-[0007]; Liu, ¶¶ 96-97. Seo's memory devices comprise memory strings with individual drain select lines ("DSL") and partially shared source select lines ("SSL").



Seo, FIG. 4 (annotated).

Seo is focused on reducing a disturbance known as hot carrier injection (“HCI”) occurring on an unselected memory string during read operations. Seo, [0008], [0048]. Specifically, the high gate voltage on unselected memory cells can cause hot electrons to be injected into an adjacent cell and disturb its data state. Ex. 1013, 254. By applying DSL and SSL voltages *before* the read operation, Seo controls channel voltages of the relevant memory strings via coupling to bit lines and source lines, reducing HCI. Seo, [0048], [0088]-[0089]; Liu, ¶ 98.

As shown below, during t1, (1) a high pass voltage is applied to the unselected word line (“Unsel WLS”), (2) an off voltage, ground, is applied to the selected word line (“Sel WL”), and (3) a high prepare voltage, V2, is applied to the unselected string (“Unsel DSL”). During t2, (1) a high pass voltage, Vpass, is applied to the unselected word line, (2) a read voltage, Vread, is applied to the selected word line, and (3) an off voltage, ground, is applied to the unselected string.



Seo, FIGs. 8, 4 (annotated); Liu, ¶ 99.

Seo's method creates an electric field that removes fast charges, just like the '342 patent. Liu, ¶ 100.

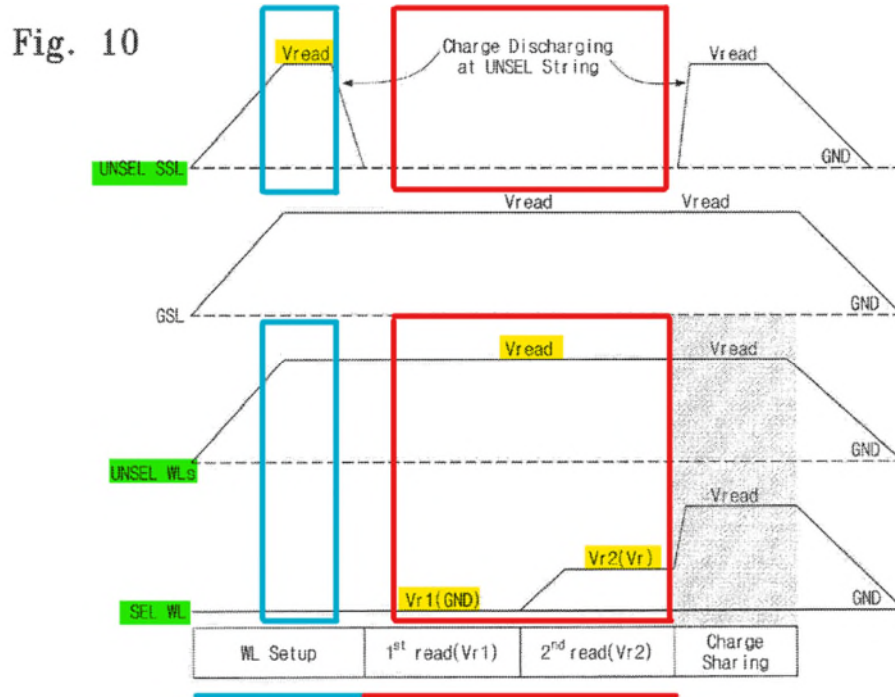
B. Nam

Nam was published on January 1, 2015. Nam, Cover. Nam is prior art under 35 U.S.C. §102(a)(1)-(2) (AIA).

Nam relates to read-verify operations of conventional 3D NAND flash memory devices. Nam, Abstract, [0029], [0065], [0155], [0164], Fig. 2A; *See* Liu, ¶¶ 101-02. Nam discloses immune disturbance read modes to control channel charges before and after read operations, though Nam's focus is on the post-read period. Nam, [0070]; Liu, ¶¶ 103-04.

As shown below, during WL Setup, (1) a high pass voltage, V_{read} , is applied to the unselected word line ("Unsel WLS"), (2) an off voltage, ground, is applied to the selected word line ("Sel WL"), and (3) a high prepare voltage, V_{read} , is applied

to the unselected string (“Unsel SSL”). During the 1st and 2nd read period, (1) a high pass voltage, V_{read} , is applied to the unselected word line, (2) read voltages, V_{r1} and V_{r2} , are applied to the selected word line, and (3) an off voltage, ground, is applied to the unselected string.



Nam, FIG. 10 (annotated); Liu, ¶ 105.

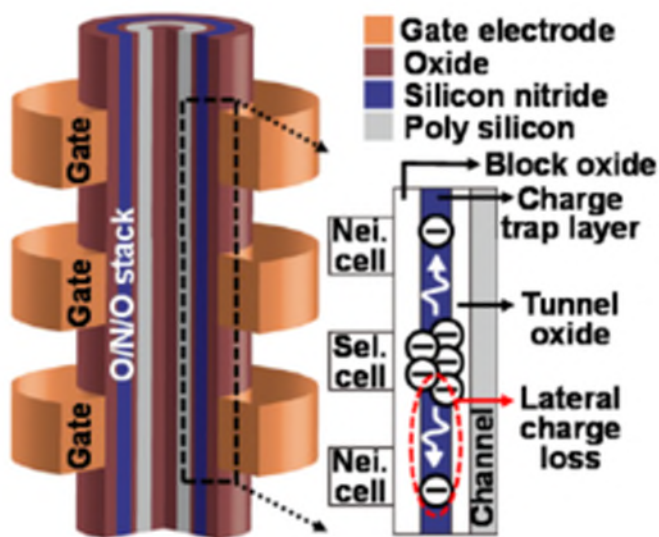
Nam’s method creates an electric field that removes fast charges, just like the ’342 patent. Liu, ¶ 105.

C. Choi

Choi was presented at the IEEE 2016 Symposium on VLSI Technology Digest of Technical Papers. Choi; Ex. 1020, Ex. B. Choi was published online at IEEE Xplore on September 22, 2016. Ex. 1021. This Symposium is an annual event

dating back decades. *See Nanya Tech. Corp. v. Lone Star Silicon Innovations, LLC*, IPR2018-00062, Paper 7 at 2, 4 n.3 (PTAB Apr. 25, 2018) (instituting trial based on a paper from the 1999 counterpart publication). The Symposium was announced and discussed on industry websites and on social media in advance and its program was archived. Ex. 1020, Exs. A-B. Choi is cited in pre-'342 patent publication and non-patent literature. Exs. 1022-1023. Choi is prior art to the '342 patent under 35 U.S.C. §102(a)(1) (AIA) and was publicly and readily accessible by a POSITA before 2019. Liu, ¶ 106.

Choi documents an evaluation of fast-charge loss in charge-trap 3D NAND Flash memory.



Choi, FIG. 1 (annotation in original).

Choi evaluates fast-charge loss, which occurs within seconds of cell programming (which Choi refers to as “early retention”²) and which causes undesirable drifts in threshold voltages. Choi, 1:16-24. Choi found that lateral fast-charge loss (i.e., in a direction parallel to the length of a memory string) is the “primar[y]” mechanism of early retention. *Id.*, 1:26-32, 2:48-52, 1:9-12. Choi explains that “a large lateral electric field is generated at the edge of the cell in which there is a greater chance for stored charges in a charge trap layer to spread laterally.” *Id.*, 2:16-18. “[T]he edge of the cell” refers to an interface with an adjacent cell, as Figure 1 above illustrates. Thus, the charges move to neighboring cells. Liu, ¶¶ 107-09.

As shown below, within “a few sec[onds]” after programming, the threshold voltage may shift and lead to “a verification fail.”

² Choi discusses “fast charge loss within a few seconds, which is referred to as early retention.” Choi, Abstract.

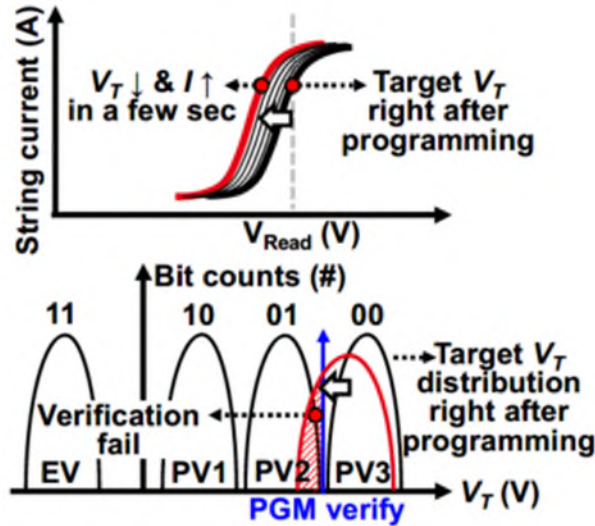


Fig. 2. Schematic of the early retention and its effect on V_T and I . The early retention threatens the MLC capability and the tight V_T distribution.

Choi, Fig. 2. Fast-charge loss is an issue because the threshold value being verified will change unless fast-charge loss occurs before verification. Liu, ¶¶ 110-11.

IX. THE '342 PATENT'S CLAIMS ARE OBVIOUS

A. *Ground 1: Claim 7 Is Obvious Over Seo in View of Choi*

Seo in view of Choi and the knowledge of a POSITA renders claim 7 obvious.

Liu, ¶¶ 112-13.

1. Claim 1

[1.Pre] “A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:”

To the extent the preamble is limiting, Seo discloses, or at least renders obvious, the preamble. Liu, ¶ 114.

Seo discloses a method of reading a “[*m*]emory device” with “a *memory cell* array” (Seo, Abstract),³ which is “*three-dimensionally* structured.” *Id.*, [0050]; *see also* [0004] (“Flash memory,” as “NOR” or “NAND”), [0006] (“Flash memory,” including “*three-dimensional semiconductor devices*.” Thus, Seo discloses 3D Flash memories. Liu, ¶¶ 115-16.

Seo’s “memory cells” are “*read*” by a “*read operation*.” Seo, Abstract; [0072]. Seo’s read operation is on a *target memory cell*, i.e., at the intersection of the selected word line (“Sel WL”) and “selected memory string.” *Id.*, [0089]-[0090], FIG. 5, §§V.A.1-2. Thus, Seo discloses *[a] method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device*.⁴ Liu, ¶ 117.

Seo would have been understood to disclose its read operation for verification. Liu, ¶¶ 118-21. Seo generally discloses its read operation, and as was well known, a fundamental use of a read operation was for verification after a program. *See* §V.A.2. What’s more, Seo discloses embodying its invention in devices that “program.” Seo, [0108]. Verification is necessarily part of programming in flash

³ Emphasis added unless otherwise noted.

⁴ For clarity, the claim mapping portion uses red italics for claim language.

memories, and thus Seo would have been understood to disclose using its read operation after the “program operations” that it references. *See* §V.A.2.

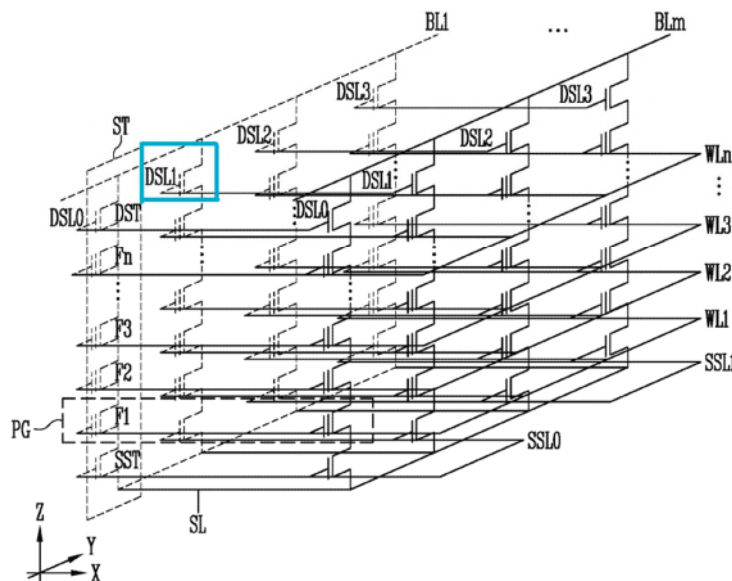
At the very minimum, Seo in view of Choi renders it obvious to perform Seo’s read operation immediately after a program operation to verify successful programming. *See* Choi, FIG. 2 (verification), §IX.A.3 (motivations); Liu, ¶ 122.

[1.A] “applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period”

Seo discloses this limitation.

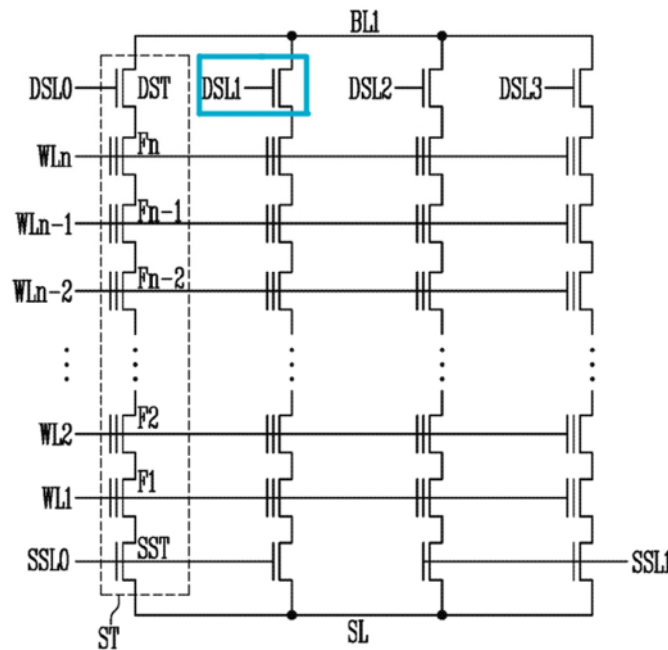
In Seo, each “drain select transistor” (“DST”), to which a “drain select line[]” (“DSL”) connects, is a *top select gate of a ... memory string*. Seo, [0048], [0055].

FIG. 3



Id., FIG. 3 (annotated).

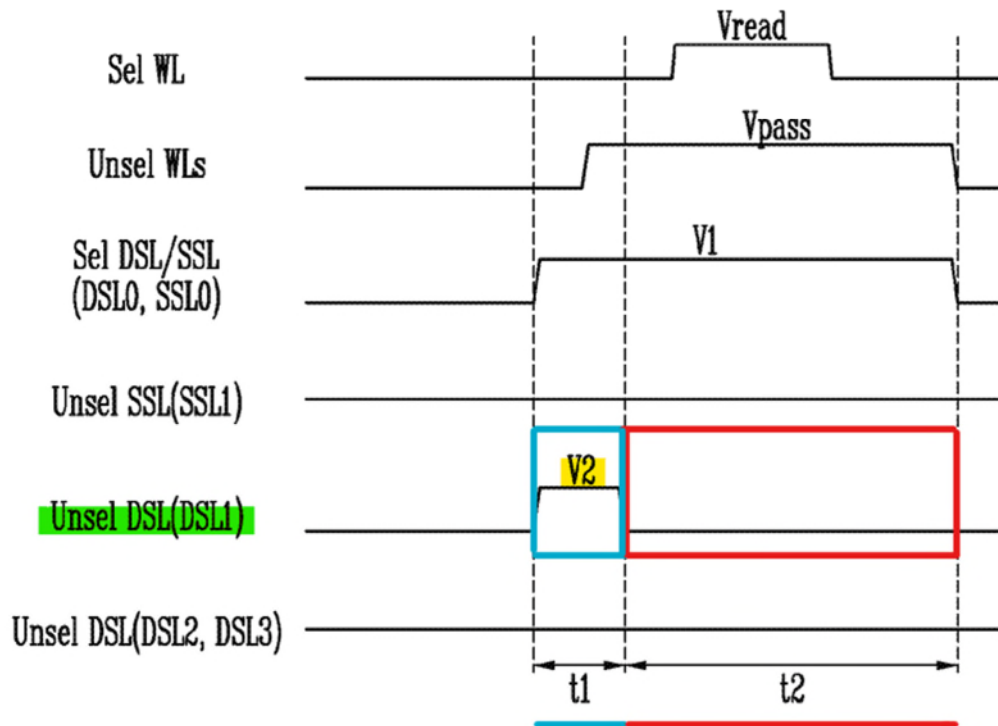
FIG. 4



Id., FIG. 4 (annotated).

Figure 8, shown below, illustrates a read operation. Seo, [0086]. t_1 corresponds to *a first time period* and t_2 corresponds to *a second time period*. As part of the read operation, a “voltage V_2 ”—the *prepare voltage*—is *applied* to “DSL1” that “correspond[s] to the unselected memory string.” *Id.*, [0088]. This voltage turns on DSL1 (*id.*) as does the ’342 patent’s *prepare voltage* (Ex. 1001, 12:56-62). The voltage application on an unselected DSL occurs *during* (at a point in the course of) the *first time period* (“ t_1 ”)—followed by a low voltage, e.g., ground (V_{ss}) being applied—*an off voltage*—*during a second time period* (“ t_2 ”).

FIG. 8



Seo, FIG. 8 (annotated), [0075], [0088]-[0089].

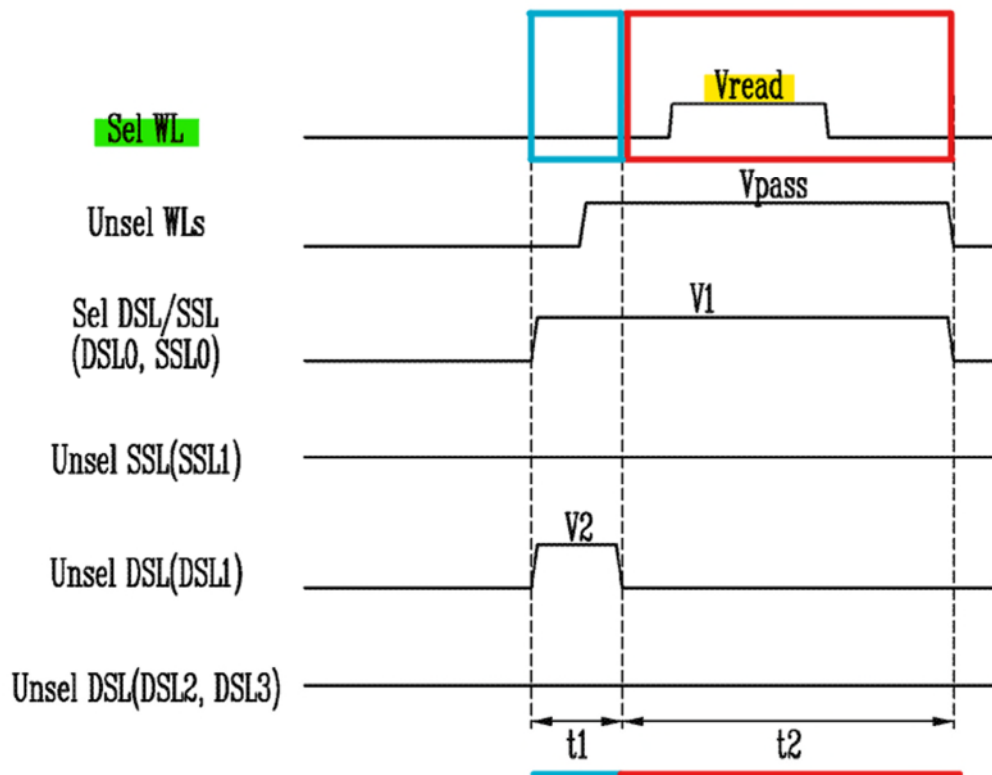
Thus, Seo discloses *applying, on an unselected top select gate of an unselected memory string* (e.g., Unsel DSL (DSL1)), *a prepare voltage during a first time period* (e.g., V2 during t1) *and an off voltage during a second time period* (e.g., off voltage during t2). Liu, ¶¶ 123-27.

[1.B] “applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period;”

Seo discloses this limitation.

As shown below, a zero voltage—an *off voltage*—is applied to a *selected word line* (“Sel WL”) during “t1” (the *first time period*), and the “*read voltage Vread*” may [then] be *applied* during “t2” (the *second time period*). Seo, [0088]-[0090].

FIG. 8



Id., FIG. 8 (annotated).

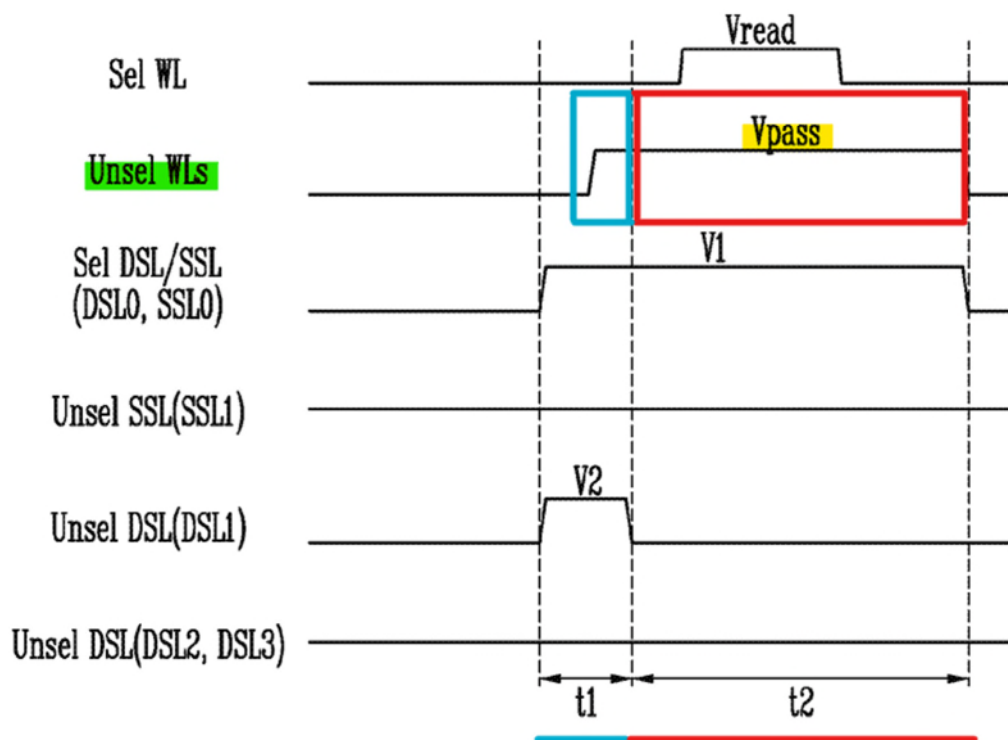
Thus, Seo discloses *applying, on a selected word line associated with the target memory cell* (e.g., Sel WL), *the off voltage during the first time period* (0 volts during t1) *and a read voltage during the second time period* (Vread during t2). Liu, ¶¶ 128-30.

[1.C] “applying, on an unselected word line, a pass voltage during the first time period and the second time period,”

Seo discloses this limitation.

Seo discloses that a “*pass voltage* V_{pass} ” is applied to “*unselected word lines*” (“Unsel WLs”) during the *first* and *second time periods*, t_1 - t_2 . Seo, [0082], [0083], [0089].

FIG. 8



Id., FIG. 8 (annotated).

Thus, Seo discloses *applying, on an unselected word line* (e.g., Unsel WLs), *a pass voltage during the first time period and the second time period* (e.g., V_{pass} during t₁ and t₂). Liu, ¶¶ 131-33.

[1.D] “wherein the read-verification operation removes fast charges of the target memory cell during the first time period.”

Seo discloses this limitation or, at least, renders it obvious in view of Choi. Liu, ¶ 134.

In the context of charge-trap memories, the ’342 patent discloses that “[r]emoving the fast charges of the target memory cell includes” applying the voltages of limitations [1.A]-[1.C]. Ex. 1001, Abstract. As §§IX.A.1[1.A]-[1.C] demonstrate, Seo discloses these voltages. Specifically, Seo teaches having a higher voltage on unselected WLs (e.g., adjacent WLs to the selected WL) *during the first time period*. §§ IX.A.1[1.B]-[1.C]. As the ’342 patent recognizes, this voltage differential removes fast charges. See Ex. 1001, 12:24-34, VII.C; Liu, ¶¶ 135-36.

Seo discloses, or would have been understood to disclose, charge-trap 3D memories. Liu, ¶¶ 137-40. Recall that Seo discloses that its read operation is for a 3D Flash memory device. §IX.A.1[1.Pre]. Charge-trap memory is a type of 3D memory device, and what’s more, suffers from the “disturb phenomenon” that Seo specifically addresses (Seo, [0008]). Ex. 1017, 101, 108. And a charge-trap memory was one of two basic types of 3D Flash memory devices. *Id.*, 101, 144. Indeed, charge-trap memories were incredibly popular, textbook material in 2019. *Id.*, 101.

Thus, Seo discloses, and would have been understood to disclose, performing its read operation on charge-trap memories, which removes fast charges. Liu, ¶ 141.

To the extent that PO argues that Seo does not disclose a “charge-trap” memory or removal of “fast charges” (which is incorrect), Seo in view of Choi renders obvious claim [1.D], because it would have been obvious to employ Seo’s read operation in a 3D charge-trap memory with the knowledge that it removes fast charges in view of Choi. *See* §IX.A.3. Choi specifically discloses a “3-D NAND flash memory with a charge trap layer.” Choi, 1:16-17. Choi addresses the issue of “early retention (fast charge loss within a few seconds).” *Id.*, Title. “[S]hallowly trapped electrons” are more likely to be lost due to lateral movement when “a large lateral electric field is generated at the edge of the [memory] cell,” i.e., near the interfaces with adjacent cells. *Id.*, 1:28-29, 2:4-25, FIG. 1. The lateral electron movement from the selected memory cell to its neighboring memory cells (labeled “[l]ateral charge loss” though appearing vertically in the figure due to the orientation of the memory string) is shown below:

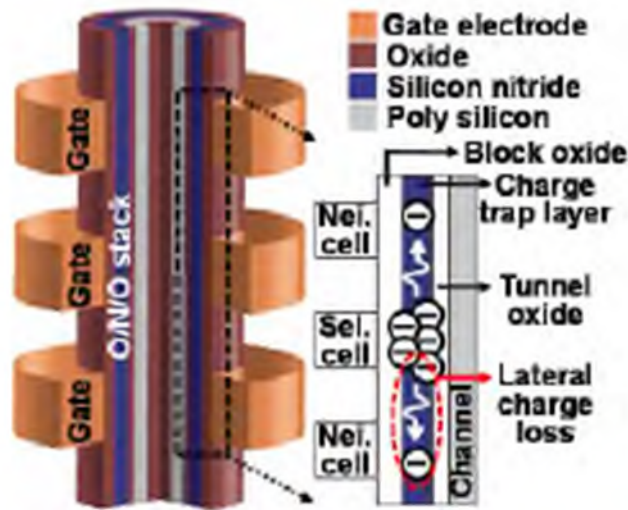


Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

Id., FIG. 1 (annotation in original). Seo creates such “a large lateral electric field.” Accordingly, it would have been obvious to employ Seo’s read operation in Choi’s charge-trap memory with Choi’s express disclosure of removing fast charges. Liu, ¶¶ 142-43; §IX.A.3.

Accordingly, Seo discloses, or at least in view of Choi renders obvious, *wherein the read-verification operation removes fast charges of the target memory cell during the first time period* (e.g., voltage differential on the WLs during t1 creates an electric field that removes charges from charge-trap memory cells). This removal would occur any time a read occurs within a few seconds of a program operation, e.g., during verification. Choi, 1:2-5; Liu, ¶ 144.

2. Claim 7

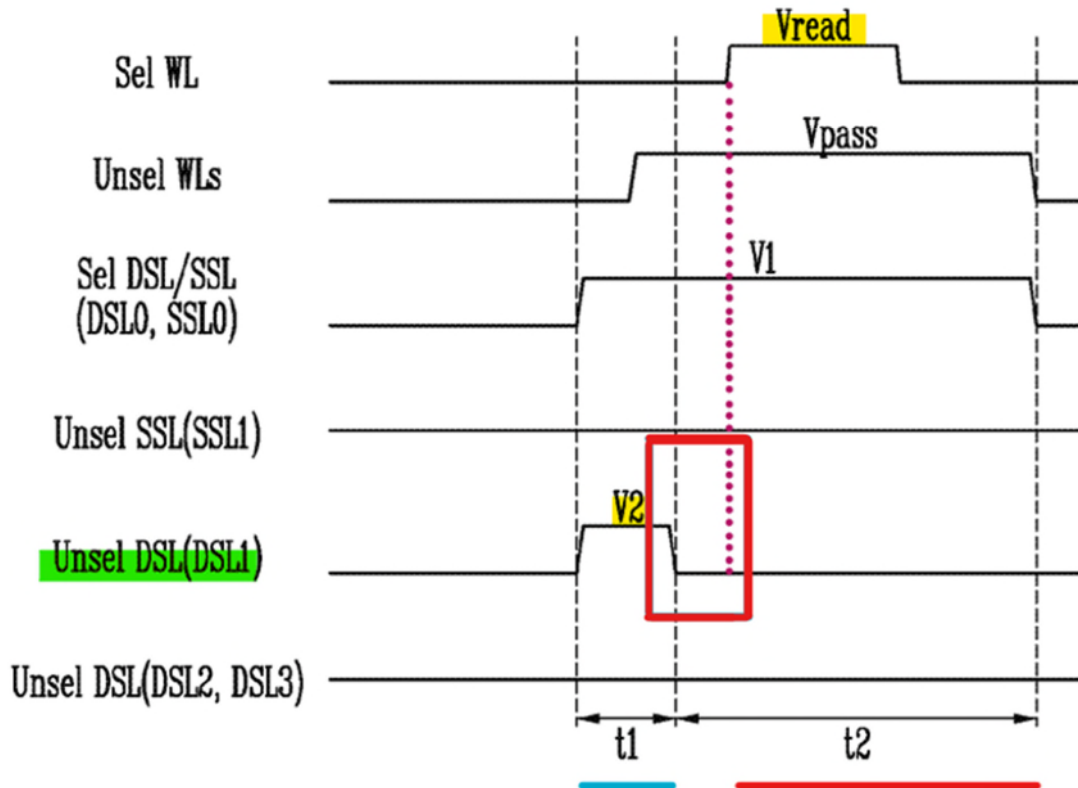
Claim 7 depends from claim 1 and further requires:

[7] “wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell”

Seo discloses, or at least renders obvious, this limitation. Liu, ¶¶ 145-46.

Seo’s *read voltage* is Vread on Sel WL, and the voltage of the unselected top select gate is Seo’s Unsel DSL. *See* limitations [1.A]-[1.B]. Accordingly, this limitation corresponds to the below:

FIG. 8



Seo, FIG. 8 (annotated); Liu, ¶ 147. When *applying the read voltage* occurs, the voltage on *the unselected top select gate* (Unsel DSL1) is 0V. As described below, it would have been understood, or at least obvious, that 0V *equals to a threshold voltage of an unselected memory cell*, e.g., an erased cell. Liu, ¶¶ 148-49.

As an initial matter, recall that erased memory cells may have a zero threshold voltage. See §V.A.2; Liu, ¶ 148.

An erase operation will erase the entire block, i.e., an array of memory strings. Ex. 1017, 91-93; *see also* Seo, [0108] (recognizing “erase”). Thus, after an erase

and the first programming operation, there will necessarily be erased and programmed unselected cell(s).

Further, after the erase, the programming will typically occur from top to bottom or from bottom to top, e.g., program the lowest row of memory cells, then the next one up, etc. Ex. 1024, [0115], [0130]. After the first program, a program operation will involve both unselected programmed and erased cells.

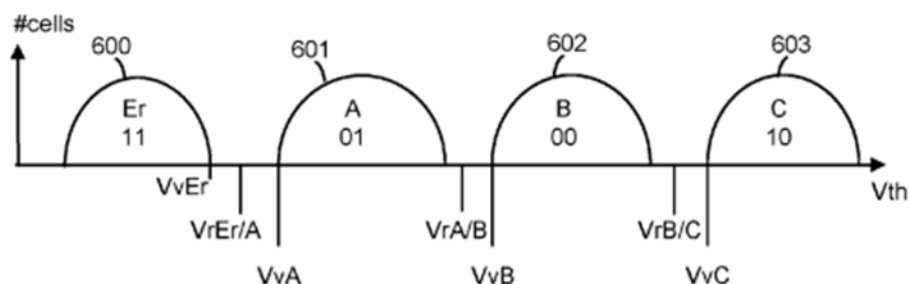
Each approach, bottom to top or top to bottom, was an obvious implementation of Seo. Such techniques were conventional (see above). Further, each approach was known to be beneficial. First, each approach provides for easily knowing the state of the rows above and below the selected row, enabling access operations that reduce disturb issues. Ex. 1025, 8:18-53. Second, a sequential program order simplifies controller decoding operations. Third, it would have been necessary to implement a programming scheme for Seo's device, and these sequential programming schemes were well understood. Each approach was highly predictable and routine to implement, because each approach merely involves using a pointer that increments either up or down. Liu, ¶¶ 150-52.

With either approach, a read on any but the topmost or the bottommost row involves unselected memory cells that are erased (e.g., above) and programmed (e.g., below). Thus, *an unselected memory cell*, e.g., an erased cell in some embodiments, has a zero threshold voltage, and *a voltage of the unselected top select*

gate will be *equal to a threshold voltage of an unselected memory cell*. *Id.*, ¶ 153-54.

Again, recall for a given erase threshold window, the threshold distribution for the erased state may include zero volts because its window spans negative and positive values. *See* §V.A.2; Liu, ¶ 155. As such, some erased cells will have a zero threshold voltage. *See Unwired Planet, LLC v. Google Inc.*, 841 F.3d 995, 1002 (Fed. Cir. 2016) (citing *Hewlett-Packard Co. v. Mustek Sys., Inc.*, 340 F.3d 1314, 1326 (Fed. Cir. 2003)) (“combinations of prior art that sometimes meet the claim elements are sufficient to show obviousness”).

More specifically, Seo discloses a memory device comprising program and erase operations. Seo, [0108], [0119]. Thus, as a POSITA would have expected, an erased state and one or more programmed data states exist in Seo’s device. *See also* §V.A.2. Seo’s read voltage V_{read} is used to determine the data state of the selected memory cell. For example, by adopting the following data state windows and by setting V_{read} to $V_{vEr/A}$, Seo’s read-verification operation can determine whether the selected cell is in the erased state Er .



Ex. 1016, FIG. 6. Recall that a POSITA would have understood that the Er threshold window may be entirely in the negative domain or may include a zero threshold voltage within its window. §V.A.2. This selection of the erased threshold voltage window is a choice among a finite number of possible windows. *Id.* And including zero volt in the erased state’s threshold window was not only well known, but an implementation of major memory device manufacturers. *Id.* Indeed, it was well understood how to implement these various windows for access operations. *Id.* Thus, it would have been obvious to configure a memory device to comprise an unselected memory cell having a zero threshold voltage. *Geo. M. Martin Co. v. All. Mach. Sys. Int’l LLC*, 618 F.3d 1294, 1302 (Fed. Cir. 2010) (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 421 (2007)) (affirming district court finding that one out of three options “is exactly the type of ‘finite number of identified, predictable solutions’ ... [for which] the result, when expected, is ‘the product not of innovation but of ordinary skill and common sense’”); Liu, ¶ 156.

3. Motivation to Combine

A POSITA would have been motivated, with a reasonable expectation of success, to apply Choi's teachings to Seo regarding: (1) charge trap memory and stack teachings (alternating gate/dielectric layers), and (2) verification and fast charge removal. Liu, ¶ 157.

As an initial matter, both Seo and Choi address issues in the field of 3D NAND flash memory, and more specifically, read operations. Seo, Abstract; Choi, 1:14-26. And Choi describes the physics underlying certain of these issues (fast charges). What's more, Seo is a patent application assigned to SK Hynix Inc., and many of Choi's authors are from SK Hynix's research center. *See* Seo, Cover; Choi, Cover. Thus, a POSITA would have been motivated to consider Choi to understand and improve on Seo's memory device. Liu, ¶ 158.

As to Choi's charge trap memory and stack: first, while Seo does not describe in detail its 3D NAND memory cells, Choi does. Choi recognizes the promise of charge-trap technology and stacked 3D NAND memories while addressing the challenges thereof, and thus a POSITA would have considered Choi to implement the basic structure of Seo's 3D NAND memory. Choi, 1:16-20; Liu, ¶ 159. Second, before 2019, "most of 3D memories [were] based on 'charge trap' cells." Ex. 1017, 15. Charge-trap technology was thought to be more "scalable than floating gate." *Id.* Thus, a POSITA would have been motivated to consider Choi's popular 3D

memory implementation. Liu, ¶ 160. Third, Seo’s read operation creates a voltage differential. §IX.A.1[1.D]. Choi teaches that this voltage differential de-traps fast charges from the charge-trap layer. Liu, ¶ 161. And Seo’s disclosure of reducing read disturbance is also directly applicable to a charge-trap device. Thus, a POSITA would have been motivated to consider applying Choi’s charge-trap memory teachings to Seo’s read operation, given the benefits of Seo’s read operation to charge-trap memories. *Id.*, ¶ 162.

A POSITA would have had a reasonable expectation of success in applying Choi’s structural teachings to Seo. First, before 2019, charge-trap memory was the norm for 3D memory. Ex. 1017, 15. Second, Seo already graphically depicts a 3D memory architecture with, effectively, gate layers and memory pillars. Seo, FIG. 3. Third, not only were such structures known, but Choi illustrates that the device physics were also known. Liu, ¶¶ 163-66.

As to Choi’s read-verification step and fast charge removal teachings: first, both Seo and Choi address issues relating to the reliability of read operations. Seo, [0008]; Choi, 1:16-26. A POSITA considering the reliability issues in Seo would have been motivated to consider references that address the same issue. Liu, ¶ 167. Second, while Seo focuses on hot-charge injection (“HCI”), Choi focuses on fast-charge loss. *See* §§VIII.A, VIII.C. Both issues were well known to a POSITA. Thus, knowing that Seo only expressly addresses HCI, a POSITA would have been

motivated to consider Choi's teachings regarding an additional reliability issue. Liu, ¶ 168. Third, Seo's read operation in t1 creates a voltage differential. See §IX.A.1[1.D]. A POSITA would have been motivated to consider the effect of this voltage differential, which Choi explains. And Choi expressly teaches this effect in the context of program-verify operations. Choi, FIG. 2; Liu, ¶ 169. Fourth, Choi describes a use case for Seo's read operation and teaches that Seo's read operation would be beneficial to verify after programming. For example, Choi found that lateral fast-charge loss was critical for de-trapping, and thus a POSITA would have recognized that Seo's lateral-electric-field-inducing voltage differential was a particularly good mechanism for removing fast charges. Further, Choi describes that because of fast charge loss, a typical read-verify may be unsuccessful. Choi, FIG. 2. This is because the threshold may shift after verification. *Id.* Thus, a POSITA would have recognized that using Seo's read operation to verify, which removes the fast charges, would result in a more accurate verification, because any threshold shifting would occur before verification. Liu, ¶ 170.

Importantly, a POSITA also knew that a read operation was applicable to "the normal read operation" or "the verification read operation for verifying the success of the program operation." Ex. 1028, [0103]. And there was great benefit to using the same fundamental read operation for both purposes, because one finely tunes the read to avoid read interference issues, and there is no reason to "reinvent the wheel."

Thus, the ordinary knowledge of a POSITA also supports applying Seo's read as a verification operation. Liu, ¶¶ 171-73.

A POSITA would have had a reasonable expectation of success in applying Choi's read-verification and fast-charge-removal teachings to Seo. First, as explained above, Seo's memory is structurally similar to Choi's from a high-level perspective. Second, Choi teaches the device physics of Seo's read operation as it relates to fast charges, thus detailing Seo's operational characteristics. Third, Choi makes clear that Seo's read operation would remediate fast charge issues in a verification that occurs close in time to a program operation. Fourth, it was known how to use a read operation for verification (e.g., the read voltage (used as the verify voltage) may be slightly adjusted, while leaving the other voltages the same), which was conventional. *See* Ex. 1029, [0181], Ex. 1019, 25:2-8; Ex. 1028, [0054]-[0055]. Liu, ¶¶ 174-78.

B. Ground 2: Claim 7 Is Obvious Over Nam in View of Choi

Nam in view of Choi and the knowledge of a POSITA renders claim 7 obvious. Liu, ¶¶ 179-80.

1. Explanation of Figures

This Ground focuses on Nam's "immune disturbance read operation" as largely set forth in Figure 10 and its accompanying description. As Nam discloses, however, "the inventive concept [is] more fully described with reference to FIGS. 1

to 10.”⁵ Nam, [0147]. Other figures in Nam, e.g., Figure 19, also describe use cases of Nam’s “immune disturbance read operation.” *Id.*, [0155]-[0156]. Thus, this Ground cites to various figures of Nam.

Figures 1-3 and 5 depict exemplary structural aspects of Nam’s memory array. Nam, [0033]-[0036], [0038]. Figure 3 also illustrates a prior art pre-sensing and sensing⁶ scheme. *Id.*, [0094]-[0096]. In various places, the specification refers back to Figure 3, because Nam’s immune disturbance read operation uses Figure 3’s prior art sensing scheme (whereas Nam’s focus is on the phases before and after sensing).⁷ *Id.*, [0122]. Figure 5 also illustrates the physics of charge sharing among memory cells. *Id.*, [0099]-[0100]. Figure 4 depicts exemplary threshold and erase voltage values. *Id.*, [0098].

⁵ In each description of Figures 6-10, the specification states that it is “an exemplary embodiment of the inventive concept.” Nam, [0147]. However, as this Section explains, each of these figures builds upon the preceding figures.

⁶ The sensing phase measures the threshold value of the target memory cell. Nam, [0096], Liu, ¶ 184.

⁷ Figure 3 includes an error in indicating that the bottom select gate would be at ground during sensing. Other figures on which this Ground relies demonstrate that the bottom select gate is at a *pass* voltage during sensing. Liu, ¶ 184.

Figures 6-10 effectively provide a build that adds different signals in describing the immune disturbance read operation over four time periods: (1) WL Setup (pre-sensing), (2) 1st and 2nd reads (sensing), (3) Charge Share, and (4) Recovery. Nam, FIGs. 6-10. Relevant to this Ground are the first two periods: (1) WL Setup (pre-sensing), and (2) 1st and 2nd reads (sensing). *Id.* Figure 6 effectively starts the build in disclosing the immune disturbance read operation with respect to voltages on “UNSEL WLs” (unselected word lines) and “SEL WL” (selected word line), and the signals on these lines are identical for Figures 6-10 with respect to the first two periods. *Id.*, FIG. 6. Figures 7-9 distinguish between the UNSEL WLs for different treatment in the Charge Sharing and Recovery periods (periods that are not relevant to this Ground). *Id.*, FIGs. 7-9. Figure 9 also illustrates the waveform of “SEL SSL” (selected top select gate) and “GSL” (bottom select gate) voltages. *Id.*, FIG. 9. Figure 10 further depicts the “UNSEL SSL” (unselected top gate). *Id.*, FIG. 10, [0122] (“Referring to FIG. 10, an immune disturbance read operation on unselected string selection lines UNSEL SSL *may further include* applying ... to ... UNSEL SSL”). Figure 10, however, omits the “SEL SSL” (selected top select gate) waveform from Figure 9.⁸ *Id.*; Liu, ¶¶ 181-92.

⁸ In any event, it goes without saying that SEL SSL is high during the read operation as well, because it is necessary to read the memory cells. Liu, ¶ 192.

2. Claim 1

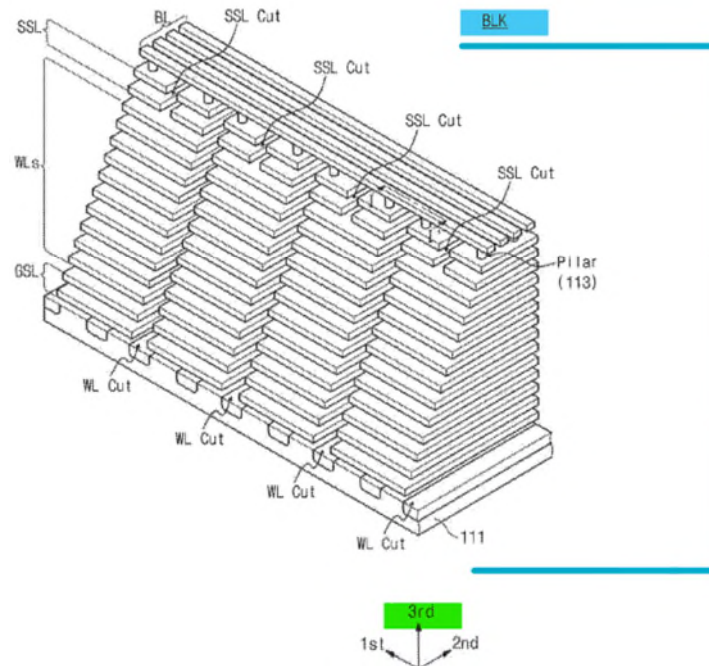
[1.Pre] “A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:”

To the extent the preamble is limiting, Nam discloses it. Liu, ¶ 193.

First, Nam teaches: “[a] method of reading a nonvolatile memory device” that includes the step of “sensing a state of a memory cell.” Nam, Abstract. Nam discloses that its read operation (“immune disturbance read operation”) is applicable *after* a program operation, e.g., a *read-verification operation*. *Id.*, [0026] (“a verification read operation”), [0155] (“immune disturbance read operation may be selectively performed at a program verification operation”), FIG. 19. The operation occurs on “memory cells corresponding to the selected word line W_{Lm-3} and the selected string selection line SSL₁,” i.e., a *target memory cell*. *Id.*, [0096]; Liu, ¶¶ 194-96.

Second, Nam’s discloses that its operations are applicable to a *three-dimensional* memory device. Nam, [0029] (“vertical NAND flash memory”), [0065] (“[e]ach of the memory blocks” may “have a *three-dimensional* structure”).

Fig. 2A



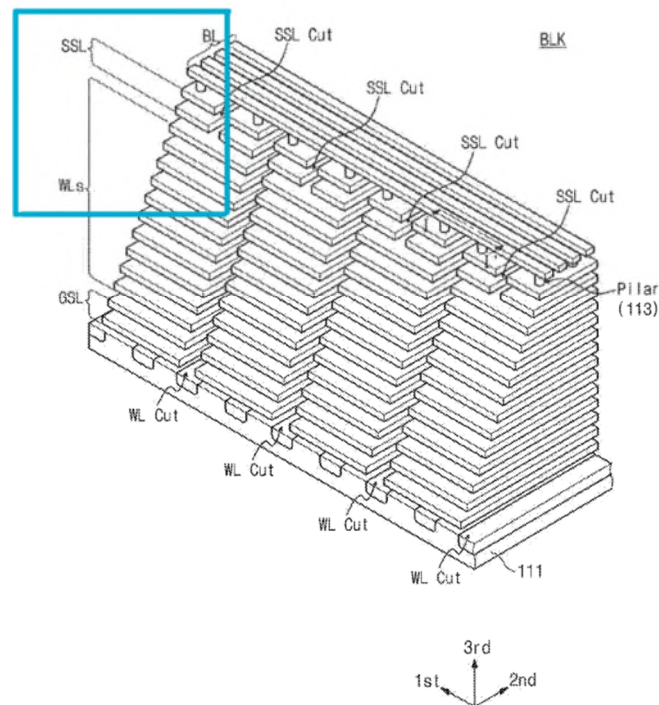
Id., FIG. 2A (annotated). Thus, Nam discloses *a method for conducting a read-verification operation* (e.g., an immune disturbance read operation) *on the memory cells connected with the selected word line may be performed on a target memory cell* (e.g., memory cell connected to a selected word line/string) *in a three-dimensional (3D) memory device* (e.g., three-dimensional memory). Liu, ¶ 197.

[1.A] “applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period”

Nam discloses this limitation. Liu, ¶ 198.

As an initial matter, Nam refers to the *top select gate* as a “string selection line SSL.” Nam, [0064].⁹ As shown below, the SSL layers reside at the top of the memory stack and select string(s).

Fig. 2A

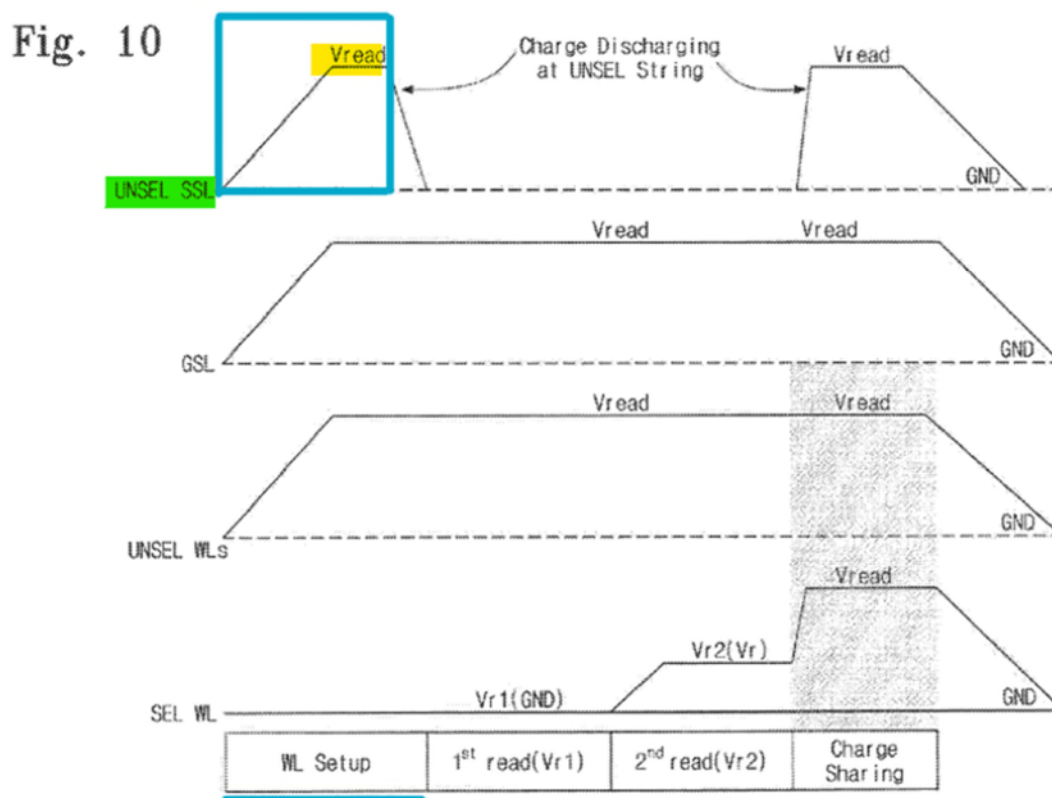


Nam, FIG. 2A (annotated), [0076].

⁹ At times, Nam refers to “string selection transistors,” which are the individual transistors of the SSL layers. Nam, [0133]; Liu, ¶ 199 n.3. But typically, Nam simply refers to applying voltages to the SSL, which this Petition will refer to when discussing applying the relevant voltages to the select gate layers.

“FIG. 10 is a timing diagram illustrating an immune disturbance read operation according to an exemplary embodiment of the inventive concept.” Nam, [0122]. As shown below, Figure 10 includes *a first time period*, i.e., “WL Setup,” and *a second time period*, i.e., “1st read[Vr1]” and “2nd read[Vr2].” *Id.*, [0104].

During *a first time period*, “the read pass voltage Vread may be applied to unselected string selection lines UNSEL SSL before a sensing operation (e.g., before the 1st read and 2nd read).” Nam, [0122].

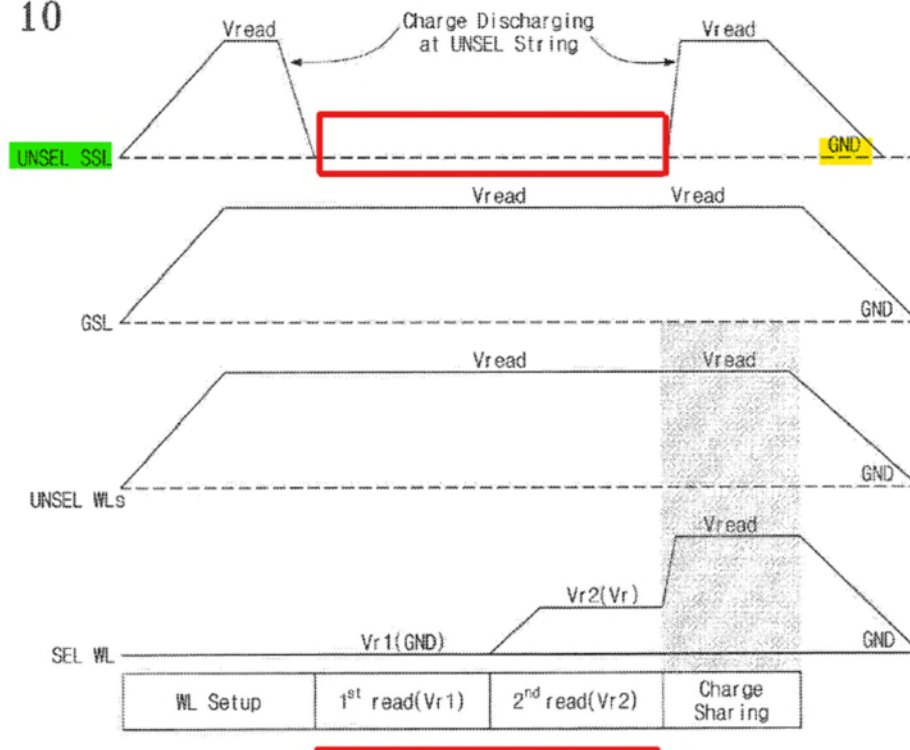


Id., FIG. 10 (annotated.). While not a requirement, Nam’s Vread pass voltage is within the exemplary ’342 range (Ex. 1001, 2:40-44). Nam, [0098] (“Vread may be

about 7V”). Also, like Figure 6 of the ’342 patent, Nam’s Vread pass voltage is greater than the voltage applied to the selected word line during the reading phase. Compare Ex. 1001, FIG. 6 (Vprepare versus Vread), with Nam, FIG. 10 (Vread versus Vr2(Vr); see also Liu, ¶¶ 199-202.

Further, during *a second time period*, Nam discloses applying an *off voltage*—namely, GND (ground)—to unselected string selection lines UNSEL SSL.

Fig. 10



Nam, FIG. 10 (annotated). Ground is an *off voltage* because it does not turn on the transistor. *Id.*, [0098] (compare with voltage that turns on transistor); Liu, ¶ 203.

Note that the description of Figure 10 states: “[a]n operation of applying the read pass voltage Vread to unselected string selection lines UNSEL SSL at a sensing

operation *may be substantially the same as that described with reference to FIG. 3, and a description thereof is thus omitted.*” Nam, [0122]. There, and as shown above,¹⁰ Nam discloses that application of Vread terminates when the sensing operation begins: “after boosting charges of the unselected strings ST2 to ST4 are discharged or shared, bit lines BLi and BLi+1 may be pre-charged, **a ground voltage GND may be applied to the unselected string selection lines** SSL2, SSL3 and SSL4, a read voltage Vr may be applied to the selected word line WLm-3, and the read pass voltage Vread may be applied to the remaining word lines WL0 to WLm-4 and WLm-2 to WLm. *Under this bias condition, a sensing operation may be performed*” *Id.*, [0096]; Liu, ¶¶ 204-05.

Thus, Nam discloses *applying, on an unselected top select gate of an unselected memory string* (e.g., UNSEL SSL), *a prepare voltage during a first time period* (e.g., Vread during WL Setup) *and an off voltage during a second time period* (e.g., GND during 1st and 2nd read periods). Liu, ¶ 208.

¹⁰ The applied voltage transitions from *Vread to ground* at the start of the sensing period (1st and 2nd reads) and then after sensing, transitions from *ground to Vread*, further demonstrating that during the sensing, “a ground voltage GND may be applied to the unselected string selection lines.” Nam, [0096], FIG. 10; Liu, ¶¶ 206-207.

[1.B] “applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period;”

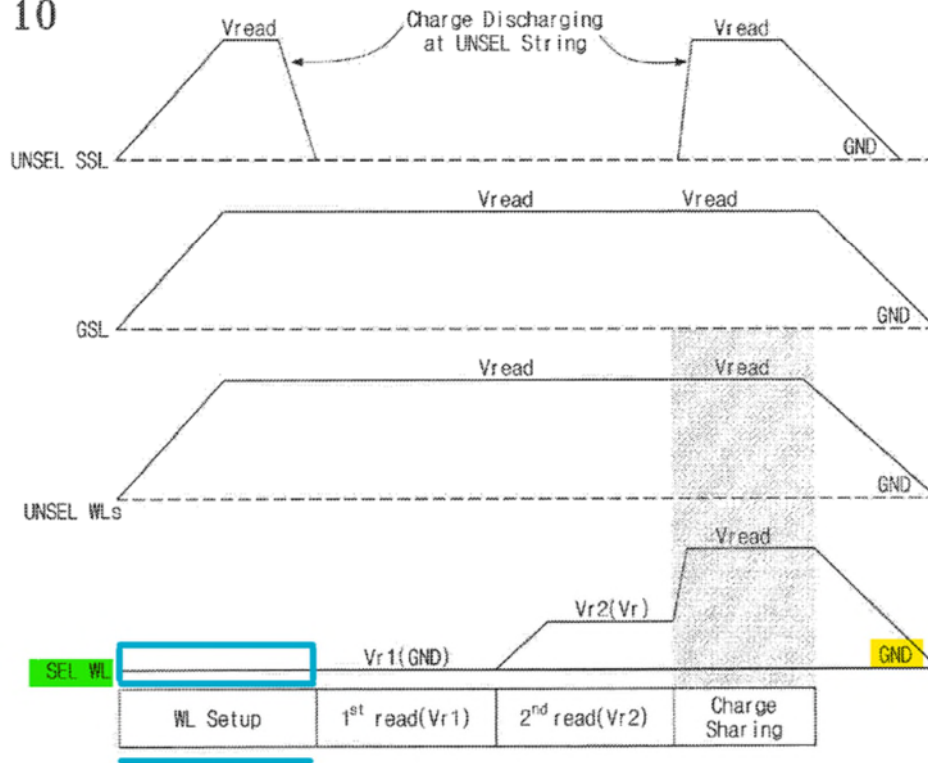
Nam discloses this limitation.

Nam describes how the “data stored” within a *memory cell* can be “determined through read operations.” Nam, [0104]. This “read operation” occurs on “memory cells” that correspond to “the selected wordline” (i.e., *selected word line associated with the target memory cell*), *id.*, [0094]-[0096] (“a sensing operation may be performed to detect on or off states of memory cells corresponding to the selected word line”).

Nam discloses how “[i]n the word line setup section WL Setup [*the first time period*], a ground voltage GND may be applied to a selected word line SEL WL.”¹¹ Nam, [0105].

¹¹ GND may be 0 volts. Nam, [0100].

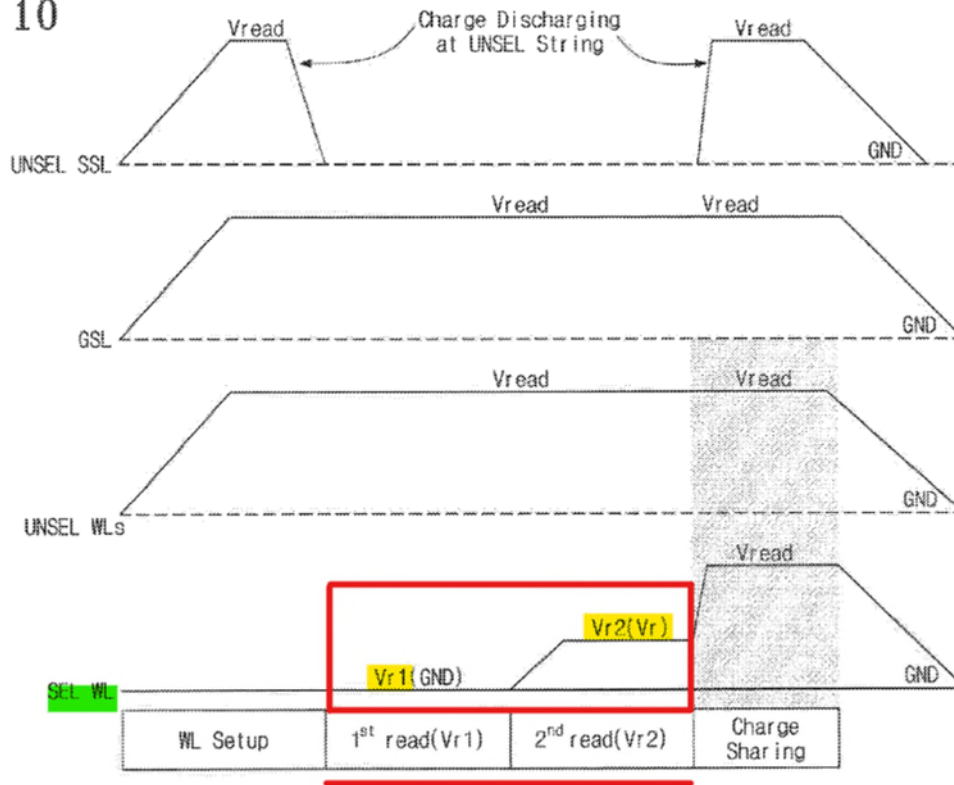
Fig. 10



Id., FIG. 10 (annotated).

Next, in the “first read section read” and “second read section” (*the second time period*), a “sensing operation may be performed.” Nam, [0106]. This involves applying a “read voltage V_r ,” such as “a first read voltage $Vr1$ ” and “a second read voltage $Vr2$ ” to the selected wordline. *Id.*, [0096], [0104], [0106].

Fig. 10



Id., FIG. 10 (annotated).

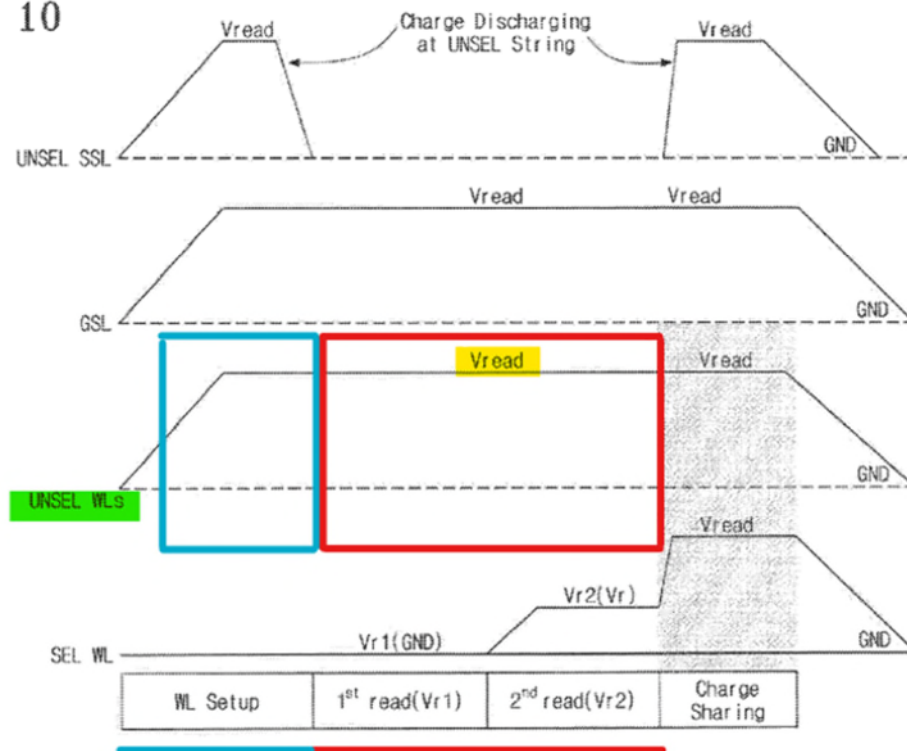
Thus, Nam discloses *applying, on a selected word line associated with the target memory cell* (e.g., SEL WL), *the off voltage during the first time period* (e.g., Ground during WL Setup) *and a read voltage during the second time period* (e.g., Vr1(GND) during 1st read period and Vr2(Vr) during 2nd read period). Liu, ¶¶ 209-13.

[1.C] “applying, on an unselected word line, a pass voltage during the first time period and the second time period,”

Nam discloses this limitation.

During both the WL Setup (*the first time period*) and the 1st and 2nd reads (*the second time period*), Nam discloses that a “read pass voltage Vread may be applied to the remaining word lines,” i.e., *unselected word lines*. Nam, [0096], [0105] (“[i]n the word line setup section WL Setup [*the first time period*], . . . a read pass Vread voltage may be applied to unselected word lines UNSEL WLs”).

Fig. 10



Id., FIG. 10 (annotated).

Thus, Nam discloses *applying, on an unselected word line* (e.g., UNSEL WLs), *a pass voltage during the first time period and the second time period* (e.g., read pass Vread during WL Setup, and 1st and 2nd reads). Liu, ¶¶ 214-16.

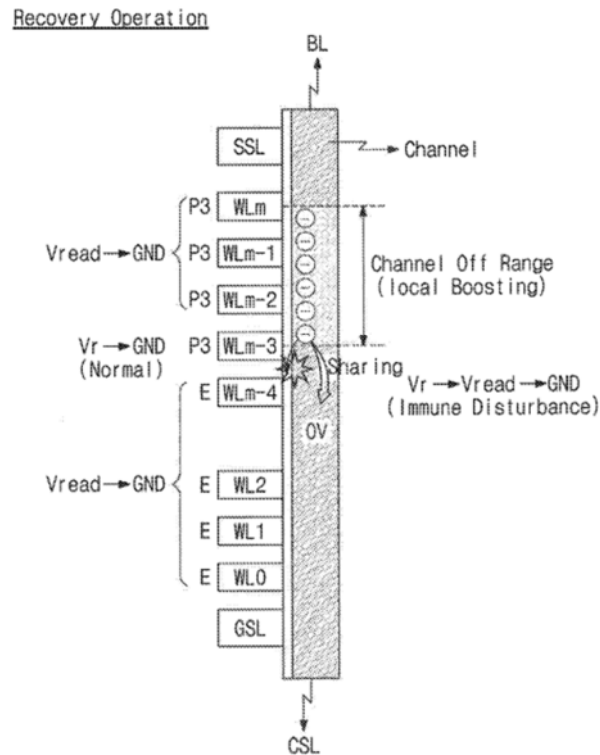
[1.D] “wherein the read-verification operation removes fast charges of the target memory cell during the first time period”

Nam discloses this limitation or, at a minimum, renders it obvious in view of Choi. Liu, ¶ 217.

As an initial matter, Nam discloses several times that its memory may include charge-trap memory cells. Liu, ¶¶ 218-21.

First, Nam broadly describes its memory as applicable to “NAND flash memory.” Nam, [0164], Claim 24. NAND flash memory includes charge-trap memory cells. Ex. 1017, 101. Second, Nam depicts a charge-trap device:

Fig. 5



Nam, FIG. 5, [0099]. As shown above, the 3D vertical channel includes a solid, continuous memory channel, unlike conductive gate memories. Ex. 1017, 105, 145-48.

At a minimum, given these multiple disclosures, a POSITA would have found that Nam's teachings are applicable to charge-trap devices. §IX.A.1[1.D] discusses that charge-trap memories were obvious in view of disclosures relating to 3D Flash, which Nam discloses. See §IX.B.2[1.Pre]; Liu, ¶ 222.

Next, as described above, Nam teaches the requisite waveforms for the claimed *read-verification operation*. See limitations [1.A]-[1.C]. Specifically, Nam teaches having a higher voltage on unselected WLs (including WLs adjacent to the

selected WL) relative to the selected WL during the *first time period*, WL Setup. *Id.* In charge trap devices, this creates a lateral electric field that removes fast charges. *See* Ex. 1001, 12:24-34; *see also* §VIII.C; Liu, ¶ 223.

To the extent that Patent Owner argues that Nam is deficient because it does not recite removing fast charges, Nam in view of Choi render this limitation obvious. *See* §IX.B.4. Choi expressly teaches that voltage differential removes fast charges. *See* §IX.A.1[1.D]. Thus, in view of Choi, a POSITA would have understood that Nam's read-verification operation removes fast charges in a charge-trap memory. Liu, ¶ 224.

Accordingly, Nam discloses, or at least in view of Choi renders obvious, *wherein the read-verification operation removes fast charges of the target memory cell during the first time period* (e.g., voltage differential from the read-verification operation removes charge from Nam's charge trap memory cells). Liu, ¶ 225.

3. Claim 7

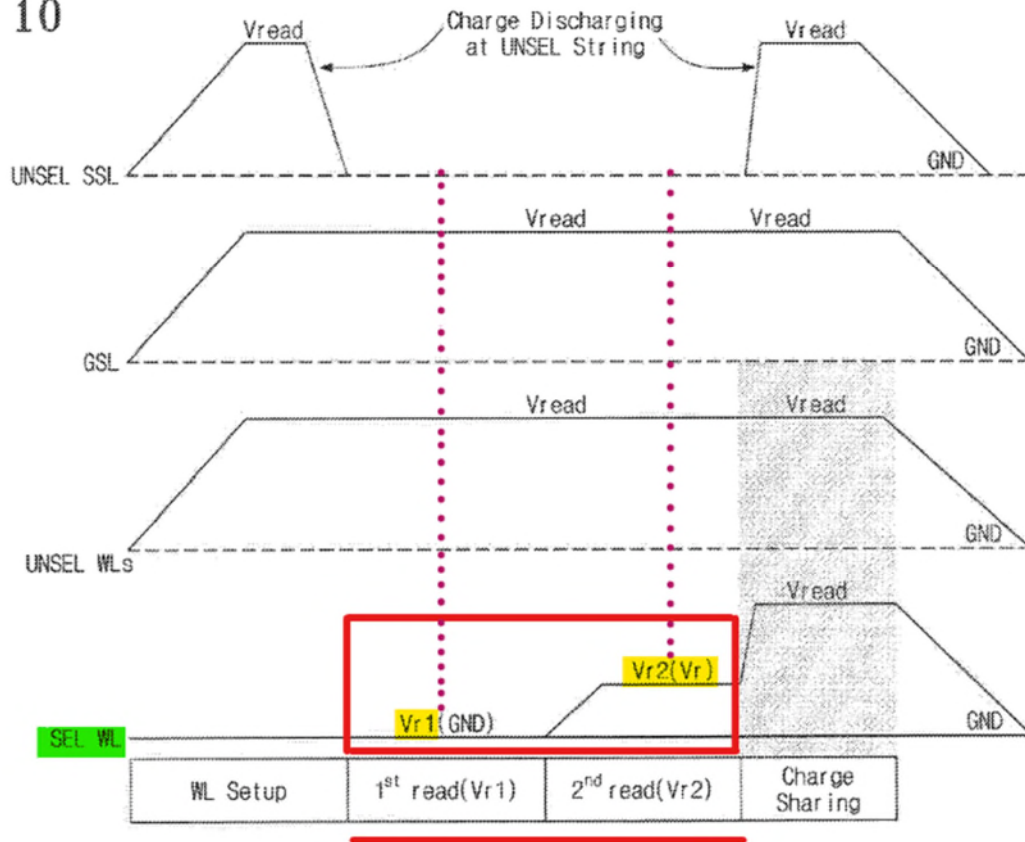
Claim 7 depends from claim 1 and further requires:

[7] “wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell.”

Nam discloses, or at least renders obvious, this limitation. Liu, ¶¶ 226-27.

Recall that *applying the read voltage during the second time*, and more specifically, *applying the read voltage*, refers to when Vr1 and Vr2 are applied. See §IX.B.2[1.B].

Fig. 10



Nam, FIG. 10 (annotated); limitation [1.B]; Liu, ¶ 228.

When this occurs, the *voltage of the unselected top select gate* is 0 volts. As described below, it would have been understood, or at least obvious, that 0V *equals to a threshold voltage of an unselected memory cell*, e.g., an erased cell. Liu, ¶¶ 229-32.

As §IX.A.2 explains, after a block erase and program operations, there will be unselected memory cells that have threshold voltages corresponding to E, P1, P2, and P3 (after the programming progresses past the first row) and both bottom to top and top to bottom programming was obvious. Nam, [0098] (showing data states E and P1-3), FIG. 4 (threshold states); Ex. 1017, 91-93 (conventional block erase); *see also* Nam, [0024] (“program/erase cycle” of block); Ex. 1024, [0115], [0130] (bottom up or top to bottom programming); Ex. 1025, 8:18-53 (benefits of knowing row states). And as a POSITA would have known, erased memory cells in some embodiments may have a zero threshold voltage. *See* §V.A.2; Liu, ¶ 230.

Moreover, Nam discloses a memory device comprising program and erase operations. Ex. Nam, [0069]. Nam further specifically discloses an erased state E and three programmed data states P1, P2, and P3. *Id.*, [0098], FIG. 4. Although Nam illustrates its data states with a typical non-zero threshold-voltage distribution, that is merely “an exemplary embodiment.” *Id.*, [0098]. Recall that a POSITA would have understood that the erased state E threshold window may be entirely in the negative domain or may include a zero threshold voltage within its window. §V.A.2. This selection of the erased threshold voltage window is a choice among a finite number of possible windows. *Id.* And including zero volt in the erased state’s threshold window was not only well known, but an implementation of major memory device manufacturers. *Id.* Indeed, it was well understood how to

implement these various windows for access operations. *Id.* Thus, it would have been obvious to configure a memory device to comprise an unselected memory cell having a zero threshold voltage. *Geo. M. Martin*, 618 F.3d at 1302; Liu, ¶ 231.

Thus, some of the unselected memory cells will be in the erased state and, therefore as explained in §IX.A.2, one or more such cells in some embodiments have a zero threshold voltage, equal to the *voltage of the unselected top select gate*. Liu, ¶ 232; *Unwired Planet*, 841 F.3d at 1002.

4. Motivation to Combine

A POSITA would have been motivated, with a reasonable expectation of success, to apply Choi's teachings to Nam regarding fast charge removal and charge-trap memory cells. Liu, ¶ 233.

First, both Nam and Choi address issues in the field of 3D NAND flash memory, and more specifically, read operations. Nam, [0013]-[0017], [0030]; Choi, 1:14-26. And Choi describes the physics underlying certain of these issues (fast charges). Thus, a POSITA would have been motivated to consider Choi to understand and improve on Nam's memory device. Liu, ¶ 234.

Second, Nam focuses on post-read disturbance while Choi focuses on fast-charge loss. *See* §§VIII.B-C. In other words, Choi's teachings are particularly instructive to Nam's WL Setup, which Nam does not detail. Thus, a POSITA would

have been motivated to consider Choi's teachings to improve and understand issues relating to the WL Setup period. Liu, ¶ 235.

Third, Nam creates a voltage differential by applying a higher voltage on unselected word lines than on the selected word lines during the first time period (WL Setup). *See* §IX.B.2[1.D]. A POSITA would have been motivated to consider the effect of this, which Choi addresses. And Choi expressly teaches the effect in the context of program-verify operations. Choi, FIG. 2; Liu, ¶ 236.

Fourth, while Nam does not detail its charge-trap memory cell disclosures, Choi details the various components. Choi also details the advantages of charge-trap memories. *See* §IX.A.3; Liu, ¶ 237.

A POSITA would have had a reasonable expectation of success in applying Choi's fast-charge-removal and charge-trap memory cell teachings to Nam. Liu, ¶¶ 238-42. First, Nam's memory is structurally similar to Choi's from a high-level perspective. *Compare* Nam, FIGs. 2A, 2B, 5 *with* Choi, FIGs. 1, 5. Second, Choi teaches the device physics of Nam's read operation as it relates to fast charges, thus detailing Nam's operational characteristics. Third, Choi makes clear that Nam's read operation would remediate fast charge issues in a verification that occurs close in time to a program operation. Finally, charge-trap memories were textbook material in 2019. *See* §IX.A.3.

X. SECONDARY CONSIDERATIONS

Petitioner is unaware of any applicable secondary considerations of nonobviousness. None were identified during prosecution. *See generally* Ex. 1002. Even if such considerations existed, none would overcome the strong *prima facie* showing of obviousness.

XI. CONCLUSION

For the foregoing reasons, Petitioner respectfully requests institution of IPR and cancellation of claim 7.

Petition for *Inter Partes* Review of U.S. Patent No. 11,600,342

Respectfully submitted,

ORRICK, HERRINGTON & SUTCLIFFE LLP

Dated: May 17, 2024

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CERTIFICATE OF COMPLIANCE

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW complies with the type volume limitation in 37 C.F.R. § 42.24(a). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 10,098 words.

Dated: May 17, 2024

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing Petition for *Inter Partes* Review and associated exhibits were caused to be served on May 17, 2024 via overnight courier upon the following counsel of record for Patent Owner:

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