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Nathaniel Frank-White

Nathaniel E Frank-White

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2016 VLSI TECHNOLOGY SYMPOSIUM

2016 Symposia on VLSI Technology and Circuits

2016 VLSI CIRCUITS SYMPOSIUM

PROGRAM

VLSI Program

Schedule of Events:

Tuesday, June 14
Joint Reception – Palace Lounge, 7:15 p.m. – 8:00 p.m.
Joint Technology/Circuits Panel Session – Tapa II, 8:00 p.m. – 10:00 p.m.
Technology Panel Session – Tapa I, 8:00 p.m. – 10:00 p.m.

Wednesday, June 15
Executive Panel – Coral Ballrooms 4 & 5, 5:20 p.m. – 6:50 p.m.
Joint Luau Banquet – Great Lawn, 7:00 p.m. – 9:00 p.m.

Thursday, June 16
Luncheon Talk – Nautilus Suite, 12:15 p.m. – 1:30 p.m.
Solid State Circuits Society Young Professionals, Honolulu Lanai, 6:00 p.m. – 8:00 p.m.
Circuits Evening Panel Sessions, Tapa I and II, 8:00 p.m. – 10:00 p.m.

Friday, June 17
Solid State Circuits Society 30th Symposium on VLSI Circuits Luncheon for SSCS Members, Honolulu Suite, 12:15 p.m. – 1:30 p.m.

For full program information, click on the buttons below.

Technology Program | Circuits Program | Program at a Glance - PDF | Program Glance - Excel (download)

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2016 Symposia on VLSI Technology and Circuits announces call for papers

The official Call for Papers has been issued for the 2016 Symposia on VLSI Technology and Circuits, to be held at the Hilton Hawaiian Village June 13-16, 2016 (Technology) and June 15-17, 2016 (Circuits). The deadline for paper submissions to both conferences is January 25, 2016. The late-news paper submissions deadline for the Symposia on VLSI Technology is March 24, 2016; there is no late-news submission for the Symposium on VLSI Circuits. Complete details for paper submission can be found online at: http://www.vlsisymposium.org/authors/

For the past 28 years, the combined annual Symposia on VLSI Technology and Circuits has provided an opportunity for the world's top device technologists, circuit and system designers to engage in an open exchange of leading edge ideas at the world's premier mid-year conference for microelectronics technology. Held together since 1987, the Symposia on VLSI Technology and Circuits have alternated each year between sites in the US and Japan, enabling attendees to learn about new directions in the development of VLSI technology & circuit design through the industry's leading research and development presentations.

The comprehensive technical programs at the two Symposia are augmented with short courses, invited speakers and several evening panel sessions. Since 2012, the Symposia have presented joint focus sessions that include invited and contributed papers on topics of mutual interest to both technology and circuit attendees.

The Symposium on VLSI Technology seeks technical innovation and advances in all aspects of IC technology, as well as the emerging IoT (Internet of Things) field, including:

- ***IoT systems & technologies***, including ultra-low power, heterogeneous integration, sensors, connectivity, power management, digital/analog, microcontrollers and application processors
- ***Stand-alone & embedded memories***, including DRAM, SRAM, non-volatile and emerging memory technologies
- ***CMOS Technology, microprocessors & SoCs***, including scaling, VLSI manufacturing concepts and yield optimization
- ***RF / analog /digital technologies*** for mixed-signal SoC, RF front end; analog, mixed-signal I/O, high voltage, imaging, MEMS, integrated sensors
- ***Process & material technologies***, including advanced transistor process and architecture, modeling and reliability; alternate channel; advanced lithography, high-density patterning; SOI and III-V technologies, photonics, local interconnects and Cu/optical interconnect scaling
- ***Packaging technologies & System-in-Package (SiP)***
- ***Photonics Technology & "Beyond CMOS" devices***

The Symposium on VLSI Circuits seeks original papers showcasing technical innovations and advances in the following areas:

- ***Digital circuits and processor techniques*** for standalone and embedded processors
- ***Memory circuits, architectures & interfaces*** for volatile and non-volatile memories, including emerging memory technologies
- ***Clock generation and distribution*** for high-frequency digital and mixed-signal applications
- ***Analog and mixed-signal circuits***, including amplifiers, filters and data converters
- ***Wireline receivers & transmitters***, including circuits for inter-chip and long-reach applications
- ***Wireless receivers & transmitters***, including circuits for WAN, LAN, PAN, BAN, inter-chip and mm-wave applications
- ***Power management circuits***, including battery management circuits, voltage regulators, energy harvesting circuits
- ***Application-oriented circuits & VLSI systems***, imagers, displays, and sensors for biomedical and

- ***Application-oriented circuits & VLSI systems***, imagers, displays, and sensors for biomedical and healthcare applications

Joint technology and circuits focus sessions feature invited and contributed papers highlighting innovations and advances in materials, processes, devices, integration, reliability and modeling in the areas of advanced memories, 3D integration, and the impact of technology scaling on advanced circuit design. Submissions are strongly encouraged in the following areas of joint interest:

- ***Design in scaled technologies***: scaling of digital, memory, analog and mixed-signal circuits in advanced CMOS processes
- ***Design enablement***: design for manufacturing, process/design co-optimization, on-die monitoring of variability and reliability
- ***Embedded memory technology & design***: SRAM, DRAM, Flash, PCRAM, RRAM, MRAM and NVRAM memory technologies
- ***3D & heterogeneous integration***: power and thermal management; inter-chip communications, SIP architectures and systems

Papers sought for "big integration"

Authors are encouraged to submit papers that showcase innovations that extend beyond single ICs and into the module, including focus areas in the Internet of Things (IoT), industrial electronics, "big data" management, biomedical applications, robotics and smart cars. These topics will be featured in focus sessions as part of the program.

Best Student Paper Award

Awards for best student paper at each Symposia will be chosen, based on the quality of the papers and presentations. The recipients will receive a financial award, travel cost support and a certificate at the opening session of the 2017 Symposium. For a paper to be reviewed for this award, the author must be enrolled as a full-time student at the time of submission, must be the lead author and presenter of the paper, and must indicate on the web submission form that the paper is a student paper.

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VIPack™ IV FOSiP

2016 Symposia on VLSI Technology & Circuits

06/13/2016 - 06/16/2016 -All Day

Location: Hilton Hawaiian Village

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The annual Symposium on VLSI Technology and Circuits will be held at the Hilton Hawaiian Village, Honolulu, Hawaii from June 13-16, 2016 (Technology) and June 14-17, 2016 (Circuits). The theme of this year's program is "Inflections for a Smart Society." The program includes focus sessions, panel discussions and short courses, including focus sessions on "**Systems & Embedded Memory**" and "**Interconnect & 3D Integration,**", and panel discussions, **"How Moore's Law, Industry Consolidation and System Trends Are Shaping the Memory Roadmap,"** **"More Moore, More than Moore or Mo(o)re Slowly?"**

This year marks the 36th anniversary for the Symposium on VLSI Technology, and the 30th anniversary for the Symposium on VLSI Circuits. The two conferences have been held together since 1987, providing an opportunity for the world's top device technologists, circuit and system designers to exchange leading edge research on microelectronics technology, with alternating venues between Hawaii and Japan.

Sponsoring Organizations

The Symposium on VLSI Technology is sponsored by the IEEE Electron Devices Society and the Japan Society of Applied Physics, in cooperation with the IEEE Solid State Circuits Society.

The Symposium on VLSI Circuits is sponsored by the IEEE Solid State Circuits Society and the Japan Society of Applied Physics, in cooperation with the Institute of Electronics, Information and Communication Engineers.

Find further information, registration and a complete program at: http://www.vlsisymposium.org.

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UPCOMING EVENTS

2023 Symposium on VLSI Technology & Circuits: Call for Papers Closes Feb. 1
Feb 1, 2023

2022 Phil Kaufman Award Ceremony and Banquet Honoring Dr. Giovanni De Micheli
Feb 23, 2023

TestConX 2023 - Call for Presentations
Mar 5, 2023

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PAST EVENTS

Inaugural Chiplet Summit Set for January 24-26
Jan 24, 2023

SEMICON Japan 2022 to Spotlight Innovations Driving Semiconductor Industry Growth

Dec 14, 2022

68th Annual IEEE International Electron Devices Meeting

Dec 3, 2022

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'Inflections for a Smart Society' theme for Hawaii's June symposia on VLSI technology and circuits

01 April, 2016 at 9:00 AM Posted by: Sheetal Kumbhar

As semiconductor scaling continues, the microelectronics industry faces a new inflection point, building upon the heterogeneous integration of leading-edge and mature technologies, and driving 'smart' system level applications which will transform the industry.

As an international conference on semiconductor technology that defines the pace, progress and evolution of microelectronics, the annual *Symposia on VLSI Technology & Circuits* (June 13 – 17, Hilton Hawaiian Village, Honolulu, HI, USA) have made this industry transition its focal point, with the conference theme *'Inflections for a Smart Society'* serving as the thread connecting keynote presentations, panel discussions, focus sessions and short courses, reflecting the robust and diverse innovation taking place in the microelectronics industry.

"The Internet of Things, 'Big Data' and smart cars have put the centre of gravity around heterogeneous integration, with RF, mixed signal, digital and packaging technologies in the first row," said Raj Jammy, Symposium on VLSI Technology general chair. "As we reach the limits of geometric scaling, we must add a critical functional scaling dimension to our technology innovation through 3D, embedded emerging memories, system-in-package."

"To investigate innovative system directions for a smart society, the conference will focus on areas where the 'Internet of Things' is transforming industrial electronics, 'Big Data' management, biomedical applications, robotics and smart cars," explained Jeffrey Gealow, Symposium on VLSI Circuits general chair. "To achieve this transformation, the Symposia continue to focus strongly on design/technology co-optimisation."

Both plenary sessions reinforce the inflection theme, with the Symposium on VLSI Technology opening with an address on **"Future Automotive Technology"** by Takao Asami, Nissan's senior vice president; and followed by a review of "*How MEMS Sensors Will Enable the Next Wave of New Products*," by Stephen Lloyd, VP of engineering and new product development at **InvenSense, Inc**.

The Symposium on VLSI Circuits will highlight the industry's "More-than-Moore" drivers with a plenary presentation on *"Accelerating the Sensing World Through Imaging Evolution"* by Tetsuo Nomoto, **Sony**'s vice-president and senior general manager.

As part of the unique Symposia program, there will be joint Technology and Circuits focus sessions, including a joint panel discussion on examining **"***More Moore, More than Moore or Mo(o)re Slowly***,"** a topic that underlines the industry's current soul searching.

In addition, an executive panel will discuss "*Semi Business beyond Scaling*," formed by industry executives addressing the question on how inflections that go beyond traditional

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Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND flash memory

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13 Author(s)
Bongsik Choi ; Sang Hyun Jang ; Jinsu Yoon ; Juhee Lee ; Minsu Jeon ; Yongwoo Lee ; Jungmin Han ; Jieun Lee ; Dong... View All Authors

Abstract:
A fast charge loss within a few seconds, which is referred to as early retention, was observed in tube-type 2y word-line stacked 3-D NAND flash memory for the first time, and the origin of the early retention was comprehensively evaluated. Using a fast-response pulse I-V system, the early retention characteristics from microseconds to seconds were thoroughly investigated, and the correlations with various program and erase levels were examined using solid and checkerboard patterns. Our findings indicate that the early retention mainly originates from the lateral charge loss through the shared charge trap layers and suggest that the program and erase levels should be balanced and optimized to reduce the early retention.

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SECOND ANNOUNCEMENT AND CALL FOR PAPERS

2016 SYMPOSIUM ON VLSI Technology

Hilton Hawaiian Village, HONOLULU, Hawaii, USA
Monday – Thursday, June 13-16, 2016
(June 13 Short Course,
June 14-16 Technical Sessions)

The 2016 Symposium on VLSI Technology welcomes the submission of original papers on all aspects of IC and IoT technology. The VLSI Circuits Symposium will be held at the same location with two days of overlap. A single registration allows participants to attend both Symposia, to synergize on topics of joint interest and to gain an excellent overview of the interactive technology-circuits fields.

Symposium Scope

Papers will be selected based on technical innovation, advances relative to previously published work, credibility of claims, and quality of writing and illustrations. The scope includes:

- **IoT Systems and Technologies** including ultra-low power technologies; heterogeneous integration; sensors, display, connectivity; power management; digital/analog, micro-controllers and application processors.
- **Stand-Alone and Embedded Memories** technology and reliability for DRAM, SRAM, Non-Volatile, Emerging Memories.
- **CMOS Technology, Microprocessors and SoCs** including scaling, VLSI manufacturing concepts, and yield optimization.
- **RF / Analog / Digital Technologies** for mixed-signal SoC; RF front end; analog, mixed-signal, I/O, high-voltage, imaging, MEMS, integrated sensors.
- **Process and Material Technologies** including advanced transistor process and architecture, modeling and reliability; alternate channel; advanced lithography, high-density patterning; SOI and III-V technologies; photonics; local interconnects and Cu/optical interconnects scaling.
- **Packaging Technologies and System-in-Package (SiP)** including through-silicon-vias (TSVs) and 3D-system integration.
- **Photonics Technology and Beyond CMOS Devices**

Best Student Paper Award

Best Student Paper Award selection will be based on quality and presentation of the paper at the Symposium. The winning student will be presented a monetary award and a certificate at the 2017 Symposium opening session. The student must be enrolled as a full-time student at the time of submission, be the leading author and presenter of the paper, and indicate when submitting the paper that the paper should be considered for the award.

Joint Technology and Circuits Focus Sessions

Joint technology and circuits focus sessions will be offered in the following special topics of joint interest:

- **Design in scaled technologies:** scaling of digital, memory, analog and mixed-signal circuits in advanced CMOS processes
- **Design enablement:** design for manufacturing, process-design co-optimization, on-die monitoring of variability and reliability
- **Embedded memory technology and design:** SRAM, DRAM, Flash, PCRAM, RRAM, MRAM, etc.
- **3D and heterogeneous integration:** power and thermal management, inter-chip communication, SiP architectures and applications

Innovative System Directions

Authors are encouraged to submit papers on "big integration" that showcase innovations that extend beyond a single IC and into the module. These include focus areas of **Internet of Things, Industrial Electronics, Big Data Management, Biomedical** and **Robotics and Smart cars**. New focus sessions comprising invited and contributed papers will be offered.

Paper Submission

Prospective authors must submit two-page papers and abstracts using the Symposia's website, www.vlsisymposium.org. Accepted papers will be published as submitted, with **no revisions permitted**. Authors must follow detailed instructions provided within the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. The technical content beyond the abstract of the accepted paper must not be announced, published, or in any way put in the public domain prior to the Symposium. Partial travel expense support for students who are presenting papers is available upon request.

Information and Registration

The Symposia's website provides additional information, including information regarding Symposium registration and hotel reservations. To obtain assistance with any aspect of the Symposium, please contact the appropriate Secretariat.

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Paper Submission Deadline: 23:59 PST, January 25, 2016
Late News: March 24

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