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March 15, 2024

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APPLICATION NUMBER: *15/410,965*
FILING DATE: *January 20, 2017*
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ISSUE DATE: *September 03, 2019*

Certified by

Performing the Functions and Duties of the
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PTO/AIA/14 (11-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	MXIC 2194-1
	Application Number	
Title of Invention	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1 — Remove

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	HANG-TING		LUE	

Residence Information (Select One) US Residency ● Non US Residency Active US Military Service

City	HSINCHU	Country of Residence [i]	TW

Mailing Address of Inventor:

Address 1	C/O MACRONIX NO. 16 LI-HSIN ROAD
Address 2	SCIENCE-BASED INDUSTRIAL PARK

City	HSINCHU	State/Province	
Postal Code		Country [i]	TW

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	46353		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE		
Attorney Docket Number	MXIC 2194-1	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	12	**Suggested Figure for Publication (if any)**	

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Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

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Please Select One:	● Customer Number	US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	46353		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)

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Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)[i] the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

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Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

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The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	MXIC 2194-1
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Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1 — Remove

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

● Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.	Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	MACRONIX INTERNATIONAL CO., LTD.		
Mailing Address Information For Applicant:			
Address 1	NO. 16 LI-HSIN ROAD		
Address 2	SCIENCE-BASED INDUSTRIAL PARK		
City	HSINCHU	**State/Province**	
Country	TW	Postal Code	
Phone Number		Fax Number	
Email Address			

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Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

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If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	MACRONIX INTERNATIONAL CO., LTD.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	NO. 16 LI-HSIN ROAD		
Address 2	SCIENCE-BASED INDUSTRIAL PARK		
City	HSINCHU	**State/Province**	
Country i	TW	Postal Code	
Phone Number		Fax Number	
Email Address			

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Signature:

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See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Yiding Wu/			Date (YYYY-MM-DD)	2017-01-20
First Name	YIDING	Last Name	WU	Registration Number	65992

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This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3 A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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Attorney Docket No. MXIC 2194-1
(P1050004US)

DECLARATION (37 C.F.R. 1.63) FOR UTILITY PATENT APPLICATION USING AN APPLICATION DATA SHEET (37 C.F.R. 1.76) AND ASSIGNMENT

Title of Invention: **DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE**

As a below named inventor, I hereby declare that:

This declaration is directed to the attached application, or (if following box is checked):

[ ] United States application or PCT international application number _____ filed on _____.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I have reviewed and understand the contents of the application, including the claims.

I am aware of the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR Section 1.56.

Whereas, the undersigned inventor(s) has/have made certain inventions, improvements, and discoveries (herein referred to as the "Invention") disclosed in the above-identified patent application and further identified by the Docket Number provided above in the header of this document;

Whereas, Macronix International Co., Ltd., a corporation of Taiwan having a place of business at No. 16 Li-Hsin Road, Science-Based Industrial Park, Hsinchu, Taiwan (herein referred to as "Macronix"), desires to acquire, and each undersigned inventor desires to grant to Macronix, the entire worldwide right, title, and interest in and to the Invention and in and to any and all patent applications and patents directed thereto;

Now, therefore, for good and valuable consideration, the receipt and sufficiency thereof being hereby acknowledged, each undersigned inventor ("ASSIGNOR") hereby sells or has sold, assigns or has assigned, and otherwise transfers or has transferred to Macronix (the "ASSIGNEE"), its successors, legal representatives, and assigns, the entire worldwide right, title, and interest in and to the Invention, the above-identified United States patent application, and any and all other patent applications and patents for the Invention which may be applied for or granted therefor in the United States and in all foreign countries and jurisdictions, including all divisions, continuations, reissues, reexaminations, renewals, extensions, counterparts, substitutes, and extensions thereof, and all rights of priority resulting from the filing of such applications and granting of such patents. In addition, each undersigned inventor hereby authorizes and requests the Director of the United States Patent and Trademark Office to issue any United States Patent, and foreign patent authorities to issue any foreign patent, granted for the Invention, to Macronix, its successors, legal representatives, and assigns, the entire worldwide right, title, and interest in and to the same to be held and enjoyed by Macronix, its successors, legal representatives, and assigns to the full end of the terms for which any and all such patents may be granted, as fully and entirely as would have been held and enjoyed by the undersigned had this Assignment not been made; and each undersigned inventor agrees to execute any and all documents and instruments and perform all lawful acts reasonably related to recording this Assignment or perfecting title to the Invention and all related patents

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and applications, in Macronix, its successors, legal representatives, and assigns, whenever requested by Macronix, its successors, legal representatives, or assigns.

Each undersigned inventor acknowledges their prior and ongoing obligations to sell, assign, and transfer the rights under this Assignment to Macronix and is unaware of any reason why they may not have the full and unencumbered right to sell, assign, and transfer the rights hereby sold, assigned, and transferred, and has not executed, and will not execute, any document or instrument in conflict herewith. Each undersigned inventor also hereby grants Macronix, its successors, legal representatives, and assigns, the right to insert in this Assignment any further identification (including, but not limited to, patent Application Number) which may be necessary or desirable for recordation of this Assignment.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

(1) Legal Name of Inventor: HANG-TING LUE 呂函庭

Signature: Hang-Ting Lue Date: 2016.12.27

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DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE

Inventor: Hang-Ting Lue 呂函庭

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to high density memory devices, and particularly to memory devices in which multiple planes of memory cells are arranged to provide a three-dimensional 3D array.

Description of Related Art

[0002] As critical dimensions of devices in integrated circuits shrink to the limits of common memory cell technologies, designers have been looking to techniques for stacking multiple planes of memory cells to achieve greater storage capacity, and to achieve lower costs per bit. For example, thin-film transistor techniques are applied to charge trapping memory technologies in Lai, *et al.*, "A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory," IEEE Int'l Electron Devices Meeting, 11-13 Dec. 2006; and in Jung *et al.*, "Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node," IEEE Int'l Electron Devices Meeting, 11-13 Dec. 2006.

[0003] Three dimensionally stacked NAND flash memory with a charge trap layer (SiN) has a lateral charge migration issue, where lateral charge migration is expected to cause problems because the charge trap layer is shared between word lines. Lateral charge migration can cause unwanted results in a negative shift of the threshold voltage (*VT*) and a positive shift of the string read current immediately after programming. See Choi *et al.*, "Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory," IEEE 2016 Symposium on VLSI Technology Digest of Technical Papers.

[0004] It is desirable to provide a structure for three-dimensional integrated circuit memory including a charge trap layer (SiN) without lateral charge migration issues.

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SUMMARY

[0005] A vertical channel memory is described, which can be configured as a 3D NAND flash memory device. The memory device can include discrete charge trapping elements in recessed regions on opposing sidewalls of conductive strips in stacks of conductive strips. In embodiments, the discrete charge trapping elements are dielectric charge trapping elements.

[0006] In an example described herein, the memory device comprises a plurality of stacks of conductive strips alternating with insulating strips, where the insulating strips in the stacks have first and second sides, and the conductive strips in the stacks have first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks.

[0007] The memory device comprises vertical channel pillars disposed between the stacks, where the vertical channel pillars have first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material between and contacting the first and second channel films.

[0008] The memory device comprises data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks. The data storage structures can include tunneling layers in contact with the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips. The discrete charge trapping elements are disposed in the first recessed regions on the first sidewalls of the conductive strips. In embodiments, the discrete charge trapping elements disposed in the first recessed regions are dielectric charge trapping elements.

[0009] The conductive strips in the stacks can have second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions on the second sidewalls of the conductive strips. The data storage structures can include discrete charge trapping elements disposed in the second recessed regions in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements in the second recessed regions and the second sidewalls

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of the conductive strips. In embodiments, the discrete charge trapping elements disposed in the second recessed regions are dielectric charge trapping elements.

[0010] As described herein, discrete charge trapping elements are disposed in the first and second recessed regions on the opposing first and second sidewalls of conductive strips in a plurality of stacks of conductive strips, where the discrete charge trapping elements disposed in the first recessed regions on the first sidewall of conductive strips in a particular stack are separated from the discrete charge trapping elements disposed in the second recessed regions on the second sidewall of conductive strips in an adjacent stack by a vertical channel pillar disposed between the particular stack and the adjacent stack, the vertical channel pillar having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material between and contacting the first and second channel films. At layers of conductive strips in the stacks in a direction along the conductive strips (e.g. X-direction, FIG. 10), the discrete charge trapping elements and the vertical channel pillars are isolated by insulating structures (*e.g.* 1001-1009, FIG. 10) through the layers of conductive strips.

[0011] In one embodiment, the conductive strips in the plurality of stacks of conductive strips can include a semiconductor material such as polysilicon. In another embodiment, the conductive strips in the plurality of stacks of conductive strips can include a metal material such as tungsten.

[0012] The vertical channel pillars can be arranged so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips

[0013] Methods for manufacturing memory devices as described herein are also provided. In one embodiment, a method for manufacturing includes forming stacks of conductive strips including a semiconductor material such as polysilicon. In another embodiment, a method for manufacturing includes forming stacks of conductive strips including a metal material such as tungsten.

[0014] Other aspects and advantages of the present invention can be seen on review of the drawings, the detailed description and the claims, which follow.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0015] Figure 1 is a simplified perspective diagram of a 3D SGVC NAND memory device.

[0016] Figures 2 through 10 illustrate an example process flow for a memory architecture including data storage structures including discrete charge trapping elements.

[0017] Figure 11 is an example flow chart illustrating a manufacturing method for a memory architecture including data storage structures including discrete charge trapping elements.

[0018] Figures 12-17 illustrate an example process flow for an alternative memory architecture including data storage structures including discrete charge trapping elements.

[0019] Figure 18 is an example flow chart illustrating a manufacturing method for an alternative memory architecture including data storage structures including discrete charge trapping elements, using a gate replacement process after forming the data storage structures.

[0020] Figure 19 is a block diagram of an integrated circuit memory including a 3D memory array including discrete charge trapping elements in recessed regions on sidewalls of conductive strips.

DETAILED DESCRIPTION

[0021] A detailed description of embodiments of the present invention is provided with reference to the Figures. It is to be understood that there is no intention to limit the technology to the specifically disclosed structural embodiments and methods but that the technology may be practiced using other features, elements, methods and embodiments. Preferred embodiments are described to illustrate the present technology, not to limit its scope, which is defined by the claims. Those of ordinary skill in the art will recognize a variety of equivalent variations on the description that follows. Like elements in various embodiments are commonly referred to with like reference numerals.

[0022] Figure 1 is a simplified perspective diagram of a 3D NAND flash memory device, according to a 3D vertical channel technology having a structure as described in co-pending U.S. Patent Application No. 14/637,204 (Attorney Docket No. MXIC 2147-

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1B), filed on 3 March 2015, which application is incorporated by reference as if fully set forth herein.

[0023] The memory device includes a plurality of stacks of conductive strips. The plurality of stacks of conductive strips includes even stacks (e.g. 112 and 114) and odd stacks (e.g. 111 and 113). The even stacks of conductive strips 112 and 114 include upper strips configured as string select lines (e.g. SSL0 and SSL1), and intermediate strips configured as word lines (e.g. WL). An even stack (e.g. 112) can also include a dummy strip (e.g. DG1) between the upper strip (e.g. SSL0) and the intermediate strips (e.g. WLs) in the even stack, which is not configured to form a memory cell for data storage.

[0024] The odd stacks of conductive strips (e.g. 111 and 113) in the memory device can include upper strips configured as ground select lines (e.g. GSL0 and GSL1). An odd stack (e.g. 111) can also include a dummy strip (e.g. DG0) between the upper strip (e.g. GSL0) and the intermediate strips (e.g. WLs) in the odd stack, which is not configured to form a memory cell for data storage. At least one of the even stacks and odd stacks of conductive strips can include bottom strips configured as assist gates (AG) disposed below the intermediate strips.

[0025] The stacks of conductive strips can be disposed on an insulating layer 101 which can comprise a silicon oxide or other dielectric on a semiconductor substrate. The stacks 111-114 include layers of insulating material 121, 122, 123, 124, 125 and 126, separating the conductive strips in the stacks from one another. The conductive material can be a polysilicon material or other material selected for compatibility with the data storage structure. The layers of insulating material can comprise silicon dioxide deposited in a variety of ways as known in the art. Also, the layers of insulating material can comprise other insulating materials, and combinations of insulating materials. In this example, all of the insulating layers consist of the same material. In other examples, different materials can be used in different layers as suits a particular design goal.

[0026] Data storage structures 130 are disposed on the sidewalls of the corresponding even and odd stacks of conductive strips. Semiconductor films 140 are disposed on the data storage structures 130 on the sidewalls of the corresponding even and odd stacks. An insulating material 150 such as silicon dioxide is filled between stacks on the inside surfaces of the semiconductor films 140. In one embodiment, the insulating

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material 150 can completely fill the regions between the stacks. In another embodiment, the insulating material 150 can leave an air gap 161 at least in regions adjacent the intermediate strips of conductive strips (e.g. WL).

[0027] Semiconductor films 140 include portions 170 and 171which overlie the odd stacks 111 and 113respectively. Portions 173, 174 and 175 of the semiconductor films 140 overlie the even stack 112. Portions 177, 178 and 179 of the semiconductor films 140 overlie the even stack 114. The portions 170 and 171 connect the semiconductor films having outside surfaces disposed on the data storage structures on the sidewalls of the odd stacks 111 and 113on the common source side of the NAND strings together and provide landing areas for interlayer connectors for connection to a common source line. The portions 173, 174, 175, 177, 178 and 179 are separated and provide landing areas for interlayer connectors making independent connections to bit lines.

[0028] A patterned conductor layer or layers overlie the stacks. A first interlayer connector connects a first conductor *(e.g.* bit lines BL0, BL1, BL2) to a top surface of a first semiconductor film on the data storage structures on the sidewalls of an even stack in the plurality of stacks (e.g. 112, 114). A second interlayer connector connects a second conductor *(e.g.* source reference conductor lines 190 and 194) to a top surface of a second semiconductor film on the data storage structures on the sidewalls of a corresponding odd stack in the plurality of stacks (e.g. 111 and 113).

[0029] Data storage structures 130 can include a tunneling layer 132, a charge storage layer 131, and a blocking layer 133. The data storage structures 130 can include for example dielectric charge trapping materials known as ONO (oxide-nitride-oxide), ONONO (oxide-nitride-oxide-nitride-oxide), SONOS (silicon-oxide-nitride-oxide-silicon), BE-SONOS (bandgap engineered silicon-oxide-nitride-oxide-silicon), TANOS (tantalum nitride, aluminum oxide, silicon nitride, silicon oxide, silicon), and MA BE-SONOS (metal-high-k bandgap-engineered silicon-oxide-nitride-oxide-silicon).

[0030] Semiconductor films 140 have outside surfaces and inside surfaces. The outside surfaces are disposed on the data storage structures on the sidewalls of the corresponding even and odd stacks in the plurality of stacks forming a 3D array of memory cells (e.g. 135). The semiconductor films 140 are connected to form a current

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path 145 from an upper end to a lower end of the semiconductor film on the corresponding even stacks, and from a lower end to an upper end of the semiconductor film on the corresponding odd stacks.

[0031] The even stacks (e.g. 114) in the plurality of stacks include string select switches (e.g. 137) coupled to first string select lines (e.g. SSL1). The string select switches can include the data storage structures 130 on the sidewalls of the even stacks (e.g. 114) in the plurality of stacks. The data storage structures 130 can include charge trapping nitride material such as ONO, as described above.

[0032] Figures 2 through 10 illustrate an example process flow for a memory architecture including data storage structures including discrete charge trapping elements. To form the structure shown in Figure 2, a plurality of layers of a conductive material, such as doped polysilicon, or other material suitable for use as word lines, separated by layers of insulating material are disposed over a substrate (e.g. 200).

[0033] Figure 2 illustrates a stage of the process flow after etching the plurality of layers of the conductive material, to define a plurality of stacks of conductive strips, including stacks 210 and 220, alternating with insulating strips. For instance, stack 210 includes conductive strips 211, 213, 215 and 217 alternating with insulating strips 212, 214, 216 and 218, and stack 220 includes conductive strips 221, 223, 225 and 227 alternating with insulating strips 222, 224, 226 and 228. The conductive strips are disposed in a direction X orthogonal to a YZ plane defined by a Y direction and a Z direction. Each stack can include a bottom plane (GSL) of conductive strips, a plurality of intermediate planes (WLs) of conductive strips, and a top plane of conductive strips (SSLs), as shown in Figure 1. Although as shown in the example of Fig. 2, a trench (e.g. 250) separating two adjacent stacks (e.g. 210, 220) is flush with a top surface of a substrate (e.g. 200), in embodiments, the trench can extend into the substrate.

[0034] As shown in the example of Figure 2, a stack (e.g. 220) or an insulating strip (e.g. 228) can have a width of about 110nm (nanometers), an insulating strip (e.g. 228) can have a thickness of about 20nm, and a conductive strip (e.g. 227) can have a thickness of about 50nm.

[0035] The insulating strips in the stacks have first and second sides. For instance, an insulating strip 218 has a first side 218a and a second side 218b. The conductive strips

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in the stacks have first and second sidewalls. For instance, a conductive strip 217 has a first sidewall 217a and a second sidewall 217b.

[0036] Figure 3 illustrates a stage of the process flow after recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks. For instance, the first sidewall 217a of the conductive strip 217 is recessed relative to the first side 218a of the insulating strip 218 to define a first recessed region 317a in a side of the stack 210. Similarly, first recessed regions 311a, 313a and 315a are formed on respective first sidewalls of the conductive strips 211, 213 and 215 in a first side of the stack 210. Second recessed regions 311b, 313b, 315a and 317b are formed on respective second sidewalls of the conductive strips 211, 213 and 215 in a second side of the stack 210 opposite the first side.

[0037] The conductive material in the conductive strips can be recessed by using isotropic etching technology. As shown in the example of Figure 3, a conductive strip (e.g. 227) can be recessed by about 15 nm (nanometers) on its first sidewall and/or its second sidewall. A polysilicon lateral recess process can be performed by adding NF3, CH3F, CH2F2 with suitable gas and power in the polysilicon etcher tool. An example recipe for the polysilicon lateral recess process can include 180mT/ 500T/TCCT 1.0/100V(DC25%, Freq 200)/gas equal/ 400NF3 /10CH3F/30CH2F2/ 60-60-56-56/ 20-He/20.

[0038] Figure 4-8 illustrate forming a memory layer on sidewalls of conductive strips in the plurality of stacks. The memory layer contacts sidewalls of the conductive strips in the plurality of stacks. The memory layer can comprise a multilayer data storage structure, including tunneling layers, charge trapping material, and blocking layers, examples of which are discussed above. In one preferred example, the memory layer is implemented as illustrated below with reference to Figures 4-8.

[0039] Figure 4 illustrates a stage of the process flow after depositing blocking layers (e.g. 410) over the first sidewalls (e.g. 217a, Fig. 2) of the conductive strips (e.g. 217, Fig. 2) in the first recessed regions (e.g. 317a, Fig. 3). The blocking layers (e.g. 410) can be deposited over the second sidewalls (e.g. 217b, Fig. 2) of the conductive strips (e.g. 217, Fig. 2) in the second recessed regions (e.g. 317b, Fig. 3). The blocking layers

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(e.g. 410) can be deposited over the first sides (e.g. 218a, Fig. 2) and/or the second sides (e.g. 218b, Fig. 2) of the insulating strips (e.g. 218, Fig. 2). For instance, the blocking layers can have a thickness of about 10nm.

[0040] The blocking layers can include a combination of multilayer thin films to optimize erase saturation. For instance, the combination of multilayer thin films can include layers of materials such as High- κ (high dielectric constant as compared to silicon dioxide), capped SiN, ONO (Oxide-Nitride-Oxide, e.g. O4, N3, O3) for double trapping BE-SONOS (Band-gap Engineered Silicon-Oxide-Nitride-Oxide-Silicon). The blocking layers are further described in co-pending U.S. Patent Application No. 14/637,204 (Attorney Docket No. MXIC 2147-1B), filed on 3 March 2015, which application is incorporated by reference as if fully set forth herein.

[0041] Figure 5 illustrates a stage of the process flow after depositing charge trapping material (e.g. 510) over the blocking layers (e.g. 410) in the first recessed regions (e.g. 311a, 313a, 315a, 317a, Fig. 3). In embodiments, the charge trapping material is dielectric charge trapping material. The charge trapping material can be deposited over the blocking layers (e.g. 410) in the second recessed regions (e.g. 311b, 313b, 315b, 317b, Fig. 3). The charge trapping material can be deposited over the blocking layers over the first sides (e.g. 218a) and/or the second sides (e.g. 218b) of the insulating strips (e.g. 218). The charge trapping material can include SiN (silicon nitride). The charge trapping material can have a thickness of about 15nm to 30nm in the first recessed regions and/or the second recessed regions. Although the charge trapping material typically includes SiN, the charge trapping material can include SiON, HfO2, Al2O3, etc.

[0042] As shown in the example of Figure 5, the charge trapping material (e.g. 510) as deposited in the first recessed regions (e.g. 311a, 313a, 315a, 317a, Fig. 3) in a first side of a stack (e.g. 210) may not be separated between adjacent first recessed regions, because the charge trapping material deposited on sides of the insulating strips (e.g. 520) may connect the charge trapping material in adjacent recessed regions. Similarly, the charge trapping material (e.g. 510) as deposited in the second recessed regions (e.g. 311b, 313b, 315b, 317b, Fig. 3) in a second side of a stack (e.g. 210) may not be separated between adjacent second recessed regions.

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[0043] Figures 6, 7 and 10 illustrate methods to separate the charge trapping material into discrete charge trapping elements. In embodiments, the discrete charge trapping elements are dielectric charge trapping elements. Figures 6 and 7 illustrate methods to separate the charge trapping material between adjacent first recessed regions, and between adjacent second recessed regions, in a vertical direction (e.g. the Z-direction). Figure 10 illustrates methods to separate the charge trapping material in the X-direction. In the Y-direction, the charge trapping material (e.g. 510, FIG. 10) is separated by the vertical channel pillars (e.g. 910, 920 and 930, FIG. 10) on one side, and by the conductive strips (e.g. 217, FIG. 10) on an opposite side. The Z-direction is orthogonal to a plane defined by the X-direction and the Y-direction, and the X-direction is orthogonal to the Y-direction.

[0044] Figure 6 illustrates a stage of the process flow after an isotropic etching process is applied to the charge trapping material (e.g. 510), to pull back the charge trapping material towards the conductive strips over whose sidewalls the blocking layers (e.g. 410, Fig. 4) and the charge trapping material (e.g. 510, Fig. 5) are deposited. The isotropic etching process can remove most of the charge trapping material deposited over the blocking layers over the first sides and second sides of the insulating strips, while keeping the charge trapping material in the first recessed regions and the second recessed regions. But a small amount of the charge trapping material (e.g. 620) may still remain over the sides of the insulating strips, connecting the charge trapping material in adjacent recessed regions.

[0045] Figure 7 illustrates a stage of the process flow after an oxidation process is applied to oxidize the charge trapping material (e.g. 510) on sides of the stacks, so that the charge trapping material (e.g. SiN) deposited on sides of the insulating strips can be oxidized into an oxide layer (e.g. SiON) on sides of the stacks, while keeping the charge trapping material (e.g. SiN) in the first recessed regions and the second recessed regions. The oxide layer thus formed can serve as part of the tunneling layers which are described in connection to Figure 8. Consequently, the charge trapping material in adjacent first recessed regions on a first side of the stack are separated from each other in a vertical direction (e.g. Z-direction), as opposed to being connected via the charge trapping material on sides of the insulating strips between adjacent first recessed regions.

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Similarly the charge trapping material in adjacent second recessed regions on a second side of the stack are separated from each other in the vertical direction, as opposed to being connected via the charge trapping material on sides of the insulating strips between adjacent second recessed regions.

[0046] Figure 8 illustrates a stage of the process flow after depositing tunneling layers (e.g. 810) over the charge trapping material in the first recessed regions on the first side of the stacks and in the second recessed regions on the second side of the stacks. The tunneling layers can include a bandgap engineered composite tunneling dielectric layer comprising a layer of silicon dioxide less than 2 nm thick. In one embodiment, the composite tunneling dielectric layer consists of an ultrathin silicon oxide layer O_1 (*e.g.* <=15Å), an ultrathin silicon nitride layer N_1 (*e.g.* < =30Å) and an ultrathin silicon oxide layer O_2 (*e.g.* <=35Å), which results in an increase in the valence band energy level of about 2.6 eV at an offset 15Å or less from the interface with the semiconductor body. The O_2 layer separates the N_1 layer from the charge trapping layer, at a second offset (*e.g.* about 30Å to 45Å from the interface), by a region of lower valence band energy level (higher hole tunneling barrier) and higher conduction band energy level. The electric field sufficient to induce hole tunneling raises the valence band energy level after the second location to a level that effectively eliminates the hole tunneling barrier, because the second location is at a greater distance from the interface. Therefore, the O_2 layer does not significantly interfere with the electric field assisted hole tunneling, while improving the ability of the engineered tunneling dielectric to block leakage during low fields. These layers can be conformally deposited using for example LPCVD.

[0047] Figure 9 illustrates a stage of the process flow after forming vertical channel pillars disposed between the stacks, such as between an odd stack 210 and an even stack 220. The vertical channel pillars are formed by forming first and second channel films (e.g. 910 and 920) on the data storage structures on sidewalls of adjacent stacks, and depositing a dielectric material (e.g. 930) between the first and second channel films (e.g. 910 and 920), where the dielectric material contacts the first and second channel films (e.g. 910 and 920) on the sidewalls of the adjacent stacks. Consequently the vertical channel pillars have first and second channel films disposed on the data storage structures on sidewalls of adjacent stacks in the plurality of stacks and a

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dielectric material between and contacting the first and second channel films. In one embodiment, the dielectric material (e.g. 930) can completely fill the regions between the stacks. In another embodiment, the dielectric material (e.g. 930) can leave an air gap 961 at least in regions adjacent the intermediate strips of conductive strips in the stacks (e.g. 211, 213, 215, 217, 221, 223, 225 and 227).

[0048] The deposition techniques applied to form layers of materials in the data storage structures and channel films can be carried out by LPCVD processes, which provide excellent film quality and conformality required. The data storage structures can include blocking layers (e.g. 410), charge trapping material (e.g. 510), and tunneling layers (e.g. 810). On the other hand, tools such as atomic layer deposition ALD tools can be utilized for these films.

[0049] An even/odd level decoder (e.g. 1950, FIG. 19) can be coupled to a plurality of even/odd word lines such as the conductive strips (e.g. 211, 213, 215, 217, 221, 223, 225, and 227) in the odd stack 210 and the even stack 220 that can act as word lines.

[0050] Figure 10 illustrates a stage of the process flow after etching to isolate the data storage structures (e.g. 1010) along the conductive strips (e.g. 217, 227, 237), to form discrete charge trapping elements (e.g. 510) , and to isolate the first and second channel films (e.g. 910 and 920) and the dielectric material (e.g. 930) between the first and second channel films along the conductive strips, to form vertical channel pillars between the stacks. The discrete charge trapping elements (e.g. 510) are in contact with the tunneling layers (e.g. 810) and the blocking layers (e.g. 410) between the discrete charge trapping elements and the first sidewalls of the conductive strips (e.g. 217). The data storage structures (e.g. 1010) can include the blocking layers (e.g. 410), the discrete charge trapping elements (e.g. 510), and the tunneling layers (e.g. 810). The vertical channel pillars can include first and second channel films (e.g. 910 and 920) and a dielectric material (e.g. 930) between the first and second channel films.

[0051] Figure 10 is a cross-section taken in the XY plane along a line A-A' which is marked in Figure 9. The cross-section illustrates a layout view with a dielectric material (e.g. 930) between first and second channel films (e.g. 910 and 920), and an insulating structure (*e.g.* insulators 1001-1009) isolating the data storage structures (e.g.

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1010) and the vertical channel pillars (e.g. 910, 930, 920) along a conductive strip (e.g. 227). In one embodiment, the dielectric material (e.g. 930) can completely fill the regions between the stacks. In another embodiment, the dielectric material (e.g. 930) can leave an air gap 961 at least in regions adjacent the intermediate strips of conductive strips in the stacks (e.g. 211, 213, 215, 217, 221, 223, 225 and 227).

[0052] In the layout view, the conductive strips 217, 227 and 237 are illustrated. Each of the conductive strips in the cross-section is disposed in a separate stack of conductive strips. Although one conductive strip is shown for a respective stack, each stack can include multiple conductive strips disposed vertically and separated by insulating strips. Vertical channel pillars (e.g. 910, 930 and 920) are disposed between the conductive strips (e.g. 217, 227 and 237).

[0053] In this embodiment, the vertical channel pillars are arranged so that a first row of the vertical channel pillars (e.g. 1011-1014) disposed on the first sidewalls (e.g. 1031) of a particular stack of conductive strips (e.g. 227) is offset (e.g. 1090) in a row direction (e.g. the X direction) from a second row of the vertical channel pillars (e.g. 1021-1023) disposed on the second sidewalls (e.g. 1032) of the particular stack of conductive strips. This results in a twisted layout allowing a tighter pitch for overlying bit lines.

[0054] The example process flow illustrated in Figures 2 through 10 can result in an SGVC (single gate vertical channel) architecture including data storage structures including discrete charge trapping elements. The data storage structures are disposed at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks. The data storage structures include tunneling layers in contact with the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips, where the discrete charge trapping elements are disposed in the first recessed regions on the first sidewalls of the conductive strips. The data storage structures can include blocking layers between the discrete charge trapping elements and the second sidewalls of the conductive strips, where the discrete charge trapping elements are disposed in the second recessed regions on the second sidewalls of the conductive strips.

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[0055] Figure 11 is a flow chart illustrating a manufacturing method for a memory architecture including vertical channel pillars disposed between stacks in a plurality of stacks of conductive strips, where the vertical channel pillars have first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material between and contacting the first and second channel films, and data storage structures including discrete charge trapping elements at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks. The method includes forming a plurality of stacks of conductive strips alternating with insulating strips, where the insulating strips in the stacks have first and second sides, and the conductive strips in the stacks have first sidewalls, as described in connection to Figure 2 (Step 1111). The method includes recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks, as described in connection to Figure 3 (Step 1112).

[0056] The method includes forming data storage structures in the first recessed regions (Step 1113). This step can include depositing blocking layers over the first sidewalls of the conductive strips in the first recessed regions as described in connection to Figure 4, depositing charge trapping material over the blocking layers in the first recessed regions as described in connection to Figures 5-7, and depositing tunneling layers over the charge trapping material in the first recessed regions as described in connection to Figure 8.

[0057] Furthermore, depositing the blocking layers can include depositing the blocking layers over the first sides of the insulating strips, and depositing the charge trapping material can include depositing the charge trapping material over the blocking layers over the first sides of the insulating strips, and separating the charge trapping material between adjacent first recessed regions. Separating the charge trapping material can include removing the charge trapping material over the blocking layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions.

[0058] The method includes forming vertical channel pillars by forming first and second channel films on the data storage structures on sidewalls of adjacent stacks (Step 1114), and depositing a dielectric material between the first and second channel films, the

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dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks (Step 1115).

[0059] The method can further include etching to isolate the data storage structures along the conductive strips, to form discrete charge trapping elements in contact with the tunneling layers and the blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips, as described in connection with Figure 10.

[0060] The conductive strips in the stacks of conductive strips can have second sidewalls opposite the first sidewalls. The manufacturing method can further include recessing the second sidewalls of the conductive strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks, and forming the data storage structures including discrete charge trapping elements as described herein in the second recessed regions.

[0061] Figures 12-17 illustrate an example process flow for an alternative memory architecture including data storage structures including discrete charge trapping elements. Figure 12 illustrates an architecture similar to that shown in Figure 9. A difference is that Figure 9 illustrates stacks of conductive strips (e.g. 211, 213, 215 and 217 in stack 210; 221, 223, 225, 227 in stack 220), where the conductive strips can include a semiconductor material, while Figure 12 illustrates stacks of sacrificial strips (e.g. 1211, 1213, 1215 and 1217 in stack 1210; 1221, 1223, 1225, 1227 in stack 1220), where the sacrificial strips can include a material such as silicon nitride (SiN).

[0062] Figure 12 illustrates a stage of the process flow after a sequence of process steps similar to the process steps illustrated in Figures 2-9, using sacrificial strips instead of conductive strips as in Figures 2-9. The sequence of process steps resulting in the stage illustrated in Figure 12 includes:

[0063] Step 1: forming a plurality of stacks of sacrificial strips (e.g. 1211, 1213, 1215 and 1217 in stack 1210; 1221, 1223, 1225, 1227 in stack 1220) alternating with insulating strips (e.g. 1212, 1214, 1216 and 1218 in stack 1210; and 1222, 1224, 1226 and 1228 in stack 1220), the insulating strips in the stacks having first and second sides, and the sacrificial strips in the stacks having first sidewalls. This step is similar to the process step described in connection to Figure 2, using sacrificial strips instead of conductive strips.

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[0064] Step 2: recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks. This step is similar to the process step described in connection to Figure 3, using sacrificial strips instead of conductive strips.

[0065] Step 3: forming data storage structures in the first recessed regions. This step is similar to the process steps described in connection to Figures 4-8. This step can include depositing blocking layers (e.g. 1240) over the first sidewalls of the sacrificial strips (e.g. e.g. 1211, 1213, 1215 and 1217 in stack 1210) in the first recessed regions; depositing charge trapping material (e.g. 1250) over the blocking layers in the first recessed regions; and depositing tunneling layers (e.g. 1280) over the charge trapping material in the first recessed regions.

[0066] Furthermore, depositing the blocking layers in Step 3 can include depositing the blocking layers over the first sides of the sacrificial strips. Depositing the charge trapping material in Step 3 can include depositing the charge trapping material over the blocking layers over the first sides of the sacrificial strips, and separating the charge trapping material between adjacent first recessed regions. Separating the charge trapping material can include removing the charge trapping material over the blocking layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions.

[0067] Step 4: forming first and second channel films (e.g. 1291 and 1292) on the data storage structures on sidewalls of adjacent stacks (e.g. 1210 and 1220). This step is similar to the process steps described in connection to Figure 9.

[0068] Step 5: depositing a dielectric material (e.g. 2193) between the first and second channel films (e.g. 1291 and 1292), the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks (e.g. 1210 and 1220).

[0069] Figures 13-17 illustrate stages in the process flow to replace the sacrificial strips in the stacks with a metal material such as tungsten. Figure 13 illustrates a stage of the process flow after etching the stacks (e.g. 1210 and 1220) to form a trench (e.g. 1310, 1320), exposing the sacrificial strips in the trench (e.g. 1211, 1213, 1215 and 1217 in trench 1310; 1221, 1223, 1225, 1227 in trench 1320).

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[0070] Figure 14 illustrates a stage of the process flow after removing the sacrificial strips in the trenches (e.g. 1211, 1213, 1215 and 1217 in trench 1310; 1221, 1223, 1225, and 1227 in trench 1320). Figure 15 illustrates a stage of the process flow after depositing the metal material (e.g. 1510) in the trenches (e.g. 1310, 1320).

[0071] Figures 16 and 17 illustrate a stage of the process flow after separating the metal material (e.g. 1510) between the insulating strips in the trench, as shown in the ZY plane and the ZX plane. For instance, if the metal material includes tungsten (W), then a tungsten etch process can be applied to the metal material (e.g. 1510) in the trenches to separate the metal material between the insulating strips in the trenches.

[0072] The example process flow illustrated in Figures 12 through 17, using a gate replacement process, can result in an SGVC (single gate vertical channel) architecture including data storage structures including discrete charge trapping elements, and using a metal material for gates. The data storage structures are disposed at cross points of the vertical channel pillars between the stacks and the metal strips (e.g. 1510, FIG. 16) in the stacks. The data storage structures include tunneling layers in contact with the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers and blocking layers between the discrete charge trapping elements and the first sidewalls of the metal, where the discrete charge trapping elements are disposed in the first recessed regions on the first sidewalls of the metal strips. The data storage structures can include blocking layers between the discrete charge trapping elements and the second sidewalls of the metal strips, where the discrete charge trapping elements are disposed in the second recessed regions on the second sidewalls of the metal strips.

[0073] Figure 18 is an example flow chart illustrating a manufacturing method for an alternative memory architecture, including first forming data storage structures including discrete charge trapping elements in recessed regions in sides of stacks of sacrificial strips, and then replacing the sacrificial strips in the stacks with a metal material to form metal gates. The method includes forming a plurality of stacks (e.g. 1210, 1220) of sacrificial strips (e.g. 1211, 1213, 1215 and 1217) alternating with insulating strips (e.g. 1212, 1214, 1216 and 1218), where the insulating strips in the stacks have first and second sides, and the sacrificial strips in the stacks have first sidewalls, as described in connection to Figure 12 (Step 1811). The method includes

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recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks, as described in connection to Figure 12 (Step 1812).

[0074] The method includes forming data storage structures in the first recessed regions (Step 1813). This step can include depositing blocking layers (e.g. 1240) over the first sidewalls of the sacrificial strips in the first recessed regions as described in connection to Figure 12, depositing charge trapping material (e.g. 1250) over the blocking layers in the first recessed regions as described in connection to Figures 5-7, and depositing tunneling layers (e.g. 1280) over the charge trapping material in the first recessed regions as described in connection to Figure 12.

[0075] Furthermore, depositing the blocking layers can include depositing the blocking layers over the first sides of the insulating strips, and depositing the charge trapping material can include depositing the charge trapping material over the blocking layers over the first sides of the insulating strips, and separating the charge trapping material between adjacent first recessed regions. Separating the charge trapping material can include removing the charge trapping material over the blocking layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions.

[0076] The method includes forming vertical channel pillars by forming first and second channel films on the data storage structures on sidewalls of adjacent stacks (Step 1814), and depositing a dielectric material between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks (Step 1815).

[0077] The method can further include etching to isolate the data storage structures along the sacrificial strips, to form discrete charge trapping elements in contact with the tunneling layers and the blocking layers between the discrete charge trapping elements and the first sidewalls of the sacrificial strips, as described in connection with Figure 10, when the stacks include sacrificial strips (e.g. 1217 and 1227, Fig. 12) instead of conductive strips (e.g. 217 and 227, Fig. 10).

[0078] The sacrificial strips in the stacks of sacrificial strips can have second sidewalls opposite the first sidewalls. The manufacturing method can further include

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recessing the second sidewalls of the sacrificial strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks, and forming the data storage structures including discrete charge trapping elements as described herein in the second recessed regions.

[0079] The method includes replacing the sacrificial strips in the stacks with a metal material (Step 1816). The replacing step can include etching the stacks (e.g. 1210 and 1220) to form a trench (e.g. 1310, 1320, Fig. 13), exposing the sacrificial strips in the trench (e.g. 1211, 1213, 1215 and 1217 in trench 1310; 1221, 1223, 1225, 1227 in trench 1320); removing the sacrificial strips in the trench (e.g. Fig. 14); depositing the metal material (e.g. 1510, Fig. 14) in the trench; and separating the metal material between the insulating strips in the trench (Figs. 16 and 17), as described in connection to Figures 13-17.

[0080] Figure 19 is a block diagram of an integrated circuit memory including a 3D memory array including discrete charge trapping elements in recessed regions on sidewalls of conductive strips. The integrated circuit 1901 includes a memory array 1960 including one or more memory blocks as described herein with single gate vertical channel cells including data storage structures including discrete charge trapping elements in recessed regions on opposing sidewalls of conductive strips.

[0081] The data storage structures are disposed at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks. The data storage structures include tunneling layers in contact with the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips, where the discrete charge trapping elements are disposed in the first recessed regions on the first sidewalls of the conductive strips. The data storage structures can include blocking layers between the discrete charge trapping elements and the second sidewalls of the conductive strips, where the discrete charge trapping elements are disposed in the second recessed regions on the second sidewalls of the conductive strips. In embodiments, the conductive strips can include a semiconductor material such as polysilicon or a metal material such as tungsten.

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[0082] An SSL decoder 1940 is coupled to a plurality of SSL lines 1945, arranged in the memory array 1960. An even/odd level decoder 1950 is coupled to a plurality of even/odd word lines 1955. As described in connection to Figure 9, an even/odd level decoder 1950 can be coupled to a plurality of even/odd word lines such as the conductive strips (e.g. 211, 213, 215, 217, 221, 223, 225, and 227) in the odd stack 210 and the even stack 220 that can act as word lines. A global bit line column decoder 1970 is coupled to a plurality of global bit lines 1965 arranged along columns in the memory array 1960 for reading data from and writing data to the memory array 1960. Addresses are supplied on bus 1930 from control logic 1910 to decoder 1970, decoder 1940 and decoder 1950. Sense amplifier and program buffer circuits 1980 are coupled to the column decoder 1970, in this example via first data lines 1975. The program buffer in circuits 1980 can store program codes for multiple-level programming to indicate program or inhibit states for selected bit lines. The column decoder 1970 can include circuits for selectively applying program and inhibit voltages to bit lines in the memory in response to the data values in the program buffer.

[0083] Sensed data from the sense amplifier/program buffer circuits are supplied via second data lines 1985 to multi-level data buffer 1990, which is in turn coupled to input/output circuits 1991 via a data path 1993. Also, input data is applied in this example to the multi-level data buffer 1990 for use in support of multiple-level program operations for each of single gate vertical channel cells in the array.

[0084] Input/output circuits 1991 drive the data to destinations external to the integrated circuit 1901. Input/output data and control signals are moved via data bus 1905 between the input/output circuits 1991, the control logic 1910 and input/output ports on the integrated circuit 1901 or other data sources internal or external to the integrated circuit 1901, such as a general purpose processor or special purpose application circuitry, or a combination of modules providing system-on-a-chip functionality supported by the memory array 1960.

[0085] In the example shown in Figure 19, control logic 1910, using a bias arrangement state machine, controls the application of supply voltages generated or provided through the voltage supply or supplies in block 1920, such as read, erase, verify and program bias voltages. The control logic 1910 is coupled to the multi-level buffer

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1990 and the memory array 1960. The control logic 1910 includes logic to control multiple-level program operations.

[0086] The control logic 1910 can be implemented using special-purpose logic circuitry as known in the art. In alternative embodiments, the control logic comprises a general-purpose processor, which can be implemented on the same integrated circuit, which executes a computer program to control the operations of the device. In yet other embodiments, a combination of special-purpose logic circuitry and a general-purpose processor can be utilized for implementation of the control logic.

[0087] While the present invention is disclosed by reference to the preferred embodiments and examples detailed above, it is to be understood that these examples are intended in an illustrative rather than in a limiting sense. It is contemplated that modifications and combinations will readily occur to those skilled in the art, which modifications and combinations will be within the spirit of the invention and the scope of the following claims. What is claimed is:

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CLAIMS

1. A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material between and contacting the first and second channel films; and

data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips, the discrete charge trapping elements disposed in the first recessed regions on the first sidewalls of the conductive strips.

2. The memory device of claim 1, wherein the discrete charge trapping elements disposed in the first recessed regions are dielectric charge trapping elements.

3. The memory device of claim 1, wherein the conductive strips in the stacks have second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions on the second sidewalls of the conductive strips; and

the data storage structures include discrete charge trapping elements disposed in the second recessed regions in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements in the second recessed regions and the second sidewalls of the conductive strips.

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4. The memory device of claim 3, wherein the discrete charge trapping elements disposed in the second recessed regions are dielectric charge trapping elements.

5. The memory device of claim 1, wherein the dielectric material comprises a gap.

6. The memory device of claim 1, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

7. A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks and having second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material between and contacting the first and second channel films; and

data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips and between the discrete charge trapping elements and the second sidewalls of the conductive strips, the discrete charge trapping elements disposed in the first recessed regions on the first sidewalls of the conductive strips and disposed in the second recessed regions on the second sidewalls of the conductive strips,

wherein the vertical channel pillars are arranged so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is

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offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips.

8. The memory device of claim 7, wherein the discrete charge trapping elements are dielectric charge trapping elements.

9. The memory device of claim 7, wherein the dielectric material comprises a gap.

10. The memory device of claim 7, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

11. A manufacturing method, comprising:

forming a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls;

recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks; and

depositing a dielectric material between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks.

12. The manufacturing method of claim 11, said forming the data storage structures comprising:

depositing blocking layers over the first sidewalls of the conductive strips in the first recessed regions;

depositing charge trapping material over the blocking layers in the first recessed regions; and

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depositing tunneling layers over the charge trapping material in the first recessed regions.

13. The manufacturing method of claim 12, wherein the charge trapping material is dielectric charge trapping material.

14. The manufacturing method of claim 12, comprising:

said depositing the blocking layers including depositing the blocking layers over the first sides of the insulating strips; and

said depositing the charge trapping material including depositing the charge trapping material over the blocking layers over the first sides of the insulating strips; and separating the charge trapping material between adjacent first recessed regions.

15. The manufacturing method of claim 14, said separating the charge trapping material including removing the charge trapping material over the blocking layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions.

16. The manufacturing method of claim 11, comprising:

etching to isolate the data storage structures along the conductive strips, to form discrete charge trapping elements in contact with the tunneling layers and the blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips.

17. The manufacturing method of claim 11, wherein the conductive strips in the stacks of conductive strips have second sidewalls opposite the first sidewalls, the manufacturing method comprising:

recessing the second sidewalls of the conductive strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks; and

forming the data storage structures in the second recessed regions.

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18. The manufacturing method of claim 17,

etching to isolate the first and second channel films and the dielectric material between the first and second channel films along the conductive strips, to form vertical channel pillars between the stacks, so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips.

19. The manufacturing method of claim 11, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

20. A manufacturing method, comprising:

forming a plurality of stacks of sacrificial strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the sacrificial strips in the stacks having first sidewalls;

recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks;

depositing a dielectric material between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks; and

replacing the sacrificial strips in the stacks with a metal material.

21. The manufacturing method of claim 20, said forming the data storage structures comprising:

depositing blocking layers over the first sidewalls of the sacrificial strips in the first recessed regions;

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depositing charge trapping material over the blocking layers in the first recessed regions; and

depositing tunneling layers over the charge trapping material in the first recessed regions.

22. The manufacturing method of claim 21, wherein the charge trapping material is dielectric charge trapping material.

23. The manufacturing method of claim 20, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

24. The manufacturing method of claim 20, said replacing comprising:

etching the stacks to form a trench, exposing the sacrificial strips in the trench;

removing the sacrificial strips in the trench;

depositing the metal material in the trench; and

separating the metal material between the insulating strips in the trench.

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ABSTRACT

A memory device includes a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips having first and second sides, and the conductive strips having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks. Vertical channel pillars are disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks and a dielectric material between and contacting the first and second channel films. Data storage structures at cross points of the vertical channel pillars and the conductive strips include tunneling layers in contact with the vertical channel pillars, discrete charge trapping elements in the first recessed regions in contact with the tunneling layers and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips.

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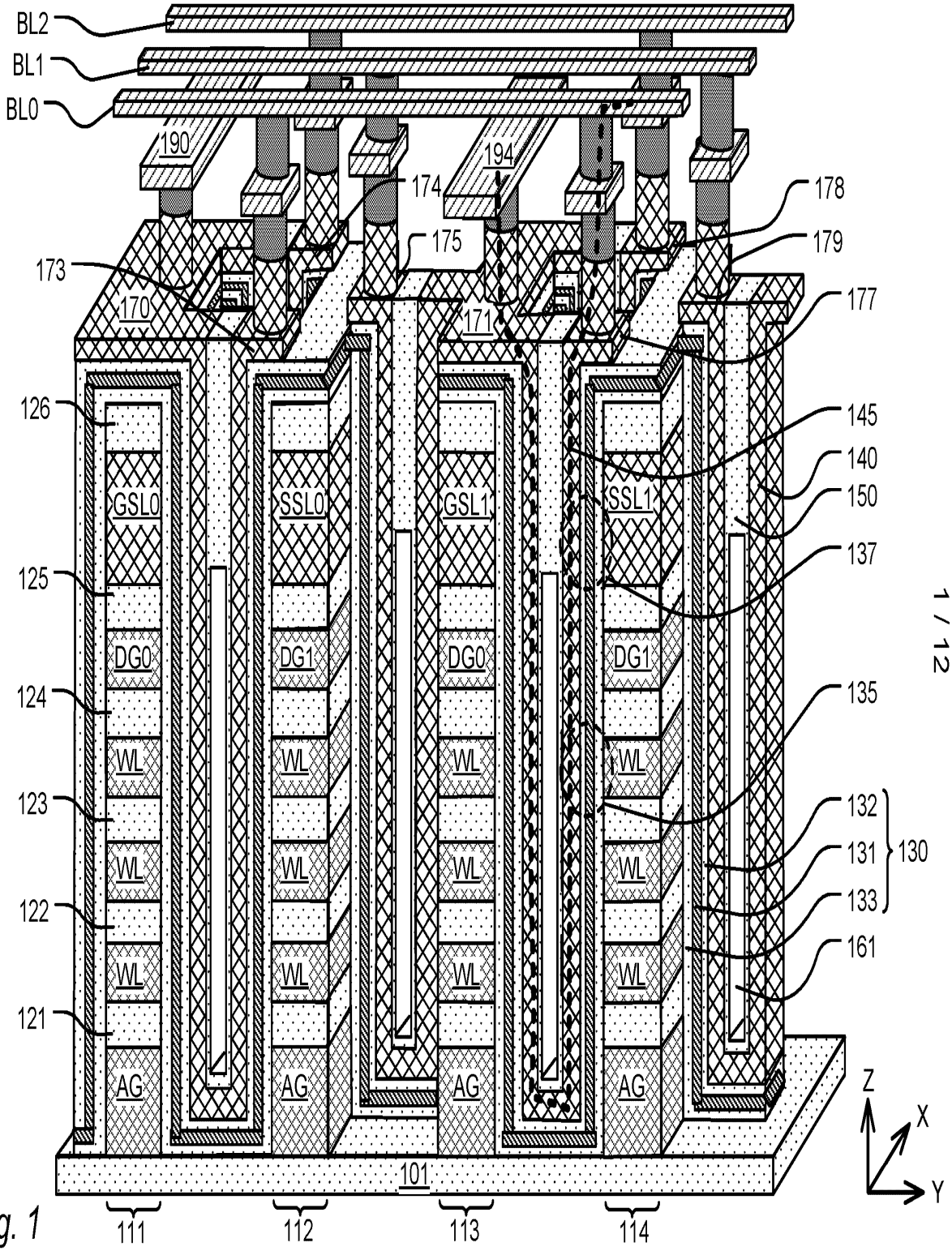

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BL1
BL0
190
194
174
178
175
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173
170
171
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126
145
140
150
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SSL0
GSL1
SSL1
137
125
DG0
DG1
DG0
DG1
124
135
WL
WL
WL
WL
123
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114

Fig. 1

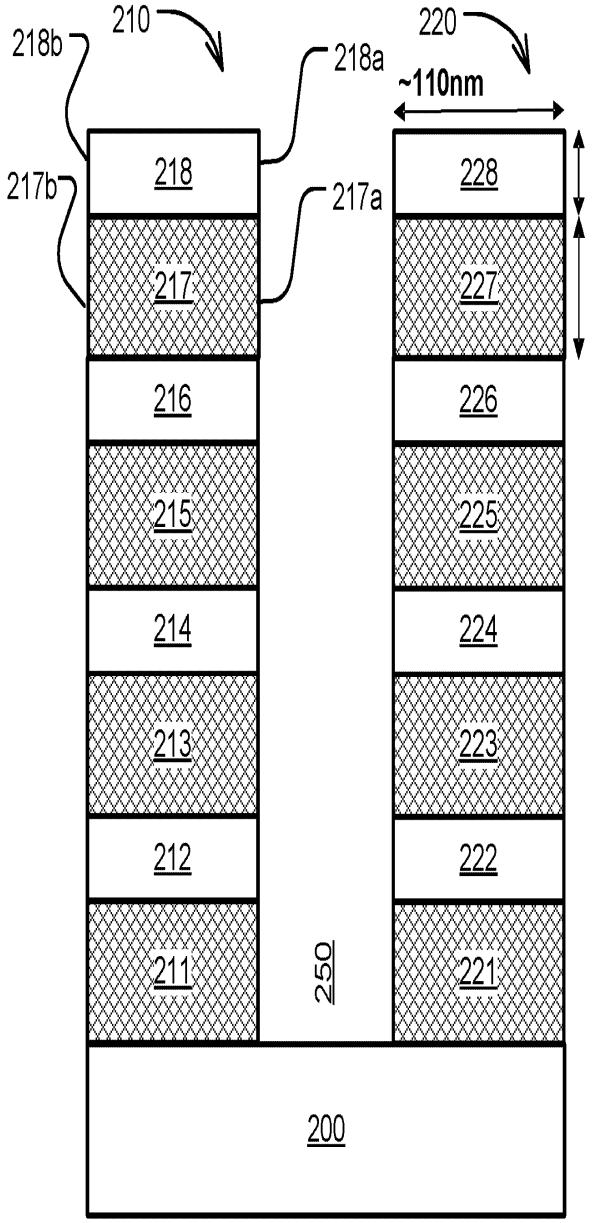
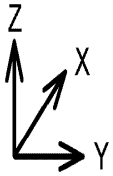

210
220
218b
218a
~110nm
217b
217a
218
228
217
227
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214
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213
223
212
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211
250
221
200

Fig. 2


Z
X
Y

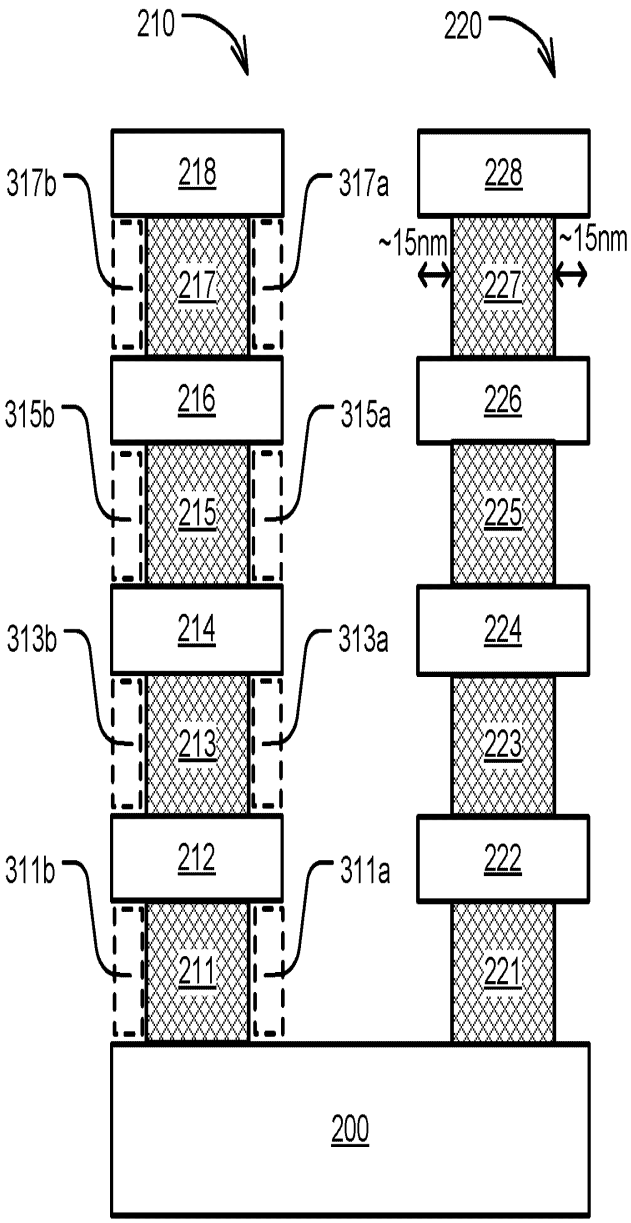
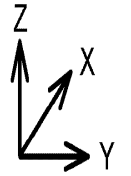

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317a
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228
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~15nm
217
227
315b
315a
216
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225
313b
313a
214
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311b
311a
212
222
211
221
200

Fig. 3


Z
X
Y

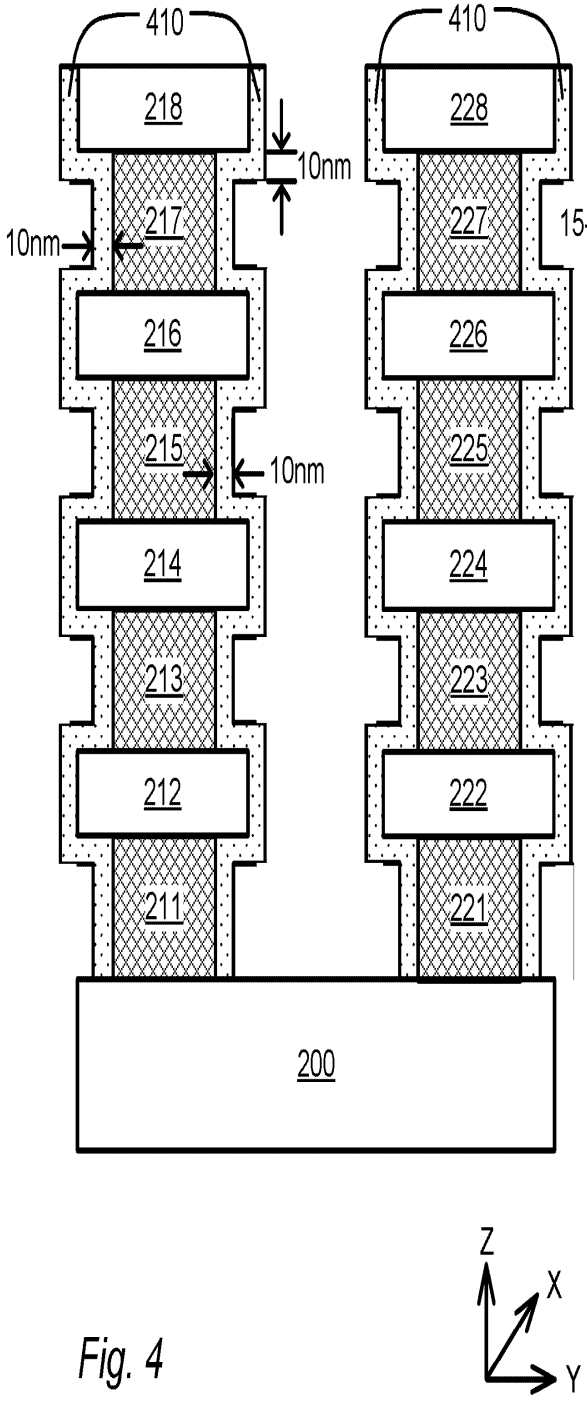

410
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10nm
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Z
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Y

Fig. 4

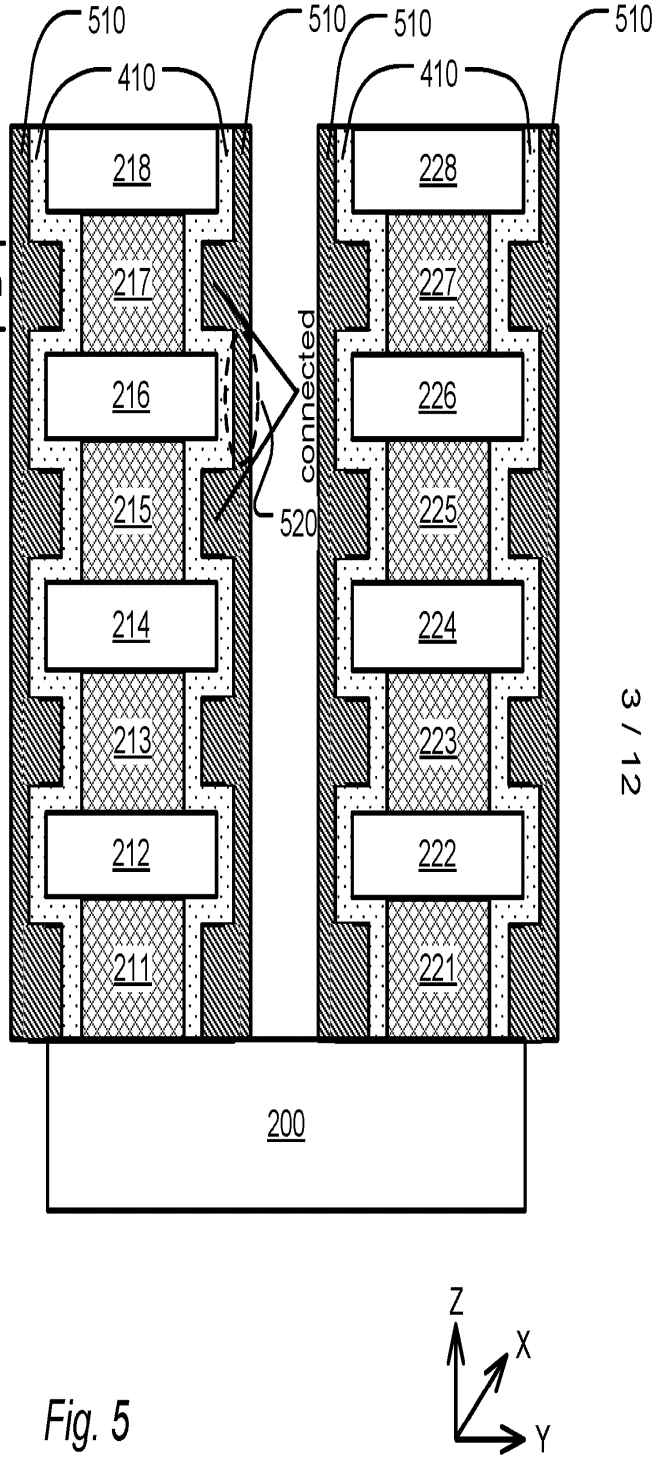

510
510
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410
218
228
15-30nm
217
227
connected
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226
520
215
225
214
224
213
223
212
222
211
221
200
Z
X
Y

Fig. 5

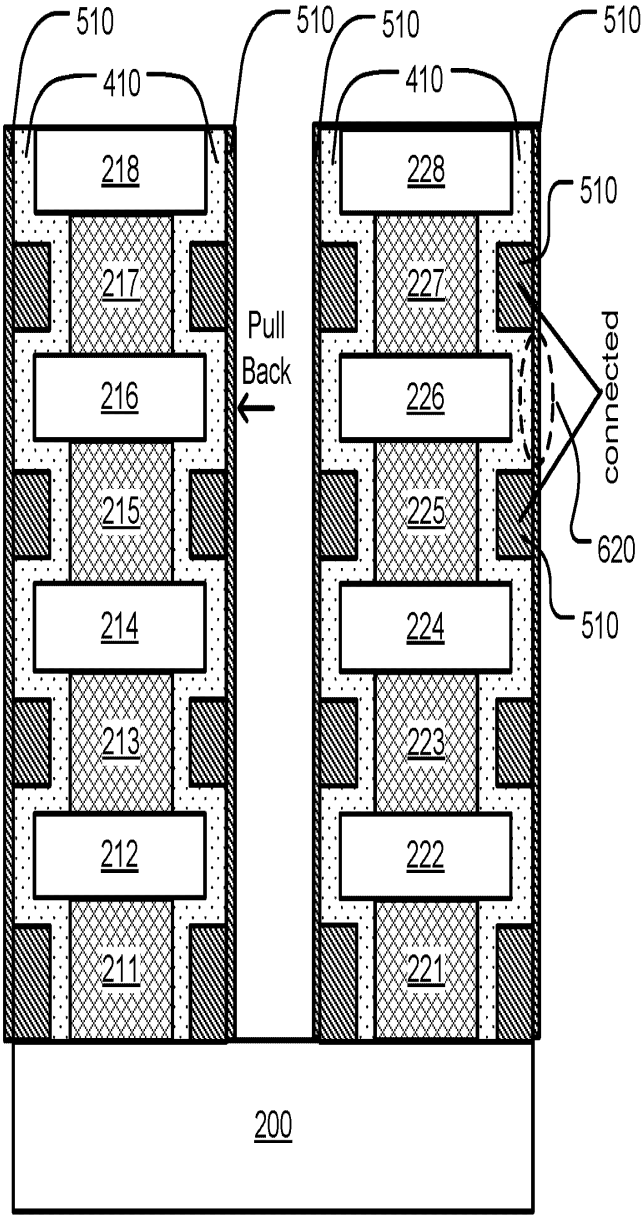

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510
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212
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Pull
Back
connected
620
510
510

Fig. 6


Z
X
Y

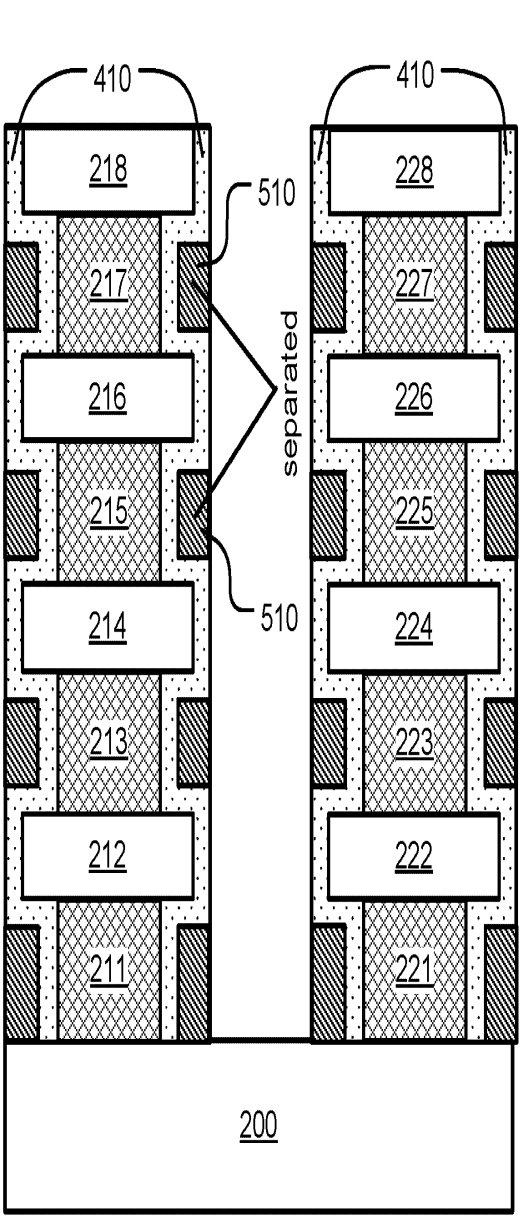
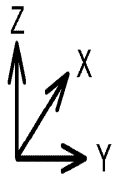

410
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510
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200
separated
510
510

Fig. 7


Z
X
Y

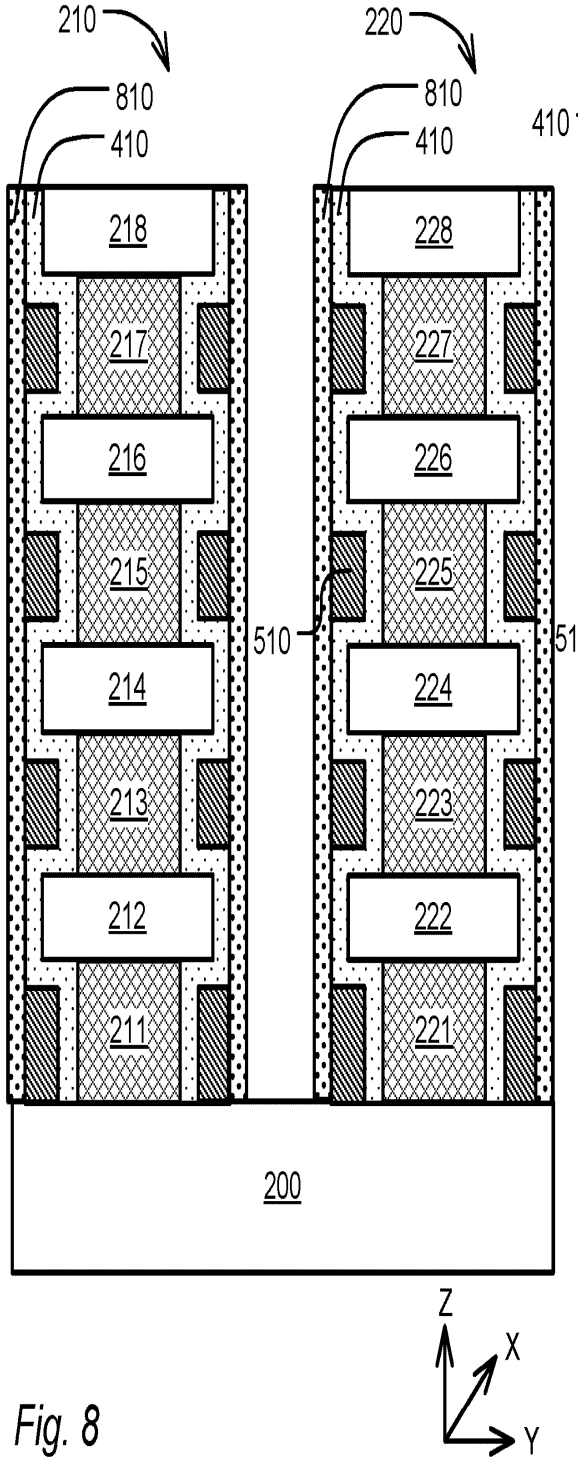


Fig. 8

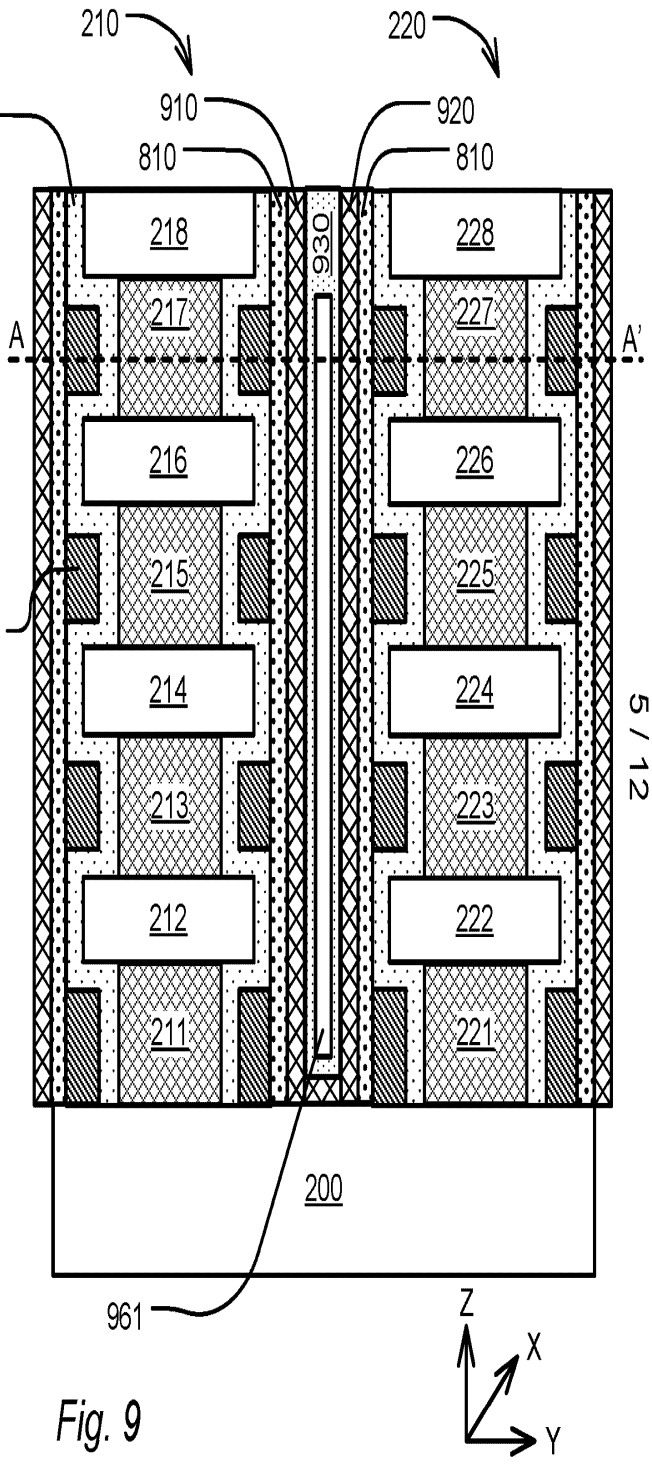


Fig. 9

Inventors: Hung-Ting Lue
Title: Confined SiN Structure for 3D NAND Architecture
Application No.
Attorney Docket No. MXIC 2194-1

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1022
1023
217
410
510
810
910
1010
1002
961
1004
961
1006
961
1008
930
1010
920
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1031
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1003
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1011
1012
1013
1014
Y
X

Fig. 10

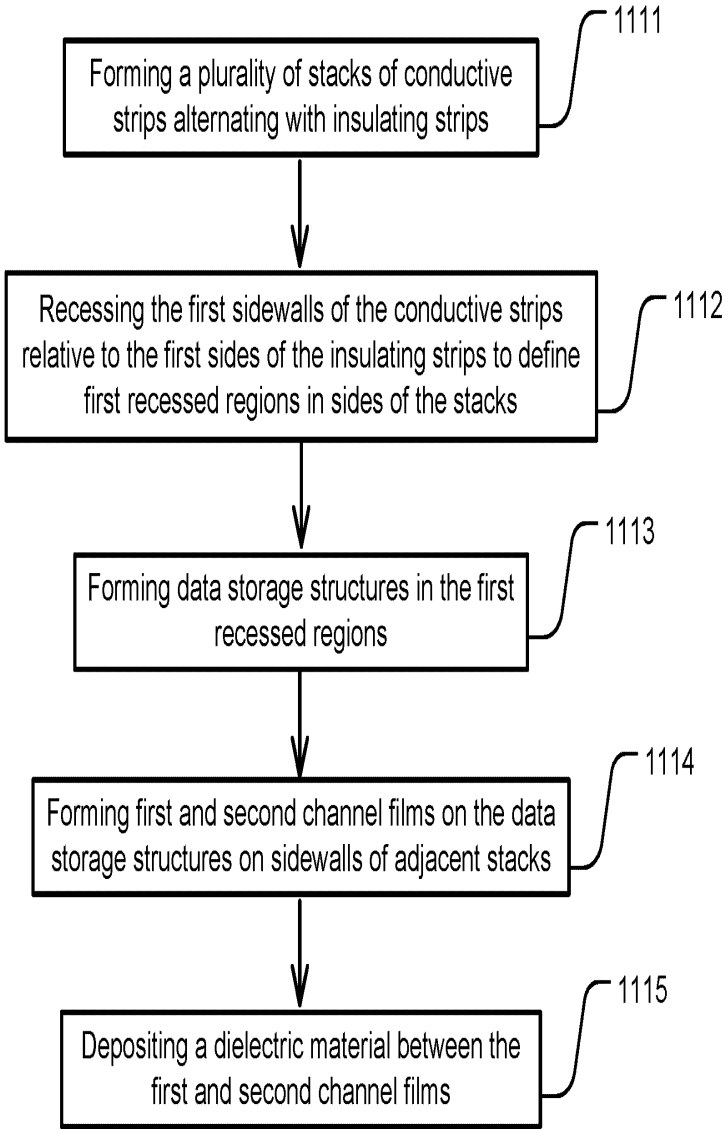

1111
Forming a plurality of stacks of conductive strips alternating with insulating strips
1112
Recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks
1113
Forming data storage structures in the first recessed regions
1114
Forming first and second channel films on the data storage structures on sidewalls of adjacent stacks
1115
Depositing a dielectric material between the first and second channel films

Fig. 11

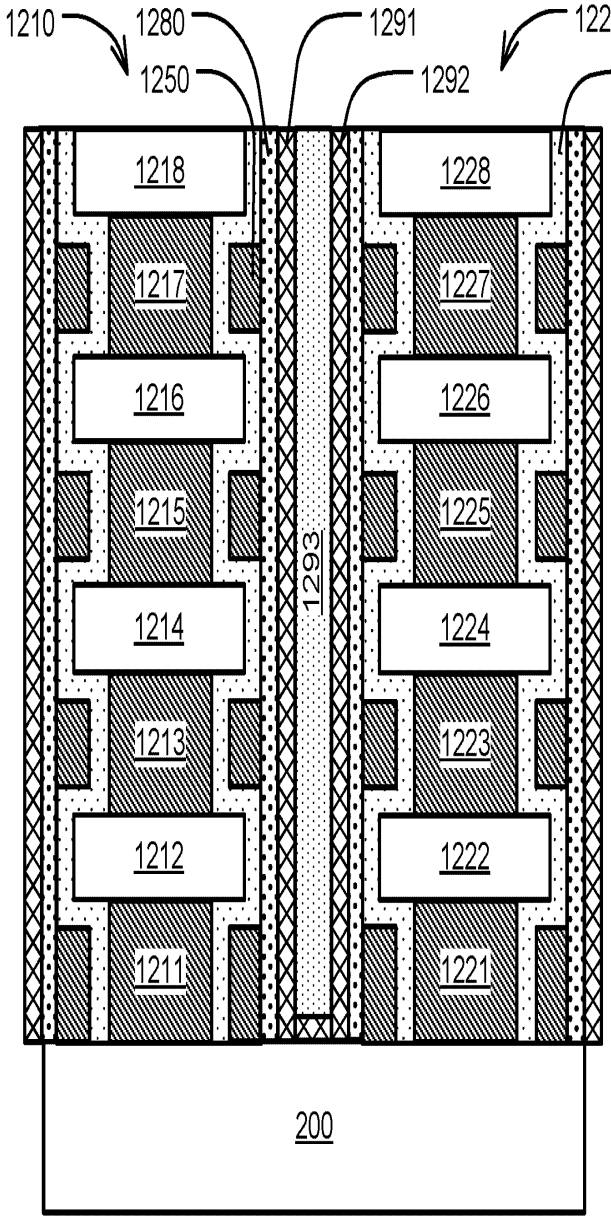


Fig. 12

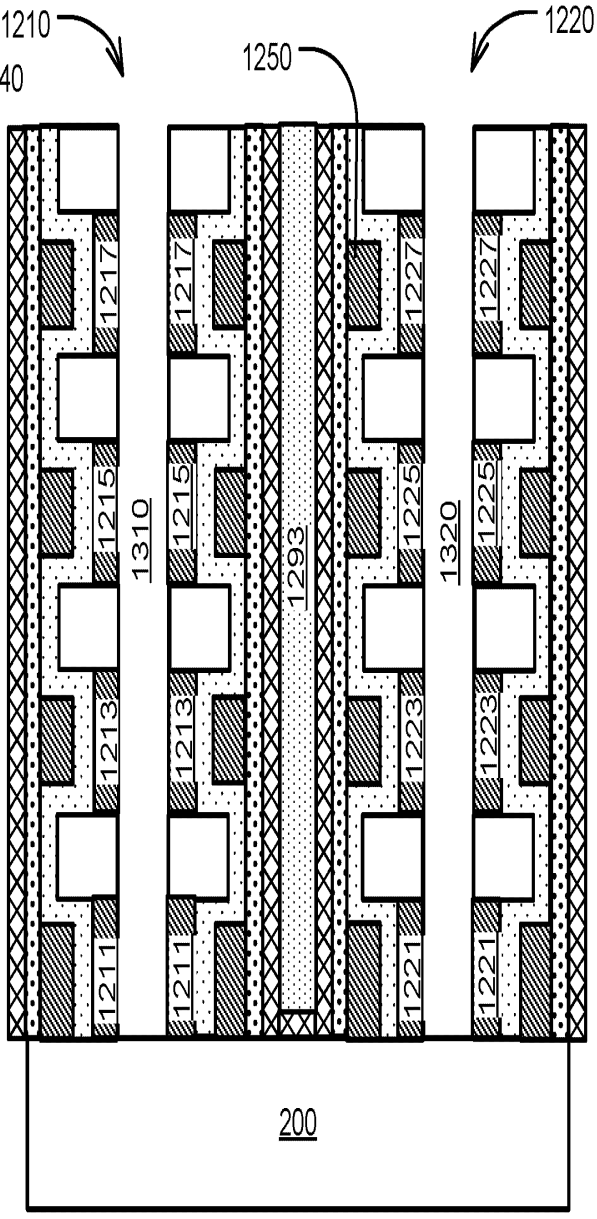


Fig. 13

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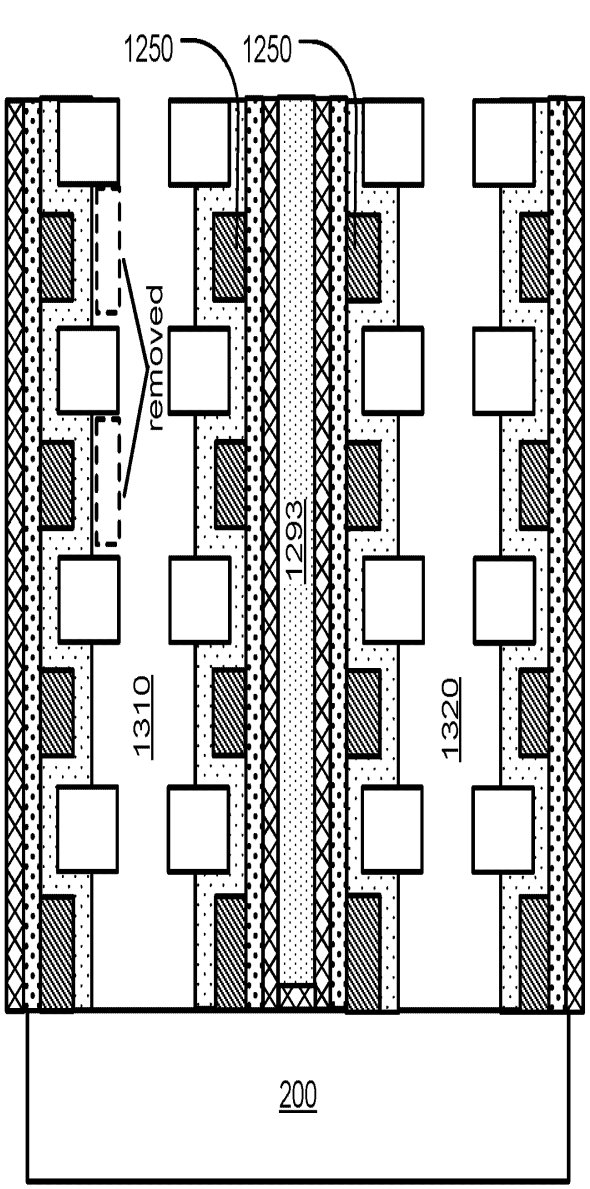


Fig. 14

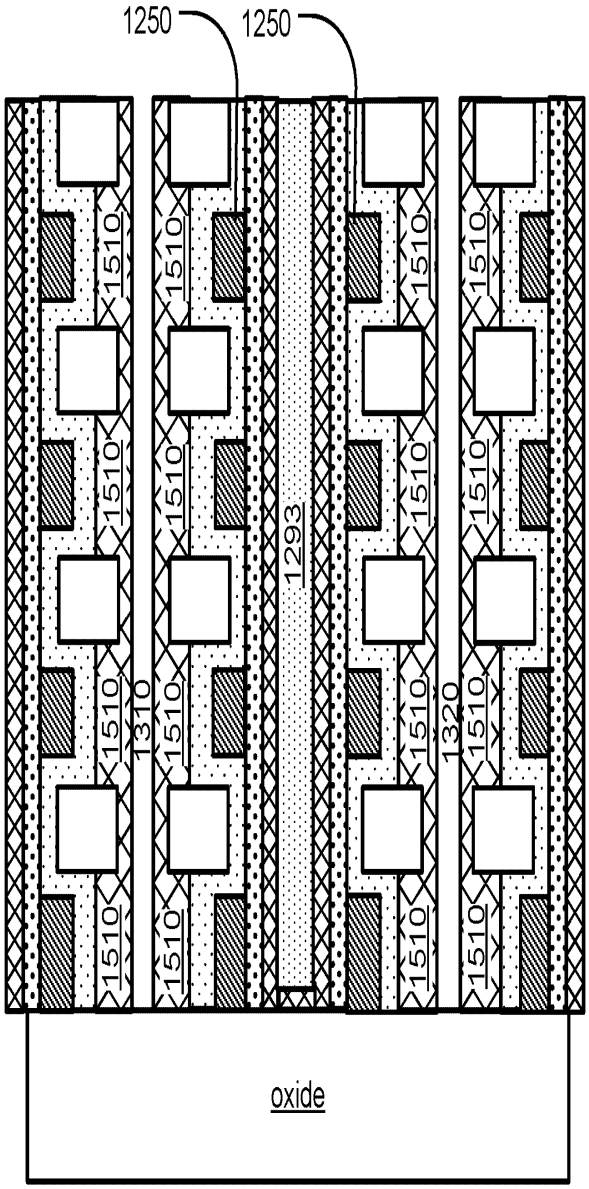


Fig. 15

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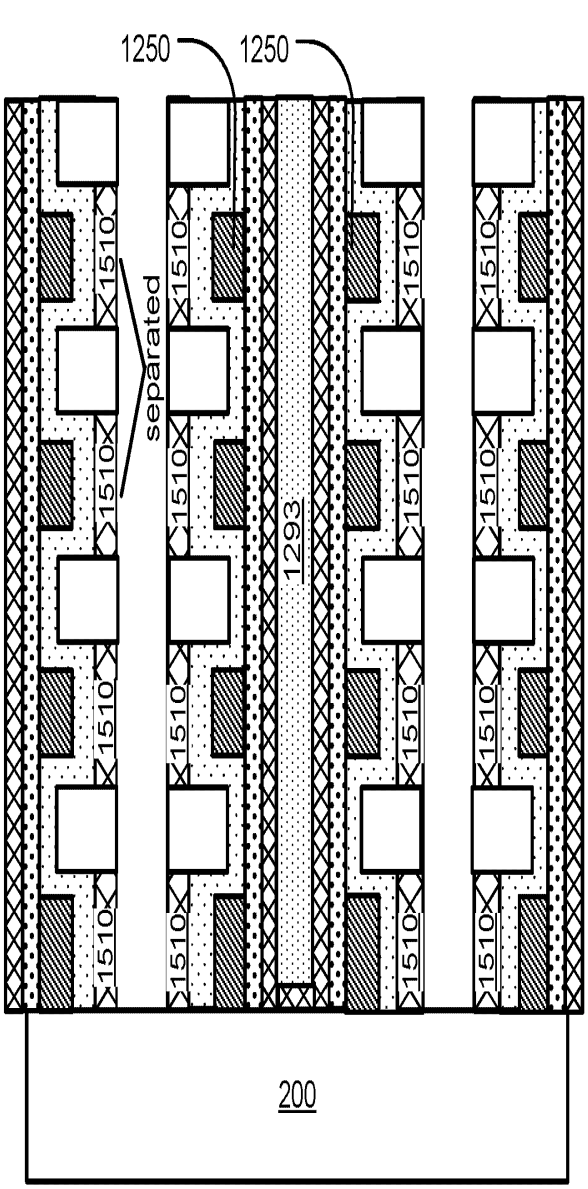


Fig. 16

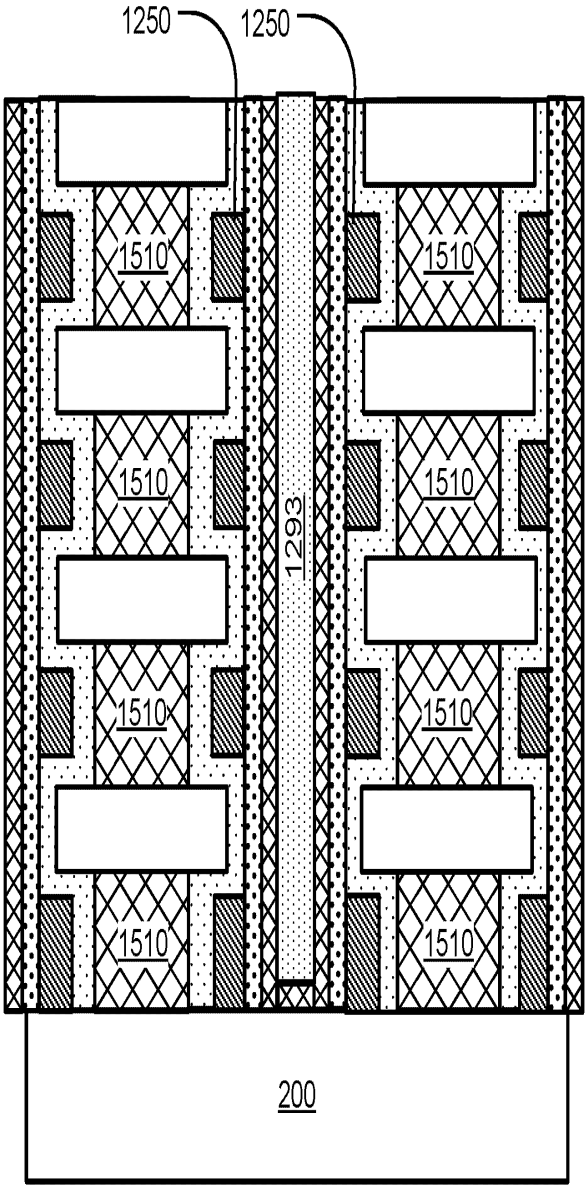


Fig. 17

Inventors: Hung-Ting Lue
Title: Confined SiN Structure for 3D NAND Architecture
Application No.
Attorney Docket No. MXIC 2194-1

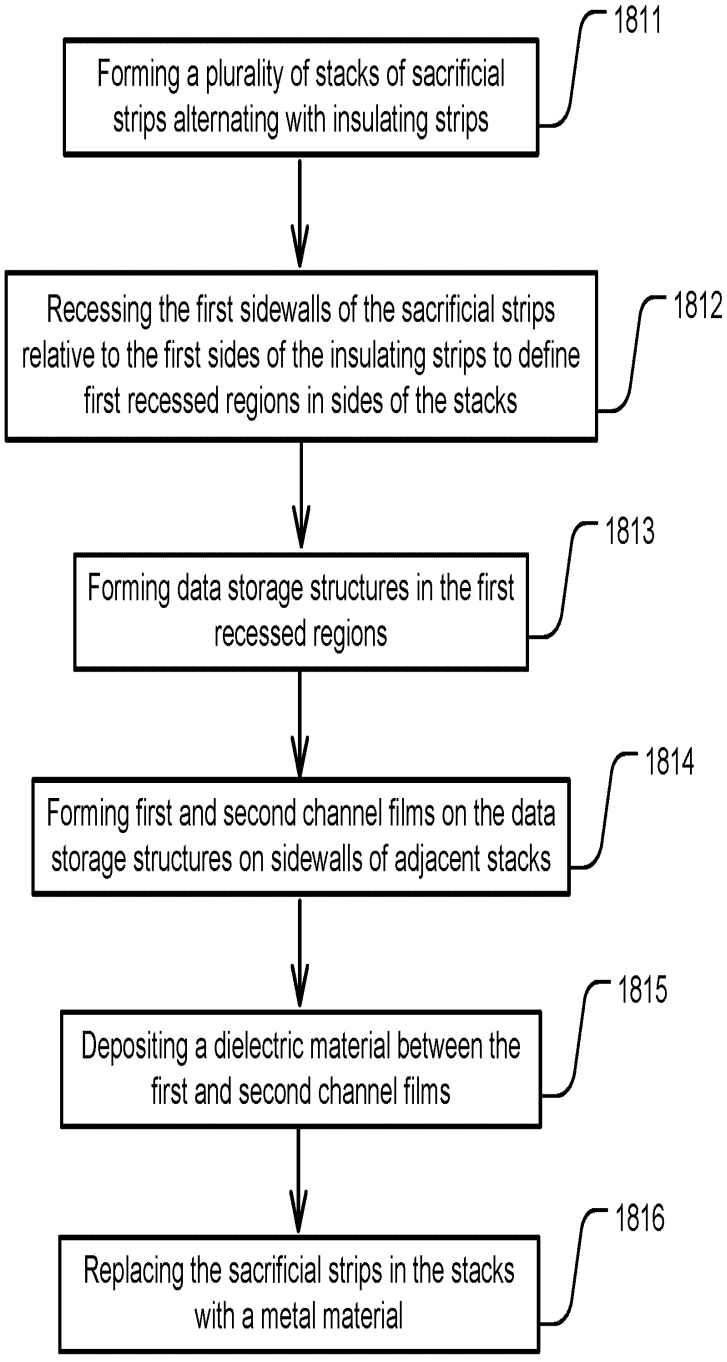

1811
Forming a plurality of stacks of sacrificial strips alternating with insulating strips
1812
Recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks
1813
Forming data storage structures in the first recessed regions
1814
Forming first and second channel films on the data storage structures on sidewalls of adjacent stacks
1815
Depositing a dielectric material between the first and second channel films
1816
Replacing the sacrificial strips in the stacks with a metal material

Fig. 18

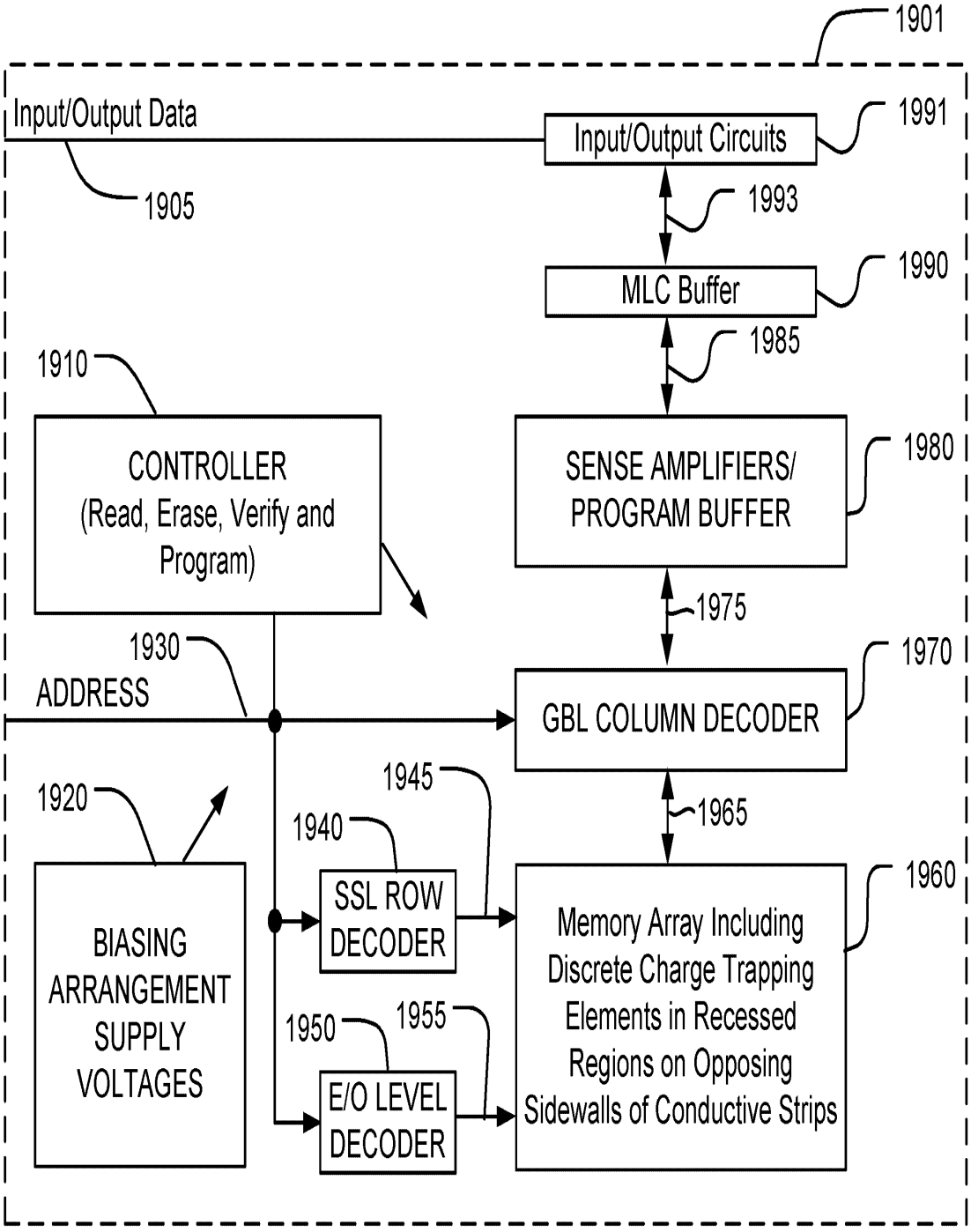


Fig. 19

Inventors: Hung-Ting Lue
Title: Confined SiN Structure for 3D NAND Architecture
Application No.
Attorney Docket No. MXIC 2194-1

Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	Hang-Ting Lue
Filer:	Yiding Wu/Amy Jonsson
Attorney Docket Number:	MXIC 2194-1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	280	280
UTILITY SEARCH FEE	1111	1	600	600
UTILITY EXAMINATION FEE	1311	1	720	720
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	4	80	320
INDEPENDENT CLAIMS IN EXCESS OF 3	1201	1	420	420
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**2340**

Electronic Acknowledgement Receipt

EFS ID:	28118606
Application Number:	15410965
International Application Number:	
Confirmation Number:	3219
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	Hang-Ting Lue
Customer Number:	46353
Filer:	Yiding Wu/Amy Jonsson
Filer Authorized By:	Yiding Wu
Attorney Docket Number:	MXIC 2194-1
Receipt Date:	20-JAN-2017
Filing Date:	
Time Stamp:	12:23:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$2340
RAM confirmation Number	012317INTEFSW12244200
Deposit Account	500869
Authorized User	Amy Jonsson
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.17 (Patent application and reexamination processing fees)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	00576616.PDF	1823074 6688cb25ca82b9d35d8094ed5ec8b6765b151dfd	no	8
Warnings:					
Information:					
2	Oath or Declaration filed	00576666.PDF	207922 8920f073194b4bd856216822e95f3ae31e6692bd	no	2
Warnings:					
Information:					
3		00571391.PDF	266002 858bcfbce254e7b3d53fb2a85eeb475e76445129	yes	28

Multipart Description/PDF files in .zip description

Document Description	Start	End
Specification	1	21
Claims	22	27
Abstract	28	28

Warnings:					
Information:					
4	Drawings-only black and white line drawings	00570575.PDF	2461514 0554f10379883f2fb7f9bf78a9766b63b105a526	no	12
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	38006 e9dbb107d5598c00aeca494b65afdd3eb2ff13f1	no	2

Warnings:	
Information:	
Total Files Size (in bytes):	4796518

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/80 (07-12)
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U.S. Patent and Trademark Office; U.S DEPARTMENT OF COMMERCE
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POWER OF ATTORNEY TO PROSECUTE APPLICATIONS BEFORE THE USPTO

I hereby revoke all previous powers of attorney given in the application identified in the attached statement under 37 CFR 3.73(c).

I hereby appoint:

☑ Practitioners associated with Customer Number: 46353

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

As attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignments documents attached to this form in accordance with 37 CFR 3.73(c).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(c) to:

☑ The address associated with Customer Number: 46353

OR

☐	Firm or Individual Name		
	Address		
	City		
	Country		
	Telephone		Email

Assignee Name and Address: Macronix International Co., Ltd., No. 16, Li-Hsin Road, Science-Based Industrial Park, Hsinchu, TW

A copy of this form, together with a statement under 37 CFR 3.73(c) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(c) may be completed by one of the practitioners appointed in this form, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	C. Y. Lu	Date	2012.09.26
Name	CHIH YUAN LU	Telephone	
Title	PRESIDENT		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: MACRONIX INTERNATIONAL CO., LTD.

Application No./Patent No.: 15/410,965 Filed/Issue Date: 2017-01-20

Titled: DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE

MACRONIX INTERNATIONAL CO., LTD., a CORPORATION

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☑ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____

   The document was recorded in the United States Patent and Trademark Office at

   Reel _____, Frame _____, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

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6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at

Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Yiding Wu/	2017-01-20
Signature	Date
YIDING WU	65992
Printed or Typed Name	Title or Registration Number

Attorney Docket No. MXIC 2194-1
(P1050004US)

DECLARATION (37 C.F.R. 1.63) FOR UTILITY PATENT APPLICATION USING AN APPLICATION DATA SHEET (37 C.F.R. 1.76) AND ASSIGNMENT

Title of Invention: **DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE**

As a below named inventor, I hereby declare that:

This declaration is directed to the attached application, or (if following box is checked):

[X] United States application or PCT international application number 15/410,965 filed on 20 January 2017

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I have reviewed and understand the contents of the application, including the claims.

I am aware of the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in 37 CFR Section 1.56.

Whereas, the undersigned inventor(s) has/have made certain inventions, improvements, and discoveries (herein referred to as the "Invention") disclosed in the above-identified patent application and further identified by the Docket Number provided above in the header of this document;

Whereas, Macronix International Co., Ltd., a corporation of Taiwan having a place of business at No. 16 Li-Hsin Road, Science-Based Industrial Park, Hsinchu, Taiwan (herein referred to as "Macronix"), desires to acquire, and each undersigned inventor desires to grant to Macronix, the entire worldwide right, title, and interest in and to the Invention and in and to any and all patent applications and patents directed thereto;

Now, therefore, for good and valuable consideration, the receipt and sufficiency thereof being hereby acknowledged, each undersigned inventor ("ASSIGNOR") hereby sells or has sold, assigns or has assigned, and otherwise transfers or has transferred to Macronix (the "ASSIGNEE"), its successors, legal representatives, and assigns, the entire worldwide right, title, and interest in and to the Invention, the above-identified United States patent application, and any and all other patent applications and patents for the Invention which may be applied for or granted therefor in the United States and in all foreign countries and jurisdictions, including all divisions, continuations, reissues, reexaminations, renewals, extensions, counterparts, substitutes, and extensions thereof, and all rights of priority resulting from the filing of such applications and granting of such patents. In addition, each undersigned inventor hereby authorizes and requests the Director of the United States Patent and Trademark Office to issue any United States Patent, and foreign patent authorities to issue any foreign patent, granted for the Invention, to Macronix, its successors, legal representatives, and assigns, the entire worldwide right, title, and interest in and to the same to be held and enjoyed by Macronix, its successors, legal representatives, and assigns to the full end of the terms for which any and all such patents may be granted, as fully and entirely as would have been held and enjoyed by the undersigned had this Assignment not been made; and each undersigned inventor agrees to execute any and all documents and instruments and perform all lawful acts reasonably related to recording this Assignment or perfecting title to the Invention and all related patents

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Micron v. YMTC
IPR2024-00912

and applications, in Macronix, its successors, legal representatives, and assigns, whenever requested by Macronix, its successors, legal representatives, or assigns.

Each undersigned inventor acknowledges their prior and ongoing obligations to sell, assign, and transfer the rights under this Assignment to Macronix and is unaware of any reason why they may not have the full and unencumbered right to sell, assign, and transfer the rights hereby sold, assigned, and transferred, and has not executed, and will not execute, any document or instrument in conflict herewith. Each undersigned inventor also hereby grants Macronix, its successors, legal representatives, and assigns, the right to insert in this Assignment any further identification (including, but not limited to, patent Application Number) which may be necessary or desirable for recordation of this Assignment.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

(1) Legal Name of Inventor: HANG-TING LUE 呂函庭

Signature: Hang-Ting Lue Date: 2016.12.27

Micron Ex. 1022, p. 61
Micron v. YMTC
IPR2024-00912

Electronic Acknowledgement Receipt

EFS ID:	28119549
Application Number:	15410965
International Application Number:	
Confirmation Number:	3219
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	HANG-TING LUE
Customer Number:	46353
Filer:	Yiding Wu/Amy Jonsson
Filer Authorized By:	Yiding Wu
Attorney Docket Number:	MXIC 2194-1
Receipt Date:	20-JAN-2017
Filing Date:	
Time Stamp:	13:15:09
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	00576683.PDF	43981 7608d0fee1876175c845534504d06a77544d8b38	no	1
Warnings:					

Information:					
2	Assignee showing of ownership per 37 CFR 3.73	373.pdf	291161 a53a19e16c8870ce6dc4b42a0a1f4df14d5a27e8	no	4
Warnings:					
Information:					
			Total Files Size (in bytes):	335142	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
15/410,965	01/20/2017	2811	2340	MXIC 2194-1	24	4

CONFIRMATION NO. 3219

FILING RECEIPT

46353
MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019

OC000000088799982

Date Mailed: 01/30/2017

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

HANG-TING LUE, HSINCHU, TAIWAN;

Applicant(s)

MACRONIX INTERNATIONAL CO., LTD., Hsinchu, TAIWAN;

Assignment For Published Patent Application

MACRONIX INTERNATIONAL CO., LTD., Hsinchu, TAIWAN

Power of Attorney: The patent practitioners associated with Customer Number 46353

Domestic Applications for which benefit is claimed - None.
A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 01/27/2017

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Micron v. YMTC
IPR2024-00912

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 15/410,965**

Projected Publication Date: 07/26/2018

Non-Publication Request: No

Early Publication Request: No
Title

DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE

Preliminary Class

257

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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IPR2024-00912

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 15/410,965

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	600
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720
TOTAL CLAIMS (37 CFR 1.16(i))	24 minus 20 =	* 4			OR	x 80 =	320
INDEPENDENT CLAIMS (37 CFR 1.16(h))	4 minus 3 =	* 1				x 420 =	420
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	2340

APPLICATION AS AMENDED - PART II

AMENDMENT A

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

AMENDMENT B

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
Application Size Fee (37 CFR 1.16(s))									
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

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Application Number	15410965
Filing Date	2017-01-20
First Named Inventor	Hang-Ting Lue
Art Unit	2823
Examiner Name	Christine A. Enad
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	First Named Inventor	Hang-Ting Lue
	Art Unit	2823
	Examiner Name	Christine A. Enad
	Attorney Docket Number	MXIC 2194-1

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	1	Choi et al., "Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND flash memory," 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, 14-16 June 2016, pp. 1-2.	
	2	Jang et al., "Vertical cell array using TCAT(Terabit Cell Array Transistor) technology for ultra high density NAND flash memory," 2009 Symposium on VLSI Technology, Honolulu, HI, 16-18 jUNE 2009, pp. 192-193.	
	3	Jung et al, "Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node," International Electron Devices Meeting, 2006. IEDM '06, 11-13 Dec. 2006, pp 1 - 4.	
	4	Lai et al., "A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory," International Electron Devices Meeting, 2006. IEDM '06, 11-13 Dec. 2006, pp 1-4.	

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Micron v. YMTC
IPR2024-00912

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2017-01-20
	First Named Inventor	Hang-Ting Lue
	Art Unit	2823
	Examiner Name	Christine A. Enad
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Name/Print	Yiding Wu	Registration Number	65,992

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Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory

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Abstract

A fast charge loss within a few seconds, which is referred to as early retention, was observed in tube-type 2y word-line stacked 3-D NAND flash memory for the first time, and the origin of the early retention was comprehensively evaluated. Using a fast-response pulse *I-V* system, the early retention characteristics from microseconds to seconds were thoroughly investigated, and the correlations with various program and erase levels were examined using solid and checkerboard patterns. Our findings indicate that the early retention mainly originates from the lateral charge loss through the shared charge trap layers and suggest that the program and erase levels should be balanced and optimized to reduce the early retention.

Introduction

Due to scaling down limits, increasing process cost, and reliability issues in planar NAND flash memory, 3-D NAND flash memory has been considered to be a very promising candidate [1-3]. Although 3-D NAND flash memory with a charge trap layer (SiN) has many merits, the retention characteristics stemming from lateral charge loss are expected to cause problems because the charge trap layers are shared between word-lines (WLs) (Fig. 1). Therefore, a fast charge loss within a few seconds, which we refer to as 'early retention,' can be observed and can cause unwanted results in a negative shift of the threshold voltage (V_T) and a positive shift of the string read current immediately after programming. This early retention threatens multi-level cell (MLC) capability (Fig. 2) and product-level reliability requirements. It has been reported that early retention can take place predominately through vertical charge loss via the tunnel or block oxide immediately after programming resulting from the shallowly trapped electrons in a charge trap layer [2]. However, we observed that severe early retention can occur through a lateral charge loss as well in the WL stacked 3-D NAND structure because of the inevitably shared charge trap layer between WLs (Fig. 3). Therefore, in this work, for the first time, we comprehensively evaluate the early retention behaviors from the lateral charge loss point of view using diverse test situations, such as various program and erase levels, and a fast-response pulse *I-V* system in tube-type 3-D NAND flash memory. Moreover, early retention on the cell states, i.e., solid and checkerboard pattern (S/P and C/P), has been thoroughly characterized (Fig. 4).

Measurement Result and Discussion

Fig. 5 shows a TEM cross-section image and the core device structure of the 2y WL stacked tube-type 3-D NAND flash memory, which is referred to as 'SMArt', used in this work [3]. Fig. 6(a) shows the conventional DC *I-V* measurement sequences for characterizing the early retention. The initialization step was performed to assure all cells were erased before programming. The early retention under various program levels (PV1, PV2, and PV3) was measured at 90 °C (Fig. 6(b)). Note that the early retention rapidly occurred within 1 min, which necessitates the measurement of the early retention within a few seconds for precise analysis. Therefore, we performed fast response pulse *I-V* measurements using incremental step pulse programming (ISPP) followed by immediate retention measurements (Fig. 7(a)). The reading phase is enabled (delay < 100 μsec) immediately after programming so that accurate early retention characteristics were obtained. The string read current was first measured (Figs. 7(b) and 7(c)) and then transformed into early retention defined as $V_{T,loss}$ (Fig. 8). First, we measured the early retention characteristics in the states of the cells, i.e., S/P and C/P, under various PV levels, as shown in Fig. 8. It should be noted that the early retention is obviously aggravated by increasing PV levels in both states. Importantly, these results showed a clear opposite trend to a previous report in which a greater PV level showed a greater $V_{T,loss}$, i.e., worsened early retention due to increased vertical charge loss [2].

To further evaluate the origin of the observed trends, we performed a TCAD simulation by considering the erasing operation in the initialization step. Thus the cell was first erased prior to programming to describe real measurement sequences. Fig. 9 shows the simulated profiles of trapped electrons and holes in a charge trap layer for different PV levels for the S/P. At the lower PV level, it is clearly observed that there were a large number of residual holes that are not fully compensated by the trapped electrons during programming. During erasing, the holes injected into the charge trap layer can spread outside of cells due to the relatively longer erasing time and the high diffusivity of the holes [4]. Therefore, the trapped electrons from the lower PV level cannot completely compensate the injected holes resulting in residual holes. As a result, a large lateral electric field is generated at the edge of the cell in which there is a greater chance for stored charges in a charge trap layer to spread laterally. To confirm the influence of the non-compensated residual holes on the early retention, additional measurement were performed by varying the erasing levels (EV1, EV2, and EV3) in the initialization step (Fig. 10). As expected, a greater EV level as well as a lower PV level resulted in worsened early retention due to residual holes. This observation indicates that the early retention mainly occurs through lateral charge loss in the shared charge trap layers rather than vertical charge loss.

Figs. 11 and 12 also show the simulation and measurement results of early retention in a C/P. It is clearly observed that the trends of the early retention for various PV and EV levels were similar in the S/P and the C/P, but the dependence of the early retention on the PV levels for the C/P was less than for the S/P (Fig. 13). That is, the early retention was easily relaxed with increasing PV levels in the S/P but not in the C/P. Moreover, it is worthwhile to note that the overall early retention was more severe in the C/P than in the S/P. Fig. 14 shows the simulated conduction band edge profile (E_C) of the SiN and the corresponding lateral electric field in the S/P and the C/P. We confirm that for the C/P, the lateral electric field was mostly governed by the erased state of neighboring cells. However, for the S/P, the lateral electric field was specifically determined from the non-compensated residual holes. In addition, more electrons could be trapped between the WLs at a greater PV level in the S/P due to the strong fringing electric field, which effectively compensated for the injected holes during erasing (Fig. 15). Therefore, the dependence of the early retention on the PV levels was more noticeable in the S/P. Note that our findings suggest that both PV and EV levels should be optimized and balanced in the S/P and the C/P to minimize the early retention (Fig. 16).

Conclusion

We comprehensively evaluated the early retention in WL stacked tube-type 3-D NAND flash memory for the first time. We found that the early retention rapidly occurs within a few seconds and primarily originates from the lateral charge loss through the shared charge trap layer. The early retention was shown to be much worse for the C/P than for the S/P. Moreover, by measuring the early retention under various PV and EV levels, we concluded that the non-compensated residual holes at the edge of the cells play a significant role in early retention and, thus, should be optimized and balanced.

References

[1] J. Jang et al., VLSI Tech. Dig., p. 192, 2009. [2] C.-P. Chen et al., IEEE IEDM, p 118, 5, 2010. [3] E.-S. Choi et al., IEEE IEDM, p 211, 2012. [4] C. Kang et al., IRPS, pp. 167-169, 2007.

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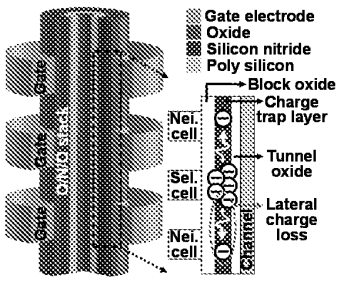


Fig. 1. Schematic of the 3-D NAND flash memory. Due to the shared charge trap layer, a fast charge loss (i.e., early retention) can occur in a lateral direction.

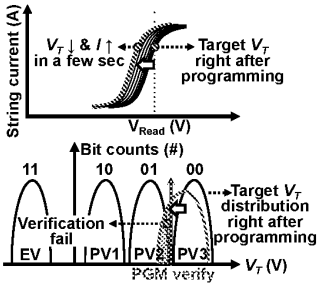


Fig. 2. Schematic of the early retention and its effect on V_T and I. The early retention threatens the MLC capability and the tight V_T distribution.

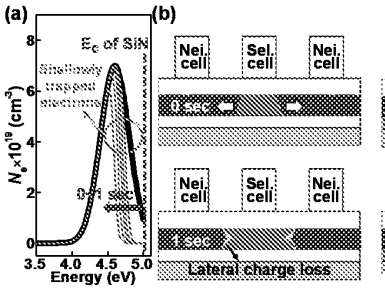


Fig. 3. (a) Simulated energy distribution of trapped electrons during the retention time (1 sec): input trap level (black line) and extracted trap levels (red line). (b) Simulated contours of the redistribution of the trapped electrons during the retention time (1 sec).

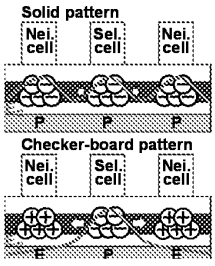


Fig. 4. (a) Schematic of the trapped electrons and holes at two different cell states, such as a S/P and a C/P. The E_C of SiN is also shown for the comparison.

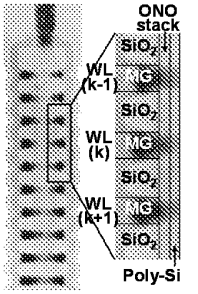


Fig. 5. TEM image of the tube-type 2y WL stacked 3-D NAND flash memory used in this work.

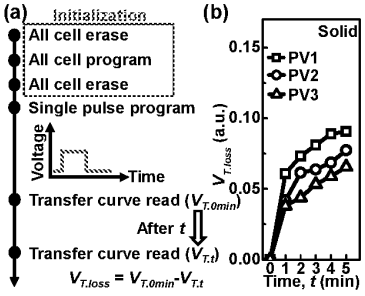


Fig. 6. (a) Sequences of the conventional DC I-V measurements. The early retention ($V_{T.loss}$) was measured by reading the transfer curves. (b) $V_{T.loss}$ vs. retention time. The fast charge loss occurred within 1 min.

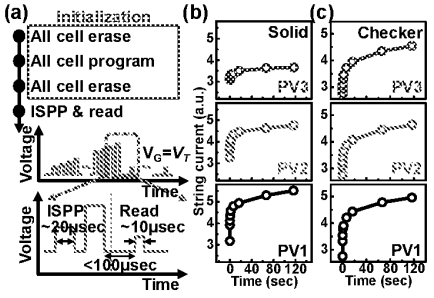


Fig. 7. (a) Sequences of the pulse I-V measurements. The ISPP was used for programming. String current vs. retention time from μsec to 120 sec as a parameter of the PV levels for the (b) S/P and (c) C/P.

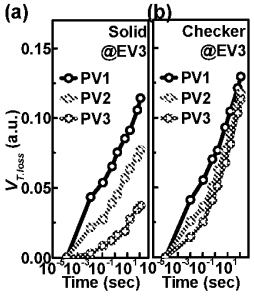


Fig. 8. Transformed early retention ($V_{T.loss}$) vs. retention time as a parameter of the PV levels for the (a) S/P and (b) C/P.

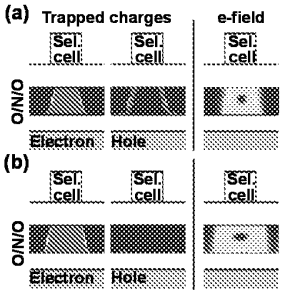


Fig. 9. Simulated contours of the trapped electrons and holes and corresponding electric field for (a) a small PV level and (b) a large PV level for the S/P.

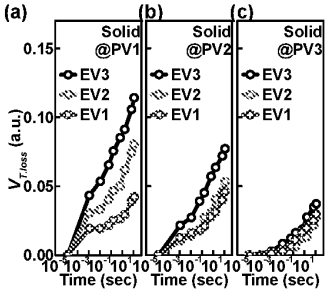


Fig. 10. $V_{T.loss}$ vs. retention time as a parameter of EV levels for different PV levels: (a) PV1, (b) PV2, and (c) PV3 for the S/P.

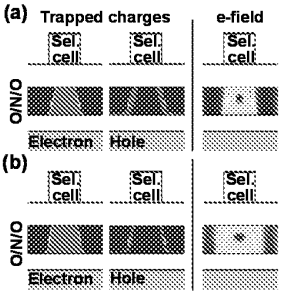


Fig. 11. Simulated contours of the trapped electrons and holes and the corresponding electric field for (a) a small PV level and (b) a large PV level for the C/P.

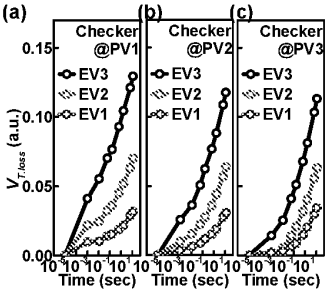


Fig. 12. $V_{T.loss}$ vs. retention time as a parameter of the EV levels for different PV levels: (a) PV1, (b) PV2, and (c) PV3 for the C/P.

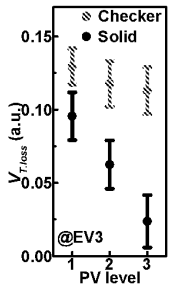


Fig. 13. Comparison of the early retention between the S/P and the C/P at a large EV level.

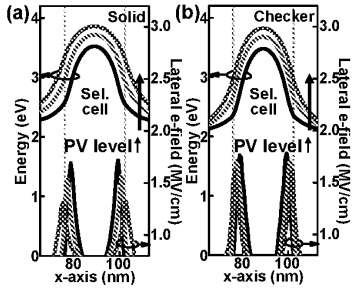


Fig. 14. Simulation of the E_C of SiN and the lateral electric field for (a) the S/P and (b) the C/P. The lateral electric field was more influenced by increasing the PV levels in the S/P than in the C/P.

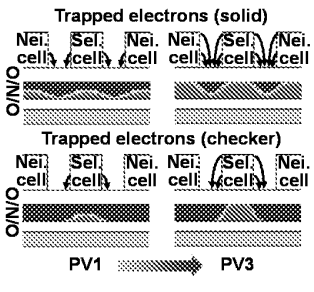


Fig. 15. Simulation of the trapped electrons in the S/P and the C/P. The trapped electrons between WLs in the S/P can easily compensate for the injected hole during erasing.

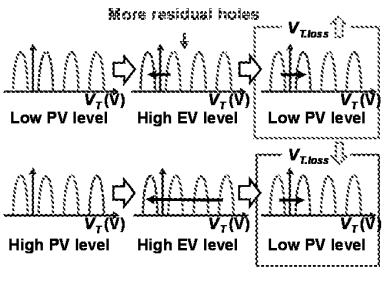


Fig. 16. Historical dependences of the early retention. The specific sequence, which was low PV level → high EV level → low PV level, may result in aggravated early retention due to residual holes at the edge of the selected cell. Therefore, balanced PV/EV levels are necessary.

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Vertical Cell Array using TCAT(Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory

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Abstract

Vertical NAND flash memory cell array by TCAT (Terabit Cell Array Transistor) technology is proposed. Damascened metal gate SONOS type cell in the vertical NAND flash string is realized by a unique 'gate replacement' process. Also, conventional bulk erase operation of the cell is successfully demonstrated. All advantages of TCAT flash is achieved without any sacrifice of bit cost scalability.

Introduction

Recently, in order to keep a trend of increasing bit density and reducing bit cost of NAND flash memories, three-dimensional Bit-Cost Scalable (BiCS) flash technology has been proposed [1]. However, there are two major concerns on the BiCS flash. First of all, it is almost impossible to implement metal gate structure for BiCS flash because it is very difficult to etch metal/oxide multilayer simultaneously. We cannot utilize various advantages of metal gate SONOS cell structure, for example, faster erase speed, wider Vth margin, and better retention characteristics [2]. Another concern is GIDL erase of BiCS flash. An extensive circuit change may be necessary to apply negative bias on word line during erase operation. Area penalty and limited erase voltage are expected.

In this paper, we propose vertical NAND flash memory cell array using TCAT technology for the first time. Above mentioned concerns can be cleared by the TCAT technology without any sacrifice of bit cost scalability.

Architecture and Key Features of TCAT Flash

Figure 1 and 2 show schematic Birds-eye view and the equivalent circuit of the TCAT flash memory. The process sequence is briefly displayed in Fig. 3. Distinctive structural differences with BiCS flash are i) oxide/nitride multilayer stack, ii) line-type 'W/L cut' etched through the whole stack between the each row array of channel poly plug, iii) line-type CSL formed by an implant through the 'W/L cut', iv) replaced metal gate lines for each row of poly plug. The most unique process is 'gate replacement' to achieve the metal gate SONOS structure. Figure 4 shows the detail. After 'W/L cut' dry etch and wet removal of sacrificial nitride layer, gate dielectric layers and gate metal are deposited in the conventional order. It is not 'gate first' process as for BiCS flash [3]. Separation of each gate node is followed by etch processes. Figure 5(a) and 5(b) show the cross sectional SEM images of the fabricated TCAT flash cell array. The cell string has six-NAND cell transistors with SSL transistor at the top and the GSL transistor at the bottom. The SSL and GSL transistors are formed simultaneously with cell transistors. The TEM view of the cell in Fig. 5(c) shows a perfect damascened metal gate SONOS structure in the vertical NAND flash cell string. The stair-like structure at the array edge for interconnection is shown in Fig. 6.

Figure 7 shows equivalent cell size trend of TCAT and BiCS flash. Despite of additional 'W/L cut' structure, cell size of TCAT flash is rather smaller than BiCS flash. It is due to 'gate first' process of BiCS flash. The minimum diameter of plug hole of BiCS flash is limited by the gate dielectric layers.

Another important feature of TCAT NAND flash memory is bulk erase operation. As shown in the schematic structure of Fig. 8, the channel poly plug in TCAT flash structure is connected to Si substrate, not n+ common source diffusion layer as in the BiCS flash. Therefore, conventional bulk erase operation can be achieved as displayed in the simulated profiles of Fig. 9 and the NAND string can be operated without any major peripheral circuit change.

Results and Discussions

Figure 10(a) and 10(b) show the Id-Vg characteristics of cell and selection transistors in a single string and the Vth distribution of cell transistors of 32 strings, respectively. Subthreshold slope is ~320mV/dec and the on-off ratio is more than 10^6. Despite poly Si channel, the Id-Vg characteristics and Vth distribution is excellent due to 'macaroni' body effect [3]. In order to suppress program disturb, Vth of selection transistors are adjusted by a device optimization. Figure 11 shows program/erase characteristics of a cell transistor. The erase operation is achieved by conventional bulk erase. The P/E speed of a cell is fast enough for multi-level cell operation. Erase saturation at ~-1V can be a concern, but it can be sufficiently lowered below -3V as the channel-hole diameter shrinks to a product level of ~45nm from 120nm of this paper. It is because that the electric field in tunnel layer becomes stronger as shown in Fig. 12. Endurance to 1E4 cycles is shown in Fig. 13 and long term data retention characteristics at 85℃ is shown in Fig. 14, respectively. Vth window of 5.6V remained after 10 years is good enough for multi-level operation.

Conclusion

We have successfully demonstrated the vertical NAND flash memory array by TCAT technology. Metal gate structure and bulk erase operation are key features of TCAT flash. With the metal gate structure, P/E characteristics and reliability is good enough for multi-level cell operation. TCAT flash is a more realistic future technology for ultra high density up to terabit

References

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[2] Chang Hyun Lee, et al, IEDM Tech. Dig., pp613-616, 2003
[3] Y. Fukuzumi, et al., IEDM Tech. Dig., pp449-452, 2007

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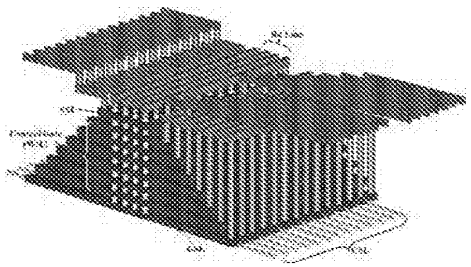


Fig.1 Birds-eye view of TCAT flash memory.

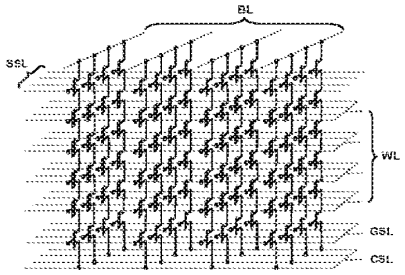


Fig. 2 Equivalent circuit of TCAT flash memory cell array.

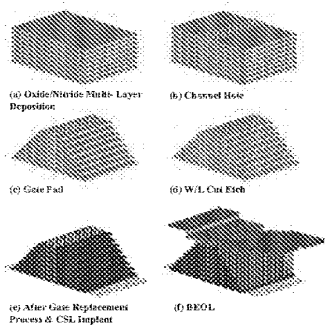


Fig. 3 Process sequence of TCAT flash memory.

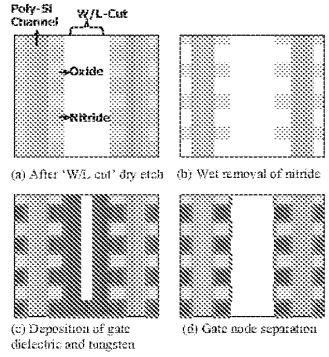


Fig. 4 Concept of the process flow named with 'gate replacement'.

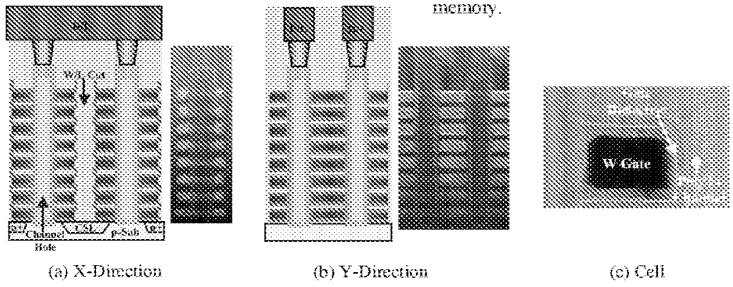


Fig. 5 Cross-sectional SEM images of TCAT flash memory cell strings, (a) X-direction, (b) Y-Direction (c) Enlarged TEM view of a cell in the vertical NAND string.

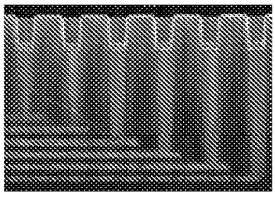


Fig. 6 Cross-sectional SEM image at cell array edge showing stair-like shaped word-line pad structure.

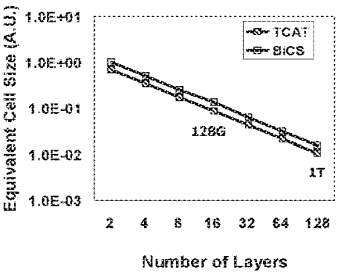


Fig. 7 Equivalent cell size trend of vertical NAND flash memories as stacked layers are doubled for each generation.

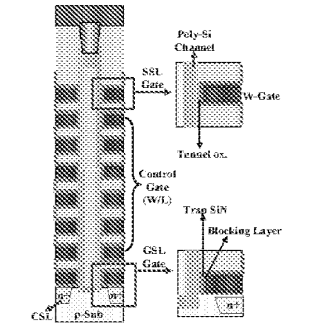


Fig.8 Schematic structures of TCAT flash cell string. Details of selection transistors are shown.

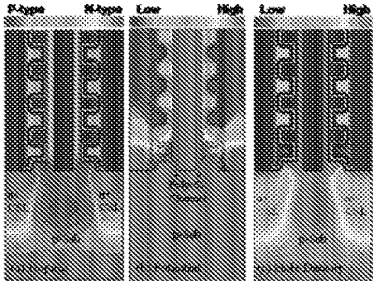


Fig. 9 Simulated profiles during bulk-erase operation of TCAT flash, (a) Doping, (b) Potential, (c) Hole density.

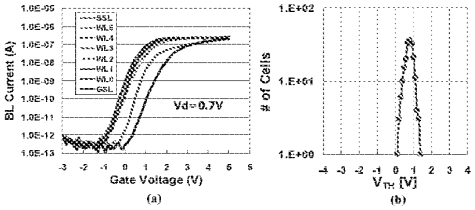


Fig. 10 (a) Id-Vg characteristics of cell and selection transistors in a single string, (b) Vth distribution of cells of 32 strings.

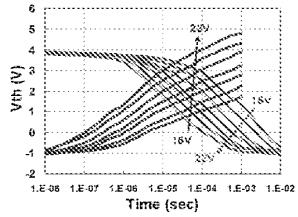


Fig. 11 P/E speed characteristics. Erase operation is achieved by conventional bulk-erase method.

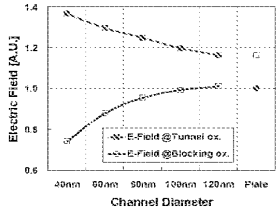


Fig. 12 Electric field in tunnel layer and blocking layer versus channel hole diameter.

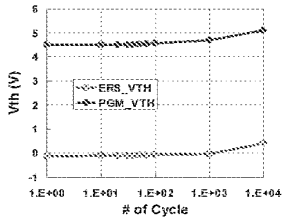


Fig. 13 Endurance characteristics of a TCAT flash cell.

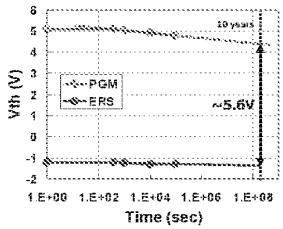


Fig. 14 Long term data retention characteristics of a TCAT flash cell at 85℃.

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Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node

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Abstract

For the first time, the 3 dimensionally stacked NAND Flash memory, is developed by implementing S^3 (Single-crystal Si layer Stacking) technology, which was used to develop S^3 SRAM previously. The NAND cell arrays are formed on the ILD as well as on the bulk to double the memory density without increasing the chip size. The feasibility of the technology was proven by the successful operation of 32 bit NAND Flash memory cell strings with 63nm dimension and TANOS structures. The novel NAND cell operational scheme, so called SBT (Source-Body Tied) scheme, is presented to maximize the advantages of 3 dimensionally stacked NAND cell structures.

Introduction

Recently, the great demands for higher density and lower bit cost in NAND Flash memories are growing because they are key devices for the mass data storage applications in various potable electronic products, such as portable audio and video players, cellular phones, USB memories and newly introduced solid state disks for PC. In order to keep trends of reducing the bit cost and increasing the bit density, the linear shrink of the patterns have been aggressively driven by developing MLC (Multi Level Cell) technology and early adopting the advanced lithographic tools .[1] However, the linear scaling down of the NAND Flash memories are approaching to the physical, electrical and reliability limitations, especially as the technology node is advancing to near 30nm dimension .

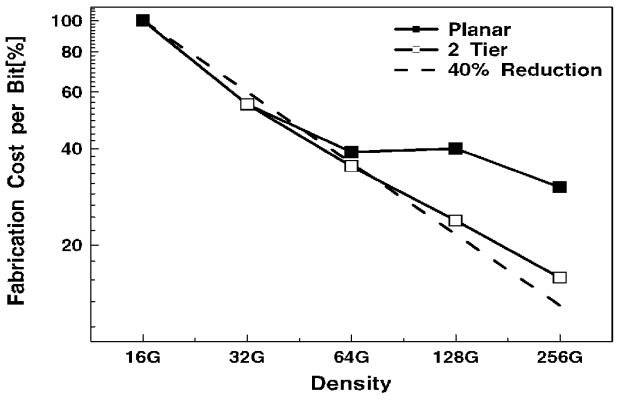
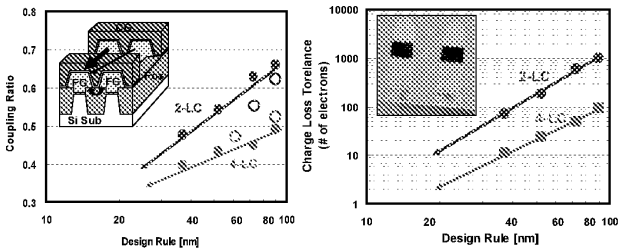


Fig. 1 Predictions of fabrication cost of NAND flash memory as the bit density increases for the planar cell and the stacked cell.

First, it has to use EUV lithography for the patterning, which is expected to be available after year 2009, according to ITRS roadmap. Even if the tool is prepared, a cost of the tool will be much more expensive and its throughput will not be comparable to those of the ArF lithography. From the standpoint of the bit cost, it means that even if the dimensions is shrunk and the density is increased, the bit cost down trends will not be kept up with the historical trends any more as shown in Fig1. The economic needs of the further shrink for the higher density will diminish and the bit growth rate in the data storage applications will slow down.

Secondly, from the electrical and reliability perspective, the further shrink below 30nm dimension, will cause the serious problems, such as electrical isolations between the word-lines and the cell nodes , the short channel effect, the cell current reduction and tolerable charge losses of the stored charges for data retention, which is less than 10, and etc. as shown in Fig.2 even in newly being developed SONOS-like structures. Furthermore, these problems are resulted from the fundamental physical limits, which are difficult to be overcome with the conventional modifications generally used in the past nodes.



(a) Coupling ratio limit **(b) Data retention limit**

Fig.2 Limitations of NAND flash memory with the shrinkage of D/R

Therefore, one of the best ways to circumvent these barriers caused by simple conventional linear shrink technology is to stack three dimensionally the cell arrays with minimizing the additional processes for stacking. As one of easy solutions to increase the density, chips or packages have been simply stacked with bonding or packing technology. However, the simple stacking process of the chips or packages cannot reduce the bit cost or the fabrication cost because they stack the already completely integrated chips. However, in our S^3 (Single-crystal Si layer Stacking) technology, the Si active layers are stacked with minimum processes and are interconnected simultaneously with the bottom cell arrays and the peripheral circuits.[2] Also, it can improve the electrical characteristics by reducing the capacitive and resistive loading without reducing the cell current.

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Process Integration

In the doubly stacked NAND Flash cell strings of Fig.3, the cell strings of the upper layers are stacked over the bottom layer ones already formed on the bulk Si Substrate. The cell strings have TANOS (TaN-AL2O3-Nitride-Oxide-Silcon) structures.[3]. In order to achieve same electrical characteristics of the cell strings in both layers, perfect SOI –like single crystal Si layers are formed on the ILD layers with S^3 technology. The bit line contacts and the common source lines are patterned simultaneously on the both layers of the cell string by etching layers vertically through the upper level Si layers to the bottom active layer as shown in Fig.4. The bit line holes are filled sequentially with the N-doped poly-Si and W. Therefore, both of the cell strings are connected through a single contact hole to the same bit line. The x-decoders of the upper and lower cell arrays are laid out separately at the other ends of the arrays as shown in Fig.5. Only three additional photo layers are used to double the density of NAND cell by stacking cell arrays on the ILD. The key processes are summarized in Table 1.

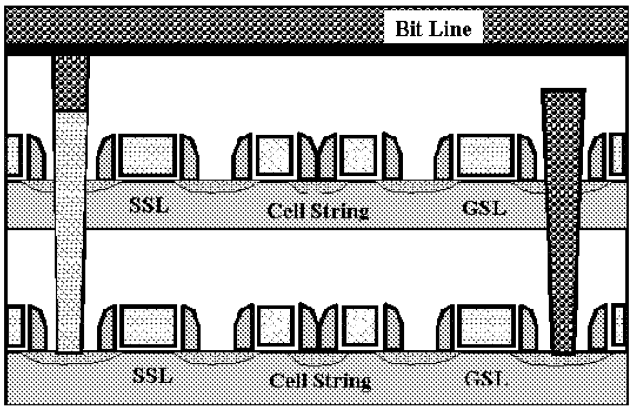


Fig. 3 Vertical structure of the 3D stacked cell string. Bit-line and common source line (CSL) are formed through 2nd active layer. Well bias is simultaneously applied by CSL. (Source-body tied)

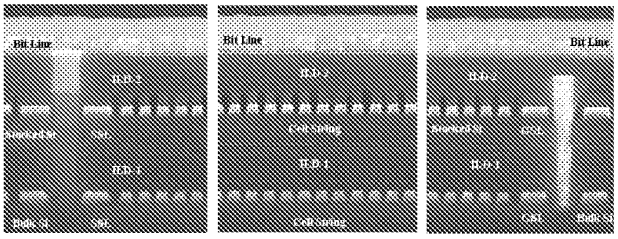


Fig. 4 Vertical SEM photograps of the fabricated 3D stacked NAND cell string. The 2nd active layer is SOI like perfect single crystal.

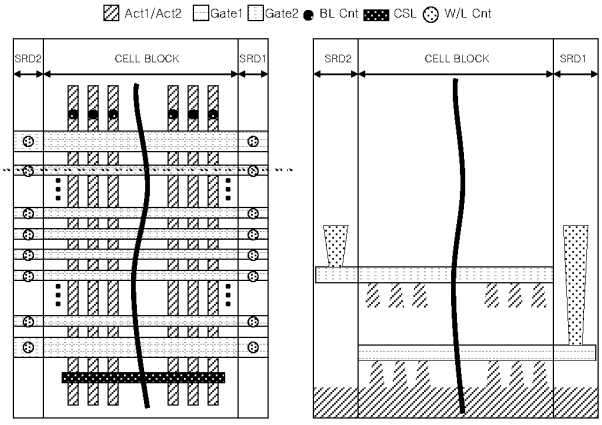


Fig. 5 Top view layout and vertical structure of word-lines and x -decoders for the doubly stacked NAND flash memory cell array.

Table I Summary of key process flow sequence for the 3D Stacked NAND flash memory.

- Well & Vth Adjust Implantation
- Active (Dual Trench Isolation)
- 1st Gate Stack Structure
  ; (Tunnel Ox/Trap SiN/Blocking Ox/TaN/WN+W)
- Gate-1 Poly Patterning
- Halo/LDD Implant, 1st Spacer, S/D Implant and RTA
- 1st ILD/ILD CMP
- ***Formation of Single Crystal Active Si for 2nd Cell String***
- 2nd Gate Stack Structure
  ; (Tunnel Ox/Trap SiN/Blocking Ox/TaN/WN+W)
- Gate-2 Poly Patterning
- Halo/LDD Implant, 1st Spacer, S/D Implant and RTA
- 2nd ILD/ILD CMP
- ***Cell Penetration Contact (for Source-Body Tied) Formation***
- Other Contacts and Metal (Bit Line)

Electrical Characteristics

Basically, the upper and lower cell strings were designed to have the same electrical characteristics. The characteristics of program and erase operations are shown in Fig.6 and Fig.7. The cell current characteristics of the upper cell strings under the worst cell bias condition are comparable with ones of the lower as shown in Fig.8. The reliability of the cell strings were measured. Fig.9 and Fig.10 show the characteristics of the endurance and the read disturbance in the stacked NAND cell strings, respectively. The differences between both cell strings are negligible. It was shown that the novel stacked NAND cell could satisfy the requirements of the NAND Flash memory product.

SBT (Source-Body Tied) Operational Scheme

In stacking NAND cell arrays, thin stacked Si layers are desirable for simplicity in integration of the processes. However, when a thin body is used, the body of the cell strings is disconnected with the other cell strings by trench isolations and is floated electrically. The cell strings with the floated body have a disadvantage in the erase operation as shown in Fig.11. In conventional body bias scheme, a block or whole cells of the string can be erased simultaneously because the body is biased negatively and all word-lines are grounded. However, in the

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floating thin body scheme, only one cell of the string can be erased at one time because the word-lines of other cells are biased at Vpass to connect the channel of the selected cell. The erase time of the product will be increased by 32 times. Therefore, in order to solve the erase problem in SOI type thin body structures, the novel operational scheme is suggested. The common source of the cell string is tied with the body of the string electrically. This scheme can erase the cell strings in an exactly same way as the conventional body bias scheme does.

But, in program operations, inhibited WL0 cell can be interfered by the leakage current through the SSL to the ground due to coupling of the grounded SSL gate as shown in Fig.12. The channel potential of the WL0 cell will not follow the program voltage of the WL0 gate. It can be improved by applying negative bias, such as -1.2V at the SSL gate as shown in Fig.13. The interference characteristics of the WL0 cell for various bias conditions are shown in Fig.14.

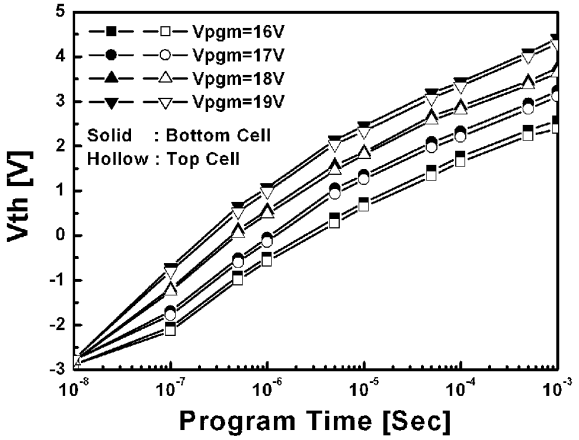


Fig. 6 Comparisons of the program speed characteristics between the top cell and the bottom cell of the stacked NAND cell strings

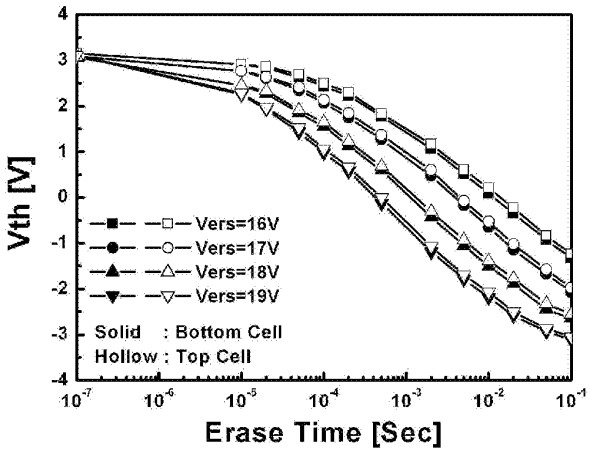


Fig. 7 Comparisons of the erase speed characteristics between the top cell and the bottom cell of the stacked NAND cell strings.

Conclusions

For the first time, the 3 dimensionally stacked NAND Flash memory cell arrays are formed on the ILD as well as on the bulk to double the memory density without increasing the chip size by implementing S^3 technology. The feasibility of the technology was proven by the successful operations of 32 bit NAND Flash memory cell strings with 63nm dimension, TANOS structures, and the novel SBT (Source-Body Tied) operational scheme.

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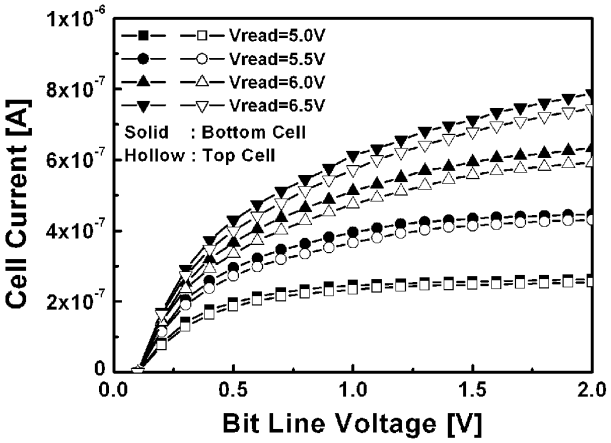


Fig. 8 The characteristics of cell current between the top cell strings and the bottom cell strings under the worst bias condition.

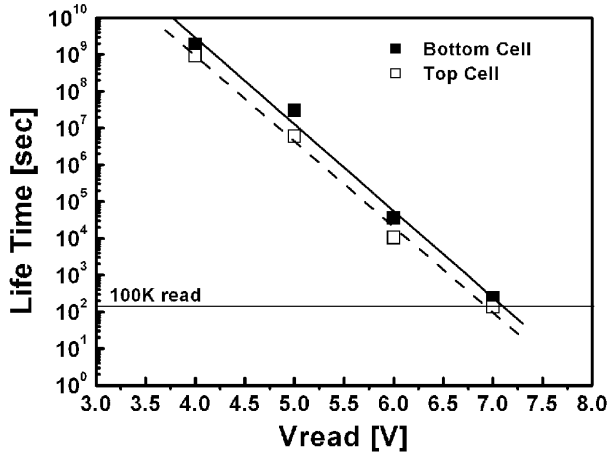


Fig. 9 Comparison of read disturbance characteristics between top cell and bottom cell.

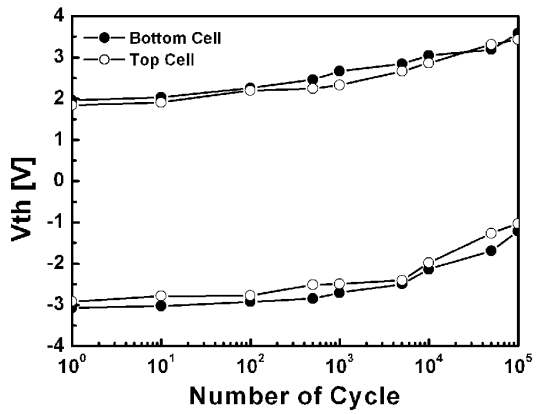


Fig. 10 Endurance characteristics of the top cell and the bottom cell of the stacked NAND cell strings

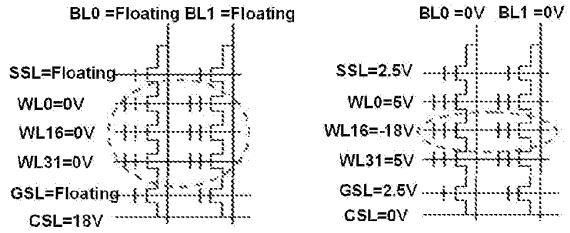


Fig. 11 Comparisons of the erase operation (a) Erase by page *without* well bias. (b) Erase by block *with* well bias.

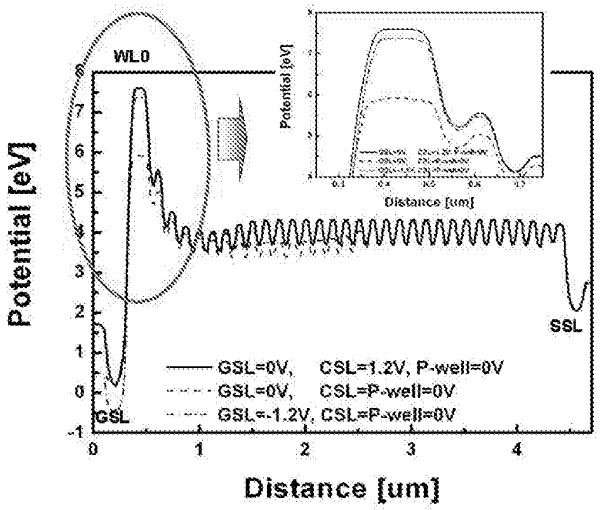
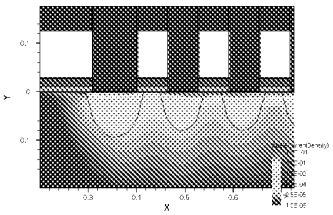
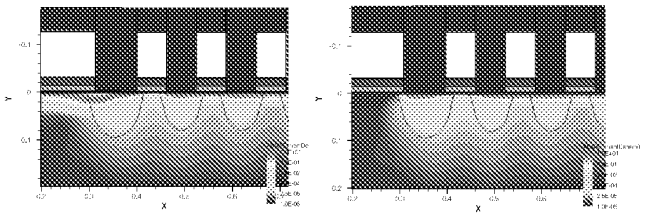


Fig. 12 Potentials of the inhibited cells at the various bias conditions during the program operation. WL0 is Vpgm and other word lines are Vpass. At the condition of dotted-line, the channel potential of inhibited cell is lowered and it resulted in poor boosting.



(a)GSL=0V, CSL=1.2V, P-well=0V (normal)



(b)GSL=0V, CSL=P-well=0V (Source-Body Tied)

(c)*GSL=-1.2V*, CSL=P-well=0V (Source-Body Tied)

Fig. 13 Current density comparisons of inhibited cells.; WL0=Vpgm, Other WLs=Vpass. At the (b) condition, some leakage current is observed at GSL Tr. , It results in lowered channel potential of the adjacent cell Tr. (inhibited WL0 cell) as shown in Fig. 12.

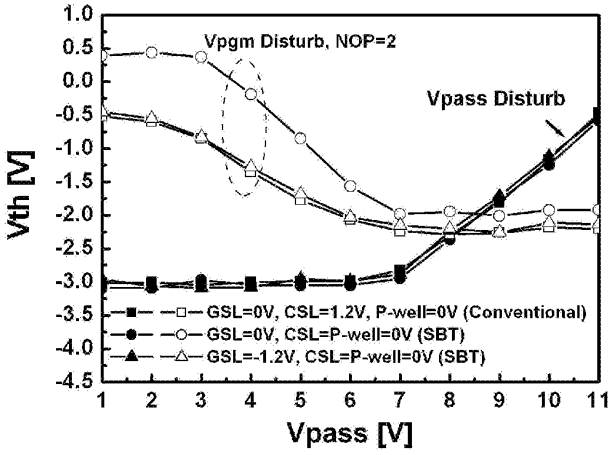


Fig. 14 Comparisons of the interference characteristics the cell strings at the bias conditions of the source-body tied scheme and the conventional well bias condition .

A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory

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Abstract

A double-layer TFT NAND-type Flash memory is demonstrated, ushering into the era of three-dimensional (3D) Flash memory. A TFT device using bandgap engineered SONOS (BE-SONOS) [1,2] with fully-depleted (FD) poly silicon (60 nm) channel and tri-gate P^+-poly gate is integrated into a NAND array. Small devices (L/W=0.2/0.09 μm) with excellent performance and reliability properties are achieved. The bottom layer shows no sign of reliability degradation compared to the top layer, indicating the potential for further multi-layer stacking. The present work illustrates the feasibility of 3D Flash memory.

I. Introduction

Recently, the NAND flash becomes very popular for portable electronics, and the demand for memory density multiplies every year. Although NAND Flash is aggressively scaled [3,4], it becomes more and more difficult to follow Moore's law to continue the scaling due to both process and device limitations. Three-dimensional (3D) multi-layer-stack memory is another path to ultra-high density memory.

We demonstrated a low-thermal budget TFT NAND device recently [2]. The TFT memory employs BE-SONOS [1] device, which provides both efficient hole tunneling erase and good data retention [1]. Moreover, BE-SONOS uses only matured frond-end materials (oxide, nitride and poly gate). This greatly enables the multi-layer stack capability without metal contamination issues. In this work, we further fabricate a double-layer TFT NAND Flash. The performance and reliability of bottom and top layers are examined to provide guidelines for further multi-layer stacking. The effects of device dimension, reliability, and NAND array operation are addressed.

II. Fabrication

The typical device parameters and fabrication flow are shown in Table 1 and Table 2. Figures 1-4 show the cross-sectional views of the double layer TFT NAND devices. The TFT device has a 60 nm thick poly silicon channel over the buried oxide. The poly silicon is an amorphous silicon (a-Si) layer deposited by low-pressure chemical vapor deposition (LPCVD) process, followed by a low-temperature thermal annealing (600 ^{0}C) for crystallization. A multi-layer O1/N1/O2 tunneling dielectric is used to achieve easy hole tunneling during erase, while eliminating the direct tunneling leakage during retention [1]. Next, SiN trapping layer (N2) and top blocking oxide (O3) are grown. A heavily doped P^+-poly gate is adopted to suppress the gate injection during –FN erase. The multi-layer ONONO are shown in Fig. 1. The device has a tri-gate structure as shown in Fig. 2.

The top oxide process has the largest thermal budget. Two top oxide (O3) formation processes are compared: an LPCVD oxide (HTO) with rapid thermal annealing, and an in-situ steam generation (ISSG) oxidation to convert a portion of the trapping nitride (N2) into oxide.

After gate patterning, shallow junction is formed by low-energy As^+ implantation. Planarization is then carried out by HDP oxide deposition and CMP. After forming the bottom-layer TFT devices, the processes are duplicated to form the top-layer TFT devices. Contact etching for the two layers are performed independently to avoid over etching. The final double-layer TFT NAND Flash memory is shown in Figs. 3-4.

III. Device Characterization

(a) Short-Channel Effect:

The *I-V* and V_T for the memory cells with various channel lengths are shown in Figs. 5, 6, respectively. Similar to bulk devices, the transconductance (g_m) increases with shorter channel lengths. Figure 6 shows that the –FN erased state (-17 V, 50 msec) follows the same Vt-roll-off characteristics with the initial state, but with 3 V lower Vt. ISSG and HTO top oxide devices show similar Vt roll-off trends.

(b) Narrow-Width Effect:

The *I-V* characteristics for memory cells with various channel widths are shown in Fig. 7. Generally a narrower device shows a better subthreshold slope (S.S.). Figure 8 shows that for a narrow device the transconductance per width (g_m/W) increases, while Vt decreases. Thus a narrower device has a better DC performance due to better gate control capability of the tri-gate structure.

(c) Program/Erase Characteristics:

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The device is programmed by +FN electron injection (Fig. 9), and erased by –FN hole tunneling (Fig. 10). P^+-poly gate is used to suppress the gate electron injection during –FN erase. Accordingly, the device can be erased into depletion mode. Both +FN program and –FN erase saturate for each bias voltage. Samples with ISSG and HTO top oxide show similar P/E speed.

(d) P/E Cycling Endurance:

The P/E cycling endurance is shown in Fig. 11. Erase degradation occurs at < 1K dumb-mode cycles. ISSG top oxide devices show better endurance than those with HTO top oxide. The top oxide process has large impact on the cell endurance because top oxide suffers a large electric field stress during P/E, while the top oxide has lower quality due to the lower thermal process.

The endurance of TFT device is understandably inferior to the bulk BE-SONOS device [1,5], where a high-temperature (950~1000 ^{0}C) process is used to convert nitride into top oxide. The reason may be attributed to that the lower temperature ISSG and HTO top oxides have lower quality that easily trap charges after P/E cycle stressing, resulting in lower endurance.

Adjusted P/E cycling (as commonly practiced) achieves better endurance (Fig. 12). The corresponding P/E shot numbers are recorded in Fig. 13. After 1K cycling the device starts to degrade and more P/E shots are needed to maintain the Vt levels. Figure 14 illustrates that ISSG top oxide has a better subthreshold slope than HTO top oxide. Typical *IV* characteristics during 10K P/E cycling are shown in Fig. 15.

IV. Comparison between the Top and Bottom Layers

Figure 16 compares the V_T-roll-off of erase saturation state for the bottom and top layers. The bottom layer has a slightly faster V_T-roll-off. In addition, the V_T distribution of the bottom-layer is wider. This is because the bottom layer undergoes a higher thermal budget. For better bottom layer performance thermal budget should be further reduced.

The P/E cycle endurance, S.S. degradation, and retention are shown in Figs. 17, 18 and 19, respectively, for the short-channel device (Lg/W=0.2/0.09 um). The bottom layer shows no sign of reliability degradation compared to the top layer. This indicates that further multi-layer stack is feasible.

V. NAND Array Functions

The reading method for the NAND array is shown in Fig. 20. Since TFT NAND array has higher series resistance compared to the bulk device, read current saturates at large gate overdrive. The read current is enhanced by increasing V_{PASS}. For V_{PASS}=7 V, and V_{READ}=1 V, the read current for a 16-string NAND array approaches 1 μA, ample for data Flash design.

The program-inhibit characteristics of TFT NAND array are illustrated in Fig. 21. Cells C and D are under medium-field gate disturb, while cell B can be program-inhibited by raising the channel potential.

VI. Summary

For the first time, a successful double-layer TFT NAND Flash memory is demonstrated. The experimental results are very encouraging for future 3D Flash memories.

VII. Acknowledgements

Special thanks to Dr. R.I. Huang, Dr. S.P. Hong, Martin Wu, Dr. Chris Luoh, Terence Hung, C.F. Chen, Bear Wu and Tammy Lin, Technology Development Center in Macronix Inc., for the important cooperation and contributions to this work.

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Poly channel thickness	60 nm
O1	1.5 nm (ISSG)
N1	2 nm (LPCVD)
O2	2 nm (LPCVD)
N2	7 nm (LPCVD)
O3	9 nm (ISSG or HTO)
Poly gate	P+-poly
Channel length	0.2 um
Channel width	0.09 um

Table 1 Typical process condition of TFT NAND device.

1. Si substrate	9. N+ S/D & pocket implantation
2. Buried oxide	10. HDP CVD deposition
3. a-Si channel deposition	11. Oxide CMP planarization
4. Low-temperature annealing	12. Repeat processes from a-Si to N+ S/D implantation
5. Channel patterning	13. ILD deposition and planarization
6. P-type well doping	14. Contact patterning
7. BE-SONOS: ONONO formation	15. Metal deposition and patterning
8. P+poly gate patterning	16. Alloy annealing

Table 2 Fabrication flow of multi-layer TFT NAND device

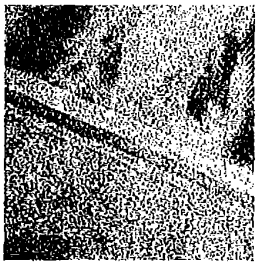


Fig. 1 TEM of the O1/N1/O2/N2/O3 structure for TFT BE-SONOS.

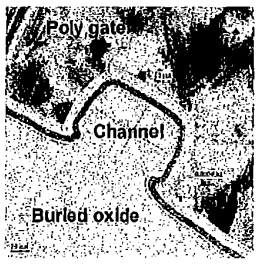


Fig. 2 Tri-gate structure of the TFT device.

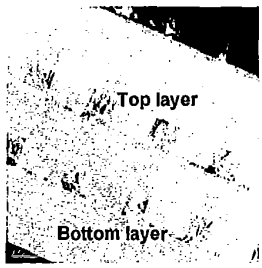


Fig. 3 Channel-length direction of double-layer TFT NAND devices.

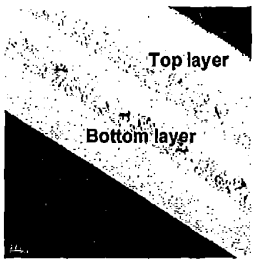


Fig. 4 Channel-width direction of double-layer TFT NAND devices.

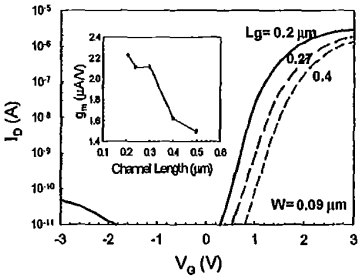


Fig. 5 *IV* characteristics for various channel length devices. Inset shows the corresponding transconductance (g_m). The channel width is 0.09 μm.

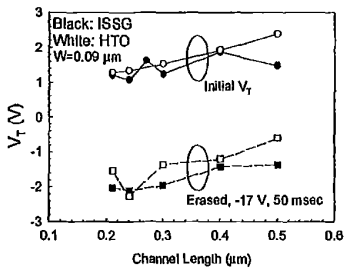


Fig. 6 Short-channel V_T roll-off characteristics for both the initial state and the –FN erased state, with ISSG and HTO top oxide.

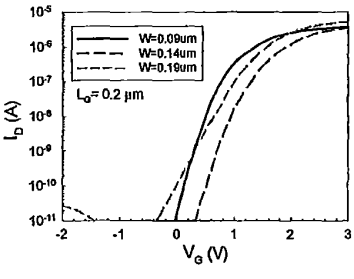


Fig. 7 *IV* characteristics for various channel width devices. Wider devices show worse subthreshold behavior. The channel length is 0.2 μ m.

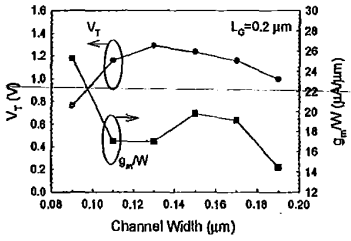


Fig. 8 Narrow-width characteristics. Both normalized transconductance (g_m/W) and V_T are shown. The narrowest device (W=0.09 μm) has the best performance.

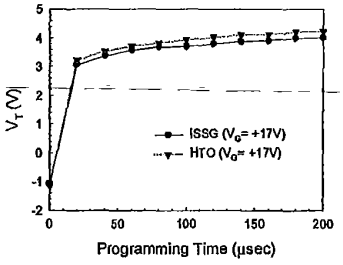


Fig. 9 Comparison of the +FN program characteristics for ISSG and HTO top oxide.

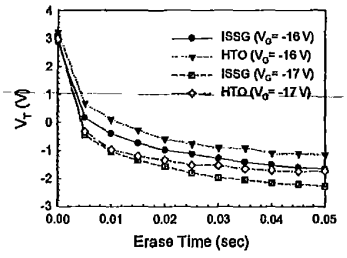


Fig. 10 Comparison of the -FN erase characteristics for ISSG and HTO top oxide.

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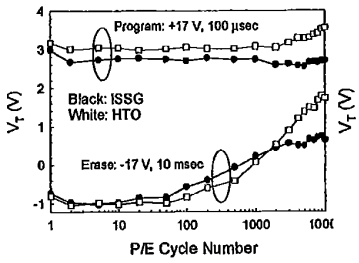


Fig. 11 Dumb-mode P/E cycling endurance (without adjusting the P/E conditions during endurance test). Both ISSG and HTO top oxide are compared.

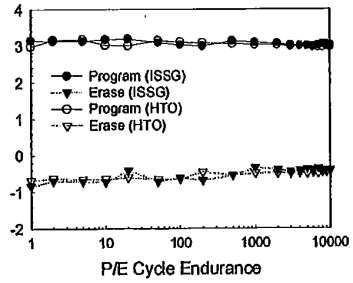


Fig. 12 P/E cycling endurance (with adjusted P/E conditions during endurance test). Both ISSG and HTO top oxide are compared.

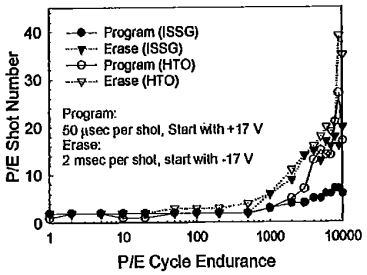


Fig. 13 The required P/E shot number during adjusted P/E tests in Fig. 12. Both ISSG and HTO top oxide are compared.

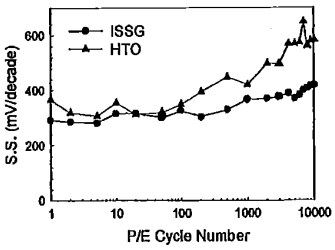


Fig. 14 Subthreshold slope degradation during 10K P/E cycling tests. Both ISSG and HTO top oxide are compared.

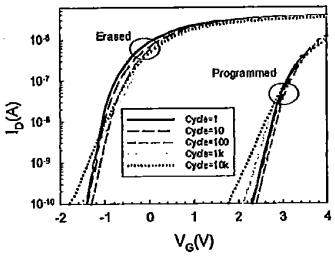


Fig. 15 *IV* characteristics of ISSG top oxide device during 10K P/E cycling endurance testing.

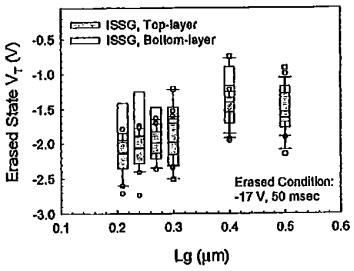


Fig. 16 Short-channel effect comparison of the top and bottom layer TFT NAND devices. A total of 28 identical devices are measured. The devices are in erase saturation state.

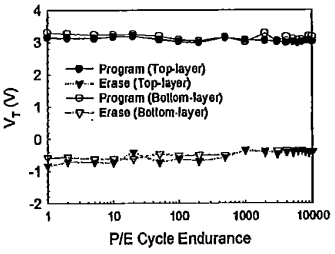


Fig. 17 Adjusted P/E cycling endurance (with adjusted P/E conditions during endurance test). Both bottom and top layers are compared. ISSG top oxide is used.

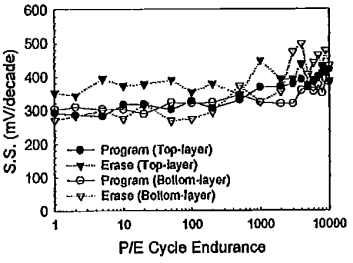


Fig. 18 Subthreshold slope degradation during 10K P/E cycling tests. Both bottom and top layers are compared. ISSG top oxide is used.

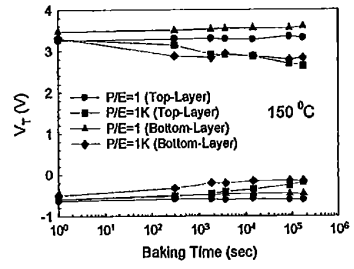
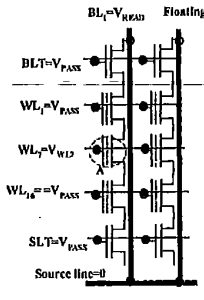


Fig. 19 Retention characteristics. Programmed and erased state with various cycle endurance are compared.



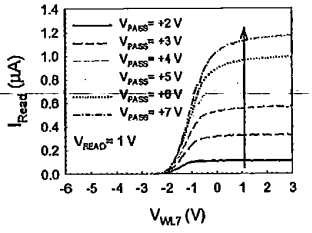
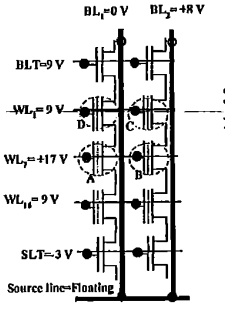


Fig. 20 Read current of a 16 WL's TFT NAND array. The devices are in erased state. For V_{PASS}=+7 V, read current can approach 1 µA, sufficient for NAND Flash design.



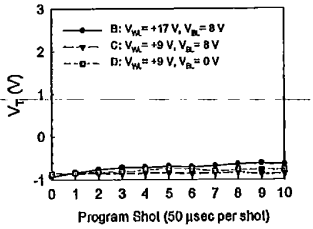


Fig. 21 Program disturb of a TFT NAND array. Cells C and D are under medium field gate disturb, while cell B can be program-inhibited by raising the channel potential.

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Electronic Acknowledgement Receipt

EFS ID:	29380903
Application Number:	15410965
International Application Number:	
Confirmation Number:	3219
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	HANG-TING LUE
Customer Number:	46353
Filer:	Yiding Wu/Kathryn Marley
Filer Authorized By:	Yiding Wu
Attorney Docket Number:	MXIC 2194-1
Receipt Date:	02-JUN-2017
Filing Date:	20-JAN-2017
Time Stamp:	13:53:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	00597513.PDF	1035440 6a46771e146b484206c29ce880fcc811ccdb fb14	no	4

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Information:					
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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/410,965	01/20/2017	HANG-TING LUE	MXIC 2194-1	3219

46353 7590 11/29/2017

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019

EXAMINER
ENAD, CHRISTINE A

ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
11/29/2017	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hmbay.com

Micron Ex. 1022, p. 87
Micron v. YMTC
IPR2024-00912

Office Action Summary	Application No. 15/410,965	Applicant(s) LUE, HANG-TING	
	Examiner CHRISTINE ENAD	Art Unit 2823	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/20/2017*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-24* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-24* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date *6/2/2017*.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

Claims 1-4, 6, 11-17, 20-22, 24 are rejected under 35 U.S.C. 102(a) (1) as being anticipated by Serov et al (US Publication No 2016/0071861).

Regarding claim 1, Serov discloses a memory device, comprising: a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips alternating with insulating strips **Fig 9A-10, 32**, the insulating strips in the stacks having first and second sides, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks **Fig 9A-10**; vertical channel pillars **Fig 9A-10, 601/602/62** disposed between the stacks, the vertical channel pillars having first **Fig 9A-10, 601** and second channel films **Fig 9A-10, 602** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 9A-10, 62** (Paragraph 0150) between and contacting the first and second channel films; and data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips **Fig 9A-10, (42/46)** in the

stacks, the data storage structures including tunneling layers **Fig 9A-10, 56** in contact with the vertical channel pillars, discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56**, and blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips, the discrete charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions on the first sidewalls of the conductive strips **Fig 9A-10**.

Regarding claim 2, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions are dielectric charge trapping elements (Paragraph 0143).

Regarding claim 3, Serov discloses the conductive strips in the stacks have second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions on the second sidewalls of the conductive strips; and the data storage structures include discrete charge trapping elements disposed in the second recessed regions in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements in the second recessed regions and the second sidewalls of the conductive strips **Fig 9A-10.**

Regarding claim 4, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** disposed in the second recessed regions are dielectric charge trapping elements (Paragraph 0043).

Regarding claim 6, Serov discloses the conductive strips in the plurality of stacks of conductive strips include a metal material (Paragraph 0133).

Regarding claim 11, Serov discloses a manufacturing method, comprising: forming a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips **Fig 9A-10, (42/46)** alternating with insulating strips **Fig 9A-10, 32**, the insulating strips **Fig 9A-10, 32**in the stacks having first and second sides **Fig 9A-10**, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls; recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks **Fig 5A-5C;** forming data storage structures in the first recessed regions **Fig 6A-8C;** forming first and second channel films **Fig 9A-10, 60** on the data storage structures on sidewalls of adjacent stacks; and depositing a dielectric material **Fig 9A-10, 62** between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks **Fig 9A-10**.

Regarding claim 12, Serov discloses said forming the data storage structures comprising: depositing blocking layers **Fig 9A-10, 52** over the first sidewalls of the conductive strips in the first recessed regions; depositing charge trapping material **Fig 9A-10, 54** over the blocking layers **Fig 9A-10, 52** in the first recessed regions; and depositing tunneling layers **Fig 9A-10, 56** over the charge trapping material **Fig 9A-10, 54** in the first recessed regions.

Regarding claim 13, Serov discloses wherein the charge trapping material is dielectric charge trapping material (Paragraph 0143).

Regarding claim 14, Serov discloses comprising: said depositing the blocking layers **Fig 9A-10, 52** including depositing the blocking layers **Fig 9A-10, 52** over the first sides of the insulating strips **Fig 6B**; and said depositing the charge trapping material **Fig 9A-10, 54** including depositing the charge trapping material **Fig 9A-10, 52** over the blocking layers **Fig 6B** over the first sides of the insulating strips **Fig 6B**; and separating the charge trapping material between adjacent first recessed regions **Fig 6A-6C.**

Regarding claim 15, Serov discloses said separating the charge trapping material **Fig 9A-10, 54** including removing the charge trapping material over the blocking layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions **Fig 6A-8C.**

Regarding claim 16, Serov discloses comprising: etching to isolate the data storage structures along the conductive strips, to form discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56** and the blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips.

Regarding claim 17, Serov discloses wherein the conductive strips in the stacks of conductive strips have second sidewalls opposite the first sidewalls **Fig 9A-10**, the manufacturing method comprising: recessing the second sidewalls of the conductive strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks; and forming the data storage structures in the second recessed regions **Fig 5A-10.**

Regarding claim 20, Serov discloses a manufacturing method, comprising: forming a plurality of stacks **Fig 9A-10, 32/(42/46)** of sacrificial strips **Fig 9A-10, 42** alternating with insulating strips **Fig 9A-10, 32**, the insulating strips **Fig 9A-10, 32**in the stacks having first and second sides **Fig 9A-10**, and the sacrificial strips **Fig 9A-10, 42** in the stacks having first sidewalls; recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks **Fig 5A-5C;** forming data storage structures in the first recessed regions **Fig 6A-8C;** forming first and second channel films **Fig 9A-10, 60** on the data storage structures on sidewalls of adjacent stacks; and depositing a dielectric material **Fig 9A-10, 62** between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks **Fig 9A-10**, and replacing the sacrificial strips in the stacks with a metal material **Fig 10, 46.**

Regarding claim 21, Serov discloses said forming the data storage structures comprising: depositing blocking layers **Fig 9A-10, 52** over the first sidewalls of the conductive strips in the first recessed regions; depositing charge trapping material **Fig 9A-10, 54** over the blocking layers **Fig 9A-10, 52** in the first recessed regions; and depositing tunneling layers **Fig 9A-10, 56** over the charge trapping material **Fig 9A-10, 54** in the first recessed regions.

Regarding claim 22, Serov discloses wherein the charge trapping material is dielectric charge trapping material (Paragraph 0143).

Regarding claim 24, Serov discloses said replacing comprising: etching the stacks to form a trench, exposing the sacrificial strips in the trench; removing the sacrificial strips in the trench; depositing the metal material in the trench; and separating the metal material between the insulating strips in the trench (Paragraph 0152-0154).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5, 7-10, 18-19, 23 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861) in view of Liu et al (US Publication No. 2016/0204117).

Regarding claims, 5, 19, and 23, Serov discloses all the limitations except for the gap in the channel region. Whereas Liu discloses leaving a gap between the first and second vertical channel films **Fig 2A-4B** (Paragraph 0075-0076). Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the device of Serov and incorporate a gap to provide a connector between device levels.

Regarding claim 18, Liu discloses etching to isolate the first and second channel films and the dielectric material between the first and second channel films along the conductive strips, to form vertical channel pillars between the stacks, so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of

conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips **Fig 2A-4B** (Paragraph 0075-0076).

Regarding claim 7, Serov discloses a memory device, comprising: a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips alternating with insulating strips **Fig 9A-10, 32**, the insulating strips in the stacks having first and second sides, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks **Fig 9A-10;** and having second sidewall opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions in sides of the stacks **Fig 9A-10;** vertical channel pillars **Fig 9A-10, 601/602/62** disposed between the stacks, the vertical channel pillars having first **Fig 9A-10, 601** and second channel films **Fig 9A-10, 602** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 9A-10, 62** (Paragraph 0150) between and contacting the first and second channel films; and data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips **Fig 9A-10, (42/46)** in the stacks, the data storage structures including tunneling layers **Fig 9A-10, 56** in contact with the vertical channel pillars, discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56**, and blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips and between the discrete charge trapping elements and the second sidewalls of the conductive strips **Fig 9A-10**, the discrete

charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions on the first sidewalls of the conductive strips and disposed in the second recessed regions on the second sidewalls of the conductive strips **Fig 9A-10.** Serov discloses all the limitations except for the offset in the channel region. Whereas Liu discloses the vertical channel pillars are arranged so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips **Fig 2A-4B** (Paragraph 0075-0076). Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the device of Serov and incorporate an offset to provide a connector between device levels.

Regarding claim 8, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** are dielectric charge trapping elements (Paragraph 0143).

Regarding claim 9, Serov discloses wherein the dielectric material comprises a gap **Fig 2A-4B** (Paragraph 0075-0076).

Regarding claim 10, Serov discloses the conductive strips in the plurality of stacks of conductive strips include a metal material (Paragraph 0133).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTINE ENAD whose telephone number is

(571)270-7891. The examiner can normally be reached on Monday - Thursday, 7:30 am - 6:00 pm, EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272 9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/CHRISTINE ENAD/
Primary Examiner, Art Unit 2823

Notice of References Cited	Application/Control No. 15/410,965	Applicant(s)/Patent Under Reexamination LUE, HANG-TING	
	Examiner CHRISTINE ENAD	Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2016/0071861 A1	03-2016	Serov; Andrey	H01L27/11556	365/185.19
*	B	US-9,111,617 B2	08-2015	Shim; Sunil	G11C16/0466	1/1
*	C	US-2017/0243879 A1	08-2017	YU; Jixin	H01L21/0214	1/1
*	D	US-9,177,966 B1	11-2015	Rabkin; Peter	H01L27/11582	1/1
*	E	US-9,147,468 B1	09-2015	Lue; Hang-Ting	G11C11/5671	1/1
*	F	US-2015/0179661 A1	06-2015	Huo; Zongliang	H01L21/764	257/57
*	G	US-2016/0204117 A1	07-2016	Liu; Jin	H01L29/66825	257/324
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Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Micron v. YMTC
IPR2024-00912

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)
Approved for use through 07/31/2016. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	15410965
Filing Date	2017-01-20
First Named Inventor	Hang-Ting Lue
Art Unit	2823
Examiner Name	Christine A. Enad
Attorney Docket Number	MXIC 2194-1

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	1	20140061776	A1	2014-03-06	KWON et al.	
	2	20160260733	A1	2016-09-08	LUE	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15410965
	Filing Date	2017-01-20
	First Named Inventor	Hang-Ting Lue
	Art Unit	2823
	Examiner Name	Christine A. Enad
	Attorney Docket Number	MXIC 2194-1

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Choi et al., "Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND flash memory," 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, 14-16 June 2016, pp. 1-2.	
	2	Jang et al., "Vertical cell array using TCAT(Terabit Cell Array Transistor) technology for ultra high density NAND flash memory," 2009 Symposium on VLSI Technology, Honolulu, HI, 16-18 jUNE 2009, pp. 192-193.	
	3	Jung et al, "Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node," International Electron Devices Meeting, 2006. IEDM '06, 11-13 Dec. 2006, pp 1 - 4.	
	4	Lai et al., "A Multi-Layer Stackable Thin-Film Transistor (TFT) NAND-Type Flash Memory," International Electron Devices Meeting, 2006. IEDM '06, 11-13 Dec. 2006, pp 1-4.	

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/CHRISTINE A ENAD/	Date Considered	11/24/2017

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	15410965
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	Art Unit	2823
	Examiner Name	Christine A. Enad
	Attorney Docket Number	MXIC 2194-1

CERTIFICATION STATEMENT

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OR

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SIGNATURE

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Signature	/Yiding Wu/	Date (YYYY-MM-DD)	2017-06-02
Name/Print	Yiding Wu	Registration Number	65,992

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15410965	LUE, HANG-TING
	Examiner	Art Unit
	CHRISTINE ENAD	2823

CPC- SEARCHED		
Symbol	Date	Examiner
H01L27/11582	11/24/2017	CE
H01L21/76802, 21/76877	11/24/2017	CE
H01L23/5226, 23/528	11/24/2017	CE

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
Assignee and inventor search conducted	11/24/2017	CE
CPC search	11/24/2017	CE
EAST Search	11/24/2017	CE

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/CHRISTINE ENAD/ Primary Examiner.Art Unit 2823

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CONFIRMATION NO. 3219

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/410,965	01/20/2017 RULE	257	2823	MXIC 2194-1

APPLICANTS
MACRONIX INTERNATIONAL CO., LTD., Hsinchu, TAIWAN;

INVENTORS
HANG-TING LUE, HSINCHU, TAIWAN;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
01/27/2017

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /CHRISTINE A ENAD/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		TAIWAN	12	24	4

ADDRESS

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019
UNITED STATES

TITLE

DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE

FILING FEE RECEIVED		
2340	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	2	("20160204117").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/24 13:25
S1	574	(("MACRONIX") near3 ("INTERNATIONAL") near3 ("CO") near3 ("LTD")).AANM.	USPAT	OR	OFF	2017/11/22 09:51
S2	358	(("LUE") near3 ("HANG-TING")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 09:51
S3	9877	(H01L27/11582.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:51
S4	13188	(H01L21/76802.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:51
S5	17402	(H01L21/76877.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S6	15471	(H01L23/5226.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S7	13459	(H01L23/528.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S8	20	(vertical near stack) and ((insulating or dielectric or insulation) near channel)and	US-PGPUB; USPAT;	OR	ON	2017/11/22 10:17

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		(tunnel or tunneling) and (blocking or block) and (trap or trapping)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S9	0	("2017/0243879").URPN.	USPAT	OR	OFF	2017/11/22 10:21
S10	28	("20070029607" | "20090230454" | "20100207194" | "20100213527" | "20110156044" | "20120012921" | "20120326221" | "20140131784" | "20150044833" | "20150076584" | "20150179660" | "20150255481" | "20150371709" | "20160133642" | "5915167" | "7575973" | "7906392" | "8084819" | "8187936" | "8461641" | "8610194" | "8735962" | "8767465" | "8823076" | "8853765" | "8981457" | "8987119" | "9023719").PN. OR ("9728546").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 10:25
S11	328	((insulating or dielectric or insulation) near channel)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 12:35
S12	0	((insulating or dielectric or insulation) near channel near gap)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S13	10	((insulating or dielectric or insulation) near channel near gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S14	346	((insulating or dielectric or insulation) near channel same gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S15	1065	((insulating or dielectric or insulation) same channel same gap)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 18:00
S16	4	("20120001249").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	OFF	2017/11/22 18:05

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			IBM_TDB			
S17	2	("20160181271").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:07
S18	8	(("20130049095") or ("20100181612") or ("20130100741")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:07
S19	51	((insulating or dielectric or insulation) same channel NEAR (SEPARATION OR gap or void))and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 18:52
S20	35	("20050280061" | "20070045708" | "20070158736" | "20070252201" | "20080073635" | "20080175032" | "20080180994" | "20090097321" | "20090184360" | "20100270593" | "20110018051" | "20120068241" | "20120119283" | "20120182806" | "20150243674" | "20150357342" | "20150371998" | "20160056168" | "6906940" | "7315474" | "7420242" | "7612403" | "7696559" | "7851849" | "8008732" | "8363476" | "8467219" | "8503213" | "8648438" | "8759899" | "8853818" | "9147468" | "9224473").PN. OR ("9401371").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 18:53
S21	7	("20160005746" | "20160163733" | "20160240551" | "9379122" | "9379131" | "9401209" | "9401371").PN. OR ("9818760").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 18:56
S22	32	((insulating or dielectric or insulation) same channel NEAR (seam or hollow))and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 19:02

EAST Search History (Interference)

<This search history is empty>

11/24/2017 1:49:36 PM
C:\Users\cenad\Documents\EAST\Workspaces\15410965.wsp

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IPR2024-00912

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15410965	LUE, HANG-TING
	Examiner	Art Unit
	CHRISTINE ENAD	2823

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/24/2017								
	1	✓								
	2	✓								
	3	✓								
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	24	✓								

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To: docket@hmbay.com,,
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Application	Document	Mailroom Date	Attorney Docket No.
15410965	CTNF	11/29/2017	MXIC 2194-1
	892	11/29/2017	MXIC 2194-1
	1449	11/29/2017	MXIC 2194-1

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of inventor(s):
Hang-Ting Lue

Application No. **15/410,965**

Confirmation No. **3219**

Filing Date: **20 January 2017**

Title: **DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE**

Group Art Unit: **2823**

Examiner: **Christine A Enad**

CUSTOMER NO. 46353

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE

Sir:

In response to the Office Action dated 29 November 2017, Applicant requests consideration of the following amendments in the above-referenced application:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 8 of this paper.

///

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In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material between and contacting the first and second channel films; and

data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips, the discrete charge trapping elements disposed in the first recessed regions on the first sidewalls of the conductive strips.

2. (original) The memory device of claim 1, wherein the discrete charge trapping elements disposed in the first recessed regions are dielectric charge trapping elements.

3. (original) The memory device of claim 1, wherein the conductive strips in the stacks have second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions on the second sidewalls of the conductive strips; and

the data storage structures include discrete charge trapping elements disposed in the second recessed regions in contact with the tunneling layers, and blocking layers

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between the discrete charge trapping elements in the second recessed regions and the second sidewalls of the conductive strips.

4. (original) The memory device of claim 3, wherein the discrete charge trapping elements disposed in the second recessed regions are dielectric charge trapping elements.

5. (original) The memory device of claim 1, wherein the dielectric material comprises a gap.

6. (original) The memory device of claim 1, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

7. (currently amended) A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks and having second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material between and contacting the first and second channel films; and

data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips and between the discrete charge trapping elements and the second sidewalls of the conductive strips, the discrete charge trapping elements disposed in the

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first recessed regions on the first sidewalls of the conductive strips and disposed in the second recessed regions on the second sidewalls of the conductive strips,

wherein the vertical channel pillars are arranged so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips.

8. (original) The memory device of claim 7, wherein the discrete charge trapping elements are dielectric charge trapping elements.

9. (original) The memory device of claim 7, wherein the dielectric material comprises a gap.

10. (original) The memory device of claim 7, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

11. (original) A manufacturing method, comprising:

forming a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls;

recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks; and

depositing a dielectric material between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks.

12. (original) The manufacturing method of claim 11, said forming the data storage structures comprising:

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depositing blocking layers over the first sidewalls of the conductive strips in the first recessed regions;

depositing charge trapping material over the blocking layers in the first recessed regions; and

depositing tunneling layers over the charge trapping material in the first recessed regions.

13. (original) The manufacturing method of claim 12, wherein the charge trapping material is dielectric charge trapping material.

14. (original) The manufacturing method of claim 12, comprising:

said depositing the blocking layers including depositing the blocking layers over the first sides of the insulating strips; and

said depositing the charge trapping material including depositing the charge trapping material over the blocking layers over the first sides of the insulating strips; and separating the charge trapping material between adjacent first recessed regions.

15. (original) The manufacturing method of claim 14, said separating the charge trapping material including removing the charge trapping material over the blocking layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions.

16. (original) The manufacturing method of claim 11, comprising:

etching to isolate the data storage structures along the conductive strips, to form discrete charge trapping elements in contact with the tunneling layers and the blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips.

17. (original) The manufacturing method of claim 11, wherein the conductive strips in the stacks of conductive strips have second sidewalls opposite the first sidewalls, the manufacturing method comprising:

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recessing the second sidewalls of the conductive strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks; and

forming the data storage structures in the second recessed regions.

18. (original) The manufacturing method of claim 17,

etching to isolate the first and second channel films and the dielectric material between the first and second channel films along the conductive strips, to form vertical channel pillars between the stacks, so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips.

19. (original) The manufacturing method of claim 11, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

20. (original) A manufacturing method, comprising:

forming a plurality of stacks of sacrificial strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the sacrificial strips in the stacks having first sidewalls;

recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks;

depositing a dielectric material between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks; and

replacing the sacrificial strips in the stacks with a metal material.

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21. (original) The manufacturing method of claim 20, said forming the data storage structures comprising:

depositing blocking layers over the first sidewalls of the sacrificial strips in the first recessed regions;

depositing charge trapping material over the blocking layers in the first recessed regions; and

depositing tunneling layers over the charge trapping material in the first recessed regions.

22. (original) The manufacturing method of claim 21, wherein the charge trapping material is dielectric charge trapping material.

23. (original) The manufacturing method of claim 20, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

24. (original) The manufacturing method of claim 20, said replacing comprising:

etching the stacks to form a trench, exposing the sacrificial strips in the trench;

removing the sacrificial strips in the trench;

depositing the metal material in the trench; and

separating the metal material between the insulating strips in the trench.

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REMARKS

The present application is being examined under the first inventor to file provisions of the AIA.

The Examiner reviewed claims 1-24. Claims 1-4, 6, 11-17, 20-22 and 24 are rejected under 35 U.S.C. 102(a)(1). Claims 5, 7-10, 18-19 and 23 are rejected under 35 U.S.C.103.

Applicant has amended claims 1 and 7.

Claims 1-24 are pending.

Claim Amendments

Applicant has amended claim 1 to recite "the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars". Support for the amendment can be found in at least the original claim 1 which includes "the vertical channel pillars having first and second channel films" on lines 6-7, and Figure 9 which illustrates tunneling layers (e.g. 810) in contact with the first and second channel films (e.g. 910, 920) in the vertical channel pillars. Applicant has made corresponding amendment in claim 7. No new matter is added.

Rejection of Claims 1-4, 6, 11-17, 20-22 and 24 under 35 U.S.C. 102(a)(1)

Claims 1-4, 6, 11-17, 20-22, 24 are rejected under 35 U.S.C. 102(a) (1) as being anticipated by Serov et al (US Publication No 2016/0071861).

Claim 1

Claim 1 includes the limitations

"vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material between and contacting the first and second channel films; and

data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars, ..."

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Emphasis added.

Serov does not anticipate at least the quoted limitations, as explained below.

Serov describes a three dimensional NAND device that includes a first semiconductor channel (e.g. 601, FIGs. 9A, 9B, 9C), a second semiconductor channel (e.g. 602, FIGs. 9A, 9B, 9C), and a dielectric core (e.g. 62, FIGs. 9A, 9B, 9C).

The Office Action asserts:

> "Regarding claim 1, Serov discloses a memory device, comprising: … vertical channel pillars **Fig 9A-10, 601/602/62** disposed between the stacks, the vertical channel pillars having first **Fig 9A-10, 601** and second channel films **Fig 9A-10, 602** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 9A-10, 62** (Paragraph 0150) between and contacting the first and second channel films; and data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips **Fig 9A-10, (42/46)** in the stacks, the data storage structures including tunneling layers **Fig 9A-10, 56** in contact with the vertical channel pillars,"

Pages 2-3, emphasis added.

FIG. 9C of Serov is reproduced below for convenience.

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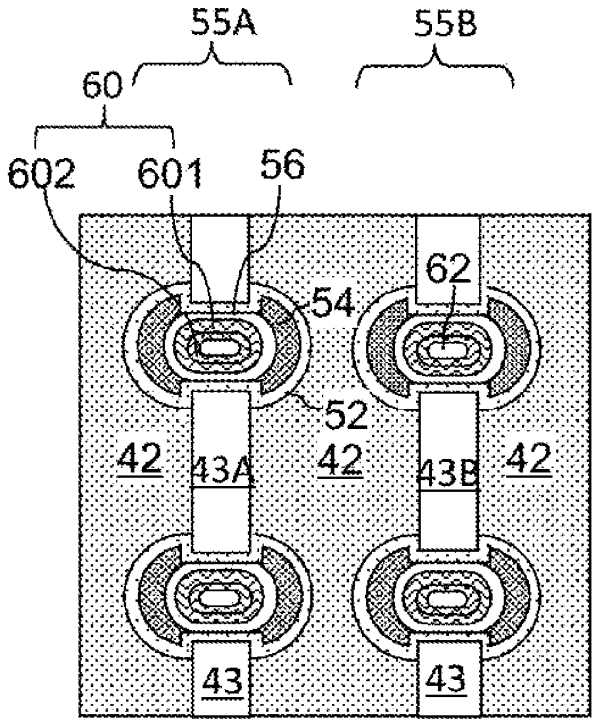


FIG. 9C

As shown in 9C of Serov, a dielectric core 62 is surrounded by a second semiconductor channel portion 602, which is surrounded by a first semiconductor channel portion 601. As such, the dielectric core 62 is NOT between the first semiconductor channel portion 601 and the second semiconductor channel portion 602, and NOT contacting the first semiconductor channel portion 601. In contrast, claim 1 requires "a dielectric material between and contacting the first and second channel films".

Furthermore, as shown in 9C of Serov, although a tunneling dielectric 56 surrounds the first semiconductor channel portion 601, the tunneling dielectric 56 is NOT in contact with the second semiconductor channel portion 602. In contrast, claim 1 requires "tunneling layers in contact with the first and second channel films in the vertical channel pillars".

Accordingly Serov does not anticipate at least the quoted limitations in claim 1.

Claim 11

Claim 11 includes the limitations

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"depositing a dielectric material between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks."

Emphasis added.

Serov does not anticipate at least the quoted limitations, as explained below.

The Office Action asserts:

"Regarding claim 11, Serov discloses a manufacturing method, comprising: … and depositing a dielectric material **Fig 9A-10, 62** between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks **Fig 9A-10.**"

Page 4; emphasis added.

As shown in 9C of Serov, a dielectric core 62 is surrounded by a second semiconductor channel portion 602, which is surrounded by a first semiconductor channel portion 601. As such, the dielectric core 62 is NOT between the first semiconductor channel portion 601 and the second semiconductor channel portion 602, and NOT contacting the first semiconductor channel portion 601. In contrast, claim 11 requires "depositing a dielectric material between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks".

Accordingly Serov does not anticipate at least the quoted limitations in claim 11.

Claim 20

Claim 20 includes the limitations

"depositing a dielectric material between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks;"

Emphasis added.

Serov does not anticipate at least the quoted limitations, as explained below.

The Office Action asserts:

"Regarding claim 20, Serov discloses a manufacturing method, comprising: … and depositing a dielectric material **Fig 9A-10, 62** between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks **Fig 9A-10, …**"

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Page 6; emphasis added.

As shown in 9C of Serov, a dielectric core 62 is surrounded by a second semiconductor channel portion 602, which is surrounded by a first semiconductor channel portion 601. As such, the dielectric core 62 is NOT between the first semiconductor channel portion 601 and the second semiconductor channel portion 602, and NOT contacting the first semiconductor channel portion 601. In contrast, claim 11 requires "depositing a dielectric material between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks".

Accordingly Serov does not anticipate at least the quoted limitations in claim 20.

Claim 1 as amended should be allowable for at least the reasons explained above.

Claims 2-4 and 6 depend from claim 1, and should be allowable for at least the same reasons as explained for claim 1, and because of the unique combinations recited.

Claim 11 as amended should be allowable for at least the reasons explained above.

Claims 12-17 depend from claim 11, and should be allowable for at least the same reasons as explained for claim 11, and because of the unique combinations recited.

Claim 20 as amended should be allowable for at least the reasons explained above.

Claims 21-22 and 24 depend from claim 20, and should be allowable for at least the same reasons as explained for claim 20, and because of the unique combinations recited.

Accordingly reconsideration of the rejection of claims 1-4, 6, 11-17, 20-22 and 24 as amended under 35 U.S.C. § 102(a) (1) is respectfully requested.

Rejection of Claims 5, 7-10, 18-19 and 23 under 35 U.S.C. 103

Claims 5, 7-10, 18-19, 23 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861) in view of Liu et al (US Publication No. 2016/0204117).

Claim 7

Claim 7 includes the limitations

"vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material between and contacting the first and second channel films; and

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data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars, ..."

Emphasis added.

The quoted limitations in claim 7 before the amendment are rejected (Page 8, the Office Action) by the same arguments as for corresponding limitations in claim 1 before the amendment (Pages 2-3, the Office Action).

Claim 7 as amended should be allowable for at least the same reasons as explained for claim 1 as amended.

Claims 8-10 depend from claim 7, and should be allowable for at least the same reasons as explained for claim 7, and because of the unique combinations recited.

Claim 5 depends from claim 1, and should be allowable for at least the same reasons as explained for claim 1, and because of the unique combinations recited.

Claims 18-19 depend from claim 11, and should be allowable for at least the same reasons as explained for claim 11, and because of the unique combinations recited.

Claim 23 depends from claim 20, and should be allowable for at least the same reasons as explained for claim 20, and because of the unique combinations recited.

Accordingly reconsideration of the rejection of claims 5, 7-10, 18-19, 23 as amended under 35 U.S.C. § 103 is respectfully requested.

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CONCLUSION

It is respectfully submitted that this application is now in condition for allowance.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 2194-1).

Respectfully submitted,

Dated: 08 January 2018

/Yiding Wu/

Yiding Wu, Reg. No. 65,992

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Electronic Acknowledgement Receipt

EFS ID:	31439393
Application Number:	15410965
International Application Number:	
Confirmation Number:	3219
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	HANG-TING LUE
Customer Number:	46353
Filer:	Yiding Wu/Amy Jonsson
Filer Authorized By:	Yiding Wu
Attorney Docket Number:	MXIC 2194-1
Receipt Date:	08-JAN-2018
Filing Date:	20-JAN-2017
Time Stamp:	17:53:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	00629000.PDF	186499 10eb079b5116edf9f0acfe141cb1a27db8da4e13	no	14

Warnings:

Information:	
Total Files Size (in bytes):	186499

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/410,965	Filing Date 01/20/2017	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	01/08/2018	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 24	Minus	** 24	= 0		x $80 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 4	= 0		x $420 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/Dorian Evans/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/410,965	01/20/2017	HANG-TING LUE	MXIC 2194-1	3219

46353 7590 05/25/2018

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019

EXAMINER	
ENAD, CHRISTINE A	

ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
05/25/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hmbay.com

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IPR2024-00912

Office Action Summary	Application No. 15/410,965	Applicant(s) LUE, HANG-TING	
	Examiner CHRISTINE ENAD	Art Unit 2823	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/8/2018*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-24* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-24* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

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DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Response to Arguments

Applicant's arguments, see Page 8-13, filed 1/8/2018 with respect to the rejection(s) of claims 1, 7, 11, 20 under USC 102 and USC 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Serov et al (US Publication No 2016/0071861) pertaining to Embodiment 1 (Fig 9B) and Embodiment 2 (Fig 16B).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6, 11-17, 20-22, 24 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861).

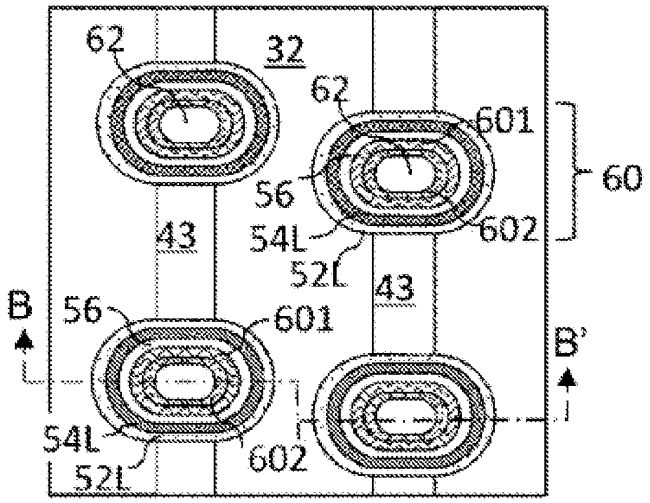


FIG. 16A

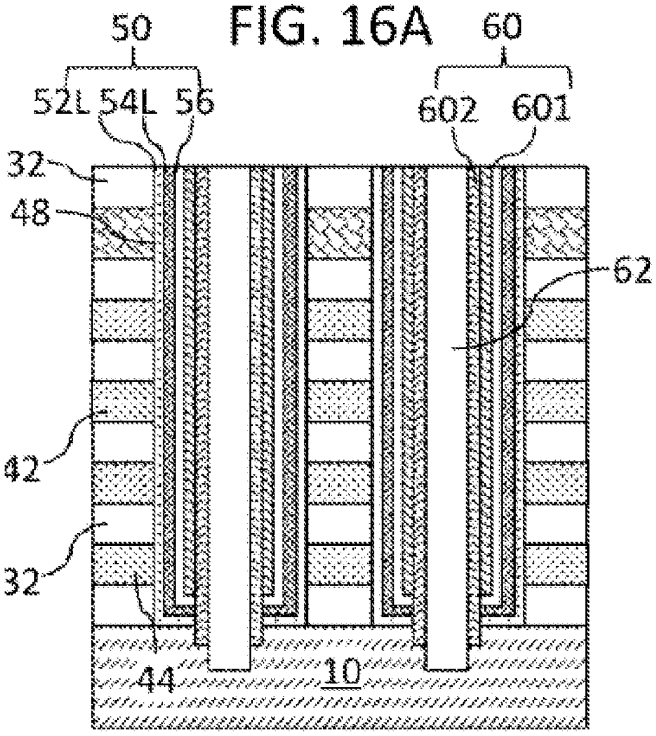


FIG. 16B

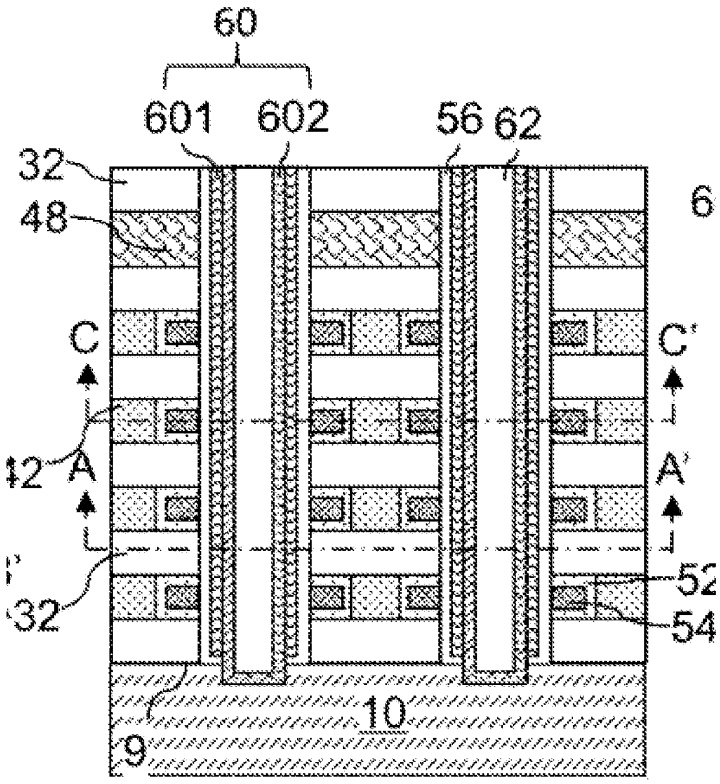


FIG. 9B

Regarding claim 1, Serov discloses a memory device, comprising: a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips alternating with insulating strips **Fig 9A-10, 32**, the insulating strips in the stacks having first and second sides, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in

sides of the stacks **Fig 9A-10**; vertical channel pillars **Fig 9A-10, 601/602/62** disposed between the stacks, the vertical channel pillars having first **Fig 9A-10, 601** and second channel films **Fig 9A-10, 602** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 9A-10, 62** (Paragraph 0150) between and contacting the second channel film; and data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips **Fig 9A-10, (42/46)** in the stacks, the data storage structures including tunneling layers **Fig 9A-10, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56**, and blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips, the discrete charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions on the first sidewalls of the conductive strips **Fig 9A-10**. **Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B, 62** between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig 16B, 602 (right side of layer 62)** ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 16B, 54** in contact

with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement.

Regarding claim 2, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions are dielectric charge trapping elements (Paragraph 0143).

Regarding claim 3, Serov discloses the conductive strips in the stacks have second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions on the second sidewalls of the conductive strips; and the data storage structures include discrete charge trapping elements disposed in the second recessed regions in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements in the second recessed regions and the second sidewalls of the conductive strips **Fig 9A-10.**

Regarding claim 4, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** disposed in the second recessed regions are dielectric charge trapping elements (Paragraph 0043).

Regarding claim 6, Serov discloses the conductive strips in the plurality of stacks of conductive strips include a metal material (Paragraph 0133).

Regarding claim 11, Serov discloses a manufacturing method, comprising: forming a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips **Fig 9A-10, (42/46)** alternating with insulating strips **Fig 9A-10, 32**, the insulating strips **Fig 9A-10,**

32in the stacks having first and second sides **Fig 9A-10**, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls; recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks **Fig 5A-5C;** forming data storage structures in the first recessed regions **Fig 6A-8C;** forming first and second channel films **Fig 9A-10, 60** on the data storage structures on sidewalls of adjacent stacks; and depositing a dielectric material **Fig 9A-10, 62** between the first and second channel films, the dielectric material contacting the second channel films on the sidewalls of the adjacent stacks **Fig 9A-10**. **Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B, 62** between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig 16B, 602 (right side of layer 62)** ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 16B, 54** in contact with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement.

Regarding claim 12, Serov discloses said forming the data storage structures comprising: depositing blocking layers **Fig 9A-10, 52** over the first sidewalls of the conductive strips in the first recessed regions; depositing charge trapping material **Fig 9A-10, 54** over the blocking layers **Fig 9A-10, 52** in the first recessed regions; and depositing tunneling layers **Fig 9A-10, 56** over the charge trapping material **Fig 9A-10, 54** in the first recessed regions.

Regarding claim 13, Serov discloses wherein the charge trapping material is dielectric charge trapping material (Paragraph 0143).

Regarding claim 14, Serov discloses comprising: said depositing the blocking layers **Fig 9A-10, 52** including depositing the blocking layers **Fig 9A-10, 52** over the first sides of the insulating strips **Fig 6B**; and said depositing the charge trapping material **Fig 9A-10, 54** including depositing the charge trapping material **Fig 9A-10, 52** over the blocking layers **Fig 6B** over the first sides of the insulating strips **Fig 6B**; and separating the charge trapping material between adjacent first recessed regions **Fig 6A-6C.**

Regarding claim 15, Serov discloses said separating the charge trapping material **Fig 9A-10, 54** including removing the charge trapping material over the blocking layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions **Fig 6A-8C.**

Regarding claim 16, Serov discloses comprising: etching to isolate the data storage structures along the conductive strips, to form discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56** and the

blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips.

Regarding claim 17, Serov discloses wherein the conductive strips in the stacks of conductive strips have second sidewalls opposite the first sidewalls **Fig 9A-10**, the manufacturing method comprising: recessing the second sidewalls of the conductive strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks; and forming the data storage structures in the second recessed regions **Fig 5A-10.**

Regarding claim 20, Serov discloses a manufacturing method, comprising: forming a plurality of stacks **Fig 9A-10, 32/(42/46)** of sacrificial strips **Fig 9A-10, 42** alternating with insulating strips **Fig 9A-10, 32**, the insulating strips **Fig 9A-10, 32**in the stacks having first and second sides **Fig 9A-10**, and the sacrificial strips **Fig 9A-10, 42** in the stacks having first sidewalls; recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks **Fig 5A-5C;** forming data storage structures in the first recessed regions **Fig 6A-8C;** forming first and second channel films **Fig 9A-10, 60** on the data storage structures on sidewalls of adjacent stacks; and depositing a dielectric material **Fig 9A-10, 62** between the first and second channel films, the dielectric material contacting the second channel films on the sidewalls of the adjacent stacks **Fig 9A-10**, and replacing the sacrificial strips in the stacks with a metal material **Fig 10, 46. Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel

arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B, 62** between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig 16B, 602 (right side of layer 62)** ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 16B, 54** in contact with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement.

Regarding claim 21, Serov discloses said forming the data storage structures comprising: depositing blocking layers **Fig 9A-10, 52** over the first sidewalls of the conductive strips in the first recessed regions; depositing charge trapping material **Fig 9A-10, 54** over the blocking layers **Fig 9A-10, 52** in the first recessed regions; and depositing tunneling layers **Fig 9A-10, 56** over the charge trapping material **Fig 9A-10, 54** in the first recessed regions.

Regarding claim 22, Serov discloses wherein the charge trapping material is dielectric charge trapping material (Paragraph 0143).

Regarding claim 24, Serov discloses said replacing comprising: etching the stacks to form a trench, exposing the sacrificial strips in the trench; removing the sacrificial strips in the trench; depositing the metal material in the trench; and separating the metal material between the insulating strips in the trench (Paragraph 0152-0154).

Claims 5, 7-10, 18-19, 23 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861) in view of Liu et al (US Publication No. 2016/0204117).

Regarding claims, 5, 19, and 23, Serov discloses all the limitations except for the gap in the channel region. Whereas Liu discloses leaving a gap between the first and second vertical channel films **Fig 2A-4B** (Paragraph 0075-0076). Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the device of Serov and incorporate a gap to provide a connector between device levels.

Regarding claim 7, Serov discloses a memory device, comprising: a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips alternating with insulating strips **Fig 9A-10, 32**, the insulating strips in the stacks having first and second sides, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks **Fig 9A-10;** and having second sidewall opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions in sides of the stacks **Fig 9A-10;** vertical channel pillars **Fig 9A-10, 601/602/62** disposed between the stacks, the vertical channel pillars having first **Fig 9A-**

10, 601 and second channel films **Fig 9A-10, 602** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 9A-10, 62** (Paragraph 0150) between and contacting the second channel films; and data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips **Fig 9A-10, (42/46)** in the stacks, the data storage structures including tunneling layers **Fig 9A-10, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56**, and blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips and between the discrete charge trapping elements and the second sidewalls of the conductive strips **Fig 9A-10**, the discrete charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions on the first sidewalls of the conductive strips and disposed in the second recessed regions on the second sidewalls of the conductive strips **Fig 9A-10.** Serov discloses all the limitations except for the offset in the channel region.

Whereas Liu discloses the vertical channel pillars are arranged so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips **Fig 2A-4B** (Paragraph 0075-0076). Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the device of Serov and incorporate an offset to provide a connector between device

levels. **Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers.

Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B, 62** between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig 16B, 602 (right side of layer 62)** ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 16B, 54** in contact with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement.

Regarding claim 8, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** are dielectric charge trapping elements (Paragraph 0143).

Regarding claim 9, Serov discloses wherein the dielectric material comprises a gap **Fig 2A-4B** (Paragraph 0075-0076).

Regarding claim 10, Serov discloses the conductive strips in the plurality of stacks of conductive strips include a metal material (Paragraph 0133).

Regarding claim 18, Liu discloses etching to isolate the first and second channel films and the dielectric material between the first and second channel films along the conductive strips, to form vertical channel pillars between the stacks, so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips **Fig 2A-4B** (Paragraph 0075-0076).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTINE ENAD whose telephone number is (571)270-7891. The examiner can normally be reached on Monday - Thursday, 7:30 am - 6:00 pm, EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on (571) 272 9820. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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/CHRISTINE ENAD/
Primary Examiner, Art Unit 2823

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15410965	LUE, HANG-TING
	Examiner	Art Unit
	CHRISTINE ENAD	2823

CPC- SEARCHED		
Symbol	Date	Examiner
H01L27/11582	11/24/2017	CE
H01L21/76802, 21/76877	11/24/2017	CE
H01L23/5226, 23/528	11/24/2017	CE

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

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SEARCH NOTES		
Search Notes	Date	Examiner
Assignee and inventor search conducted	11/24/2017	CE
CPC search	11/24/2017	CE
EAST Search	11/24/2017	CE
EAST Search	5/21/2018	CE

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/05/21 19:06
S1	574	(("MACRONIX") near3 ("INTERNATIONAL") near3 ("CO") near3 ("LTD")).AANM.	USPAT	OR	OFF	2017/11/22 09:51
S2	358	(("LUE") near3 ("HANG-TING")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 09:51
S3	9877	(H01L27/11582.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:51
S4	13188	(H01L21/76802.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:51
S5	17402	(H01L21/76877.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S6	15471	(H01L23/5226.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S7	13459	(H01L23/528.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S8	20	(vertical near stack) and ((insulating or dielectric or insulation) near channel)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/11/22 10:17

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			IBM_TDB			
S9	0	("2017/0243879").URPN.	USPAT	OR	OFF	2017/11/22 10:21
S10	28	("20070029607" | "20090230454" | "20100207194" | "20100213527" | "20110156044" | "20120012921" | "20120326221" | "20140131784" | "20150044833" | "20150076584" | "20150179660" | "20150255481" | "20150371709" | "20160133642" | "5915167" | "7575973" | "7906392" | "8084819" | "8187936" | "8461641" | "8610194" | "8735962" | "8767465" | "8823076" | "8853765" | "8981457" | "8987119" | "9023719").PN. OR ("9728546").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 10:25
S11	328	((insulating or dielectric or insulation) near channel)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 12:35
S12	0	((insulating or dielectric or insulation) near channel near gap)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S13	10	((insulating or dielectric or insulation) near channel near gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S14	346	((insulating or dielectric or insulation) near channel same gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S15	1065	((insulating or dielectric or insulation) same channel same gap)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 18:00
S16	4	("20120001249").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:05
S17	2	("20160181271").PN.	US-PGPUB; USPAT; USOCR;	OR	OFF	2017/11/22 18:07

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			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S18	8	(("20130049095") or ("20100181612") or ("20130100741")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:07
S19	51	((insulating or dielectric or insulation) same channel NEAR (SEPARATION OR gap or void))and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 18:52
S20	35	("20050280061" | "20070045708" | "20070158736" | "20070252201" | "20080073635" | "20080175032" | "20080180994" | "20090097321" | "20090184360" | "20100270593" | "20110018051" | "20120068241" | "20120119283" | "20120182806" | "20150243674" | "20150357342" | "20150371998" | "20160056168" | "6906940" | "7315474" | "7420242" | "7612403" | "7696559" | "7851849" | "8008732" | "8363476" | "8467219" | "8503213" | "8648438" | "8759899" | "8853818" | "9147468" | "9224473").PN. OR ("9401371").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 18:53
S21	7	("20160005746" | "20160163733" | "20160240551" | "9379122" | "9379131" | "9401209" | "9401371").PN. OR ("9818760").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 18:56
S22	32	((insulating or dielectric or insulation) same channel NEAR (seam or hollow))and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 19:02
S23	2	("20160204117").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/24 13:25
S24	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/05/14 11:31
S25	39484	((insulating or dielectric or insulation) same channel)and (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/05/14 12:11

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S26	19502	((insulating or dielectric or insulation) same channel) same (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/05/14 12:11
S27	305	((insulating or dielectric or insulation) same channel) near (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/05/14 12:13

5/21/2018 7:42:08 PM
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15410965	LUE, HANG-TING
	Examiner	Art Unit
	CHRISTINE ENAD	2823

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/24/2017	05/21/2018							
	1	✓	✓							
	2	✓	✓							
	3	✓	✓							
	4	✓	✓							
	5	✓	✓							
	6	✓	✓							
	7	✓	✓							
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	9	✓	✓							
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	23	✓	✓							
	24	✓	✓							

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15/410,965	01/20/2017	HANG-TING LUE	MXIC 2194-1

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Title:DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE

Publication No.US-2018-0211969-A1
Publication Date:07/26/2018

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Application	Document	Mailroom Date	Attorney Docket No.
15410965	NTC.PUB	07/26/2018	MXIC 2194-1

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EFS ID:	33532233
Application Number:	15410965
International Application Number:	
Confirmation Number:	3219
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	HANG-TING LUE
Customer Number:	46353
Filer:	Yiding Wu/Amy Jonsson
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	00660175.PDF	258790 73e7d4b8d55da892159c3904eb05a94929 16fec9	no	17

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/Amy Jonsson/
Amy Jonsson

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of inventor(s):
Hang-Ting Lue

Application No. **15/410,965**

Confirmation No. **3219**

Filing Date: **20 January 2017**

Title: **DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE**

Group Art Unit: **2823**

Examiner: **Christine A Enad**

CUSTOMER NO. 46353

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE

Sir:

In response to the Office Action dated 25 May 2018, Applicant requests consideration of the following amendments in the above-referenced application:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

An **Interview Summary** begins on page 9.

Remarks begin on page 10 of this paper.

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In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material between and contacting the first and second channel films; and

data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips and between the tunneling layers and the first sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks, the discrete charge trapping elements disposed in the first recessed regions on the first sidewalls of the conductive strips.

2. (original) The memory device of claim 1, wherein the discrete charge trapping elements disposed in the first recessed regions are dielectric charge trapping elements.

3. (original) The memory device of claim 1, wherein the conductive strips in the stacks have second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions on the second sidewalls of the conductive strips; and

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the data storage structures include discrete charge trapping elements disposed in the second recessed regions in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements in the second recessed regions and the second sidewalls of the conductive strips.

4. (original) The memory device of claim 3, wherein the discrete charge trapping elements disposed in the second recessed regions are dielectric charge trapping elements.

5. (original) The memory device of claim 1, wherein the dielectric material comprises a gap.

6. (original) The memory device of claim 1, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

7. (currently amended) A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks and having second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material between and contacting the first and second channel films; and

data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips, [[and]] between the discrete charge trapping elements and the

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second sidewalls of the conductive strips, between the tunneling layers and the first sides of the insulating strips, and between the tunneling layers and the second sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks, the blocking layers continuous across and in contact with the second sides of the insulating strips vertically between adjacent conductive strips in the stacks, the discrete charge trapping elements disposed in the first recessed regions on the first sidewalls of the conductive strips and disposed in the second recessed regions on the second sidewalls of the conductive strips,

wherein the vertical channel pillars are arranged so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips.

8. (original) The memory device of claim 7, wherein the discrete charge trapping elements are dielectric charge trapping elements.

9. (original) The memory device of claim 7, wherein the dielectric material comprises a gap.

10. (original) The memory device of claim 7, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

11. (currently amended) A manufacturing method, comprising:

forming a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls;

recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions, including forming blocking layers between tunneling layers and the first sides of the insulating strips in the

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stacks, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks; and

depositing a dielectric material between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks.

12. (currently amended) The manufacturing method of claim 11, said forming the data storage structures comprising:

depositing the blocking layers over the first sidewalls of the conductive strips in the first recessed regions and over the first sides of the insulating strips in the stacks;

depositing charge trapping material over the blocking layers in the first recessed regions; and

depositing the tunneling layers over the charge trapping material in the first recessed regions and over the blocking layers over the first sides of the insulating strips in the stacks.

13. (original) The manufacturing method of claim 12, wherein the charge trapping material is dielectric charge trapping material.

14. (original) The manufacturing method of claim 12, comprising:

said depositing the blocking layers including depositing the blocking layers over the first sides of the insulating strips; and

said depositing the charge trapping material including depositing the charge trapping material over the blocking layers over the first sides of the insulating strips; and separating the charge trapping material between adjacent first recessed regions.

15. (original) The manufacturing method of claim 14, said separating the charge trapping material including removing the charge trapping material over the blocking

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layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions.

16. (original) The manufacturing method of claim 11, comprising:

etching to isolate the data storage structures along the conductive strips, to form discrete charge trapping elements in contact with the tunneling layers and the blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips.

17. (original) The manufacturing method of claim 11, wherein the conductive strips in the stacks of conductive strips have second sidewalls opposite the first sidewalls, the manufacturing method comprising:

recessing the second sidewalls of the conductive strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks; and

forming the data storage structures in the second recessed regions.

18. (original) The manufacturing method of claim 17,

etching to isolate the first and second channel films and the dielectric material between the first and second channel films along the conductive strips, to form vertical channel pillars between the stacks, so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips.

19. (original) The manufacturing method of claim 11, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

20. (currently amended) A manufacturing method, comprising:

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forming a plurality of stacks of sacrificial strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the sacrificial strips in the stacks having first sidewalls;

recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions, including forming blocking layers between tunneling layers and the first sides of the insulating strips in the stacks, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks;

depositing a dielectric material between the first and second channel films, the dielectric material contacting the first and second channel films on the sidewalls of the adjacent stacks; and

replacing the sacrificial strips in the stacks with a metal material.

21. (currently amended) The manufacturing method of claim 20, said forming the data storage structures comprising:

depositing the blocking layers over the first sidewalls of the sacrificial strips in the first recessed regions and over the first sides of the insulating strips in the stacks;

depositing charge trapping material over the blocking layers in the first recessed regions; and

depositing the tunneling layers over the charge trapping material in the first recessed regions and over the blocking layers over the first sides of the insulating strips in the stacks.

22. (original) The manufacturing method of claim 21, wherein the charge trapping material is dielectric charge trapping material.

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23. (original) The manufacturing method of claim 20, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

24. (original) The manufacturing method of claim 20, said replacing comprising:
etching the stacks to form a trench, exposing the sacrificial strips in the trench;
removing the sacrificial strips in the trench;
depositing the metal material in the trench; and
separating the metal material between the insulating strips in the trench.

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INTERVIEW SUMMARY

Applicants express their appreciation to Examiner Christine A. Enad for the courtesy of a telephonic interview on August 23, 2018.

In advance of the interview, the undersigned submitted an interview agenda (via email Christine.enad@uspto.gov) on Monday, August 13, 2018.

The agenda proposed to discuss a proposed amendment in claim 1 including "blocking layers (410, FIG. 9) ... between the tunneling layers (810) and the first sides of the insulating strips (226);", and to discuss a proposed alternative amendment in claim 1 including "... a dielectric material (930, FIGs. 9 & 10) physically separating the first and second channel films (910, 920) at levels (A-A', FIG. 9) of data storage structures (510)".

At the interview, the Examiner suggested further clarifying the proposed amendment in claim 1 with limitations like the blocking layers in contact with the insulation strips in a vertical direction. The Examiner indicated that the proposed amendment with the suggested clarification would have a better chance of overcoming the references of record than the proposed alternative amendment.

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REMARKS

The present application is being examined under the first inventor to file provisions of the AIA.

The Examiner reviewed claims 1-24. Claims 1-24 are rejected.

Applicant has amended claims 1, 7, 11, 12, 20 and 21.

Claims 1-24 remain pending.

Each rejection is respectfully traversed below.

Claim Amendments

Applicant has amended claim 1 to recite "blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips and between the tunneling layers and the first sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks".

Applicant has amended claim 7 to recite "blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips, between the discrete charge trapping elements and the second sidewalls of the conductive strips, between the tunneling layers and the first sides of the insulating strips, and between the tunneling layers and the second sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks, the blocking layers continuous across and in contact with the second sides of the insulating strips vertically between adjacent conductive strips in the stacks".

Support for the amendments in claims 1 and 7 can be found in at least Figures 2 and 9 of the present specification, which illustrate blocking layers 410 (FIG. 9) between the tunneling layers 810 (FIG. 9) and the first sides 218a (FIG. 2) of the insulating strips (*e.g.* 218), and between the tunneling layers 810 and the second sides 218b (FIG. 2) of the insulating strips (*e.g.* 218). As shown in Figure 9, the blocking layers 410 are continuous across and in contact with the first sides of the insulating strips (e.g. 226) vertically between adjacent conductive strips (e.g. 225, 227) in the stacks. No new matter is added.

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For convenience, Figure 9 of the present specification is reproduced below, annotated with "blocking layers 410 continuous across and in contact with the first sides of the insulating strips 226 vertically between adjacent conductive strips (225, 227)".

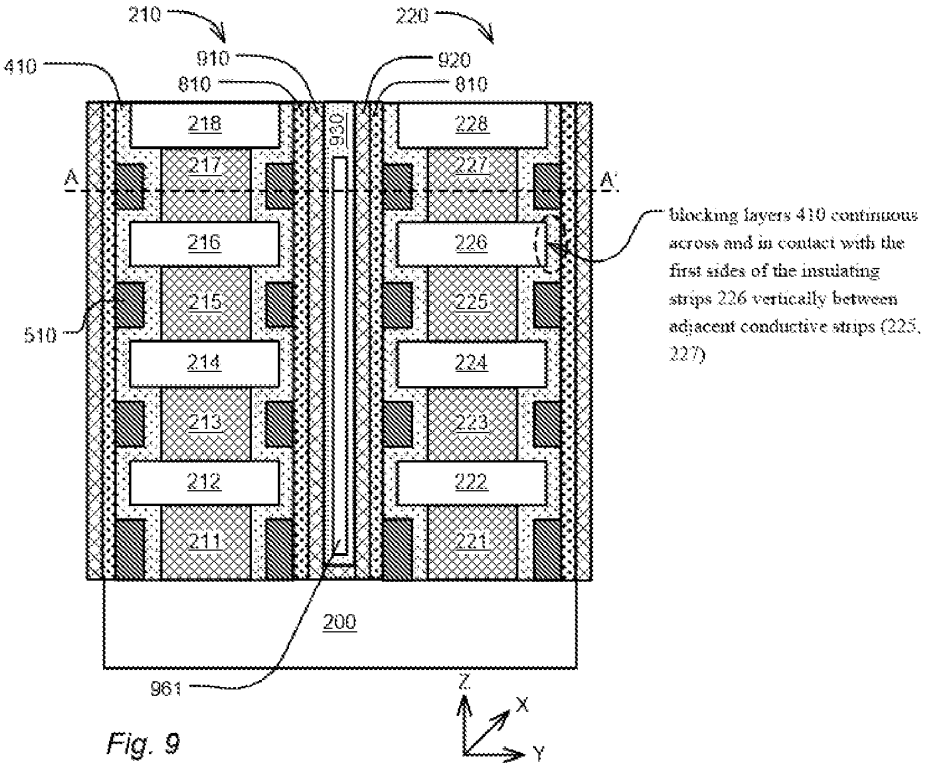


Fig. 9

Applicant has amended claim 11 to recite "forming data storage structures in the first recessed regions, including forming blocking layers between tunneling layers and the first sides of the insulating strips in the stacks, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips".

Applicant has amended claim 12 to recite

"depositing the blocking layers over the first sidewalls of the conductive strips in the first recessed regions and over the first sides of the insulating strips in the stacks;

...

depositing the tunneling layers over the charge trapping material in the first recessed regions and over the blocking layers over the first sides of the insulating strips in the stacks."

Support for the amendments in claims 11 and 12 can be found in at least Figures 4 and 5 of the present specification. Figure 4 describes "The blocking layers (e.g. 410) can be deposited

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over the first sides (e.g. 218a, Fig. 2) and/or the second sides (e.g. 218b, Fig. 2) of the insulating strips (e.g. 218, Fig. 2)." See paragraph [0039]. Figure 5 describes "The charge trapping material can be deposited over the blocking layers over the first sides (e.g. 218a) and/or the second sides (e.g. 218b) of the insulating strips (e.g. 218)." See paragraph [0041]. No new matter is added.

Applicant has made amendments in claims 20 and 21 corresponding to the amendments made in claims 11 and 12.

Rejection of Claims 1-4, 6, 11-17, 20-22 and 24 under 35 U.S.C. 103

Claims 1-4, 6, 11-17, 20-22 and 24 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861).

Claim 1

Claim 1 as amended includes the limitations

> "blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips and between the tunneling layers and the first sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks,"

Emphasis added.

Serov does not describe at least the quoted limitations, as explained below.

The Office Action asserts:

> "Regarding claim 1, Serov discloses a memory device, comprising: a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips alternating with insulating strips **Fig 9A-10,** 32, … the data storage structures including tunneling layers **Fig 9A-10, 56 …** blocking layers **Fig 9A-10,** 52 between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips,"

Pages 4-5, the Office Action; emphasis added.

However, as shown in FIG. 9B for the first exemplary device structure in Serov, the blocking dielectric layer 52 is NOT continuous across and in contact with the sides of the insulating layers 32 vertically between adjacent sacrificial material layers 42.

In contrast, claim 1 requires "blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips and between the tunneling layers and the first sides of the insulating strips, the blocking layers continuous across and in contact with

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the first sides of the insulating strips vertically between adjacent conductive strips in the stacks".

For convenience, FIG. 9B in Serov is reproduced below.

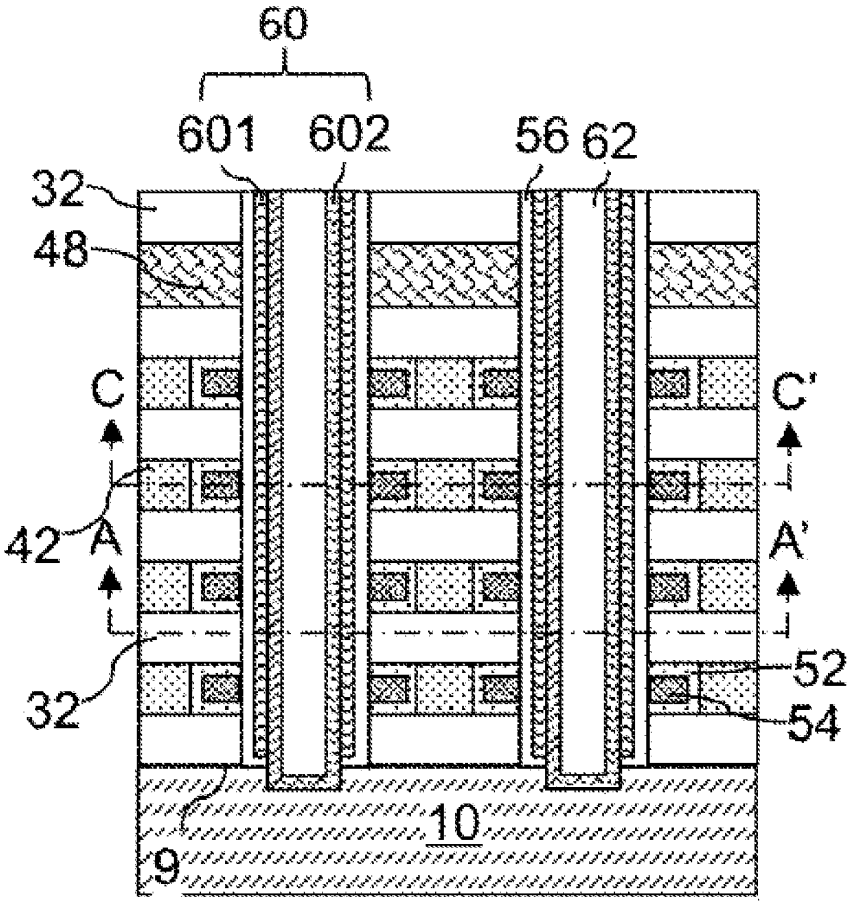


FIG. 9B

Claim 1 should be allowable for at least the reasons explained above.

Claim 11

Claim 11 as amended includes the limitations

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"forming data storage structures in the first recessed regions, including forming blocking layers between tunneling layers and the first sides of the insulating strips in the stacks, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips;"

Emphasis added.

Claim 11 is rejected with the same arguments as for the rejection of claim 1 (Page 5, the Office Action), and should be allowable for at least the same reasons as explained for claim 1.

Claim 12

Claim 12 as amended includes the limitations

"depositing the blocking layers over the first sidewalls of the conductive strips in the first recessed regions and over the first sides of the insulating strips in the stacks;

...

depositing the tunneling layers over the charge trapping material in the first recessed regions and over the blocking layers over the first sides of the insulating strips in the stacks."

Emphasis added.

The Office Action asserts

"Regarding claim 12, Serov discloses said forming the data storage structures comprising: depositing blocking layers **Fig 9A-10, 52** over the first sidewalls of the conductive strips in the first recessed regions; depositing charge trapping material **Fig 9A-10, 54** over the blocking layers **Fig 9A-10, 52** in the first recessed regions; and depositing tunneling layers **Fig 9A-10, 56** over the charge trapping material **Fig 9A-10, 54** in the first recessed regions."

Page 8, the Office Action; emphasis added.

However, Serov does not disclose depositing the tunnel dielectric 56 over the blocking dielectric layer 52 over sides of insulating layers 32, as shown in FIGs. 9A-10. This is because, at a processing step shown in FIGs. 7A-7C, the blocking dielectric layer 52 is removed outside of the lateral recess regions (paragraph [0144], Serov), before the processing step shown in FIGs. 9A-10.

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In contrast, claim 12 requires "depositing the tunneling layers ... over the blocking layers over the first sides of the insulating strips in the stacks."

Accordingly claim 12 as amended should be distinguishable over Serov.

Claim 20

Claim 20 as amended includes the limitations

"forming data storage structures in the first recessed regions, including forming blocking layers between tunneling layers and the first sides of the insulating strips in the stacks, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips;"

Emphasis added.

Claim 20 is rejected with the same arguments as for the rejection of claim 1 (Page 5, the Office Action), and should be allowable for at least the same reasons as explained for claim 1.

Claim 21

Claim 21 as amended includes the limitations

"depositing the blocking layers over the first sidewalls of the sacrificial strips in the first recessed regions and over the first sides of the insulating strips in the stacks;

depositing charge trapping material over the blocking layers in the first recessed regions; and

depositing the tunneling layers over the charge trapping material in the first recessed regions and over the blocking layers over the first sides of the insulating strips in the stacks."

Emphasis added.

Claim 21 is rejected with the same arguments as for the rejection of claim 12 (Page 8, the Office Action), and should be allowable for at least the same reasons as explained for claim 12.

Claims 2-4 and 6 depend from claim 1, and should be allowable for at least the same reasons as explained for claim 1, and because of the unique combinations recited.

Claims 12-17 depend from claim 11, and should be allowable for at least the same reasons as explained for claim 11, and because of the unique combinations recited.

Claims 21-22 and 24 depend from claim 20, and should be allowable for at least the same reasons as explained for claim 20, and because of the unique combinations recited.

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Accordingly reconsideration of the rejection of claims 1-4, 6, 11-17, 20-22 and 24 as amended under 35 U.S.C. § 102(a) (1) is respectfully requested.

Rejection of Claims 5, 7-10, 18-19 and 23 under 35 U.S.C. 103

Claims 5, 7-10, 18-19, 23 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861) in view of Liu et al (US Publication No. 2016/0204117).

Claim 7 as amended includes the limitations

> "blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips, between the discrete charge trapping elements and the second sidewalls of the conductive strips, between the tunneling layers and the first sides of the insulating strips, and between the tunneling layers and the second sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks, the blocking layers continuous across and in contact with the second sides of the insulating strips vertically between adjacent conductive strips in the stacks,"

Emphasis added; emphasis added.

Claim 7 is rejected with the same arguments as for the rejection of claim 1 (Page 5, the Office Action), and should be allowable for at least the same reasons as explained for claim 1.

Claim 5 depends from claim 1, and should be allowable for at least the same reasons as explained for claim 1, and because of the unique combinations recited.

Claims 8-10 depend from claim 7, and should be allowable for at least the same reasons as explained for claim 7, and because of the unique combinations recited.

Claims 18-19 depend from claim 11, and should be allowable for at least the same reasons as explained for claim 11, and because of the unique combinations recited.

Claim 23 depends from claim 20, and should be allowable for at least the same reasons as explained for claim 20, and because of the unique combinations recited.

Accordingly reconsideration of the rejection of claims 5, 7-10, 18-19, 23 as amended under 35 U.S.C. § 103 is respectfully requested.

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CONCLUSION

It is respectfully submitted that this application is now in condition for allowance.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 2194-1).

Respectfully submitted,

Dated: 24 August 2018

/Yiding Wu/

Yiding Wu, Reg. No. 65,992

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/410,965	01/20/2017	HANG-TING LUE	MXIC 2194-1	3219

46353 7590 08/31/2018

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EXAMINER	
ENAD, CHRISTINE A	

ART UNIT	PAPER NUMBER
2823	

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Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	15/410,965	LUE, HANG-TING	
	Examiner	Art Unit	
	CHRISTINE ENAD	2823	

All participants (applicant, applicant's representative, PTO personnel):

(1) *CHRISTINE ENAD*. (3)_____.

(2) *Yiding Wu*. (4)_____.

Date of Interview: *23 August 2018*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☒103 ☐Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *1*.

Identification of prior art discussed: *Serov (2016/0071861)*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Discussed applicants invention with regards to the prior art of record. Discussed applicants proposed amendment. Response to the outstanding office action will be forthcoming.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☒ Attachment

/CHRISTINE ENAD/ Primary Examiner, Art Unit 2823	

Micron Ex. 1022, p. 172
Micron v. YMTC
IPR2024-00912

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

The action of the Patent and Trademark Office cannot be based exclusively on the written record in the Office if that record is itself incomplete through the failure to record the substance of interviews.

It is the responsibility of the applicant or the attorney or agent to make the substance of an interview of record in the application file, unless the examiner indicates he or she will do so. It is the examiner's responsibility to see that such a record is made and to correct material inaccuracies which bear directly on the question of patentability.

Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

The Interview Summary Form shall be given an appropriate Paper No., placed in the right hand portion of the file, and listed on the "Contents" section of the file wrapper. In a personal interview, a duplicate of the Form is given to the applicant (or attorney or agent) at the conclusion of the interview. In the case of a telephone or video-conference interview, the copy is mailed to the applicant's correspondence address either with or prior to the next official communication. If additional correspondence from the examiner is not likely before an allowance or if other circumstances dictate, the Form should be mailed promptly after the interview rather than with the next official communication.

The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
7) if appropriate, the general results or outcome of the interview unless already described in the Interview Summary Form completed by the examiner.

Examiners are expected to carefully review the applicant's record of the substance of an interview. If the record is not complete and accurate, the examiner will give the applicant an extendable one month time period to correct the record.

Examiner to Check for Accuracy

If the claims are allowable for other reasons of record, the examiner should send a letter setting forth the examiner's version of the statement attributed to him or her. If the record is complete and accurate, the examiner should place the indication, "Interview Record OK" on the paper recording the substance of the interview along with the date and the examiner's initials.

Dear Examiner Enad:

Thank you for agreeing to have an interview about Application No. 15/410,965 (Attorney docket No. MXIC 2194-1) at 2:00PM EST on Tuesday, August 21, 2018, in reference to the Office Action mailed 5/25/2018. Applicant proposes the following agenda.

1. Discuss an amendment in Claim 1, regarding the 35 USC 103 rejection on claim 1 in reference to Serov (Page 5, the Office Action). The amendment includes "**blocking layers (410, FIG. 9) … between the tunneling layers (810) and the first sides of the insulating strips (226);**" Support for the amendment can be found in FIG. 9 of the present specification. In FIG. 9B of Serov, the blocking dielectric layer 52 is NOT between a tunneling dielectric 56 and insulating layers 32.
2. Discuss an alternative amendment in Claim 1, including "**… a dielectric material (930, FIGs. 9 & 10) physically separating the first and second channel films (910, 920) at levels (A-A', FIG. 9) of data storage structures (510)**". Support for the amendment can be found in FIGs. 9 and 10. In Serov, both FIG. 9C of **Embodiment 1** and FIG. 16A of **Embodiment 2** show that "If a dielectric core 62 is present, the semiconductor channel 60 laterally surrounds the dielectric core 62" (last sentence, paragraph [0155], Serov), where the semiconductor channel 60 includes a first semiconductor channel portion 601 and a second semiconductor channel portion 602. Therefore the dielectric core 62 in Serov does NOT physically separate the second semiconductor channel portion 602.

Pursuant to MPEP § 502.03, Applicant hereby authorizes the Examiner to use e-mail during prosecution of this case to initiate and conduct WebEx interviews. We acknowledge that the WebEx invitation or session could be intercepted by third parties due to use of the Internet, but are comfortable with the in-session security afforded by WebEx.

Best regards,
Yiding Wu
Haynes Beffel & Wolfeld LLP
Phone 650-712-0340
P.O. Box 366
Half Moon Bay, CA 94019
ywu@hmbay.com

Proposed Amendment in Claim 1

blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips and between the tunneling layers and the first sides of the insulating strips, …

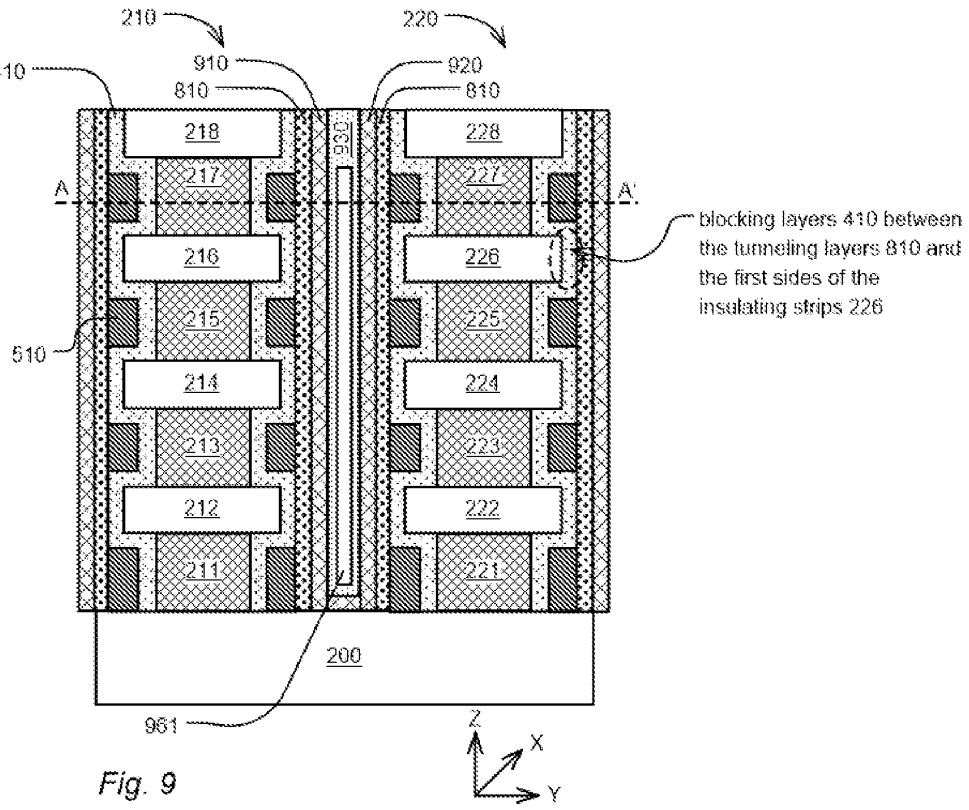


Fig. 9

Proposed Alternative Amendment in Claim 1

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating ~~between and contacting~~ the first and second channel films at levels of data storage structures; …

To: docket@hmbay.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 46353

Sep 05, 2018 04:16:28 AM

Dear PAIR Customer:

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 46353 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

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The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
15410965	INTV.SUM.APP	08/31/2018	MXIC 2194-1
	OA.APPENDIX	08/31/2018	MXIC 2194-1

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

PTO/SB/06 (09-11)
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/410,965	Filing Date 01/20/2017	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	08/24/2018	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 24	Minus	** 24	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 4	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	SLIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	brenda L gray
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/410,965	01/20/2017	HANG-TING LUE	MXIC 2194-1	3219

46353 7590 09/27/2018

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019

EXAMINER	
ENAD, CHRISTINE A	

ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
09/27/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hmbay.com

Micron Ex. 1022, p. 178
Micron v. YMTC
IPR2024-00912

Office Action Summary	Application No. 15/410,965	Applicant(s) LUE, HANG-TING	
	Examiner CHRISTINE ENAD	Art Unit 2823	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *8/24/2018*.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5)☒ Claim(s) *1-24* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-24* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

4) ☐ Other: _____.

Micron Ex. 1022, p. 179
Micron v. YMTC
IPR2024-00912

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6, 11-17, 20-22, 24 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861) in view of Alsmeier et al (US Publication No. 2012/0001249).

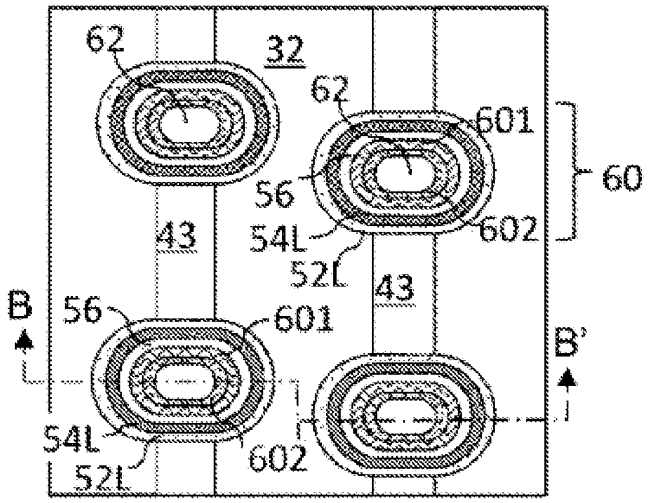


FIG. 16A

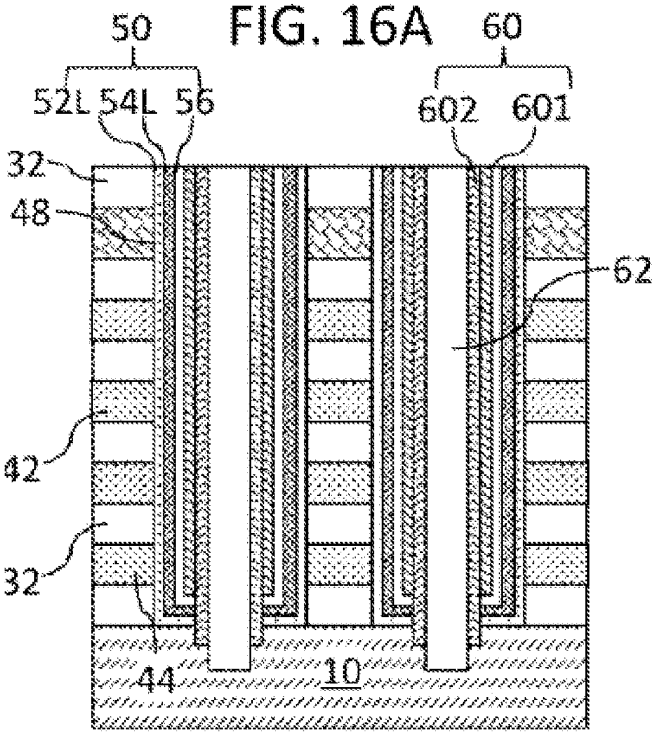


FIG. 16B

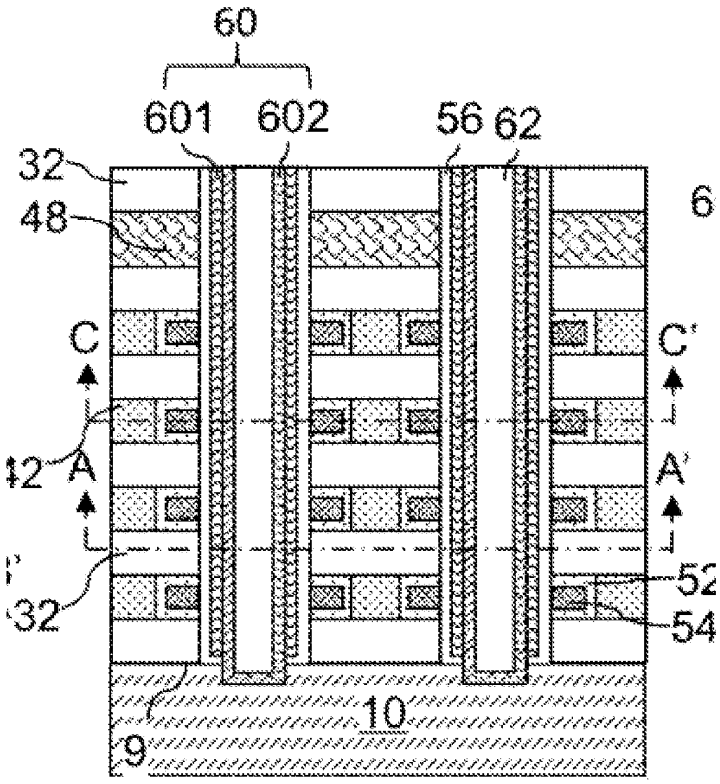


FIG. 9B

Regarding claim 1, Serov discloses a memory device, comprising: a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips alternating with insulating strips **Fig 9A-10, 32**, the insulating strips in the stacks having first and second sides, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in

sides of the stacks **Fig 9A-10**; vertical channel pillars **Fig 9A-10, 601/602/62** disposed between the stacks, the vertical channel pillars having first **Fig 9A-10, 601** and second channel films **Fig 9A-10, 602** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 9A-10, 62** (Paragraph 0150) between and contacting the second channel film; and data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips **Fig 9A-10, (42/46)** in the stacks, the data storage structures including tunneling layers **Fig 9A-10, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56**, and blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips, the discrete charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions on the first sidewalls of the conductive strips **Fig 9A-10**. **Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B, 62** between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig 16B, 602 (right side of layer 62)** ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 16B, 54** in contact

with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement. Serov discloses all the limitations except for the arrangement of the blocking layer relative to the insulating strips.

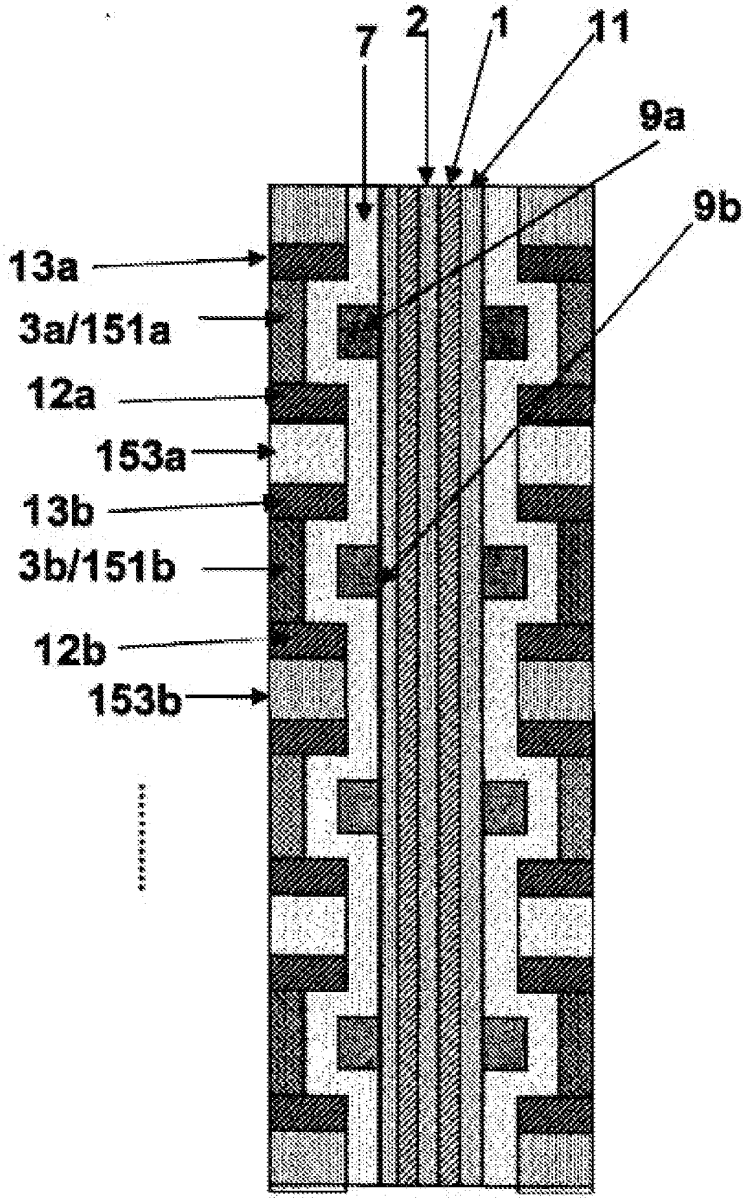


Figure 49

Whereas Alsmeier discloses data storage structures **Fig 49** at cross points of the vertical channel pillars **Fig 49, 2** between the stacks and the conductive strips in the

stacks, the data storage structures including tunneling layers **Fig 49, 11** in contact with the channel film in the vertical channel pillars, discrete charge trapping elements **Fig 49, 9** in contact with the tunneling layers **Fig 49, 11** and blocking layers **Fig 49, 7** between the discrete charge trapping elements **Fig 49, 9** and the first sidewalls of the conductive strips **Fig 49, 151** and between the tunneling layers **Fig 49, 11** and the first sides of the insulating strips **Fig 49, 153** the blocking layers **Fig 49, 7** continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks **Fig 43-51.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the layer arrangement of Serov and incorporate the arrangement of Alsmeier as an alternative arrangement to improve device performance.

Regarding claim 2, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions are dielectric charge trapping elements (Paragraph 0143).

Regarding claim 3, Serov discloses the conductive strips in the stacks have second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions on the second sidewalls of the conductive strips; and the data storage structures include discrete charge trapping elements disposed in the second recessed regions in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements in the second recessed regions and the second sidewalls of the conductive strips **Fig 9A-10.**

Regarding claim 4, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** disposed in the second recessed regions are dielectric charge trapping elements (Paragraph 0043).

Regarding claim 6, Serov discloses the conductive strips in the plurality of stacks of conductive strips include a metal material (Paragraph 0133).

Regarding claim 11, Serov discloses a manufacturing method, comprising: forming a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips **Fig 9A-10, (42/46)** alternating with insulating strips **Fig 9A-10, 32**, the insulating strips **Fig 9A-10, 32**in the stacks having first and second sides **Fig 9A-10**, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls; recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks **Fig 5A-5C;** forming data storage structures in the first recessed regions **Fig 6A-8C;** forming first and second channel films **Fig 9A-10, 60** on the data storage structures on sidewalls of adjacent stacks; and depositing a dielectric material **Fig 9A-10, 62** between the first and second channel films, the dielectric material contacting the second channel films on the sidewalls of the adjacent stacks **Fig 9A-10**. **Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B,**

62 between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig 16B, 602 (right side of layer 62)** ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 16B, 54** in contact with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement. Serov discloses all the limitations except for the arrangement of the blocking layer relative to the insulating strips.

Whereas Alsmeier discloses data storage structures **Fig 49** at cross points of the vertical channel pillars **Fig 49, 2** between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers **Fig 49, 11** in contact with the channel film in the vertical channel pillars, discrete charge trapping elements **Fig 49, 9** in contact with the tunneling layers **Fig 49, 11** and blocking layers **Fig 49, 7** between the discrete charge trapping elements **Fig 49, 9** and the first sidewalls of the conductive strips **Fig 49, 151** and between the tunneling layers **Fig 49, 11** and the first sides of the insulating strips **Fig 49, 153** the blocking layers **Fig 49, 7** continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks **Fig 43-51.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the layer arrangement of Serov and incorporate the arrangement of Alsmeier as an alternative arrangement to improve device performance.

Regarding claim 12, Serov and Alsmeier disclose said forming the data storage structures comprising: depositing blocking layers **Fig 9A-10, 52** over the first sidewalls of the conductive strips in the first recessed regions; depositing charge trapping material **Fig 9A-10, 54** over the blocking layers **Fig 9A-10, 52** in the first recessed regions; and depositing tunneling layers **Fig 9A-10, 56** over the charge trapping material **Fig 9A-10, 54** in the first recessed regions (Serov- **Fig 9A-10;** Alsmeier-**Fig 43-51**).

Regarding claim 13, Serov discloses wherein the charge trapping material is dielectric charge trapping material (Paragraph 0143).

Regarding claim 14, Serov discloses comprising: said depositing the blocking layers **Fig 9A-10, 52** including depositing the blocking layers **Fig 9A-10, 52** over the first sides of the insulating strips **Fig 6B**; and said depositing the charge trapping material **Fig 9A-10, 54** including depositing the charge trapping material **Fig 9A-10, 52** over the blocking layers **Fig 6B** over the first sides of the insulating strips **Fig 6B**; and separating the charge trapping material between adjacent first recessed regions **Fig 6A-6C.**

Regarding claim 15, Serov discloses said separating the charge trapping material **Fig 9A-10, 54** including removing the charge trapping material over the blocking layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions **Fig 6A-8C.**

Regarding claim 16, Serov discloses comprising: etching to isolate the data storage structures along the conductive strips, to form discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56** and the

blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips.

Regarding claim 17, Serov discloses wherein the conductive strips in the stacks of conductive strips have second sidewalls opposite the first sidewalls **Fig 9A-10**, the manufacturing method comprising: recessing the second sidewalls of the conductive strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks; and forming the data storage structures in the second recessed regions **Fig 5A-10.**

Regarding claim 20, Serov discloses a manufacturing method, comprising: forming a plurality of stacks **Fig 9A-10, 32/(42/46)** of sacrificial strips **Fig 9A-10, 42** alternating with insulating strips **Fig 9A-10, 32**, the insulating strips **Fig 9A-10, 32**in the stacks having first and second sides **Fig 9A-10**, and the sacrificial strips **Fig 9A-10, 42** in the stacks having first sidewalls; recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks **Fig 5A-5C;** forming data storage structures in the first recessed regions **Fig 6A-8C;** forming first and second channel films **Fig 9A-10, 60** on the data storage structures on sidewalls of adjacent stacks; and depositing a dielectric material **Fig 9A-10, 62** between the first and second channel films, the dielectric material contacting the second channel films on the sidewalls of the adjacent stacks **Fig 9A-10**, and replacing the sacrificial strips in the stacks with a metal material **Fig 10, 46. Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel

arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B, 62** between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig 16B, 602 (right side of layer 62)** ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 16B, 54** in contact with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement. Serov discloses all the limitations except for the arrangement of the blocking layer relative to the insulating strips.

Whereas Alsmeier discloses data storage structures **Fig 49** at cross points of the vertical channel pillars **Fig 49, 2** between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers **Fig 49, 11** in contact with the channel film in the vertical channel pillars, discrete charge trapping elements **Fig 49, 9** in contact with the tunneling layers **Fig 49, 11** and blocking layers **Fig 49, 7** between the discrete charge trapping elements **Fig 49, 9** and the first sidewalls of the conductive strips **Fig 49, 151** and between the tunneling layers **Fig 49, 11** and the first sides of the insulating strips **Fig 49, 153** the blocking layers **Fig 49, 7** continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive

strips in the stacks **Fig 43-51.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the layer arrangement of Serov and incorporate the arrangement of Alsmeier as an alternative arrangement to improve device performance.

Regarding claim 21, Serov and Alsmeier discloses said forming the data storage structures comprising: depositing blocking layers **Fig 9A-10, 52** over the first sidewalls of the conductive strips in the first recessed regions; depositing charge trapping material **Fig 9A-10, 54** over the blocking layers **Fig 9A-10, 52** in the first recessed regions; and depositing tunneling layers **Fig 9A-10, 56** over the charge trapping material **Fig 9A-10, 54** in the first recessed regions (Serov- **Fig 9A-10;** Alsmeier-**Fig 43-51**).

Regarding claim 22, Serov discloses wherein the charge trapping material is dielectric charge trapping material (Paragraph 0143).

Regarding claim 24, Serov discloses said replacing comprising: etching the stacks to form a trench, exposing the sacrificial strips in the trench; removing the sacrificial strips in the trench; depositing the metal material in the trench; and separating the metal material between the insulating strips in the trench (Paragraph 0152-0154).

Claims 5, 7-10, 18-19, 23 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861) in view of Liu et al (US Publication No. 2016/0204117) and Alsmeier et al (US Publication No. 2012/0001249).

Regarding claims, 5, 19, and 23, Serov discloses all the limitations except for the gap in the channel region. Whereas Liu discloses leaving a gap between the first and

second vertical channel films **Fig 2A-4B** (Paragraph 0075-0076). Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the device of Serov and incorporate a gap to provide a connector between device levels.

Regarding claim 7, Serov discloses a memory device, comprising: a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips alternating with insulating strips **Fig 9A-10, 32**, the insulating strips in the stacks having first and second sides, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks **Fig 9A-10;** and having second sidewall opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions in sides of the stacks **Fig 9A-10;** vertical channel pillars **Fig 9A-10, 601/602/62** disposed between the stacks, the vertical channel pillars having first **Fig 9A-10, 601** and second channel films **Fig 9A-10, 602** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 9A-10, 62** (Paragraph 0150) between and contacting the second channel films; and data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips **Fig 9A-10, (42/46)** in the stacks, the data storage structures including tunneling layers **Fig 9A-10, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56**, and blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips and between the

discrete charge trapping elements and the second sidewalls of the conductive strips **Fig 9A-10**, the discrete charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions on the first sidewalls of the conductive strips and disposed in the second recessed regions on the second sidewalls of the conductive strips **Fig 9A-10.** Serov discloses all the limitations except for the offset in the channel region.

Whereas Liu discloses the vertical channel pillars are arranged so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips **Fig 2A-4B** (Paragraph 0075-0076). Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the device of Serov and incorporate an offset to provide a connector between device levels. **Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers.

Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B, 62** between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig 16B, 602 (right side of layer 62)** ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel

pillars, discrete charge trapping elements **Fig 16B, 54** in contact with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement. Serov and Liu discloses all the limitations except for the arrangement of the blocking layer relative to the insulating strips.

Whereas Alsmeier discloses data storage structures **Fig 49** at cross points of the vertical channel pillars **Fig 49, 2** between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers **Fig 49, 11** in contact with the channel film in the vertical channel pillars, discrete charge trapping elements **Fig 49, 9** in contact with the tunneling layers **Fig 49, 11** and blocking layers **Fig 49, 7** between the discrete charge trapping elements **Fig 49, 9** and the first sidewalls of the conductive strips **Fig 49, 151,** between the discrete charge trapping elements and the second sidewalls of the conductive strips **Fig 49**, between the tunneling layers **Fig 49, 11** and the first sides of the insulating strips **Fig 49, 153** and between the tunneling layers and the second sides of the insulating strips **Fig 49,** the blocking layers **Fig 49, 7** continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks **Fig 43-51,** the blocking layers continuous across and in contact with the second sides of the insulating strips vertically between adjacent conductive strips in the stacks **Fig 43-51.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the

claimed invention to modify the layer arrangement of Serov and incorporate the arrangement of Alsmeier as an alternative arrangement to improve device performance.

Regarding claim 8, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** are dielectric charge trapping elements (Paragraph 0143).

Regarding claim 9, Serov discloses wherein the dielectric material comprises a gap **Fig 2A-4B** (Paragraph 0075-0076).

Regarding claim 10, Serov discloses the conductive strips in the plurality of stacks of conductive strips include a metal material (Paragraph 0133).

Regarding claim 18, Liu discloses etching to isolate the first and second channel films and the dielectric material between the first and second channel films along the conductive strips, to form vertical channel pillars between the stacks, so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips **Fig 2A-4B** (Paragraph 0075-0076).

Response to Arguments

Applicant's arguments with respect to claims 1-24 have been considered but are moot because the arguments do not apply to any of the references being used in the current rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTINE ENAD whose telephone number is (571)270-7891. The examiner can normally be reached on Monday - Thursday, 7:30 am - 6:00 pm, EST.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brett Feeney can be reached on (571) 270 5484. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CHRISTINE ENAD/
Primary Examiner, Art Unit 2823

Notice of References Cited	Application/Control No. 15/410,965	Applicant(s)/Patent Under Reexamination LUE, HANG-TING	
	Examiner CHRISTINE ENAD	Art Unit 2823	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-2012/0001249 A1	01-2012	Alsmeier; Johann	H01L27/11551	257/319
	B	US-				
	C	US-				
	D	US-				
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15410965	LUE, HANG-TING
	Examiner	Art Unit
	CHRISTINE ENAD	2823

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/24/2017	05/21/2018	09/18/2018						
	1	✓	✓	✓						
	2	✓	✓	✓						
	3	✓	✓	✓						
	4	✓	✓	✓						
	5	✓	✓	✓						
	6	✓	✓	✓						
	7	✓	✓	✓						
	8	✓	✓	✓						
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	16	✓	✓	✓						
	17	✓	✓	✓						
	18	✓	✓	✓						
	19	✓	✓	✓						
	20	✓	✓	✓						
	21	✓	✓	✓						
	22	✓	✓	✓						
	23	✓	✓	✓						
	24	✓	✓	✓						

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15410965	LUE, HANG-TING
	Examiner	Art Unit
	CHRISTINE ENAD	2823

CPC- SEARCHED		
Symbol	Date	Examiner
H01L27/11582	11/24/2017	CE
H01L21/76802, 21/76877	11/24/2017	CE
H01L23/5226, 23/528	11/24/2017	CE

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

SEARCH NOTES		
Search Notes	Date	Examiner
Assignee and inventor search conducted	11/24/2017	CE
CPC search	11/24/2017	CE
EAST Search	11/24/2017	CE
EAST Search	5/21/2018	CE
EAST Search	9/18/2018	CE

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/CHRISTINE ENAD/ Primary Examiner.Art Unit 2823

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	574	(("MACRONIX") near3 ("INTERNATIONAL") near3 ("CO") near3 ("LTD")).AANM.	USPAT	OR	OFF	2017/11/22 09:51
S2	358	(("LUE") near3 ("HANG-TING")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 09:51
S3	9877	(H01L27/11582.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:51
S4	13188	(H01L21/76802.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:51
S5	17402	(H01L21/76877.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S6	15471	(H01L23/5226.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S7	13459	(H01L23/528.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S8	20	(vertical near stack) and ((insulating or dielectric or insulation) near channel)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 10:17
S9	0	("2017/0243879").URPN.	USPAT	OR	OFF	2017/11/22 10:21

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S10	28	("20070029607" | "20090230454" | "20100207194" | "20100213527" | "20110156044" | "20120012921" | "20120326221" | "20140131784" | "20150044833" | "20150076584" | "20150179660" | "20150255481" | "20150371709" | "20160133642" | "5915167" | "7575973" | "7906392" | "8084819" | "8187936" | "8461641" | "8610194" | "8735962" | "8767465" | "8823076" | "8853765" | "8981457" | "8987119" | "9023719").PN. OR ("9728546").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 10:25
S11	328	((insulating or dielectric or insulation) near channel)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 12:35
S12	0	((insulating or dielectric or insulation) near channel near gap)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S13	10	((insulating or dielectric or insulation) near channel near gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S14	346	((insulating or dielectric or insulation) near channel same gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S15	1065	((insulating or dielectric or insulation) same channel same gap)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 18:00
S16	4	("20120001249").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:05
S17	2	("20160181271").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:07

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S18	8	(("20130049095") or ("20100181612") or ("20130100741")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:07
S19	51	((insulating or dielectric or insulation) same channel NEAR (SEPARATION OR gap or void))and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 18:52
S20	35	("20050280061" | "20070045708" | "20070158736" | "20070252201" | "20080073635" | "20080175032" | "20080180994" | "20090097321" | "20090184360" | "20100270593" | "20110018051" | "20120068241" | "20120119283" | "20120182806" | "20150243674" | "20150357342" | "20150371998" | "20160056168" | "6906940" | "7315474" | "7420242" | "7612403" | "7696559" | "7851849" | "8008732" | "8363476" | "8467219" | "8503213" | "8648438" | "8759899" | "8853818" | "9147468" | "9224473").PN. OR ("9401371").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 18:53
S21	7	("20160005746" | "20160163733" | "20160240551" | "9379122" | "9379131" | "9401209" | "9401371").PN. OR ("9818760").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 18:56
S22	32	((insulating or dielectric or insulation) same channel NEAR (seam or hollow))and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 19:02
S23	2	("20160204117").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/24 13:25
S24	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/05/14 11:31
S25	39484	((insulating or dielectric or insulation) same channel)and (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/05/14 12:11
S26	19502	((insulating or dielectric or insulation) same channel)same (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2018/05/14 12:11

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			EPO; JPO; DERWENT; IBM_TDB			
S27	305	((insulating or dielectric or insulation) same channel) near (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/05/14 12:13
S28	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/05/21 19:06
S29	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/08/23 12:43
S30	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:14
S31	1	("20180211969").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:18
S32	0	("2017/0194340").URPN.	USPAT	OR	OFF	2018/09/18 09:35
S33	1	("9831257").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:36
S34	43	("20050280061" | "20070045708" | "20070158736" | "20070252201" | "20080073635" | "20080175032" | "20080180994" | "20090097321" | "20090184360" | "20100181612" | "20100270593" | "20110018051" | "20120001249" | "20120068241" | "20120119283" | "20120147644" | "20120182806" | "20130049095" | "20130100741" | "20130134492" | "20130207178" | "20130248945" | "20140231954" | "20150263016" | "20150318301" | "20150364487" | "20160043100" | "20160181271" | "6906940" | "7153780" | "7315474" | "7420242" | "7696559" | "7851849" | "8008732" | "8363476" | "8467219" | "8503213" | "8648438" | "8759899" | "8853818" | "9147468" | "9287291").PN. OR ("9831257").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:36
S35	43	("20050280061" | "20070045708" | "20070158736" | "20070252201" | "20080073635" | "20080175032" | "20080180994" | "20090097321" | "20090184360" | "20100181612" | "20100270593" | "20110018051" | "20120001249" | "20120068241" | "20120119283" | "20120147644" | "20120182806" | "20130049095" | "20130100741" | "20130134492" | "20130207178" | "20130248945" | "20140231954" | "20150263016" | "20150318301" | "20150364487" | "20160043100" | "20160181271" |	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:36

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		"6906940" | "7153780" | "7315474" | "7420242" | "7696559" | "7851849" | "8008732" | "8363476" | "8467219" | "8503213" | "8648438" | "8759899" | "8853818" | "9147468" | "9287291").PN. OR ("9831257").URPN.				
S36	3525	(blocking same tunneling) and (memory near device)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:59
S37	1765	(blocking same tunneling same channel) and (memory near device)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:59
S38	3	(("20110147823") or ("20120001249") or ("20170278859")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 10:32

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To: docket@hmbay.com,,
From: PAIR_eOfficeAction@uspto.gov
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Subject: Private PAIR Correspondence Notification for Customer Number 46353

Sep 27, 2018 04:14:05 AM

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Application	Document	Mailroom Date	Attorney Docket No.
15410965	CTFR	09/27/2018	MXIC 2194-1
	892	09/27/2018	MXIC 2194-1

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

Doc Code: A.NE.AFCP
Document Description: After Final Consideration Pilot Program Request

PTO/SB/434 (05-13)

CERTIFICATION AND REQUEST FOR CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0

Practitioner Docket No.:	Application No.:	Filing Date:
MXIC 2194-1	15/410,965	20 January 2017
First Named Inventor:	**Title:**	
Hang-Ting Lue	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE	

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS CONSIDERATION UNDER THE AFTER FINAL CONSIDERATION PILOT PROGRAM 2.0 (AFCP 2.0) OF THE ACCOMPANYING RESPONSE UNDER 37 CFR 1.116.

1. The above-identified application is (i) an original utility, plant, or design nonprovisional application filed under 35 U.S.C. 111(a) [a continuing application (*e.g.*, a continuation or divisional application) is filed under 35 U.S.C. 111(a) and is eligible under (i)], or (ii) an international application that has entered the national stage in compliance with 35 U.S.C. 371(c).
2. The above-identified application contains an outstanding final rejection.
3. Submitted herewith is a response under 37 CFR 1.116 to the outstanding final rejection. The response includes an amendment to at least one independent claim, and the amendment does not broaden the scope of the independent claim in any aspect.
4. This certification and request for consideration under AFCP 2.0 is the only AFCP 2.0 certification and request filed in response to the outstanding final rejection.
5. Applicant is willing and available to participate in any interview requested by the examiner concerning the present response.
6. This certification and request is being filed electronically using the Office's electronic filing system (EFS-Web).
7. Any fees that would be necessary consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, extension of time fees, are being concurrently filed herewith. [There is no additional fee required to request consideration under AFCP 2.0.]
8. By filing this certification and request, applicant acknowledges the following:
    - Reissue applications and reexamination proceedings are not eligible to participate in AFCP 2.0.
    - The examiner will verify that the AFCP 2.0 submission is compliant, *i.e.*, that the requirements of the program have been met (see items 1 to 7 above). For compliant submissions:
        - The examiner will review the response under 37 CFR 1.116 to determine if additional search and/or consideration (i) is necessitated by the amendment and (ii) could be completed within the time allotted under AFCP 2.0. If additional search and/or consideration is required but cannot be completed within the allotted time, the examiner will process the submission consistent with current practice concerning responses after final rejection under 37 CFR 1.116, *e.g.*, by mailing an advisory action.
        - If the examiner determines that the amendment does not necessitate additional search and/or consideration, or if the examiner determines that additional search and/or consideration is required and could be completed within the allotted time, then the examiner will consider whether the amendment places the application in condition for allowance (after completing the additional search and/or consideration, if required). If the examiner determines that the amendment does not place the application in condition for allowance, then the examiner will contact the applicant and request an interview.
            - The interview will be conducted by the examiner, and if the examiner does not have negotiation authority, a primary examiner and/or supervisory patent examiner will also participate.
            - If the applicant declines the interview, or if the interview cannot be scheduled within ten (10) calendar days from the date that the examiner first contacts the applicant, then the examiner will proceed consistent with current practice concerning responses after final rejection under 37 CFR 1.116.

Signature	Date
/Yiding Wu/	13 November 2018
Name (Print/Typed) Yiding Wu	**Practitioner Registration No.** 65992

***Note**: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.*

☐ * Total of _____ forms are submitted.

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	34301252
Application Number:	15410965
International Application Number:	
Confirmation Number:	3219
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	HANG-TING LUE
Customer Number:	46353
Filer:	Yiding Wu/Amy Jonsson
Filer Authorized By:	Yiding Wu
Attorney Docket Number:	MXIC 2194-1
Receipt Date:	13-NOV-2018
Filing Date:	20-JAN-2017
Time Stamp:	20:02:39
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	After Final Consideration Program Request	00671358.PDF	226597 f39cbbf72067771e56f8669039bbeafb218b92c1	no	2
Warnings:					

Information:					
2	Response After Final Action	00671365.PDF	221663 57573d4b179ba23a902ffea0fdd765ededede8eb27	no	15
Warnings:					
Information:					
			Total Files Size (in bytes):	448260	

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

CERTIFICATE OF ELECTRONIC TRANSMISSION
I hereby certify that this correspondence is being electronically transmitted to United States Patent and Trademark Office on 13 November 2018.
/Amy Jonsson/
Amy Jonsson

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of inventor(s):
Hang-Ting Lue

Application No. **15/410,965**

Confirmation No. **3219**

Filing Date: **20 January 2017**

Title: **DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE**

Group Art Unit: **2823**

Examiner: **Christine A Enad**

CUSTOMER NO. 46353

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE AFTER FINAL

Sir:

In response to the Final Office Action dated 27 September 2018, Applicant requests consideration of the following amendments in the above-referenced application. An AFCP Form accompanies this Amendment:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 10 of this paper.

///

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In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating ~~between and contacting~~ the first and second channel films at levels of data storage structures; and

the data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips and between the tunneling layers and the first sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks, the discrete charge trapping elements disposed in the first recessed regions on the first sidewalls of the conductive strips.

2. (original) The memory device of claim 1, wherein the discrete charge trapping elements disposed in the first recessed regions are dielectric charge trapping elements.

3. (original) The memory device of claim 1, wherein the conductive strips in the stacks have second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions on the second sidewalls of the conductive strips; and

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the data storage structures include discrete charge trapping elements disposed in the second recessed regions in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements in the second recessed regions and the second sidewalls of the conductive strips.

4. (original) The memory device of claim 3, wherein the discrete charge trapping elements disposed in the second recessed regions are dielectric charge trapping elements.

5. (original) The memory device of claim 1, wherein the dielectric material comprises a gap.

6. (original) The memory device of claim 1, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

7. (currently amended) A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks and having second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating ~~between and contacting~~ the first and second channel films at levels of data storage structures; and

the data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips, between the discrete charge trapping elements and the second

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sidewalls of the conductive strips, between the tunneling layers and the first sides of the insulating strips, and between the tunneling layers and the second sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks, the blocking layers continuous across and in contact with the second sides of the insulating strips vertically between adjacent conductive strips in the stacks, the discrete charge trapping elements disposed in the first recessed regions on the first sidewalls of the conductive strips and disposed in the second recessed regions on the second sidewalls of the conductive strips,

wherein the vertical channel pillars are arranged so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips.

8. (original) The memory device of claim 7, wherein the discrete charge trapping elements are dielectric charge trapping elements.

9. (original) The memory device of claim 7, wherein the dielectric material comprises a gap.

10. (original) The memory device of claim 7, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

11. (currently amended) A manufacturing method, comprising:

forming a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls;

recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions, including forming blocking layers between tunneling layers and the first sides of the insulating strips in the

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stacks, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks; and

depositing a dielectric material between the first and second channel films, the dielectric material physically separating ~~contacting~~ the first and second channel films on the sidewalls of the adjacent stacks at levels of the data storage structures.

12. (previously presented) The manufacturing method of claim 11, said forming the data storage structures comprising:

depositing the blocking layers over the first sidewalls of the conductive strips in the first recessed regions and over the first sides of the insulating strips in the stacks;

depositing charge trapping material over the blocking layers in the first recessed regions; and

depositing the tunneling layers over the charge trapping material in the first recessed regions and over the blocking layers over the first sides of the insulating strips in the stacks.

13. (original) The manufacturing method of claim 12, wherein the charge trapping material is dielectric charge trapping material.

14. (original) The manufacturing method of claim 12, comprising:

said depositing the blocking layers including depositing the blocking layers over the first sides of the insulating strips; and

said depositing the charge trapping material including depositing the charge trapping material over the blocking layers over the first sides of the insulating strips; and separating the charge trapping material between adjacent first recessed regions.

15. (original) The manufacturing method of claim 14, said separating the charge trapping material including removing the charge trapping material over the blocking

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layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions.

16. (original) The manufacturing method of claim 11, comprising:

etching to isolate the data storage structures along the conductive strips, to form discrete charge trapping elements in contact with the tunneling layers and the blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips.

17. (original) The manufacturing method of claim 11, wherein the conductive strips in the stacks of conductive strips have second sidewalls opposite the first sidewalls, the manufacturing method comprising:

recessing the second sidewalls of the conductive strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks; and

forming the data storage structures in the second recessed regions.

18. (original) The manufacturing method of claim 17,

etching to isolate the first and second channel films and the dielectric material between the first and second channel films along the conductive strips, to form vertical channel pillars between the stacks, so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips.

19. (original) The manufacturing method of claim 11, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

20. (currently amended) A manufacturing method, comprising:

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forming a plurality of stacks of sacrificial strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the sacrificial strips in the stacks having first sidewalls;

recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions, including forming blocking layers between tunneling layers and the first sides of the insulating strips in the stacks, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks;

depositing a dielectric material between the first and second channel films, the dielectric material physically separating ~~contacting~~ the first and second channel films on the sidewalls of the adjacent stacks at levels of the data storage structures; and

replacing the sacrificial strips in the stacks with a metal material.

21. (previously presented) The manufacturing method of claim 20, said forming the data storage structures comprising:

depositing the blocking layers over the first sidewalls of the sacrificial strips in the first recessed regions and over the first sides of the insulating strips in the stacks;

depositing charge trapping material over the blocking layers in the first recessed regions; and

depositing the tunneling layers over the charge trapping material in the first recessed regions and over the blocking layers over the first sides of the insulating strips in the stacks.

22. (original) The manufacturing method of claim 21, wherein the charge trapping material is dielectric charge trapping material.

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23. (original) The manufacturing method of claim 20, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

24. (original) The manufacturing method of claim 20, said replacing comprising:
etching the stacks to form a trench, exposing the sacrificial strips in the trench;
removing the sacrificial strips in the trench;
depositing the metal material in the trench; and
separating the metal material between the insulating strips in the trench.

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REMARKS

The present application is being examined under the first inventor to file provisions of the AIA.

In the Office Action dated 27 September 2018, the Examiner reviewed claims 1-24. Claims 1-24 are rejected.

Applicant has amended claims 1, 7, 11 and 20.

Claims 1-24 remain pending.

Each rejection is respectfully traversed below.

Why This Response After Final Should Be Entered

Entry of the amendment is requested for consideration under the After Final Consideration Pilot AFCP.

37 C.F.R.1.116(b)(3). This Response should be entered because it could not have been submitted earlier. Specifically, the present Office Action of 09/27/2018 relied on a newly cited Alsmeier (US Publication No. 2012/0001249) for rejections under 35 U.S.C. §103. Applicant therefore could not have remedied the Examiner's concern based on the newly cited reference prior to the present Response because Applicant did not know it until now.

37 C.F.R.1.116(b)(2). Should the above is not considered sufficient reason for entering the present Response, Applicant respectfully requests that it be entered because it presents the rejected claims in better form for consideration on appeal.

Claim Amendments

Applicant has amended claim 1 to recite "a dielectric material physically separating the first and second channel films at levels of data storage structures".

Support for the amendment can be found in Figures 9 and 10 of the present specification, which illustrate a dielectric material 930 physically separating the first and second channel films 910 and 920 at levels of data storage structures 510, for example, at a level indicated by the line A-A' in Figure 9.

Applicant has made corresponding amendments in claims 7, 11 and 20. No new matter is added.

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Rejection of Claims 1-4, 6, 11-17, 20-22 and 24 under 35 U.S.C. 103

Claims 1-4, 6, 11-17, 20-22 and 24 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No. 2016/0071861), in view of Alsmeier et al., (US Publication No. 2012/0001249).

Claim 1

Claim 1 as amended includes the limitations

"vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating the first and second channel films at levels of data storage structures;"

Emphasis added.

Serov does not describe at least the quoted limitations, as explained below.

The Office Action asserts:

"Regarding claim 1, Serov discloses a memory device, comprising: …

vertical channel pillars **Fig 9A-10, 601/602/62** disposed between the stacks, the vertical channel pillars having first **Fig 9A-10, 601** and second channel films **Fig 9A-10, 602** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 9A-10, 62** (Paragraph 0150) between and contacting the second channel film; …

Embodiment 1 (Fig 9B) of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first Fig 16B, 602 (left side of layer 62) and second channel films Fig 16B, 602 (right side of layer 62) disposed on adjacent stacks in the plurality of stacks and a dielectric material Fig 16B, 62 between and contacting the first Fig 16B, 602 (left side of layer 62) and second channel film Fig 16B, 602 (right side of layer 62);"

Pages 4-5, the Office Action; emphasis added.

For convenience, FIGs. 9B, 9C, 16A and 16B of Serov are reproduced below.

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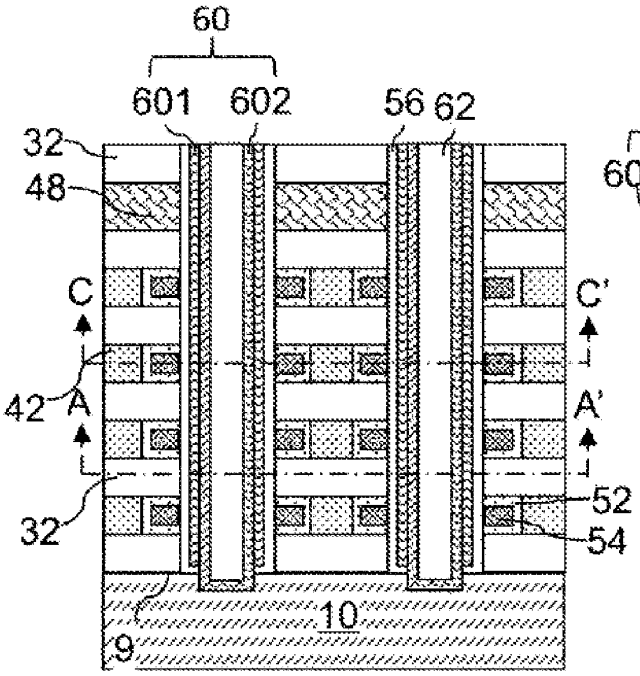


FIG. 9B

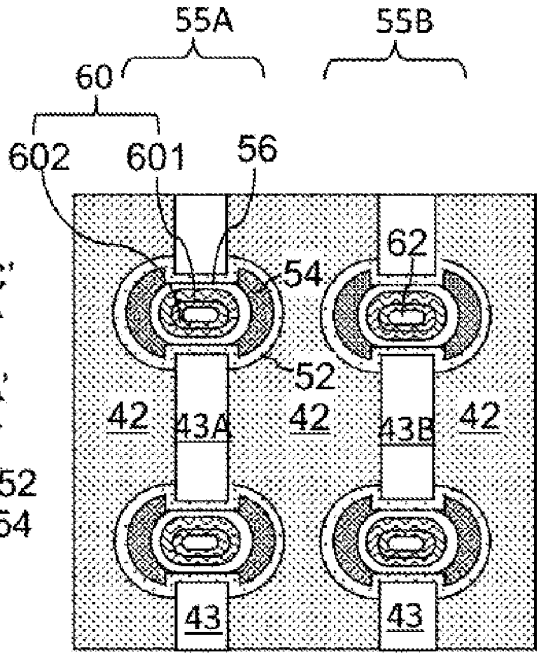


FIG. 9C

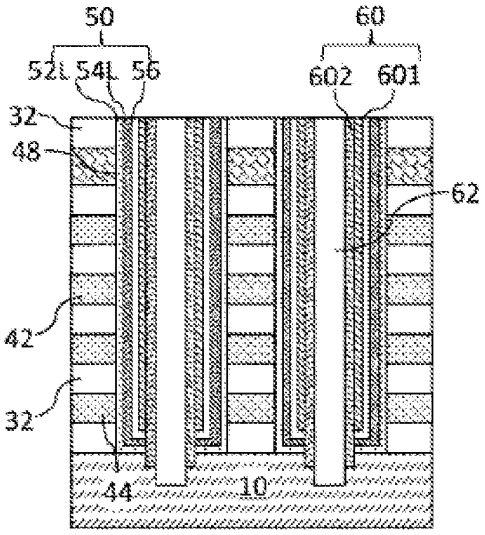


FIG. 16B

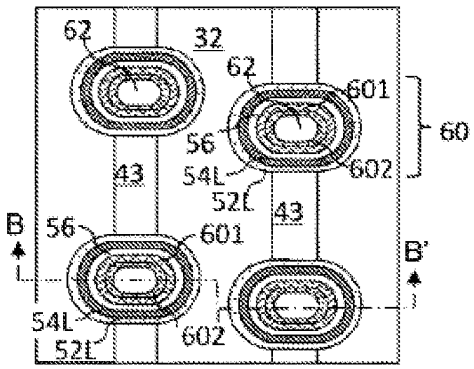


FIG. 16A

FIG. 9B is a vertical cross-sectional view of the first exemplary device structure for **Embodiment 1** (paragraphs [0030, 0031], Serov). FIG. 9C is a horizontal cross-sectional view taken along the horizontal plane C-C' of FIG. 9B (paragraph [0032], Serov).

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FIG. 16A is a top-down view of the second exemplary device structure for **Embodiment 2** (paragraphs [0043], Serov). FIG. 16B is a vertical cross-sectional view of the second exemplary device structure for **Embodiment 2** taken along the vertical plane B-B' of FIG. 16A (paragraph [0044], Serov).

Regarding "the arrangement of the channel layers", both **Embodiment 1** (FIGs. 9B, 9C) and **Embodiment 2** (FIGs. 16A, 16B) show that "Each adjoining pair of a first semiconductor channel portion 601 and a second semiconductor channel portion 602 collectively constitutes a semiconductor channel 60…" (paragraph [0150], Serov).

Both FIGs. 9C and 16A show that "If a dielectric core 62 is present, the semiconductor channel 60 laterally surrounds the dielectric core 62" (paragraph [0155], Serov), where the semiconductor channel 60 includes a first semiconductor channel portion 601 and a second semiconductor channel portion 602.

One difference between the two embodiments is that in **Embodiment 1** (FIG. 9B) the second semiconductor channel portion 602 is formed on a top surface of a substrate 10, while in **Embodiment 2** (FIG. 16B) the second semiconductor channel portion 602 is not formed on a top surface of a substrate 10. The top surface of the substrate is located at the bottom of a memory opening 49 (FIG. 4B), in which the semiconductor channel 60 is formed (FIG. 9B). However, this difference does not change the arrangement common to both embodiments that "the semiconductor channel 60 laterally surrounds the dielectric core 62" (paragraph [0155], Serov).

Consequently, in FIG. 16B, a second semiconductor channel portion 602 shown at "left side of layer 62" and at "right side of layer 62" is the same semiconductor channel portion that laterally surrounds the dielectric core 62. Similarly, in FIG. 9B, a second semiconductor channel portion 602 shown at "left side of layer 62" and at "right side of layer 62" is the same semiconductor channel portion that laterally surrounds the dielectric core 62.

Therefore Serov describes a dielectric core 62 laterally surrounded by a second semiconductor channel portion 602, and the dielectric core 62 does NOT physically separate the second semiconductor channel portion 602. In contrast, claim 1 requires

> "vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating the first and second channel films at levels of data storage structures".

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Since **Embodiment 1** and **Embodiment 2** both describe the dielectric core 62 laterally surrounded by a second semiconductor channel portion 602, it would not have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the **Embodiment 1** of Serov and incorporate the arrangement of **Embodiment 2** as an alternative channel arrangement, in order to reproduce the claimed invention.

Claim 1 should be allowable for at least the reasons explained above.

Claim 11

Claim 11 includes the limitations

"forming first and second channel films on the data storage structures on sidewalls of adjacent stacks; and

depositing a dielectric material between the first and second channel films, the dielectric material physically separating the first and second channel films on the sidewalls of the adjacent stacks at levels of the data storage structures."

Emphasis added.

Claim 11 is rejected with the same arguments as for the rejection of claim 1 (Pages 4-5, the Office Action), citing **Embodiment 1** (FIG. 9B) and **Embodiment 2** (FIG 16B) of Serov (Page 9, the Office Action).

Claim 11 should be allowable for at least the same reasons as explained for claim 1.

Claim 20

Claim 20 includes the limitations

"forming first and second channel films on the data storage structures on sidewalls of adjacent stacks;

depositing a dielectric material between the first and second channel films, the dielectric material physically separating the first and second channel films on the sidewalls of the adjacent stacks at levels of the data storage structures;"

Emphasis added.

Claim 20 is rejected with the same arguments as for the rejection of claim 1 (Pages 4-5, the Office Action), citing **Embodiment 1** (FIG. 9B) and **Embodiment 2** (FIG 16B) of Serov (Pages 12-13, the Office Action).

Claim 20 should be allowable for at least the same reasons as explained for claim 1.

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Claims 2-4 and 6 depend from claim 1, and should be allowable for at least the same reasons as explained for claim 1, and because of the unique combinations recited.

Claims 12-17 depend from claim 11, and should be allowable for at least the same reasons as explained for claim 11, and because of the unique combinations recited.

Claims 21-22 and 24 depend from claim 20, and should be allowable for at least the same reasons as explained for claim 20, and because of the unique combinations recited.

Accordingly reconsideration of the rejection of claims 1-4, 6, 11-17, 20-22 and 24 as amended under 35 U.S.C. § 103 is respectfully requested.

Rejection of Claims 5, 7-10, 18-19 and 23 under 35 U.S.C. 103

Claims 5, 7-10, 18-19, 23 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861) in view of Liu et al (US Publication No. 2016/0204117) and Alsmeier et al., (US Publication No. 2012/0001249).

Claim 7 includes the limitations

> "vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating the first and second channel films at levels of data storage structures;"

Emphasis added; emphasis added.

Claim 7 is rejected with the same arguments as for the rejection of claim 1 (Pages 4-5, the Office Action), and should be allowable for at least the same reasons as explained for claim 1.

Claim 5 depends from claim 1, and should be allowable for at least the same reasons as explained for claim 1, and because of the unique combinations recited.

Claims 8-10 depend from claim 7, and should be allowable for at least the same reasons as explained for claim 7, and because of the unique combinations recited.

Claims 18-19 depend from claim 11, and should be allowable for at least the same reasons as explained for claim 11, and because of the unique combinations recited.

Claim 23 depends from claim 20, and should be allowable for at least the same reasons as explained for claim 20, and because of the unique combinations recited.

Accordingly reconsideration of the rejection of claims 5, 7-10, 18-19, 23 as amended under 35 U.S.C. § 103 is respectfully requested.

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CONCLUSION

It is respectfully submitted that this application is now in condition for allowance.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 2194-1).

Respectfully submitted,

Dated: 13 November 2018

/Yiding Wu/

Yiding Wu, Reg. No. 65,992

MACRONIX c/o:
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(650) 712-0340 phone
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/410,965	Filing Date 01/20/2017	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	11/13/2018	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 24	Minus	** 24	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	*** 4	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	annette V smith
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/410,965	01/20/2017	HANG-TING LUE	MXIC 2194-1	3219

46353 7590 11/26/2018

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019

EXAMINER	
ENAD, CHRISTINE A	

ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
11/26/2018	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hmbay.com

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Advisory Action Before the Filing of an Appeal Brief	Application No. 15/410,965	Applicant(s) LUE, HANG-TING	
	Examiner CHRISTINE A ENAD	Art Unit 2823	AIA Status Yes

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 20 November 2018 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☑ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires ____ months from the mailing date of the final rejection.
   b) ☑ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection.The current period for reply expires ____ months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANTS FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37CFR 41.37(a).

AMENDMENTS

3. ☑ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☑ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: Newly added limitations to the independent claim (See 37CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicants reply has overcome the following rejection(s): _____
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☑ For purposes of appeal, the proposed amendment(s):(a) ☑ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☑ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: The newly added limitations would require further consideration and search. See attached interview summary.
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☑ Other: PTO2323 and interview summary.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
    Claim(s) allowed:_____.
    Claim(s) objected to:_____.
    Claim(s) rejected:1-24.
    Claim(s) withdrawn from consideration:_____.

/CHRISTINE A ENAD/ Primary Examiner, Art Unit 2823	

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Examiner-Initiated Interview Summary	Application No. 15/410,965	Applicant(s) LUE, HANG-TING	
	Examiner CHRISTINE A ENAD	Art Unit 2823	AIA Status Yes

All participants (applicant, applicant's representative, PTO personnel):

(1) CHRISTINE A. ENAD. (3) _____.

(2) Yiding Wu. (4) _____.

Date of Interview: 20 November 2018.

Type: ☑ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☑ No.
If Yes, brief description: _____.

Issues Discussed ☐ 101 ☐ 112 ☐ 102 ☑ 103 ☐ Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: 1.

Identification of prior art discussed: Kim 20180182776.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

Discussed applicants invention with regards to the Kim reference. See Paragraph 0105, Fig 14, 200 that describes a dielectric layer separating the first and second channel films..

Applicant recordation instructions: It is not necessary for applicant to provide a separate record of the substance of interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/CHRISTINE A ENAD/ Primary Examiner, Art Unit 2823	

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AFCP 2.0 Decision

Application No.	Applicant(s)	
15/410,965	LUE, HANG-TING	
Examiner	**Art Unit**	**AIA Status**
CHRISTINE A ENAD	2823	Yes

This is in response to the After Final Consideration Pilot request filed 13 November 2018.

1. **Improper Request** – The AFCP 2.0 request is improper for the following reason(s) and the after final amendment submitted with the request will be treated under pre-pilot procedure.

   ☐ An AFCP 2.0 request form PTO/SB/434 (or equivalent document) was not submitted.

   ☐ A non-broadening amendment to at least one independent claim was not submitted.

   ☐ A proper AFCP 2.0 request was submitted in response to the most recent final rejection.

   ☐ Other: _____

2. **Proper Request**

   A. After final amendment submitted with the request will not be treated under AFCP 2.0.
   The after final amendment cannot be reviewed and a search conducted within the guidelines of the pilot program.

   ☐ The after final amendment will be treated under pre-pilot procedure.

   B. Updated search and/or completed additional consideration.
   The examiner performed an updated search and/or completed additional consideration of the after final amendment within the time authorized for the pilot program. The result(s) of the updated search and/or completed additional consideration are:

   ☐ 1. All of the rejections in the most recent final Office action are overcome and a Notice of Allowance is issued herewith.

   ☐ 2. The after final amendment would not overcome all of the rejections in the most recent final Office action . See attached interview summary for further details.

   ☐ 3. The after final amendment was reviewed, and it raises a new issue(s). See attached interview summary for further details.

   ☑ 4. The after final amendment raises new issues, but would overcome all of the rejections in the most recent final Office action. A decision on determining allowability could not be made within the guidelines of the pilot. See attached interview summary for further details, including any newly discovered prior art.

   ☐ 5. Other: _____

   Examiner Note: Please attach an interview summary when necessary as described above.

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DO NOT ENTER: /C.A.E/

CERTIFICATE OF ELECTRONIC TRANSMISSION
I hereby certify that this correspondence is being electronically transmitted to United States Patent and Trademark Office on 13 November 2018.
/Amy Jonsson/
Amy Jonsson

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of inventor(s):
Hang-Ting Lue

Application No. **15/410,965**

Confirmation No. **3219**

Filing Date: **20 January 2017**

Title: **DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE**

Group Art Unit: **2823**

Examiner: **Christine A Enad**

CUSTOMER NO. 46353

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND RESPONSE AFTER FINAL

Sir:

In response to the Final Office Action dated 27 September 2018, Applicant requests consideration of the following amendments in the above-referenced application. An AFCP Form accompanies this Amendment:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 10 of this paper.

///

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To: docket@hmbay.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 46353

Nov 26, 2018 03:42:09 AM

Dear PAIR Customer:

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 46353 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
15410965	CTAV	11/26/2018	MXIC 2194-1
	INTV.SUM.EX	11/26/2018	MXIC 2194-1
	A.NE.AFCP.D	11/26/2018	MXIC 2194-1

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If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

Monday - Friday 6:00 a.m. to 12:00 a.m.

Thank you for prompt attention to this notice,

UNITED STATES PATENT AND TRADEMARK OFFICE

PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	15410965	Filing Date	2017-01-20	Docket Number (if applicable)	MXIC 2194-1	Art Unit	2823
First Named Inventor	Hang-Ting Lue			Examiner Name	Christine A. Enad		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☒ Amendment/Reply
- ☐ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
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Applicant Signature

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Signature	/Yiding Wu/	Date (YYYY-MM-DD)	2018-12-14
Name	Yiding Wu	Registration Number	65992

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Electronic Patent Application Fee Transmittal

Application Number:	15410965
Filing Date:	20-Jan-2017
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	HANG-TING LUE
Filer:	Yiding Wu/Amy Jonsson
Attorney Docket Number:	MXIC 2194-1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
RCE- 1ST REQUEST	1801	1	1300	1300
		Total in USD ($)		**1300**

Electronic Acknowledgement Receipt	
EFS ID:	34595073
Application Number:	15410965
International Application Number:	
Confirmation Number:	3219
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	HANG-TING LUE
Customer Number:	46353
Filer:	Yiding Wu/Amy Jonsson
Filer Authorized By:	Yiding Wu
Attorney Docket Number:	MXIC 2194-1
Receipt Date:	14-DEC-2018
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Application Type:	Utility under 35 USC 111(a)

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Payment was successfully received in RAM	$1300
RAM confirmation Number	121718INTEFSW17033700
Deposit Account	
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	00676263.PDF	1350177 a4ece801b54561318567e3a890b6bda533f09c35	no	3
Warnings:					
Information:					
2	Amendment Submitted/Entered with Filing of CPA/RCE	00676347.PDF	245448 2434803ecc7c381b60c2bb4cf98ba09697f15275	no	16
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30432 d93c1f9a88d7746be2e9dde0df599b5c527dc3a9	no	2
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/Amy Jonsson/
Amy Jonsson

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of inventor(s):
Hang-Ting Lue

Application No. **15/410,965**

Confirmation No. **3219**

Filing Date: **20 January 2017**

Title: **DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE**

Group Art Unit: **2823**

Examiner: **Christine A Enad**

CUSTOMER NO. 46353

MAIL STOP RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT ACCOMPANYING REQUEST FOR CONTINUED EXAMINATION

Sir:

In response to the Final Office Action dated 27 September 2018, the Advisory Action dated 26 November 2018, and accompanying a *Request for Continued Examination*, Applicant requests consideration of the following amendments in the above-referenced application:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 10 of this paper.

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In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating ~~between and contacting~~ the first and second channel films at levels of data storage structures, the adjacent stacks being physically separated from each other; and

the data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips and between the tunneling layers and the first sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks, the discrete charge trapping elements disposed in the first recessed regions on the first sidewalls of the conductive strips.

2. (original) The memory device of claim 1, wherein the discrete charge trapping elements disposed in the first recessed regions are dielectric charge trapping elements.

3. (original) The memory device of claim 1, wherein the conductive strips in the stacks have second sidewalls opposite the first sidewalls recessed relative to the second

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sides of the insulating strips which define second recessed regions on the second sidewalls of the conductive strips; and

the data storage structures include discrete charge trapping elements disposed in the second recessed regions in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements in the second recessed regions and the second sidewalls of the conductive strips.

4. (original) The memory device of claim 3, wherein the discrete charge trapping elements disposed in the second recessed regions are dielectric charge trapping elements.

5. (original) The memory device of claim 1, wherein the dielectric material comprises a gap.

6. (original) The memory device of claim 1, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

7. (currently amended) A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks and having second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating ~~between and contacting~~ the first and second channel films at levels of data storage structures, the adjacent stacks being physically separated from each other; and

the data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel

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pillars, discrete charge trapping elements in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips, between the discrete charge trapping elements and the second sidewalls of the conductive strips, between the tunneling layers and the first sides of the insulating strips, and between the tunneling layers and the second sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks, the blocking layers continuous across and in contact with the second sides of the insulating strips vertically between adjacent conductive strips in the stacks, the discrete charge trapping elements disposed in the first recessed regions on the first sidewalls of the conductive strips and disposed in the second recessed regions on the second sidewalls of the conductive strips,

wherein the vertical channel pillars are arranged so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips.

8. (original) The memory device of claim 7, wherein the discrete charge trapping elements are dielectric charge trapping elements.

9. (original) The memory device of claim 7, wherein the dielectric material comprises a gap.

10. (original) The memory device of claim 7, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

11. (currently amended) A manufacturing method, comprising:

forming a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls;

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recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions, including forming blocking layers between tunneling layers and the first sides of the insulating strips in the stacks, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks, the adjacent stacks being physically separated from each other; and

depositing a dielectric material between the first and second channel films, the dielectric material physically separating ~~contacting~~ the first and second channel films on the sidewalls of the adjacent stacks at levels of the data storage structures.

12. (previously presented) The manufacturing method of claim 11, said forming the data storage structures comprising:

depositing the blocking layers over the first sidewalls of the conductive strips in the first recessed regions and over the first sides of the insulating strips in the stacks;

depositing charge trapping material over the blocking layers in the first recessed regions; and

depositing the tunneling layers over the charge trapping material in the first recessed regions and over the blocking layers over the first sides of the insulating strips in the stacks.

13. (original) The manufacturing method of claim 12, wherein the charge trapping material is dielectric charge trapping material.

14. (original) The manufacturing method of claim 12, comprising:

said depositing the blocking layers including depositing the blocking layers over the first sides of the insulating strips; and

said depositing the charge trapping material including depositing the charge trapping material over the blocking layers over the first sides of the insulating strips; and separating the charge trapping material between adjacent first recessed regions.

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15. (original) The manufacturing method of claim 14, said separating the charge trapping material including removing the charge trapping material over the blocking layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions.

16. (original) The manufacturing method of claim 11, comprising:

etching to isolate the data storage structures along the conductive strips, to form discrete charge trapping elements in contact with the tunneling layers and the blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips.

17. (original) The manufacturing method of claim 11, wherein the conductive strips in the stacks of conductive strips have second sidewalls opposite the first sidewalls, the manufacturing method comprising:

recessing the second sidewalls of the conductive strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks; and

forming the data storage structures in the second recessed regions.

18. (original) The manufacturing method of claim 17,

etching to isolate the first and second channel films and the dielectric material between the first and second channel films along the conductive strips, to form vertical channel pillars between the stacks, so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips.

19. (original) The manufacturing method of claim 11, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

20. (currently amended) A manufacturing method, comprising:

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forming a plurality of stacks of sacrificial strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the sacrificial strips in the stacks having first sidewalls;

recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions, including forming blocking layers between tunneling layers and the first sides of the insulating strips in the stacks, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks, the adjacent stacks being physically separated from each other;

depositing a dielectric material between the first and second channel films, the dielectric material physically separating ~~contacting~~ the first and second channel films on the sidewalls of the adjacent stacks at levels of the data storage structures; and

replacing the sacrificial strips in the stacks with a metal material.

21. (previously presented) The manufacturing method of claim 20, said forming the data storage structures comprising:

depositing the blocking layers over the first sidewalls of the sacrificial strips in the first recessed regions and over the first sides of the insulating strips in the stacks;

depositing charge trapping material over the blocking layers in the first recessed regions; and

depositing the tunneling layers over the charge trapping material in the first recessed regions and over the blocking layers over the first sides of the insulating strips in the stacks.

22. (original) The manufacturing method of claim 21, wherein the charge trapping material is dielectric charge trapping material.

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23. (original) The manufacturing method of claim 20, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

24. (original) The manufacturing method of claim 20, said replacing comprising:
etching the stacks to form a trench, exposing the sacrificial strips in the trench;
removing the sacrificial strips in the trench;
depositing the metal material in the trench; and
separating the metal material between the insulating strips in the trench.

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REMARKS

In the Final Office Action dated 27 September 2018, the Examiner reviewed claims 1-24 and rejected claims 1-24. In the Advisory Action dated 26 November 2018, the proposed amendments in the response filed 13 November 2018 to the Final Office Action were not entered. The present application is being examined under the first inventor to file provisions of the AIA.

Applicant has amended claims 1, 7, 11 and 20.

Claims 1-24 remain pending.

Each rejection is respectfully traversed below.

Claim Amendments

Applicant has amended claim 1 to recite "a dielectric material physically separating the first and second channel films at levels of data storage structures, the adjacent stacks being physically separated from each other;"

Support for the amendment can be found in Figures 9 and 10 of the present specification, which illustrate a dielectric material 930 physically separating the first and second channel films 910 and 920 at levels of data storage structures 510, for example, at a level indicated by the line A-A' in Figure 9. Figures 9 and 10 also illustrate the adjacent stacks being physically separated from each other. As shown in Figure 9, stack 210 includes conductive strips 211, 213, 215 and 217 alternating with insulating strips 212, 214, 216 and 218, and stack 220 includes conductive strips 221, 223, 225 and 227 alternating with insulating strips 222, 224, 226 and 228. As shown in Figure 10, a conductive strip 217 in the stack 210 is physically separated from a conductive strip 227 in the stack 220.

Applicant has made corresponding amendments in claims 7, 11 and 20. No new matter is added.

Rejection of Claims 1-4, 6, 11-17, 20-22 and 24 under 35 U.S.C. 103

Claims 1-4, 6, 11-17, 20-22 and 24 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No. 2016/0071861), in view of Alsmeier et al., (US Publication No. 2012/0001249).

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The Advisory Action dated 26 November 2018 cited a new reference Kim (US 2018/0182776)."

Claim 1

Claim 1 as amended includes the limitations

> "vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating the first and second channel films at levels of data storage structures, the adjacent stacks being physically separated from each other;"

Emphasis added.

Kim and Serov do not describe at least the quoted limitations, as explained below.

Regarding Kim, the Advisory Action dated 26 November 2018 asserted "See Paragraph 0105, Fig 14, 200 that describes a dielectric layer separating the first and second channel films."

Kim describes

> "A plurality of channels may be formed in the one hole in the one first gate electrode."

Abstract; emphasis added.

> **"[0019]** FIG. **5** is a plan view showing a second structure that is divided into a plurality of pieces in one channel hole;
> **[0105]** In a case where the second structure is divided into four pieces, each of the semiconductor pattern **150,** the first blocking pattern **160,** the charge storage pattern **170,** the tunnel insulation pattern **180,** the channel **200,** the filling pattern **210,** and the capping pattern **220** may be also divided into four pieces."

Paragraphs [0019, 0105].

Consequently, although in the plan view of FIG. 14 of Kim, the channel 200 is divided four pieces, the four pieces are formed in one channel hole in one first gate electrode, rather than each of the four pieces being formed on physically separated gate electrodes. In contrast, claim 1 requires "the adjacent stacks being physically separated from each other".

The Final Office Action dated 27 September 2018 asserts:

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"Regarding claim 1, Serov discloses a memory device, comprising: …

vertical channel pillars **Fig 9A-10, 601/602/62** disposed between the stacks, the vertical channel pillars having first **Fig 9A-10, 601** and second channel films **Fig 9A-10, 602** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 9A-10, 62** (Paragraph 0150) between and contacting the second channel film; …

Embodiment 1 (Fig 9B) of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first Fig 16B, 602 (left side of layer 62) and second channel films Fig 16B, 602 (right side of layer 62) disposed on adjacent stacks in the plurality of stacks and a dielectric material Fig 16B, 62 between and contacting the first Fig 16B, 602 (left side of layer 62) and second channel film Fig 16B, 602 (right side of layer 62);"

Pages 4-5, the Office Action; emphasis added.

For convenience, FIGs. 9B, 9C, 16A and 16B of Serov are reproduced below.

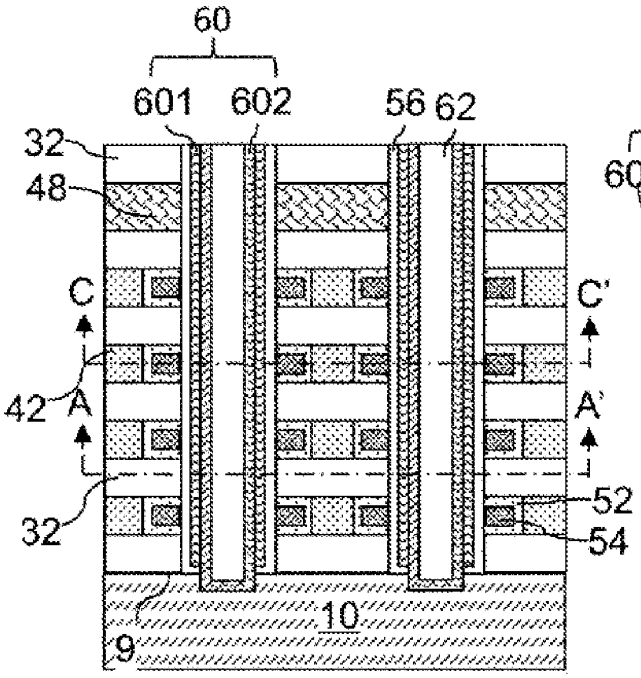


FIG. 9B

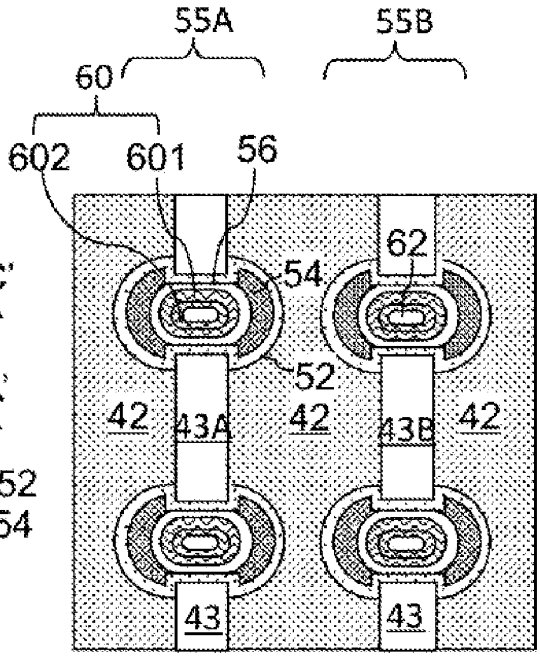


FIG. 9C

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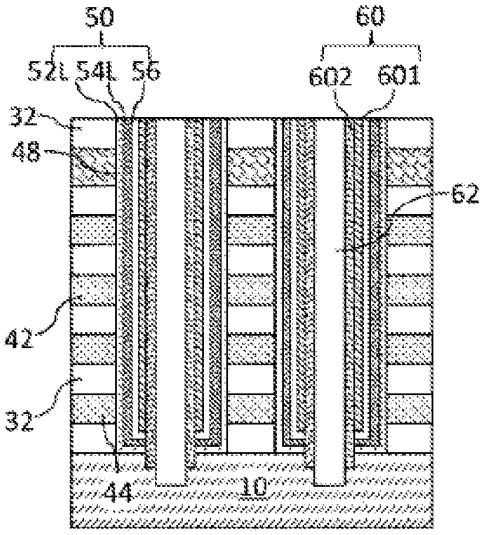


FIG. 16B

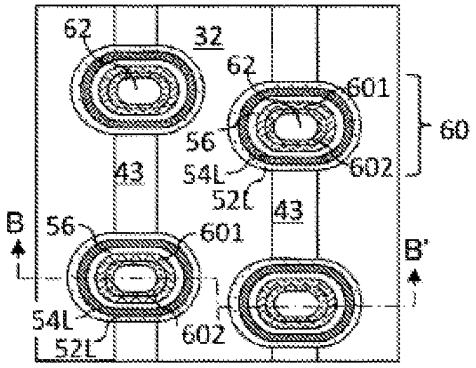


FIG. 16A

FIG. 9B is a vertical cross-sectional view of the first exemplary device structure for **Embodiment 1** (paragraphs [0030, 0031], Serov). FIG. 9C is a horizontal cross-sectional view taken along the horizontal plane C-C' of FIG. 9B (paragraph [0032], Serov).

FIG. 16A is a top-down view of the second exemplary device structure for **Embodiment 2** (paragraphs [0043], Serov). FIG. 16B is a vertical cross-sectional view of the second exemplary device structure for **Embodiment 2** taken along the vertical plane B-B' of FIG. 16A (paragraph [0044], Serov).

Regarding "the arrangement of the channel layers", both **Embodiment 1** (FIGs. 9B, 9C) and **Embodiment 2** (FIGs. 16A, 16B) show that "Each adjoining pair of a first semiconductor channel portion 601 and a second semiconductor channel portion 602 collectively constitutes a semiconductor channel 60…" (paragraph [0150], Serov).

Both FIGs. 9C and 16A show that "If a dielectric core 62 is present, the semiconductor channel 60 laterally surrounds the dielectric core 62" (paragraph [0155], Serov), where the semiconductor channel 60 includes a first semiconductor channel portion 601 and a second semiconductor channel portion 602.

One difference between the two embodiments is that in **Embodiment 1** (FIG. 9B) the second semiconductor channel portion 602 is formed on a top surface of a substrate 10, while in **Embodiment 2** (FIG. 16B) the second semiconductor channel portion 602 is not formed on a top surface of a substrate 10. The top surface of the substrate is located at the bottom of a memory

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opening 49 (FIG. 4B), in which the semiconductor channel 60 is formed (FIG. 9B). However, this difference does not change the arrangement common to both embodiments that "the semiconductor channel 60 laterally surrounds the dielectric core 62" (paragraph [0155], Serov).

Consequently, in FIG. 16B, a second semiconductor channel portion 602 shown at "left side of layer 62" and at "right side of layer 62" is the same semiconductor channel portion that laterally surrounds the dielectric core 62. Similarly, in FIG. 9B, a second semiconductor channel portion 602 shown at "left side of layer 62" and at "right side of layer 62" is the same semiconductor channel portion that laterally surrounds the dielectric core 62.

Therefore Serov describes a dielectric core 62 laterally surrounded by a second semiconductor channel portion 602, and the dielectric core 62 does NOT physically separate the second semiconductor channel portion 602. In contrast, claim 1 requires

> "vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating the first and second channel films at levels of data storage structures".

Since **Embodiment 1** and **Embodiment 2** both describe the dielectric core 62 laterally surrounded by a second semiconductor channel portion 602, it would not have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the **Embodiment 1** of Serov and incorporate the arrangement of **Embodiment 2** as an alternative channel arrangement, in order to reproduce the claimed invention.

Claim 1 should be allowable for at least the reasons explained above.

Claim 11

Claim 11 includes the limitations

> "forming first and second channel films on the data storage structures on sidewalls of adjacent stacks, the adjacent stacks being physically separated from each other; and
>
> depositing a dielectric material between the first and second channel films, the dielectric material physically separating the first and second channel films on the sidewalls of the adjacent stacks at levels of the data storage structures."

Emphasis added.

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Claim 11 is rejected with the same arguments as for the rejection of claim 1 (Pages 4-5, the Office Action), citing **Embodiment 1** (FIG. 9B) and **Embodiment 2** (FIG 16B) of Serov (Page 9, the Office Action).

Claim 11 should be allowable for at least the same reasons as explained for claim 1.

Claim 20

Claim 20 includes the limitations

"forming first and second channel films on the data storage structures on sidewalls of adjacent stacks, the adjacent stacks being physically separated from each other;

depositing a dielectric material between the first and second channel films, the dielectric material physically separating the first and second channel films on the sidewalls of the adjacent stacks at levels of the data storage structures;"

Emphasis added.

Claim 20 is rejected with the same arguments as for the rejection of claim 1 (Pages 4-5, the Office Action), citing **Embodiment 1** (FIG. 9B) and **Embodiment 2** (FIG 16B) of Serov (Pages 12-13, the Office Action).

Claim 20 should be allowable for at least the same reasons as explained for claim 1.

Claims 2-4 and 6 depend from claim 1, and should be allowable for at least the same reasons as explained for claim 1, and because of the unique combinations recited.

Claims 12-17 depend from claim 11, and should be allowable for at least the same reasons as explained for claim 11, and because of the unique combinations recited.

Claims 21-22 and 24 depend from claim 20, and should be allowable for at least the same reasons as explained for claim 20, and because of the unique combinations recited.

Accordingly reconsideration of the rejection of claims 1-4, 6, 11-17, 20-22 and 24 as amended under 35 U.S.C. § 103 is respectfully requested.

Rejection of Claims 5, 7-10, 18-19 and 23 under 35 U.S.C. 103

Claims 5, 7-10, 18-19, 23 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861) in view of Liu et al (US Publication No. 2016/0204117) and Alsmeier et al., (US Publication No. 2012/0001249).

Claim 7 includes the limitations

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"vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating the first and second channel films at levels of data storage structures, the adjacent stacks being physically separated from each other;"

Emphasis added; emphasis added.

Claim 7 is rejected with the same arguments as for the rejection of claim 1 (Pages 4-5, the Office Action), and should be allowable for at least the same reasons as explained for claim 1.

Claim 5 depends from claim 1, and should be allowable for at least the same reasons as explained for claim 1, and because of the unique combinations recited.

Claims 8-10 depend from claim 7, and should be allowable for at least the same reasons as explained for claim 7, and because of the unique combinations recited.

Claims 18-19 depend from claim 11, and should be allowable for at least the same reasons as explained for claim 11, and because of the unique combinations recited.

Claim 23 depends from claim 20, and should be allowable for at least the same reasons as explained for claim 20, and because of the unique combinations recited.

Accordingly reconsideration of the rejection of claims 5, 7-10, 18-19, 23 as amended under 35 U.S.C. § 103 is respectfully requested.

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CONCLUSION

It is respectfully submitted that this application is now in condition for allowance.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 2194-1).

Respectfully submitted,

Dated: 14 December 2018

/Yiding Wu/

Yiding Wu, Reg. No. 65,992

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/410,965	01/20/2017	HANG-TING LUE	MXIC 2194-1	3219

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EXAMINER	
ENAD, CHRISTINE A	

ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
01/18/2019	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

docket@hmbay.com

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Office Action Summary	Application No. 15/410,965	Applicant(s) LUE, HANG-TING	
	Examiner CHRISTINE A ENAD	Art Unit 2823	AIA Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 12/14/2018.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-24 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-24 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

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DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on **12/14/2018** has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6, 11-17, 20-22, 24 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861) in view of Alsmeier et al (US Publication No. 2012/0001249) and Kim (US Publication No. 2018/0182776).

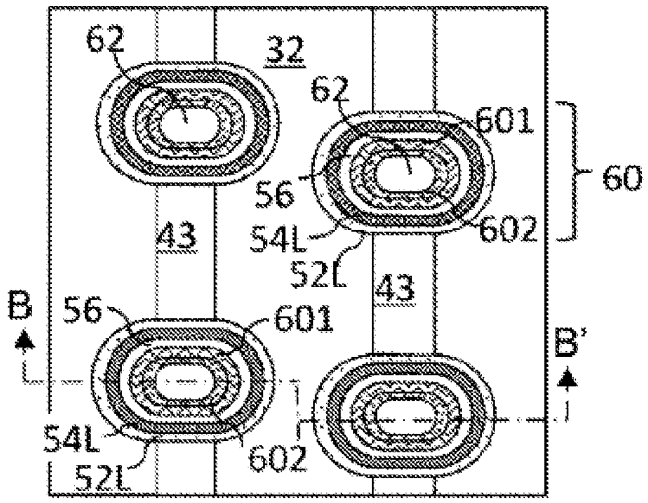


FIG. 16A

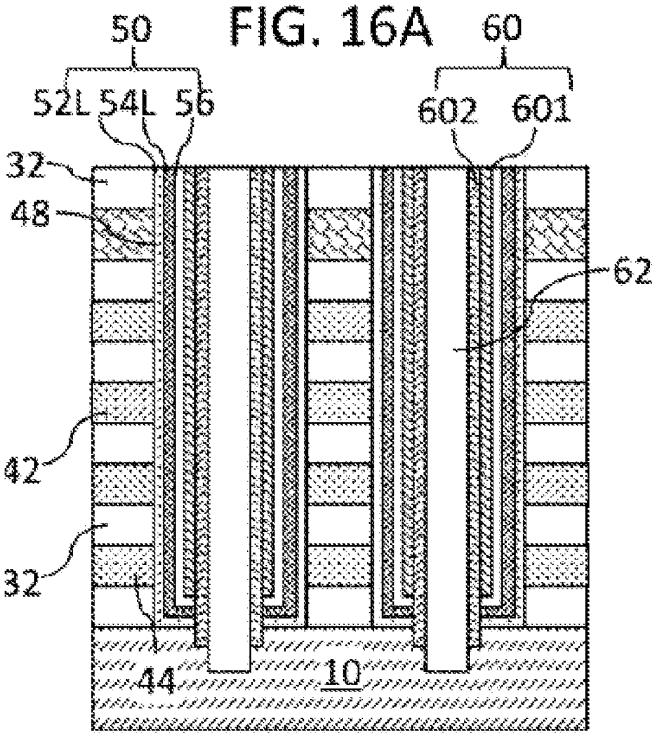


FIG. 16B

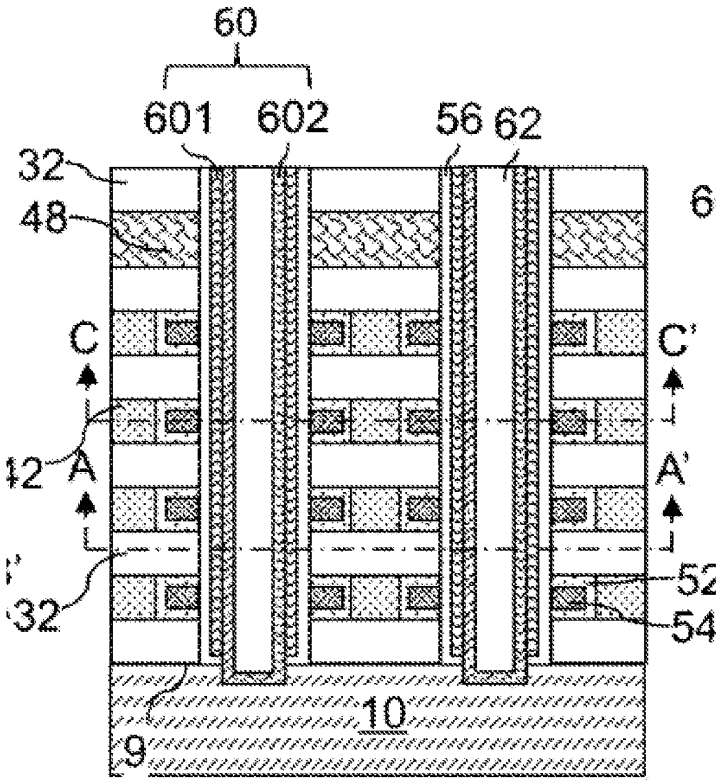


FIG. 9B

Regarding claim 1, Serov discloses a memory device, comprising: a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips alternating with insulating strips **Fig 9A-10, 32**, the insulating strips in the stacks having first and second sides, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks **Fig 9A-10**; vertical channel pillars **Fig 9A-10, 601/602/62** disposed

between the stacks, the vertical channel pillars having first **Fig 9A-10, 601** and second channel films **Fig 9A-10, 602** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 9A-10, 62** (Paragraph 0150) between and contacting the second channel film; and data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips **Fig 9A-10, (42/46)** in the stacks, the data storage structures including tunneling layers **Fig 9A-10, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56**, and blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips, the discrete charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions on the first sidewalls of the conductive strips **Fig 9A-10**. **Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B, 62** between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig 16B, 602 (right side of layer 62)** ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 16B, 54** in contact with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to

modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement. Serov also discloses having the adjacent stacks being physically separated from each other **Fig 20.**

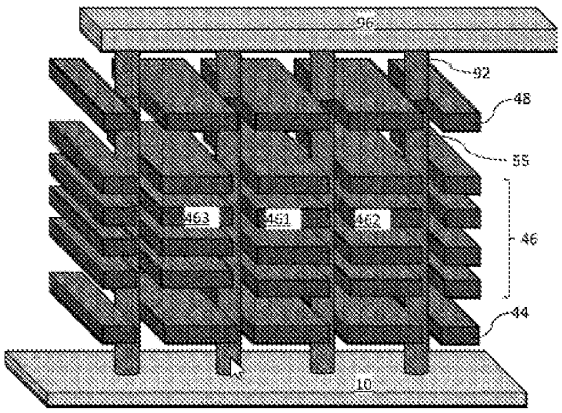


FIG. 20

Serov discloses all the limitations except for the arrangement of the blocking layer relative to the insulating strips.

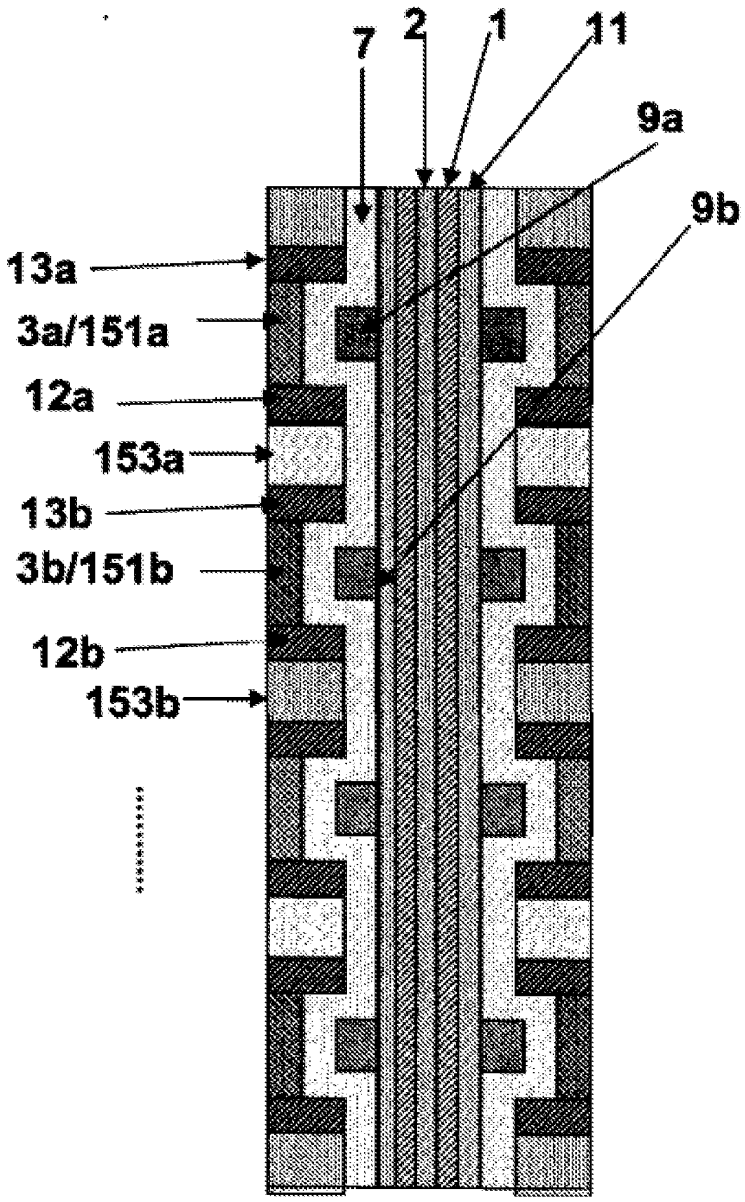


Figure 49

Whereas Alsmeier discloses data storage structures **Fig 49** at cross points of the vertical channel pillars **Fig 49, 2** between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers **Fig 49, 11** in contact with the channel film in the vertical channel pillars, discrete charge trapping elements **Fig 49,**

9 in contact with the tunneling layers **Fig 49, 11** and blocking layers **Fig 49, 7** between the discrete charge trapping elements **Fig 49, 9** and the first sidewalls of the conductive strips **Fig 49, 151** and between the tunneling layers **Fig 49, 11** and the first sides of the insulating strips **Fig 49, 153** the blocking layers **Fig 49, 7** continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks **Fig 43-51.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the layer arrangement of Serov and incorporate the arrangement of Alsmeier as an alternative arrangement to improve device performance. Serov and Alsmeier disclose all the limitations but silent on the dielectric layer separating the first and second channel region.

Whereas Kim discloses a dielectric material physically separating the first and second channel regions **Fig 18, 240 and Fig 19-20.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the arrangement of Serov and incorporate the arrangement of Kim as an alternative arrangement to improve device performance (Paragraph 0014).

Regarding claim 2, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions are dielectric charge trapping elements (Paragraph 0143).

Regarding claim 3, Serov discloses the conductive strips in the stacks have second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions on the second sidewalls of

the conductive strips; and the data storage structures include discrete charge trapping elements disposed in the second recessed regions in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements in the second recessed regions and the second sidewalls of the conductive strips **Fig 9A-10.**

Regarding claim 4, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** disposed in the second recessed regions are dielectric charge trapping elements (Paragraph 0043).

Regarding claim 6, Serov discloses the conductive strips in the plurality of stacks of conductive strips include a metal material (Paragraph 0133).

Regarding claim 11, Serov discloses a manufacturing method, comprising: forming a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips **Fig 9A-10, (42/46)** alternating with insulating strips **Fig 9A-10, 32**, the insulating strips **Fig 9A-10, 32**in the stacks having first and second sides **Fig 9A-10**, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls; recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks **Fig 5A-5C;** forming data storage structures in the first recessed regions **Fig 6A-8C;** forming first and second channel films **Fig 9A-10, 60** on the data storage structures on sidewalls of adjacent stacks; and depositing a dielectric material **Fig 9A-10, 62** between the first and second channel films, the dielectric material contacting the second channel films on the sidewalls of the adjacent stacks **Fig 9A-10**. **Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B,**

602 disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B, 62** between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig 16B, 602 (right side of layer 62)** ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 16B, 54** in contact with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement. Serov also discloses having the adjacent stacks being physically separated from each other **Fig 20.**

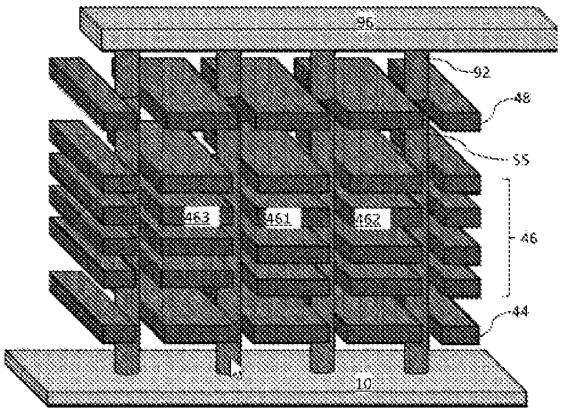


FIG. 20

Serov discloses all the limitations except for the arrangement of the blocking layer relative to the insulating strips.

Whereas Alsmeier discloses data storage structures **Fig 49** at cross points of the vertical channel pillars **Fig 49, 2** between the stacks and the conductive strips in the

stacks, the data storage structures including tunneling layers **Fig 49, 11** in contact with the channel film in the vertical channel pillars, discrete charge trapping elements **Fig 49, 9** in contact with the tunneling layers **Fig 49, 11** and blocking layers **Fig 49, 7** between the discrete charge trapping elements **Fig 49, 9** and the first sidewalls of the conductive strips **Fig 49, 151** and between the tunneling layers **Fig 49, 11** and the first sides of the insulating strips **Fig 49, 153** the blocking layers **Fig 49, 7** continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks **Fig 43-51.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the layer arrangement of Serov and incorporate the arrangement of Alsmeier as an alternative arrangement to improve device performance. Serov and Alsmeier disclose all the limitations but silent on the dielectric layer separating the first and second channel region.

Whereas Kim discloses a dielectric material physically separating the first and second channel regions **Fig 18, 240 and Fig 19-20.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the arrangement of Serov and incorporate the arrangement of Kim as an alternative arrangement to improve device performance (Paragraph 0014).

Regarding claim 12, Serov and Alsmeier disclose said forming the data storage structures comprising: depositing blocking layers **Fig 9A-10, 52** over the first sidewalls of the conductive strips in the first recessed regions; depositing charge trapping material

Fig 9A-10, 54 over the blocking layers **Fig 9A-10, 52** in the first recessed regions; and depositing tunneling layers **Fig 9A-10, 56** over the charge trapping material **Fig 9A-10, 54** in the first recessed regions (Serov- **Fig 9A-10;** Alsmeier-**Fig 43-51**).

Regarding claim 13, Serov discloses wherein the charge trapping material is dielectric charge trapping material (Paragraph 0143).

Regarding claim 14, Serov discloses comprising: said depositing the blocking layers **Fig 9A-10, 52** including depositing the blocking layers **Fig 9A-10, 52** over the first sides of the insulating strips **Fig 6B**; and said depositing the charge trapping material **Fig 9A-10, 54** including depositing the charge trapping material **Fig 9A-10, 52** over the blocking layers **Fig 6B** over the first sides of the insulating strips **Fig 6B**; and separating the charge trapping material between adjacent first recessed regions **Fig 6A-6C.**

Regarding claim 15, Serov discloses said separating the charge trapping material **Fig 9A-10, 54** including removing the charge trapping material over the blocking layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions **Fig 6A-8C.**

Regarding claim 16, Serov discloses comprising: etching to isolate the data storage structures along the conductive strips, to form discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56** and the blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips.

Regarding claim 17, Serov discloses wherein the conductive strips in the stacks of conductive strips have second sidewalls opposite the first sidewalls **Fig 9A-10**, the

manufacturing method comprising: recessing the second sidewalls of the conductive strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks; and forming the data storage structures in the second recessed regions **Fig 5A-10.**

Regarding claim 20, Serov discloses a manufacturing method, comprising: forming a plurality of stacks **Fig 9A-10, 32/(42/46)** of sacrificial strips **Fig 9A-10, 42** alternating with insulating strips **Fig 9A-10, 32**, the insulating strips **Fig 9A-10, 32**in the stacks having first and second sides **Fig 9A-10**, and the sacrificial strips **Fig 9A-10, 42** in the stacks having first sidewalls; recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks **Fig 5A-5C;** forming data storage structures in the first recessed regions **Fig 6A-8C;** forming first and second channel films **Fig 9A-10, 60** on the data storage structures on sidewalls of adjacent stacks; and depositing a dielectric material **Fig 9A-10, 62** between the first and second channel films, the dielectric material contacting the second channel films on the sidewalls of the adjacent stacks **Fig 9A-10**, and replacing the sacrificial strips in the stacks with a metal material **Fig 10, 46. Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B, 62** between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig**

16B, 602 (right side of layer 62) ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 16B, 54** in contact with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement. Serov also discloses having the adjacent stacks being physically separated from each other **Fig 20.**

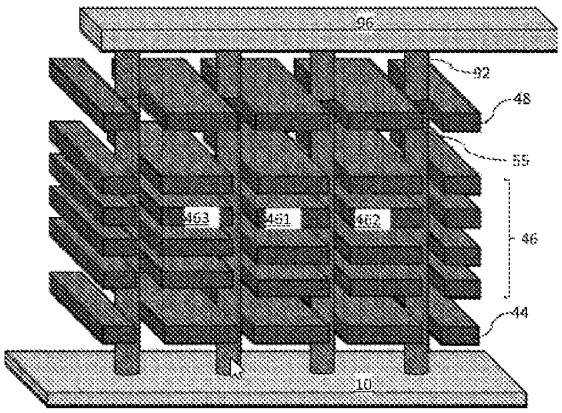


FIG. 20

Serov discloses all the limitations except for the arrangement of the blocking layer relative to the insulating strips.

Whereas Alsmeier discloses data storage structures **Fig 49** at cross points of the vertical channel pillars **Fig 49, 2** between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers **Fig 49, 11** in contact with the channel film in the vertical channel pillars, discrete charge trapping elements **Fig 49, 9** in contact with the tunneling layers **Fig 49, 11** and blocking layers **Fig 49, 7** between

the discrete charge trapping elements **Fig 49, 9** and the first sidewalls of the conductive strips **Fig 49, 151** and between the tunneling layers **Fig 49, 11** and the first sides of the insulating strips **Fig 49, 153** the blocking layers **Fig 49, 7** continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks **Fig 43-51.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the layer arrangement of Serov and incorporate the arrangement of Alsmeier as an alternative arrangement to improve device performance. Serov and Alsmeier disclose all the limitations but silent on the dielectric layer separating the first and second channel region.

Whereas Kim discloses a dielectric material physically separating the first and second channel regions **Fig 18, 240 and Fig 19-20.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the arrangement of Serov and incorporate the arrangement of Kim as an alternative arrangement to improve device performance (Paragraph 0014).

Regarding claim 21, Serov and Alsmeier discloses said forming the data storage structures comprising: depositing blocking layers **Fig 9A-10, 52** over the first sidewalls of the conductive strips in the first recessed regions; depositing charge trapping material **Fig 9A-10, 54** over the blocking layers **Fig 9A-10, 52** in the first recessed regions; and depositing tunneling layers **Fig 9A-10, 56** over the charge trapping material **Fig 9A-10, 54** in the first recessed regions (Serov- **Fig 9A-10;** Alsmeier-**Fig 43-51**).

Regarding claim 22, Serov discloses wherein the charge trapping material is dielectric charge trapping material (Paragraph 0143).

Regarding claim 24, Serov discloses said replacing comprising: etching the stacks to form a trench, exposing the sacrificial strips in the trench; removing the sacrificial strips in the trench; depositing the metal material in the trench; and separating the metal material between the insulating strips in the trench (Paragraph 0152-0154).

Claims 5, 7-10, 18-19, 23 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861) in view of Liu et al (US Publication No. 2016/0204117), Alsmeier et al (US Publication No. 2012/0001249) and Kim (US Publication No. 2018/0182776).

Regarding claims, 5, 19, and 23, Serov discloses all the limitations except for the gap in the channel region. Whereas Liu discloses leaving a gap between the first and second vertical channel films **Fig 2A-4B** (Paragraph 0075-0076). Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the device of Serov and incorporate a gap to provide a connector between device levels.

Regarding claim 7, Serov discloses a memory device, comprising: a plurality of stacks **Fig 9A-10, 32/(42/46)** of conductive strips alternating with insulating strips **Fig 9A-10, 32**, the insulating strips in the stacks having first and second sides, and the conductive strips **Fig 9A-10, (42/46)** in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks **Fig 9A-10;** and having second sidewall opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions in sides of the stacks **Fig 9A-10;** vertical channel pillars **Fig 9A-10, 601/602/62** disposed between the stacks, the vertical channel pillars having first **Fig 9A-**

10, 601 and second channel films **Fig 9A-10, 602** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 9A-10, 62** (Paragraph 0150) between and contacting the second channel films; and data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips **Fig 9A-10, (42/46)** in the stacks, the data storage structures including tunneling layers **Fig 9A-10, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 9A-10, 54** in contact with the tunneling layers **Fig 9A-10, 56**, and blocking layers **Fig 9A-10, 52** between the discrete charge trapping elements **Fig 9A-10, 54** and the first sidewalls of the conductive strips and between the discrete charge trapping elements and the second sidewalls of the conductive strips **Fig 9A-10**, the discrete charge trapping elements **Fig 9A-10, 54** disposed in the first recessed regions on the first sidewalls of the conductive strips and disposed in the second recessed regions on the second sidewalls of the conductive strips **Fig 9A-10.** Serov discloses all the limitations except for the offset in the channel region.

Whereas Liu discloses the vertical channel pillars are arranged so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips **Fig 2A-4B** (Paragraph 0075-0076). Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the device of Serov and incorporate an offset to provide a connector between device levels. **Embodiment 1 (Fig 9B**) of Serov discloses all the limitations except for the arrangement of the channel layers.

Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first **Fig 16B, 602 (left side of layer 62)** and second channel films **Fig 16B, 602 (right side of layer 62)** disposed on adjacent stacks in the plurality of stacks and a dielectric material **Fig 16B, 62** between and contacting the first **Fig 16B, 602 (left side of layer 62)** and second channel film **Fig 16B, 602 (right side of layer 62)** ; the data storage structures including tunneling layers **Fig 16B, 56** in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements **Fig 16B, 54** in contact with the tunneling layers **Fig 16B, 56.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the Embodiment 1 of Serov and incorporate the arrangement of Embodiment 2 as an alternative channel arrangement. Serov also discloses having the adjacent stacks being physically separated from each other **Fig 20.**

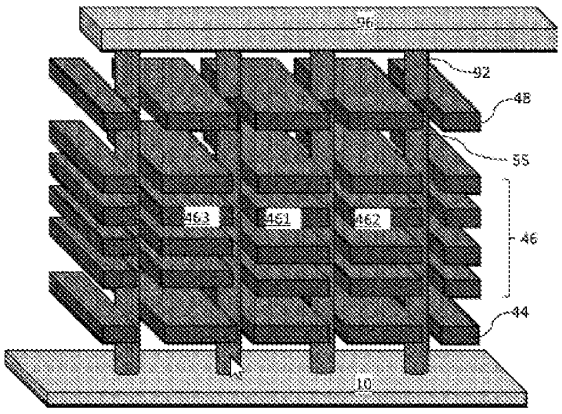


FIG. 20

Serov and Liu discloses all the limitations except for the arrangement of the blocking layer relative to the insulating strips.

Whereas Alsmeier discloses data storage structures **Fig 49** at cross points of the vertical channel pillars **Fig 49, 2** between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers **Fig 49, 11** in contact with the channel film in the vertical channel pillars, discrete charge trapping elements **Fig 49, 9** in contact with the tunneling layers **Fig 49, 11** and blocking layers **Fig 49, 7** between the discrete charge trapping elements **Fig 49, 9** and the first sidewalls of the conductive strips **Fig 49, 151,** between the discrete charge trapping elements and the second sidewalls of the conductive strips **Fig 49**, between the tunneling layers **Fig 49, 11** and the first sides of the insulating strips **Fig 49, 153** and between the tunneling layers and the second sides of the insulating strips **Fig 49,** the blocking layers **Fig 49, 7** continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks **Fig 43-51,** the blocking layers continuous across and in contact with the second sides of the insulating strips vertically between adjacent conductive strips in the stacks **Fig 43-51.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the layer arrangement of Serov and incorporate the arrangement of Alsmeier as an alternative arrangement to improve device performance.

Serov, Liu and Alsmeier disclose all the limitations but silent on the dielectric layer separating the first and second channel region.

Whereas Kim discloses a dielectric material physically separating the first and second channel regions **Fig 18, 240 and Fig 19-20.** Therefore it would have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the arrangement of Serov and incorporate the arrangement of Kim as an alternative arrangement to improve device performance (Paragraph 0014).

Regarding claim 8, Serov discloses wherein the discrete charge trapping elements **Fig 9A-10, 54** are dielectric charge trapping elements (Paragraph 0143).

Regarding claim 9, Serov discloses wherein the dielectric material comprises a gap **Fig 2A-4B** (Paragraph 0075-0076).

Regarding claim 10, Serov discloses the conductive strips in the plurality of stacks of conductive strips include a metal material (Paragraph 0133).

Regarding claim 18, Liu discloses etching to isolate the first and second channel films and the dielectric material between the first and second channel films along the conductive strips, to form vertical channel pillars between the stacks, so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips **Fig 2A-4B** (Paragraph 0075-0076).

Response to Arguments

Applicant's arguments filed 12/14/2018 have been fully considered but they are not persuasive.

In response to applicant's argument on Page 10 that the references fail to show certain features of applicant's invention, it is noted that the features upon which

applicant relies (i.e, four channels should not be formed in one get electrode) are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to CHRISTINE A ENAD whose telephone number is (571)270-7891. The examiner can normally be reached on Monday-Friday, 7:30 am - 4:30 pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Allen Parker can be reached on 303 297 4722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/CHRISTINE A ENAD/
Primary Examiner, Art Unit 2823

Notice of References Cited	Application/Control No. 15/410,965	Applicant(s)/Patent Under Reexamination LUE, HANG-TING	
	Examiner CHRISTINE A ENAD	Art Unit 2823	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20180182776-A1	06-2018	Kim; Chan-Ho	H01L27/11582	1/1
*	B	US-9401371-B1	07-2016	Lee; Guan-Ru	H01L27/11582	1/1
*	C	US-9147468-B1	09-2015	Lue; Hang-Ting	G11C11/5671	1/1
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	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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	Examiner	Art Unit
	CHRISTINE A ENAD	2823

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	11/24/2017	05/21/2018	09/18/2018	01/14/2019					
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	2	✓	✓	✓	✓					
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	9	✓	✓	✓	✓					
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	23	✓	✓	✓	✓					
	24	✓	✓	✓	✓					

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CPC - Searched*		
Symbol	Date	Examiner
H01L27/11582	11/24/2017	CE
H01L21/76802, 21/76877	11/24/2017	CE
H01L23/5226, 23/528	11/24/2017	CE

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Assignee and inventor search conducted	11/24/2017	CE
CPC search	11/24/2017	CE
EAST Search	11/24/2017	CE
EAST Search	5/21/2018	CE
EAST Search	9/18/2018	CE
EAST Search	01/14/2019	CE

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/CHRISTINE ENAD/ Primary Examiner.Art Unit 2823	

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	Examiner	Art Unit
	CHRISTINE A ENAD	2823

/CHRISTINE ENAD/ Primary Examiner.Art Unit 2823	

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	574	(("MACRONIX") near3 ("INTERNATIONAL") near3 ("CO") near3 ("LTD")).AANM.	USPAT	OR	OFF	2017/11/22 09:51
S2	358	(("LUE") near3 ("HANG-TING")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 09:51
S3	9877	(H01L27/11582.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:51
S4	13188	(H01L21/76802.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:51
S5	17402	(H01L21/76877.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S6	15471	(H01L23/5226.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S7	13459	(H01L23/528.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S8	20	(vertical near stack) and ((insulating or dielectric or insulation) near channel)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 10:17
S9	0	("2017/0243879").URPN.	USPAT	OR	OFF	2017/11/22 10:21

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S10	28	("20070029607" | "20090230454" | "20100207194" | "20100213527" | "20110156044" | "20120012921" | "20120326221" | "20140131784" | "20150044833" | "20150076584" | "20150179660" | "20150255481" | "20150371709" | "20160133642" | "5915167" | "7575973" | "7906392" | "8084819" | "8187936" | "8461641" | "8610194" | "8735962" | "8767465" | "8823076" | "8853765" | "8981457" | "8987119" | "9023719").PN. OR ("9728546").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 10:25
S11	328	((insulating or dielectric or insulation) near channel)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 12:35
S12	0	((insulating or dielectric or insulation) near channel near gap)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S13	10	((insulating or dielectric or insulation) near channel near gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S14	346	((insulating or dielectric or insulation) near channel same gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S15	1065	((insulating or dielectric or insulation) same channel same gap)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 18:00
S16	4	("20120001249").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:05
S17	2	("20160181271").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:07

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S18	8	(("20130049095") or ("20100181612") or ("20130100741")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:07
S19	51	((insulating or dielectric or insulation) same channel NEAR (SEPARATION OR gap or void))and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 18:52
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S22	32	((insulating or dielectric or insulation) same channel NEAR (seam or hollow))and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 19:02
S23	2	("20160204117").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/24 13:25
S24	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/05/14 11:31
S25	39484	((insulating or dielectric or insulation) same channel)and (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/05/14 12:11
S26	19502	((insulating or dielectric or insulation) same channel)same (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2018/05/14 12:11

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			EPO; JPO; DERWENT; IBM_TDB			
S27	305	((insulating or dielectric or insulation) same channel)near (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/05/14 12:13
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S29	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/08/23 12:43
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S31	1	("20180211969").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:18
S32	0	("2017/0194340").URPN.	USPAT	OR	OFF	2018/09/18 09:35
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S37	1765	(blocking same tunneling same channel) and (memory near device)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:59
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S45	8	("20130270631" | "20140141583" | "20150115344" | "20160148946" | "20160181264" | "9130054" | "9171729" | "9305937").PN. OR ("9576972").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 16:46
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S48	772	second near vertical near channel	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 16:59
S49	32426	memory and pillar	US-PGPUB;	OR	OFF	2018/11/19

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S50	303	S47 and S49	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 17:00
S51	1	("20180211969").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/01/14 09:56
S52	1	("20180182776").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/01/14 09:56
S53	2	(("20160071861") or ("20120001249")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/01/14 12:50

1/14/2019 5:24:28 PM
C:\Users\cenad\Documents\EAST\Workspaces\15410965.wsp

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PTO/SB/06 (09-11)
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/410,965	Filing Date 01/20/2017	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)		
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	12/14/2018	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 24	Minus	** 24	= 0	X $100 =	0
	Independent (37 CFR 1.16(h))	* 4	Minus	***4	= 0	X $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SLIE
LISA FULTON

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Application	Document	Mailroom Date	Attorney Docket No.
15410965	CTNF	01/18/2019	MXIC 2194-1
	892	01/18/2019	MXIC 2194-1

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PATENT APPLICATION INFORMATION RETRIEVAL SYSTEM

Electronic Patent Application Fee Transmittal

Application Number:	15410965
Filing Date:	20-Jan-2017
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	HANG-TING LUE
Filer:	Yiding Wu/Amy Jonsson
Attorney Docket Number:	MXIC 2194-1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	1202	1	100	100
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

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Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		100

Electronic Acknowledgement Receipt

EFS ID:	35766774
Application Number:	15410965
International Application Number:	
Confirmation Number:	3219
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	HANG-TING LUE
Customer Number:	46353
Filer:	Yiding Wu/Amy Jonsson
Filer Authorized By:	Yiding Wu
Attorney Docket Number:	MXIC 2194-1
Receipt Date:	18-APR-2019
Filing Date:	20-JAN-2017
Time Stamp:	14:51:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$100
RAM confirmation Number	041919INTEFSW14521600
Deposit Account	
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The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Req. Reconsideration-After Non-Final Reject	00693205.PDF	264119 b62f5d825b1601b78a4bfdedfe30f3f7fd62d357	no	17
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30222 a5283e3e8b4e113322401d72ea0c7cc829c74eed	no	2
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Amy Jonsson

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of inventor(s):
Hang-Ting Lue

Application No. **15/410,965**

Confirmation No. **3219**

Filing Date: **20 January 2017**

Title: **DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE**

Group Art Unit: **2823**

Examiner: **Christine A Enad**

CUSTOMER NO. 46353

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AMENDMENT AND RESPONSE

Sir:

In response to the Non-Final Office Action dated 18 January 2019, Applicant requests consideration of the following amendments in the above-referenced application:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 9 of this paper.

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In the claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating the first and second channel films at levels of data storage structures, the adjacent stacks being physically separated from each other; [[and]]

the data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips and between the tunneling layers and the first sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks, the discrete charge trapping elements disposed in the first recessed regions on the first sidewalls of the conductive strips; and

insulating structures disposed between and in contact with adjacent conductive strips, the conductive strips extending in a first direction, the insulating structures having a width in a second direction orthogonal to the first direction, wherein the data storage structures are disposed within the width between adjacent conductive strips.

2. (original) The memory device of claim 1, wherein the discrete charge trapping elements disposed in the first recessed regions are dielectric charge trapping elements.

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3. (original) The memory device of claim 1, wherein the conductive strips in the stacks have second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions on the second sidewalls of the conductive strips; and

the data storage structures include discrete charge trapping elements disposed in the second recessed regions in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements in the second recessed regions and the second sidewalls of the conductive strips.

4. (original) The memory device of claim 3, wherein the discrete charge trapping elements disposed in the second recessed regions are dielectric charge trapping elements.

5. (original) The memory device of claim 1, wherein the dielectric material comprises a gap.

6. (original) The memory device of claim 1, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

7. (currently amended) A memory device, comprising:

a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls recessed relative to the first sides of the insulating strips which define first recessed regions in sides of the stacks and having second sidewalls opposite the first sidewalls recessed relative to the second sides of the insulating strips which define second recessed regions in sides of the stacks;

vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating the first and second channel films at levels of data storage structures, the adjacent stacks being physically separated from each other; [[and]]

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the data storage structures at cross points of the vertical channel pillars between the stacks and the conductive strips in the stacks, the data storage structures including tunneling layers in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements in contact with the tunneling layers, and blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips, between the discrete charge trapping elements and the second sidewalls of the conductive strips, between the tunneling layers and the first sides of the insulating strips, and between the tunneling layers and the second sides of the insulating strips, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips in the stacks, the blocking layers continuous across and in contact with the second sides of the insulating strips vertically between adjacent conductive strips in the stacks, the discrete charge trapping elements disposed in the first recessed regions on the first sidewalls of the conductive strips and disposed in the second recessed regions on the second sidewalls of the conductive strips,

wherein the vertical channel pillars are arranged so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips; and

insulating structures disposed between and in contact with adjacent conductive strips, the conductive strips extending in a first direction, the insulating structures having a width in a second direction orthogonal to the first direction, wherein the data storage structures are disposed within the width between adjacent conductive strips.

8. (original) The memory device of claim 7, wherein the discrete charge trapping elements are dielectric charge trapping elements.

9. (original) The memory device of claim 7, wherein the dielectric material comprises a gap.

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10. (original) The memory device of claim 7, wherein the conductive strips in the plurality of stacks of conductive strips include a metal material.

11. (currently amended) A manufacturing method, comprising:

forming a plurality of stacks of conductive strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the conductive strips in the stacks having first sidewalls;

recessing the first sidewalls of the conductive strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions, including forming blocking layers between tunneling layers and the first sides of the insulating strips in the stacks, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks, the adjacent stacks being physically separated from each other; [[and]]

depositing a dielectric material between the first and second channel films, the dielectric material physically separating the first and second channel films on the sidewalls of the adjacent stacks at levels of the data storage structures; and

forming insulating structures disposed between and in contact with adjacent conductive strips, the conductive strips extending in a first direction, the insulating structures having a width in a second direction orthogonal to the first direction, wherein the data storage structures are disposed within the width between adjacent conductive strips.

12. (previously presented) The manufacturing method of claim 11, said forming the data storage structures comprising:

depositing the blocking layers over the first sidewalls of the conductive strips in the first recessed regions and over the first sides of the insulating strips in the stacks;

depositing charge trapping material over the blocking layers in the first recessed regions; and

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depositing the tunneling layers over the charge trapping material in the first recessed regions and over the blocking layers over the first sides of the insulating strips in the stacks.

13. (original) The manufacturing method of claim 12, wherein the charge trapping material is dielectric charge trapping material.

14. (original) The manufacturing method of claim 12, comprising:

said depositing the blocking layers including depositing the blocking layers over the first sides of the insulating strips; and

said depositing the charge trapping material including depositing the charge trapping material over the blocking layers over the first sides of the insulating strips; and separating the charge trapping material between adjacent first recessed regions.

15. (original) The manufacturing method of claim 14, said separating the charge trapping material including removing the charge trapping material over the blocking layers over the first sides of the insulating strips, while keeping the charge trapping material in the first recessed regions.

16. (original) The manufacturing method of claim 11, comprising:

etching to isolate the data storage structures along the conductive strips, to form discrete charge trapping elements in contact with the tunneling layers and the blocking layers between the discrete charge trapping elements and the first sidewalls of the conductive strips.

17. (original) The manufacturing method of claim 11, wherein the conductive strips in the stacks of conductive strips have second sidewalls opposite the first sidewalls, the manufacturing method comprising:

recessing the second sidewalls of the conductive strips relative to the second sides of the insulating strips to define second recessed regions in sides of the stacks; and

forming the data storage structures in the second recessed regions.

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18. (original) The manufacturing method of claim 17,

etching to isolate the first and second channel films and the dielectric material between the first and second channel films along the conductive strips, to form vertical channel pillars between the stacks, so that a first row of the vertical channel pillars disposed on the first sidewalls of a particular stack of conductive strips is offset in a row direction from a second row of the vertical channel pillars disposed on the second sidewalls of the particular stack of conductive strips.

19. (original) The manufacturing method of claim 11, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

20. (currently amended) A manufacturing method, comprising:

forming a plurality of stacks of sacrificial strips alternating with insulating strips, the insulating strips in the stacks having first and second sides, and the sacrificial strips in the stacks having first sidewalls;

recessing the first sidewalls of the sacrificial strips relative to the first sides of the insulating strips to define first recessed regions in sides of the stacks;

forming data storage structures in the first recessed regions, including forming blocking layers between tunneling layers and the first sides of the insulating strips in the stacks, the blocking layers continuous across and in contact with the first sides of the insulating strips vertically between adjacent conductive strips;

forming first and second channel films on the data storage structures on sidewalls of adjacent stacks, the adjacent stacks being physically separated from each other;

depositing a dielectric material between the first and second channel films, the dielectric material physically separating the first and second channel films on the sidewalls of the adjacent stacks at levels of the data storage structures; [[and]]

replacing the sacrificial strips in the stacks with a metal material; and

forming insulating structures disposed between and in contact with adjacent conductive strips, the conductive strips extending in a first direction, the insulating structures having a width in a second direction orthogonal to the first direction, wherein

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the data storage structures are disposed within the width between adjacent conductive strips.

21. (previously presented) The manufacturing method of claim 20, said forming the data storage structures comprising:

depositing the blocking layers over the first sidewalls of the sacrificial strips in the first recessed regions and over the first sides of the insulating strips in the stacks;

depositing charge trapping material over the blocking layers in the first recessed regions; and

depositing the tunneling layers over the charge trapping material in the first recessed regions and over the blocking layers over the first sides of the insulating strips in the stacks.

22. (original) The manufacturing method of claim 21, wherein the charge trapping material is dielectric charge trapping material.

23. (original) The manufacturing method of claim 20, said depositing a dielectric material between the first and second channel films including leaving a gap between the first and second vertical channel films.

24. (original) The manufacturing method of claim 20, said replacing comprising:

etching the stacks to form a trench, exposing the sacrificial strips in the trench;

removing the sacrificial strips in the trench;

depositing the metal material in the trench; and

separating the metal material between the insulating strips in the trench.

25. (new) The memory device of claim 1, wherein the first sidewalls of the conductive strips in the stacks are straight, and the vertical channel pillars disposed between the stacks are parallel to the first sidewalls.

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REMARKS

In the Non-Final Office Action dated 18 January 2019, the Examiner reviewed claims 1-24 and rejected claims 1-24. The present application is being examined under the first inventor to file provisions of the AIA.

Applicant has amended claims 1, 7, 11 and 20, and added a new claim 25.

Claims 1-25 remain pending.

Each rejection is respectfully traversed below.

Claim Amendments

Applicant has amended claim 1 to recite

"insulating structures disposed between and in contact with adjacent conductive strips, the conductive strips extending in a first direction, the insulating structures having a width in a second direction orthogonal to the first direction, wherein the data storage structures are disposed within the width between adjacent conductive strips."

Support for the amendment can be found in Figure 10 of the present specification. Figure 10 illustrates insulating structures (1001-1009, FIG. 10) disposed between and in contact with adjacent conductive strips (217, 227), the conductive strips extending in a first direction (X-direction), the insulating structures having a width in a second direction (Y-direction) orthogonal to the first direction, wherein the data storage structures (1010) are disposed within the width between adjacent conductive strips.

Applicant has made corresponding amendments in claims 7, 11 and 20. No new matter is added.

Figure 10 is reproduced below, annotated with "width" for the width of the insulating structures in the Y-direction.

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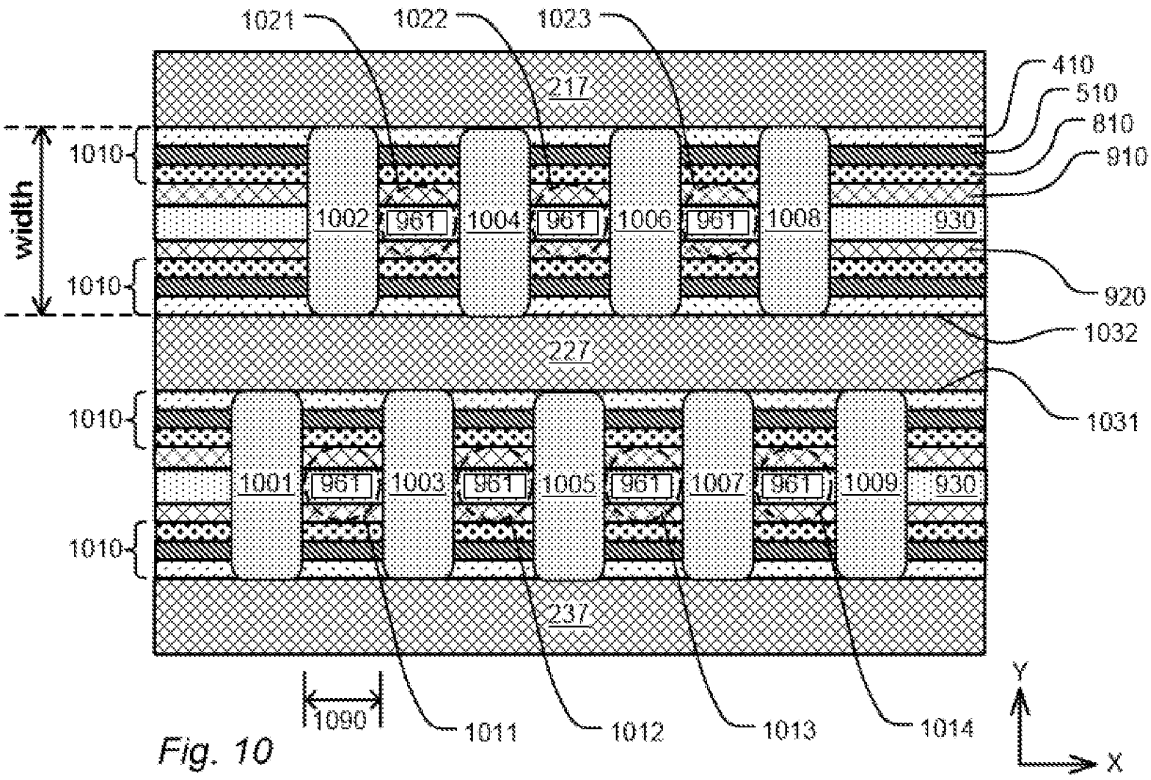


Fig. 10

Rejection of Claims 1-4, 6, 11-17, 20-22 and 24 under 35 U.S.C. 103

Claims 1-4, 6, 11-17, 20-22 and 24 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No. 2016/0071861), in view of Alsmeier et al., (US Publication No. 2012/0001249) and Kim (US Publication No. 2018/0182776).

Claim 1

Claim 1 as amended includes the limitations

"insulating structures disposed between and in contact with adjacent conductive strips, the conductive strips extending in a first direction, the insulating structures having a width in a second direction orthogonal to the first direction, wherein the data storage structures are disposed within the width between adjacent conductive strips."

Serov does not describe the quoted limitations, as explained below.

The Office Action asserts

"Regarding claim 1, Serov discloses a memory device, comprising: a plurality of stacks Fig 9A-10, 32/(42/46) of conductive strips …"

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"… the vertical channel pillars having first Fig 9A-10, 601 and second channel films Fig 9A-10, 602 disposed on adjacent stacks in the plurality of stacks and a dielectric material Fig 9A-10, 62 (Paragraph 0150) …"

"… the data storage structures including tunneling layers Fig 9A-10, 56 in contact with the first and second channel films in the vertical channel pillars, discrete charge trapping elements Fig 9A-10, 54 in contact with the tunneling layers Fig 9A-10, 56, and blocking layers Fig 9A-10, 52…"

Pages 4-5, the Office Action; emphasis added.

FIGs. 9B and 9C of Serov are reproduced below, where FIG. 9C is annotated with "W1" to indicate a width of separator insulator structures 43, and annotated with "W2" to indicate a width of a device structure including a blocking dielectric layer 52, a memory material layer 54, a tunnel dielectric 56, and first and second semiconductor channel portions 601 and 602. FIG. 9C is also annotated with an X-axis to indicate a first direction, and a Y-axis to indicate a second direction orthogonal to the first direction.

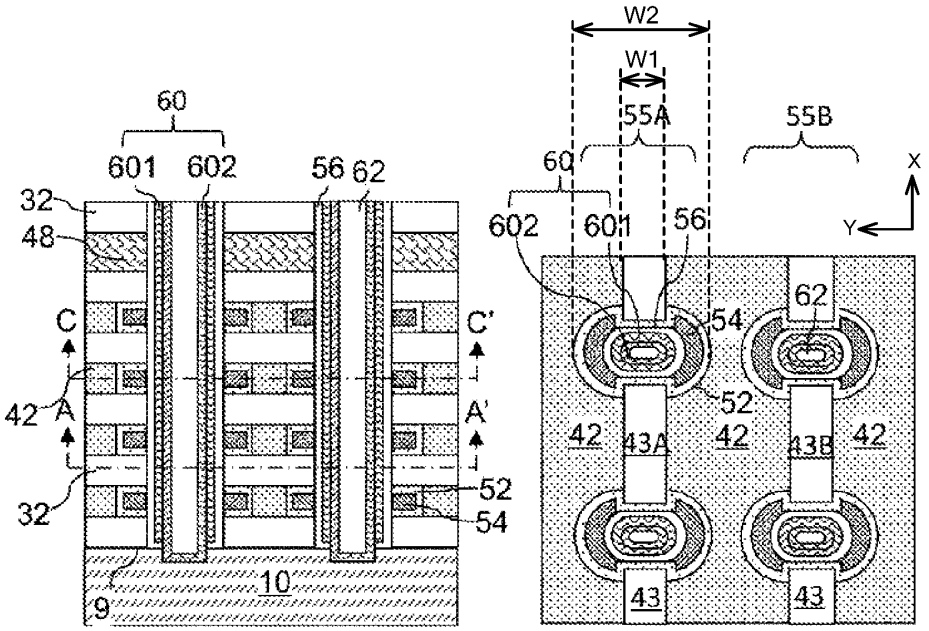


FIG. 9B FIG. 9C

As shown in FIG. 9C of Serov, device structures include data storage structures including a blocking dielectric layer 52, a memory material layer 54, and a tunnel dielectric 56. The device structures are disposed in memory openings 49 (FIG. 5C) including recess regions 49A (FIG.

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5B) between the sacrificial material layers 42. The sacrificial material layers 42 extend in a first direction (X-direction). The device structures are separated by separator insulator structures 43 which have a first width W1 in a second direction (Y-direction) orthogonal to the first direction. The device structures have a second width W2 in the second direction greater than the first width W1. In particular, the data storage structures including a blocking dielectric layer 52, a memory material layer 54, and a tunnel dielectric 56 are disposed within the second width W2 greater than the first width W1, so the data storage structures are not disposed within the first width W1.

In contrast, claim 1 as amended requires

> "insulating structures disposed between and in contact with adjacent conductive strips, the conductive strips extending in a first direction, the insulating structures having a width in a second direction orthogonal to the first direction, wherein the data storage structures are disposed within the width between adjacent conductive strips."

Claim 1 should be allowable for at least the reasons explained above.

The Office Action further asserts

> "**Embodiment 1 (Fig 9B)** of Serov discloses all the limitations except for the arrangement of the channel layers. Whereas **Embodiment 2 (Fig 16B)** of Serov discloses an alternative channel arrangement wherein vertical channel pillars **Fig 16B, 602** disposed between the stacks, the vertical channel pillars having first Fig 16B, 602 (left side of layer 62) and second channel films Fig 16B, 602 (right side of layer 62) disposed on adjacent stacks in the plurality of stacks and a dielectric material Fig 16B, 62 between and contacting the first Fig 16B, 602 (left side of layer 62) and second channel film Fig 16B, 602 (right side of layer 62);"

Page 5, the Office Action; emphasis added.

FIGs. 16A and 16B of Serov are reproduced below. Figures 9B and 9C of Serov are reproduced above.

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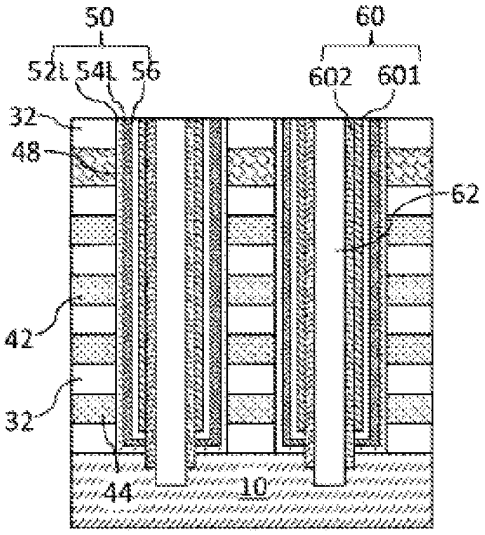


FIG. 16B

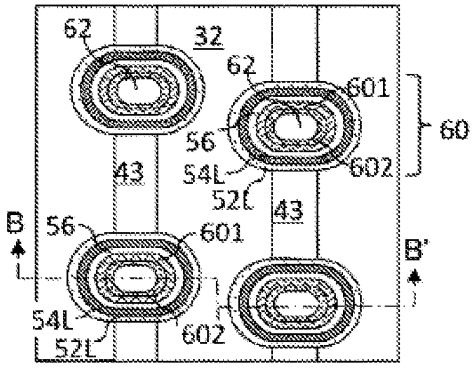


FIG. 16A

FIG. 9B is a vertical cross-sectional view of the first exemplary device structure for **Embodiment 1** (paragraphs [0030, 0031], Serov). FIG. 9C is a horizontal cross-sectional view taken along the horizontal plane C-C' of FIG. 9B (paragraph [0032], Serov).

FIG. 16A is a top-down view of the second exemplary device structure for **Embodiment 2** (paragraphs [0043], Serov). FIG. 16B is a vertical cross-sectional view of the second exemplary device structure for **Embodiment 2** taken along the vertical plane B-B' of FIG. 16A (paragraph [0044], Serov).

Regarding "the arrangement of the channel layers", both **Embodiment 1** (FIGs. 9B, 9C) and **Embodiment 2** (FIGs. 16A, 16B) show that "Each adjoining pair of a first semiconductor channel portion 601 and a second semiconductor channel portion 602 collectively constitutes a semiconductor channel 60…" (paragraph [0150], Serov).

Both FIGs. 9C and 16A show that "If a dielectric core 62 is present, the semiconductor channel 60 laterally surrounds the dielectric core 62" (paragraph [0155], Serov), where the semiconductor channel 60 includes a first semiconductor channel portion 601 and a second semiconductor channel portion 602.

One difference between the two embodiments is that in **Embodiment 1** (FIG. 9B) the second semiconductor channel portion 602 is formed on a top surface of a substrate 10, while in **Embodiment 2** (FIG. 16B) the second semiconductor channel portion 602 is not formed on a top surface of a substrate 10. The top surface of the substrate is located at the bottom of a memory

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opening 49 (FIG. 4B), in which the semiconductor channel 60 is formed (FIG. 9B). However, this difference does not change the arrangement common to both embodiments that "the semiconductor channel 60 laterally surrounds the dielectric core 62" (paragraph [0155], Serov).

Consequently, in FIG. 16B, a second semiconductor channel portion 602 shown at "left side of layer 62" and at "right side of layer 62" is the same semiconductor channel portion that laterally surrounds the dielectric core 62. Similarly, in FIG. 9B, a second semiconductor channel portion 602 shown at "left side of layer 62" and at "right side of layer 62" is the same semiconductor channel portion that laterally surrounds the dielectric core 62.

Therefore Serov describes a dielectric core 62 laterally surrounded by a second semiconductor channel portion 602, and the dielectric core 62 does NOT physically separate the second semiconductor channel portion 602. In contrast, claim 1 requires

> "vertical channel pillars disposed between the stacks, the vertical channel pillars having first and second channel films disposed on adjacent stacks in the plurality of stacks and a dielectric material physically separating the first and second channel films at levels of data storage structures, ...".

Since **Embodiment 1** and **Embodiment 2** both describe the dielectric core 62 laterally surrounded by a second semiconductor channel portion 602, it would not have been obvious to one having ordinary skill of the art before the effective filing date of the claimed invention to modify the **Embodiment 1** of Serov and incorporate the arrangement of **Embodiment 2** as an alternative channel arrangement, in order to reproduce the claimed invention.

Claim 1 should be allowable for at least the reasons explained above.

Claim 11

Claim 11 as amended includes the limitations

> "forming insulating structures disposed between and in contact with adjacent conductive strips, the conductive strips extending in a first direction, the insulating structures having a width in a second direction orthogonal to the first direction, wherein the data storage structures are disposed within the width between adjacent conductive strips."

Claim 11 is amended correspondingly to the amendments in claim 1, and should be allowable for at least the same reasons as explained for claim 1.

Claim 20

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Claim 20 as amended includes the limitations

"forming insulating structures disposed between and in contact with adjacent conductive strips, the conductive strips extending in a first direction, the insulating structures having a width in a second direction orthogonal to the first direction, wherein the data storage structures are disposed within the width between adjacent conductive strips."

Emphasis added.

Claim 20 is amended correspondingly to the amendments in claim 1, and should be allowable for at least the same reasons as explained for claim 1.

Claims 2-4 and 6 depend from claim 1, and should be allowable for at least the same reasons as explained for claim 1, and because of the unique combinations recited.

Claims 12-17 depend from claim 11, and should be allowable for at least the same reasons as explained for claim 11, and because of the unique combinations recited.

Claims 21-22 and 24 depend from claim 20, and should be allowable for at least the same reasons as explained for claim 20, and because of the unique combinations recited.

Accordingly reconsideration of the rejection of claims 1-4, 6, 11-17, 20-22 and 24 as amended under 35 U.S.C. § 103 is respectfully requested.

Rejection of Claims 5, 7-10, 18-19 and 23 under 35 U.S.C. 103

Claims 5, 7-10, 18-19, 23 are rejected under 35 U.S.C. 103 as being unpatentable over Serov et al (US Publication No 2016/0071861) in view of Liu et al (US Publication No. 2016/0204117), Alsmeier et al (US Publication No. 2012/0001249) and Kim (US Publication No. 2018/0182776).

Claim 7 as amended includes the limitations

"insulating structures disposed between and in contact with adjacent conductive strips, the conductive strips extending in a first direction, the insulating structures having a width in a second direction orthogonal to the first direction, wherein the data storage structures are disposed within the width between adjacent conductive strips."

Claim 7 is amended correspondingly to the amendments in claim 1, and should be allowable for at least the same reasons as explained for claim 1.

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Claim 5 depends from claim 1, and should be allowable for at least the same reasons as explained for claim 1, and because of the unique combinations recited.

Claims 8-10 depend from claim 7, and should be allowable for at least the same reasons as explained for claim 7, and because of the unique combinations recited.

Claims 18-19 depend from claim 11, and should be allowable for at least the same reasons as explained for claim 11, and because of the unique combinations recited.

Claim 23 depends from claim 20, and should be allowable for at least the same reasons as explained for claim 20, and because of the unique combinations recited.

Accordingly reconsideration of the rejection of claims 5, 7-10, 18-19 and 23 as amended under 35 U.S.C. § 103 is respectfully requested.

New Claim 25

Applicant has added a new claim 25 that includes the limitations

"wherein the first sidewalls of the conductive strips in the stacks are straight, and the vertical channel pillars disposed between the stacks are parallel to the first sidewalls."

Support for the new claim can be found in Figure 10 of the present specification. Figure 10 illustrates the first sidewalls (1031) of the conductive strips (217, 227, 237) in the stacks are straight, and the vertical channel pillars (910, 920) disposed between the stacks are parallel to the first sidewalls.

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CONCLUSION

It is respectfully submitted that this application is now in condition for allowance.

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 2194-1).

Respectfully submitted,

Dated: 18 April 2019

/Yiding Wu/

Yiding Wu, Reg. No. 65,992

MACRONIX c/o:
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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 15/410,965	Filing Date 01/20/2017	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

	(Column 1)	(Column 2)			
FOR	NUMBER FILED	NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $80 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $420 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	04/18/2019	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 25	Minus	** 24	= 1		x $100 =	100
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 4	= 0		x $460 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	100

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/SHAREILL A COLES/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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NOTICE OF ALLOWANCE AND FEE(S) DUE

46353 7590 05/13/2019

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019

EXAMINER
ENAD, CHRISTINE A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/13/2019

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/410,965	01/20/2017	HANG-TING LUE	MXIC 2194-1	3219

TITLE OF INVENTION: DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	08/13/2019

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

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PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

46353 7590 05/13/2019

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C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/410,965	01/20/2017	HANG-TING LUE	MXIC 2194-1	3219

TITLE OF INVENTION: DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	08/13/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
ENAD, CHRISTINE A	2811	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. Fees submitted: ❑ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

❑ Electronic Payment via EFS-Web ❑ Enclosed check ❑ Non-electronic payment by credit card (Attach form PTO-2038)

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/410,965	01/20/2017	HANG-TING LUE	MXIC 2194-1	3219

46353 7590 05/13/2019

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019

EXAMINER	
ENAD, CHRISTINE A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/13/2019

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 15/410,965	Applicant(s) LUE, HANG-TING	
	Examiner CHRISTINE A ENAD	Art Unit 2811	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☑ This communication is responsive to 4/18/2019.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☑ The allowed claim(s) is/are 1-25 . As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see **http://www.uspto.gov/patents/init_events/pph/index.jsp** or send an inquiry to **PPHfeedback@uspto.gov.**

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:

   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____ .

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____ .

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____.
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.
5. ☐ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/CHRISTINE A ENAD/
Primary Examiner, Art Unit 2811

Micron Ex. 1022, p. 318
Micron v. YMTC
IPR2024-00912

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/410,965	LUE, HANG-TING
	Examiner	Art Unit
	CHRISTINE A ENAD	2811

CPC - Searched*		
Symbol	**Date**	**Examiner**
H01L27/11582	11/24/2017	CE
H01L21/76802, 21/76877	11/24/2017	CE
H01L23/5226, 23/528	11/24/2017	CE

CPC Combination Sets - Searched*		
Symbol	**Date**	**Examiner**

US Classification - Searched*			
Class	**Subclass**	**Date**	**Examiner**

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	**Date**	**Examiner**
Assignee and inventor search conducted	11/24/2017	CE
CPC search	11/24/2017	CE
EAST Search	11/24/2017	CE
EAST Search	5/21/2018	CE
EAST Search	9/18/2018	CE
EAST Search	01/14/2019	CE
EAST Search	04/30/2019	CE

/CHRISTINE A ENAD/ Primary Examiner, Art Unit 2811	

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Micron v. YMTC
IPR2024-00912

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/410,965	LUE, HANG-TING
	Examiner	Art Unit
	CHRISTINE A ENAD	2811

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
H01L	27/11582	04/30/2019	CE
H01L	21/76802, 21/76877	04/30/2019	CE
H01L	23/5226, 23/528	04/30/2019	CE

/CHRISTINE A ENAD/ Primary Examiner, Art Unit 2811	

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Micron v. YMTC
IPR2024-00912

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/410,965	LUE, HANG-TING
	Examiner	**Art Unit**
	CHRISTINE A ENAD	2811

CPC						
Symbol					**Type**	**Version**
H01L	/	27	/	11582	F	2013-01-01
H01L	/	21	/	76802	I	2013-01-01
H01L	/	21	/	76877	I	2013-01-01
H01L	/	21	/	28282	I	2013-01-01

CPC Combination Sets							
Symbol					**Type**	**Set**	**Ranking**	**Version**
	/		/					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	25	
/CHRISTINE A ENAD/ Primary Examiner, Art Unit 2811	30 April 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	Fig 9 and Fig 10

U.S. Patent and Trademark Office — Part of Paper No.: 20190430

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Micron v. YMTC
IPR2024-00912

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/410,965	LUE, HANG-TING
	Examiner	**Art Unit**
	CHRISTINE A ENAD	2811

INTERNATIONAL CLASSIFICATION				
CLAIMED				
H01L	/	27	/	11582
H01L	/	21	/	768
H01L	/	23	/	528
H01L	/	23	/	522

NON-CLAIMED				
	/		/	

US ORIGINAL CLASSIFICATION	
CLASS	**SUBCLASS**

CROSS REFERENCES(S)						
CLASS	**SUBCLASS (ONE SUBCLASS PER BLOCK)**					

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	25	
/CHRISTINE A ENAD/ Primary Examiner, Art Unit 2811	30 April 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	Fig 9 and Fig 10

U.S. Patent and Trademark Office — Part of Paper No.: 20190430

Micron Ex. 1022, p. 322
Micron v. YMTC
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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	15/410,965	LUE, HANG-TING
	Examiner	**Art Unit**
	CHRISTINE A ENAD	2811

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	11	10	20	19										
2	2	12	11	21	20										
3	3	13	12	22	21										
4	4	14	13	23	22										
5	5	15	14	24	23										
6	6	16	15	25	24										
8	7	17	16	7	25										
9	8	18	17												
10	9	19	18												

NONE		**Total Claims Allowed:**	
(Assistant Examiner)	(Date)	25	
/CHRISTINE A ENAD/ Primary Examiner, Art Unit 2811	30 April 2019	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	Fig 9 and Fig 10

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Micron v. YMTC
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BIB DATA SHEET

CONFIRMATION NO. 3219

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
15/410,965	01/20/2017	257	2811	MXIC 2194-1

APPLICANTS
MACRONIX INTERNATIONAL CO., LTD., Hsinchu, TAIWAN;

INVENTORS
HANG-TING LUE, HSINCHU, TAIWAN;

** CONTINUING DATA **********

** FOREIGN APPLICATIONS **********

** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **
01/27/2017

Foreign Priority claimed	35 USC 119(a-d) conditions met	Verified and Acknowledged	Met after Allowance	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
❑ Yes ☑ No	❑ Yes ☑ No	/CHRISTINE A ENAD/ Examiner's Signature	❑ Initials	TAIWAN	12	24	4

ADDRESS

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019
UNITED STATES

TITLE

DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE

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2440	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	❑ All Fees ❑ 1.16 Fees (Filing) ❑ 1.17 Fees (Processing Ext. of time) ❑ 1.18 Fees (Issue) ❑ Other _____ ❑ Credit

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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("20180211969").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/04/30 18:20
S1	574	(("MACRONIX") near3 ("INTERNATIONAL") near3 ("CO") near3 ("LTD")).AANM.	USPAT	OR	OFF	2017/11/22 09:51
S2	358	(("LUE") near3 ("HANG-TING")).INV.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 09:51
S3	9877	(H01L27/11582.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:51
S4	13188	(H01L21/76802.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:51
S5	17402	(H01L21/76877.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S6	15471	(H01L23/5226.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S7	13459	(H01L23/528.cpc.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 09:52
S8	20	(vertical near stack) and ((insulating or dielectric or insulation) near channel)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/11/22 10:17

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			IBM_TDB			
S9	0	("2017/0243879").URPN.	USPAT	OR	OFF	2017/11/22 10:21
S10	28	("20070029607" | "20090230454" | "20100207194" | "20100213527" | "20110156044" | "20120012921" | "20120326221" | "20140131784" | "20150044833" | "20150076584" | "20150179660" | "20150255481" | "20150371709" | "20160133642" | "5915167" | "7575973" | "7906392" | "8084819" | "8187936" | "8461641" | "8610194" | "8735962" | "8767465" | "8823076" | "8853765" | "8981457" | "8987119" | "9023719").PN. OR ("9728546").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 10:25
S11	328	((insulating or dielectric or insulation) near channel)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 12:35
S12	0	((insulating or dielectric or insulation) near channel near gap)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S13	10	((insulating or dielectric or insulation) near channel near gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S14	346	((insulating or dielectric or insulation) near channel same gap)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 17:51
S15	1065	((insulating or dielectric or insulation) same channel same gap)and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 18:00
S16	4	("20120001249").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:05
S17	2	("20160181271").PN.	US-PGPUB; USPAT; USOCR;	OR	OFF	2017/11/22 18:07

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			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S18	8	(("20130049095") or ("20100181612") or ("20130100741")).PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/22 18:07
S19	51	((insulating or dielectric or insulation) same channel NEAR (SEPARATION OR gap or void))and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 18:52
S20	35	("20050280061" | "20070045708" | "20070158736" | "20070252201" | "20080073635" | "20080175032" | "20080180994" | "20090097321" | "20090184360" | "20100270593" | "20110018051" | "20120068241" | "20120119283" | "20120182806" | "20150243674" | "20150357342" | "20150371998" | "20160056168" | "6906940" | "7315474" | "7420242" | "7612403" | "7696559" | "7851849" | "8008732" | "8363476" | "8467219" | "8503213" | "8648438" | "8759899" | "8853818" | "9147468" | "9224473").PN. OR ("9401371").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 18:53
S21	7	("20160005746" | "20160163733" | "20160240551" | "9379122" | "9379131" | "9401209" | "9401371").PN. OR ("9818760").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/11/22 18:56
S22	32	((insulating or dielectric or insulation) same channel NEAR (seam or hollow))and (tunnel or tunneling) and (blocking or block) and (trap or trapping)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/11/22 19:02
S23	2	("20160204117").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2017/11/24 13:25
S24	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/05/14 11:31
S25	39484	((insulating or dielectric or insulation) same channel)and (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/05/14 12:11

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S26	19502	((insulating or dielectric or insulation) same channel)same (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/05/14 12:11
S27	305	((insulating or dielectric or insulation) same channel)near (tunnel or tunneling)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/05/14 12:13
S28	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/05/21 19:06
S29	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/08/23 12:43
S30	1	("20160071861").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:14
S31	1	("20180211969").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:18
S32	0	("2017/0194340").URPN.	USPAT	OR	OFF	2018/09/18 09:35
S33	1	("9831257").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:36
S34	43	("20050280061" | "20070045708" | "20070158736" | "20070252201" | "20080073635" | "20080175032" | "20080180994" | "20090097321" | "20090184360" | "20100181612" | "20100270593" | "20110018051" | "20120001249" | "20120068241" | "20120119283" | "20120147644" | "20120182806" | "20130049095" | "20130100741" | "20130134492" | "20130207178" | "20130248945" | "20140231954" | "20150263016" | "20150318301" | "20150364487" | "20160043100" | "20160181271" | "6906940" | "7153780" | "7315474" | "7420242" | "7696559" | "7851849" | "8008732" | "8363476" | "8467219" | "8503213" | "8648438" | "8759899" | "8853818" | "9147468" | "9287291").PN. OR ("9831257").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:36
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		"20130207178" | "20130248945" | "20140231954" | "20150263016" | "20150318301" | "20150364487" | "20160043100" | "20160181271" | "6906940" | "7153780" | "7315474" | "7420242" | "7696559" | "7851849" | "8008732" | "8363476" | "8467219" | "8503213" | "8648438" | "8759899" | "8853818" | "9147468" | "9287291").PN. OR ("9831257").URPN.				
S36	3525	(blocking same tunneling) and (memory near device)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:59
S37	1765	(blocking same tunneling same channel) and (memory near device)	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 09:59
S38	3	(("20110147823") or ("20120001249") or ("20170278859")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/09/18 10:32
S39	2	(("20160071861") or ("20120001249")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 16:00
S40	1	("20180211969").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 16:00
S41	39	("20050280061" | "20070045708" | "20070158736" | "20070252201" | "20080073635" | "20080175032" | "20080180994" | "20090097321" | "20090184360" | "20100270593" | "20110018051" | "20120068241" | "20120119283" | "20120182806" | "20150243674" | "20150357342" | "20150371998" | "20160056168" | "6906940" | "7315474" | "7420242" | "7612403" | "7696559" | "7851849" | "8008732" | "8363476" | "8467219" | "8503213" | "8648438" | "8759899" | "8853818" | "9147468" | "9224473").PN. OR ("9401371").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 16:29
S42	1	"15085102"	USPAT	OR	OFF	2018/11/19 16:38
S43	0	"15085102"	US-PGPUB	OR	OFF	2018/11/19 16:38
S44	2	("20120068247").PN. OR ("9748264").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 16:40
S45	8	("20130270631" | "20140141583" | "20150115344" | "20160148946" | "20160181264" | "9130054" | "9171729" | "9305937").PN. OR ("9576972").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 16:46
S46	10	("20110002178" | "20110032772" | "20120052674" | "20140008714" | "20140084357" | "20140284695" | "20140332875" | "20160155750").PN. OR ("9484353").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 16:54
S47	6894	second near channel same vertical	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 16:59

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S48	772	second near vertical near channel	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 16:59
S49	32426	memory and pillar	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 17:00
S50	303	S47 and S49	US-PGPUB; USPAT; USOCR	OR	OFF	2018/11/19 17:00
S51	1	("20180211969").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/01/14 09:56
S52	1	("20180182776").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/01/14 09:56
S53	2	(("20160071861") or ("20120001249")).PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2019/01/14 12:50

4/30/2019 7:11:28 PM
C:\Users\cenad\Documents\EAST\Workspaces\15410965.wsp

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Micron v. YMTC
IPR2024-00912

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May 13, 2019 03:36:01 AM

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UNITED STATES

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15410965	NOA	05/13/2019	MXIC 2194-1

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46353 7590 05/13/2019

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019

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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

Kathryn Marley	(Typed or printed name)
/Kathryn Marley/	(Signature)
24 July 2019	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/410,965	01/20/2017	HANG-TING LUE	MXIC 2194-1	3219

TITLE OF INVENTION: DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$1000	$0.00	$0.00	$1000	08/13/2019

EXAMINER	ART UNIT	CLASS-SUBCLASS
ENAD, CHRISTINE A	2811	257-324000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-09 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

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2
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: MACRONIX INTERNATIONAL CO., LTD.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): HSINCHU, TW

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ☒ Corporation or other private group entity ❑ Government

4a. Fees submitted: ☒ Issue Fee ❑ Publication Fee (if required) ❑ Advance Order - # of Copies _____

4b. Method of Payment: *(Please first reapply any previously paid fee shown above)*

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5. **Change in Entity Status** (from status indicated above)

❑ Applicant certifying micro entity status. See 37 CFR 1.29

❑ Applicant asserting small entity status. See 37 CFR 1.27

❑ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Yiding Wu/ Date 24 July 2019

Typed or printed name Yiding Wu Registration No. 65,992

PTOL-85 Part B (08-18) Approved for use through 01/31/2020 OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Micron Ex. 1022, p. 332
Micron v. YMTC
IPR2024-00912

Electronic Patent Application Fee Transmittal

Application Number:	15410965
Filing Date:	20-Jan-2017
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	HANG-TING LUE
Filer:	Yiding Wu/Kathryn Marley
Attorney Docket Number:	MXIC 2194-1

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1000	1000

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1000**

Electronic Acknowledgement Receipt

EFS ID:	36683440
Application Number:	15410965
International Application Number:	
Confirmation Number:	3219
Title of Invention:	DISCRETE CHARGE TRAPPING ELEMENTS FOR 3D NAND ARCHITECTURE
First Named Inventor/Applicant Name:	HANG-TING LUE
Customer Number:	46353
Filer:	Yiding Wu/Kathryn Marley
Filer Authorized By:	Yiding Wu
Attorney Docket Number:	MXIC 2194-1
Receipt Date:	24-JUL-2019
Filing Date:	20-JAN-2017
Time Stamp:	20:48:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	$1000
RAM confirmation Number	072519INTEFSW20484200
Deposit Account	500869
Authorized User	Kathryn Marley
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.16 (National application filing, search, and examination fees) 37 CFR 1.17 (Patent application and reexamination processing fees)	

37 CFR 1.19 (Document supply fees)

37 CFR 1.20 (Post Issuance fees)

37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	00706700.PDF	72064 8f3387fad711914e4c287ad001467ef430055cfd	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30150 cefa349eabede46916c15d76d8dd82bbdbd40e7e	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	102214		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
15/410,965	09/03/2019	10403637	MXIC 2194-1	3219

46353 7590 08/14/2019

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 17 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

HANG-TING LUE, HSINCHU, TAIWAN;
MACRONIX INTERNATIONAL CO., LTD., Hsinchu, TAIWAN;

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Micron Ex. 1022, p. 337
Micron v. YMTC
IPR2024-00912

To: docket@hmbay.com,,
From: PAIR_eOfficeAction@uspto.gov
Cc: PAIR_eOfficeAction@uspto.gov
Subject: Private PAIR Correspondence Notification for Customer Number 46353

Aug 15, 2019 03:37:28 AM

Dear PAIR Customer:

MACRONIX
C/O HAYNES BEFFEL & WOLFELD LLP
P. O. BOX 366
HALF MOON BAY, CA 94019
UNITED STATES

The following USPTO patent application(s) associated with your Customer Number, 46353 , have new outgoing correspondence. This correspondence is now available for viewing in Private PAIR.

The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

Disclaimer:
The list of documents shown below is provided as a courtesy and is not part of the official file wrapper. The content of the images shown in PAIR is the official record.

Application	Document	Mailroom Date	Attorney Docket No.
15410965	ISSUE.NTF	08/14/2019	MXIC 2194-1

To view your correspondence online or update your email addresses, please visit us anytime at https://sportal.uspto.gov/secure/myportal/privatepair.

If you have any questions, please email the Electronic Business Center (EBC) at EBC@uspto.gov with 'e-Office Action' on the subject line or call 1-866-217-9197 during the following hours:

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Thank you for prompt attention to this notice,

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