

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,

Petitioner,

v.

YANGTZE MEMORY TECHNOLOGIES COMPANY, LTD.,

Patent Owner.

Case IPR2024-00912
Patent 11,600,342

**PATENT OWNER'S PRELIMINARY RESPONSE
UNDER 37 C.F.R. § 42.107**

TABLE OF CONTENTS

LIST OF EXHIBITS	iii
LIST OF ABBREVIATIONS.....	iv
I. INTRODUCTION	1
II. THE CLAIMED INVENTION OF THE '342 PATENT	6
III. FILE HISTORY.....	11
A. '279 (Parent) File History	11
B. '342 File History	13
IV. CLAIM CONSTRUCTION	13
V. BACKGROUND OF THE ASSERTED ART.....	15
A. U.S. Pat. Pub. No. 2021/0027848 ("Seo") (Ex. 1005).....	15
B. U.S. Pat. Pub. No. 2015/0003169 ("Nam") (Ex. 1006).....	17
C. Choi et al., Comprehensive Evaluation of Early Retention (Fast Charge Loss Within a Few Seconds) Characteristics in Tube-Type 3-D NAND Flash Memory ("Choi") (Ex. 1007)	20
VI. PETITIONER FAILS TO ESTABLISH A REASONABLE LIKELIHOOD THAT IT WOULD PREVAIL WITH RESPECT TO THE CHALLENGED CLAIM.....	22
A. Ground 1: Seo in View of Choi Does Not Disclose or Render Obvious the claimed Read-Verification Operation that "Removes Fast Charges" of the Target Memory Cell "During [a] First Time Period"	25
B. Ground 1: Seo in View of Choi Does Not Disclose or Render Obvious "a Voltage of the Unselected Top Select Gate Equals to a Threshold Voltage of an Unselected Memory Cell".....	32
C. Ground 2: Nam in View of Choi Does Not Disclose or Render Obvious a Read-Verification Operation That "Removes Fast Charges" of the Target Memory Cell "During [a] First Time Period"	35
D. Ground 2: Nam in View of Choi Does Not Disclose or Render Obvious "a Voltage of the Unselected Top Select Gate Equals to a Threshold Voltage of an Unselected Memory Cell".....	40
VII. CONCLUSION.....	42

TABLE OF AUTHORITIES

Cases	Page(s)
<i>In re Rijckaert</i> , 9 F.3d 1531 (Fed. Cir. 1993)	4, 17, 30, 32, 37, 39
<i>Phillips v. AWH Corp.</i> , 415 F.3d 1303 (Fed. Cir. 2005) (<i>en banc</i>)	13

LIST OF EXHIBITS

Exhibit	Description
Ex. 2001	U.S. Patent No. 11,043,279 (“the ’279 patent”)
Ex. 2002	File History of U.S. Patent No. 11,043,279 (“’279FH”)
Ex. 2003	Joint Claim Construction Statement
Ex. 2004-09	Reserved
Ex. 2010	Declaration of Jonathan Bradford

LIST OF ABBREVIATIONS

Abbreviation	Term
'342	U.S. Pat. No. 11,600,342 (Ex. 1001)
'342FH	File History of U.S. Pat. No. 11,600,342 (Ex. 1002)
'279	U.S. Pat. No. 11,043,279 (Ex. 2001)
'279FH	File History of U.S. Pat. No. 11,043,279 (Ex. 2002)
Challenged Claim	'342, Claim 7
Choi	Choi et al., "Comprehensive evaluation of early retention (fast charge loss within a few seconds) characteristics in tube-type 3-D NAND Flash Memory," 2016 Symposium on VLSI Technology, Digest of Technical Papers, 78-79 (Ex. 1007)
Nam	U.S. Pat. Pub. No. 2015/0003169 (Ex. 1006)
Office	U.S. Patent and Trademark Office
Petition or Pet.	Petition for <i>Inter Partes</i> Review of U.S. Patent No. 11,600,342 (IPR2024-00912 Paper 1)
Parallel district court litigation	<i>Yangtze Memory Technologies Company, Ltd. v. Micron Technology, Inc.</i> , NDCA-3-23-cv-05792 (N.D. Cal.)
Patent Owner	Yangtze Memory Technologies Co. Ltd.
Petitioner	Micron Technology, Inc.
POSITA	Person of ordinary skill in the art
Seo	U.S. Pat. Pub. No. 2021/0027848 (Ex. 1005)

Pursuant to §42.107,¹ Patent Owner submits this Preliminary Response to the above-captioned Petition, which should be denied in its entirety based on Petitioner's failure to show a reasonable likelihood of prevailing on any asserted ground as to the single Challenged Claim.

I. INTRODUCTION

This proceeding relates to the second of two *inter partes* review petitions filed by Petitioner concerning U.S. Patent No. 11,600,342 ("342 patent"), and should be denied institution for at least the same reasons identified in Patent Owner's prior Preliminary Response.² Petitioner's second IPR challenges dependent claim 7 ("Challenged Claim") and raises the same grounds based on the Seo, Nam, and Choi references for independent claim 1, on which the Challenged Claim depends, as the

¹ All emphasis and color annotations herein are added, and all statutory and regulatory citations are to either 35 U.S.C. or 37 C.F.R., as the context indicates, unless otherwise stated.

² Patent Owner does not oppose Petitioner's claim that it needed a second petition (Paper 3), but disputes Petitioner's assertions that Patent Owner's identification of asserted claims was belated, that Patent Owner's infringement allegations are without merit and could not have been credibly alleged, and that Patent Owner has asserted a large number of '342 claims.

first IPR. This Preliminary Response presents the same arguments that were raised in the first proceeding regarding the Seo, Nam, and Choi grounds for independent claim 1, as well as additional arguments that address the Challenged Claim specifically.

As set forth in Patent Owner's earlier Preliminary Response, Petitioner's previously filed IPR2024-00793 (Pap. 1) challenging claims 1-6, 8-20 should be denied institution. IPR2024-00793, Pap. 11. The Challenged Claim in this IPR depends from claim 1, and Petitioner relies on the same combinations of Seo, Nam, and Choi again here. Pet. 8. Accordingly, Patent Owner presents the same arguments here as to the limitations of claim 1, which are required by dependent claim 7. In addition, Patent Owner presents additional arguments as to the further limitations recited by dependent claim 7. The previously-filed Preliminary Response in IPR2024-00793 did not address the added limitations of dependent claim 7 because Petitioner had not challenged dependent claim 7. Thus, any decision by the Board to institute IPR2024-00793 does not mean that a reasonable likelihood of success also exists in this proceeding.

U.S. Patent No. 11,600,342 ("the '342 patent," Ex. 1001) is directed to a novel technique for conducting a read-verification operation on a target memory cell of a three-dimensional ("3D") non-volatile flash memory device that removes "fast charges" prior to verifying the programmed value of a memory cell. '342, 1:29-31,

1:49-54. As explained by the '342, programming operations may create “fast charges” in the memory cell, which are shallowly-trapped electrical charges that can be dislodged and, if not removed, can result in inaccurate threshold voltage determinations. '342, 1:33-36, 1:41-45, 8:62-65, 9:4-7.

The new read-verification operation taught by the '342 and recited in the claims is characterized by several features not found in or rendered obvious by the prior art. The new approach improves over traditional read-verification operations, in part, by using a two-step process. A “prepare voltage,” an “off voltage,” and a “pass voltage” are applied to particular device structures to remove fast charges during a first time period, followed by switching to a “read voltage,” an “off voltage,” and a “pass voltage” during a subsequent second time period in order to sense the programmed state of the target memory cell. *See, e.g.*, '342, 1:52-2:2, 12:24-40, Fig. 6. In some embodiments, this further includes applying a “read voltage” when a voltage of the unselected top select gate equals “a threshold voltage” of an unselected memory cell. '342 2:28-39.

By tailoring the voltages being applied, “an electric field parallel to the channel can be established” that “extends into the charge storage layer 424, the tunneling layer 426, and the channel layer 338” sufficient to “de-trap the fast charges” so that they can be “recombined ... or be removed through the conductive path established in the channel of the unselected memory cells.” '342 12:24-34.

Accordingly, the '342 teaches removing fast charges prior to the sensing step in the second time period, thus minimizing undesirable threshold voltage shifts and enabling more accurate threshold voltage readings during the read-verification operation. '342, 8:49-53, 8:62-65.

Institution should be denied because the Petition fails to establish a reasonable likelihood of prevailing with respect to claim 7—the sole Challenged Claim.

Petitioner does not assert that any of the cited references anticipates the Challenged Claim. Instead, Petitioner raises obviousness arguments—relying primarily on hindsight and flawed inherency arguments. Specifically, Petitioner argues that the devices in its proposed combinations remove fast charges during a read-verify operation based solely on the mistaken premise that applying a higher voltage to the unselected word lines inherently removes fast charges. The cited art does not discuss using a higher voltage to remove these fast charges, let alone specify sufficient detail to show that fast charges are in fact removed. Petitioner instead appears to rely on the mere possibility of fast charge removal, which is insufficient under binding Federal Circuit law. *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (“[t]he mere fact that a certain thing *may* result from a given set of circumstances is not sufficient” to show a feature is disclosed or rendered obvious); *see also* MPEP 2112.

Additionally, in addressing the language of claim 7, Petitioner relies on an internally inconsistent mapping that requires the same voltage to be both a “threshold voltage” that turns on the memory cells and an “off voltage” that does not turn on the memory cells.

Petitioner’s Ground 1 relies on Seo and Choi as purportedly rendering obvious removing fast charges during Seo’s read operation, but the references provide no such teaching. Petitioner seemingly concedes that Seo does not expressly teach removing fast charges. Instead, Petitioner incorrectly assumes that applying a “higher voltage” on unselected word lines inherently results in removing fast charges. See Pet. 42-44. Specifically, Petitioner cites and mischaracterizes the ’342 and Choi as supposedly teaching that Seo’s “voltage differential” would remove fast charges. See Pet. 42-44 (citing ’342, 12:24-34). But the ’342 and Choi do not suggest that the mere difference between unselected and selected word line voltages removes fast charges, nor do they otherwise suggest that the Seo’s read operation removes fast charges. Indeed, Seo does not even disclose the particular voltages applied, or the duration of its read operation. Thus, Petitioner has not shown that removing fast charges is inherent in Seo’s read operation, or that removing fast charges would have been obvious. Additionally, Petitioner has further failed to show that the additional limitation of dependent claim 7 has been satisfied, as Petitioner relies solely on an internally inconsistent mapping that requires the same voltage to act as both a

“threshold voltage” that turns on the memory cells and an “off voltage” that does not turn on the memory cells.

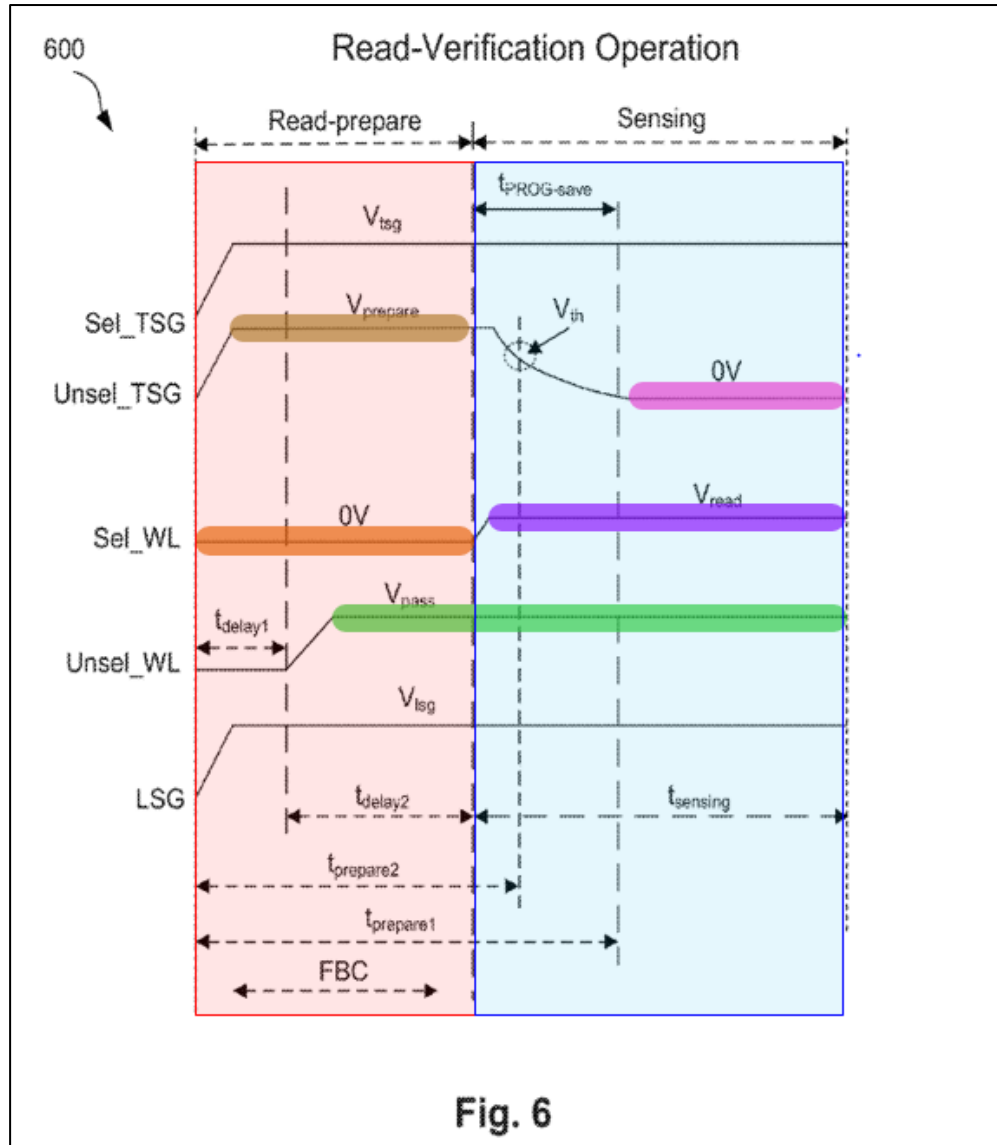
Petitioner’s Ground 2 relies on Nam and Choi as purportedly rendering obvious removing fast charges during a read-verify operation, but this second combination suffers from the same deficiencies as the Seo and Choi combination. As before, Petitioner seemingly concedes that Nam does not expressly teach removing fast charges. Instead, Petitioner argues that Nam—like Seo—discloses having a higher voltage on unselected word lines, and again mischaracterizes the ’342 and Choi as supposedly teaching that this “voltage differential” would remove fast charges. See Pet. 66-68. Also as before, with respect to the additional limitation of dependent claim 7, Petitioner’s mapping relies solely on internally inconsistent arguments for the claimed “off voltage” and “threshold voltage.” These arguments fail for the same reasons as in Ground 1.

II. THE CLAIMED INVENTION OF THE ’342 PATENT

The claimed invention of the ’342 is directed to an improved read-verification process—and an apparatus for performing this process—on a target memory cell in a three-dimensional (“3D”) non-volatile flash memory device to enable more accurate and efficient threshold voltage readings. ’342, 1:17-19, 1:41-45, 1:49-54, 8:62-65, 12:37-40, 13:48-50.

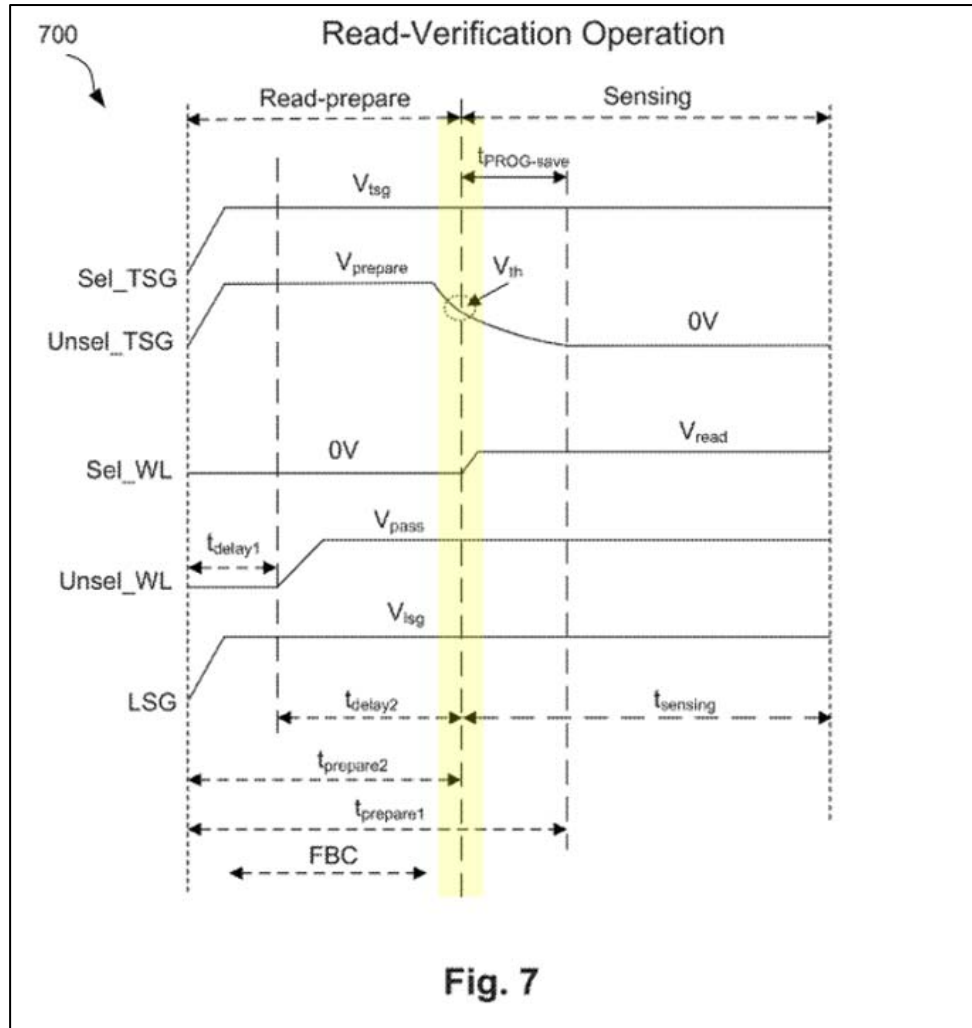
3D NAND flash memory has been developed to use “charge-trapping technology” to program a memory cell. ’342, 1:29-31. During programming, data is written to a target memory cell by altering the charge within it, which changes the “threshold voltage” of the memory cell. ’342, 1:31-32, 7:18-21, 8:43-46. The ’342 addresses the problem of “fast charges” in the memory cell, which are generated during programming operations, and which can result in a “fake high threshold voltage” unless they are removed prior to performing a read-verification operation. ’342, 1:29-45, 8:43-65 (describing that fast charges can cause threshold voltages to shift over time).

The claimed invention of the ’342 removes fast charges, in part, by making use of a two-step read-verification operation that applies different voltages during different time periods. ’342, 1:52-62, 11:14-15. For example, as shown in Figure 6, during the **first time period**, a **prepare voltage** (“ $V_{prepare}$ ”) is applied to an unselected top select gate of an unselected memory string (“Unsel_TSG”), an **off voltage** (“0V”) is applied to the selected word line of the target memory cell (“Sel_WL”), and a **pass voltage** (“ V_{pass} ”) is applied to an unselected word line (“Unsel_WL”) to remove fast charges. ’342, 11:11-33. During the **second time period**, an **off voltage** (“0V” or “ V_{off} ”) is applied to Unsel_TSG, a **read voltage** (“ V_{read} ”) is applied to Sel_WL, and the **pass voltage** (“ V_{pass} ”) continues to be applied to Unsel_WL. ’342, 1:45-61, 12:45-50.



'342, Fig. 6 (annotating the time periods and applied voltages).

Additionally, as shown in Figure 7, in some embodiments the **read voltage** (" V_{read} ") is applied to Sel_WL when "a voltage of the unselected top select gate (Unsel_TSG) equals to a threshold voltage of an unselected memory cell." '342 2:31-35.



'342 Fig. 7 (annotating the time when the voltage of the unselected top select gate (Unsel_TSG) equals a threshold voltage of an unselected memory cell).

As explained by the '342, this process is used to remove fast charges during the **first time period**, and ensure the accuracy of the sensing step in the **second time period**. Depending on the structure of the device, "an electric field parallel to the channel can be established" based on the voltages applied in the first time period that "extends into the charge storage layer 424, the tunneling layer 426, and the channel layer 338" sufficient to "de-trap the fast charges" so that they can be

“recombined ... or be removed through the conductive path established in the channel of the unselected memory cells.” ’342 12:24-34. Once the fast charges are removed during the first time period, the programmed value of the memory cell can then be measured by applying the appropriate voltages during the **second time period**. See ’342, 1:61-63, 8:43-65.

Independent Claim 1 and dependent claim 7 (the Challenged Claim) of the ’342 are method claims directed to aspects of the above-described invention. Claim 1 reads as follows:

[1.pre] A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:

[1.a] applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period;

[1.b] applying, on a selected word line associated with the target memory cell, the off voltage during the first time period and a read voltage during the second time period; and

[1.c] applying, on an unselected word line, a pass voltage during the first time period and the second time period,

[1.d] wherein the read-verification operation removes fast charges of the target memory cell during the first time period.

Dependent claim 7 reads as follows:

The method of claim 1, wherein the applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell.

III. FILE HISTORY

A. '279 (Parent) File History

The '342 claims remain patentable over the prior art of record. The '342, corresponding to U.S. App. 17/324,877, is a continuation of U.S. Pat. No. 11,043,279 (“the '279 patent,” Ex. 2001). The claims of the '279, like the claims of the '342, require the steps of: (1) “applying, on an unselected top select gate of an unselected memory string, a prepare voltage,” (2) “applying, on a selected word line associated with the target memory cell, the off voltage,” (3) “applying, on an unselected word line, a pass voltage,” and (4) “remov[ing] fast charges of the target memory cell during the first time period.” The table below maps claim 1 of the '342 to the corresponding similar limitations of claim 1 of the '279.

'342 Claim 1	'279 (Parent) Claim 1
A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:	A method for conducting a read-verification operation on a target memory cell in a three-dimensional (3D) memory device, comprising:
[blank]	removing fast charges of the target memory cell at a read-prepare step, comprising:
applying, on an unselected top select gate of an unselected memory string, a prepare voltage during a first time period and an off voltage during a second time period;	applying a prepare voltage (Vprepare) on an unselected top select gate (Unsel_TSG) of an unselected memory string;
applying, on a selected word line associated with the target memory cell, the off voltage during the first time	applying a first off voltage (Voff) on a selected word line (Sel_WL)

period and a read voltage during the second time period; and	associated with the target memory cell ; and
applying, on an unselected word line, a pass voltage during the first time period and the second time period,	applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL) ; and
wherein the read-verification operation removes fast charges of the target memory cell during the first time period.	[blank]
[blank]	measuring a threshold voltage of the target memory cell at a sensing step.

In an Office Action dated October 20, 2020, the Examiner rejected pending claims 1-3, 7, and 9 of the '279 as purportedly anticipated by U.S. Pub. No. 2019/0333590 ("Lee"), and found that the other claims recited allowable subject matter. Ex. 2002 ("279FH"), 208-213. The Applicant overcame the rejection without amendment by arguing that Lee failed to disclose "applying a prepare voltage (V_{prepare}) on an unselected top select gate (Unsel_TSG) of an unselected memory string," "applying a first off voltage (V_{off}) on a selected word line (Sel_WL) associated with the target memory cell," or "applying a pass voltage (V_{pass}) on an unselected word line (Unsel_WL)." *Id.*, 231-241. The Examiner issued a Notice of Allowance on February 24, 2021 without commenting further on the reasons for allowance. *Id.*, 242-246.

B. '342 File History

The '342 was filed on May 19, 2021 as a continuation of the '279. Ex. 1002 (“'342FH”), 1-9. In an Office Action dated July 26, 2022, the Examiner rejected all pending claims as purportedly anticipated by U.S. Pub. No. 2019/0371394 (“Yang”). Ex. 1002 ('342FH), 269-276. Following a telephonic interview on October 14, 2022, the Applicant overcame the rejection without amendment by arguing that Yang did not disclose “applying, on an unselected word line, a pass voltage during the first time period and the second time period.” *Id.*, 306-313.

The Examiner issued a Notice of Allowance on November 4, 2022. '342FH, 317-323, 327-341. In the statement for reasons for allowance, the Examiner found that the claimed limitations were allowable over the prior art of record, stating that “the prior art made of record and considered pertinent to the applicant’s disclosure does not teach or suggest the claimed limitations” of the '342 patent. *Id.*, 322.

IV. CLAIM CONSTRUCTION

The Board construes claim terms “using the same claim construction standard that would be used to construe the claim in a civil action.” §42.100(b). Under this standard, claim terms are “generally given their ordinary and customary meaning” to a person of ordinary skill in the art (“POSITA”). *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (*en banc*). A POSITA ascertains the meaning of the claims based on the claim language, specification, prosecution history, and relevant

extrinsic evidence, although the claims and patent specification are the primary sources for construing claims. *Id.*, 13:14-16.

The Petition does not formally propose any terms for construction, and neither party has proposed any '342 terms for construction in the parallel district court proceeding. *See* Pet. 27-28; Ex. 2003 (Joint Claim Construction Statement).

The Petition raises an argument regarding the scope of the terms that need not be resolved for purposes of deciding whether to institute IPR. Specifically, the Petition argues the Challenged Claim recites “applying” voltages “during” certain time periods, but “do not require applying these voltages throughout a given time period.” Pet. 27-28. Patent Owner submits that it is not necessary for the Board to resolve whether a voltage needs to be applied during the entire time period in order to resolve the arguments raised in this Preliminary Response. Even under Petitioner’s proposed interpretation, each of the Grounds fails at least because the claimed voltages recited by Claim 1 must still be used to “remove[] fast charges ... during a first time period” of the claimed “read-verification operation.” *See generally* Section VI (discussing the Grounds). Accordingly, it is not necessary for the Board to construe any claim terms to confirm that institution should be denied.

Patent Owner reserves the right to raise claim construction issues if the Board institutes IPR and in the underlying district court proceedings.

V. BACKGROUND OF THE ASSERTED ART

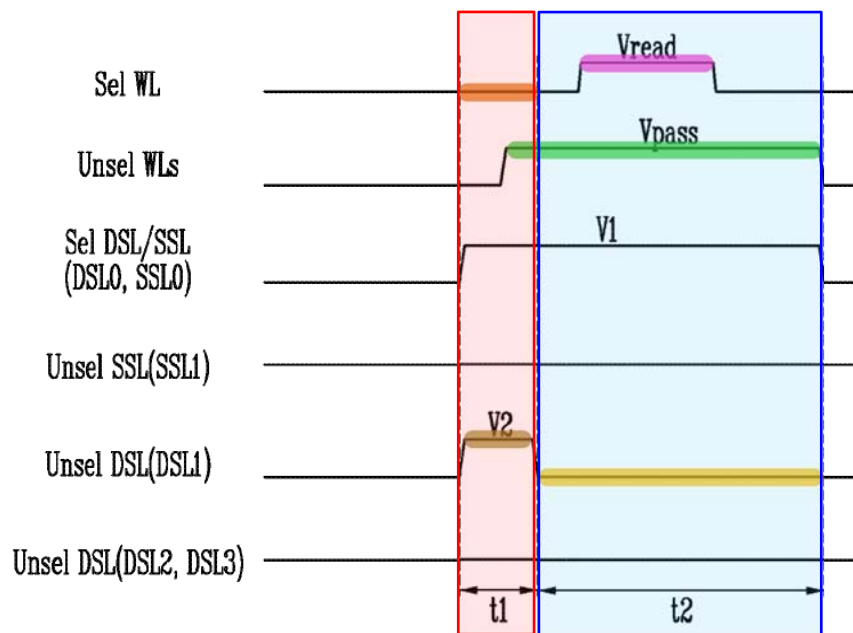
A. U.S. Pat. Pub. No. 2021/0027848 (“Seo”) (Ex. 1005)

Petitioner concedes that Seo does not anticipate the Challenged Claim. Rather, Petitioner falls back to broken obviousness combinations of Seo and Choi (Ground 1) that still fail to satisfy the Challenged Claim. *See* Pet., 9, 35-53. While Seo discloses a “read” operation for a “three dimensional” memory device with a “first time period t1” and a “second time period t2” using different voltages in each period (Seo, [0011], [0051]), Seo does not disclose or suggest that this process is sufficient to remove any fast charges as part of a read-verification operation. Indeed, Seo does not even contemplate the existence of fast charges, or that there is a benefit in removing them from a target memory cell. Rather, Seo is concerned with addressing an unrelated source of read disturbance stemming from “Hot Carrier Injection.” *See* Seo, [0048].

As shown by Fig. 8, Seo discloses different voltages being applied to unselected word lines “Unsel WLs,” selected word lines “Sel WL,” and a drain select line “DSL1.” *See* Seo, [0086]-[0090]. With respect to “Sel WL,” a **voltage** is applied during **time period t1**, which is replaced by a “**read voltage Vread**” during a “**second time period t2**.” Seo, [0090]. With respect to the “Unsel WLs,” “the **pass voltage Vpass** may be applied to unselected word lines” during both a portion of **time period t1** as well as **time period t2**. Seo, [0089]. With respect to “DSL1,” it

receives a “voltage V2 ... during a first time period t1” before dropping to some other during time period t2. Seo, [0088].

FIG. 8



Seo, Fig. 8.

Seo is missing many relevant details regarding its read operation. The duration of the time periods is not specified in Seo, beyond the fact that the second time period is longer than the first time period. *See* Seo, [0075]. Similarly, Seo does not disclose specific voltage levels, beyond the fact that the voltages V1 and V2 may have the same value and are able to “turn on” the drain select transistors. *See* Seo, [0088]. And Seo does not disclose or otherwise suggest a voltage configuration for removing fast charges from a target memory when applied as part of a read-verification operation.

Petitioner incorrectly argues that Seo’s disclosed voltages would create an electric field that removes fast charges when applied as part of a hypothetical read-verification operation within a charge-trap 3D memory. *See* Pet., 29-31, 42-44. Specifically, the Petition mistakenly cites the ’342 at 12:24-34 for the proposition that any voltage difference between an unselected word line and selected word line removes fast charges (Pet., 42)—an incorrect proposition that the cited portion of the ’342 does not support. *See, e.g.,* ’342, 12:10-40 (discussing how certain embodiments of a read-verification operation can remove fast charges in the specific device described in Fig. 4A). Nothing in Seo suggests that Seo’s disclosed voltages would be sufficient to remove fast charges. Indeed, Seo does not even disclose the magnitude or duration of the applied voltages, much less that the resulting electric fields would remove fast charges during the first portion of a purported read-verification operation. *See* Seo, [0086]-[0090]. Moreover, even if Seo’s voltage could be theoretically modified to remove fast charges, “[t]he mere fact that a certain thing *may* result from a given set of circumstances is not sufficient” to show a feature is disclosed or rendered obvious. *In re Rijckaert*, 9 F.3d 1531, 1534 (Fed. Cir. 1993) (emphasis in original).

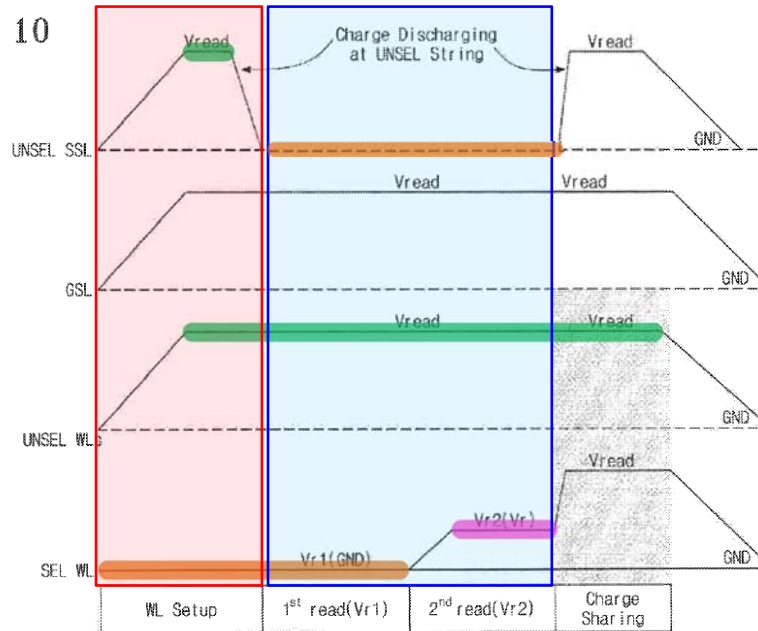
B. U.S. Pat. Pub. No. 2015/0003169 (“Nam”) (Ex. 1006)

Petitioner concedes that Nam does not anticipate the Challenged Claim. Rather, similar to Seo, Petitioner falls back to broken obviousness combinations of

Nam and Choi (Ground 2) that still fail to satisfy the Challenged Claim. *See* Pet., 9, 53-73. Nam is directed to a three-dimensional non-volatile memory device that “reduce[s] a read disturbance” by “sharing” channel charges prior to a recovery operation. *See* Nam, [0006], [0062], [0071]. Similar to Seo, Nam does not disclose or otherwise suggest any techniques for removing fast charges as part of a read-verification operation. Indeed, like Seo, Nam fails to contemplate the existence of fast charges, or that there is a benefit in removing them from a target memory cell following a programming step.

As depicted in Fig. 10, Nam discloses an “immune disturbance read operation” divided into multiple periods. During a **setup period**, Nam applies a “**read pass voltage Vread** to unselected string selection lines UNSEL SSL” and “unselected word lines UNSEL WLs” while applying a “**ground voltage**” to a “selected word line SEL WL.” *See* Nam, [0105], [0122]. During a later **sensing operation**, a “**ground voltage**” is applied to the unselected string selection lines and a “**read voltage Vr2**” is applied to selected word line, as **Vread** continues to be applied to the unselected word lines. *See* Nam, [0105]-[0106], [0122]. Nam provides an example value for Vread of “about 7V,” but does not disclose the duration of the setup period or the impact this voltage would have on fast charges. Nam [0098].

Fig. 10



Nam, Fig. 10.

Like Seo, Nam is missing relevant details regarding its read operation. Nam provides an example value for V_{read} of “about 7V,” but does not disclose the duration of the setup period. Nam [0098]. Nam also does not disclose or otherwise suggest that these voltages remove fast charges if used as part of a read-verification operation in the specific context of Nam’s memory structure.

Similar to Seo, Petitioner argues that Nam discloses “having a higher voltage on unselected WLs ... relative to the selected WL,” and mistakenly cites the ’342 at 12:24-34 for the proposition that this voltage difference is sufficient to remove fast charges (Pet. 66-68)—an incorrect proposition that the cited portion of the ’342 does not support. As before, nothing in Nam suggests that the disclosed voltages would be sufficient to remove fast charges. Just like Seo, Nam does not contemplate the

existence of fast charges, much less suggest that the magnitude and duration of the applied voltages would result in electric fields capable of removing fast charges during the first portion of a purported read-verification operation. *See generally* Nam, [0104]-[0136].

C. Choi et al., Comprehensive Evaluation of Early Retention (Fast Charge Loss Within a Few Seconds) Characteristics in Tube-Type 3-D NAND Flash Memory (“Choi”) (Ex. 1007)

Petitioner relies on Choi to address certain deficiencies in Seo and Nam as part of the obviousness combinations presented in Grounds 1-2, but Choi fails to fill in the gaps in the primary references. Choi is titled “Comprehensive Evaluation of Early Retention (Fast Charge Loss Within a Few Seconds) Characteristics in Tube-Type 3-D NAND Flash Memory,” and the authors are identified as members of Kookmin University in Seoul, Korea, and SK Hynix Inc. *See* Choi, header and footer.

Choi discloses simulations that examine “fast charge loss” phenomena (which it also refers to as “early retention” or “ $V_{T,loss}$ ”) arising in “tube-type 3-D NAND flash memory” devices using “charge trap” technology, and found that this unwanted behavior was associated with large lateral electric fields that linger within the memory cell following a sequence of erasing and programming operations. Choi, 1:1-12; *see also* Choi 1:14-24, 1:32-39.

Specifically, Choi simulated a memory cell that is “first erased prior to programming” using various different erasing levels (EV) and programming levels (PV). Choi 2:4-7. In each scenario, Choi observed that a “large lateral electric field” results from erasing and programming operations, which “indicates that the early retention mainly occurs through lateral charge loss in the shared charge trap layers rather than vertical charge loss.” Choi, 2:4-25; *see also* Choi 2:35-42 (stating the electric field is “mostly governed by the erased state of neighboring cells” or “non-compensated residual holes”). Based on the simulation, Choi concluded that “early retention mainly originates from the lateral charge loss through the shared charge trap layers,” and that “program and erase levels should be balanced and optimized” to reduce these effects. Choi, 1:1-12.

The Petition mischaracterizes this disclosure from Choi as teaching that the use of a “large lateral electric field” inherently removes fast charges, or that applying any “voltage differential” with a higher voltage to unselected word lines inherently removes fast charges. *See* Pet. 43-44, 68. But Choi says no such thing, and does not suggest any methods to actively remove fast charges that result from a programming operation. In fact, Choi disparages the large lateral electric fields that result from erasing and programming operations as a potential source of undesirable “early retention.” Choi 1:9-12. Choi says nothing about applying voltage differentials to different word lines or how to design electric fields to remove fast charges, and does

not otherwise suggest or render obvious that Seo's or Nam's purported teachings remove fast charges as part of a read-verification operation.

VI. PETITIONER FAILS TO ESTABLISH A REASONABLE LIKELIHOOD THAT IT WOULD PREVAIL WITH RESPECT TO THE CHALLENGED CLAIM

Petitioner fails to establish a reasonable likelihood that it would prevail with respect to the Challenged Claim because Petitioner has failed to show that the cited references disclose or render obvious the claimed read-verification operation to remove fast charges, as required by limitation [1.d] of independent claim 1 or the situation where the “voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell,” which is recited as part of this read-verification operation by dependent claim 7. As explained below, both of Petitioners grounds challenging claim 7 (which depends from claim 1) fail: (Ground 1) obviousness based on Seo and Choi and (Ground 2) obviousness based on Nam and Choi.

First, Seo in view of Choi does not disclose or render obvious “remov[ing] fast charges” during the first time period of the claimed read-verification operation as recited in limitation [1.d]. Petitioner seemingly concedes that Seo does not contemplate the existence of fast charges, and instead argues based on the faulty premise that a POSITA would have understood Seo's read operation as inherently removing fast charges. Petitioner's argument misrepresents the '342 and Choi as

suggesting that any voltage difference between unselected and selected word line (or resulting electric fields) would inherently remove fast charges—the '342 and Choi say no such thing. Indeed, Choi fails to disclose removing fast charges as part of a read-verification operation, and there is no evidence that its teachings on “large lateral electric fields” are applicable to Seo. Moreover, Petitioner’s proposed combination employs Seo’s read operation in Choi’s charge-trap memory, but there is no evidence that removal of fast charges is inherent in or rendered obvious by such a combination.

Second, Seo in view of Choi also does not disclose or render obvious a “voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell” as required by dependent claim 7. Indeed, Petitioner’s argument for claim 7 directly contradicts its argument for element [1.b], suggesting that the same voltage is both a “threshold voltage” that turns on memory cells and an “off voltage” that does not turn on memory cells. Specifically, the Petition argues that Fig. 8 of Seo depicts a voltage of “0V” being applied to the unselected top select gate at the relevant time and that this is a threshold voltage that turns on a memory cell. But Petitioner previously argued for element [1.b] that the same voltage value of “0V” acts as an “off voltage” that does not turn on the memory cell when applied to the selected wordline.

Third, Nam in view of Choi also does not disclose or render obvious “remov[ing] fast charges” during the first time period of the claimed read-verification operation as recited in limitation [1.d]. Like for Seo, Petitioner seemingly concedes that Nam does not contemplate the existence of fast charges, and instead argues based on the faulty premise that a POSITA would have understood Nam’s read operation as inherently removing fast charges. As before, Petitioner’s cites the ’342 and Choi for the incorrect proposition that any voltage difference between unselected and selected word line (or resulting electric fields) would inherently remove fast charges, and Petitioner’s combination with Choi further fails for the same reasons as in Ground 1.

Fourth, Nam in view of Choi also does not disclose or render obvious a “voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell” as further required by dependent claim 7. As before, Petitioner’s argument for claim 7 directly contradicts its argument for element [1.b], suggesting that the same ground voltage is both a “threshold voltage” that turns on memory cells and an “off voltage” that does not turn on memory cells when applied to the selected word line.

Because each of Petitioner’s Grounds fails to disclose or render obvious the Challenged Claim, the Board should deny institution.

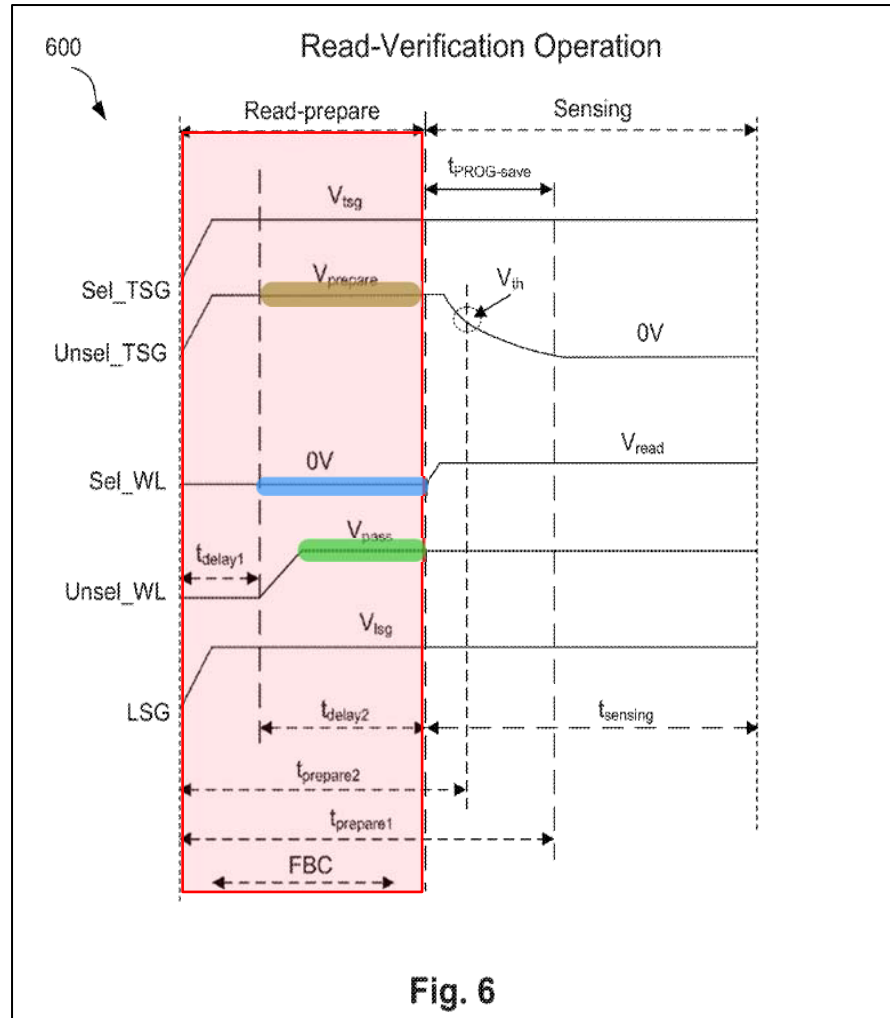
A. Ground 1: Seo in View of Choi Does Not Disclose or Render Obvious the claimed Read-Verification Operation that “Removes Fast Charges” of the Target Memory Cell “During [a] First Time Period”

Seo in view of Choi does not disclose or render obvious limitations [1.d] because Seo and Choi fail to disclose or otherwise render obvious removing fast charges during a first time period of a read-verification operation. The Petition relies on Seo as purportedly disclosing the use of a “prepare voltage,” an “off voltage,” and a “pass voltage” during a “first time period,” but seemingly concedes that Seo does not teach that the identified “voltages” removes fast charges. *See* Pet. 35-44. Instead, the Petition mischaracterizes the ’342 and Choi as suggesting that Seo’s voltages would necessarily or inherently remove fast charges when applied as part a read-verification operation. *See* Pet., 42-44. But the ’342 says no such thing, and Choi does not teach or otherwise suggest that Seo’s read-verification operation would remove fast charges in the proposed combination. Indeed, Seo does not even disclose the particular voltages being applied during its read-verification operation. Thus, the Petition fails to show that Seo (with or without the benefit of Choi) discloses or otherwise renders obvious the claimed read-verification operation that “removes fast charges of the target memory cell during the first time period” as required by the Challenged Claim.

Claim 1 of the ’342 recites a method for conducting a read-verification operation that includes applying a “prepare voltage” on an unselected top select gate,

an “off voltage” on a selected word line, and a “pass voltage” on an unselected word line during a first time period (*see* Elements [1.a]-[1.c]), **“wherein the read-verification operation removes fast charges of the target memory cell during the first time period”** (Element [1.d]).

As explained in Section II, the claimed invention of the ’342 improves read-verification operations, in part, by selectively applying voltages to an unselected top select gate, a selected word line, and an unselected word line such that the “read-verification operation removes fast charges of the target memory cell during the first time period.” ’342, Claim 1. For example, as shown in Figure 6 below, the ’342 teaches applying “a **prepare voltage**” on an unselected top select gate (“Unsel_TSG”), an **“off voltage”** on a selected word line (“Sel_WL”), and a **“pass voltage”** on an unselected word line (“Unsel_WL”) during a **first time period** in order to remove fast charges prior to sensing the value of the programmed memory cell in a second time period. *See* ’342, 1:55-61, 11:11-33.



'342, Fig. 6 (annotated). The '342 discloses using this technique to remove fast charges during the **first time period**. Depending on the structure of the device, the voltages applied, and the time period of the read-prepare operation, for example, “an electric field parallel to the channel can be established” based on the voltages applied that “extends into the charge storage layer 424, the tunneling layer 426, and the channel layer 338” sufficient to “de-trap the fast charges” so that they can be “recombined ... or be removed through the conductive path established in the channel of the unselected memory cells.” '342, 9:39-46, 12:24-34.

By comparison, Petitioner seemingly concedes that Seo does not teach any of its disclosed voltages being used to remove fast charges. *See* Pet., 42-44. As discussed in Section V.A, Seo does not acknowledge the existence of fast charges, and does not discuss any techniques for removing fast charges during a read-verification operation. Rather, Seo is concerned with trying to mitigate unrelated sources of read disturb stemming from “Hot Carrier Injection,” which occurs in a different location entirely. Seo, [0089], [0127]. Indeed, “fast charges” relate to shallowly trapped electrons in the memory cell storage layer, while “hot carrier injection” is a distinct phenomenon that takes place in the channel of the memory cell string. *Compare* Seo [0104] (“hot carriers ... may be present in a channel of the unselected memory string”) *with* ’342 2:45-47 (“removing the fast charges includes removing the fast charges from a storage layer of the target memory cell”).

Petitioner makes two flawed arguments in an attempt to address Seo’s deficiencies—both premised on the incorrect assertion that Seo’s voltages inherently remove fast charges. *See* Pet., 42-44. First, the Petition argues that Seo discloses having a “**higher voltage on unselected WLs**” as compared to selected word lines (*see* Pet., 42 (citing Seo, [0082]-[0083], [0088]-[0090])), and incorrectly asserts that “[a]s the ’342 patent recognizes, **this voltage differential removes fast charges.**” Pet., 42 (citing ’342, 12:24-34). In other words, Petitioner mistakenly argues that having a higher voltage on unselected WLs inherently removes fast charges. Second,

Petitioner argues that Seo creates a large lateral electric field and “it would have been obvious to employ Seo’s read operation in a 3D charge-trap memory ***with the knowledge that it removes fast charges in view of Choi.***” Pet. 43-44. Thus, Petitioner is mistakenly arguing that a large lateral electric field is taught by Seo, and that if applied in a 3D charge-trap memory, this voltage inherently removes fast charges. Both arguments are without merit, as explained below, and Petitioner has failed to demonstrate that Seo (or Seo in view of Choi) discloses or otherwise renders obvious the claimed read-verification operation that removes fast charges during a first time period as required by the Challenged Claim.

First, with respect to Petitioner’s argument that Seo purports to use a “higher voltage on unselected WLs” as compared to neighboring selected word lines, and that the ’342 supposedly recognizes this voltage difference as inherently removing fast charges (see Pet., 42 (citing ’342, 12:24-34); see also Seo, [0082]-[0083]), the ’342 does not state or even suggest that a mere difference between unselected and selected word line voltages will necessarily remove fast charges. Rather, the ’342 states that within the context of the memory cell structure in Fig. 4A and the voltages and timing depicted in Fig. 6, “an electric field parallel to the channel can be established” that “extends into the charge storage layer 424, the tunneling layer 426, and the channel layer 338” sufficient to “de-trap the fast charges” so that they can be “recombined ... or be removed through the conductive path established in the

channel of the unselected memory cells.” ’342 12:24-34. These statements do not suggest that Seo’s voltage amounts applied during Seo’s time period operate the same way on Seo’s memory device to generate fields with sufficient magnitude and duration to remove fast charges. Indeed, Seo says nothing about the actual voltages used during the first time period, how long the voltages are applied, or how those relate to removing fast charges in the context of Seo’s particular device. The mere possibility of removing fast charges is insufficient—under binding Federal Circuit law, “[t]he mere fact that a certain thing *may* result from a given set of circumstances is not sufficient” to show that thing is disclosed or rendered obvious. *In re Rijckaert*, 9 F.3d at 1534 (reversing rejections based on an argument that an optimal condition matching signal time to recording time was inherent in the recording prior art, where the prior art failed to disclose the means of achieving that optimal condition); *see also* MPEP 2112.

Second, Petitioner’s argument based on the combination with Choi fares no better. As explained above, Petitioner argues that Seo’s read operation would be applied to 3D charge-trap memory “with the knowledge that it removes fast charges in view of Choi,” which allegedly teaches that a “large lateral electric field” removes fast charges. Pet. 42-44. According to Petitioner, “Seo creates such ‘a large electric field.’” *Id.* at 44. As an initial matter, Seo never states that it creates a large electric field. Tellingly, Petitioner provides no citation for its assertion that Seo creates a

large electric field, other than the conclusory, unexplained assertion of its expert. *See* Pet. 44; Liu ¶138. Indeed, Seo does not discuss electric fields at all. Thus, there is no basis for Petitioner’s assumption that Choi’s teachings on large electric fields are applicable to understanding how Seo operates.

Even if Seo created a large electric field (again, something it never states or suggests), Choi does not teach that a “large lateral electric field” inherently removes fast charges. Rather, as discussed in Section V.C, Choi discloses simulations to examine “fast charge loss” phenomena and concludes that “program and erase levels should be balanced and optimized” to reduce the effects of fast charge losses. Choi, 1:1-12. In fact, Choi disparages large lateral electric fields as potentially contributing to this undesirable “early retention” phenomenon. *See* Choi 1:9-12. Specifically, Choi’s simulations show that a “large lateral electric field” potentially results from certain erasing and programming operations, which “indicates that the [fast charge loss] mainly occurs through lateral charge loss in the shared charge trap layers rather than vertical charge loss.” Choi, 2:4-25; *see also* Choi 2:35-42. But Choi does not disclose applying voltages to different word lines to generate electric fields or under what specific circumstances such generated fields would remove fast charges following a programming operation.

Finally, Petitioner’s proposed combination appears to involve “employ[ing] Seo’s read operation in Choi’s charge-trap memory” (Pet. 44, 50), but there is no

evidence that removal of fast charges is inherent in or rendered obvious by such a combination. Specifically, there is nothing in either Seo or Choi to suggest that Seo's voltages applied during Seo's time period (i.e., Seo's read operation) would operate on Choi's charge-trap memory to remove fast charges, as required by the Challenged Claim. Again, Seo does not even disclose the particular voltages or durations involved in its read operation. At most, Petitioner has suggested mere possibility, which is not sufficient to show that removing fast charges is inherent in or rendered obvious by the proposed combination. *In re Rijckaert*, 9 F.3d at 1534.

For at least the reasons provided above, Petitioner's Ground 1 fails because Seo and Choi, alone or in combination, fail to disclose or render obvious that the claimed "read-verification operation removes fast charges of the target memory cell during the first time period," as required by element [1.d] of the Challenged Claim.

B. Ground 1: Seo in View of Choi Does Not Disclose or Render Obvious "a Voltage of the Unselected Top Select Gate Equals to a Threshold Voltage of an Unselected Memory Cell"

Seo in view of Choi also does not disclose or render obvious "applying the read voltage when a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell" as required by claim 7 (the only Challenged Claim) because Petitioner's only argument is inconsistent with its argument for element [1.b]. Rather, Petitioner relies on the same voltage as both a "threshold voltage" that turns on unselected memory cells (*see* claim 7) and an "off voltage"

that turns off memory cells when applied to a selected word line (see element [1.b]). Setting aside whether Petitioner's arguments are even correct, Petitioner's Ground 1 fails because it does not present a mapping that consistently addresses the entire Challenged Claim.

Claim 7 depends from claim 1, and further requires that **“applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell.”** See '342 Claim 7.

Petitioner's only argument for claim 7 is inconsistent with its argument for element [1.b], and therefore there is no one mapping that consistently addresses the entire Challenged Claim. The Petition presents the same 0V value as both the threshold voltage that “turns on” the transistors in the memory cells, and somehow also an “off voltage” that “does not turn on” the transistors.

For claim 7, the Petition relies on 0V as the threshold voltage that **“turns on”** transistors in erased memory cells. Specifically, the Petition argues that Fig. 8 of Seo depicts a voltage of “0V” being applied to the unselected top select gate at the relevant time, and relies on testimony from its expert (Dr. Liu) to argue “it would have been understood, or at least obvious, that 0V equals to a threshold voltage of an unselected memory cell, e.g., an erased cell.” Pet. 46 (citing Liu ¶¶ 148-49). Dr. Liu explains that the term “threshold voltage” refers to the “gate voltage that **turns**

on the transistor.” Ex. 1003 ¶46 (emphasis added). But that argument directly contradicts Petitioner’s argument with respect to element [1.b], where Petitioner argues that 0V is an “off voltage” that **does not turn on** the transistors. Specifically, Petitioner argues a “zero voltage—an off voltage—is applied to a selected word line.” Pet. 40. Indeed, Petitioner states that a voltage “is an off voltage because it **does not turn on** the transistor.” Pet. 60 (emphasis added).

In other words, the Petition inconsistently suggests that the same voltage value of 0V is both a “threshold voltage” that would turn on the memory cell transistors (e.g., any “erased cell”), while also acting as an “off voltage” that would “not turn on” a memory cell transistor (e.g., an erased cell) according to Petitioner. See Pet. 39-41, 45-49, 60. Thus, Petitioner’s mappings for different elements of the Challenged Claim directly contradict each other.

For at least the reasons provided above, Petitioner’s Ground 1 fails because Seo and Cho fail to disclose or render obvious the entire Challenged Claim, including claim 7’s requirement of “a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell” in combination with the other limitations recited by independent claim 1, from which claim 7 depends.

C. Ground 2: Nam in View of Choi Does Not Disclose or Render Obvious a Read-Verification Operation That “Removes Fast Charges” of the Target Memory Cell “During [a] First Time Period”

Nam in view of Choi does not disclose or render obvious limitations [1.d] because Nam and Choi fail to disclose or otherwise render obvious removing fast charges during a first time period of a read-verification operation. Similar to Ground 1, Petitioner relies on Nam as purportedly disclosing the use of a “prepare voltage,” an “off voltage,” and a “pass voltage” during a “first time period,” but seemingly concedes that Nam does not teach that the identified voltages remove fast charges. *See* Pet. 62-68. As before, Petitioner instead mischaracterizes the ’342 and Choi as somehow suggesting that the identified voltage in Nam would necessarily or inherently remove fast charges if applied as part of a read-verification operation. *See* Pet., 56, 68. Like in Ground 1, the Petition’s misplaced arguments fail to show that Nam (with or without the benefit of Choi) discloses or otherwise renders obvious the claimed read-verification operation that “removes fast charges of the target memory cell during the first time period” as required by the Challenged Claim.

Claim 1 of the ’342 recites a method for conducting a read-verification operation that includes applying a “prepare voltage” on an unselected top select gate, an “off voltage” on a selected word line, and a “pass voltage” on an unselected word line during a first time period (*see* Elements [1.a]-[1.c]), “**wherein the read-**

verification operation removes fast charges of the target memory cell during the first time period” (Element [1.d]).

As discussed above, the claimed invention of the ’342 improves read-verification operations, in part, by selectively applying voltages to an unselected top select gate, a selected word line, and an unselected word line such that the “read-verification operation removes fast charges of the target memory cell during the first time period.” ’342, Claim 1. *See* Section II. In contrast, Petitioner seemingly concedes that Nam makes no mention of removing fast charges, and instead tries relying on either the ’342 or Choi as somehow demonstrating that Nam’s use of a “higher voltage on unselected WLs” would inherently remove fast charges in a read-verification operation. *See* Pet., 67-68.

The Petition’s arguments with respect to Nam are similar to the Ground 1 arguments. *See* Pet., 67-68. First, the Petition argues that Nam “teaches having a higher voltage on unselected WLs (including WLs adjacent to the selected WL) relative to the selected WL during the [purported] first period,” and incorrectly cites the ’342 as evidence that “this creates a lateral electric field that removes fast charges.” *See* Pet., 59-60, 67-68 (citing ’342, 12:24-34). Thus, Petitioner again is mistakenly arguing that having a higher voltage on unselected WLs inherently removes fast charges. Second, Petitioner mischaracterizes Choi as teaching that a “voltage differential removes fast charges” and, based on this assertion, argues that

“in view of Choi, a POSITA would have understood that Nam’s read-verification operation removes fast charges.” *See* Pet., 67-68. Thus, Petitioner is once again mistakenly arguing that having a higher voltage on unselected WLs inherently removes fast charges or renders doing so obvious. For similar reasons discussed for Ground 1, both arguments fail.

First, Petitioner argues that Nam purportedly teaches “having a higher voltage on unselected WLs (including WLs adjacent to the selected WL) relative to the selected WL during the [purported] first period,” and that the ’342 supposedly recognizes this voltage difference as inherently removing fast charges (*see* Pet., 59-60, 67-68 (citing ’342, 12:24-34); *see also* Nam, [0094]-[0096], [0098], [0104]-[0106], [0122]), but as explained above for Ground 1, Petitioner has not actually shown that removing fast charges is inherent. The ’342 does not suggest that the mere difference between the unselected and selected word line will necessarily remove fast charges, and there is nothing in Nam (or in the ’342) to suggest that Nam’s disclosed voltages would function in an identical manner to those described in the preferred embodiments of the ’342. In other words, there is no suggestion that Nam’s voltages applied during Nam’s time period operate the same way on Nam’s memory device to generate fields with sufficient magnitude and duration to remove fast charges. The mere possibility of removing fast charges is insufficient. *In re Rijckaert*, 9 F.3d at 1534.

Second, Petitioner’s argument based on the combination with Choi also fails. As explained above, Petitioner misrepresents Choi as “expressly teach[ing] that voltage differential removes fast charges,” and that, “in view of Choi, a POSITA would have understood that Nam’s read-verification operation removes fast charges.” Pet. 66-68 (cross-referencing the discussion of Seo with respect to limitation [1.d]). As an initial matter, Petitioner previously characterized Choi’s teachings as only suggesting that fast charges “are more likely to be lost” in the presence of “a large lateral electric field” (Pet. 43-44 (Ground 1)), rather than a mere voltage differential. Indeed, Petitioner’s argument using Choi for Ground 2 merely cross-references that prior analysis and cites to no other portion of Choi. Pet. 82. Yet Nam does not disclose or suggest that its read-verification operation creates a large lateral electric field. In fact, Petitioner has not even argued that Nam creates a large lateral electric field. Thus, there is no basis for Petitioner’s reliance on Choi for understanding whether Nam removes fast charges.

In any event, contrary to Petitioner’s conclusory assertion, Choi has no broader “express teachings” that any “voltage differential” removes fast charges—the term “voltage differential” does not even appear in Choi. Rather, as discussed before, Choi disclose various simulations examining “fast charge loss” phenomena in the context of its particular structure. See Section V.C. Specifically, Choi’s simulations show that “early retention mainly originates from the lateral charge loss

through the shared charge trap layers,” and that “program and erase levels should be balanced and optimized” to reduce these effects. Choi, 1:1-12. Choi does not disclose applying voltages to different word lines, or under what specific circumstances those voltages would remove fast charges following a programming operation. The proposed combination appears to rely on Choi for the limited purpose of understanding how Nam operates (Pet. 68), rather than modifying Nam, but there is nothing in either Nam or Choi to suggest that Nam’s voltages applied during Nam’s time period would operate on Nam’s memory device to remove fast charges, as required by the Challenged Claim. Moreover, to the extent the proposed combination uses Choi’s charge-trap memory, there is nothing in either Nam or Choi to suggest that Nam’s voltages applied during Nam’s time period (i.e., Nam’s read operation) would operate on Choi’s charge-trap memory to remove fast charges, as required by the Challenged Claim. At most, Petitioner has suggested mere possibility, which is not sufficient to show that removing fast charges is inherent or obvious in the proposed combination. *In re Rijckaert*, 9 F.3d at 1534.

For at least the reasons provided above, Petitioner’s Ground 2 fails because Nam and Choi, alone or in combination, do not disclose or render obvious a “read-verification operation removes fast charges of the target memory cell during the first time period,” as required by element [1.d] of the Challenged Claim.

D. Ground 2: Nam in View of Choi Does Not Disclose or Render Obvious “a Voltage of the Unselected Top Select Gate Equals to a Threshold Voltage of an Unselected Memory Cell”

Nam in view of Choi also does not disclose or render obvious “applying the read voltage when a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell” as required by claim 7 (the only Challenged Claim). Just as with Ground 1, Petitioner’s only argument is inconsistent with its argument for element [1.b], and relies on the same voltage as both a “threshold voltage” that turns on unselected memory cells (*see* claim 7) and an “off voltage” that turns off memory cells when applied to a selected word line (*see* element [1.b]). Again setting aside whether Petitioner’s arguments are even correct, Petitioner’s Ground 2 fails because it does not present a mapping that consistently addresses the entire Challenged Claim.

Claim 7 depends from claim 1, and further requires that **“applying the read voltage during the second time period comprises applying the read voltage when a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell.”** *See* ’342 Claim 7.

Similar to Ground 1, Petitioner’s only argument for claim 7 is inconsistent with its argument for element [1.b], and therefore there is no one mapping that consistently addresses the entire Challenged Claim. The Petition again presents the same ground voltage disclosed by Nam as both the threshold voltage that “turns on”

the memory cell transistors, and somehow also an “off voltage” that “does not turn on” the transistors.

For claim 7, the Petition relies on ground as the threshold voltage that “**turns on**” transistors in erased memory cells. Specifically, the Petition identifies Nam’s use of ground in Fig. 10 as the purported “voltage of the unselected top select gate,” and relies on its expert Dr. Liu’s testimony to argue that this “equals to a threshold voltage of an unselected memory cell, e.g., an erased cell.” Pet. 69. As discussed for Ground 1, Dr. Liu explains that the term “threshold voltage” refers to the “gate voltage that **turns on** the transistor.” Ex. 1003 ¶46 (emphasis added). In other words, Petition’s claim 7 argument is that a ground voltage will turn on erased memory cells.

But as before, that claim 7 argument directly contradicts Petitioner’s argument with respect to element [1.b], where Petitioner argues that ground is an “off voltage” that **does not turn on** the transistors. Specifically, Petitioner relies on Dr. Liu’s testimony to suggest that Nam discloses “applying, on a selected word line associated with the target memory cell (e.g., SEL WL), the off voltage during the first time period (e.g., Ground during WL Setup).” Pet. 64 (citing, Liu ¶¶209-13). Indeed, as explained for Ground 1, Petitioner states that a voltage “is an off voltage because it **does not turn on** the transistor.” Pet. 60 (emphasis added).

In other words, the Petition inconsistently relies on the same ground voltage value as both a “threshold voltage” that would turn on the memory cell transistors

(e.g., any “erased cell”), while also acting as an “off voltage” that would not turn on a memory cell transistor (e.g., an erased cell) according to Petitioner. *See* Pet. 62-64, 68-71, 60. Thus, Petitioner’s mappings for different elements of the Challenged Claim directly contradict each other.

For at least the reasons provided above, Petitioner’s Ground 2 also fails because Nam and Cho fail to further disclose or render obvious the entire Challenged Claim, including claim 7’s requirement of “a voltage of the unselected top select gate equals to a threshold voltage of an unselected memory cell” in combination with the other limitations recited by claim 1.

VII. CONCLUSION

The Petition should be denied institution as Petitioner has failed to establish a likelihood that it would prevail with respect to the Challenged Claim based on the grounds presented in the Petition.

Dated: September 13, 2024

Respectfully submitted,

ROPES & GRAY LLP

By: /James L. Davis, Jr./

James L. Davis, Jr.

Reg. No. 57,325

ROPES & GRAY LLP

1900 University Avenue, 6th Floor

East Palo Alto, CA 94303-2284

Telephone: +1-650-617-4794

James.L.Davis@ropesgray.com

Andrew T. Radsch

(*pro hac vice* forthcoming)

ROPES & GRAY LLP

1900 University Avenue, 6th Floor

East Palo Alto, CA 94303-2284

Telephone: +1-650 617 4763

Andrew.Radsch@ropesgray.com

Christopher M. Bonny

Reg. No. 63,307

ROPES & GRAY LLP

1900 University Ave., 6th Floor

East Palo Alto, CA 94303-2284

Telephone: +1-650-617-4011

Christopher.Bonny@ropesgray.com

Abed R. Balbaky

Reg. No. 76,154

ROPES & GRAY LLP

1211 Avenue of the Americas

New York, NY 10036-0003

Telephone: +1-212-841-5797

Abed.Balbaky@ropesgray.com

*Attorneys for Patent Owner, Yangtze
Memory Technologies Co. Ltd.*

CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 complies with the type-volume limitation in 37 C.F.R. § 42.24(b)(1). According to the word-processing system's word count, the brief contains 9,154 words, excluding the parts of the brief exempted by 37 C.F.R. § 42.24.

Dated: September 13, 2024

Respectfully submitted,

By: /Abed R. Balbaky/
Abed R. Balbaky
Reg. No. 76,154
ROPES & GRAY LLP

CERTIFICATE OF SERVICE

The undersigned certifies that the foregoing PATENT OWNER'S PRELIMINARY RESPONSE UNDER 37 C.F.R. § 42.107 was served in its entirety by filing through the Patent Trial and Appeal Case Tracking System (P-TACTS), as well as providing a courtesy copy via e-mail to the following attorneys of record for Petitioner listed below:

Lead Counsel	Back-up Counsel
Jeremy Jason Lang Registration No. 73,604 (jlang@orrick.com) Postal & Hand-Delivery Address: Orrick, Herrington & Sutcliffe LLP 1000 Marsh Road Menlo Park, CA 94025 T: 650-614-7400; F: 650-614-7401 P52PTABDocket@orrick.com PTABDocketJL2@orrick.com PTABDocketJ3B3@orrick.com PTABDocketJ1H1@orrick.com	Jared Bobrow <i>Pro Hac Vice</i> (jbobrow@orrick.com) K. Patrick Herman Registration No. 75,018 (pherman@orrick.com) Johannes Hsu Registration No. 74,689 (johanneshsu@orrick.com)
<i>Counsel for Petitioner Micron Technology, Inc.</i>	

Dated: September 13, 2024

By: /Jonathan Bradford/
Name: Jonathan Bradford

ROPES & GRAY LLP