

OPEN MULTIMEDIA APPLICATION PLATFORM: ENABLING MULTIMEDIA APPLICATIONS IN THIRD GENERATION WIRELESS TERMINALS THROUGH A COMBINED RISC/DSP ARCHITECTURE

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ABSTRACT

This paper describes how multimedia applications will be enabled in 3G wireless terminals thanks to the efficiency of the DSP core embedded in the TI Open Multimedia Application Platform (OMAP). OMAP H/W architecture will be described, with an emphasis on how multimedia applications (video, audio, speech) will benefit from this advanced architecture. The paper will also depict the advantages provided by a combined RISC/DSP architecture, compared to a single RISC architecture, for 3G multimedia mobile applications.

1. INTRODUCTION

Wireless handset contains 2 parts: The modem part and the applications part. The modem sends data to the network via the air interface and retrieves data from the air interface. The application part performs the functions that the user wants to have in his phone: Speech, audio, image and video, e-mail, e-commerce, fax, transmission as well as internet connections are first examples of some applications using wireless modem. Some other applications improve user interface: voice (name dialing, acoustic echo cancellation), Keyboard (T9), handwritten (character recognition). Most other applications entertain the user (Games ..), help him organize his time (PDA functionality, memo) and are very numerous. Since bandwidth in the air-transmission is limited and expensive, speech, audio image and video signals will be heavily compressed before transmission and this compression requires extensive signal processing.

The modem function required traditionally a DSP for signal processing of low layer modem and a RISC processor for upper layers. Similarly, some applications (speech, audio, video compression...) require extensive signal processing and therefore should be mapped to DSP to consume minimum power while other applications might be better mapped to RISC processors.

Depending on the number of applications and on the processor performances, the DSP and/or the micro-controller used for the modem can also be used for the application part. However for

high-end phones featuring a lot of applications enabled by the high bit rate of 2.5G and 3G, a separate DSP and RISC will be required. The Open Multimedia Application Platform (OMAP) is this platform, based on a RISC and a DSP.

In addition to enabling the numerous, media rich application made possible by 2.5G and 3G data rate, the OMAP also addresses a new capability: The capability for the applications to be dynamically downloaded from the Web. This capability requires the OMAP platform to handle dynamic environment, both on the DSP and RISC side.

2. OMAP H/W ARCHITECTURE

The OMAP hardware architecture, depicted in Figure 1, is designed to maximize the overall system performance of the 3G terminals while minimizing power consumption. This is achieved through the use of TI's state of the art TMS320C55x DSP core and high performance ARM925T CPU. Both processors utilize a cached architecture to reduce the average access time to instruction memory and eliminate power hungry external accesses. In addition both cores have a memory management unit (MMU) for virtual to physical memory translation and task-to-task protection.

The OMAP core also contains two external memory interfaces and one internal memory port. The first supports a direct connection to synchronous DRAMs at up to 100MHz. The second external interface supports standard asynchronous memories such as SRAM, FLASH, or burst FLASH devices. This interface is typically used for program storage and can be configured as 16 or 32 bits wide. The internal memory port allows direct connection to on chip memory such as SRAM or embedded FLASH and can be used for frequently accessed data such as critical OS routines or the LCD frame buffer. This has the benefit of reducing the access time and eliminating costly external accesses. All three interfaces are completely independent and allow concurrent access from either processor or DMA unit.

The OMAP core also contains numerous interfaces to connect to peripherals or external devices. Each processor has its own

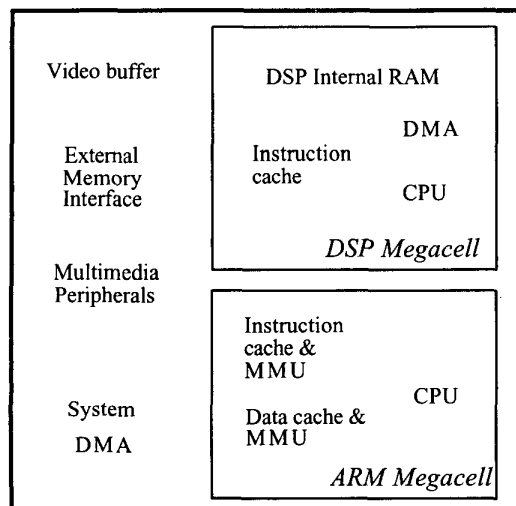


Figure 1: OMAP Architecture

external peripheral interface that supports direct connection to peripherals. To improve system efficiency these interfaces also support DMA from the respective processor's DMA unit. The Local Bus interface is a high-speed bi-directional multi-master bus that can be used to connect to external peripherals or additional OMAP based devices in a multi-core product.

Additionally, a High Speed Access Bus is available to allow an external device to share the main OMAP system memory (SDRAM, FLASH, internal memory). This interface provides an efficient mechanism for data communication and also allows the designer to reduce system cost by reducing the number of external memories required in the system.

In order to support common operating system requirements several peripherals are included such as timers, general purpose io, a UART, and watch dog timers. These peripherals are intended to be the minimum peripherals required in the system. Additional peripherals can be added on the Rhea interfaces. A color LCD controller is also included to support a direct connection to the LCD panel. The ARM DMA engine contains a dedicated channel that is used to transfer data from the frame buffer to the LCD controller where the frame buffer can be allocated in the SDRAM or internal SRAM.

3. ADVANTAGES OF A COMBINED RISC/DSP ARCHITECTURE COMPARED TO A RISC-ONLY SOLUTION

As depicted in the previous section, OMAP architecture is based on a combination of a RISC (ARM925) and a DSP (TMS320C55x). A RISC architecture, like ARM925, is best suited for control type code (OS, User Interface, OS applications), whereas a DSP is best suited for signal processing application, such as MPEG4 video, Speech applications, audio application.

A comparative benchmarking study has shown that executing a signal processing task would consume 3 times more cycles when executed on latest RISC machines (even featuring DSP extensions), compared to a TMS320C55x DSP. In terms of power consumption, it has been shown that a given signal-processing task executed on such a RISC engine would consume more than twice the power consumption required to execute the same task on a TMS320C55x architecture. The battery life, critical for mobile applications, will therefore be much higher in a combined architecture like OMAP rather than a RISC only platform.

For instance, a single TMS320C55x DSP can process in real-time a full visio-conferencing application (audio and video at 15 images/s), using only 40% of the total CPU computation capability. 60% of the CPU is therefore still available to run other applications at the same time. Moreover, in dual core architecture like OMAP, the RISC processor CPU is in that case fully available to run the operating system and its related applications. Typically, a mobile user would therefore still have access to his usual OS applications (Word, Excel...) while processing a full vision conferencing application.

A single RISC architecture would have to use its full CPU computation capability to execute only the Visio conferencing application, for twice the power consumption of the TMS320C55x. Therefore, the mobile user will not be able to execute any other application in the same time. Moreover, the battery life will be dramatically reduced.

4. TMS320C55X DSP MULTIMEDIA EXTENSIONS

The TMS320C55x DSP offers a highly optimized architecture for wireless modem and high-end applications execution. Corresponding code size and power consumption are also optimized at system level. These features also benefit a wider range of applications with some trade-offs in performance or power consumption.

The flexible architecture of the TI DSP hardware core allows extension of the core functions for multi-media specific operations. To facilitate the demands of the multi-media market for real time low power processing of streaming video and audio, the TMS320C55x family devices is the first DSP with such core level multi-media specific extensions. The software developer has access to the multi-media extensions using the *copr()* instruction as described in table 1, using combinations of TMS320C55x arithmetic instructions to create the desired dataflow.

Function of « Copr » opcodes	
<i>copr()</i>	Qualify instruction
<i>Copr(k6)</i>	Qualify instruction, pass k6 constant to MME control interface
<i>Smem=ACx, copr()</i>	Qualify instruction, write accumulator to memory (16-bit)
<i>Lmem=ACy, copr()</i>	Qualify instruction, write accumulator to memory (32-bit)

Table 1 : Description of the « copr » opcodes

Table 2, below, indicates all dataflow modes that can be built using the combination of arithmetic instructions and above opcodes.

DSP multimedia extension dataflow modes available :
<i>ACy = copr(k8, ACx, ACy)</i>
<i>ACy = copr(k8, ACx, ACy), Smem=ACz</i>
<i>ACy = copr(k8, ACx, ACy), dbl(Lmem)=ACz</i>
<i>ACy = copr(k8, ACx, Smem)</i>
<i>ACy = copr(k8, ACx, Xmem), Ymem=ACz</i>
<i>ACy = copr(k8, ACx, dbl(Lmem))</i>
<i>ACy = copr(k8, ACx, dbl(Xmem)), dbl(Ymem)=ACz</i>
<i>ACy = copr(k8, ACx, Xmem, Ymem)</i>
<i>ACx, ACy = copr(k8, ACx, ACy, Xmem, Ymem)</i>
<i>ACx = copr(k8, Ymem, Coef), mar(Xmem)</i>
<i>ACx = copr(k8, ACx, Ymem, Coef), mar(Xmem)</i>
<i>ACx, ACy = copr(k8, Xmem, Ymem, Coef)</i>
<i>ACx, ACy = copr(k8, ACy, Xmem, Ymem, Coef)</i>
<i>ACx, ACy = copr(k8, ACx, ACy, Xmem, Ymem, Coef)</i>

Table 2 : dataflow modes.

One of the first application domains that will extend the functionality of Wireless terminals is Video processing. Motion Estimation, Discrete Cosine Transform (DCT) and its inverse function (iDCT) and pixel interpolation are the most consuming in terms of number of cycles for a pure software implementation

using the TMS320C55x processor. Consequently these three are the first multi-media programming extensions that the TMS320C55x supports.

Table 3 summarizes the extension's characteristics. The overall video codec application mentioned earlier is accelerated by a factor of 2 using the extensions versus a classic software implementation. By reducing cycle count, the DSP real time operating frequency and, thus, the power consumption is also reduced.

HWA Type	Power Consumption (at max VDD)	Speed-up Factor
Motion Estimation	0.07 mA/MHz	x5.2
DCT/iDCT	0.09 mA/MHz	x4.1
Pixel interpolation	0.02 mA/MHz	x7.3

Table 3: Video Hardware Accelerators characteristics

Table 4, below, summarizes performance and current consumption (at maximum and lowest possible supply voltage) of a TMS320C55x video MPEG4 Coder/Decoder using multi-media extensions, for various image rates and formats.

Formats and rates	Millions of Cycles/s	mA @1.5 V (15C035)	mA @ 0.9V (15C035)
QCIF, 10 fps	18	12	7
QCIF, 15 fps	28	19	11
QCIF, 30 fps	55	37	22
CIF, 10 fps	73	49	29
CIF, 15 fps	110	74	44

Table 4 : MPEG4 Video Codec performance and Power

5. OMAP VIDEO APPLICATION

Video applications include two-way videophone communication and one-way decoding or encoding, which might be used for entertainment, surveillance, or video messaging. Whereas second-generation communicators support speech only, coded at 8 to 13 kbps, video alone requires at least 20 kbps for low-motion content on a small display. Third-generation wireless standards will make possible the higher bit rates required for even more sophisticated video-related applications.

Compressed video is particularly sensitive to errors that can occur with wireless transmission. To achieve high compression ratios, variable-length code words are used and motion is modeled by copying blocks from one frame to the next. When errors occur, the decoder loses synchronization, and errors propagate from frame to frame. The new MPEG-4 standard supports wireless video with special error resilience features, such as added resynchronization markers and redundant header information. The MPEG-4 data-partitioning tool, originally proposed by TI, puts the most important data in the first partition of a video packet, which makes partial reconstruction possible for better error concealment.

TI's MPEG-4 video software for OMAP was developed based on reference C software, which was then converted to use a fixed point C libraries, and then ported to TMS320C55x assembly code. The fixed point C libraries consist of routines representing all common DSP instructions. These routines perform the desired function, but also evaluate processing cycles and check for saturation, etc. Thus, these fixed point functions provide a very efficient development tool for benchmarking, and facilitates porting the C code to assembly.

As shown in previous section, the video software runs very efficiently on OMAP. The architecture is able to encode and decode in the same time QCIF (176 x144 pixels) images at 15 frames per second. The CPU loading for simultaneous encoding and decoding represents only 15% of the total DSP CPU capability. Therefore, 85% of the CPU is still available for running other tasks, such as graphic enhancements, audio playback (MP3), speech recognition.

OMAP provides not only the computational resources, but also the data-transfer capability needed for video applications. One QCIF frame requires 38016 bytes, for chrominance components downsampled in 4:2:0 format, when transferring uncompressed data from a camera or to a display. The video decoder and encoder must access both the current frame and the previously decoded frame in order to do the motion compensation and estimation, respectively. Frame rates of 10 to 15 frames per second need to be supported for wireless applications.

Third-generation standards for wireless communication, along with the new MPEG-4 video standard, and new low-power platforms like OMAP, will make possible many new video applications. It is quite probable that video applications will differentiate second- and third-generation devices, creating new markets and higher demand for wireless communicators.

6. CONCLUSION

In this paper, we have described how multimedia applications will be enabled in 3G wireless terminals thanks to the OMAP H/W architecture. The OMAP H/W multiprocessor architecture has been optimized to support heavy multimedia applications such as video and speech in 3G terminals. The flexible architecture of the TI DSP hardware core can also be extended with multi-media specific operations. This key capability allows even a further reduction of the CPU processing requirement for a given application. This enables handling of the growing and unpredictable demand for new applications in the 3G multi-media markets. TMS320C55x DSP family is the first DSP with such core level multi-media specific extensions.

7. REFERENCES

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