

A CCD/CMOS Image Sensor Array with Integrated A/D Conversion.

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I. INTRODUCTION

Integrated signal processors and images sensors have been implemented for vision applications using a variety of technologies including CCD, CCD/CMOS and CMOS [1-7]. In most of them the emphasis was limited to tasks where black and white images and small-medium resolution are required. However, for imaging sensing applications which require high sensitivity and resolution, CCDs are the dominant technology. The implementation described here uses a CCD/CMOS process technology that combines the advantages of the charge-domain sensing and computing elements with the flexibility of the CMOS circuitry [8]. A single chip digital imager has been implemented that integrates sensing elements, A/D conversion and CCD driving capability to reduce complexity and cost with respect to standard imaging systems.

II. CAMERA ARCHITECTURE

A block diagram of the prototype 32×24 pixel CCD/CMOS imager with a linear array of 32 parallel, 8-bits A/D converters is shown in Fig. 1.

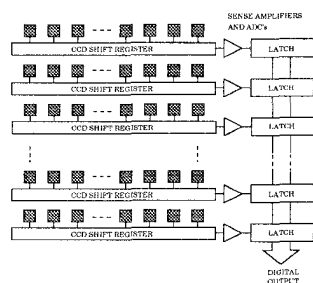


Fig. 1. Block diagram of the sensor architecture.

The image sensor array was implemented as an interline transfer (IT) CCD structure. However, a CCD floating diffusion readout circuit and a single-slope 8-bit A/D converter was implemented on the output of each CCD register row. The single-slope A/D converter was chosen for its compactness and parallelism. As the charge-signals from the sensor array are clocked out, they are readout and the A/D conversion is performed in parallel on each column. The converted digital values of a column are stored in CCD dynamic latches and shift registers for pixel serial, byte parallel output off-chip. CCD structures were found to be more compact than equivalent CMOS circuitry for

dynamic latches and shift registers. TTL input compatible CMOS drivers were also integrated for generation of proper clocking signals for the CCDs.

A. Photosensor Array

The imager was implemented using a 32×24 array of photodiode sensors and an interline transfer CCD structure. Each pixel was implemented using an n^+/p^- junction photodiode which has good sensitivity due to the absence of the polysilicon over the photosensitive region. The photodiode is separated from the CCD buried channel by a surface channel potential barrier which is controlled by a transfer gate. As is standard in interline transfer CCDs, the transfer gate is shared with a gate electrode of the interline CCD register. A horizontal antiblooming structure is also provided for each photodiode by properly biasing an n-channel transistor. The gate voltage can be adjusted to spill the excess photogenerated charge collected by the photodiode and to maximize the signal charge packet. Figure 2 shows a cross-section of the pixel with antiblooming structure and the potential profiles under working conditions.

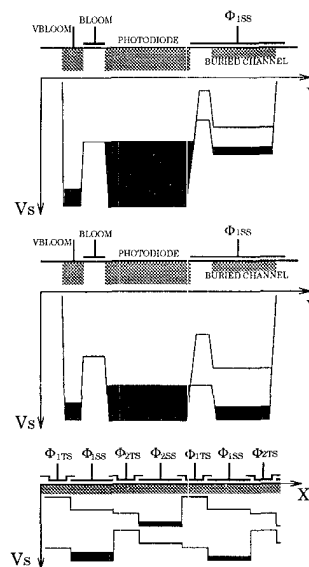


Fig. 2. Cross-section of the photodiode with the antiblooming structure.

The structure has been implemented using the first polysilicon layer for the antiblooming transistor and also for the transfer gate. The potential

barrier under the transfer gate has been realized by means of a buried channel implantation that provides a potential step of about 8 V with respect to the surface channel. The pixel dimensions are $32\mu\text{m} \times 32\mu\text{m}$ with a $20\mu\text{m} \times 15\mu\text{m}$ photosensitive region. With this type of CCD structure, the charge transfer/readout phase and charge integration phase can be overlapped in time. During the integration time, the photodiode is isolated from the CCD register by the surface potential barrier and by the antiblooming structure that prevents the excess photogenerated charge from flooding the surface potential barrier. After the integration time, the photogenerated charge is transferred to the CCD register by pulsing the photodiode transfer gate electrode to a voltage higher than its normal CCD shift register clocking levels used during readout. Each horizontal CCD register has a charge read-out circuit to provide a parallel read-out of the sensor array.

B. Sense Amplifiers

The charge amplifiers linearly convert the charge transferred through the CCD register to a voltage signal. They are based on a wide - range transconductance amplifier with a simulated GBW = 2 MHz, and 40 dB dc gain. Bias current is limited to $30\mu\text{A}/\text{amplifier}$ to contain the total power dissipation of the chip. The output of the CCD register consists of a n+/p diffusion which is precharged to a reverse voltage and then left floating. The charge packet, coming from the CCD register, is linearly converted into a voltage variation with the amount of charge .

C. Analogue to Digital Converter

The parallel array of A/D converters was implemented using a single-slope A/D converter integrated with each horizontal CCD register of the array [9]. Charge packets are readout as analogue voltages which are compared with a 2 V rising voltage ramp using a CMOS comparator. As voltage amplifier and comparator, simple wide-range transconductance amplifiers were used (Fig. 3) with $30\mu\text{A}$ bias current.

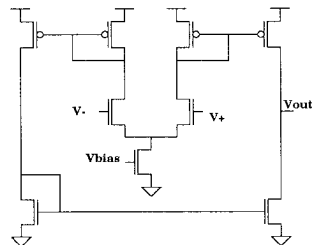


Fig. 3. CCD charge-readout amplifier.

The voltage ramp is synchronized with an exter-

nal 8-bit counter working at a clock frequency of 2 MHz corresponding to a $128\mu\text{s}$ conversion time. When the comparator switches it loads the current value of the counter into an 8-bit dynamic CCD latch and shift register (Fig. 4).

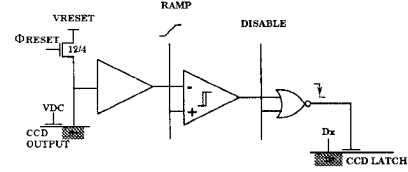


Fig. 4. Signal charge readout and conversion.

The relationship between the analogue input voltage and the digital output code can be expressed as:

$$N = \frac{1}{SR} \frac{V_{SIG}}{T_{CK}}$$

with

N : number of clock cycles

SR : voltage ramp Slew-Rate

T_{CK} : clock period

V_{SIG} : analogue voltage signal.

The data is loaded into a CCD shift register by using an input diode structure [10] as shown in Fig. 5.

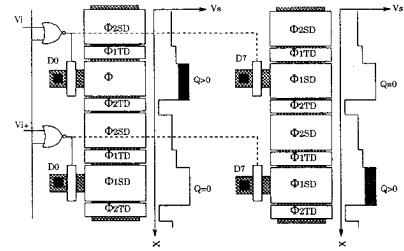


Fig. 5. CCD/CMOS Latch.

The main counter is connected to the diode and the comparator controls the CCD gate. The external binary counter uses a Gray code to reduce the uncertainty to one bit and to half the mean operating frequency of the CCD latches. When the comparator switches the CCD gate is turned off and effectively isolates the input diode from the CCD shift register. If the diode is nominally biased at a high reverse bias voltage, there will be no charge in the CCD shift register. If the diode is nominally biased at 0 Volts, a full charge packet will be loaded into the CCD shift register. At the end of the conversion time, an 8 bit digital value will be stored in the CCD shift registers for each of the CCD output rows (Fig. 5). The digital values are clocked out through eight vertical shift registers, byte-parallel, pixel serial. Since the data

is digital, the transfer efficiency and speed performance requirements of the vertical shift registers are significantly reduced. The output of each of the digital CCD shift registers has a thresholding charge-readout circuit for digital signal regeneration through one CMOS digital buffer for driving data off-chip. Both, the horizontal analogue CCD shift registers and vertical digital CCD shift registers are clocked with pseudo two-phase clocking signal [11]. The A/D converter with the 8-bit latches occupies a total area of $32\mu\text{m} \times 650\mu\text{m}$ while the single-bit latch cell is $32\mu\text{m} \times 40\mu\text{m}$.

D. Digital Output

After the A/D conversion is completed, the charge packets are clocked to the output and digitized by a comparator with a threshold V_{THR} . TTL-level drivers provide the 8-bit data to the output (Fig. 6).

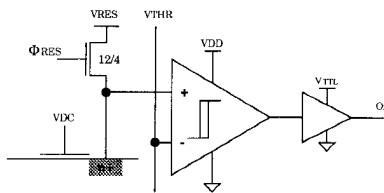


Fig. 6. Digital CCD readout and thresholding circuit.

E. CCD Drivers

The CCD phases are generated on-chip from an external master clock to ensure proper relative timing of the waveforms. Two separate CCD drivers were implemented, one for the CCD image sensor and one for the digital CCD shift registers. The generators and drivers were implemented as a flip-flop which can be forced into one state or into the other by two NMOS transistors driven in counter-phase by a TTL input signal. Each output of the flip-flop drives two CMOS output buffers with externally adjustable power supply rails which are necessary for proper clocking of the CCD registers. The maximum working frequency is 500 KHz with a load capacitance of 200 pF.

The chip uses a $2\mu\text{m}$ double-metal double-poly CCD/CMOS process and works at a maximum frame rate of 100 frames/s and dissipates less than 100 mW at 14 V power supply.

III. EXPERIMENTAL RESULTS

Electrical characterization of a single A/D converter was carried out by using the Code Density Test method [12]. The parameters of the ADC were measured by taking 3×10^5 samples and by processing the data with MATLAB program [13].

A differential nonlinearity of 1 LSB has been measured as reported in Fig. 7, while the integral

non-linearity is of about 2 LSB as shown in Fig. 8.

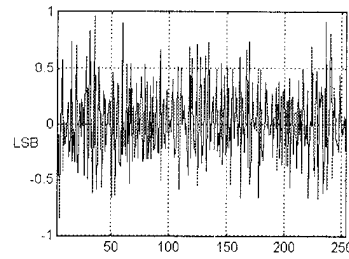


Fig. 7. Differential Nonlinearity.

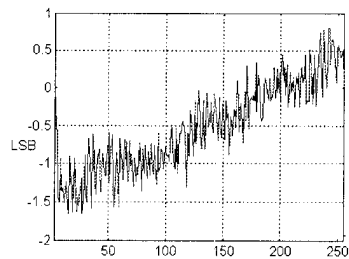


Fig. 8. Integral Nonlinearity.

The converter has 1.2% of gain error which is primarily due to the finite gain of the buffer.

The A/D converter array was also tested separately from the imager by forcing all its 32 inputs with a common dc input voltage signal. The array of converters shows a spatial non-uniformity error of ± 4 LSB reported in Figure 9. This is mainly due to the offset variations of the CCD readout amplifiers and the comparators of the array that are not offset-compensated.

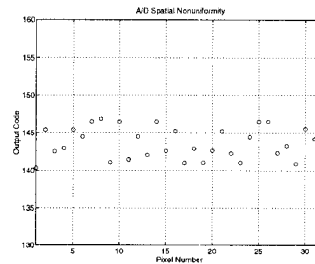


Fig. 9. A/D spatial nonuniformity.

A typical image obtained by the sensor is shown in Fig. 10. A photograph of the chip is shown in Figure 11. The total die area included bonding pads is 6mm^2 .

IV. CONCLUSIONS

A CCD/CMOS digital camera with integrated drivers is reported. The chip uses a 32×24 pixels CCD Interline-Transfer image sensor with 32 CCD/CMOS single-slope analog-to-digital converters. This highly scalable architecture is suitable for implementing high resolution modular image sensors for digital vision applications. Correlated Double Sampling technique could be integrate on each readout channel to suppress kTC and fixed-pattern noise.



Fig. 10. Typical image obtained by the sensor.

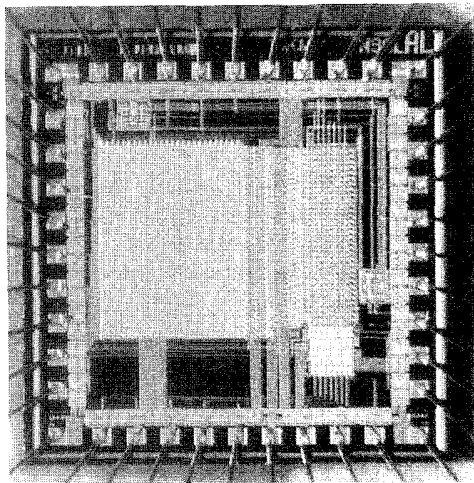


Fig. 11. Photograph of the chip.

V. ACKNOWLEDGMENTS

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