

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SONY CORPORATION,

Petitioner

v.

OPTIMUM IMAGING TECHNOLOGIES LLC,

Patent Owner

Case IPR2024-00923

Patent No. 10,873,685

PATENT OWNER RESPONSE

Mail Stop PATENT BOARD
Patent Trial and Appeal Board
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

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<u>PATENT OWNER'S LIST OF EXHIBITS</u>	
EX. 2001	Excerpt for E.D. Tex from U.S. District Courts—Combined Civil and Criminal Federal Court Management Statistics, p. 35 (June 30, 2024), accessed at https://www.uscourts.gov/statistics-reports/federal-court-management-statistics-june-2024 on August 9, 2024
EX. 2002	Global Dossier Patent Family for U.S. Pub. No. 20050280877 (Watanabe), accessed at https://globaldossier.uspto.gov/result/publication/US/20050280877/118382 on August 9, 2024
EX. 2003	Extract from the Register of European Patents for EP1608140 (Watanabe foreign counterpart), accessed at https://register.epo.org/application?number=EP05253548&Ing=en&tab=doclist on August 13, 2024
EX. 2004	Translation of Japanese Patent Application No. 2004-233872, submitted during prosecution of EP1608140 on June 1, 2006 (“EPO Translation”)
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EX. 2006	Skolnick, David, et al., “Why Use DSP? Digital Signal Processing 101 – An introductory course in DSP system design: Part 1”, Analog Dialogue, vol. 31, no. 1, pp. 3-6 (1997), accessed at https://www.analog.com/media/en/analog-dialogue/volume-31/number-1/articles/volume31-number1.pdf on August 20, 2024
EX. 2007	Harris, Tom, “How Camcorders Work - The CCD”, Internet Archive (Nov. 24, 2005), accessed at https://web.archive.org/web/20051124054808/https://electronics.howstuffworks.com/camcorder2.htm on August 17, 2024
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EX. 2009	Wilson, Tracy, et al., “How Digital Cameras Work - More on Capturing Color”, Internet Archive (Nov. 25, 2005), accessed at https://web.archive.org/web/20051125115620/http://electronics.howstuffworks.com/digital-camera5.htm on August 17, 2024
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EX. 2011	U.S. Patent No. 7,612,805 (“the ’805 Patent”)
EX. 2012	U.S. Patent No. 8,451,339 (“the ’339 Patent”)
EX. 2013	Patent Owner’s Proposed Schedule in Parallel Litigation
EX. 2014	Order Governing Proceedings, No. 4:23-cv-928, Dkt. 24 (E.D. Tex. July 23, 2024)
EX. 2015	RESERVED
EX. 2016	RESERVED
EX. 2017	Laub Expert Declaration on U.S. Patent No. 7,612,805, originally submitted in IPR2024-00924 as EX. 1003
EX. 2018	Laub Expert Declaration on U.S. Patent No. 8,451,339, original submitted in IPR2024-00925 as EX. 1003
EX. 2019	U.S. Patent No. 8,849,964 (“Ralston”), originally submitted in IPR2024-00924 as EX. 1081

EX. 2020	Laub Deposition Transcript regarding IPR2024-00923, IPR2024-00924, and IPR2024-00925, dated February 5, 2025
EX. 2021	Printout of Website titled “Digital Photo Professional” accessed at https://en.canon-cna.com/support/consumer_products/software/digital-photo-professional.html?softwareid=tcn:257-1328049&os=all on February 24, 2025
EX. 2022	Printout of Website titled “Canon EOS Rebel T6s First Impressions Review” accessed at https://www.reviewed.com/cameras/content/canon-eos-rebel-t6s-first-impressions-review on February 24, 2025
EX. 2023	Printout of Website titled “Canon T6s Review” accessed at https://www.imaging-resource.com/PRODS/canon-t6s/canon-t6sA.HTM on February 24, 2025
EX. 2024	Printout of Website titled “Canon EOS Rebel T6s Review” accessed at https://www.pcmag.com/reviews/canon-eos-rebel-t6s on February 24, 2025
EX. 2025	Printout of Website titled “Canon T6s (EOS 760D)” accessed at https://www.kenrockwell.com/canon/t6s.htm on February 24, 2025
EX. 2026	Printout of Website titled “EOS Rebel T6s” subtitled “Overview” accessed at https://www.cla.canon.com/cla/en/support/consumer/cameras/eos_cameras/eos_rebel_t6s# on February 24, 2025
EX. 2027	Printout of Website titled “EOS Rebel T6s” subtitled “Specifications” accessed at https://www.cla.canon.com/cla/en/support/consumer/cameras/eos_cameras/eos_rebel_t6s#specificationsTab on February 24, 2025
EX. 2028	Canon EOS Rebel T6s Instruction Manual accessed at https://gdlp01.c-wss.com/gds/4/0300018244/04/eos-rebel-t6s-760d-im4-en.pdf on February 24, 2025

EX. 2029	Printout of Website titled “Canon DIGIC 6 Processor and New 18Mp APS-C CMOS Sensor Arrives” accessed at https://thenewcamera.com/canon-digic-6-processor-and-new-18mp-aps-c-cmos-sensor-arrives/ on February 24, 2025
EX. 2030	Printout of Website titled “Canon EOS 80D Review” accessed at https://photographic-central.blogspot.com/2017/10/canon-eos-80d-review.html#google_vignette on February 24, 2025
EX. 2031	Printout of Website titled “More About the EOS 80D (Part 2) – Technology” accessed at https://snapshot.canon-asia.com/article/eng/more-about-the-eos-80d-part-2-technology on February 24, 2025
EX. 2032	Printout of Website titled “First Impressions Review: Using the Canon PowerShot G16” accessed at https://www.dpreview.com/reviews/first-impressions-review-using-the-canon-powershot-g16#:~:text=The%20DIGIC%206%20processor%20delivers,to%20a%20lot%20of%20people on February 24, 2025
EX. 2033	Printout of Website titled “EOS Rebel T6s” subtitled “Features” accessed at https://www.cla.canon.com/cla/en/support/consumer/cameras/eos_cameras/eos_rebel_t6s#featuresTab on February 24, 2025
EX. 2034	Printout of Website titled “Technology Used in Digital SLR Cameras” accessed at https://global.canon/en/technology/support14.html#:~:text=When%20light%20enters%20the%20camera,data%20based%20on%20the%20signal on February 24, 2025
EX. 2035	Printout of Website titled “5 Things Made Possible with DIGIC Image Processor” accessed at https://snapshot.canon-asia.com/article/eng/5-things-made-possible-with-digic-image-processor on February 24, 2025
EX. 2036	Printout of Website titled “Settings Configured in [Camera Settings]” accessed at https://cam.start.canon/en/S003/manual/html/UG-02_CameraSetting_0020.html on February 24, 2025

EX. 2037	Printout of Website titled “2019 camera market share: Canon 45.4%, Sony 20.2%, Nikon 18.6%, Fuji 4.7%, Panasonic 4.7%” accessed at https://nikonrumors.com/2020/08/14/2019-camera-market-share-canon-45-4-sony-20-2-nikon-18-6-fuji-4-7-panasonic-4-7.aspx/ on February 24, 2025
EX. 2038	Printout of Website titled “Digital Camera Market Share 2020: Only Canon, Sony and Fujifilm Grow” accessed at https://www.fujirumors.com/digital-camera-market-share-2020-only-canon-sony-and-fujifilm-grow/ on February 24, 2025
EX. 2039	Printout of Website titled “The latest digital camera global market share (2021)” accessed at https://nikonrumors.com/2022/11/22/the-latest-digital-camera-global-market-share-2021.aspx/ on February 24, 2025
EX. 2040	Printout of Website titled “Digital Camera Market Share 2022: Canon Dominates Ahead of Sony and Nikon, Fujifilm 4 th ” accessed at https://www.fujirumors.com/digital-camera-market-share-2022-canon-dominates-ahead-of-sony-and-nikon-fujifilm-4th/ on February 24, 2025
EX. 2041	Printout of Website titled “How Canon and Sony Market Shares Display a Troubling Trend” accessed at https://www.thephoblographer.com/2024/09/23/canon-and-sony-market-shares-display-a-troubling-trend/ on February 24, 2025
EX. 2042	Printout of Website titled “Trendspotting: Canon, followed by the rest (digital camera market share 2024)” accessed at https://www.starkinsider.com/2024/09/trendspotting-canon-followed-by-the-rest-digital-camera-market-share-2024.html on February 24, 2025
EX. 2043	Canon Litigation Document – HIGHLY CONFIDENTIAL – OUTSIDE ATTORNEYS’ EYES ONLY
EX. 2044	Declaration of Dr. Omid Kia – HIGHLY CONFIDENTIAL – OUTSIDE ATTORNEYS’ EYES ONLY

EX. 2045	CV of Dr. Omid Kia
EX. 2046	Joint Protective Order
EX. 2047	Redlined version of the Joint Protective Order (compared to Default Protective Order)
EX. 2048	Executed Acknowledgements

I. INTRODUCTION

Petitioner challenges claims 1-19 and 22-23 of Patent No. 10,873,685 (“‘685 Patent”). Petition, 1. Challenged claims 1, 6, and 14 are independent.

Patent Owner (“PO”) respectfully submits that Petitioner fails to meet its burden to establish obviousness for at least four reasons.

First, the Watanabe reference has many deficiencies and does not meet the limitations of the challenged claims. None of Kishida, Kita, Takane, Hisamatsu, Turner, or Liege cure these deficiencies. Petitioner also relies on the combination of Takane and Watanabe which fails for at least the same reasons.

Second, the proposed modifications/combinations are replete with hindsight bias. Petitioner relies on the testimony of Leonard Laub (“Laub”) who opined on what a person ordinarily skilled in the art **could** do, not what that person **would** do.

Third, both Petitioner and Laub fail to clearly explain **how** the proposed modifications/combinations are supposed to work.

Fourth, there are strong secondary considerations showing non-obviousness of the claimed inventions.

II. THE '685 PATENT CLAIMS NOVEL AND NON-OBVIOUS SYSTEMS FOR CORRECTING ABERRATIONS IN A DIGITAL CAMERA

A. BACKGROUND TO THE FIELD OF TECHNOLOGY

The '685 Patent claims priority to a provisional application filed July 11, 2006. EX.1001, code (60).¹

At the time of invention, a person ordinarily skilled in the art ("POSA") would understand that all digital cameras are designed to capture images by focusing light through a lens which usually includes an aperture that adjusts the amount of light reaching the sensor. EX.2044, ¶37.

A POSA would understand that the materials used to manufacture a lens affect the size, weight, price, and performance of a particular lens. EX.2044, ¶38. An image captured through a lens will have certain optical aberrations. *Id.* The nature and degree of the optical aberrations may be affected by the quality of the glass, lens coatings, and other materials used to manufacture the lens; as well as the capture settings of the camera including focal length, focusing distance, and

¹ The relevant time of invention is July 11, 2006. Neither Petitioner nor Laub identified any limitations of the claims that allegedly lack written description support. Laub did not analyze the correct time of invention. EX.2044, ¶¶34-36; EX.1003, ¶¶50, 52, 56.

aperture value. *Id.* A POSA would understand that even the highest quality and most expensive lenses are unable to capture “perfect” images and there will always be certain optical aberrations in images captured by digital cameras. EX.2044, ¶39; *see also* EX.2044, ¶¶40-41 (discussing optical versus digital aberrations).

A POSA would understand that, historically, post-production digital editing software (*e.g.*, Adobe Photoshop) was used to correct optical and digital aberrations. EX.2044, ¶42. However, as disclosed in the common specification, using post-production software was time-consuming, expensive, and requires considerable skill. *Id.*; EX.1001, 6:33-44.

A POSA would be familiar with a digital signal processor (“DSP”) generally. EX.2044, ¶43. This is a term of art and refers to a specific type of hardware component. *Id.* As discussed below, the claimed DSP must be capable of specific functionality.

A POSA would be familiar with an application specific integrated circuit (“ASIC”) generally. EX.2044, ¶¶44-45. This is a term of art and refers to a specific type of hardware component. *Id.*

B. THE ‘685 PATENT

The ‘685 Patent claims systems that perform in-camera aberration correction using novel and non-obvious combinations of hardware and software. EX.1001,

Abstract (“A system is disclosed for the automated correction of optical and digital aberrations in a digital imaging system.”)

“Though every major advance in photography has solved an important problem, there are still remaining photographic problems to be solved in order to meet the goals of *optimizing optical imaging quality* while *increasing simplicity and efficiency* and *lowering cost*.” EX.1001, 3:19-23 (emphasis added).

“The present system dramatically improves image quality. This digital imaging system eliminates, or minimizes, post-production processes. In addition, the system presents substantial cost savings as well as time savings relative to existing digital imaging systems because of the automation of integrated in-camera optical and digital corrections of aberrations.” EX.1001, 7:23-29.

The specification discloses various embodiments that use specific hardware with specific functionality. EX.2044, ¶51. The specific hardware includes, for example, a digital camera mechanism, an optical lens mechanism, a digital sensor, a microprocessor, and a DSP. *Id.* For example, the specification explains that “[d]igital filtration is performed by employing the **DSP hardware** as well as specific software in order to attain specific aberration corrections.” *Id.*; EX.1001, 32:45-47 (emphasis added).

The inventor of the ‘685 Patent realized the claimed technology efficiently balances competing considerations including space, cost, time, and power in

camera design. EX.2044, ¶52. As recognized by Laub, there is a balance between “cost and manufacturing efficiencies” in camera design. EX.1003, ¶107; EX.2020, 20:16-21:8. Laub testified that, for example, computation time would be considered by a POSA as a factor when designing a camera, “if there is a consideration for how quickly a finished result can be delivered.” EX.2020, 24:5-8.

In general, a POSA designing a camera would always want a smaller, less expensive, faster, and more powerful camera, but how to balance these competing considerations is complex. EX.2044, ¶53. The claimed technology provides a novel and non-obvious solution to this problem. *Id.* In particular, the claimed in-camera aberration correction systems and methods provide an efficient distribution of the workload using the claimed hardware and software. *Id.*

C. LEVEL OF ORDINARY SKILL

In prior litigation, the district court found that a POSA would have had “an electrical engineering degree and three years of relevant experience.” EX.1027, 6. The Board should adopt the district court’s definition at least for consistency in the different forums. *See also* EX.2044, ¶¶17, 20.²

² PO’s expert’s opinions do not change under either POSA definition. EX.2044, ¶20.

Both Petitioner and Laub ignored the district's court's POSA definition. Petition, 7; EX.1003, 191. Petitioner's proposed POSA definition is unbounded regarding what constitutes a related field and unbounded regarding the amount of experience/research. EX.2044, ¶20.

D. CLAIM CONSTRUCTION

Petitioner identified terms/phrases that need not be expressly construed in this proceeding. Petition, 7-8; Paper 10, 12; EX.2044, ¶¶54-58.³

1. “database management system” and “database”

PO submits that the terms “database manage system” (“DBMS”) and “database” should be given their plain and ordinary meaning in the context of the ‘685 Patent. EX.2044, ¶59.

Petitioner stated that a DBMS is “software used to create, store, retrieve, change, manipulate, sort, format and print... information in a database.” Petition, 18. The basic premise of Petitioner's definition is generally consistent with the

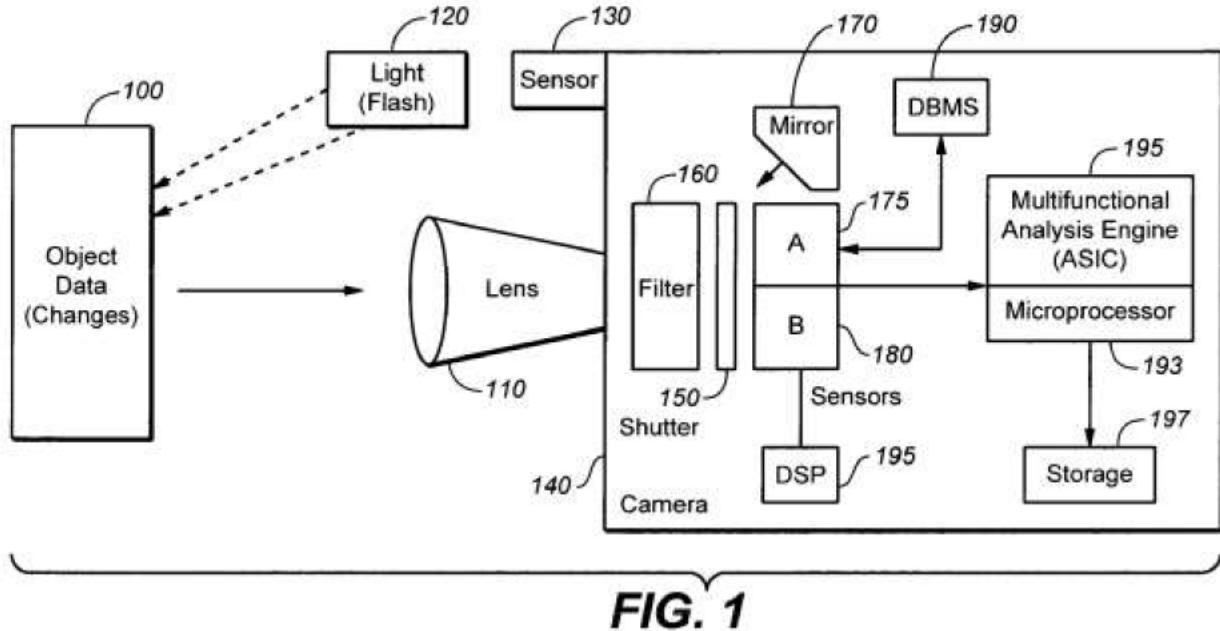
³ PO reserves all rights regarding the correct constructions for these terms/phrases. For purposes of this proceeding only, PO does not dispute Petitioner's inherent construction of claim 1[a] to mean an integrated circuit is configured to access a DBMS. EX.2044, ¶¶74-79.

plain and ordinary meaning of DBMS, except that the meaning of “print” is unclear in the context of the ‘685 Patent. EX.2044, ¶60. PO does not offer Petitioner’s definition as an express construction for DBMS because the plain meaning is sufficient and would be understood by a POSA in the context of the ‘685 Patent. *Id.*

In the Institution Decision, the Board preliminarily interpreted claim 1 of the ‘685 Patent to equate “database management system” and “database” due to antecedent basis. Paper 11, 22-24. PO addresses the Board’s preliminary analysis of claim 1 as discussed herein.

The use of the claimed DBMS/database is not merely executing code, running on a main CPU, to access a fixed look-up table of parameters as discussed herein with respect to for example Watanabe. EX.2044, ¶62. A POSA would understand that the DBMS operates in conjunction with the database as discussed herein. *Id.*

In the Institution Decision, the Board reviewed FIG. 1 of the ‘685 Patent and specifically referred to reference number 190 identifying “DBMS”. Paper 11, 3. A POSA would understand that DBMS is the acronym for database management system which operates with database 190. EX.2044, ¶63.



EX.1001, FIG. 1.

In the specification, reference number 190 describes “a database”. EX.1001, 31:39-40 (“A database (190) is connected to at least one sensor (A or B) as well.”). Although the same reference number 190 is used for DBMS in the figure and database in the description, a POSA would understand that a DBMS is used to organize/manage/update the database. EX.2044, ¶64. A POSA would understand that the DBMS and the database may be located on the same hardware component.

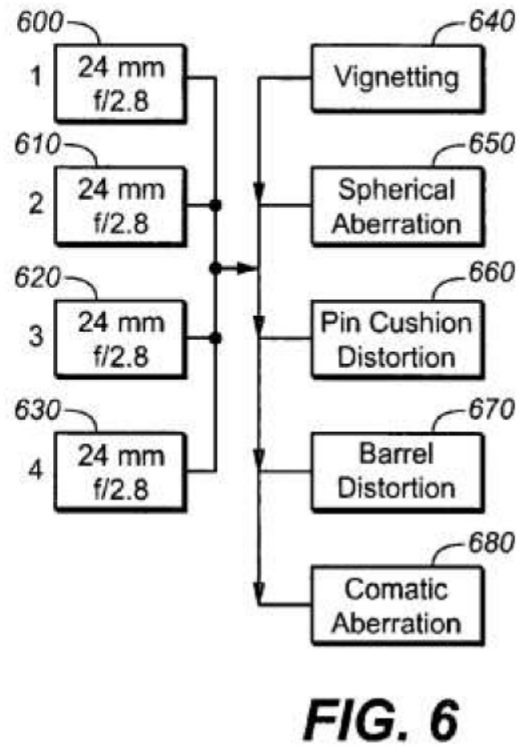
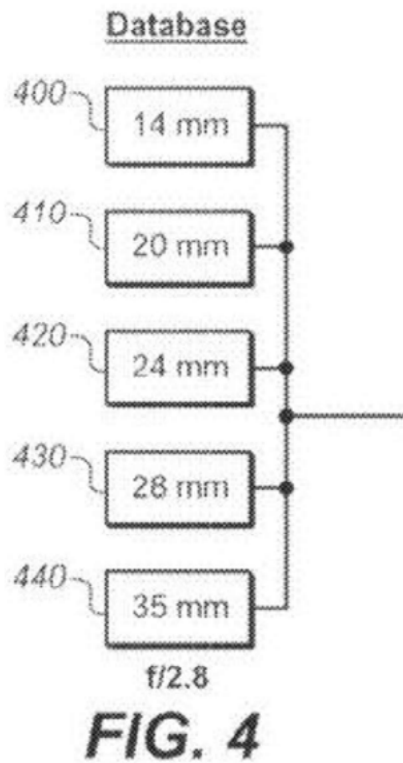
Id.

The specification also describes for example:

- “[T]he camera identifies a specific lens and refers to a database that matches the lens type with the specific aberrations.” EX.1001, 10:60-62.

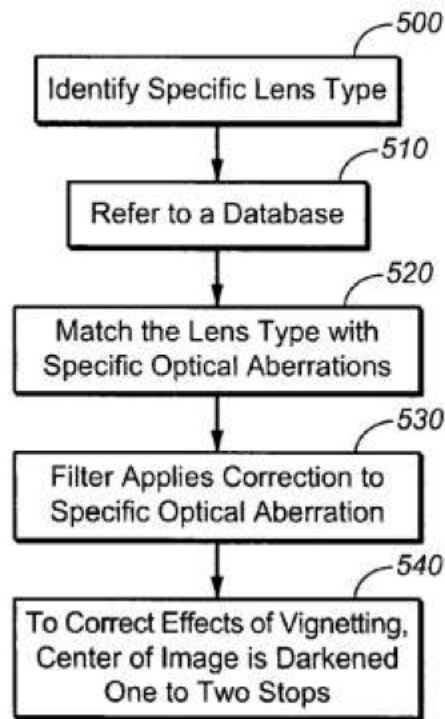
- “The in-camera digital process works by identifying a specific lens and comparing the lens pattern to an internal database.” EX.1001, 11:8-10.
- “[E]ach lens with a unique optical formula will have specific aberrations, the corrections for which will be accessible in a database.” EX.1001, 11:24-26.
- “The dynamics of correcting multiple simultaneous aberrations may be complex, but since the number and type of aberrations are constrained to a specific lens type, a centralized database may be accessed with specific corrections for each respective aberration.” EX.1001, 12:54-58.
- “For a fixed focal length lens, the camera refers to a database of information to provide information to correct specific types of aberrations; for a zoom lens, the camera's database contains multiplex information for each focal length in each respective zoom lens type.” EX.1001, 26:58-63.

FIG. 4 shows an exemplary “database” with a list of several different wide angle lenses, each with f/2.8 apertures. EX.1001, 32:14-20. FIG. 6 also shows an exemplary “database” configured for “several different types of 24 mm f/2.8 lenses (600 to 630) with different optical configurations” and the specification explains that “[t]he database is accessed to provide the multi-objective optimization solution for correcting several different optical aberrations for each specific lens formula.” EX.1001, 32:28-38.



EX.1001, FIGS. 4, 6.

FIG. 5 also shows an exemplary “digital corrective process” where “[a]fter a specific lens type is identified (500) and a database is referenced (510), the lens type is matched with the specific optical aberrations (520).” EX.1001, 32:21-24.

**FIG. 5**

The specification also describes that though multiple aberrations may be corrected simultaneously, it is possible to omit a specific correction in order to induce a particular creative effect. *See, e.g.*, EX.1001, 12:41-45.

The specification also describes the database is updatable:

- “[S]oftware files are periodically downloaded to the camera in order to update the camera settings and the database system.” EX.1001, 29:13-15.
- For example, “as the camera manufacturer provides new lenses for the camera, it becomes necessary to load new updated settings to accommodate corrections for the new lenses.” EX.1001, 29:15-18.

- As another example, “as the camera requires new software updates with improved algorithms to further optimize the corrective functions of both the optical and digital mechanisms, the camera will automatically accept these.” EX.1001, 29:18-22.

The specification explains that the updatable database is a “particularly important” feature to both the manufacturer and the user. EX.1001, 29:22-26 (“This feature is particularly important to both manufacturer and user because the ability to update software capability periodically will protect a user from needing to upgrade major hardware such as with a lens replacement.”)

Because the database may contain many different lens types (that the camera owner may utilize, add, or remove from their inventory) and many different aberration corrections for each lens type, and because the database may be used to correct multiple simultaneous aberrations, and because the database is updatable, **the database is used with a DBMS to organize/manage/update the information.** EX.2044, ¶71. This is similar to Laub’s opinion that a DBMS would be understood as being used to create, store, retrieve, change, manipulate, sort, and format information in the database. EX.1003, ¶175. This is also similar to Petitioner’s statement that “[t]he DBMS is software interfacing between an application and a database but is not itself a database.” Petition, 22.

The claims expressly recite a DBMS, and in context of the ‘685 Patent, a POSA would understand that the claimed database is updatable. EX.2044, ¶72.

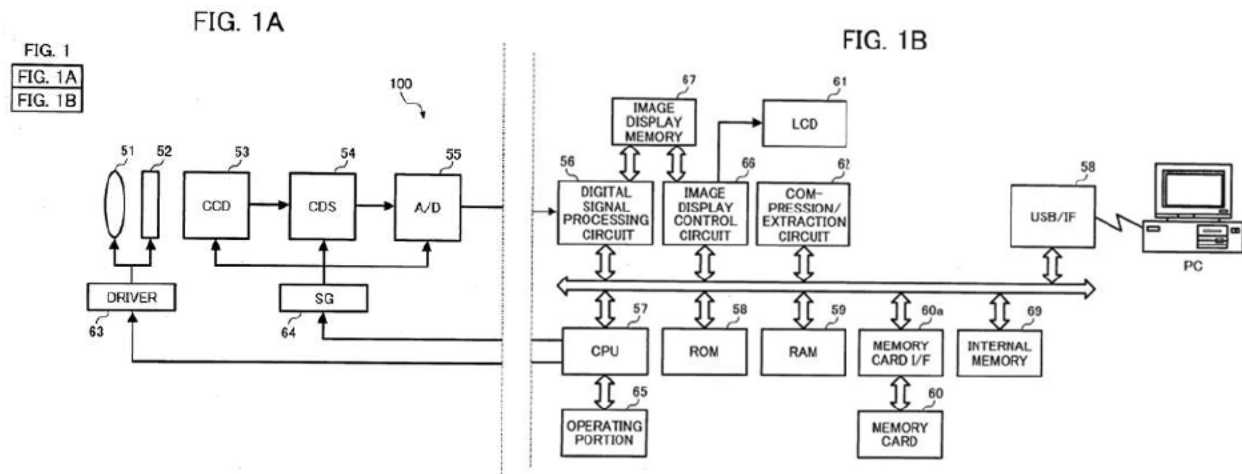
Updating the database is one of the functions performed by the DBMS. *Id.*

Using a DBMS allows flexibility, updatability, and scalability of the data in the database. EX.2044, ¶73. The claimed DBMS/database is unconventional as further discussed herein and the inventor recognized the functional benefits of the claimed DBMS/database including flexibility, updatability, and scalability as discussed herein. *Id.* A POSA reading the specification would understand that the claimed DBMS facilitates organizing/managing/updating the data in the database in a more efficient way to achieve compactness of data, without unnecessarily duplicating data in tables and increasing the memory requirements. *Id.* Furthermore, the ability to organize/manage/update a database with the DBMS allows continued efficient organization/management of data as new and/or updated data is introduced. *Id.*

III. GROUND 1 FAILS

A. OVERVIEW OF WATANABE

Petitioner relies on the first embodiment of Watanabe that is related to a “digital still camera.” EX.1005, [0040], [0042]. With respect to FIGS. 1A-1B, Watanabe discloses a digital still camera 100. EX.1005, [0035].



EX.1005, FIGS. 1A, 1B.

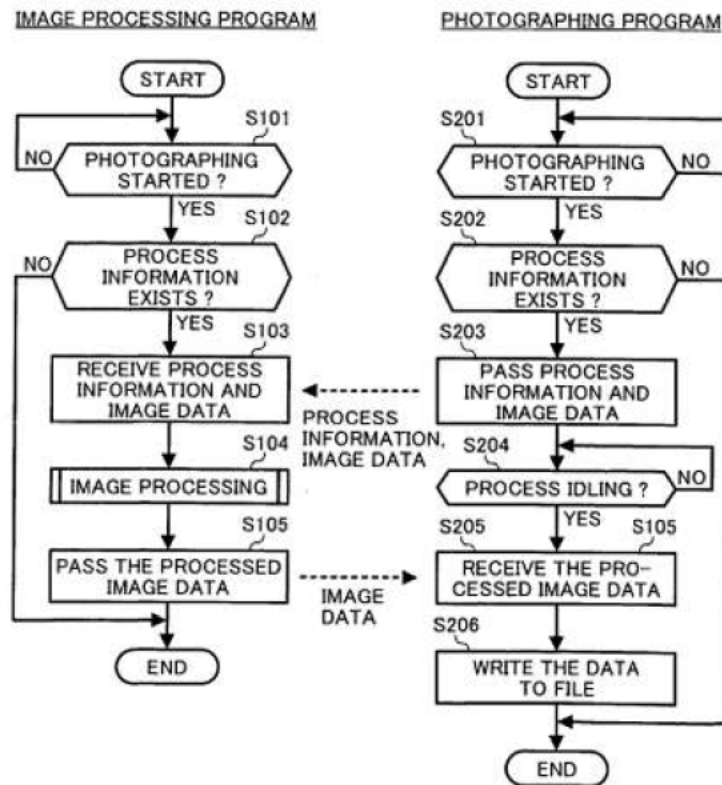
Operating portion 65 includes buttons for selecting a function by the operator, *e.g.*, a release button used at the time of photographing. EX.1005, [0041].

ROM 58 stores a control program that includes an “imaging processing program” and a “photographing program.” EX.1005, [0042].⁴ The CPU 57 executes both programs. EX.1005, [0060].

FIG. 4 of Watanabe shows the steps performed by the “imaging processing program” versus the “photographing program.”

⁴ CPU 57 “controls operation of each part of the digital still camera... by way of an [sic -a] photographing program.” EX.1005, [00042]. CPU 57 “processes image data by way of an image processing program.” *Id.*

FIG. 4



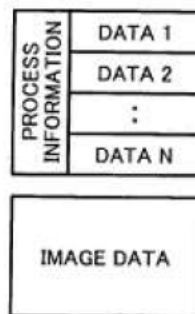
When the release button is pushed (S101 and S201), and when process information exists (S102 and S202), the image data is produced and transferred together with the process information from the photographing program to the image processing program (S103 and S203). EX.1005, [0058], [0061].

The image processing program executes an image process on the image data in accordance with the process information (S104). EX.1005, [0062].

The processed image data is then transferred from the image processing program to the photographing program (S105). EX.1005, [0062]. The processed image data is then recorded (S206). EX.1005, [0063].

With respect to FIG. 2, Watanabe explains that “various data (data 1-data N) are added to image data as process information.” EX.1005, [0046]. For example, information of a lens type, a focusing point, and a zoom position may correspond to data 1, data 2, and data 3, respectively. EX.1005, [0047], FIG. 3.

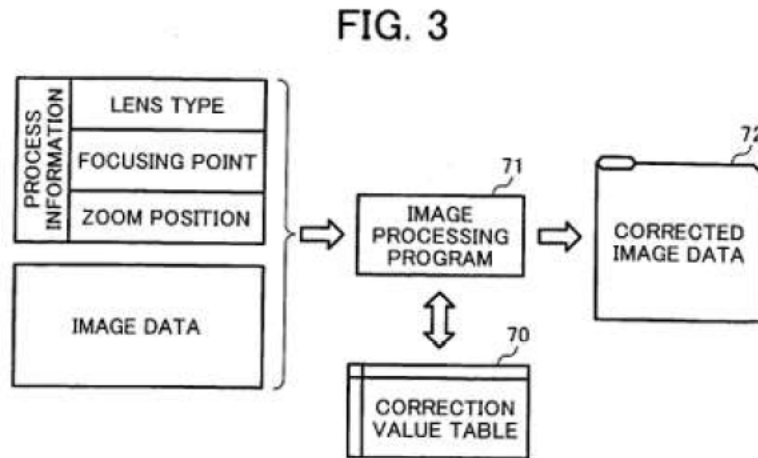
FIG. 2



With respect to FIG. 3, Watanabe discloses tables 70 with correction values, prepared in advance, for each lens type. EX.1005, [0047]. The CPU 57 determines a table according to lens type (data 1) and then determines the correction values according to the focusing point (data 2) and zoom position (data 3). EX.1005, [0047]. Thus, the image process performed by the image processing program,

discussed above with respect to FIG. 4, step 104, is selected based on data 1-data 3.

EX.1005, [0047].



In the context of Watanabe, the patentee expressly distinguished the process information of the first embodiment (identifying capture conditions) and the process information of the second embodiment (identifying aberrations). EX.1005, FIGS. 3, 6, 11, 13; EX.2005, 2-3.⁵ Watanabe teaches identification of capture conditions should be used with a look-up table (in the relied-upon first

⁵ The second embodiment of Watanabe relates to a multifunction printer 101.

EX.1005, [0067], FIG. 5. The second embodiment of Watanabe does not disclose at least the use of a DSP or a DBMS/database as claimed in the '685 Patent.

EX.2044, ¶93.

embodiment), while identification of aberrations should not use a look-up table (in the second embodiment). *Id.*

B. CLAIM 1

PO uses the same claim annotations as Petitioner for convenience of review. Petition, 78-82. PO respectfully submits that a POSA would not perform the proposed modifications as discussed herein. Petitioner is using hindsight bias.

1. *Claims 1[pre] and 1[a]*

Petitioner relies on Watanabe's digital camera 100 of FIGS. 1A and 1B, including for example lens 51, CCD 53, A/D converter 53, CPU 57, and digital signal processing circuit 56. A POSA would understand these are hardware components of Watanabe's digital camera 100. EX.2044, ¶98. Indeed, Laub referred to this disclosure in Watanabe as "a digital camera **hardware** implementation." EX.1003, ¶134 (emphasis added).

Petitioner relies on modifications to Watanabe's disclosed digital camera 100 as discussed herein. Laub opined for example that "Watanabe does not specify how the hardware components of digital camera 100 are implemented". EX.1003, ¶163. **This is not correct.** Watanabe discloses a complete hardware diagram of digital camera 100 in FIGS. 1A and 1B. EX.2044, ¶101. A POSA would be familiar with the hardware components disclosed in Watanabe and a POSA reading Watanabe

would understand the hardware capabilities and required resources. *Id.* A POSA would have understood that modifying these hardware components would affect at least the size, weight, and power-requirements of the modified camera, as well as speed and processing capabilities of the modified camera, and a POSA cannot ignore the impact of these modifications. *Id.*

Laub opined for example that “Watanabe does not limit such a hardware implementation to discrete versus integrated components” (EX.1003, ¶135) and that “Watanabe’s schematic arrangements ... could be adapted or modified without issue” (EX.1003, ¶137). **This is not correct.** Watanabe expressly discloses discrete components. EX.2044, ¶100. Watanabe discloses the use of a simple circuit 56 with limited functionality in the context of a closed, self-contained system. EX.2044, ¶146. Laub is using hindsight bias.

Laub opined for example that “Watanabe’s hardware and processes are easily programmable to perform a multitude of different tasks”. EX.2017, ¶236 (citing EX.1005, [0038]). **This is not correct.** The cited paragraph 38 of Watanabe does not suggest that the disclosed hardware has the expanded capabilities or unlimited resources supporting Petitioner’s proposed modifications as discussed herein. EX.2044, ¶102. Each of Petitioner’s proposed modifications is hindsight. Laub also fails to show a POSA would have made the proposed modifications with a reasonable expectation of success and/or predictable results in the context of

Watanabe. EX.2044, ¶103. Just because a POSA “could” do so, in hindsight, does not show that a POSA “would” do so. Petitioner fails to meet its burden.

PersonalWeb Techs., LLC v. Apple, Inc., 848 F.3d 987, 994 (Fed. Cir. 2017);

Belden Inc. v. Berk-Tek LLC, 805 F.3d 1064, 1073 (Fed. Cir. 2015).

As discussed herein, Laub repeatedly testified that a POSA “could” perform various modifications, in hindsight, but Laub fails to explain why a POSA “would” do so upon reading Watanabe. EX.2044, ¶103. Laub fails to consider the competing considerations in camera design discussed above. *Id.* Laub also fails to explain the requisite motivation for a POSA to modify Watanabe’s system as proposed. *Id.*

a. “digital video camera” and “digital video”

Watanabe expressly and repeatedly refers to a “digital still camera”. EX.2044, ¶105; EX.1005, [0040], [0042]. Watanabe does not disclose a digital video camera, let alone a digital video camera capable of correcting aberrations in digital video. Petitioner fails to meet its burden with respect to the proposed modifications to Watanabe to meet claim 1.

Watanabe does not refer to for example “video camera”, “videography”, “frame”, “buffer,” “MPEG” as would be expected if Watanabe applied to digital video. EX.2044, ¶¶105-106, 121-126. A POSA would understand that a video

camera capable of capturing sequential frames to form a video is also capable of capturing still images, **but not the other way around**. EX.2044, ¶124. A POSA would have to solve numerous problems to modify a still camera into a video camera, including particularly data throughput, which requires a buffer to hold at least one frame. *Id.*

Watanabe does not disclose a frame buffer. The omission of this key element shows that Watanabe is not meant for video. EX.2044, ¶¶121-124. Because Watanabe does not disclose at least a frame buffer, and because Petitioner provides no analysis for modifying Watanabe to be a digital video camera, including how a POSA would redesign the internal components of Watanabe's digital still camera, Petitioner fails to meet its burden. *Id.*; EX.2044, ¶¶127-129. The architecture of Watanabe is not designed to capture/correct successive frames of a digital video for at least the reasons discussed herein. *Id.*

Not only are there higher data throughput requirements for video, there are also additional operations to accommodate for example, changes of the focusing point and zoom position of subjects. As noted in the '685 Patent, Petitioner's proposed modification would not have been routine for a POSA. *See, e.g.,* EX.1001, 27:29-41 ("...video presents new classes of dynamic problems, most notably regarding the matter of tracking changing subjects in real time..."). This additional functionality is not disclosed in Watanabe.

i. Petitioner misplaces reliance on JP-872

Petitioner argues that Watanabe's discloses a digital video camera because "it captures video with a CCD and digitizes its output." Petition, 12. This is not correct. Petitioner relies on an incorrect translation of JP-872 (EX.1006). Even in a video camera, a CCD captures still image input, not video input.

The translation of JP-872 reads: "The CCD 3 is a circuit that converts the video input through the lens unit into an electrical signal (analog image data)..." EX.1006, 7. The EPO translation of JP-872 reads : "The CCD 3 is a circuit for converting an image input through the lens unit to electrical signals (analogue image data)..." (EX.2004, 8:11-14) and Watanabe reads: "The CCD 53 is a circuit for converting an image inputted through the lens unit to electrical signals (analogue image data)..." (EX.1005, [0037]).⁶ **Both the EPO translation and Watanabe refer to image input, not video input.**

⁶ As shown by Global Dossier, Watanabe has a related foreign counterpart publication, EP1608140. EX.2002; EX.2003. A translation of JP-872 was submitted by the patentee with the EPO to claim foreign priority ("EPO translation"). The EPO translation of JP-872 is different from Petitioner's translation of JP-872.

A POSA would understand that Watanabe's CCD captures still image input, not video input. EX.2044, ¶111. Laub agreed that a CCD captures still image input. EX., 149:1-11, 149:22-150:13. Thus, Petitioner misplaces reliance on JP-872 to suggest that Watanabe discloses a digital video camera.

ii. Petitioner misplaces reliance on the "NTSC signal"

Petitioner argues that Watanabe's digital camera is a digital video camera "because Watanabe describes digitizing video at sampling frequencies optimized 'for an NTSC signal.'" Petition, 12. This is not correct. A POSA would understand that the sampling rate of an A/D converter relates to sampling the pixels **in a single image**, not multiple successive images. EX.2044, ¶119.

At the time of invention, a POSA would understand the need for signal control to read out the charge accumulated in the CCD at least because each pixel acts as a capacitor and charge is accumulated relative to the received photons. EX.2044, ¶115. Biasing the capacitor and transferring the charge requires delicate and precise timing control to achieve a harmonious operation. *Id.* Watanabe discloses signal generator 64 which a POSA would understand is the primary source of this coordination and control. *Id.*

As disclosed, Watanabe's signal generator 64 is connected to and also has the requirement of driving the CDS, which also requires precise timing to remove

the dark noise from the pixel values and present it to the A/D converter. EX.2044, ¶116. Again, this requires precision to be sampled appropriately by the A/D converter. *Id.*

Watanabe's A/D converter 55 will convert each pixel's charge into a digital value by measuring the amount of charge at each pixel. EX.2044, ¶117. A POSA would understand that the A/D converter will "sample" (i.e., measure) each pixel at a particular rate, known as the sampling rate or sampling frequency. *Id.*; EX.2020, 150:14-151:6, 152:2-8.

Watanabe's reference to an "optimum sampling frequency" refers to fast processing by an A/D converter. EX.2044, ¶119. The sampling rate of the A/D converter does not suggest that Watanabe's digital still camera is a digital video camera. *Id.*

Considering the hardware disclosed in FIGS. 1A and 1B of Watanabe and the data path from the CCD, a POSA would understand that only a single image is processed, corrected and stored, before the next image is captured. EX.2044, ¶125.

Watanabe does not disclose for example the capability to keep up with the higher data throughput requirements for video. EX.2044, ¶126. Watanabe does not describe any type of buffer or temporary memory capable of supporting video. *Id.*

- iii. Petitioner fails to establish that modifying Watanabe's would have been routine

For at least the reasons discussed herein, there are engineering challenges for modifying a still camera into a video camera, none of which are addressed by Petitioner. EX.2044, ¶127. The proposed modification requires a redesign of Watanabe's still camera and Petitioner fails to explain why or how a POSA would do so upon reading Watanabe. *Id.* Petitioner is using hindsight bias. *Id.*

Petitioner also fails to establish that the necessary modifications would have been routine. EX.2044, ¶128. Petitioner fails to meet its burden. *Id.*

b. “integrated circuit”

Claim 1[a] recites “an integrated circuit”. Petitioner alleges that a POSA would have implemented Watanabe's CPU 57 and circuit 56 as an integrated system-on-chip. Petition, 15-17. Petitioner is using hindsight bias. Petitioner fails to establish a POSA “would” have been motivated to make the proposed modifications.

During deposition, **Laub confirmed it is not his opinion that a POSA would have implemented the CPU and DSP of Watanabe as a system-on-chip.** EX.2020, 82:10-13 (below); *see also id.*, 84:6-12.

10 | Q And is it your opinion that a POSITA
11 | would have implemented the CPU and DSP of Watanabe
12 | as a system-on-chip?
13 | A No.

Laub repeatedly answered “no” to questions regarding what a POSA “would” do. EX.2044, ¶133. Laub explained his opinions addressed the knowledge of a POSA and what “could” be done or “would be useful”, but **not** what “would be used” in the context of a particular reference. *See, e.g.*, EX.2020, 117:1-118:9 (“POSITAs would have had several reasons to use those teachings. None of this compels the POSITA, and none of those, no specific one of those ... would reach to the word “would” that you have been continually using, which is why you have heard so many no’s from me.”); EX.2020, 131:8-20 (“these are ways that were available as choices, implementation choices, to a POSITA”); EX.2020, 137:3-19 (explaining that “‘would be useful’ is different from ‘would be used.’”). Therefore, Petitioner fails to establish that a POSA **would have** made the proposed modifications. *PersonalWeb Techs.*, 848 F.3d at 994. Petitioner does not explain why a POSA reading Watanabe **would have** implemented an ASIC and Watanabe’s CPU 57 and circuit 56 in an integrated system-on-chip. EX.2044, ¶133.

As discussed above, Watanabe discloses CPU 57 and circuit 56 as discrete components. EX.1005, [0035], FIG. 1B; EX.2044, ¶114. PO submits that a POSA

would not have been motivated to implement Watanabe's CPU 57 and circuit 56 in an integrated system-on-chip. EX.2044, ¶134. A POSA would understand that a system-on-chip is usually designed for a very specific purpose. *Id.* However, Watanabe's CPU 57 and circuit 56 serve different purposes and perform multiple different functions. *Id.*

Watanabe discloses that CPU 57 "controls operation of each part of the digital still camera... by way of an [sic – a] photographing program." EX.1005, [0042]. Therefore, it would not have been obvious to implement CPU 57 and circuit 56 as a system-on-chip. EX.2044, ¶134. The CPU 57 does not only control circuit 56. *Id.* CPU 57 processes and executes programs stored in ROM and RAM. EX.1005, [0039]. CPU 57 also controls each part of the system according to the photographing program. *Id.*, [0059]. If the proposed combination were made, the overall efficiency of the camera would be reduced as a CPU would still be required to control other functions within the camera. EX.2044, ¶134. There would be slower communication and less efficient memory sharing between CPU 57 and the other camera components. *Id.* Therefore, a POSA would not be motivated to combine Watanabe's CPU 57 and circuit 56 as an integrated system-on-chip. *Id.*

In his declaration, Laub relied on a RISC processor in an exemplary system-on-chip in Texas Instruments TMS320C8x. EX.1003, ¶¶135-136. Laub offered no opinions on whether Watanabe's CPU is a reduced instruction set (RISC)

computer. EX.2020, 35:9-22. In deposition, Laub clarified that he has “made no such proposal” that the CPU of Watanabe would be a RISC processor in the proposed modification of Watanabe. EX.2020, 38:20-39:1. Laub testified that a RISC would have been known to a POSA and that a POSA “could very well have chosen to use” a RISC in order to implement Watanabe. EX.2020, 36:14-38:19. Thus, Laub testified that a POSA “could” have done so, but did not opine or explain that a POSA would have done so. EX.2044, ¶135.

Petitioner fails to explain how the alleged benefits of a system-on-chip would be applicable to Watanabe’s modified system. EX.2044, ¶136. Petitioner fails to explain how the proposed modification would have been routine or within the ordinary skill of a POSA and that a POSA would have been motivated to make the proposed modification upon reading Watanabe. *Id.* Petitioner is using hindsight bias. *Id.*

Moreover, even if a POSA were to redesign Watanabe’s camera, implementing Watanabe’s CPU and DSP as an integrated system-on-chip is not one of only two alternatives. EX.2044, ¶137. Petitioner is using hindsight bias. *Id.* Petitioner does not explain why a POSA would have selected this particular

proposed implementation. *Id.*⁷ Petitioner does not explain how the modified system of Watanabe would work.

c. “digital signal processor” (DSP)

Claim 1[a] recites “a digital signal processor”. Petitioner relies on Watanabe’s digital signal processing circuit 56 as the alleged DSP. Petition, 24.

A POSA would understand that Watanabe’s digital signal processing circuit 56 is a hardware component. EX.2044, ¶141. Interpreting a circuit to be a functional block contradicts the common understanding of a POSA of the word “circuit” which refers to hardware.⁸ *Id.* Laub testified that Watanabe’s digital signal processing circuit 56 is a “functional block.” EX.2020, 166:3-11. **This contradicts the common understanding of a POSA.** EX.2044, ¶141. A POSA reading Watanabe would understand that the circuit 56 has limited functionality, that is just sufficient for its purpose in the context of Watanabe’s system, with certain interface requirements as dictated by the figure. *Id.* A POSA would further understand the

⁷ For example, Petitioner does not address the other components disclosed in Watanabe (*e.g.*, circuit 66, circuit 62, ROM 58, RAM 59). EX.2044, ¶137.

⁸ Laub agreed that the word “circuit” refers to an electrical or electronic circuit. EX.2020, 31:8-18.

various input and output requirements dictated by the type of data that is discussed in Watanabe. *Id.* Petitioner fails to explain that a POSA would be motivated to modify Watanabe's circuit 56 to meet the claimed DSP. *Id.*

Laub agreed that a DSP "generally was well-known." EX.2020, 27:7-15. Laub admitted that "the specification of the patent presumes that a person reading that patent would understand what is referred to when the phrase 'digital signal processor' is used." EX.2020, 28:17-29:10. However, Laub opined that anything that processes digital signals is a DSP. EX.1003, ¶¶157, 161; EX.2020, 27:16-28:12, 56:14-15. **Laub's analysis is not correct.** DSP is a term of art and refers to a specific type of hardware. EX.2044, ¶142. The claims recite DSP hardware with specific functionality. *Id.*

Petitioner fails to establish that Watanabe's circuit 56 corresponds to a DSP as claimed. EX.2044, ¶143. For example, Petitioner fails to show that Watanabe's circuit 56 has flexible programming or uses software as opposed to fixed functionality hard-coded into the circuit itself. *Id.* Laub admits that a POSA would understand differences between a DSP and an ASIC based on flexible programming using software. EX.2017, ¶157; EX.2020, 52:15-53:11. Petitioner previously relied on EX. 2019 ("Ralston") which distinguishes a DSP from an

ASIC based on the flexible programming of a DSP. *See* EX.2044, ¶145; EX.2019, 7:65-8:16.⁹

Laub stated his opinions do not address whether Watanabe's circuit 56 is capable of being flexibly programmed. EX.2020, 58:15-59:3. In view of a POSA's knowledge of a DSP, Petitioner fails to show that Watanabe's circuit 56 corresponds to the claimed DSP.

d. “database management system” (DBMS)

Claim 1[a] recites “a database management system”. Petitioner relies on Watanabe's control program that allows the CPU 57 to access tables 70. Petition, 18-20. Petitioner fails to establish that Watanabe's control program accessing tables 70 corresponds to the DBMS as claimed.

Watanabe's tables 70 are “prepared in advanced” and include predetermined correction values for a distortion aberration. EX.1005, [0006], [0047]. There is no disclosure that Watanabe's control program creates, stores, changes, manipulates, sorts, formats, or prints information in tables 70 under Laub's definition of DBMS.

⁹ Petitioner's varying arguments regarding DSPs and ASICs in the related IPRs show that Petitioner is hindsight biased and using the challenged claims as a roadmap. EX.2044, ¶103.

EX.2044, ¶149. There is no disclosure that Watanabe's control program organizes/manages/updates the information in tables 70 as would be understood by a POSA. *Id.*

As discussed above, a POSA would understand that the use of the claimed DBMS/database is not merely executing code, running on a main CPU, to access a fixed look-up table of parameters as described in Watanabe. EX.2044, ¶¶150-152.

A POSA reading Watanabe would understand that tables 70 are stored in read-only memory (ROM) 58. EX.2044, ¶152; EX.1005, [0039]. Watanabe only discloses fixed tables that are prepared in advance. EX.2044, ¶152. Watanabe's tables 70 are not updatable and are not organized/managed/updated by Watanabe's control program. *Id.* For example, Watanabe does not disclose the tables can be updated for new lenses. *Id.* Watanabe highlights one of the problems the '685 Patent was designed to avoid. *Id.* For at least these reasons Watanabe fails to disclose or render obvious the claimed DBMS/database. *Id.*

2. Claim 1[d]

Claim 1[d] recites "database". Petitioner relies on Watanabe's tables 70. Petition, 22-23. As discussed above, Petitioner does not show that Watanabe's tables 70 are updatable and a POSA would understand that the use of the claimed

DBMS/database is not merely executing code, running on a main CPU, to access a fixed look-up table of parameters as described in Watanabe. EX.2044, ¶154.

3. *Claim 1[f]*

Petitioner relies on Watanabe's circuit 56 as allegedly performing digital filtration to correct an optical image aberration as claimed. Petition, 24-25. For at least the reasons discussed herein, Petitioner fails to show that Watanabe's circuit 56 corresponds to the claimed DSP. *See infra*, section III.B.1.

Additionally, Petitioner's characterization of Watanabe's circuit 56 is incorrect. EX.2044, ¶¶155-178. A POSA reading Watanabe would understand that Watanabe's CPU, not circuit 56, performs the aberration correction. *Id.*

a. **Watanabe's CPU 57 – not circuit 56 - executes a correction process**

Watanabe expressly discloses that “CPU 57 executes... a correction process on image data...” EX.1005, [0042]. Watanabe also discloses that “RAM 59 temporarily stores data *to be processed by the CPU 57*”. EX.1005, [0039] (emphasis added).

Watanabe discloses that CPU 57 “processes image data by way of an image processing program.” EX.1005, [0042]. Watanabe further discloses that “CPU 57 executes the image processing program” including step 104 for “image processing” shown in FIG. 4. EX.1005, [0060]; FIG. 3 (image processing program 71 accessing

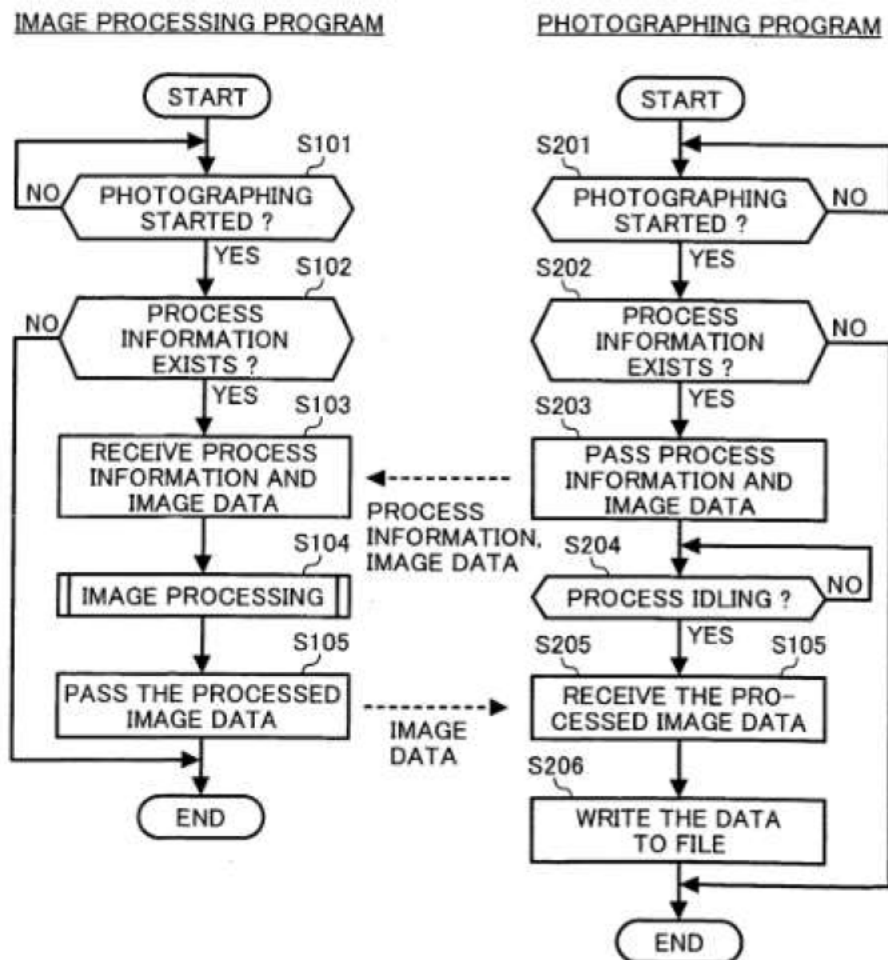
correction value table 70). The CPU 57 also executes step 105 to pass the processed image data to the photographing program. EX.1005, [0058], [0062].

A POSA reading Watanabe would understand that it is Watanabe's CPU 57 that performs aberration correction, not circuit 56. EX.2044, ¶160. Watanabe relies heavily on CPU 57 which has more functionality and more processing power, than circuit 56. *Id.* Watanabe's heavy dependence on the CPU 57 is contrary to the claimed inventions of the '685 Patent that efficiently distribute the workload by using the claimed DSP for specific functions. *Id.*

Watanabe does not disclose that circuit 56 corrects an aberration by applying digital filtration, or that circuit 56 corrects an aberration using the correction values in tables 70. EX.2044, ¶161. Watanabe does not disclose Watanabe's CPU 57 passing correction values to Watanabe's circuit 56. EX.2044, ¶162. Watanabe expressly teaches away from transmitting process data "between apparatuses" because the process becomes "complicated". EX.1005, [0008]. Instead, Watanabe teaches the image processing program and the photographing program can be executed in a single component, the CPU 57. EX.2044, ¶162. The photographing program passes process information and image data to the image processing program (steps 103, 203), the image processing program performs image processing (step 104), and the image processing program passes the

processed image data to the photographing program (steps 105, 205), **all of which is done within the CPU 57.** *Id.*; EX.1005, FIG. 4.

FIG. 4



Petitioner misinterprets Watanabe's one sentence disclosure that "the digital signal processing circuit 56 sorts out the image data inputted from the A/D converter 55 into color-difference data and brightness data, and executes various process, correction and a data process for image compressing/extracting."

EX.1005, [0038]; EX.2044, ¶163. This sentence does not disclose that Watanabe's

circuit 56 performs aberration correction to image data based on the process information. *Id.* Nor does this sentence disclose that Watanabe's circuit 56 obtains correction values from tables 70. *Id.* Regardless of whatever "correction" may be performed by Watanabe's circuit 56, there is no disclosure that circuit 56 performs the functions of the claimed DSP. *Id.*

Claim 1[f] specifically refers to correcting the "optical image aberration." Therefore, any digital corrections that may be performed by Watanabe's circuit 56 do not meet this claim limitation. EX.2044, ¶164 (discussing for example gamma correction and other digital corrections that may be performed). Petitioner fails to establish that Watanabe's circuit 56 performs the specific functions of the claimed DSP.

Watanabe further confirms that it was conventional thinking to use CPU-intensive processes to perform aberration correction, which is opposite to the claimed inventions of the '685 Patent. EX.2044, ¶165.

b. Watanabe's CPU executes distortion correction OR peripheral light intensity correction

Watanabe's distortion correction and peripheral light intensity correction are different correction processes. EX.2044, ¶¶166-167. Laub agreed that the correction values for distortion aberration correction are not the same as the correction values for peripheral light intensity correction. EX.2020, 90:15-19. A

POSA reading Watanabe would understand these are different correction processes with different correction values. EX.2044, ¶¶166-169.

Watanabe discloses “an image process such as distortion aberration correction *or* peripheral light intensity correction can be executed.” EX.1005, [0064](emphasis added). Watanabe discloses “a predetermined correction process” is executed “in conformity with the process information”. EX.1005, [0042], [0058]. At step 104 of FIG. 4, the image processing program of Watanabe does not perform **both** distortion correction and peripheral light intensity correction. EX.2044, ¶170.

Watanabe’s CPU is capable of performing both correction processes, and selects/performs one of the predetermined correction processes based on the process information. Petitioner fails to establish how and why a POSA would have modified Watanabe’s circuit 56 to perform any aberration correction, let alone both correction processes. As discussed herein, Watanabe’s circuit 56 does not have access to correction values in tables 70; a POSA reading Watanabe would not be motivated to have Watanabe’s CPU pass process information to circuit 56 to select correction values; and a POSA would not be motivated to have Watanabe’s CPU 57 select correction values/algorithms and pass them to circuit 56 for processing. EX.2044, ¶¶173-176. As discussed herein, Watanabe’s circuit 56 is a fixed circuit with limited functionality.

C. CLAIM 2

Petitioner argues that claim 2 recites “optical aberrations” and that this plural recitation has no antecedent basis in claim 1. Petition, 26. This is not correct. The preamble of claim 1 recites “optical image aberrations” where aberrations is plural. EX.2044, ¶180.

Petitioner alleges that Watanabe discloses correcting “curvature aberration” and “lens distortion”. Petition, 27. This is not correct. Petitioner misplaces reliance on the translation of JP-872 (EX.1006).

Petitioner argues that the translation of JP-872 discloses “curvature aberration” but the translation is not correct. The EPO translation of JP-872 reads “distortion aberration correction” (EX.2004, 10:10-11) and Watanabe reads “distortion aberration correction” (EX.1005, [0046]). Petitioner therefore relies on an incorrect translation of JP-872. Neither the EPO translation of JP-872 nor Watanabe refer to “curvature aberration correction.” EX.2044, ¶¶182.

Consistent with the Board’s previous interpretation, claim 2 of the ‘685 Patent differentiates “lens distortion” aberration and “curvature of field” aberration. Paper 11, 30. The Board previously interpreted JP-872 as failing to disclose “curvature of field” correction. *Id.* Neither JP-872 nor Watanabe disclose “curvature aberration” as alleged by Petitioner.

D. CLAIM 5

1. Claim 5[a]

Watanabe discloses Watanabe's CPU 57 "determines a table according to a lens type." EX.1005, [0047]. However, Watanabe does not disclose each lens type is "registered" in the alleged database as required by claim 5[a].

Petitioner fails to show that that Watanabe's control program, the alleged DBMS, registers each lens type in tables 70. EX.2044, ¶¶186-188. Registering each lens type, especially new lenses, is one of the functions of the claimed DBMS. *Id.* Watanabe does not disclose or render obvious the claimed DBMS/database at least because Watanabe only discloses fixed tables that are prepared in advance. *Id.*; EX.1005, [0047]. Watanabe highlights one of the problems that the '685 Patent was designed to avoid.

2. Claims 5[b] and 5[c]

As discussed above, Petitioner fails to establish that Watanabe discloses corrections for curvature aberration.

Moreover, Petitioner fails to explain how Watanabe's correction values meet both "multiple optical aberrations" in claim 5[b] and "filtration solutions" in claim 5[c]. EX.2044, ¶192. Claims 5[b] and 5[c] recite **listing** "multiple optical aberrations" and **listing** "filtration solutions" in the database. *Id.* Petitioner fails to show that Watanabe meets claims 5[b] and 5[c]. *Id.*

3. *Claims 5[d] and 5[e]*

As discussed above, Watanabe discloses the CPU performs the alleged correction, not circuit 56, the alleged DSP. *See infra*, section III.B.3.

E. CLAIM 6

PO incorporates the above discussion of claim 1. *See infra*, section III.B.

F. CLAIM 7

PO incorporates the above discussion of claim 2. *See infra*, section III.C.

G. CLAIM 12

PO incorporates the above discussion of claim 1. *See infra*, section III.B.

For at least the reasons discussed above, Petitioner fails to establish that “an SoC is an obvious design choice” as alleged.

H. CLAIM 14

PO incorporates the above discussion of claim 1. *See infra*, section III.B.

Additionally, with respect to claims 14[e], 14[f], and 14[g], Petitioner states that there were only two known alternatives: (1) storing the algorithm as executable code in Watanabe’s circuit 56 or (2) storing the algorithm in some other memory and loading the algorithm into the circuit 56 as needed. Petition, 36. **This is not correct.** There are not only “two” alternatives. EX.2044, ¶173. The algorithm could be hard-coded into the circuit. *Id.* A POSA would have understood

Watanabe's circuit 56 is a hard-coded circuit. EX.2044, ¶¶173-176. A POSA would have understood that using a hard-coded circuit, such as circuit 56, provides for fast computation.¹⁰ *Id.*

Both proposed alternatives rely on modifications to Watanabe. EX.2044, ¶¶174-175. Watanabe does not disclose that circuit 56 includes software comprising executable code. *Id.* Watanabe does not disclose that circuit 56 is configured to access correction values tables 70. There is no suggestion that a POSA would load an algorithm into circuit 56 "as needed". *Id.*

Watanabe expressly distinguishes prior art "where process data need[s] to be transmitted between apparatuses" because "the process becomes complicated." EX.1005, [0008]. Therefore, a POSA reading Watanabe would not be motivated to have Watanabe's CPU pass process information to circuit 56; and a POSA would not be motivated to have Watanabe's CPU 57 select correction values/algorithms and pass them to circuit 56 for processing. EX.2044, ¶176. As discussed above, the selection and processing is all done by Watanabe's CPU 57. *Id.*

¹⁰ Laub testified that computation time would be considered by a POSA as a factor when designing a camera, "if there is a consideration for how quickly a finished result can be delivered." EX.2020, 24:5-8.

I. CLAIM 15

PO incorporates the above discussion of claim 2. *See infra*, section III.C.

J. CLAIM 29

PO incorporates the above discussion of claim 2. *See infra*, section III.C. PO submits the Board correctly determined in the Institution Decision that Petitioner fails to meet its burden. Paper 11 at 29-30.

IV. GROUND 2 FAILS

A. OVERVIEW OF KISHIDA

Kishida relates to correction of an observation image by **a microscope**. EX.1007, Abstract. Kishida does not teach in-camera aberration correction as claimed in the '685 Patent. EX.2044, ¶207. Kishida teaches exposure or white balance correction based on a shading prediction result. EX.1007, [0010]. Kishida explains that the shading prediction result is predicted from the background image, **which is an image captured separately from the object image and does not include the object**. EX.1007, [0015]. Kishida explains that the background image is stored in a memory unit of the PC 46 itself. EX.1007, [0043].

Kishida explains “[t]he user of this system first removes the observation specimen on the stage 18 from the field of view of the observation image. Here, an instruction is given to operate an input device 47, such as a mouse, to click one of the positions on the background photographing button 301 displayed on the

imaging screen When the PC 46 receives this instruction, it starts executing the steps shown in Fig. 4.” EX.1007, [0045].

B. THE PROPOSED COMBINATION OF WATANABE+KISHIDA

Petitioner fails to address the technological incompatibility of Watanabe and Kishida. EX.2044, ¶¶223-224. Petitioner fails to establish that a POSA interested in optimizing a digital camera would look to a reference focused on an exemplary microscope. *Id.* Petitioner does not explain how Kishida’s use of an external PC even could, let alone would, be implemented in Watanabe’s digital camera. *Id.*

Petitioner does not explain how Watanabe+Kishida avoids the “known problems with processing requirements.” Petition, 40; EX.2044, ¶224. Laub does not explain how implementing Kishida’s techniques in Watanabe’s system does not require “huge” additional processing power. EX.1003, ¶325; EX.2044, ¶224. Neither Petitioner nor Laub explain how Watanabe+Kishida would work. Petitioner fails to meet its burden. *PersonalWeb Techs.*, 848 F.3d at 994.

Laub opined that “Kishida implemented its techniques in software” and that the software “could [be] incorporated in Watanabe’s ‘control program’.” EX.1003, ¶225 (citing EX.1007, [0020]). Laub’s analysis fails for at least because the cited paragraph 20 of Kishida does not support Petitioner’s proposed modification. EX.2044, ¶225. Kishida discloses “executing this program with a computer”.

EX.1007, [0020]. As discussed herein, the teachings of Watanabe and Kishida are technologically incompatible.

1. Technological incompatibility of Watanabe and Kishida

Petitioner fails to consider how shading correction is actually performed by Kishida. EX.2044, ¶228. Kishida's exposure correction control based on a shading prediction result is performed by the external PC 46 of Kishida. EX.1007, [0044] (“...in the following explanation, the processing performed by the PC 46 is realized by the CPU of the PC 46...”). Thus, the process of Kishida does not relate to in-camera correction. EX.2044, ¶229. Petitioner fails to explain how Watanabe+Kishida would work.

Petitioner fails to address a background image as taught by Kishida and Petitioner fails to explain how this technique would be implemented in Watanabe's system, or why a POSA would be motivated to do so. EX.2044, ¶231. Kishida explains that the prediction result is predicted from the background image, **which is an image captured separately from the object image and does not include the object**. EX.1007, [0015].

In the context of microscopes, there is a consistent, static background and it is possible to capture a background image **in which the observation specimen is not present**. *See, e.g.*, EX.1007, [0048]. In the context of a microscope, the device

is stationary, situated on a workbench with a target image area that has consistent and repeatable imaging characteristics. EX.2044, ¶232. In the context of digital cameras, there is not a consistent background and it is unlikely a background image without the subject could be obtained. *Id.* Further, it is unlikely an image with the subject would have the exact same background as the background image. *Id.*

Petitioner also fails to address a control value as taught by Kishida and Petitioner fails to explain how this technique would be implemented in Watanabe's system, or why a POSA would be motivated to do so. EX.2044, ¶233; EX.1007, [0052], [0058]. Kishida's control value is specific to the background in the background image. *Id.* While this control value may be suitable for a microscope with a static background, it would not be practical for a digital camera. *Id.*

Petitioner also fails to address the order of corrections in Watanabe+Kishida. EX.2044, ¶236. Kishida warns that if the shading correction is applied to an image after an exposure or white balance correction has already been applied to the image, there is a risk of over-correction. EX.1007, [0007]. Watanabe does not disclose performing different corrections in a different order. EX.2044, ¶236. Petitioner does not address how Watanabe's control program would purposefully order the corrections allegedly performed by Watanabe's circuit 56, consistent with the teachings of Kishida. *Id.*

Petitioner fails to meet its burden regarding the proposed combination of Watanabe+Kishida. *PersonalWeb Techs.*, 848 F.3d at 994.

C. CLAIMS 3, 13, AND 19

PO incorporates the above discussion of claim 1. *See infra*, section III.B. For at least the reasons discussed above, Petitioner fails to establish that Watanabe's circuit 56 corresponds to the claimed DSP.

Moreover, Petitioner fails to establish that the teachings of Watanabe and Kishida are technologically compatible. EX.2044, ¶¶228-236. PO submits they are not. A POSA would not be motivated to make the proposed combination.

Petitioner alleges that Watanabe alone discloses correction of vignetting based on correction values stored in tables 70. Petition, 40. Petitioner further alleges that Kishida discloses correction of vignetting. Petition, 43. Petitioner fails to explain how Watanabe's vignetting correction technique is properly combinable with Kishida's vignetting correction technique. EX.2044, ¶239. Petitioner is using hindsight bias. *Id.* For at least the reasons discussed above, the techniques of Watanabe and Kishida are technologically incompatible. *Id.* Petitioner never considered for example the background image required to perform Kishida's technique.

As discussed above, Petitioner fails to explain how and why a POSA would have implemented Kishida's technique in Watanabe's system. Petitioner fails to explain how Watanabe+Kishida would work.

V. **GROUND 3 FAILS**

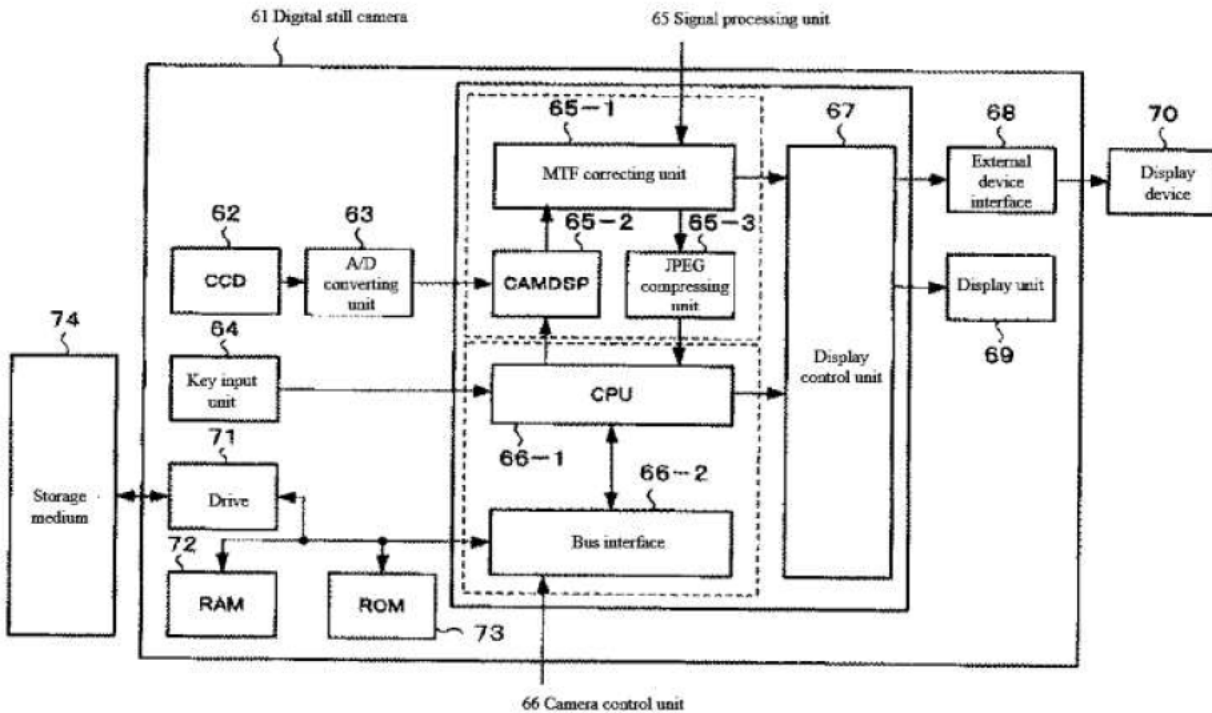
A. OVERVIEW OF KITA

Kita discloses “a method to restore the lost high-frequency-domain frequency characteristics... using the inverse function of the lens MTF characteristics.” EX.1008, [0078].

“[A]n image of a certain block is cropped from the original image, and a frequency-domain image is generated from the cropped time-domain image” and “this frequency-domain image is multiplied by the filter of the inverse function of the transfer function according to the amount of optical adjustment for the optical system using a multiplier.” EX.1008, [0010]. Then, “the result of this multiplication is converted from the frequency domain back to the time domain.”

Id.

FIG. 6 of Kita shows signal processing unit 65 including MTF correcting unit 65-1, camera processing unit (CAMDSP) 65-2, and JPEG compression unit 65-3.



EX.1008, FIG. 6.

Kita teaches the zooming amount, defocusing amount, and diaphragming amount are determined by an exchange between CAMDSP 65-2 and camera control unit 66. EX.1008, [0049].¹¹ The image information output from CAMDSP 65-2 is input to the MTF correcting unit 65-1 at the same time as the zooming

¹¹The CAMDSP is a different component than the MTF correcting unit 5-1.

EX.2044, ¶256. Thus, Kita teaches that the component specifically identified as a digital signal processor in Kita is not itself involved with the application of a fast Fourier transform and thus, teaches away from the claims of the '685 Patent. *Id.*

amount, defocusing amount, and diaphragming amount (e.g., aperture of an iris diaphragm). EX.1008, [0057]. The zooming amount, defocusing amount, and diaphragming amount are used as keys to select MTF correction filters. EX.1008, [0059]. The MTF correction filter is determined from table 87 according to each parameter. EX.1008, [0059]. **The MTF correction filter is applied by the MTF correction unit 65-1.** EX.1008, [0046].

B. THE PROPOSED COMBINATION OF WATANABE+KITA

As discussed herein, Watanabe's method uses correction values in tables 70. EX.2044, ¶248. There is nothing in Watanabe to suggest or otherwise invite a POSA to use Kita's techniques in the frequency domain. *Id.* Petitioner fails to establish that Watanabe's system could or would implement the functionality discussed in the cited portions of Kita. *Id.* MTF compensation as considered by Kita is completely different than the teachings of Watanabe. *Id.* Petitioner also fails to establish that Watanabe's circuit 56, the alleged DSP, could implement the functionality discussed in the cited portions of Kita. *Id.*

Moreover, in a related IPR, Petitioner alleges an ASIC would be used for repetitive and labor intensive functions. IPR2024-0095, Petition, 47. Here, however, Petitioner alleges that the alleged DSP of Watanabe would be modified to perform FFT processing. EX.2044, ¶264. Petitioner's analysis is inconsistent. *Id.*

Petitioner fails to explain how or why a POSA would be motivated to make the proposed modification. *Id.*

A POSA would not have been motivated to combine Watanabe+Kita as proposed. EX.2044, ¶¶248-253. Petitioner is using hindsight bias. *Id.*

1. Technological incompatibility of Watanabe and Kita

Petitioner argues that a POSA would implement Kita's techniques in Watanabe's control program, without considering how Kita actually uses FFT for its intended purpose. EX.2044, ¶255. A POSA would understand that FFT is a way to represent data in the frequency domain to then further process the image data. *Id.* The FFT itself does not perform any correction. *Id.* Watanabe does not consider manipulating data in this manner for processing using a MTF filter. *Id.* A POSA reading Watanabe would not consider doing so either. *Id.*

Petitioner does not address the hardware components of Watanabe or explain how Watanabe's hardware supports Kita's techniques. EX.2044, ¶257. Petitioner further does not address Kita's hardware used for Kita's techniques. *Id.* Kita relies on distinct hardware elements that are not present or discussed in Watanabe's system. EX.2044, ¶¶258-261.

Petitioner also does not explain how Kita's techniques, software or otherwise, could be implemented in Watanabe's system, at least because Kita's approach is so different from that of Watanabe. EX.2044, ¶¶262-264.

2. Watanabe+Kita changes Watanabe's principle of operation

Aberrations, such as vignetting, contribute to degradation of the MTF and the MTF reflects their total effect. Therefore, based on the teachings of Kita, the MTF correction filter would correct vignetting and there would be no need to perform the vignetting correction methods disclosed in Watanabe. EX.2044, ¶267. Petitioner fails to explain how and why incorporating the teachings of Kita into Watanabe's system would add additional correction capabilities to the methods disclosed in Watanabe, as opposed to a wholesale replacement of the methods disclosed in Watanabe. *Id.* Petitioner is using hindsight bias. *Id.*

C. CLAIMS 4, 8, 9, AND 16

As discussed above, Petitioner fails to explain how and why a POSA would have implemented Kita's techniques in Watanabe's system. Petitioner fails to show that Watanabe+Kita renders obvious the alleged DSP applying a FFT to correct an aberration as recited in the claims.

At no point does Petitioner address Watanabe's circuit 56, the alleged DSP in its analysis. Petition at 46. There is nothing in Watanabe or Kita to suggest that

Watanabe's circuit 56, the alleged DSP, is capable of applying FFT-based image processing as disclosed in Kita. EX.2044, ¶¶269-271. There is no evidence that a POSA would have been motivated to modify Watanabe's circuit 56 to do so.

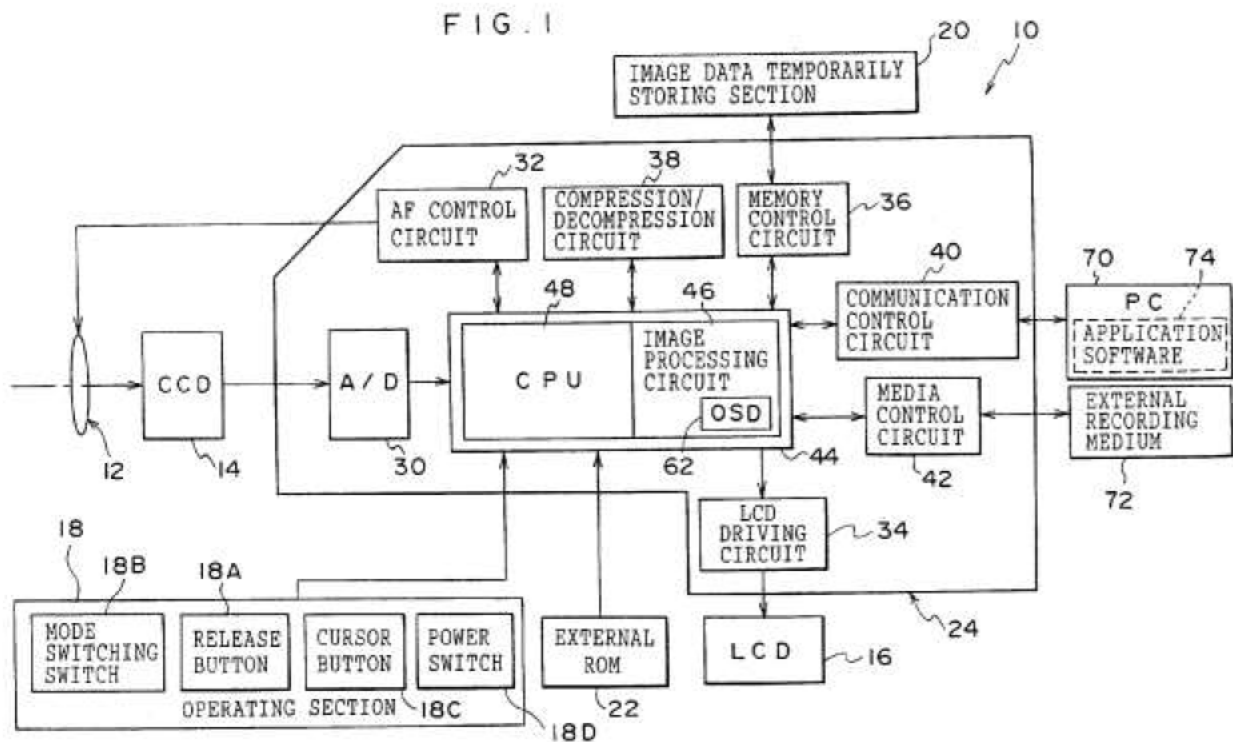
Petitioner and Laub point to discrete teachings in each reference without considering each claim as a whole. EX.2044, ¶272. Neither Petitioner nor Laub explain how these discrete teachings would have been combined to arrive at the claims of the '685 Patent. *Id.*

The teachings of Watanabe and Kita are technologically incompatible such that a POSA reading Watanabe would not have been motivated to use FFT-based image processing as disclosed in Kita. EX.2044, ¶¶272-273. A POSA would understand that Watanabe's system is not capable of FFT-based image processing as disclosed in Kita. *Id.* Petitioner fails to explain how modifying Watanabe's circuit 56, the alleged DSP, to perform FFT was within the ordinary skill of a POSA and would have been routine. *Id.*

VI. GROUND 4 FAILS

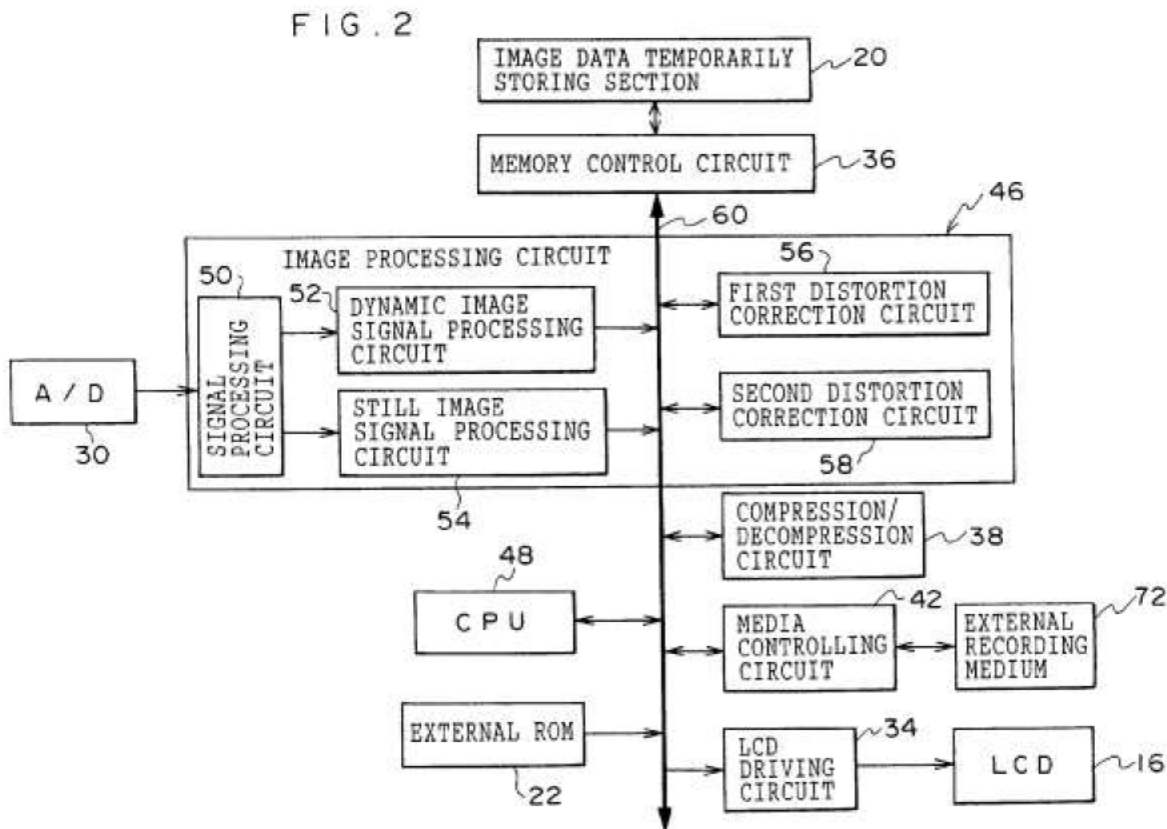
A. OVERVIEW OF TAKANE

Takane's FIG. 1 shows a digital camera 10 including image processing circuit 46.



EX.1009, FIG. 1

Takane's imaging processing circuit 46 is further shown in FIG. 2:



EX.1009, FIG. 2

Takane discloses the signal processing circuit 50 inputs digital image data from the A/D converter, processes the data, *e.g.*, white balance adjustment, gamma correction, sharpness correction, and converts the RGB data into a YC signal.

EX.1009, [0044]. The output of circuit 50 is connected to the dynamic image signal processing circuit 52 and the still image signal processing circuit 54.

EX.1009, [0044]-[0045]. The signal processing circuit 52/54 converts the gradation such that the image size becomes a predetermined image size set in advance.

EX.1009, [0047]. Then, the data is input to the first distortion correction circuit 56 or the second distortion correction circuit 58. EX.1009, [0053].

Takane expressly distinguishes the functionality of the first distortion correction circuit 56 from the second distortion correction circuit 58.

The first distortion correction circuit 56 can carry out processing at a low correction accuracy. EX.1009, Abstract, [0061], [0115]. The first distortion correction 56 carries out processing when the release button 18A is depressed halfway for a “preview display.” EX.1009, [0091], [0117].

“The correction accuracy is intentionally lowered, and the processing time can be shortened and the circuit structure of the first distortion correction circuit 56 can be made simple.” EX.1009, [0061]. For example, in the described embodiment, “only the distortion in the horizontal direction is corrected at the first distortion correction circuit 56.” EX.1009, [0062].

The second distortion correction circuit 58 can carry out processing at a high correction accuracy. EX.1009, Abstract. The second distortion correction 58 carries out processing when the release button 18A is fully depressed at the time of “actual photographing.” EX.1009, [0092], [0117].

The parameters stored in the second distortion correction circuit 58 give priority to the quality of each image and provide a high correction accuracy. EX.1009, [0063]. Unlike the first distortion circuit 56, the second distortion circuit

58 will correct optical distortion in both the horizontal and vertical directions.

EX.1009, [0094].

B. THE PROPOSED COMBINATION OF WATANABE+TAKANE

Petitioner does not explain how Takane's techniques actually work and Petitioner does not explain how or why a POSA would have incorporated those teachings into Watanabe's system. EX.2044, ¶286.

Petitioner fails to address that Takane teaches the use of different circuits with different functionality. EX.2044, ¶¶286-289. Takane's signal processing circuit 50 performs white balance adjustment. EX.1009, [0044]. Takane's distortion correction circuits 56/58 perform distortion correction. EX.1009, [0054]. Petitioner fails to explain how these functionalities could or would be incorporated in Watanabe's circuit 56, the alleged DSP. EX.2044, ¶289.¹² For example, Takane's circuits 56/58 provide different levels of correction and use different parameters. EX.2044, ¶290; EX.1009, [0059]. Also, Takane's circuit 56 is used to provide a "preview" image when the release button 18A is depressed halfway. EX.1009,

¹² Laub opined that Watanabe+Takane would not require additional circuitry.

EX.1003 at ¶¶380, 386, 389, 390. Laub fails to explain how and why

Watanabe+Takane would work.

[0085], [0086], [0087]. Petitioner does not explain how Watanabe's system could be modified to provide "preview" displays. EX.2044, ¶291.

As further discussed herein, Takane's teachings are not properly combinable with Watanabe because it would change Watanabe's principle of operation, specifically with respect to tables 70. EX.2044, ¶293. Takane expressly teaches away from using tables and instead stores correction parameters in the circuits 56/58. *Id.* Petitioner fails to explain why a POSA would be motivated to combine inapposite teachings of two references that describe completely different approaches. *Id.*

Petitioner is using hindsight bias. EX.2044, ¶289. A POSA would not have been motivated to make the proposed modifications to Watanabe. *Id.*

C. CLAIMS 10 AND 18

Petitioner relies on the functionality of Takane's signal processing circuit 50, added to Watanabe's circuit 56. Petition, 48. Petitioner fails to explain how and why a POSA would implement the functionality of Takane's circuit 50 into Watanabe's circuit 56. EX.2044, ¶¶297-302. Petitioner does not even explain how Takane performs, e.g., white balance adjustment. *Id.*

D. CLAIMS 28 AND 30

Petitioner relies on the functionality of Takane's correction circuits 56/56. Petition, 49. For at least the reasons discussed above, Petitioner fails to explain how and why a POSA would implement this functionality into Watanabe's circuit 56. EX.2044, ¶¶305-306.

VII. GROUND 5 FAILS**A. OVERVIEW OF HISAMATSU**

Hisamatsu expressly relates to a "still camera". EX.1010, [0002], [0005]. Hisamatsu discloses an "arithmetic operation unit" that performs "data arithmetic operation processing". EX.1010, [0005], [0019].

B. PROPOSED COMBINATION OF WATANABE+HISAMATSU

In the Background section, Hisamatsu lists certain known aberrations. EX.1010, [0002]. Just because these aberrations were known does not show that Hisamatsu corrects these aberrations. EX.2044, ¶311. Petitioner does not establish that Hisamatsu discloses how to correct these aberrations. *Id.* For example, Petitioner does not describe or otherwise explain the "data arithmetic operation processing" for correcting these aberrations. EX.1010, [0019]. Petitioner is using hindsight bias and fails to explain how and why a POSA would implement Watanabe+Hisamatsu. EX.2044, ¶¶312-315.

C. CLAIMS 22, 23, AND 25

Petitioner fails to establish that Hisamatsu discloses machine readable instructions or that Hisamatsu's techniques are implemented using software. EX.2044, ¶¶316-317. Petitioner fails to establish that Hisamatsu discloses correcting for spherical, chromatic, or coma aberrations. *Id.* Petitioner fails to explain how a POSA would have incorporated Hisamatsu's teachings into Watanabe's system. *Id.* Petitioner is using hindsight bias. *Id.*

VIII. GROUND 6 FAILS

A. OVERVIEW OF TURNER

Turner explains "[l]ight scattering effects are removed from the corrected image frame **based upon characteristics of the digital sensor.**" EX.1011, Abstract (emphasis added).

Turner requires selecting a stable region of interest in a received image frame. EX.1011, FIG. 3, [0020], [0021]. Then, Turner receives a plurality of images frames from the digital sensor when exposed to a known light quality, *e.g.*, calibration device. EX. 1011, Abstract, [0020]. Then, Turner receives a plurality of image frames from the digital sensor when exposed to dark conditions, *e.g.*, placing a lens cover over the sensor to generate a dark condition. EX. 1011, Abstract, [0020]. Then, Turner enhances the image frame. EX.1011, [0022].

B. THE PROPOSED COMBINATION OF WATANABE+TURNER

Petitioner does not explain how Turner operates and Petitioner does not explain how a POSA would incorporate the teachings of Turner into Watanabe's system. EX.2044, ¶¶325-326. For example, Watanabe does not discuss correction values based on the characteristics of CCD 53. *Id.*

Petitioner fails to explain how and why a POSA would have used Turner's teachings regarding exposure to light and dark conditions. EX.2044, ¶¶327-328. Petitioner fails to establish that the proposed modifications would have been routine. *Id.*

C. CLAIM 24

Petitioner fails to establish that Turner discloses machine readable instructions or that Turner's techniques are implemented using software. EX.2044, ¶330. Petitioner fails to explain how a POSA would have incorporate Turner's teachings into Watanabe's system. *Id.* Petitioner is using hindsight bias. *Id.*

IX. GROUND 7 FAILS**A. OVERVIEW OF LIEGE**

Liege discusses an "appliance chain" where the system corrects/modifies defects introduced by each appliance in the chain. EX.1012, 30:18-20. Formatted information 15 represents the defects of each appliance. EX.1012, 31:41-45.

Liege discloses that the observer (e.g., the photographer) is an appliance.

EX.1012, 8:19-36, 9:49-52. **Liege refers to astigmatism of an observer, not astigmatism aberration in an image.** EX.1012, 4:13-19 (explaining the formatted information is “related to the vision characteristics of the observer, especially functional anomalies of the eyes and/or of the brain of the observer.”), 36:21-25.

B. THE PROPOSED COMBINATION OF WATANABE+LIEGE

Petitioner does not explain how Liege operates and Petitioner fails to explain how a POSA could have or would have incorporated Liege’s teachings into Watanabe’s system. EX.2044, ¶¶335-341. Petitioner also fails to establish that Watanabe’s system is capable of performing corrections as taught by Liege. *Id.* For example, Petitioner does not discuss operators as disclosed in Liege. *Id.*

Petitioner alleges that Watanabe’s table 70 would be modified to include formatted information 15.1-15.n (Petition, 52), but this information is not sufficient to perform image processing based on the teachings of Liege, because the operators 23.1-23.n require **modified formatted information 15.1’-15.n’**. EX.2044, ¶¶340-341.

C. CLAIM 25

Liege refers to astigmatism of an observer, not astigmatism aberration in an image. For at least the reasons discussed above, Petitioner fails to meet its burden. *PersonalWeb Techs.*, 848 F.3d at 994.

X. GROUND 8 FAILS

A. THE PROPOSED COMBINATION OF TAKANE+WATANABE

In the proposed combination of Takane+Watanabe, Petitioner alleges that Takane would be modified to store the correction parameters in a table in Takane's ROM 22 and that Takane's software would retrieve the correction parameters and load them into the distortion correction circuits at the time of image capture. Petition, 57,60; EX.2044, ¶¶349-351. A POSA would not have been motivated to modify Takane based on the teachings of Watanabe as proposed. *Id.*

Petitioner relies on Takane's digital camera shown in FIGS. 1 and 2, including for example lens 12, CCD 14, A/D converter 30, CPU 48, and image processing circuit 46. A POSA would understand these are hardware components of Takane's digital camera 10. EX.2044, ¶348.

Laub opined that "Takane does not describe how distortion correction circuits 56 or 58 are implemented." EX.1003, ¶474. **This is not correct.** Takane discloses complete hardware diagrams in FIG. 1 and FIG. 2. EX.2044, ¶346. A POSA would be familiar with the hardware components disclosed in Takane and a

POSA reading Takane would understand the hardware capabilities and required resources. *Id.* A POSA would have understood that modifying these hardware components would affect at least the size, weight, and power-requirements of the modified camera and a POSA cannot ignore the impact of these modifications. *Id.*

Laub opined that “Takane leaves the camera’s data storage and retrieval techniques to the implementer.” EX.1003, ¶442. **This is not correct.** Takane expressly discloses that the correction parameters are set in advance and stored in the correction circuits 56/58 themselves. EX.1009, [0054],[0059]; EX.2044, ¶353.

The proposed modification would change Takane’s principle of operation. Takane teaches storing correction parameters in circuits 56 and 58 and does not use a separate table as disclosed in Watanabe. EX.2044, ¶¶355-356. A POSA would not be motivated to modify Takane based on Watanabe as proposed. *Id.* Storing the parameters in tables in Takane’s ROM 22 would be inefficient and change Takane’s principle of operation. *Id.*

1. The proposed modification changes Takane’s principle of operation

As discussed herein, Takane expressly discloses that the correction parameters are “stored in advance” in the correction circuits 56/58 themselves. EX.1009, [0054] (“Parameters expressing a polynomial... are stored in advance in

each of the first distortion correction circuit 56 and the second distortion correction circuit 58.”), [0059] (“[T]he parameters... are set in advance...”); EX.2044, ¶362.

Takane teaches away from storing the correction parameters in a separate table, and modifying Takane to store the correction parameters in a separate table would change Takane’s principle of operation. EX.2044, ¶406.

Takane expressly teaches away from prior art that uses a table of correction amounts that require a large storage capacity, which reduces the work region and increases costs. EX.1009, [0007]. Takane also distinguishes prior art that stores the correction parameters (the coefficients of the polynomial) in a separate table. EX.1009, [0008]. Takane instead teaches storing the correction parameters in the correction circuits 56/58 in advance. EX.2044, ¶356. Therefore, Petitioner’s proposed combination of Takane+Watanabe changes Takane’s principle of operation. EX.2044, ¶355.

A POSA would understand that because the correction parameters are stored in the circuits 56/58 “in advance”, the correction parameters are stored in the circuits 56/58 before the time of image capture. EX.2044, ¶¶352-353. For example, a POSA reading Takane would understand that the image size and/or focal length is designated by the user in advance, before the time of image capture, and the correction parameters are stored in the correction circuits 56/58 in advance, before

the time of image capture. *Id.* The correction parameters are selected based on the designated image size and/or focal length. EX.2044, ¶251; EX.1009, [0060].

Takane discloses that the user can designate/set various image capture parameters such as image size or focal length before the time of image capture. EX.2044, ¶¶360-361; EX.1009, [0034], [0047], [0048], [0049]. These image capture parameters are different from the correction parameters (polynomial coefficients) used by distortion correction circuits 56/58. *Id.*

2. A POSA would not be motivated to store correction parameters in the external ROM 22 as opposed to in the correction circuits 56/58

Takane's ROM 22 is described as an external ROM. EX.1009, FIG. 1, [0052]. Takane discloses "an external ROM 22 in which various programs, parameters, conversion tables and the like are stored in advance." EX.1009, [0033]. However, the parameters stored in Takane's ROM 22 are **not** the correction parameters stored in the correction circuits 56/58. EX.2044, ¶364. The parameters stored in Takane's ROM 22 relate to image capture parameters. *Id.*

For example, Takane explains the ROM 22 stores bitmap data "in advance" to be "superposed" on the subject and displayed on the LCD 16. EX.1009, [0070], [0071]. These image capture parameters do relate to image processing, but the image capture parameters are not the same as the correction parameters stored in

circuits 56/58. EX.2044, ¶364. For example, focal length is an image capture parameter and the focal length may be “superposed” on the image. *Id.*; EX.1009, [0090].

Instead of using the external ROM 22 to store correction parameters, Takane explains that correction parameters are set in advance and stored in the correction circuits themselves. EX.2044, ¶365; EX.1009, [0054].

Petitioner argues a POSA would be motivated to use external ROM 22 for “simplified and streamlined access.” Petition, 57. However, Takane’s correction parameters are already stored in circuits 56 and 58 and moving the correction parameters to an external ROM would **not** provide simplified and streamlined access for circuits 56 and 58. EX.2044, ¶366.

A POSA would understand that storing the parameters in tables in Takane’s ROM 22 would require more processing power, more memory space, increase costs, and be highly inefficient. EX.2044, ¶357. A POSA would not be motivated to make the proposed modifications. *Id.* Petitioner is applying hindsight bias using the claims of the ‘685 Patent as a roadmap. *Id.*

Laub testified that, for example, computation time would be considered by a POSA as a factor when designing a camera, “if there is a consideration for how quickly a finished result can be delivered.” EX.2020, 24:5-8. **A POSA reading Takane would understand that storing the correction parameters in the**

circuits 56/58 speeds up computation time. EX.2044, ¶358. A POSA reading Takane would not be motivated to slow down computation time. *Id.* Takane repeatedly refers to speed as a consideration. *See, e.g.,* EX.1009, [0012], [0014], [0015], [0016], [0017]; [0021], [0022], [0061], [0062].

To the extent Petitioner is suggesting to add additional correction parameters or additional correction algorithms to Takane based on the teachings of Watanabe, that is not clearly set forth in the petition. Even so, a POSA reading Takane would not be motivated to add additional correction parameters or additional correction algorithms for processing by the first distortion correction circuit 56, the alleged DSP. EX.2044, ¶¶367-368. Takane's first distortion correction circuit 56 purposefully uses fewer parameters and provides lower accuracy. *Id.*

3. Petitioner does not explain how Takane+Watanabe would work

Petitioner also does not clearly specify the alleged “database” and DBMS teachings of Watanabe that would be incorporated into Takane. For example, Petitioner does not explain how Watanabe's process information would be used with respect to Takane's correction parameters. EX.2044, ¶¶369-370.

Watanabe discloses a photographing program that appends the process information (lens type, focusing point, zoom position) to the image data and an image processing program that determines a table and then a correction value. *Id.*

Takane does not disclose separate imaging processing versus photographing programs, the transfer of process information, or the reference to tables for correction values. *Id.* Instead, Takane simply stores correction parameters in Takane's correction circuits 56/58. *Id.*

Petitioner does not explain how the alleged DBMS/database teachings of Watanabe would be incorporated into Takane's system or how Takane+Watanabe would work. Petitioner fails to meet its burden. *PersonalWeb Techs.*, 848 F.3d at 994.

4. Laub's deposition testimony contradicts Petitioner's allegations

In view of Laub's deposition testimony, the proposed combination of Takane+Watanabe is not supported and not explained. EX.2044, ¶381. Petitioner fails to show a rational basis for the proposed modification and Laub's deposition testimony directly contradicts the allegations in the petition. *Id.* Laub could not explain the proposed modification or the motivation for the proposed modification during deposition. *Id.* Both Petitioner and Laub fail to show that a POSA would have been motivated to make the combination as proposed. *Id.*

During deposition, Laub testified that he has "not proposed a modification" to Takane. EX.2020, 109:9-12. When questioned if Laub is relying on a modified system of Takane based on Watanabe's teachings of a database, Laub answered

“that is wrong”. EX.2020, 138:15-19. **This testimony directly contradicts the petition.** Petition, 57 (Takane+Watanabe “modifies Takane’s teachings”).

Laub appears to suggest that a POSA would use Watanabe’s teachings to “implement” – “not modify” – storing parameters in tables comprising a database. EX.2020, 111:4-12; EX.2020, 117:8-9 (“It’s not a modification; it is a – an implementation”). **However, Laub could not explain the proposed “implementation.”** EX.2044, ¶374.

Laub testified that Takane+Watanabe does not store the correction parameters in Takane’s ROM 22. EX.2020, 114:19-115:3. **This testimony directly contradicts Laub’s declaration.** EX.1003, ¶451. When asked if the parameters are not stored in Takane’s ROM 22, Laub acknowledged that was a contradiction of paragraph 293 of his declaration. EX.2020, 115:13-18.¹³

Laub refused to answer whether in Takane+Watanabe, the parameters “would” be stored in Takane’s ROM 22. EX.2020, 115:19-22, 116:1-118:9. **Laub fails to support that a POSA would be motivated to make the modification proposed in the petition.** EX.2044, ¶376.

¹³ PO notes that paragraph 293 of Laub’s declaration on the ‘805 Patent is the same as paragraph 451 of Laub’s declaration on the ‘685 Patent.

Laub confirmed it is not his opinion that a POSA would modify Takane to store correction parameters in Takane's ROM 22 instead of the circuits themselves. EX.2020, 109:4-8, 110:6-112:3. Laub testified that Takane+Watanabe does not store the correction parameters in Takane's ROM 22 in addition to storing those parameters in Takane's circuits 56/58. EX.2020, 114:4-9. **Again, Laub could not explain the proposed "implementation".** EX.2044, ¶377.

Laub's inconsistent testimony fails to support Petitioner's reliance on Takane+Watanabe. EX.2044, ¶378.

Laub testified that Watanabe's database "is something that *could* be used by a POSITA as a way to implement Takane." EX.2020, 118:5-7 (emphasis added). However, Laub did not opine that a POSA "would" have done so. EX.2020, 117:1-118:9. **Laub fails to support that a POSA would be motivated to make the modification proposed in the petition.** EX.2044, ¶380.

B. CLAIM 1

1. Claim 1[a]

a. "integrated circuit"

Petitioner does not clearly identify the component(s) of Takane that allegedly correspond to the claimed integrated circuit. Petition at 59. It is not clear if Petitioner is relying on Takane's main controlling section 24 implemented as a one-chip LSI or Takane's image processing circuit 46. EX.2044, ¶¶384-385.

a. “digital signal processor” (DSP)

Petitioner fails to establish that Takane’s circuit 56 corresponds to the claimed DSP.

Throughout the analysis of claim 1, it is clear that Petitioner is relying on Takane’s first distortion correction circuit 56 as allegedly corresponding to the claimed DSP. Petition, 60 (analyzing 1[a]), 61 (analyzing 1[c] and 1[d]), 63 (analyzing 1[f]). Laub confirmed in deposition that he is relying on Takane’s first distortion correction circuit 56 as corresponding to the claimed DSP. EX.2020, 127:11-20.

A POSA would understand that Takane’s circuit 56 is a hardware component. EX.2044, ¶387. Interpreting a circuit to be a functional block contradicts the common understanding of a POSA of the word “circuit” which refers to hardware. *Id.*

Laub agreed that a DSP “generally was well-known.” EX.2020, 27:7-15. Laub admitted that “the specification of the patent presumes that a person reading that patent would understand what is referred to when the phrase ‘digital signal processor’ is used.” EX.2020, 28:17-29:10. However, Laub opined that any of Takane’s circuits that process digital signals could be regarded as DSPs. EX.1003,

¶473.¹⁴ **This is not correct.** DSP is a term of art and refers to a specific type of hardware. EX.2044, ¶388. The claims recite DSP hardware with specific functionality. *Id.*

Petitioner fails to establish that Takane’s circuit 56 corresponds to a DSP as claimed. EX.2044, ¶389. For example, Petitioner fails to show that Takane’s circuit 56 has flexible programming or uses software as opposed to fixed functionality hard-coded into the circuit itself. *Id.* As discussed above, Petitioner, Laub, and EX.2019 (“Ralston”) distinguish a DSP from an ASIC based on the flexible programming of a DSP. EX.2044, ¶¶390-391; EX.2017, ¶¶157, 319; EX.2020, 52:15-53:11; EX.2019, 7:65-8:16. Neither Petitioner nor Laub addressed whether Takane’s circuit 56 is capable of being flexibly programmed. EX.2044, ¶392. In view of a POSA’s knowledge of a DSP, Petitioner fails to show that Takane’s circuit 56 corresponds to the claimed DSP. *Id.*

Indeed, Takane expressly discloses that for the circuit 56, “[t]he correction accuracy is intentionally lowered, and the processing time can be shortened and the ***circuit structure*** of the first distortion correction circuit 56 can be made ***simple***.” EX.1009, [0061] (emphasis added). For at least this additional reason, Petitioner

¹⁴ Laub testified that “anything that processes a signal in a digital manner” is a DSP. EX.2020, 27:16-28:12, 56:14-15.

fails to show that Takane's circuit 56 corresponds to the claimed DSP. EX.2044, ¶393.

b. "database management system" (DBMS)

Petitioner relies on Watanabe's DBMS teachings in Takane+Watanabe. Petition, 60-61. PO incorporates the discussion of claim 1[a] and the alleged DBMS in Watanabe in Ground 1 herein. *See infra*, section III.B.1.

PO disagrees with Petitioner's allegations regarding Takane+Watanabe for at least the reasons discussed above regarding the proposed combination of Takane+Watanabe. EX.2044, ¶398. Takane expressly discloses that the correction parameters are stored in advance in Takane's circuit 56. EX.1009, [0054]. As such, a POSA would not be motivated to combine Takane and Watanabe as proposed. The proposed modification would change Takane's principle of operation. Petitioner also fails to explain how Takane+Watanabe would work.

2. Claim 1[d]

Petitioner relies on Watanabe's database teachings in Takane+Watanabe. PO incorporates the discussion of claim 1[d] and the alleged database in Watanabe in Ground 1 herein. *See infra*, section III.B.2.

For the same reasons discussed above, PO also disputes that there were only two known alternatives for storing algorithms. EX.2044, ¶¶401-405. Takane's

correction parameters (the coefficients of the polynomial) are used in a hard-coded algorithm in the circuit. *Id.* As discussed above, Takane teaches away from storing corrections in a separate table (EX.1009 at [0007]-[0008]) and instead discloses storing the correction parameters in the correction circuits. *Id.*

Both proposed alternatives rely on modifications to Takane. *Id.* There is no suggestion in Takane that circuit 56 includes software comprising executable code. *Id.* And Takane expressly discloses that the correction parameters are stored in advance in the circuit 56. *Id.*

C. CLAIM 6

PO incorporates the above discussion of claim 1 herein. *See infra*, section X.B.

D. CLAIM 10

For claim 6, from which claim 10 depends, Petitioner relies on Takane's circuit 56 as the alleged DSP. Petition, 64. Petitioner fails to establish that Takane's circuit 56 performs white balance adjustment as alleged. EX.2044, ¶¶408-410.

For claim 10, Petitioner relies on Takane's signal processing circuit 50 as the alleged DSP. EX.1003, ¶528. Petitioner's analysis is inconsistent.

E. CLAIM 14

PO incorporates the above discussion of claim 1 herein. *See infra*, section X.B.

For at least the reasons discussed above, a POSA would not be motivated to modify Takane to “forward” an algorithm to circuit 56 as alleged because the correction parameters are stored in circuit 56. EX.1003, ¶412. Petitioner fails to establish a POSA would be motivated to modify Takane as proposed.

F. CLAIM 18

PO incorporates the above discussion of claim 10 herein. *See infra*, section X.D.

G. CLAIMS 27, 28, 30

Petitioner fails to establish that Takane’s distortion correction is implemented using software. EX.2044, ¶¶415-417.

XI. SECONDARY CONSIDERATIONS OF NON-OBVIOUSNESS**A. LONG-FELT NEED**

Laub admits the well-known problems related to optical aberrations and the competing considerations in camera design to try to solve those problems. EX.2044, ¶418; EX.1003, ¶¶75, 78, 113, 116.

Historically, aberration correction was done on an external computer as discussed above regarding Adobe Photoshop and/or Russ. EX.2044, ¶419. However, this requires significant time, cost, and expertise as discussed above. *Id.* Additionally, conventional cameras stored and transferred compressed images (JPEG) which are inherently degraded in terms of image quality when compared to RAW images, which means the post-production editing was performed on an already degraded compressed image. *Id.*

Conventional wisdom taught against adding significant hardware needed to perform the processing as described in the claims due to limitations of size, weight, power, cost, and mobility and a POSA would not think to arrive at the claimed technology because aberration correction was conventionally done on an external computer. EX.2044, ¶420.

A POSA would have understood the long-felt need for improved image quality by way of aberration correction, but there were significant engineering challenges in achieving in-camera aberration correction as claimed in the '685 Patent. EX.2044, ¶421. The claimed technology solves this long-felt need and does so by efficiently balancing competing considerations of size, weight, power, cost, and mobility in the camera itself. *Id.* The claimed technology recites hardware and software that provides in-camera aberration correction capabilities and uniquely balances limited space, power consumption, and expense of a desirable digital

camera. *Id.* By efficiently performing in-camera aberration correction within the image processing pipeline within the camera, the result is far improved image quality, even when compared to post-production editing. *Id.* The claimed technology enables in-camera aberration correction with the use of multiple different lenses with multiple different camera systems. *Id.* This is extremely beneficial in solving the known problems facing many photographers, engineers, and camera manufacturers. *Id.*

Further, using a DBMS/database as claimed in a compact self-contained device, such as a digital camera, is by itself unconventional because without the express teachings of the '685 Patent, the POSA would not look to implement the features of a DBMS in such a device. EX.2044, ¶422. Furthermore, the ability to organize/manage/update a database allows continued efficient organization/management of data as new and/or updated data is introduced. *Id.*

It is unconventional for a POSA to consider access to a DBMS within the image processing pipeline of a compact self-contained device. EX.2044, ¶423. A POSA would conventionally take all efforts to make this processing portion of the device as efficient as possible and adding a DBMS would initially be thought of as unnecessary overhead. *Id.* The teachings of the '685 Patent enable a POSA to understand that the correction data can be retrieved from and updated within an

organized database and processed efficiently within the image processing pipeline.

Id.

The long-felt need for the claimed technology is evidence of non-obviousness. EX.2044, ¶424.

B. CANON LITIGATION

In prior litigation, Canon Inc. (“Canon”) was accused of infringing related Patent Nos. 7,612,805 (“’805 Patent”) and 8,451,339 (“’339 Patent”). Canon filed IPRs against the ‘805 and ‘339 Patents and also filed a declaratory judgment action against the ‘685 Patent and related Patent No. 10,877,266 (“’266 Patent”). EX.2044, ¶¶425-427.

Among the various accused infringing products, the Canon EOS Rebel T6s was a very popular Canon product. EX.2044, ¶¶429, 431. Reviews of this product touted the advanced capabilities including the in-camera aberration correction features. *Id.*; EXS.2022-2025.

PO’s expert performed an analysis of exemplary claim 1 of the ‘685 Patent and the Canon EOS Rebel T6s, based on public information; and opined that the Canon EOS Rebel T6s incorporated the claimed technology. EX.2044, ¶¶430, 432, 433; EXS.2026-2036.

PO's expert also found that Canon consistently held approx. 45-48% market share of the digital camera industry from 2019-2024. EX.2044, ¶434; EXS.2037-2042.

After nearly two years of litigation between PO and Canon,

EX.2044, ¶435; EX.2043.

In view of Canon's market share, litigation investigation and investment, and represents further evidence of non-obviousness.

XII. CONCLUSION

For at least the reasons set forth herein, PO respectfully requests that the challenged claims be confirmed patentable.

Respectfully submitted,

Date: February 26, 2025

By: /s/ Thomas M. Dunham

Thomas M. Dunham

Reg. No. 39,965

Cherian LLP

1901 L Street NW, Suite 700

Washington, D.C. 20036

(202) 838-1567

ATTORNEY FOR PATENT OWNER,
OPTIMUM IMAGING TECHNOLOGIES
LLC

CERTIFICATE OF COMPLIANCE

This Patent Owner Response (“POR”) consists of 13,971 words, which is no more than 14,000 words, excluding table of contents, table of authorities, certificate of service, this certificate, or table of exhibits. The POR complies with the type-volume as mandated in 37 C.F.R. § 42.24. In preparing this certificate, counsel has relied on the word count of the word-processing system used to prepare the paper (Microsoft Word).

Respectfully submitted,

Date: February 26, 2025

By: /s/ Thomas M. Dunham

Thomas M. Dunham

Reg. No. 39,965

Cherian LLP

1901 L Street NW, Suite 700

Washington, D.C. 20036

(202) 838-1567

ATTORNEY FOR PATENT OWNER,
OPTIMUM IMAGING TECHNOLOGIES
LLC

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), the undersigned hereby certifies the PATENT OWNER RESPONSE and all exhibits thereto were served on the undersigned date via email, as authorized by Petitioner, at the following email addresses:

SMcKeown-PTAB@WolfGreenfield.com

AWichman-PTAB@WolfGreenfield.com

RPritzker-PTAB@WolfGreenfield.com

Respectfully submitted,

Date: February 26, 2025

By: /s/ Thomas M. Dunham

Thomas M. Dunham

Reg. No. 39,965

Cherian LLP

1901 L Street NW, Suite 700

Washington, D.C. 20036

(202) 838-1567

ATTORNEY FOR PATENT OWNER,
OPTIMUM IMAGING TECHNOLOGIES
LLC