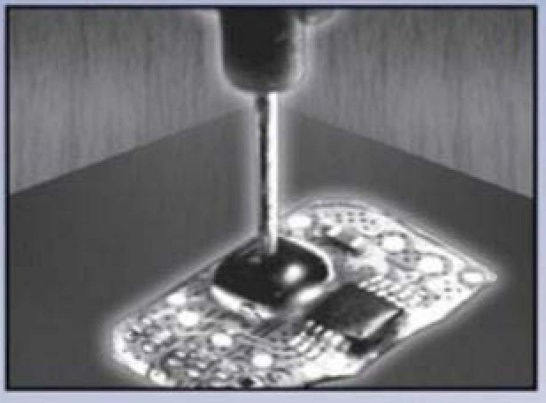
Encapsulation Technologies for Electronic Applications



Haleh Ardebili
Michael G.Pecht

Materials and Processes for Electronic Applications Series

Petitioner Samsung Ex-1055, 0001

MATERIALS AND PROCESSES FOR ELECTRONIC APPLICATIONS

Series Editor: James J. Licari
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William Andrew is an imprint of Elsevier
Linacre House, Jordan Hill, Oxford OX2 8DP, UK
30 Corporate Drive, Suite 400, Burlington, MA 01803, USA

First edition 2009

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British Library Cataloguing in Publication Data
A catalogue record for this book is available from the British Library

Library of Congress Cataloging-in-Publication Data
A catalog record for this book is available from the Library of Congress

ISBN: 978-0-8155-1576-0

For information on all William Andrew publications
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Printed and bound in United States of America

09 10 11 12 11 10 9 8 7 6 5 4 3 2 1

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Dedicated to my parents and my family, especially to my son, Arvin, and my husband, Pradeep.

Haleh Ardebili

Dedicated to my parents, my family, my students, my friends and my colleagues.

Michael G. Pecht

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Preface

The use of electronics has become intimately intertwined with human lives. From laptops and mobile phones to medical instruments and aircraft control units, electronic devices are used in most products today and in increasingly varying environments. The dominant trend is toward smaller, lighter, and faster electronic devices. Electronic packaging and plastic encapsulation play a significant role in this trend. With advances in electronic packaging including three-dimensional packaging (or die-stacking), wafer-level packaging, environmentally friendly or "green" encapsulant materials, and extreme high- and low-temperature electronics, a book on encapsulation technologies used in electronic applications has become essential.

This book describes the fundamentals of plastic encapsulation, discusses advances in encapsulation materials and technologies, and explores the intersection of emerging technologies such as nanotechnology and biotechnology with encapsulant materials. The main emphasis of this book is on the encapsulation of microelectronics; however, the encapsulation of connectors and transformers is also addressed.

The book is organized into eight chapters. Chapter 1 presents an overview of electronic packaging and encapsulation. Various types of plastic-encapsulated microelectronics including 2D and 3D packages are discussed. Chapter 2 is devoted to plastic encapsulant materials, which are categorized according to encapsulation technology. A separate section is devoted to environmentally friendly or "green" encapsulant materials. Chapter 3 is focused on encapsulation process technologies including molding, glob-topping, potting, underfilling, and printing encapsulation. In this chapter, the encapsulation of wafer-level and 3D packages is also discussed. Chapter 4 discusses the characterization of encapsulant properties including manufacturing, hygro-thermo-mechanical, electrical, and thermal properties. Chapter 5 describes encapsulation defects and failures, while Chapter 6 presents defect and failure analysis techniques including both non-destructive and destructive tests. Chapter 7 is focused on qualification and quality assurance of encapsulated microelectronics. Both virtual and product qualification processes are discussed and accelerated tests and industry practices are presented.

Petitioner Samsung Ex-1055, 0006

The final chapter, Chapter 8, explores trends in and challenges for electronics, packaging, and plastic encapsulation. Moore's law and "More than Moore" are presented. Evolution from integrated circuits to system-in-package and system-on-package is discussed. Extreme high- and low-temperature electronics are described. Furthermore, plastic encapsulation associated with microelectromechanical systems, nano-electronics and nanotechnology, bioelectronics and biosensors, and organic light emitting diodes and photovoltaics is discussed.

This book is most suitable for the professional engineer and material scientist interested in electronic packaging and plastic encapsulation. Entrepreneurs in the electronics industry can also benefit from this book. Additionally, this book can be used as a textbook in an elective course for senior undergraduates or first-year graduate students with a background in material science or electronics.

Acknowledgments

Many people have supported and contributed to this book. We would like to acknowledge the contributions of the following people: Luu T. Nguyen, Edward B. Hakim, Rakesh Agarwal, Ajay Arora, Vikram Chandra, Lloyd W. Condra, Abhijit Dasgupta, Gerard Durback, Rathindra N. Ghoshtagore, Qazi Ilyas, Lawrence W. Kessler, Pradeep Lall, Junhui Li, Anupam Malhotra, Steven R. Martell, Tsutomu Nishioka, Thomas E. Paquette, Ashok S. Prabhu, Dan Quearry, Janet E. Semmens, and Jack Stein. Also, we like to acknowledge the studies published in IEEE, ASME, and other journals that have become invaluable references for the discussions in this book.

We like to especially thank Dr. James J. Licari for his insightful and constructive review comments and suggestions throughout the development and writing of this book. We also would like to thank William Andrew Publishing (acquired by Elsevier). In particular we acknowledge the positive and consistent support of Martin Scrivener and Millicent Treloar. Furthermore, we would like to thank Elsevier (U.S.A.) and Exeter Premedia Services (India) for providing a smooth and positive transition during the publication process. We would like to thank the University of Houston's Department of Mechanical Engineering faculty, staff, and students, and in particular the department chair, Professor Matthew Franchek, for their support and encouragement. We would like to thank the members, faculty, staff, and students at CALCE, University of Maryland, College Park, for their contributions to research and education

Petitioner Samsung Ex-1055, 0007

in the field of electronic packaging, which has benefited this book. Finally, we like to thank our family and friends for their support during this time-intensive endeavor.

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March 2009

Petitioner Samsung Ex-1055, 0008

Table of Contents

Preface

1 Introduction
- 1.1 Historical Overview
- 1.2 Electronic Packaging
- 1.3 Encapsulated Microelectronic Packages
  - 1.3.1 2D Packages
- 1.4 Hermetic Packages
  - 1.4.1 Metal Packages
  - 1.4.2 Ceramic Packages
- 1.5 Encapsulants
  - 1.5.1 Plastic Molding Compounds
  - 1.5.2 Other Plastic Encapsulation Methods
- 1.6 Plastic versus Hermetic Packages
  - 1.6.1 Size and Weight
  - 1.6.2 Performance
  - 1.6.3 Cost
  - 1.6.4 Hermeticity
  - 1.6.5 Reliability
  - 1.6.6 Availability
- 1.7 Summary

References

2 Plastic Encapsulant Materials
- 2.1 Chemistry Overview
  - 2.1.1 Epoxies
  - 2.1.2 Silicones
  - 2.1.3 Polyurethanes
  - 2.1.4 Phenolics
- 2.2 Molding Compounds
  - 2.2.1 Resins
  - 2.2.2 Curing Agents or Hardeners
  - 2.2.3 Accelerators
  - 2.2.4 Fillers
  - 2.2.5 Coupling Agents
  - 2.2.6 Stress-Relief Additives
  - 2.2.7 Flame Retardants

2.2.8 Mold-Release Agents
2.2.9 Ion-Trapping Agents
2.2.10 Coloring Agents
2.2.11 Market Conditions and Manufacturers of Encapsulant Materials
2.2.12 Material Properties of Commercially Available Molding Compounds
2.2.13 Materials Development
2.3 Glob-Top Encapsulants
2.4 Potting and Casting Encapsulants
2.4.1 Dow Corning Materials
2.4.2 General Electric Materials
2.5 Underfill Encapsulants
2.6 Printing Encapsulants
2.7 Environmentally Friendly or “Green” Encapsulants
2.7.1 Toxic Flame Retardants
2.7.2 Green Encapsulant Material Development
2.8 Summary
References

3 Encapsulation Process Technology
3.1 Molding Technology
3.1.1 Transfer Molding
3.1.2 Injection Molding
3.1.3 Reaction-Injection Molding
3.1.4 Compression Molding
3.1.5 Comparison of Molding Processes
3.2 Glob-Topping Technology
3.3 Potting and Casting Technology
3.3.1 One-Part Encapsulants
3.3.2 Two-Part Encapsulants
3.4 Underfilling Technology 154
3.4.1 Conventional Flow Underfill
3.4.2 No-flow Underfill
3.5 Printing Encapsulation Technology
3.6 Encapsulation of 2D Wafer-Level Packages
3.7 Encapsulation of 3D Packages
3.8 Cleaning and Surface Preparation
3.8.1 Plasma Cleaning

3.8.2 Deflashing
3.9 Summary
References

4 Characterization of Encapsulant Properties
4.1 Manufacturing Properties
4.1.1 Spiral Flow Length
4.1.2 Gelation Time
4.1.3 Bleed and Flash
4.1.4 Rheological Compatibility
4.1.5 Polymerization Rate
4.1.6 Curing Time and Temperature
4.1.7 Hot Hardness
4.1.8 Post-cure Time and Temperature
4.2 Hygro-thermomechanical Properties
4.2.1 Coefficient of Thermal Expansion and Glass Transition Temperature
4.2.2 Thermal Conductivity
4.2.3 Flexural Strength and Modulus
4.2.4 Tensile Strength, Elastic and Shear Modulus, and %Elongation
4.2.5 Adhesion Strength
4.2.6 Moisture Content and Diffusion Coefficient
4.2.7 Coefficient of Hygroscopic Expansion
4.2.8 Gas Permeability
4.2.9 Outgassing
4.3 Electrical Properties
4.4 Chemical Properties
4.4.1 Ionic Impurity (Contamination Level)
4.4.2 Ion Diffusion Coefficient
4.4.3 Flammability and Oxygen Index
4.5 Summary
References

5 Encapsulation Defects and Failures
5.1 Overview of Package Defects and Failures
5.1.1 Package Defects
5.1.2 Package Failures
5.1.3 Classification of Failure Mechanisms

5.1.4 Contributing Factors
5.2 Encapsulation Defects
5.2.1 Wire Sweep
5.2.2 Paddle Shift
5.2.3 Warpage
5.2.4 Die Cracking
5.2.5 Delamination
5.2.6 Voids
5.2.7 Non-uniform Encapsulation
5.2.8 Flash
5.2.9 Foreign Particles
5.2.10 Incomplete Cure
5.3 Encapsulation Failures
5.3.1 Delamination
5.3.2 Vapor-Induced Cracking (Popcorning)
5.3.3 Brittle Fracture
5.3.4 Ductile Fracture
5.3.5 Fatigue Fracture
5.4 Failure Accelerators
5.4.1 Moisture
5.4.2 Temperature
5.4.3 Exposure to Contaminants and Solvents
5.4.4 Residual Stresses
5.4.5 General Environmental Stress
5.4.6 Manufacturing and Assembly Loads
5.4.7 Combined Load–Stress Conditions
5.5 Summary
References

6 Defect and Failure Analysis Techniques for Encapsulated Microelectronics
6.1 General Defect and Failure Analysis Procedures
6.1.1 Electrical Testing
6.1.2 Non-destructive Evaluation
6.1.3 Destructive Evaluation
6.2 Optical Microscopy
6.3 Scanning Acoustic Microscopy
6.3.1 Imaging Modes
6.3.2 C-Mode Scanning Acoustic Microscope

6.3.3 Scanning Laser Acoustic Microscope
6.3.4 Case Studies
6.4 X-ray Microscopy
6.4.1 X-ray Generation and Absorption
6.4.2 X-ray Contact Microscope
6.4.3 X-ray Projection Microscope
6.4.4 High-Resolution Scanning X-ray Diffraction Microscope
6.4.5 Case Study: Encapsulation in Plastic-Encapsulated Devices
6.5 X-ray Fluorescence Spectroscopy
6.6 Electron Microscopy
6.6.1 Electron–Specimen Interaction
6.6.2 Scanning Electron Microscopy
6.6.3 Environmental Scanning Electron Microscopy (ESEM)
6.6.4 Transmission Electron Microscopy
6.7 Atomic Force Microscopy
6.8 Infrared Microscopy
6.9 Selection of Failure Analysis Techniques
6.10 Summary
References

7 Qualification and Quality Assurance
7.1 A Brief History of Qualification and Reliability Assessment
7.2 Qualification Process Overview
7.3 Virtual Qualification
7.3.1 Life-Cycle Loads
7.3.2 Product Characteristics
7.3.3 Application Requirements
7.3.4 Reliability Prediction using PoF Approach
7.3.5 Failure Modes, Mechanisms, and Effects Analysis (FMMEA)
7.4 Product Qualification
7.4.1 Strength Limits and Highly Accelerated Life Test
7.4.2 Qualification Requirements
7.4.3 Qualification Test Planning
7.4.4 Modeling and Validation
7.4.5 Accelerated Testing
7.4.6 Reliability Assessment

7.5 Qualification Accelerated Tests
7.5.1 Steady-State Temperature Test
7.5.2 Thermal Cycling Test
7.5.3 Tests That Include Humidity
7.5.4 Solvent Resistance Test
7.5.5 Salt Atmosphere Test
7.5.6 Flammability and Oxygen Index Test
7.5.7 Solderability
7.5.8 Radiation Hardness
7.6 Industry Practices
7.7 Quality Assurance
7.7.1 Screening Overview
7.7.2 Stress Screening and Burn-In
7.7.3 Screen Selection
7.7.4 Root-Cause Analysis
7.7.5 Economy of Screening
7.7.6 Statistical Process Control
7.8 Summary
References

8 Trends and Challenges
8.1 Microelectronic Device Structure and Packaging
8.2 Extreme High- and Low-Temperature Electronics
8.2.1 High Temperatures
8.2.2 Low Temperatures
8.3 Emerging Technologies
8.3.1 Microelectromechanical Systems
8.3.2 Bioelectronics, Biosensors, and Bio-MEMS
8.3.3 Nanotechnology and Nanoelectronics
8.3.4 Organic Light-Emitting Diodes, Photovoltaics, and Optoelectronics
8.4 Summary
References

Index

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1 Introduction

Electronics are used in a wide range of applications including computing, communications, biomedical, automotive, military, and aerospace. They must operate in varying temperature and humidity environments ranging from indoor controlled conditions to outdoor climate changes. Exposure to moisture, ionic contaminants, heat, radiation, and mechanical stresses can be highly detrimental to electronic devices and may lead to device failures. Therefore, it is essential that the electronic devices be packaged for protection from their intended environment, as well as to provide handling, assembly, and electrical and thermal considerations.

Electronic packaging may involve either hermetic (ceramic or metallic) packaging or non-hermetic (plastic) encapsulation. Currently, more than 99% of microelectronic devices are plastic encapsulated. Improvements in encapsulant materials and cost incentives have stretched the application boundaries for plastic electronic packages. Many electronic applications that traditionally used hermetic packages such as military are now using commercial off-the-shelf (COTS) plastic packages. Plastic encapsulation has the advantages of low cost, availability, and manufacturability.

Much of the focus is aimed at the research and development of new and improved encapsulants. With recent trends in environmental awareness, new environmentally friendly or "green" encapsulant materials (i.e., without brominated additives) have emerged. Plastic packages are also being considered for use in extreme high and low temperature electronics. 3D packaging and wafer-level packaging require unique encapsulation techniques. Encapsulants also play a role in emerging technologies. Modified existing or newly developed encapsulant materials are being developed for microelectromechanical systems (MEMS), bio-MEMS, bioelectronics, nanoelectronics, solar modules, and organic light-emitting diodes. Nanocomposite encapsulants with improved material properties are also being explored.

In this chapter, a historical overview of encapsulation is provided. Electronic packaging including package levels, encapsulated microelectronic devices, hermetic packages, and encapsulation methods and materials are discussed. Microelectronic packages including both 2D and 3D packages are described. Finally, a comparison of hermetic versus plastic packages is presented.

Petitioner Samsung Ex-1055, 0016

1.1 Historical Overview

Electronic devices have been packaged in a variety of ways. Among the first package types was a preformed package made of Kovar (an alloy of nickel, cobalt, manganese, and iron). Kovar, a trade name of Westinghouse Electric and Manufacturing Company, and invented by Howard Scott in 1936 [1], has the advantage of a coefficient of thermal expansion (CTE) similar to that of glass. It is a suitable choice for sealing to glass because of lower CTE mismatch stresses.

One of the early transistor packages is shown in Fig. 1.1 [2]. In this package, the emitter, collector, and base connector leads were inserted

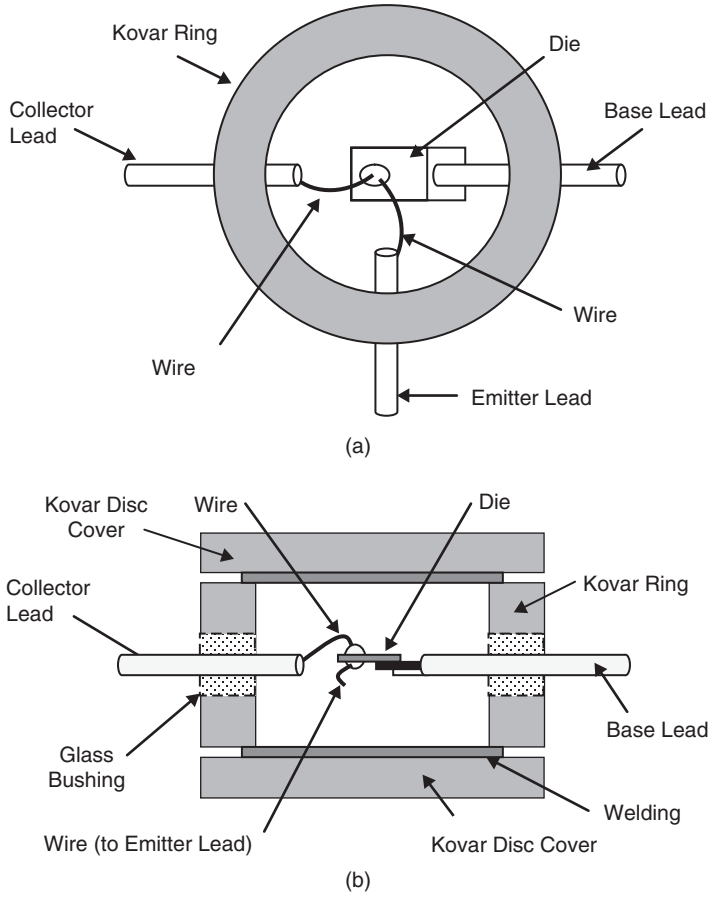


Figure 1.1 Kovar transistor package: (a) top view; (b) side view [2].

Petitioner Samsung Ex-1055, 0017

through a glass bushing positioned in a Kovar ring or cylindrical housing. The bushing was made of a suitable electrical insulating and moisture impervious (hermetic) glass material. The transistor device was then bonded to the base lead and interconnected to the emitter and collector leads using wires. The Kovar disc covers were later hermetically sealed by welding. Ceramic packages, similar in construction to the Kovar casing, appeared later as less expensive alternatives.

The first plastic-encapsulated packages appeared on the market in the early 1950s. By the early 1960s, plastic encapsulation emerged as an inexpensive, simple alternative to both ceramic and metal encasings, and during the 1970s, virtually all high-volume integrated circuits (ICs) were encapsulated in plastic. By 1993, plastic-encapsulated microelectronics accounted for over 97% of the worldwide microcircuit production.

Most early microelectronic devices were compression molded where the molding compound is heated and compressed inside the mold. Potting soon emerged as a suitable alternative. Potting involved positioning the electrical circuit in a container and pouring the liquid encapsulant into the cavity. Figure 1.2 shows a typical transistor encapsulated using the "can and header" method [3]. The transistor chip was soldered to a carrier which was then attached to the header assembly. The header assembly consisted of three parallel conductive lead-posts sealed into a button-like header made of pre-molded plastic encapsulant material such as a phenolic. The header served as a support for maintaining the relative positioning of the

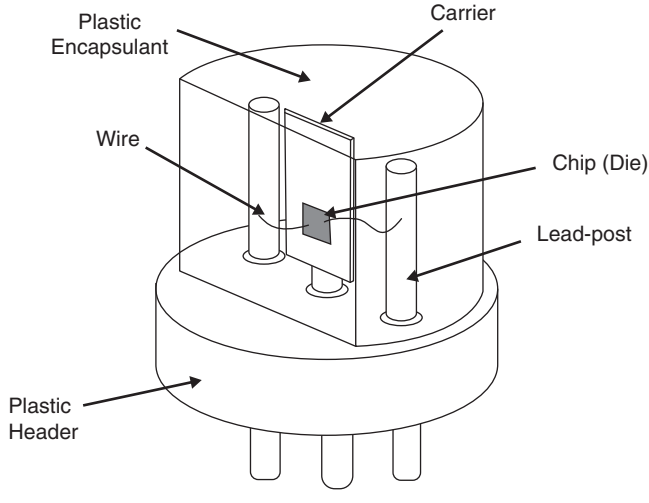


Figure 1.2 "Can and header" transistor package [3].

Petitioner Samsung Ex-1055, 0018

three posts. The microelectronic chip was electrically connected to the side lead posts via wire bonding. The assembly of lead-posts and carrier was then encapsulated with commercially available plastic encapsulant materials such as Dow Chemical Company's epoxy encapsulants.

Transfer molding gained worldwide acceptance as an economical method best suited for mass production. In transfer molding, the microelectronic chips are loaded into a multi-cavity mold and constrained, and the encapsulant is transferred from a reservoir into the cavity under heat and pressure. The encapsulant, typically a thermosetting polymer, is cured in the cavity to form the final electronic package. In transfer molding, unlike compression molding, no additional pressure is applied during heating and curing of the encapsulant. Furthermore, the closed mold design in transfer molding allows for more intricate chips to be encapsulated with better tolerances compared to compression molding.

Figure 1.3 shows one of the first molds used for transfer molding of a transistor device [4]. The metal lead-posts were gripped and firmly held in proper position as the multi-part lower portion of the mold was clamped together. The leads were bent and flattened on top, and the semiconductor device was placed on one flattened lead and wire bonded to the other two leads. A thin mask was placed on top with a disc-shaped exposed area, and the chip and the leads were passivated with metallic oxide such as alumina. The mask was removed and the upper portion of the mold was

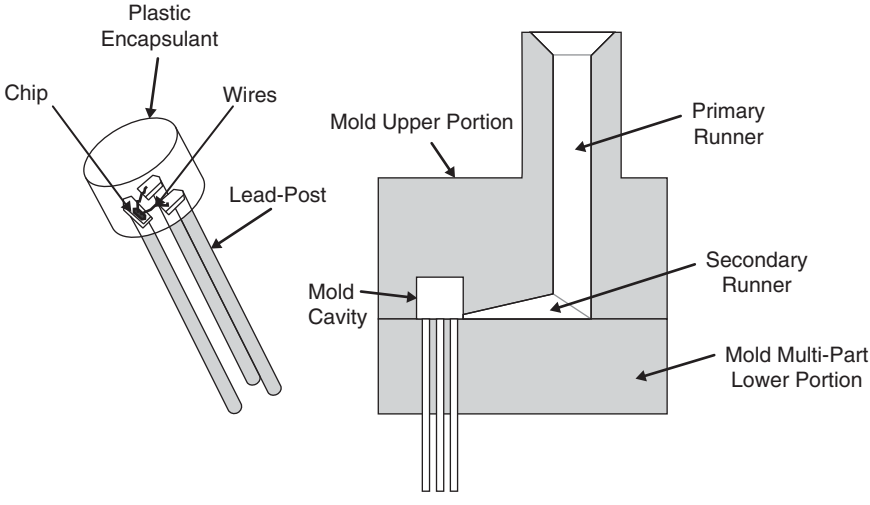


Figure 1.3 Transfer molding of a semiconductor chip [4].

Petitioner Samsung Ex-1055, 0019

then pressed on the lower portion. Powdered plastic or preforms were introduced through the cylindrical runner and became molten due to the high temperature of the upper mold portion. A piston was then pressed into the runner transferring the molten plastic through the gate into the cavity above the semiconductor device assembly. The plastic cured and solidified in the cavity. The mold opened to release the plastic molded parts. One of the disadvantages of this method was that the thin wire bonds were frequently damaged due to the high pressure and velocities of the encapsulant.

A novel approach to the problem of wire damage during transfer molding was to use a bottom-side gated process, in which the molding compound entered the cavity from the side opposite to the bond wires and in a motion path parallel to the wires (Fig. 1.4), thereby reducing the chances of breaking the delicate wires.

Although epoxy novolac was the first material used for plastic encapsulation, phenolics and silicones were the dominant plastics of the 1960s. At that time, plastic packages were plagued by numerous reliability problems due largely to the poor quality of the encapsulation system. Moisture-induced failure mechanisms, such as corrosion, cracking, and interfacial delamination, were significant. At that time, plastic packages encountered formidable challenges in gaining acceptance for use in government and military applications. While plastic packaging offered an economically viable alternative, the military continued using metal and ceramic packages due to higher reliability, ruggedness, and traceability.

Over the years, with improvements in encapsulant materials, die passivation, metallization technology, and assembly automation, plastics have

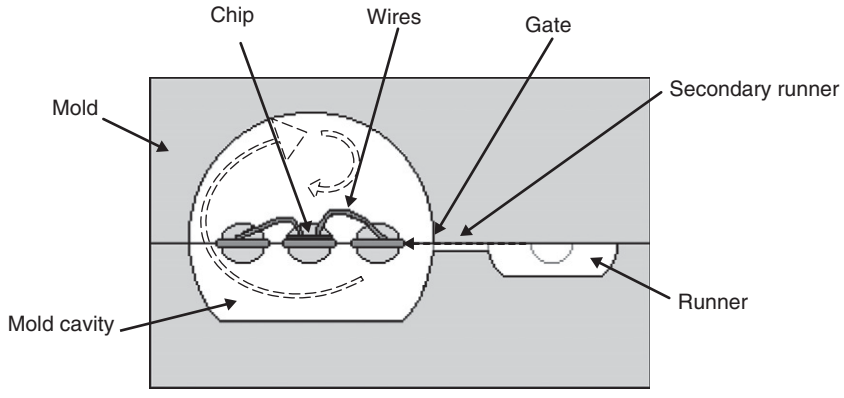


Figure 1.4 Transfer molding with bottom-side gating [5].

Petitioner Samsung Ex-1055, 0020

dominated the electronic packaging industry. The reliability of plastic packages was no longer considered a stumbling block to their widespread application. In 1994, after the so-called "Perry Memo" (named after then Defense Secretary William Perry), the US military officially started the wider use of plastic-encapsulated electronic packages. The main driving force for this transition was cost. A hermetically packaged ceramic IC can cost up to ten times more than a plastic-packaged IC—if a suitable one is even available on the market at all. Not surprisingly, COTS technology plastic packages are now widely used in aerospace and military applications [6,7].

In the 2000s, with major advantages in cost, size, weight, performance, and availability, plastic packages attracted more than 99% of the market share of worldwide microcircuit sales. Ceramic packages are used only in harsh military applications and specialized low-volume, high-performance systems. Much of the electronics packaging research performed today involves developing new smaller, lighter, cheaper, and more reliable plastic packages. Plastic-encapsulated microcircuits will continue to account for the vast share of the ICs market in coming years, but hermetic packages, with their special characteristics, will continue to have a unique market in the electronics industry.

Over the decades numerous formulations of epoxies have been developed with lower curing shrinkages and contamination levels. Since the early 1970s, epoxies have taken over as the main encapsulating material. Although silicones are still sometimes used, in the 2000s the typical encapsulant is an epoxy resin matrix with a complex mixture of cross linkers, accelerators, flame retardants, fillers, coupling agents, mold-release agents, and flexibilizers.

Plastic packages can be pre-molded or post-molded. In the pre-molding process, a package base is prepared from a pre-molded plastic (or sometimes a metal substrate). The chip is then placed on the base and connected to an I/O fan out pattern with wire. A pre-molded plastic lid or housing is attached on top, using an epoxy adhesive to protect the die and wire bonds, and forms a cavity inside the package. Figure 1.5 shows a pre-molded package [8,9]. Pre-molded packages are most often used for high-pin-count devices or pin-grid arrays that are not amenable to flat lead-frames and simple fan out patterns.

In the post-molded package, the die is first attached to a lead-frame and connected to an I/O fan out pattern with wire, which is then loaded into a multi-cavity molding tool and encapsulated in a thermoset molding compound via the transfer molding process. Post-molded packages are less expensive than pre-molded ones because there are fewer parts

Petitioner Samsung Ex-1055, 0021

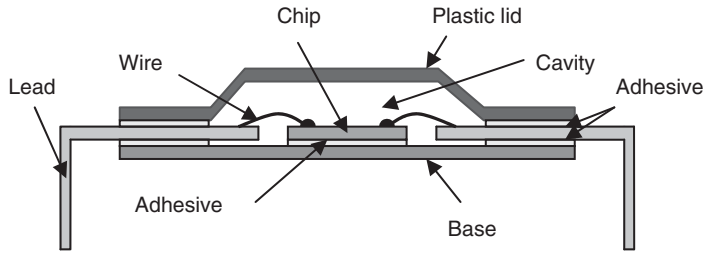


Figure 1.5 A pre-molded plastic package [9].

and assembly steps. About 90% of plastic packages are made using post-molding techniques.

1.2 Electronic Packaging

The main objectives of electronic packaging are (a) the protection of the IC chip (or die) and (b) the interconnection of IC chips to other electronic components (i.e., IC chips, printed circuit boards (PCBs), transformers, and connectors) for transfer of electrical signals. An electronic package may be designed to

- reduce or remove heat that is either generated internally during device operation or due to the external environment;
- provide resistance to humidity and moisture;
- provide resistance to ionic contaminants;
- protect from radiation;
- reduce thermo-mechanical stresses; and
- provide mechanical support.

Electronic packaging generally begins at the chip or wafer level. Figure 1.6 shows a flowchart of a conventional plastic packaging of an IC chip. The passivated silicon die is cut out from the wafer using a diamond blade. The passivation layer is deposited by plasma-enhanced chemical vapor deposition, or by a spin-on technique for polyimides. The silicon chip is then attached to the lead-frame die-paddle using an electrically conductive or electrically insulative polymeric adhesive such as epoxy or polyimide. In some cases, metal and glass die-attachments are used for microcircuits or power devices that dissipate large amounts of heat or for high-reliability space applications where low outgassing is a requirement [10]. Metal or glass attachment materials, however, are more brittle, more

Petitioner Samsung Ex-1055, 0022

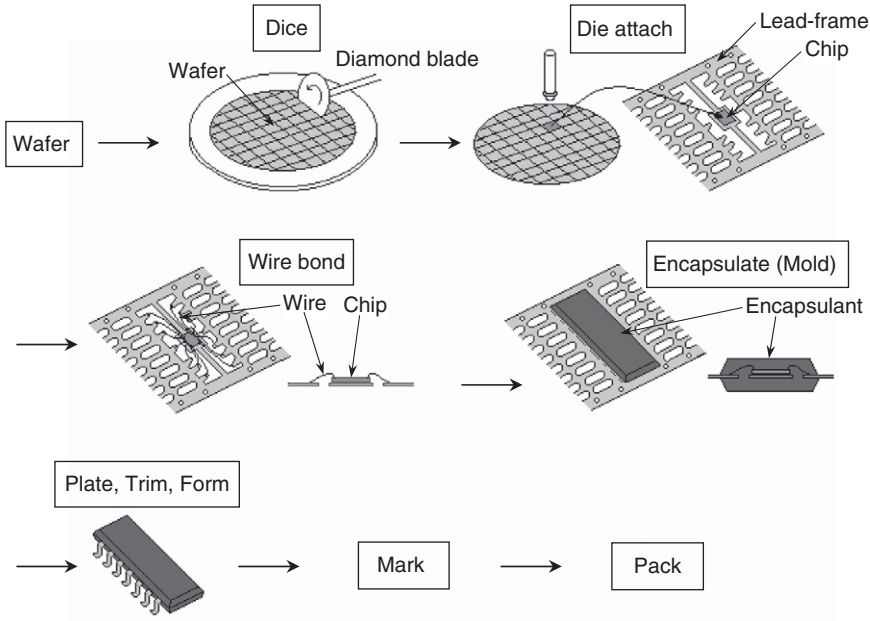


Figure 1.6 Plastic package assembly flowchart [11].

costly, and require higher processing temperatures than polymer adhesives.

The lead-frame, which consists of a die-adhesive-paddle and leads, is fabricated by either stamping or etching process. Stamping is more cost effective than etching, but it is limited to two hundred pins or fewer. The lead-frame is usually plated with silver, a tin-lead solder, or nickel-palladium before encapsulation to improve the adhesion of the bond wires.

After the attachment to the die-paddle, the chip is wire bonded to the leads for electrical connection. The bond wires are usually thermosonically bonded (ball-bonded) to the aluminum bonding pads on the chips and ultrasonically bonded (wedge-bonded) to the fingers of the lead-frame.

The interconnected chip assembly is then encapsulated. Encapsulation techniques include molding, potting, printing, glob-top, and underfill. Before encapsulation, the lead-frame assembly is plasma cleaned to remove the stamping oils from the stamped lead-frame and thus improve adhesion during encapsulation. After encapsulation the leads are deflashed. During the encapsulation process, molding compound can flow through the mold parting line and onto the leads of the device. This extra molding compound

Petitioner Samsung Ex-1055, 0023

is known as "flash." If this flash is left on the leads, it will cause problems in the downstream operations of lead trimming, forming, and solder dipping and/or plating.

Finally, the leads are trimmed and the excess lead-frame metal is cut. The leads are formed into various shapes, including dual in-line, gull-wing, or J-leads. The exposed surfaces of the lead-frame are plated with tin or a tin-lead alloy to prevent lead corrosion and enhance solderability during assembly onto the printed wiring board.

Other methods besides wire bonding for electrical connection to the PCB include tape-automated bonding (TAB) and flip-chip bonding. TAB is an automated surface-mount method that can provide interconnection for chips with large numbers of input-output terminals (≤ 500). Figure 1.7 shows the flow of a TAB process.

In the TAB process, a continuous polymer tape is fabricated with fine-pitched metal lead-frames spaced along its length. A window is made in the center of each lead-frame where the chip is to be placed. The leads of the lead-frame are then bonded to the chips, on which bonding platforms, or "bumps," have been deposited by electrolytic or electroless gold plating and liftoff photolithography. The connections to the lead-frame fingers are typically made by thermocompression bonding. The chip face may then be

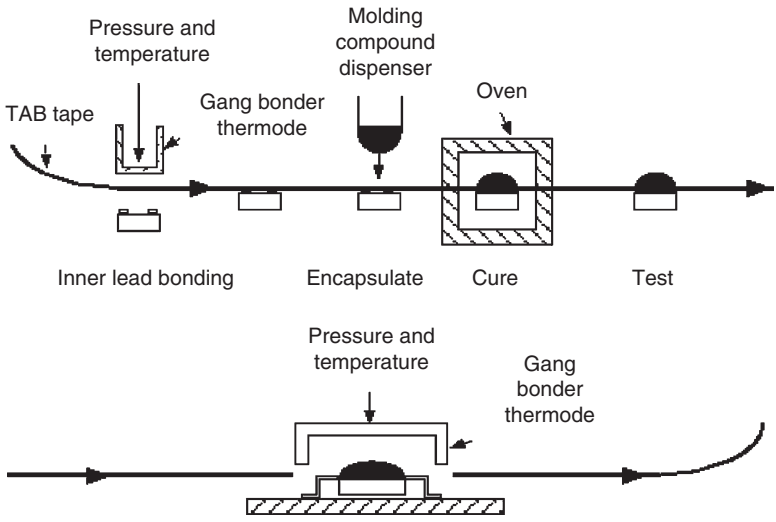


Figure 1.7 Outline of a complete tape-automated bonding (TAB) process using liquid plastic encapsulants.

Petitioner Samsung Ex-1055, 0024

coated with liquid plastic encapsulant and cured. The reel of radial-spread, coated chips is then sent to the substrate (or circuit card) assembly line, where individual chips are excised from the tape, the leads are formed, and the package is bonded to the substrate.

Electronic packaging can be classified into several packaging levels as shown in Fig. 1.8. The first level packaging consists of the interconnection and encapsulation of the IC chip. As the chip itself contains integrated microcircuits including transistors, resistors, and capacitors, it is commonly considered as a zero level package.

The second level packaging consists of the connection of the microelectronic package to the PCB. Additional protection of encapsulated microelectronics on PCBs can be achieved by the application of a polymer coating [12]. PCBs may be further interconnected to a mother board, known as third level packaging. The fourth and final packaging level is the packaging of the mother board (or PCBs) in an electronic system such as a laptop computer or a cellular phone. There are several exceptions to the mentioned packaging levels; for example, the chip may be directly connected to the PCB and then encapsulated, or the PCBs may be directly packaged in an electronic system, foregoing third level packaging. Furthermore, there are numerous variations to the packaging and interconnection styles and designs in each level, particularly in first level microelectronic packaging.

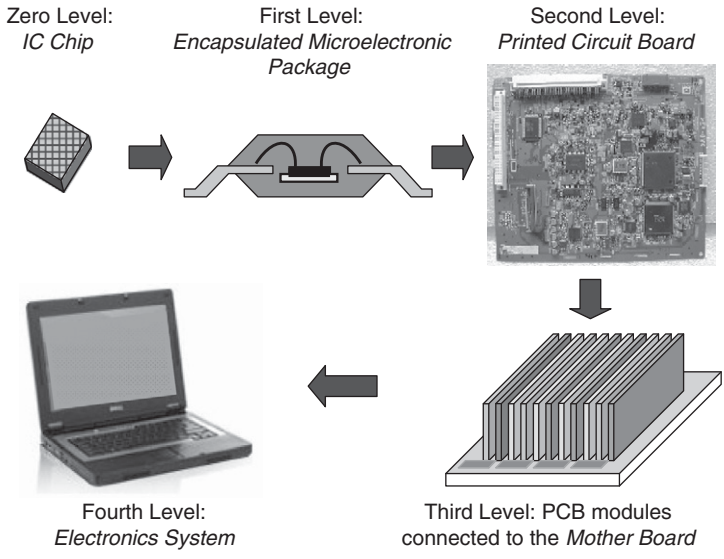


Figure 1.8 Electronic packaging levels.

Petitioner Samsung Ex-1055, 0025

1.3 Encapsulated Microelectronic Packages

Encapsulated microelectronic package styles vary in size, shape, and materials. However, many traditional plastic packages consist of a lead-frame, a die (IC chip), a die-paddle, a die-attach adhesive, bond wires, and plastic molding compound. A cross-section of a package highlighting these components is shown in Fig. 1.9.

The package lead-frame is usually made of copper, Alloy 42 (42% Ni/58% Fe), or Alloy 50 (50% Ni/50% Fe). Its function is to act as a carrier strip for package assembly, to support the die for handling, wire bonding, and assembly, to provide an electrical connection, and aid in heat dissipation.

The passivation layer on the silicon chip is typically made of silicon dioxide (SiO_2) doped with 2–5% phosphorous, silicon nitride (Si_3N_4), polyimide, or silicon carbide (SiC). The function of the passivation layer is to protect the circuit elements from mechanical damage during handling; it also acts as a barrier to ions, moisture, gases, and alpha particles. SiO_2, although a barrier to moisture, is still permeable to some ions, such as sodium. Such ions can migrate to the pn junctions on the dies, gain an electron, be deposited as metals, and destroy the device [13].

The bond wires serve as the electrical contact from the die bond pads to the lead-frame. They are generally made of copper- or beryllium-doped gold, silicon- or magnesium-doped aluminum, or copper.

The die-attach is typically made of epoxy, polyimide, or cyanate ester adhesive. Other attachment materials include solders, gold eutectic, or silver glass. The primary function of the die-attach is to hold the die in place and fixed to the lead-frame die-pad. The molding compound is a polymeric material such as epoxy or silicone. Some thermo-mechanical properties of typically used materials in a microelectronic package are presented in Table 1.1.

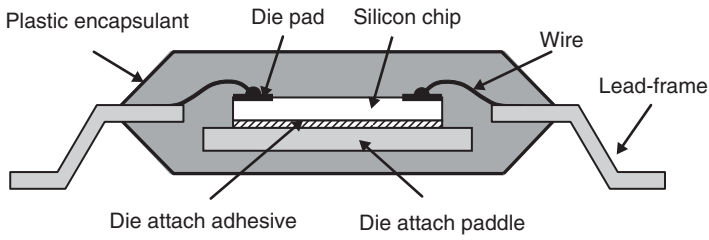


Figure 1.9 Cross-section of a plastic package.

Petitioner Samsung Ex-1055, 0026

Table 1.1 Thermo-mechanical Properties of Commonly Used Materials in Plastic-Encapsulated Devices [14–18]

Component	Material	Coefficient of Thermal Expansion (ppm/°C)	Elastic Modulus (GPa)	T_g (°C)
Lead-frame and die-adhesive paddle	Copper	16–18	110–130	–
	Alloy 42	4–5	130–145	–
Molding compound	Epoxy/silica	7–25 ($<T_g$) 40–70 ($>T_g$)	15–30 ($<T_g$) 0.2–2 ($>T_g$)	110 to 200
Chip	Silicon	2.3–3.5	129–187	–
Wire	Gold	14.1–14.4	78–79	–
Die-pad	Aluminum	23.0–23.7	70.0–70.4	–
Die-attach adhesive	BMI/silver	40–69 ($<T_g$) 104–170 ($>T_g$)	0.10–6.70	–64 to 75

The classifications of microelectronic packages are based on 2D or 3D packaging design, interconnection to PCB (leads or substrate), lead technology (through-hole or surface-mount), the shape of the leads, and how many sides of the package have leads. Microelectronic package types are shown in Fig. 1.10 and will be discussed in the following sections.

1.3.1 2D Packages

Two-dimensional microelectronic packages can be either single-chip or multi-chip packages. Encapsulated single-chip packages can be categorized into two groups: lead-frame and substrate. The lead-frame packages can be further divided into two types: packages that are through-hole mounted to the PCB and packages that are surface-mounted.

1.3.1.1 Through-Hole Mounted Packages

Through-hole technology is relatively old, and has been replaced by surface-mount technologies in most applications. Although through-hole technologies made up more than 80% of the market in 1980, it was used in less than 15% of components in 2000, and this percentage continues to decrease every year. Developed in the 1960s, through-hole technology requires that package leads be inserted into plated through-holes in the circuit board. Once inserted, the leads are wave-soldered to secure the

Petitioner Samsung Ex-1055, 0027

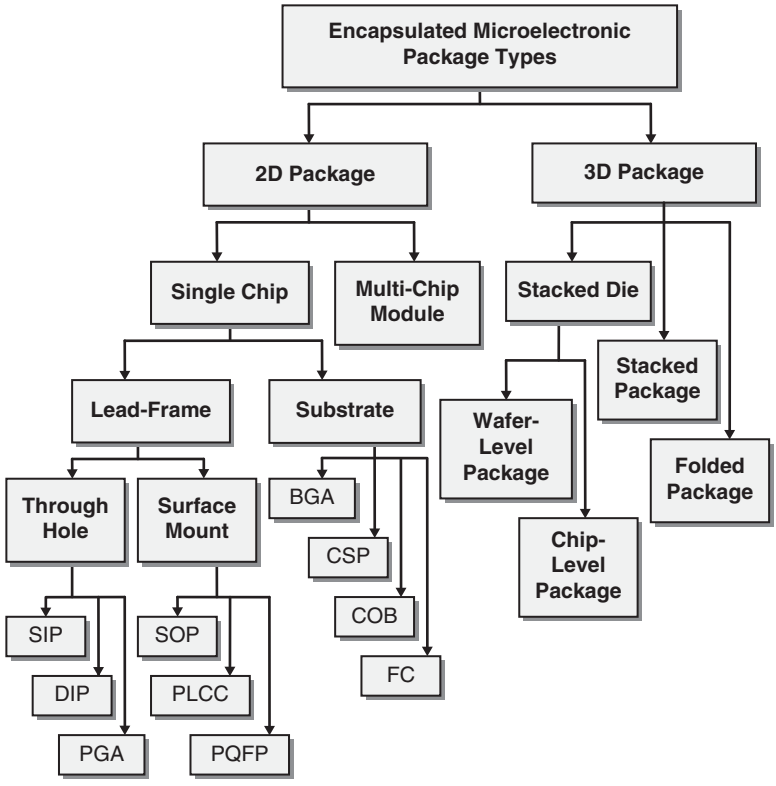


Figure 1.10 Classification of encapsulated microelectronic package types.

BGA: Ball-grid array; COB: Chip-on-board; CSP: Chip scale package; DIP: Dual in-line package; FC: Flip-chip; PGA: Pin-grid array; PLCC: Plastic-leaded chip carrier; PQFP: Plastic quad flatpack; SIP: Single in-line package; SOP: Small-outline package.

electrical connection. This mounting technology ensures a mechanically strong solder bond in which the thermal mismatches of the leads and board material can easily be tolerated. However, plated through-holes are costly, require the component to occupy more space on the board, and can only be mounted on one side of the board. The common families of through-hole packages are dual in-line package (DIP), single in-line package (SIP), and pin-grid array (PGA) package.

Plastic dual in-line packages (PDIPs), the most commonly used packages in the 1980s, have a rectangular plastic body with two rows of leads (Fig. 1.11). The leads are bent down and aligned with the vertical axis as shown in Fig. 1.11 for through-hole insertion mounting. The design of PDIP allows high-volume manufacturing at low cost. SIPs are rectangular with leads on one of the long sides, offering a high profile but small

Petitioner Samsung Ex-1055, 0028

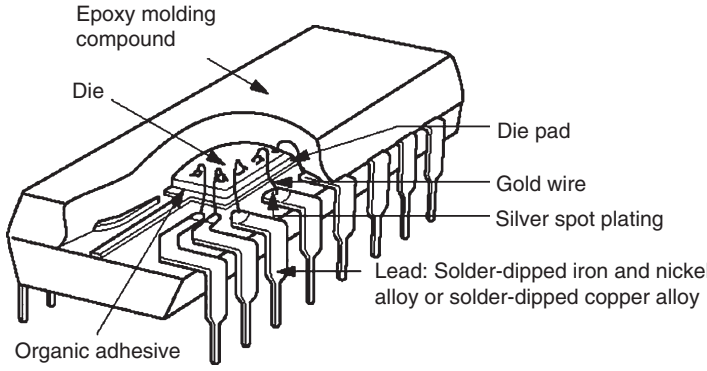


Figure 1.11 Dual in-line package.

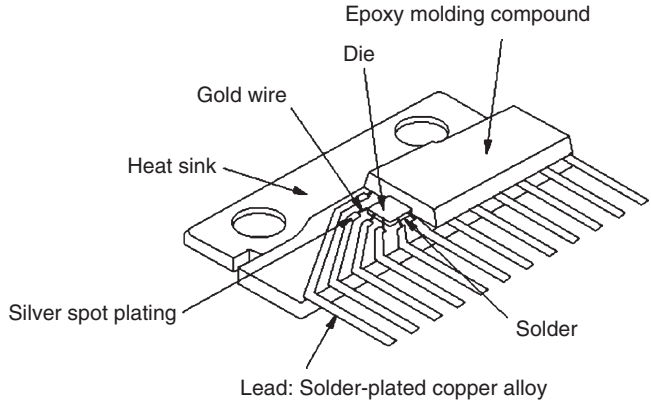


Figure 1.12 Single in-line package.

footprint on the board (Fig. 1.12). They offer all the advantages of DIPs in ease and low manufacturing cost.

Plastic pin-grid arrays are packages with leads located in a grid array under a plastic body (Fig. 1.13). Heat sinks can be incorporated if needed.

1.3.1.2 Surface-Mounted Packages

The common families of surface-mounted packages are small-outline package (SOP), plastic-leaded chip carrier (PLCC), quad flatpack (QFP), TAB, and ball-grid array (BGA). These packages are designed for low-profile mounting on printed wiring boards, and also allow for mounting components on both sides of the circuit board.

Petitioner Samsung Ex-1055, 0029

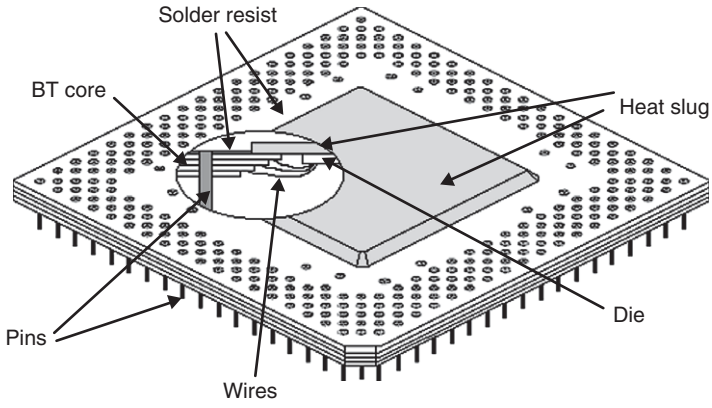


Figure 1.13 Pin-grid array package.
BT: Bismaleimide triazine.

SOPs are like DIPs, with leads on two sides of the package body (Fig. 1.14). The difference between the two is that the leads on the SOP are L-shaped in order to allow for mounting onto the surface of the circuit board. There are many variations of this device, including thin small-outline package (TSOP), heat-sinked small-outline package, and shrink small-outline package. Small-outline J-leaded (SOJ) packages are also a variation of SOP. The leads of SOJ are formed in a J-bend configuration and folded under the body. The advantage of SOJ is an even smaller footprint than that of a gull-wing, although solder joint inspection becomes more difficult.

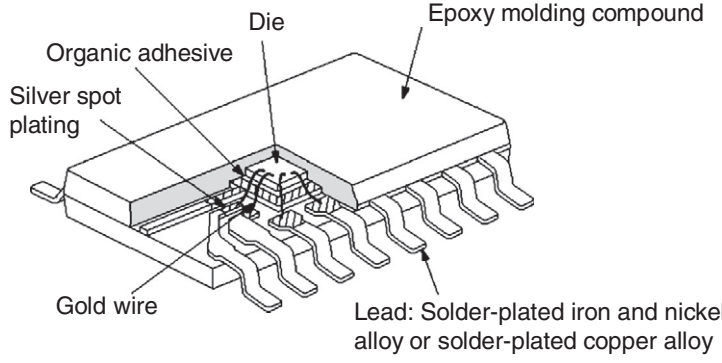


Figure 1.14 Small-outline package.

Petitioner Samsung Ex-1055, 0030

TSOPs, with their compact profiles, became a key product of the 1990s. By most estimates, TSOPs will also be used increasingly in surface-mount SOPs in the future, especially for memory, as demand for space-saving packages grows [19]. PLCCs are similar to SOJs except that the leads are on all four sides of the plastic body (Fig. 1.15). The interconnect leads of PLCCs are shorter on average and more consistent in length than those of equivalent DIPs. QFPs are square or rectangular plastic packages with leads distributed on all four sides (Fig. 1.16). QFPs are similar to PLCCs in shape and performance, but have gull-winged leads instead of being J-leads.

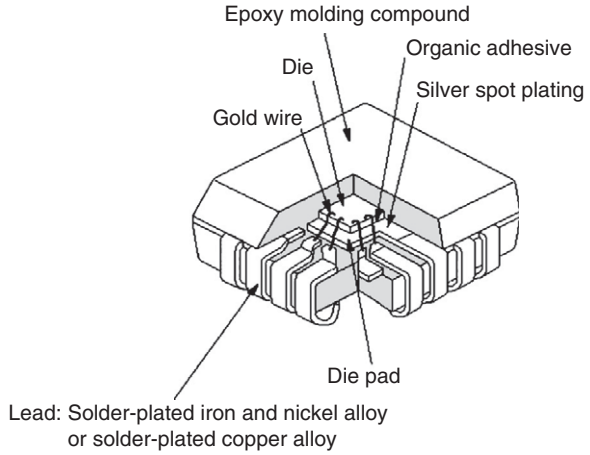


Figure 1.15 Plastic-leaded chip carrier package.

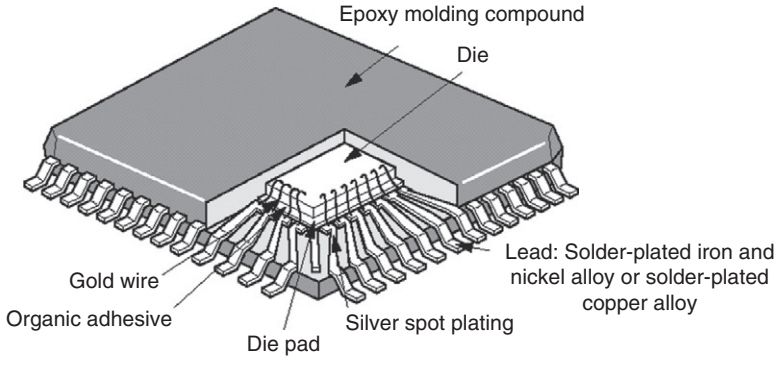


Figure 1.16 Quad flatpack.

Petitioner Samsung Ex-1055, 0031

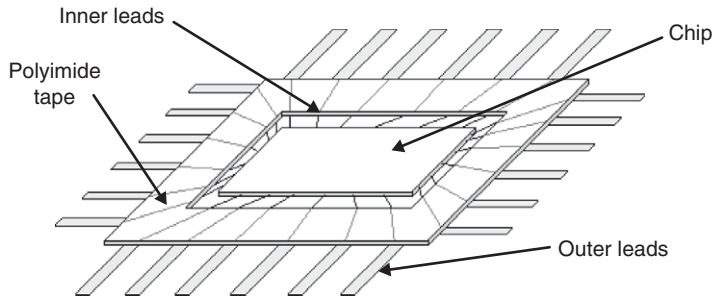


Figure 1.17 Tape-automated bonding package.

A TAB package is illustrated in Fig. 1.17. A TAB carries a chip not enclosed in a molded plastic body, but covered by a thin glass wafer, with its copper leads bonded to a polyimide tape, which has the form of a standard cine-film. These tapes are robust and can be used for automatic placement and soldering on specially designed equipments.

1.3.1.3 Substrate Packages

In BGA packages, instead of a lead-frame, an organic substrate is used. The substrate is generally made of bismaleimide triazine or polyimide. The chip is mounted to the top of the substrate, and solder balls constructed on the bottom of the substrate make connections to the circuit board. This design allows for shorter circuit interconnect lengths, which improve electrical performance, as well as a smaller package size. Variations of the BGA style include wire-bonded plastic ball-grid array (PBGA), flip-chip plastic ball-grid array (FC-PBGA), and tape-automated-bonded plastic ball-grid array. Wire-bonded PBGA and FC-PBGA package styles are illustrated in Figs. 1.18 and 1.19.

The chip scale packages (CSPs) have emerged with dimensions only slightly larger than the chip itself. Their size is no larger than 20% over the actual die size. The advantages of CSPs over traditional molded BGAs are typically lower cost due to less substrate waste, less tooling for manufacture, less mold compound waste, and the smaller footprint [20]. Several CSP configurations were developed to provide lower cost, high I/O, high density, and compact packages. One such package was developed by Tessera, called the μBGA (Fig. 1.20).

Petitioner Samsung Ex-1055, 0032

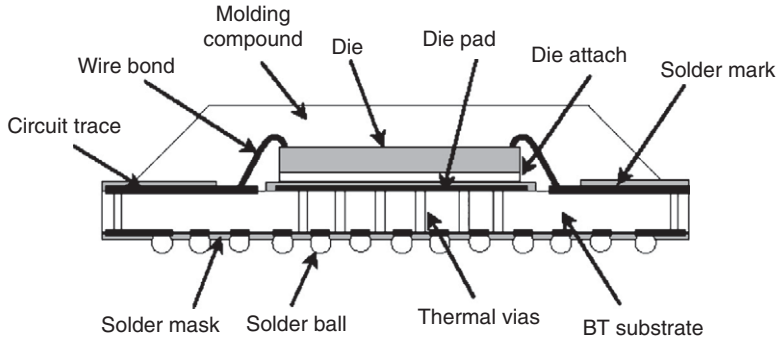


Figure 1.18 Wire-bonded plastic ball-grid array package [21].
BT: Bismaleimide triazine.

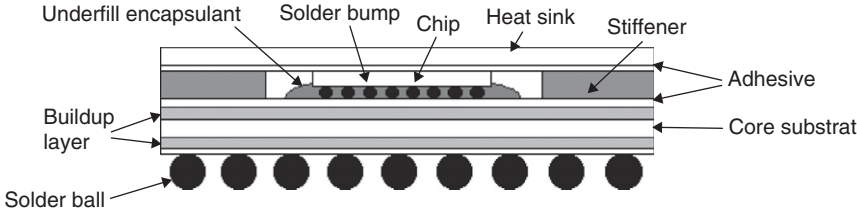


Figure 1.19 Flip-chip plastic ball-grid array package.

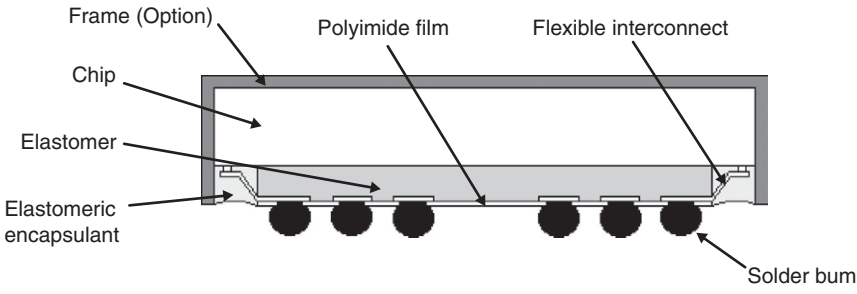


Figure 1.20 Chip scale package (μBGA developed by Tessera).

1.3.1.4 Multi-Chip Module Packages

Two-dimensional multi-chip module (MCM) packages consist of multiple IC chips positioned on the same plane and interconnected to a substrate. MCMs can be packages in many different styles. Figure 1.21 shows an MCM with PBGA package design [22].

Petitioner Samsung Ex-1055, 0033

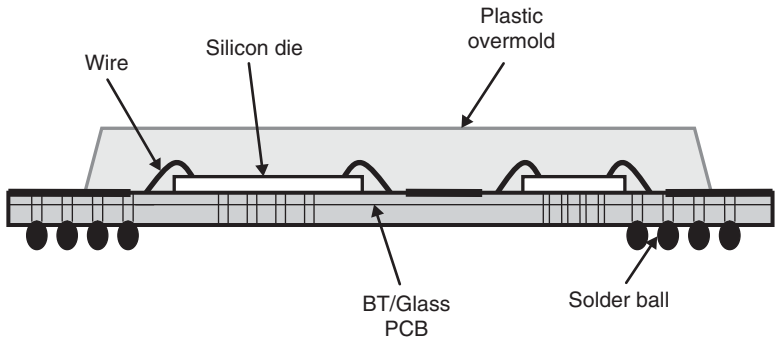


Figure 1.21 Multi-chip module plastic ball-grid array package [22].
BT: Bismaleimide triazine; PCB: Printed circuit board.

1.3.2 3D Packages

The trend in electronics is smaller, thinner, and lighter products. Over the years, the IC chips have significantly reduced in size and the electronic packages have undergone various design modifications and improvements. A focus of the electronics industry has been directed on the package silicon efficiency. Silicon efficiency is defined as the ratio of the silicon chip area to that of the package. A 100% silicon efficient package has the same mounting area (footprint) as that of the silicon chip.

For many years, the electronic industry has made improvements in the footprint size and silicon efficiency of single-chip 2D packages by varying package design. For example, CSPs offer more silicon efficiency compared to the conventional packages such as TSOPs. Two-dimensional multi-chip modules (2D MCMs) were also designed to improve silicon efficiency and device performance. In comparison, a typical CSP can reduce the package footprint to 57% of that of TSOP while a 2D MCM package footprint reduces to 62% of that of TSOP [23].

In spite of the improvements in 2D packaging designs, today's competitive electronics market, in particular the handheld and portable electronics industry, demands further improvements in silicon efficiency, packaging size reduction, and device performance. Innovative 3D packaging designs have emerged as a solution for smaller package footprints and higher device performance.

In 3D packaging, multiple chips can be stacked vertically or horizontally (side-by-side) allowing the use of the third dimension (z-axis) for the electrical interconnection. This leads to a significant improvement (exceeding 100%) in silicon efficiency. Furthermore, 3D packaging offers

Petitioner Samsung Ex-1055, 0034

improved device performance. Shorter interconnection paths between the stacked IC chips in 3D packages can lead to faster signal transfer and subsequent improved performance.

Three-dimensional packaging designs can be classified into three main groups: stacked die, stacked packages, and folded packages. 3D packages can also be further classified as wafer-level or chip-level packages depending on the assembly process.

1.3.2.1 Stacked Die

Stacked die packages are 3D packages where the IC chips are stacked and interconnected. Stacked die packages can be either chip-level or wafer-level packages. In wafer-level packages, some or all parts of the packaging process take place on the wafer. In chip-level packages, the wafer is diced and all the packaging process takes place over the IC chip.

1.3.2.1.1 3D Chip-Level Packages

An early 3D stacked die design from Irvine Sensors [24] is a side-by-side stacked die perpendicular to the supporting substrate as shown in Fig. 1.22. The chips are bonded together on their faces, and interconnected along one edge on the same access plane. A disadvantage of this earlier design was limited interconnection area due to one plane accessibility.

Another 3D package design from Thomson-CSF [25] is a stacked die either perpendicular or parallel to the PCB where all die faces are accessible for interconnection except for the base side. Figure 1.23 shows top and side views of the wire interconnection and the die stacking design.

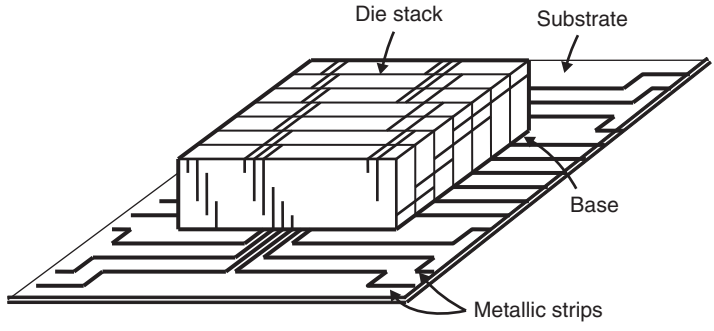


Figure 1.22 Horizontally stacked die design [24].

Petitioner Samsung Ex-1055, 0035

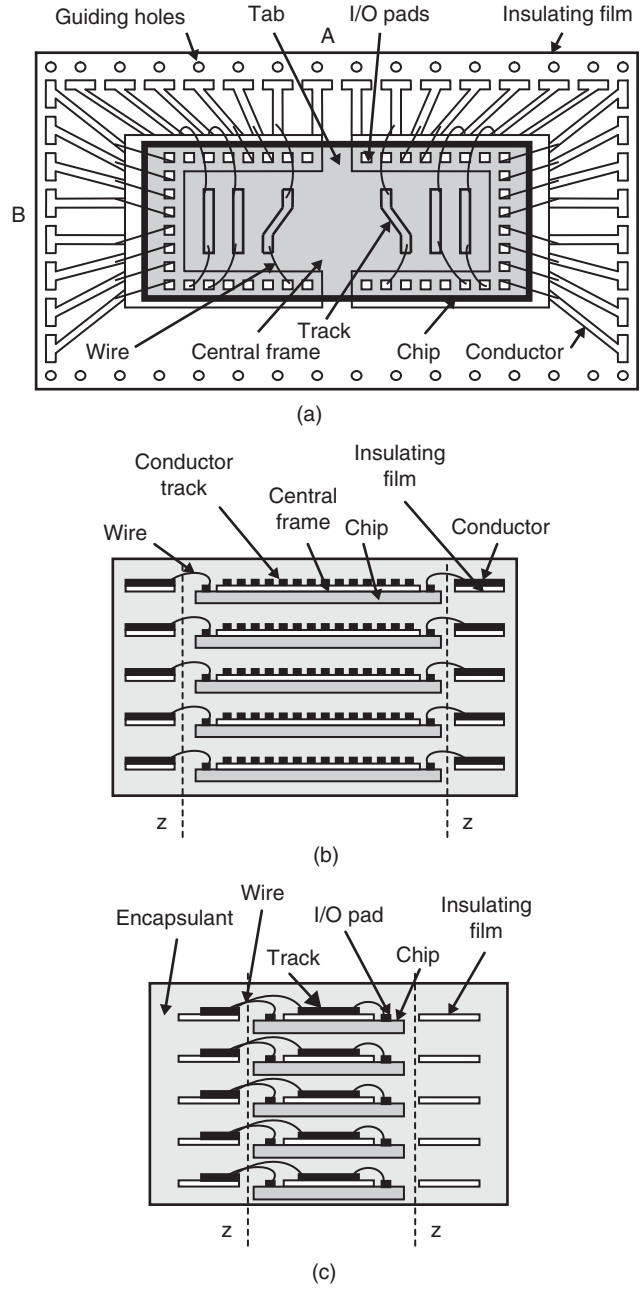


Figure 1.23 A 3D package design interconnected by wiring with improved interconnection accessibility: (a) top view; (b) side view A; (c) side view B [25].

Petitioner Samsung Ex-1055, 0036

Figure 1.24 shows the 3D packaging process. The chips are stacked and interconnected by wire bonding to the interposer frame. The stacked assembly is then encapsulated with a thermoset resin such as epoxy. Next, the encapsulated assembly is cut to expose the wire cross-section. The surfaces are then metallized for 3D interconnection. This method of 3D packaging is known as the Thomson approach [26] and the package is referred to as "MCM-V" (vertical multi-chip module).

In the 3D packaging and the interconnection design shown in Fig. 1.24, one of the main concerns is the potential parasitic capacitance between the conductor traces on the package surface and the shielding metallization.

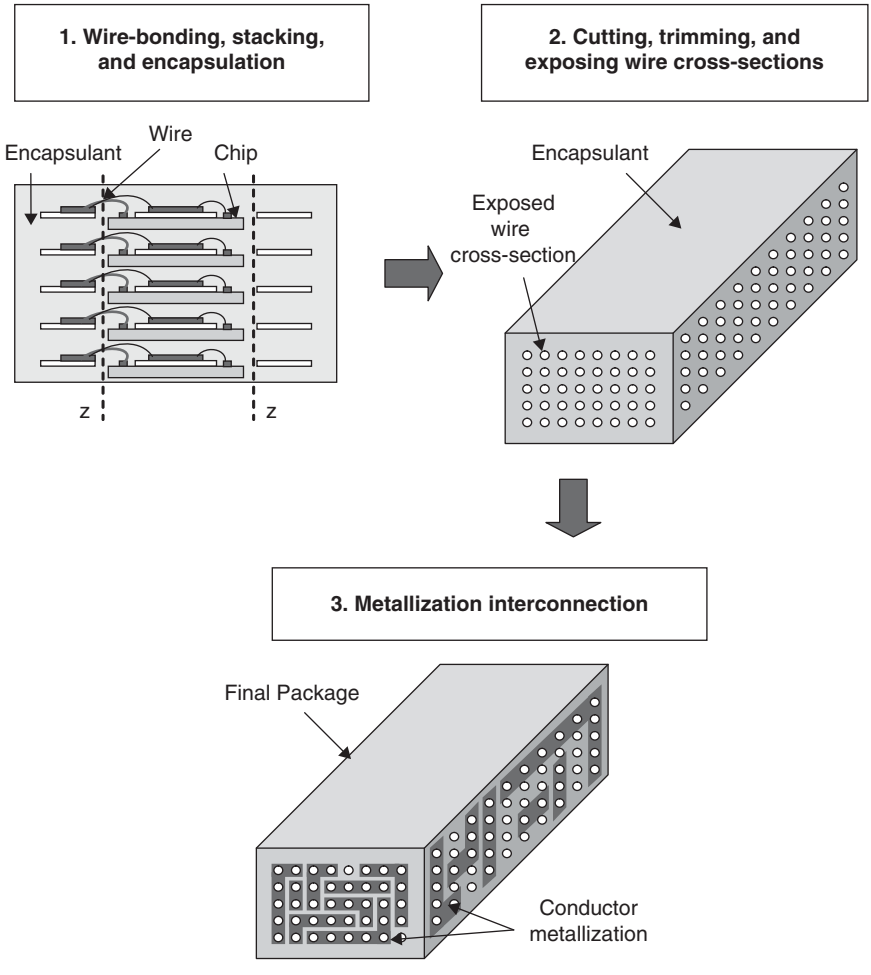


Figure 1.24 3D packaging process using the Thomson approach [25].

Petitioner Samsung Ex-1055, 0037

As the capacitance is directly proportional to the area of the facing metallization surfaces, a solution is to reduce the facing surfaces. The conductors can be set back by few micrometers up to a few hundred micrometers. Grooves can then be cut into the package face, perpendicular to the face, up to the set-back conductors, and then metallized. This method significantly reduces the facing metallization surfaces, and subsequently, the parasitic capacitance [27]. The metallized grooves can be designed in various shapes as shown in Fig. 1.25.

Die stacks can be interconnected using TAB. Figure 1.26(a) shows a 3D package design by Matsushita [28] where the TAB leads are used for vertically stacked IC chips. Figure 1.26(b) shows another stack design used by Texas Instruments [29] where the IC chips are stacked side by side and interconnected to a substrate using TAB leads.

In addition to the homogeneous die stacking designs mentioned, there are also non-homogeneous stacking designs where the die sizes may differ and the stacking areas may not be aligned. Two non-homogeneous stacking designs are shown in Fig. 1.27 [30]. The stacking in Fig. 1.27(a) is referred to as the "Towers of Hanoi" design where the dies, gradually decreasing in size, are stacked vertically, and are wire bonded to the adjacent die. Figure 1.27(b) shows a cross-bonded stacking where the die areas are not aligned.

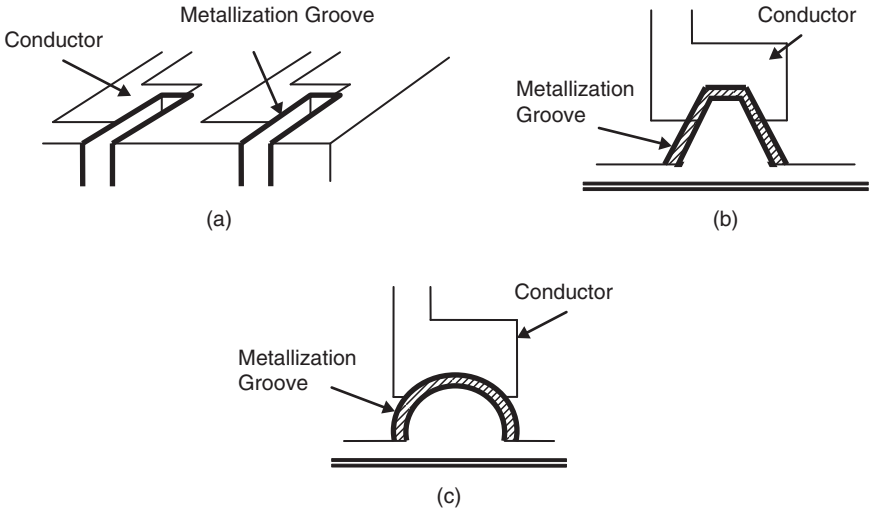


Figure 1.25 Interconnection metallization grooves in 3D packaging design with various shapes: (a) rectangular; (b) V-shaped; (c) circular [27].

Petitioner Samsung Ex-1055, 0038

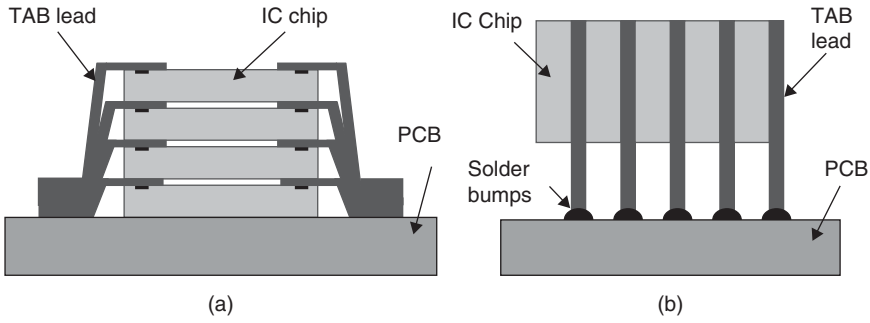


Figure 1.26 Homogeneous die stacking designs using TAB: (a) vertical stacking design by Matsushita [28]; (b) horizontal stacking design by Texas Instruments [29].

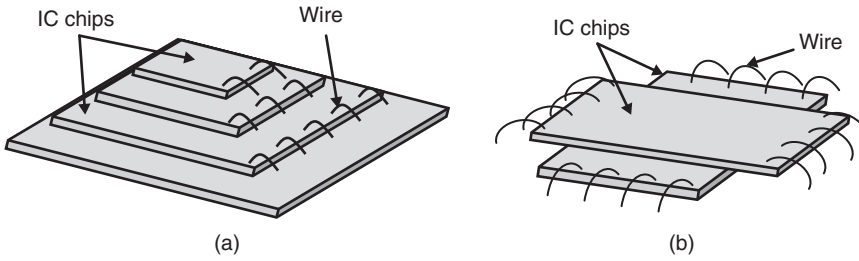


Figure 1.27 Non-homogeneous die stacking designs: (a) telescopic or "Towers of Hanoi" design; (b) cross-bonded [30].

Another 3D packaging design known as chip-in-polymer (CIP) consists of stacking and embedding the IC chips in a thin-film/polymer matrix and interconnecting using vias [31,32]. Figure 1.28 shows a CIP package with five memory chips stacked and embedded in a polymer matrix.

1.3.2.1.2 3D Wafer-Level-Packages

In 3D wafer-level packaging (WLP) any or all parts of the packaging process such as via formation, stacking, bonding, and encapsulation can take place on the wafer. There are several options for the interconnection vias in 3D WLP as shown in Fig. 1.29. For a conventional IC chip that is not designed for 3D packaging, the through-vias are formed outside the die-pads. In the case of IC chips designed for 3D packaging, the interconnection via can be created during IC chip processing, either

Petitioner Samsung Ex-1055, 0039

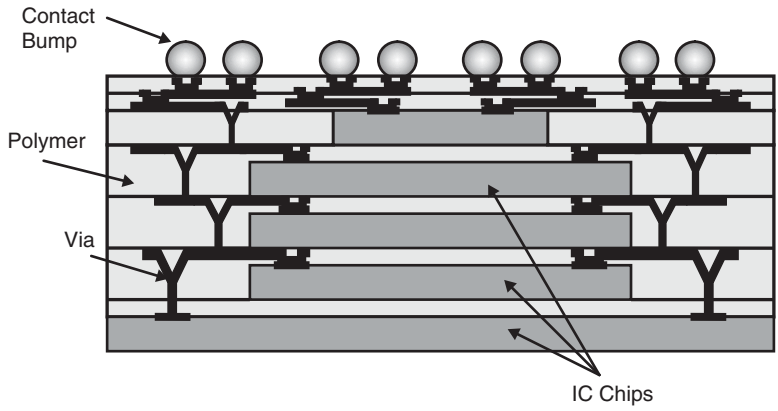


Figure 1.28 Chip-in-polymer package [31,32].

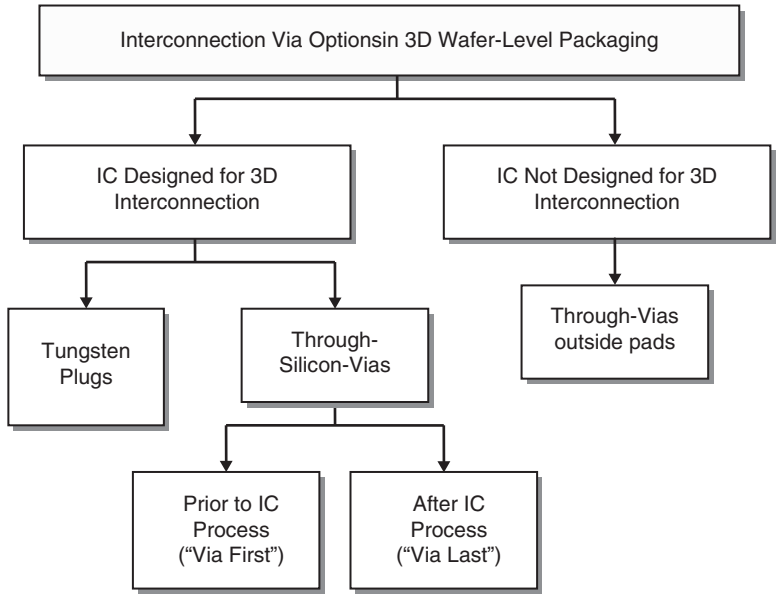


Figure 1.29 Interconnection via options for 3D wafer-level packaging [33].

before IC device processing (referred to as the "via first" method) or after ("via last").

A 3D wafer-level die stacking design by the Association of Super-Advanced Electronics Technologies (ASET) includes Cu through-vias outside the die-pad and Cu bump bonding as shown in Fig. 1.30 [33–35].

Petitioner Samsung Ex-1055, 0040

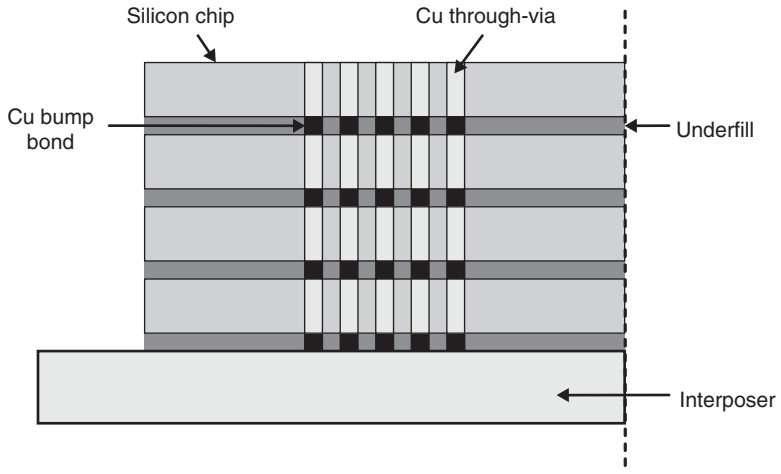


Figure 1.30 Cross-section of 3D die stacking design by ASET using Cu through-vias and Cu bump bonding [34,35].

This 3D package design is suitable for conventional IC chips that were not originally designed for 3D packaging.

A wafer-level die stacking technology developed by NEC Electronics, Oki Electric Industry, and Elpida Memory consists of stacking memory chips with through-vias and feed-through interconnections (FTIs) referred to as SMAFTI (SMArt chip-FTI) technology [36] shown in Fig. 1.31. The vias in the memory die are created using the "via first" method depicted in Fig. 1.32. Highly doped poly-silicon through-silicon vias are created for

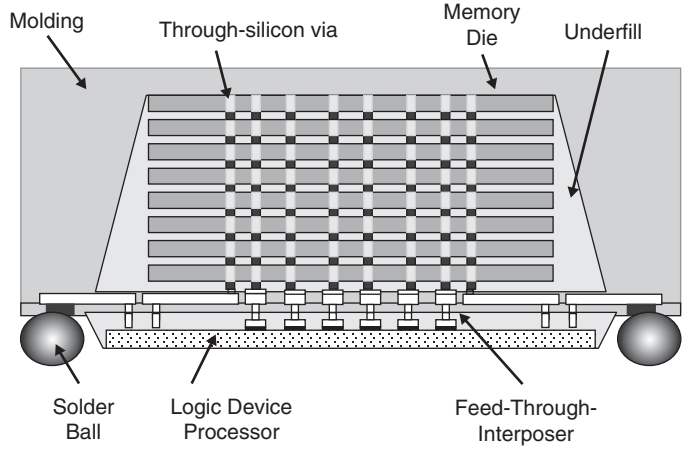


Figure 1.31 Stacked die package with through-silicon via [36].

Petitioner Samsung Ex-1055, 0041

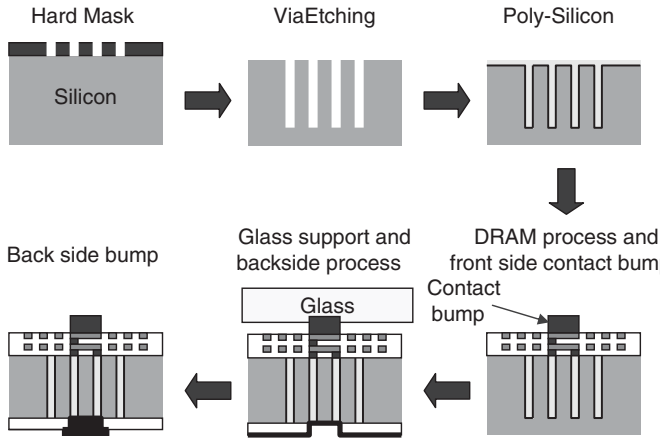


Figure 1.32 Through-silicon via process flow using "via first" method for 3D packaging interconnection [36].

DRAM: Dynamic random access memory.

vertical interconnection inside the memory device and frontside and backside bumps are created for contact.

The SMAFTI assembly process is shown in Fig. 1.33. In WLP, there are two choices for assembly: die to wafer (D2W) or wafer to wafer (W2W). The D2W process has the advantage of assembling known good die. Known good dies are fully tested IC chips that have passed all functional tests and are ready to be bonded and packaged.

In the SMAFTI assembly process, after the W2W or D2W stacking and bonding to the feed-through interconnection, the underfill is injected to encapsulate the contact bumps between the chips in the stack [37]. The multiple stacks on the support wafer are then molded as shown in Fig. 1.33. The support wafer is then removed and the wafer is diced. Finally, the processor device is bonded to the FTI in each die stack assembly and the solder balls are formed.

Another type of via for 3D interconnection for IC devices designed for 3D packaging is a through-via made from tungsten that is created during IC processing on the wafer [33]. Figure 1.34 shows two wafer layers stacked with their Cu pads aligned and in contact. The tungsten plug is created in the backside of the top wafer, which connects the last metallization in the top wafer to the aluminum pad on the surface of the stack. An aluminum pad is used for wire bonding and final packaging. The smaller vias are used to vertically interconnect the metallization layers [38].

Petitioner Samsung Ex-1055, 0042

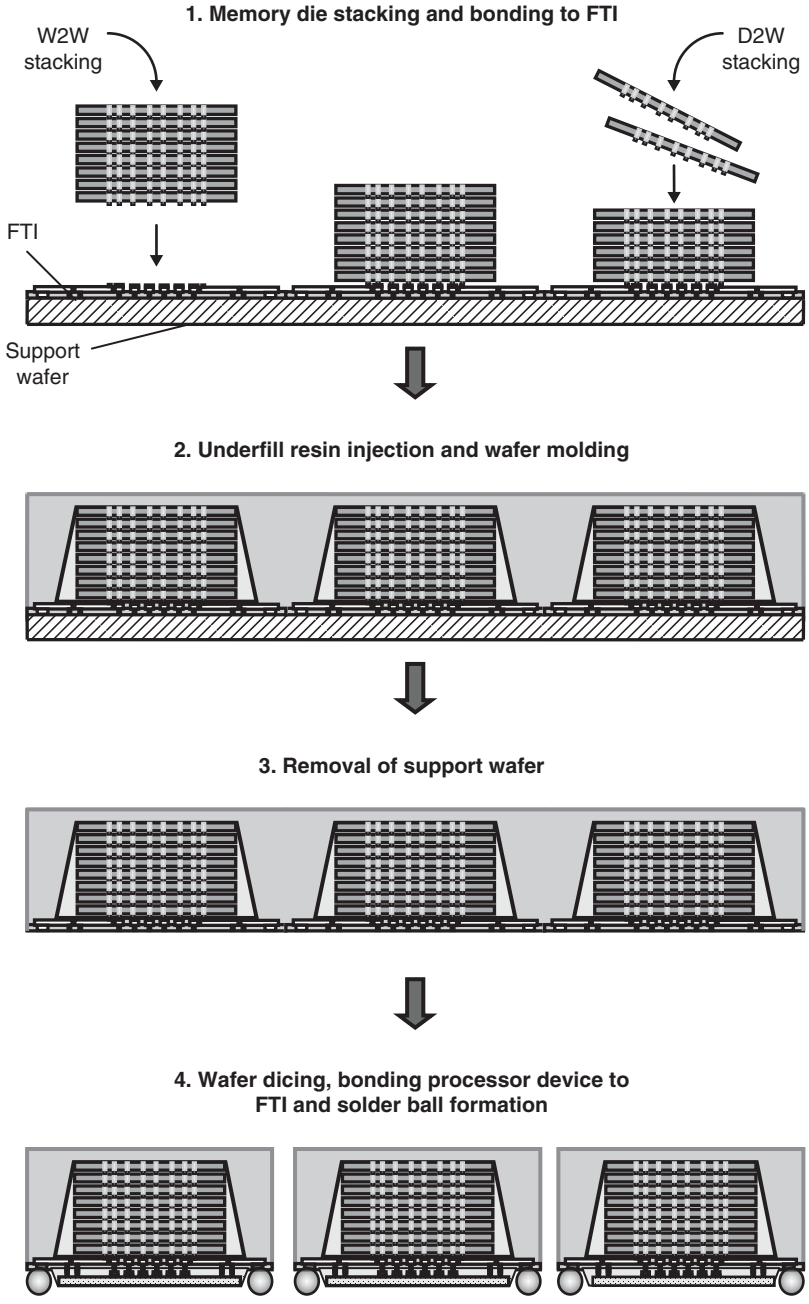


Figure 1.33. Assembly flow of wafer-level 3D stacked die package using SMAFTI technology [37].

D2W: Die to wafer; FTI: Feed-through interconnection; W2W: Wafer to wafer.

Petitioner Samsung Ex-1055, 0043

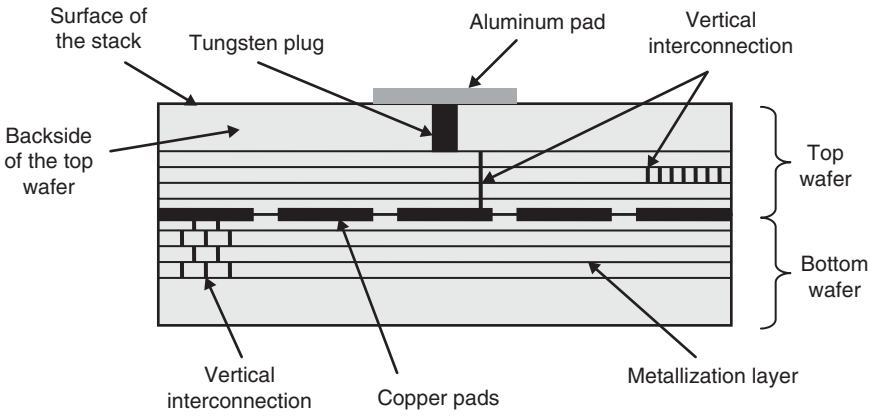


Figure 1.34. Stacked wafer packaging design with tungsten plug interconnection ("super-contact") used by Tezzaron [38].

1.3.2.2 Stacked Packages

Three-dimensional packaging designs can also be applied to packaged single chip or multi-chip modules where the packages are stacked and interconnected to the PCB using the third or z-dimension. A 3D stacked molded interconnect device package [31] is shown in Fig. 1.35, where the single chip device is encapsulated, contact bumps are formed on the chip, and the packages are stacked and interconnected.

Figure 1.36 shows a few other single-chip package or MCM stack designs. Figure 1.36(a) shows stacked TSOPs interconnected to the PCB.

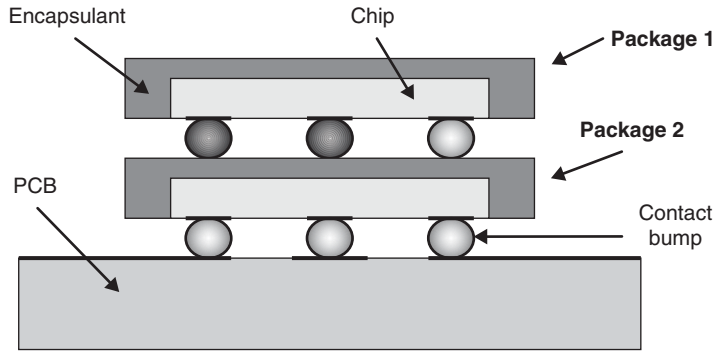


Figure 1.35 Molded interconnect device package stacking design [31].
PCB: Printed circuit board.

Petitioner Samsung Ex-1055, 0044

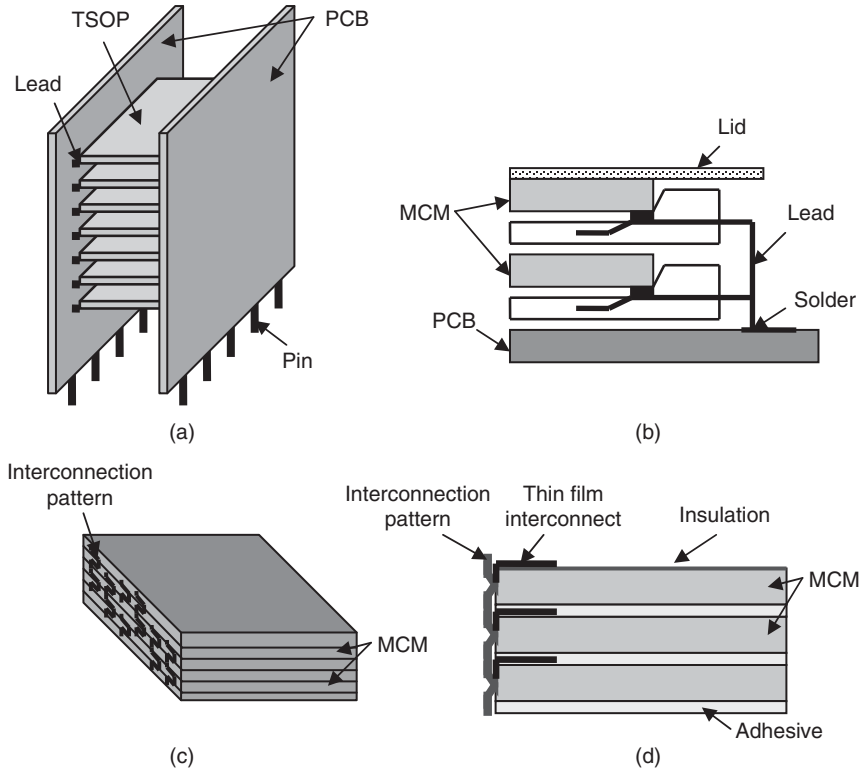


Figure 1.36 Stacked package designs: (a) stacked TSOPs; (b) stacked QFP-format MCMs; (c) 3D stacked MCMs with HDI technology (3D-MCM-HDI); (d) cross-section of 3D-MCM-HDI [29,39].

HDI: High density interconnection; MCM: Multi-chip module; PCB: Printed circuit board; QFP: Quad flatpack; TSOP: Thin small-outline package.

Figure 1.36(b) shows a design used by Matsushita Electronic Components in which stacked MCMs are interconnected with leads as depicted and soldered to the PCB. This design is referred to as "stacked QFP-format MCMs" [29]. Figure 1.36(c) and (d) shows a 3D MCM stacking design using high density interconnection from General Electric [39]. In this design, multiple IC chips are attached and interconnected to a flexible substrate known as chip-on-flex MCMs (COF-MCMs). The COF-MCMs are then stacked, bonded with adhesives, and interconnected using thin film interconnection technology. The 3D package is then bonded to the PCB from the side using contact bumps.

Petitioner Samsung Ex-1055, 0045

1.3.2.3 Folded Packages

In a folded package, a flexible substrate is used for interconnection of the IC chips (or packaged devices) and is folded to form a 3D package. Figure 1.37(a) shows a flexible substrate with bonded flip-chips prior to folding. In Fig. 1.37(b) the substrate is folded into a 3D package configuration [40].

Folded package designs by Entorian Technologies Inc. [41] use folded flexible circuits for z-axis interconnection as shown in Fig. 1.38. Figure 1.38(a) shows two CSPs interconnected by folding a flex circuit [19], and Fig. 1.38(b) shows two TSOPs interconnected by folding the flex ends in contact with the leads [42].

1.4 Hermetic Packages

Hermetic packages are cavity packages that are designed to seal against moisture and corrosive gases. They are made of materials that are highly moisture impermeable such as ceramics and metals. A metal or ceramic lid (or housing) is welded or attached to a package base to produce the hermetic seal. The base is baked-out to ensure a dry environment inside the package prior to sealing. The interconnection in hermetic packages can be glass-to-metal feed-throughs for extended leads or integral leads. Figure 1.39 shows a metal flatpack with extended electrical leads.

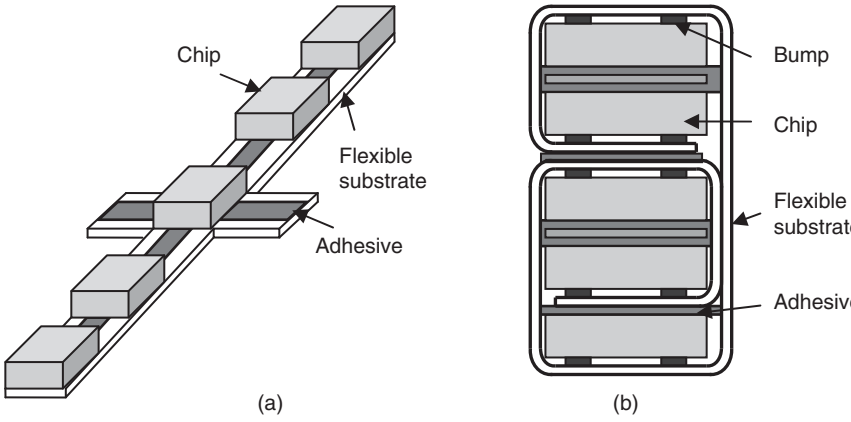


Figure 1.37 (a) Flip-chips on a flexible substrate prior to folding; (b) folded stacked flip-chip design [40].

Petitioner Samsung Ex-1055, 0046

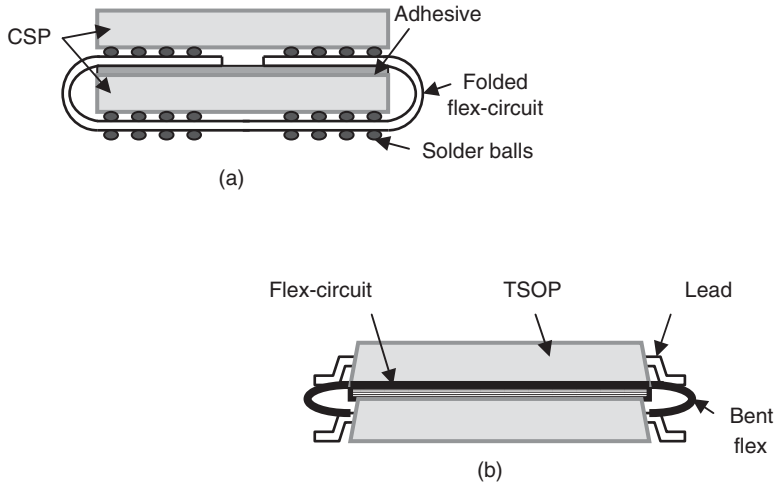


Figure 1.38 Folded package designs by Entorian (formerly Staktek) with (a) CSPs and (b) TSOPs interconnected using a folded flexible circuit [19,41,42].
CSP: Chip scale package; TSOP: Thin small-outline package.

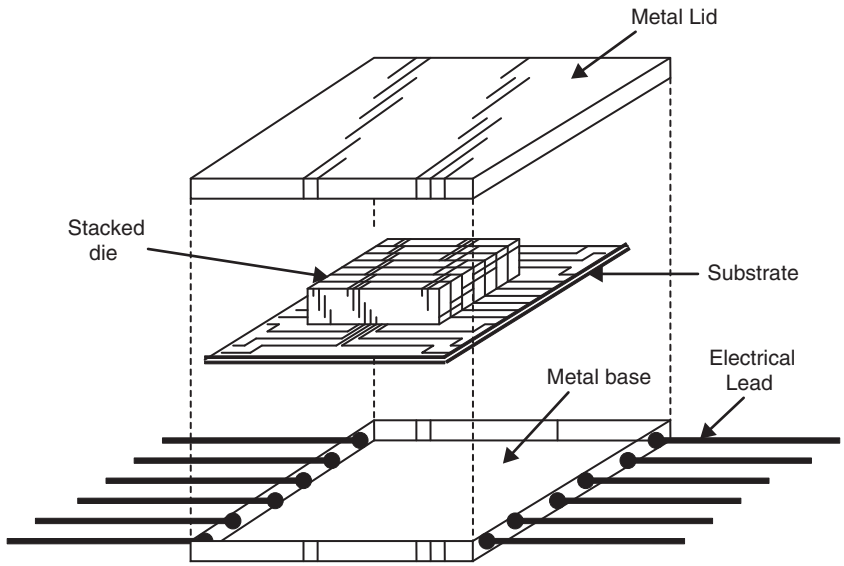


Figure 1.39 A metal flatpack consisting of a metal lid sealed to a base with extended leads forming a hermetic package [24].

Petitioner Samsung Ex-1055, 0047

1.4.1 Metal Packages

One of the first microelectronic packages was a metal package, specifically a Kovar (29% Ni/17% Co/54% Fe) preformed package. Kovar is a nickel–cobalt ferrous alloy and its coefficient of thermal expansion is similar to that of hard (borosilicate) glass. It is a suitable choice for sealing between metal and glass or ceramic parts. Another metal used in hermetic packaging is Alloy 42. The properties of Kovar and Alloy 42 are listed in Table 1.2.

1.4.2 Ceramic Packages

Ceramic packaging has significantly decreased in the electronic packaging industry, in particular in commercial electronics. Ceramic packages are more expensive compared to their plastic counterparts; however, they are highly hermetic, which helps protect the electronics from moisture and corrosive gas.

One specific application of ceramic packaging is in microelectromechanical systems (MEMS). Exposure to plastic encapsulation contact

Table 1.2 Properties of Two Common Metals Used in Hermetic Packages

	Kovar	Alloy 42
Composition	Nickel (Ni): 29% Cobalt (Co): 17% Silicon (Si): 0.10% Carbon (C): 0.02% Manganese (Mn): 0.30% Iron (Fe): Remainder	Nickel (Ni) : 39/41% Chromium (Cr): 0.05% Manganese (Mn): 0.60% Silicon (Si): 0.02% Carbon (C): 0.05% Aluminum (Al): 0.02% Cobalt (Co): 0.05% Phosphorus (P): 0.02% Sulfur (S): 0.02% Iron (Fe): Remainder
Coefficient of thermal expansion	30–200°C: 5.5 ($\times 10^{-6}$ m/m · C) 30–500°C: 6.2 30–900°C: 11.5	30–200°C: 4.5 ($\times 10^{-6}$ m/m · C) 30–500°C: 8.0 30–900°C: 12.3
E	20×10^6 psi	21×10^6 psi
Yield strength	50,000 psi	40,000 psi
Ultimate strength	75,000 psi	72,000 psi

Petitioner Samsung Ex-1055, 0048

stresses and environmental stresses can be detrimental to MEMS components such as micro-sensors and micro-mechanical elements, thus making ceramic packaging a more suitable choice.

A common type of ceramic material used in electronic packaging is low temperature co-fired ceramic (LTCC). LTCC has shown a track record of high reliability in military applications [43].

Ceramics have the advantage of a wide range of material properties. The coefficient of thermal expansion of ceramics can match that of silicon chips, 3 ppm/ºC, or that of copper lead-frame, 17 ppm/ºC. Dielectric constants can vary from 4 to 10,000. Thermal conductivities also vary from one of the best insulators to better than aluminum metal 220 W/m K. Dimensional stability as measured by shrinkage control has been achieved at better than $\pm 0.1\%$ of nominal shrinkage, allowing as many as 30–50 layers of ceramic to be metallized [44].

1.5 Encapsulants

Encapsulants protect the semiconductor chips from the environment. More than 99% of commercial microelectronic devices are plastic encapsulated. Plastic packages offer several advantages over ceramic and metallic packages, including lower design and manufacturing costs, lighter weight, and smaller size [11,45]. In addition to encapsulation, conformal coating can be applied for further protection of the microelectronics. Coating methods and materials have been previously addressed by J.J. Licari [12].

The most common type of encapsulants is molding compound. Other types of plastic encapsulation methods include glob-topping, potting, printing, and underfilling.

1.5.1 Plastic Molding Compounds

Molding compounds are supplied as molding bricks (preforms) that are ready for use in transfer-molding machines to produce SIPs, DIPs, PLCCs, and QFPs. PGA carriers, carriers with cans, for example, frequently use multi-component liquid epoxies or preforms.

Molding compounds must posses adequate mechanical strength, good adhesion to package components, manufacturing and environmental chemical resistance, electrical resistance, a low coefficient of thermal expansion, high thermal stability, and moisture resistance in the use temperature range.

Molding compounds used for encapsulation can be classified as thermoplastics, thermosetting polymers, and elastomers. Thermoplastics are those

Petitioner Samsung Ex-1055, 0049

materials that can be remelted when heated. Thermosetting polymers are materials with cross-linked polymer chains that have no melting temperature after they are cured. Elastomers are thermosetting polymers that have very high elasticity.

The majority of encapsulant materials used today are thermosetting polymers. Thermosetting molding compounds based on epoxy resins or, in some niche applications, organosilicone polymers, are widely used to encase electronic devices. Polyurethanes, polyimides, and polyesters are used as encapsulants and coatings to protect modules and hybrids intended for use under low temperature and high humidity conditions. Modified polyimide coatings have the advantages of high thermal stability, low moisture permeability, low coefficient of thermal expansion, and high material purity.

Thermoplastics are rarely used for encapsulation, because they require unacceptably high temperature and pressure processing conditions. Remelting thermoplastic encapsulants can be detrimental to the semiconductor device if the melting temperature is too high. They are also low purity materials, and can lead to moisture-induced metallization corrosion.

Thermoplastics, on the other hand, can be recycled and are environmentally friendly. Therefore, research has been carried out to improve the properties of thermoplastic materials [46]. A thermoplastic material developed by a Motorola research group exhibits a thermal conductivity an order of magnitude greater than the conventional molding compound materials, making it a potential encapsulant for high power semiconductor device applications [46]. A high purity fluoropolymer thermoplastic material developed by a 3M Innovative Properties group also has a potential use in semiconductor packaging [47].

Elastomers are another type of polymers that are generally soft and deformable at ambient temperatures due to their subambient glass transition characteristics. They have limited usefulness as encapsulants for conventional packages because of their deformability and low level purity. However, they can be useful for adhesives, seals, and encapsulation of flexible components.

1.5.2 Other Plastic Encapsulation Methods

Other types of encapsulation methods include glob-topping, potting, underfilling, and printing encapsulation. Glob-top encapsulant materials are dispensed as liquids over the semiconductor device, and then cured to

Petitioner Samsung Ex-1055, 0050

form a protective barrier. Common materials used as glob-top encapsulants are silicones and epoxies.

Potting and casting encapsulants are used for larger components such as transformers, connectors, and MCMs. In potting, the device is put inside a "pot" (or a mold) and liquid resin is poured into the pot, which becomes a part of the encapsulated electronic unit. Casting is similar to potting except that the pot is removed at the end of the encapsulation process. Silicones, epoxies, and polyurethanes are common potting and casting encapsulants.

Underfill encapsulants are generally used in flip-chip packages, CSPs, and BGA packages to provide mechanical support, structural stability, and protection of solder balls. Commonly used underfill encapsulant materials are epoxy thermosets.

The printing encapsulation method is used for smaller and thinner packages. It involves printing using a stencil (stencil printing) or printing onto existing cavities interconnection bumps (cavity printing). A suitable printing encapsulant material is liquid epoxy resins with low warpage (out-of-plane deformation) characteristic.

1.6 Plastic versus Hermetic Packages

Plastic packages offer many advantages over hermetic packages in the areas of size, weight, performance, cost, and availability. The reliability of plastic-encapsulated products has also improved significantly over the past few decades.

1.6.1 Size and Weight

Commercial plastic microelectronic packages generally weigh about half as much as ceramic packages. For example, a fourteen-lead PDIP weighs about 1 gram, versus 2 grams for a fourteen-lead ceramic dual in-line package (CERDIP). There is little difference in size between plastic and ceramic DIPs; however, smaller configurations (such as SOPs) and thinner configurations (such as TSOPs) are available only in plastic packages. The use of SOPs and TSOPs also enables better-performing circuit boards due to higher packing density and shorter interconnection paths leading to reduced component propagation delays.

Size and weight of microelectronic packages are important concerns especially for avionics and handheld consumer electronics industries. Smaller form factor (a designation used for characterizing motherboard size)

Petitioner Samsung Ex-1055, 0051

indicates a higher board density, more functionality packed into the board, and smaller-sized microelectronic packages. In terms of weight, a lighter package leads to a lighter overall payload for the same board functionality. With the emergence of 3D die stack packaging, plastic-encapsulated package density can increase even further, leading to smaller and lighter electronic packages.

1.6.2 Performance

The dielectric constant of plastic encapsulants is generally lower than that of ceramics (about 9 or 10). Because the high frequency signal propagation delay is proportional to the square root of the dielectric constant, higher dielectric constant materials such as ceramics have adverse effects on signal propagation speed. Therefore, plastic packages are generally preferred to ceramic packages with respect to performance.

Plastic packages that offer high signal propagation speed include 2D packages such as plastic quad flatpacks (PQFPs), PGAs, and BGAs and 3D die stack packages. In addition to plastic encapsulation, these packages have higher pin count and packaging density. Low pin count and low density plastic packages such as DIPs are not as effective in signal propagation.

Another factor related to plastic packaging that affects performance is the lead inductance. Copper lead-frames typically used in plastic packages have smaller lead inductance compared to that of the Kovar leads used in ceramic packages. This results in further improvement in the performance of plastic microelectronic packages relative to their ceramic counterparts in the same form factor.

1.6.3 Cost

The cost of a complete plastic package is driven by several factors, including die, encapsulation, production volume, size, assembly, screening, burn-in, final testing, yields, and qualification tests. Because more than 99% of the IC market is plastic-packaged, the cost has been lowered by high demand, competition, and high-quality automated volume manufacturing. Some low-volume, hermetic ceramic parts may cost up to 100 times more than their commercial plastic counterparts.

Hermetic packages usually have a higher material cost and are fabricated with more labor-intensive processes. For example, Thomson-CSF reported a 45% purchase cost reduction for each of twelve printed wiring

Petitioner Samsung Ex-1055, 0052

boards in a manpack transceiver application implemented with plastic rather than ceramic components [48]. Another factor that drives up the cost of hermetically packaged ICs is the rigorous testing and screening required for the low-volume hermetic parts. When both types are screened to customer requirements, ELDEC estimated that purchased components for plastic encapsulation of ICs cost 12% less than their hermetic counterparts, primarily due to the economics of high-volume production [49].

The cost benefits of plastic packages decrease with higher integration levels and pin counts, because of the high price of the die in relation to the total cost of the packaged device. While these cost benefits may not be realized for complex monolithic very-large-scale ICs, cost advantages may accrue for complex package styles, such as MCMs, because of the ease of assembly. Indeed, the trend toward future multi-chip modules in laminates (MCM-L) packaged in form factors such as PQFPs or BGAs will make plastic packages even more popular. In MCM-L, several dies and passive components can be combined on a PCB substrate and integrated onto a lead-frame to enhance part functionality. This approach shortens the time to market (by using readily available dies to eliminate the need for die integration), increases the process yield (there are no large dies and no mixture of such different technologies as complementary metal-oxide semiconductor and bipolar), and lowers package cost (compared with a ceramic equivalent).

1.6.4 Hermeticity

The hermeticity of cavity packages depends on various factors including the cavity pressure and the sealing quality. A widely used method of evaluating hermeticity is the helium leak test. Helium has the advantage of higher diffusion rate and easier identification with a mass spectrometer. In helium leak tests the package is subjected to pressurized helium in a vessel (bomb). Upon removal from the vessel, the helium that had entered the package through the leak is detected as it escapes the package.

Conditions for a helium fine leak test are shown in Table 1.3 [50]. The package is exposed to helium at pressure P_E measured in psia (pounds-force per square inch absolute) and for a minimum time of t_1 measured in hours. The time t_2 is the maximum dwell time between the release of pressure and the leak detection. R_1 is the measured rate of helium detected through the leak in atm cm^3/sec. The package is rejected if the leak rate is above the specified limit R_1. The times, t_1

Petitioner Samsung Ex-1055, 0053

Table 1.3 Fixed Conditions for Helium Fine Leak Testing [50]

Package Volume (cm^3)	P_E (psia ± 2 psia)	Minimum Exposure Time, t_1 (hrs)	Maximum Dwell Time, t_2 (hrs)	R_1, Reject Leak Rate Limit (atm cm^3/sec)
<0.05	75	2	1	5×10^{-8}
≥0.05 to <0.5	75	4	1	5×10^{-8}
≥0.5 to <1.0	45	2	1	1×10^{-7}
≥1.0 to <10.0	45	5	1	5×10^{-8}
≥10.0 to <20.0	45	10	1	5×10^{-8}

and t_2, and pressures are based on the Rome Air Development Center Report [51].

Hermeticity evaluation of a cavity package can be both an advantage and a disadvantage. The advantage is the availability of non-destructive standard tests such as the helium leak test to ensure package protection against moisture and corrosive gas for high reliability applications. Due to the lack of a cavity in plastic-encapsulated packages and higher encapsulant permeability, standard hermeticity tests on plastic packages are neither feasible nor applicable. Other tests have been devised to assess the reliability of the plastic packages exposed to moisture such as highly accelerated temperature/humidity stress test or temperature humidity bias testing, but they are destructive in nature and can be used on a sampling basis for quality assurance of the plastic-encapsulated microelectronics (PEMs) batch.

Hermeticity testing of cavity packages has several disadvantages. The helium leak detection method requires an expensive test setup (equipment can cost about $15,000). Also, the leak rate must be greater than 10^{-12} cm^3/sec to be detected. For small cavity packages such as MEMS (10^{-5} cm^3) this limitation can lead to poor resolution measurements [52,53]. Other issues with the helium leak test include the narrow test range, low detection efficiency, and the failure to detect large leaks due to large porosities [54].

Other methods used for hermeticity evaluation include Fourier transform infrared (FTIR) spectroscopy, quality factor (Q factor) measurement, and calcium layer resistance measurement. In the FTIR spectroscopy method, the package is bombed with a gas such as nitrous oxide and the gas pressure variations inside the package are measured using FTIR spectroscopy [55]. The disadvantages of this method are that the package has to be transparent to IR and that the gas inside the

Petitioner Samsung Ex-1055, 0054

package prior to hermetic sealing and bombing must be controlled for accurate measurements. The package geometry may also cause interferences [53].

The Q factor measurement method is based on the Q factor of a resonator encapsulated inside the package. A well designed and fabricated MEMS resonator has a high Q factor in vacuum, but the Q factor degrades with increasing pressure [53]. This method is very sensitive, but it has several disadvantages including sensor drift based measurement limitation because of material instabilities, unreliable determination of small pressure changes, and calibration difficulties [52].

The calcium layer resistance measurement method is based on the reactivity of calcium to oxygen and water [53]. The electrical resistance of the calcium layer increases upon exposure to the oxygen and water that has passed through the leaks. The main disadvantage of this method is that the calcium layer has to be prepared under a controlled atmosphere, because it is highly reactive even at ambient temperature.

1.6.5 Reliability

The reliability of PEMs, which was traditionally a major concern, has increased tremendously since the 1970s, due largely to improved encapsulating materials, die passivation, and manufacturing processes. In particular, modern encapsulating materials now have lower ionic impurities, better adhesion to other encapsulation materials, a higher glass transition temperature, higher thermal conductivity, and better matching of the coefficients of thermal expansion to the lead-frame. Advances in passivation include better die adhesion, fewer pinholes or cracks, low ionic impurity, low moisture absorption, and thermal properties well matched to the substrate. The failure rate of plastic packages has decreased from about 100 per million device hours in 1978 to about 0.05 per million device hours in 1990 [56]. Industry data comparing hermetic and plastic microcircuits on standard reliability tests have generally shown PEMs to be equivalent to hermetic parts [57].

Table 1.4 summarizes the results of three studies comparing the reliability of plastic and hermetic packages. A study by Rockwell International, Collins Group [58], compared PDIPs and plastic surface-mounted devices to CERDIPs in conditions simulating a worst-case avionics environment. The large difference in failure rates, shown in Table 1.4, is due to the loss of hermeticity of glass seals. The failure mechanism for both plastic and hermetic parts was metallization damage due to moisture. The parts for the

Petitioner Samsung Ex-1055, 0055

Table 1.4 Thermo-mechanical Reliability [58–60]

Study	Package	Number Failed/ Number Tested	Failure Rate	Comments
Grigg (Rockwell, Collins)	Plastic	1/2,920	0.0016%/1,000 hrs	0.034% defective
	Hermetic	2/1,200	0.0061%/1,000 hrs	0.167% defective
Lidback (Motorola SPS)	Plastic	11/133,747	0.083%/1,000 cycles	0.008% defective
	Hermetic	46/46,473	0.099%/1,000 cycles	0.099% defective
Villalobos (Motorola TED)	Plastic	23/9,177	0.44%/1,000 cycles	0.25% defective
	Hermetic	7/1,844	0.38%/1,000 cycles	0.38% defective

study were obtained from five different vendors (Texas Instruments, Motorola, National, Signetics, and Fairchild). The results of the other two studies (thermal cycling) listed in Table 1.4 also show that the failure rates of plastic packages are comparable to those of the hermetic equivalents [59,60].

The automotive industry uses some of the commercial industries' most stringent qualification standards with zero allowable rejects. The tests include temperature cycling, thermal shock, humidity, life testing, high-temperature reverse bias, intermittent operational life testing, and autoclave (live steam). Plastic parts from most vendors pass these tests without problems, indicating a broad, industry-wide ability to meet automotive standards [61]. In general, PEMs lend themselves well to automatic assembly techniques, which eliminate manual handling and operator error, resulting in high yields and low assembly costs. On the other hand, even for high-volume production of hermetic packages, automated assembly pick-and-place machines have been known to crack hermetic seals or chip ceramic packages.

Plastic-encapsulated packages have shown significant improvement in reliability and in some studies, as depicted in Table 1.4, even comparable reliability to their hermetic counterparts. Hermetic packages continue to

Petitioner Samsung Ex-1055, 0056

be highly reliable packages because of their specific design to seal against moisture and corrosive gases, therefore, eliminating associated reliability problems. However, the effectiveness of the hermetic package design relies heavily on the quality and reliability of the seal. For applications that are highly sensitive to moisture and gases, hermetic packages with high quality seals, continue to be used for maximum reliability.

1.6.6 Availability

Plastic devices are assembled and packaged on continuous production lines, as opposed to the on-demand production of hermetic parts, thus making plastic packages much more readily available than hermetic devices. This is mainly because market forces (cost and volume) encourage most designs to be developed first as plastic-encapsulated. Lead times for plastic packages are significantly shorter. The problems associated with restarting a hermetic line are absent in continuous plastic production lines.

Hermetic packages are developed only when there are perceived high-performance requirements and sufficient market interest. Thus, some parts are simply not available from major manufacturers in hermetic form. Furthermore, the US military and government, the major purchasers of hermetic parts, have become a relatively small portion of the total electronics market (less than 1% in 1995), although they accounted for nearly 80% of the total market in the 1960s. With package technology moving to surface-mount, development of ceramic packages has lagged further in the microelectronics market, making adaptation of plastic-packaged ICs to government and military applications more critical. With global competition, industrial research in materials and manufacturing processes will continue to focus on plastic packages. In 2000, over 99% of all ICs were packaged in plastic.

1.7 Summary

This chapter presented an overview to electronic packaging and plastic encapsulation. Electronic packaging consists of hermetic (ceramic or metallic) packaging or non-hermetic (plastic) encapsulation. More than 99% of microelectronic devices are plastic encapsulated.

Packaging levels and encapsulated microelectronic package types including 2D and 3D packages were discussed. 2D packages are further classified into through-hole, surface-mount, or substrate packages. 3D packages can

Petitioner Samsung Ex-1055, 0057

be stacked die, stacked packages, or folded packages. 3D packages have emerged in response to the demand for smaller, faster, and higher density electronics. They offer higher silicon efficiency and better performance compared to 2D packages.

Encapsulation methods including molding, glob-topping, underfilling, potting, and printing were outlined. One of the most commonly used encapsulant materials is epoxy molding compound. In the final section, a comparison of hermetic versus non-hermetic encapsulation was provided with respect to size, weight, performance, cost, reliability, hermeticity, and availability. Plastic packages offer the advantages of lower weight, smaller size, lower cost, better performance, higher availability, and manufacturability.

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Petitioner Samsung Ex-1055, 0058

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Petitioner Samsung Ex-1055, 0061

2 Plastic Encapsulant Materials

Encapsulant materials can be classified based on the encapsulation technologies into five major groups: molding compound, glob-top, potting, underfill, and printing encapsulation materials. Epoxies are the most common molding compound materials. Silicones, polyurethanes, and phenolics are also used as primary encapsulant materials or resins. Other materials may be added to the encapsulant, referred to as "additives," to achieve various functions and properties. The selection of the additives is influenced by the overall functions of the encapsulant product, processing techniques and conditions, cost, and availability.

A molding compound may contain over ten additives such as fillers, accelerators, flame retardants, and curing agents. Each additive has a specific function that contributes to the encapsulation process and overall performance and reliability of the encapsulated package. For instance, silica fillers used as additives in molding compounds reduce the coefficient of thermal expansion (CTE) and increase thermal conductivity of the molding compound. This will lead to lower thermal mismatch stress between the molding compound and the adjacent materials and, therefore, improve the reliability of the electronic package.

A class of encapsulant materials under active research are the environmentally friendly or "green" molding compounds. Conventional flame retardants in molding compounds are found to be toxic to the environment and, therefore, have been restricted or removed from green compounds. As a consequence, alternative non-toxic flame retardant substitutes have emerged. Furthermore, other types of green materials have been developed such as self-extinguishing molding compounds that do not require any flame retardants.

In this chapter, first an overview of the chemistry of common encapsulant materials is presented. Next, the material composition and the constituents in molding compound, glob-top, potting, underfill and printing encapsulant systems are described. Also, the material properties of commercially available encapsulant products from each category are included. Finally, environmentally friendly or "green" encapsulant materials are described.

2.1 Chemistry Overview

The chemistry of the encapsulant material directly affects its properties, processing characteristics, and performance. Epoxies, silicones,

Petitioner Samsung Ex-1055, 0062

polyurethanes, and phenolics are common polymeric materials used in the encapsulation of electronic devices.

Polymers are macromolecules consisting of long chains of smaller molecules or monomers. Polymers can be linear, branched, or cross-linked (Fig. 2.1). Thermosetting polymers such as epoxies are liquid branched polymers that form cross networks through chemical linking (cross-linking). The cross-linking process is referred to as curing or hardening process because the material is transformed from a soft and liquid form into a hardened state.

Polymerization reactions are generally categorized into two types: addition and condensation. Figure 2.2 depicts an addition (or chain reaction) process flow. In the initiation stage, the monomer (denoted by M) reacts with a highly reactive free radical (a peroxide) and forms a reactive monomer. The reactive monomer then chemically reacts with another monomer, and this addition process continues (propagation stage) until two reactive molecules find each other (by random collision) and the process terminates. Silicones can be synthesized by either addition or condensation process. In addition polymerization, the final polymer chain has the same basic chemical structure as the original monomer.



Figure 2.1 Polymers chains: (a) linear, (b) branched, and (c) cross-linked.

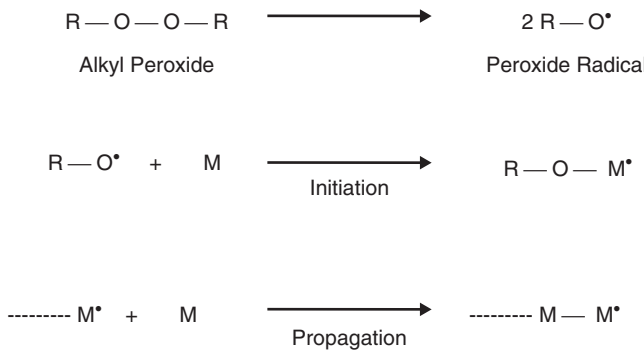


Figure 2.2 Addition polymerization process.

Petitioner Samsung Ex-1055, 0063

In the condensation process, two monomers react to form a chemically different monomer (Fig. 2.3). During this chemical reaction, a molecule from the original monomer may be eliminated and the monomer is condensed. However, in some cases, elimination does not occur such as in polyurethane polymerization. Therefore, condensation may also be referred to as "step-growth mechanism" because the common pattern in this type of polymerization is the stepwise forming of the chains [1]. The condensation process can produce either linear or cross-linked polymers depending on the functionality of the monomers. Epoxies, polyurethanes, and phenolic resins are developed by condensation.

2.1.1 Epoxies

Epoxies consist of chemical structures known as "epoxy" functionalities, as shown in Fig. 2.4. Liquid epoxies crosslink through these reactive chemical sites, and transform into hardened and insoluble solid materials.

The simplest form of epoxy material and most widely used is made from the chemical reaction of bisphenol A (BPA) and epichlorohydrin which converts to (2,2-bis [4-(2′3′ epoxy propoxy)phenyl] propane) known

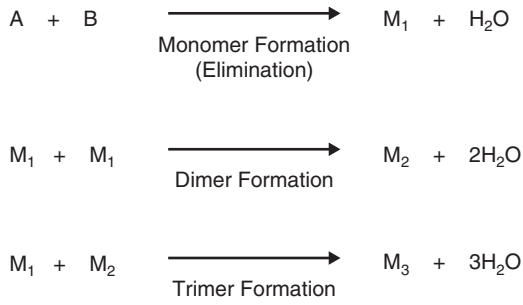


Figure 2.3 Condensation or step-growth polymerization.

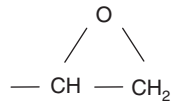


Figure 2.4 Epoxy functionality.

Petitioner Samsung Ex-1055, 0064

as diglycidyl ether of bisphenol A (DGEBA) [2,3]. Figure 2.5 shows the chemical formulation for DGEBA monomer and higher molecular weight polymer. The full representation of the benzene ring (C_6H_6) present in most encapsulant chemical formulas is shown in Fig. 2.6.

Aliphatic epoxies are another type of epoxies made by epoxidizing alcohols, glycols, and polyols (aliphatic backbones containing OH units) by reaction with epichlorohydrin [2]. Aliphatic epoxies can also be produced by peracetic acid epoxidation of polyolefinic compounds such as unsaturated animal and vegetable oils, polyesters, polyethers,

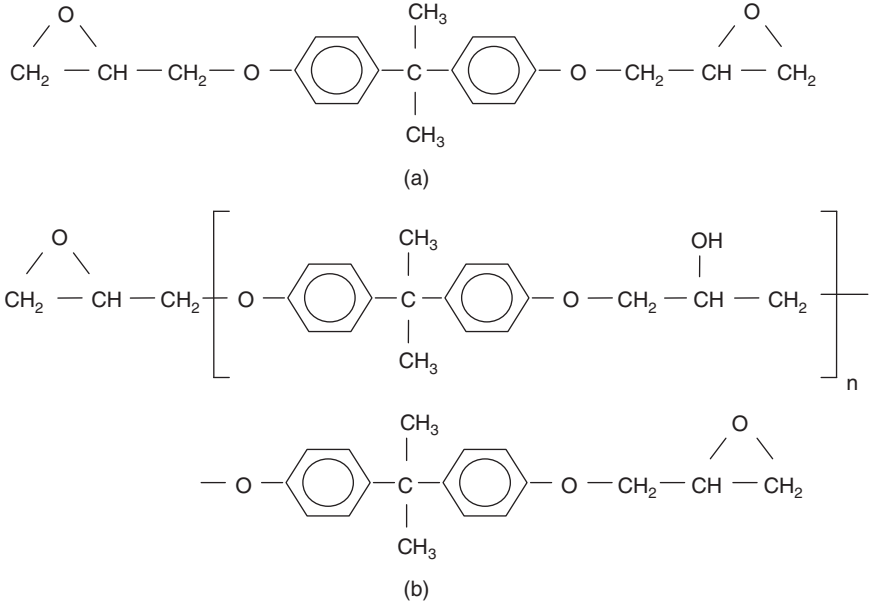


Figure 2.5 Diglycidyl ethers of bisphenol A as (a) a monomer and (b) a higher molecular weight polymer [3].

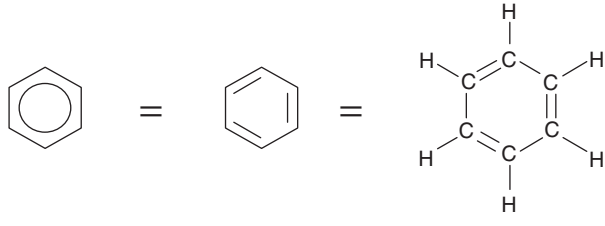


Figure 2.6 Benzene ring representations.

Petitioner Samsung Ex-1055, 0065

and butadiene derivatives. A specific type of aliphatic epoxy is cycloaliphatic resin with ultraviolet (UV) light stability and very good electrical properties. Cycloaliphatic epoxies are made by peracetic acid epoxidation of cycloaliphatic olefins.

Novolac epoxies are produced by first phenol reacting with formaldehyde and then the resulting phenol-formaldehyde resin (Novolac) reacting with epichlorohydrin [2]. The formation of epoxy novolac is shown in Fig. 2.7. A widely used novolac epoxy is ortho-epoxy cresol novolac (Fig. 2.8). Epoxy novolac resins cured with amine or anhydride curing agents generally exhibit good high temperature properties and improved chemical resistance mainly due to their high cross-link density and high aromatic structures.

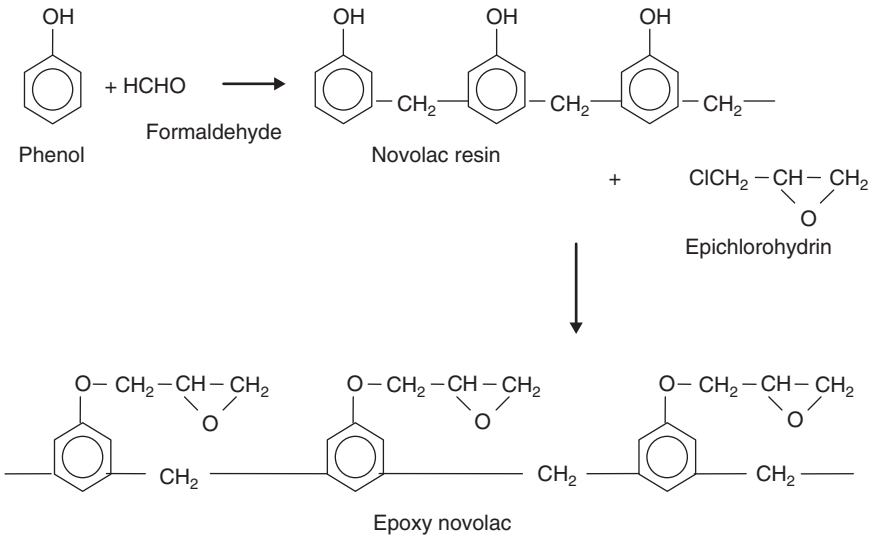


Figure 2.7 Epoxy novolac formation [4].

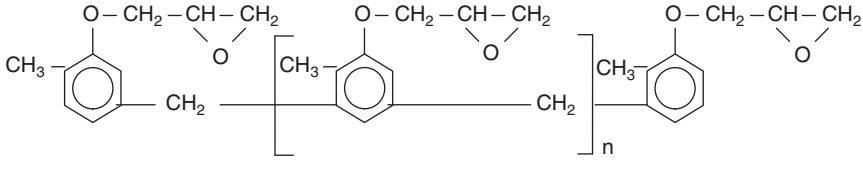


Figure 2.8 Ortho-epoxy cresol novolac [5].

Petitioner Samsung Ex-1055, 0066

2.1.2 Silicones

The name silicone was given by F.S. Kipping in 1901 to describe a new product with the formula R_2SiO as shown in Fig. 2.9, where R can be methyl (CH_3), phenyl (C_6H_5), vinyl ($CH{=}CH_2$), or trifluoropropyl ($C_3H_4F_3$). Because of the combination of organic groups (i.e., methyl, vinyl, etc.) and inorganic backbone (Si–O), silicone materials exhibit some unique properties such as both high and low temperature flexibility and stability, high electrical insulation resistance, high purity, moisture resistance, and excellent biocompatibility [3,6].

A widely used siloxane polymer is polydimethylsiloxane (PDMS) [$-Si(CH_3)_2O-$], as shown in Fig. 2.10 [3,6,7]. PDMS is formed from the hydrolysis of dimethyldichlorosilane (Di). Figure 2.11 shows the process flow for the formation of Di from the basic natural element, sand (silica) [8]. The shorthand notation M is $-Me_3SiO-$ and D is $-Me_2SiO-$.

Silicones can be polymerized by addition or condensation mechanisms. Figure 2.12 shows the condensation mechanism for moisture-cured silicones. Figure 2.13 shows the free-radical addition polymerization for dimethyl polysiloxane using a peroxide catalyst [4].

2.1.3 Polyurethanes

Polyurethanes were first synthesized in 1937 by Otto Bayer. Polyurethanes are produced from the reaction of dialcohol with diisocyanate. The

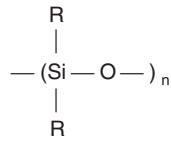


Figure 2.9 General formula of silicone.

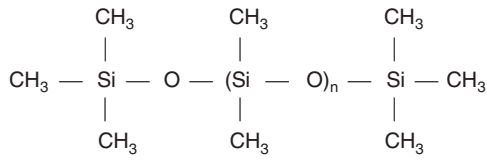


Figure 2.10 Polydimethylsiloxanes terminated with trimethylsilyloxy [3].

Petitioner Samsung Ex-1055, 0067

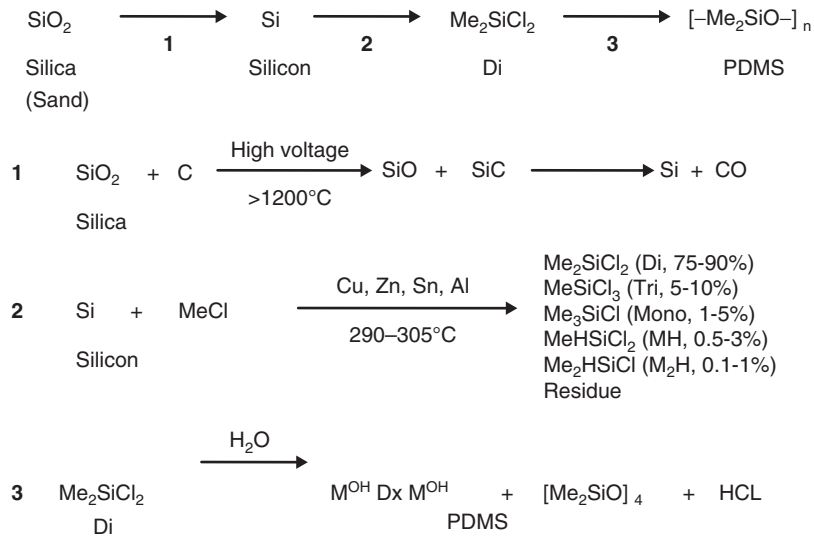


Figure 2.11 Formation of polydimethylsiloxane (PDMS) from sand [8].

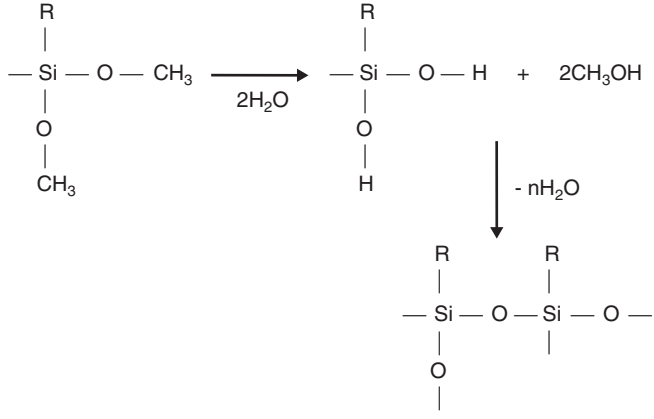


Figure 2.12 Condensation mechanism for moisture-cured silicones [4].

type of diisocyanate commonly used is tolylene (toluene) diisocyanate, which is usually synthesized from a mixture of the 2,4- and 2,6-isomers of toluene [1]. An example of an aromatic/aliphatic polyurethane formation is shown in Fig. 2.14.

Polyurethanes are classified into six types based on the classification by the American Society for Testing and Materials (ASTM D-16) [4]. The classification of polyurethanes is based on the chemistry and curing

Petitioner Samsung Ex-1055, 0068

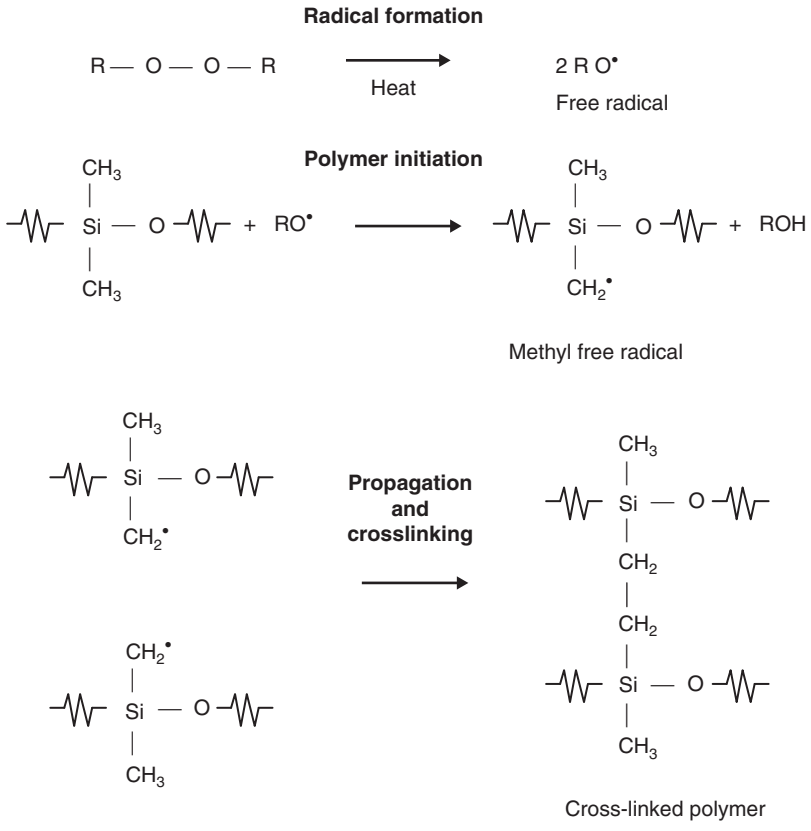


Figure 2.13 Free-radical addition polymerization for dimethyl polysiloxane with a peroxide catalyst [4].

characteristics as listed in Table 2.1. Types IV and V are two-part systems while the others are one-part systems. Types III, IV, and V are the most widely used polyurethanes in electronics encapsulation. Type III polyurethane has the unique advantage of an indefinite shelf life (storage life before expiration), as it contains blocked isocyanates that are non-reactive. Unblocking and polymerization is achieved by heating. The unblocking mechanism for Type III polyurethane is shown in Fig. 2.15.

2.1.4 Phenolics

Phenolic or "phenol-formaldehyde" resins were developed by Leo H. Baekeland in 1909 [9]. Also referred to as "bakelite," phenolic resins are formed by mixing and heating phenol (C_6H_5OH) with formaldehyde

Petitioner Samsung Ex-1055, 0069

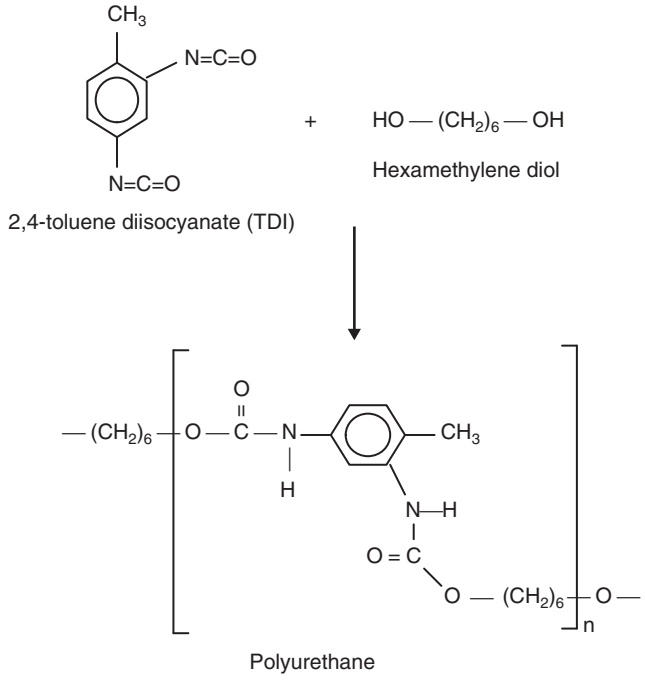


Figure 2.14 An aromatic/aliphatic polyurethane [1].

Table 2.1 Polyurethane Classifications According to ASTM [4]

Polyurethane Type	Parts	Chemistry	Curing Agent or Mechanism
Type I	1	Oil-modified urethanes	Oxidation at ambient
Type II	1	Contains free reactive isocyanate groups	Ambient moisture
Type III	1	Phenol-blocked isocyanates	Heating
Type IV	2	Part 1: Pre-polymer with free isocyanate groups Part 2: Catalyst	Catalyst
Type V	2	Part 1: Pre-polymer with free isocyanate groups Part 2: Polyol	Polyol
Type VI	1	Polymerized urethanes thinned with solvents	Solvent evaporation

Petitioner Samsung Ex-1055, 0070

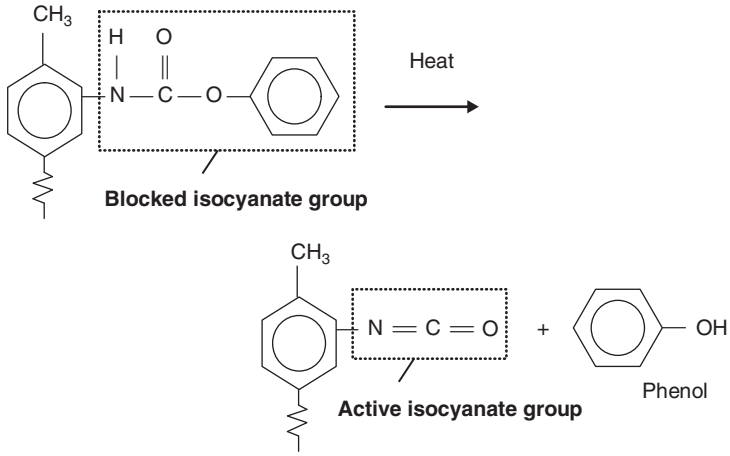


Figure 2.15 Unblocking mechanism for Type III polyurethanes [4].

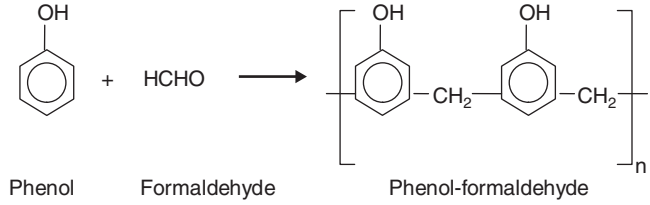


Figure 2.16 Phenolic resin.

(HCHO) (Fig. 2.16) and polymerized by condensation. Phenolic resins were the first synthetically made polymeric material, not based on any natural molecule [10].

2.2 Molding Compounds

A molding compound is a proprietary multi-component mixture of an encapsulating resin with various additives. The three main constituents in a molding compound are resins, curing agents (hardeners), and accelerators. The other additives in the molding compound include fused silica, coupling agents, flame retardants, stress-relief additives, adhesion promoters, mold-release agents, coloring agents, and ion-trapping agents. The composition of a typical epoxy molding compound is shown in Fig. 2.17. Table 2.2 lists these components and their functions in molding compounds [11].

Petitioner Samsung Ex-1055, 0071

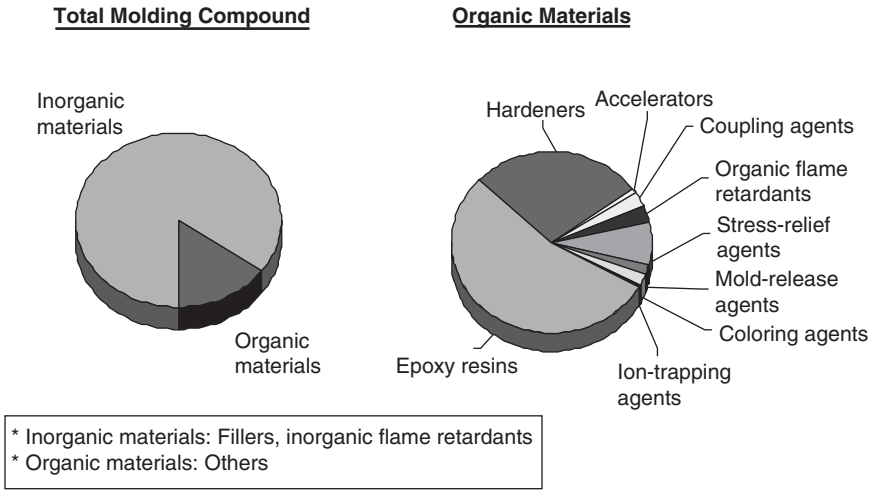


Figure 2.17 Contents of a typical epoxy molding compound by weight.

2.2.1 Resins

The earliest resin materials used for plastic packaging of microelectronic devices were silicones, phenolics, and BPA epoxies because of their excellent molding characteristics. Silicones were used as molding compound resins because of their high-temperature performance and purity. However, poor adhesion of silicones with the device and metallization resulted in device failures in salt spray tests and flux penetration during soldering. Although epoxy materials offer much better adhesion than silicones, the common epoxies (BPA) have a low glass transition temperature in the range of 100–120°C and high concentrations of corrosion agents such as chloride ions. In the formulation of epoxy-molding compounds, novolac epoxies displaced BPA materials because of their higher epoxide functionality and heat-distortion temperatures.

Integrated circuits (ICs) molded with phenolics experienced early corrosion failures caused by the generation of ammonia during post-mold curing, the presence of high levels of sodium and chloride ions, and high moisture absorption. Molding compounds have moved steadily toward all-epoxy systems as the high-temperature novolac materials were improved and the hydrolyzable impurity levels were driven below 20 ppm.

All epoxy resins contain the epoxide (also known as ethoxylene or oxirane) group, in which an oxygen atom is bonded to two adjacent (end) carbon atoms. Because the resins are cross-linkable (thermosetting) each

Petitioner Samsung Ex-1055, 0072

Table 2.2 Contents of Epoxy Molding Compounds [12]

Component	Concentration (phr)	Major Function	Typical Agents
Epoxy resins	Matrix	Matrix for mold compound	Epoxy cresol novolac, biphenyl, dicyclopentadiene, multifunctional
Curing agents (hardeners)	Up to 70	Linear/cross polymerization	Polyphenol, amine, acid anhydride
Accelerators	Very low (<3)	Enhance rate of polymerization, reduce cycle and cure time	Amines, imidazole, organophosphine, urea, Lewis acids and their organic salts
Inert fillers	550–1,200	Reduce cost, decrease CTE, increase TC, reduce moisture absorption, reduce resin bleed	Silica (widely used), aluminum nitride, alumina
Coupling agents	Very low (<5)	Improve adhesion between organic and inorganic materials	Epoxy silanes, amino silane, titanate, aluminum chelate
Flame retardants	10	Retard flammability	Brominated epoxy, antimony oxide, phosphate ester, solid phosphate, aluminum trihydrate
Stress-relief agents	Up to 25	Reduce stress in package, improve toughness, provide thermal shock and impact protection	Silicone, butyl rubber, aliphatic epoxide, polybutyl acrylate
Mold-release agents	Very low (<3)	Aid in release of package from mold	Stearic acid, natural wax, synthetic wax
Coloring agents	5	Reduce photonic activity, reduce device visibility	Carbon black

CTE: Coefficient of thermal expansion; phr: Parts per hundred epoxy resin; TC: Thermal conductivity.

Petitioner Samsung Ex-1055, 0073

resin molecule must have two or more epoxy groups. Most commonly, the epoxide group is attached linearly to a chain of $–CH_2–$ and is called a glycidyl group. This group is attached to the rest of the resin molecule by an oxygen, nitrogen, or carboxyl linkage forming a glycidyl ether, amine, or ester. The resin is cured by the reaction of the epoxide group with compounds containing a plurality of reactive hydrogen atoms (curing agents) such as primary, secondary, or tertiary amines, carboxylic acid, and mercaptan. Catalytic cures are affected by Lewis acids, Lewis bases, or metal salts, resulting in the linear homopolymerization of the epoxide group forming polyether linkages. The viscosity of the base resin for the encapsulant grade materials is kept low by limiting the average degree of polymerization of the novolac epoxy to values around 5. Commercial formulations differ primarily in the distribution of the degree of polymerization, with an average molecular weight of about 900. Longer and shorter chain lengths provide looser or tighter cross-link structures, with varying ductility and glass transition temperatures.

In electrical and electronic applications, three types of epoxy resins are commonly used: the diglycidyl ethers of bisphenol A (DGEBA) or bisphenol F (DGEBF), the phenolic and cresol novolacs, and the cycloaliphatic epoxides. Liquid DGEBAs are synthesized from petrochemical derivatives. They are readily adaptable for electrical and electronic device encapsulation. DGEBF is less viscous than DGEBA. The epoxy cresol novolacs, essentially synthesized in the same way as DGEBA, are primarily solids. Because of their relatively superior elevated-temperature performance, the epoxy cresol novolacs are the most commonly used molding compounds for plastic-encapsulated microelectronics (PEMs). The cycloaliphatic epoxides or peracid epoxides, usually cured with dicarboxylic acid anhydrides, offer excellent electrical properties and resistance to environmental exposure.

In the transition to thin quad flat packages, where the encapsulation is relatively thinner and covers a larger area, further improvements in the encapsulant material were necessary to withstand the manufacturing and package reliability requirements. Multifunctional and biphenyl epoxy resins have been developed to address the need. The multifunctional epoxy resin shows very low shrinkage, low stress, and high glass transition temperature (>170°C). Biphenyl resin is composed of 80% biphenyl and 20% novolac resin. Biphenyl resins exhibit high strength, low stress, and low moisture absorption. These two types of epoxy resins are primarily used for surface-mount packages.

Epoxy encapsulating resins have been synthesized with improved popcorn resistance (during reflow soldering in printed wiring assembly).

Petitioner Samsung Ex-1055, 0074

Factors contributing to popcorn resistance are moisture diffusion, adhesion, curing shrinkage, physical strength at elevated temperatures, and package toughness [13]. These factors are addressed by modifying molding compound chemistry and composition. For example, certain types of popcorn-resistant compounds exhibit almost no shrinkage while curing, while other types have improved adhesion strength. These improved compounds result in PEMs that routinely survive solder immersion shock tests without failure. Table 2.3 gives the mechanical and electrical properties of selected epoxy resins. Table 2.4 lists the advantages and disadvantages of commonly used polymeric materials used in PEMs.

2.2.2 Curing Agents or Hardeners

The binder system of a plastic encapsulant product consists of an epoxy resin, hardener or curing agent, and (if necessary) an accelerating catalyst. The conversion of epoxies from the liquid (thermoplastic) state to tough, hard thermoset solids is accomplished by the addition of chemically active compounds known as hardeners. Epoxidized phenol novolac and epoxidized cresol novolac are most often used. The composition of the resin and the hardener system, therefore, is optimized for the specific application. For example, phenol novolacs can be incorporated in the matrix resin to increase cure speed. In general, the glass transition curing temperature is maximized at an epoxide to hydroxyl ratio of about one.

Hardeners and accelerators perform the primary function of setting the extent and rate of polymerization of the resin. Consequently, the selection of the agent and cure chemistry is as important as the choice of resin. Often, the same agent is used for both cure and acceleration. The cross-linking reactions of epoxy resins are affected by aliphatic or aromatic amines, carboxylic or its derivative acid anhydrides, and complex phenols, whereas homopolymerization is affected by Lewis acids or bases and their organic salts. The most widely used hardeners are amines and acid anhydrides. While aliphatic amines react rapidly at room temperature, aromatic amine hardeners impart higher thermal stability and improved chemical resistance. Depending on the hardener used, the reactions proceed through different chemistries. Because this reaction is virtually quantitative, the resin and curing agent are mixed in the ratio of one amino hydrogen to one epoxide. In the case of anhydrides and phenols as curatives, cross-linking occurs through the hydroxyl groups. Table 2.5 lists the curing properties of different classes of curatives used

Petitioner Samsung Ex-1055, 0075

Table 2.3 Mechanical and Electrical Properties of Selected Epoxy Resins

Curing Agent Type	Anhydride	Aliphatic Amine	Aromatic Amine	Catalytic	High-Temperature Anhydride	Epoxy Novolac Anhydride	Dianhydride
Typical curing agents	HHPA	DETA	MPDA	BF_3-MEA	NMA	NMA	PMDA
Parts	78	12	14	3	90	87.5	55
Resin	DGEBA	DGEBA	DGEBA	DGEBA	DGEBA	Novolac	DGEBA
Catalyst type/phr	BDMA/1	–	–	–	BDMA/1	BDMA/1.5	–
Cure cycle (hrs/°C)	4/150	24/25 + 2/200	2/80 + 2/200	2/120 + 2/200	4/150 + 3/200	2/90 + 4/165 + 16/200	4/150 + 14/200
Heat deflection temperature (°C)	130	125	150	174	170	195	280
Tensile strength (MPa)							
at 25°C	72	75	85	43	75	66	22
at 100°C	37	32	45	29	46	–	14
Tensile modulus (GPa)							
at 25°C	2.80	2.87	3.30	2.70	3.40	2.94	2.70
at 100°C	2.10	1.80	2.20	1.90	1.40	–	–
Elongation (%)							
at 25°C	5.6	6.3	5.1	3.0	2.7	3.2	–
at 100°C	11.1	9.0	7.2	9.1	7.2	–	–
Flexural strength (MPa) at 25°C	126	103	131	112	112	147	59

(*Continued*)

Petitioner Samsung Ex-1055, 0076

Table 2.3 Mechanical and Electrical Properties of Selected Epoxy Resins (*Continued*)

Curing Agent Type	Anhydride	Aliphatic Amine	Aromatic Amine	Catalytic	High-Temperature Anhydride	Epoxy Novolac Anhydride	Dianhydride
Flexural modulus (GPa) at 25°C	3.22	2.48	2.80	–	4.80	3.69	3.61
Compressive strength (MPa) at 25°C	111	224	234	–	116	159	254
Compressive modulus (GPa) at 25°C	5.09	1.89	2.13	–	0.73	2.22	2.41
Volume resistivity (ohm cm)							
at 25°C	4×10^{14}	2×10^{16}	1×10^{16}	–	2×10^{14}	10^{16}	–
at 100°C	2×10^{14}	5×10^{12}	–	–	3×10^{12}	–	–
at 150°C	1×10^{10}	–	–	–	3×10^{11}	–	–
at 200°C	5×10^{7}	–	–	–	1×10^{9}	–	7×10^{11}
Dielectric constant, 60 Hz							
at 25°C	3.3	3.49	4.60	3.53	3.36	3.43	3.57
at 100°C	3.3	4.55	4.65	3.51	3.39	–	3.70
at 150°C	–	5.8	5.40	3.69	3.72	–	3.732
Dielectric constant, 1 kHz							
at 25°C	3.2	3.26	4.50	4.50	3.26	3.45	3.52
at 100°C	3.4	4.65	4.60	4.60	3.01	–	3.65
at 150°C	4.0	4.83	4.90	4.90	3.29	–	3.70

Petitioner Samsung Ex-1055, 0077

Dielectric constant, 1 MHz								
at 25°C	3.2	3.33	3.85	3.20	2.99	3.20	3.2	
at 100°C	3.4	4.36	4.30	3.25	3.90	–	3.4	
at 150°C	3.6	4.23	4.60	3.30	3.29	–	4.0	
Dissipation factor, 60 Hz								
at 25°C	0.005	0.005	0.008	0.008	0.008	0.0066	0.007	
at 100°C	0.003	0.002	0.008	0.008	0.009	–	0.005	
at 150°C	0.003	0.003	–	–	0.009	–	0.008	
Dissipation factor, 1 kHz								
at 25°C	0.007	0.006	0.017	0.009	0.006	0.0058	0.008	
at 100°C	0.004	0.056	0.006	0.011	0.003	–	0.004	
at 150°C	0.07	0.048	0.035	0.046	0.039	–	0.004	
Dissipation factor, 1 MHz								
at 25°C	0.013	0.034	0.038	0.024	0.021	0.016	0.022	
at 100°C	0.015	0.048	0.02	0.015	0.013	–	0.019	
at 150°C	0.02	0.033	0.015	0.012	0.013	–	0.013	

BDMA: Benzyldimethylamine; BF_3-MEA: Boron trifluoride-monoethylamine; DETA: Diethylenetriamine; DGEBA: Diglycidyl ether of bisphenol A; HHPA: Hexahydrophthalic anhydride; MPDA: Meta-phenylene diamine; NMA: Nadic methyl anhydride; PMDA: Pyromellitic dianhydride.

Petitioner Samsung Ex-1055, 0078

Table 2.4 Properties of Common Polymeric Encapsulants for Microelectronic Packages

Polymeric Material	Advantages	Disadvantages
Epoxies	• Good chemical and mechanical protection • Low moisture absorption • Suitable for all thermosetting processing methods • Excellent wetting characteristics • Ability to cure at atmospheric pressure • Excellent adhesion to a wide variety of substrates under many environmental conditions • Thermal stability up to 200°C	• High stress • Moisture sensitivity • Short shelf life (can be extended under low temperature storage conditions)
Silicones	• Low stresses • Excellent electrical properties • Good chemical resistance • Low water absorption • Thermal stability up to 315°C • Good UV resistance	• Low tensile tear strength • High cost • Attacked by halogenated solvents • Poor adhesion • Long cure time
Polyurethanes	• Good mechanical properties (toughness, flexibility, resistance to abrasion) • Low viscosity • Low moisture absorption • Ambient curing possible • Thermal stability up to 135°C • Low cost	• Poor thermal stability • Poor weatherability • Flammable • Dark color • High ionic concentration
Phenolics	• High strength • Good moldability and dimensional stability • Good adhesion • High resistivity • Thermal stability up to 260°C • Low cost	• High shrinkage • Poor electrical properties • High cure temperature • Dark color • High ionic concentration

Petitioner Samsung Ex-1055, 0079

Table 2.5 Curing Properties of Pure DGEBA Epoxy Resin Curing Agents Used in Molding Compounds [11]

Curative Type	Concentration Range (Parts/100 Parts of Resin)	Typical Cure		Typical Post-cure		Pot Life at 25°C (hrs)	Heat Deflection Temperature (°C)
		Time	Temp. (°C)	Time (hrs)	Temp. (°C)		
Aliphatic tertiary amines and derivatives (room temperature cure)	12–50	4–7 days	25	0–1	150–200	0.25–3	55–124
Cycloaliphatic amines (moderate temperature cure)	4–29	0.5–8 hrs	60–150	0–3	150	0.25–20	100–160
Aromatic amines (elevated temperature cure)[a]	14–30	4 hrs	80–200	2	150–200	5–8	145–175
Carboxylic and anhydrides (elevated temperature cure)[a]	78–134	2–5 hrs	25–150	3–4	150–200	24–120	74–197
Lewis acids and bases (elevated temperature cure)[a]	3	7 hrs	120–200	4	~200	>250	175
Latent curing agents (elevated temperature cure)	6	1 hr	175	1	175		135

[a]Two-step cure.
DGEBA: Diglycidyl ether of bisphenol A.

Petitioner Samsung Ex-1055, 0080

with epoxy resins. Because of their excellent moldability, electrical properties, and heat and humidity resistance [14], phenol novolac and cresol novolac hardeners have become the dominant curatives for microelectronic packaging.

2.2.3 Accelerators

To promote cure within a reasonable period of time, it is often necessary to use accelerators. Accelerators reduce the in-mold cure time and improve productivity by catalytic activity. Typical accelerators include aliphatic poylamines or tertiary amines, phenols, nonyl phenol, resorcinol, or semi-inorganic-derived accelerators such as triphenyl phosphite.

For transfer molding of microelectronic devices epoxy resins are B-staged (partially cured) to produce storage-stable thermosetting epoxy slugs known as prepregs. The B-staged resin is formed by reacting terminal epoxides with aminohydrazides at 70–80°C to yield B-staged resins with excellent storage stability.

2.2.4 Fillers

Fillers are employed in epoxy resins for a variety of reasons. ASTM D-883 defines a filler as "a relatively inert material added to a plastic to modify its strength, performance, working properties, or other qualities or to lower costs." Epoxy resins cannot be used alone for encapsulants due to their high CTE and low thermal conductivity. Thus, inert inorganic fillers are added to the molding compound to lower its CTE, increase thermal conductivity, raise the elastic modulus, prevent resin bleed at the molding tool parting line, and reduce encapsulant shrinkage during cure (and thus, reduce residual thermomechanical stress). Microstructurally, particle shape, size, and distribution in the chosen filler dictate the rheology of the molten epoxy molding compound. The advantages and disadvantages of using fillers are given in Table 2.6. Typical fillers and their properties are given in Table 2.7.

Historically, fillers with the optimum combination of required properties were crystalline silica or alpha quartz. Crystalline silica fillers have a thermal conductivity of 14 W/m K and a CTE of 15 ppm/°C. For example, an epoxy resin with a CTE of about 78 ppm/°C, loaded to 84% by weight with crystalline silica fillers, exhibits a reduced CTE of 25 ppm/°C for the filled molding compound. Crystalline silica was replaced by ground fused silica, which provided lower CTE, density, and viscosity. A formulation

Petitioner Samsung Ex-1055, 0081

Table 2.6 Advantages and Disadvantages of using fillers [15]

Advantages	Disadvantages
• Reduced formulation cost • Reduced shrinkage • Improved toughness • Improved abrasion resistance • Reduced water absorption • Increased heat deflection temperature • Decreased exotherm • Increased thermal conductivity • Reduced thermal expansion coefficient	• Increased weight • Increased viscosity • Machining difficulties • Increased dielectric constant

Table 2.7 Typical Fillers and Their Characteristic Properties [16,17]

Property	Fused Silica	Cryst. Silica	AlN	Al_2O_3	BN	SiC	Si_3N_4
Thermal conductivity (W/m K)	1.3	14	130–260	20–25	20	90–270	30
CTE (ppm/°C)	0.5	15	4.4	6.7–7.1	0	3.7	3.0
Electrical resistance (ohm cm)	$10^{14–18}$	10^{14}	10^{14}	10^{13}	10^{11}	$>10^{13}$	$>10^{14}$
Dielectric constant (RT, 1 MHz)	3.9	3.8–5.4	8.7–8.9	8.9	4.1	40	8.0
Density (g/cm^3)	2.2	2.64	3.26	3.89	1.90	3.21	3.20
Young's modulus (GPa)	73	310	331	345	43	407	310
Vicker hardness (GPa)	6	9–11	12	20	<3	30	15

CTE: Coefficient of thermal expansion; RT: Room temperature.

Petitioner Samsung Ex-1055, 0082

with a similar type of epoxy resin (i.e., CTE of 78 ppm/°C) requires only 68% by weight of fused silica fillers to produce the same CTE reduction (i.e., 25 ppm/°C).

The addition of particulate fillers generally reduces strength characteristics such as tensile strength and flexural strength. Fillers do not usually provide any significant enhancement of glass transition temperature, or other measures of heat distortion temperatures. Fillers allow the possibility of modifying various thermal characteristics including the thermal conductivity and thermal expansion coefficient. Thermal conductivity can be increased by a factor of about five by the addition of fillers such as alumina. Generally, an increase in filler content increases thermal conductivity. Figure 2.18 shows data on the effect of filler content on thermal conductivity. Thermal conductivity can also be enhanced by the addition of other filler materials such as aluminum nitride (AlN), silicon carbide, magnesium oxide, and silicon nitride [18]. Thermal conductivity as high as 4.5 W/m K has been achieved by using biphenyl resin and AlN powder. But AlN is thermodynamically unstable against environmental factors such as air and humidity, so silica-coated AlN (SCAN) was developed by Dow Chemical Company to overcome the hydrolytic instability of AlN [19].

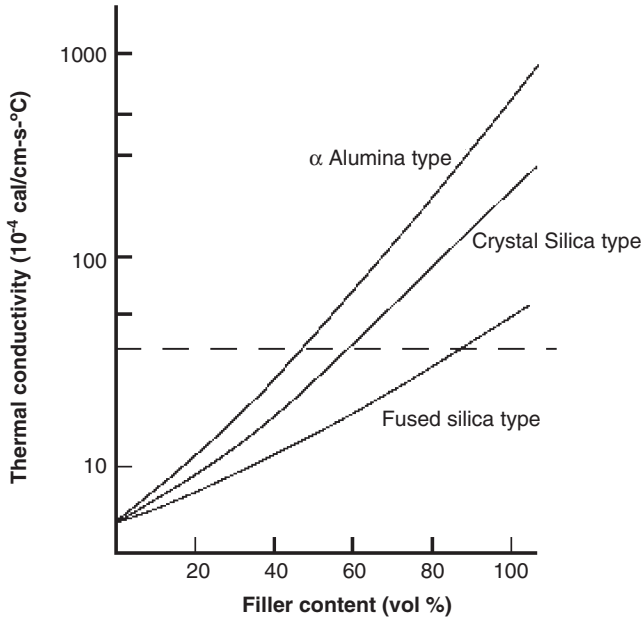


Figure 2.18 Relationship between filler content and thermal conductivity of the molding compound [18].

Petitioner Samsung Ex-1055, 0083

Although fillers are effective to increase thermal conductivity, Proctor and Solc [20] have shown the futility of using filler materials to produce thermal conductivity of more than 100 times that of the base resin. They estimated that a practical maximum limit for thermal conductivity improvement is about 12 times that of the thermoset resin.

Rosler evaluated various fillers for optimizing the CTE and the thermal conductivity for specific applications [18]. Figure 2.19 presents the effect of lowering the CTE of the molding compound as a function of the crystalline silica, alpha-alumina, and fused silica volume percentage.

Variables such as particle size, particle size distribution, particle surface chemistry, and particulate volume fraction have been found to be the most important variables necessary for property enhancement. Increasing the quantity of fillers contributes to lowering CTE and increasing thermal conductivity, but high loading also causes an increase in viscosity and decrease in flowability. A broader distribution of particles can result in decreased viscosity of the resin compound.

The addition of the fine particles can significantly increase the spiral flow of the molding compound up to a certain level. The fine particles loaded into the small spaces between large-sized particles seem to have a

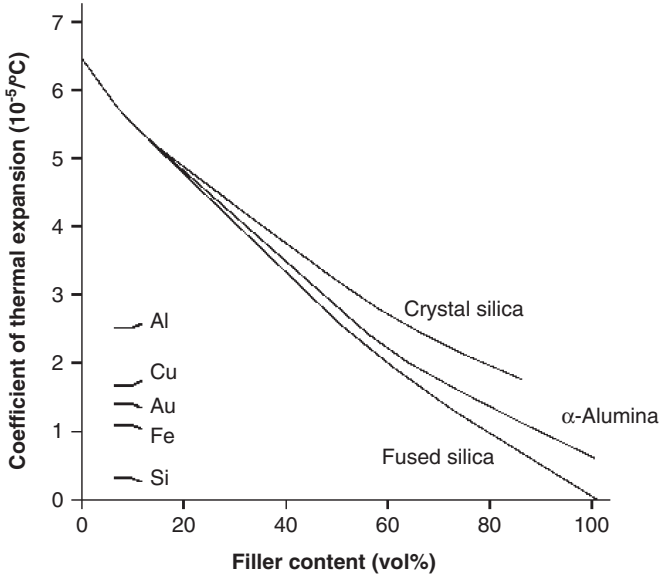


Figure 2.19 Effect of lowering the coefficient of thermal expansion of the molding compound as a function of the crystalline silica, alpha-alumina, and fused silica volume percentage.

Petitioner Samsung Ex-1055, 0084

lubricant effect by limiting the friction between fillers; however, the fine particles have large surface area and extremely large amounts of fine particles decrease the spiral flow. The lubricant effect also depends on the shape of the ultra-fine particles. The better the sphericity of the particles, the larger the spiral flow length of the molding compounds. So maximal filler loading can be achieved without increasing viscosity by adopting fillers with ultra-fine particles, good sphericity, and broad size distribution [21].

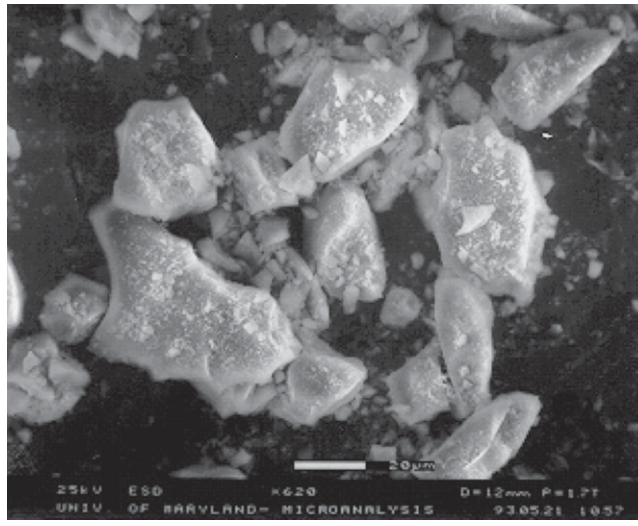
In low-stress epoxy resins, spherical silica particles are usually blended with crushed silica to further lower the CTE, by increasing filler loading with a non-linear increase of viscosity. The lower CTE leads to lower thermal mismatch stresses between the encapsulant and the adjacent materials. However, an increase in the melt viscosity of the molding compound can increase void density and increase the difficulty of achieving a uniform encapsulant flow over large areas.

Figure 2.20 shows a scanning electron micrograph of the particle size distribution of a typical spherical fused-silica additive used in the fused-silica filler stock. The effect of the filler figure ratio (angular:spherical), as measured by the molding compound's spiral flow length for two volume-percentages filler loadings, is shown in Fig. 2.21. However, as Fig. 2.22 shows, the moisture ingress susceptibility of the molding compound, as measured by the "popcorn" effect during 215°C, 90-second vapor phase soldering, increases with higher percentages of spherical silica filler.

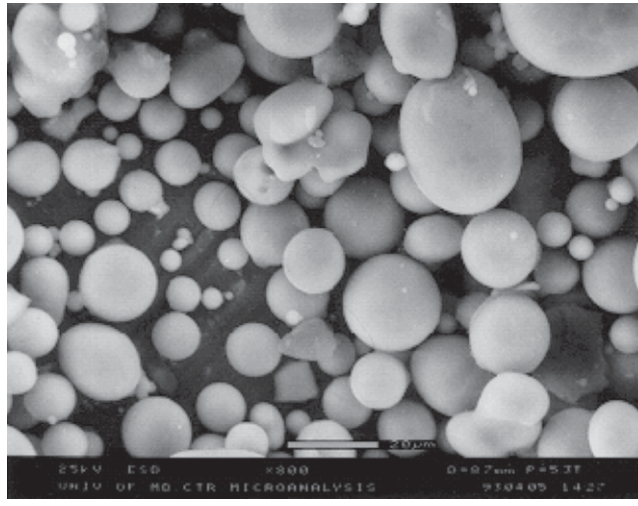
The characteristics of filler materials also greatly influence wire sweep. An increase in filler content results in greater wire sweep. Wire sweep can be reduced with the use of spherical fillers, which have a smaller surface area than ragged fillers. Molding compounds with spherical fillers will have a lower viscosity than compounds with an equal weight percentage of ragged fillers and, therefore, exert a lower viscous drag force on the wires. Spherical fillers provide a statistically significant decrease in wire sweep with an increase in average filler size. As the filler particle size increases, the surface area decreases for a given weight percentage of filler [22].

The influence of varying the thermal conductivity of the epoxy molding compound on the thermal performance of the IC package has also been evaluated [23]. In this case, by varying the filler types (e.g., fused and crystalline silica, aluminum oxide, aluminum and boron nitride, silicon carbide, and diamond), the particle sizes, and the filler size distribution, the thermal conductivities of the composites were estimated. The resulting effectiveness in dissipating heat away from the package was computed for three different surface-mount packages, namely SOIC 8-lead, 16-lead wide, and 24-lead wide. The results indicated that an enhanced molding

Petitioner Samsung Ex-1055, 0085



(a)



(b)

Figure 2.20 Micrograph of (a) typical ground angular fused silica and (b) spherical fused silica filler used in mixing with ground angular fused silica in molding compound. (Courtesy of Minco Inc., TN.)

compound can cause a decrease in thermal resistance of the package equivalent to what can be achieved with a molded-in heat spreader. However, when thermally enhanced lead-frames are used, the effect of the modified compounds is less significant.

Petitioner Samsung Ex-1055, 0086

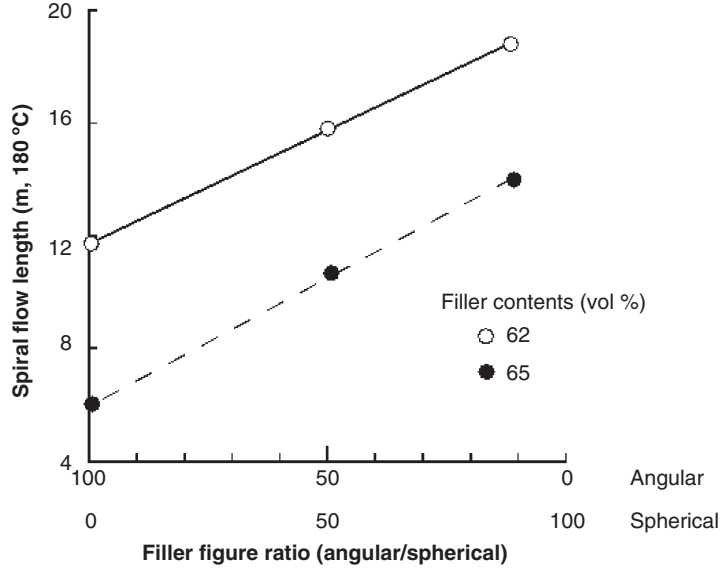


Figure 2.21 The effect of the filler figure ratio (angular:spherical) as measured by the molding compound's spiral flow length for two volume-percentages filler loadings.

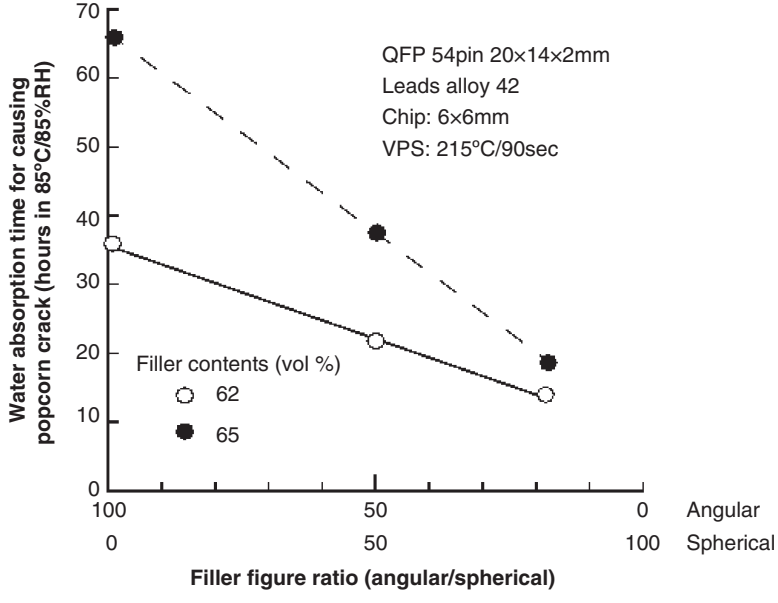


Figure 2.22 Moisture ingress susceptibility of the mold compound as measured by the popcorn effect.

Petitioner Samsung Ex-1055, 0087

Most polymers undergo shrinkage during the polymerization and cross-linking process, which can be damaging in many applications. Incorporation of fillers reduces shrinkage by simple bulk replacement of resin with an inert compound that does not participate in the cross-linking process. Filler addition results in increased viscosity and improved toughness. Investigations have shown that the incorporation of particulate fillers such as silica, glass microspheres, and alumina trihydrate can increase the toughness of various epoxy formulations [24–27].

The main source of radiation in plastic packages comes from fillers. However, the use of synthetic high-purity silica fillers in recent years has brought down the alpha emission rates (AERs) of molding compounds below the detection level of most proportional counters. Ditali and Hasnain [28] studied AER sources in an electronic part and developed Table 2.8, which shows that outside the major alpha-source contamination of the die itself, the lead-frame material is more contaminated (per unit surface area) than the plastic encapsulant, and ceramic package materials are more alpha-emitting than plastic encapsulants.

An approximate conversion factor of AER to soft-error rate is 0.001. AER is defined as 0.1% SEU (single event upset) per thousand operating hours for the contaminated material in contact with the die active surface and alpha-particle energies in the range of 4–6 MeV. An AER of about 0.001 can be obtained from 10 ppb of U-238 (4.2 MeV alpha) or 4 ppb of Th-230 (4.7 MeV alpha).

2.2.5 Coupling Agents

The adhesion between the filler and the polymer must be strong for the filler to be effective. The filler-polymer interface is not stress-bearing and it presents a position of mechanical weakness. Coupling agents are used to increase the adhesion between fillers and polymers by linking them with covalent bonds [29]. Commonly used coupling agents include silanes, titanates, aluminum chelates, and zircoaluminates. Interfacial adhesion enhances mechanical strength and improves processability. The adhesion of fillers to the polymer matrix through coupling agents also extends to the device and lead-frame, reducing delamination failure.

2.2.6 Stress-Relief Additives

The toughness and stress-relaxation response of the epoxy resins can be enhanced by the addition of flexibilizers and stress-relief agents.

Petitioner Samsung Ex-1055, 0088

Table 2.8 Alpha Emission Rate (AER) of Various Processing Films, Lead-Frames, and Packaging Materials [28]

Substance (alpha/cm^2/hr)	AER
Die	
Bare silicon (Si)	0.00020
Si + CVD oxide (TEOS)	0.00164
Si + plasma oxide	0.00188
Si + plasma nitride	0.00443
Si + tungsten	0.00308
Si + aluminum	0.00682
Si + polysilicon	0.00098
Si + field oxide	< 0.00010
Si + BPSG	< 0.00010
Si + CVD nitride	< 0.00010
Fully processed without WSi_x	0.02400
Fully processed with WSi_x	0.04230
Die coat (polyimide)	< 0.00010
Lead-frames	
1 Meg DIP	0.00677
1 Meg ZIP	0.00258
256 K DIP	0.00124
64 K DIP	0.00109
Packaging material	
Plastic	0.00080
Ceramic DIP (vendor A)	0.02320
Ceramic LCC (vendor A)	0.02530
Ceramic DIP (vendor B)	0.03230
Ceramic DIP (vendor C)	0.02610

BPSG: Borophosphosilicate glass; CVD: Chemical vapor deposition; DIP: Dual in-line package; LCC: Leaded chip carrier; TEOS: Tetraethyl orthosilicate; ZIP: Zig-zag in-line package.

Stress-relief additives lower the thermomechanical shrinkage stresses that can initiate as well as propagate cracks in the molding compound or in the device passivation layer. In terms of molding compound property modification, stress-relief agents lower the elastic modulus, improve toughness and flexibility, and lower the CTEs.

Inert flexibilizers, such as phthalic acid esters or chlorinated biphenyls, remain as a separate phase. Reactive flexibilizers remain in the epoxy

Petitioner Samsung Ex-1055, 0089

matrix as a single-phase material and thus lower the tensile modulus and improve the ductility of the encapsulant. They also reduce the exotherm (generated heat) and in certain circumstances reduce shrinkage too. Flexibilizers can also improve adhesive joint properties such as lap shear, peel strength, impact strength, and low-temperature crack resistance. Table 2.9 gives the influence of flexibilizers on epoxy resins. Stress-relief agents, on the other hand, remain as a second dispersed phase either during or prior to cure [30,31].

In epoxy molding compounds, the major stress-relief agents used are silicones, acrylonitrile-butadiene rubbers, and polybutylacrylate. Silicone elastomers, with their high purity and high-temperature properties, are the most favored stress-relief agents. Silicone elastomers interface-modified with polymethyl methacrylate possess uniform domain sizes (1–100 μm); they inhibit passivation layer cracking, aluminum line deformation, and cracking.

Table 2.9 Influence of Flexibilizers on Epoxy Resins

	Difunctional amine			Polysulfide			Polyamide	
Flexibilizer	–	25	25	50	25	50	43	100
Epoxy resin	100	100	100	100	100	100	100	100
Amine hardeners	20	13.2	20	20	20	20	–	–
Pot-life (min)	20	69	44	76	13	6	150	–
Viscosity 25°C (cP)	3,700	1,070	870	490	–	–	210,000	210,000
Flexural strength (MPa)	110	99	122	–	105	–	73	80
Compressive yield stress (MPa)	103	96	98	–	85	–	88	73
Impact strength (J/1.27-cm notch)	0.95	1.11	1.4	10.85	0.68	2.3	0.41	0.43
Heat distortion temperature (°C)	95	44	40	< 25	53	32	81	49

Petitioner Samsung Ex-1055, 0090

2.2.7 Flame Retardants

The aim of adding flame retardant substances to the molding compound is to meet Underwriters Laboratories (UL) requirements, to prevent flammability and to improve the component's shelf life, because epoxy resins are inherently flammable. Flame retardants were traditionally in the form of halogens (such as bromine) added to the epoxy resin backbone. One of the conventional flame retardants is the homologous brominated DGEBA. When used with normal non-halogenated resin, it gives flame-extinguishing properties, as flame retardancy is achieved by the bromine liberated at the decomposition temperature. Approximately 13–15 wt% of bromine is required to make an epoxy flame resistant [11]. Table 2.10 compares the thermal, mechanical, and electrical properties of a brominated BPA-based epoxy resin with those of a "standard" epoxy resin. Brominated flame retardants have been found to be toxic to the environment and, therefore, have been restricted or removed from the environmentally friendly or "green" molding compounds. More information on brominated flame retardants is provided in Section 2.7.

Antimony trioxide is another conventional flame retardant synergist with a generally higher cost. In conventional molding compounds, homologous brominated DGEBA epoxy and heterogeneous antimony oxides were used synergically [18]. The mechanism to extinguish fire by halogen and antimony type flame-retardant agent is as follows: The heavy specific gravity halogen antimony complex, which forms at high temperature, covers the flaming area and thus stops the supply of oxygen, which eventually stops the flame.

Table 2.10 Properties of Standard and Brominated Epoxy Resins [11]

Epoxy Resin Type	Standard	Brominated
Formulation (parts by weight)		
Bisphenol A-epichlorohydrin epoxy resin	100	–
Brominated bisphenol A resin	–	100
4,4′-Methylenedianiline	26	19.3
Gel time, 50 g at 100°C (min)	15	14
Heat distortion temperature (°C)	150	148.8
Flexural strength (MPa)	125.5	131.7
Dielectric constant (10 MHz)	3.31	3.28
Dissipation factor (10 MHz)	0.029	0.030
Volume resistivity (1 min/cm)	3.1×10^{14}	3×10^{14}

Petitioner Samsung Ex-1055, 0091

The flame resistance properties of molding compounds are studied through three ways: (1) resin structure, (2) filler content, and (3) new flame retardant. The inherent structure of the resin influences flame resistance. For example, a molecule that contains more aromatic rings shows greater tendency for flame resistance. High filler loading improves flame resistance. Antimony pentoxide (Sb_2O_5) was investigated and seemed to be a potential substitute for antimony trioxide (Sb_2O_3), as Sb_2O_5 is insoluble in water while Sb_2O_3 is slightly soluble in water. Using Sb_2O_5 as an antiflammable agent was also shown to be effective in reducing the degradation of resin bond strength and improving the high-temperature storage life performance of the molding compound [17]. Other alternative non-halogenated flame retardants investigated include metal hydroxides, metal hydrates, nitrogen-based substances, and phosphorus-containing retardants. Alternative non-halogenated and non-toxic flame retardants used in environmentally friendly or "green" molding compounds are discussed in Section 2.7.

2.2.8 Mold-Release Agents

Upon completion of the molding compound mixing and manufacturing process (also referred to as "compounding") and package encapsulation, the molding compound must be released from the compounding and molding equipments. Because of the excellent adhesion of the molding resins, such as epoxy, to all types of surfaces, release from the equipment may be difficult. Therefore, mold-release agents are added to the molding compound to facilitate the release of the compound from the equipment. To ensure that the mold-release agents do not degrade the epoxy adhesion to the package components, the activity of the release agent must be controlled as a function of temperature.

Mold-release agents are usually in the form of microplates that vary from liquids to pasty solids to finely divided powders. In general, the release agent should be insoluble in the resin mixture, should not melt at the curing temperature, and should be applied in a continuous film. The selection of the release agent is determined by the material of construction of the mold and the type of encapsulation selected.

Different release agents in epoxy molding compounds are used for compounding (~100°C) and molding (~175°C) operations. The adhesion of epoxy molding compound to the lead-frame at room temperature is not affected by the higher temperature (~175°C) mold-release agents that have solidified and lost effectiveness at lower temperature. The release

Petitioner Samsung Ex-1055, 0092

agent used for compounding, if not completely degraded, could become active at near 100°C use temperature and lead to some delamination in the package. Mold-release agents for epoxy molding compounds include silicones, hydrocarbon waxes, inorganic salts of organic acids, and fluorocarbons. Of these, hydrocarbon waxes, such as carnauba wax, are the most common for molding compounds used in microelectronic encapsulation. Silicones and fluorocarbons have poor functional temperature selectivity, while organic acid salts can corrode metallic package elements.

2.2.9 Ion-Trapping Agents

The objective of ion-trapping agents is to reduce the conductivity of any accumulated water at the metal–encapsulant interfaces inside the package, and thus to retard any electrolytic corrosive degradation processes. The incorporation of ion-getter agents into the epoxy molding compound makes residual alkali and halide ions such as Na^+, K^+, Cl^-, and Br^- in the epoxy unavailable for dissolution into any diffused, accumulated water in the package. Ion-trapping agents in epoxy molding compounds are hydrated metal oxide powders with particles several micrometers in diameter. These materials react with highly active alkali and halide ions to form nearly water-insoluble alkali and halide compounds. In about 5 wt% concentration, ion-getter additives have been reported to reduce aluminum cathodic and chemical corrosion by 1.5–3 times [32]. The main application of such formulated molding compounds is in packages where the encapsulant thickness is around a few mils, as in ultra-thin outline packages.

2.2.10 Coloring Agents

Coloring agents are added to the molding compound to distinguish between different device types in packages and eliminate device visibility through the normally pale yellow epoxy encapsulant. The colors are produced by the addition of thermally stable organic dyes or pigments. The coloring agent used in most plastic-encapsulated silicon ICs is carbon black, even though it does add slightly to the electrical conductivity of epoxy and can also reduce moisture resistance. The concentration of carbon black is usually less than 0.5% to avoid problems related to moisture absorption and impurities.

Petitioner Samsung Ex-1055, 0093

2.2.11 Market Conditions and Manufacturers of Encapsulant Materials

Miniaturization, thin-walling, electromagnetic interference shielding, and printed circuit board (PCB) fabrication advances are some of the technologies driving resin selection and consumption in electronic components such as connectors, bobbins, switches, capacitors, resistors, and PCBs, among others. Portable electronic devices, the most rapidly growing segment of the industry, place ever-increasing demands on plastic electronic components, the most important of which are the need for higher heat resistance and improved impact strength.

According to Business Communications Co., thermoplastic and thermoset consumption was estimated at slightly over 586 million pounds in 2006. It is expected to increase to over 700 million pounds by 2011 resulting in an annual growth rate of 4.3%.

Resin consumption in electronic components encompasses a select group of engineering resins led in volume by nylon and thermoplastic polyesters. Based on value, however, higher performance resins such as polyphenylene sulfide, polyimides, and liquid crystal polymers are more significant factors in the market. Engineering thermoplastics (ETPs) dominate the molded electronic component segment, of which connectors are the dominant part. On the thermoset side, epoxies are far and away the most dominant resins in two major applications—PCB laminates and encapsulants—contributing as much as 56% of the total resin market.

Thus, there are two distinct markets: ETPs for high-performance needs in molding electronic parts and thermosets for PCBs and encapsulation. There is minimal crossover; very little ETP volume is consumed in PCB laminates and encapsulants, and only relatively small amounts of thermosets are used to mold electronic components.

Resin competition is practically all in the ETP arena and is quite intense, as all of the ETPs in this study target connectors as a prime market. This competitive scenario also applies to other molded electronic parts and places some resin producers at a disadvantage, because several of them market competing resins for the same product (e.g., GE Plastics, Bayer, BAS).

Encapsulants and the equipment used to dispense them have become among the fastest growing, most sophisticated areas of semiconductor packaging. As chips become more complex, and more costly, the need to protect them from moisture via the package and its encapsulant has taken on a new urgency. Newly emerging markets, flash memory, for example,

Petitioner Samsung Ex-1055, 0094

are demanding greater levels of equipment automation for chip scale packages, lower-stress encapsulants, higher adhesion, and anti-popcorning materials; in short, they require a quantum leap in encapsulant processing.

The main molding material manufacturers are Nitto Denko, Sumitomo Bakelite, and Plaskon. The following sections give brief descriptions of these companies and their material property tables. A list of some other companies producing encapsulating materials is also provided in Fig. 2.23.

Nitto Denko is a diversified materials company headquartered in Osaka, Japan. They have manufacturing plants worldwide, including three in the United States. The company was founded in 1918 to produce electrical insulating materials. About 30% of its business is electronics-related. Other areas include industrial products, packaging products, engineering plastics, medical products, and membrane products.

Sumitomo Bakelite is a plastics manufacturing company based in Tokyo, Japan. About half of their business is electronics-related, with a 1999 total of sixty billion yen (~$500 million). About 30% of its business is electronics-related. Other markets in which they operate include materials for the automotive, medical, building, and packaging markets.

Plaskon is a division of Cookson Semiconductor Packaging Materials (CSPM) based in Alpharetta, GA. It was acquired from BPAmoco in 1999. CSPM manufactures cleaners, fluxes, solder pastes, adhesives, and underfills. Design is done in Georgia, while manufacturing is in Singapore. The company has applications engineers based in the United States, Singapore, Europe, South Korea, and the Philippines.

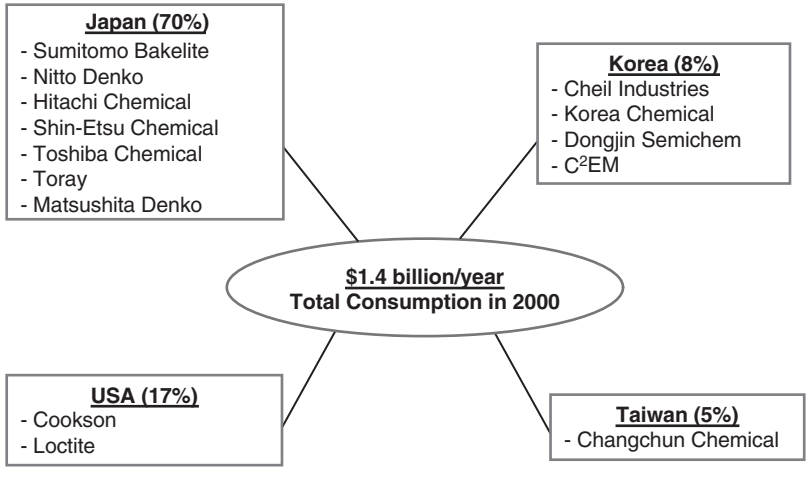


Figure 2.23 Status of epoxy molding compound manufacturers.

Petitioner Samsung Ex-1055, 0095

2.2.12 Material Properties of Commercially Available Molding Compounds

The molding compound is typically characterized by a set of properties that determine its suitability for a given application and process. From a manufacturing perspective, viscosity and flow characteristics as well as curing time and temperature are important factors in determining which encapsulant materials should be used. From a performance viewpoint, key characteristics range from electrical, mechanical, and thermal properties to chemical and humidity resistance, the water solubility of contaminants, and adhesion to chip/component surfaces. Key properties include the following:

- mold-filling characteristics, resin bleed, hot hardness, and mold staining;
- spiral flow length;
- shear viscosity at low shear rates;
- cure time;
- flow resistance;
- glass transition temperature;
- thermomechanical properties;
- thermal conductivity;
- dielectric constant;
- thermal stability;
- coefficient of thermal expansion;
- electrical resistivity;
- flexural strength and modulus;
- hydrolyzable ionic purity;
- moisture solubility and diffusion rates;
- adhesion strength to lead-frame materials;
- alpha-particle emission (if applicable); and
- popcorn resistance for surface-mount technology.

Technical information on the above properties and information on optimum processing conditions for specific molding compounds is provided by suppliers. Table 2.11 provides properties of a typical molding compound.

In this section the properties of commercially available encapsulating materials from Nitto Denko, Sumitomo Bakelite, and Plaskon are provided.

Petitioner Samsung Ex-1055, 0096

Table 2.11 Properties of a Typical Molding Compound

Item	Unit	Value
Spiral flow	cm	105
Gel time	sec	50
Coefficient of thermal expansion		
α_1	ppm/°C	17
α_2	ppm/°C	68
T_g	°C	165
Thermal conductivity	10^{-2} W/m °C	67
Flexural strength		
25°C	N/mm^2	120
240°C	N/mm^2	16
Flexural modulus		
25°C	10^2 N/mm^2	120
240°C	10^2 N/mm^2	6.5
Specific gravity	–	1.82
Volume resistivity (150°C)	Ω cm	10^{13}
UL flame class	UL-94	V-0
Water absorption (boiling, 24 hrs)	wt%	0.30
Extracted water		
Na^+	ppm	1
Cl^-	ppm	5

2.2.12.1 Nitto Denko

For all the materials in Table 2.12, the cure time is 120 seconds at 175°C (except for MP-8000AHP, for which the cure time is 90 seconds). Post-cure is 5 hours at 175°C for all the materials listed.

2.2.12.2 Sumitomo Bakelite

The properties of encapsulating materials from Sumitomo Bakelite are given in Table 2.13.

2.2.12.3 Plaskon

The properties of encapsulating materials from Plaskon are given in Table 2.14.

Petitioner Samsung Ex-1055, 0097

Table 2.12 Properties of Select Nitto Denko Molding Compounds

Material	Type	Max. Moisture Absorption (%)*	Viscosity at 175°C (Pa sec)	Spiral flow at 175°C and 1000 psi (cm)	Gel Time (sec)	T_g (°C)	CTE1, CTE2 (ppm/°C)	Thermal Conductivity (W/m K)	Flexural Modulus at Room Temp. (GPa)	Dielectric Constant at 1 MHz
MP-7000	Biphenyl, conventional	0.35*	15	100	25	125	16, 65	0.71	16	3.6
MP-7000H	Biphenyl, rapid cure	0.35*	25	70	15	125	16, 65	0.71	16	3.6
MP-7000V	Biphenyl, low alpha	0.35*	15	100	25	125	16, 65	0.71	16	3.6
MP-7100	Biphenyl, conventional	0.29*	15	100	25	125	13, 55	0.75	19	3.7
MP-7100H-3	Biphenyl, rapid cure	0.25*	20	70	20	125	11, 50	0.80	19	3.7
MP-7250	Biphenyl, conventional	0.30*	23	100	22	125	13, 57	0.75	15	3.7
MP-7410TA	Biphenyl, conventional	0.17**	7.5	100	28	120	8, 32	0.88	27	3
MP-8000A	OCN, conventional	0.60**	23	80	17	158	18, 70	0.67	13	3.7
MP-8000AHP	OCN, rapid cure	0.60**	30	55	10	158	18, 70	0.67	13	3.7
MP-8950CH	OCN, conventional	0.24**	14	95	20	135	10, 43	0.76	20	3.7
HC-30-2	OCN, conventional	0.50**	17	85	17	169	28, 70	1.47	15	4.6
HC-100-X1	Special, BGA	0.18**	10	110	25	160	6, 25	0.97	27	3.6
MP-4000H7	Special, high thermal	0.40**	80	65	37	162	23, 60	2.51	22	4.7

BGA: Ball-grid array; CTE: Coefficient of thermal expansion; OCN: Ortho-cresol novolac; RH: Relative humidity.
*After 120 hrs at 85°C/85% RH.
**After 48 hrs in boiling water.

Petitioner Samsung Ex-1055, 0098

Table 2.13 Material Properties for Sumitomo Bakelite Molding Compounds

Material	Type	Max. Moisture Absorption after 24 hrs Boiling (%)	Spiral Flow (cm)	Gel Time at 175°C (sec)	T_g (°C)	CTE1, CTE2 (ppm/°C)	Thermal Conductivity (W/m K)*	Flexural Modulus at Room Temp. (GPa)**	In-mold Cure Time (sec)	Post-Mold Cure Time (hrs)
EME-6300H	OCN, industry standard, low stress	0.30	80	40	165	17, 68	0.67	11.8	90	4
EME-6600CS	DCPD, short post-mold cure	0.16	90	30	150	10, 40	0.75	20.6	60	2
EME-6600H	DCPD, short post-mold cure, low CTE	0.12	90	30	150	8, 34	0.92	26.5	100	2
EME-6710S	OCN, low stress, high temp.	0.30	75	40	170	13, 65	0.67	11.3	90	4
EME-6650R	OCN, short post-mold cure, low stress	0.22	100	35	165	11, 45	0.75	18.6	60	2
EME-6730B	OCN, low stress	0.22	110	30	150	11, 49	0.71	12.7	60	4
EME-7320CR	Biphenyl, thin profile	0.22	140	23	145	13, 52	0.75	17.2	45	8
EME-7351UT	Biphenyl, thin profile	0.18	100	30	130	10, 45	0.83	23.0	60	8
EME-7372	Biphenyl/OCN, thin profile	0.19	100	33	135	9, 38	0.92	25.5	60	3
EME-7720TA	Multifunctional for BGA/CSP, high T_g	0.33	133	27	195	11, 40	0.80	20.6	45	4
EME-7730L	Biphenyl, for BGA/CSP	0.17	120	35	150	10, 36	0.88	24.0	70	4

BGA: Ball-grid array; CSP: Chip scale package; CTE: Coefficient of thermal expansion; DCPD: Dicyclopentadiene; OCN: Ortho-cresol novolac.
*1.0 W/m K = 0.0023885 cal/cm s K.
**1 GPa = 101.97 kgf/mm^2.

Petitioner Samsung Ex-1055, 0099

Table 2.14 Material Properties for Plaskon Molding Compounds

Material	Max. Moisture Absorption (%)*	Viscosity at 175°C (Pa s)	Spiral Flow at 175°C and 1000 psi (cm)	Gel Time (sec)	Molding Temp. (°C)	Molding Pressure (psi)	In-mold Cure Time (sec)	Post-Mold Cure Time (hrs)	T_g (°C)	CTE1, CTE2 (ppm/°C)	Thermal Conductivity (W/m K)	Flexural Modulus at Room Temp. (Mpsi)	Dielectric Constant at 1 kHz
3400	0.50	8–15	63–87	18	170–185	750–1000	60–120	4–12	155	20, 62	0.7	2.2	3.8
AMC-2RA	0.50	7	76	10	165–175	500–1000	60–90	0–0.3	155	12, 61	0.7	2.2	3.6
AMC-2RC	0.50	7	76	10	175	800–1400	30–90	0–2	155	12, 61	–	2.4	3.6
LS-16	0.45	12.5	56	8	165–175	500–1000	30–40	0–0.3	165	16, 67	0.7	1.7	3.3
S-7P	0.49	8.5	100–130	15–23	170–185	900–1200	60–120	4–12	150	18, 45	0.7	1.9	3.8
S-7PG	0.49	9.0	60–90	10–18	170–185	900–1200	60–120	4–12	170	18, 65	0.7	1.9	3.6
SMT-B-1FX	0.59	5.4	103	16	175	800–1200	60–150	0–4	218	13, 53	0.8	2.2	3.9
SMT-B-1LAS	0.59	4.5	140	15	170–185	750–1000	120–180	4–5	220	16, 68	0.7	2.0	3.7
SMT-B1LV	0.59	5.0	130	19	170–185	750–1250	120–180	4–6	225	14, 58	0.7	1.8	4.0
SMT-B-1RC	0.59	5.5	105	12	175	800–1200	60–150	0–4	226	15, 55	0.8	1.9	3.9
SMT-B-1 150.910-1	0.38	5.5	140	18	170–185	750–1250	70–120	0–3	170	10, 50	0.7	2.6	4.0

*Approximate moisture absorption by weight gain method following 168 hrs of 85°C/85% RH soak.

Petitioner Samsung Ex-1055, 0100

2.2.13 Materials Development

New molding compound materials are continuously being researched and developed for the purpose of improved properties, compatibility with fast-changing semiconductor and packaging technologies, and environmental friendliness. The overall approach in encapsulant molding compound development is provided in Fig. 2.24. Reliability, composition, and moldability are the top factors in driving the development of new molding compound development. New materials including environmentally friendly or "green" substances, new component designs, and continuous process improvements define the direction of plastic packaging improvements. A separate section (Section 2.7) has been dedicated to the discussion of environmental friendly or "green" encapsulant materials including a discussion of toxic flame retardants and "green" material development.

In addition to green molding compound development, another consequence of environmental awareness regarding electronic packaging and assembly materials is the push toward lead-free solder. Conventionally, tin–lead (Sn–Pb) eutectic solders were used during the process of mounting semiconductor packages onto the substrate. However, there is a global movement toward restricting or abolishing the use of Sn–Pb solders. Because the lead in the solder can flow into the ground via acid rain and can harm the human body, it is considered a toxic substance. However, using lead-free solder brings to the forefront several other issues that must also be addressed such as

- increase of reflow temperature;
- cost up (price of the solder);
- change in reliability of interconnects.

Among the issues related to lead-free solder, the increase of reflow temperature when lead-free solder is used is the most critical for semiconductor molding compounds. The melting point of conventional Sn–Pb solder is 183ºC and the reflow temperature is around 240ºC. However, the melting point of tin–silver group solder, one of the candidate lead-free solders, is higher, at around 210–220ºC. It is necessary to reflow at 260ºC to obtain the same connection reliability as before, as the workability (wettability) is inferior to that of the Sn–Pb solder. Accordingly, dimensional deformation and the vapor pressure generated by absorbed water in the molding compound will increase with rising processing temperatures.

As a result, a compound that passes JEDEC (Joint Electron Devices Engineering Council) Level 1 (absorption under 85ºC, 85% RH, 168 hours)

Petitioner Samsung Ex-1055, 0101

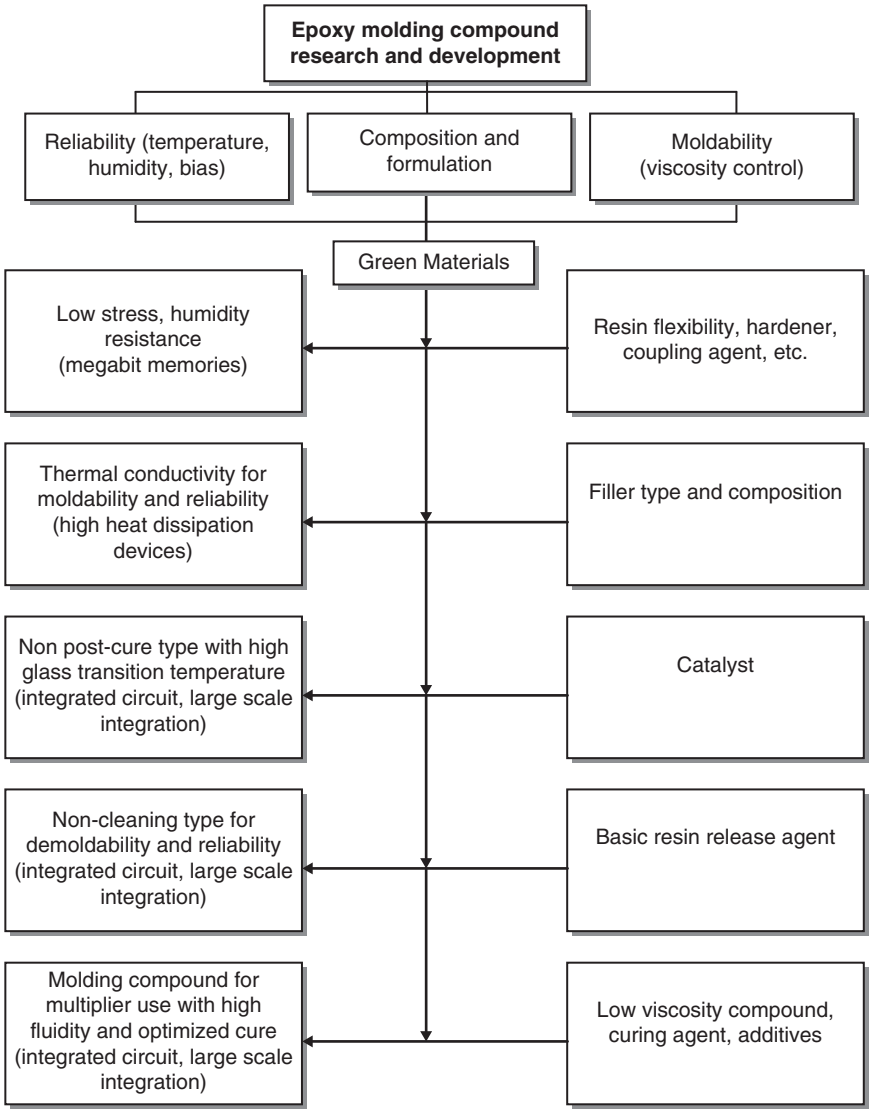


Figure 2.24 Material development trends of epoxy molded compounds.

with three reflow passes of 240ºC may crack or delaminate when treated under 260ºC reflow. Therefore, it is necessary to raise the level of the polymer's insulation. Some investigations are underway to develop a novel molding compound that generates no defective products during 260ºC reflow, and that is bromine and anitmony free.

Petitioner Samsung Ex-1055, 0102

Another issue considered in new material development is improvement in heat conductivity. An investigation has been conducted to evaluate a thermally enhanced molding compound containing SCAN® filler. This new molding compound improves the thermal and electrical performance of packaged power devices. Power metal-oxide semiconductor field effect transistors (MOSFETs) in S0-8 packages were evaluated for shifts in electrical characteristics and reliability.

Thermally conductive filler material has also been developed by the Dow Chemical Co. for use in thermally enhanced molding compounds and glob-tops. SCAN is a hydrolytically stable aluminum nitride powder with a particle size distribution and ionic purity appropriate for use in encapsulating microelectronic devices. SCAN is a thermally conductive filler that can significantly enhance the thermal dissipation characteristics of an epoxy molding compound without compromising other performance parameters such as reliability. The molding compound used in this study was a formulation (75 wt% SCAN) based on a standard ortho-cresol novolac epoxy formulation and is available commercially from a major Japanese molding compound supplier.

Figure 2.25 shows the transient thermal response (in still air) of devices assembled with the mold compound containing SCAN compared to those assembled with the standard mold compound. It is clear that the molding

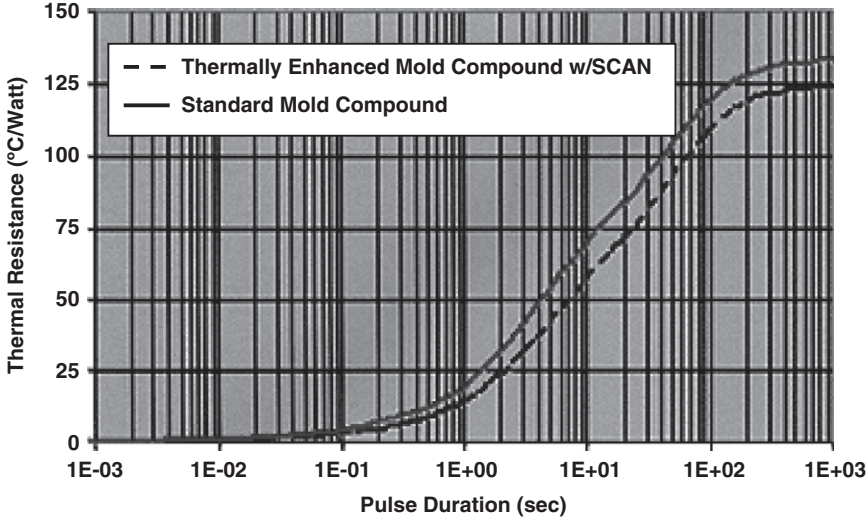


Figure 2.25 Transient thermal response curves for devices assembled with the SCAN mold compound (dashed line) versus those assembled with the standard mold compound (solid line).

Petitioner Samsung Ex-1055, 0103

compound containing SCAN has lower thermal resistance, about 8% lower under steady-state Direct-Current (DC) conditions.

The electronic materials division of Henkel (previously Dexter Corp.) has developed a molding material to act as both underfill and encapsulant. The approach Henkel is using is to synthesize filler particles that are highly spherical. Without any "catch points" or "hooks" in the particles, the molding compound has flow properties good enough for void-free underfilling. Non-spherical particles catch onto surfaces, and each other, to interrupt flow and cause voids.

2.3 Glob-Top Encapsulants

Glob-top encapsulants are highly viscous pastes used to encapsulate bare chip devices such as flip-chip and chip-on-board. These materials are dispensed as liquids on top of a semiconductor device and then cured to form a protective barrier. An example of the glob-topping encapsulation is shown in Fig. 2.26. Glob-top encapsulation is also used for tape-automated bonding (TAB) devices, due to the fragility of the tape.

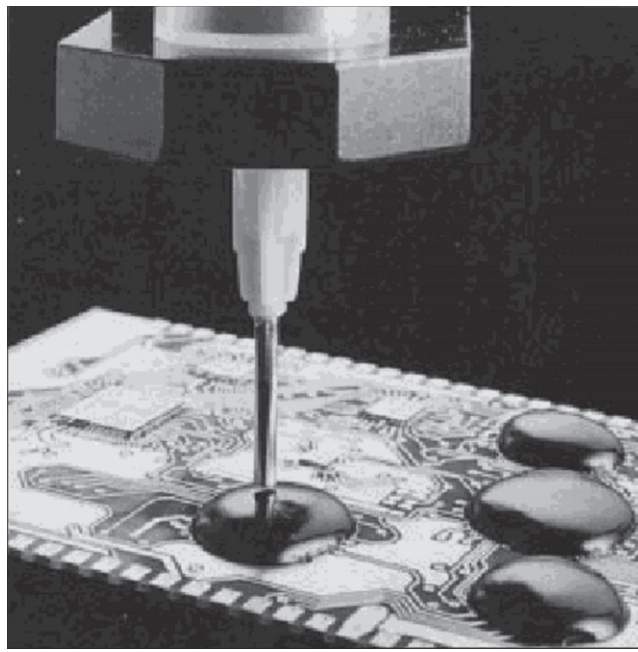


Figure 2.26 Glob-topping components on a circuit card [33].

Petitioner Samsung Ex-1055, 0104

Glob-top encapsulants are thermoset epoxy or silicone resin formulations, filled to a medium level with inorganic fillers, although some glob-top encapsulants are supplied as a single-component frozen mix in a dispenser. After cure, epoxy-based glob-tops yield a rigid matrix with a moderate glass transition temperature, whereas silicone or polyurethane-based glob-tops provide a flexible compliant mass.

During application and cure, glob-tops must possess balanced viscosity, thixotropy, and bleed resistance properties. Low viscosity is particularly required for encapsulant flow into thin gaps in flip-chip and flip-TAB encapsulations. Other desirable glob-top characteristics include fast cure without voids, a low level of hydrolyzable ionics, adequate mechanical strength, low stress, good moisture resistance, good adhesion to all encapsulated surfaces, appropriate thermal conductivity, and good insulating properties.

To ensure chip reliability, the choice of resin is critical. Low-viscosity epoxies, silicone-modified epoxies, and silicone materials are the most widely used polymers for this application. To avoid bubble formation, glob-top coatings must be solvent-free and low-stress after cure.

Table 2.15 lists glob-top materials from Henkel Loctite Corporation, one of the leading manufacturers of glob-top encapsulant products.

2.4 Potting and Casting Encapsulants

Potting and casting are encapsulation techniques generally used for larger electronic units such as transformers, connectors, power supplies, sensors, amplifiers, high-voltage resistor packs, and relays. In potting, the electronic device is positioned inside a “pot” or a case and the liquid potting resin is poured in, covering the device completely (Fig. 2.27). The resin is cured and solidified, and the case becomes a part of the encapsulated electronic unit. In casting, a similar process takes place, except that at the end of the process the case is removed from the encapsulated unit (www.pottingsolutions.com). Common materials used for potting and casting of electronic units are silicones, epoxies, and polyurethanes. Dow Corning Corporation, General Electric Company, and National Starch and Chemical Company are three major manufacturers of potting and casting materials.

2.4.1 Dow Corning Materials

More than 30 years were spent on the study of silicones by Kipping, but the commercial value of silicones was not realized until 1943 when Corning Glass and Dow Chemicals (set up as Dow Corning Corporation)

Petitioner Samsung Ex-1055, 0105

Table 2.15 Henkel Loctite Corporation Glob-Top Encapsulants [34]

Product	Color	Viscosity at 25°C ($\times 10^3$ C_p)	CTE1, CTE2 (ppm)	T_g (°C)	Hardness Shore D	Curing Schedule	Shelf Life at 4°C
Hysol® EO1016	Black	62	46, 140	126	86	20 min at 150°C	12 mo
Hysol® EO1060	Black	20	40, –	125	–	4–6 hrs at 125°C	5 mo
Hysol® EO1061	Black	50	40, –	125	–	3 hrs at 140°C	7 mo
Hysol® EO1080	Black	60	35, 125	121	86	20 min at 150°C	12 mo
Hysol® FP4323	Black	220	29, –	160	97	4 hrs at 150°C	9 mo at –40°C
Hysol® FP4402	Black	100	22, –	155	97	5 hrs at 150°C	5 mo at –40°C
Loctite® 3534	Dark red	60	20, 72	139	–	60 min at 150°C	–

mo: Months.
Note: Typical property values; not to be used as specifications.

began the manufacturing process of silicone polymers (Plastiquarian, http://www.plastiquarian.com/kipping.htm). Since then, Dow Corning has been one of the major manufacturers of silicone materials used in electronics encapsulation and coating. Table 2.16 lists Dow Corning silicone materials used for potting and casting of electronic parts and their selected material properties.

Pot life or working time is the time starting from the mixing of parts A (i.e., resin) and B (i.e., catalyst) until the mixture remains suitable for use. As the viscosity gradually increases during curing, some manufacturers define pot life based on the viscosity of the mixture. For example, Dow Corning defines pot life as the time required for viscosity to double after parts A and B (base and curing agents) are mixed.

2.4.2 General Electric Materials

General Electric (GE) room temperature vulcanization (RTV) silicone products are used as electronics coating, adhesives, sealants, and potting

Petitioner Samsung Ex-1055, 0106

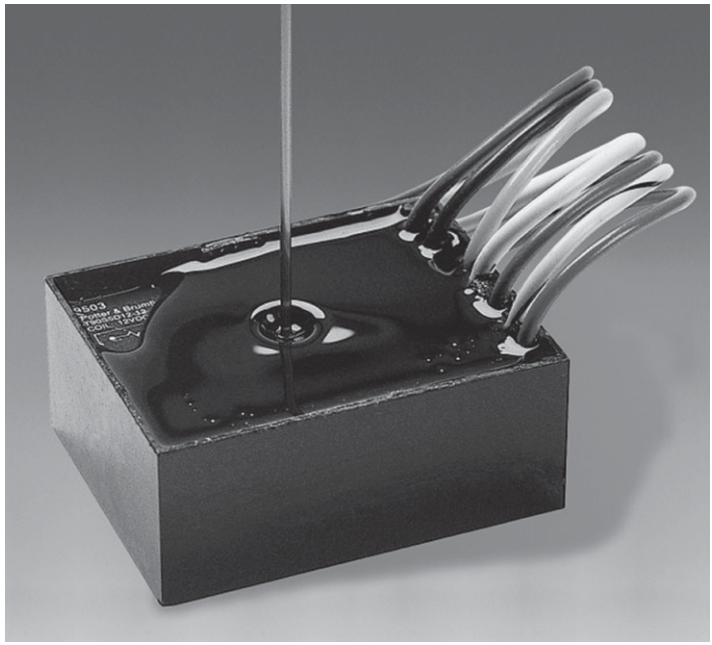


Figure 2.27 Potting with silicone material. (Courtesy of ITW Polymer Technologies, http://www.insulcast.com/solutions.html.)

encapsulants for various applications Table 2.17 shows RTV silicone application in aviation electronics. RTV silicones generally cure (vulcanize) at room temperature, although some may require higher temperatures. RTV silicones can be one-part or two-part products. The curing process is either by addition or by condensation. The profile of RTV silicones is shown in Fig. 2.28.

Condensation cure silicone products cure when exposed to ambient moisture. It takes some time for the product to completely cure because the moisture must diffuse through the material to reach the inner unexposed parts. The reaction mechanism and viscosity of the material can also affect the curing time. At 25°C and 50% RH (typical room condition), complete curing takes about 24–48 hours. In some cases, full physical properties may take a longer time (i.e., 7–14 days) to develop.

Tables 2.18 and 2.19 list the material properties of GE condensation cure RTV products for one-part and two-part systems, respectively. Tack-free time refers to the amount of time it takes for a condensation cure RTV product to form a cured outer layer. The uncured product is generally tacky or sticky, and thus tack-free layer indicates curing.

Petitioner Samsung Ex-1055, 0107

Table 2.16 Dow Corning Silicone Potting Products

Product	Mix Ratio	Color	Viscosity ($\times 10^3$ cps or mPa s)	Durometer, Shore A	Dielectric Constant at 100 Hz	Working Time at RT	Linear CTE (ppm)	Curing Time at RT	Curing Time at 150°C	Shelf Life from Date of Manufacture at RT (months)
Sylgard® 160	1:1	Gray	4	60	3.30	30 min	240	24 hrs	5 min	18
Sylgard® 164	1:1	Gray	12.8	61	3.34	14 min	220	35 min	_	15
Sylgard® 170	1:1	Dark gray to black	2.9	40	3.17	15 min	270	24 hrs	_	24
Sylgard® 170 Fast Cure	1:1	Dark gray to black	2.85	42	2.97	<5 min	_	10 min	_	18
Dow Corning® 96-082 A & B	1:1	Black	1.1	31	3.14	14 days	285	_	30 min	12
Sylgard® 182	10:1	Clear	3.9	50	2.65	>8 hrs	310	_	10 min	24
Sylgard® 184	10:1	Clear	3.9	50	2.65	>2 hrs	310	~48 hrs	10 min	24
Dow Corning® 3-6121	10:1	Translucent	25	30	2.92	2 hrs	290	~48 hrs	10 min	18
Dow Corning® 3-8264	1:1	Black	2.9	45	3.11	5 hrs	290	_	<30 min	9
Dow Corning® 567	1:1	Black	1.5	45	2.85	>3 days	300	_	15 min	24
Dow Corning® 255	10:1	Gray to black	5.5	25	2.95	>5 min	311	~4 hrs	_	_

CTE: Coefficient of thermal expansion; RT: Room temperature.
Note: Typical property values; not to be used as specifications.

Petitioner Samsung Ex-1055, 0108

Table 2.17 General Electric Silicones Used for Potting of Aviation Electronics

Electronic Applications	One-Component				Two-Component					
	RTV-106	RTV-116	RTV-142	RTV-160	RTV11 RTV21 RTV41	RTV-60	RTV-88	RTV560 RTV566	RTV-577	RTV-8000 Series
Circuit and terminal protection			*	*		*	*	*	*	*
Cockpit instrument sealant			*	*		*	*	*	*	*
Electrical wire sealant	*	*		*						
Sealing, potting, and encapsulating computer units			*	*		*	*	*	*	*
Electronic power equipment encapsulant					*					

Petitioner Samsung Ex-1055, 0109

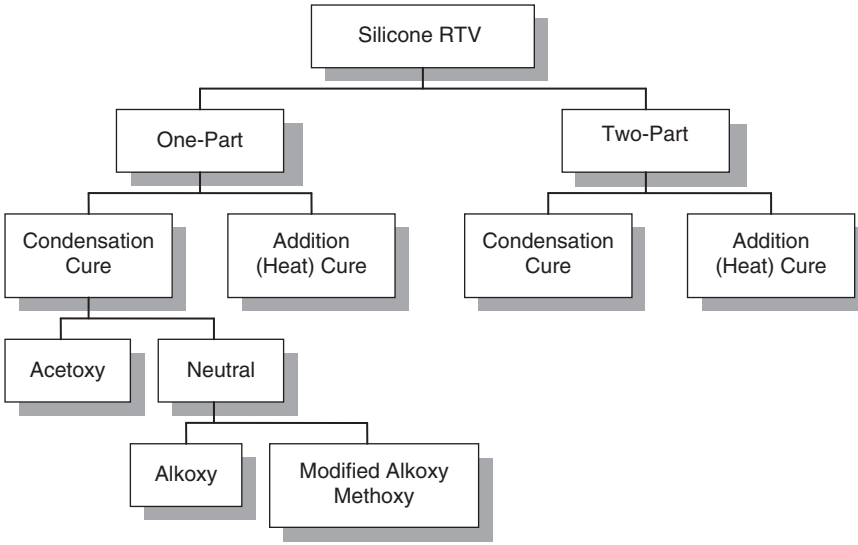


Figure 2.28 Profile of room temperature vulcanization (RTV) silicone.

In condensation cure RTV materials, during the curing process by-products are produced. Table 2.20 lists the by-products of condensation cured GE RTV encapsulants.

Addition cure RTV products cure by heating, generally at room temperature (~25°C). Heating at higher temperatures can accelerate the curing process. Addition cure potting materials usually have an inhibitor present in the formulation that prevents the curing of the liquid encapsulant until it is activated at a certain temperature, generally at room temperatures or above. The inhibitor leaves the system upon curing and no by-products remain. Tables 2.21 and 2.22 list the material properties of GE addition cure RTV products for one-part and two-part systems, respectively.

2.5 Underfill Encapsulants

In flip-chip packages, there is a thermal expansion mismatch between the silicon chip, the solder ball, and the substrate. The CTE of silicon is approximately 3 ppm/°C, and typical alumina substrate has a CTE of 6.7 ppm/°C. Large strains are observed in the outermost solder bumps due to this thermal expansion mismatch. The strain increases, as the semiconductor chips are made larger. To compensate for this mismatch, a liquid underfill resin with a CTE close to that of the solder bumps (~30 ppm/°C)

Petitioner Samsung Ex-1055, 0110

Table 2.18 General Electric One-Part Condensation Cure RTV Encapsulants

RTV	Cure Chemistry	Color	Viscosity (cps)/ Application Rate (g/min)	Temperature Range	Hardness, Shore A	Tensile Strength (psi)	Elongation (%)	Dielectric Strength (V/mil)	Dielectric Constant	Track-Free Time	Cure Time at 25°C (hrs)
106	Acetoxy	Red	400 g/min	–60 to 260°C	30	375	400	500	2.8	20 min	24
116	Acetoxy	Red	2.5×10^4 cps	–60 to 260°C	20	350	350	400	2.8	30 min	24
160	Alkoxy	White	3.5×10^4 cps	–60 to 204°C	25	275	230	500	2.8	4 hrs	24
142	Alkoxy	White	725 g/min	–60 to 204°C	34	550	400	500	2.8	4 hrs	24

RTV: Room temperature vulcanization.
Note: Typical property values; not to be used as specifications.

Petitioner Samsung Ex-1055, 0111

Table 2.19 General Electric Two-Part Condensation Cure (Alkoxy) RTV Enacpsulants

RTV	Mix Ratio (base to curing agent by weight)	Color	Viscosity ($\times 10^3$ cps)	Temperature Range	Hardness, Shore A	Tensile Strength (psi)	Elongation (%)	CTE ($\times 10^{-5}$ cm/cm °C)	Dielectric Constant (1 kHz)	Processing: Work (Pot) Life (hrs)	Processing: Cure Time at 25°C (hrs)
11	100:0.5	White	11	–54 to 204°C	41	300	160	25	3.3	1.5	24
12	20:1	Clear	1.3	–54 to 204°C	18	–	200	29	3.0	1.6	24
21	100:0.5	Pink	26	–54 to 204°C	45	310	180	20	3.8	1	1
31	100:0.5	Red	25	–54 to 260°C	30	870	170	20	4.4	2	24
41	100:0.5	White	39	–54 to 260°C	47	310	180	20	3.7	1	24
60	100:0.5	Red	40	–54 to 260°C	20	990	120	20	4.0	2	24
88	100:0.5	Red	880	–54 to 260°C	58	830	120	20	4.3	0.75	24
511	100:0.5	White	16	–115 to 204°C	42	380	170	22	3.6	1.5	24
560	100:0.5	Red	30	–115 to 260°C	55	690	120	20	3.9	2.25	24
566	100:0.1	Red	42.7	–115 to 260°C	61	800	120	–	–	1.5	24
577	100:0.5	White	700	–115 to 204°C	48	440	150	20	3.9	2	24
8111	100:2	White	9.9	–54 to 204°C	45	350	160	25	3.3	0.5	24
8112	100:5	White	11	–54 to 204°C	42	300	160	25	4.0	2	24
8262	100:5	Red	47	–54 to 260°C	25	580	150	20	3.9	2	24

CTE: Coefficient of thermal expansion; RTV: Room temperature vulcanization.
Note: Typical property values; not to be used as specifications.

Petitioner Samsung Ex-1055, 0112

Table 2.20 By-products of Condensation Cure General Electric RTV Encapsulants

Condensation Cure Product Type	Cure Chemistry	By-product
One-part	Acetoxy	Acetic acid
One-part	Alkoxy	Alcohol
One-part	Methoxy	Methanol and/or ammonia
Two-part	Catalyst	Alcohol and water

Table 2.21 General Electric One-Part Addition Cured Potting Encapsulants

Potting Encapsulant	Color	Viscosity ($\times 10^3$ cps)	Temp. Range	Hardness, Shore A	Tensile Strength (psi)	Elongation (%)	Dielectric Strength (75 mils) (V/mil)	Cure Time at 100°C (hrs)
TSE 325	White	4	–60 to 205°C	12	102	200	530	4
TSE 3251	White	8.5	–60 to 205°C	16	102	200	500	4
TSE 3221 S-W	Translucent	58	–60 to 205°C	28	406	370	635	3

Note: Typical property values; not to be used as specifications.

is deposited and cured in the gap between the chip and substrate. The use of underfill enables structural coupling of the chip and substrate, effectively decreasing the shear stress and thus lowering the applied strain on the solder joints [35]. The key properties of underfill materials are detailed in Table 2.23.

An underfill is a composite material made up of an epoxy polymer with significant amounts of filler. Additional components added to the underfill formulation are flow agents, adhesion promoters, and dyes. Although primarily used for flip-chip devices, underfills can also be used with ball-grid arrays (BGAs) and CSPs. Some common reasons for using underfills include:

- the reduction of the effect caused by the CTE mismatch between the silicon die and the substrate;
- mechanical support and stability;

Petitioner Samsung Ex-1055, 0113

Table 2.22 General Electric Two-Part Addition Cured Potting Encapsulants

Potting Encapsulant	Mix Ratio (by weight)	Color	Viscosity ($\times 10^3$ cps)	Temperature Range	Hardness, Shore A	Tensile Strength (psi)	Elongation (%)	CTE ($\times 10^{-5}$ cm/cm°C)	Work (Pot) Life at 25°C	Cure Time at 100°C
TSE 3033	1:1	Translucent	1	–60 to 204°C	30	142	130	23	6 hrs	1 hr
RTV 615	10:1	Translucent	4	–60 to 204°C	44	920	120	27	4 hrs	1 hr
RTV 655	10:1	Translucent	5.2	–115 to 204°C	45	920	120	33	4 hrs	1 hr
RTV 656	10:1	Translucent	5	–115 to 204°C	44	920	100	33	4 hrs	1 hr
RTV 627	1:1	Dark gray	1.3	–60 to 204°C	62	475	60	21	2 hrs	1 hr
RTV 6428	1:1	Dark gray	1.4	–60 to 204°C	62	475	60	21	4 min	10 min

CTE: Coefficient of thermal expansion.
Note: Typical property values; not to be used as specifications.

Petitioner Samsung Ex-1055, 0114

Table 2.23 Key Properties of Underfill Materials [36]

Property	Comments
Viscosity, flow properties	Want low viscosity and good flow so that underfill can completely fill the small gaps (50–100 μm high) between chip and substrate
Silica filler content	Filler is needed to lower the polymer's CTE to match that of the solder bumps
Filler size, distribution, and shape	Filler size, distribution, and shape affect flow properties
Thermoset polymer chemistry	Want polymer system with high glass transition temperature (T_g) for stable mechanical properties
Young's modulus	Want modulus as high as possible to enable good mechanical coupling between chip and substrate
Cure cycle	Cure cycle must be relatively short and appropriate for manufacturing
Adhesion	Want excellent adhesion to chip and ceramic surfaces when cured
Moisture sensitivity	Want excellent moisture resistance
Ionic contamination	Want low ionic contamination for semiconductor applications
Quality control	Need tight quality control on underfill materials
Cost	Need to produce high quality material at reasonable cost

CTE: Coefficient of thermal expansion.

- environmental protection from moisture, ionic residues, and unwanted substances;
- adhesion of the component to the substrate;
- protection from shock.

Recent advances in underfill formulations include no-flow underfills, which are dispensed on the substrate before the chip placement and cured during solder bump reflow [37]. The no-flow underfilling process not only eliminates the strict limits on the viscosity of underfill materials, process temperature, and package size, but also improves the production efficiency [38]. Other improvements in underfill technology include fast-cure underfills and reworkable underfills.

Table 2.24 lists underfill materials from Henkel Loctite Corporation, including applications, pot life, recommended cure schedules, and other properties.

Petitioner Samsung Ex-1055, 0115

Table 2.24 Henkel Loctite Corporation Underfill Encapsulant Products [34]

Product	Applications	Pot Life at 25°C	Recommended Cure	Viscosity at 25°C ($\times 10^3$ cps)	T_g (°C)	CTE (ppm/°C)
Hysol® FP6100	Reworkable CSP/BGA	16 hrs	10 min at 150°C	7.9	0	94
Hysol® FP4531	Flip-chip 75 μm gap	8 hrs	7 min at 160°C	9.0	144	28
Hysol® FP4549	Flip-chip 12 μm gap	24 hrs	30 min at 165°C	2.3	140	45
Hysol® FF2200	Flip-chip no-flow (fluxing)	16 hrs	Reflow profile	3	128	72
Loctite® 3513	Reworkable BGA/CSP	5 days	30 min at 100°C	3.5	140	57
Loctite® 3514	BGA/CSP underfill	5 days	60 min at 100°C	3.5	140	57
Loctite® 3563	Snap cure flip-chip	>8 hrs	5 min at 150°C	8	130	35
Loctite® 3565	High T_g flip-chip	>8 hrs	30 min at 150°C	45	155	25
Loctite® 3568	Reworkable flip-chip BGA/CSP	30 hrs	15 min at 150°C	11	110	55
Loctite® 3593	Snap cure unfilled CSP	7 days	5 min at 150°C	5.5	110	50

BGA: Ball-grid array; CSP: Chip scale package; CTE: Coefficient of thermal expansion.
Note: Typical property values; not to be used as specifications.

2.6 Printing Encapsulants

Common encapsulant materials used for printing encapsulation are liquid epoxy resins with specific low warpage characteristic. In printing encapsulation, the encapsulant material is dispensed onto stencil openings (or package cavities) and is then planarized and cured. Because of the matrix characteristics of the printing encapsulation (i.e., multiple openings in the stencil or cavities), printing encapsulation is often more susceptible to warpage than other encapsulation technologies. To reduce

Petitioner Samsung Ex-1055, 0116

warpage during printing encapsulation, low-stress encapsulants have been developed [39].

Reduction in internal stress of the encapsulant material can be achieved by modifying the standard epoxy resins with special elastomers such as silicone [39]. In a study by Okuno et al., the internal stresses of two types of epoxy systems were compared. The standard epoxy resin used for general electronic packaging showed a linear increase in internal stress as the material cooled from curing temperature, whereas the elastomer-modified epoxy material exhibited an overall lower stress value, and a much slower stress increase rate during cooling below T_g. Because of this low-stress property, the elastomer-modified epoxy systems will be less susceptible to warpage during printing encapsulation process as it cools down from curing temperatures.

2.7 Environmentally Friendly or "Green" Encapsulants

The global movement toward environmentally friendly materials began in the 1980s in Europe, which later expanded to Asia and North America. Numerous studies have revealed the hazardous and toxic effects of traditional flame retardants on the environment and health. As a consequence, the toxic flame retardants have been restricted or removed, and new environmentally friendly or "green" encapsulant materials have emerged to be free of any toxic substance. In this section, first, the toxic flame retardants are discussed and their hazardous effects on the environment are described. Then, green encapsulant material development and challenges are discussed.

2.7.1 Toxic Flame Retardants

Brominated organic compounds and antimony trioxide traditionally used in molding compounds as flame retardants are known to have deleterious impacts on the environment [40]. Brominated flame retardants (BFRs) are also referred to as halogenated flame retardants due to the presence of bromine (Br^-) which is considered a halogen. Halogens are nonmetal elements from Group 17 in the new periodic table including fluorine, chlorine, bromine, iodine, and astatine.

The other substance of concern in conventional flame retardant systems is antimony trioxide. Antimony trioxides are used as synergists to increase the activity of halogenated flame retardants by hindering the chain

Petitioner Samsung Ex-1055, 0117

reaction of the flame gas phase through stepwise release of the halogenated radicals [41].

BFRs, particularly polybrominated biphenyls (PBBs), polybrominated diphenyl ethers (PBDEs), and tetrabromobisphenol A (TBBPA) contain one or more carbon rings, making them very stable. Figure 2.29 shows the chemical structure of a PBDE, PBB, TBBPA, and hexabromocyclododecane. The chemical stability of these substances is a principal reason why BFRs have been the focus of international environmental debate.

BFRs accumulate in the food chain, and it is impossible to avoid dispersal into the environment by implementing treatment measures exclusively at point sources such as wastewater or air emissions [42]. Thus, the pollution occurs as both diffuse pollution and point-source pollution from the locations where the products are handled. Several studies also suggest possible dispersal of BFRs into the marine environment as well as into the air through evaporation [43–45].

Studies have measured rising levels of PBDEs in marine environments [46], human breast milk, adipose tissue, and blood [47], raising concerns because of PBDE's structural similarity to thyroid hormones [48]. Dutch reports of PBDE in sperm whale blubber suggest that the substances have

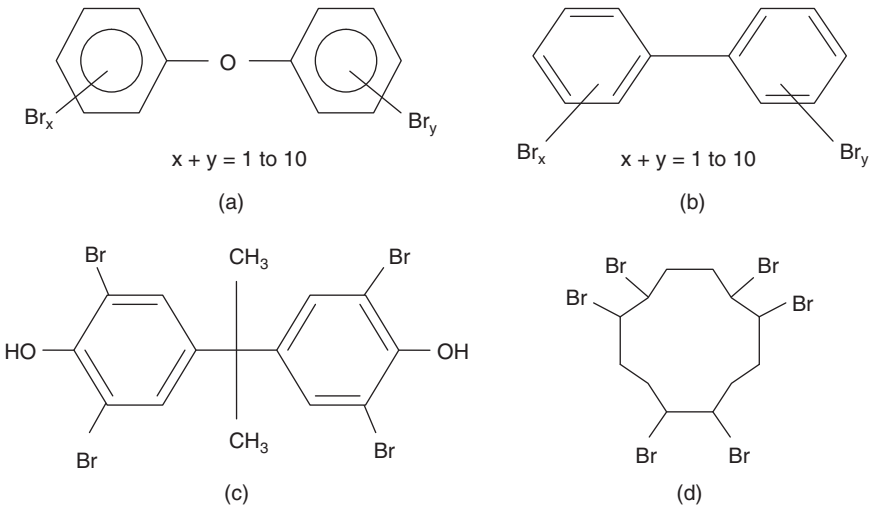


Figure 2.29 The chemical structure of: (a) polybrominated diphenyl ethers and (b) polybrominated biphenyl, where x + y can range from 1 to 10; (c) tetrabromobisphenol A; and (d) hexabromocyclododecane.

Petitioner Samsung Ex-1055, 0118

permeated the food chain in the open sea far from the primary source [49]. Measurements in seals from the North Sea and Baltic Sea show that coastal fauna is also subject to considerable exposure to PBDEs. PBDE has also been detected in fish from the Baltic Sea. Measurements in birds, seals, and whales from the Arctic and the Faroe Islands also show that BFRs have dispersed far into the environment [50]. A Finnish study shows that the concentration increases with age, which is in accordance with the properties of these substances [51].

The principal health risks of BFRs are associated with long-term effects. Antimony trioxide has been shown to have both short-term and long-term effects [52]. Table 2.25 provides toxicity of major BFRs and antimony trioxide. Among the PBDEs, the three major compounds used in North

Table 2.25 Toxicity of BFRs and Antimony Trioxide [40]

Substance	Toxicity
Deca-BDE	• Neurodevelopmental damage • Liver and thyroid tumors
Octa-BDE	• Increases liver and thyroid weight • Decrease in thyroid hormone levels
Penta-BDE	• Neurodevelopmental toxicity • Decrease in thyroid hormone levels
HBCD	• Neurodevelopmental toxicity • Interference with brain neurotransmitters • Interference with thyroid hormone
TBBPA	• Toxic to liver cells and immune system (T cells) • Interference with thyroid hormone • Inhibition of brain neurotransmitters
Antimony trioxide	• Irritation of skin, eyes, respiratory tract • Skin rash with pustules around the sweat and sebaceous glands known as “antimony spots” • Inflammation of the lungs, chronic bronchitis, and chronic emphysema • Increase in incidence of spontaneous abortions and adverse reproductive effects • Possible human carcinogen

BFR: Brominated flame retardant; Deca-BDE: Decabromodiphenyl ether; HBCD: Hexabromocyclododecane; Octa-BDE: Octabromodiphenyl ether; Penta-BDE: Pentabromodiphenyl ether; TBBPA: Tetrabromobisphenol A.

Petitioner Samsung Ex-1055, 0119

America are decabromodiphenyl ether, octabromodiphenyl ether, and pentabromodiphenyl ether.

Brominated dioxins, in particular polybrominated dibenzodioxins (PBDDs) and polybrominated dibenzofurans (PBDFs), can be formed through the incineration of wastes or combustion of consumer products containing BFRs [52]. BFRs may also contain small amounts of brominated dioxins as impurities. Due to their high toxicity and potential for bioaccumulation, PBDDs and PBDFs [53] are of major concern. According to the Environmental Protection Agency (EPA), the toxic responses of dioxins may include dermal effects, immunotoxicity, carcinogenicity, and reproductive and developmental toxicity.

The European Parliament called for the ban of all PBDEs by 2006 [47,54]. The World Health Organization (WHO) and the US EPA also recommend exposure limits and risk assessment of dioxins and similar compounds [52,55]. The European Union (EU) has proposed restricting the use of brominated biphenyl oxide flame retardants because highly toxic and potentially carcinogenic brominated furans and dioxins may form during combustion [47]. Table 2.26 provides a timeline of actions taken on BFRs (www.cleanproduction.org; www.ospar.org).

TBBPA, which is a widely used reactive flame retardant, has not conclusively been found to be a risk to the environment or human health. As part of its International Program on Chemical Safety, WHO undertook a full scientific assessment of the environmental and human health impacts of TBBPA. This study determined that TBBPA had little potential for bio-accumulation and therefore the environmental and health risks should be insignificant. The EU's risk assessment of TBBPA is currently ongoing [54]. However, the levels of TBBPA in human milk have been found to be increasing over time. In addition, the results of studies [56] suggest that TBBPA, just as PBDEs and PBBs, have the potential to replace thyroid hormones and detrimentally affect human health and behavior.

To address health concerns and the recyclability of products containing BFRs, the European Commission adopted a directive on Waste from Electrical and Electronic Equipment (WEEE) and a directive on the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment. The RoHS directive that took effect on July 1, 2006, restricts the use of six hazardous materials: lead, mercury, cadmium, chromium (VI), PBB, and PBDE [57]. The maximum concentration allowed for each substance is 0.1% (except for cadmium which is limited to 0.01%) by weight of homogeneous material.

Petitioner Samsung Ex-1055, 0120

Table 2.26 Timeline of Actions Taken on BFRs (www.cleanproduction.org; www.ospar.org) [58]

Year	Country/ Organization	Action
1989	Germany	Industrial users voluntarily agree to a phase-out of PBDEs
1989	Netherlands	Industrial users voluntarily agree to a phase-out of PBDEs and PBBs
1992	OSPAR	Places BFRs on List of Chemicals for Priority Action; recommends urgent elimination of PBDEs and PBBs
1993	Germany	PBDEs banned due to dioxin regulations
1995	North Sea	Environment Ministers commit to BFR substitution with less hazardous alternatives
1999	Sweden	Swedish Chemicals Inspectorate (Keml) recommends phase-out of PBDEs and PBBs within five years with eventual phase-out of all BFRs as part of a non-toxic future
1999	World Health Organization	Recommends that BFRs "should not be used where suitable replacements are available"
2000	OECD	Joint Meeting of the Chemicals Committee and Working Party on Chemicals accepts bromine industry's voluntary agreement to end PBB production
2003	Austria	Advocates ban on Deca-BDE
2003	Norway	Pollution Control Authority requires companies to submit reduction and phase-out plans for BFRs
2003	Netherlands	Prohibits production of bis(2,3-dibromopropyl) TBBPA
2004	EU	Deca-BDE undergoing debate
2004	Norway	Ban on Penta- and Octa-BDE
2004	USA	Volunteer phase-out of Penta- and Octa-BDE by manufacturers
2005	Norway	Ban on Deca-BDE, HBCD, and TBBPA
2006	EU	RoHS Directive banning Penta-, Octa-, and Deca-BDE in all electrical and electronic equipment sold or imported into the EU, but later removed ban on Deca-BDE
2006	Japan	Japanese RoHS (in compliance to EU RoHS) restricting the use of hazardous substances including PBB and PBDE

(*Continued*)

Petitioner Samsung Ex-1055, 0121

Table 2.26 Timeline of Actions Taken on BFRs (www.cleanproduction.org; www.ospar.org) [58] (*Continued*)

Year	Country/ Organization	Action
2006	Maine, USA	Ban on Penta- and Octa-BDE
2007	California, USA	Following EU RoHS directive, restricting the use of hazardous substances including PBB and PBDE
2007	China	Chinese RoHS (similar to EU RoHS) restricting the use of hazardous substances including PBB and PBDE
2008	EU	Re-instated ban on Deca-BDE
2010	Maine, USA	Initial ban on Deca-BDE extended to electronics
2020	OSPAR	Phase-out goal for all BFRs

BFR: Brominated flame retardant; Deca-BDE: Decabromodiphenyl ether; HBCD: Hexabromocyclododecane; Octa-BDE: Octabromodiphenyl ether; PBB: Polybrominated biphenyl; PBDE: Polybrominated diphenyl ether; Penta-BDE: Pentabromodiphenyl ether; RoHS: Restriction of the use of certain Hazardous Substances; TBBPA: Tetrabromobisphenol A.
Source: Cleanprodution.org; OSPAR (www.ospar.org/).

These waste-disposal regulations require separate and controlled disposal of halogen-containing scrap [59], such as personal computers. In addition, Austria and Switzerland have completely banned the use of PBB. In Germany and the Netherlands, voluntary agreements have been made concerning the phasing out of PBB and PBDE. Germany required the content of dioxins and furans in products to stay below certain limits, which has reduced the use of PBDE and PBB [60,61]. The Chemicals Inspectorate in Sweden has proposed to completely phase out BFRs, and the Swedish TCO 95 label used on computers requires that no organically bound bromine be used in parts weighing more that 25 grams [62].

2.7.2 Green Encapsulant Material Development

Environmentally friendly or "green" encapsulant materials are materials that are free of toxic flame retardants. The level of environmental

Petitioner Samsung Ex-1055, 0122

friendliness in electronic packages, however, may vary depending on the substances restricted or removed. Table 2.27 lists different levels of "green" packaging [63].

Molding compound manufacturers and the electronic packaging industry are highly active in the research and development of green encapsulants and have published many relevant studies on this topic [44,64–79]. A general and widely used approach for the development of green molding compounds is presented in Fig. 2.30.

The development of green molding compounds is initiated by the restriction or removal of the conventional toxic substances including BFRs and antimony trioxide synergists from the conventional molding compound. In the absence of conventional flame retardants, the flame resistance of the new green material can be achieved by three distinct approaches: (1) change resin/hardener structure, (2) increase filler content, and/or (3) use non-halogenated flame retardants. These three approaches can be implemented independently or concurrently. Based on the development approach, green materials can be further classified into two groups: (a) green materials with non-halogenated flame

Table 2.27 Limits for "Green" Packaging and Assembly Materials [63]

Green Level	Element/Compound	Limit (ppm)
Lead free	Lead	1000
RoHS compliant	Lead	1000
	Mercury	1000
	Cadmium	100
	Chromium (VI)	1000
	Polybrominated biphenyl	1000
	Polybrominated diphenyl ether	1000
Fully green	All of above plus:	
	Bromine	900
	Chlorine	900
	Antimony	900
	TBTO	Not used
	Phosphorus	Not used

RoHS: Restriction of the use of certain Hazardous Substances; TBTO: Tributyltin oxide.

Petitioner Samsung Ex-1055, 0123

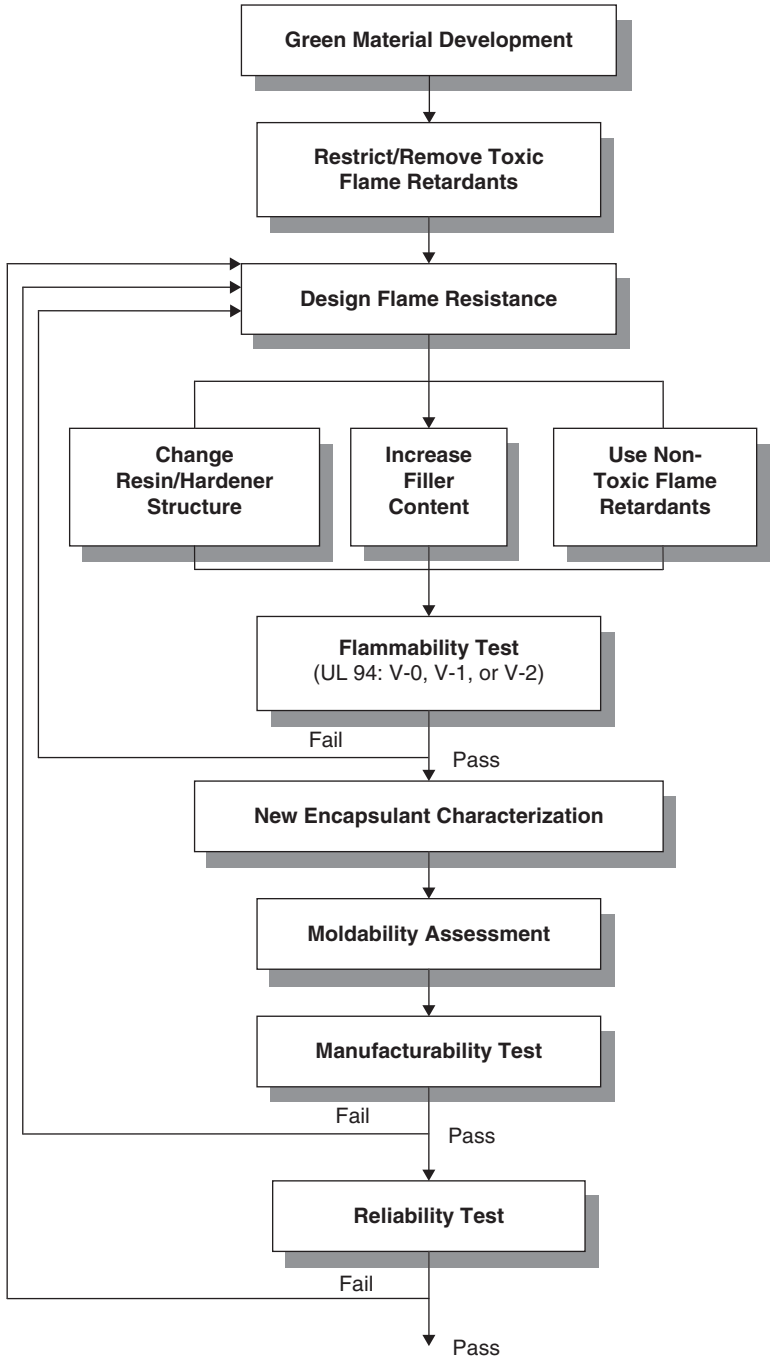


Figure 2.30 General approach to green material development.

Petitioner Samsung Ex-1055, 0124

retardants and (b) green materials without flame retardants (self-extinguishing).

Upon the synthesis of the green encapsulant material, the flame retardancy of the new material must be evaluated by conducting the UL-94 flammability test. The flame retardancy ratings are generally based on the UL vertical burning test (i.e., V-0, V-1, and V-2). If the green material fails the flammability test, it must undergo a redesigning process, which may include further modifying the resin structure, filler content, and/or an alternative flame retardant system.

After passing the UL-94 test, the green encapsulant material is characterized and various critical properties that can affect the manufacturing quality and package reliability are measured. These properties may include adhesion strength, flexural strength, moisture absorption, and thermomechanical properties. The material properties attained at this stage may be indicative of improved or deteriorated manufacturability and reliability of the encapsulated package; for example, reduction in moisture sorption characteristics may reveal higher package reliability. However, for more definitive manufacturability and reliability assessment, the encapsulated packages must undergo specific moldability, manufacturability, and reliability tests.

In moldability testing, potential molding defects are identified and the severity of the defects is measured. The encapsulation defects may include package warpage (out-of-plane deformation or non-coplanarity), wire sweep (wire deformation during molding), external voids (caused by air entrapment during encapsulation), and delamination (debonding or de-adhesion of encapsulant from the adjacent material). The encapsulation defects will be discussed more comprehensively in Section 5.2 (Chapter 5).

The manufacturability of the encapsulated packages is directly related to the occurrence and severity of the encapsulation defects. For example, packages with lower warpage after molding and post-mold curing have been shown to exhibit higher percentage yield [74]. The commonly selected test areas from the assembly line for manufacturability evaluation and percentage yield tests include molding, marking, lead trimming/forming, solder ball placement (for BGA packages), and saw singulation (for wafer-level packages) [66,74].

After moldability and manufacturability tests, the packages encapsulated with green material are subjected to reliability testing. Among the widely used reliability tests are moisture sensitivity level test, thermal cycling test, and highly accelerated stress test. More details on reliability tests for electronic packages are provided in Chapter 7.

Petitioner Samsung Ex-1055, 0125

2.7.2.1 Green Materials with Non-Halogenated Flame Retardants

Many manufacturers, including Nikko Denko, Sumitomo Bakelite, and Shin-Etsu Chemical have developed green molding compounds with alternative non-toxic flame retardants. Several options for non-halogenated (non-brominated) flame retardants have been explored. Figure 2.31 shows organic and inorganic non-toxic flame retardants considered for new green compounds. Non-halogenated inorganic flame retardants include metal hydrates, metal oxides, ammonium polyphosphates, and red phosphorus. Organic non-halogenated flame retardants include organophosphates and nitrogen-based compounds.

The mechanisms of flame retardants vary based on the type of chemical reactions. In general, flame retardants can retard the flaming and burning of the compound by trapping the essential chemical elements for the burning reaction, by blocking oxygen through formation of char, or by generating water. Figure 2.32 illustrates the flame retardancy mechanisms for

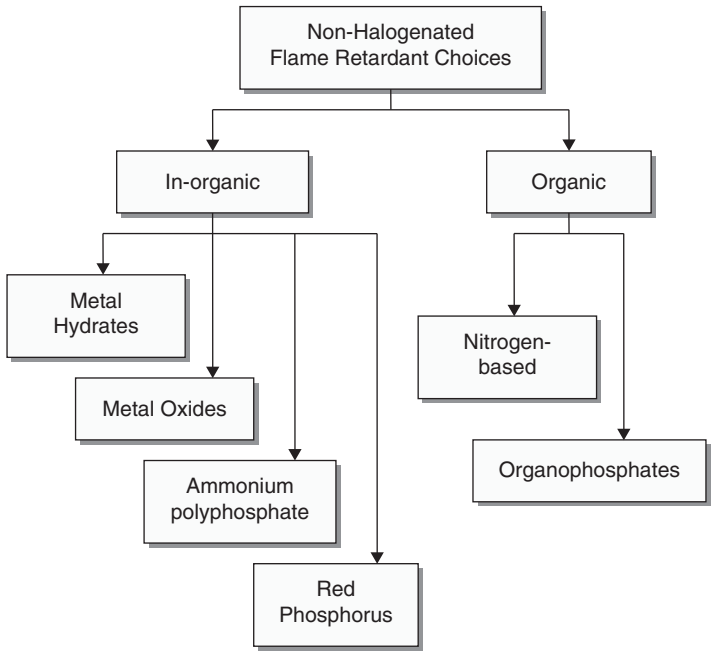


Figure 2.31 Choices of non-toxic flame retardants.

Petitioner Samsung Ex-1055, 0126

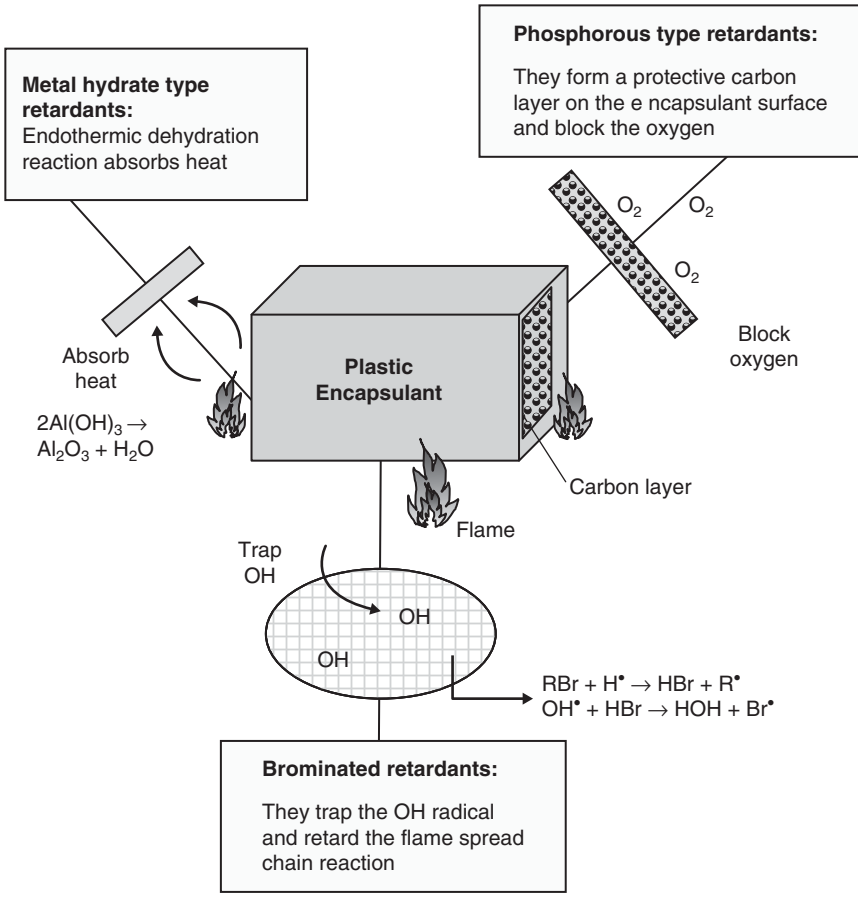


Figure 2.32 Comparison of mechanisms in three different flame retardant systems: brominated, metal hydrate, and phosphorous type.

three types of flame retardants [65]: metal hydrate, phosphorus-based, and conventional toxic brominates.

Table 2.28 lists five different non-halogentaed flame retardant types including phosphorus-based, nitrogen-based, metal hydrates, metal oxides, and high carbon/hydrogen ratio resins (highly aromatic). The main flame retardant substances from each group, the mechanisms of flame retardancy, advantages, and disadvantages are provided [65,67,69].

A non-halogenated flame retardant group under special scrutiny is the red phosphorous flame retardants. It has been shown that if red phosphorus is not sufficiently coated, it can cause failure in semiconductor devices [44,80,81]. During the late 1990s to 2002, Sumitomo Bakelite developed

Petitioner Samsung Ex-1055, 0127

Table 2.28 Advantages and Disadvantages of Non-halogenated Flame Retardant Systems [65,67,69]

Type	Main Materials	Mechanism	Advantage	Disadvantage
Phosphorous	• Poly ammonium phosphate • Phosphoric ester • Red phosphorous	• Formation of char, blocking oxygen	• Good flame retardation	• High water absorption • Decrease in electrical properties • Red phosphorus can lead to reliability problems
Nitrogen	• Melamine • Cyanuric acid derivative	• Formation of "fluffy" or expanded char, insulating the substrate	• Reduced smoke	• Poor flame retardation • High amount required (reduced spiral flow, strength)
Metal hydrate	• Aluminum hydroxide • Magnesium hydroxide • Borate	• Discharge of water which can cover the surface • Formation of char layer	• Good HTSL • Applicable to all epoxy/phenolic systems • Magnesium hydroxide has an activation temperature of about 350°C, suitable for reflow process (>220°C)	• Poor flame retardation • Aluminum hydroxide has relatively low activation temperature (180–200°C), not suitable reflow process (>220°C) • High amount required (reduced spiral flow, strength) • Higher filler loading can compromise electrical and physical properties

(*Continued*)

Petitioner Samsung Ex-1055, 0128

Table 2.28 Advantages and Disadvantages of Non-halogenated Flame Retardant Systems [65,67,69] (*Continued*)

Type	Main Materials	Mechanism	Advantage	Disadvantage
Metal oxide	• Molybdenum compound (transition metal oxide)	• Hydrogen extract • Formation of char layer	• Good HTSL • Reduced smoke • Good ball bond strength retention • Applicable to all epoxy/ phenolic systems	• Good dispersion needed for flame retardation
High carbon/ hydrogen ratio resins (highly aromatic)	• Some biphenyl types • Some naphthalene types	• Formation of char and blocking oxygen	• Good flame retardation with high filler content • Improved reflow crack resistance	• Poor reactivity • High cost

HTSL: High-temperature storage life.

Petitioner Samsung Ex-1055, 0129

and marketed a series of green molding compounds, known as EME-U series, which consisted of stabilized red phosphorus as the flame retardant. However, this flame retardant caused serious failures to the package devices, due to the insufficient stabilization of the red phosphorus. The molding compounds with red phosphorus flame retardant were phased out in 2002.

The insufficient coating of red phosphorus flame retardant fillers can lead to the formation of phosphoric ions and acids, which can serve as electrolyte and cause electrochemical migration of the lead material (Fig. 2.33) [81]. The migrated lead material can form an unwanted conductive path and can cause a resistive short and leakage current failure between leads within the package. It can also cause an increase in electrical resistance and opening of the wire bonds. Such problems with new and alternative flame retardant materials for environment friendly molding compounds can be avoided by adequate evaluation and qualification testing.

Phosphorous-based flame retardants in general are considered to be less environmentally friendly compared to other non-halogenated flame retardants. If added to water in lakes and rivers, phosphorus can lead to higher production of algae and aquatic plants. As these algae die, during the

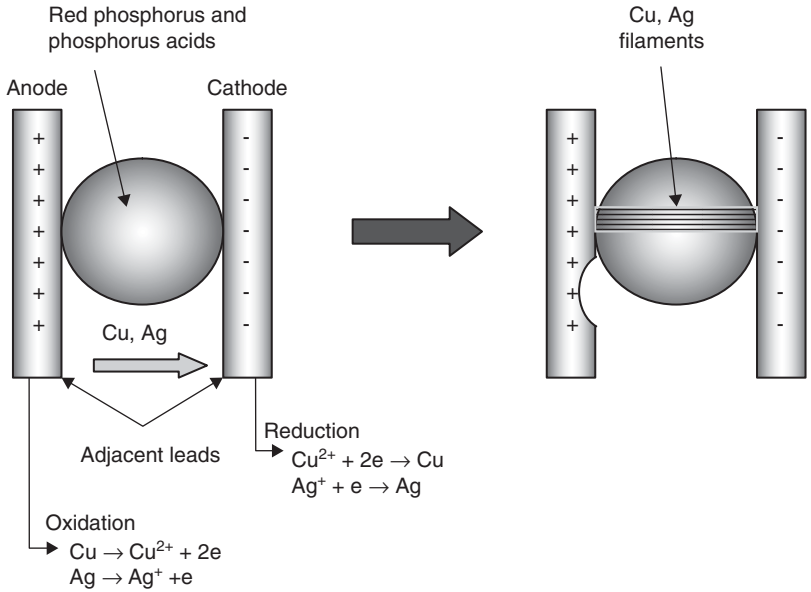


Figure 2.33 Electrochemical reactions at the inner adjacent leads and the formation of copper and silver filaments between the leads [81].

Petitioner Samsung Ex-1055, 0130

process of decomposition by bacteria, higher amount of oxygen may be consumed. This process is referred to as eutrophication. The potential eutrophication by phosphorous-based flame retardants may lead to killing of fish and other biological systems in need of oxygen [72,82]. Phosphates, however, are not toxic to people or animals unless they are present at very high levels, causing digestive problems [82].

In addition to environmental issues, phosphorus-based flame retardants in general have higher moisture sorption characteristic leading to reliability problems in encapsulated packages [72]. The combination of potential environmental and reliability problems has rendered phosphorus-based substances to be less desirable as flame retardants. Thus, the criteria for green encapsulant material development for many manufacturers have extended to bromine-free, antimony-free, and phosphorus-free [63,72,74,83,84].

Sumitomo Bakelite Co., Ltd., has developed green epoxy resin molding compounds under the brand name Sumikon® EME, including E500, E600, G500, G600, and G700 series (Table 2.29). The EME encapsulant materials listed in Table 2.29 are free of bromine-, antimony-, and phosphorous-based flame retardants.

Loctite (Henkel) has developed green molding compounds under the brand name "GR series." Table 2.30 lists the green compounds with nontoxic flame retardants and high temperature stability, their applications, and properties [83].

The green molding compounds developed by Shin-Etsu Chemical Co., Ltd., incorporate a silicone flame-resisting system in place of the antimony compounds and brominated epoxy resins. These compounds successfully satisfy UL-94, V-0 (the highest level in UL). Shin-Etsu Chemical markets the products under the brand name "KMC-2000 Series" (Table 2.31).

Nitto Denko's green molding compounds are under the brand name "GE series" derived from the conventional "MP series." Table 2.32 lists green compounds suitable for lead-frame packages and their features (Nitto Denko Corporation, http://www.nittoeurope.com/). The Nitto Denko GE series molding compounds use metal hydroxide flame retardants [77]. The green compounds for BGA packages belong to grade "GE-100 series."

2.7.2.2 Green Materials without Flame Retardants

A group of green encapsulant materials have been developed that do not contain any flame retardants. Figure 2.34 shows the self-extinguishing mechanism in a type of green compound developed by Nippon

Petitioner Samsung Ex-1055, 0131

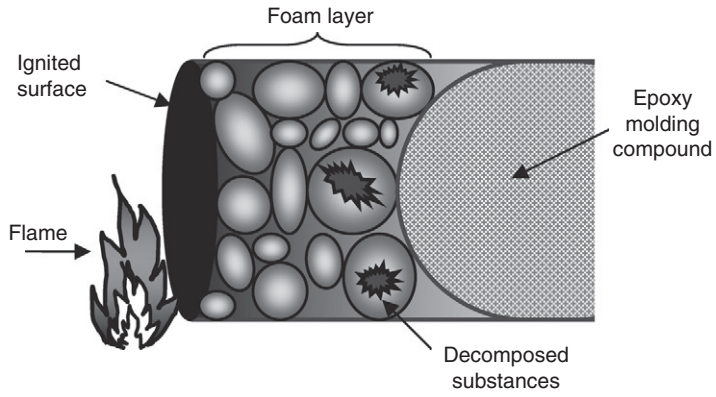


Figure 2.34 Self-extinguishing mechanism for an environmentally friendly epoxy molding compound from NEC without flame retardants [85].

Table 2.29 Sumitomo Bakelite Green Molding Compounds

Grade	Features	Main Applications
EME-E500	Low pin count device	DIS, DIP, SO
EME-E590	High thermal conductivity	TO-220F
EME-E630	Low stress	DIP, SO, PLCC, QFP
EME-E670	Ultra low stress	DIP, SO, power module
EME-G500	Low pin count device	DIP, SO, PLCC, QFP
EME-G600	Standard	DIP, SO, PLCC, QFP
EME-G620	Better MSL	DIP, SO, PLCC, QFP
EME-G630	Standard	DIP, SO, PLCC, QFP
EME-G700	Best MSL	DIP, SO, PLCC, QFP
EME-G750	EME for laminate package; low warpage	BGA, CSP
EME-G760	Standard EME for laminate package; long flow	BGA, CSP
EME-G770	Standard EME for laminate package; better MSL	BGA, CSP
EME-G790	Next generation EME for laminate package; low warpage; long flow	BGA, CSP

BGA: Ball-grid array; CSP: Chip scale package; DIP: Dual in-line package; MSL: Moisture sensitivity level; PLCC: Plastic-leaded chip carrier; QFP: Quad flatpack; SO: Small-outline.
Source: http://www.sumibe.co.jp.

Petitioner Samsung Ex-1055, 0132

Table 2.30 Green Molding Compounds from Loctite [34]

Product	Description	T_g (°C)	CTE1 (ppm/°C)	CTE2 (ppm/°C)	Flexural Modulus (MPa)	Flexural Strength (GPa)	Moisture Absorption (85°C/ 85% RH, 168 hrs)	260°C Reflow Profile
MG15F-MOD11	Asymmetric and surface-mount packages, high T_g, low stress power CSP	235	14	55	17.00	120	0.37	J1
GR330	Low cost, through-hole discrete diodes, and IC	150	19	50	17.00	139	0.40	
GR360	High performance, good reliability, low cost, applicable for low pin count PDIP ICs	170	19	65	16.90	140	0.045	
GR380	SMD, PDIP, SOIC packages and QFP; low stress, high voltage rectifier, power discrete and small-outline transistors	160	17	70	13.50	130	0.35	
GR625	Surface-mount discrete, IC, QFP, passes JEDEC Level 1, 260°C reflow	140	13	40	17.50	130	0.25	J1
GR640	Designed for small signal and small-outline transistors, high speed auto-mold, fast cure	165	21	65	16.20	155	0.80	J2
GR725	Automotive (20,000 hrs @ 185°C), designed for surface-mount discrete packages operating at high temperature	135	12	35	20.00	116	0.28	J1

Petitioner Samsung Ex-1055, 0133

GR750	High thermal conductivity, designed to improve thermal management for semiconductor devices, high adhesion to copper and copper alloys	160	23	70	19.70	120	0.90	
GR828	Specifically designed for SO packages up to TSSOP/TQFP	145	13	45	18.00	127	0.25	J1
GR9800	Designed for flip-chip in-array package application; applicable for underfill and overmolding flip-chip assemblies with gap sizes as low as 40 μm	200	14	48	14.50	110	0.40	J2
GR9810	Laminate-based packages; designed for use as an overmold; low warpage	195	11	35	23.00	120	0.30	J2
GR9820	Matrix QFN, very low stress, ultra low warpage, adhesion can be optimized for specific lead-frame metallization	195	11	35	21.80	110	0.31	J1
GR9825	Single cavity QFN lead-frame packages	145	13	45	18.00	127	0.25	J1
GR9840	Designed for smart card applications requiring excellent molding through small gate areas	165	21	65	16.2	155	0.80	

CSP: Chip scale package; CTE: Coefficient of thermal expansion; IC: Integrated circuit; JEDEC: Joint Electron Devices Engineering Council; PDIP: Plastic dual in-line package; QFN: Quad flat no-leads; QFP: Quad faltpack; SMD: Surface-mount device; SO: Small-outline; SOIC: Small-outline integrated circuit; TQFP: Thin quad flatpack; TSSOP: Thin shrink small-outline package.

Note: Typical property values; not to be used as specifications.

Source: http://www.loctite.com/int_henkel/loctite/binarydata/pdf/lt3758a_SemiMoldComp.pdf.

Petitioner Samsung Ex-1055, 0134

Table 2.31 Green Epoxy Molding Compounds from Shin-Etsu [86]

Application Design and Materials	PBGA Package					L/F Package		
	Laminate		BOC	Ceramic	QFN	PPF	Cu–Ag	Alloy 42
	Rigid	Tape						
MSL 1-2 at 260°C								
KMC-2520	*	*	*	*	*			
KMC-2520L	*	*		*	*			
KMC-2260G-1								*
KMC-284		*					*	*
MSL 2-3 at 260°C, high T_g								
KMC-2210G	*	*						
KMC-2210G-8T	*	*	*	*	*			
KMC-2212G	*	*		*	*			
MSL 1-3 at 260°C, standard								
KMC-2110G							*	*
KMC-2160G						*	*	

BOC: Board-on-chip; L/F: Lead-frame; MSL: Moisture sensitivity level; PBGA: Plastic ball-grid array; PPF: Pre-plated finish; QFN: Quad flat no-leads.

Petitioner Samsung Ex-1055, 0135

Table 2.32 Nitto Denko Green Molding Compounds for Lead-Frame Packages

Product	Chemistry	Features
GE-7470-A	Biphenyl	Higher MSL for PPF and Cu L/F
GE-7470L-AW	Biphenyl	For long wire
GE-7470L-B44	Biphenyl	Higher MSL for silver plate
GE-1030	Biphenyl	Low cost solution
GE-200	OCN	Low cost for small packaging
GE-880	OCN	Low cost for surface-mount device packaging

L/F: Lead-frame; MSL: Moisture sensitivity level; OCN: Ortho-cresol novolac; PPF: Pre-plated finish.
Source: http://www.nittoeurope.com/.

Electric Company, Ltd. (NEC) without flame retardant [85]. Upon ignition, the green molding compound immediately produces a stable foam layer that hinders heat transfer during combustion and extinguishes itself. The self-extinguishing green molding compound consists of phenol–aralkyl type epoxy resin filled with 70% fused silica powder. The resin and hardener both include a multi-aromatic group in their main chain.

An important characteristic of the green molding compound developed by NEC that contributes to the self-extinguishing mechanism is the low elasticity of the compound at high temperature. The volatile materials from inside the compound at high temperature cause the surface materials to transform into a foam layer. The low elasticity of the green compound may be attributed to the low cross-link density of the epoxy resin and hardener network due to the added multi-aromatic group. Also, the high stability of the foam layer can be attributed to the high pyrolysis resistance of the green compound.

Kyocera Chemical has also developed a type of green molding compound for automotive applications (“Perfect Green”) which does not contain any alternative flame retardant, such as phosphine compound and which is claimed to have excellent heat resistance and thermal cycle reliability [87]. The flame resistance of the green compounds was achieved by (a) modifying the molecular structure of matrix resin and (b) increasing the filler loading in the molding compounds.

Petitioner Samsung Ex-1055, 0136

2.8 Summary

This chapter presented the basic plastic encapsulant materials used in electronic packaging including molding, glob-top, potting, underfill, and printing encapsulants. The chemistry of the encapsulant materials was discussed. Epoxies are the most common molding compound materials. Silicones, polyurethanes, and phenolics are other types of primary encapsulant materials. Additives are materials added to the molding compounds to achieve various functions and properties and may include hardeners, accelerators, fillers, coupling agents, stress-relief materials, flame retardants, mold-release agents, ion-trapping agents, and coloring agents.

Some of the commercially available encapsulant products from leading manufacturers were discussed including Nitto Denko, Sumitomo Bakelite, Plaskon, Loctite (Henkel), General Electric, Dow Corning, and Shin-Etsu. The environmentally hazardous effects of conventional flame retardants in molding compounds were mentioned, and environmentally friendly "green" materials free of halogenated flame retardants and antimony trioxide were discussed.

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Petitioner Samsung Ex-1055, 0139

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Petitioner Samsung Ex-1055, 0141

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Petitioner Samsung Ex-1055, 0142

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3 Encapsulation Process Technology

Encapsulation techniques used in electronic applications can be classified into five main technologies: molding, glob-topping, potting, underfilling, and printing. Figure 3.1 shows the types of encapsulation technologies. The selection of a suitable encapsulation method generally depends on several factors including equipment and labor cost, production volume, molding cycle, application requirements, package reliability, encapsulant material, and package type. Furthermore, package-related factors that can affect the choice of encapsulation technique include package thickness, dimensional control, presence of intricate parts, small cavities or narrow spaces, array packaging, warpage control, 2D or 3D packaging, wafer-level or chip-level packaging, and interconnection type (i.e., solder balls, leads).

3.1 Molding Technology

Several molding techniques are available for the encapsulation of microelectronic packages. The most widely used is the transfer molding process; others include injection molding, reaction-injection molding, and compression molding.

3.1.1 Transfer Molding

The transfer molding process is the most common encapsulation method for essentially all plastic packages in integrated circuit technology. Transfer molding is a process of encapsulating microelectronic devices in a closed mold using a thermosetting material that is transferred under pressure. Thermosets are polymers that are fluid at low temperatures and react irreversibly when heated to form a cross-linked network no longer capable of being melted. Figure 3.2 depicts the transfer molding process. The preheated molding compound—preform (pellet)—is placed in an auxiliary chamber, called the transfer pot, and is forced by the transfer plunger to flow through runners and gates into the closed cavity or cavities.

The transfer molding process offers several advantages over other molding techniques. Due to the extreme high pressure involved during the injection molding process, transfer molding is more suitable for the encapsulation of intricate parts with inserts. Encapsulation by transfer molding is also less prone to wire sweep.

Petitioner Samsung Ex-1055, 0144

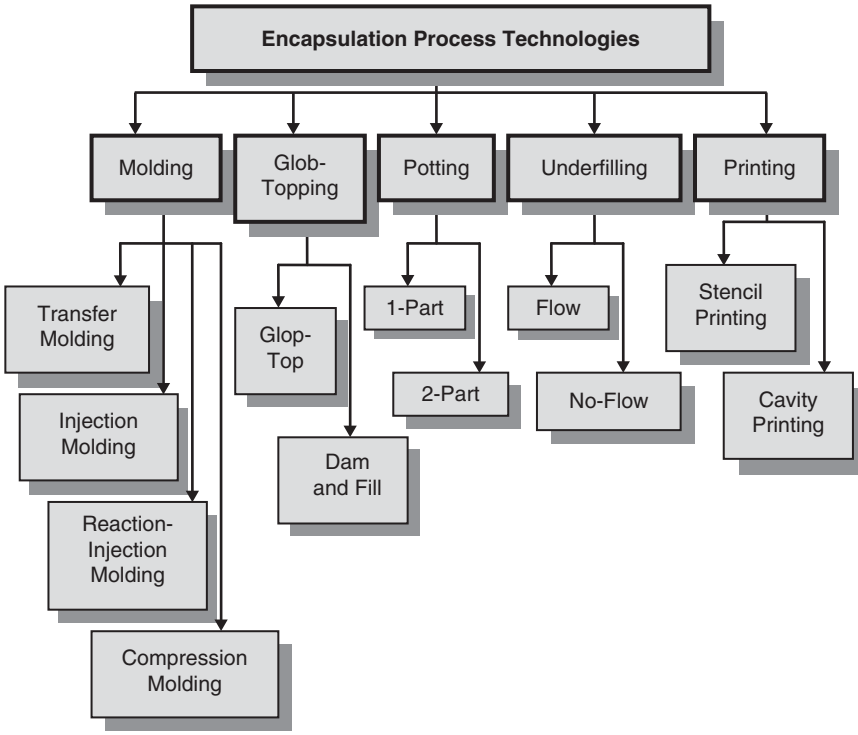


Figure 3.1 Types of encapsulation technologies.

The transfer molding process is also more suitable for high production volume and short loading and molding cycle. Transfer pots can be connected to multiple runners for simultaneous molding of the parts; therefore, fewer and larger molding compound preforms need to be loaded into the transfer pot with relatively shorter loading times compared to multiple transfer pots with fewer runners.

The transfer molding technique generally requires low tool and maintenance costs. Deep loading wells are not necessary in transfer molding, and the mold sections can be made thinner because the stresses involved during closing of the mold are lower. The wear of the molds is also lower in transfer molding and the tendency toward breakage of pins is less. As the encapsulated components are produced in closed molds, which are subjected to less mechanical wear and erosion by the molding material, closer tolerances on all molded dimensions are possible in transfer molding.

One of the main limitations of the transfer molding process is the amount of scrap material. The material left in the pot and also in the sprue and runner is irreversibly reacted (cross-linked) and must be discarded.

Petitioner Samsung Ex-1055, 0145

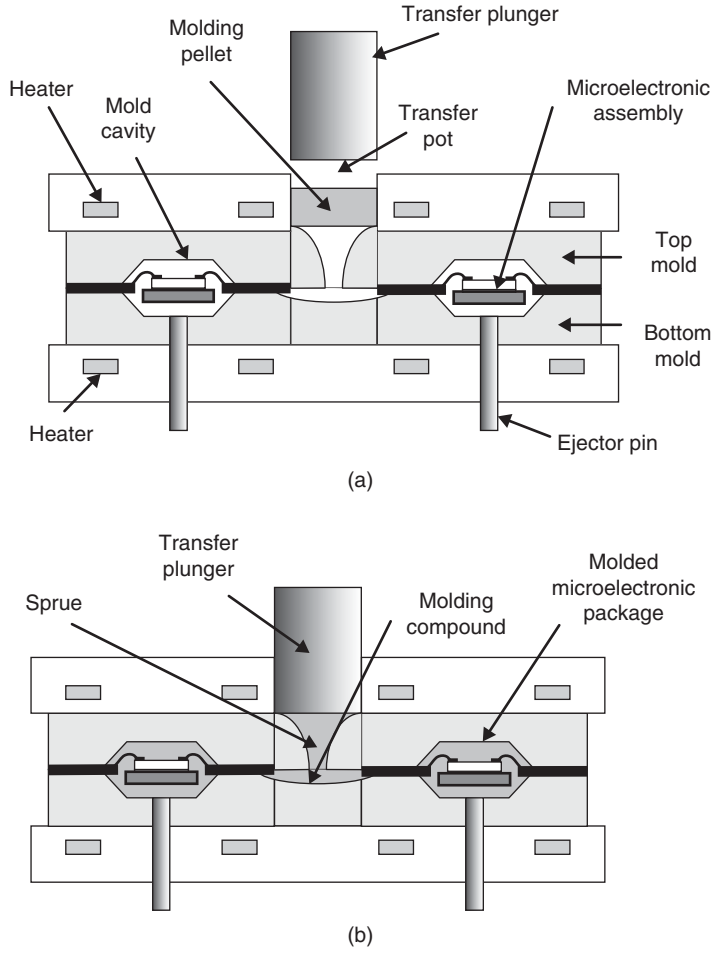


Figure 3.2 Encapsulation by transfer molding: (a) before molding; (b) after molding [1,2].

This is unavoidable and for small articles, it represents a sizable percentage of the weight of the pieces molded. However, in the fully automatic transfer molding presses employed for electronic parts, the savings elsewhere, including mold costs and finishing costs, usually offsets the loss of material.

3.1.1.1 Molding Equipment

Transfer molding requires four key pieces of capital equipment: a preheater, a press, the die mold, and a cure oven. The transfer molding press

Petitioner Samsung Ex-1055, 0146

is normally hydraulically operated. Auxiliary ram-type transfer molds are commonly used in transfer molding.

The mold has a built-in transfer pot separate from the mold cavities as shown in Fig. 3.3. The molding compound is placed in the pot. Both the volume and the size of the molding compound preforms have to be appropriately selected for the press capacity. The mold is then clamped. The transfer plunger is activated to apply the transfer pressure to the molding compound. The molding compound is driven through the runners and gates into the cavities. Figure 3.3(a) shows the top view of a transfer molding setup design with multiple transfer pots and plunger where each transfer pot is connected to only two cavities. Figure 3.3(b) shows a single transfer pot and plunger connected to multiple cavities.

Since the 1980s, aperture-plate and multi-plunger molds have been the dominant approaches to plastic-encapsulated microelectronics (PEMs) molding. Table 3.1 compares the features of these molding methods.

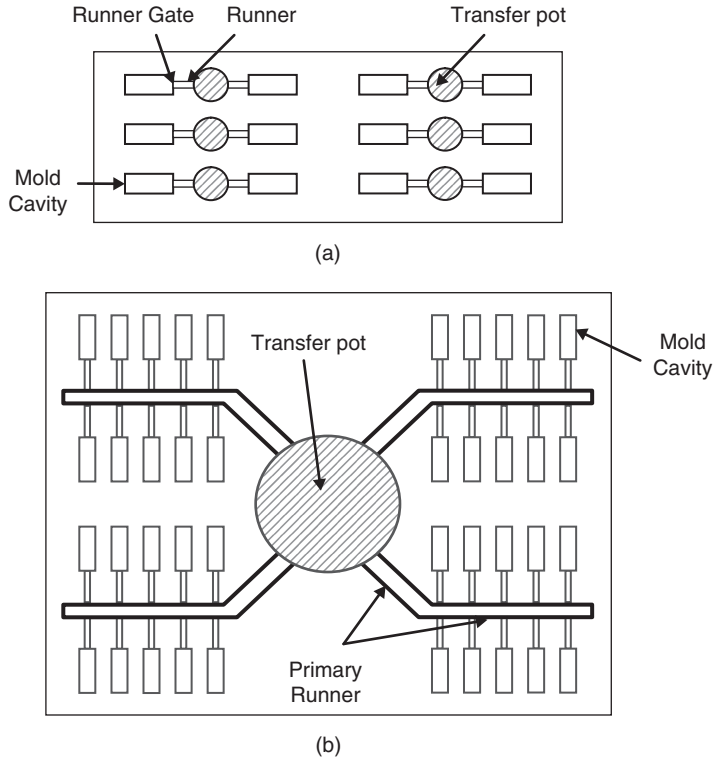


Figure 3.3 Top view of transfer molding designs with (a) multiple transfer pots and (b) single transfer pot with multiple cavities [1].

Petitioner Samsung Ex-1055, 0147

Table 3.1 Comparison of Molding Tools

Feature	Aperture-Plate Molds	Multi-plunger Molds
Number of cavities	Several thousand possible	From 2 to 100
Flexibility of package types	Extremely flexible	Relatively inflexible
Process setup and control	Moderate	Straightforward for automated tools
Flow-induced stress problems	Minimum	Intermediate
Flash and bleed	Minimum	Average
Molding compound waste (%)	20–40	10–25
Package yield per cycle	High	Very high
Ejection	External ejection	Ejector pins in each cavity
Flow time and cavity material uniformity	Good	Excellent
Packing pressure (MPa)	1.4–2.8	Variable on number of cavities fed from a pot (1.4–4.1)
Temperature profile and stability	Requires care	Excellent
Automation susceptibility	Intermediate	Very high
Capital cost	Low	High (lower for small tools)
Labor cost	High	Low
Maintenance cost	Medium	High, due to automation

Aperture-plate molds are a patented transfer molding technology (US Patent No. 4,332,537, June 1, 1982) exclusively developed for PEMs. An aperture-plate mold design is shown in Fig. 3.4. An aperture-plate (or cavity plate) mold is constructed by assembling a series of stacked plates. The lead-frames form the aperture plates. The top and bottom of the body are formed by separate plates. The bottom body-forming plate contains the runner system, while the top plate is finished for either laser or ink marking. The gates are positioned between the runners, parallel to the bottom of the body; the aperture plate cavities can be formed anywhere along this intersection, and their width can be any fraction of this length of intersection. This flexibility of gate positioning, along with the much lower pressure drop across the gate in an aperture plate, results in negligible wire sweep

Petitioner Samsung Ex-1055, 0148

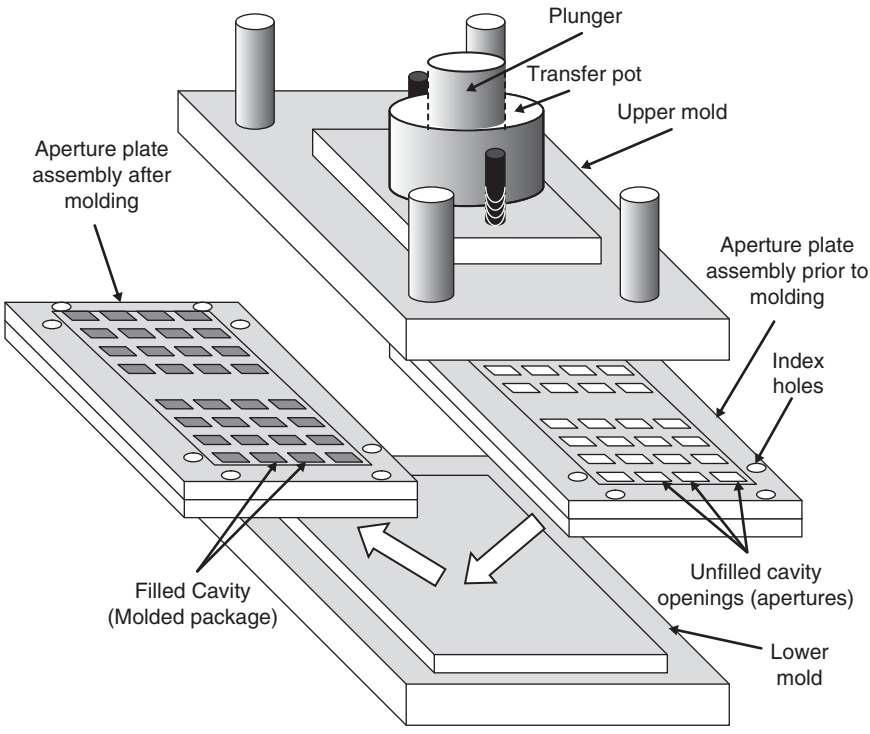


Figure 3.4 Aperture-plate (or cavity plate) molding setup [3].

and paddle shift during molding. These molds are also highly adaptable for different package types and pinouts.

Multi-plunger molds, also called gang-pot molds, have a number of transfer plungers, typically feeding one to four cavities from each transfer pot. They are highly automated and can be easily set and optimized for a new molding compound. However, their productivity is much less than aperture-plate molds due to the number of cavities available (up to hundred in multi-plunger vs. thousand in aperture-plate). Also, the use of low preform-preheat temperatures in manual tools can lead to some molding-compound temperature-related problems. Figure 3.5 shows a multi-plunger mold used for simultaneous encapsulation of dual in-line packages and quad flatpacks (QFPs). Figure 3.6 shows a multi-plunger mold with each pot feeding just one cavity.

The multi-plunger mold consists of two halves, referred to as the top and bottom molds. The mating surface of these two halves is called the parting line. Platens are massive blocks of steel used to bolt the two mold

Petitioner Samsung Ex-1055, 0149

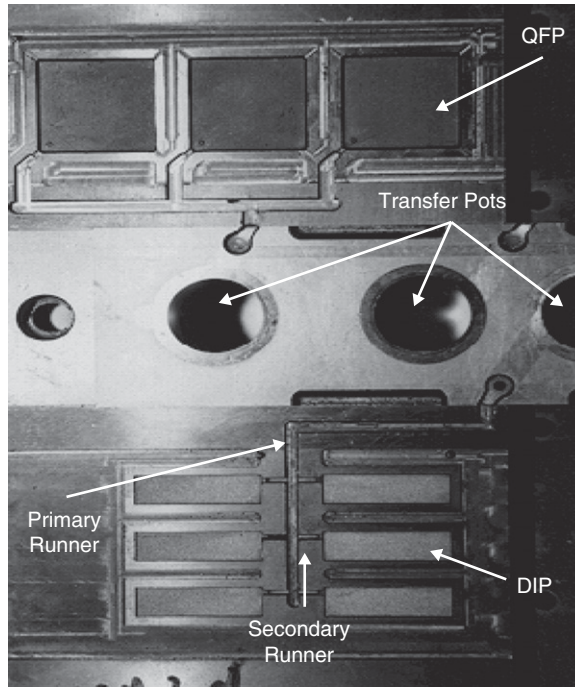


Figure 3.5 Multi-plunger mold used for simultaneous encapsulation of dual in-line packages (DIPs) and quad flatpacks (QFPs). (Courtesy of National Semiconductor 1994.)

halves to the molding press. Figure 3.7 shows different parts of a transfer mold press including platens and cavities. Figure 3.8 shows a close-up top view of a transfer pot, runners, and cavities. The mold press also includes guide pins and ejector pins. The guide pins ensure proper alignment and movement of the two halves. The ejector pins aid the ejection of the component after the mold has opened.

The gates in the molding equipment are located such that they can be easily removed and polished if necessary. Properly designed gates should allow proper flow of material as it enters the mold cavity. Gates should be located at points away from the functioning parts of the molded component.

Vents are provided in all transfer molds to facilitate the escape of trapped air. The locations of these vents depend on the part design, and locations of pins and inserts. The vent is sufficiently small so that it allows the air but not the molding compound to pass through. Vents are often placed at the far corners of the cavity, near inserts where a knit line will be formed, or at the point where the cavity fills last.

Petitioner Samsung Ex-1055, 0150

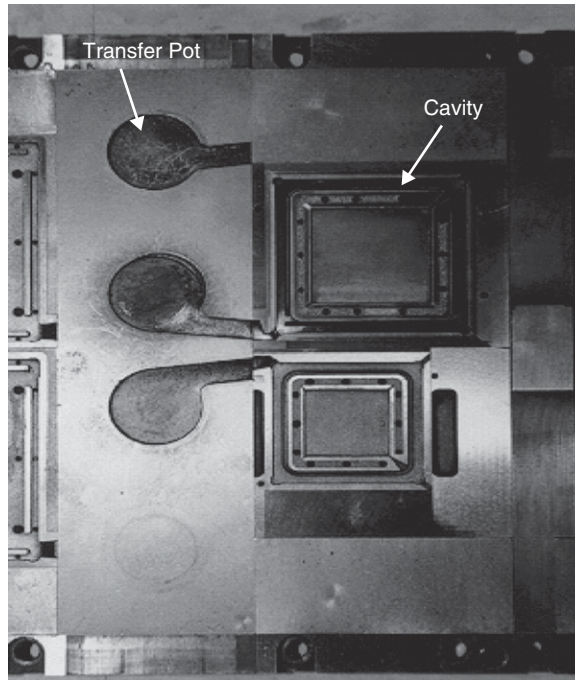


Figure 3.6 Multi-plunger mold with each pot feeding just one cavity. (Courtesy of National Semiconductor 1994.)

The specific mold design depicted in Fig. 3.8 is used for the encapsulation of QFPs. In this design, one transfer pot feeds more than ten cavities. The top part of the figure shows the lead-frame with the encapsulated packages. The bottom part of the figure shows the cavities. As seen the material flows through the runners and gates.

3.1.1.2 Transfer Molding Process

A typical transfer molding process flow is shown in Fig. 3.9. In this process, lead-frames are loaded (six to twelve in a row) in the bottom half of the mold. For both plate and cavity-chase molds this is performed at a workstation separate from the molding press. A cavity-chase mold uses a loading fixture; most molding operations have automated lead-frame loaders. The moving platen and the transfer plunger initially close rapidly, but the speed reduces as they close. The transfer plunger rate profile is depicted in Fig. 3.10.

After the mold is closed and clamping pressure is applied, the preform of molding material (which has usually been preheated to around 95°C, which is below the transfer temperature) is placed in the pot, and the transfer

Petitioner Samsung Ex-1055, 0151

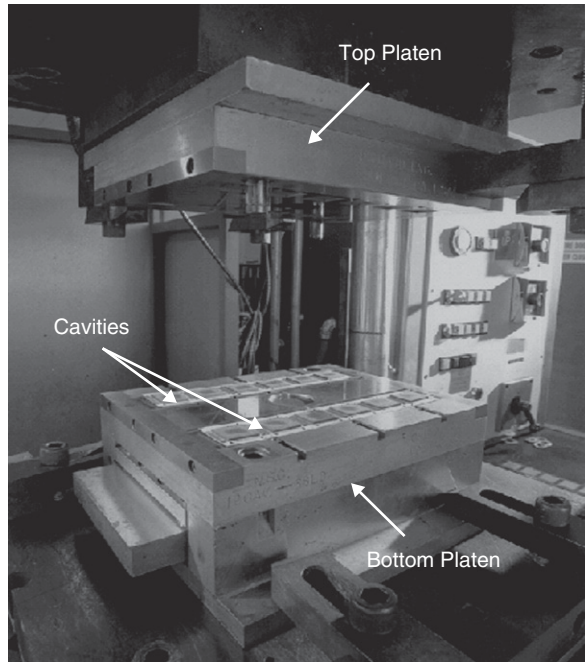


Figure 3.7 Different parts of a transfer mold. (Courtesy of National Semiconductor 1994.)

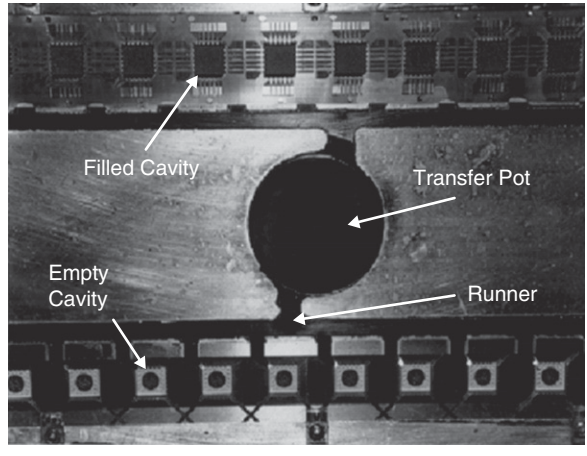


Figure 3.8 A mold used for encapsulation of quad flatpacks. (Courtesy of National Semiconductor 1994.)

plunger or ram is activated. Preheating of the molding compound typically involves a high-frequency electronic method that works on a principle similar to microwave heating. The transfer plunger then applies the transfer pressure, forcing the molding compound through the runners and gates

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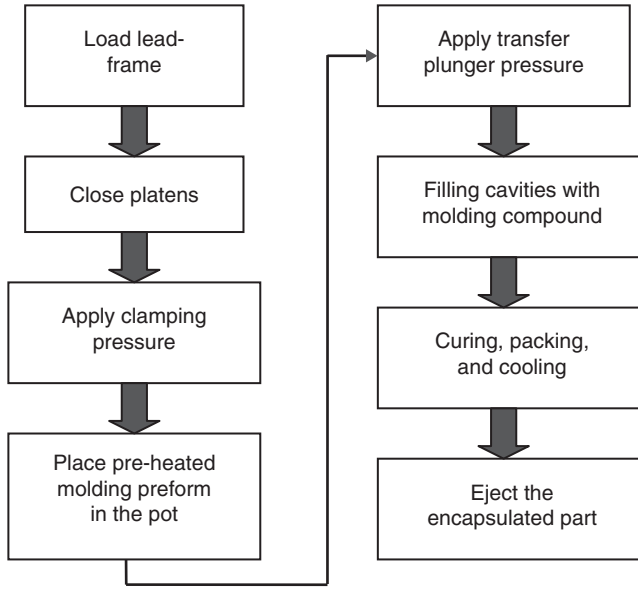


Figure 3.9 Transfer molding process flow.

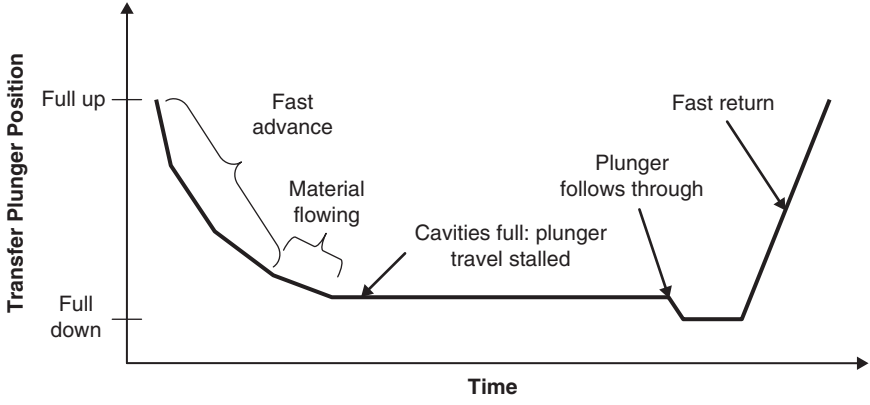


Figure 3.10 Various stages of a typical transfer molding process [4].

and into the cavities. This pressure is maintained until the cavities are filled. The mold then slowly opens; a step known as the slow breakaway. Sometimes it is desirable to have the transfer plunger move forward so that it pushes out the cull, or the material remaining in the pot. Finally, the encapsulated microelectronic package is ejected using the ejector system in the mold. In an aperture-plate mold, the plates themselves are loaded with the lead-frame strips, as they shuttle in and out of the molding press.

Petitioner Samsung Ex-1055, 0153

Several parameters in the transfer molding process must be controlled to ensure optimal results. These parameters include the temperatures of the pot and the mold, the transfer pressure, the mold-clamping pressure, and the transfer time to fill the mold cavities completely.

The mold temperature should be high enough to ensure rapid curing of the part, but not too high to pre-cure and solidify the molding compound before it reaches the cavities. The most common method of heating the molds is electric heating. Multiple electric heating cartridges are placed in both the top and bottom halves of the molds (as shown previously in Fig. 3.1) to ensure heating of all the cavities.

The mold-clamping pressure is the pressure applied on the mold sections. It must be sufficiently high to ensure complete closure of the mold halves during molding compound flow and curing. A properly controlled mold-clamping pressure can prevent or minimize flash.

The transfer plunger pressure, also known as transfer pressure, is the pressure applied by the transfer plunger that forces the molding material to fill all parts of the cavities. As the mold is filled, the molding material will shrink due to the curing process. At this point, the transfer plunger pressure forces additional molding material into the cavities to compensate for the shrinkage. This process is referred to as packing, and the applied pressure is known as packing pressure.

There are essentially two phases to cavity filling. Phase I consists of the molding compound melt flowing into and filling the cavity as depicted in Fig. 3.11. Phase II involves curing, packing, cooling, and solidification. When the molding compound material fills the mold, it begins to react. The viscosity of the material increases, at first gradually, and as the reacting molecules become larger, the viscosity increases more rapidly and the material transform into a gel. Eventually, the molding compound is solidified and it becomes a highly cross-linked network.

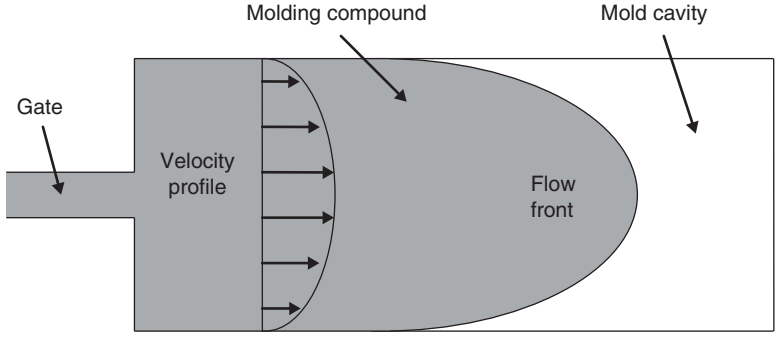


Figure 3.11 Molding compound melt flowing into the cavity.

Petitioner Samsung Ex-1055, 0154

The transfer plunger pressure must force the molding compound material through the runners and gates into the cavities and hold the material until polymerization. For high throughput, it is desirable to transfer and react the material as rapidly as possible, but decreasing the transfer time requires an increase in the transfer pressure to fill the mold. Too high transfer plunger pressures (greater than 170 MPa) can cause damage within the package, such as wire sweep short or, in extreme cases, wire bond lift-off, fracture, or shear. These problems can be avoided by careful design of the mold cavity and transfer gate parameters (i.e., angle, width, and depth) to minimize shear rate and flow stresses during cavity filling. In general, factors that tend to exacerbate these problems include high wire-loop heights, long wire bonds, bond orientation perpendicular to the advancing polymer flow front, rapid transfer times with corresponding high transfer pressures, high-viscosity molding components, and low elastic modulus wire.

An important approach to reducing the flow-induced stresses in the molding compound and improving molding yield is to decrease the velocity of the flow. During a transfer molding process with constant transfer rate and pressure control, high flow-induced stresses are produced in the cavities nearest to and farthest from the transfer pot. The middle cavities generally experience the lowest velocities and stresses. Mold mapping of flow-induced defects shows lowest yield in extreme-positioned cavities [5]. A transfer rate profile that is slow at the start, higher over the middle cavities, and slow again when the last cavities are filling can reduce the flow-induced stresses (Fig. 3.12).

Different mold designs and molding compounds require distinctive transfer pressure and rate profiles. Velocity-reducing tool changes are permanent for a particular molding compound and package design. Mold designs aim at balanced mold filling by maintaining nearly uniform pressure fronts through all segments of the mold; in these, channel cross-sectional areas are controlled for volume-flow and pressure drop uniformities in all cavities. However, in all cases, a velocity surge occurs when the molding machine switches from the transfer pressure to the packing pressure. These transient high velocities, along with the rapid compression of any remaining voids, can cause wire sweep. Using a programmable pressure controller to profile this pressure transition is the best approach to minimizing this problem.

The polymer undergoes the curing process in the mold at the typical molding temperature of 175°C for about 1–3 minutes. Following curing, the mold is opened, and the ejector pins eject the encapsulated parts. The encapsulant material must be resilient and hard enough to withstand the ejection forces without significant permanent deformation.

Petitioner Samsung Ex-1055, 0155

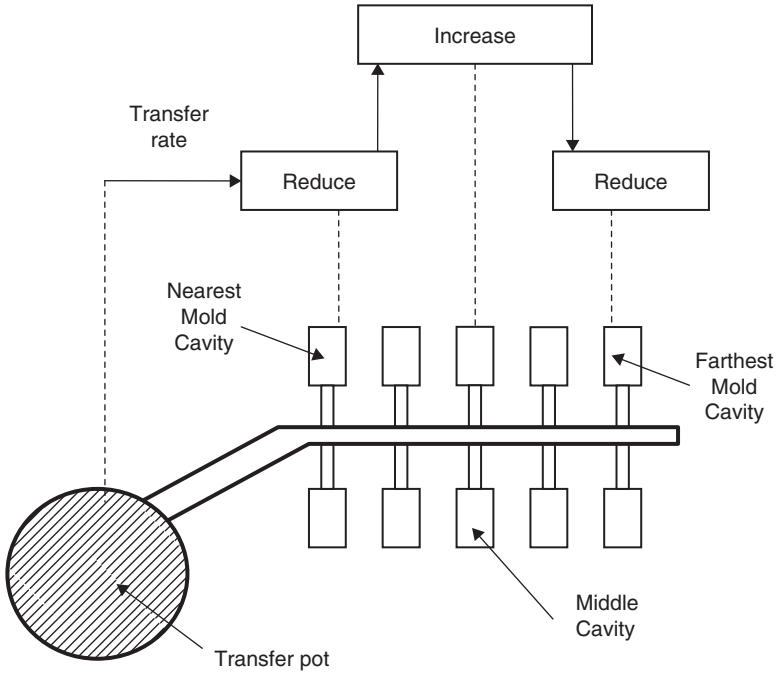


Figure 3.12 Transfer rate control based on the distance of mold cavities from the transfer pot.

After ejection, the molded lead-frame strips are loaded into magazines, which are post-cured in a batch (4–16 hours at or below 175°C) to complete the cure of the encapsulant. In some instances, post-curing is performed after code marking to eliminate an additional heat-cure cycle. However, with laser marking, this is not the case. The most important consideration in post-mold cure analysis is the development of thermomechanical properties. For example, the glass transition temperature (T_g) of the encapsulant material is significantly influenced by the extent of reaction (cross-linking density), as depicted in Fig. 3.13, indicating the value of proper post-cure treatment in realizing full material properties.

3.1.1.3 Molding Simulation

The transfer molding process is more complicated and difficult to treat analytically than either thermoplastic extrusion or injection molding, because of the time-dependent behavior of the molding compound, the irregular cross-sections of the runners, and the presence of inserts in the cavities. However, once a good quantitative model of the transfer molding

Petitioner Samsung Ex-1055, 0156

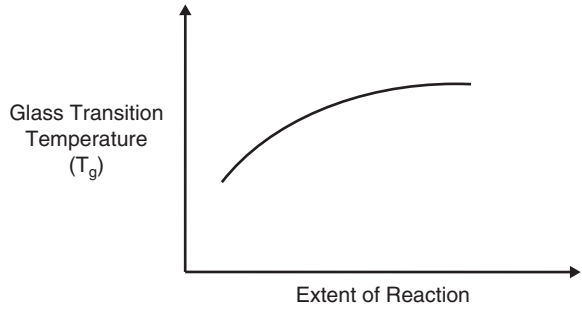


Figure 3.13 The glass transition temperature of the encapsulant versus the extent of reaction.

process has been proven, substantial time and cost can be saved. Long and expensive experimental runs no longer need to be carried out by trial and error to debug a mold or qualify a new compound.

Modeling the dynamics of transfer molding has met with moderate success [6,7]. The approach typically involves formulating a chemo-rheological description of the epoxy molding compound and coupling it with a network flow model. The gating factor for a successful simulation is a good characterization of the compound to determine its kinetic and rheological behavior. Most often, the curing reaction of the epoxy can be described by an autocatalytic expression. The dynamic viscosity, as measured generally through a plate and cone viscometer, is reasonably well covered by the Castro–Macosko model [7]. By incorporating this material information into a flow model that includes the geometrical intricacies of a multi-cavity mold, an understanding of the filling characteristics of a particular compound can be obtained.

With a rheological model, a variety of scenarios can be simulated to optimize processing conditions and mold design [7–9]. For instance, different temperatures, pressures, and packing settings can be estimated to provide optimized filling profiles. To reduce wire sweep, the dominant-yield loss concern for fine-pitch packages, an analytical model of wire deformation can be coupled with rheological and kinetic information to improve process conditions and package layout design rules [8]. Void formation and warpage have also been predicted in transfer molding flow simulations using Hele-Shaw models and the 3D finite-volume method and verified experimentally to identify the critical process parameters and prevent defects [10,11]. Once a mold has been translated into its geometrical equivalent, various combinations of runner sizes, gate locations, gate dimensions, and cavity layout can be evaluated.

Petitioner Samsung Ex-1055, 0157

3.1.2 Injection Molding

Injection molding was initially developed for thermoplastic materials, but with slight modifications in the process it can also be used for thermosetting encapsulants. It is a technique used for making large volumes of molds with relatively low labor costs and process automation. A disadvantage of injection molding is that the equipment can be expensive due to design complexity and the need to withstand high pressures. An injection molding apparatus is shown in Fig. 3.14.

The mold cavity is made up of two halves that are clamped together. Plastic pellets are fed into a screw from a feed hopper and are subjected to several heating zones so that when the melt comes out of the screw it is completely melted, de-aired, and dried. The plastic melt that comes out of the nozzle located at the other end of the screw is in a viscous state compressed to 3,000 kg/cm^2. High pressure is then applied to the melt to fill the mold at the required speed. Extra melt may be required to compensate for shrinkage. After the component has cooled (with chilled water) and its shape is set, the mold is opened and the component is ejected.

Moldings made by injection molding usually do not require finishing, if good practice is followed in the manufacturing phase. Small components can be manufactured in large quantities at reasonable costs. Injection molding was applied to semiconductor packaging in the 1980s with thermoplastic materials such as polyphenylene sulfide (PPS). The process was a novelty at the time, as it provided a faster alternative to transfer molding, but poor reliability quickly tempered the enthusiasm. The high viscosity

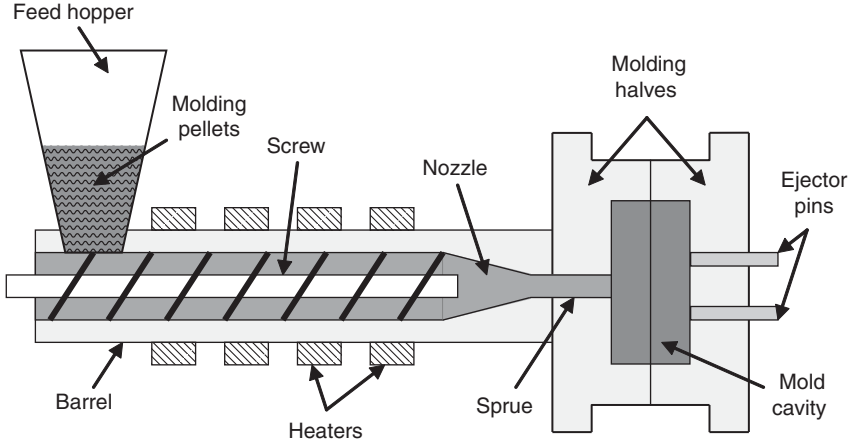


Figure 3.14 Injection molding apparatus.

Petitioner Samsung Ex-1055, 0158

of the PPS melt generated a lot of wire sweep due to the high injection pressure, which is typically an order of magnitude larger than the packing pressure of transfer molding. Furthermore, an almost total lack of adhesion between the thermoplastic and the copper lead-frames was discouraging. Injection molding dropped out of the limelight once the cost of expensive capital investment was considered.

Despite these discouraging results with PPS, internal efforts were continued at some European companies to evaluate injection molding as an option. Alternative encapsulant materials including thermosets were explored for injection molding of microelectronics. Reliability evaluation of injection-molded packages with alternative materials revealed similar reliability compared to that of others. Although wire sweep in injection-molded parts is generally greater than in transfer-molded parts, proper process optimization can minimize such defects. The differences in the methods occur mainly in process conditions and the required preventive maintenance; cleaning, parts wear, and residue removal are much more troublesome with injection molding equipment.

3.1.3 Reaction-Injection Molding

Reaction-injection molding is different from other molding processes in that the starting materials are liquids at room temperature. Polyurethanes are usually associated with the process, but if polyesters and epoxies are used as resins then the process is known as resin transfer molding. The ingredients of the melt are polyol, polyisocyanate, and a promoter for the chemical reaction that takes place during the course of molding. The reactive liquid components are prepared separately and pumped into a mixing head in fine stream liquid form where they are thoroughly mixed. From here the mixed liquid resins are pumped into the heated mold for the part to cure.

One major advantage of reaction-injection molding is that low clamping pressures are required, which means that large parts can be made at low costs. Reaction-injection molding suffers from the same fate plaguing injection molding, namely the lack of an appropriate material and expensive capital outlay. The absence of good candidate materials was not for lack of trying. Efforts by resin suppliers such as Shell and Dow Chemical did not produce a two-part epoxy system of sufficiently high purity and reactivity to compete with epoxies tailored for transfer molding. Foreign competition gained the upper hand, and both companies are now no longer active in this area. Ciba Geigy was partly successful in creating such a system in the early 1990s, although the reliability of the molded parts was

Petitioner Samsung Ex-1055, 0159

still inferior to that of the control samples made by transfer molding. Once more, when the need to retrofit molding presses with reaction-injection molding equipment was considered, there was little incentive to put more development resources into the process.

3.1.4 Compression Molding

Compression molding can be suitable for very thin packages, multi-chip modules, and wafer-level packages. Figure 3.15 shows an example of the compression molding process. A specific amount of molding compound is placed on each die to be encapsulated. The compressive forces are applied

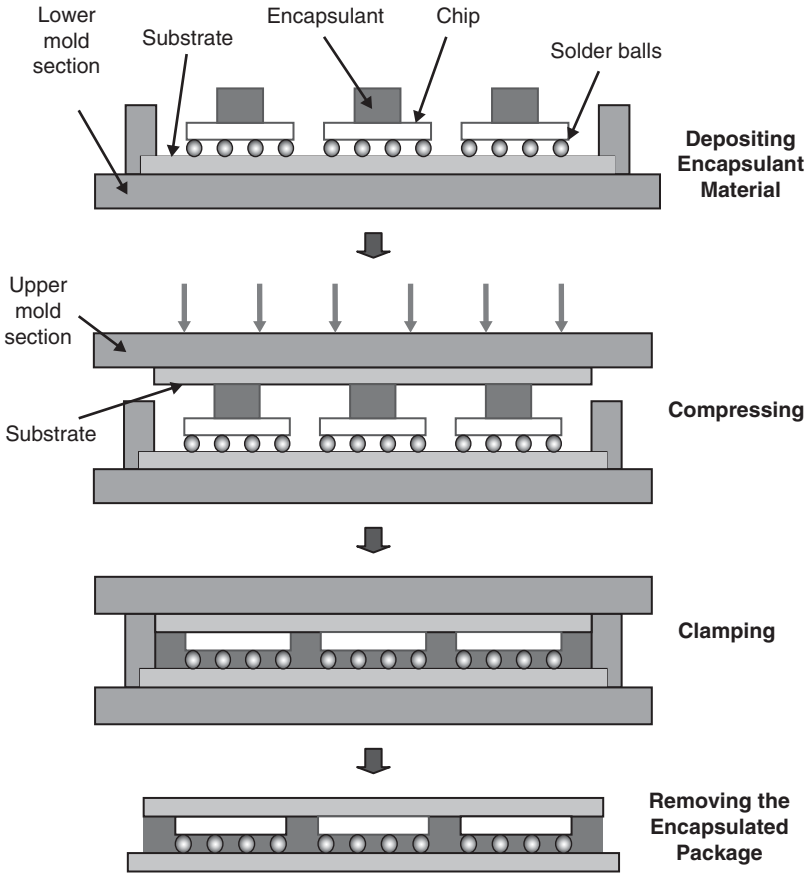


Figure 3.15 Compression molding encapsulation of a multi-chip module with flip-chips and solder ball interconnections from Hitachi [12].

Petitioner Samsung Ex-1055, 0160

to the top mold half section forcing the heated molten compound to flow around the die and into the small protrusions. The clamping pressure ensures complete flow of the encapsulant material. The clamp is then released and the encapsulated package is removed.

3.1.5 Comparison of Molding Processes

A comparison of the four types of molding technologies used for microelectronic encapsulation is shown in Table 3.2.

Table 3.2 Comparison of Molding Processes

Molding Technology	Advantages	Disadvantages
Transfer molding	• Multiple cavities, thus high yield • Lower molding equipment cost • Short cycle time • Low tool maintenance costs	• High molding pressure • Molding material may be wasted, thus higher material expense • Requires removal of flash
Injection molding	• Good surface finish • Good dimensional control • Low labor cost • High production rates	• Poor material availability • Extremely high pressure • Rapid tool wear (screw and barrel wear) • High capital investment
Reaction-injection molding	• Energy efficiency • Low mold pressure • Good wetting of chip surface • Adaptability to TAB	• Few resin systems available for electronic packaging • Requires good mixing • High capital investment
Compression molding	• Suitable for very thin packages, multi-chip modules, and wafer-level packages • Lower molding equipment cost • Short cycle time	• May require removal of flash • Extra cost due to wasted material • High molding pressure

TAB: Tape-automated bonding.

Petitioner Samsung Ex-1055, 0161

3.2 Glob-Topping Technology

Glob-top technology is used to directly encapsulate devices on the printed circuit board (PCB) such as flip-chip and chip-on-board. In glob-topping, the surface to be coated is positioned under a dispensing nozzle connected to a liquid encapsulant reservoir. The bonded chip surface is generally heated to facilitate spreading of the encapsulating compound. Material flowing out of the nozzle impinges against the surface and fans outward (thus the term radial-spread coating, also used to describe the process). Process control parameters include reservoir pressure, resin viscosity, clearance between the nozzle and surface, dispensing pressure pulse, and physical design of the nozzle. After the deposition, the coated package is cured by heating in a resistance-, microwave-, or radiant-heated enclosure or oven. Post-curing of the coating may be performed off-line in a batch process, if necessary. The volume of the encapsulating material and the void control are two important parameters in the operation as they affect the encapsulation appearance and quality. A commercially available liquid encapsulant dispensing system is shown in Fig. 3.16.

During the glob-topping process, care must be taken to ensure that all important electronic elements are completely covered in order for the full reliability advantages of the encapsulation to be realized. Compared with transfer molding, glob-topping has two advantages: the lack of molding pressure and flow-related problems such as wire sweep. However, manufacturing disadvantages include a long cycle time, dispensing time, voids, and a narrow selection of low-viscosity encapsulating compounds. The glob-top encapsulated packages are also more susceptible to moisture and high shrinkage stress compared to molded lead-frame packages such as QFPs and small-outline packages. That is because of the one-sided encapsulation and the possibility of de-adhesion at the interface of the encapsulant and substrate, which can significantly increase the rate of moisture diffusion into the package.

There are two widely used dispensing techniques: “glob-top” and “dam-and-fill.” Encapsulating using a glob-top dispensing process requires the material to be dispensed through a needle valve to cover the chip and wire bonds. The volume of the encapsulating material and void control are two important parameters in the operation, as they affect the encapsulation’s appearance and quality. Too little volume dispensed will leave the wire bonds unprotected, whereas too much can leave a high-profile dome of encapsulant that may make the total package too large. A glob-top encapsulated chip-on-board is shown in Fig. 3.17.

Petitioner Samsung Ex-1055, 0162

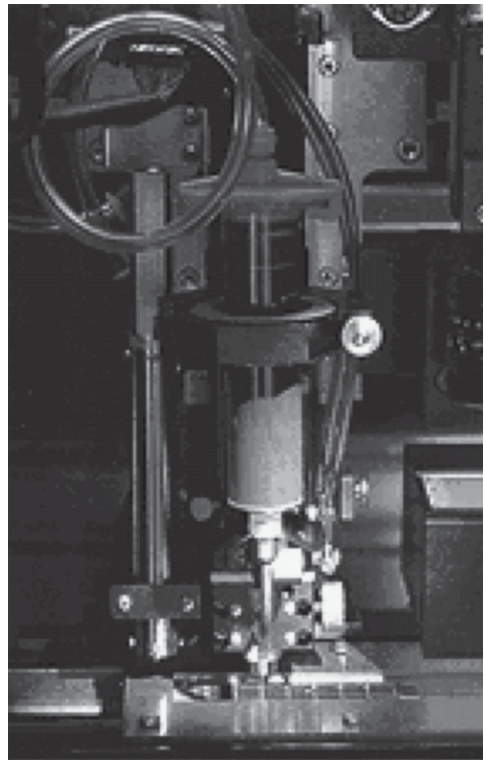


Figure 3.16 An example of a liquid encapsulant dispensing system, the Camelot 3900.

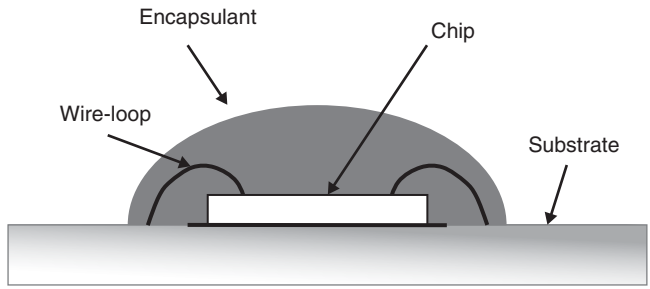


Figure 3.17 Glob-top encapsulation of chip-on-board.

Another method for glob-top encapsulation is the two-step process, known as dam-and-fill. Figure 3.18 illustrates the schematic for the dam-and-fill encapsulation of chip-on-board. First, the dispensing needle creates a dam around the die to be encapsulated with a high viscosity material.

Petitioner Samsung Ex-1055, 0163

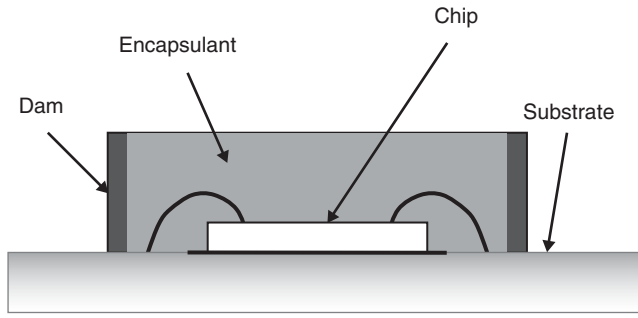


Figure 3.18 Dam-and-fill encapsulation of chip-on-board.

The area within the dam is then filled with less viscous material, which flows to create a thin layer around the wire bonds and over the chip. The dam limits the flow of the less viscous filler material, allowing the use of a thinner filler material, faster filling, and a more uniform encapsulation height compared to the glob-top dispensing process [13].

The encapsulant material properties and the dispensing–heating system play critical roles in the encapsulation quality of the die and wire bonds. The encapsulant material should have a relatively low viscosity and comparable coefficient of thermal expansion value to that of the die, wire bonds, and substrate. Temperature control also plays a major part in the material viscosity variation. A thermal heat source built into the dispensing system should be used to increase the material temperature (i.e., 30–50°C) during dispensing to achieve lower viscosity and to enhance flow. The temperature of the encapsulant during dispensing is highly dependent on the type of material. In some cases, the substrate or PCB is also heated (i.e., 60–110°C) prior to dispensing to ensure a smooth flow of the encapsulant [14,15]. The heat allows the encapsulant to flow completely around the wire bonds which leads to the elimination or reduction of trapped air pockets and, subsequently, voids in the package.

The selection of the dispensing equipment is important in producing a high quality and long-term repeatable process. There are three types of dispensers: syringe valve, auger pump with rotary positive displacement valve (RPDV), and true positive displacement pump (TPDP) [13]. The syringe valve consists of a needle attached to a syringe filled with the encapsulant material. Applied air pressure causes the glob-top encapsulant to flow and dispense. The flow rate is dependent on the encapsulant viscosity and applied pressure.

Petitioner Samsung Ex-1055, 0164

Auger pumps with RPDV offer a more stable flow compared to syringe valves. Figure 3.19 shows the relationship between the dispensing parameters in the auger pump. By decreasing the size of the needle and slowing the flow, the pressure drop in the auger pump at the exit location increases. Also, increasing the auger pump motor speed causes an increase in the flow rate. To increase the accuracy of the auger pump, a mass calibration system is necessary [13]. With a mass calibration system, the flow rate is monitored by the dispenser and the dispensing speed is adjusted automatically to maintain a consistent dispensing volume over time.

TPDP offers the highest accuracy and stability among all the dispensing pump technologies. TPDP uses a metal piston to displace a volume in a closed chamber leading to a controlled encapsulant flow. A slow movement of the piston ensures a continuous flow.

Liquid dispensing techniques developed to ensure void-free encapsulation include dispense-in-vacuum and pressure cure. In vacuum processing, the product is placed under a vacuum during, or immediately after, the dispensing of the resin. Vacuum processing can speed up resin flow and virtually eliminates voiding within the encapsulant. In pressure curing, the product is placed in a pressure cooker at high temperature and pressure, immediately following resin dispensing. The pressure helps to collapse any voids and the temperature helps to speed up resin curing. Tessera has used both of these processes together, with dispensation occurring under vacuum and curing occurring under pressure [16].

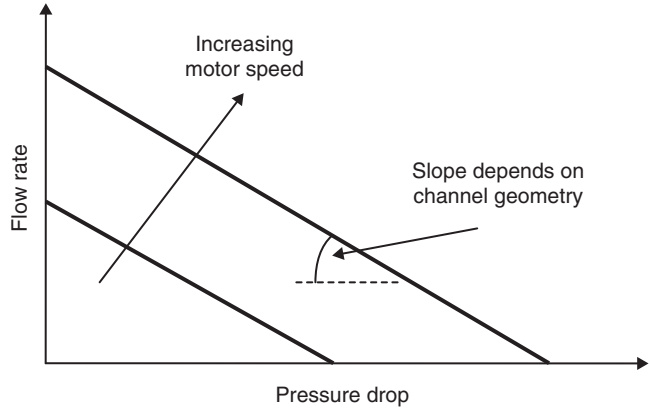


Figure 3.19 Relationship between the dispensing parameters in an auger pump with rotary positive displacement valve [13].

Petitioner Samsung Ex-1055, 0165

3.3 Potting and Casting Technology

Potting and casting is used for the encapsulation of connectors, power supplies, sensors, high-voltage resistor packs, relays, and other larger electronic units. Two common steps involved in potting and casting are dispensing and curing. The potting/casting liquid encapsulant is poured or dispensed into a "pot," case, or mold containing the electronic device as shown in Fig. 3.20. The liquid encapsulant is then cured and is transformed into a hardened state. Other steps may be required either prior to dispensing or after curing, depending on the specific type of encapsulant, cure chemistry, and potting or casting processes. Two-part encapsulants must be mixed prior to dispensing.

The terms potting and casting are sometimes used interchangeably to refer to the process of dispensing potting material into a pot. However, in the potting process, the case or container remains a part of the encapsulated unit, whereas in the casting process, the case or mold is removed.

Potting cases or trays are generally made of plastic materials, but metals can also be used if better heat dissipation is needed. Plastic potting cases can be made of polymeric materials such as acrylonitrile-butadiene-styrene,

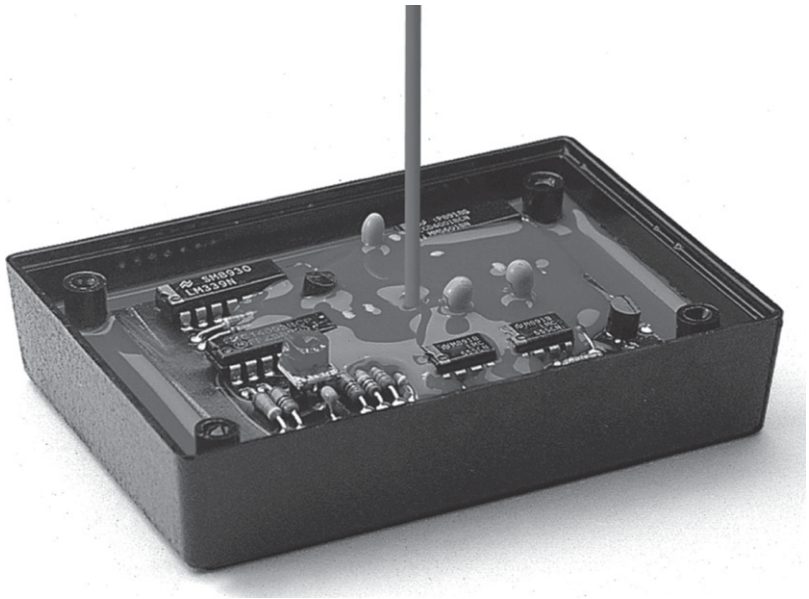


Figure 3.20 Potting using Insulcast® epoxy compound. (Courtesy of ITW Polymer Technologies, http://www.insulcast.com/solutions.html).

Petitioner Samsung Ex-1055, 0166

nylon, and polyvinyl chloride with or without fiber glass for better bond development (www.pottingsolutions.com). Glass filled polyester, polyphenylene oxide, and polycarbonate are suitable for high temperature application. Polyethylene and polypropylene are not recommended for potting because they do not generally bond well with the potting material. Potting cases can vary in shapes from simple rectangular boxes to complex shapes.

Casting molds are usually designed for a specific device encapsulation. Mold release agents are added for separating the mold from the encapsulated device. The potting compound is dispensed through the channel in the mold. After curing, the mold is separated and the channel is cut off.

When handling potting materials (i.e., mixing, pouring, etc.), protective gloves are recommended to avoid potential health problems due to contact with the chemicals. Nitrile and latex gloves are suitable choices for potting and casting purposes. Glasses are recommended for eye protection.

The geometry of the potting application can play a role in selecting a suitable potting material curing chemistry (i.e., one-part or two-part, addition or condensation cure). Figure 3.21 shows general guidelines from General Electric Company for the selection of the curing chemistry of the room-temperature-vulcanizing potting material based on various geometries (General Electric Encapsulant Products Brochure). The geometries that are small, less complex, and exposed to the atmosphere allow curing by moisture or heat and, therefore, all four types of curing systems can be used. The geometries that are more complex or do not have exposure to atmospheric moisture are limited to mostly addition cure encapsulants (heat cured).

3.3.1 One-Part Encapsulants

One-part encapsulants consist of an already mixed resin and hardener. The hardener is inactive until it is exposed to heat, moisture, or UV light. One-part encapsulants have generally shorter shelf life (storage life) than two-part systems and the range of properties available are generally limited.

The one-part potting material is poured into the pot or case containing the electronic part until it covers the entire unit. Prior to dispensing, if the potting material contains fillers, it is recommended to be mixed to ensure uniform distribution. The dispensed liquid resin/hardener mixture is then cured generally with ambient moisture (condensation cure), heating, or UV light (addition cure).

Petitioner Samsung Ex-1055, 0167

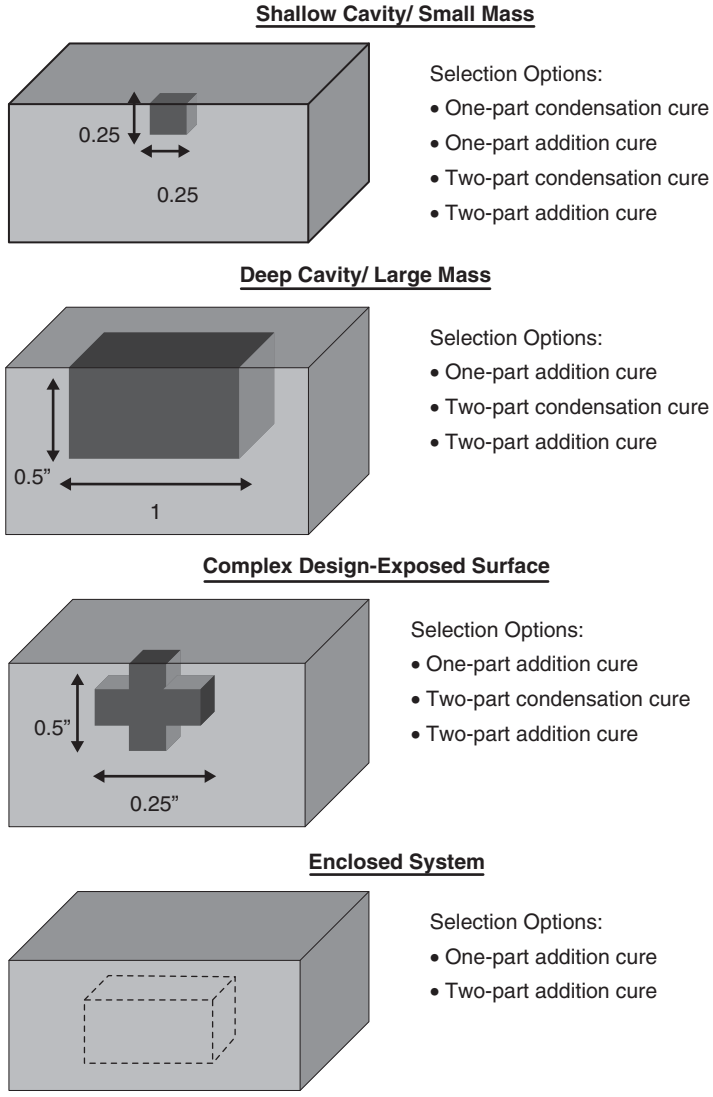


Figure 3.21 Guidelines suggested by General Electric on RTV cure chemistry selection options based on the application geometry (General Electric Encapsulant Products Brochure).

RTV: Room temperature vulcanization.

3.3.2 Two-Part Encapsulants

Two-part potting encapsulants consist of a resin and a hardener that are separate and must first be mixed. Mixing proportions are either by weight or volume. Prior to combining parts A and B, it is recommended to mix

Petitioner Samsung Ex-1055, 0168

each part to ensure uniformity. Parts A and B are then combined and mixed thoroughly. The mixture is then poured into the pot containing the electronic unit, until the whole unit is completely covered.

There are several advantages to two-part encapsulants. They can be cured at room temperature. They offer a wider range of properties compared to one-part encapsulants. Furthermore, two-part encapsulants have a longer storage life. The disadvantages of two-part encapsulants include the need for precise ratio measurements and thorough mixing.

Inadequate mixing can be detrimental to the curing quality of the encapsulant product. Attention should be given to any visual signs of insufficient mixing such as light colored streaks or marbling in the mixture (Dow Corning Potting Materials Brochure). Automatic mixing and dispensing equipments are recommended for adequate mixing and dispensing, especially for those fast-curing encapsulants.

During the mixing and pouring of the liquid mixture, careful attention must be given to prevent or minimize air entrapment. It is preferred (if practical) to dispense under vacuum, particularly for those electronic components that have small voids or cavities. For some applications that are sensitive to air entrapment, de-airing with 28–30 inches of mercury vacuum may be required (Dow Corning Potting Materials Brochure).

3.4 Underfilling Technology

Underfill encapsulation plays a significant role in the protection and reliability of flip-chip packages. Underfill can reduce the effect of the global thermal expansion mismatch between the silicon chip and the substrate. It can reduce the stresses and strains in the solder bumps and redistribute them over the entire chip area; otherwise they would be increasingly concentrated near the corner solder bumps of the chip. The protection of the chip from moisture, ionic contaminants, radiation, and hostile operating environments "with thermal, mechanical, shock, and vibration stresses" is the other advantage of underfill encapsulants. In one study, it was found that the underfill encapsulation improved the reliability of a flip-chip package by tenfold [17]. The disadvantages of underfill encapsulants include the difficulty of rework and the reduction of manufacturing throughput. A class of no-flow underfill encapsulant materials has emerged to reduce the manufacturing processing steps and increase production throughput. Figure 3.22 compares the processing steps of capillary underfill and no-flow underfill.

Petitioner Samsung Ex-1055, 0169

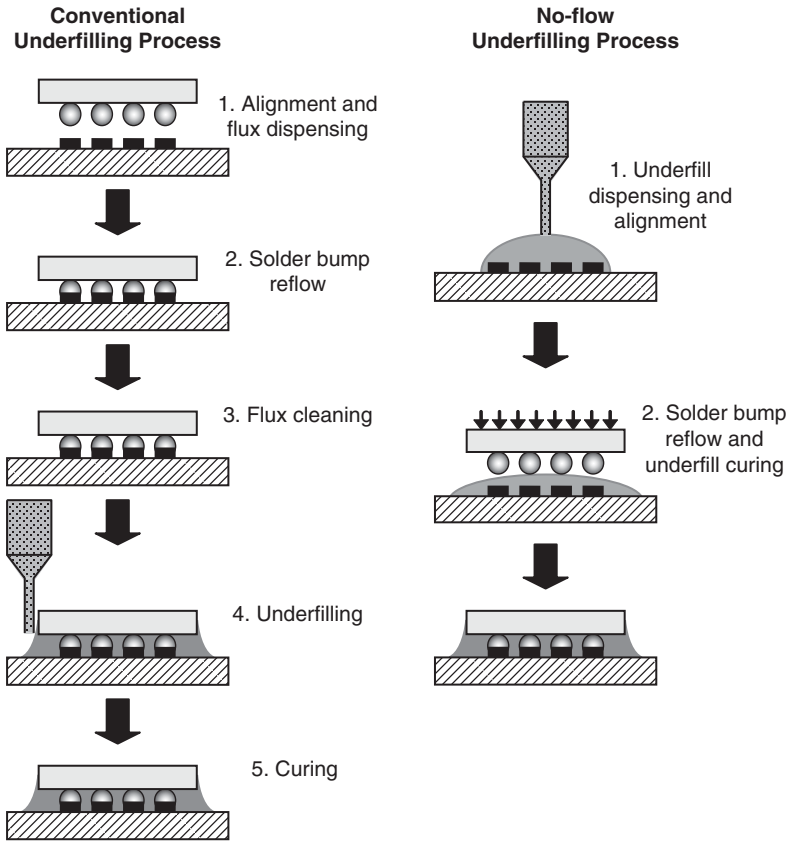


Figure 3.22 Conventional versus no-flow underfilling process flow.

3.4.1 Conventional Flow Underfill

Due to a thermal mismatch between the substrate and the die material, an underfill material acts as a cushion layer during thermal cycling and effectively protects the solder joints from being damaged. The underfilling process involves dispensing a controlled amount of material into a gap between a chip and substrate as shown in Fig. 3.23. The underfill material is dispensed along a line adjacent to the edge of the die where capillary action wicks the material beneath the die, filling the spaces between the die, substrate, and interconnect bumps. It is critical that the gap between the die and the substrate is completely filled with underfill material, as the life of the chip assembly is dependent on it. To ensure that the material flows correctly, the substrate needs to be uniformly heated. If the

Petitioner Samsung Ex-1055, 0170

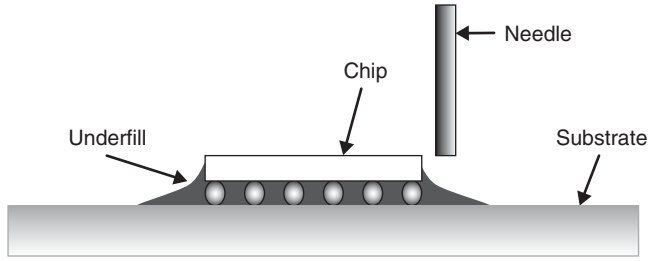


Figure 3.23 Schematic diagram of flip-chip underfill encapsulation [18].

temperature is too high, the dispensed underfill may not flow efficiently and may result in long flow time or incomplete filling.

The fillet dispense pattern must be optimized for complete underfill and to eliminate air pockets within the fluid as it flows beneath the die. The underfill material may be dispensed along one edge of the die, along two adjacent edges in an "L" pattern, or along two adjacent edges and part of a third. The shape of the die and maximum distance for flow helps determine the best pattern that will completely underfill the chip.

Every underfill process has a volume of fluid that must be dispensed to assure proper underfill. This volume can be found by calculating the volume of the space between the die and the substrate, adding the volume required for the fillet, then subtracting the volume of the interconnect bumps. If too little volume is dispensed, the underfill will be incomplete and ineffective. Too much dispensed fluid leads to material waste and increases the manufacturing cost [19].

The final step in the underfill process is the curing of the material. The assembly is soaked at a specified temperature range for a specified length of time for the material to cure. The time and temperature of the curing process is dependent on the underfill material used. This step is usually the most time-consuming. New materials are being developed to reduce the curing time.

Two key factors related to void-free underfilling are (1) the gap between the flip-chip active surface and the PCB solder mask top surface and (2) the assembled board holding time prior to the underfill process [20]. A relatively large gap between the flip-chip and the PCB can lead to an increase in underfill wave front speed and overcoming surface tensions of the die/underfill and solder mask/underfill interfaces. Shorter assembled PCB holding time can lead to less moisture absorption, thereby reducing the risk of underfill void.

Petitioner Samsung Ex-1055, 0171

3.4.2 No-flow Underfill

Productivity can often be improved by combining multiple operations into one. Researchers at Motorola working on organic boards came up with the idea of combining underfill and flux into a single material [21–23]. Their process involved dispensing the underfill–flux onto the board, placing the chip on top, and then running the assembly through a reflow solder oven. Universities later pursued the idea, called "no-flow" underfill [22], and found that it solved many materials-associated problems.

Conventional underfill technology has relied on capillary flow and has been in use for some time. However, this technology needs separate flux dispensing, flux cleaning, solder bump reflow, underfill dispensing, underfill flow, and off-line underfill curing steps. Thus, the conventional underfilling process is tedious and expensive. A no-flow underfill encapsulant is dispensed on the die or substrate prior to attaching the die to the board or carrier. The encapsulant is cured during reflow of interconnect bumps, and also acts as a flux during the reflow process.

One of the disadvantages of no-flow underfills is the elimination of silica fillers and the subsequent higher coefficients of thermal expansion relative to conventional flow underfills leading to potential reliability problems. Silica fillers are absent from the encapsulant because they can interfere with solder joint formation. Innovative methods have been developed to allow the addition of silica fillers to no-flow underfills without compromising solder joint formation, such as double-layer no-flow underfilling and nano-filler technology [24,25]. No-flow underfilling can also be more expensive [26].

3.5 Printing Encapsulation Technology

Printing encapsulation technology is used for smaller, thinner, and high density packages where narrow spaces require a more refined encapsulation technique. Among the packages that are encapsulated using printing technology are ball-grid arrays (BGAs), chip-scale packages (CSPs), multichip modules (MCMs), wafer-level packages (WLPs), and light-emitting diodes. Printing encapsulation is performed either by using a stencil (stencil printing) or by printing onto existing cavities such as vias and spaces between interconnection bumps (cavity printing).

In the stencil printing encapsulation process (also known as screen printing), a stencil or screen is positioned on a wafer or a substrate consisting of multiple devices to be encapsulated. A process flow for stencil printing

Petitioner Samsung Ex-1055, 0172

is shown in Fig. 3.24. The stencil windows (openings) define the areas to be encapsulated. Liquid encapsulant is then deposited on the stencil and using a squeegee the encapsulant is pushed into the openings. There may be several squeegee runs across the stencil to ensure complete and planar encapsulation. The planarization process using squeegees is shown in Fig. 3.25. After complete encapsulation with liquid resin, the encapsulant is then cured, and the stencil and substrate are separated.

The vacuum printing encapsulation system (VPES) developed by Okuno and his team at Sanyu Rec. Co. is designed to ensure complete and void-free

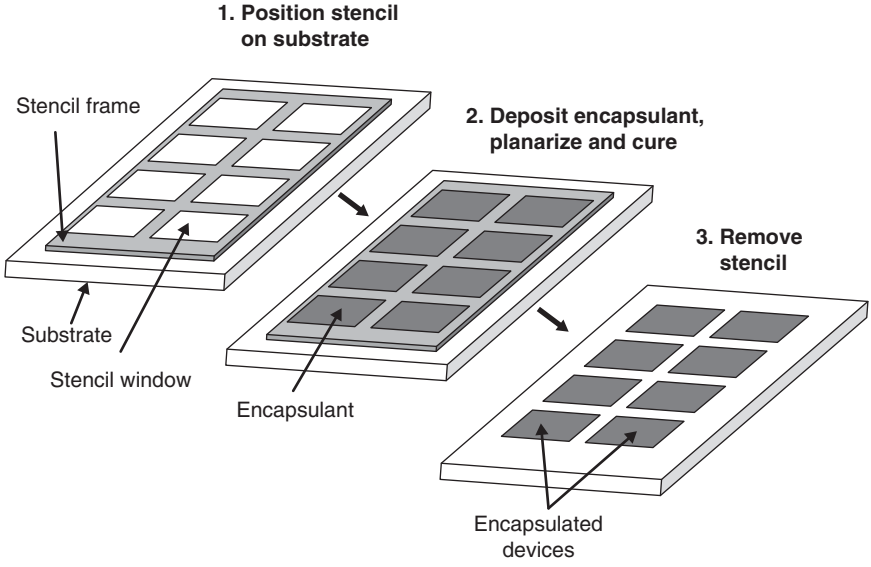


Figure 3.24 General process flow for stencil printing.

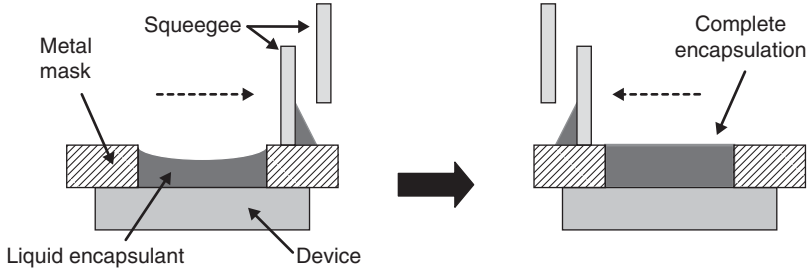


Figure 3.25 Planarization process using squeegee during printing encapsulation [27].

Petitioner Samsung Ex-1055, 0173

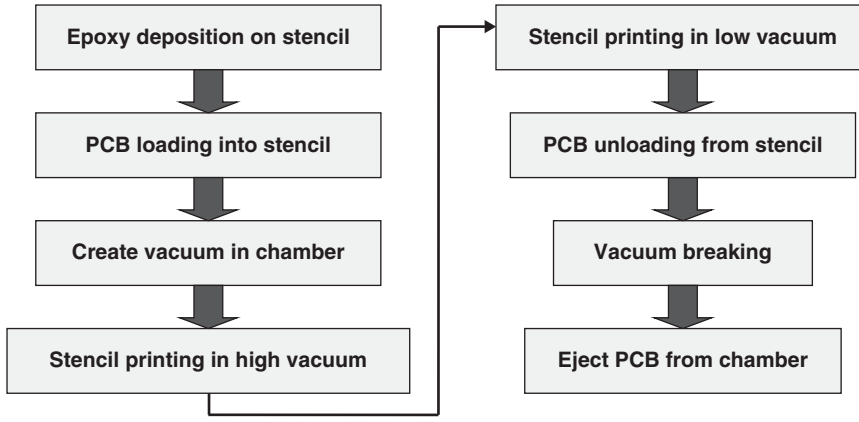


Figure 3.26 Process flow for the SANYUREC vacuum printing encapsulation system [28].

encapsulation because of high pressure vacuum (150 torr) [27]. Figure 3.26 shows the process flow for printing encapsulation using the SANYUREC VPES-HAVI machine [28].

Printing encapsulation can also be conducted on wafer-level CSP (WL-CSP) cavities or vias (cavity printing). Figure 3.27 shows an encapsulated WL-CSP using cavity printing [29]. First, a dry film photoresist layer is deposited on top of a pre-processed wafer. The wafer consists of multiple bond pads and input/output redistribution metal layers. The photoresist is patterned to create multiple trench and via openings. The trench opening is filled with liquid photoresist material, and the via opening is filled with conductive metal to form via plugs. The dry film photoresist is removed and the encapsulant is printed on the wafer. The encapsulation in this WLP, as shown in Fig. 3.27, is discontinuous due to the presence of trench openings and via plugs. This discontinuity can be advantageous by preventing warpage caused by coefficient of thermal expansion mismatches.

3.6 Encapsulation of 2D Wafer-Level Packages

The single-chip WLP is similar to a CSP in package configuration. The main difference between a single-chip WLP and a CSP is the packaging assembly process. Single-chip WLPs are made using wafer-level packaging technology in which the interconnection bumping and testing

Petitioner Samsung Ex-1055, 0174

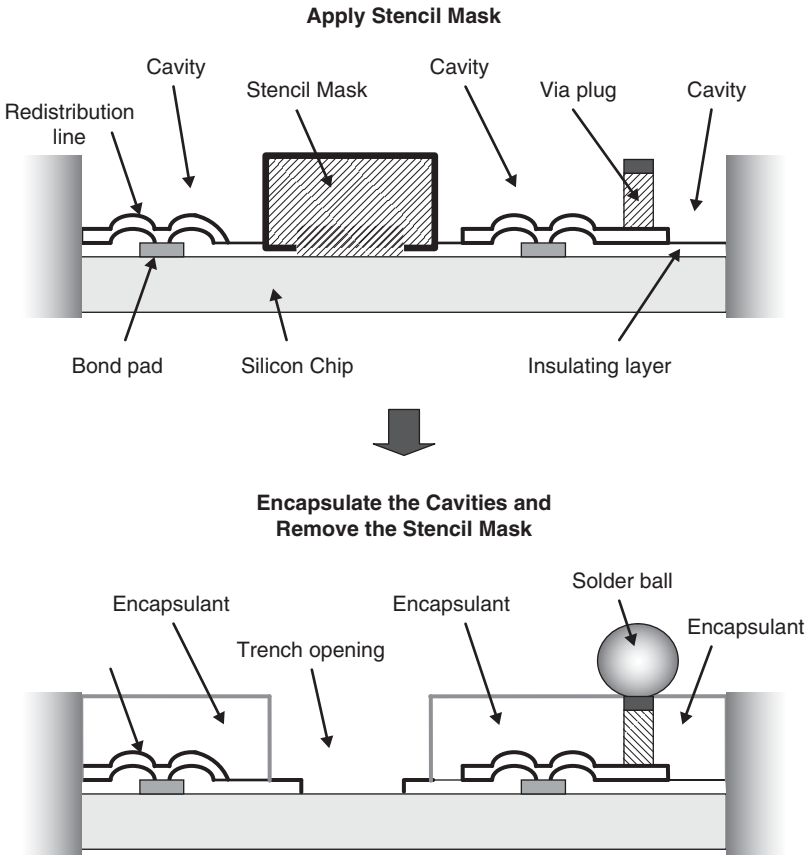


Figure 3.27 Cavity printing encapsulation of a wafer-level chip-scale package in the protrusions created by photoresist material and via plugs [29].

is performed on the wafer [30]. In conventional CSP assembly flow, the wafer is diced and the interconnection bumping and testing is performed on the chip. Due to the similarity to CSPs, single-chip WLP technology has been referred to as super-CSP, ultra-CSP, xtreme-CSP, and WL-CSP by manufacturers.

Conventional CSPs are generally required to have underfill encapsulation for reliability of solder ball interconnections, but that is not the case for WLPs. For WLPs with small dies (DNP (distance from neutral point) < ~2 mm), generally underfilling is regarded as optional and not a requirement [30]. In the case of larger dies (5–10 mm), underfilling can be required depending on the specific applications.

Petitioner Samsung Ex-1055, 0175

The encapsulation process in WLPs can take place either on the wafer or on the chip. Encapsulation before wafer dicing is not considered a criteria for wafer-level packaging.

WLPs are encapsulated by a variety of methods. For WLPs with smaller-sized dies and solder balls, the conventional underfilling technology applied to CSPs is not suitable and alternative encapsulation methods are used. One method is printing encapsulation, which was discussed in the previous section. Printing encapsulation has the advantage of encapsulation in small spaces. An example of WL-CSP encapsulated with printing technology was shown in Fig. 3.27.

Another encapsulation method used for WLPs is compression molding. Figure 3.28 shows a WL-CSP by Fujitsu encapsulated by compression molding. Figure 3.29 shows the process for compression molding. A temporary film is placed between the upper mold and the encapsulation to protect the metal post during compression molding and eliminate molding residue during the release. Figure 3.30 shows the process flow for wafer-level packaging which in this case includes encapsulation on the wafer and before dicing.

3.7 Encapsulation of 3D Packages

Three-dimensional packages can be encapsulated using a variety of techniques. Encapsulation of 3D packages can take place on the wafer (3D wafer-level encapsulation) or on the chips (3D chip-level encapsulation).

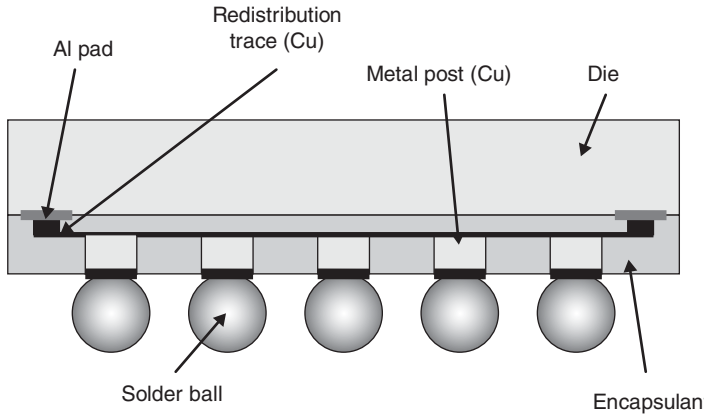


Figure 3.28 Cross-section of a wafer-level chip-scale package (Super CSP™) from Fujitsu [31].

Petitioner Samsung Ex-1055, 0176

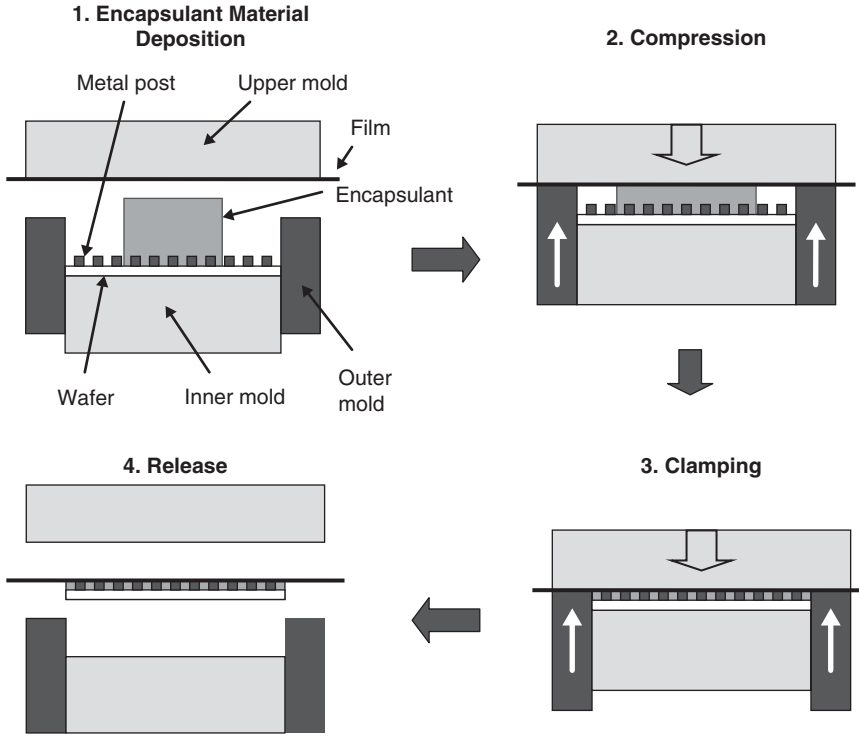


Figure 3.29 Compression molding method used for the encapsulation of a wafer-level chip-scale package (Super CSP™) from Fujitsu [31].

Encapsulation methods such as transfer molding and injection molding, traditionally used for 2D packages, are also applicable to some 3D package designs. Figure 3.31 shows a 3D stacked die leadless package with wire bonding encapsulated using transfer molding from Nippon Electric Company, Ltd. Figure 3.32 shows a 3D leaded package with injection molding encapsulation from Samsung.

Compression molding can also be used for 3D stacked chip-level packages or WLPs with contact bumps. Figure 3.33 depicts encapsulation of an MCM stack package by compression molding from Hitachi.

3D package based on the Thomson approach (Fig. 3.34) can be encapsulated by potting [32]. The die stack assembly is positioned inside a mold (or cast) and liquid potting encapsulant is poured into the mold. After the encapsulant is hardened, the molded structure is cut to expose the wires. A final step is the metallization for interconnection.

An encapsulation technique specific to 3D packaging is the chip-in-polymer (CIP) [33]. Figure 3.35 shows the process flow for a CIP package.

Petitioner Samsung Ex-1055, 0177

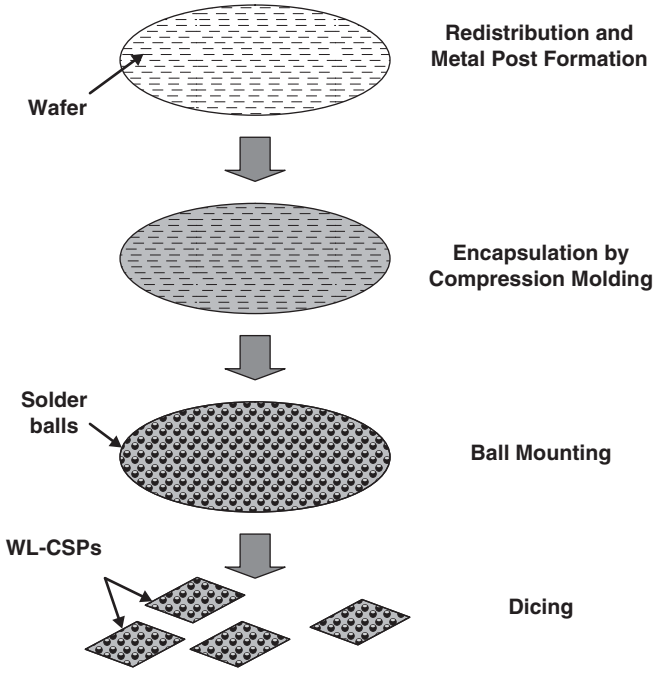


Figure 3.30 Process flow for Super CSP™ using wafer-level packaging from Fujitsu [31].

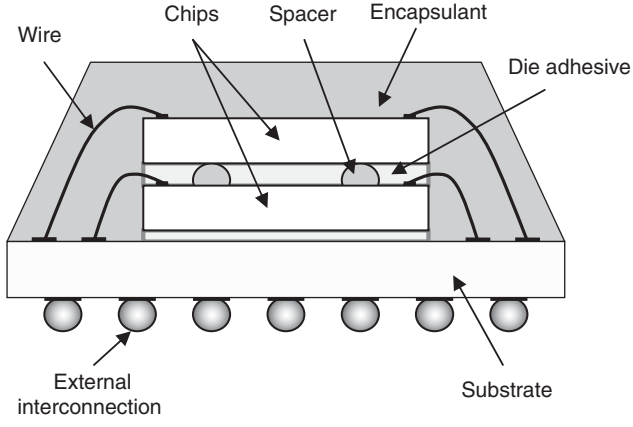


Figure 3.31 Die stack encapsulation using transfer molding from Nippon Electric Company, Ltd. [34].

Petitioner Samsung Ex-1055, 0178

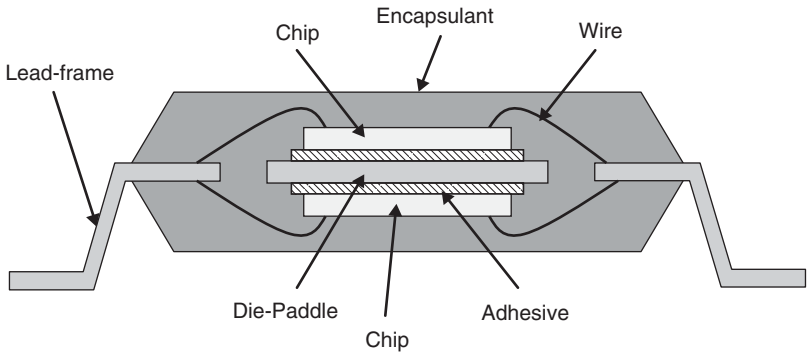


Figure 3.32 Die stack with injection molding encapsulation from Samsung [35].

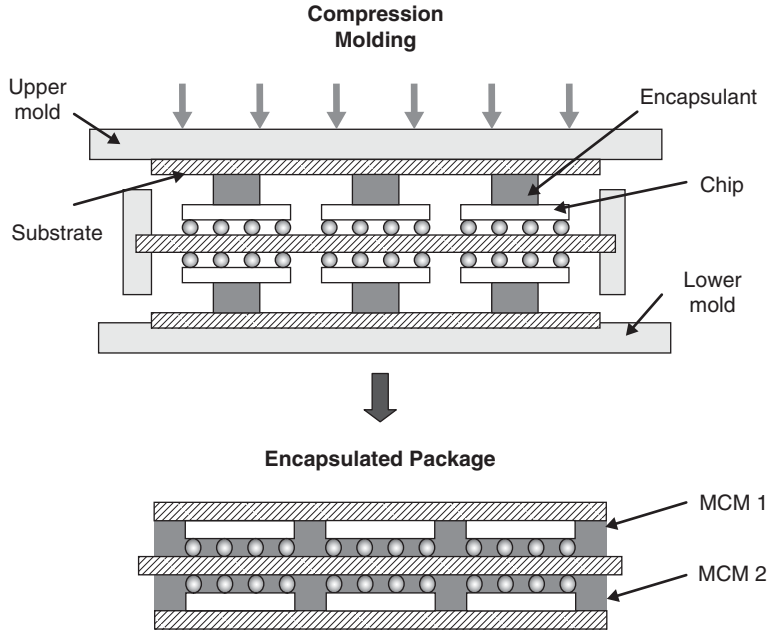


Figure 3.33 Compression molding encapsulation of a 3D multi-chip module (MCM) stack package from Hitachi [12].

First, the wafers are thinned down to less than 50 μm by spin etching, plasma etching, or dry polishing. Ultra-thin silicon wafers are highly flexible and least prone to brittle fracture. The wafer is then diced and the thin chip is glued to the substrate using an adhesive. The chip is covered with a layer of dielectric material (either epoxy resin or clad-copper foil based on

Petitioner Samsung Ex-1055, 0179

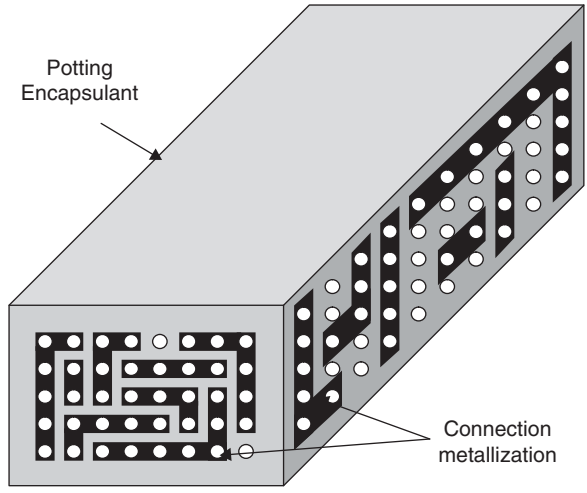


Figure 3.34 Molding encapsulation of a 3D Thomson package [36].

epoxy). Micro-vias are formed by laser drilling. The process steps are repeated to produce multiple layers of embedded chips. Finally, metal contact bumps are formed for external interconnection.

Three-dimensional die stack packages with copper (Cu) through-vias and Cu bump bonds developed by the Association of Super-Advanced Electronics Technologies are encapsulated by a method similar to no-flow underfilling and compression molding. Non-conductive particle (NCP) resin is deposited on the chip as shown in Fig. 3.36. Compressive pressure is applied on the upper chip forcing the resin to re-distribute in the spaces between the contact bumps and between the chips. This method of encapsulation uses forced flow, which is a faster process compared to capillary flow used in conventional underfilling. Another advantage of this encapsulation method is that the bump connection and encapsulation is done simultaneously (similar to no-flow underfilling). To avoid extra resin coming off along the chip edges, the NCP amount must be carefully controlled [37].

3D die stack packages manufactured using SMAFTI (SMArt chip-feed-through interconnection) technology [38] are subjected to two encapsulation steps that take place on the silicon support wafer as shown in Fig. 3.37. First, the underfill encapsulant is injected into the gaps between the die stacks and between the bottom stack and the FTI, simultaneously, to protect the contact bumps. This is similar to the conventional underfill technique used for 2D packages, except that several stacks

Petitioner Samsung Ex-1055, 0180

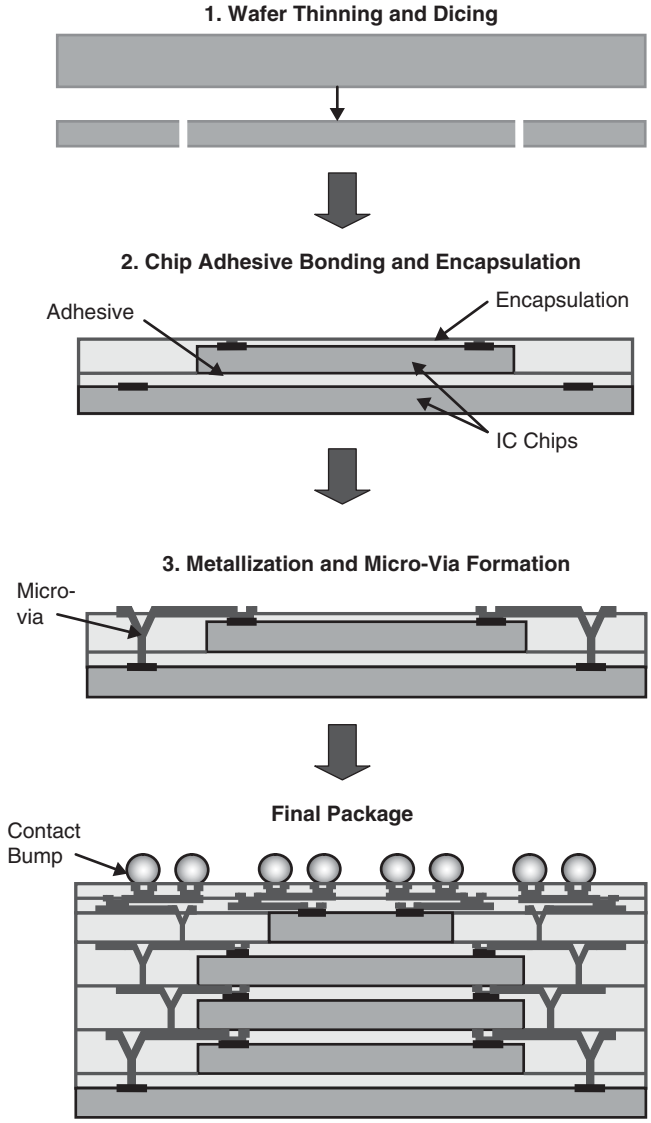


Figure 3.35 Process flow for a chip-in-polymer package.

are encapsulated simultaneously. In the second encapsulation step, the stacked chips are encapsulated using wafer molding technology where the entire wafer with multiple die stacks is overmolded. The molded wafer is then cut to produce individual molded 3D die stack packages.

Another example of simultaneous underfilling encapsulation is shown in Fig. 3.38 applied to a modular stack package [39]. Several MCMs are

Petitioner Samsung Ex-1055, 0181

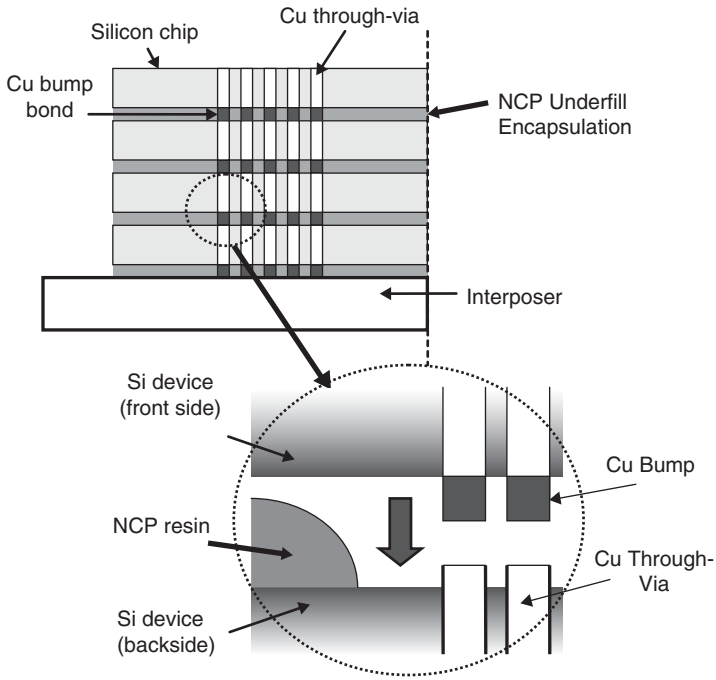


Figure 3.36 Compression molding encapsulation of stacked die interconnection bumps using non-conductive particle (NCP) resin [40].

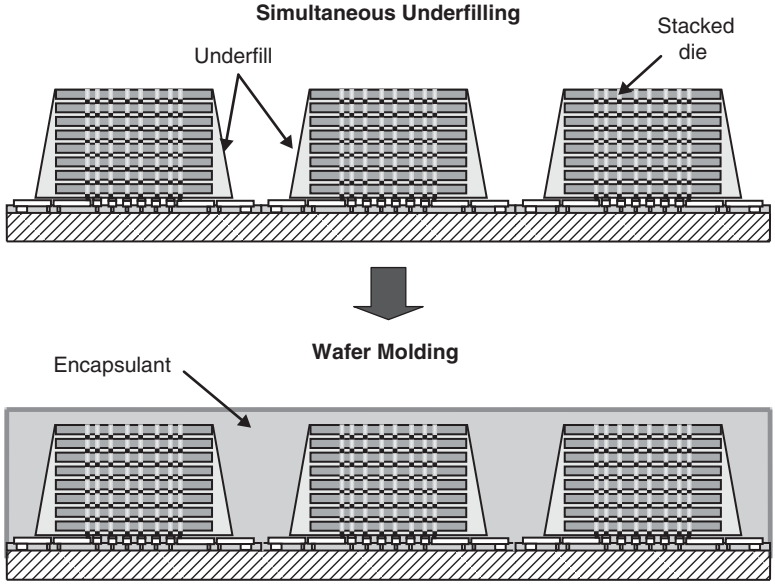


Figure 3.37 Encapsulation of wafer-level stacked dies including simultaneous underfilling and wafer molding [41].

Petitioner Samsung Ex-1055, 0182

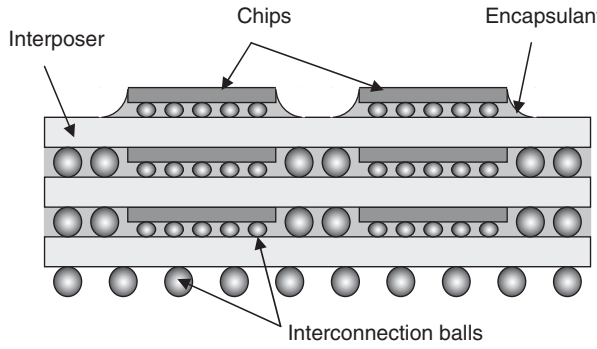


Figure 3.38 Stacked modular package [39].

stacked vertically and interconnected using ball bonding. The modular stack is then encapsulated using a one-step underfilling process where the gaps between the chips and the gaps between the module stacks are all filled simultaneously.

During underfilling encapsulation of 3D stack packages, a uniform dispensing rate is necessary to prevent wicking of the underfill material into the next layers [42]. In addition, air-entrapment can cause voids in 3D underfilling. Larger sized voids tend to occur in the lower layers and smaller voids on the upper layers. A method of spot dynamic heating can be used to assist the capillary flow to produce void-free encapsulation. In this method, a thermal gradient is induced to bias the flow patterns and flow rates leading to a void-free encapsulation of multilayer packages.

An encapsulation technique used in 3D packaging is printing encapsulation where through-vias used for z-axis interconnection are filled using cavity printing technology. Figure 3.39 shows 3D interconnection via encapsulation using VPES [43]. More than one squeegee run may be needed for complete and planar encapsulation.

3D stacked molded-interconnect device (MID) packages can be encapsulated by transfer molding techniques. Figure 3.40 shows the chip-level encapsulation and assembly of MID stacked packages. The chip is bonded to a flexible substrate (flex) and is encapsulated on one side using the transfer molding technique. The flexible substrate is then removed and contact bumps are mounted. Finally, the MID packages are stacked, bonded to one another, and the 3D stacked package is interconnected to the PCB. This process can also be modified to wafer-level packaging where instead of one chip the total wafer is encapsulated and then diced.

Petitioner Samsung Ex-1055, 0183

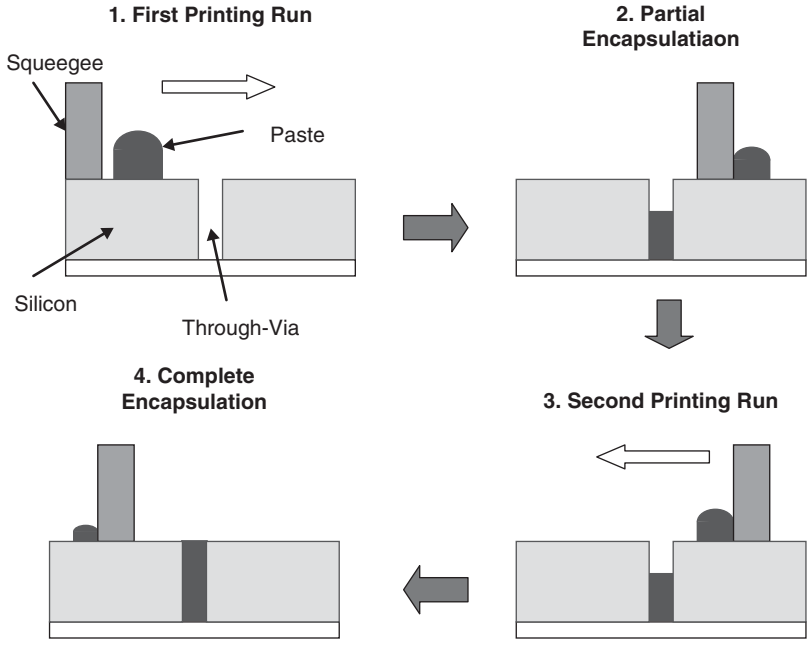


Figure 3.39 Filling 3D interconnection via using the vacuum printing encapsulation system [43].

3.8 Cleaning and Surface Preparation

Prior to encapsulation, the electronic device is cleaned to remove any undesirable substances such as oil from prior manufacturing processes. The cleaned part surface has better adhesion to the encapsulant, and thus is less prone to adhesion failures during manufacturing and operation. Plasma cleaning and deflashing are discussed next.

3.8.1 Plasma Cleaning

Plasma cleaning is a method to remove surface contaminants such as the stamping oils from the stamped lead-frames and metal oxides. It can also be used for surface modifications such as etching. Plasma cleaning can improve the adhesion strength of the internal interfaces and thereby reduce delamination.

Plasma is a mixture of positive ions, negative ions, and electrons produced by an electrostatic or electromagnetic field. The ions or charged molecules (excited radicals) remove contaminants by physically sputtering them from

Petitioner Samsung Ex-1055, 0184

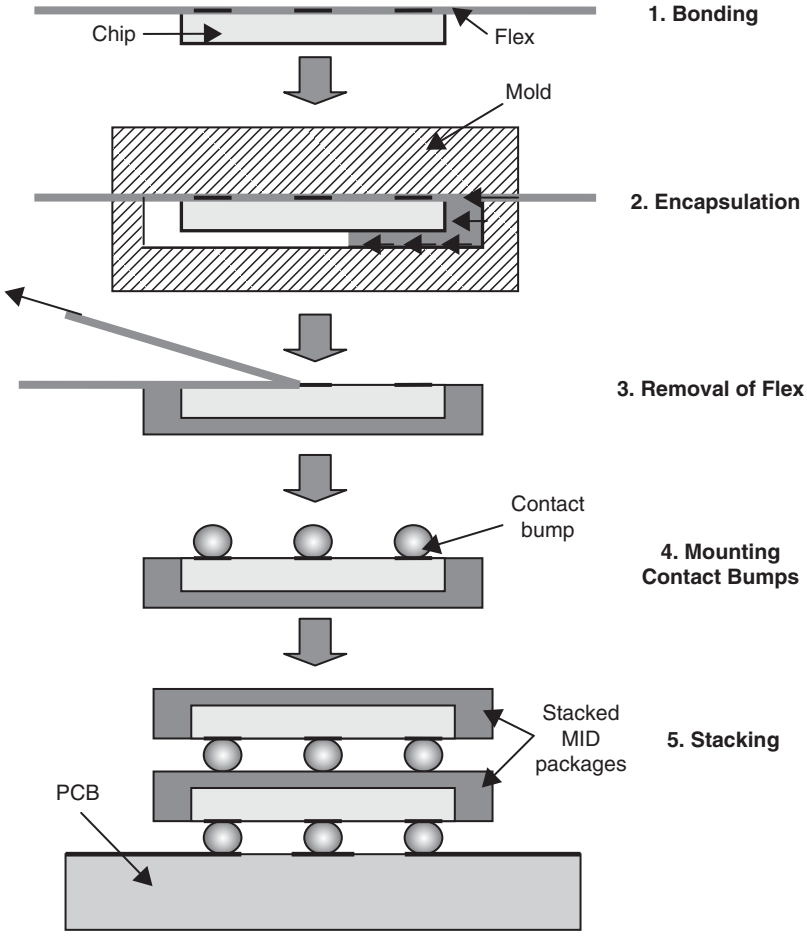


Figure 3.40 Process flow for the chip-level encapsulation and assembly of molded interconnect device (MID) stacked packages [33].

the surface or by reacting with them chemically. In chemical removal, the plasma breaks the contaminant molecules into water vapor, carbon dioxide gas, and small, volatile organic molecules. These are then exhausted from the area. Plasma cleaning processes are traditionally done in vacuum chambers using argon or oxygen plasmas.

Plasmas are effective for removal of very thin organic layers. Thus, plasma cleaning has found application in the semiconductor industry. It can improve the reliability of wire bonding by removing the contaminants from the bond pad surface, thus increasing the quality and strength of the wire bond [44]. Plasma cleaning can also be used to prepare surfaces

Petitioner Samsung Ex-1055, 0185

before plating on plastics. Plasmas are best suited for line-of-sight cleaning where the surface to be cleaned is exposed to the line of sight of the cleaning media.

Plasma cleaning of substrates is used to improve the adhesion strength of the internal interfaces and thereby reduce delamination. The reduction in delamination also leads to less popcorning. One of the components most prone to popcorning is plastic ball-grid array due to the presence of a moisture permeable organic substrate.

During plasma cleaning of BGAs, the BGAs are loaded in magazines and manually placed in a plasma etcher. Plasma is formed between the powered shelf and the grounded shelf due to capacitive coupling when electricity is supplied. The plasma chamber is pumped down to a base pressure of 90 millitorr and then filled with argon gas during plasma operation, which lasts five minutes. As argon is an inert gas, the surface cleaning occurs due to physical processes only. This is similar to sputtering where argon abrades atoms from the surface. This is equivalent to activating the surface for better adhesion by removing organic contaminants. Figure 3.41 shows a YES plasma cleaning system (Glen Technologies).



Figure 3.41 YES G1000 plasma cleaner (Glen Technologies).

Petitioner Samsung Ex-1055, 0186

Plasma cleaning can also use oxygen, ozone, or UV rays during the cleaning process instead of argon. Studies conducted at SGS Thompson used an oxygen plasma instead of argon for the inert ambient, but otherwise used the same plasma cleaning equipment. Oxygen may clean faster, as it can react chemically with the surface contaminants and also clean by physical bombardment. However, oxygen can sometimes overetch the substrate, and its effects are not so reproducible or controllable. From a safety point of view, oxygen is also not as convenient as argon. Ozone and UV for cleaning instead of plasma cleaning have also been tried. These experiments were performed on glob-top BGAs and plastic-leaded chip carriers. Similar results are obtained, but mostly in a laboratory environment as opposed to a production line. Ozone cleaning can be done at atmospheric pressure and is fairly inexpensive, but treats one surface at a time. Plasma cleaning is a volume process that can be performed on many packages simultaneously in magazines. Hence the plasma cleaning throughput can be large.

Cleaning with plasma provides the best results if conducted before die attach and before molding. Comparisons of plasma cleaning studies can be seen in Table 3.3.

Table 3.3 Comparisons of Plasma Cleaning Studies

Company	Package	Cleaning	Conclusion
Alphatec Study	PBGA	Plasma (Ar)	Delamination is reduced dramatically by plasma cleaning, especially before overmolding
SGS Thompson	PBGA	Plasma (O_2)	Solder mask to mold adhesion improves dramatically, plasma process window is wide, and process time is very short
Motorola	TQFP	Plasma (Ar)	Cleaning greatly improves adhesion between mold and copper lead-frame and between mold and polyimide die coating
Motorola	GTBGA	Plasma ($He + O_2$)/UV	Cleaning before overmolding is most important
Motorola	PLCC	O_3/UV	Cleaning before overmolding is important

GTBGA: Glob-top ball-grid array; PBGA: Plastic ball-grid array; PLCC: Plastic-leaded chip carrier; TQFP: Thin quad flatpack.

Petitioner Samsung Ex-1055, 0187

Plasma cleaning in vacuum, also known as low-pressure plasma (LPP) cleaning, has the advantages of suitable processing temperatures for thermally sensitive electronics and uniform glow discharge that produce the same rate of material processing over large areas. However, there are also several disadvantages to LPP cleaning. Vacuum equipments are expensive and require maintenance. Robotic assemblies maybe needed to take the object in and out of the vacuum system. Also, the size of the objects to be subjected to LPP cleaning is limited by the size of the vacuum chamber [45].

An alternative to LPP is atmospheric-pressure plasma (APP). There are two types of APP sources: thermal and non-thermal. Thermal APP sources are not suitable for electronics applications due to extremely high processing temperatures ranging from 400°C to 3,000°C [45]. A type of non-thermal plasma discharge suitable for semiconductor material processing is the atmospheric-pressure plasma jet (APPJ). APPJ can be used for surface cleaning and modification, selective etching, and thin-film deposition. APPJ has almost all the advantages of LPP sources such as suitable processing temperatures and uniform discharge, but without the vacuum-related drawbacks [45–47].

The APP source consists of two closely spaced electrodes that can be of various configurations. A common electrode configuration for APPJ consists of two concentric cylinder electrodes with the inner electrode grounded and the outer electrode powered at 13.56 MHz [46,47]. Helium and other gasses enter the jet from the gas feeder and flow in between the two electrodes. Figure 3.42 shows an APPJ apparatus. As the gas passes through the electrodes space, it becomes excited and ionized. The fast-flowing effluent consisting of ions and electrons exits the jet through the exit nozzle and bombards the surface to be cleaned.

3.8.2 Deflashing

During the molding process, molding compound can flow through the mold parting line and onto the leads of the device. In its thinnest form, this material is known as resin bleed. A thicker bleed of material is known as flash. If this material is left on the leads, it can cause problems in the downstream operations of lead trimming, forming, and solder dipping and/or plating.

The deflashing process usually consists of mechanical abrasion to remove both light and heavy flash material from the lead-frame. If only

Petitioner Samsung Ex-1055, 0188

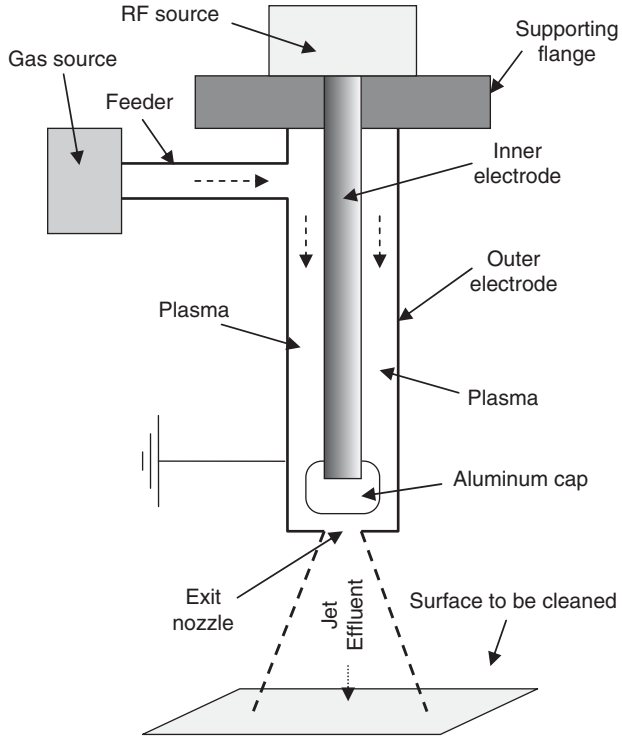


Figure 3.42 The atmospheric-pressure plasma jet apparatus [48].

a thin resin bleed is present, it may be chemically softened followed by mechanical removal of the residue [49]. Media deflashers use a mixture of pressurized air and an abrasive to mechanically remove the material from the surface of the lead-frame. In many cases, a plastic granular medium is used to remove the flash and slightly abrade the lead-frame. The use of natural media, such as walnut shells and apricot pits, is not recommended, as these materials tend to leave an oily residue behind that hinders solder dipping. After removing the resin, the plastic medium will also matte-finish the lead-frame. This roughening can enhance the adhesion of the solder material to the lead-frame, increasing the durability of the solder adhesion during the steam aging test. Another method of deflashing uses a slurry mixture of water and abrasive material and high-pressure water to remove the resin from the lead-frame; however, this does not abrade the lead-frame in any way to enhance soldering.

Petitioner Samsung Ex-1055, 0189

In some cases, media deflashing can be used to remove the plastic junk from between the dam bar and package body. If this is not accomplished during deflashing, the device must be fed through a dejunking operation to prevent damage in the trim-and-form operation.

3.9 Summary

There are five main types of encapsulation technologies used in electronic applications: molding, glob-topping, potting, underfilling, and printing encapsulation. Molding technologies used for the encapsulation of microelectronic devices include transfer molding, injection molding, reaction-injection molding, and compression molding. Transfer molding is the most popular encapsulation method. Compression molding has application in MCM packages and WLPs.

Glob-topping is the direct encapsulation of the microelectronic device such as flip-chip and chip-on-board on the printed circuit board. It consists of two techniques: glob-top and dam-and-fill. The potting method is generally used for the encapsulation of larger electronic units such as connectors and power supplies. Underfilling is used for encapsulating and protecting the solder-ball interconnects and flip-chip and BGA packages. There are two methods of underfill dispensing techniques: conventional flow and no-flow. Printing encapsulation has been used for BGAs, CSPs, MCMs, WLPs, and light-emitting-diodes. Printing encapsulation can be further classified into stencil printing and cavity printing.

The two most common encapsulation techniques used for 2D WLPs include compression molding and printing encapsulation. 3D packages are encapsulated in a variety of techniques. Conventional encapsulation methods such as transfer molding and injection molding can also be applied to stacked die packages with wire bonding. Compression molding can be applied to stacked chip-level packages or WLPs with contact bumps. More complex 3D packages such as Thomson package with multiple stacks of wire-bonded chips can be encapsulated by potting or casting. 3D stacked WLPs with contact bump interconnections can also be encapsulated using simultaneous underfilling of multiple layers and wafer-level molding.

Cleaning and surface preparation techniques include plasma cleaning and deflashing. Plasma cleaning removes the stamping oils and other contaminants from the lead-frames by using ionized gasses. The deflashing process consists of mechanical abrasion to remove flash material from the lead-frame.

Petitioner Samsung Ex-1055, 0190

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Petitioner Samsung Ex-1055, 0192

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Petitioner Samsung Ex-1055, 0193

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Petitioner Samsung Ex-1055, 0194

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4 Characterization of Encapsulant Properties

Encapsulants are typically characterized by a set of properties and parameters that determine their suitability for a given application and process. The properties of encapsulant materials can be classified into four groups: (1) manufacturing properties, (2) hygro-thermomechanical properties, (3) electrical properties, and (4) chemical properties. Table 4.1 provides some of the typical properties of encapsulants provided by manufacturers and suppliers.

From the manufacturing perspective, viscosity and flow characteristics, gel time, and curing and post-curing times and temperatures are important properties that determine which encapsulant material or encapsulation technique should be used.

From a performance and functional viewpoint, key properties range from mechanical including flexural modulus and strength to electrical properties including dielectric constant and dissipation factor to hygroscopic including moisture absorption and diffusion coefficient.

4.1 Manufacturing Properties

The properties of encapsulant materials during the manufacturing and encapsulation process are critical in determining suitability of the materials for a particular encapsulation technique or packaging design. Manufacturing characteristics include spiral flow length, bleed and flash, gelation time, polymerization rate, hot hardness, and curing and post-curing times and temperatures.

4.1.1 Spiral Flow Length

The ASTM D3123 [1] or SEMI G11-88 [2] test consists of flowing molding compound through a spiral coil of semicircular cross-section until the flow ceases. The spiral flow test is not a viscometric (viscosity measurement) test. It is a test that evaluates the heat-induced melting (or fusion) of encapsulant material under pressure, melt viscosity, and gelation rate. The spiral flow test is used both to compare different materials and to control molding compound quality. However, it cannot resolve the viscous and kinetic contributions to the flow length. Higher viscosity and

Petitioner Samsung Ex-1055, 0196

Table 4.1 Typical Properties of Encapsulants Frequently Reported by Suppliers

Group	Properties and Characteristics	Unit
Manufacturing properties	Spiral flow	cm
	Gel time	sec
	Viscosity	poise
	Shear rate	sec^{-1}
	Cure temperature	°C
	Cure time	sec
	Hot hardness	–
	Post-cure time	hour
Hygro-thermomechanical properties	Coefficient of thermal expansion (CTE1 and CTE2)	ppm/°C
	Glass transition temperature	°C
	Flexural strength	MPa
	Flexural modulus	GPa
	Elongation	%
	Moisture absorption	%
	Moisture diffusion coefficient	cm^2/sec
	Thermal conductivity	W/m K
Electrical properties	Volume resistivity	Ohm cm
	Dielectric constant	–
	Dielectric strength	MV/m or V/mil
	Dissipation factor	%
Chemical properties	Ionic impurity	ppm
	Flammability	UL rate

longer gel time could compensate each other to provide identical flow lengths. The molding tool used in this test is shown in Fig. 4.1.

A "ram-follower" device, specified in SEMI G11-88 [2], is a transducer device that measures the linear velocity of the transfer molding ram. It can record ram displacement versus time. It can separate the molding compound flow time from the gel time (when the material ceases to flow) in the total spiral length formation time of different molding compounds. The molding tool used in the spiral flow test covers the range of several hundreds per second of shear rate, and thus the test results have no impact on yield and productivity. The SEMI G11-88 [2] test results can be used for improving molding process quality by defining the mold flow lengths and times that are most compatible with the particular molding tool.

Petitioner Samsung Ex-1055, 0197

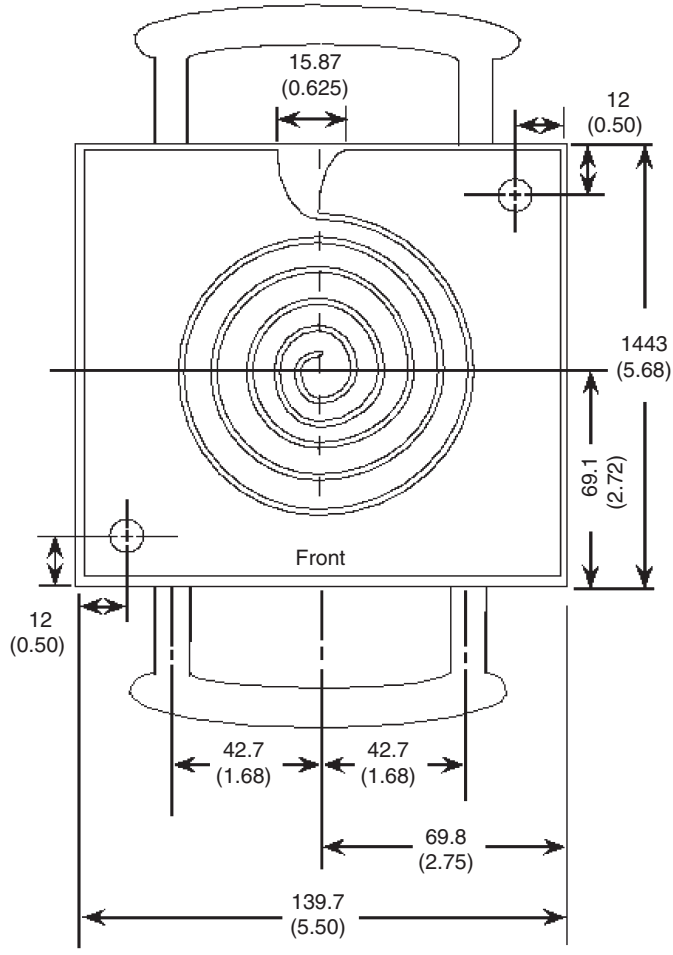


Figure 4.1 Molding tool used for the spiral flow length test from ASTM D3123 [1].

4.1.2 Gelation Time

The gelation time is the amount of time it takes for the plastic encapsulant in the liquid form to transform into a gel. The encapsulant in the gel form is a highly viscous material that can no longer flow or be smeared into a thin coating. The gelation time of a thermoset molding compound is usually measured with a gel plate. In gel time evaluation with a gel plate, a small amount of the molding compound powder is softened to a thick fluid on a precisely controlled hot plate (usually set at 170°C) and periodically probed to determine gelation.

Petitioner Samsung Ex-1055, 0198

The SEMI G11-88 [2] standard recommends using the spiral flow test as a comparative evaluator. Gelation times indicate the productivity of a molding compound. Shorter gelation times lead to faster polymerizations rates and shorter times for mold cycle, increasing production.

4.1.3 Bleed and Flash

Resin bleed and flash are molding problems where the molding compound unintentionally flows out of the cavity and onto the lead-frame at the parting line of the mold. Whereas flash is caused by the escape of the entire molding compound, resin bleed includes only the strained out resin. Although the root causes of these two problems can be traced back to the processing conditions of molding, the mold design, and mold defects, resin bleed is generally considered to be more related to the molding compound material. Resin bleed occurs more often with formulations containing low viscosity resin and large filler particles. Also, the process conditions such as excessive packaging pressure applied after the cavity has filled or too low clamping pressure applied to the mold halves can lead to resin bleed.

SEMI G45-88 is a standardized test for assessing a material's potential for resin bleed and flash. It is a transfer molding experiment that measures the flow of molding compound in a shallow channel mold (6–75 μm) and simulates flash and bleed in production tools. The propensity of resin bleed and flash from improper molding compound properties is indicated by long spiral flow lengths obtained in that test.

4.1.4 Rheological Compatibility

The rheological compatibility of a molding compound with a device to be packaged can be tested in a molding tool by trial molding operation. Rheological incompatibility can cause wire sweep, die-paddle shifting, or incomplete filling of the mold cavity resulting in voids. X-ray analysis of the molded packages and cross-sectioning of the molded bodies through the paddle support are the primary methods of evaluation for these trials. Long wire bond spans (>2.5 mm) and oversized paddle supports are normally used to create worst case scenarios of wire sweep and paddle shift.

The mold-filling characteristics are controlled by the pressure drop through the gates, where the molding compound experiences maximum shear stress. Highly viscous molding compounds at high deformation rates

Petitioner Samsung Ex-1055, 0199

in the gates can lead to incomplete filling problems. The molding compound flow through the gates closely approximates the flow through a sudden contraction or a converging channel, and has both shear and extensional (rheological term analogous to normal) stress components.

Statistically confident sampling of all stochastic phenomena, such as gate clogging by gel or filler particles, requires a large number of molded packages. The analysis of mold trial results should consider molding compound density and the consequent package sectioning analysis for porosity appraisal.

Incomplete filling of the mold due to low packing pressure can lead to high porosity in the encapsulant. Highly porous encapsulant can allow excessive moisture penetration, which can damage the molded device. This problem is more common in molding tools that have a large number of cavities (>150), packages of large volume such as plastic quad flatpacks and large chip carriers, or package designs with four-sided leads requiring corner gating.

Moisture has a profound effect on decreasing the viscosity of epoxy molding compounds, and the degree of this effect is a function of the additives and curing agents used in different formulations [3]. Compared to dry conditions, moisture can decrease the viscosity of molten molding compound up to 40% (or more) at ~0.2 wt% water (or higher).

The effect of moisture on reduction of viscosity with respect to shear rate known as "shear thinning behavior" is shown in Fig. 4.2. The viscosity of a molding compound with moisture is simply lowered with little change in shear rate dependence and power-law index. Although moisture-induced melt viscosity lowering is beneficial in overcoming flow-stress-induced and mold filling problems, excessive moisture content can cause excessive resin bleed and voids. Therefore, the moisture sorption properties of molding compounds and the degree of effect of moisture on shear thinning behavior are important factors in the selection of a molding compound.

4.1.5 Polymerization Rate

The encapsulant material's polymerization reaction may include several competing reactions among three or four reactive species. The chain segments that form are complicated and difficult to predict. Thus, thermal analysis methods, which assume that the fraction of the total heat of reaction liberated is proportional to the fraction of complete chemical conversion, are preferred for these types of highly filled opaque systems. Several different empirical forms have been offered to fit conversion data for the

Petitioner Samsung Ex-1055, 0200

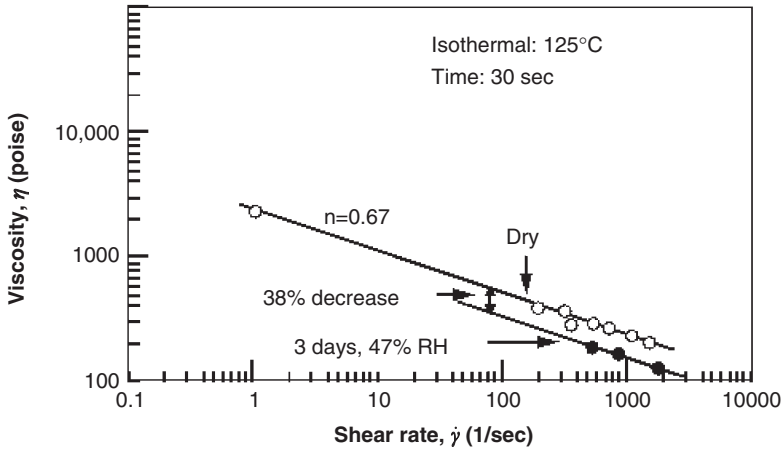


Figure 4.2 Effect of moisture on the shear thinning behavior [3].

epoxy molding compounds. They do not reflect the molecular dynamics of the reaction, but are instead phenomenological in that they assess the engineering behavior of the reaction without a theoretical basis for the reaction mechanism or reaction order. Hale et al. [4–6] developed one of the most noteworthy forms:

$$\frac{dX}{dt} = (k_{r1} + k_{r2}X^{m_r})(1-X)^{n_r} \tag{4.1}$$

where the four fitting parameters for the conversion of epoxide groups, X, as a function of reaction time are as follows: m_r and n_r are the pseudo-reaction orders and k_{r1} and k_{r2} are the rate constants. For a typical epoxy molding compound $m_r = 3.33$, $n_r = 7.88$, $k_{r1} = \exp(12.672 - 7560/\mathrm{T})$, and $k_{r2} = \exp(21.835 - 8659/\mathrm{T})$ [6]. Figure 4.3 shows the isothermal fractional conversion of epoxide groups with a drop-off in reaction rate near complete conversion. These conversion constants differ from one molding compound to the other and thus form the basis of evaluation of the polymerization rate of the compound in question. The differential scanning calorimeter (DSC) has been used to obtain the degree of polymerization of filled molding compounds [5]. By measuring the heat of reaction versus time during an isothermal cure, the fractional conversion as a function of time can be expressed as equal to the fractional total liberation of heat:

$$\frac{\Delta H_{t-t_1}}{\Delta H_{total}} = \frac{X}{100} \tag{4.2}$$

Petitioner Samsung Ex-1055, 0201

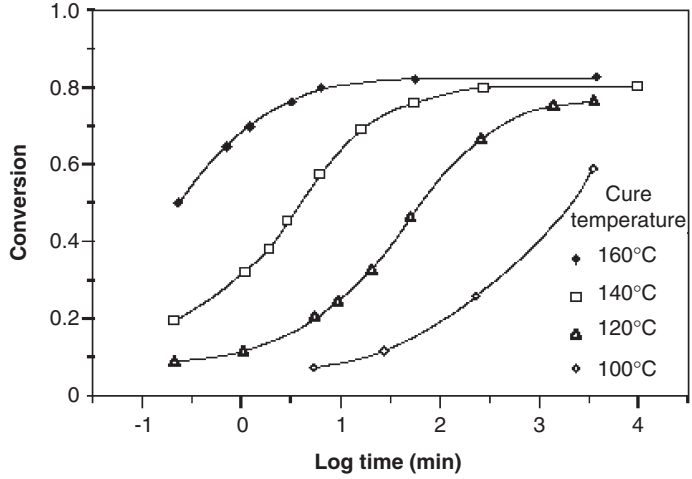


Figure 4.3 A plot of conversion versus time for an epoxy molding compound during cure [4].

An extensive analysis of the polymerization kinetics is generally not required for material selection. The secondary effects of cure kinetics such as gel time, mechanical properties, and glass transition temperature (T_g) are sufficient to compare different molding compounds effectively.

4.1.6 Curing Time and Temperature

Curing or hardening occurs when the polymer resin, in the liquid state, is transformed into a gel-like form and is eventually hardened. On a molecular level, the polymer chains in the cured state have cross-links and are constrained to move. The productivity of plastic package molding depends on the rate of the cross-linking and chemical conversion.

Mold filling can occur in as little time as 10 seconds at 150–160°C (specified by the supplier), and the cure time required before the parts can be ejected from the mold can range from 1–4 minutes. The cure time is about 70% of the molding cycle time. Shorter cure times will generally have shorter flow times into mold cavities before gelation. Multiplunger machines are designed to handle these short flow times and cure times to provide high molding productivity. Most molding tools require molding compounds that flow for 20–30 seconds and then cure to an ejectable state in less than one additional minute.

An important property related to the curing process is high-temperature hardness, also known as hot hardness. Hot hardness is the stiffness of the

Petitioner Samsung Ex-1055, 0202

encapsulant material at the end of the cure cycle. A certain degree of hot hardness is required before the molded strip of parts can be ejected safely from specific molds. The ejection of the strip from the molding tool is also dependent on the characteristics of the mold. These mold characteristics are the draft angle of the vertical surfaces, the surface finish of the tool, and the number and size of ejector pins. Different molding compounds attain this green strength at different points of the cure cycle due to either percentage conversion achieved or low modulus above the T_g. It is thus a productivity issue and can be either determined by molding trial or supplied by the vendor. A hot hardness value of about 80 on the Shore D scale within 10 seconds of opening the mold is considered acceptable.

4.1.7 Hot Hardness

An important property of the encapsulant material related to the curing process is high-temperature hardness, also known as hot hardness. Hot hardness may indicate the degree of cure of the encapsulant material at the end of the cure cycle. Hot hardness can be measured using the standardized ASTM D2240 durometer hardness method (Plastics Web, http://www.ides.com/property_descriptions/ASTMD2240.asp). In this method, the indentation resistance of the plastic encapsulant is measured from the depth of penetration of a conical indenter as shown in Fig. 4.4. Hardness values can range from 0 (indicating full penetration) to 100 (no penetration). If durometer A results are greater than 90 (indicative of a relatively hard material) then durometer D tests are used. If durometer D results are less than 20 (a relatively soft material), then durometer A tests are used.

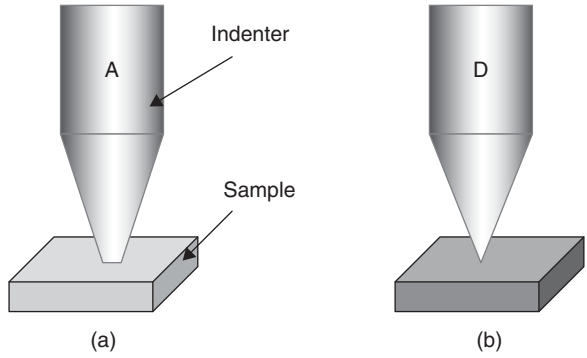


Figure 4.4 Hardness measurement from indentation resistance using (a) durometer A for softer materials and (b) durometer D for harder materials.

Petitioner Samsung Ex-1055, 0203

A certain degree of hot hardness is required before the molded strip of encapsulated parts can be ejected safely from specific molds. The ejection of the strip from the molding tool is also dependent on the characteristics of the mold. These mold characteristics are the draft angle of the vertical surfaces, the surface finish of the tool, and the number and size of ejector pins. Different molding compounds attain hot hardness at different points of the cure cycle due to either the percentage conversion achieved or low modulus above the T_g. It is thus a productivity issue and can be either determined by molding trial or supplied by the vendor. A hot hardness value of about 80 on the Shore D scale within 10 seconds of opening the mold is considered acceptable.

4.1.8 Post-cure Time and Temperature

Post-cure is the additional heating of the encapsulant after the curing process to ensure complete cross-linking of the polymer chains, and thus stabilizing the cross-linking dependent properties such as T_g. At temperatures above T_g of the material, cross-linking is more rapid. As the temperature reduces to T_g or below T_g, the rate of cure or cross-linking can become very slow [7]. This is the reason why post-cures at elevated temperatures are normally used to ensure that all of the epoxy groups are consumed [7]. Most epoxy molding compounds require about 1–4 hours of post-cure at 170–175°C for complete cure.

4.2 Hygro-thermomechanical Properties

Hygro-thermomechanical properties refer to the properties of the plastic encapsulants that are hygroscopic (moisture-related), thermal, and/or mechanical. Hygro-thermomechanical properties of encapsulant materials commonly characterized include coefficient of thermal expansion (CTE), T_g, thermal conductivity, flexural strength and modulus, tensile strength, elastic modulus, elongation, adhesion strength, moisture absorption, moisture diffusion coefficient, coefficient of hygroscopic (moisture) expansion, gas permeability, and outgassing.

4.2.1 Coefficient of Thermal Expansion and Glass Transition Temperature

The CTE of a material represents the change in dimension per unit change in temperature. The dimension can be volume, area, or length. The rate of

Petitioner Samsung Ex-1055, 0204

thermal expansion varies from material to material and with the temperature. The fact that different materials expand differently with the same increase in temperature necessitates that elements attached together have the same or similar CTEs to avoid the possibility of delamination. The T_g is an inflection point in the expansion versus temperature curve above which the rate of expansion (and therefore the CTE) increases significantly, about 3–5 times. A sample plot of CTE and T_g assignment is shown in Fig. 4.5.

CTE and T_g are two important properties that are often reported by most encapsulant suppliers. They can be measured by using a thermomechanical analyzer (TMA). The tests are described in ASTM D696 [8] or SEMI G13-82 standards. ASTM D696 [8] uses the fused quartz dilatometer to measure the CTE. The specimen is placed at the bottom of the outer dilatometer tube with the inner one resting on it. The measuring device, which is firmly attached to the outer tube, is in contact with the top of the inner tube and indicates the variations in length of the specimen with changes in temperature. Temperature changes are brought about by immersing the outer tube in a liquid bath or another controlled temperature environment maintained at the desired temperature.

To measure the CTE of a material, typically, a graph of expansion versus temperature is plotted. The CTE is the slope of the plotted line

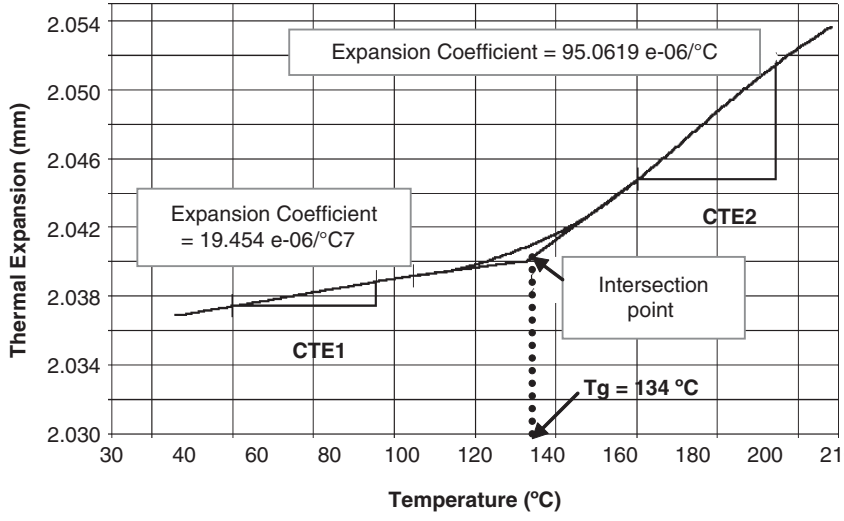


Figure 4.5 Assignment of coefficients of thermal expansion (CTEs) and glass transition temperature (T_g) of the molding compound using the thermomechanical analyzer.

Petitioner Samsung Ex-1055, 0205

(Fig. 4.5). The T_g is the intersection point between the lower temperature CTE (CTE1 or α_1) and the higher temperature CTE (CTE2 or α_2). The T_g separates the temperatures associated with a glassy polymer from that related to leathery or rubbery polymers.

The T_g, being a manifestation of the total viscoelastic response of a polymer material to an applied strain, depends on the rate of strain, the degree of strain, and the heating rate. As improper molding and post-cure conditions can affect both CTE and T_g, most plastic-encapsulated microelectronics manufacturers re-measure these parameters on a predetermined quality control schedule.

There are many techniques for measuring the T_g of plastic encapsulant materials including TMA [9], DSC [10], dynamic mechanical analysis [11], and dielectric methods [12]. Both T_g and CTE measurements are sensitive to a variety of experimental and processing factors such as measurement technique and cooling or heating rates [9,10].

A commonly used method for assigning T_g is using the TMA (Fig. 4.6). The sample is positioned on the sample holder of the TMA under the

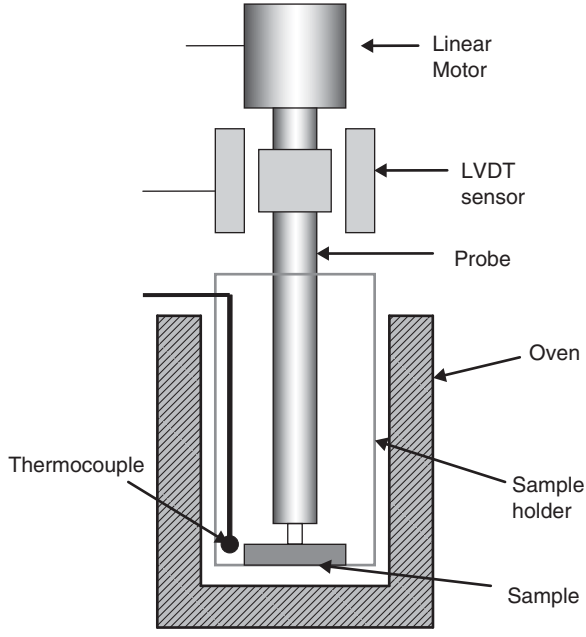


Figure 4.6 Schematics of the thermomechanical analyzer.

LVDT: Linear variable differential transformer.

Petitioner Samsung Ex-1055, 0206

probe, and the oven is enclosed around the sample and probe tip. As the temperature increases or decreases in the oven, the plastic sample will expand or shrink accordingly. The dimensional changes in the sample are measured by a linear variable differential transformer. The temperature change is monitored by the thermocouple next to the sample. A plot of dimensional change versus temperature can be produced similar to the one shown in Fig. 4.5 where CTEs and T_g can be determined.

Another method for measuring T_g is using the DSC. The schematics of the DSC are shown in Fig. 4.7. The reference and sample containers are positioned inside microfurnaces. As the microfurnace heats up, the difference in heat flow between the sample and the reference is measured and plotted. A step change in heat flow is indicative of glass transition of the material and the T_g can be assigned at the middle of the inclined line as depicted in Fig. 4.8.

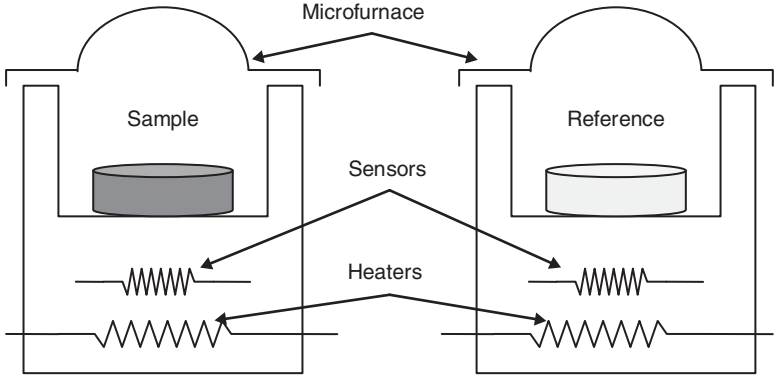


Figure 4.7 Schematics of the differential scanning calorimeter [13].

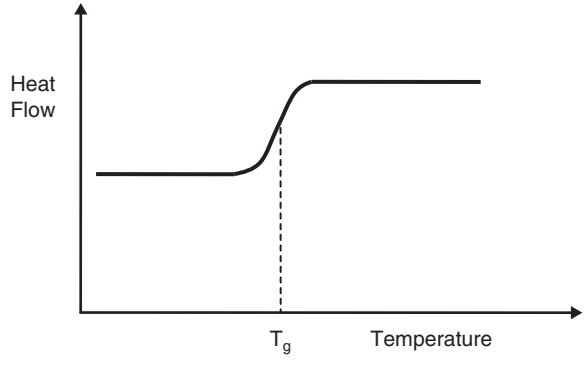


Figure 4.8 Assigning T_g using the differential scanning calorimeter.

Petitioner Samsung Ex-1055, 0207

There are many material and process parameters that can affect the T_g of the molding compound. One of these material parameters is cross-linking density. As the polymer cross-links, its segmental mobility becomes restricted and its T_g increases [7,14–16]. Figure 4.9 shows plots of T_g versus cross-linking density [15,17]. Up to 95% of potential cross-links are established during molding of integrated circuits [15].

The composition and chemistry of the molding compounds can also affect T_g and CTE. As the filler has a much lower CTE than the resin, it decreases the CTE of the molding compound**.** Post-mold curing can create additional cross-linking due to additional heat exposure of the molding compound, and can increase the T_g of the molding compound [17]. Post-mold cure effects on T_g depend on temperature, time, and type of chemistry [15].

Another factor that influences the assignment of T_g is cooling versus heating. The T_g of the encapsulant material can be determined from either heating or cooling tests. Lower cooling and heating rates can ensure more stable and precise measurements. Typical heating or cooling rates of DSC and TMA tests on dry samples can range from 5–20°C/min [10]. Furthermore, it has been found that the cooling tests produce more reproducible T_g values compared to heating tests [9,10,18]. This observation can be explained as follows: Measurement on cooling has the advantage of starting from an equilibrium state (i.e., liquid or rubbery state) that eventually reaches a non-equilibrium state (glassy state). Conversely, measurement on heating begins with a non-equilibrium state that must be first characterized [15].

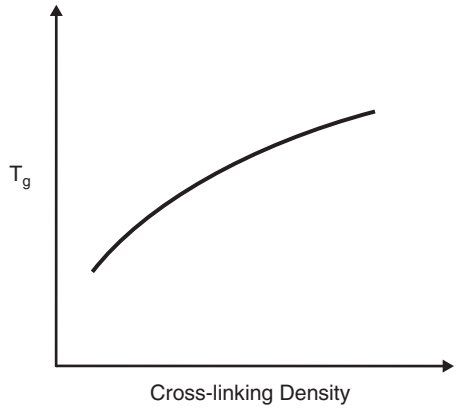


Figure 4.9 Effect of cross-linking density on the T_g of polymeric materials.

Petitioner Samsung Ex-1055, 0208

The T_g of polymeric materials can decrease due to absorbed moisture. This phenomenon can be explained using the "free volume theory." The volume of the polymeric material consists of "occupied volume" and "free volume." The occupied volume is the sum of the space occupied by the actual molecules and the volume due to thermal vibrations of the molecules (Fig. 4.10). If the spatial domains of the molecules were in perfect contact with one another, then the volume of the polymer would be equal to its occupied volume, but that is not the case. The free volume is the volume due to holes or voids caused by packing irregularities [19–22].

As the polymer is cooled from temperatures above the T_g, both occupied and free volumes decrease. The occupied volume decreases because of the reduction in thermal vibrations of the molecules. As the temperature is cooled, the free volume also decreases due to decrease in thermally activated motions (i.e., translation and rotation) of the polymer molecules. At the T_g, the free volume becomes too small to allow the molecules to change their relative position (referred to as "critical free volume") and thus the free volume is "frozen." Below the T_g, the volume of the polymeric material continues to decrease but only due to reduction in thermal vibrations of the molecules and, therefore, there is a sharp decrease in the CTE of the polymer (Fig. 4.11) [22].

As the moisture diffuses through the polymeric material, the water molecules may slide between the polymer chains and cause an increase in the free volume of the polymeric material [22]. At a temperature equal to the T_g of the dry resin, the free volume of the moisturized material will be larger than that of dry polymer. Therefore, the free volume will continue to

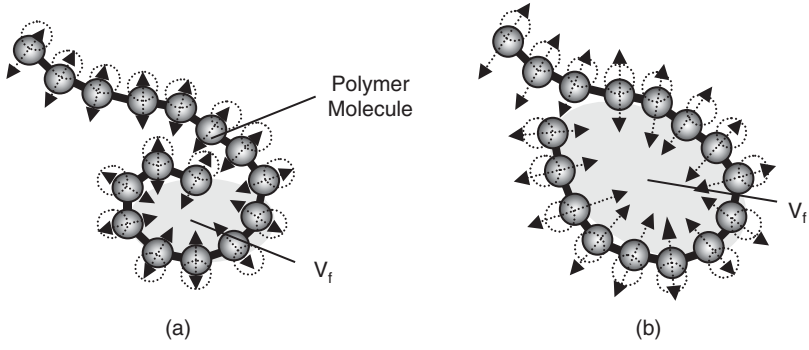


Figure 4.10 Volume expansion due to (a) thermal vibrations of the polymer molecules only (shown by ↔) and (b) thermal vibrations and relative repositioning of the molecules (shown by gray area). V_f is the free volume.

Petitioner Samsung Ex-1055, 0209

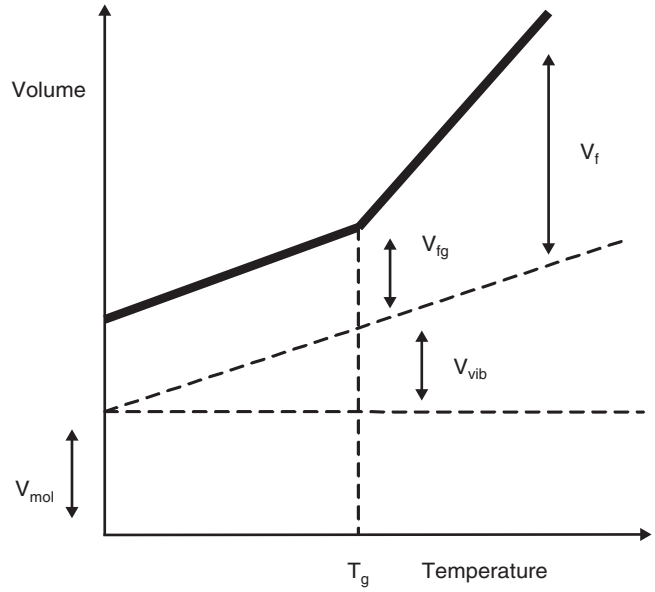


Figure 4.11 Free volume theory, where V_{mol} is the actual space occupied by polymer molecules, V_{vib} is the volume due to thermal vibrations of the molecules, V_{fg} is the free volume "frozen" at T_g, and V_f is the free volume above T_g.

decrease even below the T_g of the dry polymer until it reaches the critical free volume where the polymer chains are immobilized. This lower temperature at which the critical free volume has been reached is the effective glass transition temperature of the moisturized resin.

4.2.2 Thermal Conductivity

Thermal conductivity is the material's intrinsic capability to diffuse heat. Alternatively, in an electrical analogy (used frequently), the inverse of thermal conductivity (i.e., the thermal resistivity) is the material's propensity to impede the flow of heat. More formally, thermal conductivity can be expressed in terms of the Fourier's law of steady-state heat conduction (in one dimension along the x-direction):

$$Q = kA\frac{dT}{dx} \tag{4.3}$$

where Q is the heat flow (measured in watts), k is the thermal conductivity (units of W/m K), A is the cross-sectional area perpendicular to which the heat is flowing, and T is the temperature. Again, to draw an analogy to

Petitioner Samsung Ex-1055, 0210

electrostatics, Q would signify current, the temperature differential dT corresponds to the potential difference, while dx/kA is the material's resistance to current (heat flow).

A commonly used technique for measuring heat conductivity is the standardized ASTM C177 guarded hot-plate method [23]. In the guarded hot-plate apparatus [23], two identical specimens are positioned on opposite sides of the main heater (Fig. 4.12). The main and guard heaters are maintained at the same temperature. The auxiliary heaters are kept at a lower temperature. The purpose of guard heaters is to minimize the amount of lateral heat transfer from the main heater. The heat flow Q is supplied electrically and is therefore known. Thermocouples are placed at each surface to monitor the temperatures. Therefore, the temperature difference, ΔT, across the specimen length, ΔL, can be measured. When temperature and voltage readings become steady, thermal equilibrium has been reached. The thermal conductivity of the plastic specimen is determined by:

$$k = \frac{Q/A}{\Delta T/\Delta L} \tag{4.4}$$

Thermal conductivity is an important property of an encapsulant used for high heat dissipating devices or for devices with long duty cycles. When designing or determining appropriate thermal management systems for a given electronic system or package, the encapsulant material often lies in the path through which heat is being dissipated. Knowledge of this

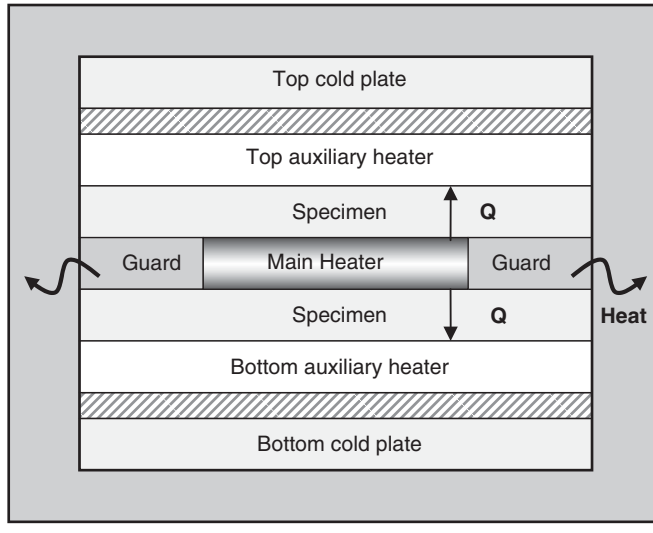


Figure 4.12 Guarded hot-plate technique for measurement of thermal conductivity.

Petitioner Samsung Ex-1055, 0211

material parameter is thus critical for designing the overall thermal management system. Although one would like this value to be as high as possible, typically as characteristic of most polymers, the thermal conductivity of encapsulants is rather low (~0.2 W/m K, in contrast to, for example, copper, 385 W/m K).

4.2.3 Flexural Strength and Modulus

Mechanical properties of encapsulants include elastic modulus (E), %elongation, flexural strength (S), flexural modulus (E_B), shear modulus (G), and cracking potential. Mechanical properties play an important role in package stresses. Lowering of stress factors (i.e., elastic modulus, %strain, CTE) can lead to lower stress and thus higher reliability. For example, the tensile stresses in a plastic package can depend on elastic modulus and tensile strain (i.e., due to CTE mismatch) as shown in Young's equation:

$$\sigma = E\varepsilon \tag{4.5}$$

The flexural strength and flexural modulus are derived from the standardized ASTM D790-71 and ASTM D732-85 tests and reported by suppliers. ASTM D790 suggests two test procedures to determine the flexural strength and flexural modulus. The first procedure suggested is a three-point loading system utilizing center loading on a simply supported beam (Fig. 4.13). This procedure is designed principally for materials that break at comparatively small deflections. In this procedure the bar rests on two

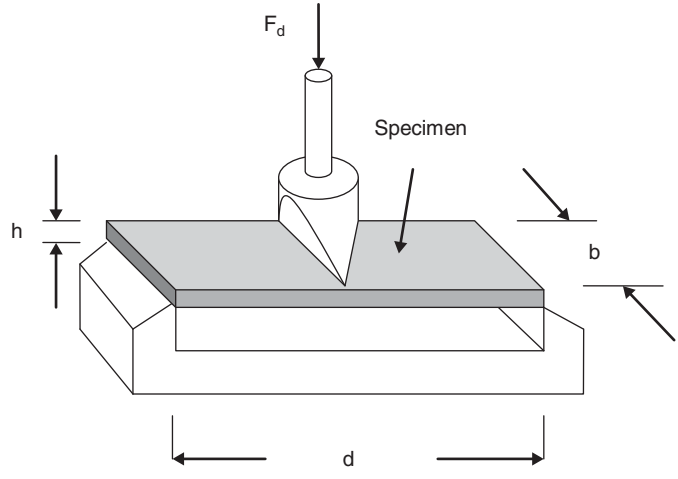


Figure 4.13 Schematics of the three-point bend test [13].

Petitioner Samsung Ex-1055, 0212

supports and is loaded by means of a loading nose midway between the supports.

The second procedure involves a four-point loading system utilizing two load points equally spaced from their adjacent support points with a distance of either one-third or one-half of the support span. This test procedure is designed particularly for large deflections during testing. In either of the cases, the specimen is deflected until rupture occurs in the outer fiber. The flexural strength is equal to the maximum stress in the outer fiber at the moment of break. It is calculated using

$$S = \frac{3P_{rupture}l}{2(b_{beam})^3 d} \tag{4.6}$$

where S is the flexural strength, $P_{rupture}$ is the load at rupture, l is the support span, b_{beam} is the width of the beam, and d is the depth of the beam.

The flexural modulus is calculated by drawing a tangent to the steepest initial straight-line portion of the load deflection curve, and is given by

$$E_B = \frac{l^3 m}{4 b_{beam} d^3} \tag{4.7}$$

where m is the slope of the tangent to the initial straight-line portion of the load deflection curve and E_B is the flexural modulus.

4.2.4 Tensile Strength, Elastic and Shear Modulus, and %Elongation

The tensile modulus, tensile strength, and %elongation are derived from ASTM D638 and D2990 test methods [24,25]. The tensile properties of molding compounds, determined according to ASTM D638, use "dog-bone" shaped molded or cut specimens with fixed dimensions and held by two grips at the ends. Care is taken to align the long axis of the specimen and the grips with an imaginary line joining the points of attachment of the grips to the machine. They are incrementally loaded to obtain stress–strain data at any desired temperature. A typical curve is shown in Fig. 4.14.

The tensile strength can be calculated by dividing the maximum load (in newtons) by the original minimum cross-section area of the specimen (in m^2). The %elongation is calculated by dividing the extension at break by the original gauge length and this ratio is expressed as a percentage. The modulus of elasticity is obtained by calculating the slope of the initial linear portion of the stress–strain curve. If Poisson's ratio for the material is known or separately determined from tensile strain measurements,

Petitioner Samsung Ex-1055, 0213

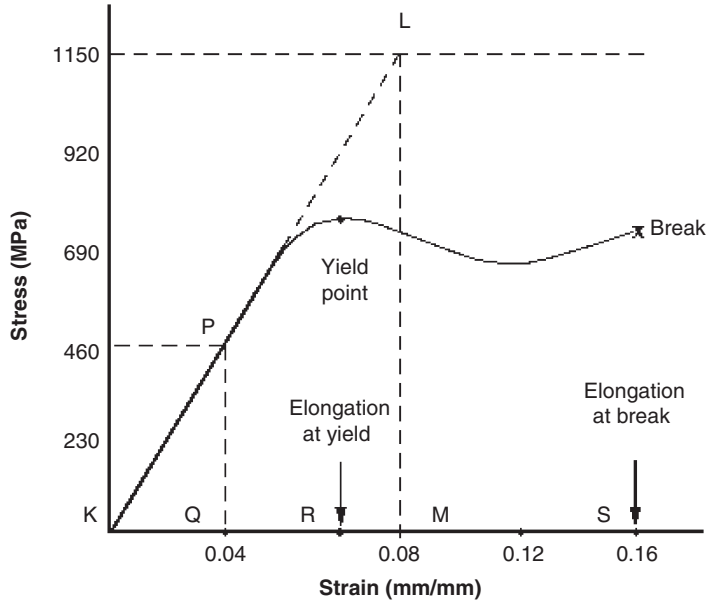


Figure 4.14 A typical curve of incrementally loaded specimens from stress–strain data.

the shear modulus of the molding compound can be estimated. It is important to note that the stresses encountered in encapsulated microelectronics are actually a complex mixture of tensile and shear stresses.

The evaluation of the cracking potential of the molding compound is particularly important for devices where a relatively small amount of molding compound surrounds a relatively large die (e.g., memories, small-outline packages, and ultra-thin packages). In the absence of any standard procedure for such evaluation, ASTM D256A and D256B Izod impact test procedures are commonly followed. The specimen is held as a vertical cantilever beam in test method ASTM D256A and is broken by a single swing of the pendulum with the line of initial contact being at a fixed distance from the specimen clamp and from the centerline of the notch and on the same face as the notch. A variation of this test is ASTM D256B, where the specimen is supported as a horizontal simple beam and is broken by the single swing of the pendulum with the impact line midway between the supports and directly opposite the notch. These are overstress tests for the cracking potential of epoxy molding compounds even under extreme thermomechanical stress conditions and do not test their important region of viscoelasticity. However, they are simulative of trim and form, and handling impact-induced cracking susceptibility.

Petitioner Samsung Ex-1055, 0214

A fracture test that models the actual strain history of the package for thermomechanically induced failure is the previously mentioned ASTM D790-71 three-point flexural bending test used to determine flexural modulus. Here a 0.05-mm (2-mil) diameter center-notched rectangular specimen is center strained at a rate that simulates the manufacturing cycle (i.e., 20%/min for liquid-to-liquid thermal shock and 0.1%/min for device on–off operation in air (1°C/min)). The area under the stress–strain curve is proportional to the energy to break at the test temperature. The low-temperature data are usually the discriminating factor between molding compounds because the molded body experiences the greatest stress at lower temperatures far removed from the molding temperature.

As the melt viscosity of a molding compound is shear rate-dependent and a typical mold is subject to different shear rates at different points of the molding compound flow channel, the expected shear rates for a specific molding tool need to be calculated first under no-slip boundary conditions. The general ranges of experienced shear rates are hundreds of reciprocal seconds in the runner, thousands through the gate, and tens in the cavity. Considerations must also be given to the temperature and time dependence of the shear rate-dependent viscosity of the molten molding compound.

The selection of molding compounds based on the shear dependence of viscosity should identify one that has the lowest viscosity at low shear rates and high cavity temperatures for wire sweep and/or paddle shift prone devices and in multi-cavity molds where complete filling before gelation is a concern [26]. A material whose viscosity is more temperature insensitive performs better in all suboptimal tool designs.

The time dependency of a molten molding compound's viscosity originates from two opposite phenomena. The epoxy curing process will increase the average molecular weight and, hence, the viscosity increases with time. However, the increasing molding temperature causes a decrease in viscosity leading to an overwhelming effect in the early phases of curing. Ultimately, both the molecular weight and the viscosity approach infinity at gelation. Flow-induced stresses, particularly in distant cavities, could thus be very significant at the latter stages of mold filling. Consequently, molds with longer flow lengths and longer flow times need molding compounds with longer gel times at the 150–160°C mold filling temperature. This requirement is a trade-off for higher productivity.

4.2.5 Adhesion Strength

Poor adhesion of a molding compound to the die, die-paddle, and lead-frame can lead to defects and failures such as delamination, popcorning,

Petitioner Samsung Ex-1055, 0215

chip cracking, and chip metallization deformation. Therefore, adhesion is one of the most important discriminating properties of a molding compound to be chosen for a particular physical and materials design of a package. The theory and practice of adhesion of integrated circuits' molding compounds to package elements have been treated by Kim and Nishimura et al. [27–29]. The adhesion property of molding compounds can be designed to the specific requirements of a device by adjusting highly reactive additives, polymer viscosity, and polymer reaction rates. This adjustment can lead to a significant increase in adhesion to specific substrates.

Methods for measuring the adhesion property of molding compounds include button (puck) shear, die shear, 180°C peel, and lead-frame tab pull test [28–30]. A standard method used in industry for characterizing the adhesion of mold compounds to lead-frame materials is the button (puck) shear test [31]. The schematics of the button shear test is shown in Fig. 4.15 [32]. Generally, the shear test of molding compound on a silicon sample is difficult because silicon substrates are easily fractured during testing due to their brittle properties. Therefore, the samples with fractured silicon substrates must be identified and removed and only the remaining samples can be used for adhesion measurements. Another method for measuring adhesion is the die shear test using a shear stress application method similar to the button shear test. Figure 4.16 shows a modified die shear test for adhesion strength measurement [28,29].

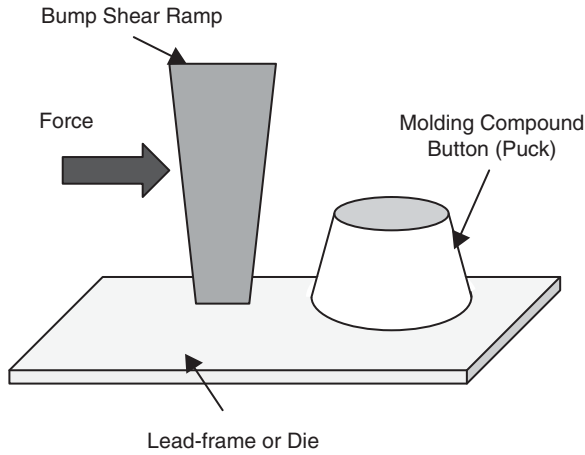


Figure 4.15 Button (puck) shear test for adhesion measurement [28,29,32].

Petitioner Samsung Ex-1055, 0216

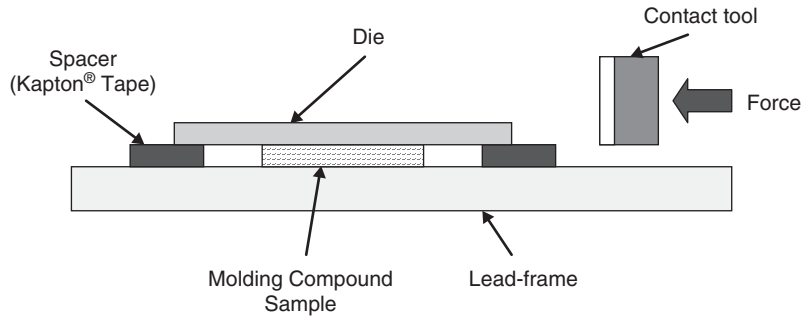


Figure 4.16 Schematics of a modified die shear adhesion test setup [28,29].

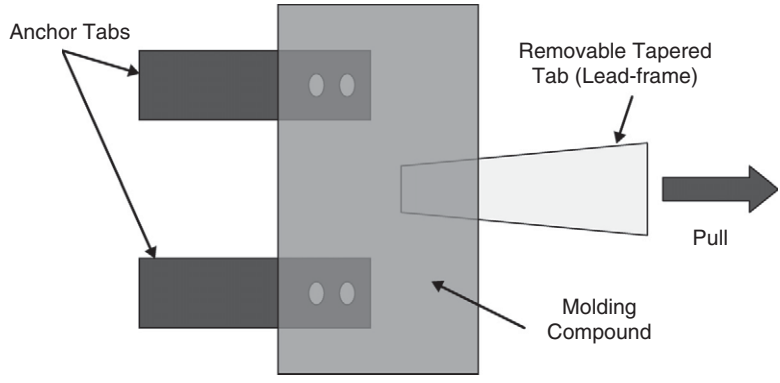


Figure 4.17 Schematics of the lead-frame tab pull test [28,29,33].

Another common adhesion test is the lead-frame tab pull test, which measures the adhesion of lead-frames to the molding compound. Figure 4.17 shows the schematics of the tab pull test. The molding compound is molded with a lead-frame tapered tab on one side and two anchor tabs on the other side that are partially inside the mold. The lead-frame tab is then pulled using a tensile tester and the adhesion strength is measured. The molding process used for this test must be identical to that used in production. For maximum simulation of manufacturing conditions, a custom designed lead-frame is used in a production mold to generate the adhesion test specimens.

Another method for adhesion strength measurement is the 180°C peel test [28,29,34]. In this method, the encapsulant material is molded on the flat surface of another material and the force required to pull them apart is measured as shown in Fig. 4.18. The other material can be a lead-frame

Petitioner Samsung Ex-1055, 0217

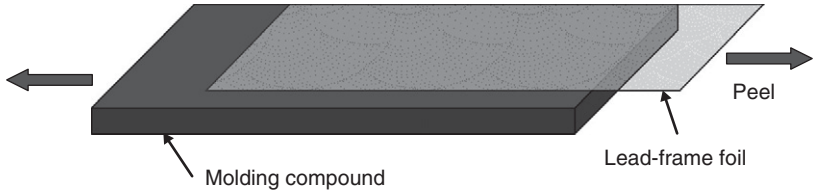


Figure 4.18 Schematics of the 180°C peel test [28,29].

and die material or a plastic coating material such as polyimide and silicone.

4.2.6 Moisture Content and Diffusion Coefficient

Due to the adverse effects of moisture on the reliability of the encapsulated device (i.e., corrosion, T_g reduction, swelling mismatch), accurate moisture content and diffusion measurements in encapsulant materials are essential for package design and materials selection. Two important parameters related to moisture absorption in polymeric materials are the moisture content and the diffusion coefficient.

Moisture content can be determined by exposing the encapsulant specimen to a specified humidity for a specified time. A common testing condition used for the evaluation of moisture content and often reported by encapsulant suppliers is soaking in boiling water for 24 hours. A common testing condition used for moisture diffusion coefficient evaluation is exposure to 85°C/85% relative humidity (RH) for one week (168 hours) which is based on the moisture sensitivity level 1 characterization in IPC/JDEC standards (IPC/JDEC J-STD-20, IPC Association Connecting Electronic Industries (originally founded as Institute for Printed Circuits) and JEDEC Solid State Technology Association (once known as the Joint Electron Device Engineering Council)). Moisture content (%) is calculated by taking the ratio of weight gain (wet weight minus dry weight) to dry weight and multiplying by 100.

Another widely used testing condition by manufacturers for characterizing the moisture absorption properties of molding compounds involves soaking the molding compound samples in distilled water [35]. The water must be maintained at a specified temperature, often at room temperature (i.e., 23°C or 73.4°F). The percentage weight gain is then measured after a specified time: either after 24 hours or until there is no weight gain (saturation moisture content).

Petitioner Samsung Ex-1055, 0218

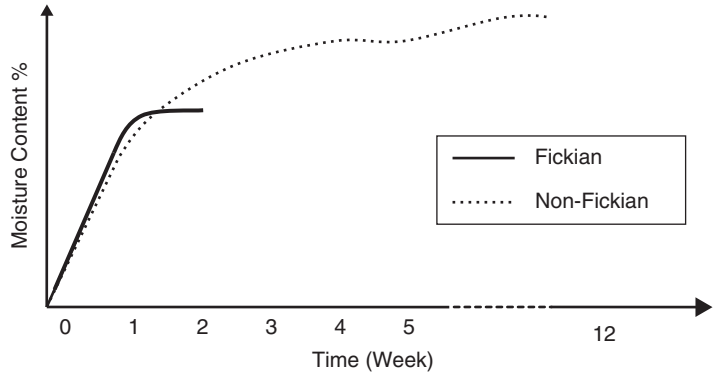


Figure 4.19 Fickian and non-Fickian moisture diffusion.

Polymeric materials can exhibit different moisture diffusion characteristics. There are essentially two main types of moisture diffusion behavior in polymers: Fickian and non-Fickian (Fig. 4.19). Simple polymeric systems generally exhibit Fickian moisture diffusion behavior. Non-Fickian behavior has been observed in encapsulant materials such as epoxy molding compounds [36–40] due to the complex nature of the hygrothermal behavior of the polymer network.

4.2.6.1 Fickian Diffusion

Assuming a thin specimen made of simple polymeric material, moisture diffusion can be modeled using one-dimensional Fick's law:

$$\frac{\partial C}{\partial t} = D\,\frac{\partial^2 C}{\partial x^2} \tag{4.8}$$

where C is the moisture concentration at time t and D is the moisture diffusion constant of the diffusion medium [41]. Applying initial and boundary conditions and solving Fick's diffusion equation [40,41], the one-dimensional Fickian moisture diffusion coefficient can be determined by

$$\frac{M_t}{M_\infty} = 4\left(\frac{Dt}{\pi l^2}\right)^{1/2} \tag{4.9}$$

where M_t is the total amount of moisture that entered the polymeric sheet at time t, M_∞ is the equilibrium moisture content (or moisture content at

Petitioner Samsung Ex-1055, 0219

infinite or very long time), l is the thickness of the plane specimen sheet, and D is the diffusion coefficient presented in cm^2/sec. M_t and M_∞ can be obtained from weight gain measurements of the polymeric specimen exposed to moisture, and D can be calculated from the slope of the M_t versus $t^{1/2}$ curve. M_t is calculated as

$$M_t\,(\%) = \frac{W(t) - W_{dry}}{W_{dry}} \times 100 \tag{4.10}$$

where $W(t)$ is the weight of the moisturized specimen at time t and W_{dry} is the weight of the dry specimen.

If the specimen exhibiting Fickian moisture diffusion is not thin and diffusion from other dimensions must be considered, then the 3D Fickian diffusion model may be used. General moisture diffusion models consist of essentially three main equations: moisture concentration, diffusivity, and solubility equations. The 3D Fickian equation related to moisture concentration is expressed as

$$\frac{\partial C}{\partial t} = D\left(\frac{\partial^2 C}{\partial x^2} + \frac{\partial^2 C}{\partial y^2} + \frac{\partial^2 C}{\partial z^2}\right) \tag{4.11}$$

where C is the local concentration (g/cm^3), x, y, and z are the Cartesian coordinates (cm), D is the diffusivity (cm^2/sec) and t is the time (sec) [41,42].

The second main equation of diffusion in polymeric materials involves the effect of temperature on the moisture diffusion coefficient, expressed as

$$D = c_1 \exp\left(-\frac{E_a}{kT}\right) \tag{4.12}$$

where c_1 is a constant, E_a is the activation energy (eV), k is Boltzmann's constant (8.617×10^{-5} eV/K), T is the absolute temperature of the polymeric material (in kelvin), and the units of D are cm^2/sec. Kitano et al. [43] found that $c_1 = 0.472$, and $E_a = 0.5$ eV.

The third equation is related to the moisture solubility coefficient, S, which depends on the temperature of the polymeric material:

$$S = c_2 \times 10^{-4} \exp\left(\frac{E_a}{kT}\right) \tag{4.13}$$

where c_2 is a constant (often set to 4.96×10^{-4}), E_a is the activation energy (often set to 0.40 eV), T is the temperature (in kelvin) of the polymeric material, and S is in moles/MPa cm^3 [43].

Petitioner Samsung Ex-1055, 0220

4.2.6.2 Non-Fickian Diffusion

Encapsulant materials such as epoxy molding compounds can exhibit non-Fickian moisture diffusion behavior. In non-Fickian diffusion (Figs. 4.19 and 4.20), moisture uptake may initially exhibit characteristics similar to Fickian diffusion (i.e., relatively rapid with constant diffusivity), but it can eventually slow down and exhibit variable diffusivity. In non-Fickian diffusion, it may take a significantly longer period of time (even up to several months) to reach saturation. In some cases of non-Fickian behaviors, two distinct stages of moisture sorption can be observed, commonly referred to as dual-stage sorption.

Many studies have explained and modeled non-Fickian diffusion behavior in polymeric materials [39–41,44,45]. One theory suggests [40] that non-Fickian behavior is caused by water molecules forming hydrogen bonds with hydrophilic polymer chains, while free (unbound) water molecules present in micro- and macro-voids produce Fickian diffusion behavior. Figure 4.20 shows the suggested effect of bound and unbound water molecules on moisture diffusion. Figure 4.21 illustrates the bound and unbound water molecules in epoxy molding compounds.

Another theory [44] suggests that the chemical sorption at the resin–filler interfaces in encapsulant systems is the dominant mechanism involved in

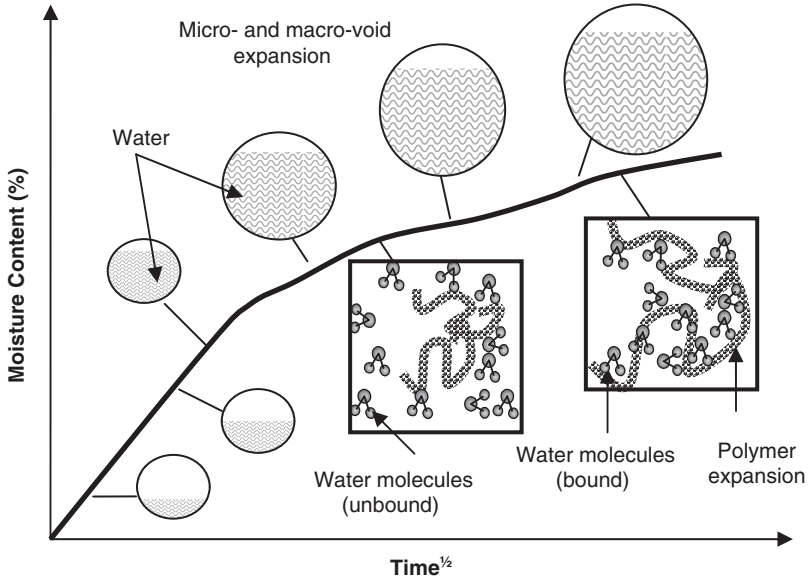


Figure 4.20 Effect of bound and unbound water molecules on moisture diffusion.

Petitioner Samsung Ex-1055, 0221

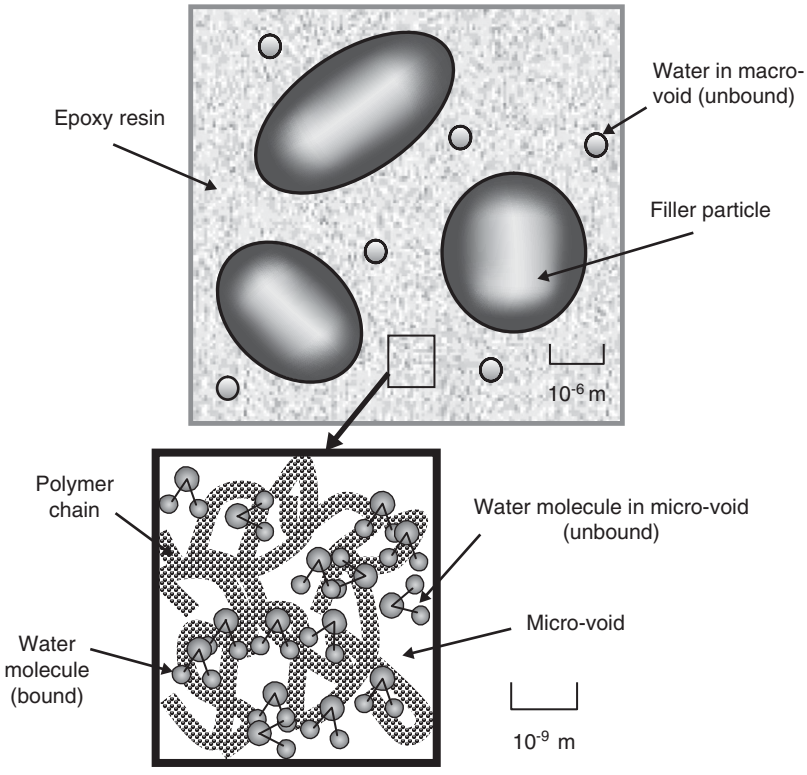


Figure 4.21 Water in molding compound materials present as free molecules in macro- and micro-voids, or bound to polymer chains.

non-Fickian diffusion. It is postulated that the moisture from the neighboring bulk resin can be depleted due to the resin–filler chemical sorption resulting in a secondary diffusion. Figure 4.22 depicts the non-Fickian diffusion due to resin–filler chemical sorption.

The model for non-Fickian sorption can be expressed as a non-linear diffusion equation

$$\frac{\partial C}{\partial t} = \frac{\partial}{\partial x}\left(D(C)\,\frac{\partial C}{\partial x} \right) \tag{4.14}$$

where D is the variable diffusivity dependent on the moisture concentration C [39]. The non-linear finite element analysis (FEA) optimization technique can be used to model non-Fickian moisture diffusivity as a continuous function of moisture concentration. An advantage of the FEA optimization technique is that it can be based on only a single moisture sorption experiment, saving significant time and cost compared to other techniques,

Petitioner Samsung Ex-1055, 0222

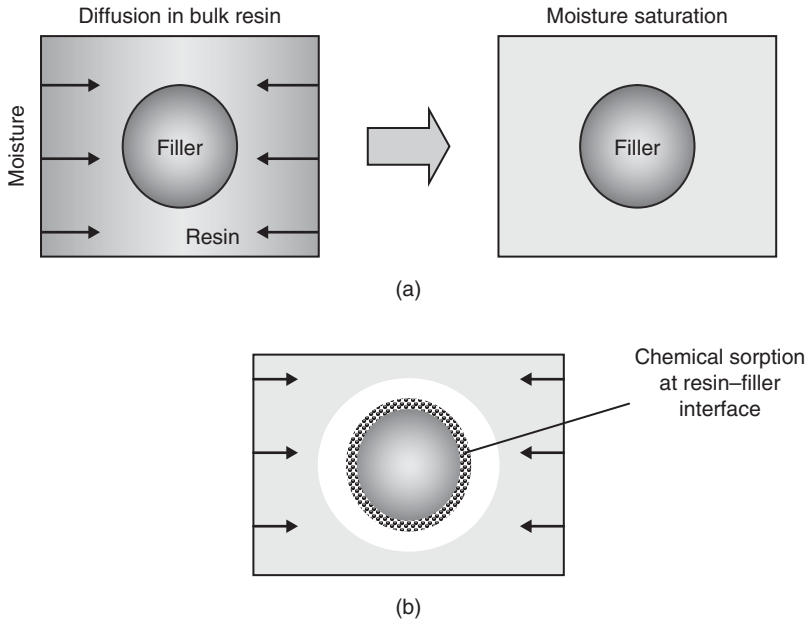


Figure 4.22 Mechanisms of (a) Fickian and (b) non-Fickian diffusion based on chemical sorption at the resin–filler interface [44].

such as the multiple sorption method, which require several sorption experiments [39].

4.2.7 Coefficient of Hygroscopic Expansion

As the moisture diffuses through the encapsulant material it may lead to volumetric expansion of the material, commonly referred to as hygroscopic swelling or expansion. The material property related to hygroscopic swelling characteristics of the encapsulant is known as the coefficient of hygroscopic expansion (CHE) or the coefficient of moisture expansion, analogous to the coefficient of thermal expansion. The CHE can be determined from

$$\varepsilon_h = \beta C \tag{4.15}$$

where ε_h is the hygroscopic strain, β is the CHE in mm^3/g (or mm^3/mg), and C is the moisture concentration in g/mm^3 (or mg/mm^3).

The hygroscopic strain and moisture concentration can be measured by the simultaneous application of thermomechanical analysis and thermogravimetric analysis to a moisturized specimen subjected to

Petitioner Samsung Ex-1055, 0223

desorption [40,45,46]. Thermomechanical analysis is used for measuring the linear deformation (shrinkage) of the moisturized specimen as the moisture escapes. Thermogravimetric analysis is used for measuring the moisture content loss.

The moisture concentration C can be calculated by dividing the moisture content by the total volume of the specimen, which is essentially an average concentration. Zhou et al. [47] considered the non-uniform distribution of moisture concentration in the specimen in the calculation of the CHE. The average and non-uniform CHEs are the same initially during the moisture desorption process. However, the CHE values differ as the moisture concentration becomes non-uniform. Swelling of the polymeric material can also be characterized as hygroscopic strain per moisture content (wt%).

A summary of the various techniques used for the measurement of hygroscopic swelling in polymeric materials is presented in Table 4.2. Swelling coefficients can vary with different materials. The swelling coefficients are also observed to increase with temperature [40,45,46].

The mechanism of hygroscopic swelling can be explained as follows. As water permeates through the polymeric material, some of the water molecules form hydrogen bonds to the polymer chains. This bonding can lead to unfolding or expansion of the polymer chains and, consequently, the encapsulant as a whole. Figure 4.23 depicts the expansion of the polymer chain due to water bonding. Non-Fickian moisture diffusion can be related to the hygroscopic swelling mechanism in polymeric materials. When the water molecules form hydrogen bonds with the polymer chains, the bound water molecules and the subsequent molecular expansion and deformation can lead to anomalous or non-Fickian diffusion behavior.

The concern regarding moisture expansion of encapsulant materials in electronic packages is the swelling mismatch between the encapsulant and other adjacent impermeable materials in the package that do not swell such as copper lead-frame, die-paddle, and silicon die. Stresses caused by hygroscopic swelling mismatches can be detrimental to the reliability of the package. It has been shown that the hygroscopic mismatch strains in encapsulant materials can be three times (or more) higher than thermal mismatch strains [40,46].

Hygroscopic stresses can be measured and calculated similarly to thermomechanical stress. Based on thermal–hygro analogy, hygroscopic stresses can be modeled using commercial finite element software. In place of temperature and thermal expansion coefficients, moisture concentration (C) and coefficient of hygroscopic expansion are, respectively, substituted.

Petitioner Samsung Ex-1055, 0224

Table 4.2 Studies of Swelling Measurement in Polymeric Materials

Test Materials	Measurement Technique	Swelling Coefficient or CHE	Reference Study
Epoxy–glass laminate on a copper sheet	Bending measurement using a microscope with a graduated eyepiece	0.31% linear strain per weight percent of water	Berry and Pritchet 1984 [48]
Epoxy resin (TGDDM)	Archimedean method (fluid body displacement)	0.3–0.6% volumetric swelling per % volume of water (~ 0.1–0.2% linear swelling per % volume of water)	El'Saad et al. 1990 [49]
Polyimide	Bending measurement using Michelson interferometry	0.024% max. linear out-of-plane strain per %RH (~ 0.6% per % moisture content) and 0.0039% max. linear in-plane strain per %RH (~ 0.1% per % moisture content)	Buchhold et al. 1998 [50]
Electronic packaging underfills	Thermomechanical analysis and thermogravimetric analysis	0.17–0.63 linear strain per moisture concentration (mm^3/mg)	Wong et al. 2000 [46]
Epoxy molding compounds	Thermomechanical analysis	0.3–0.6 (linear strain per weight percent of water) at 85°C	Ardebili et al. 2003 [40]
Epoxy molding compounds	Moiré interferometry	0.19–0.26 (strain per weight percent of water) at 85°C	Stellrecht et al. 2004 [51]
Epoxy molding compound	Thermomechanical analysis and thermogravimetric analysis	129–168 strain per moisture concentration (mm^3/g) at 110–220°C	Shirangi et al. 2008 [45]

CHE: Coefficient of hygroscopic expansion; TGDDM: Tetraglycidyl-4,4′-diaminodiphenylmethane.

Petitioner Samsung Ex-1055, 0225

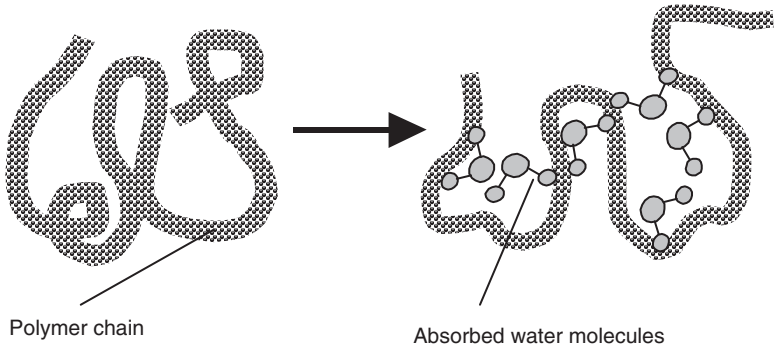


Figure 4.23 Moisture expansion mechanism of polymer chains.

Moisture concentration within the package can also be modeled with commercial finite element software using a thermal–moisture analogy. Moisture concentration discontinuity across bi-material interfaces can be overcome with the use of continuous field variables such as "partial pressure" [42] or "wetness" [52].

4.2.8 Gas Permeability

In addition to moisture, gasses such as hydrogen, oxygen, nitrogen, and carbon dioxide can permeate and diffuse into encapsulant materials. Corrosive gasses can be detrimental to the reliability of the encapsulated microelectronic package. The techniques for measuring permeability can be classified into two main types: weighed-cell and partition-cell methods [53]. Water vapor permeability, for example, can be determined by the weighed-cell method. In this method, the polymer membrane is used to seal a shallow vessel containing humidifying solution or desiccant, and the resulting cell is kept at a fixed temperature in either a desiccator or a humidity cabinet. The rate of transmission of water vapor is obtained by periodic weighing.

Permeability can also be measured using the partition-cell method. A dry film of a given polymer is inserted between two chambers that are then degassed completely. The diffusing vapor, adjusted to a desired pressure, is then introduced quickly into one of the chambers. The amount of vapor that permeates through the film is measured as a function of time. The apparatus is designed so that the vapor pressures in the two chambers are maintained at given values during a particular experiment. The amount of vapor that has passed through unit area of the film for a given time may

Petitioner Samsung Ex-1055, 0226

be plotted against time. The resulting curve is called the permeation curve [54]. The standardized ASTM D1434 [55] test also provides the technique for measuring gas permeability based on the differential pressure method.

Given the gas or vapor pressures p_1 and p_2 on the two sides of a sheet of thickness l and rate of transfer F, the permeability coefficient P can be determined through the following relationship:

$$F = \frac{P(p_1 - p_2)}{l} \tag{4.16}$$

Simple gases such as hydrogen, oxygen, nitrogen, and carbon dioxide undergo simple Fickian diffusion in polymers [56]. The molecular sizes of these gases are much smaller than the monomer unit of a given polymer, and the interaction between the two components is believed to be very weak. Therefore, the diffusing molecule can jump from one position to a neighboring one without the complications that would have occurred in case of a larger diffusing molecule bonding with the polymer chain [54].

4.2.9 Outgassing

Outgassing is the slow release of trapped gas from inside the plastic package. A source of trapped gases is the gases absorbed from the environment during packaging and assembly. Examples of commonly absorbed gases are nitrogen, oxygen, argon, carbon dioxide, hydrogen, methane, ammonia, and water vapor [57]. Another source of trapped gases is processing residuals and by-products of chemical reactions during material processing, packaging, and assembly that have remained trapped. Processing residuals may include isopropyl alcohol, acetone, trichloroethylene, and tetrahydrofuran.

Outgassing is a major concern particularly in vacuum environments such as in space. Space-related outgassing problems have been observed in the past. Gasses from outgassing can condense on optical lenses and sensors and reduce device functionality. Contaminant gasses from outgassing can also be hazardous to electronic devices leading to reliability problems such as corrosion. The ASTM standard test method ASTM E595-93 [58] specifies measurement and calculation techniques for outgassing of polymeric materials. There are two main outgassing parameters: total mass loss (TML) and collectable volatile condensable materials (CVCM). A third optional parameter, water vapor regained (WVR), may also be measured.

Petitioner Samsung Ex-1055, 0227

A critical portion of the outgassing measurement setup is shown in Fig. 4.24 [58]. The testing apparatus consist of two resistance-heated copper bars, specimen chambers, and a collector chamber. The copper heater bar is generally 650 mm in length with a 25 mm^2 cross-section. The collector chamber is comprised of a removable chromium-plated collector plate maintained at a fixed temperature of 25°C.

Prior to the outgassing measurement, the specimen is preconditioned at 50% RH and 23°C for 24 hours, and weighed. The specimen is weighed with the aluminum boat (container). Before testing, the collector plate is also weighed. The plastic specimen is then subjected to 125°C at a pressure less than 7×10^{-3} Pa (5×10^{-5} torr) for 24 hours. The vapor due to outgassing passes from the specimen through the open section of the specimen chamber into the collector plate. The specimen (in the aluminum boat) and collector plate are then removed, put in desiccators, cooled to room temperature, and then weighed. This test procedure will produce TML and CVCM measurements. For the optional WVR measurement, the

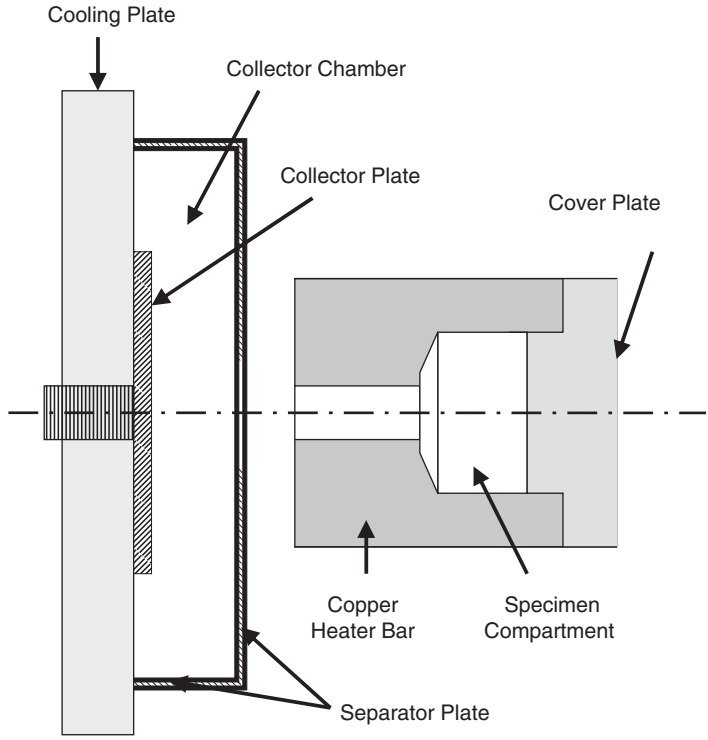


Figure 4.24 Outgassing measurement setup [58].

Petitioner Samsung Ex-1055, 0228

specimens are returned to 50% RH at 23°C for 24 hours, and then weighed after conditioning.

TML is calculated as:

$$\% \; TML = (L/S_I) \times 100 \tag{4.17}$$

where S_I is the initial specimen mass and L is the specimen loss mass (g) (difference between the final specimen mass S_F and S_I). The specimen is generally weighed with the aluminum boat, thus, the initial and final specimen mass measurements include the weight of the boat B_I. To calculate the specimen weights, the weight of the boat measured initially, B_I, must be excluded from the specimen/boat measurements.

CVCM is given by:

$$\% \; CVCM = (C/S_I) \times 100 \tag{4.18}$$

where C is the mass of the condensables (g) (difference between the final mass of the collector plate C_F and the initial mass of the collector plate C_I).

The third optional outgassing parameter, WVR is expressed as

$$\% \; CVCM = (S_F' - S_F)/S_I \times 100 \tag{4.19}$$

where S_F' is the mass of the specimen after reconditioning (at 50% RH and 24 hours).

4.3 Electrical Properties

The electrical properties of the molding compound must be controlled for superior performance. The electrical properties include dielectric constant and dissipation factor (ASTM D150), volume resistivity [59], and dielectric strength [60].

Dielectric constant ε (also known as relative permittivity) is given by

$$\varepsilon = C_S/C_v \tag{4.20}$$

where C_s is the capacitance of a capacitor with the encapsulant material specimen as the dielectric and C_v is the capacitance with vacuum as the dielectric. For materials that are to be used to insulate electrical components the dielectric constant should be low.

Dissipation factor is the ratio of the power dissipated to the power applied in the test specimen. It is also related to loss angle δ and phase angle θ as follows

Petitioner Samsung Ex-1055, 0229

$$D = \tan \delta = \cot \theta = 1/(2\pi f R_p C_p) \tag{4.21}$$

where f is the frequency, R_p is the equivalent parallel resistance, and C_p is the equivalent parallel capacitance.

Volume resistivity is the resistance of the plastic encapsulant to the leakage current through the body (volume) of the material. The higher the volume resistivity, the lower the leakage current and the less conductive the material is. ASTM D257 [59] suggests various electrode systems to determine the volume resistivity by measuring the resistance of the material specimen and by a measurement of the voltage or current drop under specified conditions and the specimen and electrode dimensions. The test specimen may be in the form of flat plates, tapes, or tubes. Figure 4.25 shows the application and electrode arrangement for a flat plate specimen. The circular geometry shown in the figure is not necessary, although convenient. The actual points of measurements should be uniformly distributed over the area covered by the measuring electrodes.

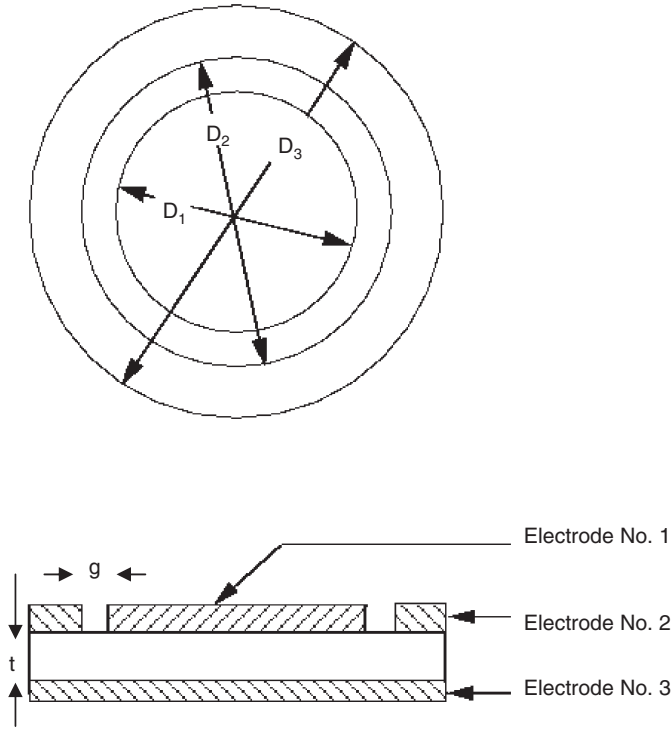


Figure 4.25 Electrode arrangement for measurement of volume resistivity of a flat specimen [59].

Petitioner Samsung Ex-1055, 0230

The dimensions of the electrodes, the width of the electrode gap, and the resistance are measured with a suitable device having the required sensitivity and accuracy. The time of electrification is normally 60 seconds and the applied voltage is 500 ± 5 V. The volume resistivity is given by

$$\rho_v = \frac{A_{elec}}{t} R_v \tag{4.22}$$

where A_{elec} is the effective area of the measuring electrode, R_v is the measured volume resistance, and t is the average thickness of the specimen.

The dielectric strength of the encapsulant material is defined as the maximum voltage required for a dielectric breakdown through the material. The higher the dielectric strength of a material the better is its quality as an insulator. ASTM D149 [60] requires that alternating voltage at a commercial power frequency, normally 60 Hz, be applied to a test specimen. The voltage is increased from zero, or from a level well below the breakdown voltage, until dielectric failure of the test specimen occurs. Dielectric strength is expressed as volts per unit thickness. The test voltage is applied using simple test electrodes on opposite faces of the specimens. The specimens may be molded, cast, or cut from a flat sheet or plate. Methods of applying voltage include a short-time test, a step-by-step test, and a slow rate-of-rise test. The second and third methods usually give conservative results.

Epoxy composites in dry environments and at room temperatures have similar electrical properties. The deterioration of some materials may occur after being stored in a moist environment at high temperatures.

4.4 Chemical Properties

Chemical properties of the encapsulant material are those properties that are either related to reactive chemical elements (i.e., ions) or they involve chemical reactions (i.e., flammability). Chemical properties include ionic impurity, ion diffusion, and flammability.

4.4.1 Ionic Impurity (Contamination Level)

The contamination level of the plastic encapsulant affects the long-term reliability of the encapsulated electronic package. The SEMI G29 standard procedure is used to determine water-soluble ionic levels in epoxy molding compounds. A water extract is first tested for electrical conductivity and then quantitatively analyzed by column chromatography. Separate determination

Petitioner Samsung Ex-1055, 0231

of hydrolyzable halides (from the resin, flame retardants, and other impure additives) is particularly crucial in assuring long-term reliability of plastic-encapsulated microelectronics. Long term (48 hours), high pressure, and sometimes hot water (up to 100°C) extraction from the molding compound and subsequent elemental analysis is needed for such evaluation. Modern molding compound formulations contain as low as 10 ppm of the corrosion-inducing ionics. Atomic absorption spectroscopy and X-ray fluorescence techniques are used to determine the content of other undesirable contaminants such as sodium, potassium, tin, and iron. Encapsulants used for memory devices, where single-event upsets from alpha-emitting impurities in the filler silica must be minimized, require determination of uranium and thorium content in the molding compound.

4.4.2 Ion Diffusion Coefficient

Encapsulant molding compounds contain ionic contaminants including chloride ions from epichlorohydrin used in the epoxidation of the resin and bromine ions incorporated into the resin as a flame retardant [61]. Chloride ions are known to break down the protective oxide on the surface of aluminum metallization and accelerate corrosion. When the absorbed moisture is combined with ions, there is an opportunity for electrolytic corrosion to occur on the metal surfaces of the device and package elements. However, the rate of corrosion in an encapsulated microcircuit may depend upon the rate of ion transport through the encapsulant.

Previous studies have suggested [61] that ion diffusion rates vary with molding compound formulation, the solution pH, and the ion concentration. The presence of ion-getters in molding compounds can hinder the diffusion of ions by bonding with them and trapping the ions in the bulk encapsulant [62]. The scanning electron microscope-energy dispersive X-ray analysis and the time-of-flight-secondary ion mass spectrometry analysis indicate that the mode of diffusion of ions in the encapsulants is primarily through the polymer resin matrix as opposed to diffusion at the interface of the resin and the filler particles. The calculated diffusion coefficients were slower than the literature values for moisture diffusion or the diffusion of gases. In fact, under basic conditions, the ions tend to diffuse through the molding compound almost as a front, suggesting that the ions bind to the encapsulant and that the diffusion of ions in molding compounds can be modeled using a Type II non-Fickian model [61].

Petitioner Samsung Ex-1055, 0232

4.4.3 Flammability and Oxygen Index

Encapsulation compounds and plastic-encapsulated parts must conform to Underwriters Laboratory flammability ratings (UL 94 V-0, UL 94 V-1, or UL 94 V-2). Molding compounds are evaluated for flammability by UL 94 vertical burning (http://www.ul.com/plastics/flame.html) and ASTM D2863 [63] oxygen index tests. Table 4.3 lists the test summaries of the three UL 94 vertical burning tests. In the UL 94 test a 127 mm × 12.7 mm (5 in. × 0.5 in.) cured epoxy test bar of a predetermined thickness is ignited multiple times in a gas flame and the burning time per ignition, total burning time for ten ignitions (five specimens), and the extent of burning are recorded for proper UL rating (Fig. 4.26).

In the ASTM D2863 [63] oxygen index test, a 0.6 cm × 0.3 cm × 8 cm bar of epoxy molding compound is positioned vertically in a transparent test tube as shown in Fig. 4.27. A mixture of oxygen and nitrogen is forced into the tube. The specimen is then ignited and the minimum volume fraction of oxygen in the oxygen–nitrogen mixture that will sustain burning of the molded bar is specified.

4.5 Summary

This chapter presented the characterization techniques used for determining the encapsulant properties. The properties of encapsulant materials

Table 4.3 UL Vertical Flammability Test Summaries

UL 94 Test	Test Summaries
V-0	• Burning (flaming combustion) must stop within 10 sec, and glowing combustion within 30 sec, after the removal of the test flame. • No flaming drips are allowed that will ignite the cotton.
V-1	• Burning (flaming combustion) must stop within 30 sec, and glowing combustion within 60 sec, after the removal of the test flame. • No flaming drips are allowed that will ignite the cotton.
V-2	• Burning (flaming combustion) must stop within 30 sec, and glowing combustion within 60 sec, after removal of the test flame. • Flaming drips are allowed.

Source: Boedeker Plastics (http://www.boedeker.com/bpi-ul94.htm); Plastics Web (http://www.ides.com/property_descriptions/UL94.asp).

Petitioner Samsung Ex-1055, 0233

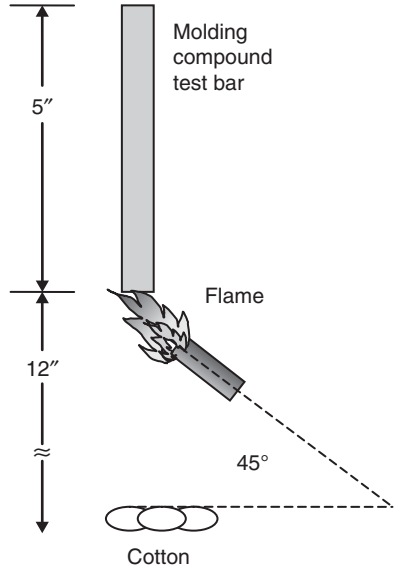


Figure 4.26 UL vertical flammability test (http://www.ides.com/property_descriptions/UL94.asp; http://www.ul.com/plastics/flame.html).

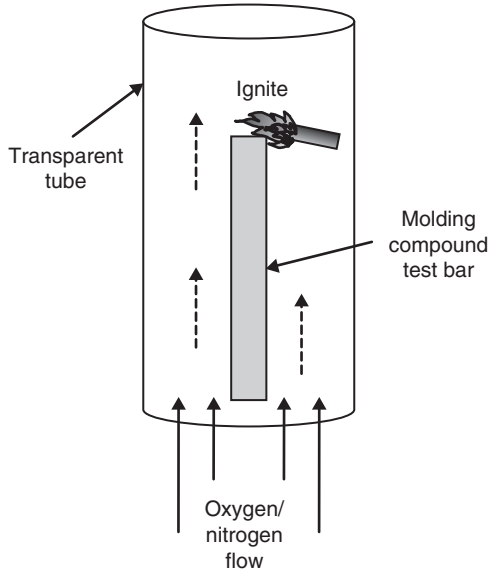


Figure 4.27 Testing apparatus for the ASTM D2863 oxygen index test (ASTM D2863; http://www.ides.com/property_descriptions/ASTMD2863.asp) [63].

Petitioner Samsung Ex-1055, 0234

are critical in determining the suitability of the materials for specific encapsulation techniques, packaging designs, manufacturing processes, and electronics applications.

Encapsulant properties can be classified into four groups: manufacturing, hygro-thermomechanical, electrical, and chemical properties. Manufacturing properties include spiral flow length, gelation time, bleed and flash, rheological compatibility, polymerization rate, curing time and temperature, hot hardness, and post-cure time and temperature. Hygro-thermomechanical properties consist of coefficient of thermal expansion, glass transition temperature, thermal conductivity, flexural strength and modulus, tensile strength, elastic and shear modulus, elongation, adhesion strength, moisture absorption, diffusion coefficient, coefficient of moisture expansion, gas permeability, and outgassing. Electrical properties include dielectric constant, dissipation factor, volume resistivity, and dielectric strength. Finally, chemical properties include ionic impurity, ion diffusion coefficient, and flammability. Encapsulant properties are used to evaluate the suitability of the material for specific electronics applications and manufacturing processes.

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Petitioner Samsung Ex-1055, 0239

5 Encapsulation Defects and Failures

Defects are undesirable and unintended features in the package that are created during the manufacturing and assembly processes. If a package exhibits features that do not conform to the product specifications, it is said to be defective. Defects can occur in an encapsulated microelectronic package at any stage in manufacturing and assembly including die passivation, lead-frame fabrication, chip adhesion, wire bonding, encapsulation, and lead forming. Defects can be reduced or eliminated by careful control of the processing parameters, optimal package design, and material selection. In some cases, defective parts can be screened out.

Failure occurs when a mechanical, thermal, chemical, or electrical process causes unacceptable product performance. A product that exhibits performance parameters and characteristics outside the acceptable specified range is said to have failed. Presence of defects can initiate or accelerate the failure mechanisms in the package and lead to earlier and unexpected failures. Failures can be predicted using failure mechanism models and can be designed against by careful selection of material and package parameters. Accelerated tests are conducted on packages to qualify them and identify those prone to early failures.

This chapter gives an overview of defects and failures that are possible in a plastic-encapsulated package and then discusses defect and failure types associated with the encapsulation, the contributing factors, and predictive models. Finally, the loads and stresses that accelerate failures in a package are presented. The defect and failure analysis techniques and screening and accelerated tests will be discussed in Chapters 6 and 7.

5.1 Overview of Package Defects and Failures

Plastic-encapsulated microelectronic devices or assemblies are susceptible to various types of defects and failures. An outline of these defects and failure types, and their contributing factors are discussed in this section.

5.1.1 Package Defects

An illustration of defect sites and types in a plastic-encapsulated microelectronic package is shown in Fig. 5.1. Table 5.1 outlines the defect sites, types, and potential sources.

Petitioner Samsung Ex-1055, 0240

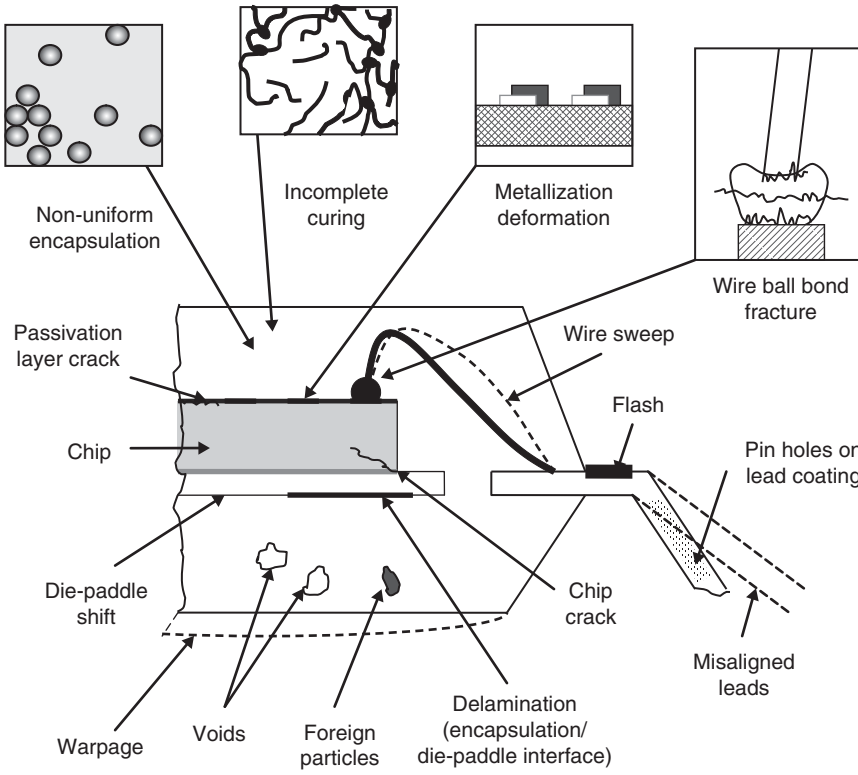


Figure 5.1 Defect sites and types in a plastic-encapsulated device.

5.1.2 Package Failures

Failures can occur at any location in the package, referred to as failure sites, and can be caused by different types of mechanisms, known as failure mechanisms. Common failure sites for the various failure mechanisms in plastic-encapsulated microelectronic packages are schematically illustrated in Fig. 5.2. Typical failure mechanisms, corresponding sites in plastic packages, and failure modes are summarized in Table 5.2.

Interactions between various failure mechanisms can occur when different types of loads are applied. For example, a thermal load can trigger mechanical failure due to a thermal expansion mismatch between adjacent materials in a structure. Other interactions include stress-assisted corrosion, stress-corrosion cracking, field-induced metal migration, passivation and dielectric cracking, hygro-thermal-induced package cracking, and temperature-induced acceleration of chemical reactions. In such cases,

Petitioner Samsung Ex-1055, 0241

Table 5.1 Plastic Package Defects and Their Potential Sources in Manufacturing

Defect Site	Defect Type	Potential Source
Die	Fractured die	Non-uniform die-attach; improper setup of bonder; excessive force during bonding; dicing; wafer-level molding stresses; electrical overstress in test
	Corroded die	Passivation cracks, pin holes, and delamination; inappropriate storage conditions; contamination
	Deformed metallization	Residual stresses in the encapsulant due to inadequate post-curing; improper die size to plastic thickness ratio
Die passivation	Passivation pin holes and voids	Deposition parameters; viscosity-curing characteristics of spun-on passivation
	Delaminated passivation	Contamination on die
Wire	Wire sweep	Encapsulant viscosity; flow velocity; voids and fillers in the encapsulant; poor wire bond geometry; delayed packing profile
	Bond-pad cratering	Improper bonder setup; insufficient pad metal thickness; wrong pad metal underlayer
	Bond liftoff, shearing, and fracture	Improper wire bonding parameters; contamination
Lead-frame	Paddle shift	Encapsulant viscosity and flow velocity; poor lead-frame design
	Pin holes in lead and paddle coating	Deposition parameters; contamination; flash; storage
	Misaligned leads	Improper handling or forming
	Burrs on lead-frame	Improper etching; reversed blanking
	Cracked lead	Blanking parameters; defective metal sheet; improper trim
	Poor solder wetting of land or lead	Excessive solder temperature; contamination; flash
Package	Package non-planarity, warping, or bowing	Die shift; die size; die-attach void or delamination; high molding stress

(*Continued*)

Petitioner Samsung Ex-1055, 0242

Table 5.1 Plastic Package Defects and Their Potential Sources in Manufacturing (*Continued*)

Defect Site	Defect Type	Potential Source
Encapsulant	Foreign inclusion	Inadequate screening of encapsulant; improper molding process
	Encapsulant voids	Entrapping of air during raw material feeding; inadequate venting of the mold; high encapsulant viscosity; high moisture content in encapsulant
	Disbonded and delaminated regions with encapsulant	Contamination or entrapped void
	Package cracking (popcorning)	Voids in the plastic encapsulant; excessive absorbed moisture; handling procedure; insufficient bake before reflow or vapor
	Incomplete cure	Insufficient heating during post-cure; inaccurate ratio and insufficient mixing of two-part potting encapsulants
	Non-uniform encapsulation	Non-uniform thickness due to substrate tilt and squeegee pressure variation during printing encapsulation; material non-homogeneity due to aggregation of filler particles during encapsulant flow; inadequate mixing during potting
	Improper marking	High viscosity of the encapsulant and improper curing; surface contamination

the combined effect of the failure mechanisms is not necessarily the sum of the individual effects.

5.1.3 Classification of Failure Mechanisms

Failure mechanisms can be classified based on the rate of damage accumulation [1]. Figure 5.3 shows the classification of failure mechanisms.

Petitioner Samsung Ex-1055, 0243

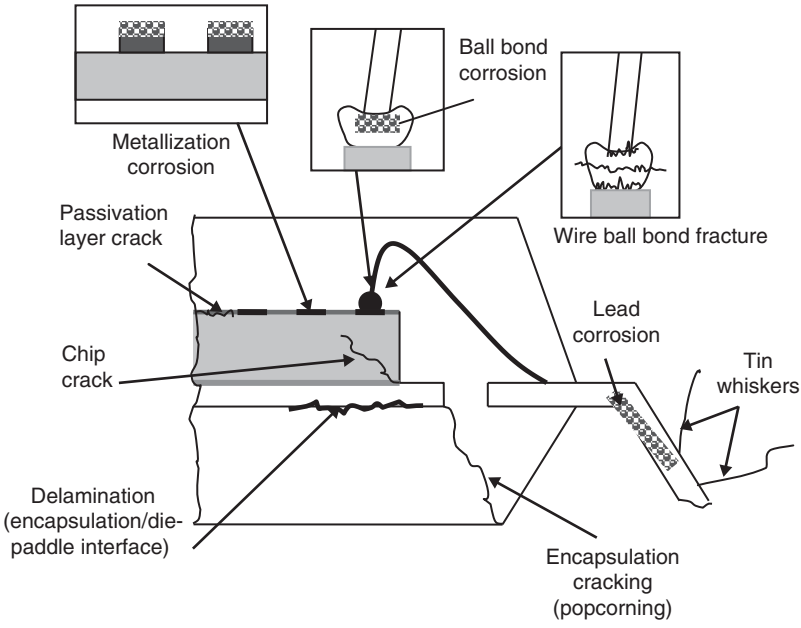


Figure 5.2 Failure sites and modes in plastic-encapsulated devices.

The classification is especially useful in reliability analysis studies, where time to failure is a critical parameter.

Failure mechanisms fall into two broad categories: overstress and wearout. Overstress failures are often instantaneous and catastrophic. Wearout failures occur due to the incremental accumulation of damage over time, often leading first to performance degradation and then to device failure. Further classification of failure mechanisms is based on the type of load that triggers the mechanism: mechanical, thermal, electrical, radiation, chemical, etc.

Mechanical loads include physical shock, vibration (e.g., under the hood of a car), loads exerted by filler particles on the silicon die (because of encapsulant shrinkage upon curing), and inertial forces (e.g., in the fuse of a cannon shell being fired). Structural and material responses to these loads may include elastic deformation, plastic deformation, buckling, brittle or ductile fracture, interfacial separation, fatigue crack initiation, fatigue crack propagation, creep, and creep rupture.

Thermal loads include high temperatures during die-attach curing, heating prior to wire bonding, encapsulation, post-mold curing, rework on neighboring components, dipping in molten solder, vapor-phase soldering, and reflow soldering. External thermal loads lead to changes in dimensions because of thermal expansion, and can change such physical properties as

Petitioner Samsung Ex-1055, 0244

Table 5.2 Failure Sites, Failure Modes, Failure Mechanisms, and Environmental Loads on a Plastic-Encapsulated Microelectronic Device

Failure Site	Failure Mode	Failure Mechanism	Environmental Load	Critical Interactions and Remarks
Die edge, corner or surface scratch due to machining, dicing, or handling	Spalling crack, vertical crack, horizontal crack, electrical open	Crack initiation, crack propagation	Temperature gradients and changes	Encapsulant shrinkage, modulus of elasticity of encapsulant, CTE mismatch among die, die-attach and encapsulant
Metallization traces, edges	Corrosion, increase in resistance, electrical short or open, notching, electrical parameter drift, metallization shift, intermittence, intermetallics	Electromigration, oxidation, electrochemical reaction, interdiffusion, thermal mismatch with encapsulant	Current density, humidity, voltage bias	Often passivation cracking precedes; residual stresses in the metallization
Stress concentration on the passivation from bearing of sharp edge of filler particle; die passivation defect	Transistor instability; corrosion of metallization, electrical open, shift in parametrics	Overstress, fracture, oxidation, electrochemical reaction	Cyclic temperature, temperature below glass transition temperature, humidity	Encapsulant shrinkage, sharp edges of filler, mismatch in CTE of chip, passivation and encapsulant

Petitioner Samsung Ex-1055, 0245

Die-attach void, crack, contamination site	Delamination of die, non-uniform transfer of stresses to die pad from the die; eventual loss of electrical function	Crack initiation and propagation	Cyclic temperature	Moisture in die attach; viscosity of die attach thickness, CTE mismatch between die pad and die
Bonding wire	Breakage	Axial fatigue	Cyclic temperature	Filler particle bearing, mismatch in CTE of wire and encapsulant
Ball bond	Electrical open, increased junction resistance, shift in electrical parametrics; bond lift, cratering, intermittence	Shear fatigue, axial overstress, Kirkendall voiding, corrosion, diffusion and interdiffusion, intermetallics at the base of the bond, neck in the wire	Absolute temperature, humidity, contamination	Lack of interdiffusion barrier layer
Stitch-bond heel, base, neck	Electrical open, increased junction resistance, shift in electrical parametrics, bond lift, cratering, intermittence	Fatigue, Kirkendall voiding, corrosion, diffusion and interdiffusion	Absolute temperature, humidity, contamination	Lack of interdiffusion barrier layer
Bond pad	Substrate cracking, bond-pad lift-off, eventual loss of electrical function, shift in electrical parametrics, corrosion	Overstress, corrosion	Humidity, electrical bias	CTE mismatch between bond pad and substrate, lack of passivation layer

(*Continued*)

Petitioner Samsung Ex-1055, 0246

Table 5.2 Failure Sites, Failure Modes, Failure Mechanisms, and Environmental Loads on a Plastic-Encapsulated Microelectronic Device (*Continued*)

Failure Site	Failure Mode	Failure Mechanism	Environmental Load	Critical Interactions and Remarks
Die and encapsulant interface	Eventual electrical open	De-adhesion or delamination	Humidity, contamination, temperature cycling about glass transition temperature	Residual stresses, formation of moisture layer at the interface, loss of adhesion, CTE mismatch
Passivation and encapsulant interface	Corrosion of metallization shift in electrical parameters	De-adhesion or delamination	Humidity, contamination, temperature cycling about glass transition temperature of encapsulant	Lead design, residual stresses, loss of adhesion, CTE mismatch between encapsulant and lead, lead pitch
Bond wire and encapsulant interface	Corrosion of die bond pad, increase in junction resistance, electrical open	De-adhesion, shear fatigue	Humidity, contamination, temperature cycling about glass transition temperature of encapsulant	CTE mismatch between encapsulant and wire
Encapsulant	Eventual loss of electrical function, loss of mechanical integrity	Thermal fatigue cracking, depolymerization	Temperature cycling about glass transition temperature of encapsulant	Delamination of die pad and encapsulant, corner radius

Petitioner Samsung Ex-1055, 0247

Leads	Reduced solderability, increased electrical resistance	Dewetting	Contamination, solder temperature	Lead finish porosity
Tin plated leads	Electrical short	Tin whisker growth, interdiffusion, stress relief, recrystallization, grain growth	Humidity, corrosion, applied external stress (bending, scratches)	Residual stresses, CTE mismatch stresses, impurities, and grain orientation can contribute to tin-whisker growth
Die and encapsulant interface, encapsulant cracking at die corner and emerging either at the leads, base or top of the device	Popcorning; eventual loss of electrical function, electrical open	Vaporization of entrapped moisture, doping of the device bottom, dynamic fracture of the encapsulant	Temperature above the boiling point of entrapped moisture, rate of change of temperature due to solder-reflow processes	Adhesion strength of encapsulant and die-pad, entrapment of vaporized moisture

CTE: Coefficient of thermal expansion.

Petitioner Samsung Ex-1055, 0248

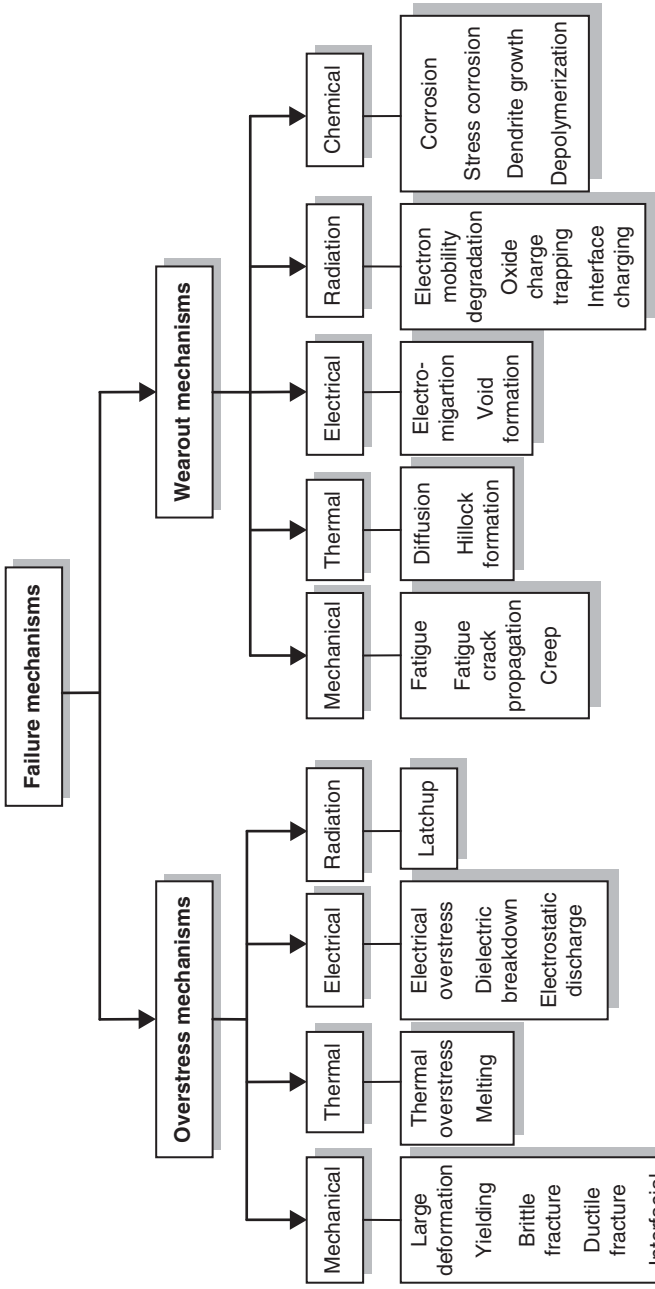


Figure 5.3 Classification of failure mechanisms [1].

Petitioner Samsung Ex-1055, 0249

the creep flow rate. Mismatches in coefficients of thermal expansion (CTEs) can often cause local stresses that can lead to failure of the package structure. Excessive thermal loads can also lead to burning of flammable materials in the package.

Electrical loads include, for instance, a sudden current surge through the package (e.g., in the ignition system of a car engine during start-up), fluctuation in the line current due to a defective power supply or a sudden jolt of transferred electricity (e.g., from improper grounding procedures), electrostatic discharge, electric overstress, applied voltage, and input current. These external loads may produce dielectric breakdown, surface breakdown of voltage, dissipation of electric power as heat energy, or electromigration. They may also increase electrolytic corrosion, current leakage due to formation of dendrites, and thermally induced degradation.

Chemical loads include chemically severe environments that result in corrosion, oxidation, and ionic surface dendritic growth. Moisture in a humid environment can be a major load on a plastic-encapsulated package because of the permeability of moisture through encapsulants.

Moisture absorbed by the plastic can leach catalyst residues and polymerization by-products from the encapsulant, then ingress to the die metallization bond pads, semiconductor, and various interfaces and activate failure mechanisms that degrade the package. For instance, reactive flux residues coating the package after assembly can migrate through the encapsulation to reach the die surface. Subtle changes in dielectric properties such as dielectric constant and dissipation factor from moisture absorption, ingress of ions, or variations with temperature are particularly critical in high frequency circuits. Reduction in breakdown voltage especially for high voltage transformers is also a concern for some plastics.

Depolymerization, also referred to as reversion, especially of some epoxy-polyamides and polyurethanes, can be caused by extended exposure to high temperature and humidity environments. Since reversion of encapsulants may take months or years, accelerated tests can be used to identify the encapsulants that are prone to this failure.

5.1.4 Contributing Factors

Factors that contribute to package defects and failures are typically associated with material composition and properties, package design, environmental conditions, and process parameters. Identification of the contributing factors is an important step in the process of elimination and prevention of package defects and failures. The contributing factors can be

Petitioner Samsung Ex-1055, 0250

identified through experimental and modeling analysis. Physics-based modeling and numerical parametric studies are preferred; however, for more complex defect and failure mechanisms, trial-and-error methods are used to identify the critical contributing factors. Trial-and-error methods are generally less efficient and more expensive due to the time consuming experiments and equipment modifications.

A method of representing the contributing factors is a cause and effect diagram generally referred to as a fish-bone diagram due to its unique shape (also known as Ishikawa diagram, named after its inventor). Fish-bone diagrams can be used to illustrate the complex cause and effect relationship between the contributing factors and package defects and failures. In a fish-bone diagram multiple causes can be identified and grouped into several categories. In manufacturing applications, the fish-bone categories were originally known as 6Ms—referring to machine, method, material, measurement, man (human factors), and mother nature (environmental factors). Some of these categorizes can be combined and modified for specific applications. A fish-bone diagram for package delamination is shown in Fig. 5.4 [2]. The categories consist of design, process, environment, and material.

5.2 Encapsulation Defects

Encapsulation defects are unintended features and characteristics of the package due to the encapsulation process. Defects due to encapsulation process can directly affect the quality of the encapsulant material. Examples of such defects include voids, incomplete curing, and non-uniform encapsulation. Furthermore, the encapsulation process can induce defects in non-encapsulant elements in the package such as wire sweep, die cracking, and flash. Interfaces in the package are also susceptible to the encapsulation process and can be subjected to delamination or de-adhesion.

5.2.1 Wire Sweep

Wire sweep is the displacement and deformation of wire loop during the encapsulant flow. Wire sweep can be measured as the maximum lateral wire displacement x or as a ratio of maximum displacement x to wire length (L), x/L, as depicted in Fig. 5.5 [3]. Wire sweep defects can cause two possible failures in the package. In high-density wire assemblies, wire sweep can lead to an actual contact with another wire and cause electrical

Petitioner Samsung Ex-1055, 0251

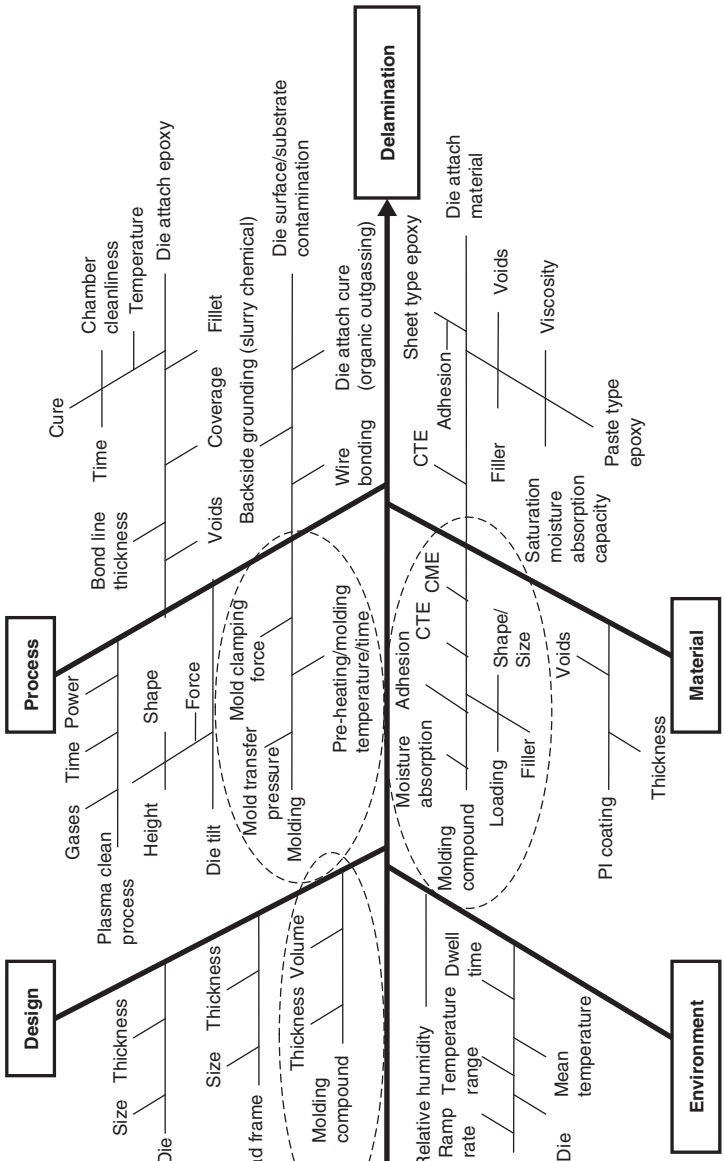


Figure 5.4 Cause and effect (fish-bone) diagram depicting the contributing factors to delamination in a typical plastic-encapsulated microelectronic package [2]. Dashed circles represent the encapsulation factors.

Petitioner Samsung Ex-1055, 0252

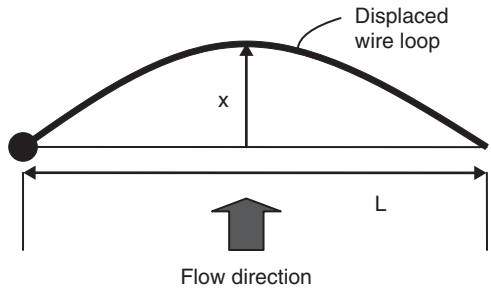


Figure 5.5 Definition of wire sweep.

shorting. Furthermore, the stresses on ultra-thin wires with wire sweep can cause breakage or weakening of the bond joint.

Factors contributing to wire sweep include package design, wire layout, wire material and dimensions, molding compound properties, wire bonding process, and encapsulation process. The wire parameters that affect wire sweep include wire diameter, wire length, and wire breaking load. The study by Onodera et al. [3] verifies that increase in wire length in the encapsulated package can lead to higher wire sweep rate. In the same study, the encapsulation method was shown to also play a role in the magnitude of the effect of wire length on wire sweep. Figure 5.6(a) shows the effect of wire diameter on the wire sweep ratio. Experiments by Terashima et al. [4] show that as the wire diameter increases, the wire sweep ratio decreases. Also, the larger the wire breaking load, the lower is the wire sweep ratio, as depicted in Fig. 5.6(b).

Wu et al. [5] investigated the effect of wire orientation angle, curing time, molding temperature, and gate position on wire sweep. A 3D model was used to simulate the molding compound flow around curved wire bonds. The model was based on the numerical method described by Tay et al. [6] with an additional effect of transient resin curing incorporated in the model.

Two gate positions were investigated in this study: left centered and bottom left corner. If the gate is left centered as shown in Fig. 5.7, maximum wire sweep occurs at a 90 degree orientation where the wire is normal to the main flow (wires #7 and #20). A shift in the position of the gate to the left lower corner changes the wire sweep profile such that the wire sweep increases in the lower and left positioned wires (#1 and #20), and reduces in the upper and right positioned wires (#7 and #13).

Wire density is another important factor in wire sweep. As the packages become thinner and smaller, the wire density increases leading to an

Petitioner Samsung Ex-1055, 0253

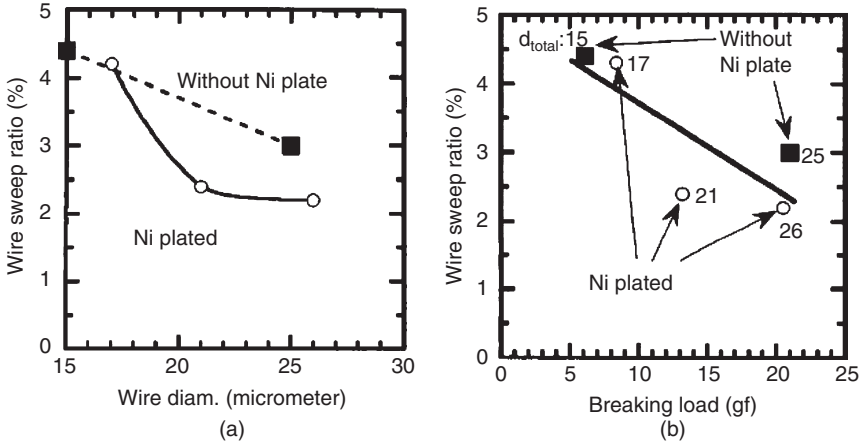


Figure 5.6 Relationship between wire sweep ratio and (a) wire diameter and (b) wire breaking load [4].

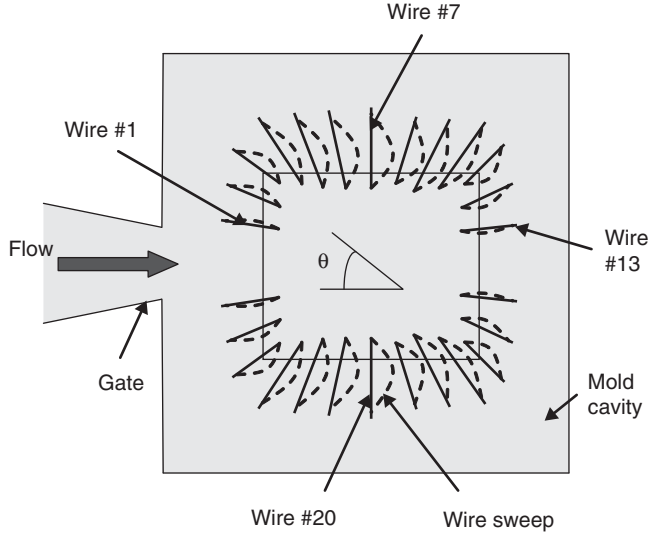


Figure 5.7 Extent of wire sweep based on the wire orientation angle [5].

increasing concern of the effect of wire density on wire sweep. Secondary parameters such as mold cavity thickness, wire diameter, and wire position from the centerline can influence the extent of the effect of wire density on wire sweep. Pei et al. [7] found that if the ratio of the mold cavity thickness to wire diameter (*H*/*D*) is small, the effect of wire density on wire sweep

Petitioner Samsung Ex-1055, 0254

is not significant. As the ratio *H*/*D* increases, the wire density effect becomes more prominent and should be included in the wire sweep prediction models. In this study the computational fluid dynamics (CFD) software FIDAP (fluids dynamics analysis package) was used to simulate the flow of molding compound and the effect of wire density. The model parameters consisted of the velocity of the flow between two parallel plates at distance *H*, and the diameter *D* and the spacing between two cylinders (representing two wires), and the position of the wire relative to the centerline *e*. Figure 5.8 shows the geometrical parameters used in the model.

3D stacked die packages with wire bonding interconnection are more susceptible to wire sweep due to multiple levels of wire bonding and higher wire density [2,8,9]. The wire bond height in die stack package can be higher for the upper stack compared to the lower stack wire. The wire loop profiles also may differ in die stack packages due to different stacking designs. Examples of different wire loop profiles for two different die packages are shown in Fig. 5.9. In a homogeneous die stack design, the chips have the same size and can be stacked using interposers. In a pyramid die stack design, also known as telescopic or "towers of Hanoi" design, the chip sizes decrease in the upper layer.

To reduce wire sweep in plastic-encapsulated devices, bond finger clearance and wire bond layout should be taken into consideration. In 3D die stack packages, placing the die with fewer wires at the bottom of the stack allows for greater bond finger pitch [9]. Excessive molding pressure can also contribute to wire sweep [2]. Modified designs of wire loop profiles have emerged to minimize wire sweep [8].

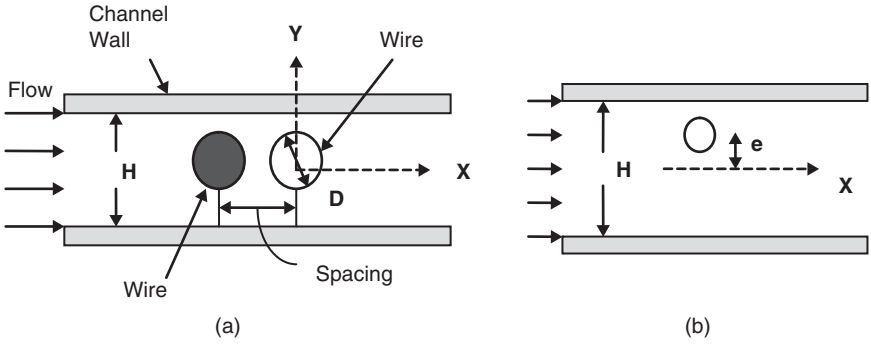


Figure 5.8 Parameters for modeling the effect of wire density on wire sweep: (a) wires on the centerline; (b) deviation from centerline [7].

Petitioner Samsung Ex-1055, 0255

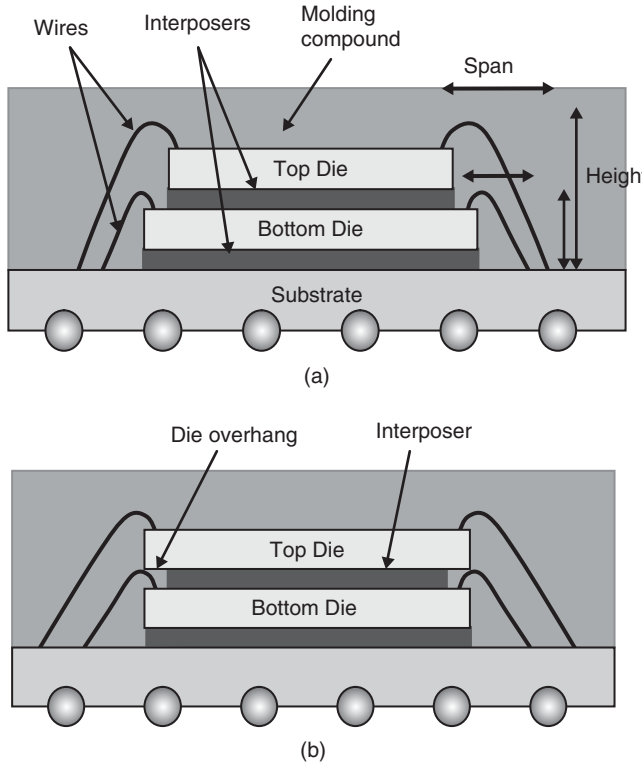


Figure 5.9 Wire profiles in various 3D die stack package designs: (a) pyramid design; (b) homogenous with overhanging die [8].

5.2.2 Paddle Shift

Paddle shift is the deformation and shifting of the die-paddle, the carrier that holds the die. Paddle shift is caused by unbalanced encapsulant flow in the upper and lower mold cavities. Figure 5.10 illustrates paddle shift due to encapsulation.

The factors contributing to paddle shift include encapsulant flow properties, lead-frame assembly design, and material properties of both encapsulant and lead-frame. Lead-frame packages such as thin small-outline packages (TSOPs) and thin quad flatpacks (TQFPs) are prone to paddle shift and lead deformation due to the thinner lead-frame assembly [10].

Several studies have investigated paddle shift and developed predictive models [10–15]. Mold filling is generally modeled using governing flow equations that consist of continuity, moment, and energy conservation

Petitioner Samsung Ex-1055, 0256

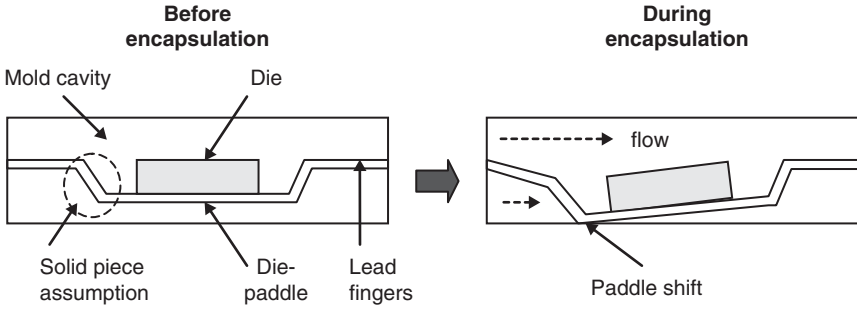


Figure 5.10 Paddle shift during encapsulation [13].

equations. The numerical simulation is performed using finite element software. To reduce simulation complexity, the lead-frame including die-paddle and lead fingers in some models are assumed to be one solid piece. In the study by Han and Wang [11], the openings in the lead-frame were considered and the encapsulant flow through the openings was modeled. In the study by Su et al. [12], 3D mold filling was simulated using FIDAP 3D CFD software. Pei and Hwang [13] used Moldex3D-RIM molding software for modeling mold filling.

5.2.3 Warpage

Warpage is the out-of-plane bending and deformation of the package. Warpage due to the encapsulation process can lead to reliability problems such as delamination and die cracking [16]. Warpage can also create manufacturing problems such as in plastic ball-grid arrays (PBGAs) where it can cause non-coplanarity of the solder balls during solder reflow leading to mounting problems during package assembly onto a printed circuit board [17]. The warpage modes observed in plastic-encapsulated packages include concave, convex, and combined modes as shown in Fig. 5.11 [18,19]. Examples of post-encapsulation concave warpage are shown in Fig. 5.12 [17,20].

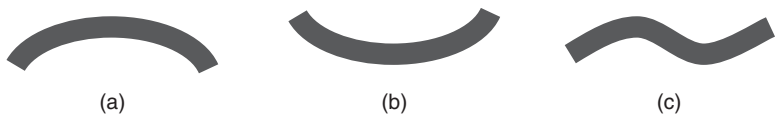


Figure 5.11 Warpage modes: (a) concave, (b) convex, and (c) combined.

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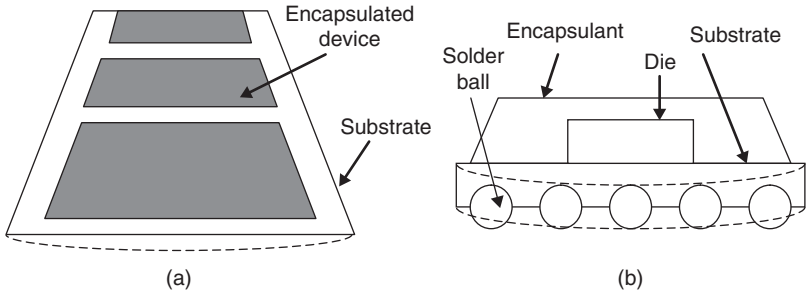


Figure 5.12 Concave mode warpage in (a) an array of encapsulated devices and (b) a single plastic ball-grid array.

Several studies have investigated and modeled warpage due to the encapsulation process. The initial models of warpage considered CTE mismatch stresses as the only source of warpage. Later studies showed evidence of other factors contributing to warpage. Kelly et al. [21] found that chemical shrinkage of the molding compound plays a significant role in the warpage of integrated circuit packages and is particularly important in packages where there are unequal thicknesses of molding compound above and below the die. Figure 5.13 shows temperature profile during molding and post-mold curing that lead to cooling shrinkage [20]. During the curing and post-curing, the encapsulant undergoes chemical shrinkage at high curing temperature, referred to as "hot chemical shrinkage" [22,23]. Figure 5.14 shows the volume shrinkage of encapsulant during curing and cooling stages. The chemical shrinkage that occurs during curing is reduced

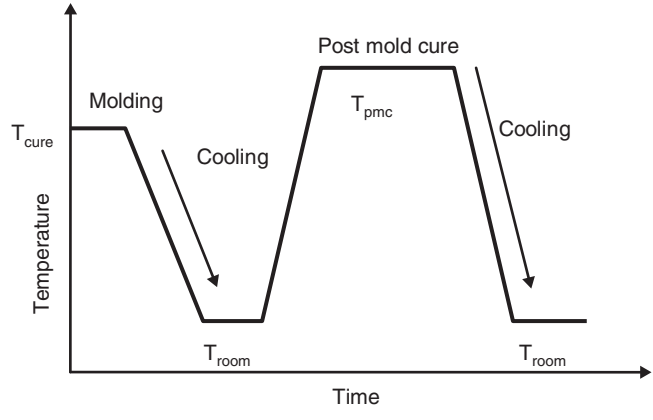


Figure 5.13 Temperature profile during molding and post-mold cure [20].

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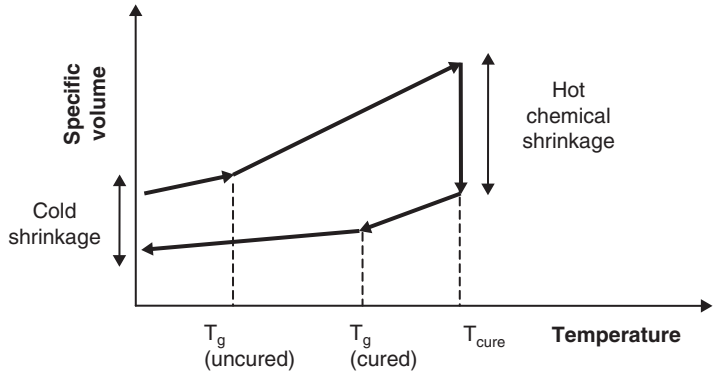


Figure 5.14 Encapsulant volume shrinkage due to curing and cooling [22].

when the encapsulant material is cooled to room temperature due to the increase in the glass transition temperature (T_g) of the cured material and subsequent effects of the CTEs above and below T_g.

More improved models of warpage have emerged that include both the effect of CTE mismatch and curing/compression shrinkage [20,22–26]. Chen et al. [25] modeled warpage as a function of pressure, volume, temperature, and degree of cure. In this study, the packing pressure and curing time were found to significantly increase warpage as compared to mold temperature and filling pressure.

The composition of the encapsulant also contributes to warpage. Okuno et al. [23] found that modification of the encapsulant material with special elastomer leads to lower warpage as depicted in Fig. 5.15. Yang et al. [20] found that warpage is reduced when the filler loading is increased in the encapsulant material.

Lin et al. [18] found the moisture in the molding compound preform to be another contributing factor to warpage. Statistical analysis of the warpage measurements including mode identifications (concave, convex, and combined) revealed a more severe warpage in samples exposed to 72 hours of clean room environment compared to samples with less or no exposure time (i.e., 0–24 hours) indicating an adverse effect of moisture on warpage.

Package geometry such as die thickness, encapsulant thickness, and die-paddle downset also can influence warpage. Die-paddle downset is the amount by which the die-paddle is recessed. For small packages the influence of downset is small, but it is very strong for large packages. For large

Petitioner Samsung Ex-1055, 0259

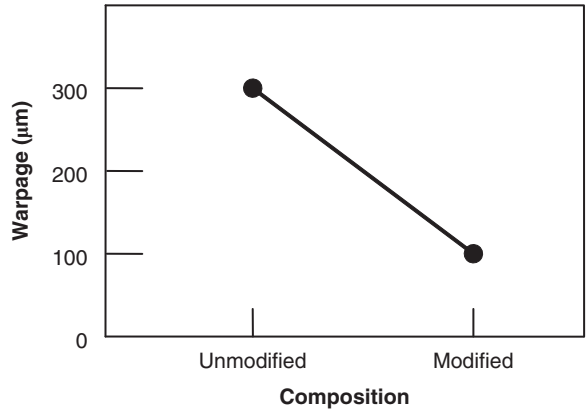


Figure 5.15 Effect of encapsulation composition on warpage [23].

packages 1 μm of downset results in 1 μm of warpage [21]. Increasing the die thickness has been shown to reduce warpage [23].

Package warpage can be minimized by careful selection of encapsulation material and composition, processing parameters, package geometry, and environmental exposure prior to encapsulation. Wafer-level encapsulation is especially susceptible to warpage since it involves the encapsulation of the entire wafer that is relatively thin and brittle. Warpage in wafer-level printing encapsulation can be reduced by using more flexible materials [16,23].

In some cases, warpage can be compensated by encapsulating the back side of the electronic assembly. For example in case of large ceramic circuit boards or multilayer boards where the external connections are at the sides, backside encapsulation can reduce warpage.

5.2.4 Die Cracking

The stresses due to the encapsulation process can cause die fracture. The encapsulation process generally can aggravate any existing microcrack in the die that was initiated during previous assembly steps. Examples of assembly steps that may cause die crack initiation are wafer or die thinning, backgrinding, and die-attach assembly steps [27,28]. A fractured die that has failed mechanically does not necessarily lead to electrical failure: The crack in the die may or may not cause instantaneous electrical failure of the device depending on the crack growth path. Even if the crack initiates from the back of the die, bifurcation and growth of the crack tip may

Petitioner Samsung Ex-1055, 0260

lead to transverse propagation. The crack can propagate through the entire die without traversing any sensitive structures.

The mechanical failure of the silicon die is often attributed to brittle fracture. The mechanics of brittle fracture is discussed further in Section 5.3.3. Wafer-level encapsulation is more prone to die cracking due to the thin and brittle silicon wafer. Processing parameters such as clamping pressure and mold transfer pressure during transfer molding process must be carefully controlled to prevent die cracking.

3D die stack packages are susceptible to die cracking due to the stacking design. The design factors contributing to die cracking in 3D die stack package include die stack configuration, substrate thickness, molding compound volume, and mold cap thickness [2].

5.2.5 Delamination

Delamination or de-adhesion is the separation of the encapsulant at the interface with an adjacent material. Delamination can occur at various sites in the encapsulated microelectronic package and can be classified according to the type of interface as depicted in Fig. 5.16.

Poor interfacial adhesion is a major contributing factor in delamination due to the encapsulation process. Poor adhesion can be caused by voids at the interface, surface contamination during encapsulation, and incomplete curing. Other contributing factors in delamination include shrinkage stresses [29] due to curing and cooling, and warpage. During cooling, the mismatch

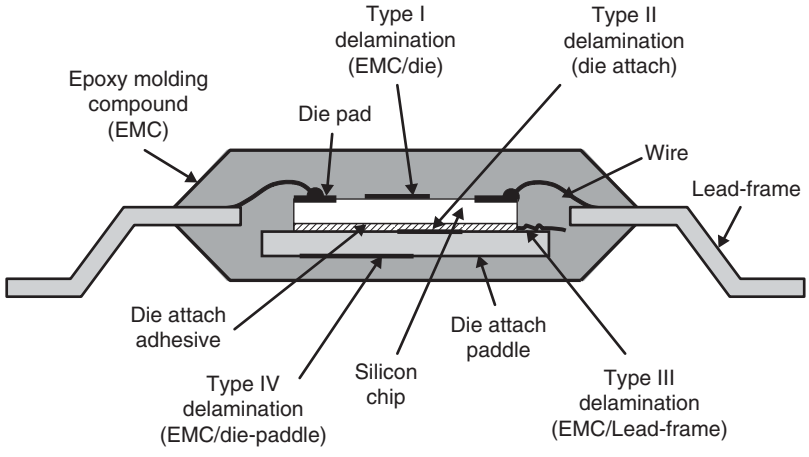


Figure 5.16 Delamination types [12].

Petitioner Samsung Ex-1055, 0261

between the CTEs of the encapsulant and the adjacent material can lead to thermo-mechanical stresses that can cause delamination.

The thermal strain, ε_{th}, due to the CTE mismatch at the interface between the encapsulant and adjacent material (Fig. 5.17) with CTEs of α_E and α_A, respectively, subjected to temperature change (ΔT) can be determined by

$$\varepsilon_{th} = (\alpha_E - \alpha_A)\Delta T \tag{5.1}$$

Delamination can occur either during the encapsulation process, during post-encapsulation manufacturing steps, or when the device is in operation. Temperature change during the encapsulation process is from curing temperature to room temperature. Further discussion of the delamination mechanism is provided in Section 5.3.

5.2.6 Voids

Voids are caused by air pockets trapped inside the epoxy material during the encapsulation process. Voids can occur during any type of encapsulation process including transfer molding, underfilling, glob-topping, potting, and printing while the encapsulant is exposed to air. However, voids can be reduced by minimizing air exposure such as venting the air away or using vacuum.

An example of void defect that can occur during printing encapsulation is shown in Fig. 5.18(a). Performing the printing encapsulation process under vacuum can eliminate the voids. Figure 5.18(b) shows the void-free encapsulation using vacuum printing encapsulation system (VPES). The vacuum pressures applied in VPES reported in several studies were in the range of about 1–300 torr (or 0.1–40 kPa). One atmospheric pressure is about 101 kPa or 760 torr.

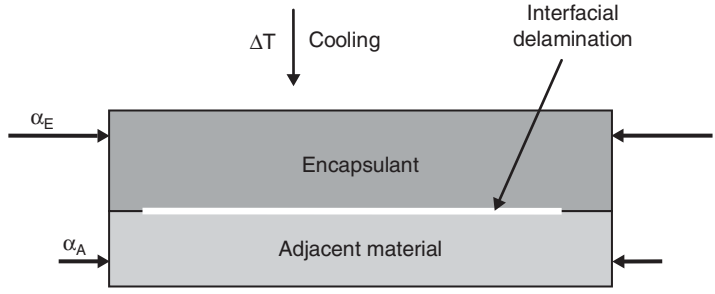


Figure 5.17 CTE mismatch strains and stresses at the interface between the encapsulant and adjacent material contributing to delamination.

Petitioner Samsung Ex-1055, 0262

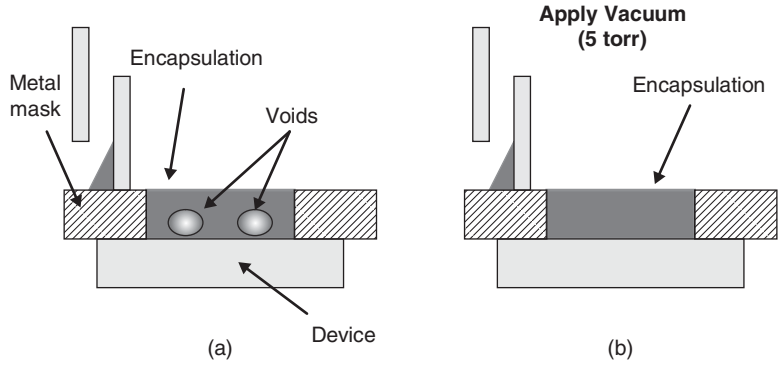


Figure 5.18 (a) Void defect and (b) void-free encapsulation in vacuum using a vacuum printing encapsulation system [23].

Kim et al. [30] compared two different encapsulation techniques, including underfilling and vacuum printing encapsulation of a system-in-package (SiP). The underfilling was conducted using capillary flow and the printing encapsulation was performed using VPES. Results revealed that the VPES process is superior to capillary underfilling of the SiP with respect to void formation. The voids were identified from images obtained by scanning acoustic transmit or tomography, also known as scanning acoustic microscopy (SAM). Defect and failure analysis techniques using SAM will be discussed in a later chapter.

In addition to using vacuum during encapsulation, other methods to prevent voids involve optimizing the squeegee material to improve the rolling of the encapsulant and improving the encapsulant flow by reducing encapsulant viscosity [16].

Several studies have investigated void formation during encapsulation [31–33]. Chang et al. [33] investigated void formation during transfer molding encapsulation of a TSOP using two sets of models, namely, true 3D model and Hele-Shaw approximation model. The true 3D model is based on continuity, momentum and energy conservation equations. In this model, a volume fractional function was used to track the advancement of the flow interface position.

The Hele-Shaw model is an approximation of the true 3D model based on the following assumptions: (a) for thin cavities, the velocity gradients in the gapwise direction are much larger than other velocity gradients; (b) the heat convection in the gapwise direction can be neglected; and (c) the heat conduction in the flow direction is negligible. Based on the mentioned assumptions, the Hele-Shaw approximation

Petitioner Samsung Ex-1055, 0263

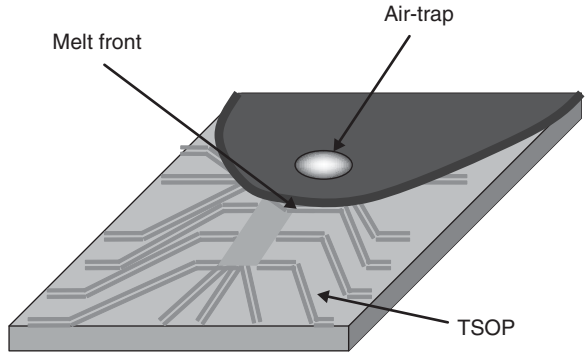


Figure 5.19 Air-trap formation during transfer molding of a thin small-outline package (TSOP) [33].

model for mold filling in thin cavity can be reduced to two simplified equations.

Both models, true 3D and Hele-Shaw, were numerically simulated using 3D finite-volume method [33]. The Hele-Shaw model simulation offered several advantages over the true 3D simulation including less computer memory (about 50 times less) and less simulation time (25 minutes as opposed to 7 hours for true 3D).

The results of mold filling simulations indicate that as the leading bottom melt front contacts the die, the flow is hindered [33]. A portion of the melt front moves upward and fills the top mold-half, through the large opening region, at the periphery around the die. The emerging melt front and the catching-up melt front enclose in the area in the top mold-half, and consequently, an air-trap defect is formed. Figure 5.19 shows the front melt and the location of air-trap observed experimentally and predicted numerically. If the trapped air escapes before the encapsulation hardens, the void will disappear, otherwise, it becomes a permanent defect. Escape paths (air vents) are designed to eliminate voids during encapsulation.

5.2.7 Non-uniform Encapsulation

Non-uniformity in the size or material composition of the encapsulation is considered a defect, if it is sufficient to cause warpage or delamination. Some encapsulation techniques such as transfer molding, compression molding, and potting are less prone to non-uniform thickness defect. Wafer-level printing encapsulation is particularly susceptible to non-uniform thickness because of the processing characteristics [16]. To ensure uniform encapsulation thickness the wafer carrier should be fixed with minimum

Petitioner Samsung Ex-1055, 0264

tilt for better squeegee positioning. Also a squeegee position control can be devised to ensure constant squeegee pressure and thus uniform encapsulation thickness.

Non-homogeneity or non-uniform material composition can occur when the filler particles are aggregated in certain areas and are not uniformly distributed in the encapsulant before hardening. Non-homogeneity can occur during potting encapsulation due to the inadequate mixing of the potting compound.

5.2.8 Flash

Flash is the molding compound that has passed through the mold parting line and is deposited onto the leads of the device during the transfer molding encapsulation process. Insufficient clamping pressure is a main contributor to flash. If the molding residue is not removed from the leads, it can lead to various problems such as insufficient bonding and adhesion in the next assembly steps. Resin bleed is the thinner form of flash. The method of removing flash and resin bleed from the leads referred to as deflashing was discussed previously in Section 3.8.2.

5.2.9 Foreign Particles

The presence of foreign particles in the encapsulant material is due to exposure to contaminated environment, equipment, or material during encapsulation process. Foreign particles can diffuse through the encapsulation and deposit onto metallic parts of the package such as the integrated circuit chip and wire bonds, and cause corrosion and other subsequent reliability problems in the package.

5.2.10 Incomplete Cure

Encapsulant properties such as glass transition temperature are affected by the extent of curing; thus, complete curing is necessary for full realization of the encapsulant properties.

Incomplete curing can be caused by insufficient curing time and low curing temperatures. In many encapsulation methods, curing during encapsulation is followed by post-curing to ensure complete curing of the encapsulant. Also, in two-part potting encapsulation, slight deviation from the mix ratios can lead to an incomplete cure, further emphasizing the importance of accurate measurements.

Petitioner Samsung Ex-1055, 0265

5.3 Encapsulation Failures

Encapsulant failure can occur during package assembly stage or during device operation. Particularly during the assembly of encapsulated microelectronic package onto the printed circuit board, the package is subjected to high solder reflow temperatures leading to either delamination at the encapsulant interface or fracture. The external loads and stresses that can cause delamination consist of vapor, moisture, temperature, and combined loads. Encapsulant fractures can be classified according to the failure mechanisms into vapor-induced cracking, brittle fracture, ductile fracture, and fatigue fracture.

5.3.1 Delamination

Delamination is the separation of the encapsulant from an adjacent material at the interface. Post-encapsulation delamination failures may occur during package assembly or during device operation. There are many factors that contribute to delamination, among which are the external loads such as vapor, moisture, and temperature.

An important type of delamination that can occur during the package assembly is commonly referred to as vapor-induced (or steam-induced) delamination because of the failure mechanism involving water vapor pressure at relatively high temperatures. During the assembly of the plastic-encapsulated package onto the printed circuit board, the assembly temperature is rapidly raised above the glass transition temperature of the molding compound (ranging from 110°C to 200°C) to a temperature of approximately 220°C or more, which is required to melt the solder. At the high reflow temperature, the pre-existing moisture inside the plastic encapsulant/metal interfaces voporizes into steam. The stresses due to the thermal mismatch between the molding compound and the adhering materials, the steam pressure, and hygroscopic swelling lead to interfacial de-adhesion or delamination. Sometimes, the vapor-induced delamination is followed by package cracking.

Several studies have investigated vapor-induced delamination mechanism during solder reflow process using experimental and theoretical methods. In the study by Pecht and Govind [34] in-situ deformation measurements were conducted on plastic packages preconditioned at dry and humid environments and exposed to solder reflow temperatures. The deformation measurements indicate that the water in the plastic package evaporated at the interface and caused delamination and popcorning.

Petitioner Samsung Ex-1055, 0266

The experimental results also suggest an initial stable and gradual crack propagation that is followed by a sudden catastrophic fracture. Tay and Lin [35] investigated the role of hygroscopic swelling in vapor-induced delamination and found that it had only slight influence on the delamination mechanism.

Several models have been developed to predict and evaluate the effect of various load, material, and geometrical factors on vapor-induced delamination [36–38]. The models developed by Tay et al. [37] and Guojun and Tay [38], calculate the strain energy release rate during delamination as a function of stress intensity factors and material constants. The vapor-induced delamination model proposed by Guojun and Tay [38] incorporates the governing equations for heat transfer, moisture diffusion, solubility, vapor pressure, and thermal and hygroscopic strains. The crack propagation at the interface that leads to the separation of the two materials, as depicted in Fig. 5.20, is modeled using fracture mechanics equations [39,40]. In this study, a modified crack surface displacement extrapolation method was used for evaluating the crack tip stress intensity factor, K.

The effect of various loads on delamination can be determined by calculating the rate of strain energy release, G. The equation for determining total G is given by

$$G_{Total} = \frac{(K_{I,t} + K_{I,h} + K_{I,p})^2 + (K_{II,t} + K_{II,h} + K_{II,p})^2}{\cosh^2(\pi\varepsilon)E^*} \tag{5.2}$$

where subscripts I and II refer to opening and sliding cracking modes, respectively, and subscripts t, h, and p refer to thermal, hygroscopic, and vapor pressure factors, respectively. The material constants ε and E^* are dependent on shear modulus, Young's modulus, and Poisson's ratio of the

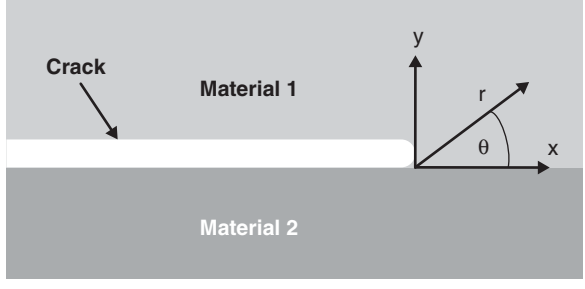


Figure 5.20 Crack propagation at the interface leading to delamination [38].

Petitioner Samsung Ex-1055, 0267

two materials. The strain energy release rates due to temperature, hygroscopic swelling, and vapor pressure—G_t, G_h, and G_p, respectively—can be determined using Equation 5.2, including only the respective load factors. Modeling results show that G_t is the most dominant component and G_h is negligible during the solder reflow process. G_p is also negligible for small crack lengths (below 0.5 mm), but can become significant for larger crack lengths.

As the electronic industry transitions to "green" or environmental friendly materials such as lead-free solders, the potential failures during lead-free solder reflow has been the focus of many studies [38,41–43]. A common concern is the generally higher reflow temperature of lead-free solders compared to that of conventional lead-based solders. In the same study by Guojun and Tay [38], it has been shown that G_t and G_p during lead-free solder reflow is much higher than those during eutectic tin-lead solder reflow process, indicating a more severe delamination problem associated with lead-free solders.

Lam et al. [36] proposed a criteria for delamination based on the number of moles of steam evaporated into the void during solder reflow process normalized with respect to the crack area, denoted by N_s, and the critical value for delamination, N_c. When N_s exceeds N_c,

$$N_s \geq N_c \tag{5.3}$$

delamination occurs. It was found that temperature distribution and defect size significantly influence the value of N_c and the onset of delamination.

Li et al. [44] found that void growth under combined vapor pressure and thermal stress can lead to void coalescence and delamination. A representative material cell containing a single microvoid, shown in Fig. 5.21, was used to model void growth. The thick shell has external and internal radii—R_1 and R_2, respectively—and is subjected to thermal stress, σ^T, on the external surface and vapor pressure, p, on its internal surface. The governing equations for modeling radially symmetric deformation include equilibrium equation, strain-energy function, constitutive equation, and the boundary condition. Theory of cavity formation and unstable void growth in incompressible hyper-elastic encapsulant material was used to relate the applied stress to void growth. The results indicated that the critical stress for unstable void growth is highly influenced by the change in temperature.

Other factors that may have influence on encapsulant delamination include moisture-induced degradation of the interfacial adhesion and hygroscopic swelling of the encapsulant material. The strain and stress due

Petitioner Samsung Ex-1055, 0268

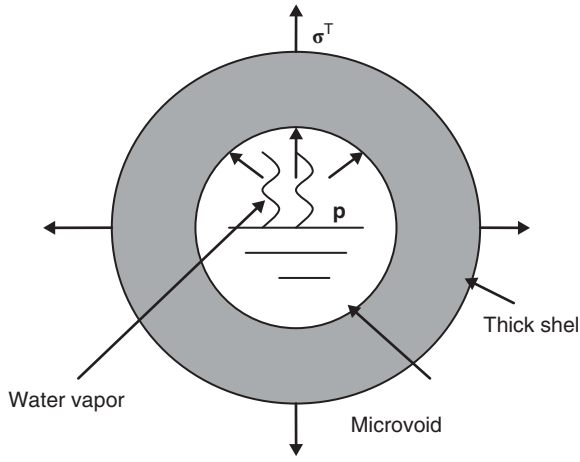


Figure 5.21 Mechanical model for investigating void deformation and growth.

to the coefficient of hygroscopic expansion (CHE) mismatch between the encapsulant and adjacent materials can contribute to the delamination. The CHE, also known as the coefficient of moisture expansion (CME), of various encapsulant materials have been measured in several studies [45–48]. Poor interfacial adhesion due to pre-existing void defects and contaminated surfaces during the assembly process can further accelerate the moisture-induced delamination failure mechanism.

The mechanism of delamination can also be described based on the amount of work required for de-adhesion and deformation at the interface of adhering materials. The work required to induce delamination, or separate the interfaces, includes the work necessary for de-adhesion as well as the work required to deform, elastically or inelastically, the separating bulk phases for crack extension. The total fracture energy, G, can be written as

$$G = W_a + W_p \tag{5.4}$$

where W_a is the reversible work of adhesion and W_p is the irreversible work of deformation in the two phases. W_a is defined as

$$W_a = \gamma_1 + \gamma_2 + \gamma_{12} \tag{5.5}$$

where γ_1 and γ_2 indicate the intra-molecular attractive forces known as surface tension in materials 1 and 2, respectively, and the γ_{12} refers to the interfacial tension between them as depicted in Fig. 5.22. Thus, the total adhesive strength of a joint depends not only on its interfacial properties, but also on the mechanical properties of the bulk phases [49].

Petitioner Samsung Ex-1055, 0269

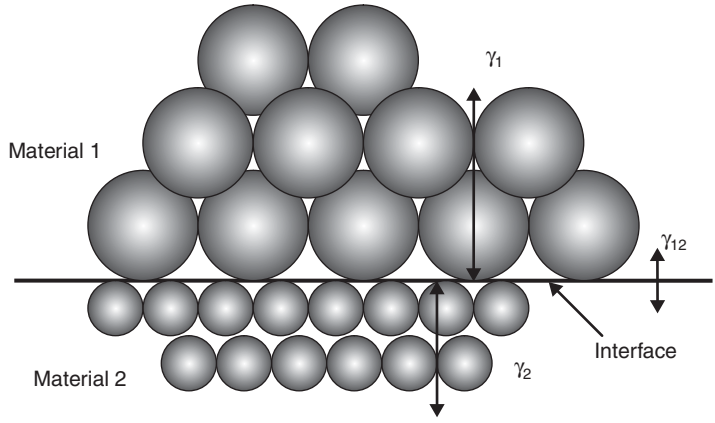


Figure 5.22 An interface model based on intramolecular attractive forces [49].

Experimentally, the interfacial bonding strength can be characterized in terms of the electron binding energy between pairs of materials, and is a unique property of that pair. Thus, the interfacial fracture toughness must be measured for commonly used material pairs in packaging applications.

Interfacial bonding strength can be characterized in terms of the electron binding energy between pairs of materials, and is a unique property of that pair. Thus, the interfacial fracture toughness must be measured for commonly used material pairs in packaging applications.

The adhesive strength is found to be affected by the cure conditions [50]. Phenomena such as undercuring, void formation, epoxy degradation, and residual stresses can lead to poor adhesive strength. Residual stresses are often introduced as a result of temperature dependent elastic modulus and CTE mismatches in adhering materials.

In the delamination process with Alloy-42 as the lead-frame material, the delamination starts at the die bonding layer and propagates from the side surface to the bottom surface of the die pad, as shown in Fig. 5.23(a). In the delamination process with copper alloy as the lead-frame material, the delamination starts at the interface between the bottom surface of the die pad and the resin, as shown in Fig. 5.23(b), and propagates from the side surface of the die pad to the side surface of the chip [51]. The difference in the delamination processes between copper-based and Alloy 42 lead-frames can be attributed to their difference in adhesion strength. Copper-based lead-frames generally can bond to the epoxy molding compound with lower adhesion strength compared to lead-frames made of Alloy 42.

Petitioner Samsung Ex-1055, 0270

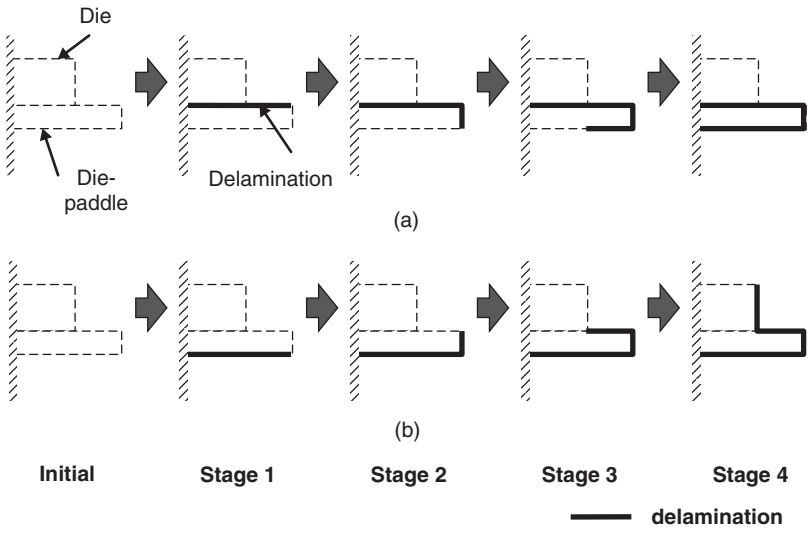


Figure 5.23 Stages of delamination from (a) the top and (b) the bottom of the die-paddle.

The mechanism by which moisture reaches the interfaces in the package is an important factor in vapor-induced and moisture-induced delamination. Moisture diffuses, either through the bulk encapsulant or along the interface between the lead-frame and molding compound. Experiments with moisture sensors reveal that when the adhesion between the molding compound and the lead-frame is good, the main path of ingress into the package is through the bulk of the encapsulant [52,53]. However, when this adhesion is degraded by improper assembly procedures—for example, oxidation from bonding temperatures, lead-frame warpage from insufficient stress relief, or excessive trim and form forces [54], —delamination and microcracks are introduced at the package outline and either moisture or water vapor can diffuse readily along this path.

At each interface, moisture can cause hydration of the polar epoxy bonds, and thus weaken and degrade the interfacial chemical bonds. However, different molding compounds respond differently to moisture exposure. Low-stress epoxy compounds, for instance, with silicone modifiers added for stress reduction, tend to be more susceptible to changes induced by moisture than molding compounds without silicone. A low glass transition temperature also decreases moisture absorption. The effect of package moisture absorption on the adhesion of epoxy mold compounds to copper lead-frames has been investigated [49] and the general trend observed is shown in Fig. 5.24.

Petitioner Samsung Ex-1055, 0271

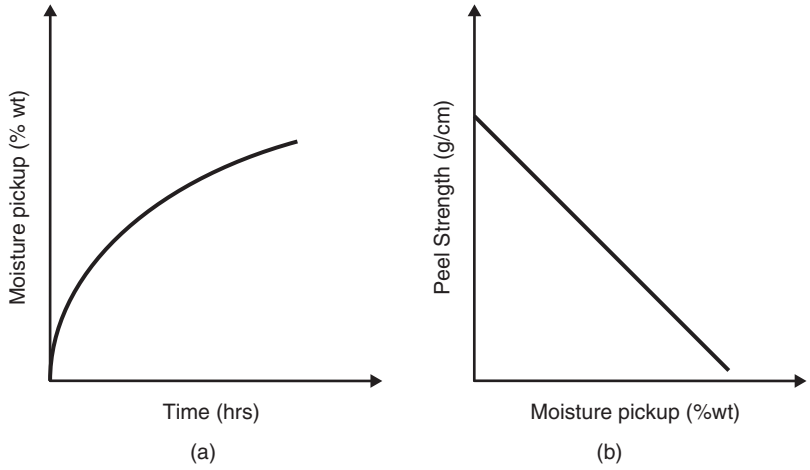


Figure 5.24 (a) Package moisture absorption and (b) its effect on the adhesion of epoxy mold compounds to copper lead-frames [48].

Degradation in bond strength can be detected by a gradual decrease in signal intensity during analysis with acoustic microscopy. Scanning acoustic tomographs conducted on plastic devices suggested that moisture absorbed by the encapsulant tended to migrate to the various interfaces in the package [55].

Surface cleanliness is a crucial requirement for good adhesion. Oxidized surfaces, such as copper-alloy lead-frames exposed to high temperatures, often lead to delamination [49,56]. The presence of nitrogen or a forming-gas shroud helps to avoid oxidation and is recommended during high-temperature processes.

Low-affinity surface finishes, such as silver-spot plating, enhance interfacial adhesion. Traditionally, silver plating of the die pad is employed for bias control and to prevent oxidation on leads. Unfortunately, silver plating adheres poorly to molding compounds and can also cause silver migration and electrical shorting [54,55]. Newer lead-frame designs use spot plating to minimize both the amount of precious metal used and the lead-frame coverage, which is susceptible to delamination.

Lubricants and adhesion promoters in molding compounds have been shown to encourage delamination in plastic packages, and must be delicately balanced [49]. Lubricants facilitate removal of the molded parts from the mold cavities at the risk of greater interfacial delamination. On the other hand, adhesion promoters ensure good interfacial adhesion between the compound and the component, but parts may be hard to pry out of the mold cavity.

Petitioner Samsung Ex-1055, 0272

Delamination not only presents a path for the diffusion of water vapor, but also is the source of resin cracking. A delaminated interface is a site of crack initiation and propagation through the bulk resin when subjected to high external loads. Saitoh and Toya [51] studied the effect of different lead-frame materials on the location of the delamination that results in resin cracking. With Alloy-42 as the lead-frame material, the delamination which most easily produces resin cracking is that between the bottom surface of the die- paddle and the resin. Other interfacial delaminations appear to have little impact on resin cracking. With copper alloy as the lead-frame material, the delamination that most easily produces resin cracking occurs in the die bonding layer [51].

5.3.2 Vapor-Induced Cracking (Popcorning)

During the assembly of plastic-encapsulated devices on the printed circuit boards, package cracking (or popcorning) can occur as a result of vapor pressure and the internal stresses generated by the reflow solder temperature profile. Vapor-induced cracking consist of two main stages: vapor-induced delamination and cracking (see Fig. 5.25). The mechanism of vapor-induced delamination during solder reflow process has been discussed in the previous section. Vapor-induced cracking is known as popcorning because of the audible popping sound produced as the entrapped high pressure vapor escapes the package through the crack, similar to that produced during popcorn cooking.

Many studies have investigated popcorning in plastic packages [57–63]. The criteria for popcorning found by Matsushita Electric Industrial Corporation [64] can be expressed as:

$$\sigma_p \geq \sigma_R \tag{5.6}$$

where σ_p is maximum stress at the edge of the die-paddle and σ_R is flexural strength of the molding compound at solder reflow temperature.

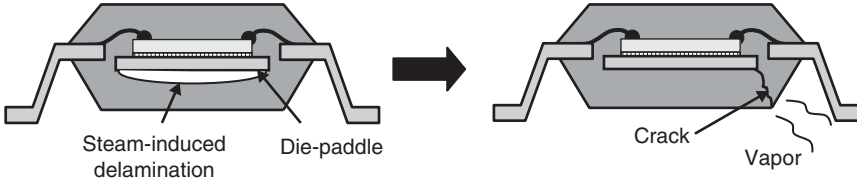


Figure 5.25 Popcorning stages: delamination and cracking.

Petitioner Samsung Ex-1055, 0273

The maximum stress is related to the water vapor pressure and package geometry:

$$\sigma_p = \frac{1}{3} cp\left(\frac{a}{h}\right)^2 \tag{5.7}$$

where c is a constant, p is the water vapor pressure at soldering temperature, a is the longer dimension of the paddle, and h is the package thickness under the paddle. Figure 5.26 shows the correlation of 260°C dip-soldering-induced plastic quad flatpack cracking with varying die pad sizes, obtained by Matsushita [64].

Fracture mechanics can be used to determine stress intensity factors during popcorning [60,65]. The effective 3D stress intensity factor, K_{eff}, at the tip of the crack can be determined as

$$K_{eff}^{3D} = f \cdot \sqrt{(K_I^{2D})^2 + (K_{II}^{2D})^2} \tag{5.8}$$

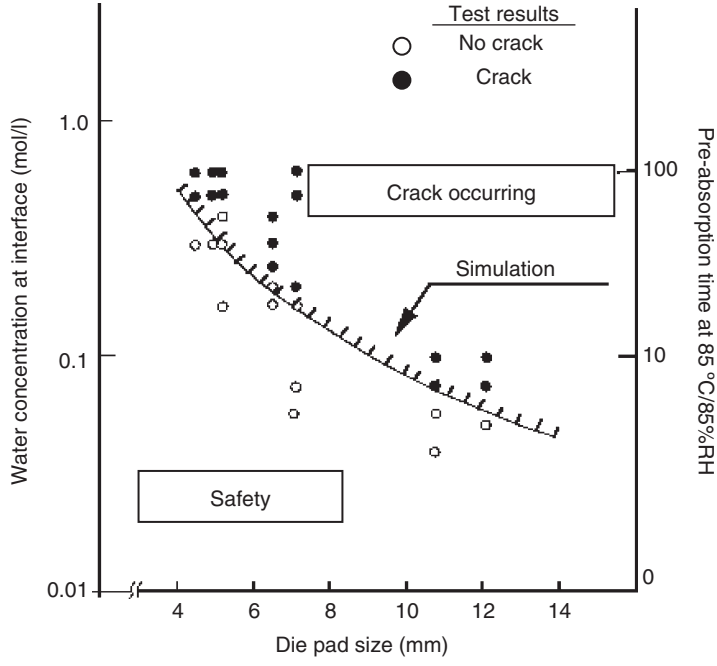


Figure 5.26 Correlation of 260°C dip-soldering-induced plastic quad flatpack cracking with varying die-pad sizes [64].

Petitioner Samsung Ex-1055, 0274

where f is the 2D to 3D correction factor and subscripts I and II represent cracking modes [60]. When K_{eff} exceeds the fracture toughness of epoxy molding compound, popcorning occurs.

The cracks often propagate from the die-paddle to the bottom surface of the package (Fig. 5.25) where they are difficult to see during visual inspection of soldered boards. Occasionally, depending on package dimensions, cracks may propagate to the top of the package or along the plane of the leads to the package sides, where they become more visible [66]. Larger and thinner packages such as QFPs and TQFPs are extremely susceptible to popcorning [67]. Also, popcorning is more prevalent with higher ratios of paddle area to device area and of paddle area to minimum encapsulant thickness [59]. Other problems that may occur during popcorning include ball bonds shear from the bond pads, and silicon craters beneath the ball bonds. The main factors contributing to popcorning are:

- the material properties of the encapsulant, the lead-frame, the die, and the die-paddle;
- the lead-frame design;
- the ratio of the paddle area to the minimum encapsulant thickness surrounding the paddle;
- the adhesion of the encapsulant to the die-paddle and the lead-frame;
- the moisture absorbed in the encapsulant;
- the contamination level;
- the voids in the encapsulant; and
- the reflow process parameters [54].

The simplest way to reduce package failures during surface-mounting is to keep the molded devices in a sealed, moisture-barrier bag with desiccant until they are attached to the circuit board. However, this imposes restrictions on component handling in the factory and can reduce efficiency for very-low-volume assembly plants.

Temperature baking is often used to reduce the moisture content of the plastic packages before mounting and eliminate moisture-related cracking. According to Lin et al. [68,69], the safe allowable moisture content is around 1100 ppm, or approximately 0.11% by weight. Baking the components at 125°C for 24-hour drives off a sufficient amount of the absorbed moisture. Residual moisture of 0.08% by weight can thus be obtained, allowing the manufacturer and user sufficient shelf life.

Petitioner Samsung Ex-1055, 0275

However, integrated circuit packages have been shown to withstand damage due to package cracking at moisture levels as high as 0.3% by weight [70]. Therefore, dry-bagging precautions, based on the 0.11% moisture content limit have been questioned for their usefulness and cost-effectiveness. Instead, parts are classified based on their storage floor life (out of bag) at the board assembly site. The parts are classified into 6 levels, and appropriate precautions are taken during handling. Further discussion of moisture level classification will be provided in the following chapters.

The resistance of molding compound to soldering heat can be improved by improving the adhesion strength, mechanical strength, and moisture absorption ratio [71]. The glass transition temperature of the molding compound can be increased until it is close to the solder reflow temperature. Although epoxy molding compounds are capable of reaching this level of glass transition temperature, the problem is maintaining post-encapsulation low die stresses. An opposite approach keeps the glass transition temperature below the solder reflow temperature to dissipate strain, while increasing the modulus of the molding compound in the rubbery region. This approach ensures that the material does not sustain enough water vapor-induced deformation to damage the package [72]. Increasing the strength of the molding compound above the glass transition temperature will prevent tearing of the encapsulant.

Other methods to prevent package cracking include designing packages to decrease stress on the plastic due to water vapor and using plastic molding compounds with high bending strengths at soldering temperatures. In addition to improving molding compound properties, other materials in the package can be also be optimized for added resistance to popcorning during solder reflow process. Kim and Lee [73] found that the selection of chip and die-paddle material with higher strength at room temperature can significantly improve popcorning resistance of the plastic package.

A polyimide film with excellent adhesion to both the die pad and the molding compound can be formed to suppress possible molding compound exfoliation from the die pad and to reduce the stress from moisture vaporization under solder heat [71]. Adhesion promoters, such as coupling agents, have been used to increase the adhesion of the encapsulant to the lead-frame and the die-paddle. Special lead-frame designs intended to increase the "tooth," or roughness, of the lead-frame can reduce or eliminate delamination of the encapsulant from the surface, particularly in the area of the die-paddle [74].

Petitioner Samsung Ex-1055, 0276

Cracks in plastic packages are usually initiated at the stress concentration points on the lead-frame (i.e., edges and burrs) and propagate through the thinnest plastic region. Burrs are small size deformations on the lead-frame surface created during the stamping process. Reversing the stamping direction to cause burrs at the top of the lead-frame or etching the lead-frame (coining) can reduce the amount of cracking [71].

Package cracks sometimes extend from die-bond voids at die edges, so a void-free die-bonding process is crucial. This technique requires forming the central portions of the longer sides of the die pad, where the maximum stress is concentrated, inward to the chip outline (anchoring).

Fukuzawa et al. [75] suggest providing a vent hole in the plastic encapsulant underneath the die pad to allow vaporized moisture to exit. To be effective the hole must be drilled through the encapsulant into the die-attach material. Moisture in the plastic package tends to diffuse toward the largest void in the molding compound; as the largest void, the vent hole facilitates moisture diffusion out of the package. This may be an economical method of preventing popcorning, however, objections to this method arise because drilling a vent hole induces a defect in the package and may cause unforeseen reliability problems later.

5.3.3 Brittle Fracture

Brittle fracture generally occurs in materials that exhibit low levels of yielding and inelasticity such as the silicon die. Brittle fracture may also occur in encapsulant material due to the effect of highly loaded brittle silica fillers. When the material is under excessive stress levels, sudden catastrophic crack propagation can initiate from a microscale defect such as a void, inclusion, or discontinuity.

Fracture mechanics can be used to model the brittle failure at the defect sites. Figure 5.27 shows the coordinate system used for modeling the Mode I crack propagation. Mode I cracking, also referred to as opening crack, is the most common type of cracking and it is due to tensile stress. Other cracking modes include Mode II (sliding mode) and Mode III (tearing mode) which are due to in-plane shear and out-of-plane shear, respectively.

The stress field at the vicinity of the Mode I crack [39,40], assuming plane stress ($\sigma_z = 0$), is described by

$$\sigma_x = \frac{K_I}{\sqrt{2\pi r}} \cos\frac{\theta}{2}\left(1 - \sin\frac{\theta}{2}\sin\frac{3\theta}{2}\right) \tag{5.9}$$

Petitioner Samsung Ex-1055, 0277

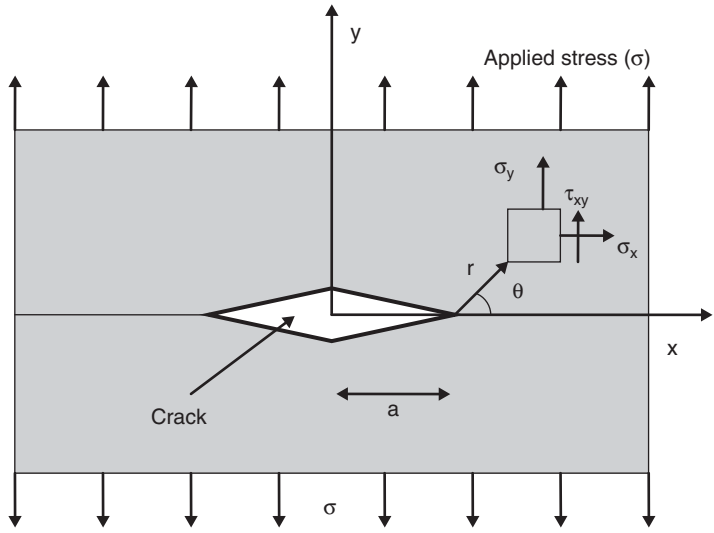


Figure 5.27 Coordinate system for modeling Mode I crack propagation.

$$\sigma_y = \frac{K_I}{\sqrt{2\pi r}} \cos\frac{\theta}{2}\left(1 + \sin\frac{\theta}{2}\sin\frac{3\theta}{2}\right) \tag{5.10}$$

$$\tau_{xy} = \frac{K_I}{\sqrt{2\pi r}} \sin\frac{\theta}{2}\cos\frac{\theta}{2}\cos\frac{3\theta}{2} \tag{5.11}$$

K_I is the stress intensity factor and can be expressed as

$$K_I = \beta\sigma\sqrt{\pi a} \tag{5.12}$$

where β is the stress intensity modification factor which is dependent on geometrical factors such as crack size and location, σ is the uniaxial applied stress, and a is the crack half-length.

K_I is a function of size and shape of the crack, geometry, and applied stresses. Crack propagation occurs when K_I equals or exceeds the critical stress intensity factor, K_{IC} [40,76]:

$$K_I \geq K_{IC} \tag{5.13}$$

The critical stresses intensity facture, K_{IC}, also known as the fracture toughness of the material, is a material property which characterizes the ability of a material to resist fracture. K_{IC} for engineering polymers and ceramics is between 1 and 5 MPa [40].

Kitano et al. [77] developed a method for measuring the critical stress intensity factor for an encapsulant ruptured by brittle fracture. The specimen

Petitioner Samsung Ex-1055, 0278

employed was cut from a plastic package and loaded to cause fracture, as shown in Figs. 5.28 and 5.29. Typically, the crack initiated at an angle of approximately 135° clockwise (or 45° counter-clockwise) from the chip bottom-encapsulant interface. The crack initiation orientation is along the direction of the maximum shear stress which can be predicted from plane-stress transformation equations.

Assuming a power law distribution of the stress,

$$\sigma(r) = \frac{K_{stress}}{r^{\lambda}} \tag{5.14}$$

where $\sigma(r)$ is a circumferential stress component at distance r from the corner, K_{stress} is the stress intensity factor, and σ is the exponent. The value of the exponent is determined from the slope of the straight line obtained by plotting log $\sigma(r)$ versus log r. The assumption of the power law stress distribution can be verified by plotting the stress intensity factor for the circumferential stress component as a function of the angle, measured from

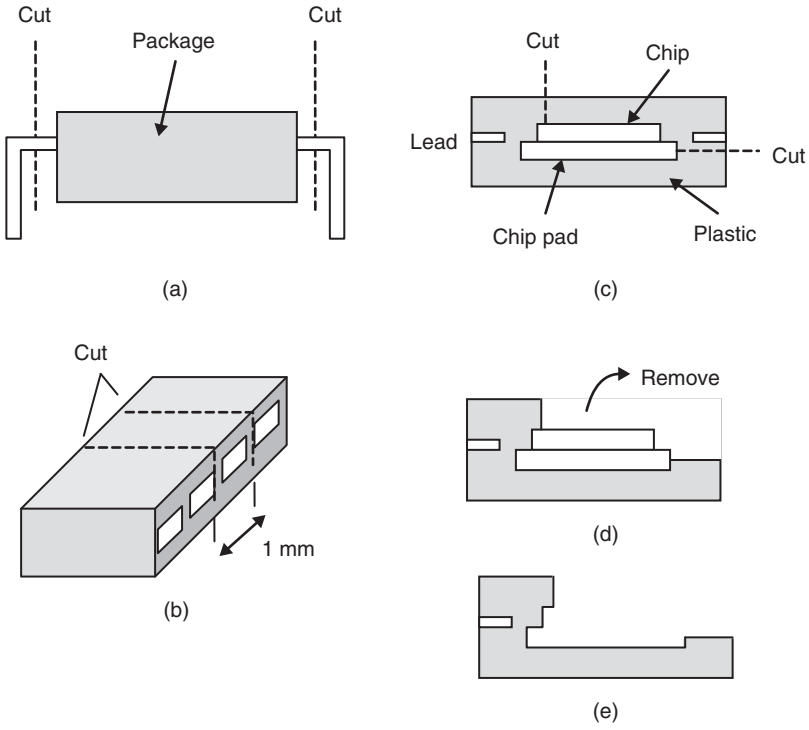


Figure 5.28 Specimen cut out from a plastic package for obtaining critical stress intensity factor for the encapsulant [77].

Petitioner Samsung Ex-1055, 0279

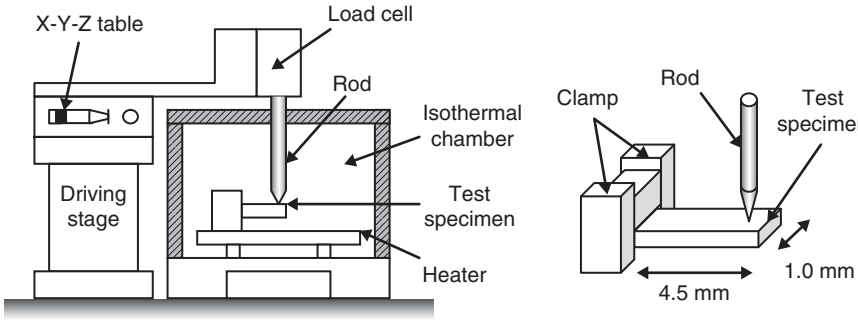


Figure 5.29 Loading to fracture of the specimen [77].

the base of the die, where the stress intensity factor peaks at an angle of 135°. Because crack initiation takes place at the same angle, the failure criteria or critical stress intensity factor can be computed using scaling technique:

$$K_{stress} = x.f_{load} \tag{5.15}$$

where x is the stress intensity factor along the angle axis at $\theta = 135°$ for a 1 N load and f_{load} is a scaling factor for the load.

5.3.4 Ductile Fracture

Encapsulant materials are susceptible to both brittle and ductile fracture depending on environmental and material factors including temperature (below or above T_g), viscoelastic properties of the polymeric resin, and filler loading. Even in encapsulant materials that are highly loaded with brittle silica fillers, ductile fracture may still occur due to the viscoelastic polymeric resin. The crack tip in epoxy molding compounds has been observed to exhibit a localized yielding zone. Crack-tip blunting may occur depending on the formulation of the molding compound (for example, whether it includes either silicone modifiers or flexibilizers incorporated directly into the molecular network). The fracture toughness of the molding compound also depends on the composition of the formulation. Resin chemistry filler technology (type, size, distribution, and interfacial adhesion treatment) plays an important role [78].

When plasticity around the crack tip is appreciable, the J-integral is often used to provide a measure of the energy release rate of an advancing crack. The value of the J-integral, the crack-driving force for fracture in

Petitioner Samsung Ex-1055, 0280

ductile materials, is often calculated using an engineering approach [79,80]. The linear elastic component of the J-integral is related to the stress intensity factor, K:

$$J = \begin{cases} \dfrac{K^2}{E} & plane\,stress \\ \dfrac{(1-v^2)K^2}{E} & plane\,strain \end{cases} \tag{5.16}$$

where v is Poisson's ratio. The plastic component of the J-integral can be obtained using the pure bending plane strain solution [81]. The presence of initial crack-like defects is not important for ductile fracture, because the crack propagation time often dominates the time to failure.

5.3.5 Fatigue Fracture

When the encapsulant is subjected to repetitive cyclic stresses below the ultimate strength of the material, it can fracture due to accumulated fatigue damage. The cyclic stresses can arise due to hygroscopic, thermal, mechanical, or combined loads applied to the encapsulant material. Fatigue failure is a wearout mechanism that typically initiates a crack at a point of discontinuity or defect.

Fatigue fracture mechanism consists of three stages: crack initiation (Stage I), stable crack propagation (Stage II), and sudden, unstable, and catastrophic failure (Stage III). The fatigue crack propagation in Stage II is a stable increase in crack length under cyclic stresses. The rate of increase in crack length per cycle can be described by Paris' law [39,40,82]:

$$\frac{da}{dN_f} = C\left(\Delta K_I\right)^m \tag{5.17}$$

where a is the crack length, N_f is the number of cycles to failure, ΔK_I is the stress intensity factor range, and C and m are material constants. The stress intensity factor range can be further expressed as:

$$\Delta K_I = \beta(\Delta\sigma)\sqrt{\pi a} \tag{5.18}$$

where $\Delta\sigma$ is the stress range, difference between the maximum and minimum stresses.

Petitioner Samsung Ex-1055, 0281

For encapsulants, m is approximately 20 [82], much higher than the typical value for fatigue crack propagation in metals (typically from 2 to 8), indicating faster crack propagation in encapsulants. The final stage of fatigue fracture does not really involve fatigue, and sudden fracture occurs when K_I reaches K_{IC}, the critical stress intensity factor for undamaged material.

The number of cycles to fatigue fracture can be obtained by integrating Paris' equation:

$$N_f = \frac{1}{C}\int_{a_i}^{a_f} \frac{da}{(\Delta K_I)^m} \tag{5.19}$$

Nishimura et al. [82] estimated the life of a package subjected to thermal cycles using Paris' integral equation (Equation). The stress intensity factor for a change in temperature was calculated using finite element methods, and the relationship was expressed as a polynomial, $f(a)$. The constants C and m have been determined for the encapsulant materials using single-edge-notch specimens [82]. The initial crack length, a_i, was taken to be some small value dependent on manufacturing defects, but the total number of cycles to failure is relatively insensitive to initial crack length, provided the crack is small.

The number of cycles to failure can also be determined empirically using stress-life (S-N) curves. S-N curves are constructed by applying cyclic stresses below the ultimate strength of the material, and measuring the number of cycles to failure for the specific applied stress range. The stress range is related to cycles to failures by a power law function [83] and can be used to determine cycles to failure:

$$N_f = b\sigma^c \tag{5.20}$$

Fracture-mechanics-based techniques have been used to characterize fatigue crack propagation at polymer-metal interfaces. Under cyclic loading, crack growth rate was found to have a power-law dependence on the strain energy and release energy range, and exhibited a crack growth threshold, much like the fatigue crack growth threshold stress intensity factor range for monolithic bulk metals, polymers, and ceramics.

For an adhesive joint exhibiting bulk linear-elastic behavior, i.e., away from the crack tip region, the strain energy release rate, G, is given by

$$G = \frac{P^2}{2B}\frac{\partial C}{\partial a} \tag{5.21}$$

Petitioner Samsung Ex-1055, 0282

where P is the applied tensile load, B is the width of the adhering materials, and $\partial C/\partial a$ is the rate of change of compliance C with respect to crack length a [84].

Interfacial fatigue crack propagation resistance was found to increase with surface roughness. This was attributed to a reduction in effective driving force for fatigue fracture along the rougher interfaces and could be accounted for by a crack-deflection model [85].

5.4 Failure Accelerators

Environmental and material loads and stresses such as moisture, temperature, and contaminants can accelerate failure mechanisms in a plastic-encapsulated package. The rate at which the failure mechanisms are affected by the failure accelerators depend on material properties, processing defects, and package design.

Encapsulation plays a critical role in package failures. Properties such as moisture diffusion coefficient, saturation moisture content, ion diffusion rate, CTE, and coefficient of hygroscopic swelling of the encapsulant material can significantly affect the rate of failure mechanisms.

5.4.1 Moisture

Moisture can accelerate failures including delamination, cracking, and corrosion in encapsulated microelectronic packages. Mechanisms involved in moisture-induced failure acceleration include moisture-induced adhesion degradation, hygroscopic swelling stresses, moisture vapor pressure, moisture-assisted transportation of ions, and moisture effects on encapsulation properties [86–88]. Moisture can change the properties of the encapsulant material such as the glass transition temperature, elastic modulus, and bulk resistivity.

Characterization of moisture effects on material properties and the investigation of moisture induced failure mechanisms are necessary for accurate reliability assessment of encapsulated electronic devices exposed to moisture. Because of the differences in formulation of various encapsulant materials and subsequent variation in moisture sorption characteristics, the effects of moisture on material properties can vary from one type of encapsulant to another.

Many studies have modeled moisture diffusion and sorption in plastic-encapsulated packages [38,46,89–96]. Both Fickian and non-Fickian models

Petitioner Samsung Ex-1055, 0283

have been explored. Characterization of moisture diffusion in encapsulant materials was discussed in Section 4.2.6.

A 1D Fickian model can be used to compute the moisture concentration at the die-encapsulant interface [90,91]. Ignoring the temperature gradient in the encapsulant and evaluating molding compound properties at the mean temperature of the die and package, the moisture concentration at the die–encapsulant interface can be determined by solving the 1D differential equation (Equation 4.8) and obtaining:

$$C(x,t) = C_0 - \sum_{n=0}^{\infty} \left\{ \frac{4(-1)^n C_0}{\pi(2n+1)} - F_n \right\} \exp\left[-\frac{1}{4l^2}(2n+1)^2 \pi^2 Dt \right] \cos\left[\frac{1}{2l}(2n+1)\pi x \right] \quad (5.22)$$

where F_n is the Fourier coefficient given by

$$F_n = \frac{2}{l} \int_0^l C_0(x) \cos\left[\frac{1}{2l}(2n+1)\pi x \right] dx \quad (5.23)$$

The history effect—that is, the variance of the ambient humidity due to time—is input into the solution through the term $C_0(x)$. Figure 5.30 shows moisture absorption and desorption curves for a plastic package as a function of exposure time in hours [90]. The level of moisture saturation is defined as the ratio of the actual absorbed moisture mass to the saturated absorbed moisture mass. Absorption curves correspond to the number of hours at 85°C/85% relative humidity (RH); desorption corresponds to 80°C.

The boundary and initial conditions for moisture concentration must also be determined. The moisture flux at the die-encapsulant interface is assumed to be zero:

$$\frac{\partial C(x=0,t)}{\partial x} = 0 \quad (5.24)$$

At the surface exposed to the ambient, a steady-state moisture concentration is given by the ambient temperature T_a, the relative humidity, and the encapsulant moisture saturation coefficient as

$$C(x=h,t) = RH\ P_{sat}(T_a) S \quad (5.25)$$

Petitioner Samsung Ex-1055, 0284

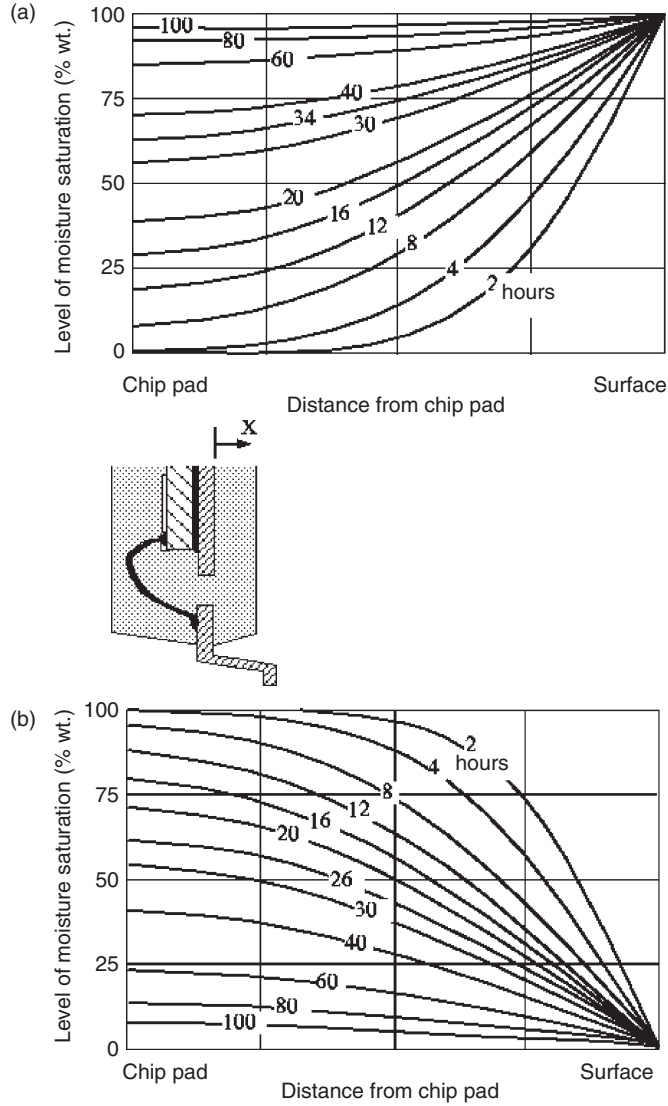


Figure 5.30 (a) Moisture absorption at 85°C/86% RH and (b) desorption at 80°C for a plastic package [90].

Petitioner Samsung Ex-1055, 0285

where the $P_{sat}(T_a)$ is the saturation vapor pressure at the ambient temperature. The initial condition is the moisture concentration, as a function of distance from the die-encapsulant interface:

$$C(x, t = 0) = C_0(x) \tag{5.26}$$

Belton et al. [97] suggested that moisture induced swelling leads to microcracking in the material. Baking the encapsulant removes the moisture from the bulk, but the cracks do not self-heal, as they do with thermoplastics. When the encapsulant is again exposed to hot, humid conditions, moisture is reabsorbed, and the cumulative micro-damage remains. The absorption and resorption coefficients are similarly affected.

Swelling due to moisture absorption is one of the reasons for plastic package deformation. In highly filled materials, moisture can either condense in microcracks (it is believed this occurs at the interface of the filler particle—polymer) or dissolve into a polymer. As a first approximation, a simple additive elongation equation can be used:

$$\frac{\Delta l_e}{l_e} = \frac{1}{3}(1 - v_{filler})\frac{\Delta m}{M_c}\frac{\rho_C}{\rho_W} \tag{5.27}$$

where v_{filler} is the volume part of the filler, Δm is the quantity of absorbed water, M_c is the mass of composite, ρ_c the specific density of composite, and ρ_w the specific density of water.

For typical epoxy novolac composites the pressure cooker test (120°C/100% RH/100 hours at 2 atm) leads to a moisture uptake of 0.9–1%. According to Equation 5.9 the elongation is 0.27–0.33%. Direct measurements with epoxy novolac premixes give elongations between 0.22% and 0.3%. This means that most of the moisture in encapsulating composites is absorbed in the polymer.

An elongation of 0.2–0.3% is equal to an increase in temperature of 90–110°C from sorption isotherm studies. Therefore, the combination of moisture absorption and increased temperature may cause deformation to a package.

Both finite element simulations of moisture diffusion during preconditioning of plastic integrated circuit packages and the simultaneous diffusion of heat and moisture during vapor phase reflow soldering have shown results in good agreement with experimental data. It was found that, irrespective of the manner of moisture preconditioning (moisture absorption or desorption), the same critical water vapor pressure is obtained and that the water vapor in the delaminated interface never reached saturation during the short period when solder reflowed and re-solidified.

Petitioner Samsung Ex-1055, 0286

Finite element simulation of moisture weight gain or loss in PBGA package as a function of time has been conducted, considering the effects of package geometry and material selection. The results were found to be close to experimental values. The conclusion is that popcorn failures result when moisture concentration in the die attach region exceeds 0.0048 g/cm^3.

For moisture diffusion processes with no local sources and sinks, accompanied by simultaneous heat conduction in the same region, the equations are:

$$\frac{\partial}{\partial x_i} D_{ij} \left(\frac{\partial C}{\partial x_j} \right) = \frac{\partial C}{\partial \tau} \tag{5.28}$$

$$\frac{\partial}{\partial x_i} \left(k_{ij} \frac{\partial T}{\partial x_j} \right) = \rho \, c_p \frac{\partial T}{\partial \tau} \tag{5.29}$$

$$\nabla \cdot k \nabla T = \rho \cdot c_p \frac{\partial T}{\partial \tau} \tag{5.30}$$

where C is the moisture concentration, D is the moisture diffusivity, x is the Cartesian coordinate, and τ is the time. T is the temperature, k is the thermal conductivity, ρ is density and c_p is the specific heat. D and k are assumed to be functions of temperature [35].

5.4.2 Temperature

Temperature is a critical failure accelerator in plastic-encapsulated microelectronics. The effects of temperature on package failures are often evaluated based on the temperature level with respect to the glass transition temperature of the molding compound, the CTE of the respective materials, and the resulting thermo-mechanical stresses.

The glass transition temperature is the point at which the modulus of a polymer decreases markedly, though such a reduction is gradual over a small range of temperature. As a polymer approaches the glass transition temperature, the flexural modulus drops, the CTE increases, the ionic/molecular mobility increases, and the adhesion strength decreases.

Temperature can have secondary effects on failures by changing the temperature-dependent properties of the package materials such as moisture diffusion coefficient and solubility. Certain failure mechanisms such as corrosion and intermetallic diffusion are also accelerated by elevated temperatures. The presence of halogenated species from conventional

Petitioner Samsung Ex-1055, 0287

molding compound materials, can lead to the acceleration of intermetallic diffusion at temperatures even lower than normal [57,98,99].

Equations of the effect of temperature on various material parameters have been presented in previous sections. Thermal strain due to CTE mismatches is expressed in Equation 5.1. Temperature dependencies of properties such as diffusion coefficient and solubility are stated in Equations 4.12 and 4.13, respectively. Package heating due to high temperatures can be modeled using heat transfer equations expressed in Equations 5.29 and 5.30.

5.4.3 Exposure to Contaminants and Solvents

Contaminants provide sites for failure mechanism initiation and propagation. Sources of contaminants are atmospheric pollutants, moisture, solder flux residues, ionic impurities in plastic materials, corrosive elements produced by thermal degradation, and outgassing by-products in die-attach adhesives (usually epoxies).

Migration paths of contaminants can vary, depending on the integrated circuit package assembly process. Outgassing by-products of the die-attach curing operation are deposited directly onto the lead-frame or the die surface. Once encapsulated by the molding compound, polymerization residues (e.g., catalyst fragments or initiator radicals) can be transported into the package by the diffusing water. Similarly, external contaminants on the leads or package surface can also be brought into the package by absorbed water. A solid transport medium is not required, especially with corrosion induced by outgassing products [54]. In this case, exposure to fumes released by the molding compound at high temperatures is sufficient to degrade a bonding interface. These fumes originate from the decomposition of silicone modifiers and the resin blend, and can attack any exposed aluminum on the bond pads to form porous intermetallics highly detrimental to device performance.

Ionic contaminants can be found in corrosion by-products. Contamination due to saliva results in a corrosion product containing trace amounts of aluminum, potassium, chlorine, sodium, calcium, and magnesium. The presence of zinc may be due to perspiration contamination, since zinc is a common element in many antiperspirants. However, with current clean room and operator controls, these contaminants are now unlikely.

Corrosion is a chemical or electrochemical degradation of the metallic interconnect elements. The plastic encapsulant is not prone to corrosion, but it can aid in the corrosion of metallic components in the package such as the die metallization, lead-frame and wire-bond by allowing the moisture

Petitioner Samsung Ex-1055, 0288

and contaminants to diffuse through and reach the metallic sites [100,101]. A time-dependent wearout failure process, the rate of corrosion depends on the component materials, the availability of an electrolyte, the concentration of ionic contaminants, the geometry of the metallic elements, and the local electric field. Common forms of corrosion are uniform chemical, galvanic, and pitting [58].

Levels of water-extractable ions of molding compounds vary. Conventional molding compounds have less than 25 parts per million (ppm) for halides (chlorides and bromides), 20 ppm for calcium, 10 ppm for potassium and sodium, and 3 ppm for tin. High impurity levels are sufficient to initiate corrosion under typical environmental conditions. Indeed, the conductivity of water extracts and the concentration of water-leachable ions are generally good predictors of reliability [102] but good die passivation and ion-getters can negate the problem. Also, low moisture and ion diffusion coefficients can delay corrosion initiation.

Lantz et al. [103] found that the chloride ions dissolved in the molding compound diffused through the material as a front. The rate of ion diffusion was found to be nine orders of magnitude slower than that of moisture diffusion indicating that the encapsulant can be effective in delaying ion transportation to the die surface in the package. The significantly lower rate of ion diffusion in molding compounds can be due to binding of ions to the ion-getters and the functional groups in the encapsulant material. It was also observed that the rate of ion diffusion increased above the glass transition temperature.

During cleaning operations, packages may be exposed to solvents including isopropyl alcohol, methyl ethyl ketone, and chlorinated fluorinated organic solvents. It is important to address how quickly such solvents permeate the encapsulant, what type of chemical or physical damage they do to the epoxy network, and what influence they have on performance. For applications in which exposure to solvents (such as jet fuel or hydraulic oil) is routinely unavoidable during preventive maintenance or field conditions, more reliability field data need to be collected.

5.4.4 Residual Stresses

Residual stresses are generated in a package immediately after die attach. Depending on the nature of the die-attach (e.g., polyimide, silicone, or silicone-modified epoxy), various stress levels can be achieved [104]. New molding compounds are being synthesized for lower CTEs, lower stiffness, and higher glass transition temperatures. However, trying

Petitioner Samsung Ex-1055, 0289

to optimize the stress level requires more than just selecting the lowest-stress die-attach or molding compound materials. The best combination for a package configuration will involve trade-offs between various parameters [105].

Molding imparts stresses that are quite high, since the encapsulant shrinks more than other package materials. Stress-test chips are being employed to characterize assembly stresses [53,106]. The lead-frame stamping process leaves residual stresses and sharp burrs that act as stress concentrators. The magnitude of the residual stresses depends on the package design, which includes both the paddle and the lead-frame. Because of the additive effects of pre-existing residual stresses and moisture-induced stresses, the higher the residual stresses are in the package, the lower will be the critical amount of absorbed moisture that leads to vapor-induced delamination or cracking.

5.4.5 General Environmental Stress

Depolymerization is characterized by the breaking of polymeric bonds, which can turn the solid polymer into a gummy liquid comprising monomers, dimers, and other lower-molecular-weight species. Elevated temperatures and a closed environment usually accelerate depolymerization.

Exposure to seemingly harmless conditions, such as outdoor sunlight, may lead to gradual depolymerization. The ultraviolet rays in sunlight and atmospheric ozone can be powerful agents that depolymerize epoxy by scissioning the molecular chains.

Depolymerization can be prevented either by avoiding conditions that induce reversion or by using polymers tested for reversion resistance. Products that need to perform under hot and humid conditions require reversion-resistant polymers. Prediction of a material's behavior from chemical structure classification alone is unreliable. In addition, due to the proprietary nature of epoxies, the exact formulation is often not provided by compound manufacturers to integrated circuit suppliers [55].

To insure that polymer reversion will not occur, compound suppliers usually do extensive experimentation on the ingredients, using various stoichiometric ratios to produce a mix with the optimum properties. Reversion due to temperature or temperature/humidity can be detected by changes in the IR spectrum. There are also some empirical physical tests for hydrolytic reversion such as IPC-TM-650 Method 2.6.11 used for solder masks but also can be used for encapsulants and adhesives. Shore hardness testing can also be performed.

Petitioner Samsung Ex-1055, 0290

5.4.6 Manufacturing and Assembly Loads

Failure may result from manufacturing and assembly conditions, including high and low temperatures, temperature changes, handling loads, and loads on wire bond and die-paddle assemblies due to flowing encapsulant. Popcorning of surface-mount plastic packages is one example. The design team must identify manufacturing and assembly stresses and account for them in developing appropriate guidelines. Generally, electronic manufacturing, assembly, and packaging are performed in controlled clean rooms where moisture, temperature, particulates, and handling conditions are monitored and controlled.

5.4.7 Combined Load–Stress Conditions

Failure accelerators such as temperature and moisture are often present in combination during manufacturing, assembly, or operation. Combined load and stress conditions generally produce more severe acceleration of failures. This fact has been used in the design of acceleration tests for the purpose of screening defected parts and identifying packages prone to failures.

Figure 5.31 shows an example of accelerated testing on plastic dual in-line packages (DIPs) using combined load-stress condition. Both assembled and unassembled plastic DIPs are tested. Temperature cycling and coupled temperature, humidity, and bias (THB) tests are applied to plastic DIPs for use in avionic environments [107]. Temperature-cycling tests are within the range of –55°C and +85°C through 1,000 cycles, and THB tests are 1,000 hours at 85°C, 85% RH with intermittent electrical bias. Based on the results of the combined load and stress accelerated tests, life estimates for the plastic-encapsulated microcircuits can be determined. The life of the plastic DIPs subjected to the accelerated tests shown in Fig. 5.31, was estimated to be more than twenty years. More on life estimation from accelerated tests is discussed in Chapter 7.

5.5 Summary

This chapter discussed the encapsulation defects and failures including wire sweep, paddle shift, warpage, voids, flash, non-uniform encapsulation, foreign particles, delamination, popcorning and fracture. With new package designs, materials, and manufacturing and process parameter controls, many plastic-encapsulated microelectronics defects and failures are being

Petitioner Samsung Ex-1055, 0291

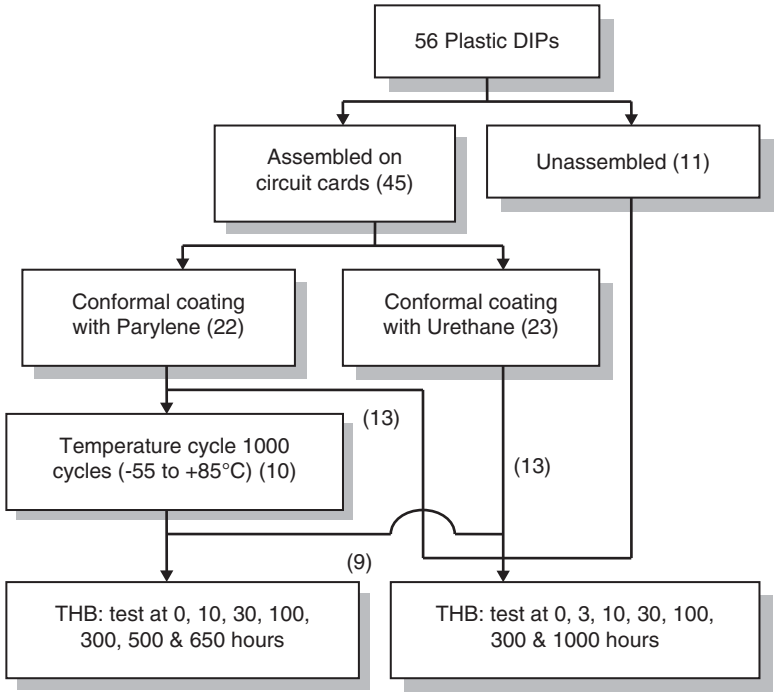


Figure 5.31 Temperature cycling and temperature, humidity, and bias (THB) tests on plastic dual in-line packages (DIPs).

eliminated or significantly reduced. An understanding of the encapsulation defects and failure mechanisms and respective models, relevant contributing factors, acceleration factors, and methods of eliminating such defects and failures is critical in ensuring a high quality and reliability encapsulated product. Contribution of loads, materials, design, and processing factors to more dominant failures should be used to identify specific applications that a given package design can tolerate for a desired cost and performance over time.

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6 Defect and Failure Analysis Techniques for Encapsulated Microelectronics

Defect and failure analysis play a critical role in producing reliable and high quality electronic packages. Identification and analysis of defects and a subsequent reduction or elimination of such defects can lead to significant improvements in manufacturing processes and result in higher quality packages. Furthermore, the information about the failure modes, sites, and mechanisms can be used to improve reliability of the encapsulated packages. For higher reliability, the factors affecting failure modes and mechanisms can be addressed during the package designing process. Proper selection and application of various analysis techniques is crucial in obtaining accurate and useful information on defects, failure modes, and mechanisms in encapsulated packages.

Defects and failures in plastic-encapsulated packages may appear with a variety of physical morphologies (e.g., large/small, subtle/coarse), and can occur anywhere in the package including the external package, internal package, die surface, die subsurface, or interface. To conduct effective failure analysis on electronic devices and packages, a disciplined step-by-step process must be followed to ensure that no relevant information is lost. The multitude of design, assembly, and manufacturing technologies demands a corresponding multitude of defect and failure analysis techniques. This chapter provides general information about the various defect and failure analysis techniques applied to encapsulated microelectronic packages with emphasis on techniques relevant to the plastic encapsulation defects and failures.

6.1 General Defect and Failure Analysis Procedures

Failure analysis techniques of plastic-encapsulated microelectronic packages can be broadly classified into two types: destructive and non-destructive. Non-destructive techniques, such as optical microscopy, scanning acoustic microscopy (SAM), and X-ray testing, are techniques that do not affect the package in any manner. They do not alter the existing defects and failures in the package or introduce new ones. Prior to non-destructive

Petitioner Samsung Ex-1055, 0302

evaluation (NDE), electrical measurements of the failed packages are made to identify failure mode. Although considered a non-destructive technique, X-ray testing may degrade the electrical properties of some devices and must, therefore, be applied after electrical evaluation.

Destructive techniques, such as decapsulation, can physically and permanently change the package. They can alter the existing defects. For example, the harsh process of decapsulation can destroy evidences of existing defects or failures in the package. Therefore, the order at which the defect and failure analysis techniques are applied is highly important. Non-destructive techniques must take place before destructive techniques. Non-destructive techniques are disadvantaged by certain resolution limitations. Defects of 1 μm or less are rarely detected by either X-rays or acoustic microscopy, but may be identifiable by other techniques such as scanning electron microscopy which may require package decapsulation.

6.1.1 Electrical Testing

Electrical testing of plastic-encapsulated microelectronics is generally performed prior to NDE. It consists of measuring all relevant electrical parameters which can reveal the failure mode (i.e., catastrophic, functional, parametric, programming, or timing) and used to identify the failure site.

Electrical testing involves the detection of shorts, opens, parametric shifts, changes in resistance, or other abnormal electrical behavior on the die, between the die and the interconnects, and between the interconnects and the circuit board. The types of electrical measurements may include integrated circuit functional and parametric testing, impedance, continuity, surface resistance, contact resistance, and capacitance [1].

6.1.2 Non-destructive Evaluation

The purpose of NDE is to identify and document defects like cracks, voids, delamination, wire sweep, warpage, discoloring, and softening without destroying the package. The first step in NDE is visual examination. Visual examination is performed with either the naked eye or an optical microscope.

Visual examination is then followed by other non-destructive analysis techniques including SAM, X-ray microscopy, and atomic force microscopy (AFM). SAM is used to identify delamination, voids, and die-tilt

Petitioner Samsung Ex-1055, 0303

in plastic-encapsulated packages without the need to open the package. X-ray microscopy is another particularly useful non-destructive technique to identify defects such as wire sweep, voids, and die-paddle shift. However, X-ray radiography may change the electrical properties of the device, so it must be applied only after the electrical measurements of the packaged device have been completed.

Failures involving deformation such as package warpage can be measured using either contact [2] or non-contact methods. A type of contact measurement technique is AFM. The AFM cantilever which spans over the package surface (or the package is scanned under the cantilever) and the cantilever deflection is recorded. Three-dimensional topographical maps of the surface can be constructed using AFM by plotting the local sample height versus horizontal probe tip position.

The shadow-Moiré method is a non-contact method based on the geometric interference of a shadow grating projected on the warped sample surface, and a real grating projected on a flat reference surface [3–5]. Improvements in the shadow-Moiré technique offer higher sensitivity and increase in dynamic range of warpage measurements [5].

Another type of visual evaluation of the package is the dye penetration test (MIL-STD-883, Method 1034). In the non-destructive version of this test (avoiding cross-sectioning of the package), the whole package can be immersed in a solution of a dye under vacuum. The package is then removed and inspected for microcracks, voids, and delamination.

6.1.3 Destructive Evaluation

Destructive evaluation is the defect and failure analysis of encapsulated microelectronic packages which involves destroying a portion or all of package. Destructive evaluation may include analytical testing of the plastic encapsulant material, decapsulation (plastic removal or package opening), internal examination of the package using various techniques, and selective layer removal.

6.1.3.1 Analytical Testing of the Encapsulant Material

Analytical testing on the plastic encapsulant material including hardness testing and infrared (IR) spectrographic analysis can reveal the curing quality of the material. Incomplete cure leads to inadequate encapsulant properties such as low glass transition temperature (T_g) which may cause reliability problems in the encapsulated package.

Petitioner Samsung Ex-1055, 0304

Durometer hardness test can indicate the curing quality of the plastic encapsulant material based on hardness. The term durometer was originally used by A.F. Shore in 1920s referring to his measurement device, but now it is used for both the hardness measurement and the measuring equipment. In durometer hardness test, the surface of the package is pressed with an indentor to measure hardness [6]. Various types of indentors (i.e., Type A, D, DO, M, etc.) recommended for specific types of surfaces (i.e., hard, soft, etc.) are listed in ASTM D2240 [6] standard test methods for durometer hardness. Low values of hardness (soft surface) may indicate improper or incomplete cure.

In IR spectrographic analysis of the plastic encapsulant, a small chip of the plastic (about 10–20 mg) is removed and subjected to IR spectrum. The spectrum from the plastic specimen is then compared to that of an original known good sample. The information obtained reveals whether the formulation of the plastic material has been altered by the supplier and whether the material is under- or over-cured.

Other methods of curing evaluation include dynamic differential scanning calorimeter (DSC) scans, and isothermal DSC scans. A small piece of plastic encapsulant is removed from the package, and subjected to DSC scan where the extent of curing is measured.

6.1.3.2 Decapsulation (Removal of the Encapsulant)

Most failure analysis techniques for plastic-encapsulated microelectronics packages require decapsulation to examine and locate the defects inside the plastic packages. Several methods are generally employed for plastic removal including chemical methods, such as sulfuric and nitric acid etching, thermo-mechanical methods [7], and plasma etching [8]. The chemical or solvent used to remove the plastic encapsulant depend on the type of plastic. For example, cured epoxies are difficult to remove and require strong acid solutions, while the silicones can be removed using fluorinated solvents. A comparison of decapsulation methods is given in Table 6.1.

The classic wet chemical decapsulation technique is usually applied in several steps: First a cavity is milled on the top of the package above 25–75 μm of the bond wires. An X-ray side-view image of the package will reveal the height of the wire loops. In case of 3D stacked die packages with relatively small clearance above the top die, care must be taken during the decapsulation process to avoid damage to the wire bonds [9].

The package is then heated and sulfuric acid (H_2SO_4) or nitric acid (HNO_3) is dripped periodically into the milled cavity in the plastic

Petitioner Samsung Ex-1055, 0305

Table 6.1 Comparison of Various Decapsulation Methods [7,8,10]

Decapsulation Method	Advantages	Disadvantages
Chemical	• Low cost • Highly reliable method • The reaction of thoroughly dehydrated acid with aluminum metallization is slow • Metallization is untouched • Relatively lower temperature process (i.e., 70°C for nitric acid etching)	• Contaminants from the surface of the die may be removed, preventing surface chemical analysis • The released water from epoxy decomposition, if in large quantity, may lead to localized corrosion of aluminum metallization • Safety measures must be taken to protect the operator from chemicals exposure
Thermo-mechanical	• The die surface can be analyzed • Top of the package including potential defects in the passivation, voids in epoxy, and uncured epoxy can be examined	• Electrical testing not possible because bond wires are destroyed • Potential for destroying the entire device • Package must be exposed to extremely high temperature, near 500°C • Only appropriate for packages with gold eutectic die attachment, and not suitable for epoxy attachment

(*Continued*)

Petitioner Samsung Ex-1055, 0306

Table 6.1 Comparison of Various Decapsulation Methods [7,8,10] (*Continued*)

Decapsulation Method	Advantages	Disadvantages
Mechanical	• Slow removal of the molding compound allows for the examination of the area of interest • Suitable for the analysis of leakage failure caused by a material in the molding compound shorting the adjacent wire bonds	• Physical damage to the die surface may occur preventing surface analysis • Wire damage prevents electrical testing • Relatively slow process
Plasma etching	• Highly effective method, even in cases where acid etching does not work • Gentle method, can be applied as to acid sensitive materials • Safe method, no chemicals involved • Clean method	• Decapsulation time is too long, up to several hours • Potential for artifact failures that can be mistaken as a real failure mode

Petitioner Samsung Ex-1055, 0307

encapsulant until the die is exposed. The temperatures at which chemical etching is performed range from 85°C to 140°C for nitric acid, and 140°C to 240°C if sulfuric acid is used. After etching, the device is rinsed. In case of etching with sulfuric acid, the device is rinsed with large amounts of de-ionized water, followed by acetone, and finally dried with nitrogen or dry air. In chemical etching with nitric acid, the device is rinsed with acetone only, and then dried. The nitric acid when diluted is highly reactive with aluminum metallization, sometimes even used as metal etchant in wafer fabrication, and therefore any contact with water must be avoided during the rinsing process [7].

During chemical etching, heating accelerates the reaction of the plastic encapsulant decomposition and speeds the decapsulation process; however, it also removes contamination from the surface of the die, reducing the effectiveness of subsequent chemical analysis. Another chemical decapsulation method is jet etching which employs automated equipment known as the jet etcher. The acid jet hits the top of the package until the die is exposed. During jet etching, the package is generally covered with a rubber mask except for the section being etched. Jet etching is a faster approach than the manual drip methods, and is usually implemented for large scale decapsulation, where the time required to open each device becomes critical. It is also a more controlled, efficient, and cleaner process.

Automated equipment for chemical etching using acid injection techniques and fluoroelastomer gaskets (or masks) has been available for many years. Such equipment has allowed volume manufacturers to expose die and lead-frame structures in a few seconds, and in a very efficient and cost effective manner. A growing number of lower volume manufacturers and system integrators are employing automated etching equipment to reduce labor overhead and gain repeatability of results.

Two prevalent technologies of automated acid decapsulation are available. The first technology uses fresh acid from standard bottles. The temperature is elevated in a heat exchanger and the encapsulant material is decapsulated. The resultant waste acid/residue mixture is then collected in standard bottles for disposal. The advantages are repeatable results and the cleanest possible etch. The disadvantage is a slightly higher acid consumption for medium volume runs.

The second technology involves continuously recycling a heated bath of acid through the device cavity. The advantage is slightly lower acid consumption for medium volume runs. However, this advantage is lost for low volume runs due to the fixed 40 milliliter fill amount required. The disadvantages lie in the introduction of byproduct contaminants and the

Petitioner Samsung Ex-1055, 0308

progressively slower etch rate over usage which is difficult to control by typical operators. Longer runs require bath refills.

Programmability of the multi-controller in the decapsulator allows regulation of the acid used, etch temperature, heat-up time, etch time, acid volume, and rinse time. Programmability enables a sequence best suited for a particular device type to be used and, in so doing, provides the accuracy and reproducibility needed for quality assurance testing and failure analysis. Temperature equilibrium and the use of fresh acid for both etching and rinsing cycles ensures absolute reproducibility in plastic removal, leaving the exposed die contamination free and ready for subsequent inspection and testing. The etching and rinsing cycles are performed in an inert atmosphere that eliminates the possibility of device corrosion, which will occur in the presence of any reactive gases, especially water vapor and oxygen.

While 90% red fuming nitric acid is the most commonly used etchant, certain encapsulants are resistant to and cannot be etched with nitric acid. Plastic ball-grid array (PBGA) and low-stress thermal encapsulants, used for transistor outline and some dynamic random access memory devices, fall into this category. These encapsulants can be etched with high purity or fuming varieties of sulfuric acid at relatively elevated temperatures of up to 240°C. This high temperature is effective at removing almost all commonly used encapsulants, including epoxy and urethane-based molding compounds.

Packages including dual in-line, plastic-leaded chip carrier (PLCC), quad flatpack (QFP), and small-outline, can be decapsulated with fuming nitric acid at lower temperatures such as 85°C. A chemical laboratory equipped with fume hoods and chemical containment is required. Many medium to large size packages can still be opened using the eye dropper on a hot plate method.

The manual method subjects the die to multiple temperature shock cycles, sacrifices lead-frame integrity, and destroys solder balls. As such, it typically renders the device electrically non-functional. Figures 6.1 and 6.2 illustrate a decapsulator and a decapsulated package, respectively.

In the thermo-mechanical decapsulation method, the leads are first bent 90° to 180° to make the bottom of the package accessible for sanding. The package bottom is sanded until the die-paddle and lead-frame are exposed. The package is then exposed to a high temperature of about 500°C for 20–30 seconds. Because of the induced thermo-mechanical stresses, the die separates from the epoxy molding compound, and can be lifted away for defect and failure analysis [7]. Since this method does not

Petitioner Samsung Ex-1055, 0309

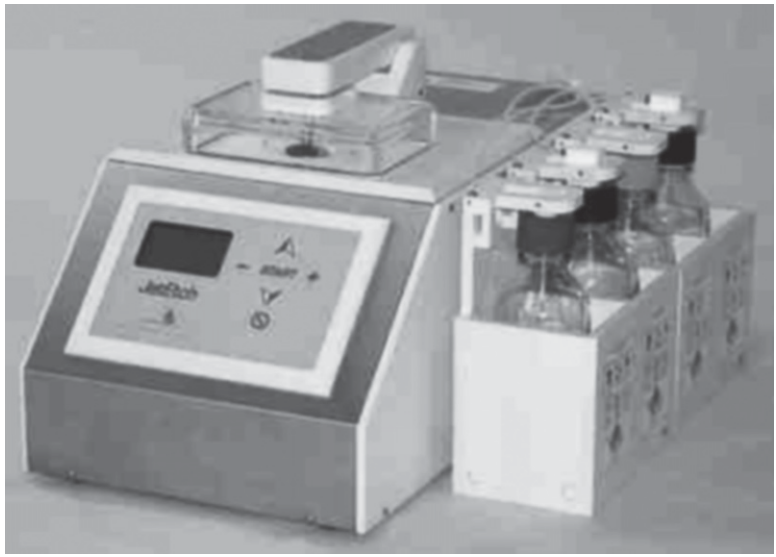


Figure 6.1 An automated acid decapsulator (JetEtch model 250 by Nisene Technology Group). *Source*: http://www.calce.umd.edu/general/Facilities/decap.htm.

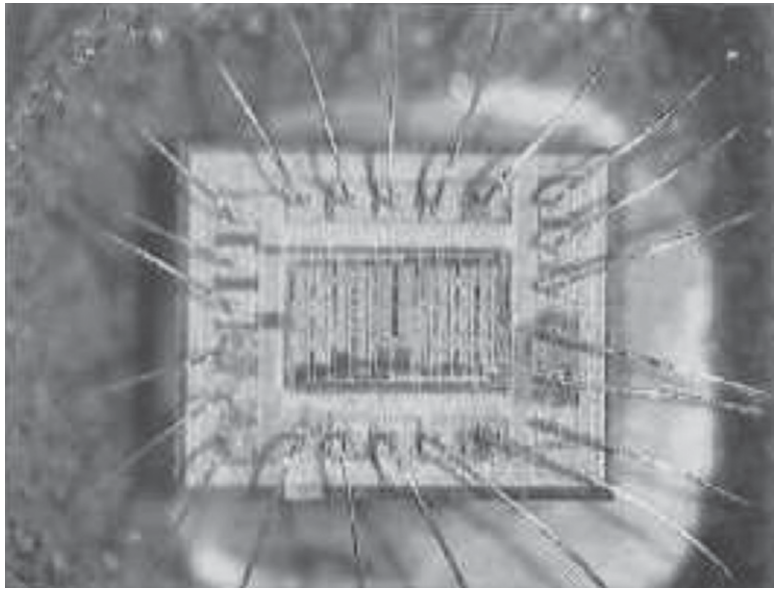


Figure 6.2 Decapsulated package.

Petitioner Samsung Ex-1055, 0310

involve contact with any chemicals that react with contaminants at the die surface, it is typically used to identify failures that may be caused by metallization corrosion. The primary disadvantage of this method is the loss of electrical continuity that may occur due to the damage or removal of the wires.

The mechanical decapsulation method involves grinding the molding compound to reach a specific area of interest for examination. It is specifically useful for analyzing leakage failures in plastic packages such as in PBGAs where a material in the molding compound shorted the adjacent wire bonds causing leakage failure [10]. In leakage failure analysis, the electrical data can be used to isolate the defect location by identifying the specific signal with lower resistance. In this method, no heating or chemicals are involved; however, physical damage to the die surface and wire damage prevent further surface analysis and electrical testing of the device.

In plasma etching decapsulation method, low temperature plasmas (ionized gas) of electrically excited oxygen are emitted on the plastic encapsulants and turning the material into ash which is then removed. In this method, many parts can be processed simultaneously, but the process takes many hours and extensive operator intervention. The best uses of plasma etching either occur where acid etching cannot remove the encapsulant or as a final treatment for acid sensitive polyimide die coat or lead frame materials. The plasma treatment has proven valuable because of its selectivity, gentleness, cleanliness, and safety [8]. The overall decapsulation time is generally too long for routine use and limits the application of plasma etching to the more critical failure analysis studies. Great care must also be taken to avoid artifact failure, which may be mistaken as a real failure mode. It is advantageous to mechanically remove as much material as possible above the area to be investigated prior to plasma processing.

6.1.3.3 Internal Examination

Internal examinations after package decapsulation can be performed using a variety of failure analysis techniques. These techniques are selected according to the possible location of the failure in the package, the expected size of the failure to be examined, and other factors. The failure analysis techniques used for internal examination may include optical microscopy, electron microscopy, infrared microscopy, and X-ray fluorescence (XRF) spectroscopy.

Petitioner Samsung Ex-1055, 0311

6.1.3.4 Selective Layer Removal

Some defects, such as evidence of electrical overstress or pinholes in insulating films that can lead to short circuits, may be sub-surface and hence not visible. This necessitates individually removing the various component layers on the semiconductor device structure. The two commonly used layer removal methods are wet etching and dry etching [11].

Oxides and metallizations are usually removed using wet chemical etching. Nitride passivation layers are removed by etching with fluorine containing plasmas or argon ion milling.

6.1.3.5 Locating the Failure Site and Identifying the Failure Mechanism

There are many possible techniques to locate a failure site. The most important step in failure analysis is identifying the cause of the failure and its mechanism. It is performed by fully considering the location of the failure, its morphology and history, and the conditions of the package's manufacture and application. For example, a crack in the plastic encapsulant can be identified from non-destructive visual examination. Further testing including X-ray microscopy and SAM can reveal internal delamination and cracks. Upon determining the failure site and mode, the failure mechanism can then be investigated based on the manufacturing and application history and conditions. A possible failure mechanism in this case is popcorning (cracking) during manufacturing (i.e., solder reflow process) due to high temperature and vapor pressure.

6.1.3.6 Simulation Testing

In some cases, failures such as large cracks, voids, or wire debonding (opens) are immediately evident. At other times, however, direct evidence of the mechanism is destroyed either by the failure itself or by the subsequent analysis. These cases require simulation testing to reproduce the observed failures. The encapsulated microcircuit can be stressed to failure using environmental facilities or electrical loading logically related to in-use failure. Environmental conditions such as elevated temperature, temperature cycling, and elevated relative humidity can be selected.

Petitioner Samsung Ex-1055, 0312

The following techniques applied to defect and failure analysis of plastic-encapsulated microelectronic packages will be discussed in the next sections:

- optical microscopy;
- scanning acoustic microscopy;
- X-ray microscopy;
- X-ray fluorescence spectroscopy;
- electron microscopy;
- atomic force microscopy; and
- infrared microscopy.

6.2 Optical Microscopy

Optical microscopy is a commonly used tool for failure analysis in various levels of packages. It is considered one of the most basic inspection techniques. Optical microscopes are generally inexpensive, convenient, and easy to use. Since the majority of semiconductor specimens are opaque, all of the microscopes employed are metallurgical microscopes meaning that they are equipped for through-the-lens, reflected illumination.

Optical microscopy consists mainly of a light-illuminating system and an eyepiece system. The light-illuminating system determines the objective magnification, numerical aperture, resolution, depth, and curvature of field. The eyepiece system consists of selectable magnifications. A Zeiss optical microscope is shown in Fig. 6.3.

Specimens can be examined in reflected light, or transmitted light if the specimen is made of transparent material. Optical microscopy techniques include bright field, dark field, phase contrast, differential interference contrast (DIC), polarized light, and others [12].

In comparison with electron and other microscopes, optical microscopes work without requiring a high vacuum or a conducting material. The disadvantage is that resolution is limited by the wavelength of visible light. Resolution, d, is related to wavelength, λ, by

$$d = \frac{\lambda}{2A} \tag{6.1}$$

where A is the numerical aperture.

Petitioner Samsung Ex-1055, 0313



Figure 6.3 Zeiss optical microscope.

The various optical microscopy techniques are summarized below.

Bright-Field. This basic inspection technique is best suited for observing smooth, reflective surfaces (e.g., oxide coated silicon, metallurgically polished surfaces, etc.). This technique does not work very well when trying to detect small particles and transparent contamination films. In addition, small changes in topography may not be easily detected (less than 2.0 μm). Figure 6.4 shows the bright-field image of a sample.

Dark-Field. This technique is readily available, but not commonly used and involves a modification to the bright-field illumination path by the placement of a dark-field annulus in the central portion of the objective such that the central rays present in bright-field are now blocked. This, plus a special 360° annular mirror built into the objective, allows an oblique illumination pattern to be incident on the specimen. The limitations of

Petitioner Samsung Ex-1055, 0314

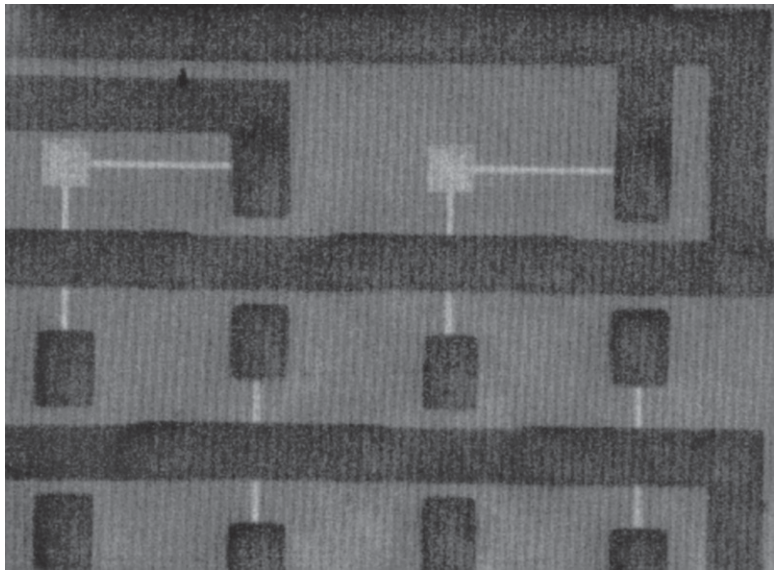


Figure 6.4 Bright-field image.

bright-field are overcome with dark-field; thus, particles, scratches, pinholes, and other defects are easily detected in smooth semiconductor and metallurgical sections. The oblique illumination takes advantage of a feature's ability to scatter, diffract, or refract light. Figure 6.5 shows the dark-field image of a sample.

Polarized Light. This technique takes advantage of the anisotropic optical characteristics of some specimens. Such samples have varying refractive indices that depend on the angle of illumination. To observe a specimen using polarized light technique, two special filters must be inserted in the microscope. The first one, called the polarizer, is inserted in the light path while the second one, called the analyzer, is inserted into the optical pathway between the objective rear aperture and the observation tubes or camera portray [13]. Samples with low contrast can be enhanced (e.g., inspection of silver dendrites on a ceramic substrate). Grain boundaries and certain intermetallic phases in metallurgical sections can be more easily observed (e.g., gold/aluminum intermetallic under ball bonds).

Differential Interference Contrast. This technique produces an image with topographical information. In a DIC optical microscope, the beam from the light source passes through a polarizer filter, then through a special prism, known as "Nomarski–Wollaston prism," and finally through

Petitioner Samsung Ex-1055, 0315

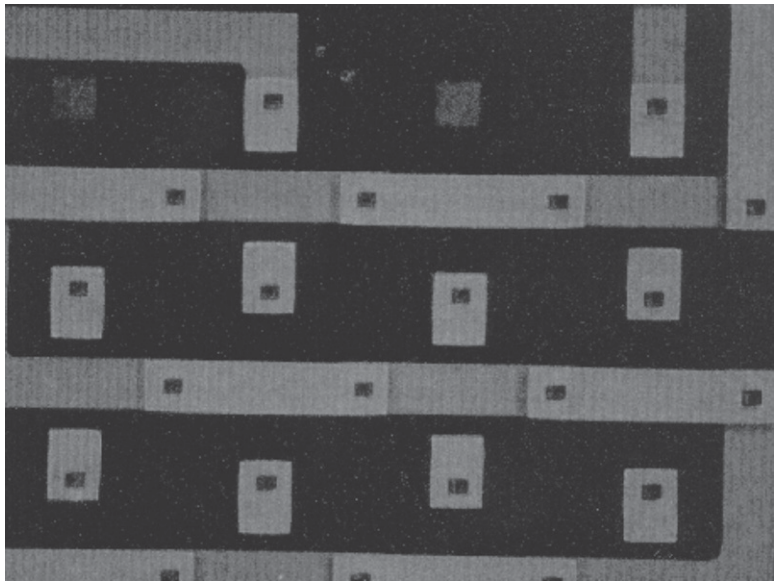


Figure 6.5 Dark-field image.

a condenser lens after which the separated polarized light beams enter the specimen at slightly different distances (0.2 μm apart). If the refractive indexes of the two adjacent points differ, then the two beams refract differently, and show different brightness on the DIC image leading to a perception of height.

Fluorescence Microscopy. This technique uses a high energy light source (e.g., mercury or xenon), which is filtered using a band pass filter (e.g., 390–489 nm). This near UV light strikes the sample causing some atoms to become excited which eventually results in the emission of light of a longer wavelength (visible). Many organic compounds will have a specific transmittance character that may be identified. Prime application of this technique is fluorescence dye penetration in which an epoxy bearing the dye is forced into a specimen and examined after curing. Cross-sections yield accurate records of defect paths through which the dye passes (e.g., internal cracks in plastic packages or delaminations at plastic-to-metal interfaces).

6.3 Scanning Acoustic Microscopy

Assembly-related packaging defects in plastic-encapsulated integrated circuits or other encapsulated electronic components are a major source of

Petitioner Samsung Ex-1055, 0316

reliability problems. Although certain applications have relatively stringent requirements, the typical defects may include molding compound delamination at the interface with the lead-frame, die, or die-paddle, molding compound cracks, die-attach delamination, die tilt, and voids in the molding compound. Each of these defects can be non-destructively detected and viewed using SAM also known as scanning acoustic tomography or acoustic micro-imaging (AMI). The SAM technology is based on the reflection and transmission characteristics of ultrasound waves in various materials.

SAM can be used to inspect multiple devices in order to screen out defective units prior to use or to ensure the output quality of a molding process in line. SAM techniques can respond to a full range of needs, from production volume screening to detailed laboratory defect and failure analysis. It is important to fully characterize the defect and understand the failure mode. Used properly, SAM can provide valuable data not available by any other technique. Moreover, since it is non-destructive, components are not sacrificed. For reliability studies, the growth rate of a flaw can be monitored as the component cycles through environmental stresses or through its normal operating life.

SAM is performed using two main microscopes: the scanning laser acoustic microscope (SLAM™) and the C-mode scanning acoustic microscope (C-SAM®). Both are routinely used to evaluate plastic-encapsulated devices and have been codified into standards [14,15].

6.3.1 Imaging Modes

A large variety of imaging modes are possible in SAM as shown in Fig. 6.6. AMI modes include A-scan, B-scan, C-mode, bulk-scan, quantitative B-scan analysis mode (Q-BAM™), 3D time-of-flight (TOF), through-transmission or THRU-Scan™, multi-scan, surface-scan, 3D image of a die stack package or 3V™, and tray-scan.

6.3.2 C-Mode Scanning Acoustic Microscope

C-SAM® (a registered trademark of Sonoscan Inc.) is useful for defining the exact nature of flaws in plastic-encapsulated microelectronic package. Unlike SLAM™, which images all depths simultaneously, C-SAM® can be used depth-selectively (www.sonoscan.com). The basic operating principles of C-SAM® are illustrated in Fig. 6.7 [16]. A focused spot of ultrasound is generated by an acoustic lens assembly at frequencies typically ranging from 10 to 100 MHz. The angle of the rays from the lens is generally kept

Petitioner Samsung Ex-1055, 0317

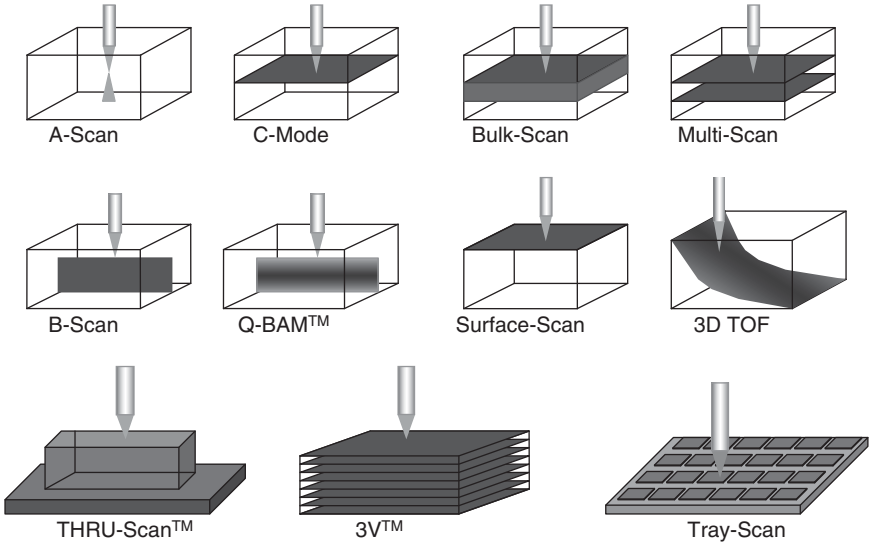


Figure 6.6 Acoustic imaging modes (www.sonoscan.com).
Q-BAM: Quantitative B-scan analysis mode; TOF: Time-of-flight.

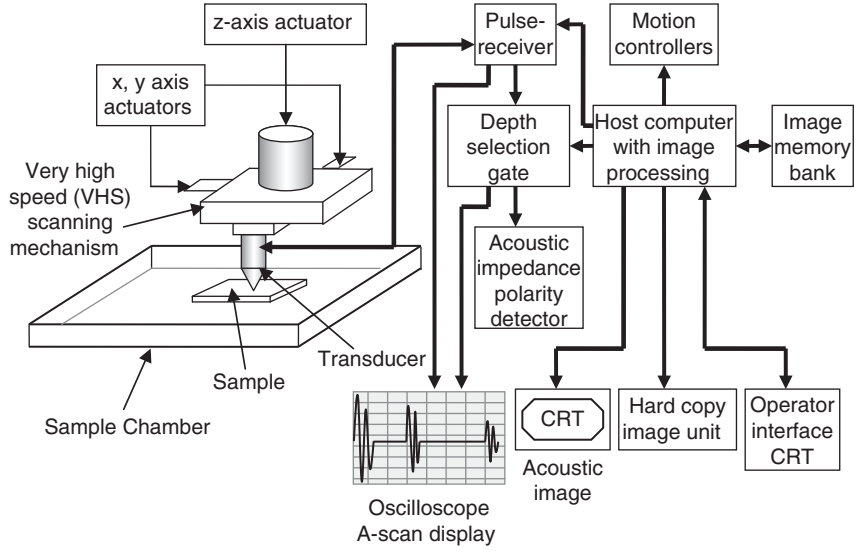


Figure 6.7 Block diagram of a C-mode scanning acoustic microscope (C-SAM®).

small so that the incident ultrasound does not exceed the critical angle of refraction between the fluid coupling and the solid sample. C-SAM® introduces a very short acoustic pulse into the sample; return echoes are produced at the sample surface and at specific interfaces within the part. The echo

Petitioner Samsung Ex-1055, 0318

return time is a function of the distance from the interface to the transducer and the speed of sound in the sample. An oscilloscope display of the echo pattern, known as an A-scan, shows the echo levels and their time-distance relationships with the sample surface (Fig. 6.8). An electronic gate "opens" for a specific time duration allowing only the echoes from a specific depth level to be imaged while excluding echoes from all other levels. The gated echo signal brightness modulates a cathode-ray tube (CRT) that is synchronized with the transducer position. To make an acoustic image, a mechanical scanner moves the transducer over the sample and produces the data in tens of seconds or less depending on the field of view.

With C-SAM®, several distinct imaging techniques can be chosen to analyze a sample; the most common is the C-mode scan. In C-mode, a focused transducer is scanned over the planar area of interest and the lens is focused to some depth, as illustrated in Fig. 6.9. The echoes arising from that depth are electronically gated for display. The electronic gate may be adjusted to be either narrow or wide, and the depth information content of the image will correspond to the thin or thick "slice." For example, in a plastic-encapsulated integrated circuit, a narrow gate can produce an isolated image of the die surface alone, whereas a wider gate can image the die surface, the perimeter of the paddle, and the lead-frame simultaneously. In C-SAM®, the gate can be used to non-destructively micro-section the sample. By changing the configuration of the C-SAM® instrumentation, other imaging modes that emphasize particular structural features and defects can be accessed. These are briefly described below. Figure 6.10 shows a picture of a die surface obtained using C-SAM®.

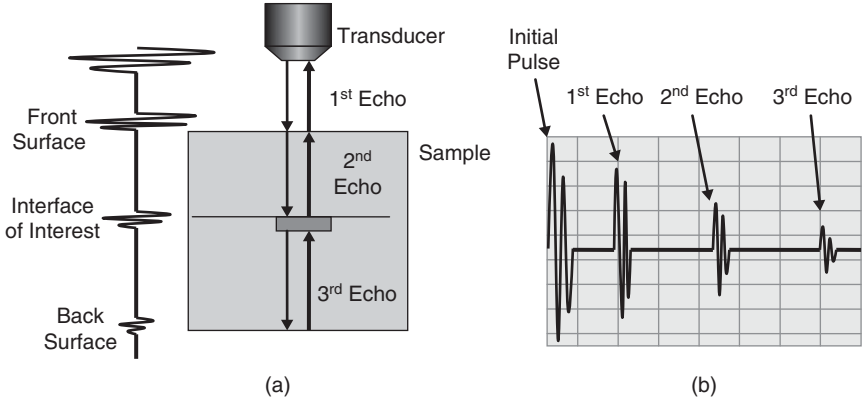


Figure 6.8 A-scan imaging: (a) echo levels and time–distance relationship with the sample surface; (b) typical A-scan oscilloscope display pattern (http://www.sonix.com).

Petitioner Samsung Ex-1055, 0319

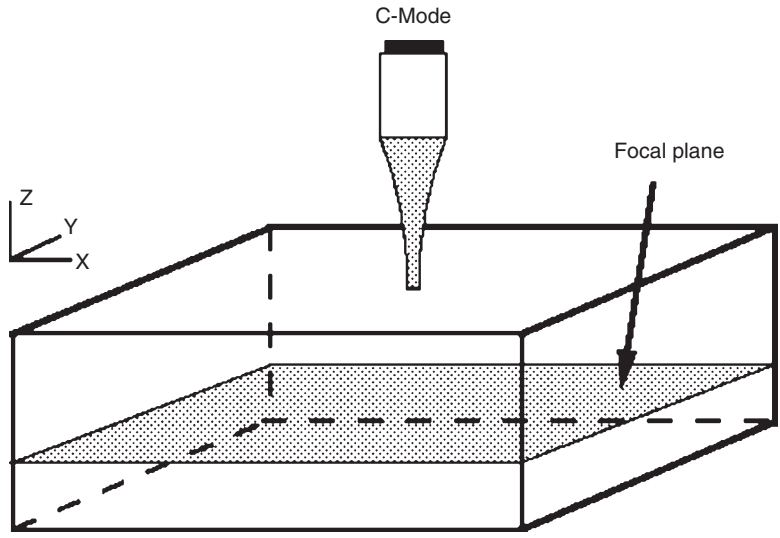


Figure 6.9 Schematic of a C-mode acoustic scan.

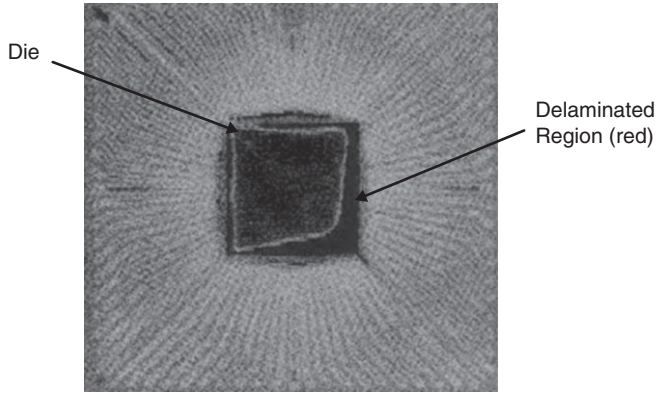


Figure 6.10 Image of a die surface using C-SAM®.

The gray-scale image on the CRT can be converted into false color for contrast enhancement of the amplitude information. The images can also be color-coded with echo polarity or phase information [17]. Positive echoes, which arise from reflections off a higher acoustic impedance interface, are displayed in a gray scale with one color scheme, while negative echoes, from reflections off lower acoustic impedance interfaces, are displayed in a different color scheme. The acoustic impedance, Z, is a material characteristic related to acoustic wave propagation. In particular,

Petitioner Samsung Ex-1055, 0320

$$Z = \rho v_{sound} \tag{6.2}$$

where ρ is the mass density and v_{sound} is the velocity of sound for the material through which the wave is propagating. The velocities of sound for typical materials can be found in Selfridge [18]. When an acoustic wave is incident upon a boundary between two materials, part of the wave is reflected and part is transmitted as shown in Fig. 6.11. If the interface is delaminated, the incident wave is fully reflected. Typical acoustic impedance values for common materials are shown in Table 6.2.

Depending on the relative magnitudes of Z_1 and Z_2, the reflected wave can carry positive or negative polarities. In C-SAM® operation, the A-scan mode oscilloscope trace displays the echo pattern of interfaces encountered by the acoustic pulse. Each echo has a characteristic amplitude and polarity, depending on the nature of the corresponding interface.

Focused acoustic wave transducers have limited depths of field over which accurate data can be obtained. Outside of this area, the apparent magnitude of an echo can be lower due to defocusing. Moreover, the shape

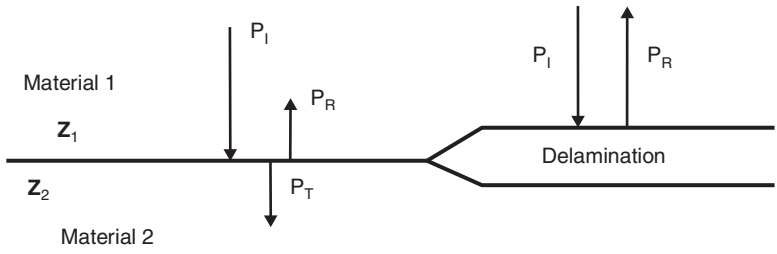


Figure 6.11 Acoustic wave reflectivity at the interface of two materials.

Table 6.2 Typical Acoustic Impedance Values

Material	Acoustic Impedance (10^6 rayl) or (10^6 kg s^{-1} m^{-2})
Air (vacuum)	0
Water	1.5
Plastic	2–3.5
Glass	15
Aluminum	17
Silicon	20
Copper	42
Alumina (depends on porosity)	21–45
Tungsten	104

Petitioner Samsung Ex-1055, 0321

of the echo might be distorted, since the angular rays may not all return to the transducer at the correct time. Therefore, polarity data might not be valid.

Acoustic impedance polarity detection (AIPD) in a sample allows quantitative determination of the nature of internal interfaces. For example, the echo amplitude from a plastic/silicon interface (good bond) is close to that from a plastic/air-gap interface (delamination), but the echoes are 180° out of phase. This technique allows the operator to determine whether a material is interfaced with a "harder" or "softer" material on the other side (strictly speaking, acoustic impedance is neither hard nor soft, but this analogy is appropriate in some cases.) The technique of displaying a unified image, containing both amplitude and polarity information simultaneously [17], has an important role in integrated circuit defect detection.

Bulk-scanning is performed by positioning the electronic gate or window between the internal interfaces of the plastic-encapsulated package where the material texture, non-homogeneities, and voids can be detected. For example, if the electronic gate is placed behind the top surface echo of an integrated circuit but in front of the lead-frame echo, it is easy to identify agglomerations of filler material and voids in the encapsulant. AIPD is needed to differentiate filler from void spaces, since both produce large amplitude echoes.

Through-transmission scan or THRU-Scan™ images are produced by recording the ultrasonic energy transmission through the entire component, instead of only that reflected from interfaces. In this mode, which can be accomplished by C-SAM® or SLAM™ (Fig. 6.12), defects anywhere in

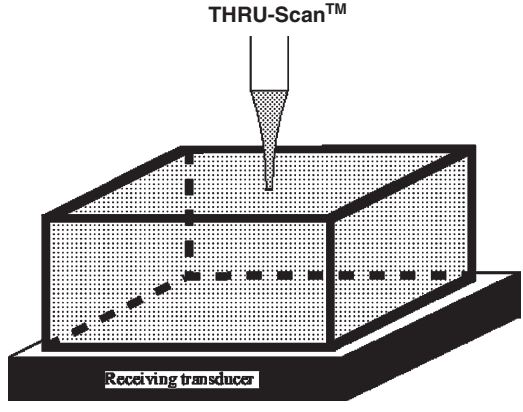


Figure 6.12 Schematic of a through-transmission scan.

Petitioner Samsung Ex-1055, 0322

the part will block the ultrasound and cause dark features to appear in the image. With C-SAM®, the transmission scan or THRU-Scan™ (a trademark of Sonoscan Inc.) mode requires ultrasound transducers placed on both sides of the sample, one for producing the ultrasound and the other for receiving it. THRU-Scan™ can be used to determine with only one scan whether a defect exists in a sample. THRU-Scan™ can also be of great help in confirming reflection-mode data; in particular, some highly absorbing samples can distort the ultrasonic pulse shape so severely that AIPD is difficult to use. Furthermore, with THRU-Scan™, the presence of delamination does not affect echo polarity.

The major difference between SLAM™ and C-SAM® with regard to THRU-Scan™ is the speed of imaging. C-SAM® requires tens of seconds to mechanically scan the transducer over the area of interest, whereas SLAM™ produces 30 images per second. Therefore, SLAM™ is generally used for higher speed inspection, such as is needed for on-line screening applications.

While in the reflection-mode techniques echo amplitudes are recorded as corresponding gray scales, in the TOF scan, the arrival time of the echo is converted to a gray scale (see Fig. 6.13). In this mode, the echo amplitude has no bearing on the gray scale, except that it must be large enough to be detected. This type of image is useful for a general overview of the depth of the defect or failure feature such as a crack. Although the image

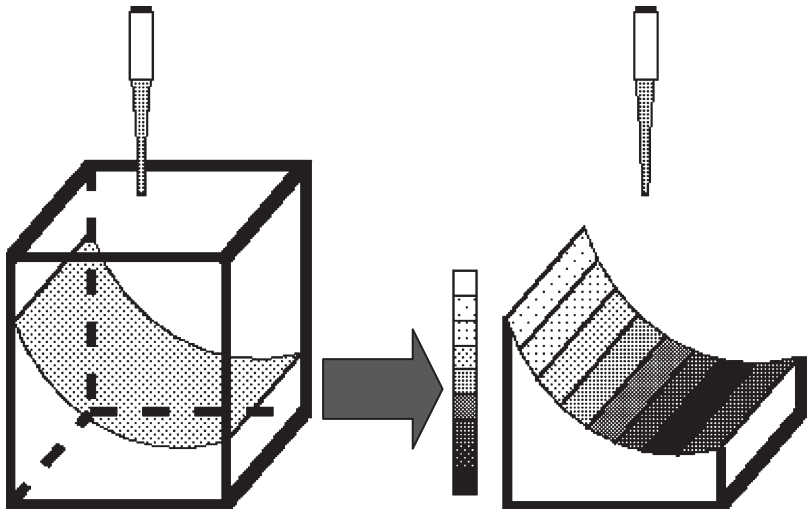


Figure 6.13 Time-of-flight scan where the arrival time of the echo is converted to gray scale.

Petitioner Samsung Ex-1055, 0323

may appear visually similar to a conventional C-mode image, the information content is quite different. When projected into three dimensions, the TOF image gives a perspective of the contour of the internal interface. TOF scans are useful for profiling cracks in plastic packaged integrated circuits. The crack profile is produced by 3D projection of the arrival times of the crack reflection echoes at different depth levels as illustrated in Fig. 6.14.

In transmission and TOF scans, the planar location of each pixel on the CRT corresponds to a planar position on the sample. However, in the B-scan mode, the planar CRT pixels correspond to one dimension of the plane and the depth position in the sample. B-scan is analogous to the technology employed by the medical ultrasound scanners used in hospitals. In conventional B-scan, a vertical cross-sectional image is produced of the sample along any line across it, just as if the sample were cut open with a saw. The image is made by scanning the transducer across one dimension of the plane, recording echoes that return from all depths, and displaying these on the vertical axis of the CRT. Unfortunately, in conventional B-scan the echoes are not in focus at all depths due to the fixed transducer lens focal position. Figure 6.15 illustrates a B-scan cross-section of a sample in which the dark shading represents the limited focal zone of the transducer. In Q-BAM™, a trademark of Sonoscan Inc., however, the transducer is also indexed in the depth direction throughout the entire thickness of the component in order to ensure continuous uniform focus. The Q-BAM™ cross-section is illustrated in Fig. 6.16. In a Q-BAM™ image, the echo TOF information is converted to metric depth data so that the operator can see a unified display of the cross-section in the one dimension of the plane and depth plane, along with its planar location.

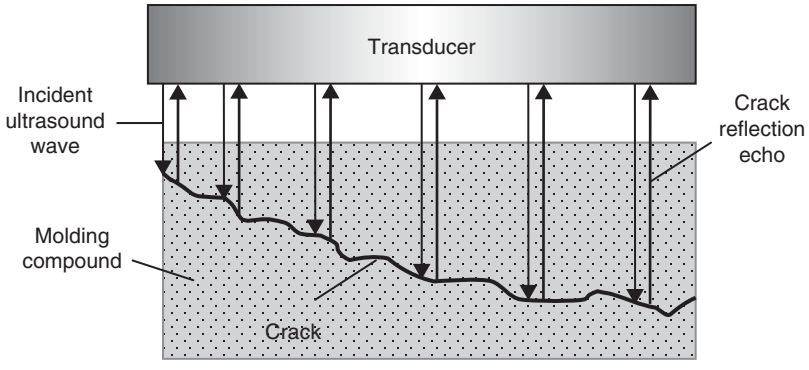


Figure 6.14 Crack profiling using time-of-flight scanning.

Petitioner Samsung Ex-1055, 0324

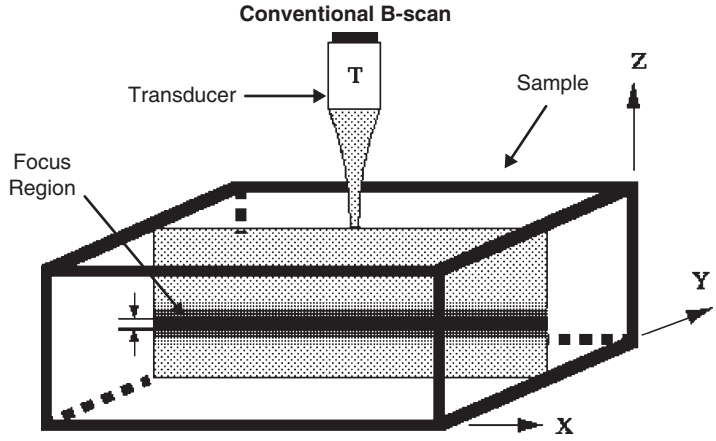


Figure 6.15 B-scan cross-section of a typical sample; the dark shading represents the focal zone of the transducer wherein the acoustic data are most accurate.

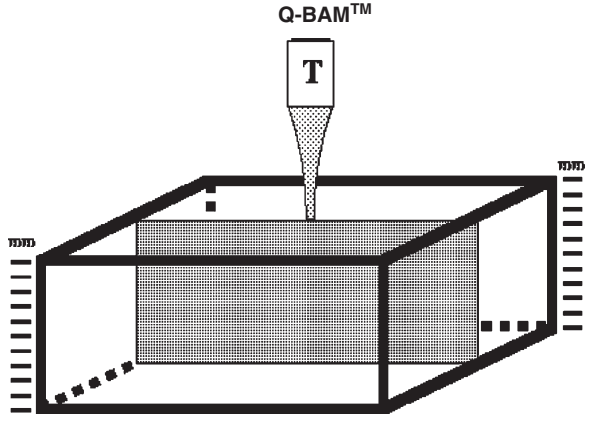


Figure 6.16 Quantitative B-scan analysis with accurate depth information over the entire depth range.

6.3.3 Scanning Laser Acoustic Microscope

Scanning laser acoustic microscopy, also a trademark of Sonoscan Inc., is a through-transmission technique operating over a frequency range of 10–500 MHz ([16], www.sonoscan.com); however, due to the absorption of ultrasound by polymers, the highest acoustic frequencies are not needed for inspecting encapsulated integrated circuits. With SLAM™, a plane wave of continuous ultrasound is introduced to one side of the sample and travels through it to the opposite side. Variations in the ultrasound wave

Petitioner Samsung Ex-1055, 0325

pattern due to differential attenuation in the sample are detected by a scanning laser beam. Since high-frequency ultrasound does not travel in a vacuum or in air, flaws characterized by air gaps block transmission to the detector in the affected area and appear dark in the acoustic image. The true real-time imaging capabilities of SLAM™ (typically 30 pictures/second) make it a useful technique for production line, high-volume screening.

The basic operating principle of SLAM™ is illustrated in Fig. 6.17. Ultrasound illuminates the area of a sample to be inspected. The ultrasound passing through the sample causes tiny perturbations of a mirrored surface on a plastic cover slip mirror. A focused laser beam scans the surface of the plastic block and reads off the acoustic levels. SLAM™ images the entire sample thickness simultaneously. As a by-product of laser scanning, the SLAM™ can also produce optical images. SLAM™ produces images and data in several different modes. The most common, "shadowgraph" mode, images the structure throughout the thickness of the sample; this allows the distinct advantage of simultaneous viewing of defects anywhere in the sample, like X-ray radiography. In situations requiring focus on one specific plane, holographic reconstruction of the SLAM™ data can be employed [16]. In the other mode, "interferogram" mode, "fringes" appear on the CRT acoustic image display, related to the scattering of ultrasound waves and velocity variations in the sample. Figure 6.18 shows example of fringe patterns. Scrambled fringe patterns, as shown in Fig. 6.18(a), are indicative of porous materials in which strong wave scattering occurs. Dense materials generally produce a more distinct fringe patterns, as shown in Fig. 6.18(b), with minimal scattering [19].

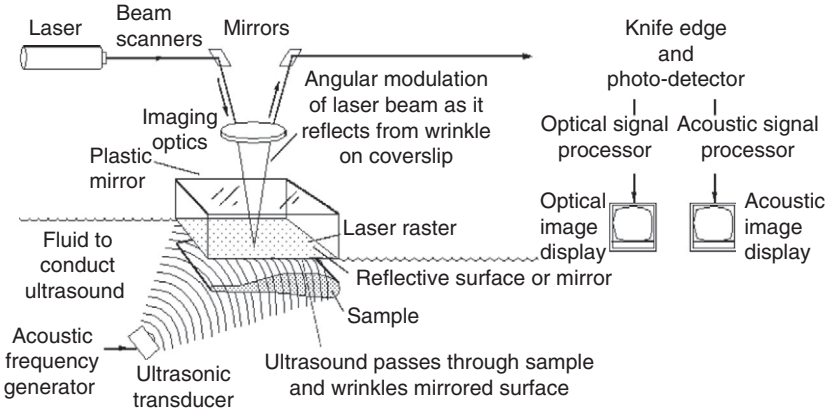


Figure 6.17 Block diagram of the scanning laser acoustic microscope (SLAM™).

Petitioner Samsung Ex-1055, 0326

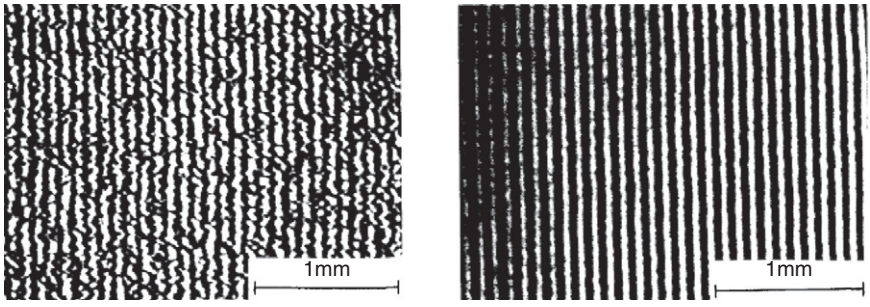


Figure 6.18 Acoustic fringes produced by (a) a porous material and (b) a dense material (© 1991 IEEE) [19].

In addition to acoustic image capability, an optical image is produced by the direct laser-scanned illumination of the sample surface. The optical image serves as an operator reference for landmark information, artifacts, and positioning of the sample. With an auxiliary lens, the SLAM™ optical mode can be utilized as a high resolution optical scanning laser microscope.

With SLAM™, the brightness of the image corresponds to the acoustic transmission level. By removing the sample and restoring the image brightness level with a calibrated electronic attenuator, precise insertion loss data about the material composition can be obtained. The attenuation and velocity data can reveal information about the modulus of elasticity, void population, filler aggregation, and the degree of epoxy cure. In particular, the attenuation coefficient of the material can reflect the distribution of the encapsulation voids which are the scatterers of ultrasonic waves [19].

6.3.4 Case Studies

Several case studies are presented to demonstrate the application of AMI in plastic-encapsulated microelectronic packages.

6.3.4.1 C-mode Imaging of Delaminations in a 40-Pin PDIP

C-mode reflection images of a 40-pin plastic dual in-line package (PDIP) were made from the top surface; the transducer was focused at the die face.

Petitioner Samsung Ex-1055, 0327

The sample was then turned over, and the transducer was focused to the surface of the die-paddle. (Unfortunately, this text cannot reproduce the standard C-mode color display, so the figures present the data in various other ways.)

Figure 6.19(a) shows an amplitude image of the sample that presents the amplitudes of all echoes as brightness levels on the CRT, regardless of polarity. In this useful image all structures are revealed at the level of focus selected. This figure shows unusual brightness changes around the die and lead-frame, presumably due to delamination. Using AIPD, the echo polarity data can be distinguished. Figure 6.19(b) gives a delamination image that consists only of negative echoes. White features shown in this image are all disbonded from the molding compound. Figure 6.19(c) is a black-and-white unified display that electronically codes bonds as bright and disbonds as black. Figure 6.19(d) is a black-and-white unified display of the same sample as viewed from the back side. This PDIP has extensive delaminations on both sides of the lead-frame, as well as small delaminations on the die face and paddle area. Lead-frame delaminations of this type are frequently a result of poor control of the molding process [20].

6.3.4.2 Rapid Screening for Defects Using THRU-Scan™ Imaging

To accurately determine whether a plastic-encapsulated integrated circuit has assembly defects, three or more reflection-mode or C-mode scans are usually performed on each component. The series of scans typically includes the following:

- focusing from the top side of the integrated circuit to the die surface; if the lead-frame is also in focus, it is included in this scan for all top-side delaminations, voids, and cracks;
- while still viewing the integrated circuit from the top side, refocusing the transducer to the back side of the die (if possible) to search for die-attach delamination and voids;
- turning the part over and focusing from the back side to the die-paddle and lead-frame to search for additional anomalies; since this procedure is very time consuming, each component can be screened instead with the through-transmission modes of either SLAM™ or C-SAM®.

Petitioner Samsung Ex-1055, 0328

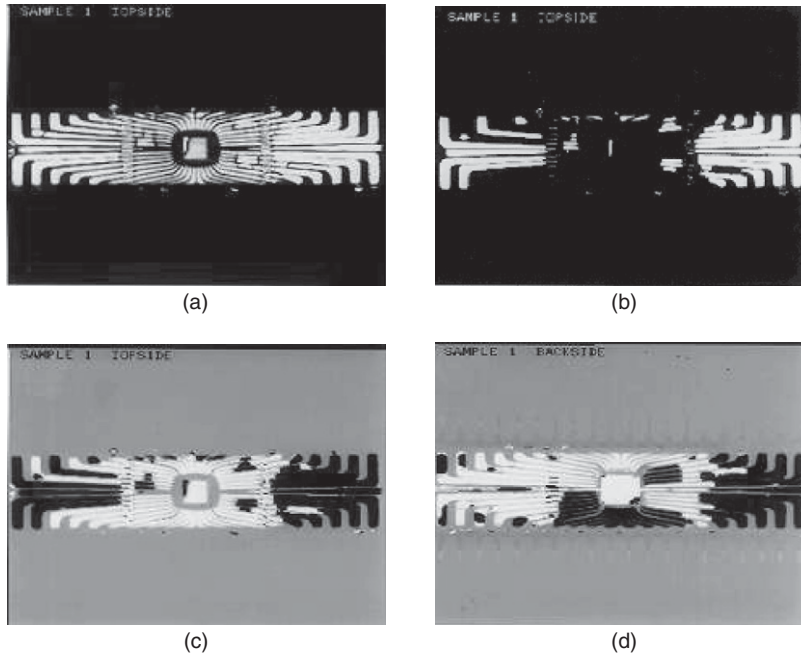


Figure 6.19 (a) Amplitude image of a sample presenting the amplitudes of all echoes (all white). (b) Delamination image consisting only of negative (disbond) echoes (in white). (c) A black and white unified display in which disbonds are dark. (d) A black and white unified display of the same sample as viewed from the back side.

In this case, just one scan reveals the presence of defects throughout the package. Although this does not necessarily determine the depth of the defect, it is quite accurate in the planar dimension.

Figure 6.20(a) is a through-transmission scan of a 72-pin plastic QFP that reveals a large acoustically opaque (black) central zone. Acoustic opacity results from a gap separation between layers of material, in this case caused by a popcorn crack. The reflection amplitude image of the same device is shown in Fig. 6.20(b). Although the polarity data are not shown here, the molding compound is delaminated from the die face. Turning over the part and scanning from the bottom surface in the same mode, Fig. 6.20(c) indicates delamination over the entire surface of the paddle as well. In addition, a dark circular region around the die-paddle is due to a crack that extends from the die-paddle out toward the package

Petitioner Samsung Ex-1055, 0329

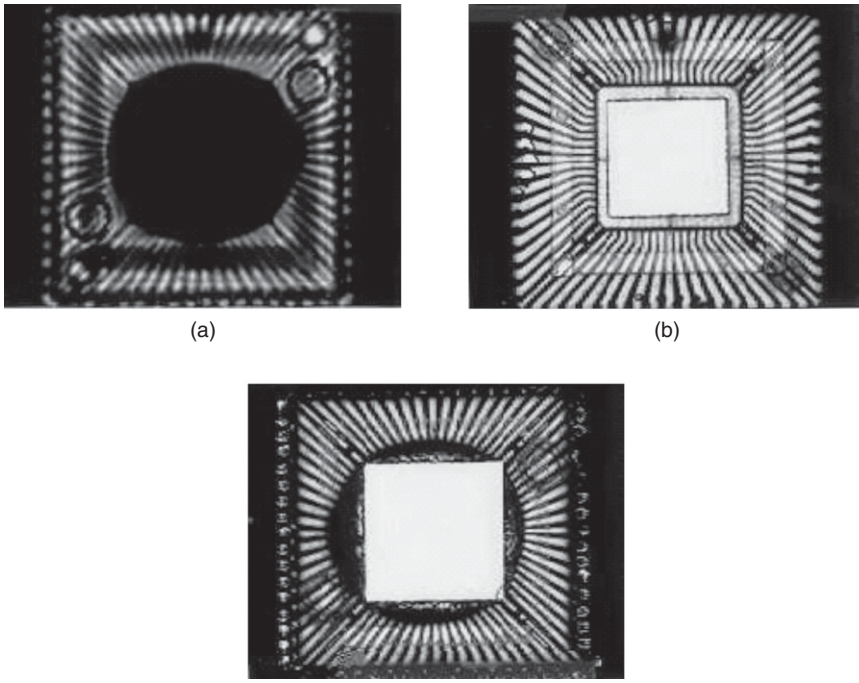


Figure 6.20 (a) Through-transmission scan from the top surface of a 72-pin plastic quad flatpack revealing a large acoustically opaque (black) zone. (b) The reflection amplitude image of the device. (c) Scan from the bottom surface revealing delamination over the entire surface of the paddle.

surface. The echoes from the crack interface occur earlier than those from the zone of focus, so the image of the lead-frame appears to be missing within the circular zone.

Figure 6.21(a) is a through-transmission scan of another plastic QFP that appears to have a problem in the die-paddle area. A close look at the image, which has been "saturated" or overexposed in the lead-frame area to bring out detail in the center, suggests that the dark delamination area is spatially restricted to the die itself. This indicates the problem may be associated with poor molding compound die adhesion or die attach delamintaion. To gain more certainty, top-side and back-side C-mode reflection scans were done; the amplitude images are shown in Fig. 6.21(b) and (c). Since the AIPD reveals no negative (delamintaion) signals, molding compound adhesion is good. Therefore, the die attach itself is the problem,

Petitioner Samsung Ex-1055, 0330

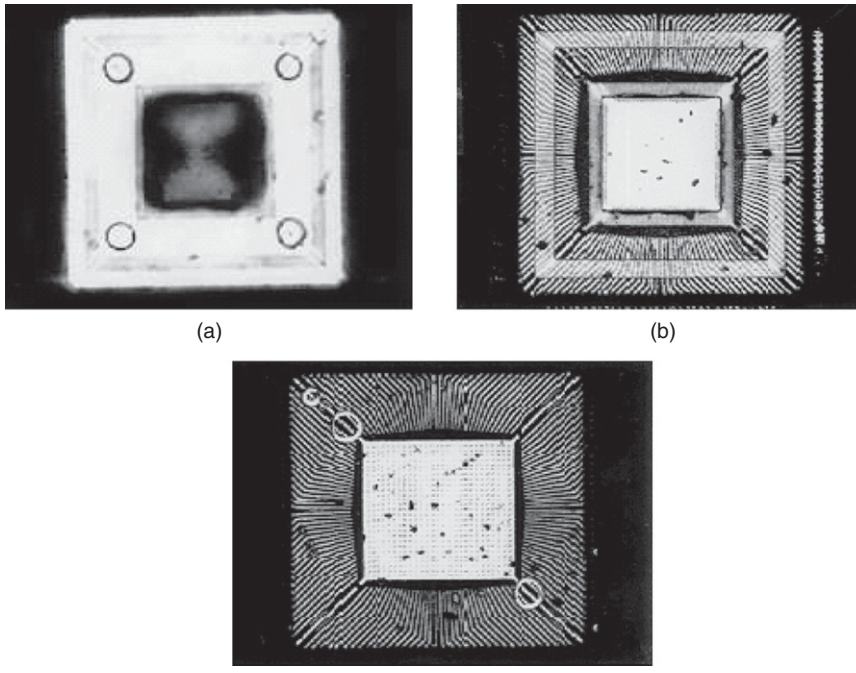


Figure 6.21 (a) A through-transmission scan of a plastic quad flatpack that has a problem in the die/paddle area. (b) Reflection image from the topside. (c) Reflection image from the back side.

since it is the only other interface in the integrated circuit that could block the ultrasound.

In addition to the die attach problem, there are a number of tiny black spots in all three images. These correspond to molding compound voids that typically arise during the molding process if the packing pressure profile is not adjusted properly [20]. Voids such as these threaten reliability most when they are located on and around the silicon chip or the wire bonds. Because of the broad distribution of voids and the poor die attach, in Fig. 6.18 this device could exhibit poor reliability such as poor thermal dissipation.

The series of images in Figs. 6.17 and 6.18 illustrate how THRU-Scan™ can be used to detect the presence of defects and determine their spatial extent. The reflection mode is then used complementarily to further analyze the defect types and locations. The THRU-Scan™ serves as a guide to distinguishing the good from bad parts and provides an image of the lateral dimensions of defects.

Petitioner Samsung Ex-1055, 0331

6.3.4.3 Non-destructive Cross-Section Analysis of Plastic-Encapsulated Devices Using Q-BAM™ and TOF Imaging

Cross-section analysis techniques generally involve decapsulation (a destructive procedure) and exposure of the inside of the package for defect and failure analysis. Acoustic imaging can offer a non-destructive cross-section analysis of the encapsulated package. C-mode acoustic images are not suitable for cross-section analysis because they are generally made of an internal horizontal plane of the sample, located at a given depth. To obtain more complete depth information, a systematic series of planar scans can be made at different depths, or a quantitative B-scan (one dimension of the horizontal plane and the depth) can be made at any position along another dimension of the plane.

Figure 6.22(a) shows a Q-BAM™ image of a US penny, imaged through the coin and focused at the rear surface. The cross-section is, of course, acoustic not metallurgical, and the analysis will be non-destructive. The top half of the CRT screen is a C-mode scan of the penny; the bottom half of the screen shows one dimension of the planar plane and the depth scan made across the coin's diameter. The bottom line of the C-mode image is also the precise location of the Q-BAM™ image; this gives the analyst a cross reference for the data. The bottom surface of the coin appears to have dimensional changes associated with the embossed pattern on the surface, as well as some overall distortion of the surface flatness. Thus, the Q-BAM™ can be used to search the depth of a component to accurately locate features with respect to the top and bottom surfaces. Figure 6.22(b) shows a 68-lead PLCC cross-sectioned midway through a dark spot in the die region. The Q-BAM™ reveals a molding compound void 0.6 mm above the die surface, which is far enough above the die to be considered safe. Note that the Q-BAM™ shows the height differences between internal structures. On either side of the Q-BAM™ image, a scale is calibrated by both echo arrival time and distance of travel, as determined by the velocity of sound in the material. Figure 6.22(c) shows another device, with a popcorn crack originating from the edges of the die-paddle and traveling toward the surface of the package. The crack intersects the surface on the left side, but not on the right. Figure 6.22(d) shows a significant degree of paddle shift. This is typically caused by a rapid increase in packing pressure after the mold filling step; the differential packing rates between the top and bottom zones of the lead-frame lead to this type of anomaly (as well as to wire sweep problems). In this figure, the die can be seen above the lead-frame, and a faint outline of the wires can be seen extending from the die surface to the lead-frame fingers.

Petitioner Samsung Ex-1055, 0332

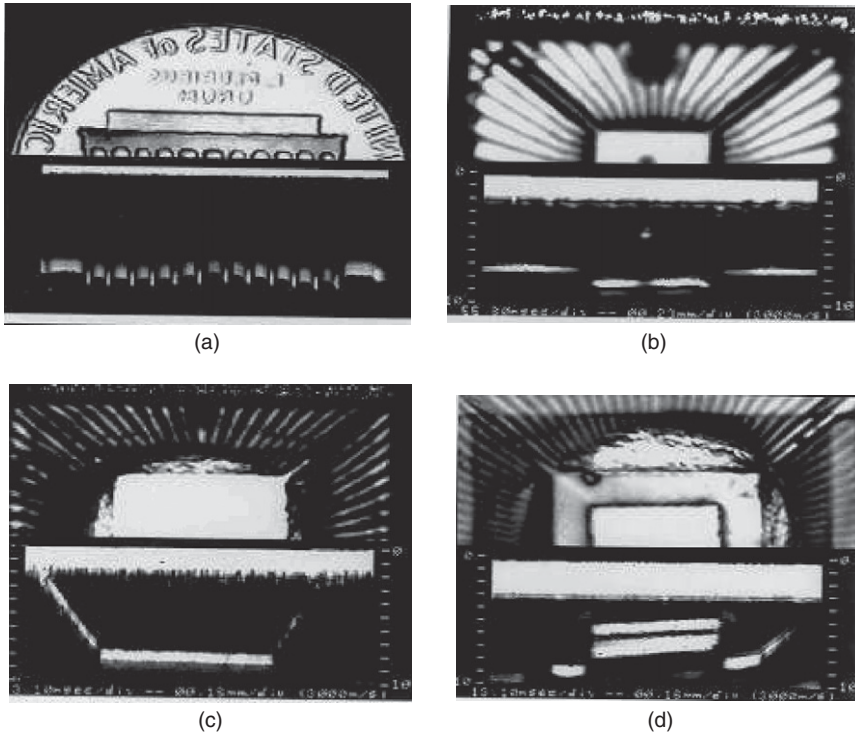


Figure 6.22 (a) A Q-BAM™ image of a US penny imaged through the coin and focused at the rear surface. (b) A 68-lead plastic-leaded chip carrier cross-sectioned midway through a dark spot. (c) Device with a popcorn crack originating from the edges of the die-paddle. (d) A significant degree of paddle shift.

Figure 6.23 shows a TOF image of another popcorn-cracked integrated circuit. In this case, the image is produced by recording the echo arrival times. In addition, however, the data are projected isometrically, to produce a true three-dimensional perspective of the crack profile within the package. In combination with the Q-BAM™ images, both qualitative and quantitative perspectives of plastic package anomalies can be produced.

6.3.4.4 Production Rate Screening Using Tray-Scan Imaging

The scanning area can be enlarged to scan trays of parts and improve the efficiency of on-line screening. Larger scanning area requires more time for scanning (with C-SAM), but the process of loading and unloading individual parts is circumvented.

Petitioner Samsung Ex-1055, 0333

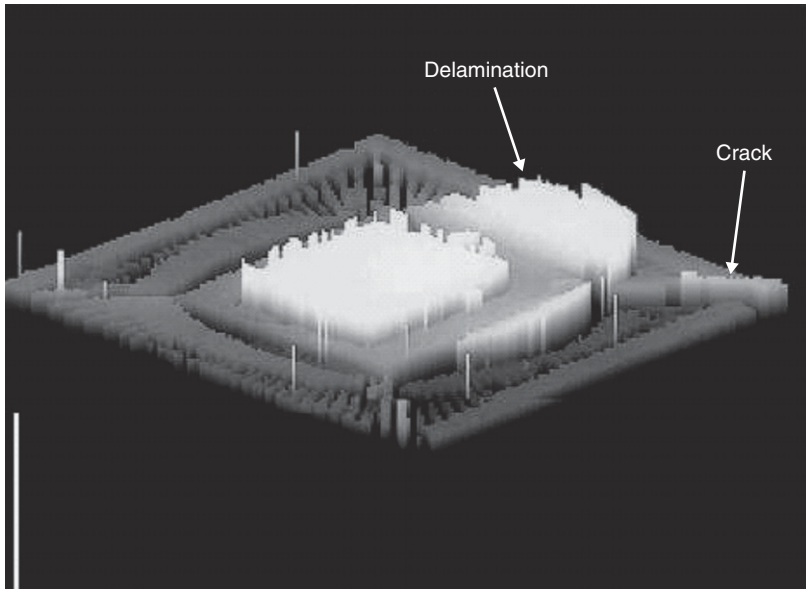


Figure 6.23 A time-of-flight image of a "popcorn"-cracked integrated circuit.

Figure 6.24 shows 32 memory chips in the field-of-view at the same time. This is a reflection C-mode image, with a unified black-and-white display in which delaminations are coded black. Because of slight height differences between the devices, it is necessary to use an echo tracking technique called front interface echo (FIE) tracking. In this method, the instrument senses the height of the top surface of each component and then adjusts the digital gates appropriately during the scanning process. Without this feature, some echoes could miss the electronic gate because of signal arrival time differences. FIE tracking is also useful for following the contours of curved or tilted devices.

6.3.4.5 Molding Compound Characterization

Characterizing molding compound materials has generally been done from a chemical perspective; physical characterization has usually been limited to density, modulus/stiffness, thermal expansion, and moisture absorption. SAM offers the additional possibility of quantitatively measuring the molding compound degree of cure, homogeneity, porosity, and the overall distribution of filler. The parameters that are measured acoustically are the velocity of sound and the attenuation coefficient. For example, the

Petitioner Samsung Ex-1055, 0334

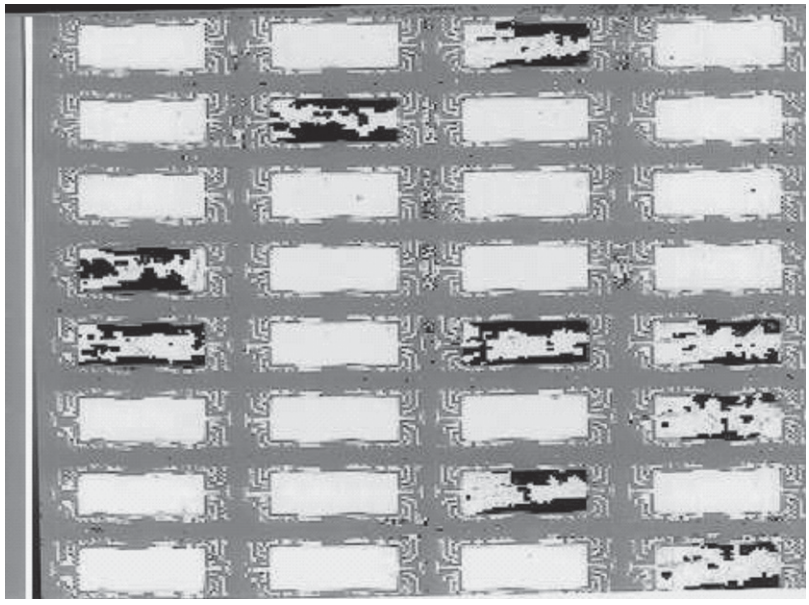


Figure 6.24 Tray-scan imaging of 32 memory chips.

absorption of ultrasound increases greatly with porosity. It has also been observed that more flexible molding materials are far more lossy (absorbing) than stiff materials. This is why lower acoustic frequencies are required to inspect devices containing large dies, which are subjected to far greater mechanical and thermal stresses. Data from typical molding compounds are shown in Fig. 6.25.

Evaluation Checklist:

- Void content of molding compound
- Bulk scan top
  - Bulk scan bottom
  - Paddle shift
- Die tilt
- Die surface delamination
- Die-attach delamination
- Lead-frame delamination
- Paddle delamination
- Package cracks
- Q-BAM™ acoustic cross-section
- 3D TOF crack profiling (for 3D void and crack profiles)

Petitioner Samsung Ex-1055, 0335

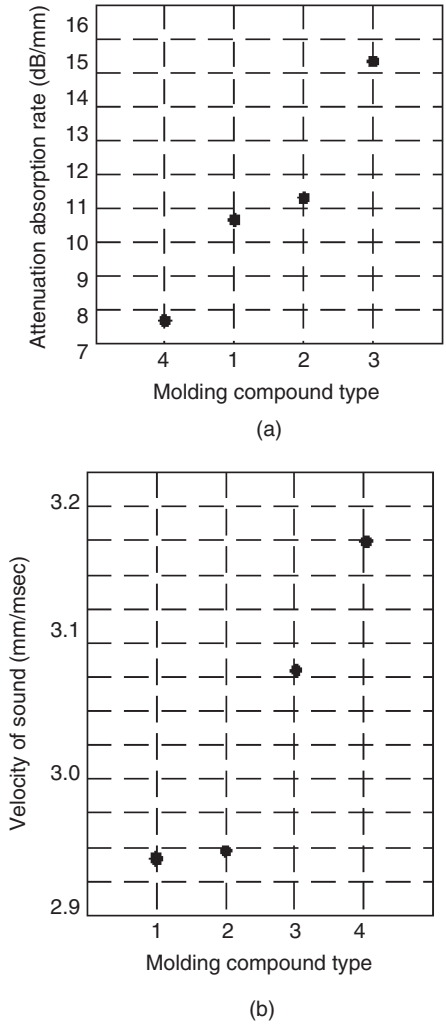


Figure 6.25 (a) Attenuation absorption rate measurements for molding compounds of the same basic formulation with variations in particle size and additives. (b) Velocity of sound measurements for molding compounds of the same basic formulation with variations in particle size and additives.

6.4 X-ray Microscopy

The principal advantage of X-ray microscopy for failure analysis is the nature of the image contrast that X-rays produce as a result of differential absorption of the primary X-rays by the specimen. The degree of absorption depends both on the species of atoms in the specimen and

Petitioner Samsung Ex-1055, 0336

on their atomic number. It is thus possible not only to reveal the presence of different microstructural features, but also to obtain information about their composition. Various X-ray microscopes that reveal microstructural features of the specimen include X-ray contact microscope, projection microscope, reflection microscope, and diffraction microscope. Compositions are analyzed using X-ray spectroscopes which will be discussed later.

Another advantage of the X-ray microscope is the comparatively deep penetration of X-rays into thick specimens, which enables detection of the internal structure of electronic packages or components without opening the package. X-ray microscopy (also called microradiography) is therefore a non-destructive technique that, like SAM, does not require package decapsulation.

Further benefit of using X-ray microscopy is that the package or component can be examined in its natural state; neither a conductive coating nor high vacuum is needed, as they are with conventional electron microscopes. No medium like water or oil is required either, while it is for SAM. However, X-ray radiation may change the electrical properties of microelectronic packages, so it should not be used when the electrical properties of the package are under investigation.

An X-ray image is formed as a projection of contrast through the whole thickness of a specimen. Difficulties thus arise in analyzing an image of overlapped multiple components. Because of the short wavelength of X-rays, better ultimate resolution can be obtained using X-rays than can be obtained using light, although it is not as good as that obtained using electrons. In applying X-ray microradiography, the difficulty is finding a way to focus the X-rays (electrons, on the other hand, can be focused by a magnetic or condensing lens). X-rays carry no electric charge, so neither magnetic nor electrostatic lenses affect them. The ultimate resolution is usually around 1 μm, although a resolution in the 10-nm region can be achieved with effort. Attention must be paid to radiation safety when an X-ray microscope is used.

6.4.1 X-ray Generation and Absorption

X-rays are usually generated in an X-ray tube. The X-rays that pass through the specimen are detected by exposing a film (conventional) or using a charge-coupled device detector. Figure 6.26 shows a schematic cross-section of an X-ray tube [12]. In a conventional X-ray machine, under a high-voltage potential, electrons are produced by a heated

Petitioner Samsung Ex-1055, 0337

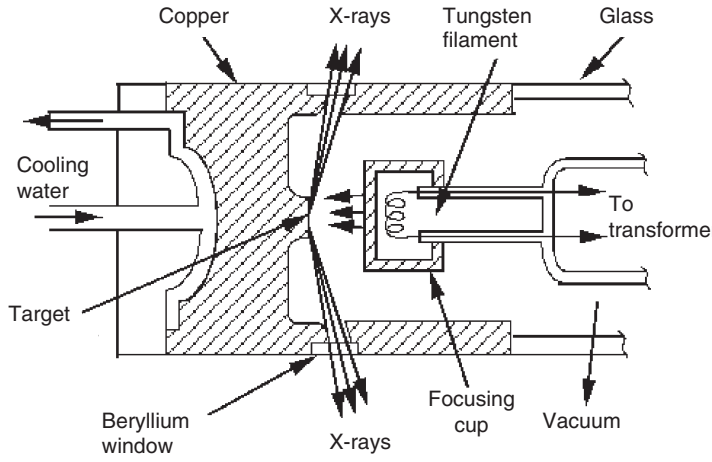


Figure 6.26 Schematic cross-section of an X-ray tube [12].

tungsten filament and are accelerated and focused onto the anode, a metal (e.g., copper) target. The accelerated primary electrons are then decelerated as they collide with the atoms of the target material. X-rays are generated by the energy released by the collisions. Less than 1% of the energy of the primary electrons is actually converted to X-rays; most of the remainder takes the form of heat which is dissipated via a water-cooling system.

Generated X-rays are emitted in all directions and allowed to escape from the tube through windows, as shown in Fig. 6.26. X-ray tubes are usually evacuated down to a pressure of about 10^{-4} torr (a pressure of 1 torr = 1 mm of Hg) in order to minimize the collision of electrons with gas molecules. Permanently sealed tubes are often used to avoid the need for a vacuum pumping system. The quantity of X-rays emitted by the tube is controlled by varying the current heating the tungsten filament, while the wavelength of the X-rays is determined by the magnitude of the accelerating voltage. Two types of X-ray spectra, the continuous spectrum and the characteristic spectrum, are classified according to features of their wavelengths.

The energy of a primary electron is given by $E = eV$ where e is the charge carried by the electron and V is the accelerating potential. If the electron is completely stopped by a single collision, the energy of the generated X-ray quantum can be given by $E = Kv_{quan}$, where k is the Plank constant and v_{quan} is the velocity of the quantum. Since $v = v_{light}/\lambda$, where

Petitioner Samsung Ex-1055, 0338

v_{light} is the velocity of light and λ is the wavelength of the X-rays, $\lambda = kc/qV$. Substituting the values of these constants, λ = 1240/V, where λ is measured in nanometers and V in volts.

Generally, only a small fraction of the primary electrons is completely stopped by a single collision. The majority of the electrons are decelerated by repeated collisions with other atoms. The X-rays generated by these collisions have lower energies and, thus, longer wavelengths. Consequently, a continuous spectrum with a broad range of wavelengths is generated. The minimum wavelength of the spectrum is determined by the accelerating voltage of the primary electrons.

The determination of a characteristic spectrum is a very different matter. A characteristic spectrum is determined by the target material. When an inner shell electron in an atom of target material is knocked out by a collision with a primary electron, the atom becomes unstable. Another electron in the same atom will jump down to fill the vacancy by losing the energy, ΔE, and an X-ray quantum is generated with the wavelength, $\lambda = kv_{light}/\Delta E$. Since ΔE is a specific quantity associated with the particular energy change occurring in this atom, the wavelength generated is characteristic of this atomic species. Several characteristic wavelengths coexist for a particular species, determined by the ΔE released by the electron jumping down between different shells in the atom. A characteristic K-line spectrum of a species, produced by the transition from upper shells into K-shells, generally includes K_{a1}, K_{a2}, K_{β} radiation, with their specific wavelengths. Table 6.3 lists the wavelengths emitted by some typical target materials.

When an X-ray beam passes through a particular material, its intensity is reduced because the material absorbs some X-rays. The linear absorption coefficient is determined by the atomic number of the material and the

Table 6.3 Characteristic X-ray Wavelengths Emitted by Target Materials

Element	K_{a2} (nm)	K_{a1} (nm)	K_{β} (nm)
Cr	0.229315	0.228962	0.208480
Fe	0.193991	0.193597	0.175653
Co	0.179278	0.178892	0.162075
Ni	0.166169	0.165784	0.150010
Cu	0.154433	0.154051	0.139217
Mo	0.071354	0.070926	0.063225
Ag	0.056378	0.055936	0.049701
W	0.021381	0.020899	0.018436

Petitioner Samsung Ex-1055, 0339

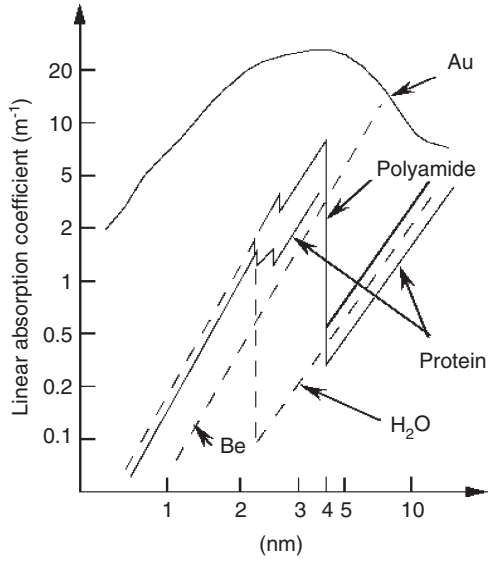


Figure 6.27 The absorption coefficient versus the wavelength of X-ray in the continuous region for a number of materials [21].

X-ray wavelengths. Figure 6.27 shows the linear absorption coefficient versus the X-ray wavelength in the continuous region for a number of materials [21]. Assuming that a 3.0-nm X-ray wavelength is considered, the μ value changes from approximately 25 μm^{-1} for gold and 2.5 μm^{-1} for polyimide to 0.15 μm^{-1} for water. In other words, a given attenuation is generated by a thickness of 0.04 μm of gold, 0.4 μm of polyimide, or 7 μm of water. There is a difference of about one order of magnitude between the absorption coefficients for polyimide and gold; this difference provides a good contrast for imaging electronic packages. These data also provide a thickness ratio between different materials that the X-rays can penetrate.

6.4.2 X-ray Contact Microscope

Contact microscopes are widely used in the electronic packaging field in both manufacturing and research. In contact microscopy, the specimen is placed in contact with an X-ray image receptor, such as a film cassette or film pack, at a certain distance from an X-ray source (Fig. 6.28). The X-rays transmitted through the specimen form an image on the receptor

Petitioner Samsung Ex-1055, 0340

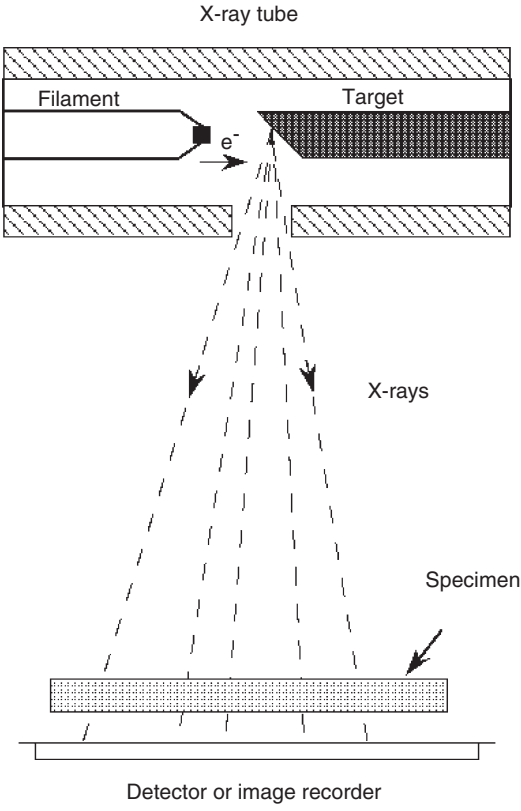


Figure 6.28 Schematic of X-ray contact microscopy.

at, effectively, unit magnification. The resulting film is then examined under an optical microscope. The entire internal structure of the specimen can be viewed on the X-ray film. Selected areas may subsequently be enlarged photographically.

To operate a contact X-ray properly, several parameters and aspects should be considered:

- X-ray high voltage setting and current setting;
- material and thickness of specimen;
- position of specimen;
- exposure time.

The intensity of the primary X-rays is a function of both high-voltage settings and current setting. The intensity of the X-rays penetrating the

Petitioner Samsung Ex-1055, 0341

specimen is dependent on the intensity of the primary X-rays, the absorption coefficient of the specimen, the material, and the thickness of the specimen. The brightness and contrast of the radiographic image shown on the film is, in turn, controlled by the intensity of the penetrating X-rays, the X-ray exposure time, and the sensitivity of the film. Optimum parameter selections to obtain a good X-ray radiograph are usually based on empirical practice. Aside from these parameter selections, lead shielding around the specimen and/or underneath the film helps to increase the image contrast. According to the Abbe diffraction theory, geometrical blurring in the image, gets worse as the specimen to film distance is increased. To obtain high resolution and keep the blurring minimal, the film should be placed as close to the specimen as possible. Beyond this, the resolution of the X-ray photograph is dependent on that of the optical microscope used for later film-image examination.

6.4.3 X-ray Projection Microscope

Unlike the X-ray contact microscope, the X-ray projection microscope provides a primary magnification. The principle of this microscope is demonstrated in Fig. 6.29. The electron beam is focused by a set of magnetic lenses to a tiny spot on the target material. The specimen is placed within a millimeter of the target so that the X-rays bombard only a small area of the specimen. The magnification of the film image produced is calculated as the sum of the target-specimen distance and the specimen-film distance, divided by the target-specimen distance. Since the target-specimen distance is very small with respect to the specimen-film distance, the X-ray image has a magnification effectively equal to the ratio of the specimen-film distance to the target-specimen distance.

Like the image from an X-ray contact microscope, the primary X-ray photograph is viewed subsequently at higher magnifications under an optical microscope. Because the primary image already has a certain magnification, the resolution limit of the technique is determined by those of both the X-ray microscope and the optical microscope. Using the X-ray projection technique, resolutions of 0.1–1 μm can be achieved, with a primary magnification of up to about 1000×.

Image contrast with the X-ray projection microscope is achieved in the same way as with contact microscope. The applications and operations of the projection technique are also similar to those of the contact microscope. In addition to higher magnification, the projection technique also provides a greater depth of field, which allows images of stereoscopic pairs,

Petitioner Samsung Ex-1055, 0342

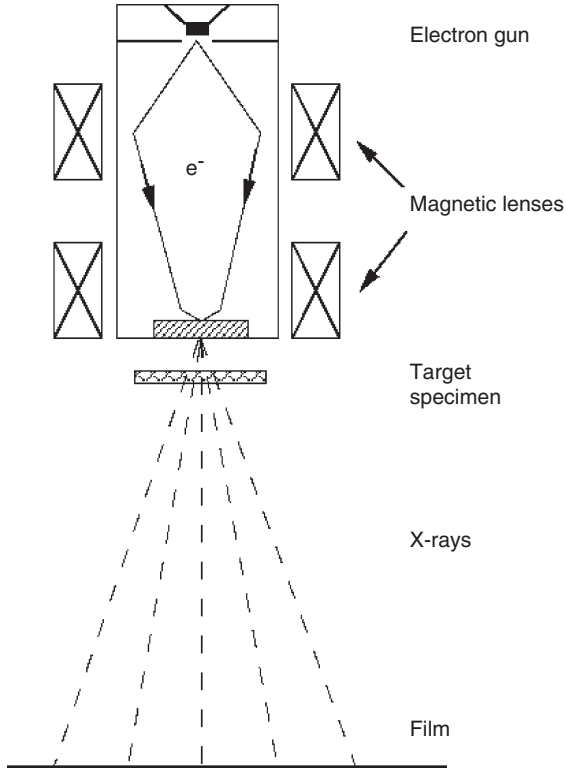


Figure 6.29 Principle of X-ray projection microscope.

even at high magnification. However, the X-ray projection microscope is much more complex and expensive than the contact microscope.

6.4.4 High-Resolution Scanning X-ray Diffraction Microscope

Recent developments in X-ray microscopy have led to the invention of a high-resolution scanning X-ray diffraction microscope (HR-SXDM) where detailed diffraction patterns can be recorded while the sample is scanned through the focal spot of the beam. Conventional X-ray (or electron) scanning microscopes can measure only the total transmitted intensity. HR-SXDM combines the high penetration power of X-rays with the high spatial resolution of diffractive imaging. Up to several tens

Petitioner Samsung Ex-1055, 0343

of thousands of diffraction images from HR-SXDM are treated with special algorithms where the images form into one super-resolution X-ray micrograph [22,23].

An important advantage of HR-SXDM is the new possibility of depth analysis. Conventional scanning electron microscopes generally provide high-resolution images of the surface of the specimen, and the samples must be kept in vacuum. Super-resolution X-ray microscopy (SR-XM) does not have such requirements. Using SR-XM, failure analysts can look deeply into semiconductors and interior encapsulated package without destroying them. Thus, HR-SXDM is a powerful non-destructive analysis technique for characterizing nanometer defects inside the encapsulated package. It is a particularly useful analysis tool for advanced semiconductor devices and encapsulated packages with nanometer features.

6.4.5 Case Study: Encapsulation in Plastic-Encapsulated Devices

An X-ray contact microscope (MICRO RT Model B-510) was employed for this case study. Plastic-encapsulated packages were placed on a manipulator system that can be moved in three directions for adjusting specimen position in a specimen chamber. The adjustment was monitored via a TV imaging system. An X-ray sensitive film was inserted between the packages and the manipulator system.

A good radiographic image was obtained by adjusting the specimen position and properly selecting the X-ray tube voltage and current, the film type, and the exposure time. Higher tube voltages, and sometimes higher current, are employed for examinations of thicker specimens. Lower tube voltages are usually selected if the films are more sensitive to X-rays. Xeroradiography, Kodak X-Omat TL, and Polaroid Type 52, 53, and 55 are the common selectable films. An optimum exposure time is determined by the X-ray absorption of the materials, the thickness of the specimen, the tube voltage and current, the specimen position and the film type. A comparative exposure guide can be found in the operator's manual of the MICRO RT Series Radiography System (Model B-510).

Figure 6.30 shows the top and side views of two 18-pin PDIPs. The packages were thermocycled 100 times between 25°C and 200°C. The study focused on examining the internal structure of the packages after the thermal cycling test. Two packages were positioned, one flat and one sideways, on the manipulator. X-ray radiographies were captured by

Petitioner Samsung Ex-1055, 0344

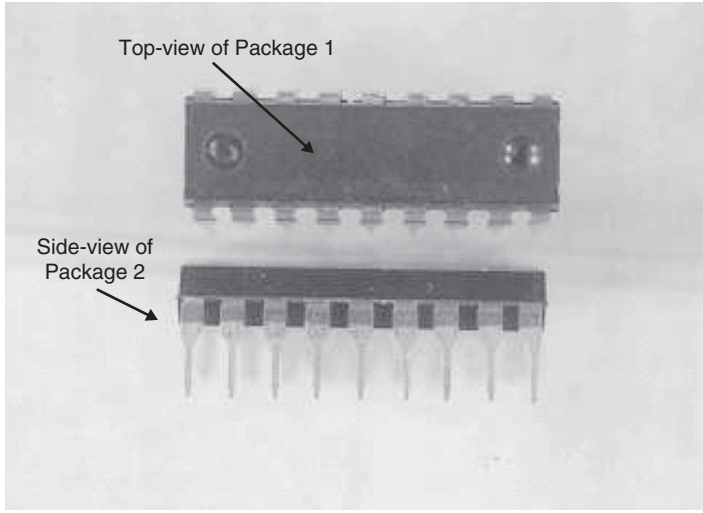


Figure 6.30 Top and side views of the 18-pin plastic dual in-line packages.

subjecting the packages to 70 kV tube voltage and 0.4 mA tube current, with Polaroid Type 55 film, for 2 minutes. To minimize the geometrical blurring, the films were placed as close as possible to the plastic packages, allowing one-to-one magnification of the specimens on the films. An optical microscope was then employed to enlarge the negative images captured on the films.

Figure 6.31 shows the enlarged X-ray images of the same two packages (shown in Fig. 6.30). The radiograph is, in fact, a projective image of the specimen. It is sometimes difficult to interpret the image, especially when many components are overlapped in the packages. Although the top-view image in Fig. 6.31 (upper image) shows wires clearly, the central area image is a projection of molding compound, die, die-attach paddle, and molding compound again, as shown in Fig. 6.32(a). It is difficult to visualize the interfaces between any two components. The side-view image in Fig. 6.31 (lower image) shows the plastic/die interface and a dark strip between the molding compound and the die, indicating the plastic/die interfacial delamination.

The side-view image in Fig. 6.31 does not show the paddle/plastic interface clearly because the interface image was overlapped with the image of leads. Paddle/plastic interfacial delamination can be observed by rotating the package 90° to view the non-leaded side as illustrated in Fig. 6.32(b). Both plastic/die and paddle/plastic interfacial delamination can be verified by scanning acoustic microscopic examination.

Petitioner Samsung Ex-1055, 0345

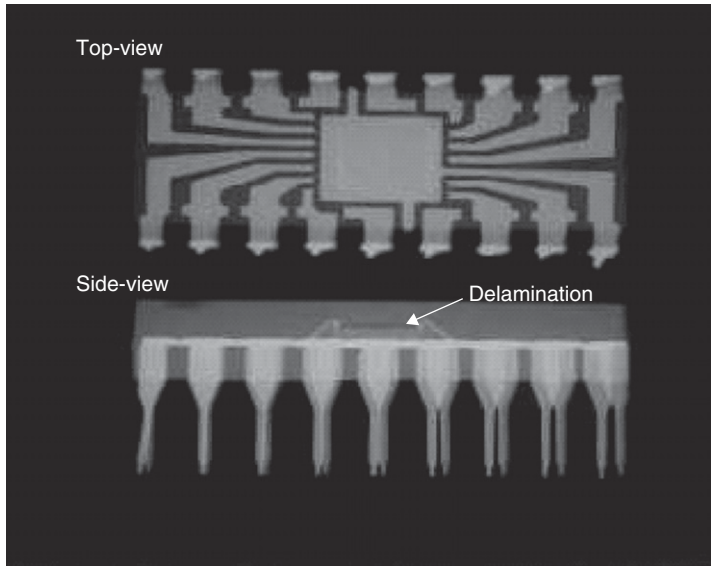


Figure 6.31 X-ray radiograph with the top-view image showing the internal structure of the 18-pin plastic dual in-line package and the side-view image showing plastic/die delamination.

6.5 X-ray Fluorescence Spectroscopy

XRF spectroscopy is a fast, accurate and non-destructive technique used to identify and detect material composition. It is compatible with solid, liquid, and powdered samples, and requires no or minimal sample preparation. There is no need to place the sample in vacuum chamber as with energy dispersive spectroscopy systems. XRF spectrometer types can vary from light hand-held devices to table-top machines.

A movable X–Y stage and variable Z-axis source allows great flexibility with sample size: from a single surface-mount chip to a hand-held portable electronic device. A video camera in sync with the emitter allows continuous monitoring of the position on the sample, making it possible to locate an area of interest prior to analysis.

XRF spectrometers can operate in two main modes: material analysis mode and thickness measurement mode [1]. The material analysis mode of the XRF spectrometer is capable of wide range of material analysis from aluminum (Z = 13) to uranium (Z = 92). Material composition ranging from 0.1% to 100% can be detected accurately. A typical XRF spectrometer system may consist of four collimators with programmable, motorized controls. Analysis of small regions of interest on the

Petitioner Samsung Ex-1055, 0346

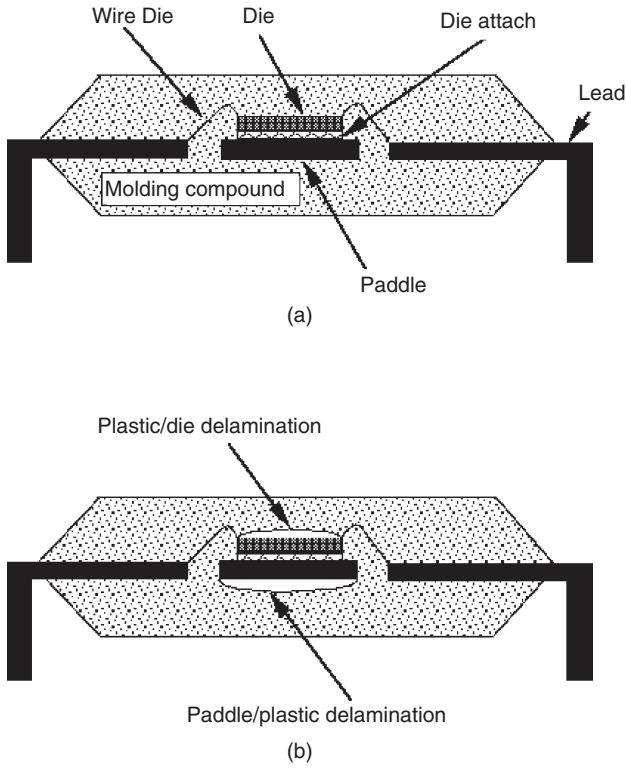


Figure 6.32 Plastic package (a) without delamination and (b) with both plastic/die and paddle/plastic delamination.

specimen can be achieved with the minimum XRF collimator size of 100 μm.

The XRF spectrometer thickness measurement mode provides the ability to measure the depth of known layers of material. Each layer can be either a single element or an alloy. The depth of penetration in XRF spectrometry varies based on the materials used, but over 50 μm is possible.

6.6 Electron Microscopy

The first electron microscope was fabricated in 1930s. The basic idea arose from the understanding that the concentrating action of a magnetic field in focusing an electron beam was analogous to that of a lens used with visual light. Today there are hundreds of electronic microscope models, including numerous variations on the basic idea. In comparison with the optical microscope, scanning acoustic microscope, and X-ray

Petitioner Samsung Ex-1055, 0347

microscopes, electron microscopes have far superior resolution power. A certain type of electron microscope can even reach atomic scale resolution. An additional feature is that electron microscopes are not restricted solely to providing microstructural information. It is also possible to obtain electron diffraction patterns that offer crystallographic information. Direct chemical analysis provides compositional information on specimens.

6.6.1 Electron–Specimen Interaction

Electron microscopy has been developed with numerous microanalysis techniques based on the electron-specimen interaction. The conventional techniques are scanning electron microscopy (SEM), transmission electron microscopy (TEM), scanning and transmission electron microscopy (STEM), and electron microscopies combined with other analysis techniques, such as X-ray and acoustic imaging. When an electron microscope is in operation, the electrons generated by high voltages, often part of the so called primary electron beam, are aimed at the specimen. As shown in Fig. 6.33, the primary electron beam interacts with the specimen in a numbers of ways.

A portion of the primary electrons will be transmitted through the specimen if it is thin enough. The transmitted electrons can be both unscattered (coming out of the specimen along the direction of primary electron beam) and scattered (with angles apart from the direction of primary electron beam). Since both unscattered and scattered electrons are transmitted through the specimen, they carry the microstructural information of the specimen. Transmission electron microscopes collect the electrons with a comprehensive detection system and project the microstructural images onto a fluorescent screen. A TEM image is a projection of the microstructure of the specimen.

When the primary electron beam is targeted at the specimen, a portion of the primary electrons are back-scattered from the upper surface of the specimen. As the incident high-energy primary electrons interact with the specimen, a portion of the specimen electrons can also be excited and emitted from the upper surface of the specimen, referred to as secondary electrons. Both backscattered and secondary electrons carry the morphological information from the specimen surface. A back-scatter electron detector and a secondary electron detector assembled in a scanning electron microscope will collect these electrons and transmit the signals to a CRT. SEM images obtained from secondary electron analysis generally have a well defined and three-dimensional appearance and can be used to obtain morphological information of the specimen surface. Images obtained

Petitioner Samsung Ex-1055, 0348

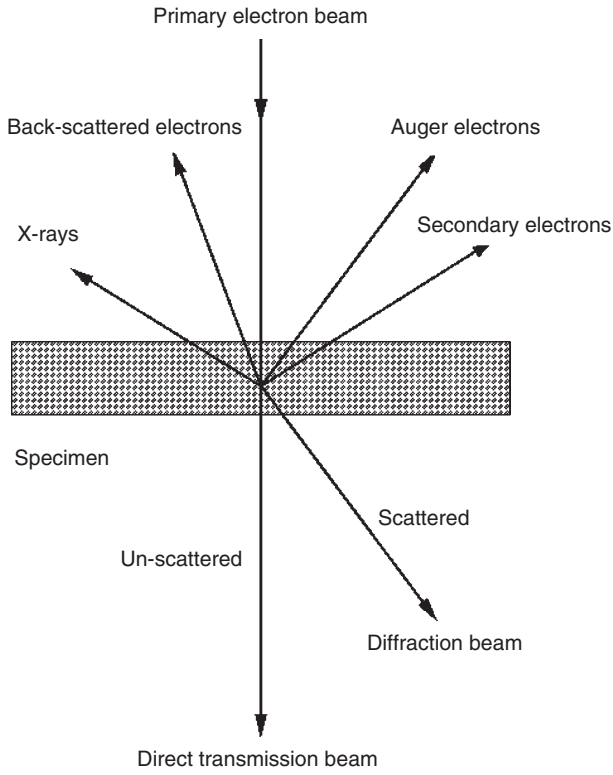


Figure 6.33 Signals created by the interaction of high-energy electrons with the specimen.

from backscattered electrons are used for the analysis of the chemical composition and the crystallographic structure of the specimen. STEM is a combination of SEM and TEM.

In addition to the detectors for TEM and SEM images, further signal detection systems, can also be established with an electron microscope. As an electron escapes a specimen atom, another electron at a higher energy level in the atom may fall into the vacancy leading to a release of energy. Sometimes the released energy causes an emission of a second electron, called Auger electron. X-rays and Auger electrons excited from the specimen carry information on the energy levels of the atomic electron orbital, and can be collected to identify chemical elements unambiguously. The energy analysis of X-rays can be carried out using either wavelength dispersion or, more often, energy dispersion. In general, all elements with atomic numbers greater than Z = 10 (neon) can be detected using energy dispersive X-ray (EDX) spectroscopy, although the technique can be extended down to boron (Z = 5).

Petitioner Samsung Ex-1055, 0349

Auger electrons are collected by Auger electron spectroscopy (AES). Auger electrons have energies determined by the energy levels in the parent atom and are characteristic of that atom. Since Auger electrons have energies typically in the range 0–2000 eV, the distance that they can travel in a solid before losing energy is limited to approximately 1–2 nm. This characteristic gives the AES technique its high surface sensitivity.

6.6.2 Scanning Electron Microscopy

A modern analytical scanning electron microscope consists of electron optics, comprehensive signal detection facilities, and a high vacuum environment. A schematic diagram of the scanning electron microscope is shown in Fig. 6.34.

The electron optical system includes an electron gun, condenser lenses, scanning coils, and an objective lens. The electron source is usually a pointed tungsten or lanthanum hexaboride filament that emits a stream of

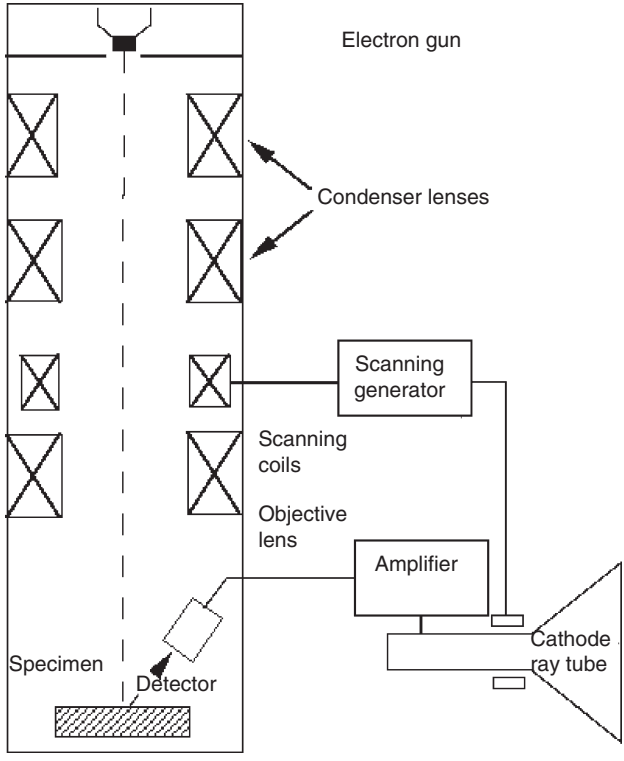


Figure 6.34 Schematic diagram of the scanning electron microscope.

Petitioner Samsung Ex-1055, 0350

electrons. The filament is kept at a high potential and the electron beam is accelerated through a small hole in the grounded anode before being focused on the specimen by means of a system of condenser lenses. This accelerating potential determines the wavelength of the electrons, λ. For an accelerating voltage of 10 kV, for instance, the electron wavelength is on the order of 10^{-2} nm. If the imaging system of the electron microscope could be made as effective as that of the optical microscope, then the limit of resolution would in theory be of the same order as the wavelength. Unfortunately, the condenser lens aberrations associated with the use of magnetic fields for focusing are so great that the practical resolution limit is on the order of 10^{0} nm. Normally, the accelerating voltage for a scanning electron microscope is in the range of 5–30 kV, though in some special cases 1–5 kV is used. The resolution limit is also affected by the conductivity of the specimens. The high resolution is achieved with specimens of high conductivity.

Two detection systems are generally used for imaging with a scanning electron microscope: the secondary electron detector and the back-scattering electron detector. With lower energies (<50 eV), secondary electrons generated due to the interaction of the high-energy electron beam with the surface layers can travel in the solid material for about few nanometers before escaping the surface. As a result, secondary electrons generated at distances further than few nanometers from the surface fail to escape from the specimen. This feature makes secondary electron imaging high resolution. However, due to the small interaction volume near the specimen surface (only few nanometers thick) and the relatively weak signals produced, secondary electrons have low contrast images. Traveling distances of backscattering electrons (with energies >50 eV) reach 10–100 μm, depending upon the specimen material. Strong signals are generated because of the large interaction volume in the specimen. Therefore, backscattering images have sharper contrast but lower resolution than secondary electron images.

A high vacuum system is essential for conventional SEMs and TEMs. The vacuum level must be sufficient to avoid collisions between electrons and gas molecules that could affect the routine interaction of primary electrons with the specimen by changing electron paths. Moreover, the residual materials from the collision reactions deposit on the specimen, objective aperture, and other microscope elements, causing contamination that obscures the microstructural observation and modifies the imaging properties of the instrument. In conventional electron microscopes, column pressures are on the order of 10^{-6} torr, and electron gun pressures can reach 10^{-9} torr (a pressure of 1 torr = 1 mmHg). Three levels of vacuum system—a

Petitioner Samsung Ex-1055, 0351

mechanical pump (10^{-3} torr), a diffusional pump (10^{-6} torr), and an ion pump (10^{-9} torr)—are typically utilized to provide high vacuum conditions.

Selection and adjustment of operational variables are critical in order to obtain SEM images with high quality. Accelerating voltage, beam current, and final aperture size are the primary variables in SEM operation. High accelerating voltage is essential to SEM resolution, as illustrated before. However, the effect of interaction volume and specimen charging must be considered. Higher voltage is usually applied to obtain backscattering images, while lower voltage is used to get secondary scattering images. Specimen charging becomes more severe for a poorly conductive specimen when high accelerating voltage is applied. Beam current is often adjusted by selecting the spot size of the electron beam; a strong signal requires a large beam and thus a reduced resolution. Aperture size also affects resolution. A small aperture gives good resolution and is often used for images with high magnification; a large aperture is needed to allow the passage of a large beam, and is suitable for X-ray spectroscopy. Aperture size also affects the depth of field. A large aperture is needed if a low magnification limit is approached.

Specimens for conventional SEM analysis must be covered with a thin, conductive coating to avoid electrical charging. A number of coating materials and techniques are available. The most common materials used are carbon, gold, gold-palladium, platinum, and aluminum.

The SEM technique is a widely applied and powerful tool in both semiconductor device and package inspection. Small defects such as pinholes and hillocks on semiconductors, voids caused by electrostatic discharge, short circuits induced by electrical overstress, hairline fractures of passivation layers, open circuits due to electromigration in metallization, dendrite growth, and bonding failures can be visually inspected. SEM can also be used as an electrical testing instrument. When bias is applied to the devices, the SEM image contrast is enhanced by the magnitude of the bias voltage; this technique is called voltage contrast. The negatively biased areas in the device appear bright, while positively biased areas appear dark. Defective sites can be detected by comparing the contrast of the biased areas.

6.6.3 Environmental Scanning Electron Microscopy (ESEM)

ESEM is a special type of SEM that work under controlled environmental conditions and require no conductive coating on the specimen. The pressure in the sample chamber of an environmental scanning electron

Petitioner Samsung Ex-1055, 0352

microscope can be adjusted from 1 to 20 torr or from 1 to 50 torr in terms of different models; that is, only 1–2 orders of magnitude lower than the atmosphere. In comparison, the pressure in the sample chamber of a conventional SEM has to be 10^{-5} torr or less, which is 6–7 orders of magnitude lower than the atmosphere. The pressure condition allows the researcher to examine unprepared, uncoated specimens that are free of surface charging and high vacuum damage. This makes it possible to examine specimens in their natural states. The environment in ESEM can be selected from among water vapor, air, nitrogen, argon, oxygen, etc. Dynamic characterization of wetting, drying, absorption, melting, corrosion, and crystallization can be performed using ESEM.

Environmental scanning electron microscopes are able to work with certain pressures and without surface charging because the secondary electron detector is designed on the principle of gas ionization. This is illustrated in Fig. 6.35. As primary electrons are emitted from the gun system, the secondary electrons on the specimen surface are accelerated toward the detector, which is biased by a moderate electric field. The collisions between the electrons and gas molecules liberate more free electrons, and thereby provide more signals. Positive ions created in the gas effectively neutralize the excess electron charge built up on the specimen. Proper operating pressure controls the specimen surface charging.

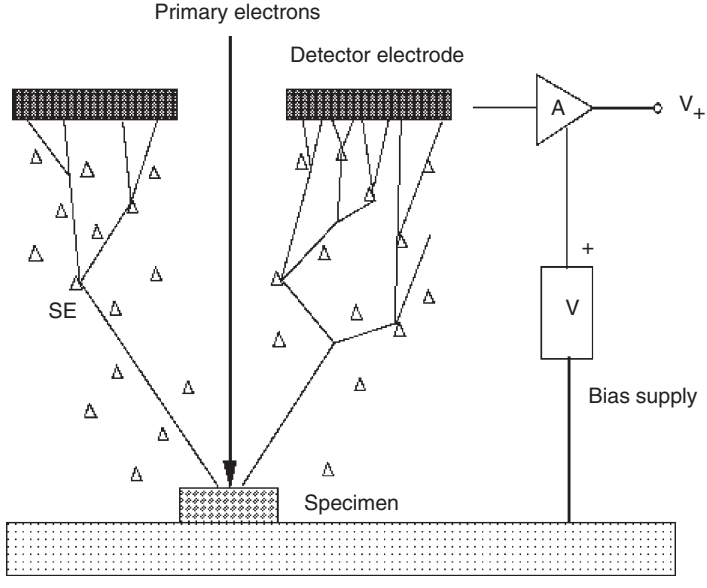


Figure 6.35 Schematic diagram of the environmental scanning electron detector.

Petitioner Samsung Ex-1055, 0353

Depending on the environmental requirements, the pressure source can be water vapor, air, argon, nitrogen, or other gases. Four-stage vacuum levels (electron gun chamber, optical column, detector chamber, and specimen chamber) are maintained from 10^{-7} to 10^{1} torr by a computer controlled vacuum system.

The specimen chamber pressure is one of the important ESEM parameters, in addition to the parameter settings for conventional SEM. Adjusting the specimen chamber pressure helps provide stronger signals, and consequently sharper contrast for ESEM imaging, because the adjustment controls the number of gas molecules between the specimen and the secondary electron detector. The environmental relative humidity in the specimen chamber can also be varied by adjusting the chamber pressure. Relative humidity can be varied in the range of 20–90% at around room temperature. However, this is not an easy procedure, because other parameters, such as electron beam size, voltage, image contrast, and brightness, must be adjusted appropriately to maintain a good image.

The low vacuum level required for the specimen chamber allows a large working space in the chamber. A temperature stage, mechanical test system, in either tensile, compression, four-point bending, or shear mode, and a micromanipulator/microinjector system can be installed in the specimen chamber to enable various dynamic investigations, such as the simulation of different failure mechanisms on electronic packages. Another advantage of ESEM is that, working under controlled environmental conditions, it can still function as well as ordinary SEM without such trade-offs as a loss of resolution.

6.6.4 Transmission Electron Microscopy

TEM is composed of comprehensive electron optics, an electron emission and projection system, and a high vacuum environment. A schematic diagram of TEM is given in Fig. 6.36. The electron optics system consists of an electron gun, condenser lenses, objective lens, and a projector lens system. High vacuum is also a critical issue for successive imaging and the prevention of contamination. Higher voltage is applied to the electron gun than in SEM, so the primary electrons can carry sufficient energies to penetrate the specimen. The ultimate voltage for a TEM can generally be from 100 to 1000 kV, depending on the requirement of resolving power for a particular TEM. TEMs with higher ultimate voltages have higher resolving power and handle thicker specimens. The ultimate resolution of TEMs with ultra-high-voltage can reach sub-angstrom levels (1 angstrom = 1×10^{-10} m).

Petitioner Samsung Ex-1055, 0354

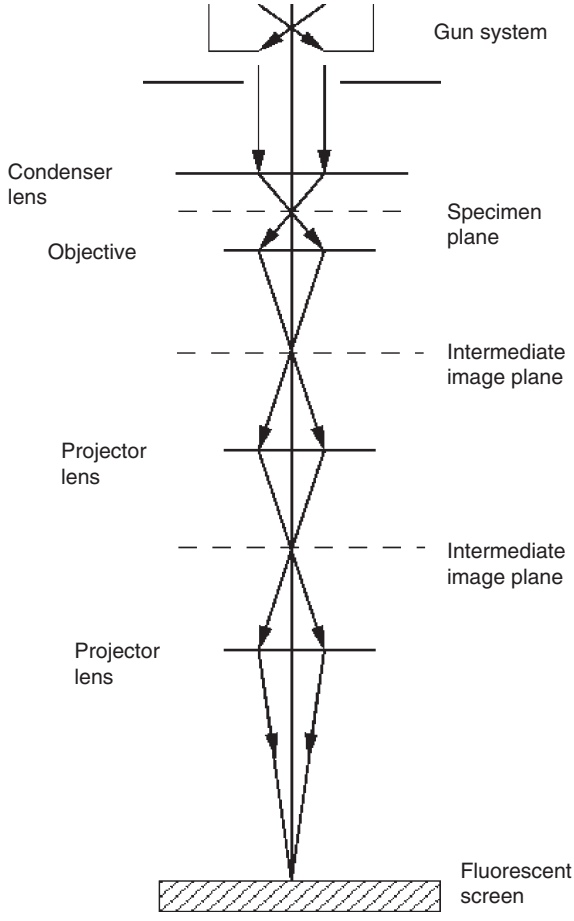


Figure 6.36 A schematic diagram of transmission electron microscopy.

Alternative operating modes can be utilized in applying TEM to defect and failure analysis of electronic materials and packages. Bright-field and dark-field modes can be selected to obtain different diffraction contrast images; high resolution mode can be used to get phase contrast images, especially useful for failure analysis in semiconductor/oxide/metallization interfacial failure modes. These three modes are discussed below.

Bright-Field Mode. As discussed previously, electrons transmitted through the specimen are divided into unscattered electrons and scattered electrons. The former moves parallel to the primary beam and is called the direct beam; the latter is scattered from the primary beam direction and is called the diffracted beam, if the electrons are scattered without energy

Petitioner Samsung Ex-1055, 0355

loss. The angle that the diffracted electrons make with the direct beam, defined according to Bragg's law, is 2θ. In practice there are, of course, a number of these diffracted beams for any crystalline specimens. Normally, all the diffracted beams are stopped by the objective aperture, and only the direct beam contributes to what is known as a bright-field image, as shown in Fig. 6.37(a). The bright-field imaging mode is most often selected in TEM operation.

Dark-Field Mode. As an alternative to bright-field imaging, the direct beam may be obstructed and one of the diffracted beams is allowed to form the image. This dark-field image is illustrated in Fig. 6.37(b). Dark-field imaging can be obtained by displacing the objective aperture, as shown in the figure, leading to poorer resolution since the electron beam is now off-axis. As an alternative, the electron gun may be tilted so the primary beam strikes the specimen at an angle. Since the diffracted electrons are now used for imaging, the contrast will be the reverse of that seen under bright-field imaging. The dark-field technique is particularly useful when imaging defects, since the electrons contributing to the image are diffracted from the defect alone.

High-Resolution Mode. Dark-field and bright-field contrast together are known as diffraction contrast. While the diffraction contrast can reveal many microstructural features, it cannot reveal the periodic crystal structure itself. A high resolution technique creates the possibility of revealing

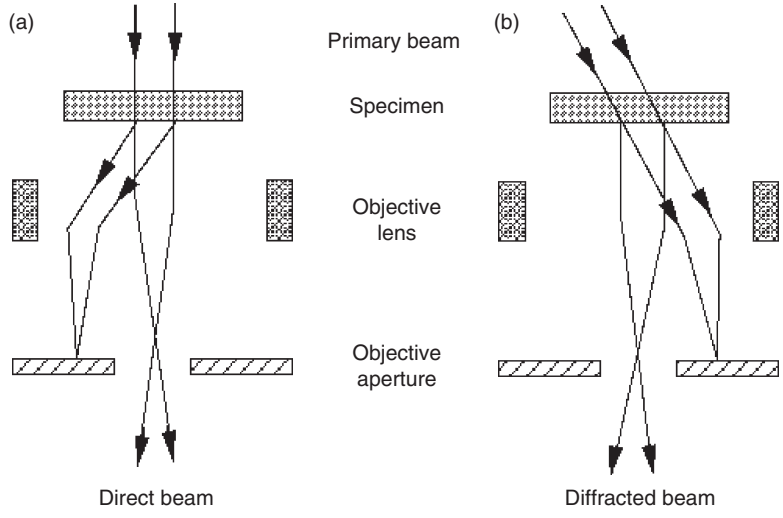


Figure 6.37 Illustration of diffraction contrast: (a) bright-field and (b) dark-field illumination.

Petitioner Samsung Ex-1055, 0356

phase contrast, which can provide periodic crystal structure information. Phase contrast is obtained from the phase difference between a direct beam and diffracted beams. Atomic planes are imaged by opening up the objective aperture to allow one or more diffracted beams through, in addition to the direct beam.

TEM specimen preparation is a destructive and time consuming procedure. The chip is micro sectioned into disks typically 0.5 mm thick and 3 mm in diameter. The disk is then polished to a thickness of several micrometers. An ion etching technique mills the center of the disk to a thickness a tenth of a nanometer or less. The last step is the same conductive coating required in conventional SEM specimen preparation. Temperature substage and strain substage are also employed in TEM investigations. In the failure analysis of plastic packages, SEM is more popular than TEM.

6.7 Atomic Force Microscopy

AFM can be operated in several different modes depending on the application. AFM imaging modes can be classified into two types: static (contact) [24] and dynamic (non-contact). The schematics of AFM are shown in Fig. 6.38. The light from the laser source is reflected by the cantilever, detected by the photodiode, and then processed by the electronics. Thus, topographical information can be obtained from the cantilever position on the specimen surface.

To prevent the AFM cantilever tip from collision with the sample surface and subsequent damage, the distance between the tip and the sample is maintained during scanning by a feedback mechanism [25]. Therefore, the force between the tip and the sample in AFM remains constant and damage is prevented.

Conventionally, the sample in AFM is mounted on a piezoelectric tube that can move the sample in the z direction for maintaining a constant force, and the x and y directions for scanning the sample [26]. An alternative is a "tripod" configuration of three piezo crystals each scanning in the x, y, and z directions. The use of tripod can remove any distortion effects that may be observed with tube scanners. The topography of the sample is the map of the area obtained as a function of x and y.

6.8 Infrared Microscopy

Infrared microscopy is often applied after package opening. Infrared light easily passes through silicon (if not heavily doped) and is reflected by

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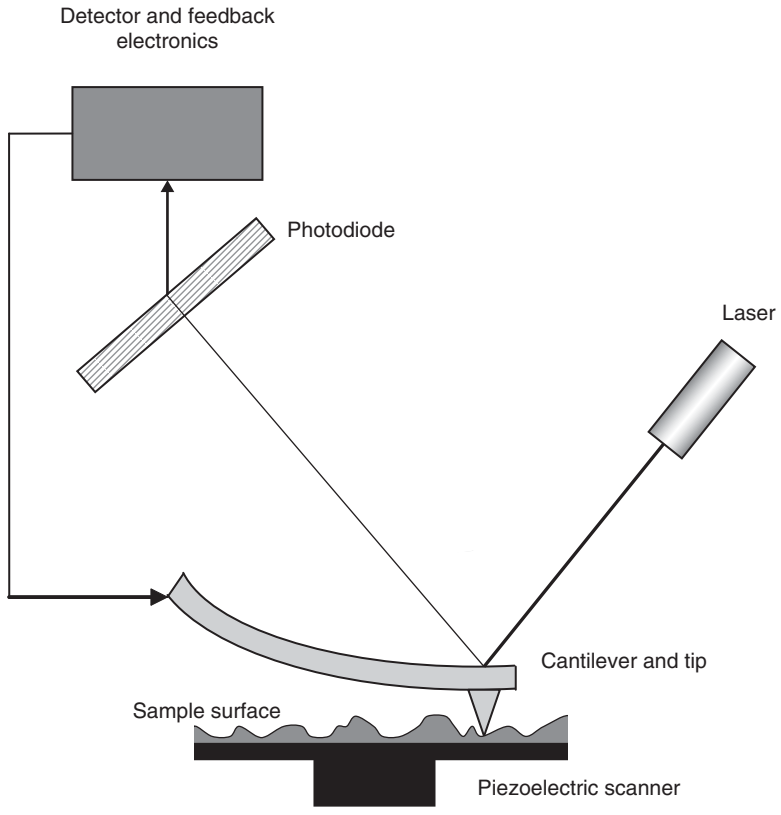


Figure 6.38 Atomic force microscopy schematics.

the object on the opposite surface (e.g., aluminum). Since the bulk of the material in semiconductors is silicon, this allows imaging through the device backside for internal and top surface anomalies (such as chip-outs) and features (such as metal lines). The microscope is also an emission profile imager, which allows the examination of the pattern of IR light being emitted by laser diodes. This is key information for determining the failure mechanism in laser diodes.

In thermal emission detection and analysis, using IR radiation with a wavelength of ~10 μm, the temperature distribution on the device surface can be displayed using a scanning infrared microscope and a gray scale to differentiate the temperatures and pinpoint hot spots. Measurement accuracy depends to a considerable extent on magnification, average temperature, and emissivity. Since silicon is essentially transparent at IR wavelengths of 0.8–1.3 μm, a microscope using special IR transmitting optics, combined with an IR camera and monitor, can readily be employed

Petitioner Samsung Ex-1055, 0358



Figure 6.39 Scanning infrared microscope.

to investigate failure modes in die subsurfaces. Failures at the interface between a gold ball bond and an aluminum metallization pad, sub-surface corrosion of the aluminum metallization, silicon precipitates, and damage due to electrostatic discharge in a device are readily diagnosable. The infrared microscopy can be used for optical inspection through the silicon die, inspection of aluminum-gold bond quality, metal conductor corrosion, die cracks, near-field IR imaging of light-emitting diodes, and semiconductor lasers. Although infrared microscopy is considered very useful for the failure analysis of plastic-encapsulated components, it is not fully satisfactory because of its resolution limit. Infrared microscopy is restricted to the failure analysis of sub-micrometer structures. Moreover, many packaging materials are not IR transparent, so that the transmission IR technique is limited to a few materials, such as silicon and gallium arsenide. Figure 6.39 shows a scanning infrared microscope.

6.9 Selection of Failure Analysis Techniques

The failure analyst must decide which of the various primary and advanced defect and failure analysis techniques should be used to detect

Petitioner Samsung Ex-1055, 0359

defects and failure modes for a particular package. Using inappropriate analysis techniques will affect the analysis and may result in an incorrect conclusion. The failure analysis sequence must begin with NDE followed by destructive techniques. Furthermore, the technique selection can be highly influenced by the consideration of both the condition of the package to be analyzed and the performance of the failure analysis instrument. Significant factors, related to the condition and construction of the package or component, include:

- history (process, application, environment);
- materials;
- structure size;
- geometry;
- possible failure modes; and
- possible location of the failure.

Factors related to the performance of the analysis tool include:

- resolution;
- penetration;
- method (destructive or non-destructive);
- specimen preparation requirement;
- cost; and
- time.

To analyze a failed package the processing and application history of the package should first be obtained. This will help to select the proper failure analysis technique and quickly locate the failure. Electrical bias, temperature, relative humidity, vibration conditions, and radiation are all considered environmental historical conditions of the package. If this information is not available, experience becomes critical. Knowing the construction materials of the package is also important. For instance, metallic materials may cause electromigration induced failure, polymeric materials may lead to moisture absorption related failure, and a package of multiple materials may have a mismatch between coefficients of thermal expansion causing interfacial failure.

Consideration of the size of the components in a package also helps in selecting the proper failure analysis tool. For example, contamination failure on the surface of a plastic package can be identified easily by a conventional optical microscope, while that on the gate surface of a field-effect transistor with a sub-micrometer gate length has to be detected by an

Petitioner Samsung Ex-1055, 0360

analysis tool with high resolution, like a scanning electron microscope. Considering the geometry of a package, possible failure modes, and possible locations of the failure is essential for decisions such as, whether it is necessary to open the package; whether a non-destructive failure analysis technique can be utilized, and so forth.

Reviewing the package status should enable a failure analyst to understand the relevant failure analysis requirements of a particular failed package and select the proper analysis technique that matches the requirements.

Each technique has its own resolution and penetration limits. Figure 6.40 shows an overall comparison of lateral resolution versus depth of penetration for the various failure analysis techniques. X-ray microscopy offers the best depth of penetration, followed by SAM; a 1 μm lateral resolution seems to be the limit. Among these techniques, only electron microscopy (i.e., TEM, SEM, and ESEM) is able to pass the resolution limit. In fact, TEM provides the best resolution. Oxide layers in semiconductor substrates usually are less than 1 μm thick (ranges from a few nanometers to hundreds), so oxide failures are best detected by those techniques.

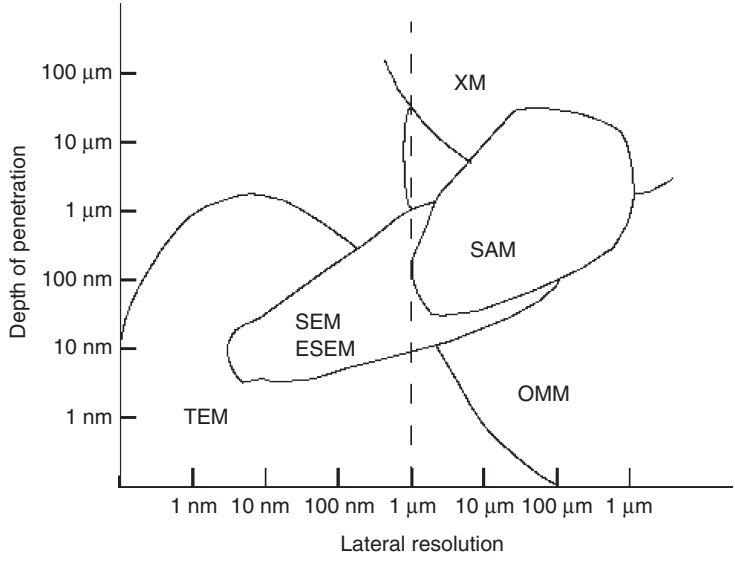


Figure 6.40 Schematic comparison of lateral resolution versus depth of penetration of various failure analysis techniques.

ESEM: Environmental scanning electron microscopy; OM: Optical microscopy; SAM: Scanning acoustic microscopy; SEM: Scanning electron microscopy; TEM: Transmission electron microscopy; XM: X-ray microscopy.

Petitioner Samsung Ex-1055, 0361

Specimen preparation and destructive requirements also must be taken into account. The use of electron microscopes, except for the environmental scanning electron microscope, usually requires destructive specimen preparation, for example, sectioning, layer removal, permanent coating, and package decapsulation. TEM requires specimen sectioning, while conventional SEM requires at least conductive coating. Some failure modes in microelectronic packages, such as microcracking, interfacial delamination, and debonding, can be introduced by specimen preparation, confusing the analyst.

Fortunately, a number of non-destructive analysis techniques, such as SAM and X-ray microscopy, can be used to detect internal failure modes. These non-destructive techniques, however, cannot provide images with high resolution. A compromise needs to be achieved between resolution and non-destructive methods. Among the previous failure analysis techniques, it is evident that the ESEM and AFM perform with relatively high resolution and without requiring layer removal or permanent coating, but ESEM and AFM detect only failures exposed on the specimen surface; they cannot image internal failures in plastic packages without decapsulation. The most effective defect and failure analysis method is to first detect the internal failures using non-destructive techniques and then confirm by cross-sectioning or decapsulation and application of higher resolution analysis tools.

Generally, the failure analysis with the higher resolution techniques will cost more, and will take longer if specimen preparation is required. TEM (0.2-nm resolution) usually costs 30–40 times more than optical microscopy (1-μm resolution). There are, however, some exceptions, especially for newly developed failure analysis techniques. Commercialized AFM competes in resolution with scanning electron microscope (2–5 nm), and costs only about 20% of the latter. The cost also depends on other factors. SAM gets similar results, or even lower if a low frequency transducer is employed. Its resolution is comparable to that of optical microscopy.

Defect and failure analysis techniques related to the encapsulation are listed in Table 6.4. External and package failure modes can be inspected without decapsulation. Internal failure modes usually require decapsulation for failure inspection, unless non-destructive techniques like SAM or X-ray microscopy are utilized. In most cases, more than one technique is listed in Table 6.4 for analyzing a particular defect or failure mode. These provide alternatives when resolution or location of the failure must be taken into account. SAM, for instance, is the proper selection for detecting interfacial delamination because of its non-destructive penetration ability. However, the resolution of SAM is not high enough to inspect

Petitioner Samsung Ex-1055, 0362

Table 6.4 Encapsulation Defects and Failures and Proper Analysis Techniques

Defect or Failure	Analysis Technique
Wire sweep	XM, OM
Paddle shift	XM, OM
Encapsulant voids or foreign particles	SAM, SEM, ESEM
Encapsulant cracks	OM, ESEM, SEM, EDX, SLAM
Encapsulant/die delamination	SAM, IRM, ESEM, SEM, OM, SLAM

EDX: Energy dispersive X-ray spectroscopy; ESEM: Environmental scanning electron miscroscopy; IRM: Infrared microscopy; OM: Optical microscopy; SAM: Scanning acoustic microscopy; SEM: Scanning electron microscopy; SLAM: Sacanning laser acoustic miscoscopy; XM: X-ray microscopy.

interfacial delamination in devices with a sub-micrometer scale, such as very large-scale integration (VLSI) and ultra-large-scale integration (ULSI) devices. ESEM is recommended for those cases, but care must be taken because the cross-sectioning of the specimen may be required. Often, two or more analysis techniques are employed in order to confirm a particular defect or failure mode.

6.10 Summary

Defect and failure analysis technique play key role in producing high quality and reliable encapsulated microelectronic packages. The most effective sequence of failure analysis consist of nondestructive evaluation followed by destructive techniques. Non-destructive methods include optical microscopy, X-ray microscopy, scanning acoustic microscopy, and atomic force microscopy. Prior to NDE, complete electrical testing is conducted to reveal failure mode and possibly failure site.

Destructive evaluation includes analytical testing of the encapsulant material, decapsulation, internal evaluation, selective layer removal, failure simulation, and final examination. Internal evaluation after decapsulation and cross-sectioning may involve electron microscopy, optical microscopy, infrared microscopy, and XRF spectroscopy.

The use of high resolution electronic microscopy has increased with the booming popularity of VLSI and ULSI. Conventional SEM and TEM require high vacuum conditions and specimen coating preparation. Environmental scanning electronic microscopy allows investigation of

Petitioner Samsung Ex-1055, 0363

microscopic morphologies under controlled environmental conditions without conductive coating, and has become an attractive technique for microstructural characterization of microelectronic packages. The advantage ESEM particularly facilitates is investigation of devices with dielectric materials, such as polymers and ceramics. Both static and cyclic environmental effects on different package levels can be dynamically investigated using ESEM.

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Petitioner Samsung Ex-1055, 0364

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Petitioner Samsung Ex-1055, 0365

7 Qualification and Quality Assurance

Electronic packages must conform to specific quality and reliability requirements in their intended applications. Quality is the degree of conformance of a product to the relevant specifications, guidelines, and workmanship criteria. Electronic packages must exhibit features and characteristics that are within specified tolerance ranges. Reliability is defined as the ability of a product to perform its function without failure and within specified performance limits, for a specified time, at specified life-cycle application conditions. In simple terms, reliability is the probability of survival, or the probability of not failing.

To evaluate quality and reliability, electronic packages must undergo a process known as "qualification." Qualification is the process of demonstrating that an electronic package is capable of meeting or exceeding the specified quality and reliability requirements. It includes verification of their function and performance, validation in the system application (if applicable) and qualification for processability and reliability [1,2]. It aims to evaluate performance of electronic packages under specified operating and environmental conditions within a specified period of time.

Qualification process includes virtual qualification, product qualification, and mass production qualification. Virtual qualification is used to qualify the design of an electronic package according to the reliability requirements. Product qualification is used to evaluate the prototype of the electronic package. Mass production qualification takes place during the mass manufacturing of the products to verify quality and functionality. Packages with defects (unintended features that exhibit non-conformity to quality) can be identified and removed through a series of tests called quality assurance testing or "screening." Physics-of-failure (PoF) facilitates the qualification process by providing understanding of the failure mechanisms in electronic packages to make the qualification more effective.

In this chapter, first a brief history of qualification and reliability assessment is provided. Then, the qualification process for electronic packages is presented. Various stages of the qualification process including virtual qualification, product qualification, and mass production qualification (i.e., quality assurance testing or screening) are discussed. Quality assurance process is further discussed including types of screening tests, screening stresses and duration, screening within process flow, and screening reduction and elimination.

Petitioner Samsung Ex-1055, 0366

7.1 A Brief History of Qualification and Reliability Assessment

Qualification and reliability assessment can be dated back to 1940s during World War II when a team led by Dr. Wernher von Braun developed the first reliability model for the V-1 missile [3–5]. Long before that, however, engineers have naturally strived for reliable or failure-free products. For example, in 1860 A. Wohler obtained a fatigue failure curve known as the "S-N curve" which showed the applied stress (S) versus number of cycles to failure (N) for a mechanical element [3]. Using the S-N curve, the product was designed to be failure free below a certain application stress.

The first reliability assessments for electronics took place in 1950 when an ad hoc group was formed on reliability of electronic equipment which was then followed by the formation of the Advisory Group on the Reliability of Electronic Equipment (AGREE) in 1952 by US Department of Defense. One of the first reliability handbooks was titled *Reliability Factors for Ground Electronics Equipment* published by McGraw-Hill in 1956 and sponsored by the Rome Air Development Center (RADC).

In November of 1956, a publication titled *Reliability Stress Analysis for Electronic Equipment* was released by RCA (Radio Corporation of America). This publication presented models for calculating failure rates for components and for the first time, the concept of activation energy and the Arrenhius relationship were included. Other reliability publications soon followed including the *RADC Reliability Notebook* in 1959, *Reliability Applications and Analysis Guide* in 1960, *Failure Rates* in 1962, and the military handbook known as MIL-HDBK-217 in 1965 [6].

The MIL-HDBK-217 published by the Navy provided only a single point failure rate of 0.4 failures per million hours for application to all monolithic integrated circuits. In 1973, a new reliability prediction model was developed by RCA based on previous work by the Boeing Aircraft Company. The proposed model was composed of two additive portions: a steady-state temperature-related failure rate and a mechanical failure rate. The characteristics of the devices were considered only as a pair of complexity factors, and the failure distribution during the operation lifetime was assumed to be exponential. This model was published as MIL-HDBK-217B by the Air Force. Other versions of MIL-HDBK-217 have been published such as C, D, E, and F containing modifications to the original reliability models.

Petitioner Samsung Ex-1055, 0367

Reliability modeling and prediction has come a long way since its infancy. Earlier reliability models for integrated circuits that used single value failure rates were less accurate and did not consider the effect of stresses, materials, and configuration. The failure data collected at that time was affected by factors such as equipment accidents, repair blunders, improper reporting, and mixed operational environmental conditions conspiring to produce a failure rate that appeared to be constant [7]. Furthermore, the early generations of electronic components were plagued by intrinsically high failure rates [8]. The failures due to infant mortality and wearout mechanisms with multi-modal subpopulations would have resulted in a roughly constant failure rate during the operation lifetime.

The failure rate curve for an electronic component generally consists of three types of failures: infant mortality, random, and wearout failures. Infant mortality failures are attributed to defects and flaws in the electronics product due to manufacturing and assembly processes. The second portion of the curve is the constant random failure rate during the normal life of the product due to unknown and random causes. The third portion is the failure rate due to wearout failures which increase over time. One of the initial failure rate curves depicting the three types of failures is referred to as the "bathtub curve" as shown in Fig. 7.1. The infant mortality failure rate in this case continuously decreases with time.

Several studies have shown that the bathtub curve may not accurately represent many electronic failures [7–10]. Infant mortality failure rate may consist of multi-modal failure rate distributions in the early phase of component operation lifetime as shown in Fig. 7.2. Such a failure rate

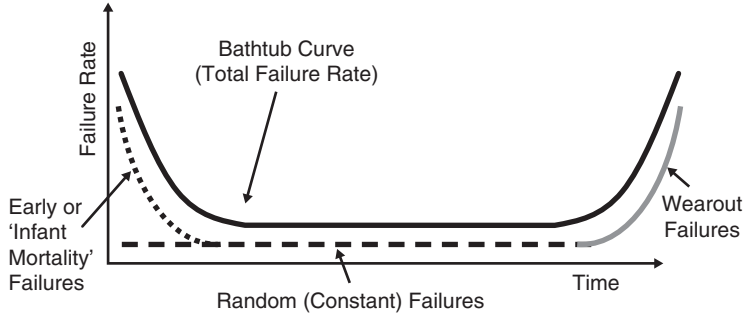


Figure 7.1 Bathtub curve consisting of infant mortality and random and wearout failures.

Petitioner Samsung Ex-1055, 0368

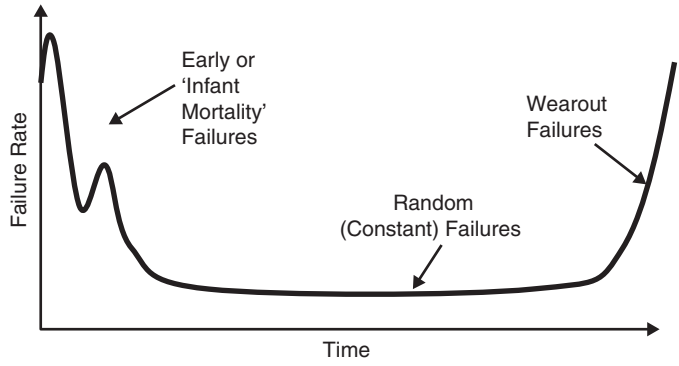


Figure 7.2 The rollercoaster curve [7].

curve is referred to as the "rollercoaster curve." In failure rate curves similar to the one shown in Fig. 7.2, while each failure rate subpopulation is increasing, the population for the early failures may still be decreasing as a whole.

With improvements in failure analysis techniques, root-cause analysis, and physical modeling, the reliability evaluation of electronics has evolved from purely probabilistic assessments based on field failure data to predictive models based on PoF mechanisms which incorporate the package characteristics and life-cycle loads. The PoF concepts pioneered by Pecht et al. in the 1990s have provided the contemporary electronics community with a unified approach in dealing with electronics reliability. The key philosophy is to develop a fundamental understanding of the underlying mechanisms that govern the degradation of electronics hardware. Then, by assigning rate constants or maximum limits to these various failure mechanisms, insight is obtained with regard to the anticipated lifetime of the electronics [11–18].

The PoF approach involves the identification and understanding of the physical processes (or mechanisms) that cause degradation and ultimately produce failure. It is an approach to the design and development of reliable product to prevent failure, based on the knowledge of root cause failure mechanisms [2]. The PoF approach can be used in reliability engineering applications including design-for-reliability, reliability prediction, test planning, and prognostics. To be used in design and test of a product, PoF requires that the product and its anticipated life-cycle loading profile are sufficiently defined to identify potential failure sites and failure mechanisms.

Petitioner Samsung Ex-1055, 0369

A failure mechanism is the physical (e.g., chemical, mechanical, thermodynamic) process that causes degradation at sites which may lead to product failure. Whether a specific failure mechanism will be active in a product and cause failure, will depend on the environmental (e.g., temperature, humidity, contaminants, radiation) and the operating (e.g., voltage, current, generated temperature) load conditions. In addition to loading conditions, failure mechanisms depend on the product architecture and materials. The life predictions from PoF based models can be further verified using properly designed accelerated tests that consider the effects of various stress stimuli on the electronic product.

Identification of failure mechanisms as the basis of reliability assessment and qualification test design for a system has been accepted by the EIA/JEDEC and SEMATECH, an association of semiconductor manufacturing companies like Intel, IBM, AMD, Infineon, Phillips, and Texas Instruments. Intel's product qualification method [19] consists of the following actions:

- defines environmental loads, lifetime and manufacturing use conditions based on target market segments (e.g., desktop, server, notebook);
- determines probable stresses with reliability implications;
- estimates stress levels for modeling and the modes of testing (e.g., stand alone, board mounted);
- defines accelerated stress conditions necessary to identify failure mechanisms;
- determines final stress conditions for testing follow the PoF principles.

The IEEE (Institute of Electrical and Electronics Engineers) 1413 standard [20] identifies the framework for the reliability prediction process for electronic systems (products) and equipment. An IEEE 1413-compliant reliability prediction report must include reasons why the reliability predictions were performed, the intended use of the reliability prediction results, cautions as to how the reliability prediction results must not be used, and where precautions are necessary.

Traditionally, most aspects of design, development, testing, and qualification of electronics and electronic equipments have been controlled by specifications, standards, handbooks, regulations, and guidebooks [21]. This is especially the case for military electronics which have been required to conform to strict military specifications or "specs" (MILSPECS). The objective of the specs was to narrow the uncertainty and variability with

Petitioner Samsung Ex-1055, 0370

regard to design, product, reliability, etc.; however, over time the specs have become more burdensome than beneficial.

With rapid technological advancements, significant problems have been encountered regarding the implementation and updating of handbooks and specifications, leading to numerous exceptions, bureaucracies, document pile up, and staff increase and a quagmire of regulations that could only be understood by limited expert contractors. As the microcircuit industry began to grow rapidly and the electronic components usage increased, the commercial electronics industry started to differentiate from the military in 1960s. Commercial equipment manufacturers realized that each supplier had different designs and processes requiring the use of tailored process controls rather than a single common approach.

The reliability prediction methodologies including models based on field data, test data, physics of stress and damage, and handbooks are compared in Table 7.1. The aspects compared are taken from IEEE Reliability Prediction Standard 1413 [20] which identifies the key required elements for a credible reliability prediction. The handbooks listed are from companies and organizations including Reliability Analysis Center, Bell Communications (now Telecordia), Society of Automotive Engineers (SAE), and the US military.

Qualification must include the appropriate reliability prediction methodology that identifies the failure modes, mechanisms, product characteristics, and life-cycle environmental stresses. Qualification process is planned with respect to the failure rate characteristics of the product including infant mortality, random, and wearout failures. Infant mortality failures are reduced or eliminated by quality assurance methods including manufacturing process improvements and statistical control, and if necessary, by screening. Wearout failures are predicted and designed against during design and product qualification. The advancements in reliability models and prediction methods have led to a more comprehensive and effective electronics qualification process.

7.2 Qualification Process Overview

The qualification process is composed of three stages: virtual qualification, product qualification, and mass production qualification as depicted in Fig. 7.3. Virtual qualification, also known as “design qualification,” is the evaluation of the functional and reliability performance of the product design without any physical testing on the product. Virtual qualification involves using computer-assisted modeling and simulation based on PoF

Petitioner Samsung Ex-1055, 0371

Table 7.1 Comparison of Various Reliability Prediction methodologies [5]

Included or Identified?	Field Data	Test Data	Stress and Damage Models	Handbook Methods				
				MIL-HDBK-217	RAC's PRISM	SAE's HDBK	Telecordia SR 332	CNET's HDBK
Methodology source	Yes	Yes	Yes	No	Yes	No	No	No
Assumptions	Yes	Yes	Yes	No	Yes	Yes	Yes	No
Sources of uncertainty	Can be	Can be	Can be	No	No	No	No	No
Result limitations	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Failure modes	Can be	Can be	Yes	No	No	No	No	No
Failure mechanisms	Can be	Can be	Yes	No	No	No	No	No
Confidence levels	Yes	Yes	Yes	No	No	No	No	No
Life-cycle environmental conditions	Can be[1]	Can be[2]	Yes[3]	No[4]	No[4]	No[4]	No[4]	No[4]
Materials, geometry, and architecture	Can be	Can be	Yes	No	No	No	No	No
Part quality	Can be	Can be	Yes	Yes	No	No	Yes	Yes
Reliability data and experience	Yes	Yes	Yes	No	Yes	No	Yes	No

[1]If field data is collected in the same or a similar environment which accounts for all the life-cycle conditions.
[2]It can consider through design of the tests used to assess product reliability.
[3]As input to physics-based models for the failure mechanisms.
[4]It does not consider the different aspects of environment.
CNET: Center National D'Etudes des Telecommunications (French National Center for Telecommunications Studies); RAC: Reliability Analysis Center; SAE: Society of Automotive Engineers.

Petitioner Samsung Ex-1055, 0372

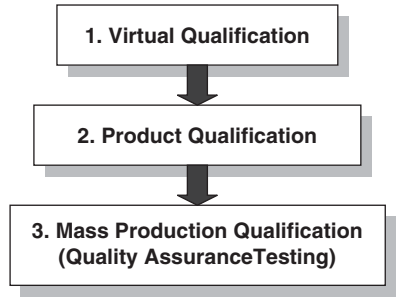


Figure 7.3 Qualification process stages.

mechanics, and therefore, it is also referred to as the physics-of-failure-based approach [22].

Product qualification is the evaluation of the product based on the physical testing on the manufactured prototype. Product qualification tests are very often applied under accelerated stress conditions (thus known as accelerated testing) and verify whether the product has met or exceeded its intended quality and reliability requirements. The conditions and types of accelerated tests can be determined from preliminary physical tests that identify the strength limits of the product prototype.

After virtual and product qualification, the electronic packages are mass produced. During and after the manufacturing process, the products are inspected and tested to evaluate their quality and defective parts are screened out. This process is the third stage in the overall qualification process, and is more commonly referred to as quality assurance testing or screening.

Virtual and product qualification efforts are part of a larger process of product design and development as shown in Fig. 7.4. At various intersections of the process, maturity levels can be assigned to indicate progress and specific readiness for the next phase. The design and product qualification process may include feedback iterations shown in Fig. 7.5. If the product design is found to be unqualified during the virtual qualification process, it is modified and then virtually re-qualified before proceeding to the next phase. Similarly, when a design has successfully passed through the virtual qualification process, but does not meet the qualification requirements during product qualification stage, feedback iterations may be necessary. In this case, the virtual qualification process and specifically, the PoF based models may have to be re-evaluated and modified. After design completion, the product is manufactured in high volume and subjected to quality assurance testing during and after the process.

Petitioner Samsung Ex-1055, 0373

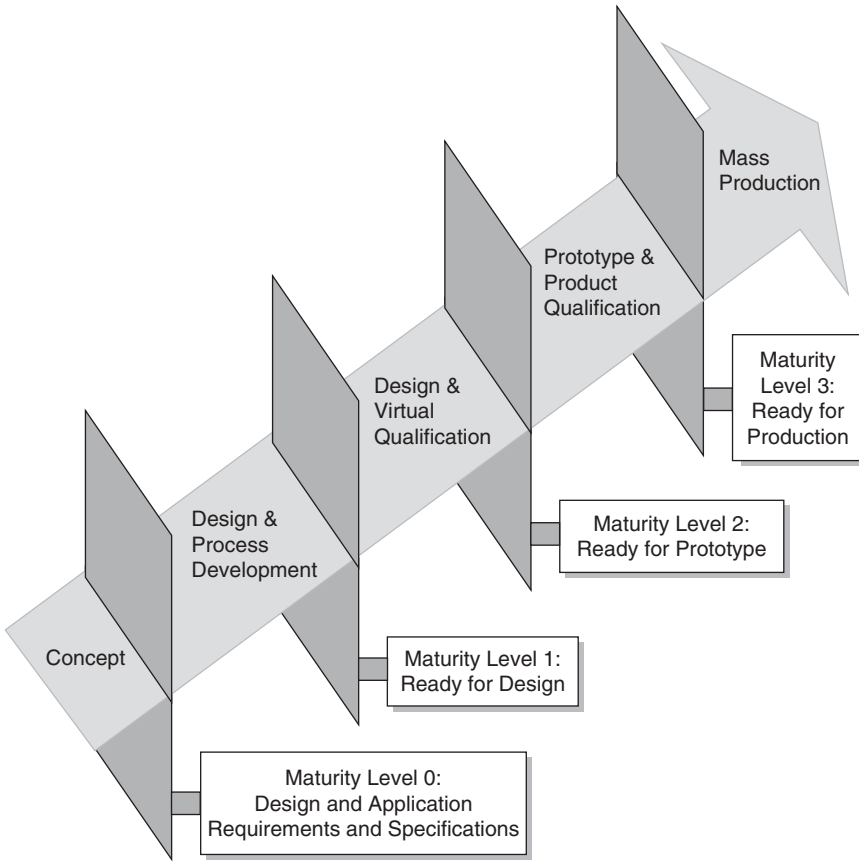


Figure 7.4 Virtual and product qualification within the product development process flow (Freescale Semiconductor Inc., http://www.freescale.com/files/abstract/misc/CPA_QA_HANDBOOK.pdf).

A qualification process must:

1. Determine the aim of the specific qualification process in terms of nominal design aim and application requirements. For example, a requirement may be that the number of failed electronic parts should not exceed 4 out of 500 which is equivalent to 0.8% failure rate or 99.2% reliability.
2. Identify the potential failure mechanisms and modes associated with failure sites (during manufacture, system assembly, transportation, storage, and service), and determine the relevant acceleration models and factors.

Petitioner Samsung Ex-1055, 0374

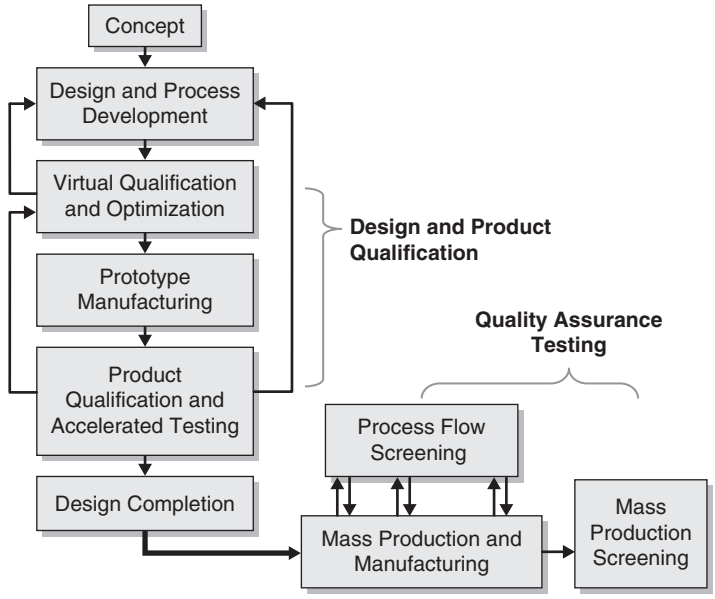


Figure 7.5 Qualification and quality assurance testing within the product design and manufacturing process flow including iterative feedback process.

3. Determine the strength limits under environmental and operational conditions. Environmental stresses may include temperature, moisture, contaminants, and thermo-mechanical stresses. Typical operational stresses include time and spatial dependent electrostatic discharge, current, and voltage.
4. Select stress types and stress levels for qualification tests according to identified failure mechanisms. The acceleration factor and strength limits should be considered to select proper stress levels.
5. Conduct qualification tests and collect necessary failure data to assess the quality and reliability of the product. A sample size is chosen to achieve the qualification goals and also by considering the tradeoff of cost and time. Proper failure criteria should be defined to identify failures from monitored parameters.
6. Interpret test data to evaluate the quality and reliability of the product. The evaluation results should also be used to calibrate PoF model predictions. Results and conclusions with feedback should be reported for continuous design and process improvement.

The objectives of qualification testing are to (a) evaluate the quality of a product to see if it meets the design requirements, (b) develop information

Petitioner Samsung Ex-1055, 0375

on the integrity of a device and its structure, (c) estimate the expected service life and reliability, and (d) evaluate the effectiveness of materials, processes, and designs. Qualification tests estimate expected life and design integrity of a device. Most tests are not conducted under the normal application conditions, but at accelerated levels of stresses to accelerate potential failure mechanisms at associated sites in a device.

Successful qualification of a sampling of microelectronic packages does not assure that all packages made by the same manufacturer to the same specifications will also meet the qualification requirements. Qualification should be conducted by the manufacturer, although the customer may do so for special applications. Data from all possible sources should be used in qualification. These sources include material and component suppliers' test data, qualification data from similar items, and accelerated test data from materials, components, and subassemblies.

7.3 Virtual Qualification

Virtual qualification is the first stage of the overall qualification process. It is the application of PoF based reliability assessment to determine if a proposed product can survive its anticipated life cycle. Virtual qualification (also called simulation-assisted reliability assessment) assesses whether a part or system can meet its reliability goals under anticipated life-cycle profiles based on its materials, geometry, and operating characteristics. The technique involves the application of simulation software to model physical hardware to determine the probability of the system's meeting desired life goals [23–25].

Virtual qualification can be applied at the design stages and, hence, it allows the reliability assessment process to be moved into the design phase [26,27]. It allows the design team to consider qualification at the initial stages of design, technology and functional definition, and supplier selection. This methodology takes advantage of advances in computer-aided engineering software permitting components and systems to be qualified based on analysis of the susceptibility of their designs to failure using the critical failure mechanisms and the applicable failure models associated with them. The reliability assessment tool assesses the designs for reliability in the environments present in the life-cycle profile, using a database of validated PoF models. It calculates times-to-failure (TTFs) for the mechanisms that cause failures and evaluates the effects of different manufacturing processes on reliability by calculating the TTF as a function of typical manufacturing tolerances and defects.

Petitioner Samsung Ex-1055, 0376

Virtual qualification facilitates selection of cost-effective test parameters for validating reliability assessment and design and also aids in the selection of components by providing information on their impact on reliability. Because the virtual qualification process does not involve manufactured prototypes and physical testing, it is a much more economical and time-efficient process compared to a manufactured product qualification process [28].

The flowchart of the virtual qualification process is shown in Fig. 7.6. The inputs consist of life-cycle profile and product characteristics. The life-cycle profile can be further categorized as environmental and operational stresses as shown. The inputs are fed into a PoF model and simulation

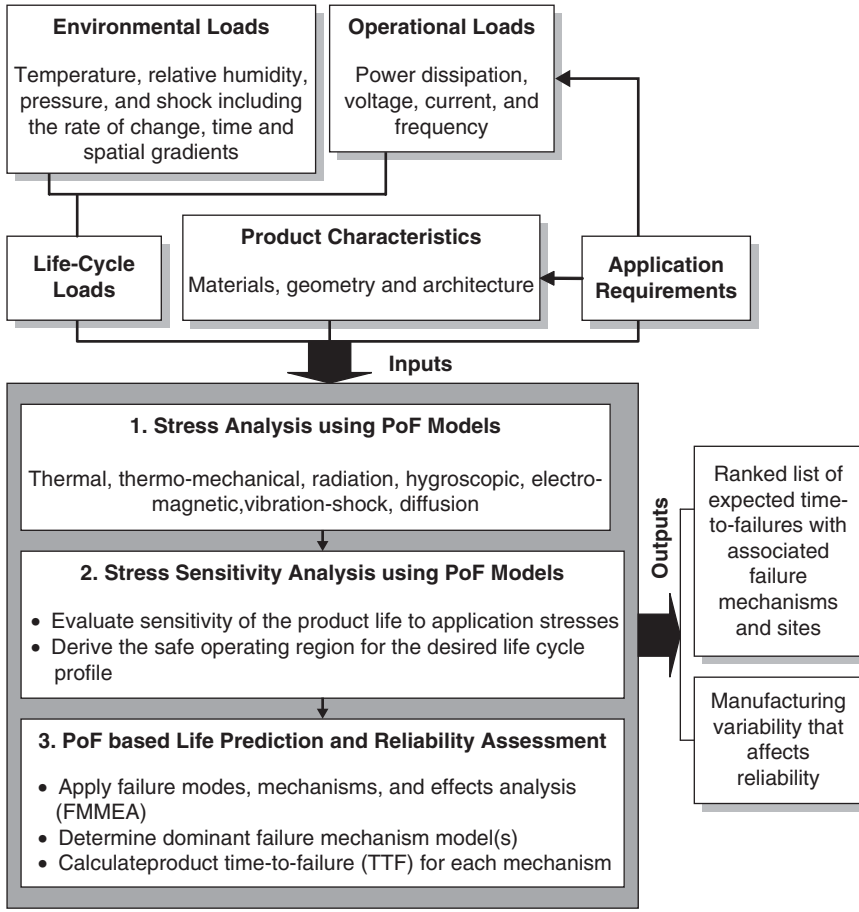


Figure 7.6 Flowchart of virtual qualification.

Petitioner Samsung Ex-1055, 0377

software where stress analysis, reliability assessment, and stresses sensitivity analysis are performed. The outputs of virtual qualification are predicted TTF based on the most dominant failure mechanisms, stress margin conditions, and screening and accelerated testing conditions.

In addition to TTF prediction and reliability assessment, virtual qualification combined with advanced optimization techniques can be used to optimize the design criteria including cost, electrical performance, thermal management, physical attributes, and reliability. By examining potential trade-offs between the aforementioned criteria, ideal values can be achieved for specific applications.

In the virtual qualification process, it is imperative to use the most accurate inputs including material properties, design configuration, dimensions, and operational and environmental conditions. Furthermore, the failure mechanism models used in TTF prediction and reliability assessment must be valid. If the data or models on which the virtual qualification is performed is inaccurate or unreliable, any qualification results based on the data or models are suspicious.

7.3.1 Life-Cycle Loads

A well-designed electronic package must survive the loads applied during storage, handling, transportation, and operation. Furthermore, the subassemblies of the products must survive subsequent manufacturing and assembly loads. The qualification process must therefore, simulate all the loads that a package is subjected to in its lifetime, known as the "life-cycle loads."

Life-cycle loads can be classified as operational and environmental loads. Operational loads include power dissipation, voltage, current, frequency, etc. Environmental loads are those loads that the electronic package is subjected to during manufacturing, storage, transportation, handling, and operation. Operational loads include conditions such as mean temperature, temperature limits, number, and limits of typical temperature cycles [29], humidity, vibration, mechanical shocks, radiation, contaminants, and corrosive environments. The level of these loads along with net change, rate of change, and the duration of exposure are important determinants of the magnitude of stresses induced in a product.

The environmental conditions used in the virtual qualification are the conditions experienced by the electronic package, and measured (or predicted) near the package. The system level conditions may or may not be relevant depending on the influence of exterior environment on the

Petitioner Samsung Ex-1055, 0378

package conditions and whether temperature and humidity control system is used.

Environmental loads range from controlled and relatively benign to extreme and harsh. An example of a controlled environment is the telephone exchange, where the electronic device case temperature is relatively constant and the humidity is maintained at a desired level. Conversely, microelectronic devices inside a laptop computer located in an enclosed car during summer season may be subjected to high thermal loads or the electronics mounted in a missile system can be subjected to severe temperature, humidity, and high levels of pyrotechnically produced vibration and mechanical shock during a missile launch.

In application conditions where the environment is not controlled, the load profiles of temperature, humidity, vibration, contamination, and radiation level as a function of time are often predicted based on past experience. Primary stresses experienced by devices mounted in systems operating in some typical environments are listed in Table 7.2. Climatic data can be found in military handbook MIL-HDBK-310 and IPC-SM-785 [30]. Automotive environmental conditions can be found in J1211 "Recommended Environmental Practices for Electronic Equipment Design" and in JASO D001 "General Rules of Environmental Testing Methods for Automotive Electronic Equipment." SAE Recommended Practice J1879 "General Qualification and Production Acceptance Criteria for Integrated Circuits in Automotive Applications" provides further detailed information for integrated circuit qualification testing.

The load conditions imposed by the manufacturing processes must be accounted for in the design and qualification of a product. Examples of manufacturing conditions that may be of relevance and that may need to be considered in the design and qualification of a device include electrostatic discharge, soldering temperature, rate of change of temperature during soldering, duration of exposure to solder heat, flux used for soldering, cleaning agents and solvents, mechanical agitation used during cleaning operation, liquid quenching after soldering, and terminal forming operations. Often rework conditions such as repair of neighboring components or devices that include exposure to hot air, cleaning agents, and solvents are important and require explicit testing for device reliability. Storage conditions are especially important for plastic-encapsulated memory devices because storage may affect the state of the memory cells within the device.

Since a product may experience numerous loads, it is necessary to identify the critical loads that are applied to the product. Some of the loads

Petitioner Samsung Ex-1055, 0379

Table 7.2 Life-Cycle Loads in Key Applications

Application	Use Environment							Manufacturing Conditions (°C)	Storage Conditions (°C)
	T_{min} (°C)	T_{max} (°C)	ΔT* (°C)	t_D** (hrs)	Cycles/year	Humidity	Vibrations		
Consumer goods	0	60	35	13	365	Low	Low	25–215	–40 to 85
Computers	15	60	20	2	1460	High	Low	25–260	–40 to 85
Tele-communications	–40	85	35	12	365	High	Medium	25–260	–40 to 85
Commercial aircraft	–55	95	20	2	3000	High	High	25–260	–55 to 125
Automotive (under hood)	–55	125	100	1	300–2200	High	High	25–215	–55 to 125
Missile	–65	125	100	1	1	Low	Pyrotechnic shock, acoustical noise	25–260	–60 to 70

*The cyclic temperature swings are not the difference between the maximum and minimum temperatures that can be experienced; they are significantly smaller and move between the extremes primarily due to seasonal and geographic variations.
**t_D is the time duration for the temperature cycle.

Petitioner Samsung Ex-1055, 0380

will play major roles in activating and accelerating the failure of the product, while other loads can be ignored. For example, radiation can often be ignored for ground based electronic products, since the radiation level is too low to affect the function of product or cause any damage. The same load may also be considered to have different criticality for different products under different conditions. For example, a mechanical shock caused by dropping a cell phone onto hard ground, while may be critical to the electronic parts in the cell phone, may have no effect on a product without electronics. The loads that can or cannot be ignored depend on the critical failure mechanisms that are identified in the analysis steps.

7.3.2 Product Characteristics

The characteristics of the product design such as package dimensions, materials, types, and configurations must be included in the virtual qualification process. Materials used to construct a product can influence the stress at potential failure sites within the product due to external and internal loads and the process of damage accumulation. To determine the extent to which the materials influence stress and damage, their physical properties also need to be used as inputs to PoF-based failure models. For example, a failure in a solder joint may be driven by stress arising from repeated temperature excursions through a fatigue failure mechanism. In this case, the coefficient of thermal expansion of a material is needed to determine the cyclic stress state. In another case, a failure may occur due to reduction in contact force between connector elements through a stress relaxation mechanism. This condition will require the elastic modulus of the connector elements, loading elements and their housings to determine the contact force and its degradation pattern. Properties for common materials used in electronic products can be found in references.

Products are not normally produced by a single manufacturing process, but require a sequence of different processes to achieve all the required attributes of the final product. These manufacturing process steps apply stresses on materials and as a result residual stresses may be present in the final products. The manufacturing processes may even modify some of material properties. Material property inputs to PoF-based assessments must reflect the final properties, final values, and their tolerances after the completion of the manufacturing processes. Properties of general electronic packaging materials can be found in the references [31,32].

Since the physical sample or prototype is not available at this stage, the manufacturing quality control and tolerances must be taken into account to

Petitioner Samsung Ex-1055, 0381

ensure accuracy. It is important to note that the quality control processes and tolerances of different device manufacturers can vary greatly. Therefore, their specific design, production, test, and measurement procedures must be evaluated and certified. For example, simply obtaining and using a material property value from the literature as input in the virtual qualification analysis may not produce accurate results. It may be acceptable for preliminary calculations; however, accurate virtual qualification results can only be obtained if the range of properties based on different material processing are also considered.

7.3.3 Application Requirements

While the environmental loads define the conditions under which the product must operate, the application requirements define what the product is expected to do in such conditions during its useful life. The application requirements are based on the customer's needs and the supplier's capabilities. These requirements can involve the component's functional, physical, testability, maintainability and safety characteristics.

Application requirements directly influence operation loads and product characteristics. Application requirements are usually stated in terms of nominal and tolerance ranges of parameters such as electrical outputs, mechanical strength, corrosion resistance, appearance, moisture protection, and duty cycle. Often, there are multiple requirements, which could compete (e.g., many products are expected to be both strong and light or thermally conductive and electrically resistive).

All of the requirements must be acceptable by both the supplier and the customer in order for reasonable qualification tests to be defined. This is often difficult, and if all the relevant requirements cannot be known, then reasonable assumptions must be made. Sometimes, the customer's requirements are not well defined, or the customer is reluctant to give assent to some assumptions. In this case, the only recourse available to the manufacturer is to make the best assumptions possible and to inform the customer. It is never acceptable to simply ignore a requirement.

7.3.4 Reliability Prediction using PoF Approach

The PoF approach and modeling is the essential part of the virtual qualification process. Since, no physical tests are performed during virtual qualification, the accuracy and completeness of the models and simulation tools based on PoF mechanisms are critical.

Petitioner Samsung Ex-1055, 0382

The TTF and reliability prediction and assessment tools based on PoF must also exhibit a diverse array of capabilities. It should be able to predict reliability of products under a wide range of environmental conditions. It should be able to predict TTF for fundamental failure mechanisms. The effect of different manufacturing processes on reliability should be considered. This software tool is the cornerstone of the virtual qualification process.

In PoF methodology, the product environmental conditions must be input as a series of defined stresses such as thermal, thermo-mechanical, hygro-mechanical, shock, and vibration. The results from stress analysis are used with the stress response of the selected product design characteristics to identify the failure modes, and mechanisms associated with failure sites. To predict reliability, the TTF at identified failure sites for the anticipated use conditions must be determined.

Numerical and/or analytic models that are based on failure mechanisms and forecast TTF are used to make PoF-based reliability predictions. These models may be referred to as failure models or PoF models. PoF models provide the different stress–time relationships, which describe the failure mechanisms [2]. In general, inputs to these failure models include specific product geometry and material information, as well as stress information. Stress information needs to include stress levels as well as duration or frequency of application of stress. The TTF predicted by a failure mechanism generally represent time to specific percentage of failure depending on how a model is developed and validated.

Since the inputs to all the models have known or expected levels of uncertainties associated with them, simulation of those uncertainties allow development of a series of possible TTFs and the statistical distribution that represents the failure probability over time. Using these distribution parameters, confidence interval can be associated with the estimated TTFs and other reliability parameters. After the calculation, the lowest TTF resulted by the dominant failure mechanism and site is selected as the predicted service life of the device. This information can be used to determine whether a device will survive in its intended application.

In the PoF approach, specific PoF based models must be employed to describe the failure mechanisms [33]. In PoF models, the stresses and the various stress parameters and their relationships to materials, geometry, and product life are considered. Each potential failure mechanism is represented by one or more of the prevalent models. For electronic products, there are many PoF models describing the behavior of components like printed circuit boards (PCBs), interconnections, and metallization under various

Petitioner Samsung Ex-1055, 0383

conditions, such as temperature cycling, vibration, humidity, and corrosion. A model should provide repeatable results, be sensitive to the variables and interactions that are causing degradations and failures, and predict the behavior of the product over the entire domain of its operational environment. This type of a model allows development of accelerated tests and also allows transformation of the accelerated test results to application conditions.

Many PoF models are available in literature, such as a strain range based model for solder joint fatigue [34], which describes temperature-cycle-induced solder interconnect fatigue; Black's model and its variations [35], which describes electromigration in semiconductor device metallization; the Fowler–Nordheim model [36], which describes the time-dependent dielectric breakdown due to tunneling in gate oxide devices; and Pecht and Rudra model [37] that described conductive filament formation in the PCB. Models applicable to electronic products are available in references [29,38,39]. If no models are available or if the models are found to be not applicable to the specified failure sites and loads, then new models can be developed. The new models are created by using controlled experiments that identify the design and environmental factors governing failure and the mathematical relationship linking those factors to the TTF. New failure mechanisms or variations of known failure mechanisms in products usually arise with the introduction of new materials and/or technologies. As a result, research into failure of new materials and technologies is critical to evaluating their life expectancies.

The PoF approach is employed throughout the development cycle to assess stress margins and establish process controls so that device reliability can be continuously improved. Using PoF, manufacturers can give reliability assurances to customers with a greater degree of confidence. Customers can better assess and minimize their risks. This is important because products which fail in the market undermine customers' confidence in the manufacturer, and the customer who acquires unsatisfactory products can harm his own business and, potentially, that of other consumers as well.

7.3.5 Failure Modes, Mechanisms, and Effects Analysis (FMMEA)

FMMEA can be used to identify and rank the dominant failure mechanisms and modes in a product subjected to life-cycle loads. FMMEA is

Petitioner Samsung Ex-1055, 0384

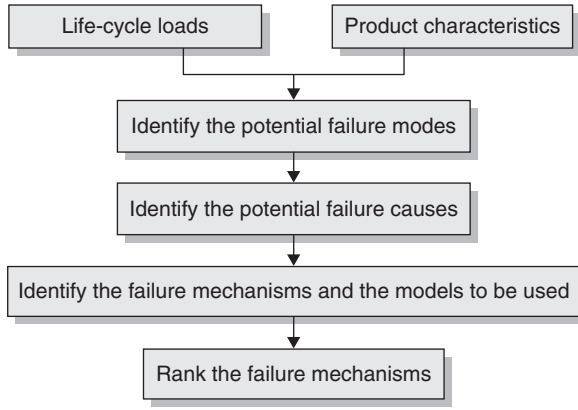


Figure 7.7 Failure modes, mechanisms, and effects analysis (FMMEA) flowchart.

based on the more traditional FMEA (failure modes and effects analysis) [40], but with the added failure mechanisms identification. The flowchart for the FMMEA methodology is shown in Fig. 7.7. The inputs to FMMEA are the life-cycle load profile and the product characteristics [41].

The FMMEA process begins by defining the system to be analyzed. A system is a composite of subsystems or levels that are integrated to achieve a specific objective. The system is divided into various sub-systems or levels and it can continue to the lowest possible level, which is a component or element.

A failure mode is the effect by which a failure is observed. For the elements that have been identified, possible failure modes for each given element are listed. For example, the potential failure modes of a solder joint are either open or intermittent change in resistance, which can hamper the solder joint function as an electrical interconnect. In cases where information on possible failure modes that may occur is not available, potential failure modes may be identified using numerical stress analysis, accelerated tests to failure, past experience, and engineering judgment. A potential failure mode may be the cause of a potential failure mode in a higher level subsystem, or system, or be the effect of one in a lower level component.

FMMEA is based on an understanding of the relationships between product requirements and the physical characteristics of the product (and their variations in the production process), the interactions of product materials with loads (stresses at application conditions), and their influence on the product's susceptibility to failure. FMMEA combines life-cycle environmental and operating conditions and the duration of the

Petitioner Samsung Ex-1055, 0385

intended application with knowledge of the active stresses and potential failure mechanisms. Potential failure mechanisms for a product are determined based on known failure mechanisms, functional sites, and materials in the product, as well as the anticipated stresses arising in the product.

FMMEA prioritizes the failure mechanisms based on their occurrence and severity to provide guidelines for determining the major operational stresses and environmental and operational parameters that must be accounted for in the design or be controlled. The life-cycle profile is used for evaluating failure susceptibility. If certain environmental and operating conditions are non-existent or generate a low stress level that is below trigger conditions for a mechanism, the failure mechanisms that are exclusively dependent on those environmental and operating conditions are assigned low occurrence. Quality levels of products also affect the possible occurrence level for a failure mechanism. PCBs made with very low levels of hollow glass fiber and high adhesion strength between fiber bundles and epoxies will have a lower occurrence level of conductive filament formation failure than the ones with higher levels of hollow glass fibers and low bonding strength.

Severity ratings are obtained from the failure modes and sites associated with the mechanism and not from the mechanism itself. The same failure mechanism may result in a small change in some electrical parameters at one site and shut down the system in another site. The severity will be at higher level for the later case.

The high-priority failure mechanisms identified through a combination of occurrence and severity are the critical mechanisms. Each critical failure mechanism has one or more associated sites, modes, and causes in an FMMEA result. FMMEA process as part of a virtual or design qualification can provide effective design feedback in terms of specific materials, architecture, and process improvements to meet or exceed the reliability and functionality requirements.

7.4 Product Qualification

Upon completion of virtual qualification, the product prototypes are manufactured and the product qualification process begins. In the product qualification process, physical tests including strength limits and highly accelerated life test (HALT) and accelerated tests are applied to the manufactured prototype to verify whether it meets its functionality and reliability requirements. The flowchart for the product qualification process is shown

Petitioner Samsung Ex-1055, 0386

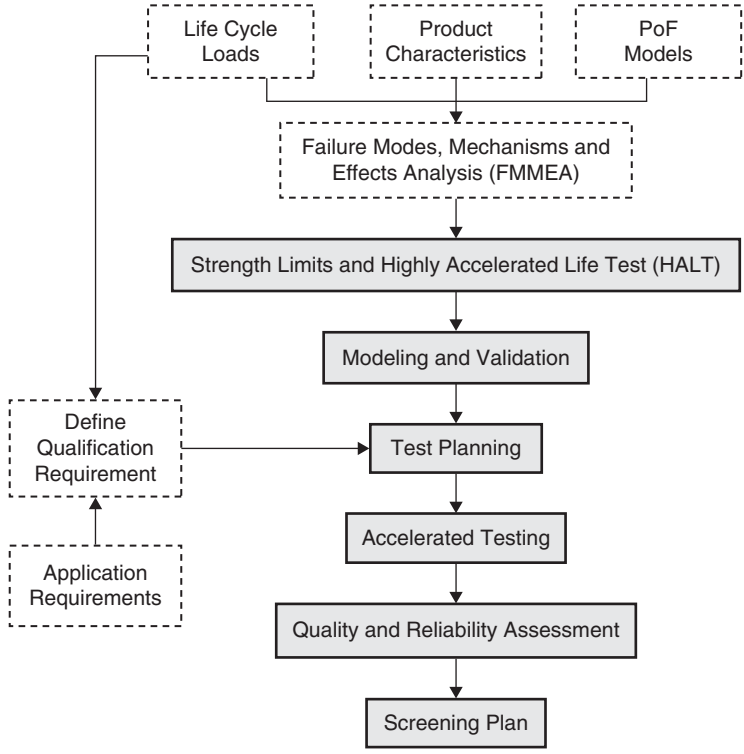


Figure 7.8 Product qualification flowchart.
PoF: Physics-of-failure.

in Fig. 7.8. If the design and manufacturing processes that were initially considered during the virtual qualification process has not been modified, then product qualification process essentially begins with strength limit testing or HALT. Conversely, any changes made to the product characteristics outside the design and manufacturing tolerance ranges requires virtual re-qualification or a product qualification process that includes the re-definition of product characteristics and a repeat of the FMMEA process.

7.4.1 Strength Limits and Highly Accelerated Life Test

HALT is the first physical testing performed during the product qualification stage. The term HALT was originally coined by Gregg K. Hobbs in 1988 [42] referring to the accelerated tests that lead to design ruggedness

Petitioner Samsung Ex-1055, 0387

and improvement. The HALT process flow for the purpose of design improvement is shown in Fig. 7.9 [42].

In product qualification, HALT can be used to identify the operational and destruct limits and margins, known as the "strength limits" as shown in Fig. 7.10. The specification limits are provided by the manufacturer to limit the use conditions by the customer. The design limits are the stress conditions at which the product is designed to survive. The operational limits of the product are reached when the product can no longer function at the accelerated conditions due to a recoverable failure. The stress value

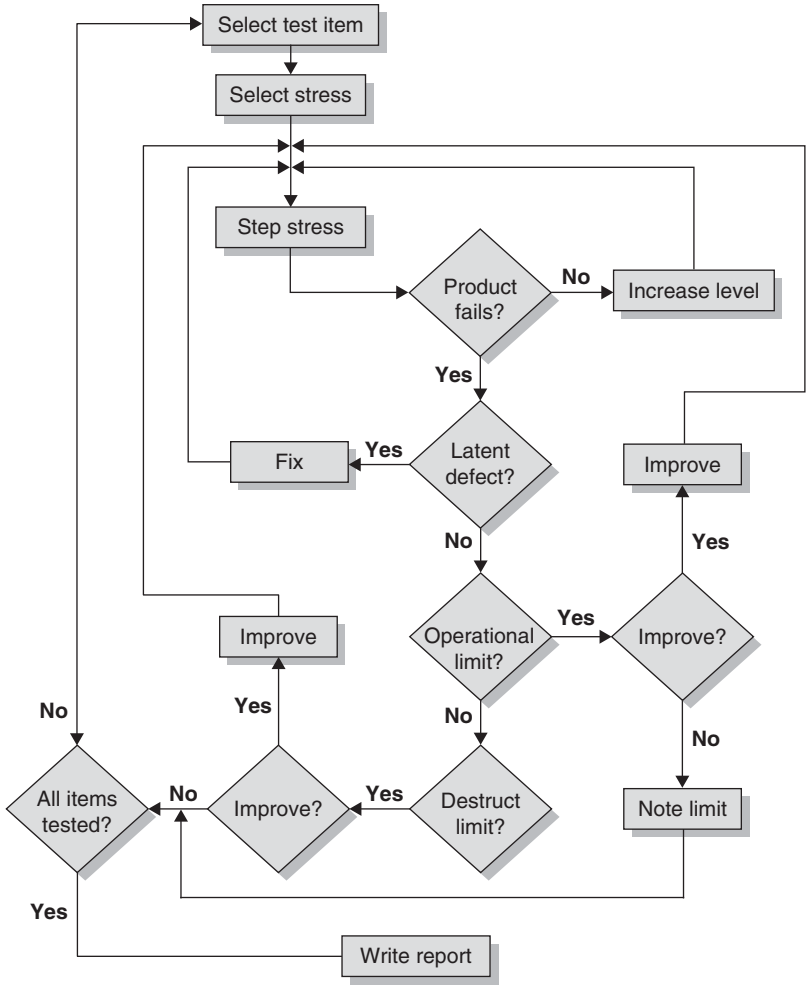


Figure 7.9 HALT process for the purpose of design improvement [42].

Petitioner Samsung Ex-1055, 0388

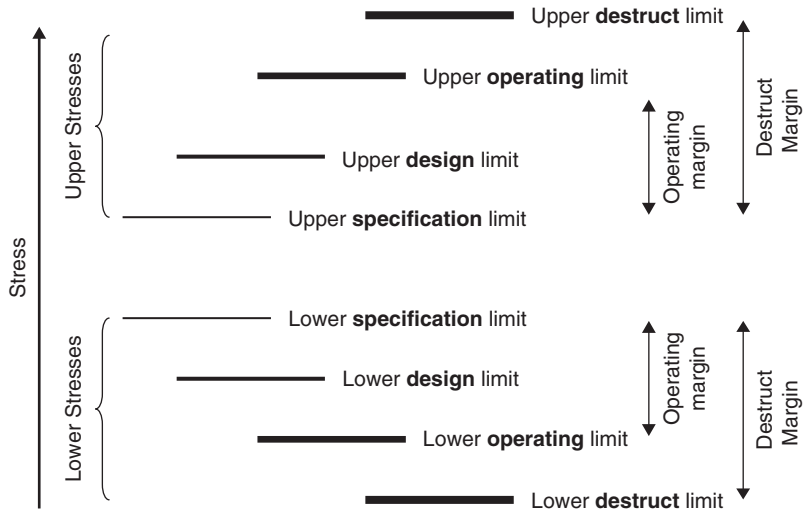


Figure 7.10 Strength limits and margins obtained from HALT.

at which the product fails permanently and catastrophically is identified as the destruct limit. When the product fails to function at a certain stress level, it must be evaluated at a lower stress level to determine whether it has reached its operational limits or has failed permanently. Generally, large margins are desired between the operational and destruct limits, and between the actual performance stresses and the specification limits of the product, ensuring higher inherent reliability.

Accurate mean strength limits and margins can be identified only if sufficient numbers of samples are tested to reveal complete distribution characteristics. Figure 7.11 shows the operating and destruct limits as probability distributions. The strength limits obtained from HALT can be used in planning the accelerated test and screening conditions. The destruct limits can be used as the baseline for highly accelerated stress screening (HASS) tests during production level qualification. If the product demonstrates survivability well beyond its operational limits or the limits of screening equipment, then the search for destruct limits can be terminated.

7.4.2 Qualification Requirements

Qualification requirements are the reliability and quality requirements of the product in compliance to the application requirements [2]. Qualification requirements must define the objectives and contents of the qualification

Petitioner Samsung Ex-1055, 0389

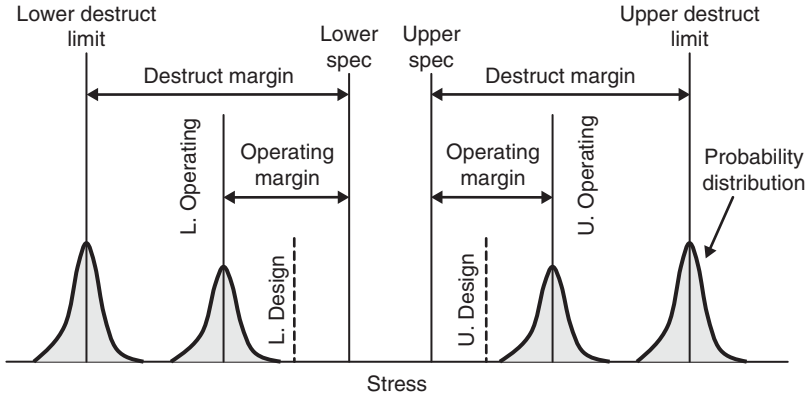


Figure 7.11 Lower (L.) and upper (U.) operating and destruct limits obtained from distributions [42].

activities. They are based on the application requirements specified by the customer including functional performance, application conditions and time (use condition profile), processing conditions, robustness against random external stresses, and expected statistical reliability properties such as tolerable infant mortality failures. Qualification requirements must also be defined based on the life-cycle load profile of the product. These loads include what the product experiences during its life cycle including manufacturing, assembly, storage, transportation, and operation.

There are essentially four levels of qualification: similarity, comparison, goal certification, and accelerated testing/life prediction (Fig. 7.12). Qualification by similarity is the lowest level of qualification where products,

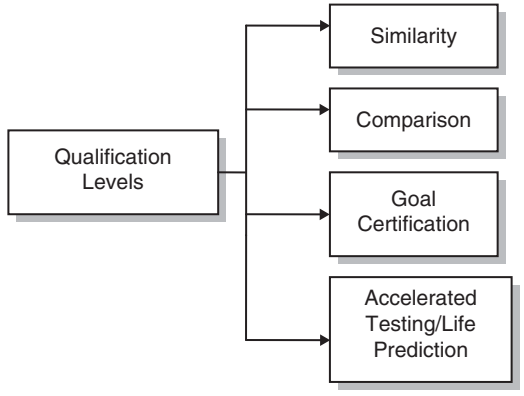


Figure 7.12 Qualification levels.

Petitioner Samsung Ex-1055, 0390

processes and packages are qualified by being similar to that which has been previously qualified to a higher level. Similarity qualification is achieved using engineering argument based on logical reasoning and no actual tests are performed. For example, if a certain packaged die pass a series of environmental tests, it is likely that a similar style package with different die design will also pass the same tests. Thus, different types of integrated circuit chips in the same type of package can be qualified by similarity. This type of qualification requires the least amount of resources, but has a high risk of omitting potentially critical information that can be only attained from higher levels of qualification and testing.

The second level is qualification by comparison. Specific tests are performed to compare results, but not necessarily to meet any reliability goals in a specific time period. Comparison qualification tests generally collect attributes rather than variables. For example, package related qualifications can involve "standard" testing where an acceleration factor may be absent for comparison to normal life. This does not mean that such tests are without value; however, favorable results can not be easily translated to specific statements about expected lifetime. For example, a device that passes 100 temperature cycles without failure may be perceived to be reliable; however, without a specific acceleration factor, no specific median lifetime can be determined. In comparison testing, quality attributes such as thermal performance maybe measured which can be directly correlated to specific reliability.

The third level of qualification is goal certification which involves meeting specific goals in terms of life or reliability. An example of this level of qualification is the life test that verifies reliability performance for warranty time periods or expected operational life and, accordingly, must meet specific reliability goals. This level of qualification is different from previous lower level, qualification by comparison, because the test results are directly related to reliability. It is different from the next higher level, since the end-of-life of the product need not be measured. In order to test a product for an expected warranty period of one year, a test may be conducted without acceleration for the same duration of one year. In this test, the failure modes, mechanisms, acceleration factors, and lifetime can not be determined; however, the test data may indicate a reliable product because it survived the warranty period. This level of qualification is the most common and is particularly used in military specifications.

The fourth and highest level of qualification involves accelerated testing and the TTF measurement. Tests are conducted on the electronic package to simulate the life-cycle environmental stresses under accelerated conditions

Petitioner Samsung Ex-1055, 0391

for time compression. In this level of qualification, failure modes and mechanisms associated with failure sites are likely to be identified, and the median lifetime and reliability can be determined from the tests results and acceleration factors.

7.4.3 Qualification Test Planning

The qualification requirements have to be converted to target values and tolerances that the product or the elements of the product have to meet. Relevant parameters and target values and tolerances are determined in order to meet or exceed the requirements. For example, a useful life requirement of a product has to be met by all its elements. By analysis, a weak element which has potential to fail earlier than others can be determined. Then a useful life requirement can be assigned to this element to make it meet a target useful life value and tolerance.

The qualification test conditions and stress levels are determined from the life-cycle profile of the product, FMMEA, experience from previous similar products, and the qualification requirements. Target values and tolerances have to be met by the product or product elements under the test conditions selected with respect to the life-cycle profile. Critical failure mechanisms, identified by FMMEA, associated with failure sites and failure modes will be considered in the qualification tests. When these failure mechanisms are combined with the reliability requirements, the targeted failure mechanisms in the qualification tests can be determined. If a failure mechanism identified to be critical in the FMMEA has no significant impact on the product's life within the reliability requirements, then this failure mechanism will not be considered in the qualification test. For example, if in the FMMEA, corrosion on PCBs alone will cause failure of the product in 10 years, but the reliability requirement is that the product operates without failure for 5 years, then corrosion will not be a concern in the qualification testing.

The selection of the qualification test stress level should ensure that the stress will induce the same failure mechanism as it would under operating conditions without introducing any new failure mechanism. The transformation between the qualification test results and the actual life under application conditions should also be considered [43].

Sample size selection is a critical issue in reliability qualification test planning. Sample sizes should be adequate for the characterization of the failure distribution. If the testing properties are systematically common to all products of a similar type, the sample size can be small. If the testing is

Petitioner Samsung Ex-1055, 0392

for a small fraction of defective products, the sample size should be large corresponding to the small fraction to be determined.

7.4.4 Modeling and Validation

An acceleration factor (AF) must be determined to translate the results from the accelerated testing to the product life at normal use environment. AF can be calculated either from PoF-based models or empirically. The AF based on PoF models (AF_P) is determined by taking the ratio of TTF at normal conditions predicted by PoF models to that predicted at accelerated conditions:

$$AF_P = TTF_{Normal\ Stress} / TTF_{Accelerated\ Stress} \tag{7.1}$$

The PoF models can be further validated using the results from the strength limits testing (HALT) and the AF_P can be adjusted accordingly. Another method of determining the AF is by empirical modeling (AF_E) based on curve fitting of the HALT data. Figure 7.13 shows the process of TTF of product life using PoF models, physical tests including HALT, and accelerated testing and AF. AF can be determined either by using PoF models (AF_P) or empirically (AF_E).

The stress levels must be carefully selected so as to neither introduce nor remove any critical failure mode and mechanism identified earlier. Excessive stress acceleration may induce a failure mechanism that may not normally occur during product service life. Each stress may cause the acceleration of several failure mechanisms but with different sensitivities. For example, temperature can cause the acceleration of corrosion, moisture diffusion, ionic contamination, and swelling, but at different rates. Conversely, each failure mechanism may be accelerated by several different stresses. For example, moisture diffusion is accelerated by both temperature and humidity.

7.4.5 Accelerated Testing

For most electronic products that have a minimum life of several years and short manufacturing lead times, it is not practical or economical to run qualification tests at normal operating conditions. Especially for long life and high reliability products, test periods can become quite long at the operating conditions. For example, a failure rate of 0.1% per 1000 hr with zero observed failures at a 60% confidence level would require 915,000

Petitioner Samsung Ex-1055, 0393

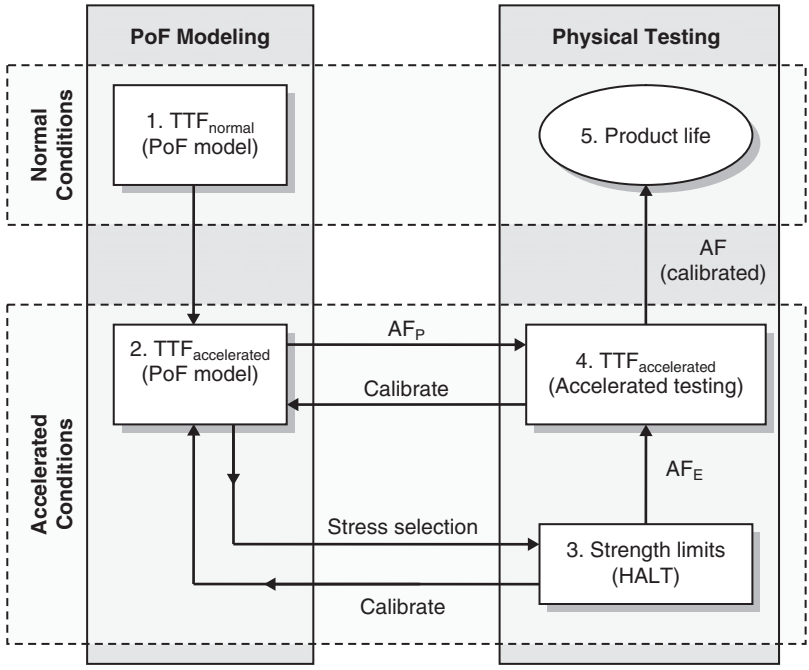


Figure 7.13 Flowchart of product life and time-to-failure (TTF) prediction based on physics-of-failure (PoF) modeling and accelerated testing.

device-hours of operation assuming a constant failure rate. The required device sample size and number of testing hours can be calculated from the binomial function with a given failure rate of 0.001, number of failures equal to zero, and a confidence level of 60. In this case, 915 devices with 1000 hours of operation or 92 devices with 10,000 hours operation will both satisfy the required conditions. However, these device-hours plans are neither economical nor time effective. The qualification tests are therefore, performed at accelerated stress conditions to compress the TTF and "speed up" the failure mechanisms.

Accelerated testing can be classified into two types: qualitative and quantitative. In qualitative accelerated testing the focus of the test is to identify the failure modes and mechanisms without predicting the normal lifetime of the product. In quantitative accelerated testing the normal life of the product is predicted from the accelerated test data.

The failure data from the accelerated tests are generally distributed in time, and must therefore be analyzed using statistical methods. A desired

Petitioner Samsung Ex-1055, 0394

level of statistical confidence can be obtained by controlling the sample size. Sometimes a Bayes approach [44] is applied to continuously update failure assessment based on past data and newly acquired available information.

Accelerated testing causes the life aging process of products to occur at a rate faster than it would under normal operating conditions. Although this time compression is desirable, it must not lead to any loss of useful knowledge. If time compression is the only consideration, the test results may become misleading. Therefore, a properly planned and executed accelerated testing involves the following steps:

- determining which failure mechanism(s) will be accelerated;
- selecting stress(es) to accelerate the failure mechanism(s);
- determining the level of the stress(es) to be applied;
- designing the test procedure, such as multiple-level acceleration or step-stress acceleration;
- extrapolating the test data to the application conditions.

Table 7.3 lists various failure mechanisms observed in plastic-encapsulated microelectronic packages and the corresponding acceleration stresses. Care must be taken in specifying the accelerated conditions so that failure modes or mechanisms are neither added nor removed. Excessive acceleration of a stress may trigger a failure mechanism that may be dormant at service loads. This failure mechanism shifting may provide misleading

Table 7.3 Selected Failure Mechanisms Relevant to Encapsulation and the Corresponding Acceleration Parameters

Failure Mechanism	Acceleration Parameters
Fatigue crack initiation	• Step load or displacement • Thermal shock
Fatigue crack propagation	• Vibration • Cyclic load displacement or temperature
Moisture diffusion	• Absolute temperature • Relative humidity • Moisture concentration, moisture gradient
Delamination	• Absolute and cyclic temperature • Relative humidity • Contaminants
Popcorning	• Relative humidity followed by thermal shock

Petitioner Samsung Ex-1055, 0395

service-life predictions. Each stress may also cause multiple failure mechanisms to be accelerated with differing sensitivities. For example, temperature accelerates electromigration, ionic contamination, and surface charge spreading, but at different rates. Conversely, a particular failure mechanism may be activated by multiple stresses. For example, corrosion is accelerated by both temperature and humidity. In light of these complexities, accelerated qualification testing should not be employed without a thorough understanding of how the test correlates with service conditions.

A qualification test to demonstrate acceptable reliability must be conducted for a long enough clock or calendar time to show that the application requirements have been met. For example, if the application requirement is for a time-to-first-failure of 10 years, and the qualification test is conducted under conditions which accelerate the relevant failure by a factor of 20, then a statistically valid sample size must be tested for at least six months (10 years divided by 20) before the first wearout failure occurs.

The nature of information required determines the type(s) of accelerated tests to be conducted. Besides selecting the forcing function and its level, it is also important to determine the way the load should be applied; for example, thermal effects due to convective heat transfer between the product and the surrounding air can be appreciably different from those generated by internal heat sources.

Test acceleration can involve event compression, test level exaggeration, or both. Event compression involves increasing the frequency of occurrence of the environmental forcing function as compared to field conditions. For example, if a product is subjected to two temperature cycles in its operating environment and six temperature cycles in the test, then the accelerated test involves a three-to-one event compression. Test level exaggeration consists of applying large loads on the product as compared to field loads. It is possible to combine event compression and test level exaggeration in a single test to increase the degree of acceleration. Short-term tests can involve a gradual increase in exaggerated test levels until product failure. Long-term tests may involve application of constant forcing functions (which are more severe than the field operating load) in event compression mode to detect product weaknesses.

After the accelerated testing, detailed failure analysis of failed samples is a crucial step in the qualification and validation program. Without such analyses and feedback to the design team for corrective action, the purpose of the qualification program is defeated. In other words, it is not adequate simply to collect failure data. The key is to use the test results to provide insights into, and consequent control over, relevant failure mechanisms and to prevent them in cost effective manner [26].

Petitioner Samsung Ex-1055, 0396

A good way to design tests can be found in the book by Montgomery [45] on the use of fractional factorial arrays used in design of experiments. Since failures are often related to higher level (i.e., system) design and manufacturing factors, qualification of microelectronics should be conducted on samples assembled using representative assembly materials and processes, as well as representative higher level design practices. Data should be collected from sufficient device-hours and clock or calendar time to cover anticipated failures and useful life requirements. If the tests are designed to be comprehensive, then accelerated test models can be used to apply the data thus obtained to a range of product requirements.

7.4.6 Reliability Assessment

Reliability assessment is performed based on the accelerated test data and the PoF models. The reliability of the product is determined in terms of TTF at the identified failure sites for a specific failure mechanism due to specific load condition. With the failure sites, stress inputs, and failure models, the reliability of a product is estimated and reported in terms of TTF of the identified failure sites. Most failure models define TTF under a specific loading condition. In the qualification test, the reliability of products is defined in order to meet the specified reliability requirement under qualification test conditions.

For most products, the life-cycle profile consists of multiple loading conditions. As a result, methods for evaluating TTF over multiple loading conditions must be derived. One approach is to cast the TTF for a specific failure mechanism in terms of the ratio of exposure time to the stress condition over TTF for the stress condition, which is often referred to as the damage ratio. If the exposure time is equivalent to the TTF, then the ratio would equal to one. If one assumes that damage accumulates in a linear fashion, the damage ratios for the same failure site and mechanism can be added over multiple defined stress conditions. It is then assumed that once the accumulated damage ratio equals one, failure at the site would occur. For the same site and the same failure mechanism and for fixed duration load events, a specific damage ratio can be determined. For example, drop of a hand held device from a certain height may result in a loss of ten percent of the life of a solder interconnect. In this case, each drop will result in an increment of 0.1 damage ratio for the solder interconnect. For repetitive events, a damage rate may be established by

Petitioner Samsung Ex-1055, 0397

the uses the appropriate failure models to estimate the number of events required to produce failure. The damage rate is then defined as one over the estimated number of survivable events. For example, if a failure model estimates that a solder interconnect can survive 2000 temperature cycles, then the damage rate per cycle is 0.0005.

In general, TTF data is obtained as a distribution for each failure site and failure mechanism. This distribution on TTF is achieved by considering the input parameters to the failure models as distributions. In reality all dimensional and material properties are distributed about a nominal value as a result of variations in manufacturing. The same is true for the environmental loads. The PoF-based reliability assessment allows for utilization of these natural variations in the reliability assessment. With the TTF distribution on each site known, reliability can be evaluated in different metrics such as hazard rate, warranty return rate, or mean TTF.

In addition to evaluating TTF, the use of failure models allows for the examination of TTF sensitivity to material, geometry, and life-cycle profile. By considering the impact of the identified material and product geometries and loading conditions, the most influential parameters can be identified. This information can be used to improve design through closer attention to critical design parameters.

7.5 Qualification Accelerated Tests

When determining which tests to use for qualification, some important factors should be considered:

- there can be significant differences among manufacturers of the same part number;
- there can be significant differences among part numbers from the same manufacturer;
- distributors methods can impact reliability;
- next-level processes such as adding a heat sink or assembly on printed wiring board can impact reliability.

This section provides an overview of some of the major qualification tests for microelectronic packages. The specific standards relevant to each test will be discussed in a separate section on industry practices. The reader is referred to Chapter 5 for a more detailed discussion on failure mechanisms. For more generic information on failure mechanism

Petitioner Samsung Ex-1055, 0398

modeling, the interested reader is also referred to the tutorial series on failure mechanisms in the IEEE Transactions on Reliability [14].

Often, the reliability requirements will change from one product application to another. For example, if a product is to be used in a ground application in tropical areas, then humidity-related failures may be considered most likely, and the appropriate data for qualification must be derived from accelerated humidity testing, or combined temperature and humidity. If the same product is to be used in a space satellite with a low earth orbit, humidity is not an issue, unless long-term storage occurs.

7.5.1 Steady-State Temperature Test

High-Temperature Storage Test. This test accelerates temperature-induced failures such as interdiffusion, Kirkendall voiding, depolymerization, decomposition, outgassing, and oxidation of plastic materials. In electrically programmable read only memory devices, the test accelerates charge loss from floating gates in the device which is limited by gate oxide layer defects. Devices are stored in a controlled elevated temperature (typically around 150°C) for extended times (of more than 1000 hours) without electrical bias. Interim electrical parametric measurements and final measurements are conducted at the conclusion of the test. The electrical measurements include contact test, parametric shifts, and at-speed functional tests. Damage, such as package cracking, an increase junction thermal resistance, or depolymerization, may also be considered a failure.

High-Temperature Operation Test. This test evaluates the capability to withstand maximum power operation at elevated temperatures. Electrical configurations include steady-state reverse bias, forward bias, or a combination of the two. Electrical frequency is set to maximum operating design level or to the limit of the test equipment. The test is usually conducted at a junction temperature, below the glass transition temperature of the plastic encapsulant. A simple model to describe junction temperature with respect to the case and ambient temperature is

$$T_j = T_a + (q_{jc} + q_{ca})P \tag{7.2}$$

where θ_{ca} is the case-to-ambient thermal impedance, which depends on the system equipment, whether it is forced air or still air cooling; θ_{jc} is the junction-to case thermal impedance, which depends on the thermal impedance of the plastic-encapsulant package; and P is the power.

Petitioner Samsung Ex-1055, 0399

7.5.2 Thermal Cycling Test

This section discusses temperature cycling, thermal shock, and combined power and temperature cycling tests. For plastic-encapsulated microelectronics, the high-temperature limit should be kept below the glass transition temperature of the molding compound.

Temperature Cycling. The temperature cycling test consists of the application of some temperature variation of a specified amplitude about a mean value. Temperature is usually varied at a fixed rate followed by a dwell period, subjecting interfaces of dissimilar materials in a device to mechanical fatigue.

In a plastic-encapsulated microelectronic device, test results are affected by encapsulant thickness, die size, die passivation integrity, wire bond, die cracks, and adhesion at the interfaces, including passivation to encapsulant, die pad to encapsulant, and lead fingers to encapsulant. For a device interconnected to a substrate (or circuit board), the fatigue endurance of the device-to-board interconnection structure can also be evaluated.

Temperature cycling is conducted in an environmental chamber equipped with a temperature-control device, a heating unit, and a cryogenic cooling unit with sufficient thermal capacity so that the sample can be heated and cooled within the specified time span in dry, flowing air. The dwell time at each extreme is the minimum needed to establish thermal equilibrium with the sample load, and sufficient stress relaxation (if this is a key parameter of the failure mechanism of concern). Post-stress examination includes electrical parametric and functional tests and inspection for mechanical damage such as package cracking.

Thermal Shock. This test is conducted to validate unit integrity under extreme temperature gradients. Sharp temperature gradients can cause die cracking, delamination, die-passivation cracking, deformation of interconnections, and encapsulant cracking. The shock is applied by cyclic immersion of specimens in suitable fluids maintained at specified temperatures. The test is concluded after the desired number of cycles has been completed, generally with the final immersion being in the "highest-stress" cold bath. The fluids should be chemically inert, stable at high temperatures, non-toxic, non-combustible, of low viscosity, and compatible with package materials. Specimens are warmed to room temperature prior to measurements. End tests include electrical measurements and inspection for mechanical damage.

Power and Temperature Cycling. The purpose of this test is to expose samples to worst-case temperature conditions during operation. The failures

Petitioner Samsung Ex-1055, 0400

are generally those that are observed in a temperature cycling test. The test chamber is similar to that used for temperature cycling, except that mounting sockets with electrical feed-throughs are provided for the application of bias to test devices. Power may be cycled on and off, with or without synchronization with the temperature cycle. Electrical measurements to check for functionality and parametric limits, and visual inspection to detect mechanical damage should be conducted.

The severity of the test may be influenced by the temperature at which the residual stresses are zero. Residual stresses are caused by temperature changes during encapsulation process—specifically, from curing and glass transition temperatures to ambient room temperatures. The residual stresses are zero at or above the glass transition temperature (T_g) of the encapsulant which lies in the 150–180°C range. In a temperature cycling test, the lower temperature limit that is farther from the glass transition temperature should control the severity of the test. The distribution and magnitude of residual stresses can be altered by humidity-induced swelling of the encapsulant.

Since a successful test is usually one in which no failures occur, there is always the question as to whether or not appropriate stresses, and levels thereof, have been applied to adequately test the product. It is also unknown whether the product barely passed, in which case there is a question regarding the reliability margin; or whether it would have passed a much more stressful test, in which case the product may be overdesigned. There is also the question of relating the results of tests to service conditions and performance. For this reason, at least some customers are placing more emphasis on achieved field reliability, and leaving it to the supplier to develop and implement an acceptable plan.

7.5.3 Tests That Include Humidity

This section discusses the following tests that include humidity: autoclave, combined temperature-humidity-bias, highly accelerated stress test (HAST), and combined temperature-humidity-voltage cycling. A test to classify moisture sensitivity is also presented.

Autoclave Test. This test is also known as a "pressure cooker" test to evaluate moisture resistance, and is the simplest of the accelerated humidity tests. Typically, specimens are stored in saturated steam, at a pressure of 103 ± 7 kPa (15 ± 1 psig) and 121°C in a sealed autoclave. The steam is produced from deionized water. The devices are suspended at a minimum height of 1 cm above the initial water level in the chamber.

Petitioner Samsung Ex-1055, 0401

Severe conditions of pressure and temperature, not typical of actual operating environments, can be used to accelerate moisture penetration through the package. Galvanic corrosion is the major failure mechanism. Ionic contaminants in the encapsulant and phosphorus in the passivation are factors that accelerate corrosion in plastic-encapsulated microelectronics. However, test chamber contaminants can produce spurious failures, which are evidenced by external degradation of a package such as corroded device terminals/leads or the formation of conducting matter between the terminals.

Temperature-Humidity-Bias Stress Tests. The temperature-humidity-bias test is one of the most commonly applied accelerated tests. Its purpose is to test for moisture ingress and corrosion of leads, bond pads, and metallization, with attendant high leakage current in the integrated circuits. Specimens are subject to a constant temperature and constant elevated relative humidity (RH) under electrical bias. Depending on the device type, bias may be applied either constantly or intermittently. Applying a continuous DC voltage to low power complementary metal-oxide semiconductor devices maximizes the chance of formation of electrolytic cells, because individual device power dissipation is minimized. In the case of high-power devices, the continuous electrical power can lead to a relatively large amount of heat dissipation which can drive away the moisture near the die that is needed for electrolytic corrosion and other moisture related failures. Therefore, high-power devices are generally subjected to voltage cycling.

In plastic-encapsulated microelectronic packages, due to the low thermal conductivity of the plastic encapsulant, continuous electrical bias can increase the die temperature and also drive moisture away. Thus, plastic packages are subjected to power cycling. If the power ON/OFF cycle time is such that moisture escapes the plastic during the ON period, and the OFF period is shorter than it takes for moisture to ingress to the die-encapsulant interface, then it is expected that the total number of failures would be decreased, due to reduced humidity-related package failures during the ON state, and reduced bias-related failures during the OFF state [46]. The cycled conditions must be optimized for individual device types to induce a maximum opportunity for failure.

The temperature-humidity-bias test is usually conducted at 85 ± 2°C with relative humidity of 85 ± 5% at a maximum rated operating voltage. Electrical measurements are usually conducted upon removal of the test devices. In some cases, samples may be dried before testing. The failure criteria are parametric shifts outside of specific limits, non-conformal functionality under specified nominal and worst-case conditions, or any other performance irregularities.

Petitioner Samsung Ex-1055, 0402

Highly Accelerated Temperature and Humidity Stress Test. HAST consists of elevated temperature and humidity, and can be coupled with electrical biasing with controlled current. The test can cause corrosion of metallization and bond pads, delamination of interfaces, increased intermetallic growth, wire bond failures, and reduction in isolation resistance.

In a typical HAST test, unsaturated steam with constant relative humidity in the range of 50% to less than 100% at a constant temperature, usually greater than 100°C, is used. Details of the test method are described by Gunn et al. [47] and Danielson et al. [48].

Cycled Temperature, with Constant Humidity and Bias. In this test, a device is subjected to thermal cycling under a high level of moisture with electrical bias. The failure mechanisms targeted by this test include electrolytic as well as galvanic corrosion, de-adhesion, delamination, and crack propagation. The potential failure sites include interfaces between the lead-fingers and the encapsulant, ball-bond, stitch-bond, bond-pads, and metallization corrosion.

This test is conducted in an environmental chamber capable of maintaining a controlled relative humidity level and a heat–cool cycle while electrically biasing the test units. Deionized water is used in the chamber as a moisture source. Typically, test units are subjected to temperature cycles of 30–65°C with heating and cooling times of 4 hours each and a dwell time of 8 hours at each temperature extreme. Relative humidity is generally maintained at a constant value in the range of 90–98%. A chart-type recorder with suitable chamber monitoring instrumentation is provided for continuous recording of chamber temperature and relative humidity.

Test to Classify Moisture Sensitivity Level for Surface-Mount Devices. Molding compounds, used for manufacturing surface-mount plastic electronic packages, which absorb moisture, can result in cracking of the plastic material and/or its delamination from the chip or the lead-frame when a package is exposed to high temperature during reflow soldering. The failure mechanism, called popcorning, represents the worst-case situation that sometimes takes place because of unfavorable combinations of high moisture content, elevated thermal stress, and package design features, leading to low structural strength and propensity for crack initiation and propagation. The reader is referred to Chapter 5 for more information on popcorning.

Moisture sensitivity levels for surface-mount plastic integrated circuits based on IPC/JEDEC standard classification (Table 7.4) can be grouped into three basic categories:

- moisture insensitive: there is no need to keep the integrated circuits in dry pack;

Petitioner Samsung Ex-1055, 0403

Table 7.4 IPC/JEDEC J-STD-20 MSL Classifications

Moisture Sensitivity Level	Floor Life		Standard Soak Requirements	
	Time	Condition (°C/%RH)	Time (hrs)	Condition (°C/%RH)
1	Unlimited	≤ 30 /85%	168	85/85
2	1 year	≤ 30 /60%	168	85/60
2a	4 weeks	≤ 30 /60%	696	30/60
3	168 hours	≤ 30 /60%	192	30/60
4	72 hours	≤ 30 /60%	96	30/60
5	48 hours	≤ 30 /60%	72	30/60
5a	24 hours	≤ 30 /60%	48	30/60
6	Time on label	≤ 30 /60%	Time on label	30/60

Source: http://www.siliconfareast.com/msl.htm.

- moisture sensitive with unlimited floor time: the integrated circuits must be stored in dry pack until the dry pack is opened in a factory environment of 30°C (max.) at 85% RH (max.), where it can be left for unlimited time prior to PCB assembly and soldering;
- moisture sensitive with limited floor time: the integrated circuits must be stored in dry pack until the dry bag is opened in a factory environment of 30°C (max.) at 60% RH (max.), where it can be left for a limited time depending on the specific level prior to PCB assembly and soldering.

To classify surface-mount plastic-encapsulated packages into different moisture sensitivity levels, the packages are subjected to the following moisture preconditioning levels: (1) 85°C/85% RH, (2) 85°C/60% RH, and (3) 30°C/60% RH for specific test durations as listed in Table 7.6. After moisture preconditioning, the packages are then exposed to PCB assembly simulation sequences test. The assembly simulation test consists of infrared reflows at a typical temperature of about 220–240°C and a number of chemical exposures (cleaning). At the conclusion of this test, the packages are visually inspected under a 40× microscope for external cracks. C-mode scanning acoustic microscopy can also be used to observe any internal surface delamination or cracks in the devices. Complete electrical measurements must then be carried out at the appropriate points. If no evidence of cracking and electrical failure is observed, then the package has passed the particular moisture sensitivity level.

Petitioner Samsung Ex-1055, 0404

Subsequently, the packages are subjected to the temperature-humidity-bias stress test. The purpose of this test is to accelerate moisture ingress, as well as the effect of corrosion on metallizations.

As the microelectronic packages become smaller and as the electronics industry transition to lead-free solder, the applicability of the original JEDEC moisture sensitivity standards need to be re-evaluated. Smaller packages subjected to typically higher lead-free solder reflow temperatures are more likely to fail the original JEDEC moisture levels. In a study by Mercado and Chavez [49], a bump chip carrier (BCC®) was found to be saturated after only 59 hours of exposure to moisture sensitivity level 2 (MSL2) at 85°C/60% RH whereas a relatively larger and thicker QFP package generally is not close to saturation even at the end of the 168 hours MSL2 soaking duration. In the same study, due to the relatively higher reflow temperature of lead-free solders, it was found that a cooling rate of 2.4°C/second induced a 20% higher crack driving force at the encapsulant/die interface. Therefore, the original JEDEC standards should be modified to reduce the severity of the conditions on the smaller sized packages subjected to lead-free solder reflow.

7.5.4 Solvent Resistance Test

This test evaluates the capability of samples to withstand detrimental effects caused by chemicals used in assembly processes such as swelling, cracking, de-adhesion of the encapsulant, and corrosion of the leads. Chemicals included in this test are those used in the solder reflow and flux cleaning, such as fluxes and solvents. A procedure for a solvent resistance test proposed by Lin and Wong [50] for plastic-encapsulated microelectronic assemblies is presented in Table 7.5.

Table 7.5 Encapsulant Chemical Resistance Test Procedure [50]

Chemical	Exposure	Cleaning	Failure Criteria
Alpha-100, EC-7, and 1,1,1-trichloroethane	2-hr soak in each chemical in sequence	Soak in isopropanol for 10 min; rinse in running distilled water for 15 min; dry in a clean oven at 120°C for 1 hr	Examine under microscope for swelling, crack, de-adhesion, and corrosion
Polyalphaolefin	96-hr soak		

Petitioner Samsung Ex-1055, 0405

7.5.5 Salt Atmosphere Test

This test evaluates corrosion resistance of lead-frames exposed to seacoast environments. Failure mechanisms that can be accelerated include electrochemical degradation, such as pitting, pinholes, blistering, and flaking of the package leads. This test is usually conducted following the lead-bending operation.

Specimens are placed in an environmental chamber in a flowing salt fog at 35°C for a specified duration. The salt fog is generated by atomizing a 0.5–3.0% by weight sodium chloride solution with compressed air to create a mass flux of 7–35 mg/m^2/min. (0.8×10^{-3} to 4×10^{-3} oz/ft^2/min). The pH of the solution is maintained between 6.0 and 7.5. Care is taken to avoid the use of a chamber contaminated by prior tests. The specimens are placed in the chamber to achieve maximum exposure to the salt fog. Test duration is typically 96 hours.

7.5.6 Flammability and Oxygen Index Test

These tests evaluate flammability of molding compounds. Flammability is the property of a material whereby flaming combustion is prevented, terminated, or inhibited following application of a flaming or non-flaming source of ignition, with or without subsequent removal of the source. Underwriters Laboratories material flammability standard UL-STD-94 assigns a flame-retardant grade to a material based on its burning rate. The various grades are HB, V-0, V-1, V-2, and 5V, where HB indicates the highest and 5V the lowest burning rate.

A numerical value to flammability is assigned by the oxygen index. The oxygen index is the percent oxygen in an oxygen-nitrogen mixture that will just sustain combustion of a material. The oxygen index is obtained in compliance with test method ASTM D-2863. Decreasing flammability is indicated by a higher oxygen index. When flammability and oxygen index tests are not feasible, the EEC "glow wire" and "needle flame" tests may be used. Flammability of encapsulants can be reduced significantly by compounding with halogenated compounds, phosphate esters, and antimony trioxide.

7.5.7 Solderability

This test evaluates the ability of leads on a device to solder wetting. The wettability of a metal surface depends on the integrity of the corrosion resistant coating, contamination-free surface, solder temperature, specific heat of the lead material, and lead design [51].

Petitioner Samsung Ex-1055, 0406

The technologies used in solderability assessment tests are either dip-and-look or wetting balance. In a dip-and-look approach the surface to be soldered is dipped into a molten solder bath. The extent of surface coverage upon removal is visually judged in order to estimate solderability of the surface. Some of the concerns with dip-and-look tests include the apparent enhancement of solderability due to solder freezing upon removal from the solder bath, and the undetected microscopic dewetting.

A wetting balance test measures the force of attraction between the surface and the molten solder with time. It is insensitive to dewetting of solder, because dewetting begins only upon removal of the surface from the molten solder.

7.5.8 Radiation Hardness

This test is used only in qualification of devices intended for applications such as space missions, where the plastic-encapsulated microelectronic package must withstand gamma-rays, cosmic rays, X- rays, alpha-particle radiation, and beta radiation. The radiation hardness test exposes a device to a specified total ionizing dose of radiation followed by parametric electrical tests.

Radiation-caused failure mechanisms are electron pair generation and lattice displacement. Traces of radioactive elements in package materials, such as uranium and thorium from inorganic fillers, are intrinsic sources of ionizing radiation that can cause errors in programmable devices. In logic and memory devices, radiation exposure can cause soft errors in dynamic memory devices, electrical parametric upsets, and latch-up.

7.6 Industry Practices

Manufacturers often formulate their own qualification procedures in keeping with market practice and customer specifications. A wide variety of accelerated tests—involving various stress levels and combinations of stresses—are used by device manufactures. Table 7.6 provides a listing of typical stresses, levels, and durations [52–54]. However, the test conditions are often dictated by customer requirements, which are not derived from PoF. Harsh stress levels are imposed during testing based on the rationale that, if the packages last longer under more stringent conditions, then the parts must be of better quality [54]. However, this approach fails to consider the fact that subjecting the devices to harsh stresses may induce other failures, or may not be cost-effective.

Petitioner Samsung Ex-1055, 0407

Table 7.6 Example Test Conditions Used in Industry [52–54]

Test	Motorola	Intel	Texas Instruments	Signetics	Micron	American Micro Devices	National Semiconductor
Temperature cycle	–65 to 150°C 1000 cycles	–55 to 125°C 500 cycles	–65 to 150°C 500 cycles	–65 to 150°C 500 cycles	–65 to 150°C 1000 cycles	–65 to 150°C 1000 cycles	–65 to 150°C 1000 cycles
Autoclave	121°C 15 psig 96 hrs	121°C 96 hrs	121°C 15 psig 240 hrs	127°C 20 psig 336 hrs	121°C 15 psig 96 hrs	121°C 15 psig 168 hrs	121°C 15 psig 500 hrs
Temperature and humidity with bias	85°C 85% RH 1008 hrs	85°C 85% RH	85°C 85% RH 1000 hrs	85°C 85% RH 2000 hrs	85°C 85% RH 1000 hrs	85°C 85% RH 2000 hrs	85°C 85% RH 1000 hrs
Operating life	Max. rated = 1008 hrs	–	125°C 1000 hrs	150°C 2000 hrs	150°C 1000 hrs	125°C 168 hrs	125°C 1000 hrs
High temperature storage	–	200°C 48 hrs	–	175°C 2000 hrs	150°C 1008 hrs	125°C 2000 hrs	150°C 1000 hrs
Solder heat resistance	–	–	260°C 10 sec	–	–	–	260°C 12 sec
Low temperature life	–	–	–	–10°C 1000 hrs	–10°C 1008 hrs	–	–40°C 1000 hrs

Petitioner Samsung Ex-1055, 0408

To demonstrate the device capabilities in order to meet customer requirements, tests must be chosen that will accelerate TTF in a predictable and understandable manner. The stress conditions must be selected in such a way that failures from accelerated tests are those that will be expected to occur at normal device operation.

Whenever a change in material, package technology, or process technology is introduced, each test must be reevaluated to determine its effectiveness in uncovering potential weaknesses.

The appropriate approach is to first identify the root causes of failure for the devices and develop qualification tests that focus on those particular causes. This is the essence of the PoF approach to qualification, which, by testing for the primary cause behind a failure, precludes the possibility of failures occurring. When qualification testing results in unexpected failures, then further investigation is necessary to determine the root causes behind them.

Table 7.7 lists various test methods that may be used to detect the failures. Some of these tests are applicable only to specific use environments and manufacturing conditions. For example, solder heat resistance evaluates a package's ability to resist popcorning during solder reflow operation for surface-mount devices. The radiation hardness test is suggested only for devices (i.e., memory) that are susceptible to and are expected to be exposed to either extrinsic or intrinsic radiation.

7.7 Quality Assurance

Electronic products must conform to specific quality requirements. According to the International Standards Organization (ISO), quality is defined as the totality of features and characteristics of a product or service that bear on its ability to satisfy stated or implied needs [55]. Poor quality is generally due to defective materials, out-of-control manufacturing processes, and improper handling. Table 7.8 provides the definition of various quality assurance related terms.

Quality conformance leads to an increase in the product yield. The parameter variability to be controlled in quality conformance may be due to any one or a combination of the following factors:

- raw material property variability between lots and suppliers;
- variability in a manufacturing process parameters due to inaccuracies of process monitoring and control devices;

Petitioner Samsung Ex-1055, 0409

Table 7.7 Possible Test Methods and Conditions for Tests Used in Qualification of Plastic-Encapsulated Microelectronic Packages

Test	Test Conditions	Simulated Environment	Applicable Standards
Low-temperature operating life (LTOL)	–10°C/V_{max}/max. frequency/minimum 1000 device hours/outputs loaded to draw rated current	Field operation in sub-zero environment	JQA 108, JESD 22A 108C
High temperature operating life (HTOL)	125°C/V_{max}/max. frequency/minimum 1000 device hours/outputs loaded to draw rated current	Field operation in normal environment	MIL-STD-883 method 1005 JQA 108, JESD 22A 108 C
Temperature cycling (TC)	500 cycles, –65 to 150°C at a ramp rate of 25°C/min and with 20-min dwell at each temperature extreme	Day–night, seasonal, and other changes in environment temperature	MIL-STD-883 method 1010, JESD 22A 104C
Temperature cycling, humidity and bias (TCHB)	60 cycles, voltage ON/OFF at 5-min intervals, 95% RH, 30–65°C with heating and cooling time of 4 hrs each and a dwell of 8 hrs at each temperature extreme	Slow changes in environment conditions while device is operating	JESD 22-A 100-A
Power and temperature cycling (PTC)	Only on devices that experience rise in junction temperature greater than 20°C, min. 1000 cycles of –40 to 125°C	Changes in environment temperature while device is operating	JESD 22-A 105-A
Thermal shock (TS)	500 cycles of –55 to 125°C	Rapid change in field or handling environment	MIL-STD-883 method 1011, JESD 22A 106B
High temperature storage (HTS)	150°C for 1000 hrs min.	Storage	JQA-103, MIL-STD-883 method 1008, JESD 22-A-103-C

(*Continued*)

Petitioner Samsung Ex-1055, 0410

Table 7.7 Possible Test Methods and Conditions for Tests Used in Qualification of Plastic-Encapsulated Microelectronic Packages (*Continued*)

Test	Test Conditions	Simulated Environment	Applicable Standards
Temperature-humidity-bias (THB)	V_{max}/85°C/85% RH/1000 hrs	Operation in high humidity environment	JESD 22-A-101-A
Highly accelerated stress test (HAST)	V_{max}/130°C/85% RH/240 hrs min.	Operation in high humidity environment	JESD 22-A 110
Pressure cooker or autoclave (ACL)	Precondition for surface-mount devices, 15 psig/121°C/100% RH/240 hrs	High humidity environment, moisture ingress through cracks	MIL-STD-883 method 1005 JEDEC-STD-22 method 102A
Lead integrity (LI)	As appropriate for package type and lead configuration	Manufacturing environment	MIL-STD-883 method 2004 JESD22-B105-A
Bond strength (BS)	As appropriate for wire-bond or lead configuration	Manufacturing environment	MIL-STD-883 method 2011C/D
Die shear (DS)	Consistent with the device specifications	Characterization of die-encapsulant interface	MIL-STD-883 method 2019
Mechanical shock (MS)	Five shock pulses of g-level and duration as per device specification along a particular axis	Avionics or spacecraft launch environment	MIL-STD-2002, JESD22-B104-C
Vibration variable frequency (VVF)	Logarithmic variation from 20 to 2000 Hz and back to 20 Hz in a time duration of more than 4 min, four times each applicable axis	Avionics or spacecraft launch environment	MIL-STD-2007, JESD22-B105-A
Flammability (FL)	With or without removal of ignition source	Characterization of encapsulant flammability	UL-94-V0 or V1

Petitioner Samsung Ex-1055, 0411

Oxygen index (OI)	Sustained combustion of a material	Characterization of encapsulant flammability	ASTM-STD-2863
Solder heat resistance (SH)	260 ± 10°C for 10 sec	Vapor phase or reflow solder heat	JESD22-B106-A
Solderability (SOA)	Dip and look, or wetting balance	Characterize solderability as manufactured or after storage	MIL-STD-883 method 2003
Salt atmosphere (SA)	Salt fog at 35°C, pH 6–7.5, 200 hrs	Ship board corrosive environment	MIL-STD-1009, JESD22-A 107-A
Solvent resistance (SR)	For example, solder flux, flux cleaning solvents, and liquid coolant	Assembly environment	MIL-STD-883 method 2015
Electrostatic discharge (ESD)	Human body model: 1 A (for 1500 V) exponentially decreasing with time constant 300–400 nsec, or charged device model: 1500 V, 15 A, 4–5 oscillations in 15 nsec	Damage by electrostatic discharge	MIL-STD-883 method 3015, JQA 2
Latchup (LU)	Appropriate charging voltage	Voltage excursion	JQA 3, JESD78A
Radiation hardness (RA)	Specified total ionizing dose of radiation	Space and high radiation environment	MIL-PRF-38535, MIL-STD-883 method 5005-E, MIL-HDBK-816

JQA refers to Joint Qualification Alliance having Ford Motor Company, AT&T, and Hewlett Packard as members; MIL-STD-883 refers to a military standard "Test Methods and Procedures for Microelectronics"; JESD refers to JEDEC Standard No.22 "Test Methods and Procedures for Solid State Devices Used in Transportation/Automotive Applications"; ASTM refers to American Society for Testing Materials.

Petitioner Samsung Ex-1055, 0412

Table 7.8 Quality Related Terminology

Term	Definition
Quality	Totality of features and characteristics of a product or service that bear on its ability to satisfy stated or implied needs
Quality conformance	Monitoring and controlling critical parameters within acceptable variabilities
Quality control	Operational techniques and activities that are used to fulfill requirements for quality [55]
Quality assurance	Planned and systematic actions necessary to provide adequate confidence that a product or service will satisfy given requirements for quality [55]
Quality surveillance	The continuing monitoring and verification of the status of procedures, methods, conditions, processes, products and services, and analysis of records in relation to stated references to ensure that specified requirements for quality are being met
Inspection	Activities such as measuring, examining, testing, gauging one or more characteristics of a product or service and comparing these with specified requirements to determine conformity
Yield	Percentage of products that pass all tests
Defect	The non-fulfillment of intended features and usage requirements

- human error and workmanship inadequacies; and
- unintended stresses (e.g., contaminants, particles, vibration) in the manufacturing environment.

The quality assurance process involves statistical process control, in-process monitoring, and if necessary, screening tests. Quality assurance requires the manufacturer to:

- identify potential defects using in-line process monitors and statistical process control;
- conduct root cause analysis to determine the defects and failure mechanisms that would cause early-life failures of the product;
- determine where in the process flow the defects arose, and implement process improvements to solve the process problems;

Petitioner Samsung Ex-1055, 0413

- evaluate the economy of screening, and select screens that activate the failure mechanisms which will expose the potential defects;
- reduce or eliminate screening as warranted.

7.7.1 Screening Overview

Screening is a process of inspection and testing of 100% of the devices in a lot (or batch) for the purpose of identification and elimination of defects. Screening can be classified as stress and non-stress screening. Stress screening involves subjecting the electronic parts to electrical and environmental stresses in order to precipitate failures. Non-stress screens are essentially non-contact-type tests that are performed to detect defects rather than precipitate failures by applying loads. Non-stress screens include visual inspection, radiography, acoustical microscopy, electrical functional tests, and electrical parametric tests. If screening must be conducted, then the preferred screens are non-stress, followed by stress screens.

Screening is a quality conformance task. It is an audit process to ensure that the product's materials and manufacturing conform to the control limits of the production processes. Screening involves both the early detection of product parameters that are out of tolerance limits and the precipitation of defects. Defect detection is most effective when conducted at the time the defect is created. Thus, in order to be proactive, screening should be part of the in-line manufacturing processes associated with quality control. Screening at individual process stages can ensure that defects detected are attributed to a specific manufacturing step, thereby facilitating immediate corrective action and minimizing troubleshooting and rework costs. In some cases, a defective part may be eliminated immediately, preventing additional costs from accruing on a product of poor quality.

Defects can be classified into two types with respect to screening: patent defects and latent defects. Patent defects are inherent or induced defects that can be detected by non-stress screening tests such as inspection and functional test [56]. Latent defects cannot be detected by inspection or functional tests, and can be precipitated to early failures under stress screening. With advancements in electronics technologies and significant improvements in reliability, many studies question the effectiveness of screening in precipitating defects, and suggest that the screening process may be more harmful to the product than beneficial.

Through an understanding of the failure mechanisms that affect the product, PoF allows for the identification of design parameters which

Petitioner Samsung Ex-1055, 0414

affect product life and the stress conditions which can be used to precipitate failure. This information is used to select appropriate stress tests to be used as screens. PoF is used to define stress conditions that will produce failures in defective products with design parameters below a desired threshold. More importantly, it identifies the damage induced in products subjected to a screen which is critical information in determining if the screen will result in compromised reliability of the surviving products [57].

7.7.2 Stress Screening and Burn-In

Burn-in is a stress screening test performed on electronic parts to precipitate defects. The process consist of placing the parts in a thermal chamber for a specific amount of time and applying accelerated thermal stress under an electrical bias during and after which they are tested for functional performance. Other accelerated conditions may also be applied during burn-in including voltage, humidity, electric field, and current density [58]. The parts that fail the device manufacturer's specifications are discarded and the parts that pass are used.

Burn-in as a screening requirement originated during the Minuteman Missile Program where it was found to be an effective test in precipitating defects in low-volume and immature electronic parts. By 1968, burn-in was included in the military standard MIL-STD-883 [59], and was implemented in many military and non-military parts qualification process. However, with maturing technologies and improvements in parts quality and reliability, the effectiveness of burn-in has diminished.

There is evidence that burn-in is no longer precipitating defects [60–62]. The failure rates during burn-in have reduced dramatically from approximately 800 parts per million in 10^9 hours in 1975 to only 1 part in million in 1991 [63]. In 1990, the Motorola Reliability Group commented that [64]: "The reliability of integrated circuits has improved considerably over the past five years. As a result, burn-in prior to usage does not remove many failures. On the contrary, it may cause failures due to additional handling." In 1994, Mark Gorniak of US Air Force stated that [64] "Although manufacturers continue to use these screens today, most of the screens are impractical or need modification for new technologies, and add little or no value for mature technologies."

Many manufacturers have eliminated burn-in and instead rely on parts family assessment and qualification [61,62]. The manufacturer

Petitioner Samsung Ex-1055, 0415

part family assessment depends on the supplier. Parts must come from a supplier that:

- periodically certifies the parts;
- implements statistical process control;
- has acceptable qualification testing results;
- abides by procedures to prevent damage or deterioration (e.g., handling procedures, such as electrostatic discharge bags);
- provides change notifications.

The qualified parts from the supplier are then subjected to the manufacturer qualification process. The results of the qualification tests can be used to assess whether burn-in is necessary or not. If the qualification tests produce no failures, and the manufacturing process is in control, then the part quality can be assessed with confidence and without the need for burn-in.

7.7.3 Screen Selection

Screening can detect or expose defects by inspection (non-stress screening) or by subjecting the product to electrical, mechanical, or thermal loads (stress screening). The applied loads in stress-screening are not necessarily representative of service loads, and are often applied at an accelerated level to reduce the TTF for a weak product. A stress screen may activate more than one failure mechanism at more than one site in a product.

Stress screens can be further categorized as wearout screens and overstress screens based on the failure mechanism that causes failures in weak products. Wearout screens activate fatigue, diffusion, and tribological wear mechanism, whereas overstress screens cause the stress level at the defect site to exceed the local strength, leading to catastrophic failures. Wearout screens include temperature cycling and vibration. These screens lead to damage accumulation and eventually cause failures in weak products that have defects. A fraction of the useful life of the product is also consumed by the screens due to damage accumulation. Ensuring that the remaining useful life of the screened product meets the requirement is critical. The screen parameters should be such that failures occur only at the defect sites with minimal consumption of the useful life.

Overstress screens include bond pull test and thermal shock. An overstress screen is preferred over a wearout screen, because an overstress screen precipitates failure instantaneously and does not cause damage

Petitioner Samsung Ex-1055, 0416

accumulation in a defect-free product. However, overstress screens must be very carefully implemented or they can cause product yield problems.

A defective product that will fail early in service by a wearout failure mechanism may be detected by employing an overstress screen. For example, consider a defective product that has a crack in the solder joint which fails early in service due to stable crack propagation driven by environmental temperature cycles. An overstress screen constituting a mechanical shock applied to the leads can detect the lead with the cracked solder joint if the load is within the design limits, but high enough to cause unstable crack propagation in the solder joint if the crack length is larger than an allowable value.

Screens must be selected and tailored for the specific defects or failure mechanism(s) at the specific defect site(s) in order to be effective. The defects and the potential defect site(s) depend on the product processing technology. Table 7.9 lists common screens and defects exposed by each screen.

Regardless of the screens employed, the design life of the product must not be compromised. The life used up by screening can be calculated by continuously running the screen over and over again until failure occurs; the percentage life used from a single screen can then be calculated. One can also run an accelerated life test on the previously screened products and apply the appropriate acceleration model to compute the remaining service life at use conditions.

7.7.3.1 Screen Stress Levels

Step-stress analysis is a common technique used to establish screening stress levels. In this procedure, progressively stronger stresses are imposed on a sample of the product. Failure analysis is conducted on the failed product to determine the cause of each failure. If the cause is due to a latent defect, and not due to overstress, the stress level is increased to the next higher level. The process is continued until overstress failures are observed. The stress level that causes overstress failures determines the upper limit of the stress and the stress for the screen is decided based on the defects that are required to be precipitated.

Another technique for establishing screen stress level is called error seeding, whereby known measurable defects are introduced into the product. Thus, the failure mechanisms and the stresses that stimulate the defects are known. The stress level is progressively increased until all seeded defects in the sample are precipitated. The stress level is thus fixed to screen out the known defects. While simple in principle, error seeding is difficult and expensive in practice.

Petitioner Samsung Ex-1055, 0417

Table 7.9 Screens and the Defects They Can Expose

Screen	Defects Exposed	Effectiveness	Cost	Limitations
Visual inspection (optical microscopy)	• Package non-planarity • Surface defect, such as improper marking, passivation cracks, contamination, foreign material, burrs on leads and paddle • Misaligned leads • Lifted or broken wires • Lifted or chipped die • Improper die mounting • Dimensional inaccuracies • Encapsulant flash • Corroded die • Metallization voids • Bridging conductive paths • Localized corrosion • Bond intermetallics • Chipped die and improper metallization	Good	Inexpensive	• Labor intensive • Probability of escape increases with increasing complexity and magnification • Automated inspection is often preferred to reduce human subjectivity and human error

(*Continued*)

Petitioner Samsung Ex-1055, 0418

Table 7.9 Screens and the Defects They Can Expose (*Continued*)

Screen	Defects Exposed	Effectiveness	Cost	Limitations
X-ray microscopy	• Package non-planarity • Misaligned leads • Lifted or broken wires • Wire sweep • Paddle shift • Voids	Good	Moderate	• Subject to operator interpretation
Acoustic microscopy	• Encapsulant voids and inclusions; • Paddle shift • Wirebond sweep • Cracked die • Interface cracks, delaminations, and disbonded areas • Die attach voiding	Good	Moderate	• Subject to operator interpretation • Only scanning laser acoustic microscopy is production oriented
Temperature cycling (air to air)	• Encapsulant cracking, delamination of interfaces	Good	Inexpensive	• Damage accumulation technique which can use up useful life
Thermal shock	• Delamination	Poor	Expensive	• Highly accelerated stress • Can cause unwanted problems to arise (best as sampling technique opposed to a screen)
Moisture resistance	• Contaminants in package, on the leads, or on the die	Good	Expensive	• Can use up useful life (best as sampling technique as opposed to a screen)

Petitioner Samsung Ex-1055, 0419

In addition to the two methods mentioned above, the failure site with the failure mechanism can be effectively used in screen selection. The method involves the development of models that incorporate possible manufacturing variations or flaws. The stresses required to precipitate the latent defects are then computed. The quantitative model can also provide a means to assess the damage introduced by the screen in defect-free products. These models often involve finite element analysis.

7.7.3.2 Screen Duration

In stress screening, one may find multimodal distributions caused by a combination of early failures (due to defects) and wearout failures (due to physicochemical processes). The distribution of TTF can vary in many ways. By plotting failure density along the y coordinate and TTF on the x coordinate, distributions such as mono-modal, bi-modal or multi-modal can be obtained. The failure density, $f(t)$, at time t is expressed by

$$f(t) = \frac{1}{N}\frac{d[N - \bar{N}(t)]}{dt} \tag{7.3}$$

where N is the device population at time $t = 0$, and $N(t)$ is the number of devices at time t.

A multimode distribution of failure density can arise when there are mixed products, designs, vendors, or manufacturing lines. Figure 7.14 illustrates a TTF distribution characteristic of a mixed population of products from different vendors. The combination of the individual TTF distributions results in a distribution with multiple peaks. The duration for the application of a screening stress, for a known failure distribution, should satisfy the condition that the remaining life be greater than or equal to the expected life of the product.

Figure 7.15 shows a failure distribution pattern with two peak subpopulations of devices (i.e., the area under the first two peaks) and a main population (i.e., the area under the largest peak) separated by a region of useful life which has low failure probability. A stress screen can be employed that consumes time, t_s, at operating conditions, exposing the defective product. The useful life of the remaining devices is shortened by a time equal to t_s.

If the two peaks are close to each other, as shown in Fig. 7.16, screening would consume a significant portion of the design life. In some cases, if the failure mechanisms associated with each peak can be activated independently, then screening is realistic, as long as the removal of the

Petitioner Samsung Ex-1055, 0420

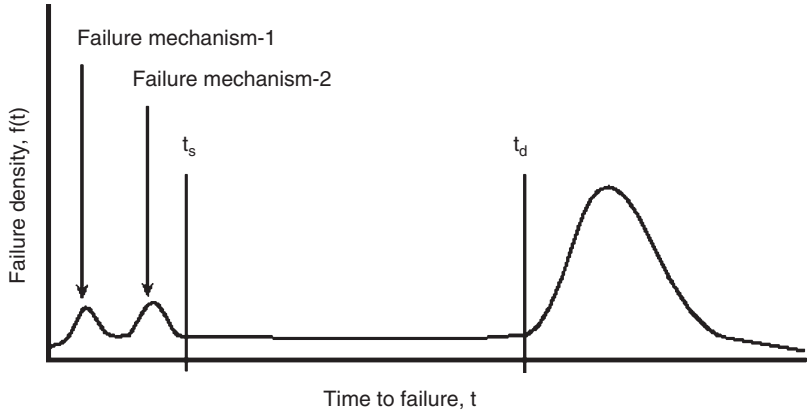


Figure 7.14 A time-to-failure distribution characteristic of a mixed population of products from different vendors.

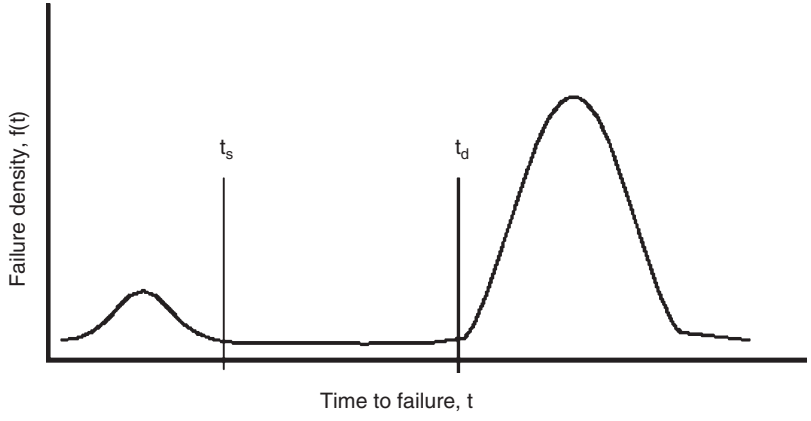


Figure 7.15 A failure distribution pattern with two weak subpopulations of devices.

mechanism causing the earlier failures does not seriously reduce the useful life of the remaining devices. Screening should be conducted to precipitate the failure mechanism that causes failures of the first group so that the useful life of the remaining screened product is not reduced.

7.7.4 Root-Cause Analysis

Failures that arise as a result of screening must be analyzed to determine their root-cause. Fault tree analysis may help eliminate certain possible causes. Using simulation and controlled experiments, the causes of the

Petitioner Samsung Ex-1055, 0421

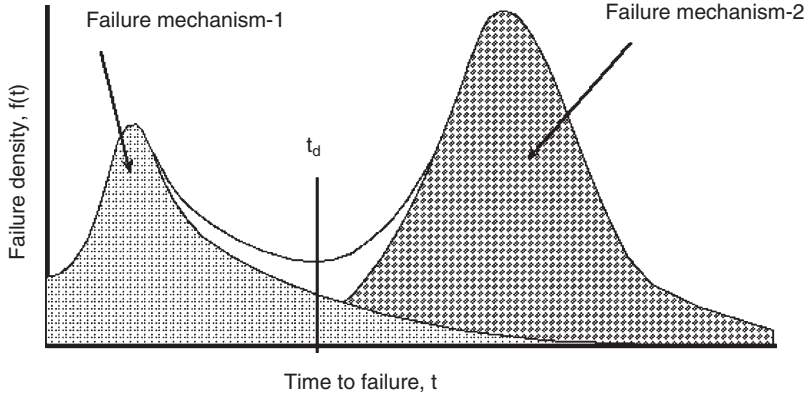


Figure 7.16 Failure distribution pattern with two peak subpopulations of devices close to each other.

defects and their contributing factors are established. The major factors are in turn traced back to possible root causes in defective material, design, manufacture, handling, or testing. Manufacturing defects may be caused by process parameters that are out of the tolerance limits, unstable, not immune to noise, and by contaminants present in the environment. Once the root-cause has been identified, a large amount of old and new material must be generated, processed through the stress, and the results statistically compared.

If almost all the products fail in a properly designed screen test, it shows that the design is incorrect. If a large number of products fail, a revision of the manufacturing processes is required. If the number of failures in a screen test is negligible, the processes should be in control and any observed faults may be beyond the control of the design and production process. At the time the process matures and screening rejects decrease, the decision to screen is economical, because it may be appropriate to replace a 100% screen for statistical process control purposes (the preferred approach). High product reliability can be assured only through the use of robust product designs, capable processes that are kept in control, and qualified components and materials from qualified supplier processes.

7.7.5 Economy of Screening

The decision as to when and how to screen a product is largely influenced by the economics of screening. In making this decision, the following factors must be considered: the expected level of defects existing in the product; the cost of field failures (cost of not screening); the cost of

Petitioner Samsung Ex-1055, 0422

screening; the potential cost of introducing new defects by screening; and, if applicable, the reduction in useful life.

In the early life cycle of a product, failure mode effects techniques should be initiated. At each process step, the possible flaws that might be added to the product are identified and statistically based controls or monitors added to the process flow. Such techniques are generally more economical and more sensitive to detecting process changes.

Screening techniques should then be reviewed for inclusion based on engineering judgment and the history from similar products. A cost-effective screening procedure addresses all potential defects, employs screens that cause minimal damage to good products, and ensures that the screened products meet the service life requirement. The time required for the individual screen must be minimized to make it cost-effective. Screens can be applied either sequentially or simultaneously, depending on the latent defects that are targeted, available hardwares, and manufacturing constraints.

Products with standard designs and relatively mature processes need to be screened only if service failure returns indicate early failures, or as a check to ensure that the processes are under control. Screening is recommended for all new products, and those that do not employ mature manufacturing processes. Screening in such cases not only improves the reliability of the new products but also assists in process control.

7.7.6 Statistical Process Control

Process control represents action on the process to avoid the production of substandard work, rather than action on the output to segregate any substandard work that has been made. Controlling the process is clearly preferable to inspecting the output.

Statistical process control is a methodology to analyze a process and its outputs, so as to continually reduce variation in processes and products. The goal is to stop defects from occurring in order to cost-effectively provide product that meets customer requirements.

Statistical process control involves conducting measurements on critical process parameters of the products. Control charts are plotted, and upper and lower control limits are established. The control charts reveal when the process is drifting out of control, and steps are taken to bring the process within control limits before it drifts out to some unacceptable value. The control parameter can be either a variable or an attribute. Accordingly, there are two basic types of control charts: control charts for variables (x-bar charts, range charts) and control charts for attributes (p charts, c charts).

Petitioner Samsung Ex-1055, 0423

The generic steps in statistical process control include evaluation of process behavior by means of control charts, determination of process variability, and corrective actions to ensure that the process is in control. This real-time feedback can be used to stop a process before a defect occurs. Defects that can be introduced by means other than systematic drifts in a process are not the target of statistical process control.

The most widely used quality system is ISO 9000 which is a series of standards created by ISO (ISO 9000:2005). The purpose of ISO 9000 is to promote the international exchange of goods and services by means of developing an international quality and reliability standard.

Another widely used statistical process control methodology and quality system is Six Sigma which was initiated by Motorola in mid 1980s. It was later fine-tuned and popularized by General Electric and Allied Signal in 1990s. The premise of Six Sigma is based on a statistical goal that the failure rate of a product must be as low as that at six standard deviations (represented by sigma or σ) from the mean of any process, design, or product parameter as depicted in Fig. 7.17. A product or process with six sigma quality has 3.4 defects in million which translates into 99.99976% reliability.

The Six Sigma process consists of five main phases: define, measure, analyze, improve, and control (DMAIC) as shown in Fig. 7.18. In Six Sigma methodology, the following actions must be taken:

- Define the product or process opportunities or problems;
- Measure the performance of products and processes;

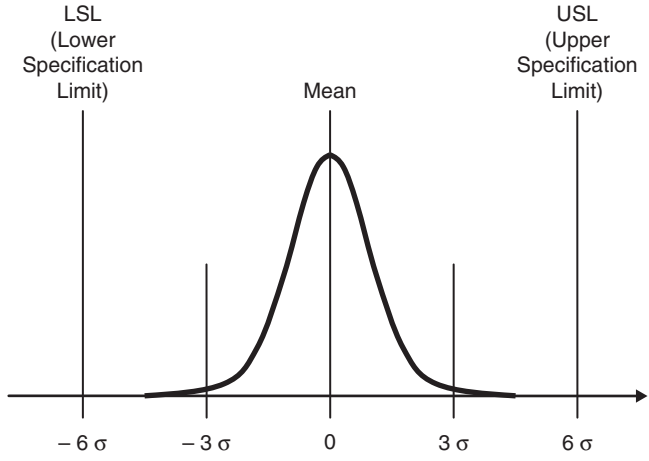


Figure 7.17 Six Sigma statistical goal for process and product quality.

Petitioner Samsung Ex-1055, 0424

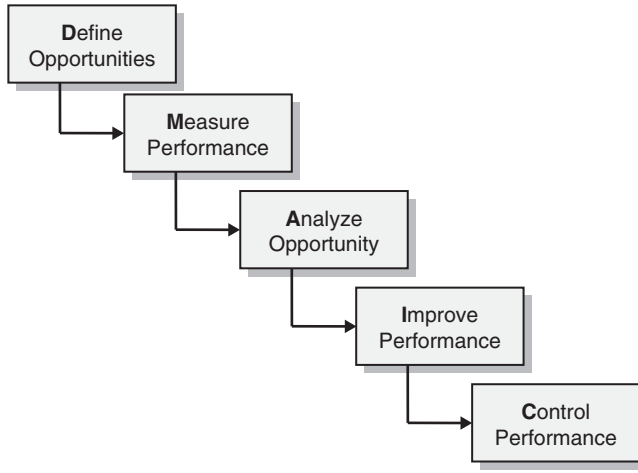


Figure 7.18 Six Sigma process DMAIC.

- Analyze the opportunities or problems to identify root causes;
- Improve the performance by redesigning processes and minimizing variability;
- Control the processes to ensure permanent improvements.

7.8 Summary

Qualification is an application-specific process involving the evaluation of the product with respect to its quality and reliability. The aim of the qualification process is to verify whether the product meets or exceeds reliability and quality requirements of the intended application.

Qualification process consists of three stages: virtual qualification, product qualification, and mass production qualification (or quality assurance testing). Virtual qualification is based on PoF model predictions on the life of the design without any physical testing. Virtual qualification is relatively less expensive and less time consuming than product qualification. Product qualification involves physical tests on the manufacturer prototype including HALT to determine the strength limits of the product and accelerated testing for reliability assessment. Accelerated testing is used in qualification process because it provides the advantage of time compression. It accelerates the failures to occur earlier in time due to the higher levels of stresses than what the product would experience in an application

Petitioner Samsung Ex-1055, 0425

environment. They are, therefore, more time and cost-efficient. However, it should be ensured that only the failure mechanism under evaluation is being accelerated, while no other failure mechanisms are introduced.

The third stage of qualification is quality assurance testing or screening. The overall quality assurance process consists of statistical process control, in-process monitoring, and screening. The purpose of screening is to precipitate defects. Screening can be classified as stress and non-stress screening. Burn-in is a stress screening that involves applying high thermal stresses to the electronic packages under electrical bias and conducting functional tests during and after.

As the technology has matured and improvements have been made to part quality and reliability, the effectiveness of stress screening and burn-in have diminished. Stress screening may need to be conducted only if the technology is new and many defects are expected. In general, if screening has to be done, non-stress screening is preferred to stress screening. Also, if screening must be done, screening during the process flow is preferred to the end-of-the-line or final product screening. The information from the root-cause analysis on the defects and failures observed during screening can be used to improve the package design, materials, and processes, and thus reduce or eliminate future defects. The preferred approach in quality assurance, however, is statistical process control and part family assessment. If the part is determined to be meeting quality requirements, the qualification results can be used to determine whether screening is needed or not.

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Petitioner Samsung Ex-1055, 0426

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Petitioner Samsung Ex-1055, 0427

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Petitioner Samsung Ex-1055, 0429

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Petitioner Samsung Ex-1055, 0430

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8 Trends and Challenges

Microelectronic devices, packaging designs, and materials have dramatically improved over the past decades. Integrated circuit (IC) chips are now much smaller and faster, and the packaging is more efficient, reliable, and cost-effective. In this chapter, the trends and challenges for future microelectronic devices, packaging, and plastic encapsulants are presented. Recent trends in applications of plastic packages for extreme high and low temperatures are stated. Trends and challenges in the plastic encapsulation of microelectromechanical systems (MEMS), bio-MEMS, and bioelectronics, nano-electronics, and organic light-emitting diodes (OLEDs), photovoltaics, and optoelectronics are discussed.

8.1 Microelectronic Device Structure and Packaging

Microelectronic chip technology has developed significantly over the past half a century. The IC complexity and the number of transistors per chips have increased continuously over the years. Figure 8.1 shows the trend in the number of transistors per chip made by Intel Corporation following Moore's law prediction. First introduced in 1965 by Gordon Moore (one of the co-founders of Intel), and later updated in 1975, Moore's law predicts that the IC complexity (i.e., number of transistors per chip) doubles every 2 years. One of the latest Intel chips is the Dual-Core Intel Itanium 2 processor 9000 series with more than 1.7 billion transistors per chip, more than 200 times the number of transistors a decade earlier. This trend, however, will eventually reach a limit. The semiconductor sizes are becoming smaller approaching 32 and eventually 22 nm [1,2]. As the size approaches atomic scales, it is more difficult to fit higher number of transistors on a chip.

As semiconductor complexity reaches its physical limits, the focus is shifting towards improving packaging designs, functional diversification, and materials innovations. Focusing beyond Moore's law has led to the arrival of a new technological era known as More than Moore (MtM) [3–10].

As depicted in Fig. 8.2, the miniaturization trend in transistors will continue to follow Moore's law reducing to 32 and 22 nm sizes and reaching beyond complementary metal-oxide semiconductor devices. Simultaneously,

Petitioner Samsung Ex-1055, 0432

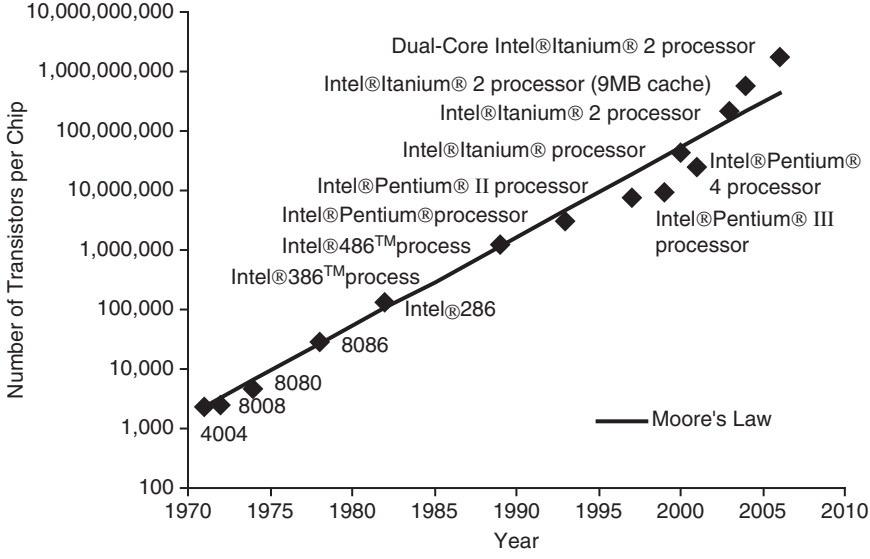


Figure 8.1 Number of transistors per chip following Moore's law (www.intel.com).

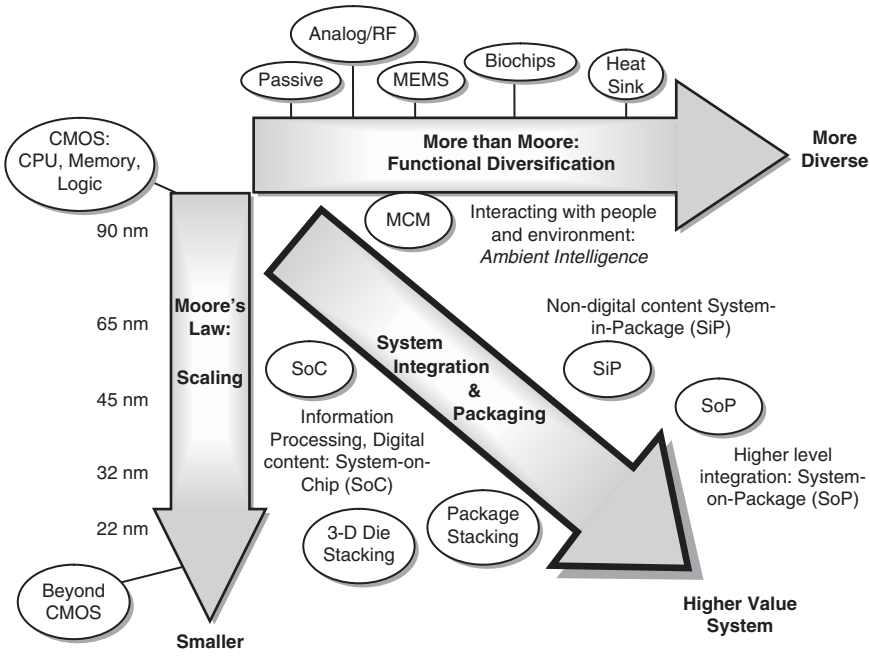


Figure 8.2 Moore's law, "More than Moore" approaches combined with system integration for development of high value systems [1,8].

CMOS: Complementary metal-oxide semiconductor; CPU: Central processing unit; MCM: Multi-chip module; MEMS: Microelectromechanical systems; RF: Radio-frequency.

Petitioner Samsung Ex-1055, 0433

a second trend of More than Moore is occurring where the functional diversification of components increases in a package including IC chips, sensors, passives, MEMS, biochips, etc. With functional diversification, electronics interaction with people and environment is further developed and "ambient intelligence" can be achieved. A third trend is system integration and packaging innovations which benefits from other two trends, smaller transistors and more diverse devices, and leads to higher value systems.

From a historical perspective, system integration and miniaturization trend began in 1960s with the development of ICs on a single chip known as system-on-chip as shown in Fig. 8.3. The level of integration and percent of miniaturization has increased since then to include both passive, active components and other functionally diverse devices such as MEMS, biochips, sensors, and radio-frequency (RF) devices all in a single package known as system-in-package (SiP). The development of SiP was further

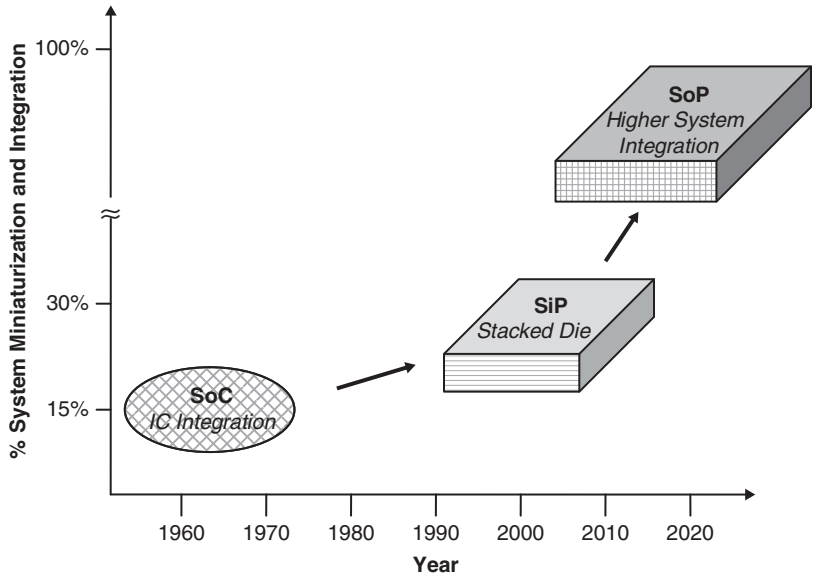


Figure 8.3 Miniaturization and integration trends of ICs in 1960s to systems in 2020s [10].

IC: Integrated circuit; SiP: System-in-package; SoC: System-on-chip; SoP: System-on-package.

Petitioner Samsung Ex-1055, 0434

enabled by packaging innovations such as 2D packaging (i.e., multi-chip modules) and 3D packaging (i.e., die stacking).

System integration and miniaturization is expected to increase to an even higher level referred to as system-on-package (SoP) which is forecasted to take place by 2020s [3,10]. Using SoP integration, the second level packaging that traditionally involves printed circuit boards, connectors, sockets and thermal cooling devices can effectively disappear and be integrated inside the single package along with IC chips, passive devices, MEMS, sensors, RF devices, and biochips.

Figure 8.4 shows a historical timeline and trend for microelectronic packaging. Besides demand for miniaturization, other factors such as environmentally friendly materials and emerging technologies can influence the trend. The early package designs such as dual in-line packages and Small outline packages (SOPs) developed in 1970s were replaced by ball-grid arrays (BGAs), flip-chips, and chip-scale packages (CSPs) in 1980s and 1990s. The packages developed in 2000s include SiP including 3D die stacking, wafer-level package ([1], iNEMI, www.inemi.org) which will continue to be used well into 2010s and even 2020s. Environmentally friendly or "green packaging" will continue to be an integral aspect of packaging materials and designs. Packages in 2010s and 2020s may also include emerging device packages and SoPs.

Table 8.1 lists some of the challenges foreseen in microelectronic packaging [1]. Figures 8.5 and 8.6 show requirement trends for single-chip device and packaging technology based on the International Technology Roadmap for Semiconductors (ITRS) [1]. Figure 8.5 shows a selection of the dimensional and pin count characteristics of single-chip packages over the next several years. The dynamic random access memory (DRAM) half pitch is expected to reduce to about 10 nm by early 2020s at a decreasing rate of 3 nm per year. The chip size is expected to remain the same, or in case of high-performance package slightly increase to 750 mm^2 in 2020s. The package overall profile is required to be reduced to 0.15 mm for low-cost/hand held packages in 2020s. The maximum package pin count is predicted to increase to about 5000 for cost-performance device and close to 9000 for high-performance device in 2020s.

Figure 8.6 shows selected performance and thermal characteristics of the single-chip packages [1]. The maximum power is predicted to approach 2 watts/mm^2 for cost-performance device packages in 2020s. The performance of on-chip is expected to reach slightly more than 14 GHz by early 2020s for both cost- and high-performance single-chip packages. The extreme operating and maximum junction temperatures for low cost packages

Petitioner Samsung Ex-1055, 0435

Figure 8.4 Semiconductor packaging and encapsulation technology trend.

µBGA: Micro-ball-grid array; DIP: Dual in-line package; LQFP: Low-profile quad flatpack; MEMS: Microelectromechanical systems; PCB: Printed circuit board; PLCC: Plastic-leaded chip carrier; QFP: Quad flatpack; SOP: Small outline package; TBGA: Tape-automated-bonded plastic ball-grid array; TQFP: Thin quad flatpack; TSOP: Thin small-outline package; WBGA: Wire-bonded ball-grid array.

Petitioner Samsung Ex-1055, 0436

Table 8.1 Some of the Challenges in Future Semiconductor Packaging [1]

Challenges	Issues
Wafer-level chip scale package	• I/O pitch for small die with high pin count • Solder joint reliability and cleaning process • Wafer thinning and handling technologies • CTE mismatch compensation for large die
Embedded components	• Low cost embedded passives: R, L, C • Embedded active devices • Wafer-level embedded components
Thinned die packaging	• Wafer/die handling for thin die • Different carrier materials (organic, silicon, ceramics, glass, laminate core) impact • Establish new process flow • Reliability and testability • Different active devices • Electrical and optical interface integration
Close gap between chip and substrate	• Increased wireability at low cost • Improved impedance control • Improved planarity and low warpage at higher process temperatures • Low moisture absorption • Increases via density in substrate core • Alternative plating finish to improve reliability • T_g compatible with Pb-free solder processing (including rework at 260°C)
3D packaging	• Thermal management • Design and simulation tools • Wafer to wafer bonding • Through wafer via structure and via fill process • Singulation of TSV wafers/die • Test access for individual wafer/die • Bumpless interconnect architecture
Flexible system packaging	• Conformal low cost organic substrates • Small and thin die assembly • Handling in low cost operation
Small die with high pad count and/or high power density	• May exceed the capabilities of current assembly and packaging technology • Requiring new solder/UBM with improved current density capabilities, and higher operating temperatures

(*Continued*)

Petitioner Samsung Ex-1055, 0437

Table 8.1 Some of the Challenges in Future Semiconductor Packaging [1] (*Continued*)

Challenges	Issues
System-level design capability to integrate chips, passives, and substrates	• Performance, reliability and cost optimization for complex systems • Complex standards required for information types, management of information quality, and a structure for moving the information • Embedded passives may be integrated into the "bumps" as well as the substrates
Emerging device types (organics, nanostructures, biological)	• Organic device packaging requirements not yet defined (e.g., will chips grow their own packages) • Biological interfaces will require new interface types

T_g: Glass transition temperature; TSV: Through silicon via; UBM: Under bump metal.

is expected to remain unchanged at 55°C and 125°C, respectively. The extreme operating and maximum junction temperatures for single-chip packages designed for harsh environment applications are expected to withstand extreme operating and maximum junction temperatures of 200°C and 220°C, respectively.

Table 8.2 shows a roadmap for chip-to-substrate and substrate-to-board packaging [1]. The general trend is reduction of pitch sizes for various bonding techniques. Pitch sizes are expected to be in the range of 10–85 μm (or 0.01–0.085 mm) for various chip-to-substrate bonding techniques in 2020s. Substrate-to-board bonding pitch sizes are expected to reach 0.5 mm or below for various BGAs, CSPs, and quad flatpacks by the year 2020s with the exception of plastic BGA pitch size of 0.65 mm.

As the bonding pitch sizes decrease for chip-to-substrate or substrate-to-board bonding, the requirement for encapsulant material and encapsulation technique becomes more stringent. The encapsulant material must flow easily through narrow spaces and small protrusions and the encapsulation technique must have lower pressure to protect and minimize damage in the delicate bonding assembly.

The maximum number of stacked dies in wafer-level CSPs is expected to increase to twelve levels by early 2020s for the case of memory chips as shown in Fig. 8.7. The standard and wireless chips are expected to remain at three-level die stacks for the next several years.

Petitioner Samsung Ex-1055, 0438

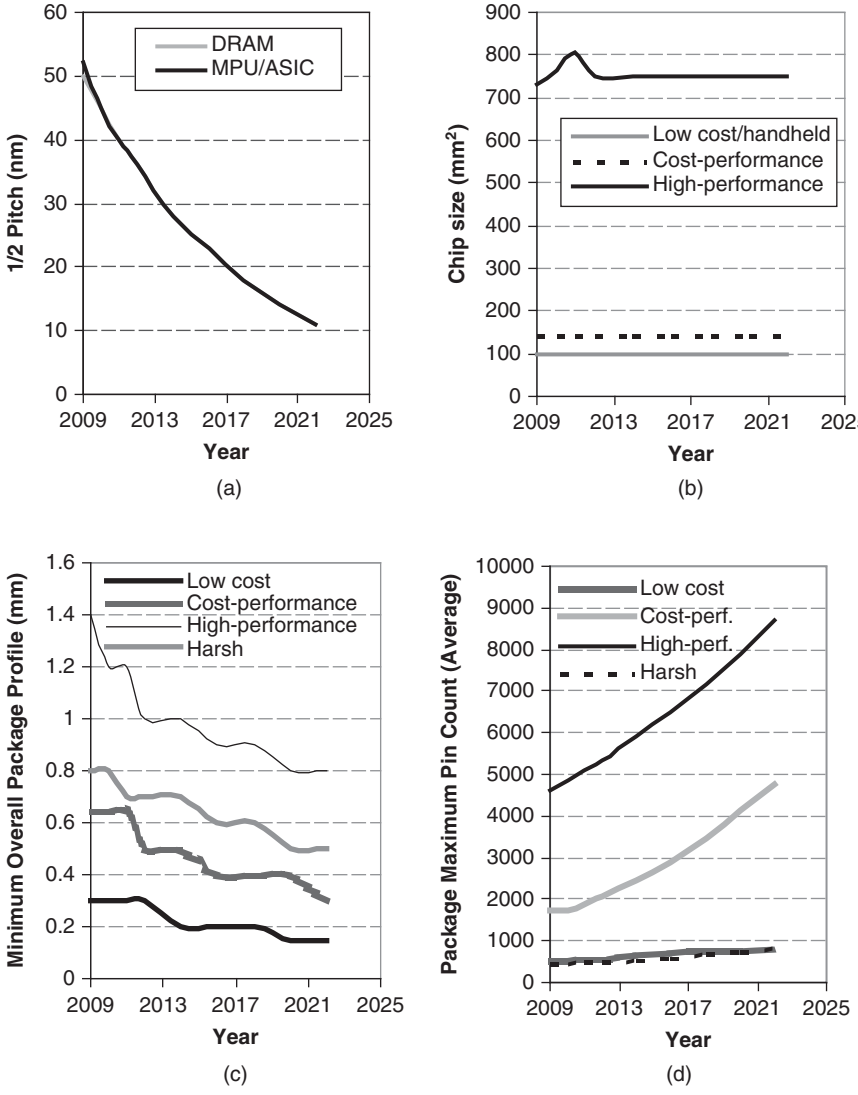


Figure 8.5 Trends in single-chip package technology based on ITRS requirements for (a) ½ pitch size, (b) chip size, (c) minimum overall package profile, and (d) maximum pin count [1].

ASIC: Application Specific Integrated Circuit; DRAM: Dynamic random access memory; ITRS: International Technology Roadmap for Semiconductors; MPU: Micro-Processing Unit.

Table 8.3 shows some of the challenges foreseen in packaging materials. Two common challenges related to encapsulant materials are stress reduction on low-κ wafer structures and compatibility with environment friendly lead-free materials and processing. Specifically, for encapsulants, the challenge is

Petitioner Samsung Ex-1055, 0439

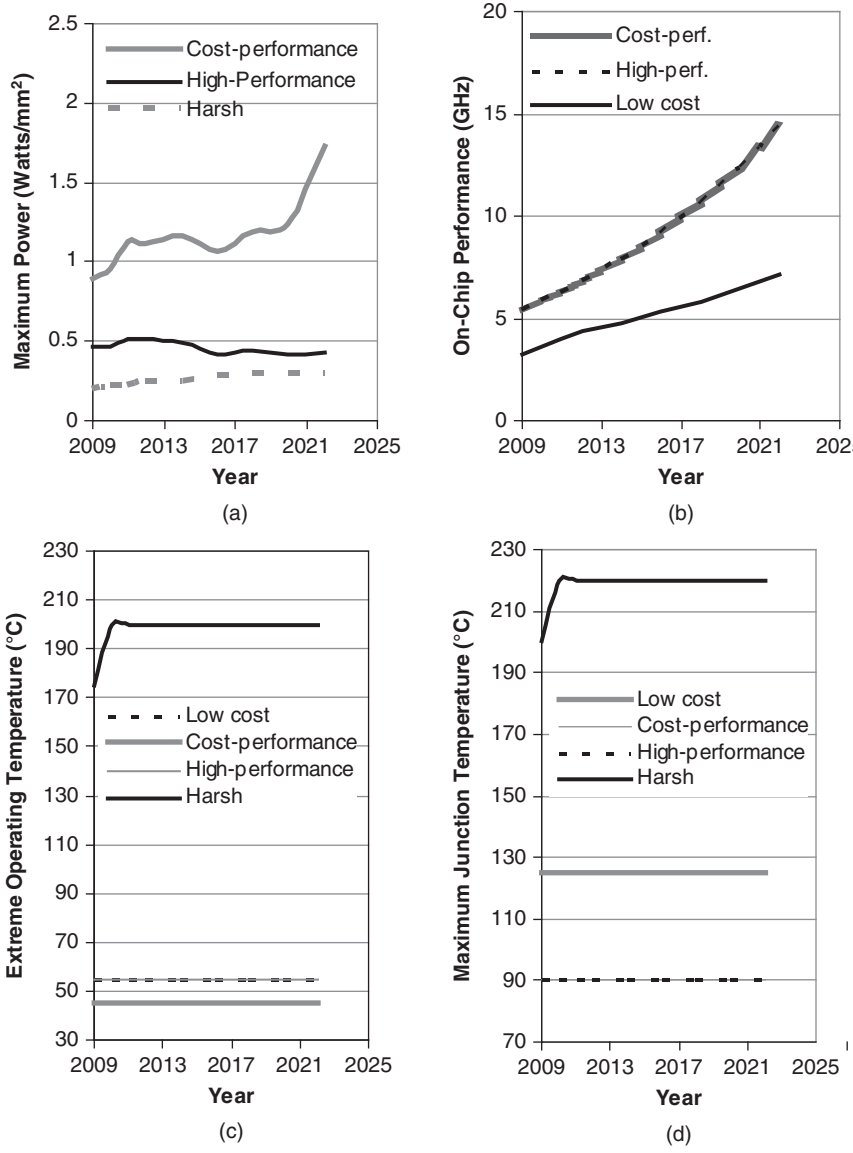


Figure 8.6 Trends in single-chip package technology based on ITRS requirements for (a) maximum power, (b) on-chip performance, (c) extreme high operating temperatures, and (d) maximum junction temperatures [1].

to minimize moisture absorption for high temperature lead-free applications, and for underfills, compatibility with lead-free reflow characteristics.

Compression molding technique is more suitable for thinner packages compared to transfer molding. In conventional compression molding the

Petitioner Samsung Ex-1055, 0440

Table 8.2 Chip-to-Substrate and Substrate-to-Board Bonding Technology Roadmap [1]

Year	2009	2010	2012	2014	2016	2018	2020	2022
Chip-to-Substrate Bonding								
Wire bond								
Single in-line (μm)	35	35	30	30	25	25	25	25
Wedge pitch (μm)	20	20	20	20	20	20	20	20
Flip-chip								
Area array (both organic and ceramic substrate) (μm)	130	130	110	100	85	95	90	85
On tape or film (μm)	10	10	10	10	10	10	10	10
TAB (μm)	35	35	35	35	35	15	15	15
Substrate-to-Board Bonding								
BGA solder ball pitch (mm)								
Low-cost and handheld	0.65	0.65	0.5	0.5	0.5	0.5	0.5	0.5
Cost-performance	0.65	0.65	0.5	0.5	0.5	0.5	0.5	0.5
High-performance	0.8	0.8	0.65	0.5	0.5	0.5	0.5	0.5
Harsh	0.65	0.65	0.5	0.5	0.5	0.5	0.5	0.5
CSP area array pitch (mm)	0.2	0.2	0.15	0.1	0.1	0.1	0.1	0.1
QFP lead pitch (mm)	0.3	0.3	0.3	0.3	0.2	0.2	0.2	0.2
PBGA ball pitch (mm)	0.8	0.65	0.65	0.65	0.65	0.65	0.65	0.65

BGA: Ball-grid array; CSP: Chip-scale package; PQFP: Plastic quad flatpack; QFP: Quad flatpack; TAB: Tape-automated bonding.

Petitioner Samsung Ex-1055, 0441

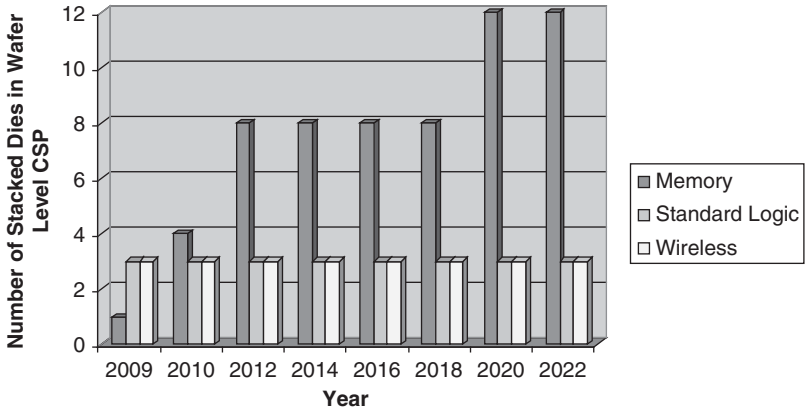


Figure 8.7 Trend for maximum stacked dies in a wafer-level chip-scale package (CSP) [1].

molding compound blocks are placed on the IC chip assembly, heated, and then compressed. The compressed molten compound is forced to flow around the chips, through wires and into protrusions.

Towa Corp (Kyoto, Japan) and Apic Yamada Corp. (Nagano, Japan) have introduced new molding machines based on modified compression molding techniques [11]. The new molding techniques introduced by Towa and Apic Yamada can lower molding pressures to a fraction of conventional transfer-molding systems and are highly suitable for thinner and more complex SiP, package-on-package (PoP), wafer-level packaging, and transparent resin packaging.

Towa Corp. has developed a type of compression molding machine called Flow Free Thin (FFT) molding system. In this molding technique, IC chips are put on a board and the board-chip assembly is immersed into a molten resin in the lower mold as shown in Fig. 8.8. The encapsulant material is then solidified, and the encapsulated package is removed. The advantages of the FFT molding technique are

- lower pressure on chips;
- gold wires are not destroyed or cut;
- suitable for map molding or wafer-level packaging which involves molding dozens of chips at once;
- does not require a gate or runner, which reduces waste, particularly important for encapsulating high-brightness LEDs with expensive transparent resins.

Petitioner Samsung Ex-1055, 0442

Table 8.3 Packaging Materials Challenges [1]

Material Challenges	Issues
Wire bond	• Materials that enable 25 and 16 μm pitch without wire sweep • Barrier metals for Cu wire bond pads to reduce intermetallics (i.e., insulated wire)
Underfills	• Ability to support 100 pitch on large die • Reduce stress on low-κ die • Compatibility with lead-free reflow temperature
Thermal interfaces	• Increased thermal conduction • Improved adhesion • Higher modulus for thin applications
Material properties	• Characterization database for frequencies above 10 GHz
Molding compound	• Molding compound for low profile multi-die packages • Compatible with low-κ wafer structures • Low moisture absorption for high temperature lead-free applications • Molding compound for hybrid wire bond and flip-chip without underfill • Gate leakage associated with charge storage in halogen free molding compounds • Metal particle contamination and carbon black causing shorts and assembly yield problems for fine pitch interconnect
Lead-free solder flip-chip materials	• Solder and UBM that supports high current density and avoid electromigration
Low stress die attach material	• High junction temperature: $T_j > 200°C$ • Requires compensation for CTE mismatch with high thermal and electrical conductivity
Rigid organic substrates Embedded passives	• Lower dielectric loss • Lower CTE and higher T_g at low cost • Improve high frequency performance of dielectrics with κ above 1000 • Requires high reliability, and better stability resistor materials • Ferromagnetics for sensor and MEMS applications

(*Continued*)

Petitioner Samsung Ex-1055, 0443

Table 8.3 Packaging Materials Challenges [1] (*Continued*)

Material Challenges	Issues
Environmentally friendly "green" materials Solder bump replacement	• Compliance with environmental regulations • Cost, reliability and performance must be compatible to that of conventional materials • Flexibility in joining to accommodate stress associated with CTE • Mismatch over the operating range
Die attach film	• Thin wafers suggest combination of dicing film and die attach film in a single film material • Materials are too thick and process convenience is not yet adequate • Embedded wiring in die attach film • Film that can be singulated by pulling for die that have been singulated with laser
Through silicon via materials challenges	• Low-cost via filling material and process (e.g., low-cost seeding and plating process) • Thin wafer handling carrier material and compatible attach material

CTE: Coefficient of thermal expansion; MEMS: Microelectromechanical systems; T_g: Glass transition temperature; UBM: Under bump metal.

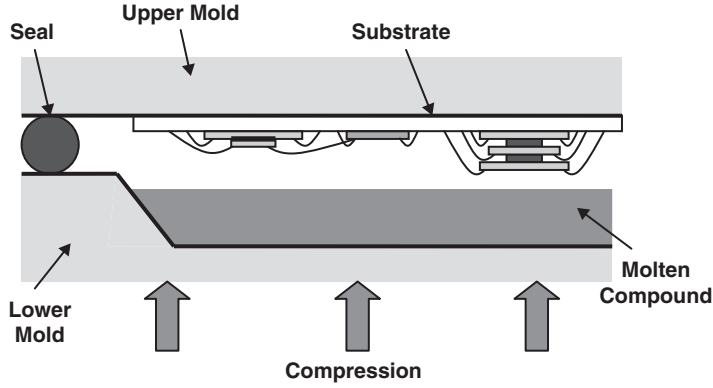


Figure 8.8 Flow Free Thin molding technique from Towa Corp. [11].

Apic Yamada Corp. (Nagano, Japan) has developed a liquid resin based molding machine using Cavity Direct Injection Molding (CDIM) technology. Figure 8.9 shows the CDIM process. The injection-compression type molding machine first injects a suitable amount of liquid resin on a

Petitioner Samsung Ex-1055, 0444

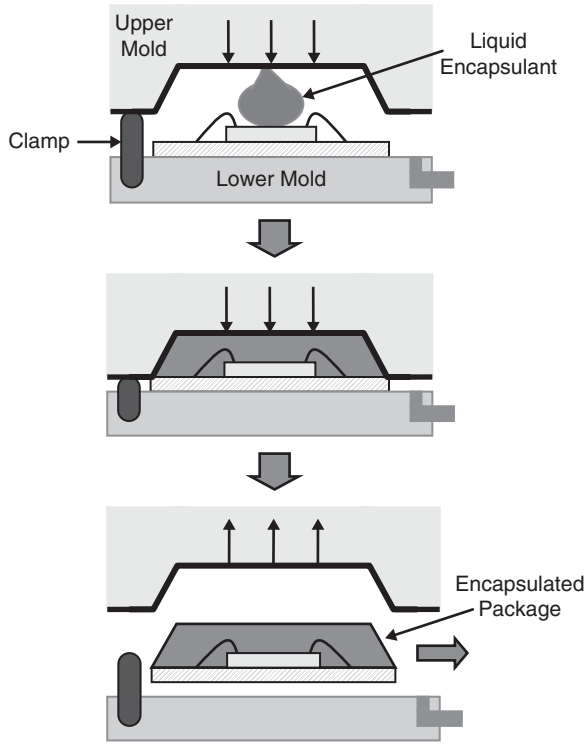


Figure 8.9 Cavity Direct Injection Molding technology from Apic Yamada Corp. [11].

board. The top mold then presses on the cavity of the chips, and the resin is solidified. The advantages of CDIM are

- low horizontal pressure during molding;
- effective for logic chips using mechanically fragile low-k materials;
- suitable for chips with multiple gold wires, leading to wire sweep reduction (i.e., less than 1% of the cases for 25 μm diameter wires).

The plastic encapsulant materials used in FFT and CDIM techniques must have optimum properties. Developing the optimum resin content is often a challenge, especially for the thinner IC packages that require easy-to-flow resins. Conventional plastic encapsulants generally include various materials such as basic epoxy material and additives such as filler (i.e., silica) and mold-release agents. The reduction in the filler volume leads to better resin flow onto the chip. However, lower filler content

Petitioner Samsung Ex-1055, 0445

reduces the coefficient of thermal expansion (CTE) leading to cracking and fracture. Plastic encapsulant manufacturers in collaboration with molding machine manufacturers have developed plastic encapsulant material with optimum flow and thermo-mechanical properties suitable for FFT and CDIM techniques.

8.2 Extreme High- and Low-Temperature Electronics

With recent advances in electronics materials and designs, the electronics industry is pushing the operating temperatures to new boundaries. Extreme high and low operating temperatures are being considered for electronics in applications such as automotive and space. In automotive applications, the goal is to push the operating temperatures higher, while in space applications, the aim is electronics operation in extreme cold temperatures of deep space. Electronics operating in extreme high and low temperatures will remove the need for heating and cooling units and the associated containment structures, and will lead to future cost savings.

8.2.1 High Temperatures

The automotive electronics per vehicle have increased over the years. This trend resulted from stricter government regulations on fuel economy and emission control which required the use of electronics [12]. Other factors such as lower cost and higher performance semiconductors have further driven this increasing trend. Automotive electronics are listed in Table 8.4.

The automotive electronics can experience wide variations in temperature depending on the specific location in the vehicle. With the advancement of semiconductors and packaging technologies, the automotive electronics industry aims to eventually place the engine electronic control units on the engine, and similarly, the transmission control units either on or in the transmission [12]. This means that the automotive control units will be exposed to ambient temperatures of 125°C or higher, which will place them in the category of high-temperature electronics according to the automotive electronics industry definition.

Table 8.5 shows the 2006 ITRS roadmap for maximum junction temperatures and operating ambient temperature extremes of semiconductors and complex ICs from 2007 ITRS [1]. The maximum junction temperature is expected to remain at 220°C through 2010s and 2020s for harsh environment

Petitioner Samsung Ex-1055, 0446

Table 8.4 Automotive Electronic Systems [12]

Category	Systems
Engine and power train	EFI (electronic fuel injection), ECU (engine control unit), TCU (transmission control unit), KCS (knock control system), cruise control, cooling fans
Chassis and safety	Active four-wheel steering, active control suspension, ABS (anti-lock brake system), TRC (traction control system), VSC (vehicle stability control), airbag system
Comfort and convenience	Preset steering wheel position, climate control, power seat, power windows, door lock control, mirror controls
Displays and audio	Radio (AM, FM, satellite), CD player, TV and DVD player, cellular phone, navigation system, instrument cluster
Signal Communications and wiring harness	Communications bus, starter, alternator, battery, diagnostic

Table 8.5 Roadmap for Maximum Junction Temperatures and Operating Ambient Temperature Extremes in Harsh Environments [1]

	Year			
	2009	2010	2016	2022
Maximum junction temperature (°C)				
Harsh	200	220	220	220
Harsh: complex ICs	175	175	175	175
Operating ambient temperature extremes (°C)				
Harsh	–40 to 175	–40 to 200	–40 to 200	–40 to 200
Harsh: complex ICs	–40 to 175	–40 to 150	–40 to 150	–40 to 150

applications, allowing for a 20 degrees lower (200°C) maximum operating ambient temperature.

The semiconductor technology must meet high temperature requirements for operation in harsh conditions. There are currently devices that are rated at 125°C (mostly for military and automotive applications) and few ICs rated at 150°C [12]. For operation at higher temperatures, derating to zero power is one feasible solution. Studies by Nelms et al. and Johnson et al. indicate that

Petitioner Samsung Ex-1055, 0447

power insulated-gate bipolar transistors and metal-oxide-semi-conductor field-effect transistors can operate at 200°C [13,14]. The limiting factor for high temperature operation is electronic packaging using plastic materials since most currently available plastic encapsulants will degrade on long-term exposure to these high temperatures.

Electronic packaging is the primary concern for high temperature electronics. Thermal cycling tests have shown that the current packaging trends such as BGA and QFN (quad-flat-no-leads) driven by computer and portable products must be re-evaluated to ensure reliability in harsh automotive environments [12]. A solution is to use underfills for BGAs and smaller I/O QFNs.

Another issue related to packaging is the glass transition temperature (T_g) of the encapsulant materials. Currently, T_g of common molding compounds and underfills is in the range of 150–200°C. Above T_g, the CTE increases 2–5 times, and thus poses significant reliability risk to the electronics. For operation in harsh automotive environments at 200°C and above, the T_g of the molding compounds and underfills must increase to above 220°C.

Higher level packaging currently used in automotive applications including molded plastic housing, silicone gel, and a cover must also be re-examined for high temperature operation. Silicone gels rated at 260°C are available; however, the material selection for the housing may be the limiting factor [12]. Plastic molding materials must meet T_g requirements at high temperature operation. With laminate-based surface-mount technology (SMT) and flip-chip packages, cast aluminum can be used. Due to the relatively high cost of hermetic packaging, the preferred choice for electronic housing material in harsh automotive applications is high temperature compatible plastic encapsulant materials.

8.2.2 Low Temperatures

Another trend is to push the electronics operating temperatures to extreme lows such as in deep space applications. Table 8.6 shows the typical operational temperatures for unheated spacecraft. Interplanetary probes launched to explore the planets in our solar system may experience extreme low ambient temperatures such as –183°C near Saturn and –222°C near Neptune.

Currently, the electronic units are maintained at approximately 20°C using on-board radioisotope heating units (RHUs) [15]. However, there are several issues with the use of RHUs including the need for active thermal

Petitioner Samsung Ex-1055, 0448

Table 8.6 Typical Operational Temperatures for Unheated Spacecraft [15]

Planet	Spacecraft Temperature (°C)
Mercury	175
Venus	55
Earth	6
Mars	–47
Jupiter	–151
Saturn	–183
Uranus	–209
Neptune	–222

control system, containment structures, and the additional cost. The use of low temperature electronics in spacecrafts will eliminate such problems. The incentive for using electronics capable of operating at extreme low temperatures extends beyond space applications and can be used in terrestrial applications including magnetic levitation transport systems, medical diagnostic, cryogenic instrumentation, and super conducting magnetic energy storage system [15].

Some of the semiconductor performance characteristics can actually improve with lower operating temperatures including reduced leakage current, reduced latch-up susceptibility, and higher speed [15]. At NASA Glenn Research Center (GRC) semiconductors are subjected to extreme low temperatures (i.e. –248C) and the performance characteristics are studied. Some of the ongoing activities at GRC include the evaluation of long term reliability of IC and power devices, and packaging for low temperature conditions.

Besides conventional silicon (Si) semiconductors, alternative types of semiconductors such as silicon-germanium (SiGe) devices are also being evaluated for low temperature electronics. SiGe devices show high gain in contrast to conventional Si bipolar junction transistor which exhibit gain loss with lower temperatures [16].

8.3 Emerging Technologies

Plastic packaging and encapsulation are influenced by emerging technologies such as MEMS, bio-chips, bio-MEMS, nanotechnology, nanoelectronics, OLEDs, photovoltaics, and optoelectronics. The requirement

Petitioner Samsung Ex-1055, 0449

and needs specific to each technology and device have resulted in innovations in plastic packaging techniques and materials. For some technologies such as MEMS devices that are traditionally packaged hermetically, plastic encapsulation is relatively a recent progress. Generally, lower cost has driven various emerging and maturing technologies towards plastic packaging. Polymers are also biocompatible, thus offering additional advantage for bio-MEMS and bioelectronics encapsulation.

8.3.1 Microelectromechanical Systems

MEMS are devices that integrate micro-sized mechanical and electronic components to sense, process, or actuate in an environment. Optoelectronic components can also be added to MEMS, referred to as micro-optoelectromechanical systems. MEMS devices are often fabricated using the same fabrication technology as the silicon IC industry. MEMS devices have found application in automotive, aerospace, biomedical, telecommunications, and military. MEMS sensors can sense and measure flow, pressure, acceleration, temperature, blood, etc., often at much lower cost compared to the conventional large measurement equipments.

Although MEMS devices have been available for the past several decades, the packaging—plastic encapsulation—is still an active area of research and development. MEMS are traditionally packaged hermetically because of the sensitivity of various parts of MEMS devices to moisture [17–19]. Hermetic packages such as ceramic packages are relatively expensive. Recent innovations in plastic packaging processes and materials combined with higher moisture resistance of MEMS elements have made it possible for the lower cost alternative plastic encapsulation of MEMS to replace traditional ceramic packaging.

An example of a MEMS plastic packaging process from Sandia is shown in Fig. 8.10 [20]. The MEMS device is encapsulated in a plastic small-outline integrated circuit (SOIC) package. After encapsulation, the plastic portion above the functional MEMS surface is etched or decapsulated as shown in the figure. The etching solution can be fuming nitric acid, fuming sulfuric acid, or a combination of the two. An external gasket is used to confine the spray of acid.

Upon the exposure of the sacrificial layer, a second etching process takes place using a different solution such as hydrochloric acid or hydrofluoric acid, confined by an internal gasket. The sacrificial layer is removed and the functional elements of MEMS device are exposed. This second etching step is also called a “release” step where the MEMS elements are

Petitioner Samsung Ex-1055, 0450

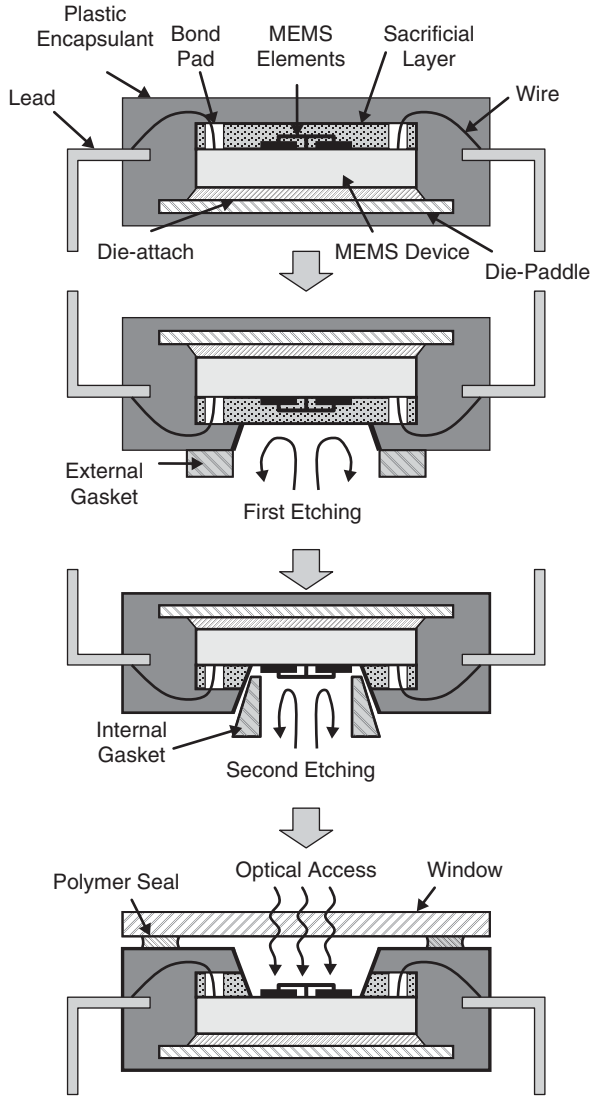


Figure 8.10 Plastic encapsulation of a MEMS device and selective decapsulation for sensor exposure, from Sandia [20].

released and are free to move, rotate, tilt, etc. After wet etching, the MEMS elements can be dried to reduce stiction (static friction). MEMS elements can also be released by dry etching such as plasma process. Optional coating can be applied to the mechanical elements to improve performance and life. Finally, a window cover is attached to the plastic package with a polymeric

Petitioner Samsung Ex-1055, 0451

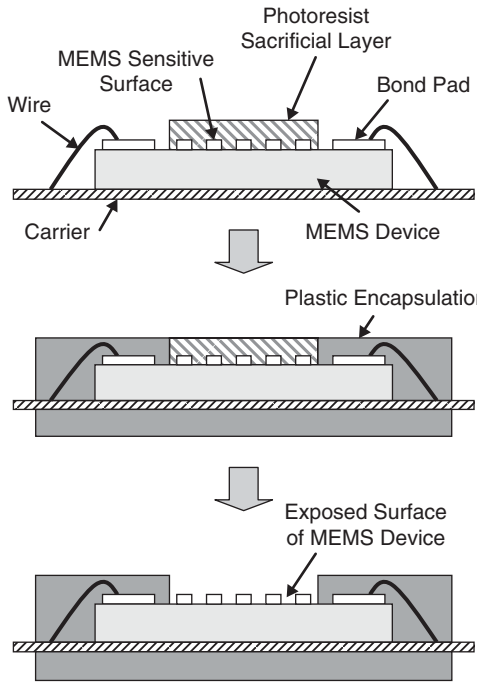


Figure 8.11 Selective plastic encapsulation of a MEMS device using sacrificial layer, from Industrial Technology Research Institute [21].

seal to provide optical access to the MEMS device. The final package is a plastic-encapsulated SOIC with a cavity and a window cover.

Figure 8.11 shows a selective plastic encapsulation process for a MEMS device from Industrial Technology Research Institute [21]. A photoresist sacrificial layer is applied to the sensitive surface of the MEMS device. The assembly is then encapsulated with plastic material. The sacrificial layer is removed exposing the sensitive area of the device. The selective encapsulation process can be applied to various types of MEMS devices. Figure 8.12(a) shows another example of selective encapsulation of a MEMS suspension sensor chip that includes a cavity constructed on the back surface. Figure 8.12(b) shows selective plastic encapsulation of a MEMS device stacked on an IC chip.

Figure 8.13 shows a selective encapsulation method for a MEMS pressure sensor from Motorola [22]. A protective dam is constructed on the outer perimeter of the pressure sensor diaphragm, thus forming a cavity between the dam and the package housing. The cavity can be filled with plastic encapsulant material. The package housing is also made of plastic material.

Petitioner Samsung Ex-1055, 0452

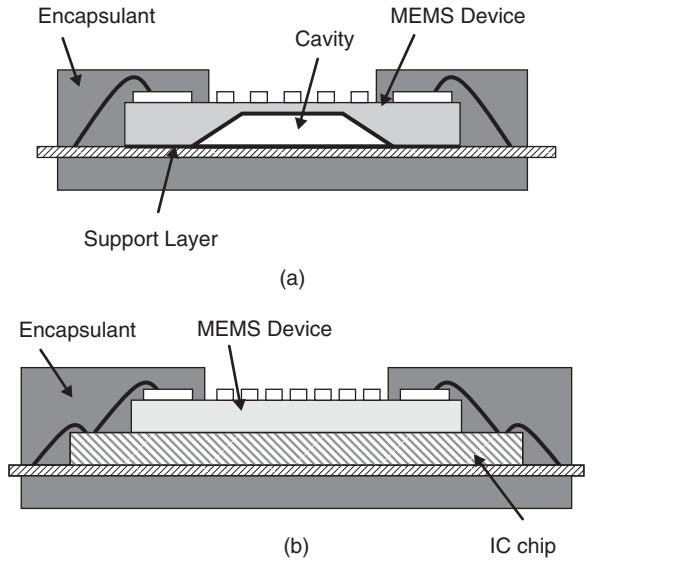


Figure 8.12 Plastic-encapsulated MEMS device package designs from Industrial Technology Research Institute: (a) MEMS device with a cavity; (b) 3D package with a MEMS device stacked on an IC chip [21].

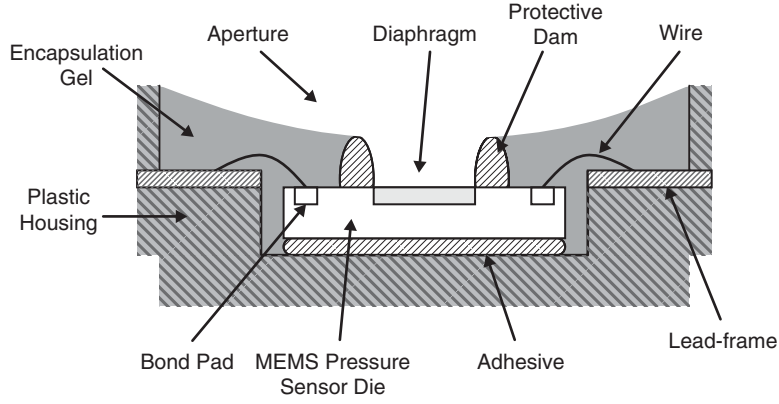


Figure 8.13 Plastic-encapsulated MEMS pressure sensor device from Motorola [22].

MEMS inertial devices are traditionally secured in ceramic packages which are hermetic, but relatively expensive. Lower cost incentives have led MEMS manufacturers to consider plastic packaging for inertial sensors. Inertial sensors including accelerometers and gyroscopes can be packaged with transfer molded packages or pre-molded packages. Since plastic

Petitioner Samsung Ex-1055, 0453

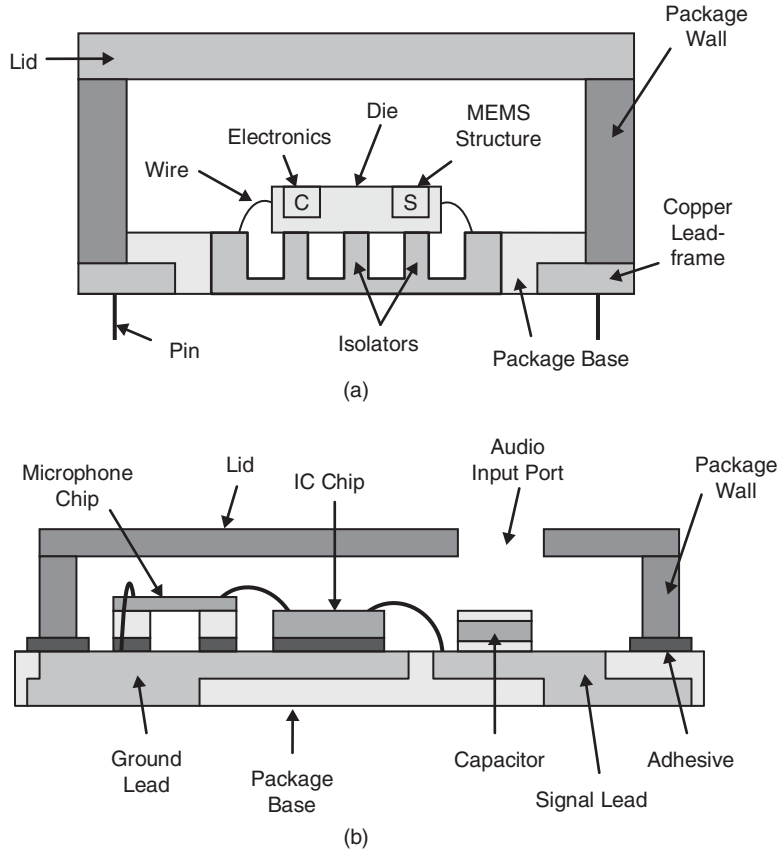


Figure 8.14 Plastic pre-molded package used for (a) MEMS inertial sensor [23] and (b) MEMS microphone [24] from Analog Devices.

packages are non-hermetic, additional processing may be required to ensure that moisture does not affect the sensor chip [23]. An example of a plastic pre-molded package used for an inertial sensor from Analog Devices is shown in Fig. 8.14 (a) [23]. Pre-molded packaging is also used for Si microphones as shown in Fig. 8.14 (b) [24].

Electronic packaging protects the IC from the external environment allowing only electrical signals to penetrate the package [25]. However, in order for MEMS to sense and actuate, interaction with more complex signals such as fluids may be required [26]. Such signals have the potential of contaminating the device if it is not protected properly, leading to a reduction in reliability. Common challenges in MEMS packaging include moisture resistance, low-cost packaging, electrical interconnection,

Petitioner Samsung Ex-1055, 0454

particle control, stiction (static friction) control, maintenance, and singulation [27].

Several plastic packaging options are available for MEMS devices. Table 8.7 shows various packaging options from Amkor Technology suitable for specific types of MEMS devices. For example, an accelerometer can be packaged in pre-molded package, or molded MicroLeadFrame® (MLF®) package. MLF® package is similar to a plastic-encapsulated CSP with copper lead-frame substrate. MLF is lead-less, and it is electrically connected to the printed circuit board through the soldered lands on the bottom surface of the package (Amkor Technology, www.amkor.com/enablingtechnologies/MEMS/index.cfm).

Challenges and requirements for MEMS packaging are listed in Table 8.8. Wafer-level packaging methods are the trends for MEMS packaging [17]. Wafer-level packaging is of interest because it solves the problems of particle contamination from manufacturing process, singulation, and degradation due to environmental contact [25].

8.3.2 Bioelectronics, Biosensors, and Bio-MEMS

Bioelectronics, biosensors, and bio-MEMS are a category of electronic devices that are specifically designed for medical or biological applications. They can be further divided into two groups: those that operate in biological environments and those that integrate biological materials as functional components of the device [28].

An important requirement for bio-devices is biocompatibility. The materials that are in contact with the biological matter must be compatible to prevent unintended effects on the biological substances. For instance, bio-electronics implanted in human body if not encapsulated with biocompatible materials can create harmful effects to the patient. The use of non-biocompatible materials could also interfere with the biological substances in a biosensor and adversely affect the sensor's performance [28]. Figure 8.15(a) and (b) shows the electrode and amplifier assembly for a microminiaturized brain implantable neuroprobe device prior to and after silicone encapsulation, respectively. Figure 8.16 shows a packaged optoelectronic biochip with a case of black epoxy potting material.

In the case of bio-MEMS that contain biological subcomponents, not only must the materials be biocompatible, but the assembly and packaging of such devices must also use biocompatible technologies. Conventional packaging processes and conditions such as high temperatures during thermo-compression wire bonding, thermosonic wire bonding or other

Petitioner Samsung Ex-1055, 0455

Table 8.7 MEMS Packaging Options from Amkor Technology

MEMS Typex	Package Type						
	Ceramic	MLF-C/ Pre-molded LF + Lid	BGA/LGA	SOIC/Cavity SOIC	Molded MLF®	SiP	Module/ μEMs
Pressure sensor			X	X		X	
Accelerometer		X			X		
Gyroscope	X	X		X			
Projector	X		X				X
Micro display	X						X
Si microphone		X				X	
Inkjet printer head							X
RF MEMS						X	
Electronic compass			X		X		
Solar energy							X

BGA: Ball-grid array; LGA: Land grid array; MEMS: Microelectromechanical systems; MLF®: MicroLeadFrame®; RF: Radio-frequency; SiP: System-in-package; SOIC: Small-outline integrated circuit. Source: Amkor Technology, www.amkor.com/enablingtechnologies/MEMS/index.cfm.

Petitioner Samsung Ex-1055, 0456

Table 8.8 ITRS Requirements and Challenges for MEMS Packaging [1]

MEMS Packaging	RF MEMS	Bio-MEMS	Inertial MEMS	Optical MEMS
Requirements	*Electrical* • Low insertion loss • Low back reflection • Low contact resistance frequency • Signal isolation • Package resonance • Low parasitics *Structural* • Low stress • Small form factor *Package* • Wafer-level package • Small form factor • Hermeticity • Low loss packaging material • Light weight	*Fluidic* • Low dead volume • Detection sensitivity • Low back pressure • Fluidic channel size • Flow rate • Heating/cooling rate *Electrical* • Interface with electronic circuits *Thermal* • Fast heating and cooling *Optical* • Low optical loss *Structural* • Low stress at fluidic joints *Package* • Modular package • Disposable	*Structural* • Low stress • Meet reliability requirements *Thermal* • Temperature stabilization *Electrical* • Sensitivity • Switching time • Frequency • Q factor *Package* • Plastic package • Wafer-level package	*Optical* • Low coupling loss • Mirror rotation/ angle *Structural* • Low stress package • Low shrinkage of UV epoxy • Low warpage *Thermal* • Thermal stabilization *Electrical* • Switching speed and time *Package* • Ceramic package • Metal package

Petitioner Samsung Ex-1055, 0457

Challenges	• Optimization of electrical and structural parameters • Low cost materials to reduce insertion loss • Form factor reduction • Passive device integration	• Co-design of fluidic, electrical, thermal, optical, and structural • Dead vacuum reduction • Channel size reduction • Zero back pressure • Flow in nano channels • Bubble elimination • Bio-compatibility of material	• Structural design • Reliability of package • Vacuum/hermeticity • Low cost • Small form factor • Integration into other systems	• Optical, structural design to meet low coupling loss/ reliability • Low cost • Integration into other systems
Potential directions	• RF system in package • Bio-RF integration	• 3D microfluidic package • Bio system in package • Plastic-based fluidic systems	• MEMS system-in-package for various applications: mobile, bio, information technology	• Wafer-level packaging

Petitioner Samsung Ex-1055, 0458

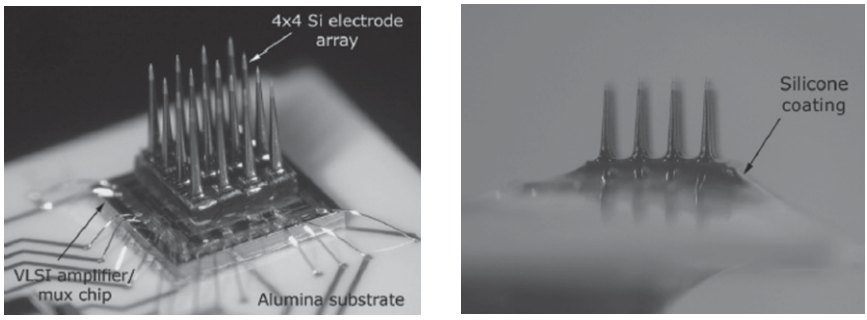


Figure 8.15 Electrode and amplifier assembly for a microminiaturized brain implantable "neuroprobe" device (a) prior to and (b) after silicone encapsulation (© 2005 IEEE) [29].

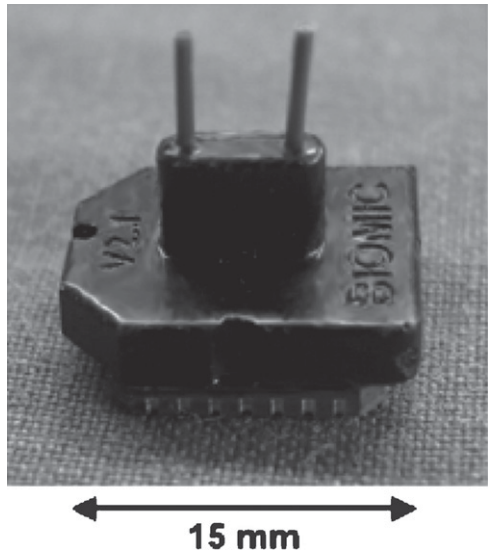


Figure 8.16 A packaged optoelectronic biochip BIOMIC with a case of black epoxy potting material; the tubings are the fluid inlet and outlet, respectively (© 2005 IEEE) [28].

thermal bonding processes can denature the bio-affinity layers on biosensor chips. Therefore, new or alternative packaging and assembly methods and materials are necessary for biosensors and bio-MEMS applications [28,30].

For instance, in the case of polymeric microfluidic bio-devices which evaluate the fluidic behavior of various biomolecules such as proteins,

Petitioner Samsung Ex-1055, 0459

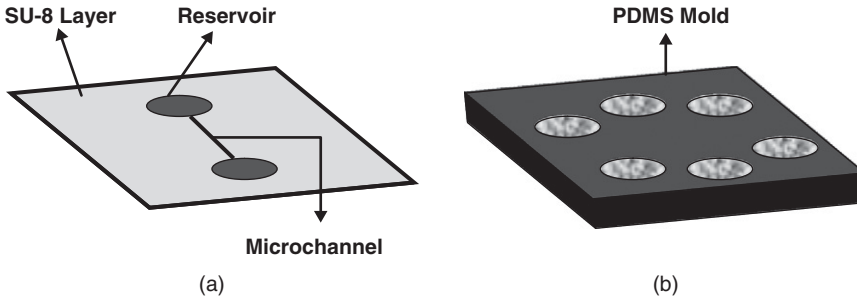


Figure 8.17 Schematics of polymeric microfluidic devices: (a) SU-8 microchannel; (b) polydimethylsiloxane (PDMS) on SU-8 pegs [31].

cells, and DNA, alternative packaging materials and techniques are being investigated. The micro-channels can be fabricated in EPON SU-8 (an epoxy-based negative photoresist), polypyrrole (PPy) can be used as a biocompatible conducting material for the electrodes, and the micro-channels can be encapsulated with polydimethylsiloxane (PDMS), a biocompatible transparent elastomer (Fig. 8.17). The biocompatibility of PPy with SU-8 and PDMS allows easier fabrication of polymeric microfluidic devices for biological applications [31].

Figures 8.18 and 8.19 show two methods for plastic encapsulation of ion-selective field effect transistor (ISFET) biosensors. ISFET biosensors are used to detect temperature and pH values of liquid solutions such as human serum. In the method depicted in Fig. 8.18, the photo-imageable protective material covers the sensing area and the perimeter. Upon removal of the central portion, the protective layer is formed into dam protecting the sensing area during encapsulation. In the method depicted in Fig. 8.19, the photo-imageable material protects the sensing area directly. The assembly is encapsulated, and then the protective material is removed.

8.3.3 Nanotechnology and Nanoelectronics

Nanotechnology is one of the emerging technologies that may be changing the face of the modern world. Futurists and visionaries such as Eric Dexler and Ray Kurzweil have predicted electronics that will be built molecule by molecule or bottom-up [32]. By the definition of nanotechnology where functional element size is below 100 nm, we are already in the nano-electronics era with 90, 65, and 45 nm DRAMs in production and use. The focus of nanotechnology, however, is more on those technologies

Petitioner Samsung Ex-1055, 0460

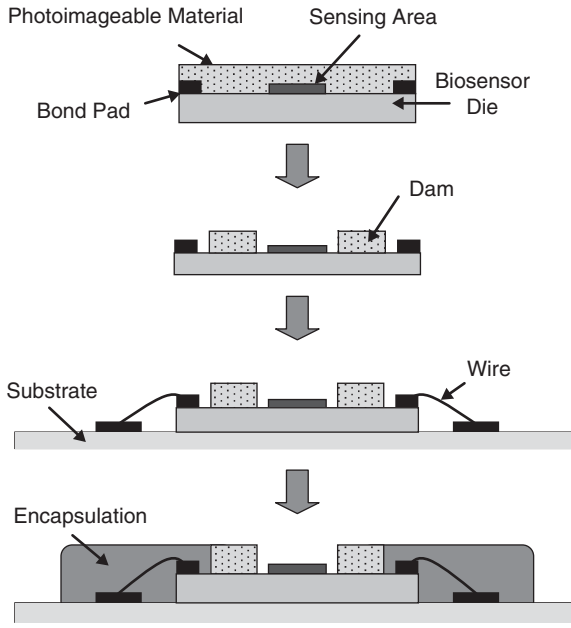


Figure 8.18 Biosensor packaging process using the protective dam method [33].

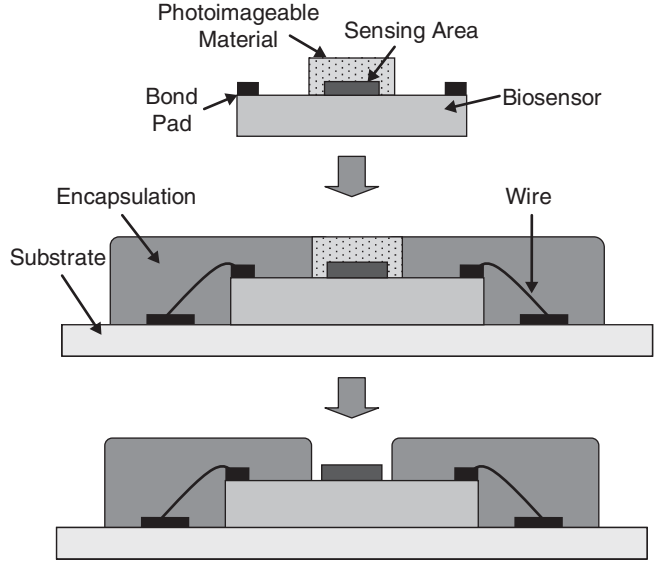


Figure. 8.19 Biosensor packaging process using the sensor area sacrificial layer method [33].

Petitioner Samsung Ex-1055, 0461

where the nano-size dimension is the enabling factor for the improved electronic characteristics.

One of the discoveries related to nanotechnology is carbon nanotube (CNT). CNTs have potential use in electronic device structures and packaging applications. They can be used for IC chip cooling due their high thermal conductivity. Added to solder, they can improve the tensile strength of the material. CNTs are also considered for improving electrical contact specifically by opening the CNT ends after growth, allowing for better wetting by solder [34].

An important application of nanotechnology relevant to plastic encapsulation of electronic devices is the use of nano-sized fillers. Nano-particles can be added as fillers to improve the properties of the encapsulant material. Many studies have investigated nano-filled encapsulants [35–41]. Three main types of nano-particle fillers explored include bentonites, nano-sized silica particles, and zeolites as shown in Fig. 8.20.

Bentonite is an aluminum phyllosilicate clay that consists mostly of montmorillonite. The substance montmorillonite (named after the location of occurrence at Montmorillon, France) is a hydrated sodium calcium aluminum magnesium silicate hydroxide with the chemical formula

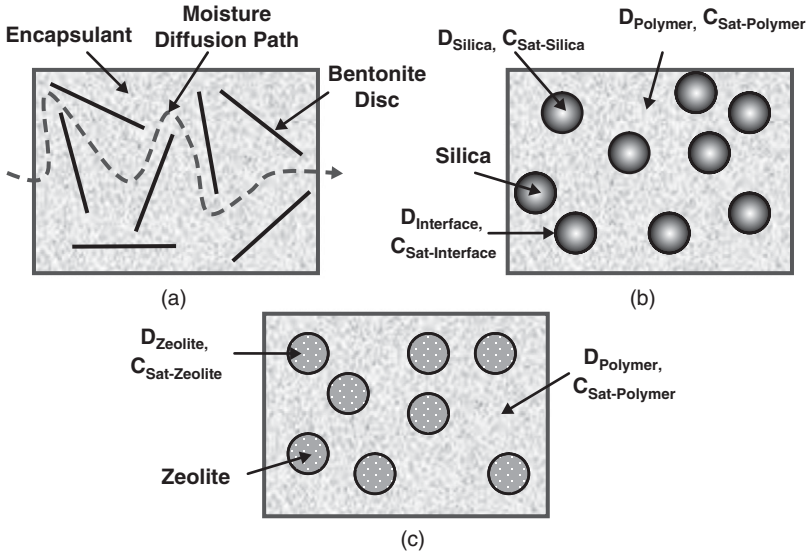


Figure 8.20 Nano-fillers explored for improving encapsulant properties: (a) bentonites, (b) silica particles, and (c) zeolites [41].

Petitioner Samsung Ex-1055, 0462

$(Na,Ca)_{0.33}(Al,Mg)_2(Si_4O_{10})(OH)_2 \cdot nH2O$. The separated bentonite discs have thickness of about 1 nm with a diameter of 200–300 nm. It is proposed that the bentonite discs can elongate the moisture diffusion path in the encapsulant material as depicted in Fig. 8.20(a) [41].

Nano-sized silica particles have a much higher surface to volume ratio as compared to micro-sized silica particles. Assuming that the surface of the particles influence the diffusion properties of the encapsulant material, then less amount of nano-silica particles are required relative to micro-sized particles to produce the same effect on the encapsulant diffusion characteristics. Figure 8.20(b) shows various diffusion coefficients (D) and saturation moisture content (C_{Sat}) influencing the overall moisture diffusion behavior.

Other nano-sized particles considered as fillers are zeolites which are hydrated aluminosilicate minerals. Zeolites have a micro-porous structure as shown in Fig. 8.20(c). Due to their regular pore structure, zeolites can catch water molecules, but not interfere with polymer chains, and therefore, hinder the moisture diffusion process [41].

The T_g of encapsulant material is one of the bottlenecks in future electronic packaging. With Pb-free high assembly temperatures and the increasing demand for high temperature electronics, there is a need for higher T_g encapsulant materials. The effect of nano-size fillers on T_g of the encapsulant materials has been investigated [38,39].

Researchers at General Electric have developed a composite encapsulant material with organo-functionalized colloidal silica nano-particles that exhibit exceptionally high T_g [38]. The size of nano-particles in this composite material is in the range of 2–20 nm.

Another study at Georgia Tech [39] found that the addition of nano-sized particles resulted in the decrease in T_g of the encapsulant material. The size of the nano-silica fillers was 100 nm, and a group of nano-fillers were surface treated with silane coupling agents. Both groups of treated and untreated nano-silica filled encapsulants showed decrease in T_g. The untreated nano-filled encapsulant showed slightly greater reduction in T_g of about 40°C reduction at 40% filler loading. Factors such as nano-filler size, surface treatment material and processing [39,40] can strongly influence the direction and degree of change in T_g of the encapsulant material.

Underfill materials that have embedded nano-size silica particles offer advantages such as resistance to settling, less scattering of light leading to improved UV optical curing, and higher thermal conductivity [34]. Furthermore, nano-particles added to no-flow underfill (NFU) materials can lower CTE and increase T_g of the material. Conventionally, NFU materials are

Petitioner Samsung Ex-1055, 0463

not filled, because the presence of fillers interferes with the solder joint formation. NFU materials, therefore, have generally higher CTE and lower T_g due to the absence of fillers.

Novel nano-silica filled NFU materials developed by General Electric has shown to exhibit lower CTE, improved fluxing properties, transparency and suitable curing kinetics necessary for good quality solder joint formation [35]. The size of the nano-particles used ranged from 5 to 100 nm, but 20 nm particles appeared to provide the optimum balance of material properties. These nano-filled underfill materials have also been considered for wafer-level underfill (WLU) [36]. Advantages of WLU are the lower cost, process time, and improved throughput. Nano-filled WLU materials can be applied to the entire wafer, after which solder bumps are exposed, wafers are diced, and finally, the single die is assembled.

A disadvantage of nano-materials, in particular, nano clays such as montmorillonite minerals is their tendency to agglomerate upon mixing into liquid. Effective dispersing and deagglomeration are often required when the nano-particle powder is wetted. Various methods and devices are available for deagglomeration including ultrasound, rotor stator mixer, piston homogenizers, and gear pumps, among which ultrasound have been found to be more effective [41].

8.3.4 Organic Light-Emitting Diodes, Photovoltaics, and Optoelectronics

The market for OLEDs used in displays and lighting applications is close to a billion mark and will continue to grow in billions in the next decade [42]. The polymer materials used in OLED devices are very sensitive to moisture and oxygen and even the slightest contact can lead to optical performance degradation. OLED packages must therefore provide sufficient protection from moisture and oxygen. The conventional packaging for glass substrate OLEDs is sealing the device using glass lid (or metallic can) with an UV-cured epoxy resin as shown in Fig. 8.21(a) [43,44]. A desiccant film is usually placed inside the package to ensure dry interior environment.

As the OLED devices evolve, for example, become flexible, the packaging must also change to meet new device and application requirements. Flexible OLEDs can be used in applications such as roll-up displays and displays embedded in fabrics or clothing. The conventional rigid packaging used for standard glass based OLEDs are no longer

Petitioner Samsung Ex-1055, 0464

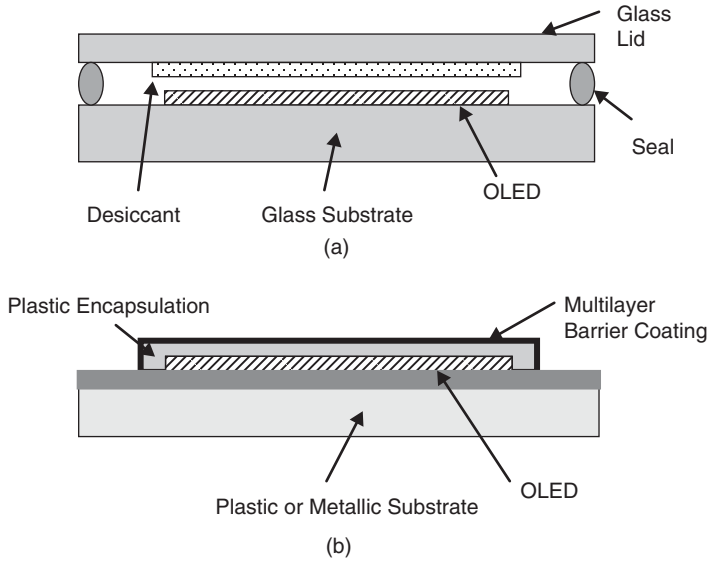


Figure 8.21 OLED packaging: (a) conventional glass-to-glass packaging; (b) plastic encapsulation with barrier coating [44].

suitable for flexible OLEDs. Plastic encapsulant materials can offer flexibility, but they are moisture and oxygen permeable.

To provide protection from moisture and oxygen and not compromise package flexibility, a thin multilayer barrier coating is applied to the external surfaces of the plastic encapsulant. An example of a plastic-encapsulated flexible OLED package from Universal Display is shown in Fig. 8.21 (b) [44]. Instead of conventional glass substrate, a plastic or metallic substrate is used. This offers device flexibility, where it can conform, bend, and flex to any surface.

Barrier coatings applied to polymer encapsulants have been extensively investigated in the past and used in food and pharmaceutical packaging. However, barrier coating for OLEDs must have several orders of magnitude more resistance to moisture and oxygen, hence sometimes referred to as "ultra" or "super" barriers.

Multilayer barrier coating used in OLED packaging generally consists of combinations of organic and inorganic dielectric layers. The presence of multiple layers can cause a permeation lag time [45] that can reduce water and oxygen permeability to more than three orders of magnitude lower compared to a single inorganic layer [46–48]. The inorganic layer of the multilayer barrier coating is commonly made of aluminum oxide deposited using plasma-enhanced chemical vapor

Petitioner Samsung Ex-1055, 0465

deposition, sputtering, or atomic layer deposition [49] on an organic layer such as polyethersulfone.

A problem with fabricating thin oxide barrier films onto plastic substrates is the presence of defects such as pinholes, cracks, and grain boundaries. These defects and pores can allow oxygen and water molecules to penetrate through the barrier coating. Using alternate organic and inorganic multi-layers coated on plastic can reduce the effect of these defects. The multiple layers can stagger the defects in adjacent layers and create a longer pathway for water and oxygen molecules, making it more difficult to travel through the plastic.

Institute of Materials Research and Engineering (IMRE) in Singapore, has developed a barrier coating that is 1000 times more effective in moisture protection [50]. The IMRE nano-engineered coating contains nanoparticles small enough to plug the pores in the coating and thus hinder moisture penetration. The result is a water transmission rate of 10^{-6} g/m^2/day which is 1000 times lower than that of conventional multilayer barriers. Consequently, the number of layers required is reduced to only two including a barrier oxide layer and a nano-particulate sealing layer. The nano-particles used in the barrier coating not only seal the defects but also can react with moisture and oxygen molecules and slow their permeation.

The conventional inorganic LED die can also be encapsulated with a polymeric optical material for protection and adjustment of the emitted spectrum. To produce white light from a blue emitting LED device, white emitting phosphor is added to a transparent encapsulation material. The white emitting particles are excited by the blue LED leading to the generation of white light.

Figure 8.22 shows the plastic encapsulation of LED arrays from General Electric [51]. The encapsulating material can be epoxy, glass filled epoxy or silicone. The encapsulant may also contain phosphor particles to convert the wavelength of the original light, for example, from blue to white. For improvement in optical efficiency, LEDs are sometimes constructed in the shape of an inverted pyramid as shown in Fig. 8.23, which may require specific packaging and assembly considerations [1].

Photovoltaic solar cells are another type of optoelectronics that have received enormous attention in recent years due to the global initiative for renewable energy. In fact, the solar photovoltaic sector is the fastest growing renewable energy source in the world after wind power [52]. Although, photovoltaic solar cells have been under research and development for the past several decades, only recently they have surpassed higher efficiency and lifetime thresholds. Solar cell modules have been

Petitioner Samsung Ex-1055, 0466

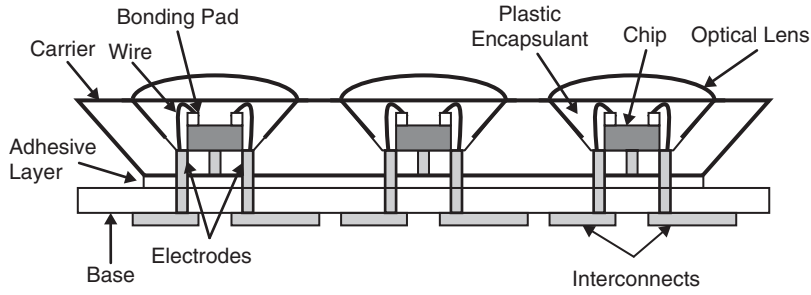


Figure 8.22 Plastic encapsulation of LED arrays from General Electric [51].

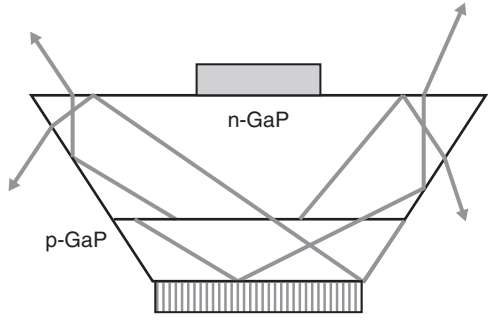


Figure 8.23 Inverted pyramid LED [1].

reported to achieve 30% or more efficiency and a guaranteed lifetime of 20–30 years or more.

Similar to OLEDs, solar cells are very sensitive to moisture and oxygen. A solar cell package can allow only very low water vapor and oxygen transmission rate that is generally not available in commercial plastic materials. Therefore, conventional rigid solar cell packages that are encapsulated in plastic material are protected from the environment with glass top and bottom layers as shown in Fig. 8.24.

The encapsulation material commonly used for solar module packaging is ethylene-vinyl acetate (EVA). Other alternative materials considered for solar cell encapsulation are cast acrylic resins, thermoplastic polyurethane, polyvinylbutyral [52,53], and non-crystalline or low-crystalline α-olefin-based copolymer [54].

EVA copolymer encapsulants commonly used in solar cell packaging are flexible and transparent, but provide inadequate heat resistance. The addition of organic peroxide to EVA is necessary for improving heat

Petitioner Samsung Ex-1055, 0467

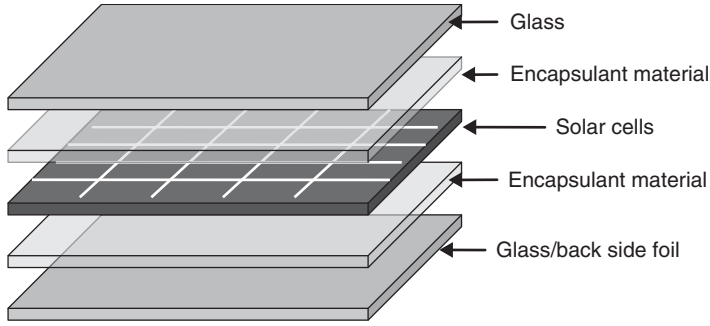


Figure 8.24 Solar cell package or module [52].

resistance. A two-step process is used where an encapsulant sheet made of EVA and organic peroxide is first prepared and then the solar cell is sealed in the sheet. Using an alternative encapsulant such as non-crystalline or low-crystalline α-olefin-based copolymer can significantly reduce the encapsulation processing time and manufacturing cost for solar cell modules [54].

Flexible solar cells, similar to flexible OLEDs must be packaged in non-rigid materials which eliminates the conventionally used glass layers. Instead, a thin barrier coating must be applied similar to that used in flexible OLED packaging. Barrier coatings can be constructed with alternative coating layers based on polyacrylate/Al_2O_3 [55]. Developments in barrier coatings such as nano-engineered IMRE bi-layer coatings [50] are also applicable to flexible solar cell modules and can lead to significant improvements in moisture protection of solar cells.

8.4 Summary

This chapter presented the trends and challenges for microelectronic devices, packaging, and plastic encapsulants. Electronics are becoming smaller, thinner, and lighter. The miniaturization trend in transistors will continue to follow Moore's law decreasing to 32 nm and lower sizes, reaching beyond complementary metal-oxide semiconductor devices. Another trend referred to as More-than-Moore is also occurring where the functional diversification of components in the package is increasing including IC chips, MEMS, biochips, sensors, passives, etc. A third trend of system integration and packaging innovations is also in effect which combined with smaller and more diversified components can lead to higher value systems such as SiP and SoP.

Petitioner Samsung Ex-1055, 0468

The packaging and encapsulation must meet such trends. Modified compression molding techniques have emerged that can lower molding pressures to a fraction of conventional transfer-molding systems and are highly suitable for thinner and more complex SiP, PoP, wafer-level packaging, and transparent resin packaging.

With recent advances in electronics materials and designs, the electronics industry has been stretching the boundaries in operating temperatures to extreme high and low in applications such as automotive and space. Electronics designed to operate in extreme high and low temperatures will not require heating or cooling units and the associated containment structures, and thus can reduce cost.

Plastic encapsulation trends and challenges related to emerging technologies such as MEMS, bio-sensors, bioelectronics, nano-electronics, OLEDs, and photovolatics were discussed. Recent innovations in plastic packaging processes and materials combined with higher moisture resistance of MEMS elements have made it possible for plastic encapsulation of MEMS to gradually replace traditional ceramic packaging. Plastic encapsulation of MEMS may include a decapsulation phase where a plastic portion above the functional MEMS surface is etched or decapsulated. Sacrificial photoresist layers are also used to protect the region of MEMS sensor and after encapsulation can be removed. MEMS devices have also been encapsulated in a pre-molded plastic package.

Packaging of bioelectronics, biosensors, and bio-MEMS specifically designed for medical or biological applications have also been discussed. An important requirement for bio-device packaging is biocompatibility. The materials that are in contact with the biological matter must be compatible to prevent unintended effects such as harming the patient or interference with the sensor's performance. Furthermore, the assembly and packaging of such devices must also use biocompatible technologies.

An important application of nanotechnology to plastic encapsulation of electronic devices is the addition of nano-sized fillers to improve the properties of the encapsulant. Three main types of nano-particle fillers explored include bentonites, nano-sized silica particles, and zeolites. Properties to be improved by nano-particles include higher moisture resistance, higher T_g, ease-flow or no-flow encapsulant characteristics.

The conventional rigid packaging used for optoelectronics such as standard glass based OLEDs and solar cells have been replaced by plastic packaging in case of flexible OLEDs and flexible solar cell modules. Because of moisture and oxygen permeability of plastic encapsulants, a thin multilayer barrier coating is applied to the external surfaces of the encapsulant. Recent advanced in nano-engineered barrier coating consist

Petitioner Samsung Ex-1055, 0469

of nano-particles plugged into nano-sized pores and defects in the coating, leading to 1000 times more moisture resistance.

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Petitioner Samsung Ex-1055, 0473

Index

Accelerated testing, 378–382
  failure mechanisms, 380
  steps, 380
Acceleration factor (AF), 360, 376–377, 378
Accelerators, 66
Acoustic impedance, 305–306
Acoustic impedance polarity detection (AIPD), 307, 307
Acrylonitrile-butadiene rubbers, 75
Addition, 48
Addition cure, 95
Additives, 47
Adhesion strength
  button shear test, 201
  180°C peel test, 203
  modified die shear test, 202
  tab pull test, 202
Adhesive, 6–8, 11, 30, 35, 75, 80, 91, 164, 254, 255, 267, 273, 275
Adhesive strength, 254, 255
Advisory Group on Reliability of Electronic Equipment (AGREE), 352
Aliphatic epoxies, 50
Aliphatic tertiary amines, 65
Alpha emission rates (AERs), 73, 74
Alumina, 4, 68–69, 95
Aluminum chelates, 73
Aluminum nitride, 68, 88
Amplifiers, 90, 440, 444
Angular fillers, 70, 72
Anhydrides, 51, 59–60
Antimony pentoxide, 77
Antimony trioxide (ATO), 76, 77, 102, 104, 108, 391
  hazardous effects, 102–103
  toxicity, 104
Aperture-plate molds, 133, 134, 138
Application requirements, 367
Aromatic/aliphatic polyurethane, 53, 55
Aromatic amines, 60, 61, 62, 65
A-scan, 302, 304, 306
ASTM C177 guarded hot-plate method, 196
ASTM D256A/D256B test, 199
ASTM D638/D2990 test methods, 198
ASTM D2240 durometer hardness method, 188
ASTM D2863 oxygen index test, 218, 219
ASTM D696/SEMI G13-82, 190
ASTM D3123/SEMI G11-88 test, 181
ASTM D790-71 test, 200
ASTM D1434 test, 212
ASTM E595-93 test, 212
Atmospheric-pressure plasma (APP), 173
Atmospheric-pressure plasma jet (APPJ), 173–174
Atomic force microscopy (AFM), 288, 298, 342, 343
Auger electron spectroscopy (AES), 335
Auger pumps with RPDV, 150
Autoclave test, 386–387
  galvanic corrosion, 387
Automated acid decapsulation, 293, 295
Automotive electronics, 431, 432

Bakelite, 54
Baking, 260, 271
Ball bond corrosion, 229
Ball-grid array (BGA), 14, 98, 157

Petitioner Samsung Ex-1055, 0474

Bathtub curve, 353
Bentonite, 447–448.
See also Montmorillonite
Benzene ring, 50
Biochip, packaged optoelectronic, 444
Biocompatibility, 440, 445, 454
Bio-devices
biocompatibility of, 440
electrode/amplifier assembly, 444
polymeric microfluidic devices, 445
Bioelectronics, 440–445
Bioelectronics, biosensors, and bio-MEMS
biosensor packaging process, 446
electrode and amplifier assembly, 444
packaged optoelectronic biochip, 444
polymeric microfluidic devices, 445
Bio-MEMS, 440
Biosensors
plastic encapsulation of ISFET, 446
Biphenyl epoxy resins, 59
Bisphenol A (bis A), 49
Black's model, 369
Bleed, 184
Bond finger clearance, 240
Bonding pads, 8, 11, 159, 170, 231, 235, 260, 273, 387–388
Bond liftoff, 140, 227
Bond-pad cratering, 227
Bound water molecules, 206, 209
Breakdown voltage, 216, 235
Bright-field, 340–341
Brittle fracture, 262–265, 262–265
measuring critical stress intensity factor, 264, 265
modeling Mode I crack, 263
Brominated biphenyl oxide flame retardants
restricting use of, 105
Brominated DGEBA, 76
Brominated dioxins
toxic responses, 105
Brominated flame retardants (BFR), 76, 102–107, 108.
See also Halogenated flame retardants
hazardous effects, 102–103
timeline of actions, 106–107
toxicity, 104
Bromine, 76, 87, 102, 107, 217
B-scan, 302, 303, 309, 310, 317
B-staged resin, 66
Buckling, 229
Bulk scan, 302, 307, 320
Burn-in. *See* Stress screening
Burrs on lead-frame, 262
Button shear test, 201

Calcium layer resistance measurement method, 40
Can and header, 3
Carbon nanotube (CNT), 447
Carboxylic, 59, 60
Casting. *See* Potting
Catalyst type, 61
Cause and effect diagram.
See Fish-bone diagram
Cavity Direct Injection Molding (CDIM) technology (Apic Yamada Corp.), 429–430
advantages, 430
Cavity printing, 36, 157, 159, 160, 168, 175
Ceramic packages, 33–34
advantage, 34
application in MEMS, 33
Chemical etching, 293, 297
Chemical properties, 216, 216–218
Chip crack, 201
Chip-in-polymer (CIP), 24, 25, 162, 166
Chip-level package, 20
Chip-on-board, 89, 147–149

Petitioner Samsung Ex-1055, 0475

Chip-on-flex (COF), 30
Chip-on-flex MCMs (COF-MCMs), 30
Chip scale packages (CSPs), 17, 18, 80, 157, 420
Chip size, 240, 420
C-mode, 302, 304, 305, 312–313, 315, 317, 319
C-mode scanning acoustic microscope (C-SAM®), 302–303, 389
Coefficient of hygroscopic expansion (CHE), 189, 208–210, 254
  expansion of polymer chain, 211
  measurement of hygroscopic swelling, 210
Coefficient of moisture expansion (CME). *See* Coefficient of hygroscopic expansion
Coefficient of thermal expansion (CTE), 2, 33, 34–35, 47, 69, 149, 159, 189–191, 208, 366, 431
Cold shrinkage, 243, 244, 246
Collectable volatile condensable materials (CVCM), 212
Coloring agents, 78
Combined load-stress condition, 276
Commercial off-the-shelf (COTS), 1
Compression molding technique, 145–146, 162, 164, 167, 425–427, 454. *See also* Flow Free Thin (FFT) molding system (Towa Corp)
Compressive modulus, 62
Compressive strength, 62
Condensation, 49, 53
Condensation cure, 92, 95–98
Connectors, 2, 7, 36, 79, 90, 151, 175, 366, 420
Contaminants, 1, 212, 273–274, 387
Contamination level, 216–217
Contributing factors, 235–236
Conventional underfill, 155
Corroded die, 227, 403
Corrosion, 273, 273–274
Corrosive gases, 31, 33, 39, 42, 211
Coupling agents, 73
Cracked lead, 227, 402
Cracking potential, 197, 199
Creep, 229, 235
Critical failure mechanisms, 377
Cross-bonded stacking, 23
Cross-linking, 48, 189
Cross-linking density, 193
Crystal silica, 68, 69
Cu bump bonding (CBB), 25, 26
Cure cycle, 61, 100, 188–189
Cure temperature, 182, 187
Cure time, 189
Curing agents/hardeners, 60–66
  properties of DGEBA epoxy resin, 65
Curing/hardening process, 48, 187–188
Curing schedule, 91
Cyanate ester, 11
Cycled temperature, with constant humidity and bias, 388
Cycloaliphatic amines, 65
Cycloaliphatic epoxies, 51, 59

Dam-and-fill technique, 147–149
Dark-field, 299–300, 341
De-adhesion. *See* Delamination
Decabromodiphenyl ether (Deca-BDE), 104–107
Decapsulation, 288, 290–296, 317, 347
  comparison of methods, 291–292
  decapsulator and decapsulated package, 295
  mechanical, 296
  plasma etching, 296
  thermo-mechanical, 294, 296
Defect and failure analysis techniques
  atomic force microscopy, 342
  destructive evaluation
    analytical testing, 289–290
    decapsulation (removal of encapsulant), 290–296
    internal examination, 296
    locating site and identifying mechanism, 297

Petitioner Samsung Ex-1055, 0476

Defect and failure analysis
techniques (*contd.*)
selective layer removal, 297
simulation testing, 297–298
electrical testing, 288
electron microscopy, 332–342
infrared microscopy, 342–344
non-destructive evaluation, 288–289
optical microscopy, 298–301
scanning acoustic microscopy, 301–321
case studies, 312–321
C-SAM®, 302–310
imaging modes, 302
scanning laser acoustic microscope, 310–312
X-ray microscopy, 322–331
Defects, 225, 227–228, 236, 287, 288, 313, 348, 399, 403–404
Deflashing, 173–175
Delaminated passivation, 227
Delamination, 246–247, 246–247, 251–258, 251–258
crack propagation, 252
CTE mismatch strains and stresses, 247
effect of loads, 252–253
effect of package moisture absorption, 257
interface model, 255
mechanical model, 254
stages, 256
types, 246
Depolymerization, 235, 235, 275, 275
Desiccant, 211, 260, 449–450
Design qualification.
See Virtual qualification
Destructive evaluation, 289, 289–298
Destructive techniques, 288.
See also Non-destructive techniques
Die attach, 7, 11, 315–316, 429
Die cracking, 245–246
Dielectric constant, 37, 62–63, 214
Dielectric strength, 216
Die-paddle shift, 184, 289
Die shear test, 201
Die to wafer (D2W), 27
Differential interference contrast, 300–301
Differential scanning calorimeter (DSC), 186, 192, 290
Diffusion coefficient, 203–204
Diglycidyl ether of bisphenol A (DGEBA), 50, 50, 59
Diisocyanate, 52–53
Dimethyldichlorosilane (Di), 52
Dissipation factor, 63, 214, 214
2D multi-chip module (2D MCM) packages, 18, 19
Dow corning materials
silicone materials, 93
2D package, 12–19
3D package, 19–31
design, 23
encapsulation, 161–169
3D packaging process, 22
3D stacked die packages, 240
3D stacked molded interconnect device package, 29
Dual-Core Intel Itanium 2 processor 9000 series, 417
Dual in-line package (DIP), 13, 14, 134, 135, 276, 420
Dual-stage sorption, 206
Ductile fracture, 265–266
Durometer, 93, 188, 290
Durometer hardness test, 90, 290
3D wafer-level die stacking design, 25, 26
3D wafer-level package, 24–29
2D wafer-level package (WLP), 159–161
Dye penetration test, 289
Dynamic random access memory (DRAM), 420

Economy of screening, 407–408
EEC “glow wire” and “needle flame” tests, 391

Petitioner Samsung Ex-1055, 0477

EIA/JEDEC, 355
Ejection, 133, 135, 140–141, 188, 189
Elastic deformation, 229
Elastomers, 35
Electrical open, 230–231, 232–233
Electrical parameter drift, 230
Electrical properties, 214–216
Electrical resistance, 34, 40, 67, 115
Electrical short, 257
Electrical testing, 288
Electronic packaging, 1, 7–10
  high temperature electronics, 433
  levels, 10
  low temperature electronics, space applications, 433–434
    silicon-germanium (SiGe) devices, 434
  objectives, 7
  operational temperatures for unheated spacecraft, 434
  plastic package assembly flowchart, 8
  tape-automated bonding (TAB) process, 9
Electronics, 1
Electron microscopy, 332–339
  advantages, 333
  electron–specimen interaction, 333–335
  environmental scanning electron microscopy (ESEM), 337–339
  scanning, 335–337
  transmission electron microscopy, 339–342
Electron-specimen interaction, 333–335
Elongation, 198–200
EME-U series, 115
Encapsulant failures
  brittle fracture, 262–265
  delamination, 251–258
  ductile fracture, 265–266
  fatigue fracture, 266–268
  vapor-induced cracking (popcorning), 258–262
Encapsulant properties, characterization of
  chemical properties
    flammability and oxygen index, 218
    ion diffusion coefficient, 217
    ionic impurity (contamination level), 216–217
  electrical properties, 214–216
    electrode arrangement, 215
  hygro-thermomechanical properties
    adhesion strength, 200–203
    coefficient of hygroscopic expansion, 208–211
    CTE and glass transition temperature, 189–195
    flexural strength and modulus, 197–198
    gas permeability, 211–212
    moisture content and diffusion coefficient, 203–208
    outgassing, 212–214
    tensile strength, elastic, shear modulus and %elongation, 198–200
    thermal conductivity, 195–197
  manufacturing properties
    bleed and flash, 184
    curing time and temperature, 187–188
    gelation time, 183–184
    hot hardness, 188–189
    polymerization rate, 185–187
    post-cure time and temperature, 189
    rheological compatibility, 184–185
    spiral flow length, 181–183
Encapsulants
  advantages, 34
  dielectric strength, 216
  market conditions and manufacturers, 79–80
  other plastic encapsulation methods, 35–36

Petitioner Samsung Ex-1055, 0478

Encapsulants (*contd.*)
plastic molding compounds, 34–35
properties, 182
Encapsulated microelectronic packages
classification, 13
2D packages
chip scale package, 18
dual in-line package, 14
flip-chip plastic ball-grid array package, 18
multi-chip module packages, 18–19
multi-chip-module plastic ball-grid array package, 19
pin-grid array package, 14
plastic-leaded chip carrier package, 16
quad flatpack, 16
single in-line package, 14
small-outline package, 15
substrate packages, 17–18
surface-mounted packages, 14–17
tape-automated bonding package, 17
through-hole mounted packages, 12–14
wire-bonded plastic ball-grid array package, 18
3D packages
chip-in-polymer package, 25
3D die stacking design, 26
folded packages, 31
homogeneous die stacking designs, 24
horizontally stacked die design, 20
and interconnection design, 22
interconnection metallization grooves, 23
interconnection vias in 3D WLP, 25
molded interconnect device package stacking design, 29
non-homogeneous die stacking designs, 24
SMAFTI technology, 28
stacked die, 20–29
stacked die package, 26
stacked package designs, 30
stacked packages, 29–30
stacked wafer packaging design, 29
through-silicon via process flow, 27
wire interconnection and die stacking design, 21
plastic package, 11
thermo-mechanical properties, 12
Encapsulation defects
delamination, 246–247
die cracking, 245–246
flash, 250
foreign particles, 250
incomplete cure, 250
non-uniform encapsulation, 249–250
paddle shift, 241–242
voids, 247–249
warpage, 242–245
wire sweep, 236–241
Encapsulation defects and failures
package defects and failures, 225–228
classification of failure mechanisms, 228–235
contributing factors, 235–236
Encapsulation failures, 251
Encapsulation of 3D packages
chip-level encapsulation and assembly of MID stacked packages, 170
compression molding, 167
die stack, 163
die stack with injection molding, 164
3D interconnection via VPS, 169
3D Thomson package, 165

Petitioner Samsung Ex-1055, 0479

multi-chip module (MCM) stack package, 164
process flow for chip-in-polymer package, 166
stacked modular package, 168
wafer-level stacked dies, 167
Encapsulation of 2D WLP
compression molding, 162
process flow for Super CSP™, 163
WL-CSP, 161
Encapsulation process technology
cleaning and surface preparation
deflashing, 173–175
plasma cleaning, 169–173
3D packages, 161–169
2D wafer-level packages, 159–161
glob-topping technology, 147–150
molding technology
comparison of molding processes, 146
compression molding, 145–146
injection molding, 143–144
reaction-injection molding, 144–145
transfer molding, 129–142
potting and casting technology
one-part encapsulants, 152–153
two-part encapsulants, 153–154
printing encapsulation technology, 157–159
types, 130
underfilling technology
conventional flow, 155–156
no-flow, 157
Encapsulation techniques, 8, 90, 129, 157, 162, 168, 181, 248, 249, 423
Energy dispersive X-ray (EDX) spectroscopy, 217
Engineering thermoplastics (ETPs), 79
Environmental loads, 363–364
Environmentally friendly encapsulants, 1, 47, 102–121
toxic flame retardants, 102–107
Environmental scanning electron microscopy (ESEM), 337–339
Environmental stress, 275
Epichlorohydrin, 49–51, 217
Epoxies, 47, 49–51, 64
aliphatic, 50
cycloaliphatic, 51
Novolac, 51
Epoxy cresol novolacs (ECN), 59
Epoxy functionalities, 49
Epoxy molded compounds
material development, 87
Epoxy resins, 57, 59
mechanical and electrical properties, 61–63
Error seeding, 402
Ethylene-vinyl acetate (EVA), 452
copolymer encapsulants, 452–453
Ethylene-vinyl acetate (EVA), 452
Eutrophication, 116

Failure accelerators, 268–276
combined load–stress conditions, 276
exposure to contaminants and solvents, 273–274
general environmental stress, 275
manufacturing and assembly loads, 276
moisture, 268–272
absorption and desorption, 270
residual stresses, 274–275
temperature, 272–273
Failure analysis techniques,
selection of, 344–348
condition and construction of package, 345
defect and, 348
lateral resolution *versus* depth of penetration, 346
performance of analysis tool, 345
Failure analysis techniques, selection of, 344–348

Petitioner Samsung Ex-1055, 0480

Failure mechanism, 226, 228–235, 297, 355, 380
chemical loads, 235
classification, 234
electrical loads, 235
mechanical loads, 229
overstress failures, 229
PoF based models, 355
thermal loads, 229, 235
wearout failures, 229
Failure mode, 230, 232, 370
Failure modes, mechanisms, and effects analysis (FMMEA), 369–371
flowchart, 370
severity ratings, 371
Failure rate curve, 353–354
Failure rates, 352
Failures, 251–266
Failure site, 226, 229, 230, 232, 297
Fatigue crack, 229, 234, 266–268, 380
Fatigue fracture, 266–268
mechanism, 266
Feed-through interconnections (FTI), 26, 27
Fickian moisture diffusion, 204, 205
Filler content, 68, 69, 72
Filler figure ratio, 72
Fillers, 66–68, 66–73
advantages and disadvantages, 67
Alpha Emission Rate (AER), 74
effect of filler figure ratio, 72
effect of lowering CTE, 69
effect on thermal conductivity, 68
moisture ingress susceptibility, 72
particle size distribution, 71
typical and characteristic properties, 67
Finite element analysis (FEA), 207
Fish-bone diagrams, 236, 237
Flame retardants, 76–77
properties of standard and brominated epoxy resins, 76
resistance properties, 77
toxicity, 76
Flammability, 218, 391
Flammability and oxygen index, 218, 391
nonfeasability. *See* EEC "glow wire" and "needle flame" tests
Flash, 9, 173, 184, 250
Flexibilizers, 75
Flexible OLEDs, 449
Flexible solar cells, 453
Flexural modulus, 197–198
Flexural strength, 197–198
Flexural strength and modulus three-point bend test, 197
Flip-chip plastic ball-grid array (FC-PBGA), 17, 18
Flow Free Thin (FFT) molding system (Towa Corp), 427, 429
advantages, 427
Flow resistance, 81
Fluids dynamics analysis package (FIDAP), 240
Fluorescence microscopy, 301
Fluorocarbons, 78
Folded flexible circuit, 31
Folded package, 31, 32
Foreign inclusion, 228
Foreign particles, 250
Formaldehyde, 51, 54
Fourier transform infrared (FTIR) spectroscopy, 39
Four-point loading test, 198
Fowler–Nordheim model, 369
Fractured die, 227, 245
Fracture test, 200
Free volume theory, 194, 195
Functional diversification, 417–419
Fused silica, 56, 66–71, 121

Galvanic corrosion, 387
Gang-pot molds. *See* Multi-plunger molds
Gas permeability, 211–212

Petitioner Samsung Ex-1055, 0481

Gate position, 133, 238
Gates, 133, 135, 238–239, 304, 307
Gel time, 183–184
General Electric materials
  by-products of condensation cure RTV encapsulants, 98
  condensation cure RTV encapsulants, 96, 97
  material properties of addition cure RTV products, 98, 99
  profile of RTV silicone, 95
  RTV silicone application, 94
GE-100 series, 116
Glass Transition Temperature (T_g), 141–142, 189–195, 190, 191, 272
  effect of cross-linking density, 193
Glob top, 89–90, 147
Glob-top encapsulants, 35–36, 89–90, 129, 147–150
  Henkel Loctite Corporation, 91
Glob-top technology
  advantages and disadvantages, 147
  Auger pumps with RPDV, 150
  dam-and-fill encapsulation, 148, 149
  encapsulant dispensing system, 148
  encapsulated chip-on-board, 148
Glop-top dispensing equipment, 147
Green encapsulant material development
  flame resistance, 108
  general approach, 109
  green packaging, 108
  with non-halogenated flame retardants, 111–116
    advantages and disadvantages, 113–114
    choices of non-toxic flame retardants, 111
    comparison of mechanisms, 112
    electrochemical reactions, 115
  without flame retardants, 116–121
    self-extinguishing mechanism, 117
Green encapsulants. *See* Environmentally friendly
Green molding compounds
  flame resistance, 121–122
  lead-free solders, 253
  Loctite, 118–119
  Nitto Denko, 121
  Shin-Etsu, 120
  Sumitomo Bakelite, 117
GR series, 116
Guarded hot-plate method, 196

Halogenated flame retardants, 102
Halogens, 102
Hardener. *See* Curing agent
Hardness Shore D, 91, 188, 189
Heat deflection temperature, 61
Heat-sink small-outline package (HSOP), 15
Hele-Shaw model, 248–249
Helium leak test, 38–39
Hermetic packages, 31–34, 36–42, 435
  ceramic packages, 33–34
  folded package designs, 32
  metal flatpack, 32
  metal packages, 33
  properties of Kovar and Alloy 42, 33
Hermetic testing, 39
Hexabromocyclododecane (HBCD), 103, 104
High density interconnection (HDI), 30
Highly accelerated life test (HALT), 371, 372–373
  strength limits and margins, 374
Highly accelerated stress screening (HASS), 374
Highly accelerated stress test (HAST), 110, 386, 396
Highly accelerated temperature and humidity stress test, 388

Petitioner Samsung Ex-1055, 0482

High-resolution scanning X-ray diffraction microscope (HR-SXDM), 328–329
advantage, 329
High temperature
automotive electronics, 432
electronics, 431, 433, 448
hardness, 187, 188
maximum junction and operating ambient temperature extremes, 432
operation test, 384
storage test, 384
Historical overview of encapsulation
"Can and header" transistor package, 3
Kovar transistor package, 2
pre-molded plastic package, 7
transfer molding, 4, 5
History of qualification, 352–356
Homogeneous stacking design, 23, 24, 240
Hot chemical shrinkage, 243, 244
Hot hardness. *See* High-temperature hardness
measurement from indentation resistance, 188
Humidity tests
Autoclave test, 386–387
cycled temperature, with constant humidity and bias, 388
highly accelerated temperature and humidity stress test, 388
IPC/JEDEC J-STD-20 MSL classifications, 389
temperature-humidity-bias stress tests, 387
test to classify moisture sensitivity level for surface-mount devices, 388
Humidity tests, 386–390
Hydrated metal oxide powders, 78
Hydrocarbon waxes, 78
Hygroscopic mismatch strains, 209
Hygroscopic swelling/expansion, 208
mechanism of, 209
Hygro-thermomechanical properties, 189, 189, 220

IEEE (Institute of Electrical and Electronics Engineers) 1413 standard, 355
Imaging modes, 302
Impact strength, 75
Improper marking, 228
Incomplete cure, 228, 250, 289
Indentation resistance, 188
Industry practices, 392–394
quality related terminology, 398
test conditions used in industry, 393
test methods and conditions, 395–397
Industry practices, 392–394
Inert flexibilizers, 74–75
Inertial forces, 229
Infant mortality failures, 353, 356, 375
Infrared (IR) spectrographic analysis, 289, 290
Infrared (IR) spectroscopy, 289
Infrared microscopy, 289, 342–344
scanning infrared microscope, 344
Inhibitor, 95
Injection molding, 143–144, 146
apparatus, 143
disadvantage, 143
In-mold cure time, 66, 84, 85
Institute of Materials Research and Engineering (IMRE), 451
Integrated circuit (IC) chips, 250, 417
chip-to-substrate and substrate-to-board packaging, 423, 426
miniaturization and integration trends, 419
packaging materials challenges, 428–429
pitch sizes, 423

Petitioner Samsung Ex-1055, 0483

Intel's product qualification method, 355
Internal examination, 296
International Technology Roadmap for Semiconductors (ITRS), 420
  challenges in future semiconductor packaging, 422–423
  maximum junction and operating temperatures extremes of semiconductors, 432
  semiconductor packaging and encapsulation, 421
International Technology Roadmap for Semiconductors (ITRS), 420
Ion diffusion, 268, 274
Ion diffusion coefficient, 217
Ionic impurity, 216–217
Ionic purity, 88
Ion-selective field effect transistor (ISFET), 445
Ion-trapping agents, 78
ISFET biosensors, 445
Ishikawa diagram. *See* Fish-bone diagram
ISO 9000, 409
Isothermal fractional conversion, 186

KMC-2000 Series, 116
Known good die (KGD), 27
Kovar package, 2, 33

Lead corrosion, 9
Lead-frame, 8–9, 11, 12, 37, 74, 121, 136, 227, 241, 255, 257–258, 261
Lead-frame tab pull test, 201–202
Lead-free solder, 86, 253
  issues related to, 86
Lead plating, 9, 173
Lead trimming, 9, 110, 173
LED
  encapsulated with polymeric optical material, 451
  inverted pyramid, 452
  plastic encapsulation, 452
Lewis acids, 59, 60, 65
Life-cycle loads, 363–366, 371. *See also* Environmental loads; Operational loads
  in key applications, 365
  load conditions imposed by manufacturing processes, 364
Light-emitting diode (LED), 157, 175, 344
Locating failure site, 297
Low-pressure plasma (LPP), 173
Low shrinkage, 59
Low stress, 59, 371
Low temperature
  electronics, 431–434
  operational temperatures, 434
Low temperature co-fired ceramic (LTCC), 34

Macro-voids, 206
Manufacturers, parts family assessment and qualification, 400–401
Manufacturers of encapsulants, 79–80
Marketing conditions of encapsulants, 79–80
Mass production qualification, electronic packages, 351
Materials development, 86–89
Maximum pin count, 420, 424
MCM-V (vertical multi-chip module), 22
MCM with PBGA package design, 19
Mechanical loads, 229
MEMS packaging, 439–440, 441–442
Metal hydrates, 77, 111–113
Metal hydroxides, 77, 116
Metallization corrosion, 35, 296, 388
Metallization deformation, 201
Metal package, 33
Methyl, 52
Micro-ball-grid array (μBGA), 17

Petitioner Samsung Ex-1055, 0484

Microelectromechanical systems (MEMS), 1, 33, 417, 435–440
ITRS requirements and challenges, 442–443
packaging options, 441
plastic-encapsulated device, 438
plastic-encapsulated pressure sensor, 438
plastic encapsulation process from Industrial Technology Research Institute, 437
pressure sensor from Motorola, 438
plastic packaging process, 436
plastic pre-molded package, 439
requirements and challenges, 442–443
Microelectronic device structure and packaging
CDIM process, 430
challenges in future semiconductor packaging, 422–423
chip-to-substrate and substrate-to-board bonding, 426
flow free thin molding technique, 429
miniaturization and integration trends, 419
Moore's law, "More than Moore" approaches, 418
number of transistors per chip, 418
packaging materials challenges, 428–429
single-chip package technology, 424, 425
stacked dies in wafer-level CSP, 427
Microelectronic packaging
historical timeline and trend for, 421
Micro-optoelectromechanical systems, 435
Micro-voids, 206, 254
MIL-HDBK-217 (military handbook), 352
Miniaturization trend, 417, 419
Minimum overall package profile, 424
Misaligned leads, 226, 227, 403, 404
Mix ratio, 93, 97, 99, 250
MicroLeadFrame® (MLG®) package, 440
Mode cracking, 22
Moisture absorption, 270
Moisture-barrier bag, 260
Moisture concentration, 205, 208, 209, 211, 269, 271–272
Moisture content, 203–208
Moisture diffusion coefficient, 189, 203, 204, 205, 268, 272
Moisture diffusion rate, 81
Moisture sensitivity, 100
Moisture Sensitivity Level (MSL), 110, 203, 388–390
Moisture sensitivity levels
categories, 388–389
IPC/JEDEC standard classification, 389
Moisture solubility coefficient, 205
Moisture weight gain, 272
Mold cavity thickness, 239
Mold characteristics, 188, 189
Mold-clamping pressure, 139
Molded-interconnect device (MID), 29, 168, 170
Molding compound preform (pellet), 129, 130, 132, 244
Molding compounds, 11, 34, 47, 56–89, 108
accelerators, 66
coloring agents, 78
contents of epoxy, 57, 58
coupling agents, 73
curing agents or hardeners, 60–66
fillers, 66–73
flame retardants, 76–77
ion-trapping agents, 78
market conditions and manufacturers, 79–80
material properties, 81–85
key properties, 81
Nitto Denko, 82, 83, 121

Petitioner Samsung Ex-1055, 0485

Plaskon, 82, 85
Sumitomo Bakelite, 82, 84
materials development, 86–89
mold-release agents, 77–78
properties, 82
resins, 57–60
status of epoxy manufacturers, 80
stress-relief additives, 73–75
transient thermal response, 88
Molding pressure, 85, 240, 427, 454
Molding processes
comparison of, 146
Molding simulation, 141–142
Mold-release agents, 77–78
Montmorillonite, 447–448
Moore's law, 417–418
More than Moore, 417–419
Mother board, 10
Multi-chip modules (MCMs), 18–19, 157
Multifunctional epoxy resin, 59
Multi-plunger molds, 132–136
Multi-scan, 302, 303

Nano-material, disadvantage of, 449
Nano-particles
nano-fillers, 447.
See also Bentonite; Silica particles, nano-sized; Zeolites
Nano-sized particles, 448
Nanotechnology, 445–449
and nanoelectronics
nano-fillers, 447
Nitrogen-based substances, 77
Nitto Denko, 80, 82
properties, 83
No-flow underfill (NFU), 448–449
Non-destructive evaluation (NDE), 288–289
Non-destructive techniques, 287
Non-Fickian Diffusion, 206–208
bound and unbound water molecules, 206, 207
mechanisms of Fickian and, 208
Non-halogenated
flame retardants, 111–116
inorganic flame retardants, 111
advantages and disadvantages, 113–114
Non-hermetic package, 1, 439
Non-homogeneity, 250
Non-homogeneous stacking designs, 23, 24
Non-uniform encapsulation, 249–250
Novolac epoxies, 51, 57, 59, 88

Octabromodiphenyl ether (Octa-BDE), 105
OLED devices, 449–450
barrier coating, 450–451
packaging, 450
plastic encapsulant materials, 450
UV-cured epoxy resin, 449
OLEDs, photovoltaics, and optoelectronics, 449–453
inverted pyramid, 452
OLED packaging, 450
plastic encapsulation of LED arrays, 452
solar cell package, 453
One-part potting encapsulants, 152–153
Operational loads, 363
Optical microscopy, 298–301
bright-field, 299, 300
dark-field, 299–300, 301
differential interference contrast, 300–301
fluorescence microscopy, 301
polarized light, 300
techniques, 299–301
Zeiss, 299
Organic light-emitting diodes (OLEDs), 449–453
Ortho-epoxy cresol novolac (O-ECN), 51
Outgassing, 212–214
measurement, 213

Petitioner Samsung Ex-1055, 0486

Overstress failures, 229
Overstress screens, 401–402
Oxygen index, 218, 391

Package assembly, 8, 11, 242, 251, 273
Package availability, 42
Package cost, 37–38
Package defects, 225–226
  sites, types, and sources, 226–228
Package designs, 420
Package failures, 226–228
  sites, modes, mechanisms, and environmental loads, 229, 230–233
Package footprint, 19
Package hermeticity, 38–40
Package performance, 37
Package reliability, 59, 110, 129
Package weight, 36–37
Packaging levels, 10
Packaging materials challenges, 428–429
Packing, 139
Packing pressure, 139
Paddle-shift, 241–242
Partition-cell method, 211
Passivation layer crack, 75
Passivation pin holes, 227
PCBs. *See* Printed circuit boards (PCBs)
Pecht and Rudra model, 369
Peel strength, 75
Peel test, 202–203
PEMs. *See* Plastic-encapsulated microelectronics (PEMs)
Pentabromodiphenyl (Penta-BDE), 104, 105
Percentage (%) elongation, 198–200
Permeation curve, 212
Phenol, 51, 60, 66
Phenol-formaldehyde, 51, 54
Phenolic and cresol novolacs, 59
Phenolic resins, 54–56.
  See also Bakelite
Phenolics, 54–56, 64
Phenyl, 52
Phosphorous-based flame retardants, 115–116
Phosphorus-containing retardants, 77
Photovoltaic solar cells, 451
Physics-based modeling, 236
Physics-of-failure (PoF) approach, 351, 354, 358
  physical properties as inputs, 366
  reliability prediction using, 367–369
Pin-grid array (PGA), 6, 13, 14, 15
Pin-holes on lead coating, 226, 227
½ pitch size trend, 424
Plaskon, 80, 82
Plasma cleaning, 169–173, 175
  APPJ apparatus, 174
  comparisons of studies, 172
  low-pressure plasma (LPP) cleaning, 173
  YES G1000 plasma cleaner, 171
Plasma-enhanced chemical vapor deposition (PECVD), 7, 450–451
Plasma etching, 164, 290, 292, 296
Plastic ball-grid array (PBGA), 17, 171, 242, 294
Plastic deformation, 229
Plastic dual in-line packages (PDIPs), 13
Plastic encapsulant materials
  chemistry
    addition polymerization process, 48
    advantages and disadvantages of polymeric materials, 64
    benzene ring, 50
    condensation or step-growth polymerization, 49
    DGEBA monomer and higher molecular weight polymer, 50
    epoxies, 49–51
    epoxy functionality, 49
    epoxy novolac formation, 51

Petitioner Samsung Ex-1055, 0487

ortho-epoxy cresol novolac, 51
phenolics, 54–56
polymers chains, 48
polyurethanes, 52–54
silicones, 52
environmentally friendly or "green" encapsulants
material development, 107–121
toxic flame retardants, 102–107
glob-top encapsulants, 89–90
potting and casting encapsulants
dow corning materials, 90–91
general electric materials, 91–95
underfill encapsulants, 95–101
Plastic-encapsulated microelectronics (PEMs), 39, 59, 132
Plastic-leaded chip carrier (PLCC), 14, 16, 172, 294
Plastic package
pre-molded/post-molded, 6–7
Plastic pin-grid array package, 14, 15
Plastic *versus* hermetic packages
availability, 42
cost, 37–38
hermeticity, 38–40
conditions for helium fine leak testing, 39
evaluation of cavity package, 39
performance, 37
reliability, 40–42
thermo-mechanical, 41
size and weight, 36–37
Polarized light, 300
Polybrominated biphenyls (PBBs), 103
Polybrominated dibenzodioxins (PBDDs), 105
Polybrominated dibenzofurans (PBDFs), 105
Polybrominated diphenyl ethers (PBDEs), 103–104
ban of, 105
Polybutylacrylate (PBA), 75
Polydimethylsiloxane (PDMS), 52, 52, 53, 445
formation, 53
Polyimide, 7, 11, 17, 35, 79, 203, 210, 261, 296, 325
Polymerization rate, 185–187
conversion *versus* time, 187
Polymerization reactions, 48
addition process, 48
condensation process (step-growth mechanism), 49
Polymers, 48
Polymethyl methacrylate (PMMA), 75
Polyolefinic compounds, 50
Polyurethanes, 52–54
aromatic/aliphatic, 55
classifications, 53–54, 55
unblocking mechanism, 56
Poor solder wetting of lead, 227
Popcorning, 258–262
Popcorn resistance, 59–60
Porosity, 185, 319–320
Post-cure temperature, 189
Post-mold cure time, 57, 110, 141, 193, 229, 243
Post-molded package, 6
Potential failure mechanisms, 371
Pot life, 91
Potting, 3, 36, 90–95, 151–154
Potting and casting encapsulants, 36, 90–95
with silicone material, 92
Potting and casting technology, 151–154
guidelines, 153
insulcast® epoxy compound, 151
one-part encapsulants, 152–153
two-part encapsulants, 153–154
advantages, 154
Potting geometry, 152
Power and temperature cycling, 385–386
Power supplies, 90, 151
Pressure cooker test. *See* Autoclave test

Petitioner Samsung Ex-1055, 0488

Printed circuit board (PCB), 7, 79, 147, 242, 251, 258, 368, 371, 420, 440
Printing encapsulants, 101–102
Printing encapsulation, 157–159
  materials, 101–102
  method, 36
Printing encapsulation technology
  encapsulated WL-CSP, 160
  planarization process, 158
  process flow, 158, 159
  stencil, 157–158
Processing residuals, 212
Product characteristics, 366–367
  manufacturing processes, material properties, 366
Product development process flow, virtual and product qualification, 359
Product qualification, 351, 358, 371–372
  accelerated testing, 378–382
  failure mechanisms, 380
  flowchart, 372
  HALT process, 373
  levels of, 375
    accelerated testing and TTF measurement, 376–377
    comparison, 376
    goal certification, 376
    similarity, 375–376
  modeling and validation, 378
  operating and destruct limits, 375
  qualification levels, 375
  qualification requirements, 374–377
  qualification test planning, 377–378
  reliability assessment, 382–382
  strength limits and highly accelerated life test, 372–374
  strength limits and margins, 374
  TTF of product life using PoF models, 379
Q factor measurement method, 40
Quad flatpack (QFP), 14, 16, 37, 59, 134, 137, 185, 241, 259, 294, 423
Qualification, 351
Qualification accelerated tests
  flammability and oxygen index test, 391
  humidity tests, 386–390
  radiation hardness, 392
  salt atmosphere test, 391
  solderability, 391–392
  solvent resistance test, 390
  steady-state temperature test, 384
  thermal cycling test, 385–386
Qualification and quality assurance
  industry practices, 393–394
    example test conditions, 393
    test methods and conditions, 395–397
  product qualification
    accelerated testing, 378–382
    modeling and validation, 378
    qualification requirements, 374–377
    qualification test planning, 377–378
    reliability assessment, 382–383
    strength limits and highly accelerated life test, 372–374
  qualification accelerated tests
    flammability and oxygen index test, 391
    humidity tests, 386–390
    radiation hardness, 392
    salt atmosphere test, 391
    solderability, 391–392
    solvent resistance test, 390
    steady-state temperature test, 384
    thermal cycling test, 385–386
  qualification and reliability assessment, 352–356
  qualification process overview, 356–361

Petitioner Samsung Ex-1055, 0489

virtual qualification
application requirements, 367
failure modes, mechanisms, and effects analysis (FMMEA), 369–371
life-cycle loads, 363–366
product characteristics, 366–367
reliability prediction using PoF approach, 367–369
Qualification process, 351, 356.
See also Life-cycle loads
elements of, 359–360
objectives of, 360–361
qualification and quality assurance test, 360
and reliability assessment
bathtub curve, 353
history, 352–356
reliability prediction methodologies, 357
rollercoaster curve, 354
stages, 358
stages, 358
virtual and product qualification, 359
Qualification requirements, 374–377
Qualification test planning, 377–378
Qualitative accelerated testing, product, 379, 383–384
Quality, 351
Quality, International Standards Organization (ISO), 394
quality assurance, 398–399
quality conformance, 394–398
Quality assurance
failure distribution pattern, 406, 407
quality related terminology, 398
screening, 399–400
screens and defects, 403–404
screen selection
economy of screening, 407–408
root-cause analysis, 406–407
screen duration, 405–406
screen stress levels, 402–405
statistical process control, 408–410
Six Sigma process DMAIC, 410
Six Sigma statistical goal, 409
stress screening and burn-in, 400–401
TTF distribution characteristic, 406
Quality assurance testing/screening, 358
Quantitative accelerated testing, product, 379
Quantitative B-scan analysis mode (Q-BAM™), 302, 309, 310

RADC Reliability Notebook in 1959, Reliability Applications and Analysis Guide, 352
Radiation, 73
Radiation hardness, 392, 394
Radioisotope heating units (RHUs), 433
Ragged fillers, 70
Ram-follower device, 182
Random failure rate, 353
Reaction-injection molding, 144–145
advantage, 144
Reactive flexibilizers, 74
Red phosphorus flame retardants, 111, 115
Reflection-mode techniques, 308–309
Relative permittivity, 214
Reliability assessment, 352–356, 382–383
Reliability Factors for Ground Electronics Equipment, 352
Reliability modeling, 353
Reliability prediction methodologies, comparison, 356
using PoF approach, 367–369
Reliability Stress Analysis for Electronic Equipment, 352
Requirement trends, 420
Residual stresses, 274–275

Petitioner Samsung Ex-1055, 0490

Resin bleed, 173, 184
Resin-filler interface, 206, 208
Resins, 57–60
Resin transfer molding, 144
Restriction of the use of certain Hazardous Substances (RoHS), 105
Rheological compatibility, 184–185
  effect of moisture, 186
Rollercoaster curve, 354
Room Temperature Vulcanization (RTV), 91, 95, 152
Root-cause analysis, 406–407
Rotary positive displacement valve (RPDV), 149, 150
RTV silicones, 92

Salt atmosphere test, 391
Sample size selection, 377–378
SCAN® filler, 88
Scanning acoustic microscopy (SAM), 248, 287, 301, 330, 332. *See also* Acoustic micro-imaging (AMI)
  case studies, 312–321
  C-SAM®, 302–310
    acoustic impedance values, 306
    acoustic scan, 305
    acoustic wave reflectivity, 306
    A-scan imaging, 304
    B-scan, 310
    crack profile, 309
    die surface, 305
    quantitative B-scan analysis, 310
    versus SLAM™, 308
    through-transmission scan, 307
    time-of-flight scan, 308
  imaging modes
    acoustic, 303
  scanning laser acoustic microscope
    acoustic fringes, 312
Scanning and transmission electron microscopy (STEM), 333
Scanning electron microscopy (SEM), 288, 329, 333, 335–337
Scanning laser aoustic microscope (SLAM™), 302, 310–312
  acoustic fringes, 312
  operating principle, 311
Screen duration, 405–407
Screening, 399–400
  economy of, 407–408
Screen printing, 157
Screens, 402
  defects they expose, 403–404
  duration, 405–406
    failure density, 405
    failure distribution pattern, 406, 407
    TTF distribution characteristic, 406
Screen selection, 401–402
  duration, 405–406
  root-cause analysis, 406–407
  stress levels, 402–405
Selective layer removal, 297
Self-extinguishing green molding compound, 121
SEMATECH, 355
Semiconductor technology
  chip size, 420
  packaging
    challenges in, 421
    emerging technologies, 434–435
    and encapsulation technology trend, 421
    glass transition temperature, 433
    used in automotive applications, 433
  physical limits, 417
  temperature requirements, 432–433
SEMI G29 procedure, 216
SEMI G45-88 test, 184
Shadow-Moiré method, 289
Shear rate, 140, 182, 185, 200
Shear thinning behavior, 185–186

Petitioner Samsung Ex-1055, 0491

Shrink small-outline package (SSOP), 15
Signal propagation speed, 37
Silanes, 73
Silica-coated alumina nitride (SCAN), 68, 88
Silica particles, nano-sized, 448
Silicone elastomers, 75
Silicon efficiency, 19
Silicones, 52
  condensation mechanism, 53
  formation of polydimethylsiloxane (PDMS), 53
  free-radical addition polymerization, 54
  general formula, 52
  polydimethylsiloxanes, 52
Siloxane polymer, 52
Simulation testing, 297–298
Single-chip packages, 29, 30
  performance and thermal characteristics, 420
  trends based on ITRS, 424
Single-chip WLPs, 159–160
Single in-line package (SIP), 13, 14
Six sigma process, 409–410
SMAFTI assembly process, 27, 28
SMAFTI (SMArt chip-FTI) technology, 26, 27, 165
Small-outline integrated circuit (SOIC) package, 435
Small-outline J-leaded (SOJ), 15
Small-outline package (SOP), 14, 15, 147, 420
"S-N curve," fatigue failure curve, 352
Solar cell modules, 451–452, 453
  flexible, 453
Solderability, 391–392
Solvent resistance test, 390
  encapsulant chemical resistance test, 390
Spherical fillers, 70
Spiral flow test, 181
  molding tool, 183
Stacked die packages
  3D chip-level packages, 20–24
  3D wafer-level-packages, 24–29
Stacked package, 29–30
Stacked QFP-format MCM, 30
Statistical process control, 408–410
  Six Sigma process DMAIC, 410
  Six Sigma statistical goal, 409
Statistical process control, 408–410
Steady-state temperature test, 384
  high-temperature operation test, 384
  high-temperature storage test, 384
Stencil printing, 36, 157, 158
Step-stress analysis, 402
Storage floor life, 261
Strain energy release, 252–253, 267
Strain range based model, 369
Strength limits, 372–374
Stress intensity factor, 252, 259, 263–267
Stress-relief additives, 73–75
  influence of flexibilizers on epoxy resins, 75
Stress screening, 400–401
Stress screens, 401
Substrate, 17–18
Sumikon® EME, 116
Sumitomo Bakelite, 80, 82
  properties, 84
Super-resolution X-ray microscope (SR-XM), 329
Surface cleanliness, 257
Surface-mount technology, 14–17
Surface scan, 302, 303
Swelling, 208
  measurements, 210
Syringe valve, 149–150
System-in-package (SiP), 248, 419
System integration, 419, 420
System-on-chip, 419
System-on-package (SoP), 420

Petitioner Samsung Ex-1055, 0492

TAB package, 17
Tack-free time, 92
Tape-automated-bonded plastic ball-grid array (TBGA), 17
Tape-automated bonding (TAB), 9, 17, 89
Telescopic design, 24
Temperature cycling, 385
Temperature-humidity-bias stress tests, 387
Tensile modulus, 61, 198
Tensile strength, 198–200
Tetrabromobisphenol A (TBBPA), 103
THB tests, 277
Thermal conductivity, 195–197
  guarded hot-plate technique, 196
Thermal cycling test
  power and temperature cycling, 385–386
  temperature cycling, 385
  thermal shock, 385
Thermal loads, 229
Thermal mismatch stress, 47, 70, 251
Thermal shock, 385
Thermal stability, 34–35, 60
Thermal strain, 247, 273
Thermomechanical analyzer (TMA), 191–192, 209
Thermo-mechanical properties, 12
Thermoplastic polymers, 79, 452
Thermoplastics, 34–35
Thermosets, 129
Thermosetting polymers, 4, 34–35, 48
Thin small-outline package (TSOP), 1, 16, 249
Thomson approach, 22, 162
Three-point bend test, 197
Through-hole technology, 12
Through-silicon via (TSV), 26, 27
Through-transmission. *See* THRU-Scan™
Through-vias (TV), 24–26, 168
THRU-Scan™, 302, 307–308, 313, 316
Time-of-flight (TOF), 302, 308, 319
Times-to-failure (TTF), 361, 368, 379, 382, 383, 406
Tin–lead (Sn–Pb) eutectic solders
  abolishing use of, 86
Tin whiskers, 229
Titanates, 73
TMA. *See* Thermo-mechanical analyzer
Tolylene (toluene) diisocyanate (TDI)
Total mass loss (TML), 212
Towa Corp. *See* Flow Free Thin (FFT) molding system (Towa Corp)
Towers of Hanoi design, 23, 24, 240
Toxic flame retardants
  chemical structure of PBDE, PBB, TBBPA, and hexabromocyclododecane, 103
  timeline of actions taken on BFRs, 106–107
  toxicity of BFRs and antimony trioxide, 104
Transfer molding, 129
  aperture-plate mold, 134
  cavity filling, 139
  comparison of tools, 133
  defined, 129
  designs, 132
  different parts, 137
  encapsulation of quad flatpacks, 137
  equipment, 131–136
  glass transition temperature, 142
  limitations, 130–131
  multi-plunger mold, 134, 135, 136
  simulation, 141–142
Transfer molding process, 129, 131, 136–141
  process flow, 138
  stages, 138
  transfer rate control, 141

Petitioner Samsung Ex-1055, 0493

Transfer plunger, 129, 132, 134, 136–140
Transfer-plunger pressure (transfer pressure), 139–140
Transfer pot, 129, 130, 132
Transfer-rate control, 141
Transformers, 7, 36, 90, 191, 235
Transmission electron microscopy (TEM), 333, 339–342
  bright-field mode, 340–341
  dark-field mode, 341
  diffraction contrast, 341
  high-resolution mode, 341–342
Trapped gas, 212
Tray-scan, 302, 303, 320
Trends and challenges
  emerging technologies
    bioelectronics, biosensors, and bio-MEMS, 440–445
    microelectromechanical systems, 435–440
    nanotechnology and nanoelectronics, 445–449
    OLEDs, photovoltaics, and optoelectronics, 449–453
  extreme high- and low-temperature electronics, 431–434
  microelectronic device structure and packaging, 417–431
Trial-and-error methods, 235, 236
Trifluoropropyl, 52
True positive displacement pump (TPDP), 150
Tungsten plug, 27, 29
Two-part potting encapsulants, 153–154

UL flame class, 81
UL vertical flammability test, 218, 219
Unbalanced encapsulant flow, 241
Unbound water molecules, 206
Underfill, 98
Underfill encapsulants, 36, 95–101
  advantages, 98, 100
  Henkel Loctite Corporation, 101
  key properties, 100
  recent advances, 100
Underfilling technology, 154–157
  advantages and disadvantages, 154
  conventional flow, 155–156
  conventional *versus* no-flow process flow, 155
  factors related to void-free, 156
  flip-chip encapsulation, 156
  no-flow disadvantages, 157
Underwriters Laboratory (UL), 76, 218, 391

Vacuum printing encapsulation system (VPES), 158–159, 247, 248
Vapor-induced cracking, 258–262. *See also* Popcorning
  contributing factors, 260
  preventing package cracking, 260–262
  quad flatpack cracking, 259
  stages, 258
Vapor-induced delamination, 251–252, 258, 261, 275
Vertical flammability test, 218
Vertical multi-chip module (MCM-V), 22
Via first method, 25
Via last method, 25
Vibration, 229, 345, 363–364, 368–369
Vicker hardness, 67
Vinyl, 52
Virtual qualification, 351, 361–370
  flowchart, 362
  life-cycle loads, 365
Viscosity, 185, 200–201
Visual examination, 288
3V™, 302, 303
Voids, 247–249
  air-trap formation, 249

Petitioner Samsung Ex-1055, 0494

Voids (*contd.*)
defect and void-free encapsulation, 248
Hele-Shaw model, 248–249
Volume resistivity, 215, 216

Wafer-level chip-scale package (CSP), 427
Wafer-level package (WLP), 1, 20, 24–29, 145, 157, 159–161, 420, 427, 440, 454
Wafer-level packaging, 440
Wafer-level underfill (WLU), 449
advantages of, 449
Wafer to wafer (W2W), 27
Warpage, 242–245
concave mode, 243
contributing factors, 243–245
effect of encapsulation composition, 245
modes, 242
temperature profile, 243
volume shrinkage, 244
Waste from Electrical and Electronic Equipment (WEEE), 105
Water vapor regained (WVR), 212
Wearout failures, 229, 274, 353, 356, 381, 402, 405
Wearout screens, 401
Weighed-cell method, 211
Wet chemical decapsulation technique, 290
Wetting balance test, 392
Wire ball bond fracture, 226, 229
Wire-bonded plastic ball-grid array (PBGA), 17, 18
Wire bond height, 240
Wire diameter, 238, 239
Wire orientation angle, 239
Wire sweep, 236–241
contributing factors, 238
density, 238–240
diameter and breaking load, 239
extent, 239
geometrical parameters, 240
profiles, 241
Working time. *See* Pot life

X-ray contact microscope, 325–327
parameters and aspects, 326
X-ray fluorescence spectroscopy, 331–332
operating modes, 331–332
X-ray generation, 322–325
X-ray microscopy
advantages, 321–322
case study: encapsulation in plastic-encapsulated devices, 329–331
contact microscope, 325–327
generation and absorption, 322–325
absorption coefficient *versus* X-ray wavelength, 325
X-ray tube, 323
X-ray wavelengths, 324
high-resolution scanning diffraction microscope, 328–329
projection microscope, 327–328
principle, 328
X-ray projection microscope, 327–328
X-ray wavelengths, 324, 325

Zeolites, 448
Zircoaluminates, 73

Petitioner Samsung Ex-1055, 0495