

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FORMFACTOR, INC.,

Petitioner,

v.

TECHNOPROBE S.P.A.,

Patent Owner.

INTER PARTES REVIEW OF
U.S. PATENT NO. 11,035,885
Case IPR2024-00933

DECLARATION OF FREDERICK L. TABER

Ex. 1003

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I. INTRODUCTION

1. My name is Frederick L. Taber. I have been retained by counsel for Petitioner, FormFactor, Inc., as an expert witness in this *inter partes* review to examine whether claims 1- 23 of U.S. Patent No. 11,035,885 (“the ’885 patent) are patentable over certain prior art.

2. I have personal knowledge of all the facts set forth herein, and if called to testify at any hearing in this *inter partes* review, I would competently testify and verify that testimony contained herein.

3. I am being compensated at my hourly rate of \$600 per hour. I am also being reimbursed for out-of-pocket expenses. My compensation does not depend in any way on the outcome of this proceeding or the particular opinions I express, or the testimony I give.

4. I expect to be available for deposition and to testify at the evidentiary hearing in this *inter partes* review to the extent required.

5. This declaration contains my conclusions and a summary of my analysis including a summary of my conclusions; an overview of my qualifications as an expert; an overview of the scope and terms of my engagement for this declaration; an overview of the materials I have considered in arriving at my conclusions; an overview of the terminology and legal principles that I applied in my analysis; an overview of the technical background of the subject matter; an

overview of the '885 patent; an analysis of the level of ordinary skill in the art related to the '885 patent; and an analysis of the asserted references; and a patentability analysis of the challenged claims.

6. I have been informed that Patent Owner Technoprobe S.p.A asserted the '885 patent in *Technoprobe S.p.A. v. FormFactor, Inc.*, Case No. 1:23-cv-00842-JCG (D. Del.).

7. This declaration is based on information currently available to me. I intend to continue my investigation and study, which may include a review of documents and information that may yet be produced, as well as deposition testimony from depositions for which transcripts are not yet available or that may yet be taken in this review. Therefore, I expressly reserve the right to expand or modify my opinions as my investigation and study continue, and to supplement my opinions in response to any additional information that becomes available to me, any matters raised by Patent Owner and/or other opinions provided by Patent Owner's expert(s), or in light of any relevant orders from the Patent Trial and Appeal Board or other authoritative body.

II. BACKGROUND AND QUALIFICATIONS

8. My qualifications and professional experience are described in my Curriculum Vitae, a copy of which can be found in Ex. 1023. The following is a brief summary of my relevant qualifications and professional experience.

9. I have studied and practiced electrical engineering in the field of electronic test for my entire professional career, approaching 54 years. Of that, about 22 years was directed at design and development of test systems, followed by nearly 32 years focused on wafer probes and socketing used to provide temporary electrical contact to electronic components (a Device Under Test) being tested.

10. I hold a Bachelor's Degree in Electrical Engineering from Southeastern Massachusetts University (now the University of Massachusetts at Dartmouth).

11. My 50-plus years of industry experience include work for IBM Corporation (approximately 34 years), followed by consulting within the wafer probe and socket industries (approaching 20 years) and the founding and operation of a technical conference related to sockets for packaged electronics burn-in and testing (15 years - concurrent with my previously stated consulting). I was on the Board of Advisors to Chip Scale Review (an industry magazine) from 2004 - 2006, and then again from 2011 through 2014. Additionally, I served on the Advisory Board for Advanced Packaging magazine from 2006-2009.

12. My extensive experience with probe card technology includes the design and development of advanced wafer probe technologies. During this time, I managed and led the IBM team that developed an advanced wafer probing

technology, as well as the team that evaluated commercially available wafer probe technologies for use within IBM. I was a founding member of the SEMATECH Wafer Probe Council and served as a member of the organizing committee for the Semiconductor Wafer Test Workshop (focuses on wafer probing technology, and is the premier forum on wafer probing in the world) during 2000-2017 including being the Proceedings coordinator from 2007-2014.

13. My early work at IBM, from 1970 through 1992 focused on test system development and manufacturing introduction and test program development. This work involved the design and development of advanced automatic test systems for a wide range of IBM technologies, including memory circuit cards, large multi-chip modules (had substrates where over 100 chips were packaged, called TCMs, for Thermal Conduction Modules), and wafer testers. The wafer test work included advanced collaborative work with a tester supplier to design, develop and introduce a wafer test system for advanced bi-polar technology. While working within the wafer tester area, I became knowledgeable about all of the components of a wafer test system, including the test system itself, the test head, the prober and wafer probe cards and sockets, along with ancillary equipment like wafer probe metrology equipment, wafer probe cleaning technologies, etc.

14. My most recent work at IBM (1992-2004) includes leadership of the development, manufacturability (development of processes from the lab to volume production), and manufacturing introduction of an advanced wafer probe technology (TFI), which may continue in use today. Included in this work was the development of an advanced space transformer using glass ceramic technology. I was also extensively involved in advancements to an existing buckling beam probe technology (*i.e.*, COBRA) to improve its bandwidth and current carrying capabilities, along with cost reduction initiatives. Within semiconductor test at IBM, the need for a portfolio of wafer probe technologies to meet the demands of particular semiconductors existed, so at times I was called upon to seek a variety of wafer probe technologies from suppliers, including cantilever type technologies. I managed the team that evaluated these suppliers' wafer probe technologies and made improvement recommendations. When I retired from IBM in 2004, I held the position of Senior Engineering Manager within the IBM Microelectronics' World Wide Test Organization.

15. I have presented a number of papers related to wafer probe technology at prestigious conferences, including papers on advanced wafer probe technologies. I hold two U.S. Patents concerning wafer probing technology. I have also been a paper reviewer (wafer probing topics) for the IEEE's (Institute for Electrical and

Electronics Engineers) International Test Conference, the largest test conference in the world. These are detailed in my curriculum vitae.

16. In the 1990's, my team represented IBM within the SEMATECH Wafer Probe PTAB (Project Technical Advisory Board). Later, I proposed forming a new wafer group within SEMATECH and when that Wafer Probe Council was founded, I became the first chairman; a post I held until my retirement from IBM. Notable accomplishments by the Probe Council during my tenure were the establishment of semi-annual benchmarking survey on wafer probe practices within the Probe Council's member companies, initiating a wafer probe section within the test chapter of the ITRS (International Technology Roadmap for Semiconductors), development of a wafer probe technology Cost of Ownership model, and the early work on a Wafer Probe Supplier "report card" (to assess wafer probe suppliers' performance on a number of technical and operational parameters).

17. I have been a member of the IEEE, the world's largest technical professional organization, since 1999 and was awarded as a Golden Core member in 2003, and Lifetime Membership in 2023.

18. I retired from full-time work at IBM as of May 2004. From 2004 to the present, I have been working as a test technology consultant, with a focus on Wafer Probing and Socketing projects. I keep up to date on developments in the

field of Wafer Probing due to my work as a test technology consultant. I have served as an expert witness in several patent litigation cases related to wafer probe technology. I was an active test technology consultant both before and at the time the application resulting in the '885 patent was filed.

III. MATERIALS REVIEWED

19. In reaching the conclusions described in this declaration, I have relied on the documents and materials recited herein as well as those identified in this declaration, including the '885 patent, the prosecution history of the '885 patent, the prior art references, and information discussed and any other references specifically identified in this declaration, including the materials identified in the chart below.

Exhibit	Description
Ex. 1001	U.S. Pat. No. 11,035,885 (the "'885 patent")
Ex. 1002	The '885 Patent Prosecution History
Ex. 1003	Declaration of Frederick L. Taber
Ex. 1004	Korea Patent No. 10-1384714 ("Kim KR")
Ex. 1005	Certified English Translation of Kim KR
Ex. 1006	U.S. Pub. No. 2015/0198632 A1 ("Kim")
Ex. 1007	Japanese Patent Pub. No. H11-352182 ("Tezuka")
Ex. 1008	Certified English Translation of Tezuka
Ex. 1009	U.S. Pat. No. 6,417,684 ("Schmid")
Ex. 1010	U.S. Pat. No. 5,225,777 ("Bross")
Ex. 1011	U.S. Pat. No. 9,470,715 ("Fan")
Ex. 1012	U.S. Pub. No. 2014/0197860 ("Hsu")
Ex. 1013	Introduction to Probe Cards, by Rod Schwartz (1998 SWTest Conference)
Ex. 1014	U.S. Pat. No. 4,622,514 ("Lewis")
Ex. 1015	U.S. Pat. No. 10,281,491 ("McQuade")

Ex. 1016	EP3555638A1 Prosecution History
Ex. 1017	Excerpt of JP2019-531897 Prosecution History
Ex. 1018	Certified English Translation of Excerpt of JP2019-531897 Prosecution History
Ex. 1019	Nakamoto Decl ISO Motion for Admission <i>Pro Hac Vice</i>
Ex. 1020	Scheduling Order in <i>Technoprobe S.p.A. v. FormFactor, Inc.</i> , Case No. 1:23-cv-00842-JCG (D. Del.)
Ex. 1021	Patent Owner's Amended Complaint in <i>Technoprobe S.p.A. v. FormFactor, Inc.</i> , Case No. 1:23-cv-00842-JCG (D. Del.)
Ex. 1022	United States District Courts — National Judicial Caseload Profile, <i>available at</i> https://www.uscourts.gov/sites/default/files/fcms_na_distprofile1231.2023_0.pdf (last accessed May 9, 2024)
Ex. 1023	Curriculum Vitae of Frederick L. Taber
Ex. 1024	[Reserved]
Ex. 1025	[Reserved]
Ex. 1026	USPTO Memorandum, Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation (June 21, 2022)
Ex. 1027	Cover Pleading of Patent Owner's Infringement Contentions
Ex. 1028	SWTest Willtechnology Presentation
Ex. 1029	SWTest Willtechnology Presentation – WayBack June 3, 2016
Ex. 1030	SWTest Willtechnology Presentation – WayBack December 6, 2016
Ex. 1031	SWTest Willtechnology Presentation – June 7, 2016 Podium Proceedings

IV. SUMMARY OF OPINIONS

20. Claims 1-2, 4, 8-11 and 14 of the '885 patent are unpatentable as being anticipated by Kim.

21. Claims 1-2, 4, 7-11 and 14 of the '885 patent are unpatentable as obvious in light of Kim.

22. Claims 5-6, 16-20 and 23 are unpatentable as obvious in light of Kim and Schmid.

23. Claim 3 is unpatentable as obvious in light of Kim and Fan.

24. Claims 12 and 13 are unpatentable as obvious in light of Kim and Bross.

25. Claim 15 is unpatentable as obvious in light of Kim and the 2016 SWTest Presentation.

26. Claims 21 and 22 are unpatentable as obvious in light of Kim, Bross and Schmid.

V. UNDERSTANDING OF THE LAW

27. I am not a legal expert. In forming my opinions, I have been informed of and applied the legal standards as follows. I understand that the legal standards relating to anticipation and obviousness apply to the '885 patent based on its effective filing date of June 14, 2019. My opinions herein would not change if the '885 patent were determined to be entitled to claim priority to the filing date of December 11, 2017, February 24, 2017, or December 16, 2016.

28. I understand that a patent claim is invalid if the claimed invention is not new. For a claim to be invalid on the basis of anticipation because it is not new, all of its elements must be present, either expressly or inherently, in a single

previous device or method, or described, either expressly or inherently, in a single previous publication or patent.

29. I understand that the description in a reference does not have to be in the same words as the claim, but all the requirements of the claim must be there, either stated expressly or necessarily implied or inherent to one of ordinary skill in the field of technology of the patent at the time of the invention, so that someone of ordinary skill in the field of technology of the patent looking at that one reference would be able to make and use the claimed invention. I further understand that to be necessarily implied or inherent, the claim element must be a necessary part of the reference that is not expressly disclosed. Merely being one option is not sufficient for a claim element to be necessarily implied or inherent to a person of ordinary skill in the art (“POSA” or “POSITA”).

30. I have been informed that in relying upon the theory of inherency, there must be a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.

31. I have been informed that a patent claim is invalid under 35 U.S.C. § 102(a)(1) if the invention defined by the claim was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.

32. I understand that a U.S. patent constitutes prior art to a claimed invention under 35 U.S.C. § 102(a)(2) if the patent issues from an application that was filed before the effective filing date of the claimed invention.

33. I understand that a patent claim is “obvious” and therefore invalid when the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a POSITA to which the subject matter pertains.

34. In making an obviousness determination, I understand that there are several factors to consider: (1) the scope and content of the prior art; (2) the level of ordinary skill in the art at the time of the effective filing date of the claimed invention; (3) the differences between the claimed invention and the prior art, if any, and (4) objective considerations, if any exist, such as any commercial success, copying, prior failure by others, licenses, longstanding need, and unexpected results.

35. I understand that prior art used to show that a claimed invention is obvious must be “analogous art.” Prior art is analogous art to the claimed invention if (1) it is from the same field of endeavor as the claimed invention (even if it addresses a different problem) or (2) the reference is reasonably pertinent to the problem faced by the inventor (even if it is not from the same field of endeavor as the claimed invention).

36. I have been informed and understand that the U.S. Supreme Court has recognized several rationales for combining references or modifying a reference to show obviousness of claimed subject matter. Some of these rationales include the following: (a) combining prior art elements according to known methods to yield predictable results; (b) simple substitution of one known element for another to obtain predictable results; (c) use of a known technique to improve a similar device (method, or product) in the same way; (d) applying a known technique to a known device (method, or product) ready for improvement to yield predictable results; (e) choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success; and (f) some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention.

37. Also, I have been informed and understand that obviousness does not require physical combination/bodily incorporation, but rather consideration of what the combined teachings would have suggested to a POSITA at the time of the effective filing date of the claimed invention.

38. I understand that it is improper to engage in hindsight when trying to determine the obviousness of a patent claim. I understand that the obviousness inquiry must be conducted from the standpoint of a POSITA at the time of the effective filing date of the claimed invention. What is known today, and what is

learned from the teachings and disclosures of the patent itself containing the claim under analysis, should not be considered.

39. I have been informed that various “secondary considerations” (sometimes referred to as objective indicia of non-obviousness) may support a determination of non-obviousness and that such secondary considerations must be considered as part of an obviousness analysis. I have been informed that secondary considerations of non-obviousness may include:

- commercial success of a product due to the merits of the claimed invention;
- a long felt need for the solution provided by the claimed invention;
- unsuccessful attempts by others to find the solution provided by the claimed invention;
- copying of the claimed invention by others;
- unexpected and superior results from the claimed invention; and
- acceptance by others of the claimed invention as shown by praise from others in the field or from the licensing of the claimed invention.

40. I understand that in order for such “secondary considerations” evidence to be relevant to the obviousness inquiry, there must be a relationship or “nexus” between the advantages and features of the claimed invention and the evidence of secondary considerations.

41. I understand that if a claim is not obvious, then the claims that depend from it are not obvious.

42. I have been advised that in an *inter partes* review the claim terms generally should be given their ordinary and customary meaning as a POSITA would have understood them at the time of the effective filing date of the claimed invention and in light of the patent and its prosecution history. Furthermore, I have been instructed that a claim's plain language can help guide the interpretation of the claim terms in question, and the manner in which a claim term is used in a claim may be informative of its meaning.

43. Further, I have been informed that in an *inter partes* review proceeding, only claim terms that are actually in dispute need be construed. Thus, terms that are not in dispute, or ones for which alternative constructions would not render a different finding, do not need to be construed.

44. I have also been advised that the claim terms being construed must be construed in light of, and consistent with, the intrinsic evidence of the patent. I understand that a patent's intrinsic evidence includes the patent's prosecution history (which includes the prior art considered by the Examiner(s)), the patent's claims, and the patent's written description as given in the specification of the patent.

45. I have also been advised that when the meaning of a patent's claim term is disputed, the specification of the patent itself is the best guide to the meaning of that claim term. I understand that while embodiments given by the specification can help understand the meaning of claim terms, preferred embodiments and other examples given in the specification should not further limit the claims by being read into the claim terms being construed.

46. I also understand that an inventor may act as his or her own lexicographer by specifically defining his or her own terms within the specification such that they then possess a specific meaning that can be different than the meaning they would otherwise have. I also understand that such an inventor can overcome the plain and ordinary meaning of a given claim term if he or she clearly and explicitly defines or redefines a claim term.

47. I have also been advised that after the patent's claims and specification, the next critical source of evidence regarding the meaning of a patent's claim terms comes from the patent's prosecution history. I understand that the prosecution history contains remarks made by the applicant during prosecution of the application that issues as the patent and those remarks may act to define, redefine, disclaim, or limit the meaning of a claim term, and that if a patentee made statements during prosecution that so limits the scope of a claim term, it is

improper for a patent owner to regain the scope given up during prosecution that leads to the issuance of the patent.

48. I have also been advised that in addition to the intrinsic evidence discussed above, extrinsic evidence may also be considered when construing claims, although it is generally not as significant as the intrinsic record itself when understanding the meaning of a claim term. It is my understanding that extrinsic evidence is any relevant evidence that would inform the understanding of the claim terms such as textbooks, dictionaries, expert testimony, treatises, or other like material.

49. I understand that a patent claim must particularly point out and define the boundaries of the subject matter to be protected by that claim. I understand that this requires that a patent claim be sufficiently definite. I understand that a patent claim is indefinite, and thus invalid, if its claims, when read in light of the intrinsic record, fail to inform a POSITA with reasonable certainty about the scope of the invention.

VI. LEVEL OF ORDINARY SKILL IN THE ART

50. In rendering the opinions set forth in this declaration, I was asked to consider the patent claims and the prior art through the eyes of a POSITA (or POSA) at the time of the effective filing date of the claimed invention, which I understand is potentially as early as December 16, 2016 (the earliest priority date

identified on the face of the '885 patent). I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field; the teachings of the prior art, and the sophistication of the technology at the time of the effective filing date of the claimed invention. I understand that a POSITA is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a POSITA would also have knowledge from the teachings of the prior art, including the art cited below.

51. Based on the technologies disclosed in the '885 patent, I believe that a POSITA would include someone with a minimum education level of Bachelor of Science degree in the sciences applicable to wafer probing technology and 3-5 years of experience in designing and/or using probe technologies, or the equivalent in training and work experience. Degrees applicable to wafer probing may include Electrical Engineering, Mechanical Engineering, and Materials Engineering. Additional graduate education could substitute for professional experience, and significant work experience could substitute for formal education. The POSITA would have been familiar with and up to date on semiconductor device probing technology, including vertically oriented buckling beam probing and understand the issues described in the Background

of the Invention section of the '885 patent. The POSITA would understand and be able to implement the various techniques that had been used to probe semiconductor devices. And the POSITA would understand the tradeoffs associated with the various techniques as described in the relevant literature.

52. Specific to the asserted '885 patent, without limiting the overall skills previously noted, a POSITA would be knowledgeable about the design, materials and function of a probe card's components: buckling beam type (such as COBRA style) and Spring Probe (such as Pogo™) contact elements, upper and lower guide plates, intermediate guide plate(s), space transformers and probe card printed circuit boards (PCB). With regard to space transformers and printed circuit boards, a POSITA would be familiar with the design of the metallization used in those components and the application and use of circuit devices (capacitors, etc.) with those components.

53. Well before December 16, 2016, which is the earliest priority date of the '885 patent that Patent Owner claimed, my level of skill in the art was at least that of a POSITA. I am qualified to provide opinions concerning what a POSITA would have known and understood at the time of the effective filing date of the claimed invention, and my analysis and conclusions herein are from the perspective of a POSITA as of that date.

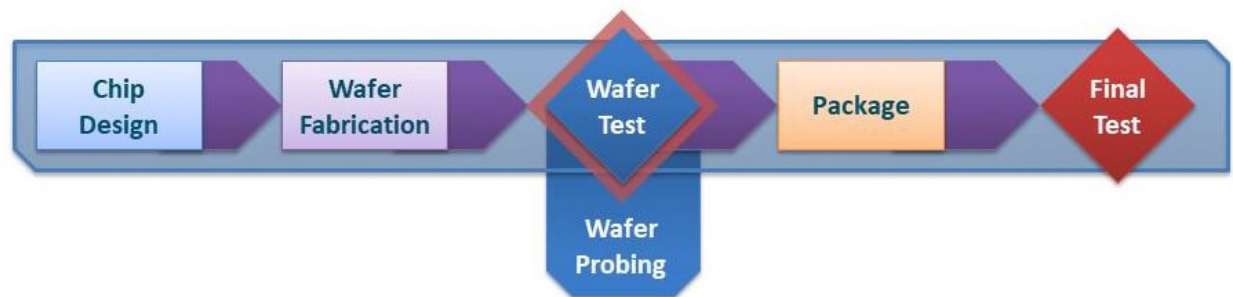
VII. BACKGROUND ON THE STATE OF THE ART

A. Wafer Test

54. Driven by semiconductors, electronics are pervasive in our lives.

Mobile phones, laptops, automobiles, household appliances, and other devices too numerous to mention, all rely on semiconductors to function.

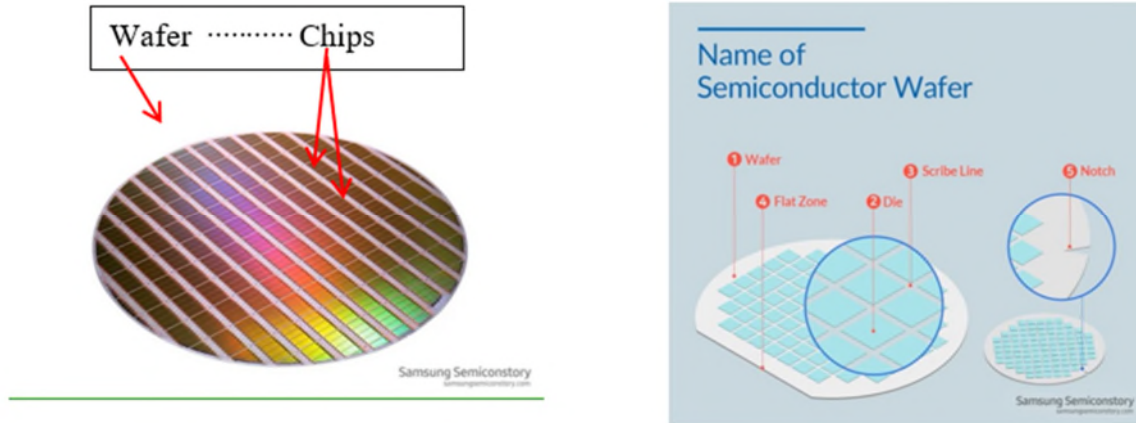
Overview of the Semiconductor Process Flow



55. After a chip is designed, it is then fabricated. Semiconductors are produced on a thin, round disk called a wafer. The wafer is typically made of silicon, though other materials are also used for special applications. Through a series of complex processes, a grid-like array of semiconductor devices, commonly called chips, die or integrated circuits (IC), is produced (referred to as being “fabbed”). Each chip may contain thousands of transistors and other electronic

components. Typically, every chip on a wafer is of the same design (function).

The illustrations below are from (2/2024):¹



56. Over the years, to increase productivity and to lower costs, the maximum wafer diameter has increased (more chips per wafer), yet smaller sizes remain in use. Today, a 300mm wafer is the largest size in regular production.

57. Additionally, increasing miniaturization, at a rate predicted by Moore's law,² has increased the density of transistors on a chip, along with higher

¹ <https://semiconductor.samsung.com/support/tools-resources/fabrication-process/eight-essential-semiconductor-fabrication-processes-part-1-what-is-a-wafer/> (annotated).

² Moore's law, named after technologist Gordon Moore from Intel, states that the number of transistors in a dense integrated circuit doubles approximately every two

operational performance, greater power requirements and copious growth in the number of transistors on a chip. These factors consequently result in not only an increased number of input and output (“I/Os”) electrical contact points for signals, power and ground, but much tighter spacing between the I/Os. These electrical contact points are where the chip electrically connects to external devices.

Typically, the contact points are presented as bond pads (to which a tiny wire can be bonded) or a solder connection (where a soldered connection can be made).

Wafer test systems, including probe cards, have had to evolve to address wafer size and the effects of miniaturization.

58. Each chip on a wafer is separated from adjacent chips by a kerf (or scribe line). During the fab process, a type of probe card may be used to test within the kerf to verify that certain in-process parameters are within specification. However, this declaration will discuss probe cards later, focusing on their use once a wafer has finished being fabricated.

59. Once the fab process is completed, the wafer(s) is/are tested – this is called wafer test, wafer probe or sometimes just ‘sort’ – sorting “good” chips from “bad” ones. Chips being tested are often called the Device Under Test (“DUT”).

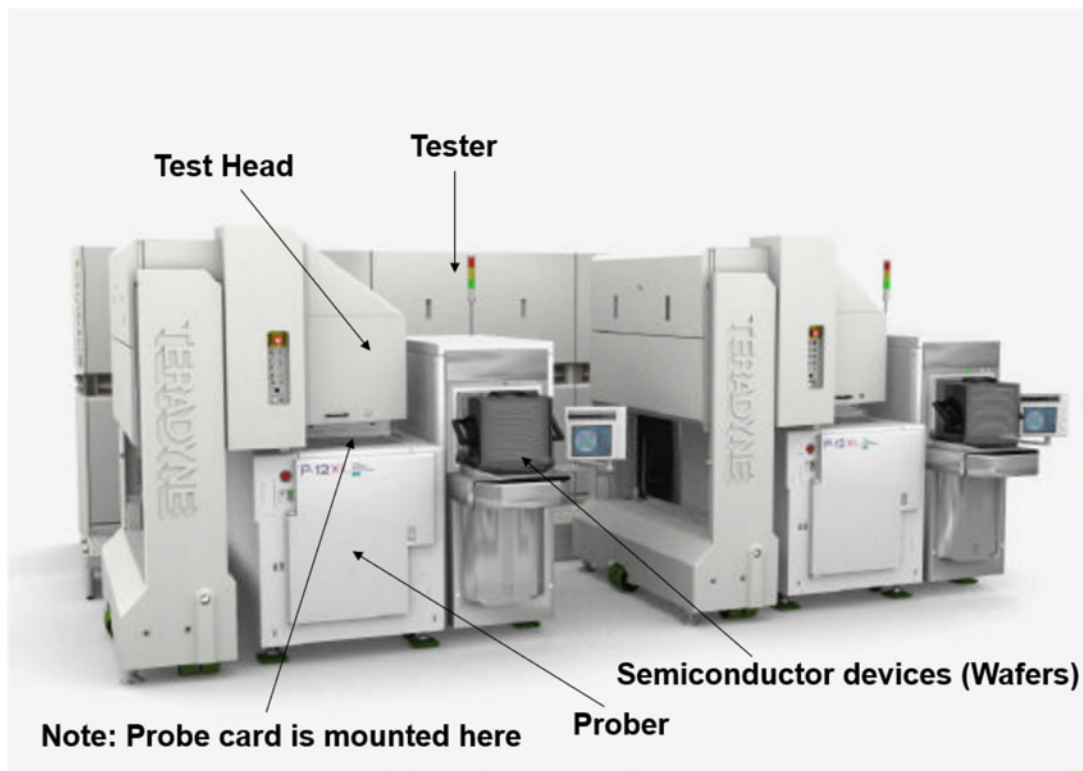
years (<https://www.intel.com/content/www/us/en/newsroom/resources/moores-law.html#gs.6jy9p9>).

Testing identifies defects and confirms functionality before further manufacturing steps. At wafer test, a computer driven wafer test system performs a number of functions to mechanically connect to the wafer, and temporarily electrically connect the tester to all the chips on the wafer (either individually – one at a time, a subset – a group at a time, or the complete wafer - all at once). The handler aligns and positions the wafer under the wafer probe and raises the wafer up to contact the wafer probe, then testing is conducted. If testing chips individually or a subset, the handler “steps” the wafer to position each chip(s) under the wafer probe, then raises the wafer up to have the chip(s) contact the wafer probe for testing. This process is repeated until all of the chips are tested. Once the wafer probe has engaged the chip(s), the tester then applies power and stimuli (test patterns within a test program) and checks that the expected response is produced to each stimulus. Under such process, failing chips are identified.

60. As illustrated below,³ a wafer test system typically comprises several sub-system components including a tester (also known as Automatic Test Equipment – ATE), which is source for power and stimuli and captures responses to stimuli based on test programs which are unique to each chip design; a test head

³ <https://vtechworks.lib.vt.edu/server/api/core/bitstreams/0d386684-4eed-4123-b834-bb0fe6db5f09/content>

which is an electrical and mechanical interface between the tester and the probe card; a prober and a wafer handler which load and handle the wafer, and mount the wafer on a wafer chuck and precisely positions each chip below the probe contact elements. To conduct a test, the chuck is raised a precise amount (Z-direction) so that the chip I/Os are contacted by the probe contact elements.



61. In a subsequent process, the wafers are diced. This separates the individual chips on the wafer from each other. The “good” chips then are packaged (integrated into a larger assembly) and are then run through a final test after (for some types of chips) a process called “burn-in” is performed to accelerate the appearance of latent failures in the chip before final test is performed.

B. Probe Card

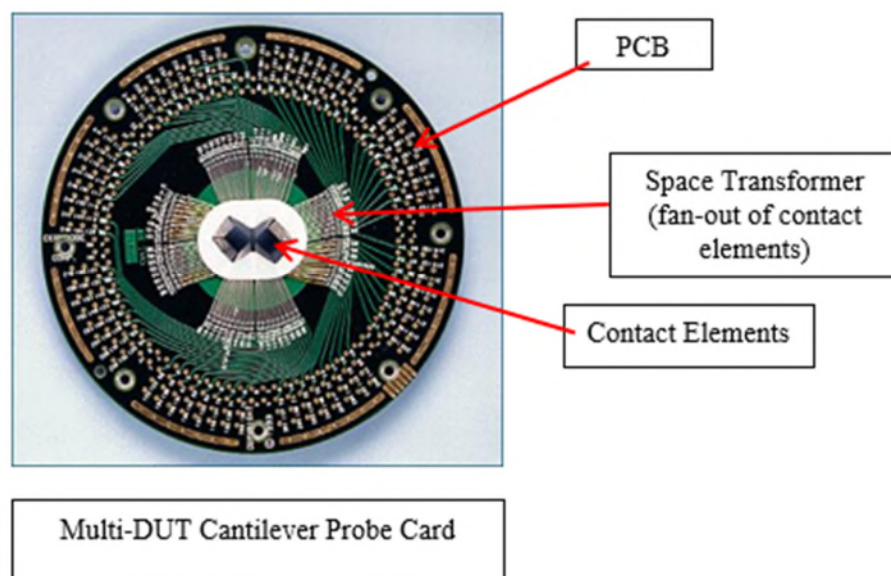
62. A probe card provides a temporary electrical interface between the test head and the chip(s) being tested, so it completes the electrical path to the chip from/to the tester, through the test head. A probe card may also have features to improve power and signal integrity; or other circuitry and devices necessary to perform the required tests.

63. Within the overall architecture of a given probe card model, the specific design parameters (*e.g.*, number and location of I/Os, signal and power routing, loop-back circuits, etc.) is usually unique to a particular chip design. So, probe cards are swapped out as wafers with a different chip design are to be tested.

64. Probe cards are comprised of a probe head housing the contact elements, a space transformation means (either a discrete space transformer component or through a fan-out of the contact elements) and a printed circuit board (*i.e.*, PCB). Sometimes there is an interposer between the probe head and a discrete space transformer component to facilitate planarization (assuring the plane of the contact elements is parallel to the plane of the chip I/Os. Rigid framework around the probe card is aimed at minimizing deflections that would affect planarity due to the forces encountered when contacting a chip.

65. Probe cards have been in use since at least the 1960s. They can be grouped into families characterized by the direction that the contact elements contact the chip I/Os: cantilever – sometime called needle (horizontal) and vertical.

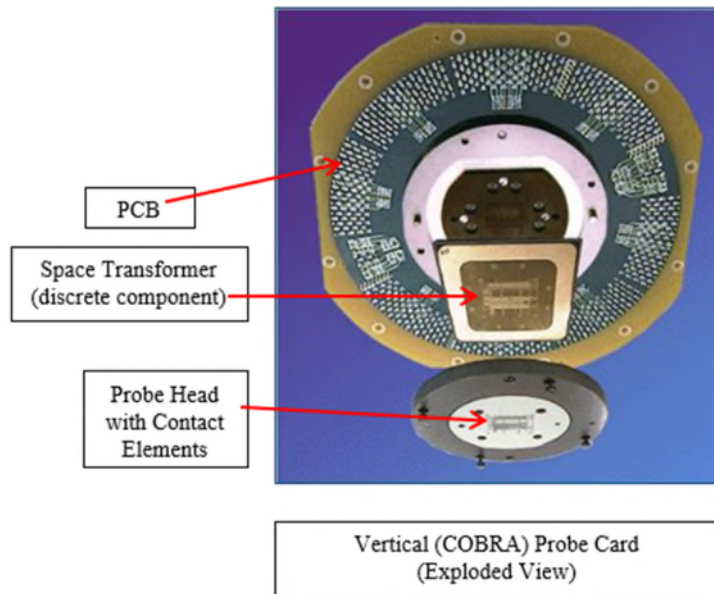
66. In the cantilever family, it is often limited to probing chips with I/Os on/near the perimeter of a chip or a simple linear arrangement. Cantilever probes are typically used for testing chips that have bond pad I/Os. A cantilever probe card is illustrated in the following figure.⁴



67. One type of commonly used vertical probing technology is buckling beam. When the handler raises the chips into contact with the contact elements, the tiny probe wires “buckle”. Vertical probes can contact I/Os anywhere on the

⁴ Ex. 1013, 29. Captions: F. Taber.

chip, and those I/Os can be bond pads or solder bumps/columns. A vertical probe card is illustrated in the following figure.⁵



68. The '885 patent identifies the contact elements (21', 21'' and 21''') as buckling beam contact elements. Ex, 1001, 11:63-66, 14:17-19.

C. Printed Circuit Board (PCB)

69. The PCB (Printed Circuit Board) is a multilayer circuit board where the space transformer (discussed below) is installed on one side and the other side has contacting points or connectors where the PCB electrically interfaces with the test head. A metal stiffener surrounds the PCB to aid in assuring planarity. The

⁵ Ex. 1013, 38. Captions: F. Taber.

PCB routes signals and power/ground between the test head side and the space transformer side. It may also include some circuitry and/or electrical components.

D. Space Transformer

70. The I/Os on a chip are very densely arranged at very small dimensions. To contact the chip, the probe head's configuration/layout of contact elements must be exactly the same pattern and spacing dimensions of the chip I/Os. While one side of the contact elements make contact with the chip, the other side makes contact with the space transformer. Thus, the space transformer of a probe card is the electrical interface between the probe head and the PCB (or sometimes to an interposer). It makes interconnections from one pitch to another pitch, by taking the tightly spaced contacts on its probe head side and electrically routing them to the PCB side at a looser spacing.

E. Guide Plate(s) and Guide Holes

71. Guide plates are used in vertical probes, such as the buckling beam type probe in the '885 patent. They are part of the probe head assembly and are used to contain and align the buckling beam contact elements. There are typically two guide plates: an upper guide plate on the space transformer side and a lower guide on the chip (DUT) side. Intermediate guide plate(s), located between the upper and lower guide plates, may also be used, for example, to bias the buckling beam probe in a desired buckling direction.

72. Guide plates contain guide holes where the contact elements, like the buckling beam type wire-shaped elements (*see* '885 patent illustrated in Fig. 2A) and the spring probes (*see* '885 patent illustrated in Fig. 7), pass through. Guide plates are an essential part of buckling beam type probes and spring probes. The guide holes are typically circular or square in cross-section, but other shapes are used. Guide holes have a diameter/side dimension that is slightly larger than that of the probe wire portion that passes through it. The tip portion and the head portion of a probe may differ in cross-section and/or size.

F. Contact Elements

73. Contact elements are also called the probes. They are the part of the probe head portion of the probe card. They physically and electrically contact the pads or solder bumps on the chip(s) being tested. Contact elements exhibit a spring-like behavior (they are compliant) and are good conductors of electricity. The contact elements are arranged within the probe head so that their tips are positioned precisely to match the I/O positions and layout of the chip being tested.

74. As the chuck on the wafer prober is raised, the contact elements first just touch the chip I/Os then the wafer is raised further to a prescribed amount of over-travel that assures good electrical contact between the chip I/Os and the contact elements. Thus, elasticity (compliance) of the contact elements is an essential characteristic.

G. Ground and Power Planes

75. The use of power and ground planes is well known in the electronics art. The large area of metal in power/ground planes, distributes power/ground over a wide area and conducts a large amount of current. The planes contribute to assuring the proper voltage is maintained while testing a chip.

76. To conduct tests on a chip, electrical power for the chip is provided from the test system through the test head, then on to the probe card, and finally to the chip. Each of these utilizes power and ground planes to distribute power and ground as needed. Some chip designs may contain thousands of contact elements carrying power and ground signals.

77. The probe card's PCB is produced using well known printed circuit board technology. It is typically comprised of multiple laminated layers. Some of these layers, including the surface layers, contain thin sheets of metal (typically copper). Through surface vias (contacting points) where the PCB interfaces with the test head, certain layers with metal sheets are connected to the test system's ground point (the return path for current), while others are connected to the test system's power supply/supplies. The power and ground planes also connect to surface vias on the space transformer side of the PCB. Thus, all vias for ground are electrically common, and those for power are also common to each other. Vias

that are neither power nor ground (signals or unused) are isolated from the power/ground planes.

78. If a chip requires more than one power level, there are separate power planes for each voltage level. A layer may be divided into sections, to split a given power or ground into multiple regions or include a mix of power and ground regions.

79. In a similar fashion, the space transformer comprises multiple layers, some of which are power or ground planes. Those power/ground planes connect to vias on each surface: upper surface to the PCB, lower surface to the probe head's contact elements.

H. Signal Input/Output (I/Os)

80. While the power and ground I/Os on a chip provide the power for the chip, the signal I/Os are the communication pathway for data to/from the chip. I/Os may be an input, an output or bi-directional. Through "instructions" from the test program, the tester stimulates the input signal I/Os and records the response from the output I/Os (bi-directional I/Os perform either function as required by the test). Signal I/Os may be digital or analog; sometimes there is a mix of both on a chip. For large, complex chips, the number of power and ground I/Os is far more than the number of signal I/Os. Typically, signal I/Os operate individually, so two or more are not connected together, however there may be instances otherwise.

81. Signal I/Os are routed from the vias on the probe head side of the space transformer through internal and/or external traces to vias on the PCB side of the space transformer. In a similar manner signal I/Os are routed from one side of the PCB to the other where they interface with the test head.

VIII. OVERVIEW OF THE '885 PATENT

A. Brief Description

82. The '885 patent is titled "Testing head having improved frequency properties." Ex. 1001, Cover. The '885 patent relates to the testing heads used to electrically test the devices that are integrated on a wafer before cutting and assembling them inside a chip containing package. *Id.*, 1:26-32.

83. The '885 patent explains that the good connection between the contact probes and the contact pads of the device under test is guaranteed by pressing the testing head on the device itself, the contact probes undergoing a bending inside the air gap between the guides and a sliding within the respective guide holes during that pressing contact. *Id.*, 1:46-52. And the testing heads of this kind are usually called "vertical probe head." *Id.*

84. Figure 1 of the '885 patent, labeled "PRIOR ART," illustrates a conventional vertical testing head structure. *Id.*, 1:58-64, Fig. 1.

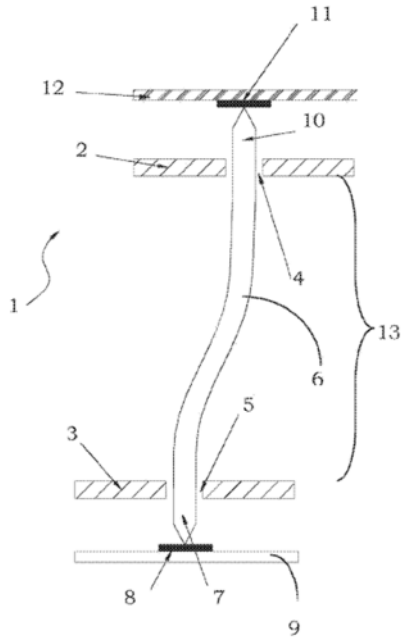


FIG. 1
PRIOR ART

85. As shown in Fig. 1, the testing head (1) comprises an upper guide (2) and a lower guide (3) separated by a gap (13). *Id.*, 1:58-61. The '885 patent explains that the guides (3, 4) have respective guide holes (4 and 5) in which a plurality of contact probes (6) slides. *Id.*, 1:61-62. The '885 patent goes on to explain that each contact probe (6) terminates at an end with a contact tip (7) apt to abut onto a contact pad (8) of a device under test integrated on a wafer (9), in order to carry out the mechanical and electrical contact between the device under test and a test equipment. *Id.*, 1:65-2:3.

86. The '885 patent further states that inside a testing head the contact elements comprise contact elements carrying power and ground signals, and

contact elements carrying operating signals (*i.e.*, input/output signals) between the test equipment and the device under test. *Id.*, 2:37-42. According to the '885 patent, the presence of contact elements carrying ground and power signals creates interferences which cause noise in the input/output signals used for the test of the device under test and such interferences limit the frequency performance of the testing head. *Id.*, 2:43-51.

87. In order to improve the frequency performance of a testing head, the '885 patent teaches a conductive portion connecting metalized guide holes of the guide in which the contact elements carrying a same type of signal can be electrically connected. *Id.*, 3:34-38. In addition, as the ground and power signals have higher current value than the input/output signals, the '885 patent teaches that it is preferable to use the two separate conductive portions connecting metalized guide holes, which are physically and electrically separated from each other, to electrically connect the group of contact elements carrying ground signals and the group of contact elements carrying power signals, respectively. *Id.*, 4:28-54.

According to the '885 patent, short-circuiting the ground contact elements and separately short-circuiting the power contact elements also avoids possible burning of the contact elements. *Id.*, 18:1-4.

B. Prosecution History

1. U.S.

88. The application leading to the '885 patent was filed on June 14, 2019 as U.S. Pat. App. 16/442,385 (“the '385 Application”) which is a continuation-in-part of international patent application No. PCT/EP2017/082180, filed on December 11, 2017 (“the '180 Application”). The '180 Application claimed priority to two Italian patent applications filed on December 16, 2016, and February 24, 2017, respectively. *Id.*, cover.

89. During prosecution of the '385 Application, the Applicant submitted an information disclosure statement identifying a list of prior art references including Korean Patent Publication No. 101421051 (the “'051 Reference”). Ex.1002, 414-422. The '051 Reference was considered but not cited by the Examiner in any office action rejecting the '385 Application.

90. Original claim 1 of the '385 Application read as follows: “A testing head apt to verify the operation of a device under test integrated on a semiconductor wafer comprises: a plurality of contact elements, each comprising a body that extends between a first end portion and a second end portion, and at least one guide provided with a plurality of guide holes apt to house the contact elements, wherein the at least one guide comprises a first conductive portion that includes and electrically connects a first group of guide holes, of the plurality of

guide holes, to each other and is apt to contact corresponding first contact elements, of the plurality of contact elements, apt to carry a first type of signal.” *Id.*, 395.

91. In a non-final office action dated November 4, 2020, the Examiner rejected claims 1-3, 9-14, 16-18, and 22-25 of the '385 Application as anticipated by reference U.S. 2008/0139017 A1 (“Kiyofuji”). *Id.*, 58-63. The Examiner also indicated that certain claims had allowable subject matter. *Id.*, 63-65.

92. In a response dated February 4, 2021, Technoprobe amended the claims to incorporate limitations from the claims that had allowable subject matter into other claims.

93. Technoprobe amended original independent claim 1 by incorporating features of allowable claim 4: “a second conductive portion that includes and electrically connects the holes of a second group of the guide holes to each other, the second group housing second contact elements of the plurality of contact elements, the second contact elements being configured to carry a second type of signal, the first and second types of signals chosen between ground signals and power signals.” *Id.*, 44.

94. Technoprobe amended original independent claim 17 by incorporating features of allowable claim 19: “a lower guide, an intermediate guide, and an upper guide, the lower guide and the intermediate guide being separated from

each other by a first gap, the intermediate guide and the upper guide being separated from each other by a second gap, each of the lower, intermediate and upper guides comprising respective guide holes for housing the contact elements, the first and second conductive portions being formed on respective faces of the upper, intermediate and lower guides.” *Id.*, 47.

95. Technoprobe rewrote allowable claim 20 in independent form including all limitations of original independent claim 17 and original claim 20: “A testing head configured to verify the operation of a device under test integrated on a semiconductor wafer, the testing head comprising:

a plurality of contact elements, each comprising a body that extends between a first end portion and a second end portion; and

at least one guide provided with a plurality of guide holes configured to house the contact elements,

wherein the at least one guide comprises:

a first conductive portion including and electrically connecting holes of a first group of the guide holes to each other, the first group housing first contact elements;

a second conductive portion including and electrically connecting holes of a second group of the guide holes to each other, the second group housing second contact elements, the first and second contact elements being

configured to carry respective same type of signal chosen between ground signals and power signals, and

a lower guide, an intermediate guide and an upper guide, the lower guide and the intermediate guide being separated from each other by a first gap, the intermediate guide and the upper guide being separated from each other by a second gap, each of the lower, intermediate and upper guides comprising respective guide holes for the housing the contact elements, the first and second conductive portions being formed on a same face of one of the upper, intermediate and lower guides and being physically and electrically separated from each other by at least one non-conductive zone.”

Id., 48.

96. The Examiner subsequently issued a notice of allowability, and the ’885 patent issued thereafter.

97. The prosecution history is notable in connection with my analysis, because it reflects the claim limitations that were viewed by the Examiner as being important to the allowance of the ’885 patent’s claims over the prior art of record.

2. Europe

98. The European counterpart patent application No. EP3555638A1 (“the ’638 Application”), which was filed on December 11, 2017, is still pending before the European Patent Office (“EPO”).

99. The original claim 1 of the '638 Application read as follows (Ex. 1016, 61):

1. A testing head (20) adapted to verify the operation of a device under test integrated on a semiconductor wafer, said testing head (20) comprising at least one guide (40, 41, 42) provided with a plurality of
5 guide holes (40h, 41h, 42h) adapted to house a plurality of contact elements (21', 21'', 21'''), each of said contact elements (21', 21'', 21''') comprising a body (21pr, 21pp) that extends between a first end portion (24) and a second end portion (25), said testing head (20) being characterized in that said at least one guide (40, 41, 42) comprises at
10 least one conductive portion (30', 30'', 30''') that includes and electrically connects the holes of at least one group (40', 40''; 40''' ; 41'; 41''; 41''' ; 42', 42'', 42''') of said guide holes (40h, 41h, 42h) to each other and is apt to contact a corresponding group of said contact elements (21', 21'', 21'''), said contact elements (21', 21'', 21''') of said
15 corresponding group being adapted to carry a same type of signal.

100. Original claim 1 of the '638 Application is in substance very similar if not identical to original claim 1 of the '385 Application.

101. During prosecution of the '638 Application, the Examiner of the EPO rejected the '638 Application based on a number of prior art references including the '051 Reference and Kim. Ex.1016, 446-47.

102. In a Written Opinion of the International Preliminary Examining Authority dated April 16, 2018, the '638 Application claims were found to be lacking either novelty or inventive step in view of four references, one of which was the '051 Reference; in particular, pending claim 1 was lacking novelty over the '051 Reference. *Id.*, 87-88.

103. Thereafter, in an amendment dated October 11, 2018, Technoprobe amended the pending application claims, including making the following amendments to claim 1:

1. A testing head (20) adapted to verify the operation of a device under test integrated on a semiconductor wafer, said testing head (20) comprising at least one guide (40, 41, 42) provided with a plurality of guide holes (40h, 41h, 42h), ~~adapted to house~~and a plurality of contact elements (21', 21'', 21''') housed in said guide holes (40h, 41h, 42h), each of said contact elements (21', 21'', 21''') comprising a body (21pr, 21pp) that extends between a first end portion (24) and a second end portion (25), said testing head (20) being characterized in that said at least one guide (40, 41, 42) comprises at least one first conductive portion (30', 30'', 30''') that includes ~~and electrically connects the holes~~ of at least one first group (40', 40'', 40'''; 41', 41'', 41'''; 42', 42'', 42''') of said guide holes (40h, 41h, 42h) and electrically connects to each other and is apt to contact a corresponding first group of said contact elements (21', 21'', 21''') housed in said at least one first group (40', 41', 42') of said guide holes (40h, 41h, 42h), and at least one second conductive portion (30'') that includes the holes of at least one second group (40'', 41'', 42'') of said guide holes (40h, 41h, 42h) and electrically connects a corresponding second group of said contact elements (21'') housed in said at least one second group (40'', 41'', 42'') of said guide holes (40h, 41h, 42h), wherein ~~thesaid~~ contact elements (21', 21'', 21''') of a same~~said~~ corresponding group are~~being~~ adapted to carry a same type of signal, and wherein the contact elements of different groups are adapted to carry different types of respective signals.

104. The '638 Application claim 1, as amended, is in substance very similar to issued claim 1 of the '885 patent, as shown below (the order of the '638 Application claim 1 is rearranged to match the order of the '885 patent claim 1). The last element of the '638 Application claim 1 differs slightly in that it just says

the different contact element groups carry different types of signals, rather than specifying that those different types are ground and power:

Claims 1 of the '885 Patent	The '638 Application claim 1 as of October 11, 2018
A testing head configured to verify the operation of a device under test integrated on a semiconductor wafer, the testing head comprising:	A testing head (20) adapted to verify the operation of a device under test integrated on a semiconductor wafer, said testing head (20) comprising:
a plurality of contact elements, each comprising a body that extends between a first end portion and a second end portion, and	each of said contact elements (21', 21'', 21''') comprising a body (21pr, 21pp) that extends between a first end portion (24) and a second end portion (25).
at least one guide provided with a plurality of guide holes configured to house the contact elements,	at least one guide (40, 41, 42) provided with a plurality of guide holes (40h, 41h, 42h) and a plurality of contact elements (21', 21'', 21''') housed in said guide holes (40h, 41h, 42h)
wherein the at least one guide comprises: a first conductive portion that includes and electrically connects a first group of guide holes, of the plurality of guide holes, to each other and is configured to contact corresponding first contact elements, of the plurality of contact elements, configured to carry a first type of signal; and	said testing head (20) being characterized in that said at least one guide (40, 41, 42) comprises at least one first conductive portion (30') that includes the holes of at least one first group (40', 41', 42') of said guide holes (40h, 41h, 42h) and electrically connects a first group of said contact elements (21') housed in at least one first group (40', 41', 42') of said guide holes (40h, 41h, 42h) ... wherein the contact elements of a same group are adapted to carry a same type of signal
[1d] a second conductive portion that includes and electrically connects the holes of a second group of the guide holes to each other, the second group housing second contact elements of the plurality of contact elements, the second contact elements being configured to carry a second type of signal	and at least one second conductive portion (30'') that includes the holes of at least one second group (40'', 41'', 42'') of said guide holes (40h, 41h, 42h) and electrically connects a second group of said contact elements (21'') housed in at least one second group (40'', 41'', 42'') of said guide holes (40h, 41h, 42h),

	wherein the contact elements of a same group are adapted to carry a same type of signal
[1e] the first and second types of signals chosen between ground signals and power signals.	and wherein the contact elements of different groups are adapted to carry different types of respective signals.

105. On December 21, 2018, a Written Opinion of the International Preliminary Examining Authority issued. The Opinion found that the pending claims of the '638 Application lacked an inventive step, citing the '051 Reference which was “considered at present as the closest prior art.” *Id.*, 324.

106. Similarly, a March 22, 2019 International Preliminary Report on Patentability found that the pending claims of the '638 Application lacked an inventive step, citing the '051 Reference which was “considered at present as the closest prior art.” *Id.*, 332.

107. In a response dated January 20, 2020, Technoprobe amended the claims again, with the amendment to pending claim 1 shown below. As shown, this amendment specified that the two types of signal are ground and power, as in the '885 patent claim 1:

1. A testing head (20) adapted to verify the operation of a device under test integrated on a semiconductor wafer, said testing head (20) comprising at least one guide (40, 41,~~42~~) provided with a plurality of
5 guide holes (40h, 41h,~~42h~~), and a plurality of contact elements (21', 21'', 21''') housed in said guide holes (40h, 41h,~~42h~~), each of said contact elements (21', 21'', 21''') comprising a body (21pr, 21pp) that extends between a first end portion (24) and a second end portion (25),
~~said testing head (20) being characterized in that~~ wherein said at least
10 one guide (40, 41,~~42~~) comprises at least one first conductive portion (30') that includes the holes of at least one first group (40', 41',~~42'~~) of said guide holes (40h, 41h,~~42h~~) and electrically connects a corresponding first group of said contact elements (21') housed in said at least one first group (40', 41',~~42'~~) of said guide holes (40h, 41h,~~42h~~),
15 and at least one second conductive portion (30'') that includes the holes of at least one second group (40'', 41'',~~42''~~) of said guide holes (40h, 41h,~~42h~~) and electrically connects a corresponding second group of said contact elements (21'') housed in said at least one second group (40'', 41'',~~42''~~) of said guide holes (40h, 41h,~~42h~~), wherein the contact
20 elements of a same group are adapted to carry a same type of signal, ~~and~~ wherein the contact elements of different groups are adapted to carry different types of respective signals, and

2. ~~The testing head (20) according to claim 1, characterized in that~~
wherein said first contact elements (21') housed in said first group (40',
25 41',~~42'~~) of said guide holes (40h, 41h,~~42h~~) are adapted to carry ground signals, and said second contact elements (21'') housed in said second group (40'', 41'',~~42''~~) of said guide holes (40h, 41h,~~42h~~) are adapted to carry power signals, and wherein said guide including the conductive portions (30', 30'') is a lower guide (40) or an intermediate guide (41) of
30 the testing head (20).

Id., 389.

108. Accompanying the amendment, Technoprobe argued that “the conductive layer of D2 [the '051 Reference] connects to each other only ground

probes while the power probes are not connected to each other” (emphasis in original).

109. After that, in a communication from the Examining Division dated May 20, 2021, the EPO rejected the subject matter of the '638 Application claim 1 as lacking an inventive step in view of the '051 Reference, and the subject matter of the remaining pending application claims as lacking an inventive step in view of the '051 Reference and other cited prior art.

110. In a response dated September 20, 2021, Technoprobe further amended the claims, including making the following amendments to claim 1:

1. A testing head (20) adapted to verify the operation of a device under test integrated on a semiconductor wafer, said testing head (20) comprising at least one guide (40, 41) provided with a plurality of guide
5 holes (40h, 41h), and a plurality of contact elements (21', 21'', 21''') housed in said guide holes (40h, 41h), each of said contact elements (21', 21'', 21''') comprising a body (21pr, 21pp) that extends between a first end portion (24) and a second end portion (25), wherein said at least one guide (40, 41) comprises at least one first conductive portion (30') that includes
10 the holes of at least one first group (40', 41') of said guide holes (40h, 41h) and electrically connects a corresponding first group of said contact elements (21') housed in said at least one first group (40', 41') of said guide holes (40h, 41h), and at least one second conductive portion (30'') that includes the holes of at least one second group (40'', 41'') of said
15 guide holes (40h, 41h) and electrically connects a corresponding second group of said contact elements (21'') housed in said at least one second group (40'', 41'') of said guide holes (40h, 41h), wherein the contact elements of a same group are adapted to carry a same type of signal, wherein the contact elements of different groups are adapted to carry
20 different types of respective signals, and wherein said first contact elements (21') housed in said first group (40', 41') of said guide holes (40h, 41h) are configured adapted to receive and carry only ground signals, and said second contact elements (21'') housed in said second group (40'', 41'') of said guide holes (40h, 41h) are configured adapted to receive and carry
25 only power signals, and wherein said guide including the conductive portions (30', 30'') is a lower guide (40) or an intermediate guide (41) of the testing head (20) when testing the device under test integrated on the semiconductor wafer.

Id., 433.

111. To distinguish the claimed invention of the '638 Application from the '051 Reference (*i.e.*, D2), Technoprobe argued that the “conductive layer” of the '051 Reference “connects to each other only ground probes, while the power probes are not connected to each other and are surrounded by the short-circuited

ground probes.” *Id.*, 424. Technoprobe further argued that “[t]he amendments introduced into claim 1 make clear that the probes of the first group carry ground signals only and the probes of the second group carry power signals only, so that these groups carry different types of respective signals.” *Id.* Technoprobe argued that the ’051 Reference “does not even suggest that the power probes could be connected to each other” and in fact “teaches away” from that arrangement.

112. After that, in an office action dated April 17, 2023, the EPO rejected the pending claims based on Kim. The EPO said that “D5 [Kim] is a similar document as D2 [the ’051 Reference] but provides some more details on the grouping of probes.” *Id.*, 446. The EPO noted specifically that Kim discloses “at least one second conductive portion that includes the holes of at least one second group of said guide holes and electrically connects a corresponding second group of said contact elements housed in said at least one second group of said guide holes (the power P) wherein the contact elements of a same group are adapted to carry a same type of signal.” *Id.*, 447. The EPO found that “[i]t appears therefore that the subject-matter of claim 1 is not new in view of D5.” *Id.*

113. Of note, the EPO also disagreed with Technoprobe’s arguments about the claims having an inventive step over the ’051 Reference. *Id.*, 447-48. And the EPO further maintained that the other pending application claims lacked novelty or inventive step. *Id.*, 449. It’s also notable that the EPO observed that “testing head

having more than two guides for vertical probes are well known to the skilled person” and positioning the conductive layer on an intermediate guide “is a mere obvious constructional detail for the skilled person.” *Id.*, 447.

114. In a response dated August 10, 2023, in an attempt to distinguish the claimed invention of the '638 Application from Kim (*i.e.*, D5), Technoprobe amended its pending claims including the following amendment to claim 1:

1. A testing head (20) adapted to verify the operation of a device under test integrated on a semiconductor wafer, said testing head (20) comprising at least one guide (40, 41) provided with a plurality of guide
5 holes (40h, 41h), and a plurality of contact elements (21', 21'', 21''') housed in said guide holes (40h, 41h), each of said contact elements (21', 21'', 21''') comprising a body (21pr, 21pp) that extends between a first end portion (24) and a second end portion (25), wherein said at least one guide (40, 41) comprises at least one first conductive portion (30') that includes
10 the holes of at least one first group (40', 41') of said guide holes (40h, 41h) and electrically connects a corresponding first group of said contact elements (21') housed in said at least one first group (40', 41') of said guide holes (40h, 41h), and at least one second conductive portion (30'') that includes the holes of at least one second group (40'', 41'') of said
15 guide holes (40h, 41h) and electrically connects a corresponding second group of said contact elements (21'') housed in said at least one second group (40'', 41'') of said guide holes (40h, 41h), wherein the contact elements of a same group are adapted to carry a same type of signal, wherein the contact elements of different groups are adapted to carry
20 different types of respective signals, and wherein said first contact elements (21') housed in said first group (40', 41') of said guide holes (40h, 41h) are configured to receive and carry only ground signals, and said second contact elements (21'') housed in said second group (40'', 41'') of said guide holes (40h, 41h) are configured to receive and carry only power
25 signals, and wherein said guide including the conductive portions (30', 30'') is a lower guide (40) or an intermediate guide (41) of the testing head (20) when testing the device under test integrated on the semiconductor wafer wherein the first conductive portion (30') and the second conductive portion (30'') are formed on a same face (FA) of the at least one guide (40) and are physically and electrically separated from each other by at least
30 one non-conductive zone (31, 31', 31'').

Id., 462.

115. Technoprobe argued that cited references including the Kim “do not disclose nor suggest that ‘the first conductive portion and the second conductive portion are formed on a same face the at least one guide and are physically and

electrically separated from each other by at least one non-conductive zone’, as now claimed in amended claim 1.” *Id.*, 454. Technoprobe specifically admitted that the Kim (*i.e.*, D5) “discloses the possibility of forming different conductive portions,” but argued that “it is completely silent about the possibility of forming said portions for different signals on a same face of the guide.” *Id.*, 455. I disagree with Technoprobe’s contentions in this regard as explained further below.

116. To my understanding, the EPO has not taken further action on the pending ’638 Application.

117. The EPO prosecution history is relevant to my analysis because the EPO’s understanding of Kim and how it reads on the subject matter claimed by Technoprobe comports with my own, as does the EPO’s views regarding the obviousness of an intermediate guide plate. It’s also relevant that Technoprobe admitted that Kim “discloses the possibly of forming different conductive portions.” *Id.*

118. In addition, having reviewed the prosecution history before the EPO, it is my opinion that the ’051 Reference discloses a guide plate electrically connecting one group of contact elements carrying one type of signal (*i.e.*, ground signal). *Id.*, 408-10. By contrast, Kim discloses a guide plate electrically connecting two separate groups of contact elements carrying two different types of signals (*i.e.*, power and ground signals), respectively. *Id.*, 446-47. And, as noted

above, Technoprobe argues that this was a material difference between the two references.

3. Japan

119. The Japanese Pat. App. No. 2019-531897 (“the ’897 Application”), is the Japanese counterpart patent application to the ’885 patent. I have reviewed the translated excerpts of that prosecution history accompanying the Petition.

120. In a communication dated October 19, 2021, the Examiner of the JPO rejected the ’897 Application claims 1-4, 11, 12, 15, 16, and 20 as lacking novelty based on Kim, and all pending claim (1-21) as lacking inventive step based on Kim and other references. Ex. 1017, 1-4.

121. Independent claim 1 and dependent claim 2 of the ’897 Application pending at that time⁶ (claims that were later rejected by the Examiner of the JPO),

⁶ Ex. 1018 has a certified translation of the October 19, 2021 rejection and the April 15, 2022 response to that rejection. In the response to the October 19, 2021 rejection, Technoprobe amended claim 1 to add in the limitations of what were claims 4 and 5. “With this amendment, Claims 4 and 5 before the amendment were deleted, and the top numbers of Claims 6 to 21 were moved up to 4 to 19.” Ex. 1018, 10-15, 19. Accordingly, the post-amendment ’897 Application claims shown in the April 15, 2022 response can be correlated to the pre-amendment claims.

are substantially the same as the limitations of claim 1 of the '885 patent. (The tables below relate the '885 claims to the pre-amendment '897 Application claims.) *Compare* Ex. 1017, 9 *with* Ex. 1001, claim 1.

Claim 1 of the '885 Patent	The '897 Application claims 1 and 2 as of October 19, 2021
A testing head configured to verify the operation of a device under test integrated on a semiconductor wafer, the testing head comprising:	A test head (20) configured to verify the operation of a device under test integrated on a semiconductor wafer, wherein
a plurality of contact elements, each comprising a body that extends between a first end portion and a second end portion, and	each of the contact elements (21', 21'', 21''') has a body (21pr, 21pp) extending between a first end (24) and a second end (25), and
at least one guide provided with a plurality of guide holes configured to house the contact elements,	the test head (20) has at least one guide (40, 41, 42) with a plurality of guide holes (40h, 41h, 42h) and a plurality of contact elements (21', 21'', 21''') housed within the plurality of guide holes (40h, 41h, 42h), and
wherein the at least one guide comprises: a first conductive portion that includes and electrically connects a first group of guide holes, of the plurality of guide holes, to each other and is configured to contact corresponding first contact elements, of the plurality of contact elements, configured to carry a first type of signal; and	said at least one guide (40, 41, 42) has at least one first group (40', 41', 42') of the plurality of guide holes (40h, 41h, 42h), and at least one first conductive part (30') electrically connecting the corresponding first group of the contact elements (21') housed within the at least one first group (40', 41', 42') of the plurality of guide holes (40h, 41h, 42h), and ... the contact elements of the same group are configured to carry the same type of signal, and the contact elements of different groups are configured to carry respective signals of different types, and

[1d] a second conductive portion that includes and electrically connects the holes of a second group of the guide holes to each other, the second group housing second contact elements of the plurality of contact elements, the second contact elements being configured to carry a second type of signal	at least one second group (40'', 41'', 42'') of the plurality of guide holes (40h, 41h, 42h), and at least one second conductive part (30'') electrically connecting the corresponding first group of the contact elements (21'') housed within the at least one second group (40'', 41'', 42'') of the plurality of the guide holes (40h, 41h, 42h), and ... the contact elements of the same group are configured to carry the same type of signal, and the contact elements of different groups are configured to carry respective signals of different types, and
[1e] the first and second types of signals chosen between ground signals and power signals.	[Claim 2] The test head (20) of Claim 1, wherein a first contact element (21') housed within the first group (40', 41', 42') of the plurality of guide holes (40h, 41h, 42h) is configured to carry a ground signal, and a second contact element (21'') housed within the second group (40'', 41'', 42'') of the plurality of guide holes (40h, 41h, 42h) carries a power signal.

122. The JPO also noted, with respect to lack of inventive step, that “although the technology cited in [Kim] has only two guides, providing three guides, as shown in Figure 1 of the Cited Document 3 Publication 0012 [another prior art reference, Japanese Unexamined Patent Application Publication No. Hei 11-248745], is a design change that can be made by a person skilled in the art.”

Ex. 1017, 3.

123. In its response to the rejection, in a filing dated April 15, 2022, Technoprobe admitted that Kim (*i.e.*, Cited Document 1) discloses “an upper plate and a lower plate with guide holes for accommodating test pins.” *Id.*, 18. Technoprobe also admitted that that Kim discloses “[t]he conductive part, which consists of a conductive layer 20 formed in the guide hole that makes contact with the test pin 30, and a conductive trace 40 formed on the surface of the guide, covers multiple guide holes.” *Id.* Technoprobe further admitted that “Test pins within a group that transmit the same signal are electrically connected to each other by conductive parts.” *Id.* Technoprobe admitted that “[t]he test pins are disclosed to be for signal, ground, or power.” *Id.*

124. In an effort to distinguish the claimed invention of the ’897 Application from Kim, Technoprobe amended independent claim 1 by further limiting that “at least one conductive part (30’, 30’’, 30’’’) is separated from another conductive part and locally separated by at least one non-conductive zone (31, 31’, 31’’) so as not to allow electrical connections between contact elements configured to carry different types of signals and/or between contact elements that must not be short-circuited, and said at least one guide (40, 41, 42) is provided with at least one insulation covering to cover the at least one non-conductive zone (31, 31’, 31’’).” *Id.*, 9. Technoprobe argued that the ’632 Reference “does not

disclose the covered insulation part that covers the non-conductive zone of the guide.” *Id.*, 18.

125. The JPO prosecution history is relevant to my analysis because the JPO’s understanding of Kim and how it reads on the subject matter claimed by Technoprobe comports with my own, as does the JPO’s views regarding the obviousness of an intermediate guide plate. It also is relevant that Technoprobe did not dispute the JPO’s characterization of Kim’s teachings as to the original claims of the ’897 Application other than as noted above, and in fact admitted Kim’s disclosures as noted above, nor did Technoprobe dispute the JPO’s conclusions regarding the obviousness of adding a third guide plate.

IX. OVERVIEW OF THE PRIOR ART REFERENCES

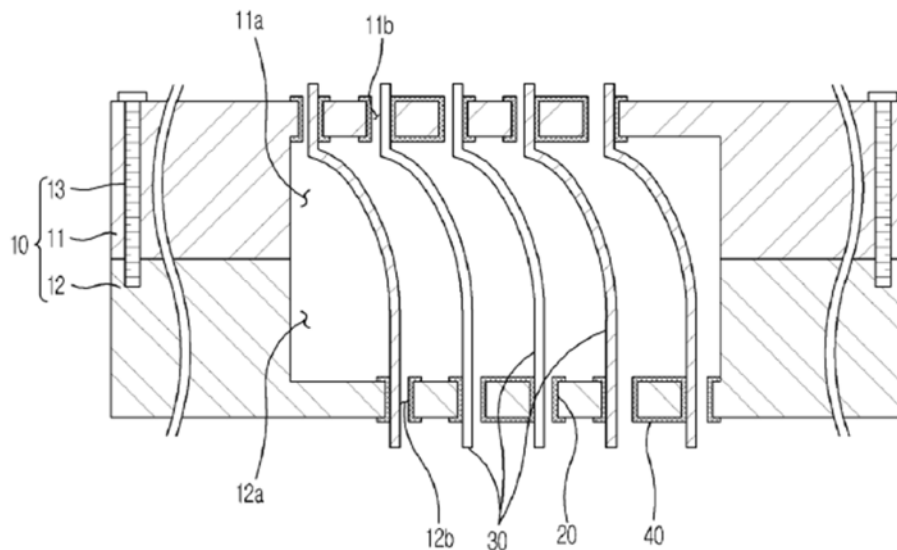
126. I have reviewed and am familiar with the following prior art references: (1) Kim, (2) Schmid, (3) Fan, (4) Bross, (5) SWTest Willtechnology Presentation.

A. Kim

127. U.S. Patent Application Publication No. 2015/0198632 (Ex. 1006, “Kim”) was filed on January 14, 2015 and published on July 16, 2015. Kim also ultimately resulted in issued U.S. Patent No. 10,928,422 on February 23, 2021. Kim relates to a semiconductor test device. Ex. 1006, Abstract. Similar to the ’885 patent, Kim also sought to solve the problems caused by the noise and

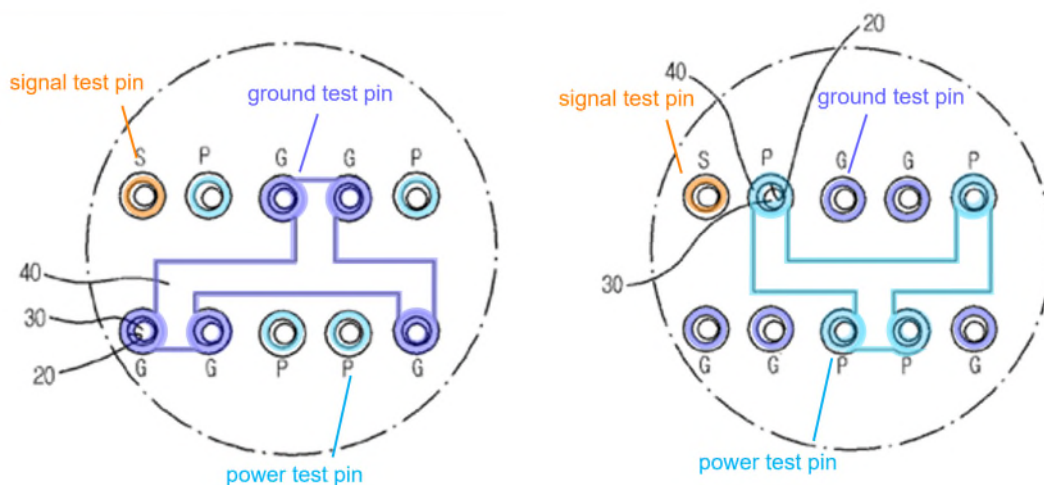
frequency performance. *Id.*, [0003], [0014], [0016], [0051]. To solve these problems, Kim discloses the same kind of probe card as the '885 patent.

128. Specifically, Kim explains and illustrates in Fig. 2 an exemplary probe card including a guide plate (10), a conductive layer (20), testing pins (30) and a conductive trace (40). *Id.*, [0033], Fig. 2. The guide (10) supporting the testing pins (30) comprises an upper plate (11) and a lower plate (12), and each with a plurality of guide holes (11b, 12b). *Id.*, [0034].



129. Kim teaches that both the conductive trace (40) and conductive layer (20) are formed on the guide (10) using a conductive material. *Id.*, [0034]. The testing pins (30) in contact with the conductive layers (20) on the guide (10) are electrically contacted to one another through the conductive trace (40). *Id.*, [0038], [0042]. Kim further discloses that the testing pins (30) carrying the same type of

signal such as ground and power are electrically connected to one another. *Id.*, [0051], [0062], Figs. 5a and 5b (annotated and color-coded below).



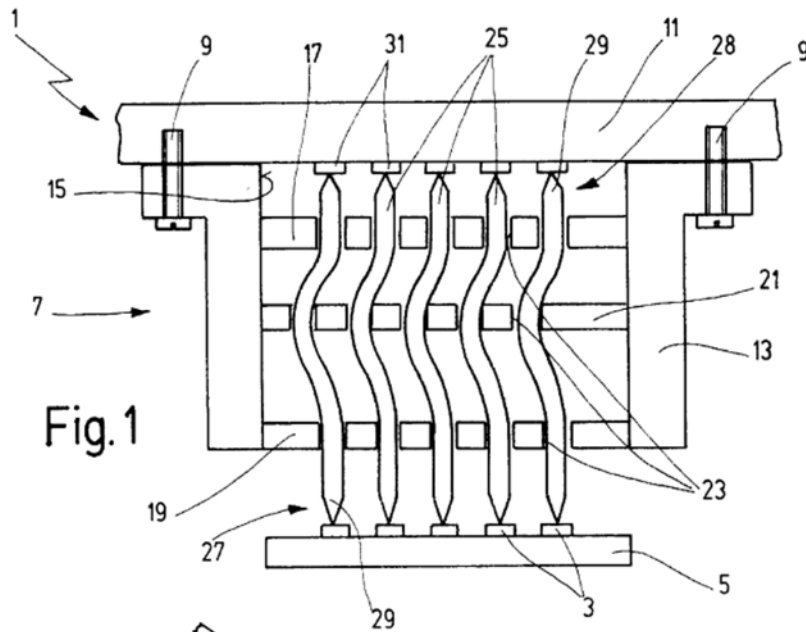
130. As a result, Kim concludes that a plurality of testing pins (30), transmitting *identical* signals without interference with testing pins (30) transmitting *different* signals, can be conveniently connected. *Id.*, [0051] (emphasis added).

131. More details about Kim are discussed in the sections below setting forth grounds of invalidity.

B. Schmid

132. U.S. Pat. No. 6,417,684 (Ex. 1009, “Schmid”) was filed on October 15, 1998 and published on July 9, 2002. Schmid discloses a wafer testing probe with three guide plates separated from each other. Schmid discloses a test head (1) for making contact simultaneously with a plurality of test points (3), which are

arranged next to one another, of an electric component (5) under test. Ex. 1009, 3:25-35, Fig. 1.



133. Specifically, Schmid discloses that the test head (1) has a first guide panel (17), a second guide panel (19) and a third guide panel (21) that are held parallel to one another and at a distance from one another. *Id.*, 3:41-54. Schmid further teaches that each of the guide panels (17, 19, 21) has several feed through openings (23) through which pin shaped contact elements (25), also referred to as test probes, are “axially displaceably guided”. *Id.* Schmid explains that the contact elements (25) are composed of an elastic, preferably spring elastic and resilient material, for example spring metal, and are here designed as buckling wires, and the guide panels (17, 19, 21) are preferably composed of an electrically non-conductive material, for example a plastic, glass, ceramic, silicon, or the like.

Id. Schmid also explains that the third guide panel (21) is arranged in the intermediate space between the first and second guide panels (17, 19). *Id.*, 3:58-61.

C. Fan

134. U.S. Pat. No. 9,470,715 (Ex. 1011, “Fan”) is directed to a probe head applied to a probe card. Ex. 1011, 1:13-15. Fan describes that the probe head includes a plate 100 having a composite coating layer 300 on the surface of the guide holes of the plate and describes methods for producing the composite coating layer. *Id.*, 3:1-7, 4:17:38, 8:8-10, Figs. 1A, 1B, 2, 4. Fan illustrates in Fig. 4 that the plate 100 is made of either non-conductive materials, semiconductor materials or conductive materials with high strength and easy to fabricate. *Id.*, 3:41-43. Fan also notes that the plate may be made of ceramics. *Id.*, 3:45. And the surfaces of the plate 100 may be insulated to prevent the probes 200 that are inserted to the plate 100 from electrically interrupt[ing] each other. *Id.*, 5:1-14, Figs. 2, 4. Specifically, Fan teaches an “insulating layer 600” which can cover some or all of the guide plate surface. *Id.*, 5:1-14, Fig. 4. Fan teaches that the “insulating material can be coated on” the guide plate material. *Id.*, 5:29-32.

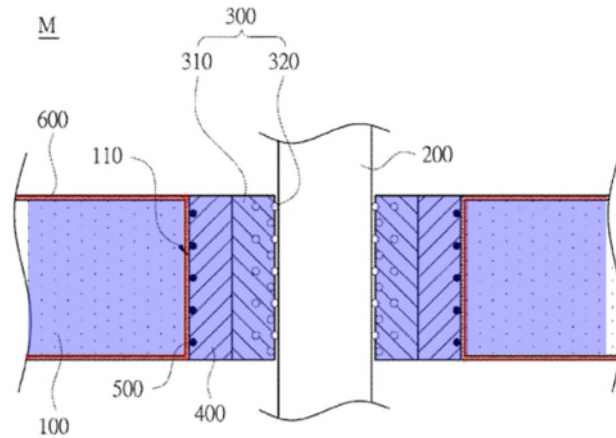


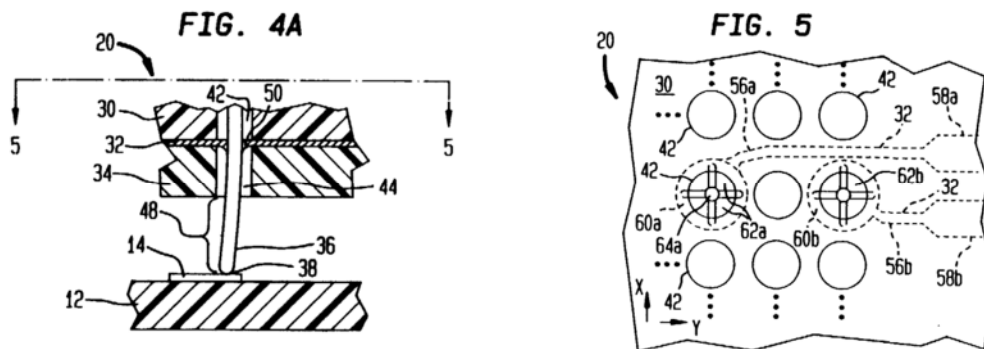
FIG. 4

Id., Fig. 4 (color-coding added).

D. Bross

135. U.S. Pat. No. 5,225,777 (Ex. 1010, “Bross”) is directed to an electrical test probe assembly using buckling beam contact elements, and to a method of fabrication which provides a very high density of probe assembly elements for making a multitude of electrical connections over a small area to very large scale integrated (VLSI) circuits. Ex. 1010, Abstract, 1:5-10. Bross describes a test fixture 10 (a suitable support) on which are mounted a plurality of very large scale integrated (VLSI) circuits 12 and a probe assembly 20 contacting the VLSI circuits 12. Each VLSI circuit 12 has a large number of very small surface contact pads 14 closely spaced in orthogonal directions and lying substantially in a flat plane on the upper face of the VLSI circuit. These surface pads 14 provide miniature electric contacts to internal active elements of the VLSI circuit 12. *Id.*, Figs. 1A-1B; 3:62-4:25.

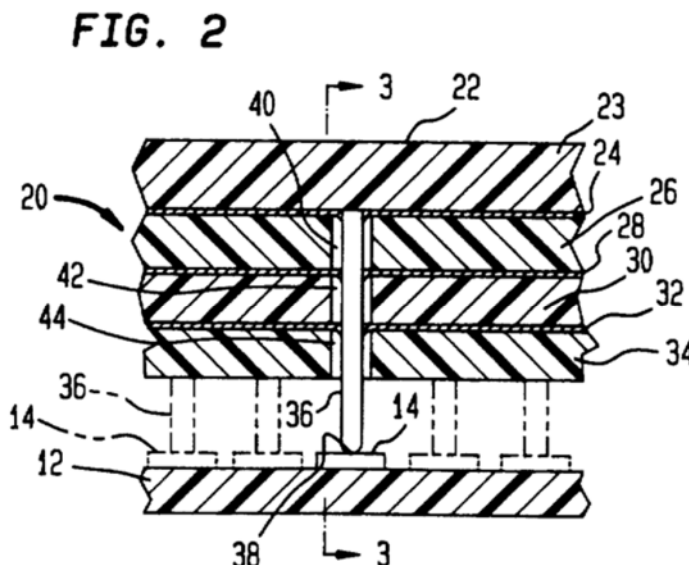
136. Bross describes the layer of conductive circuitry 32 positioned beneath the insulating layer 30 and is seen to comprise a plurality of electrically isolated printed-circuit traces (conductors), with the dotted lines 56a and 56b as examples in Fig. 5. *Id.*, Figs. 4A and 5, 6:23-32. As many or as few of these circuit traces 56a and 56b may be provided in the layer of conductive circuitry 32 as required by the desired member of interconnections to and from the respective probe elements 36. *Id.*, 6:28-31, cl.1 “A probe assembly comprising: a body containing a plurality of insulating and conductive layers positioned horizontally in a vertically stacked multi-layer arrangement.”



Id., Figs. 4A and 5.

137. Bross also discloses a laminating method or multilayer technique (metallization of guide plates) or “a multi-layer arrangement of insulating and conducting layers within the body of the probe assembly.” *Id.*, Abstract. Bross shows in Fig. 2 as an example, “multi-layer arrangement comprises a top insulating layer 23, a first conductive layer 24, a second insulating layer 26, a second conductive layer 28, a third insulating layer 30, a third conductive layer 32, and a

fourth or bottom insulating layer 34. Each of the conductive layers typically comprises a plurality of individual conductors. These individual conductors are sometimes denoted as a ‘printed circuit’.” *Id.*, Fig. 2, 4:41-49.

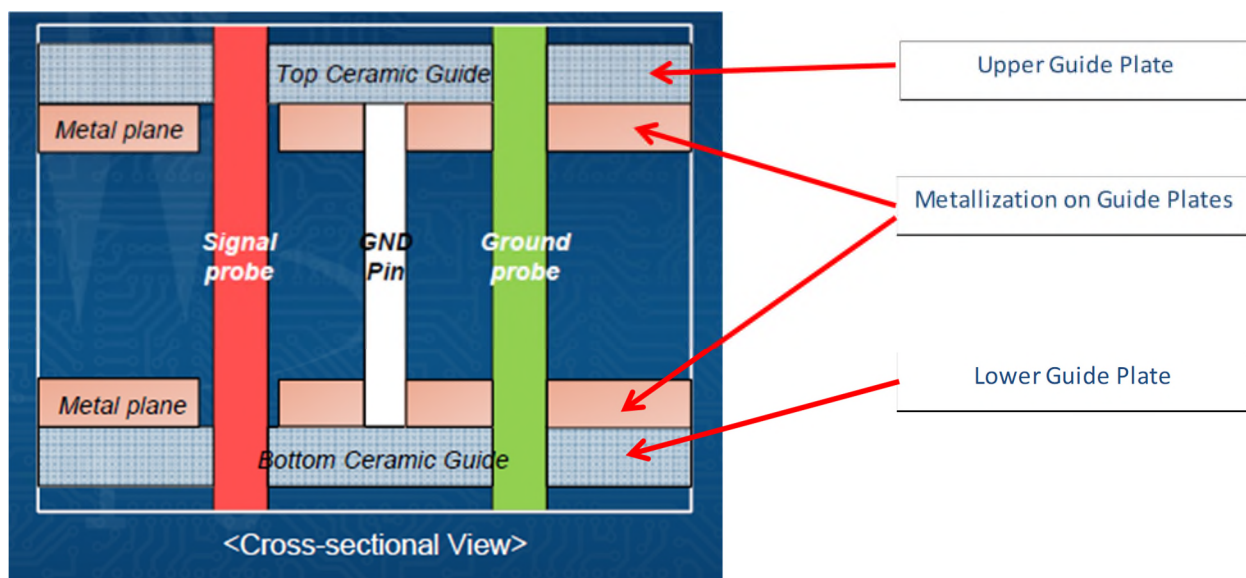


Id., Fig. 2.

138. Bross explains that this laminating method or multilayer technique (metallization of guide plates) is well known in the art. For example, “These layers of insulation and conductors are suitable bonded together into a unitary structure to provide a multilayer arrangement, such as is well known in the art.” *Id.*, 4:49-52. Additionally, “[t]he positions, spacings, and shapes of the conductive traces 56a, 56b, etc., are provided in accordance with design rules well known to those skilled in the art of designing and fabricating multi-layer circuitry.” *Id.*, 6:36-40. “Still further, a multi-layer arrangement with a different number of layers or of different designs from that disclosed may be employed.” *Id.*, 7:46-48.

E. 2016 SWTest Willtechnology Presentation

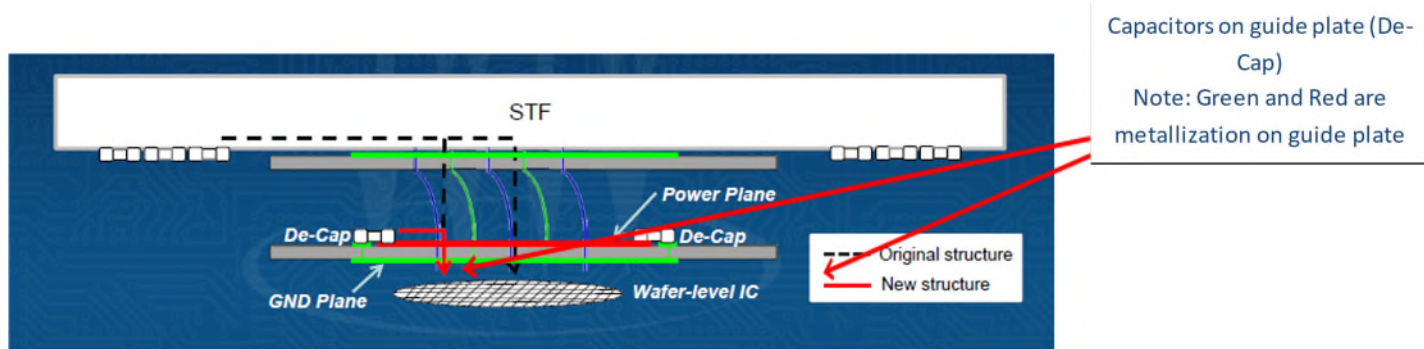
139. The 2016 Willtechnology presentation at the Semiconductor Wafer Test Workshop (“SWTest”),⁷ titled “A Proposal of a New Probe Head Design in Vertical Probe Cards for Low Crosstalk and PDN impedance,” (2016 SWTest Presentation, Ex. 1028), was authored by Kyung Hyun Chang and Hyun Min Kim from Willtechnology Co., Ltd., and presented on June 7, 2016. Exs. 1028-1030; Ex. 1031, 52-70. This presentation discloses metallized guide plates, *i.e.*, conductive portions for ground and power. *See* Ex. 1028, 8, 15 and 16.



Id., 8 (annotations added).

⁷ Both “Will Technology” and “Willtechnology” are used in this presentation. For this Declaration, “Willtechnology” is used.

140. The 2016 SWTest Presentation also discloses having circuit components such as capacitors on a guide plate and connecting capacitors (de-caps) on a guide plate between the ground and power metallization (conductive portions).



Id., 15 (annotations added).

141. The 2016 SWTest Presentation was publicly available at least before December 6, 2016, if not earlier. The presentation was publicly presented at the SWTest on Tuesday, June 7, 2016. Ex. 1030; Ex. 1031, 52-70. As Patent Owner admits, presentations at the SWTest 2023 conference were “public presentations.” See Ex. 1021, ¶¶ 26, 28, 29, 32.

142. Indeed, SWTest is the premier conference for wafer probing technology. It is annually attended by over 500 technologists in that field. I have attended SWTest conferences multiple times. And I have served as the chair at some of the sessions at SWTest conferences over the years, including the 2016 SWTest where Willtechnology presented “A proposal of a New Probe Head

Design in Vertical Probe Cards for Low Crosstalk and PDN impedance” (Ex. 1028) in the June 7, 2016 session.

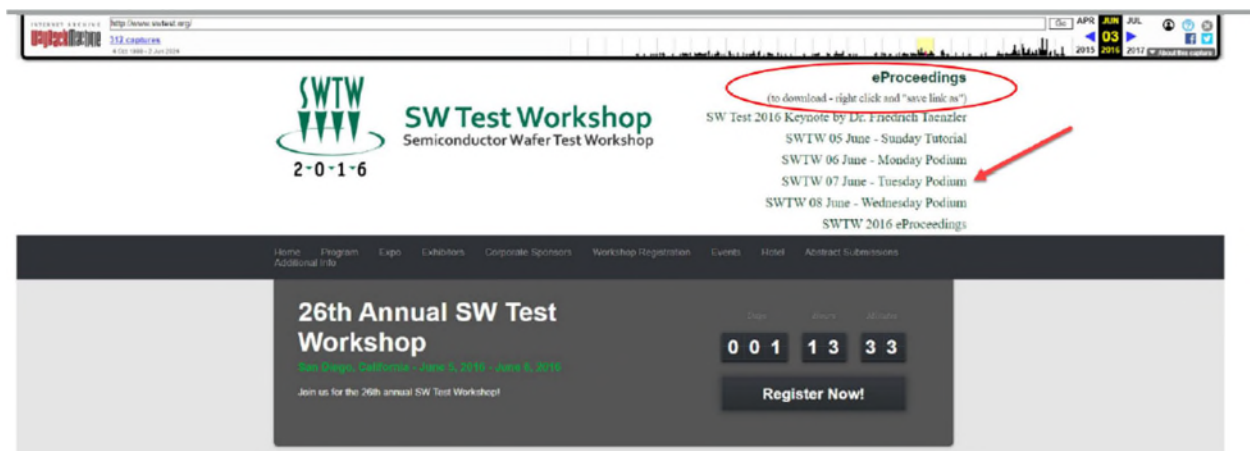
143. As a chair and attendee (one who registers at the conference) of the SWTest conferences, I am very familiar with them. Before the conference, SWTest calls for papers. Authors who wish to make a presentation at the conference may submit abstracts to the conference portal. Then SWTest selects the presentations for the conference based on the submitted abstracts. Authors whose abstracts were selected create presentations for the conference and deliver (present) their presentation to the audience of attendees at the conference. When I served as a chair, I made introductions and took questions.

144. At the conference, the proceedings which include all the presentations at the conference are distributed, electronically or in hard copy, to the attendees. Generally, there are 3 levels of registration: full conference registration, exhibitor registration, and hybrid registration of conference and exhibit registrations. The attendees with full conference registration or hybrid registration have access to the proceedings during the time of the conference.

145. Shortly after the conferences, SWTest posts the proceedings to the archive section of the SWTest website, and the proceedings are accessible by the public, attendees and non-attendees, from the Internet for free. Even people who did not attend SWTest can read the proceedings that are available through the

library. And they do not need to attend the conference to have the benefit of seeing the material that was presented.

146. The 2016 SWTest is no exception. As shown in the Internet Archive (Wayback Machine) webpage captures, by June 3, 2016, the SWTest webpage provided download links to the e-proceedings including the “SWTW 07 June - Tuesday Podium” that contains the 2016 SWTest Presentation. Ex. 1029 (annotation added).



147. The downloadable content from the June 3, 2016 SWTest webpage, the PDF of the June 7 Tuesday Podium presentation (Ex. 1031) which contains the 2016 SWTest Presentation (Ex. 1031 at 52-70; Ex. 1028) at the link was available for the public to download by at least December 6, 2016. Ex. 1030.



Id.

148. The Presentation was widely disseminated among hundreds of attendees over four days at the 2016 SWTest. The hundreds of the attendees include technologists from various entities in the semiconductor testing field. The Proceedings of SWTest were distributed electronically to every attendee by at least June 3, 2016 and to the public by at least December 6, 2016.

X. GROUND 1: KIM ANTICIPATES CLAIMS 1-2, 4, 8-11 AND 14

A. Claim 1

149. All elements of claims 1 are disclosed by Kim as explained below.

1. **Claim [1P]: A testing head configured to verify the operation of a device under test integrated on a semiconductor wafer, the testing head comprising**

150. Kim discloses a testing head configured to verify the operation of a device under test integrated on a semiconductor wafer.

151. The '885 patent explains in the specification and illustrates in Fig. 2A a testing head (20) for testing electronic devices integrated on a semiconductor wafer. Ex. 1001, 5:66-6:3, Fig. 2A.

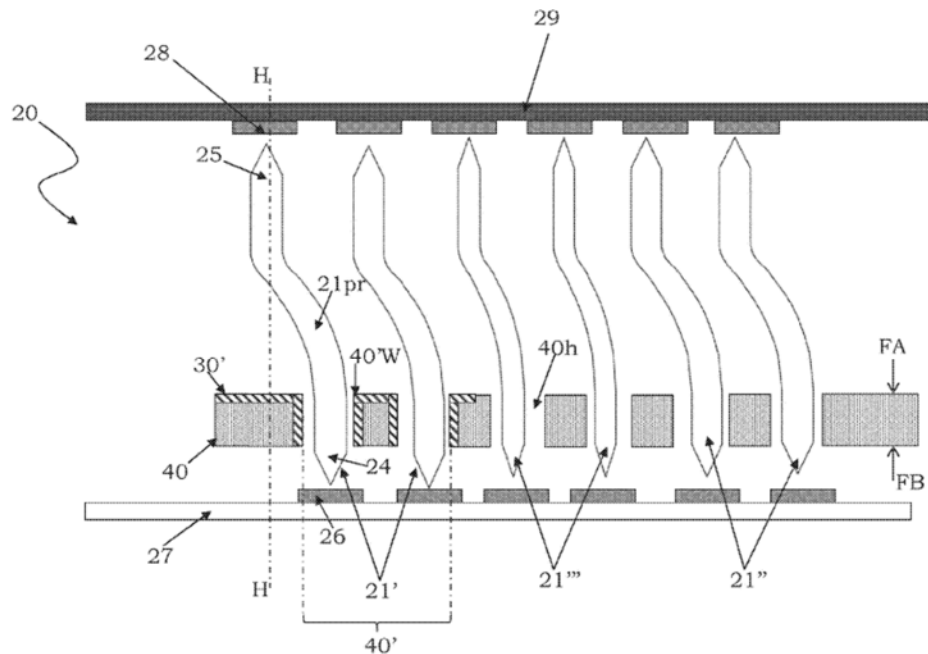
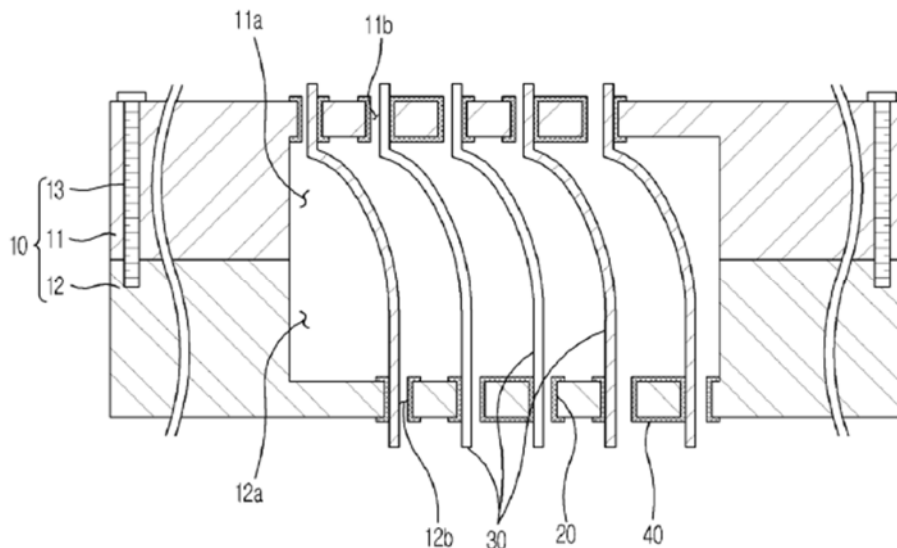


FIG. 2A

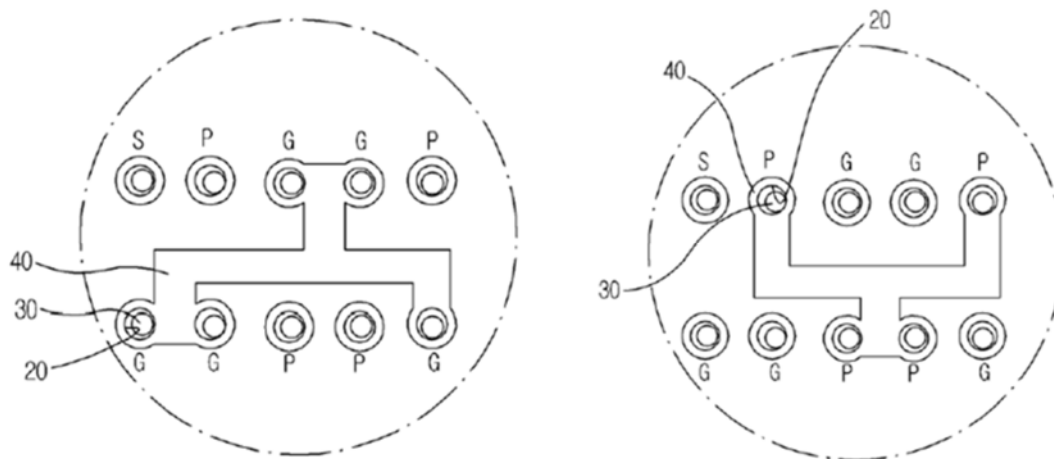
152. The '885 patent specifically teaches that the testing head (20) used to verify the operation of a device comprises at least two regions: the first region apt to receive power and ground signals, and a second region apt to receive/send input/output signals from/to a test equipment connected to the testing head (20). *Id.*, 6:29-33.

153. Kim discloses a semiconductor test device (1) for testing the electrical characteristic of the chip manufactured at the wafer level. Ex. 1006, Abstract, [0005]-[0006], [0032]-[0034]. Kim explains that the semiconductor testing device

could be implemented in a probe card. *Id.*, [0031]. As illustrated in Fig. 2, Kim discloses an exemplary semiconductor test device which constitutes the claimed “testing head” illustrated in Fig. 2A of the ’885 patent. *Id.*, Fig. 2.



154. Kim explains and illustrates in Fig. 2 an exemplary testing device (*i.e.*, probe card) including a guide plate (10), a conductive layer (20), testing pins (30) and a conductive trace (40). *Id.*, [0033], Fig. 2. The guide (10) supporting the testing pins (30) comprises an upper plate (11) and a lower plate (12), and each with a plurality of guide holes (11b, 12b). *Id.*, [0034]. Kim further explains that the guide plate (10) includes regions for testing pins (30) housed in the guide holes (11b, 12b). *Id.*, [0051], [0062], Fig. 2. As further shown in Figs. 5a and 5b, Kim illustrates that the testing pins (30) are grounding test pins, power test pins and signal test pins. *Id.*, [0051], [0062], Figs. 5a and 5b.



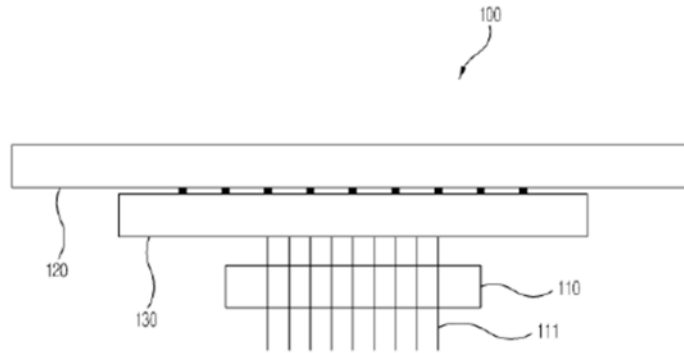
155. Thus, Kim discloses the preamble of claim [1P] because Kim’s test device (1) for testing the electrical characteristic of the chip manufactured at the wafer level constructs the claimed testing head configured to verify the operation of a device under test integrated on a semiconductor wafer.

2. Claim [1a]: a plurality of contact elements, each comprising a body that extends between a first end portion and a second end portion, and

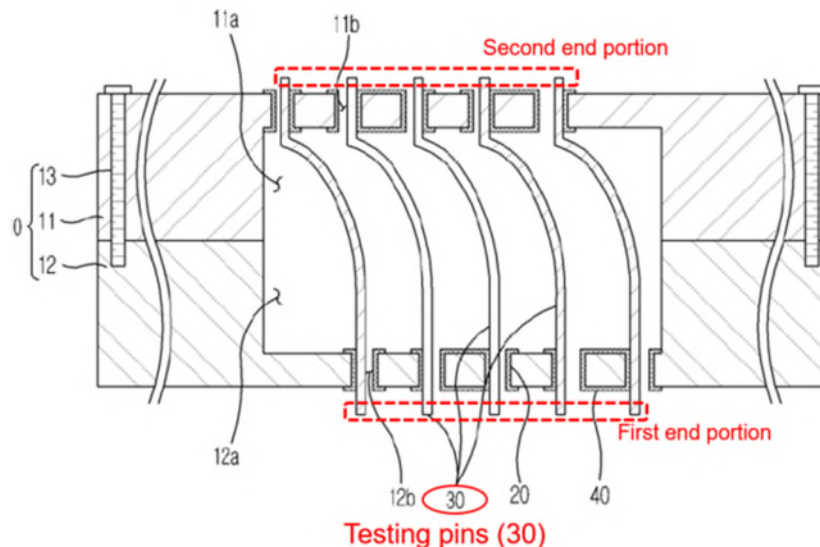
156. The ’885 patent uses the terms “contact elements” and “contact probes” interchangeably. *See, e.g.*, Ex. 1001, 1:33-34, 4:39-41, 7:1-4, 11:65-67, 14:17-19. The ’885 patent also teaches that the claimed “contact elements” could be in the form of “buckling beam” or “pogo pins” which were known in the art. *Id.*, 14:19; 2:32-33. Kim teaches that its testing pins (30) are, for example, a buckling beam type probe called cobra or various probes such as “pogo pins” or “wire probes.” Ex. 1006, [0040]. Thus, a POSITA would understand that Kim’s testing pins (30) mean the claimed “contact elements” or contact probes.

157. According to the '885 patent, each contact element of the testing head (20) comprises the body (21 pr), which extends along a longitudinal axis (H-H) between a first end portion or contact tip (24) and a second end portion or contact head (25). Ex. 1001, 7:13-16, Fig. 2A. The '885 patent explains that the contact tip (24) is apt to abut onto corresponding contact pads (26) of a device under test integrated in a semiconductor wafer (27). *Id.*, 7:17-19, Fig. 2A. The '885 patent further explains that the contact elements terminate with the contact head (25) which is apt to abut onto corresponding contact pads (28) of an interposer or space transformer (29). *Id.*, 7:20-24. A POSITA would understand that the claimed “first end portion” means the end of the contact elements at the contact tip (24) and the claimed “second end portion” means the end of the contact elements at the contact head (25), and the claimed “body” of the contact elements connect two end portions of the contact elements. *Id.*, 2:32-36.

158. As illustrated in Fig. 1, Kim discloses a conventional probe card (100) including a plurality of test pins (111) electrically contacting the chips to be tested and the test pins (111) including a body extends between the space transformer (130) and the Device Under Test (DUT). *See, e.g.*, Ex. 1006, [0010], [0012], Fig. 1. Like the '885 patent's “contact elements,” Kim's “testing pins” are used to transmit signals (ground, power, and input/output) to the device under test. *Id.*, [0019], [0025], [0032], [0042], [0044], [0045], Figs. 5a and 5b.



159. According to Kim, the bottom of the testing pins (111), which make electrical contact with the Device Under Test (DUT), constitutes the claimed “first end portion,” and the top of the test pins (111), which electrically contact the space transformer (130), constitutes the claimed “second end portion.” Kim further discloses a cross-sectional view illustrating an embodiment of the testing device in Figure 2. *Id.*, Fig. 2 (annotated).



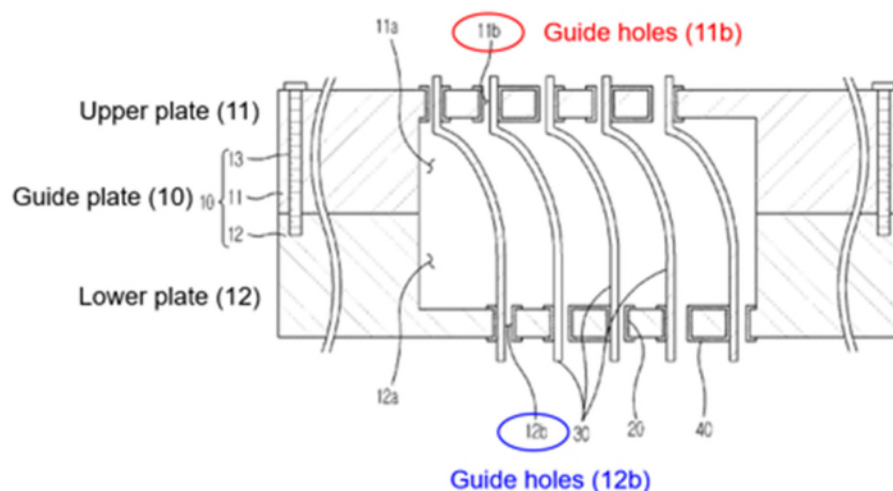
160. As shown in Fig. 2, Kim’s testing pins (30) extend from the guide holes (11b) of the upper plate (11) through the receiving grooves (11a, 12a) to the

guide holes (12b) of the lower plate (12). *Id.*, [0033]-[0037]. Kim's testing pins (30) further comprise a body extending between the end of the testing pins (30) making electrical contact with the Device Under Test (DUT) (the claimed "first end portion") and the end of the testing pins (30) electrically contacting the space transformer (130) (the claimed "second end portion").

161. Thus, Kim discloses claim [1a].

3. Claim [1b]: at least one guide provided with a plurality of guide holes configured to house the contact elements

162. Kim discloses a guide plate (10), an assembly, including an upper plate (11) formed with a plurality of first guide holes (11b), and a lower plate (12) formed with a plurality of second guide holes (12b). *Id.*, [0034]-[0037], Fig. 2 (annotated).



163. Kim explains that the testing pins (30) are inserted and placed in the first guide hole (11b) and the second guide hole (12b). *Id.*, [0039], Fig. 2.

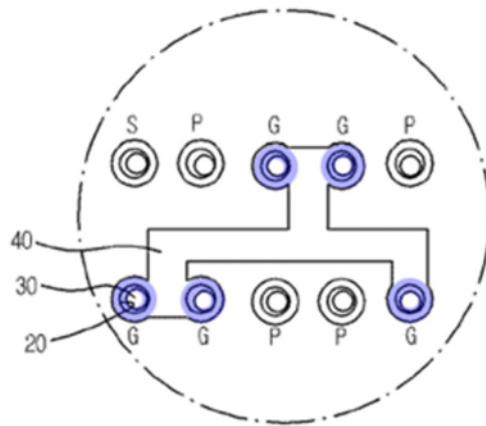
Thus, one of the upper plate (11) and the lower plate (12) of the guide plate (10) constitutes the claimed “at least one guide” that houses the testing pins (30) constituting the claimed “contact elements.”

164. Thus, Kim discloses claim [1b].

4. **Claim [1c]: wherein the at least one guide comprises: a first conductive portion that includes and electrically connects a first group of guide holes, of the plurality of guide holes, to each other and is configured to contact corresponding first contact elements, of the plurality of contact elements, configured to carry a first type of signal; and**

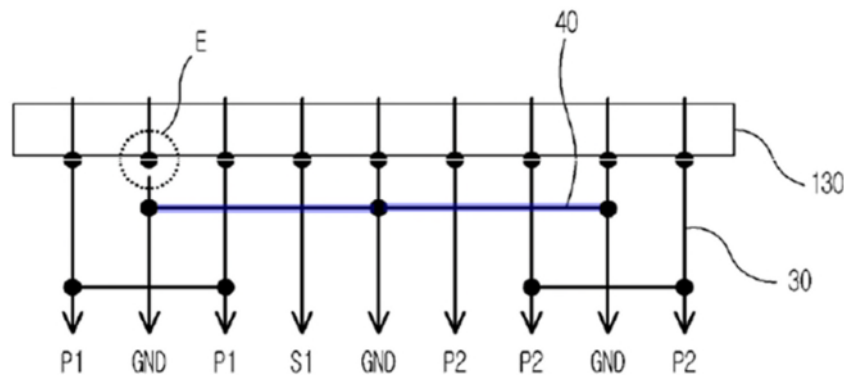
165. First, Kim teaches conductive layers (20) and a conductive trace (40) collectively constituting the claimed “first conductive portion.” *See, e.g., Id.*, [0033]. Kim explains that the plurality of the conductive layers (20) is formed by coating conductive material on one side of the upper plate (11) where the first guide holes (11b) are formed. *Id.*, [0038]. Kim further teaches that the conductive layers (20) are formed on the inner side of the guide holes. *See, e.g., id.*, Abstract, [0017]. Kim goes on to teach a conductive trace (40) also using a conductive material formed on the inner or outer side of the upper plate (11) or lower plate (12). *Id.*, [0042]. And the conductive trace (40) is connected to the conductive layer (20). *Id.*, [0043]. The connection between the plurality of the conductive layers (20) and the conductive trace (40) results in that the testing pins (30) in contact with the conductive layers (20) within the guide holes (11b, 12b) are electrically connected to the conductive trace (40). *Id.*, [0038], [0039].

166. Second, Kim teaches that the conductive layers (20), with which the testing pins (30) of transmitting the *same* signal are contacted, are connected to each other. *Id.*, [0044], [0045] (emphasis added). Kim explains that the testing pins (30) in contact with the conductive layers (20), for example, are testing pins for ground. *Id.* Kim illustrates in Fig. 5a that the testing pins (30) for ground signals are electrically connected via the conductive layers (20) formed within a group of guide holes and the conductive trace (40) electrically connecting the conductive layers (20). *Id.*, Fig. 5a (color-coding added).



167. Kim describes and illustrates in Figs. 2 and 5a that a plurality of guide holes (11b) are formed on the upper surface of the upper plate (11) of the guide plate (10) and a group of the guide holes are selected from the plurality of guide holes (11b) for housing a group of testing pins (30), which is also selected from a plurality of testing pins (30), for ground signals. *Id.*, [0051]. And, the group of

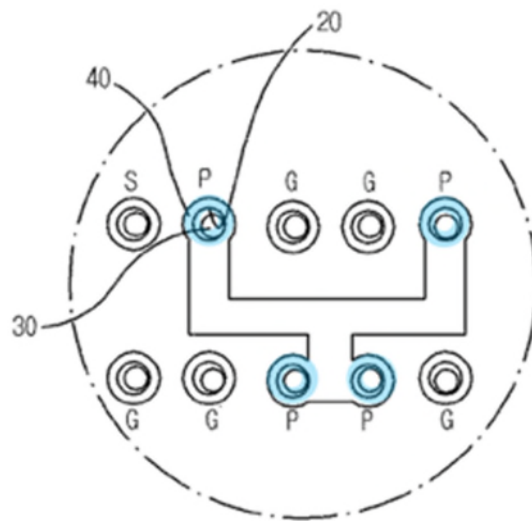
testing pins (30) for ground signals is electrically connected via the conductive layers (20) and the conductive trace (40). *Id.* Kim further illustrates a conceptual diagram demonstrating that the conductive trace (40) connects between the testing pins (30) transmitting the same type of ground signals and the conductive layers (20) in contact with the testing pins (30). *Id.*, [0044], [0045], Fig. 3 (color-coding added).



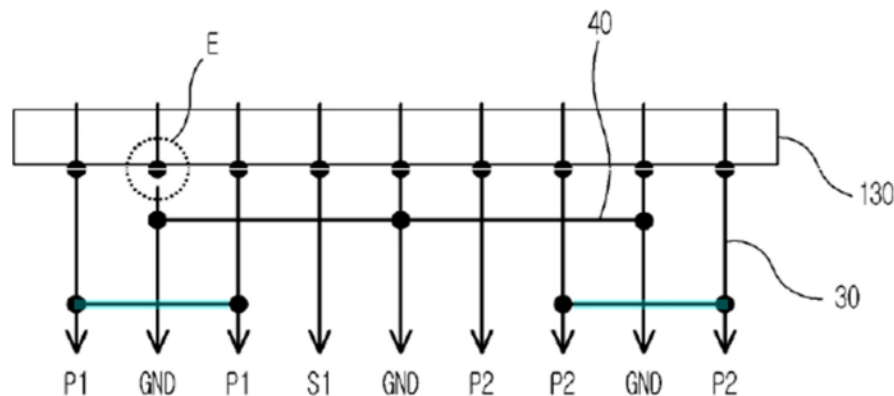
168. Thus, Kim discloses claim [1c] because Kim discloses that the two or more of the conductive layers (20) and some or all of the conductive trace (40) formed on the upper plate (11) for connecting testing pins (30) carrying ground signals constitute the claimed “first conductive portion,” two or more of the guide holes (11b) formed on the upper plate (11) for housing testing pins (30) carrying ground signals constitute the claimed “first group of guide holes,” two or more of the testing pins (30) for ground signals constitute the claimed “first contact elements,” and the “ground signal” carried by the testing pins (30) constitutes the claimed “first type of signal.”

5. **Claim [1d]: a second conductive portion that includes and electrically connects the holes of a second group of the guide holes to each other, the second group housing second contact elements of the plurality of contact elements, the second contact elements being configured to carry a second type of signal**

169. In addition to the connections among the selected group of testing pins (30) for ground signals through the conductive layers (20) in contact with the testing pins (30) in the guide holes (11b) on the guide (10) and the conductive trace (40), Kim similarly teaches how to use the conductive layers (20), the guide holes (11b) and the conductive trace (4) to electrically connect another group of testing pins (30) for another type of signal. Specifically, Kim describes and illustrates in Fig. 5b that the testing pins (30) carrying power signals are electrically connected via the conductive layers (20) and conductive trace (40). *Id.*, [0051], Fig. 5b (color-coding added).



170. Kim explains and illustrates in Figs. 2 and 5b that a plurality of guide holes (11b) are formed on the lower surface of the upper plate (11) of the guide plate (10) and a group of the guide holes are selected from the plurality of guide holes (11b) for housing a group of testing pins (30), which is also selected from a plurality of testing pins (30), for power signals. *Id.*, [0051]. And, the group of testing pins (30) for power signals is electrically connected via the conductive layers (20) and the conductive trace (40). *Id.* Kim similarly illustrates a conceptual diagram demonstrating that the conductive trace (40) connects between the testing pins (30) transmitting the same type of power signals and the conductive layers (20) in contact with the testing pins (30) within the guide holes (11b). *Id.*, Fig. 3 (color-coding added). Accordingly, Figures 5a and 5b show two different “conductive portions” (two different sets of conductive layers 20 and conductive traces 40) which, as described above, connect with two different sets of guide holes and contact elements.



171. A POSITA would understand that “P” in Kim’s figures stands for “Power,” and the “P” guide holes in Figures 5a and 5b house the testing pins for transmitting power signals, while the “P1” and “P2” shown in Figure 3 of Kim likewise are illustrating testing pins that transmit different power signals and S1 illustrates an input/output signal pin. These figures depict the three well-known types of testing pins or probes in a semiconductor testing head, namely, input/output signal, power, and ground.

172. Thus, Kim discloses claim [1d] because Kim teaches that the two or more of the conductive layers (20) and some or all of the conductive trace (40) formed on the upper plate (11) for connecting testing pins (30) carrying power signals constitute the claimed “second conductive portion,” two or more of the guide holes (11b) formed on the upper plate (11) for housing testing pins (30) carrying power signals constitute the claimed “second group of guide holes,” two or more of the testing pins (30) for power signals constitute the claimed “second contact elements,” and the “power signal” carried by the testing pins (30) constitutes the claimed “second type of signal.”

6. Claim [1e]: the first and second types of signals chosen between ground signals and power signals

173. As previously discussed in limitations 1[c] and 1[d], Kim teaches two separate groups of testing pins (30) for ground and power in contact with two separate groups of conductive layers (20) formed within two separate groups of

guide holes (11b), respectively. And the two separate groups of testing pins (30) carrying ground and power signals respectively are electrically connected by the conductive layers (20) and the conductive trace (40).

174. Without limiting the type of signal, Kim teaches that it applies to testing pins transmitting *identical* or the *same* signals. *See, e.g., id.*, [0042]-[0045] (emphasis added). Kim explains that the same or identical signals for ground and power are disclosed as examples. *Id.*, [0051], Figs. 3, 5a and 5b.

175. Thus, Kim discloses claim [1e] because Kim teaches that the claimed “first and second type of signals” carried by two separate groups of the testing pins (30) are chosen between ground signals and power signals.

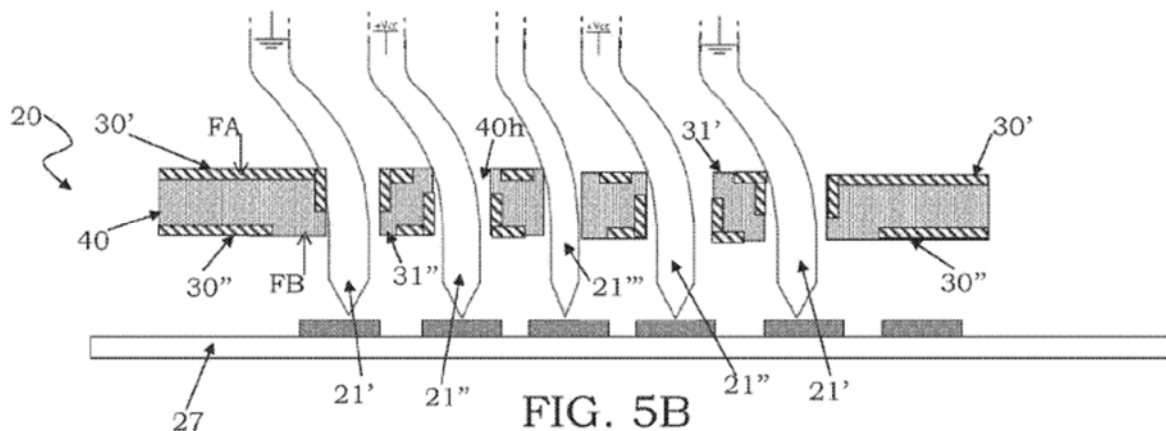
176. Thus, Kim discloses all elements of claim 1.

B. Claim 2

1. The testing head of claim 1, wherein the first conductive portion is locally interrupted by at least one non-conductive zone

177. Claim 2 is disclosed by Kim. Kim discloses the testing head of claim 1. *Supra* § XI(A). Also, the '885 patent explains and illustrates in Fig. 5B that “wherein the first conductive portion 30’ and the second conductive portion 30’” are formed on two opposite faces of the same guide” and “[i]f the first contact elements 21’ apt to carry ground signals and the second contact elements 21’” apt to carry power signals are alternated one after the other, both the conductive

portions 30' and 30'' are locally interrupted by suitable non-conductive zones 31' and 31'' (similarly to what is observed in relation to FIGS. 3A-3D), respectively, so as to avoid an electrical connection between ground contact elements and power contact elements.” Ex. 1001, 13:7-9, 13:26-44, Fig. 5B.

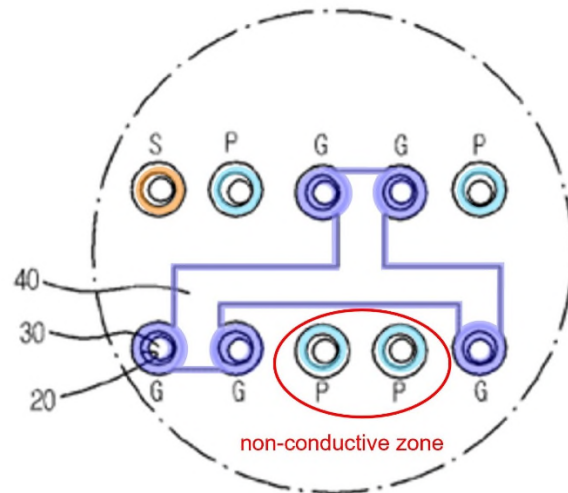


178. The '885 explains that “[t]he non-conductive zones 31' and 31'' therefore locally prevent an electrical connection between adjacent contact elements apt to carry different signals.” *Id.* at 13:34-36. As shown in Figure 5B, the non-conductive zones surround the probes that carry the other type of signal, so there is a gap in the conductive portion, and in that way the non-conductive zones “locally interrupt” the conductive portions. For example, the non-conductive zone 31' is a gap between the conductive portion 30 that connects the first and second probes 21'.

179. Kim teaches that the conductive layer (20), which is formed by coating a conductive material on the upper plate (11) and the lower plate of the guide (10), plays a role in allowing the testing pins (3) and conductive trace (40) to be electrically connected to each other. Ex. 1006, [0038]. Thus, a POSITA would understand that the material composed of the guide (10) including the upper plate (11) and the lower plate (12) is necessarily non-conductive material; there would be no reason to for the conductive layer or conductive trace on the guide if the guide itself were conductive. *See also id.*, [0062] (teaching in another embodiment that the testing pins (30) for power signals are insulated from the testing pins (30) for ground signals by the guide plate (10) in which the conductive materials formed at the edge of the guide plate is removed.).

180. In addition, as illustrated in Fig. 5a (annotated and color-coding added) below, for example, Kim discloses two rows of guide holes metalized by the conductive portion. On the second or bottom row of the guide holes, for example, the second and the third of the three guide holes referred to as “G” for housing testing pins carrying ground signals are “locally interrupted” because there is a gap on the guide plate between the two guide holes metallized by the “first conductive portion” for housing the ground testing pins. Figure 5b in Kim (not shown below) is similar, illustrating the same type of non-conductive zones that “locally interrupt” the conductive portion that connects the testing pins that

transmit power. What is shown in Figures 5a and 5b in Kim is thus the same as what is shown in Figure 3B of the '885 patent, as described above.



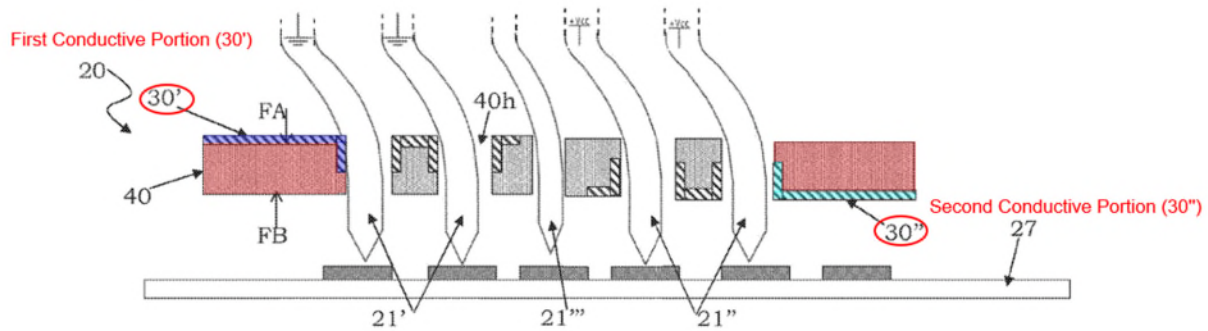
181. Thus, Kim discloses claim 2.

C. Claim 4

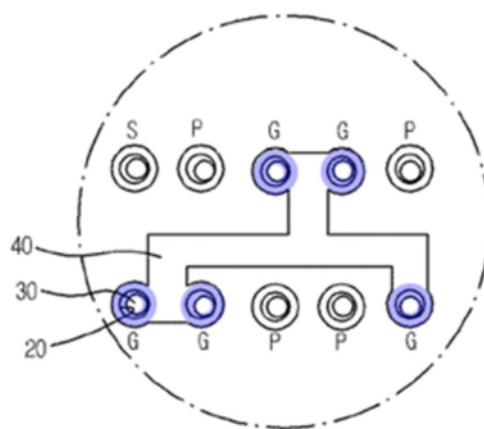
1. **The testing head of claim 1, wherein the first conductive portion is formed on a first face of the at least one guide, and the second conductive portion is formed on a second face of the at least one guide, the second face being opposite to the first face**

182. Claim 4 is disclosed by Kim. Kim discloses the testing head of claim 1. *Supra* § XI(A). Also, the '885 patent describes in the specification and illustrates in Fig. 5A that the guide (40) comprises the first conductive portion (30') formed on the face FA and the second conductive portion (30'') formed on the opposite face FB. Ex. 1001, 12:65-13:3, Fig. 5A (annotated and color-coding added).

FIG. 5A

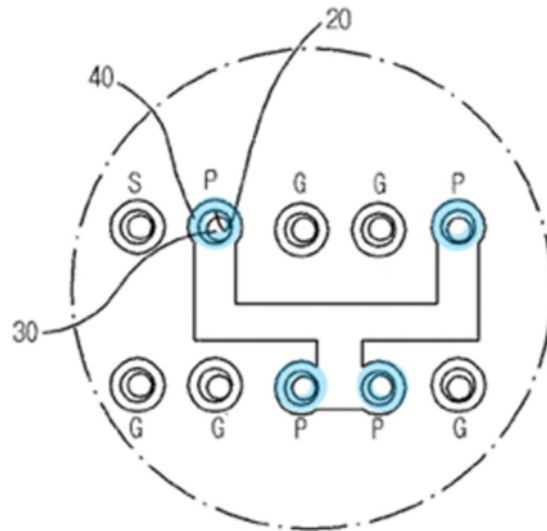


183. First, Kim teaches “the first conductive portion” and “the second conductive portion” are formed on the guide (10). *Supra* § XI(A)(4)(5). Second, Kim illustrates in Fig. 5a and describes that the conductive layers (20) electrically connecting the testing pins (30) transmitting the ground signals are formed on the upper surface of the upper plate (11). Ex. 1006, [0051], Fig. 5a (color-coding added).



184. Kim also teaches and illustrates in Fig. 5b that the conductive layers (20) electrically connecting the testing pins (30) transmitting the power signals are

formed on the lower surface of the same upper plate (11). *Id.*, [0051], Fig. 5b (color-coding added).



185. Thus, Kim discloses claim 4 because Kim teaches that the upper surface of the upper plate (11) constitutes the claimed “first surface” of the “guide,” the lower surface of the upper plate (11) constitutes the claimed “second surface” of the “guide” and the upper surface and the lower surface of the upper plate (11) are “opposite to” each other.

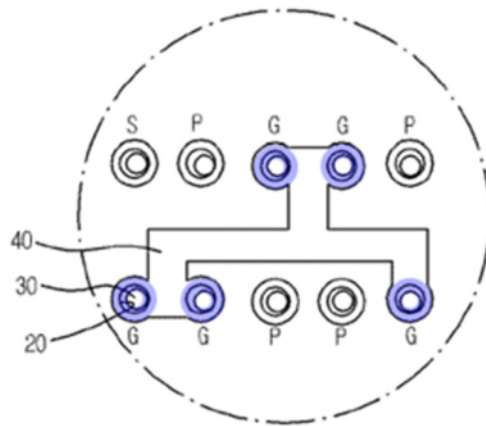
D. Claim 8

- 1. The testing head of claim 1, wherein the first conductive portion covers at least one portion of an inner surface of each guide hole of the first group of guide holes**

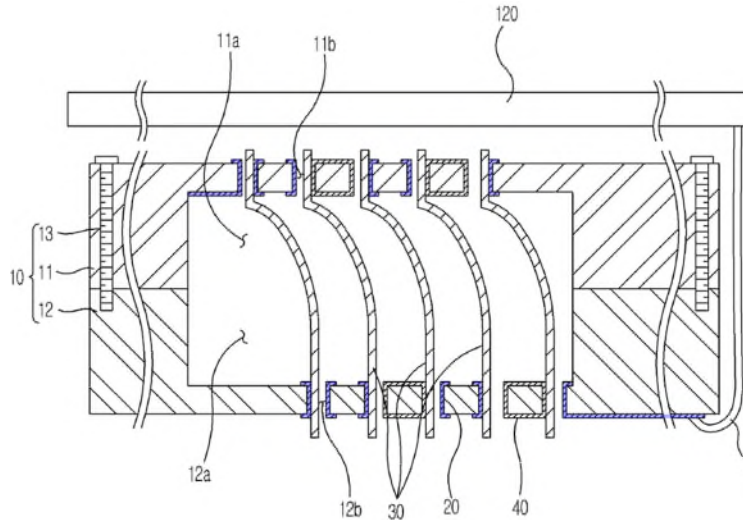
186. Claim 8 is disclosed by Kim. Kim discloses the testing head of claim 1. *Supra* § XI(A). Also, as discussed in claim [1c], Kim teaches the conductive

layers (20) and conductive trace (40), which collectively constitute the claimed “first conductive portion”, have the conductive layer (20) portion in contact with the testing pins (30) carrying ground signals within the “first group of guide holes.” *Supra* § XI(A)(4). Kim explains that the plurality of the conductive layers (20) is formed by coating conductive material on one side of the upper plate (11) where the first guide holes (11b) are formed. *Id.*, [0038]. Kim further explains that the conductive layers (20) are formed on the inner side of the guide holes.

See, e.g., id. at [0017], Fig. 5a (color-coding added).



187. As further illustrated in Fig. 2, Kim clearly depicts that the conductive layers (20) are formed on the inner side of the guide holes (11b) of the upper plate (11) and the guide holes (12b) of the lower plate (12). *Id.*, Fig. 2 (color-coding added).



188. Thus, Kim discloses claim 8 because Kim teaches that some or all of the conductive layers (20), with conductive trace (40), constitute the claimed “first conductive portion” and each of the conductive layers (20) covers at least one portion of an inner surface of each of the guide holes (11b), which constitutes the claimed “first group of guide holes” for housing the testing pins (30) for ground signals.

E. Claim 9

- 1. The testing head of claim 1, wherein the at least one guide comprises at least one common pad connected to the at least one conductive portion by a conductive track**

189. Claim 9 is disclosed by Kim. Kim discloses the testing head of claim 1. *Supra* § XI(A). In understanding the meaning of this claim, I turn to the disclosures of the '885 patent. The '885 patent first discusses “contact pads” generally. As illustrated in Fig. 1, the '885 patent teaches a testing head (1) including a plurality of contact probes (6). Ex. 1001, 1:58-64, Fig. 1 (annotated).

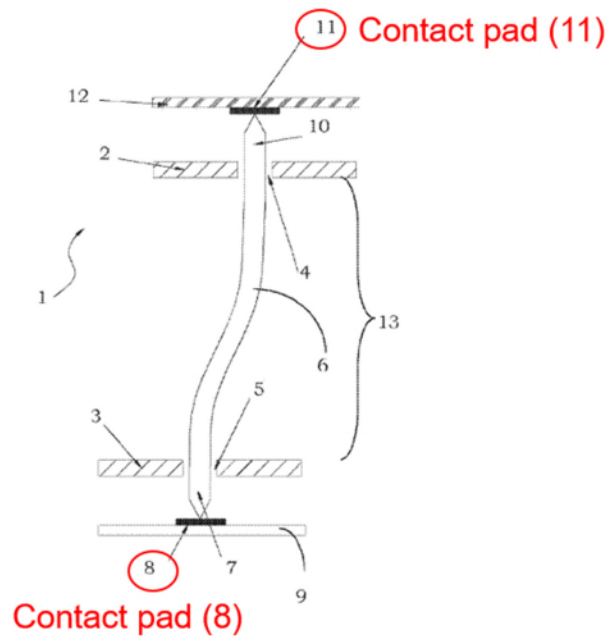


FIG. 1
PRIOR ART

190. With reference to Fig. 1, the '885 patent explains that each contact probe (6) terminates at an end with a contact tip (7) apt to abut onto a contact pad (8) of a device under test integrated on a wafer (9), in order to carry out the mechanical and electrical contact between the device under test and a test equipment (not shown) of which such a testing head is a terminal element. *Id.*, 1:65-2:3. The '885 patent further explains that each contact probe (6) has a further end zone or region which terminates with a so-called contact head (10) towards a contact pad (11) of a plurality of contact pads of a space transformer (12). *Id.*, 2:22-25.

191. The '885 patent is thus describing a “pad” as a terminal for electrical and mechanical connection between devices, which is consistent with how the term “pad” is used in the art generally.

192. The '885 patent then discusses “common pads.” Specifically, the '885 patent describes, as an example, that a common pad (36') may be used to electrically connect the first conductive portion (30') by means of a conductive track (37'). *Id.*, 15:56-60, Fig. 8A (annotated and color-coding added).

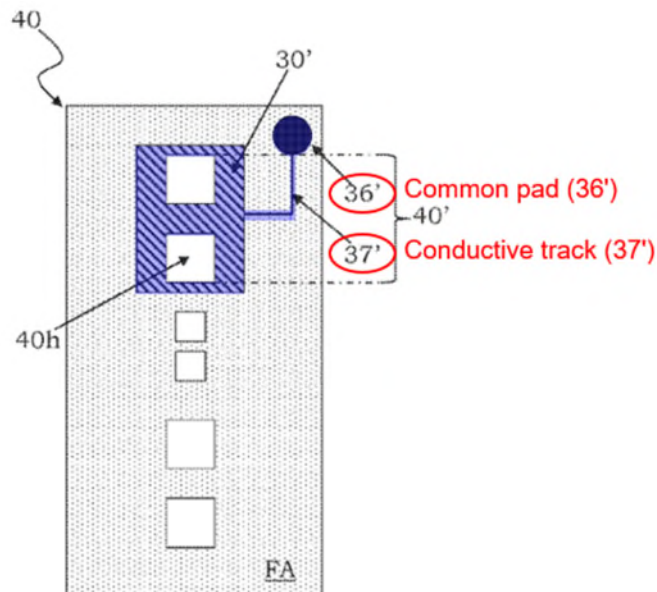


FIG. 8A

193. The '885 states that “the first contact elements 21' apt to carry ground signals are connected to the first common pad 36' by means of the first conductive track 37', the first common pad 36' therefore being a common ground pad.” '885 patent at 15:60-64. The '885 patent further states that “[t]he common pad 36' may

be connected by means of a first connection wire to a housing (not shown) of the testing head 20.” *Id.*, 16:1-3.

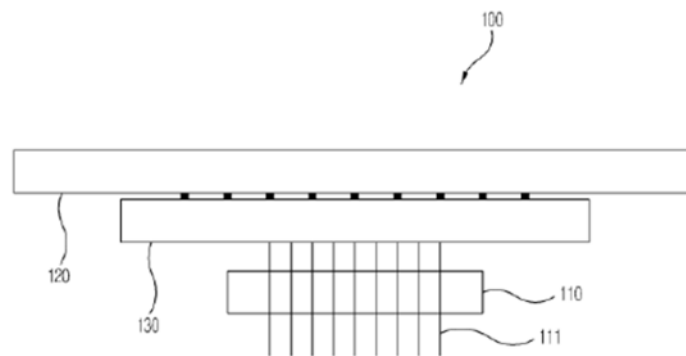
194. The ’885 patent similarly teaches a “common power pad” connected to the second conductive portion (30’’) by means of a second conductive track (37’’) and a “common signal pad” connected to the third conductive portion (30’’) by means of a third conductive track (37’’) such that the second contact elements (21’’) carrying power signals and the third contact elements (21’’) carrying input/output operating signals are connected to the second common pad (36’’) and the third common pad (36’’), respectively. *Id.*, 16:4-21, Figs. 8B and 8C. The ’885 patent explains that the presence of a common pad (36’, 36’’, 36’’) connected to the respective conductive portions (30’, 30’’, 30’’) allows to extract a respective signal from the testing head (20) to a print circuit board (PCB) connected to the testing head (20). *Id.*, 16:22-28.

195. The ’885 patent explains that “the presence of a common pad allows to access to the contact elements *directly from the housing of the testing head*, such a common pad therefore replacing the plurality of contact pads and also allowing monitoring of the respective signals.” *Id.*, 18:9-13 (emphasis added); *see also* 16:22-28 (similar).

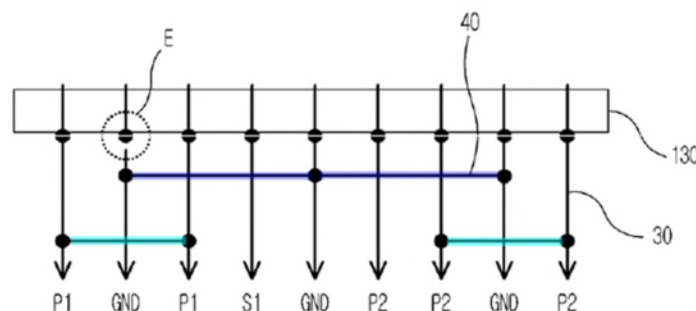
196. Thus, a POSITA would understand that the claimed “common pad” means a terminal for mechanical and electrical contact between two electrical

components that allows access to the contact elements directly from the housing of the testing head.

197. Kim discloses a conventional probe card including a main board (120), a space transformer (130), a guide plate (110) and a plurality of test pins (111). Ex. 1006, [0010], Fig. 1.

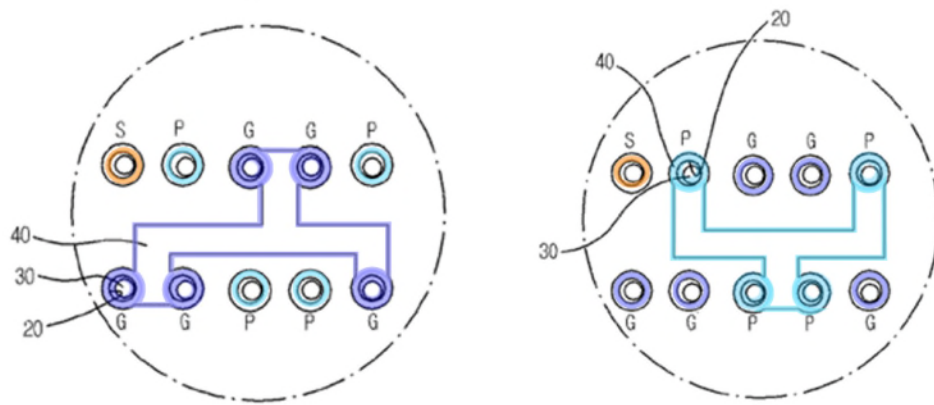


198. Kim also teaches a conductive trace (40) connecting the group of the conductive layers (20) and testing pins (30) carrying a same type of signal. *See, e.g., id.*, [0033], [0038], [0039], [0042], [0043], Fig. 3 (color-coding added).

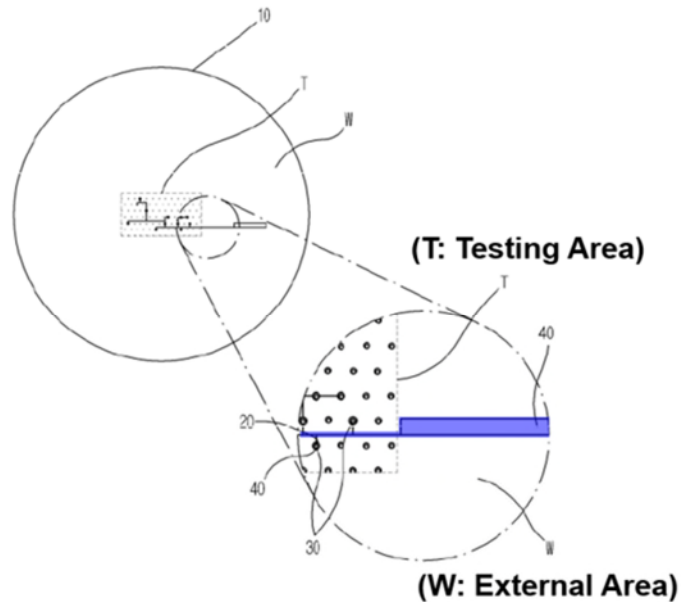


199. Kim teaches, as examples, that a group of conductive layers (20) in contact with the testing pins (30) carrying ground signals are connected by the

conductive traces (40) formed on the upper surface of the upper plate (11), and another group of conductive layers (20) in contact with the testing pins (30) carrying power signals are also connected by the conductive traces (40) formed on the lower surface of the upper plate (11). *Id.*, [0051], Figs. 5a and 5b (color-coding added).



200. In addition, Kim further discloses that the conductive trace (40) can be extended from the testing area (T), where the conductive layers (20) are formed, to the external area (W) on the guide plate (10) where the testing pins (30) are less densely installed. *Id.*, [0046], [0047], Fig. 4 (annotated and color-coding added).



201. Kim explains that the extended conductive trace (40) is designed to be directly connected to the main substrate (120) without the need for any space transformer. *Id.*, [0010], [0048]. Kim further explains that the extension of the conductive trace (40) in the external area (W) also alleviates spatial constraints and allows the formation of a conductive trace (40) with thicker wire connection between the conductive trace (40) and the main substrate, thereby enhancing high-frequency efficiency. *Id.*, [0049].

202. Thus, Kim discloses claim 9 because the conductive trace (40) extended to the external area (W) with a thicker width in the external area for a wire to be connected to the main board constitutes the claimed “common pad” as the conductive trace (40) in the testing area (T) is connected between the conductive layers (20) in contact with the testing pins (30) carrying ground or

power signals and the extended conductive trace (40) with a thicker width in the external area (W), which is a terminal for mechanical and electrical contact between two electrical components that allows access to the contact elements directly from the housing of the testing head (for example, main substrate (120)). The remainder of Kim's extended conductive trace is the "conductive track" which connects that "common pad" to the "at least one conductive portion."

F. Claim 10

- 1. The testing head of claim 1, wherein the at least one guide comprises a further conductive portion at one of the guide holes that is configured to house a single contact element, the at least one guide comprising a common pad connected to the further conductive portion by a conductive track**

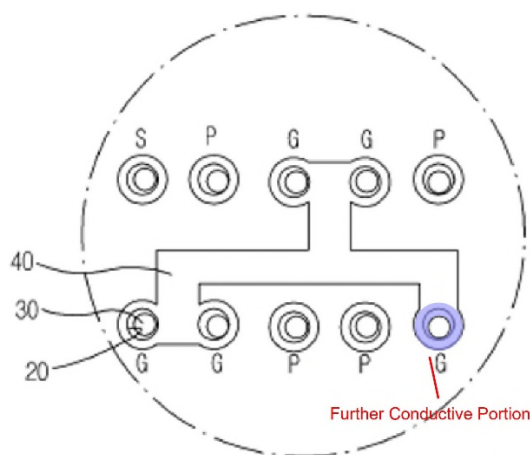
203. Claim 10 is disclosed by Kim. Kim discloses the testing head of claim 1. *Supra* § XI(A).

204. Much of the language of claim 10 mirrors that of claim 9. So, my assessment of claim 9 (including how Kim teaches a "common pad" connected via a "conductive track" to the "conductive portion" that is in contact with and electrically connects the probes for ground or for power) applies to claim 10 as well.

205. Kim also teaches that there is a "further conductive portion at one of the guide holes that is configured to house a single contact element." As described and depicted throughout Kim, the guide holes are configured to house a single

contact element, and there is a conductive portion at the guide holes. I refer, for example, back to my analysis of claim 1 and discussion of the various disclosures of Kim corresponding to those elements of the claim.

206. These disclosures satisfy the first part of claim 10, “wherein the at least one guide comprises a further conductive portion at one of the guide holes that is configured to house a single contact element.” Looking for example at the description of Figure 5a in Kim, the conductive layer 20 at one guide hole is a “further conductive portion at one of the guide holes.” Annotated Figure 5a below shows this with the “further conductive portion” colored in. As explained above with regards to claim element 1[c], two or more of conductive layers (20) at the guide holes for housing ground testing pins, along with some or all of the conductive trace (40) connecting those guide holes, constitute the “first conductive portion” of claim 1. As such, the conductive layer at one of the guide holes for ground is a “further” conductive portion.



207. Thus, Kim discloses claim 10 because (i) a conductive layer (20) in contact with each single testing pin (30) carrying a ground signal within a single guide hole (11b) constitutes the claimed “further conductive portion”, (ii) Kim’s conductive trace (40) extended to the external area (W) with a thicker width on the guide plate (10) constitutes the claimed “common pad,” (iii) the remainder of Kim’s extended conductive trace is the “common track,” and (iv) the “further conductive portion” (conductive layer 20) is connected to the conductive trace (40) in the testing area (T), which is connected to the “common track,” which in turn is connected to the “common pad,” such that the common pad is connected to the further conductive portion by a common track.

G. Claim 11

- 1. The testing head of claim 1, wherein the at least one guide comprises a further conductive portion at one of the guide holes that is configured to house a single contact element, the at least one guide comprising a conductive track that connects the conductive portion to other conductive portions**

208. Claim 11 is disclosed by Kim. Kim discloses the testing head of claim 1. *Supra* § XI(A). Also, Kim teaches “a further conductive portion at one of the guide holes that is configured to house a single contact element.” This language mirrors the language in claim 10, and as I discuss above with respect to claim 10, the conductive layer 20 at one of the guide holes, *e.g.*, one of the guide

holes housing a ground testing pin in Figure 5a, is a “further conductive portion at one of the guide holes that is configured to house a single contact element.”

209. The '885 patent further explains that it is possible to provide that at least two conductive portions such as two first conductive portions (30') of the guide (40) are electrically connected to each other by means of a conductive track (39) in the guide, so as to be able to electrically connect to each other groups of contact elements apt to carry a same type of signal but that are housed in respective groups of guide holes distanced from each other in the guide. Ex. 1001, 16:49-59, Fig. 9B (annotated and color-coding added).

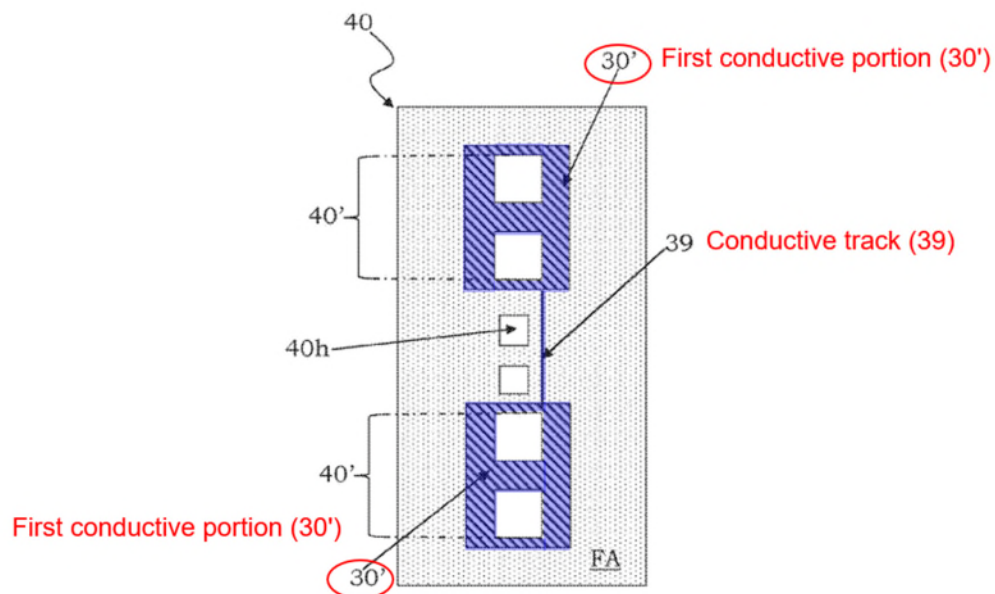
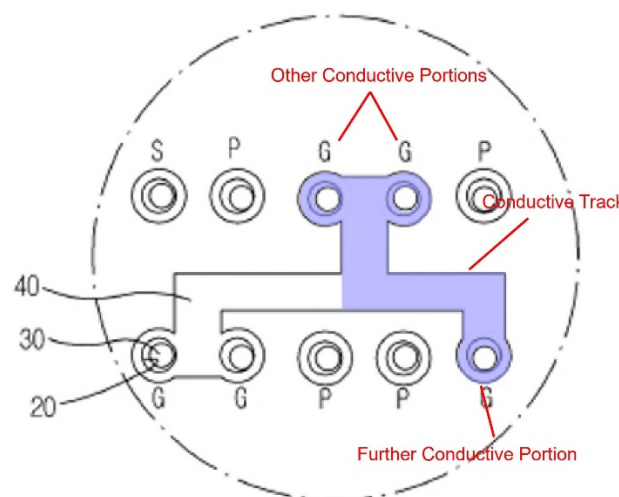


FIG. 9B

210. As shown in Figure 9B of the '885 patent above, the contiguous conductive material (30' at the top, 39, then 30' at the bottom) is labeled as “first

conductive portion,” “conductive track,” and then “first conductive portion” again. A POSITA would understand from this disclosure then that a “conductive track” can be part of one continuous stretch of conductive material between a guide hole or group of guide holes housing contact elements carrying the same type of signal.

211. Returning to Figure 5a of Kim, Kim discloses that the conductive layer (20) at the bottom right guide hole, the “further conductive portion” as discussed above,” is electrically connected “to other conductive portions,” for example, the conductive layers (20) at the two upper guide holes. The conductive trace (40) connecting the “further conductive portion” and the “other conductive portions” is a “conductive track.” This is illustrated in the annotated and color-coded Figure 5a below.



212. What is shown in Figure 5a of Kim is the same as what is shown in Figure 9B of the '885 patent, in that conductive portions around sets of one or more guide holes are electrically connected by a conductive material which is a “conductive track.”

213. Thus, Kim discloses claim 11.

H. Claim 14

1. **The testing head of claim 1, further comprising at least one conductive track that electrically connects the first and second conductive portions including and electrically connecting the holes of the first and second groups of the guide holes to each other, the contact elements included in the second group being configured to carry the first type of signal**

214. Kim discloses the testing head of claim 1. *Supra* § XI (A).

215. From the language of claim 1 and the teachings of the '885 patent, a POSITA would understand that the claimed “first and second types of signals” recited in claim 1, on which claim 14 depends, must be *two different* types of signals “chosen |between ground signals and power signals.” *See id.*, claim 1. And, in turn, the “first conductive portion that includes and electrically connects a first group of guide holes” and the “second conductive portion that includes and electrically connects a second group of guide holes” each transmit different types of signals, one ground and one power. That is what the claim itself says in the “chosen between ground signals and power signal” clause. Also, in Section VIII

above I discuss the prosecution history of the '885 patent and its foreign counterpart applications in some detail, and as I noted there, the claims were amended in view of prior art rejections to specify that both ground contact elements are electrically connected to each other and power contact elements are electrically connected to each other.

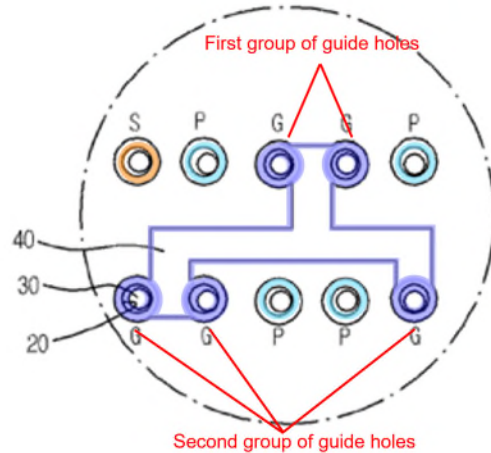
216. According to the specification of the '885 patent, the testing head (20) of the '885 patent was designed to short-circuit or electrically connect the guide holes for housing contact elements carrying a *same* type of signal. *See, e.g., id.*, 7:49-55, 17:34-38 (emphasis added). The '885 patent explains that short-circuiting contact elements carrying a same type of signal reduces noise in input/output signals and improves frequency performance. *See, e.g., id.*, 7:49-55, 17:39-46, 47-60. The '885 patent also teaches that “the at least one conductive portion can be separated from further conductive portions and/or can be locally interrupted by at least one non-conductive zone, so as not to allow an electrical connection between contact elements apt to carry a different type of signal and/or contact elements which must not be short-circuited.” *Id.*, 3:56-62. These passages are consistent with what a POSITA would readily understand: electrically connecting two sets of contact elements with *different* types of signals would not only undesirably affect the function of those contact elements, it may cause shorting or invalid test results.

217. Regardless of the claim language in claim 1, claim 14 recites a “conductive track that *electrically connects* the first and second conductive portions.” Claim 14 also recites “contact elements included in the second group being configured to carry the first type of signal.” Thus, a POSITA would understand that claim 14 is in conflict and inconsistent with claim 1. The “second group” of contact elements cannot carry both the “second type” of signal as in claim 1 (*e.g.*, power) and the “first type” of signal as in claim 14 which depends from claim 1 (*e.g.*, ground). And contact elements carrying ground and power cannot be electrically connected to each other. The boundaries of claim 14 are thus not reasonably certain to a POSITA given these inconsistencies, and I understand that means claim 14 is indefinite.

218. Notwithstanding the inconsistencies in claim 14, if the claim is interpreted to be definite, then Kim discloses the claim.

219. As illustrated in Fig. 5a, Kim teaches a plurality of conductive layers (20) electrically connecting a plurality of guide holes (11b) formed on and within the upper plate (11) for housing a plurality of testing pins (30) carrying the same type of ground signals. The plurality of the guide holes constitutes a “first” and “second” group of guide holes, which are electrically connected by the “first” and “second” conductive layers housed within those guide holes, and the contact elements within those guide holes are configured to carry “the first type of signal”

(ground). The two groups of guide holes are electrically connected by a “conductive track,” which is conductive trace 40 (in whole or in part). As I explained already in connection with Claim 11 above (*supra* § X.G), the conductive trace 40 connecting the conductive portions in and around groups of guide holes is a “conductive track” in the same way that the ’885 patent uses that term. Ex. 1006, [0051], Fig. 5a (annotated and color-coding added).



220. Accordingly, if the claimed “first and second types of signals” in claim 14 are interpreted to mean the same type of signal, then Kim anticipates claim 14.

XI. GROUND 2: KIM RENDERS CLAIMS 1-2, 4, 7-11, AND 14 OBVIOUS

A. All of Claims 1-2, 4, 8-11, and 14

221. Kim discloses the testing head of claims 1-2, 4, 8-11, and 14. I am informed that a reference, like Kim, that anticipates a claim also renders that claim

obvious. For that reason, it is my opinion that Kim also renders obvious claims 1-2, 4, 8-11, and 14.

222. In addition, if Technoprobe argues or the Board finds that Kim does not disclose any of claims 1-2, 4, 8-11, or 14, it is my opinion that a POSITA would nonetheless find those claims obvious in light of Kim's disclosures. Further, Kim also renders claim 7 obvious.

223. This section provides some bases for my opinions that would apply to any of claims 1-2, 4, 7-11, and 14. I also discuss below some additional specific opinions relevant to claims 2, 7, 9, 10, and 11.

224. As I explained previously, although the terminology used in Kim and the '885 patent is not always the same, a POSITA would understand that in the semiconductor testing industry, many different terms can be used to refer to the same device or type of device. For example, the terms "contact," "probe," "contact probe," "pin," "testing pin," "probe needle," and "contact element" are among the terms that a POSITA might use to describe the devices that are housed in the guide holes and connect the device under test at one end to the tester through the test head at the other end. Kim and the '885 patent themselves describe synonyms for these terms. The same is true for other terminology differences between Kim and the '885 Patent – for example, "conductive trace" and "conductive layer" versus "conductive track" and "conductive portion," these terms are not being used to

describe substantively different structures. At the very least, if it is argued that the any differences in terminology between Kim and the '885 patent mean that Kim does not anticipate the '885 patent, a POSITA would have understood that these differences are not material, that the '885 patent is describing a testing head comprised of known components and structures, and whatever differences would have been at most obvious variants on Kim to a POSITA.

225. I also explained above how Kim is describing the same type of semiconductor testing device as described and claimed in the '885 patent. Kim also explains that its described systems are not limited to the probe card context: “the present invention is not limited to the probe card” and instead it may be applied to “all semiconductor testing apparatus having multiple test pins.” *Id.*, [0031]. The '885 patent describes and claims a “semiconductor testing apparatus having multiple test pins.” So, if Technoprobe argues that Kim does not anticipate because the '885 patent claims a different type of device than that described in Kim (and I would not agree with such an argument), Kim still would render the claims obvious to a POSITA because a POSITA would have understood that Kim’s teachings could have been applied or adapted to the context of the devices claimed in the '885 patent.

226. Kim describes “FIG. 2 through FIG. 6” as “the semiconductor testing apparatus 1 according *to one embodiment* of the present invention.” *Id.*, [0033]

(emphasis added). Accordingly, a POSITA would understand these Figures and their accompanying descriptions to not be describing different, separate embodiments, but rather as illustrative of different aspects of the same embodiment or system. For example, Figures 5a and 5b in Kim are intended to illustrate how different pins are connected. They obviously are not showing the exact layout of an entire trace (*e.g.*, they only show one signal pin, and the operative device of course would have many more). For that reason, in my analysis of anticipation by Kim, I have cited to various descriptions in Kim.

227. If, however, Technoprobe contends that Kim is describing different embodiments (and I would not agree), at minimum it would be obvious to a POSITA to combine the teachings of those different embodiments in Kim as I have explained. There is nothing in Kim that suggests its teachings *cannot* be combined, and a POSITA would have had reasons to combine those teachings to achieve the full scope of benefits Kim describes. As one example, a POSITA would have understood that the conductive trace as depicted in Figures 5a and 5b of Kim could have been extended to an external area W, as depicted in Figure 4 of Kim, to yield the benefits of improving workability and high frequency performance like Kim describes for Figure 4.

228. Kim says in paragraph [0001], “The present application claims the benefit of Korean Patent Application No. 10-2014-0004576 filed in the Korean

Intellectual Property Office on 14 Jan. 2014, the entire contents of which are incorporated herein by reference.” I understand that this Korean patent application issued as Korean patent KR10-1384714, which is attached as Ex. 1004 to the Petition, and that a certified copy of is attached as Ex. 1005, which I refer to as “Kim KR.”

229. I have reviewed Kim KR, and in light of Kim’s incorporation by reference of Kim KR, a POSITA also would have looked to the contents of Kim KR as relevant to understanding Kim’s disclosures.

230. Kim KR is very similar to Kim. The Figures appear to be the same between Kim KR and Kim, and the content of the description also seems to be largely if not entirely identical. I do not see any inconsistencies in the descriptions of Kim KR and Kim that would affect my analysis. Kim KR confirms and supports my understanding of Kim.

231. For example, Kim KR describes Fig. 5b as follows: “Similarly, as shown in Fig. 5b, a plurality of conductive layers (20) in contact with *the power test pins (30b)* and the conductive traces (40) connecting the same are formed on the lower surface of the upper plate (12).” Ex. 1005, [0044] (emphasis added). I explained already that a POSITA would understand that the “P” testing pins in Kim transmit power. So, if there is any doubt about whether Kim expressly or inherently discloses electrically connecting *power* contact elements (and their

respective guide holes) in addition to ground contact elements, Kim KR confirms that Kim does disclose this, and thus this element at least would have been obvious to a POSITA in view of the teachings of Kim as further informed by Kim KR.

232. Other aspects of Kim KR also inform my analysis as discussed in this declaration.

B. Claims 2, 9, 10, 11, and 14

233. As described previously, claims 2, 9, 10, 11 and 14 (if claim 14 is interpreted such that it is not indefinite) all essentially describe different ways of patterning the conductive material on the guide plate in order to create specific electrical connections (“locally interrupting” a conductive portion with a non-conductive zone or adding a “further conductive portion,” a “common pad,” or connections between conductive portions via a “common track”).

234. A POSITA with general knowledge in the art in view of Kim would understand how to form, arrange, divide or pattern one or more groups of the conductive portion or portions on one or both sides of one or more guide plates in whatever way necessary and best suited to the needs of a particular product or application. Indeed, as I explained in the “Background” Section VII above, within the overall architecture of a given probe card model, the specific design parameters (*e.g.*, number and location of I/Os, signal and power routing, loop-back circuits, etc.) is usually unique to a particular chip design.

235. As a general matter, a POSITA would have been aware of printed circuit board technologies where two or more wires or traces transmitting different signals are formed on the same surface of a non-conductive substrate without electrically connecting to each other and the wires transmitting the same type of signals are electrically connected on the other side of the substrate using through holes and conductive trace. *See, e.g.*, U.S. 5,225,777 (Ex. 1010, “Bross”) (teaching that “forcing a multitude of wire-like probe elements through the vias to make selected electrical contact with portions of the conductive layers” at 3:15-17, and further teaching that “a multi-layer arrangement with a different number of layers or of different designs from that disclosed may be employed” at 7:46-48).

236. The ’885 patent identifies possible materials for the guide plates (40, 41, 42): “The guide 40 is made of a non-conductive material, for example a ceramic material such as silicon nitride, or of a glass or silicon-based material, or of a polyamide material, or of any other suitable dielectric material.” Ex. 1001, 6:25-28. Though these specific materials are well known in the art, stating them makes clear that no specific material is required for the guide plates. A POSITA is familiar with these types of materials.

237. The ’885 patent also acknowledges that “[c]onductive structures apt to electrically connect contact probes to each other are disclosed for example in US 2012/0242360 A1, KR 101 421 051 B1, US 2014/0197860 A1, and WO

2012/106220 A1.” *Id.*, 2:64-67. One of these references is the ’051 Reference discussed above.

238. U.S. Pub. No. 2014/0197860 (Ex. 1012, “Hsu”), which also is acknowledged as prior art in the foregoing passage of the ’885 patent, further shows that it was well known in the art to short-circuit a group of contact elements carrying a same type of signal depending on the current value, probe diameter, pitch between adjacent contact pads of the device under test to avoid possible burning of the contact elements due to an unexpected excessive instantaneous current running through the contact elements. *See, e.g.*, Ex. 1012, [0003], [0006], [0026]-[0029], [0035], Fig. 5 (teaching a vertical probe card with two current-diverting guide plates (20) electrically connecting testing probes (22) via conductive layers (40) formed in the through holes (36) to address the issue of probe burning.).

239. Accordingly, the ’885 patent explicitly acknowledges that using metalized guide plates to electrically connect contact probes were a known, prior art technology.

240. However, the ’885 patent is silent on the method for fabricating the metallization on the surface, interior, and holes of the guide plates. Lacking this disclosure, a POSITA would conclude that typical and well-known processes, like those used to fabricate conductive patterns, traces, hole plating, etc. on printed

circuit boards or other substrates, are employed to apply the metallization on the '885 patent's guide plates.

241. Those common processes have regularly been employed to produce circuit patterns (and an insulating coating) required by a particular design (traces, power/ground planes, plated through-holes, test pads, etc.) on printed circuit boards, substrates, etc., all being dielectric materials. So, having a variety of circuit patterns on guide plates is not new.

242. Kim also discloses several processes for applying metallization to the guide plates: "In the meantime, the conductive layer 20 and the conductive trace 40 according to one embodiment of the present invention can be manufactured by the following various method." Ex. 1006, [0056].

243. "In the first method, after the conductive material is plated or deposited on the entire surface of the guide plate 10, a photoresistor film is formed on an area for forming the conductive layer 20 and conductive trace 40 among the plated or deposited conductive materials. Then, unnecessary areas among the conductive materials formed on the entire surface of the guide plate 10 are removed through an etching solution, so that it forms the conductive layer 20 and conductive trace 40." *Id.*, [0057].

244. "In the second method, after a photoresistor is partially formed on the surface of the guide plate 10, in that the forming of the conductive layer 20 and

conductive trace 40 is unnecessary, the conductive material is entirely plated or deposited thereon. Then, the conductive materials formed on the photoresistor are removed through a lift-off method, so that it forms the conductive layer 20 and conductive trace 40 in the desiring shape.” *Id.*, [0058].

245. “In the third method, after a screen is arranged on the surface of the guide plate 10, in that the forming of the conductive layer 20 and conductive trace 40 is unnecessary, the conductive material is deposited thereon, so that it forms the conductive layer 20 and conductive trace 40 in the desiring shape. Here, the seed layer is formed on the area in which the screen is not arranged and the conductive layer 20 and conductive trace 40 can be formed through the electroplating method etc.” *Id.*, [0059]-[0060].

246. “In the last method, the conductive materials are deposited on the entire surface of the guide plate 10 and then, the conductive materials are selectively removed from the surface of the guide plate 10 through the machining, so that it forms the conductive layer 20 and conductive trace 40 in the desiring shape.” *Id.*, [0061].

247. Kim KR also discloses “the present invention is not limited to forming each group only on the upper surface and lower surface of the upper plate (11). Depending on the number of groups, it is possible to form more than one electrically connected group on a single surface.” Ex. 1005, [0045]. Likewise,

Kim teaches that the position of the conductive groups is not limited: “each group can be formed at the upper surface and the lower surface of both upper and lower plates 11 and 12 according to the number of groups.” Ex. 1006, [0052] (I note that Ex. 1006 at [0052] has a typo where “not” is missing from the text before “limited,” but it is clear from the context that “not” is what is intended.) It is of note that Kim says that “each” group can be formed at the upper / lower surface, which tells a POSITA that there is flexibility of placement. Kim further teaches that it may have “one or more conductive traces formed at one side of a surface of the guide plate.” *Id.*, [0017]. A POSITA would thus understand that Kim’s system may be implemented with more than one group of electrically connected guide holes on one side of a guide plate.

248. As further evidence of this point, the conceptual diagram of Figure 3 depicts two separate electrical connections of two separate groups of power testing pins, labeled respectively as P1 and P2, in addition to the electrical connection of the ground. A POSITA would understand that some chips being tested would require the wafer probe to have two different types of power contact probes, for example, power probes with different voltages. Accordingly, this device would have at least three different electrical connections—at least one for ground and at least two for power—so there would need to be either more than one electrical

connection on one side of a guide or electrical connections on both the upper and lower guides.

249. For all these reasons, to the extent Patent Owner argues that Kim does not expressly or inherently teach the limitations of dependent claims 2, 9, 10, 11, and 14 of the '885 patent, these limitations specifically reciting “locally interrupting” a conductive portion with a non-conductive zone or adding a “further conductive portion,” a “common pad,” or connections between conductive portions via a “common track” would have been nothing more than routine design choices to implement what are disclosed in Kim well within a POSITA’s skill, knowledge, and creativity. Such routine design choices are nothing more than the design choices using metallization in a printed circuit board and/or other types of substrates on which circuit designs are formed.

250. Regarding claim 2 specifically, Kim teaches an embodiment where a portion of the conductive material is removed such that “the testing pins 30 for signal or the testing pins 30 for power are insulated with the testing pins 30 for ground.” *Id.*, [0062]. A POSITA would understand from this disclosure and the other teachings of Kim discussed above that it would be obvious to pattern the metallization on the guide plate to “locally interrupt” the conductive portions to isolate testing pins carrying different types of signals (*e.g.*, power pins and ground pins) from each other.

251. Regarding the “common pad” limitations of claims 9 and 10, the ’885 patent explains that “the presence of a common pad allows to access to the contact elements directly from the housing of the testing head, such a common pad therefore replacing the plurality of contact pads and also allowing monitoring of the respective signals.” Ex. 1001, 18:9-13. A POSITA would understand from the teachings of the ’885 patent that the claimed “common pad” allows an external electrical component or device (*e.g.*, PCB) to electrically access or monitor a signal carried by a group of test pins carrying the same type of signal without connecting the external electrical component or device to the plurality of contact pads. The ’885 patent does not disclose what the plurality of contact pads it is referring to (DUT, space transformer, etc.). The ’885 patent illustrates a plurality of contact pads in (for example) Fig. 2A, where the space transformer 29 has a plurality of contact pads 28, and the plurality of contact pads 26 for the device under test: “the contact pads 26 and 28 of the device under test and of the space transformer 29. *Id.*, 8:1-2. Thus, a POSITA would understand the plurality of contact pads to be either on the device under test or the space transformer, and those pads carrying the same type of signal are electrically connected to a common pad on the guide plate.

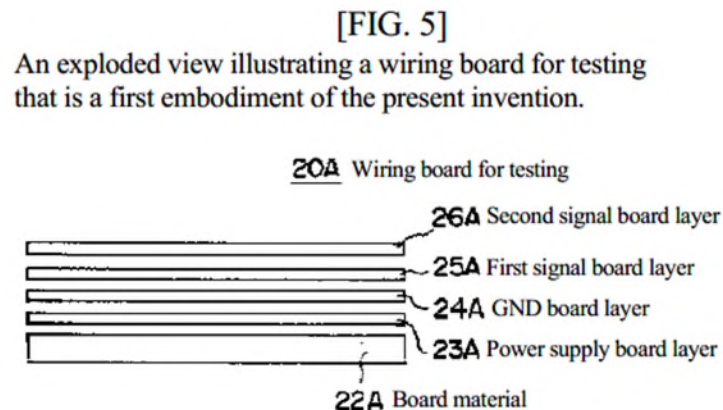
252. Turning to the disclosures of Kim, a POSITA would have understood that the extended portion of the conductive trace (40), extended from the testing area (T), where the conductive layers (20) are formed, to the external area (W) on

the guide plate (10) would have been used as a “common pad” to replace a direct electrical connection between an external electrical component or device and a plurality of contact pads of the device under test. At minimum, this would have been an obvious use and implementation of the extended conductive trace disclosed in Kim. Kim explicitly teaches that “the high conductive trace 40 can minimize the signal transduction route through the testing pin 30 with a high impedance and the signal transmitted to the testing pin 30 can be directly transmitted to the main board 120 through the thick wire J, so that the noise is minimized, thereby remarkably improving the high frequency performance thereof.” Ex. 1006, [0054]. A POSITA would have understood that this “common pad” in Kim could have been used for signal or power transmission, as disclosed in this passage, or for monitoring purposes.

253. Pads like the “common pad” claimed in claims 9 and 10 are common in probing systems and would have been well-known to a POSITA, for example for use in monitoring. As a POSITA would have known, the dimensions of a testing head are very small, with vertical probes often separated by spaces on the order of 100 microns or less. More space is available on the PCB or other components of the testing head, and accordingly, a common testing pad was known to be advantageous to enlarge the trace to probe. It was well-known in the art to use a contact pad transmitting signals carried by testing pins or contact

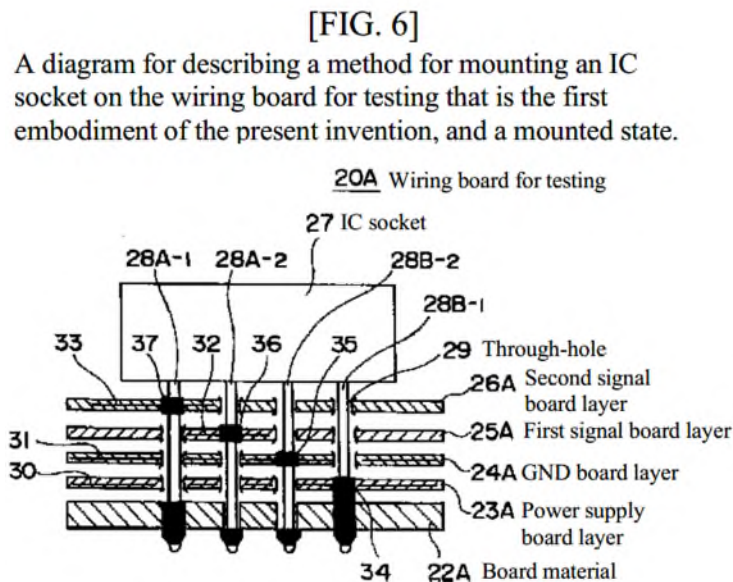
elements through a wire to an external electrical component for monitoring or testing purposes.

254. One relevant example is disclosed in Tezuka (Japanese Patent Publication No. H11-352182, Ex. 1007, certified English translation at Ex. 1008, “Tezuka”) which was filed on June 10, 1998 and published on December 24, 1999. Tezuka is directed at a wiring board for testing semiconductor device. *See, e.g.*, Ex. 1007, [0001]. Specifically, Tezuka discloses a wiring board for testing (20A) including four substrate layers including a first signal board layer (25A), a second signal board layer (26A), a GND (*i.e.*, ground) board layer (24A) and a power supply board layer (23A). *See, e.g., id.*, [0019], Fig. 5.

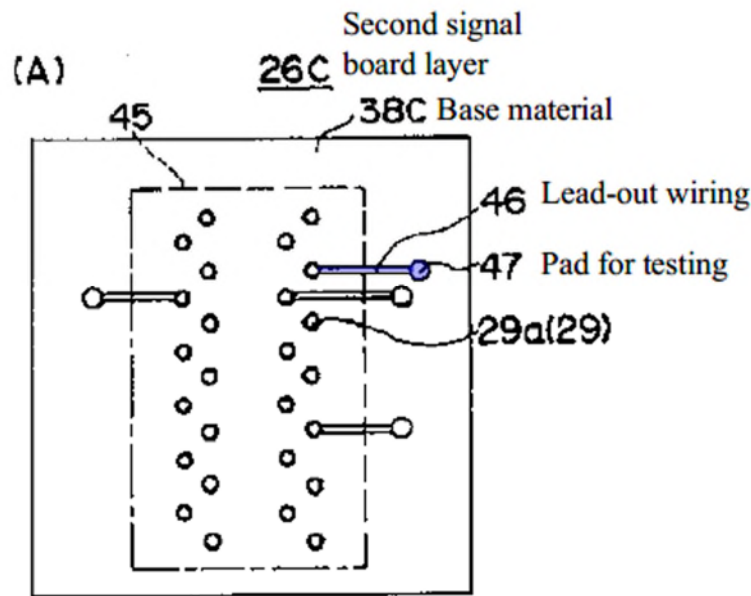


255. Tezuka goes on to teach a plurality of through holes (29) vertically penetrating each of the four board layers (23A-26A). *Id.*, [0020]. Tezuka explains that connecting portions (34-37) are formed in the through-holes (29) by soldering

and the leads (28A, 28B) can be electrically connected to each of the four board layers (23A-26A). *Id.*, [0021], [0022], Fig. 6.



256. Tezuka further teaches a lead-out wire (46) and a pad for testing (47). *Id.*, [0039]. Tezuka explains that the lead-out wire (46), which is formed collectively with the second wiring pattern (33) on the second signal board (26C), is extended to an area outside of the socket (27). *Id.*, [0039], Fig. 9A. Tezuka also explains and illustrates in Fig. 9A that the pad for testing (47) is formed at the end of the lead-out wire (46) for detecting defect of each semiconductor device mounted on the socket (27). *Id.*, [0039], [0040], Fig. 9A (color-coding added).



257. Additionally, a POSITA would understand from the teachings of Kim that the wafer probe card as taught by Kim and the socket-type testing device as taught by Tezuka are in the pertinent art. *See* Ex. 1006, [0013] (teaching that the problem that Kim intended to solve applies to “not only the probe card but also the *test socket* etc.”) (emphasis added); *see also id.*, [0041] (teaching that “in the present embodiment, the guide plate includes the upper plate 11 and the lower plate 12. However, the guide plate can be formed with one body like a socket housing of a *test socket*.”) (emphasis added).

258. Both Figure 4 of Kim and Figures 8a through 8c of the ’885 patent depict the “common pad” as a conductive portion on the guide plate made out of the same material as the conductive portion that connects the testing pins or contact elements. The ’885 patent depicts this as circular in shape, while in Kim the

extended trace is rectangular in shape, but a POSITA would have understood that the “common pad” could be patterned in whatever shape was most appropriate for the application. Indeed, Tezuka shows a known example of a circular common pad. To the extent that Technoprobe argues that the “common pad” must have a certain shape, then, that shape would have been obvious to a POSITA.

259. As the limitation of claim 10 reciting that the common pad is connected by a “conductive track” to a “further conductive portion at one of the guide holes that is configured to house a single contact element,” to the extent Patent Owner argues that this limitation requires only a single contact element be electrically connected to the common pad, Kim teaches or at least would render claim 10 obvious. Kim explicitly teaches that “a testing pin is rendered to electrically connect to another testing pin or an external substrate through a conductive layer formed in the guide hole.” *Id.*, Abstract, [0003], [0015]. It is clear from the teachings of Kim that one or more, or any number of testing pins may be electrically connected to the “common pad” through a “conductive track.” It would have been a routine design choice to a POSITA to determine how many testing pins are thus electrically connected (single or multiple) depending on which type of signal(s) or testing pin(s) carrying the signal(s) the designer intended to watch or monitor.

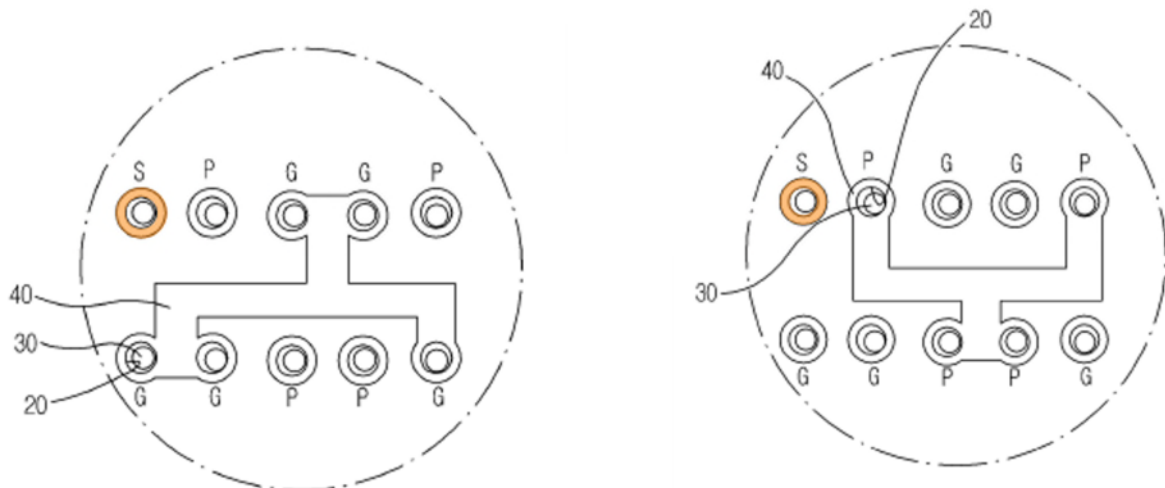
260. The '885 patent does not explain the dimensions of a “conductive track” or indicate that the width or length of the conductive track is relevant or important. As discussed above in Section X.G, the “conductive track” in the '885 patent can be part of one continuous conductive material that connects other “conductive portions” or “common pads.” The “conductive track” illustrated in some figures of the '885 patent, as drawn, appears to be somewhat “thinner” than the “conductive track” illustrated in some Figures of Kim. But to the extent Technoprobe argues that the “conductive track” claimed in the '885 patent differs from what is disclosed in Kim, or that Kim’s conductive portions on the guide plate somehow are not a “conductive track,” a POSITA would have understood the requirements of a “conductive track” connecting two other conductive portions to be an obvious design choice. As discussed above at length, a POSITA would have understood that the metallization pattern on the guide plate could be laid out in whatever arrangement makes the most sense for a particular application, and that includes a “track” between two other conductive elements of the appropriate width. This rationale would apply to all the claims reciting a “conductive track.”

C. **Claim 7**

1. **[7] The testing head of claim 1, wherein the at least one guide includes at least one third conductive portion that includes and electrically connects a third group of the guide holes to each other and house third contact elements configured to carry input/output signals between the device under test and a test equipment.**

261. Kim at least renders obvious this limitation. Claim 7 depends on claim 1. As to the limitation of claim 7, the '885 patent describes in the specification and illustrates in Fig. 2C that guide (40) further comprises a third conductive portion which electrically connects a third group of guide holes housing third contract elements carrying input/output signals. Ex. 1001, 9:11-26; Fig. 2C.

262. First, Kim discloses a conventional probe card (100) including a plurality of test pins (111) electrically contacting the chips to be tested. Ex. 1006, [0007]. Without limiting a specific type of signal, Kim explains that it applies to the testing pins transmitting *identical* or the *same* signals. *See id.*, [0019], [0025], [0032], [0042], [0044], [0045] (emphasis added). From Kim's teachings, a POSITA would understand that the groups of testing pins (30) carrying ground signals and power signals are provided only as examples. For example, Figs. 5a and 5b depict three groups of guide holes for "S," "P" and "G."



Id., Figs 5a and 5b (color-coding added).

263. A POSITA would understand from Kim's teachings that the guide hole referred to as "S" means at least a guide hole, which is formed on the guide plate (10), for housing a contact element carrying an input and output signal. It would be obvious to a POSITA that Figures 5a and 5b illustrate just a portion of a guide plate. A POSITA knows that devices/chips being tested contain more than one signal contact pad to be contacted by the probe card. Thus a POSITA would also know that a probe card's guide plates contains more than one signal guide hole. Kim further explains in another embodiment that the testing pins (30) for signals are insulated from the testing pins (30) for ground signals. *Id.*, [0062]. Thus, it would be obvious to a POSITA that Kim's testing pins (30) could have included a plurality of testing pins (30) carrying input and/or output signals in addition to the testing pins (30) carrying ground and power signals. A POSITA

would understand that the test pins (30) for ground signals and power signals as taught by Kim are used only as examples to illustrate that pins carrying the same signal can be grouped together via a conductive trace (conductive layer), where the grouping of input/output signals also would be possible.

264. Indeed, Kim explicitly explains the possibility of having the conductive trace on each of the sides of both the upper and lower die, hence 4 separate traces. *See id.*, [0018]. Kim further explains that “[p]referably, the conductive trace is electrically connected between the conductive layers with which *the testing pins of transmitting the same signal* are contacted” (*id.*, [0019] (emphasis added)); “since the conductive trace 40 ... *allow the plurality of the conductive layers 20*, with which the plurality of *testing pin 30 of transmitting the same signal* is contacted, *to be connected to each other*[.]” *Id.*, [0045] (emphasis added). The electrically connected group is not limited to one group such as the group for ground or power test pins (30), and both upper surface and lower surface of both the upper plate (11) and lower plate (12) allow forming more than one electrically connected group of test pins. *Id.*, [0052]. A POSITA would understand from Kim’s teachings that the conductive layers (20) as a “third conductive portion” is formed within and electrically connect certain guide holes (11b) as a “third group of guide holes” for housing test pins (30) carrying

“input/output signals” between the transformer (130) and the Device Under Test (DUT). *See id.*, [0009].

265. A POSITA would have had a reason to electrically connect these signal testing pins in Kim to improve performance in fulfilling certain testing requirements, such as with loop-back testing. Kim teaches that one object of the invention is to “provide a semiconductor testing apparatus in that a signal transduction length becomes short and an impedance is decreased, so that it can remarkably improve the high frequency performance.” *Id.*, [0016]. Electrically connecting two or more of the input/output testing pins would achieve this object, and furthermore, that connection would also permit the input/output testing pins to be connected directly to the main board as in the embodiment of Figure 6, further achieving this objective. *See id.*, [0048], [0064].

266. Thus, claim 7 is unpatentable as being obvious over Kim.

XII. GROUND 3: KIM AND SCHMID RENDERS CLAIMS 5-6, 16-20 AND 23 OBVIOUS.

267. All elements of claims 5-6, 16-20 and 23 are disclosed by the combination of Kim and Schmid and a POSITA would have been motivated to combine the references.

A. Motivation to Combine

268. This section provides an overview of the reasons why a POSITA would have been motivated to combine the disclosures of Kim and Schmid in a

way that would yield the alleged inventions claims in '885 patent claims 5-6, 16-20 and 23, and also explains why a POSITA reasonably would have expected success in doing so. This section applies to my assessment of the obviousness of claims 5-6, 16-20 and 23 set out in the sections that follow. Those sections also have further discussion of the motivation to combine references as to those specific claims.

269. Both Kim and Schmid are in the same field of endeavor. Kim is directed at a semiconductor testing device, which is called a probe card, structured with a plurality of testing pins (probe needles) formed at positions corresponding to the terminals of the wafer to test the electrical characteristics of chips produced at the wafer level. *See, e.g., id.*, [0005], [0006]. Kim's probe card or semiconductor testing device comprises a guide plate (10) including an upper plate (11) and a lower plate (12) with a plurality of guide holes (11b, 12b) supporting the testing pins (30) inserted and placed into the guide holes (11b, 12b). *See, e.g., id.*, [0033], [0034], [0037], Figs. 2-6. Similarly, Schmid discloses a test head in the field of semiconductors for electrically testing high precision printed circuit boards and semiconductor wafers. *See, e.g., Ex. 1009*, 3:25-30. Schmid also teaches that the test head (1) has three guide panels (17, 19, 21) that are held parallel and spaced apart from one another, and each of the guide panels (17, 19, 21) has several feed through openings (23) through which pin shaped contact elements

(25), also referred to as test probes, are axially displaceably guided. *See, e.g., id.*, 3:41-54. Thus, both Kim and Schmid are in the same field of endeavor.

270. The combination of Kim and Schmid simply constitutes a conventional a wafer probe card with the addition of the conductive material on the guide plates to connect testing pins carrying the same type of signal (*e.g.*, power and ground) as taught in Kim. Kim teaches a probe card that uses physically and electrically separated groups of conductive layers (20) and a conductive trace (40) to metalize the guide holes (11b, 12b) and the surface of a guide (10) including two separate upper and lower plates (11, 12) to electrically connect (short-circuit) physically and electrically separated groups of testing pins (30) carrying different types of signals (*e.g.*, power signal and ground signal), respectively. *See, e.g.*, Ex. 1006, [0051], [0062], Figs. 5a and 5b. Kim explicitly teaches that it is not limited to forming electrically connected group of testing pins (30) only on the upper plate (11). *Id.*, [0052]. According to Kim, each electrically connected group of testing pins (30) can be formed not only on the upper plate (11), but also on the lower plate (12). *Id.* The '885 patent explains that short-circuiting contact elements carry a same type of signal improves signal noise, and frequency performance. *See, e.g.*, Ex. 1001, 7:49-55, 17:39-46, 47-60. This is exactly the same problem that Kim sought to solve. Ex. 1006, [0003], [0014], [0016], [0051].

271. Schmid discloses a wafer probe test head using three guide plates (*i.e.*, the first guide panel (17), the second guide panel (19) and the third guide panel (21)) spaced apart from one another to guide contact elements for movement or deformation. *See, e.g.*, Ex. 1009, 1:63-65, 3:41-54, 4:25-35, Figs. 1 and 2. Thus, it was obvious to a POSITA that the combination of Kim and Schmid would yield predictable results because the use of two or more spaced guide plates in a wafer probe card was nothing more than well-known design choice.

272. Schmid is just one example of a reference that taught the use of more than two guide plates. Other examples include: U.S. Pat. No. 4,622,514 (Ex. 1014, “Lewis”), 1:29-58, 2:64-3:4, Fig. 1 (teaching a buckling beam probe including a “top mating locating guide (22),” a “bottom locating guide (34)” and an intermediate “floating die 30” distanced from one another.); *see also* U.S. Pat. No. 10,281,491 (Ex. 1015, “McQuade”), 2:53-64, 3:22-29, Figs. 3 and 4C (teaching a probe card for testing semiconductor wafer including a “first alignment plate (34),” a “second alignment plate (35)” and a “third alignment plate (36).”).

273. A POSITA would understand the benefits and reasons for adding a third guide plate to a vertical probe system like the ones described in Kim. If you apply force to a buckling beam probe (like when it makes contact with the device under test), it will bend, sometimes in unpredictable ways. One way to force the

probe to bend in a desired way is to add a third or intermediate guide plate. This was a well-known design choice as discussed above.

274. Schmid also discusses the benefits of adding a third guide plate and describes the third guide plate as “preferred.” Ex. 1009, Abstract (“A plurality of at least two and preferably three guide panels are located in the space between the test points and the contact points.”) “In a particularly preferred embodiment of the test head, a third guide panel is arranged in the intermediate space between a first guide panel and a second guide panel of the device for making contact.” *Id.*, 2:34-37. Schmid explains why this is preferred: “The third guide panel also ensures that the contact elements do not touch one another, particularly during a test procedure, so that, if appropriate, electrical insulation between the contact elements can be dispensed with, and this reduces the cost of the test head.” *Id.*, 2:49-53. Accordingly, a POSITA would have had a motivation to add a third guide plate as taught in Schmid to the systems taught in Kim.

275. In addition, the comments of both the EPO and JPO during prosecution of the ’885 patent’s counterparts, as discussed above, confirm that the addition of a third or intermediate guide plate would have been known to a POSITA as a routine design choice.

276. The POSITA starting with Kim would have thus been motivated to add a third guide plate as taught in Schmid, and conversely, the POSITA starting

with Schmid would thus have been motivated to add conductive portions to one or more of the guide plates as taught in Kim to yield the benefits taught by Kim.

277. I see nothing in the '885 patent that describes the addition of a third or intermediate guide plate as a novel aspect of the patent's design or claimed inventions, or that describe any novel or unusual benefits of adding a third guide plate specifically.

278. I also see nothing in either Kim or Schmid that would teach away from combining the disclosures of those two references in a way that would yield the subject matter of claims 5-6, 16-20, or 23 of the '885 patent.

279. Thus, it would have been obvious to a POSITA that the combination of Kim and Schmid is simply the combination of prior art elements according to known methods to yield predictable results of improving signal noise and frequency performance, and that the results of the combination would have been predictable and there would be a reasonable expectation of success in the combination.

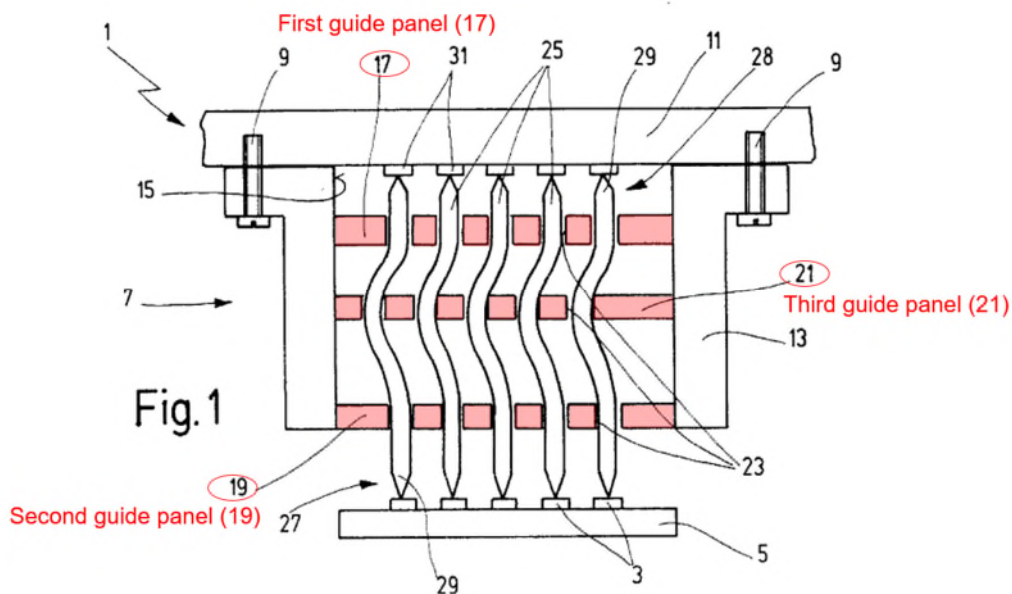
B. Claim 5

280. All elements of claims 5 are disclosed by the combination of Kim and Schmid as explained below.

1. Claim [5a]: The testing head of claim 1, wherein the at least one guide includes a lower guide, an intermediate guide, and an upper guide

281. Schmid discloses a wafer testing probe with three guide plates.

Specifically, Schmid discloses a test head (1) for making contact simultaneously with a plurality of test points (3), which are arranged next to one another, of an electric component (5) under test. *Id.*, 3:25-35, Fig. 1 (annotated and color-coding added).



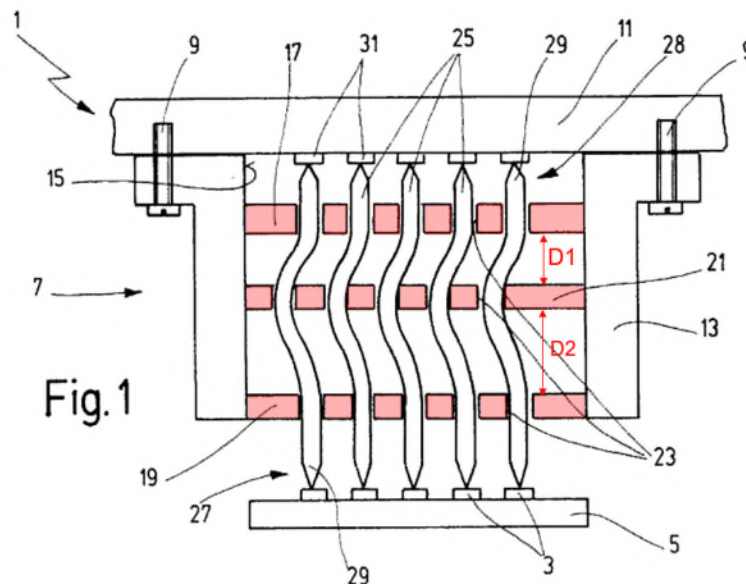
282. As illustrated in Fig. 1 and described in the specification, Schmid teaches that the test head (1) has a first guide panel (17), a second guide panel (19) and a third guide panel (21). *Id.*, 3:41-45. Schmid explains that the third guide plate (21) is in the intermediate space between the first guide panel (17) and the second guide panel (19). *Id.*, 3:58-63, Fig. 1. Thus, Schmid's first guide panel

(17) constitutes the claimed “upper guide,” the second guide panel (19) constitutes the claimed “lower guide”, and the third guide panel (21) constitutes the claimed “intermediate guide.”

283. Thus, Schmid discloses claim [5a].

2. Claim [5b] the lower guide and the intermediate guide being separated from each other by a first gap, the intermediate guide and the upper guide being separated from each other by a second gap

284. Schmid discloses and illustrates in Fig. 1 that the first guide panel (17), the second guide panel (19) and the third guide panel (21) are held parallel to one another and at a distance from one another along the axis of the sleeve of a sleeve shaped base body (13). *Id.*, 3:41-45, Fig. 1 (annotated and color-coding added).

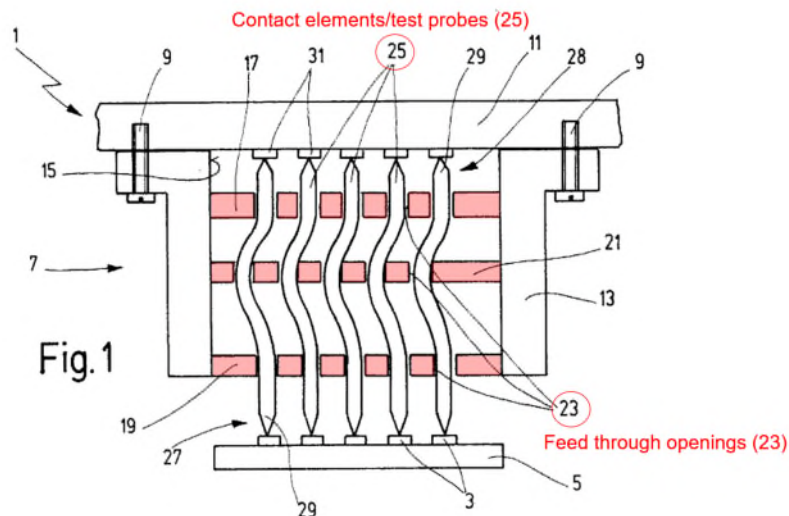


285. Thus, the distance (D1) between Schmid's first guide panel (17) and the third guide panel (21) constitutes the claimed "first gap" and the distance (D2) between Schmid's second guide panel (19) and the third guide panel (21) constitutes the claimed "second gap."

286. Thus, Schmid discloses claim [5b].

3. Claim [5c] each of the lower, intermediate and upper guides comprising respective guide holes for housing the contact elements

287. Schmid discloses and illustrates in Fig. 1 that each of the guide panels (17, 19, 21) has several feed through openings (23) through which pin shaped contact elements (25), also referred to as test probes, are axially displaceably guided. *Id.*, 3:45-49, Fig. 1 (annotated and color-coding added).



288. Thus, Schmid's feed through openings (23) formed on each of the guide panels (17, 19, 21) constitutes the claimed "guide holes" for housing the contact elements (25), which constitute the claimed "contact elements."

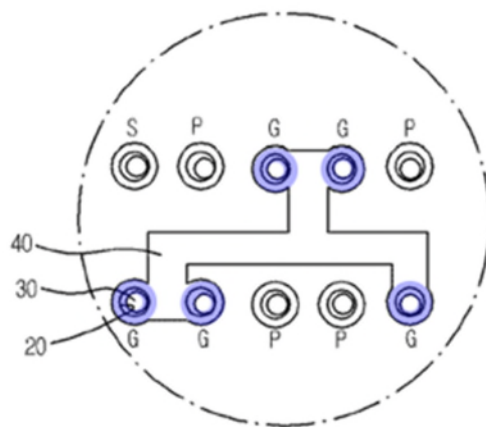
289. Thus, Schmid discloses claim [5c].

4. Claim [5d] the first and second conductive portions being formed on respective faces of the upper, intermediate and lower guides

290. Kim discloses the claimed "first and second conductive portions." *Supra* § XI(A)(4)(5). Specifically, Kim teaches a conductive layer (20) and a conductive trace (40) collectively constituting the claimed "first conductive portion." *See, e.g.*, Ex. 1006, [0033]. Kim explains that the plurality of the conductive layers (20) is formed by coating conductive material on one side of the upper plate (11) where the first guide holes (11b) are formed. *Id.*, [0038]. Kim further teaches that the conductive layers (20) are formed on the inner side of the guide holes. *See, e.g., id.*, Abstract, [0017]. Kim goes on to teach a conductive trace (40) also using a conductive material formed on the inner or outer side of the upper plate (11) or lower plate (12). *Id.*, [0042]. And the conductive trace (40) is connected to the conductive layer (20). *Id.*, [0043]. The connection between the plurality of the conductive layers (20) and the conductive trace (40) results in that the testing pins (30) in contact with the conductive layers (20) within the guide

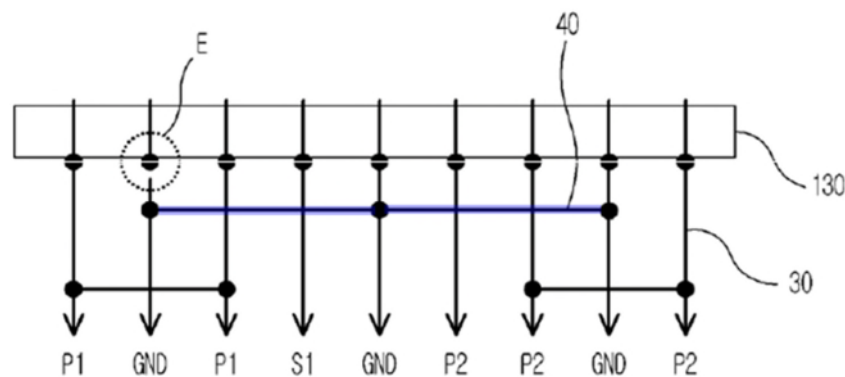
holes (11b, 12b) are electrically connected to the conductive trace (40). *Id.*, [0038], [0039].

291. Kim further teaches that the conductive layers (20), with which the testing pins (30) of transmitting the *same* signal are contacted, are connected to each other. *Id.*, [0044] (emphasis added). Kim explains that the testing pins (30) in contact with the conductive layers (20), for example, are testing pins for ground. *Id.* Kim illustrates in Fig. 5a that the testing pins (30) for ground signals are electrically connected via the conductive layers (20) formed within a group of guide holes and the conductive trace (40) electrically connecting the conductive layers (20). *Id.*, Fig. 5a (color-coding added).



292. Kim describes and illustrates in Figs. 2 and 5a that a plurality of guide holes (11b) are formed on the upper surface of the upper plate (11) of the guide plate (10) and a group of the guide holes are selected from the plurality of guide holes (11b) for housing a group of testing pins (30), which is also selected from a

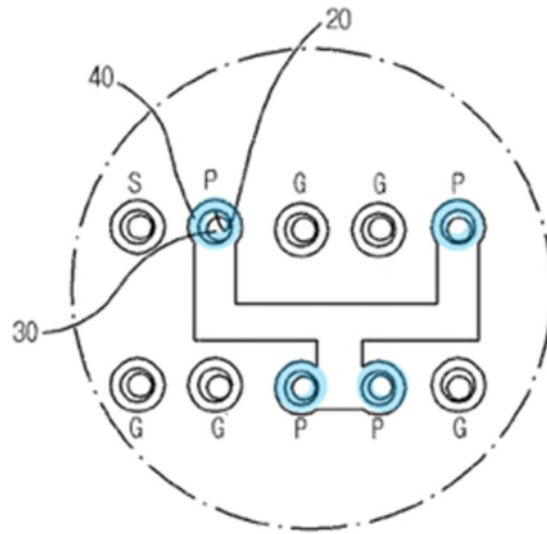
plurality of testing pins (30), for ground signals. *Id.*, [0051]. And the group of testing pins (30) for ground signals are electrically connected via the conductive layers (20) and the conductive trace (40). *Id.* Kim further illustrates a conceptual diagram demonstrating that the conductive trace (40) connects between the testing pins (30) transmitting the same type of ground signals and the conductive layers (20) in contact with the testing pins (30). *Id.*, [0044], Fig. 3 (color-coding added).



293. Thus, Kim’s conductive layers (20) and the conductive trace (40) formed on the upper plate (11) for connecting testing pins (30) carrying ground signals constitute the claimed “first conductive portion.”

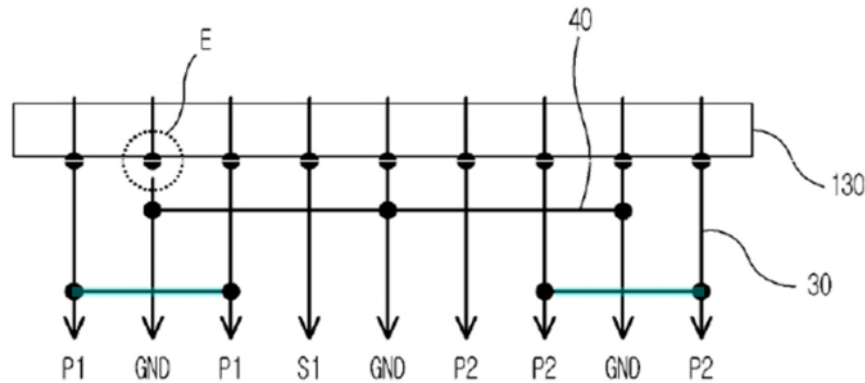
294. In addition to the connections among the selected group of testing pins (30) for ground signals through the conductive layers (20) in contact with the testing pins (30) in the guide holes (11b) on the guide (10) and the conductive trace (40), Kim similarly teaches how to use the conductive layers (20), the guide holes (11b) and the conductive trace (4) to electrically connect another group of testing pins (30) for another type of signal. Specifically, Kim describes and illustrates in

Fig. 5b that the testing pins (30) carrying power signals are electrically connected via the conductive layers (20) and conductive trace (40). *Id.*, [0051], Fig. 5b (color-coding added).



295. Kim explains and illustrates in Figs. 2 and 5b that a plurality of guide holes (11b) are formed on the lower surface of the upper plate (11) of the guide plate (10) and a group of the guide holes are selected from the plurality of guide holes (11b) for housing a group of testing pins (30), which is also selected from a plurality of testing pins (30), for power signals. *Id.* And, the group of testing pins (30) for power signals is electrically connected via the conductive layers (20) and the conductive trace (40). *Id.* Kim similarly illustrates a conceptual diagram demonstrating that the conductive trace (40) connects between the testing pins (30) transmitting the same type of power signals and the conductive layers (20) in

contact with the testing pins (30) within the guide holes (11b). *Id.*, Fig. 3 (color-coding added).



296. Thus, Kim’s conductive layers (20) and the conductive trace (40) formed on the upper plate (11) for connecting testing pins (30) carrying power signals constitute the claimed “second conductive portion.” Additionally, Kim does not limit the placement of the conductive portions to the upper plate (11). Kim further teaches that the conductive portions can also be located on the lower plate (12): “Also, in the drawings, each group is formed at only the upper surface and the lower surface of the upper plate 11. However, the present invention is [not] limited to the position of the groups. That is, each group can be formed at the upper surface and the lower surface of both upper and lower plates 11 and 12 according to the number of the groups.” *Id.*, [0052].

297. A POSITA would have understood that the combination of Kim teaching two physically and electrically separated groups of conductive layers (20) and conductive trace (40) in contact with two physically and electrically separated

groups of testing pins (30) carrying two different types of signals (*e.g.*, ground and power signals) on the upper and lower guides plates, with Schmid teaching three separate guide panels (17, 19, 21) spaced apart from one another with feed through openings (23), would result in conductive portions being formed on respective faces of the upper, intermediate and lower guides - the subject matter in claim 5d.

298. Thus, claim 5 is disclosed by the combination of Kim and Schmid.

C. Claim 6

299. The limitations of claim 6 are the same or very similar to the limitations of claim 5. Below is a table comparing the limitations of claim 6 to those of claim 5, showing the similarities between the language of the claims.

Claim 6	Claim 5
[6a] The testing head of claim 1, wherein the at least one guide includes a lower guide, an intermediate guide and an upper guide,	[5a] The testing head of claim 1, wherein the at least one guide includes a lower guide, an intermediate guide, and an upper guide,
[6b] the lower guide and the intermediate guide being separated from each other by a first gap, the intermediate guide and the upper guide being separated from each other by a second gap,	[5b] the lower guide and the intermediate guide being separated from each other by a first gap, the intermediate guide and the upper guide being separated from each other by a second gap,
[6c] each of the lower, intermediate and upper guides comprising respective guide holes for the housing the contact elements,	[5c] each of the lower, intermediate and upper guides comprising respective guide holes for housing the contact elements,
[6d] the first and second conductive portions being formed on a same face of	[5d] the first and second conductive portions being formed on respective

one of the upper, intermediate and lower guides and being physically and electrically separated from each other by at least one non-conductive zone.	faces of the upper, intermediate and lower guides.
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300. I explained above in Sections X.A, XI.A, XI.B, XII.A, XII.B why the combination of Kim and Schmid would disclose or at least render obvious to a POSITA claim 5. That analysis applies to claim 6 as well.

301. Claim 6 also includes the limitation, “first and second conductive portions being formed *on a same face* of one of the upper, intermediate, or lower guides and being physically and electrically separated from each other by at least one non-conductive zone” (emphasis added).

302. The combination of Kim and Schmid also would render obvious this limitation.

303. I explained above in Section XI.B that a POSITA would understand, based on Kim’s teachings and the knowledge that a POSITA would possess, the conductive portions of Kim could be formed on either face of a guide plate and could be arranged and patterned in different ways, including that both the ground and power connections could be formed on the same face of the guide plate.

304. From reviewing the prosecution of the pending European counterpart application, it appears that Technoprobe is arguing that Kim does not disclose or

suggest forming conductive portions for different signals on the same face of a guide.

305. I disagree with Technoprobe’s argument. Kim explains clearly that the first and second conductive groups (connecting the guide holes housing contact elements for transmitting ground and power) can be formed on the same face of a guide plate.

306. First, Kim explains that “in one embodiment of the present invention, the plurality of the conductive layers 20, with which the testing pins 30 of transmitting the same signal are contacted, and the conductive traces for connecting them *are set to a plurality of groups* and each group is formed at the upper surface and the lower surface of the upper plate 11 respectively, so that the testing pins 30 of transmitting the same signal in the narrow testing area can be easily connected.” *Id.*, [0050] (emphasis added).

307. Kim then elaborates that these “groups” of conductive layers and traces can be on the upper and lower surfaces of a guide plate, as shown in Figures 5a and 5b respectively. *Id.*, [0051]. As I already explained at length previously, Figure 5a shows the guide holes housing the ground testing pins are connected, and Figure 5b shows the guide holes housing the power testing pins are connected.

308. Kim then teaches that the position of the conductive groups need not be exactly what is shown in Figures 5a and 5b. *Id.*, [0052]. Rather, while “in the

drawings, each group is formed at only the upper surface and the lower surface of the upper plate 11,” “However...each group can be formed at the upper surface *and* the lower surface of *both* upper and lower plates 11 and 12 according to the number of groups.” *Id.* (emphasis added.) (I note that Kim, [0052] has a typo where “not” is missing from the text before “limited,” but it is clear from the context that “not” is what is intended.) It is of note that Kim says that “each” group can be formed at the upper / lower surface, which tells a POSITA that there is flexibility of placement. Likewise, Kim KR discloses “the present invention is not limited to forming each group only on the upper surface and lower surface of the upper plate (11). Depending on the number of groups, it is possible to form more than one electrically connected group on a single surface.” Ex. 1005, [0045]. And similarly, Kim teaches that “an aspect of the present invention” includes a guide plate with “one *or more* conductive traces formed at one side of a surface of the guide plate[.]” Ex. 1006, [0017] (emphasis added).

309. A POSITA would thus understand that Kim’s system may be implemented with two (or more) groups of conductive material on one side of a guide plate electrically connecting guide holes, and that those two or more groups may be carrying different types of signals, power and ground. A POSITA would have understood that this arrangement would be advantageous, and perhaps even

required, in some circumstances, for example where there are multiple power and/or ground signal groups.

310. Technoprobe itself explained, in the European counterpart prosecution, that “forming different conductive portions on a same face of the guide allows to easily arrange said conductive portions in the testing head, following the layout of the device under test (DUT).” Ex. 1016, 455.

Technoprobe argued that “[m]any layout can be easily devised” and that this feature “allows to easily follow the layout of the DUT.” *Id.* These arguments show that a POSITA likewise would have had a reason to implement Kim’s teachings with different conductive portions on a same face of the guide and would have had no trouble in so doing.

311. Kim also teaches that conductive portions carrying different types of signals would be physically and electrically separated from each other by a non-conductive zone. For example, Figures 5a and 5b, and the accompanying descriptions, show the two conductive portions physically and electrically separated by the guide plate. Similarly, Kim teaches that “the testing pins 30 for signal or the testing pins 30 for power are insulated with the testing pins 30 for ground[.]” Ex. 1006, [0062]. And as I explained above in Section XI.B, a POSITA implementing the teachings of Kim would have known that conductive elements

designed to carry different signal types would need to be separated in this manner for the device to operate properly.

312. For these reasons, the alleged invention claimed in claim 6 would have been obvious to a POSITA in view of Kim and Schmid.

D. Claim 16

313. The limitations of claim 16 are the same or very similar to the limitations of claims 1 and 5. Below is a table comparing the limitations of claim 16 to those of claims 1 and 5, showing the similarities between the language of the claims.

Claim 16	Claims 1 and 5
[16P] A testing head configured to verify the operation of a device under test integrated on a semiconductor wafer, the testing head comprising:	[1P] A testing head configured to verify the operation of a device under test integrated on a semiconductor wafer, the testing head comprising:
[16a] a plurality of contact elements, each comprising a body that extends between a first end portion and a second end portion; and	[1a] a plurality of contact elements, each comprising a body that extends between a first end portion and a second end portion, and
[16b] at least one guide provided with a plurality of guide holes configured to house the contact elements,	[1b] at least one guide provided with a plurality of guide holes configured to house the contact elements,
[16c] wherein the at least one guide comprises: a first conductive portion including and electrically connecting holes of a first group of the guide holes to each other, the first group housing first contact elements	[1c] wherein the at least one guide comprises: a first conductive portion that includes and electrically connects a first group of guide holes, of the plurality of guide holes, to each other and is configured to contact corresponding first contact elements, of the plurality of contact elements, configured to carry a first type of signal; and

[16d] a second conductive portion including and electrically connecting holes of a second group of the guide holes to each other, the second group housing second contact elements	[1d] a second conductive portion that includes and electrically connects the holes of a second group of the guide holes to each other, the second group housing second contact elements of the plurality of contact elements, the second contact elements being configured to carry a second type of signal
[16e] the first and second contact elements being configured to carry respective same type of signal chosen between ground signals and power signals; and	[1e] the first and second types of signals chosen between ground signals and power signals.
[16f] a lower guide, an intermediate guide, and an upper guide, the lower guide and the intermediate guide being separated from each other by a first gap, the intermediate guide and the upper guide being separated from each other by a second gap,	[5a]-[5b] The testing head of claim 1, wherein the at least one guide includes a lower guide, an intermediate guide, and an upper guide, the lower guide and the intermediate guide being separated from each other by a first gap, the intermediate guide and the upper guide being separated from each other by a second gap,
[16g] each of the lower, intermediate and upper guides comprising respective guide holes for housing the contact elements	[5c] each of the lower, intermediate and upper guides comprising respective guide holes for housing the contact elements,
[16h] the first and second conductive portions being formed on respective faces of the upper, intermediate and lower guides.	[5d] the first and second conductive portions being formed on respective faces of the upper, intermediate and lower guides.

314. I explained above in Sections X.A, XI.A, XII.B why the combination of Kim and Schmid would disclose or at least render obvious to a POSITA claims 1 and 5. That analysis applies to claim 16 as well.

315. For these reasons, the alleged invention claimed in claim 16 would have been obvious to a POSITA in view of Kim and Schmid.

E. Claim 17

316. As discussed previously, the combination of Kim and Schmid discloses claim 16. *Supra* § XII (D). Claim 17, which depends on claim 16 has the same limitations as claim 4. Below is a table comparing the limitation of claim 17 to those of claim 4, showing the similarities between the language of the claims.

Claim 17	Claim 4
The testing head of claim 16, wherein the first conductive portion is formed on a first face of the at least one guide, and the second conductive portion is formed on a second face of the at least one guide, the second face being opposite to the first face.	The testing head of claim 1, wherein the first conductive portion is formed on a first face of the at least one guide, and the second conductive portion is formed on a second face of the at least one guide, the second face being opposite to the first face.

317. I explained above in Sections X.A, X.C, XI.A, XII.B, XII.D why the combination of Kim and Schmid would disclose or at least render obvious to a POSITA claims 4 and 16. That analysis applies to claim 17 as well.

318. For these reasons, the alleged invention claimed in claim 17 would have been obvious to a POSITA in view of Kim and Schmid.

F. Claim 18

1. **[18] The testing head of claim 16, wherein the at least one guide includes at least one third conductive portion that includes and electrically connects holes of a third group of the guide holes to each other and house third contact elements, of the plurality of contact elements, configured to carry input/output signals between the device under test and a test equipment.**

319. Kim and Schmid, alone or in combination, disclose this limitation.

Claim 18 depends on independent claim 16. As discussed with respect to limitations [16P]-[16d], Kim and Schmid, alone or in combination, disclose Claim 16 which claim 18 is dependent upon. Claim 18 is substantially identical to claim 7, as shown in the table below. Thus, for the reasons discussed with respect to limitation [7], Kim and Schmid, alone or in combination, disclose the additional limitations (to claim 16) of this claim. *See Supra* Sections X.A, XI.A, XI.C, XII.B, XII.D.

Claim 18	Claim 7
The testing head of claim 16, wherein the at least one guide includes at least one third conductive portion that includes and electrically connects holes of a third group of the guide holes to each other and house third contact elements, of the plurality of contact elements, configured to carry input/output signals between the device under test and a test equipment.	The testing head of claim 1, wherein the at least one guide includes at least one third conductive portion that includes and electrically connects a third group of the guide holes to each other and house third contact elements configured to carry input/output signals between the device under test and a test equipment.

G. Claim 19

320. As discussed previously, the combination of Kim and Schmid discloses claim 16. *Supra* § XII (D). Claim 19, which depends on claim 16 has the same limitations as claim 9. Below is a table comparing the limitation of claim 19 to those of claim 9, showing the similarities between the language of the claims.

Claim 19	Claim 9
The testing head of claim 16, wherein the at least one guide comprises at least one common pad connected to the first conductive portion by a conductive track.	The testing head of claim 1, wherein the at least one guide comprises at least one common pad connected to the at least one conductive portion by a conductive track.

321. I explained above in Sections X.A, X.E, XI.A, XI.C, XII.B, XII.D why the combination of Kim and Schmid would disclose or at least render obvious to a POSITA claims 9 and 16. That analysis applies to claim 19 as well.

322. For these reasons, the alleged invention claimed in claim 19 would have been obvious to a POSITA in view of Kim and Schmid.

H. Claim 20

323. As discussed previously, the combination of Kim and Schmid discloses claim 16. *Supra* § XII (D). Claim 20, which depends on claim 16 has the same limitations as claim 10. Below is a table comparing the limitation of claim 20 to those of claim 10, showing the similarities between the language of the claims.

Claim 20	Claim 10
The testing head of claim 16, wherein the at least one guide comprises a further conductive portion, which includes one of the guide holes configured to house a single contact element, the at least one guide comprising a common pad connected to the further conductive portion by a conductive track.	The testing head of claim 1, wherein the at least one guide comprises a further conductive portion at one of the guide holes that is configured to house a single contact element, the at least one guide comprising a common pad connected to the further conductive portion by a conductive track.

324. I explained above in Sections X.A, X.F, XI.A, XI.D, XII.B, XII.D why the combination of Kim and Schmid would disclose or at least render obvious to a POSITA claims 10 and 16. That analysis applies to claim 20 as well.

325. For these reasons, the alleged invention claimed in claim 20 would have been obvious to a POSITA in view of Kim and Schmid.

I. Claim 23

326. Claim 23 has the same limitations as claims 1 and 6. Below is a table comparing the limitation of claim 23 to those of claims 1 and 6, showing the similarities between the language of the claims.

Claim 23	Claim 1 and 6
[23P] A testing head configured to verify the operation of a device under test integrated on a semiconductor wafer, the testing head comprising:	[1P] A testing head configured to verify the operation of a device under test integrated on a semiconductor wafer, the testing head comprising:
[23a] a plurality of contact elements, each comprising a body that extends between a first end portion and a second end portion; and	[1a] a plurality of contact elements, each comprising a body that extends between a first end portion and a second end portion, and

[23b] at least one guide provided with a plurality of guide holes configured to house the contact elements,	[1b] at least one guide provided with a plurality of guide holes configured to house the contact elements,
[23c] wherein the at least one guide comprises: a first conductive portion including and electrically connecting holes of a first group of the guide holes to each other, the first group housing first contact elements	[1c] wherein the at least one guide comprises: a first conductive portion that includes and electrically connects a first group of guide holes, of the plurality of guide holes, to each other and is configured to contact corresponding first contact elements, of the plurality of contact elements, configured to carry a first type of signal; and
[23d] a second conductive portion including and electrically connecting holes of a second group of the guide holes to each other, the second group housing second contact elements,	[1d] a second conductive portion that includes and electrically connects the holes of a second group of the guide holes to each other, the second group housing second contact elements of the plurality of contact elements,
[23e] the first and second contact elements being configured to carry respective same type of signal chosen between ground signals and power signals; and	[1d] the second contact elements being configured to carry a second type of signal, [1e] the first and second types of signals chosen between ground signals and power signals
[23f] a lower guide, an intermediate guide and an upper guide, the lower guide and the intermediate guide being separated from each other by a first gap, the intermediate guide and the upper guide being separated from each other by a second gap,	[6a] The testing head of claim 1, wherein the at least one guide includes a lower guide, an intermediate guide and an upper guide, [6b] the lower guide and the intermediate guide being separated from each other by a first gap, the intermediate guide and the upper guide being separated from each other by a second gap

[23g] each of the lower, intermediate and upper guides comprising respective guide holes for the housing the contact elements	[6c] each of the lower, intermediate and upper guides comprising respective guide holes for the housing the contact elements
[23h] the first and second conductive portions being formed on a same face of one of the upper, intermediate and lower guides and being physically and electrically separated from each other by at least one non-conductive zone.	[6d] the first and second conductive portions being formed on a same face of one of the upper, intermediate and lower guides and being physically and electrically separated from each other by at least one non-conductive zone.

327. I explained above in Sections X.A, X.B, XI.A, XI.B, XII.A, XII.B why the combination of Kim and Schmid would disclose or at least render obvious to a POSITA claims 1 and 6. That analysis applies to claim 23 as well.

XIII. GROUND 4: KIM AND FAN RENDERS CLAIM 3 OBVIOUS.

328. All elements of claim 3 are disclosed by the combination of Kim and Fan and a POSITA would have been motivated to combine the references.

A. Claim 3

1. **[3] The testing head of claim 1, wherein the at least one guide comprises at least one coating dielectric portion that covers the at least one non-conductive zone.**

329. Kim and Fan, alone or in combination, disclose this limitation. As discussed in limitations [1P]-[1e], Kim discloses claim 1 which claim 3 is dependent upon.

330. Initially, I note that the '885 patent has only a limited description of any "coating dielectric portion." Specifically, the '885 patent describes coating the

non-conductive zones, for example between different conductive portions or at guide holes that do not need to be metallized, to “prevent[] metallic debris from settling therein, so as to avoid leakage and undesired electrical connections between contact elements apt to carry a different kind of signal.” Ex. 1001, 10:37-65.

331. With respect to the additional limitation of claim 3, Fan expressly discloses a probe head with guide plates and further discloses a “coating dielectric portion that covers” some or all of the guide plate. Fan discloses a probe head including a plate 100. Ex. 1011, 3:1-7, Figs. 1A, 1B, and 4. Fan illustrates in Fig. 4 and discloses in related description that in some embodiments, an “insulating layer 600” is used to cover some or all of the surface of the guide plate 100. *Id.*, 5:1-14, Fig. 4 (color-coding added); *see also* 1:65-67 (“In one or more embodiments, the probe head further includes an insulating layer disposed between the metal layer and the plate”), 2:1-3 (“In one or more embodiments, the probe head further includes an insulating layer covering the entire surface of the plate.”). As is well-understood in the art, and as would be understood by a POSITA, a “dielectric” material is insulating.

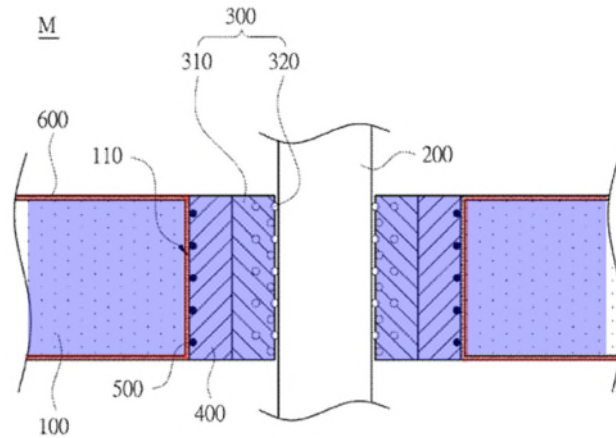


FIG. 4

332. Fan further teaches that the “insulating layer 600” may be formed on the plate by different methods, one of which is “coating.” “Alternatively, an insulating material can be *coated* on the [plate].” *Id.*, 5:15-34 (emphasis added).

333. Fan further teaches that the guide plate “can be made of *non-conductive materials*, semiconductor materials, or conductive materials....” *Id.*, 3:41-42 (emphasis added); *see also* 1:62-63 (“In one or more embodiments, the plate is made of ceramic [a non-conductive material]”).

334. Accordingly, Fan teaches, or at least renders obvious, a testing head that “comprises at least one coating dielectric portion [insulating layer 600] that covers the at least one non-conductive zone [a portion of guide 100 made of a non-conductive material].”

335. A POSITA would have found it obvious to coat non-conductive zones on the face of the guide plate disclosed in Kim with the insulating material disclosed in Fan, thereby yielding the subject matter of ’885 patent claim 3. Both

Kim and Fan are directed at semiconductor testing probes, and therefore they are in the same field of endeavor. Kim teaches that testing pins carrying different types of signals, and conductive portions carrying different types of signals (*e.g.*, the conductive layers and traces connecting guide holes housing testing pins carrying ground signals, and the conductive layers and traces connecting guide holes housing testing pins carrying power signals), should be electrically separated from each other by a non-conductive zone. For example, Figures 5a and 5b, and the accompanying descriptions, show the two conductive portions physically and electrically separated by the guide plate. Similarly, Kim teaches that “the testing pins 30 for signal or the testing pins 30 for power are insulated with the testing pins 30 for ground.” Ex. 1006, [0062]. And as I explained above in Section XI.B., a POSITA implementing the teachings of Kim would have known that conductive elements designed to carry different signal types would need to be separated in this manner for the device to operate properly. Fan teaches coating using an insulating layer (600) to insulate two conductive materials that are meant to be kept electrically separate. Ex. 1011, 5:1-35.

336. Accordingly, a POSITA would have readily understood the benefit of applying Fan’s teaching of coating a guide plate with an insulating material to improve Kim by coating non-conductive zones on the guide plate of Kim and thus helping to ensure that testing pins and conductive portions carrying different signal

types remain electrically separated. To the extent that Fan's disclosures of coating insulating layers are read to be limited to embodiments coating the guide where the guide itself is conductive or semi-conductive, a POSITA still would have understood the benefit of applying Fan's teachings to Kim to coat the non-conductive portions of Kim's guide plates. As taught in Fan, the purpose of coating the insulating layer is to help electrically separate two conductive materials. This purpose would be applicable in Kim by coating the non-conductive zones on the guide plate between testing pins and conductive portions carrying different signal types. A POSITA would have reasonably expected success in applying Fan's teachings to Kim in this manner; Fan describes how to perform the coating (notably, the '885 patent itself says nothing about how to coat the guide plate). Thus, the combination of Kim and Fan would have rendered obvious claim 3 to a POSITA.

XIV. GROUND 5: KIM AND BROSS RENDERS CLAIMS 12 AND 13 OBVIOUS.

337. All elements of claims 12 and 13 are disclosed by the combination of Kim and Bross and a POSITA would have been motivated to combine the references.

A. Motivation to Combine

338. This section provides an overview of the reasons why a POSITA would have been motivated to combine the disclosures of Kim and Bross in a way

that would yield the alleged inventions claims in '885 patent claims 12 and 13, and also explains why a POSITA reasonably would have expected success in doing so. Kim and Bross both relate to a test probe assembly. Kim discloses a guide with conductive portions, as discussed in detail above. Kim discloses various exemplary methods for forming those conductive layers, without limiting its teachings to just those methods. Ex. 1006, [0056]-[0062]. It would have been obvious for a POSITA from the teachings of Kim to select a known manufacturing method, such as the one from Bross, to form the claimed conductive portion in the claimed guide.

339. And Bross explicitly discloses that the laminating method or multilayer technique (metallization of guide plates) to form conductive layers is well known in the art. Bross states that “[t]hese layers of insulation and conductors are suitable bonded together into a unitary structure to provide a multilayer arrangement, such as is well known in the art.” Ex. 1010, 4:49-52. Additionally, “The positions, spacings, and shapes of the conductive traces 56a, 56b, etc., are provided in accordance with design rules well known to those skilled in the art of designing and fabricating multi-layer circuitry.” *Id.*, 6:36-40. “Still further, a multi-layer arrangement with a different number of layers or of different designs from that disclosed may be employed.” *Id.*, 7:46-48. Bross describes how these techniques achieve the desirable result that “each probe element makes good

mechanical and electrical contact to one or more selected conductors of the conductive layers.” *Id.*, 2:21-24.

340. Thus, a POSITA would be motivated to use the well-known laminating methods described by Bross in Kim to achieve embedding at the time of the invention and would have expected to be successful in doing so following Bross’s teachings. The combination of Kim and Bross simply constitutes a conventional testing probe with one or more insulating layers sandwiched by two overlapping conductive layers such that the two conductive layers could be electrically insulated. This is nothing more than an implementation of known art to yield predictable results. Combining the teachings of Kim and Bross in this way would result in the subject matter of ’885 patent claims 12 and 13, as discussed below.

341. I note a statement in Bross (at 5:50-52) that “The probe element 36 is also mechanically anchored or captivated in the body 22 of the probe assembly 20.” “Captivation” here refers to the fingers “gripping” the contact element, as described in Bross at 8:4-7 and in claim 2 (“The probe assembly of claim 1 wherein: the vias are vertically staggered by an amount sufficient to bow the probe elements captivated in the respective [v]ias”). I note also that Kim teaches (at [0031]), “in order to simply make the description, the probe card will be explained as the term called as a semiconductor testing apparatus. However, the present

invention is not limited to the probe card. All semiconductor testing apparatus having multiple test pins can be applied thereto.” A POSITA would have understood that any differences between the “body” taught in Bross and the guide plates taught in Kim would not detract or teach away from the combinations discussed here, that is, using the teachings of Bross to construct the guide plate(s) in Kim such that the conductive layers in Kim were embedded or overlapping.

B. Claim 12

1. [12] The testing head of claim 1, wherein the first conductive portion is embedded in the at least one guide.

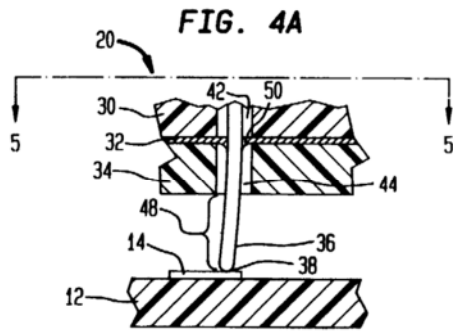
342. Kim and Bross, alone or in combination, disclose this limitation. As discussed in limitations [1P]-[1e], Kim discloses claim 1 which claim 12 is dependent upon. As to the limitation of claim 12, the ’885 patent describes an embodiment where the first conductive portion 30’ is embedded in guide 40, in this way forming a ground plane which electrically connects the guide holes of the first group 40’ within the guide 40. Ex. 1001, 8:19-26.

343. The claimed term “embedded” is used to distinguish the term “coated” or “coat” in terms of the process or method for forming conductive portions on the guide. *Id.*, 8:15-26. The ’885 patent, however, mentions nothing about how to “coat” or get the conductive portion “embedded” in the guide specifically.

344. To the extent the claimed term “embedded” can be met just by having the conductive layer on the inside of the guide hole, Kim discloses this. Kim discloses several methods for forming conductive material on the guide plate including plating or depositing using photoresistor film and etching to remove unnecessary conductive materials. *See, e.g.*, Ex. 1006, [0057]-[0059]. As I explained above in Section X.D with respect to claim 8, Kim teaches that the conductive portion covers at least part of the inner surface of the guide holes.

345. To the extent it is found that Kim does not expressly disclose this limitation, it was obvious for a POSITA to modify the teachings of Kim with Bross to arrive at claim 12. In the combination of Kim and Bross, the “first conductive portion” would be embedded in the guide rather than on the surface of the guide. Bross describes a “multi-layer” probe assembly with alternating conductive (24, 28, 32) and insulating (23, 26, 30, 34) layers, meaning that the conductive layers are embedded within the probe assembly. Ex. 1010, Abstract, Claim 1, Figs. 2, 4A, and 5, 6:23-32. For example, Bross shows in Figs. 4A and 5 and related description *the layer of conductive circuitry 32 positioned beneath the insulating layer 30* and is seen to comprise a plurality of electrically isolated printed-circuit traces (conductors), with the dotted lines 56a and 56b as examples in Fig. 5. *Id.*, 6:23-32 (emphasis added). “As many or as few of these circuit traces 56a and 56b may be provided in the layer of conductive circuitry 32 as

required by the desired member of interconnections to and from the respective probe elements 36.” *Id.*, 6:30-31; cl.1 “A probe assembly comprising: a body containing a plurality of insulating and conductive layers positioned horizontally in a vertically stacked multi-layer arrangement.” A POSITA would understand that Bross’s conductive circuitry discloses that a conductive layer contains any number of conductive traces, just as Kim contains any number of conductive traces.



Id., Figs. 4A and 5.

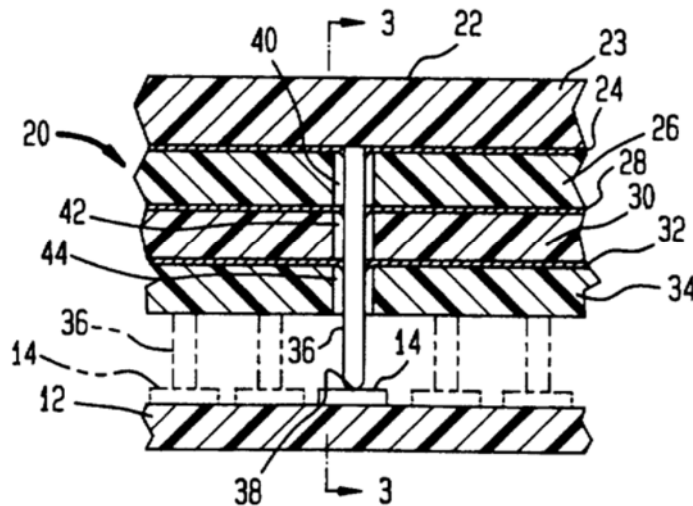
C. Claim 13

346. Kim and Bross, alone or in combination, disclose this limitation. I note that, as I explain in detail above with regards to Kim Figures 5a and 5b and their accompanying description, Kim teaches a guide plate with one conductive portion (e.g., for ground) formed on the top face of the guide, and another conductive portion (e.g., for power) for on the bottom face of the guide. If the

additional limitation of claim 13 can be met simply by having conductive portions on the top and bottom face of the guide, then Kim discloses it.

347. To the extent that it is found that this limitation is not expressly disclosed by Kim, Bross discloses “a multi-layer arrangement of insulating and conducting layers within the body of the probe assembly.” *Id.*, Abstract. Bross shows in Fig. 2 as an example, “multi-layer arrangement comprises a top insulating layer 23, a first conductive layer 24, a second insulating layer 26, a second conductive layer 28, a third insulating layer 30, a third conductive layer 32, and a fourth or bottom insulating layer 34. Each of the conductive layers typically comprises a plurality of individual conductors. These individual conductors are some times [*sic*] denoted as a ‘printed circuit’.” *Id.*, 4:41-49; Fig. 2. Thus, Bross’s “multi-layer arrangement” discloses “a plurality of conductive portions overlapped to and electrically insulated from each other.”

FIG. 2



Id., Fig. 2.

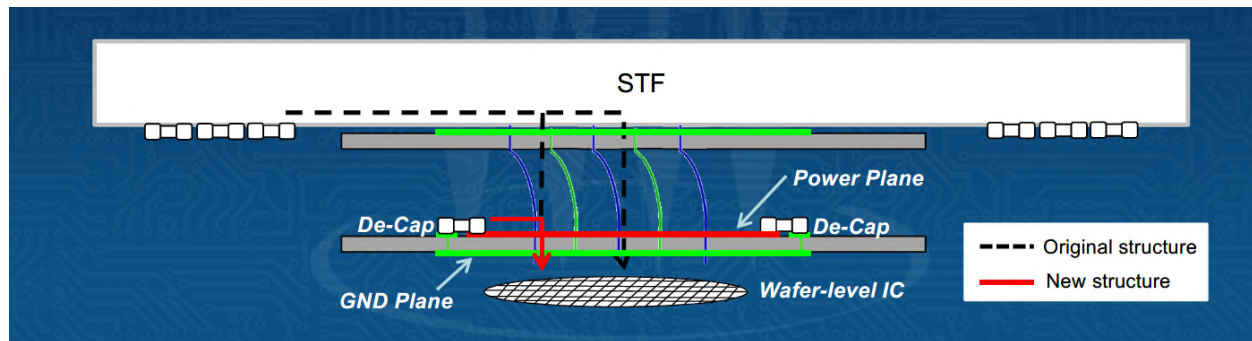
**XV. GROUND 6: KIM AND THE 2016 SWTEST PRESENTATION
RENDERS CLAIM 15 OBVIOUS.**

348. All elements of claim 15 are disclosed by the combination of Kim and the 2016 SWTest Presentation and a POSITA would have been motivated to combine the references.

A. Motivation to Combine

349. This section provides an overview of the reasons why a POSITA would have been motivated to combine the disclosures of Kim and the 2016 SWTest Presentation in a way that would yield the alleged inventions claims in '885 patent claim 15, and also explains why a POSITA reasonably would have expected success in doing so. Kim and the 2016 SWTest Presentation include technologies developed by the same company, Willtechnology Co. Ltd. Both

relate to a semiconductor testing probe card using metalized guide plates. Like Kim, the 2016 SWTest Presentation discloses a guide plate with two electrically conductive portions, the first connecting guide holes and probes carrying ground, and the second connecting guide holes and probes connecting power, as shown for example on slide 15 of the Presentation:



See also Ex. 1028, 15 (“Power, GND Plane, and De-Cap added to Probe Head”), 16 (“Implementation of Power and GND planes through gold plating”), 19 (“Introducing P/G planes and decaps on probe head leads to lower power impedance”), 8 (“Insertion of metal planes...”), 13 (showing “Low X-talk Probe Head” with “Gold plating” on the ceramic plate). It would be obvious for a POSITA to combine the two references related to the same technology developed from the same company.

350. And a POSITA also would be motivated to combine Kim and the 2016 SWTest Presentation by adding a decoupling capacitor as taught in the 2016 SWTest Presentation to the probe cards disclosed in Kim to improve the performance of the probe card. A POSITA would have known that decoupling

capacitors are commonly used to improve power integrity. De-caps are common electrical components used in probe cards to improve performance, so a POSITA would be knowledgeable about their use, function and benefit and added them to probe cards to improve their performance. Moreover, the 2016 SWTest presentation explicitly provides the motivation by discussing how adding a decoupling capacitor, in addition to connecting the power and ground probes respectively, improves the probe card by improving power integrity. *Id.*, 15-19. This is nothing more than an implementation of known art to yield predictable results.

B. Claim 15

- 1. [15] The testing head of claim 1, further comprising a circuit component, which is electrically connected at least to the first conductive portion of the at least one guide.**

351. Kim and the 2016 SWTest Presentation, alone or in combination, disclose this limitation. As discussed in limitations [1P]-[1e], Kim discloses claim 1 which claim 15 is dependent upon. As to the limitation of claim 15, the '885 patent describes that the first conductive portions 30' is electrically connected to circuit component 50, *e.g.*, a filtering capacitor. Ex. 1001, 16:60-17:24, Figs. 10A and 10B.

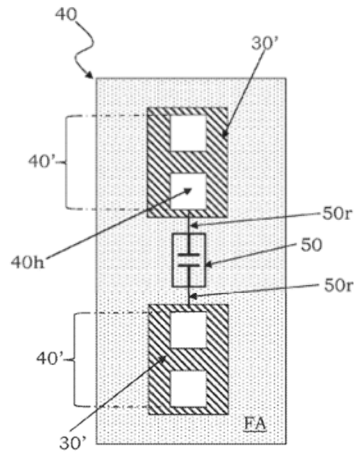


FIG. 10A

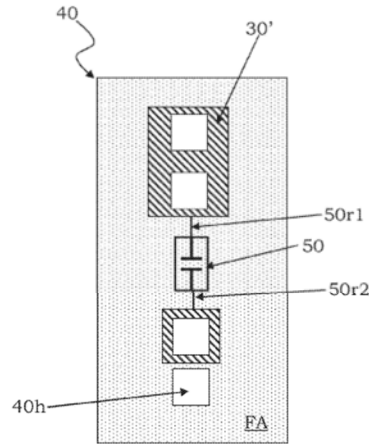
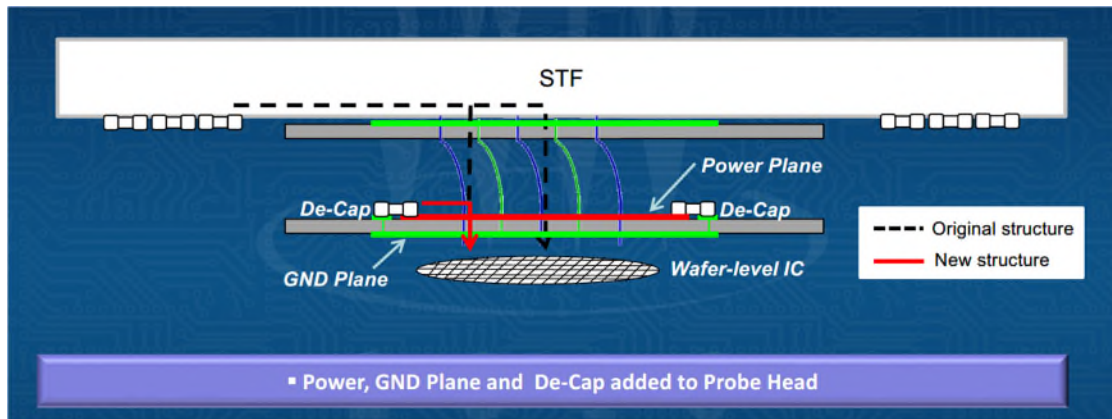


FIG. 10B

Id., Figs. 10A and 10B.

352. The '885 patent explains that having a filtering capacitor “allows to maximize the filtering effect of the capacitors 50, and therefore to reduce the interferences caused by contact elements that carry ground and power signals to a minimum, as well as to optimize the loop-back technique.” *Id.*, 17:11-14. The '885 patent also explains that “[t]he circuit component 50... may also be any other component suited for specific needs,” such as “a pair of inductors ... apt to be short-circuited in a loop-back configuration and to monitor the signal at those conductive portions.” *Id.*, 17:25-33.

353. The 2016 SWTest Presentation discloses electrically connecting a circuit component, capacitors (de-caps), between the power and ground planes (conductive portions) of the metalized guide plate.



Ex. 1028, 15.

354. A decoupling capacitor (de-cap) is a capacitor providing a bypass path for transient currents and decoupling (*i.e.*, prevent electrical energy from transferring to) one part of a circuit from another. Like the capacitor of the '885 patent, a de-cap shunts noise and reduces interferences caused by other circuit elements, reducing its effect on the rest of the circuit which helps improve power integrity.

355. At high frequencies, a de-cap serves as a bypass capacitor to decouple AC signals or voltage spikes on a power supply or other line and shunts energy from those signals, or transients right to the return path. Thus, each of the de-caps in the 2016 SWTest Presentation is the “circuit component, which is electrically connected at least to a first conductive portion of the at least one guide.”

XVI. GROUND 7: KIM, BROSS, AND SCHMID RENDERS CLAIMS 21 AND 22 OBVIOUS.

356. For the following reasons, the alleged invention claimed in claims 21 and 22 would have been obvious to a POSITA in view of Kim, Bross, and Schmid.

A. Motivation to Combine

357. As discussed in Section XII, a POSITA would have been motivated to combine Kim and Schmid to achieve the technical features recited in claim 16. As discussed in Section XIV, a POSITA would have been motivated to combine Kim and Bross to achieve the technical features recited in claims 12 and 13. And there is no reason a POSITA would have not been able to combine the teachings of Kim, Bross, and Schmid or would have been discouraged from doing so.

B. Claim 21

1. [21] The testing head of claim 16, wherein the first conductive portion is embedded in the at least one guide.

358. Kim and Bross, alone or in combination, disclose this limitation. Claim 21 depends on independent claim 16. As discussed with respect to limitations [16P]-[16h], Kim and Schmid, alone or in combination, disclose Claim 16 which claim 21 is dependent upon. Claim 21 is substantially identical to claim 12. Thus, for the reasons discussed with respect to limitation [12], Kim and Bross, alone or in combination, disclose the additional limitations (to claim 16) of this claim.

C. Claim 22

- 1. [22] The testing head of claim 16, wherein the first and second conductive portions are overlapped to and electrically insulated from each other.**

359. Kim and Bross, alone or in combination, disclose this limitation.

Claim 22 depends on independent claim 16. As discussed with respect to limitations [16P]-[16h], Kim and Schmid, alone or in combination, disclose Claim 16 which claim 22 is dependent upon. Claim 22 is substantially identical to claim 13. Thus, for the reasons discussed with respect to limitation [13], Kim and Bross, alone or in combination, disclose the additional limitations (to claim 16) of this claim.

XVII. SECONDARY CONSIDERATION

360. At this time, after review of the documents and materials cited herein, such as the prosecution history of the '885 patent, I have found no evidence of secondary considerations or objective factors of non-obviousness, and it is my opinion that claims 1- 23 of the '885 patent are obvious over the prior art. And to the extent Patent Owner alleges secondary considerations in this proceeding, it is my opinion that they would not outweigh the strong evidence of obviousness of the challenged claims of the '885 patent, as set forth herein. I have been informed that if Patent Owner presents in this proceeding evidence of objective factors that it argues support a finding of non-obviousness, I may be asked to review such

evidence and to formulate an opinion and reserve the right to address any such evidence and/or arguments that Patent Owner may raise in this regard.

XVIII. CONCLUSION

361. In summary, I have concluded that each limitation of the challenged claims is invalid as anticipated and/or obvious under 35 U.S.C. §§ 102, 103 in light of the prior art references and the knowledge of one of ordinary skill in the art, as described in this declaration.

362. Furthermore, I have used my background and experience in forming my opinions that claims 1- 23 are unpatentable as being anticipated and/or obvious over the prior art.

363. To the extent it is it is argued that any further disclosure is required for a limitation in claims 1- 23 than I have identified above, a POSITA would have found that limitation obvious to include based on the same disclosure and analysis I have identified above. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner or its expert(s) may raise, and to take into account new information as it becomes available to me.

I hereby declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. § 1001).

Executed on 6/26/2024



Frederick L. Taber