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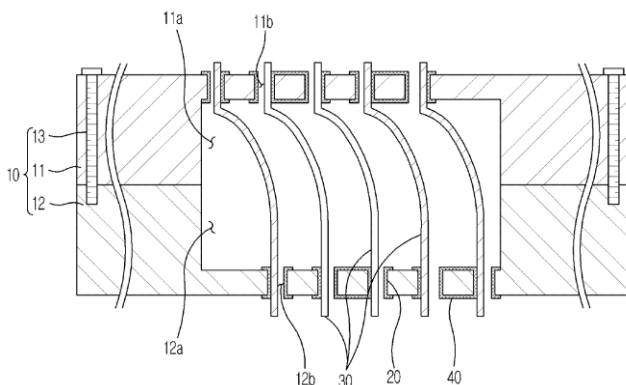
(54) Title of Invention: Semiconductor Test Device

(57) Abstract

The present invention relates to a semiconductor test device, more specifically a semiconductor test device, comprising a guide plate formed on one side with at least one guide hole, a conductive layer formed on the inner side of the guide hole, at least one test pin inserted and installed in the guide hole, with one side of the outer surface in contact with one side of the conductive layer, and the lower part electrically contacting the semiconductor to be tested and at least one conductive trace formed on the surface side of the guide plate, wherein one side is electrically connected to one side of the conductive layer.

According to the present invention, by allowing test pins to be electrically connected to other test pins or external substrates through the conductive layer formed in the guide hole, various characteristics such as electrical contact defects of test pins, spatial efficiency, noise, high-frequency characteristics, etc., can be improved. Consequently, there is an effect of enhancing the reliability of test results.

Representative figure



Claims

Claim 1

A semiconductor test device comprising:

a guide plate formed on one side with at least one guide hole;

a conductive layer formed on the inner side of the guide hole;

at least one test pin inserted and installed in the guide hole, with one side of the outer surface in contact with one side of the conductive layer, and the lower part electrically contacting the semiconductor to be tested; and

at least one conductive trace formed on the surface side of the guide plate, wherein one side of the conductive trace is electrically connected to one side of the conductive layer.

Claim 2

A semiconductor test device according to Claim 1,

wherein the guide plate comprises an upper plate formed on one side with at least one 1st guide hole; and a lower plate coupled to the underside of the upper plate, formed on one side with at least one 2nd guide hole, and the conductive traces are formed on at least one of the upper or lower surfaces of the upper plate or the upper or lower surfaces of the lower plate of the guide plate.

Claim 3

A semiconductor test device according to Claim 1,

wherein the conductive traces are formed to electrically connect between the test pins transmitting mutually identical signals and the conductive layer in contact.

Claim 4

A semiconductor test device according to Claim 1,

wherein the conductive traces are formed to electrically connect between the grounding test pins and the conductive layer in contact.

Claim 5

A semiconductor test device according to Claim 1,

wherein the conductive traces are extended from one side of the conductive layer, excluding the testing area where the test pins are densely installed, to an area on one side of the guide plate.

Specifications

Technical Field

[0001] The present invention relates to a semiconductor test device, and more specifically, a technology that enables to improve various characteristics such as electrical contact defects of test pins, spatial efficiency, noise, high-frequency characteristics, etc., consequently to enhance the reliability of test results.

Background Art

[0002] The semiconductor testing process can be roughly divided into front-end process testing, known as Electrical Die Sorting (EDS), which involves examining the electrical characteristics of chips produced at the wafer level, and back-end process testing, which involves inspecting semiconductor ICs manufactured at the package level.

[0003] Front-end process testing is performed to identify defective chips among the chips constituting the wafer. In this process, a semiconductor test device called a probe card is utilized, where electrical signals are applied to the chips composing the wafer to determine defects based on signals checked from the applied electrical signals. The probe card is structured with a plurality of test pins (probe needles) formed at positions corresponding to the terminals of the wafer.

[0004] Back-end process testing involves applying electrical signals to semiconductor devices packaged in the form of ICs to inspect whether ICs are normally operated. In this process, a semiconductor test device known as a test socket is employed. The test socket is structured with a plurality of pogo pins or conductive rubber sheets installed at positions corresponding to the IC terminals.

[0005] Additionally, semiconductor test devices can be employed to inspect (test) semiconductor packages where terminals, formed identically to the terminals of the semiconductor, are present on one side, and such terminals are interconnected or extended to connect to one side of the semiconductor package.

[0006] Fig. 1 is a cross-sectional view of a probe card, which is a front-end process testing device as an example of conventional semiconductor test device.

[0007] As seen in Fig. 1, a conventional probe card (100) comprises a guide plate (110) installed on the lower side, which includes a plurality of test pins (111) electrically contacting the chips to be tested; a main substrate (120) installed above the guide plate (110) with misalignment; and a space transformer (130) installed between the guide plate (110) and the main substrate (120) to spatially align the electrode pattern of the guide plate (110) with a narrow pitch and the main substrate (120) with a wide pitch.

[0008] In such conventional probe cards (100), when the test pins (111) come into contact with the semiconductor to be tested, electrical signals are transmitted from the semiconductor to be tested to the test pins (111). The electrical signals transmitted through the test pins (111) are then transferred to the probe interface board that is not illustrated herein through the main board (120).

[0009] Here, in the case of the conventional probe card (100), when the bottom of the test pin (111) makes electrical contact with the Device Under Test (DUT), i.e., the semiconductor under test, the top of the test pin (111) electrically contacts the space transformer (130). However, issues of inaccuracies in the DUT test results arise when the electrical contact between any one (111) of the numerous test pins (111) and the space transformer (130) becomes unstable. Consequently, the reliability of the test results is significantly compromised.

[0010] Semiconductor test devices, being equipment that examines the electrical characteristics of the target semiconductor by applying electrical signals through test pins, face issues related to electrical contact defects of these test pins. This problem is not limited to probe cards but is a common occurrence in all semiconductor test devices, including test sockets.

[0011] Furthermore, semiconductor test devices encounter challenges with poor high-frequency characteristics due to spatial constraints, necessitating the installation of a plurality of test pins in confined spaces.

Detailed Descriptions of Invention

Technical Problem

[0012] The present invention is proposed to solve the aforementioned challenges. The objective of the invention is to provide a semiconductor test device that improves various characteristics such as electrical contact defects of test pins,

spatial efficiency, noise, and high-frequency characteristics, consequently to enhance the reliability of test results, by allowing test pins to be electrically connected through a conductive layer formed in guide holes, enabling connection to other test pins or external substrates.

[0013] Another objective of the present invention is to provide a semiconductor test device that significantly enhances high-frequency performance by minimizing the signal transmission route through test pins, thereby reducing impedance.

Solution to Problem

[0014] According to the one aspect of the present invention aimed at achieving the aforementioned objectives, a semiconductor test device is provided, comprising a guide plate having at least one guide hole formed on one side, a conductive layer formed on the inner side of the guide hole, and at least one test pin inserted and installed in the guide hole, with one side of the outer side in contact with one side of the conductive layer, and the lower part electrically contacting the semiconductor to be tested; and at least one conductive trace formed on the surface side of the guide plate, wherein one side of the conductive trace is electrically connected to one side of the conductive layer.

[0015] Furthermore, the guide plate is combined with an upper plate with at least one 1st guide hole formed on one side and the lower part of the upper plate, comprising a lower plate formed on one side with at least one 2nd guide hole. Preferably, the conductive trace is formed on at least one of the upper or lower surfaces of the upper plate or the upper or lower surfaces of the lower plate.

[0016] Additionally, the conductive trace may be formed to electrically connect between the conductive layers, which contacts the test pins transmitting mutually identical signals.

[0017] Furthermore, the conductive trace is preferably formed to electrically connect between the conductive layers contacting the grounding test pins.

[0018] In addition, the conductive trace may be extended from one side of the conductive layer, excluding the testing area where the test pins are densely installed, to an area on one side of the guide plate.

Advantageous Effects of Invention

[0019] According to the present invention, as described above, by allowing the test pins to be electrically connected to other test pins or an external substrate through the conductive layer formed in the guide hole, various characteristics such as electrical contact defects of test pins, spatial efficiency, noise, high-frequency characteristics, etc., can be improved. Consequently, there is an effect of enhancing the reliability of test results.

[0020] Furthermore, the present invention achieves a significant improvement in high-frequency performance by minimizing the signal transmission route through the test pins, thereby reducing impedance. This can be accomplished by electrically connecting the test pins transmitting identical signals through the lower surface of the guide plate, and then electronically connecting the conductive trace through the main substrate to an external area on one side of the guide place, excluding the testing area.

Brief Description of Drawings

[0021] Fig. 1 is a diagram illustrating a cross-sectional view of a front-end test device, specifically a probe card, which is an example of a conventional semiconductor test device. Fig. 2 is a cross-sectional view illustrating a semiconductor test device according to one embodiment of the present invention. Fig. 3 is a conceptual diagram illustrating the state where the conductive trace according to one embodiment of the present invention connects between the test pin transmitting identical signals and the conductive layer in contact. Fig. 4 is a diagram illustrating the state where the conductive trace according to one embodiment of the present invention is extended. Fig. 5a is a diagram illustrating the upper surface of the upper plate according to one embodiment of the present invention. Fig. 5b is a diagram illustrating the lower surface of the upper plate according to one embodiment of the present invention. Fig. 6 is a diagram illustrating the state where the conductive trace according to one embodiment of the present invention is connected to the main substrate through wires. Fig. 7 is a diagram illustrating the state where the conductive material according to one embodiment of the present invention is removed using countersinking or counterboring.

Description of Embodiments

[0022] Below, a preferred embodiment of the present invention will be described in detail with reference to the accompanying drawings. In the following description, the term, semiconductor test device is used to describe a probe card for simplicity, but it should be understood that the present invention is not limited to probe cards and is applicable to all semiconductor test devices with multiple test pins. This inclusion is certainly within the technical idea of the present invention.

[0023] Fig. 2 is a cross-sectional view illustrating a semiconductor test device according to one embodiment of the present invention. Fig. 3 is a conceptual diagram illustrating the state where the conductive trace according to one embodiment of the present invention connects between the test pin transmitting identical signals and the conductive layer in contact. Fig. 4 is a diagram illustrating the state where the conductive trace according to one embodiment of the present invention is extended. Fig. 5a is a diagram illustrating the upper surface of the upper plate according to one embodiment of the present invention. Fig. 5b is a diagram illustrating the lower surface of the upper plate according to one embodiment of the present invention. Fig. 6 is a diagram illustrating the state where the conductive trace according to one embodiment of the present invention is connected to the main substrate through wires.

[0024] As shown in Figures 2 to 6, the semiconductor test device (1) according to one embodiment of the present invention comprises a guide plate (10), a conductive layer (20), test pins (30), and a conductive trace (40).

[0025] The guide plate (10) supports the test pins (30) to be described in the latter paragraph and provides the forming area for the conductive trace (40), comprising an upper plate (11) with a plurality of 1st guide holes (11b) formed on one side; a lower plate (12) coupled to the lower part of the upper plate (11) and formed with a plurality of 2nd guide holes (12b) on one side; and a fastening member (13) combined to both the upper plate (11) and the lower plate (12).

[0026] The upper plate (11) is formed roughly in a round or rectangular shape, with a 1st receiving groove (11a) formed on one side of the lower surface, and a plurality of 1st guide holes (11b) formed on one side thereof.

[0027] Furthermore, the lower plate (12) is formed in a disc or rectangular shape corresponding to the upper plate (11). On one side corresponding to the first receiving groove (11a), a second receiving groove (12a) is formed, and on one side, a plurality of second guide holes (12b) are formed.

[0028] As such, the upper plate (11) and lower plate (12) play a role in supporting the test pins (30) as well as providing the forming area for the conductive trace (40) to be described in the latter paragraphs through the outer surface and the inner surface formed by the first receiving groove (11a) and the second receiving groove (12a).

[0029] The conductive layer (20) is formed by coating a conductive material on one side of the upper plate (11) where the first guide holes (11b) are formed or on one side of the lower plate (12) where the second guide holes (12b) are formed. It plays a role in allowing the test pins (30) and conductive trace (40) to be electrically connected to each other, as described in the latter paragraph.

[0030] The test pins (30) are generally formed in a rod shape, inserted and placed in the first guide hole (11b) and the second guide hole (12b), of which one side is electrically contacted with one side of the conductive layer (20), thereby electrically connected to the conductive trace (40) through the conductive layer (20) as described in the latter paragraph.

[0031] In this embodiment, a cobra probe is illustrated as the test pin (30); however, it should be noted that the test pin (30) of the present invention is not necessarily limited to the cobra probe and certainly various probes such as pogo pins, wire probes, and the like can be used.

[0032] Furthermore, in this embodiment, the guide plate is illustrated as being comprised of the upper plate (11) and the lower plate (12); however, the guide plate can also be formed as a single body, such as the socket housing of a test socket.

[0033] The conductive trace (40) is formed on the surface of the guide plate (10), specifically at least one side of the inner or outer side of the upper plate (11), or the inner or outer side of the lower plate (12), using a conductive material, with one side connected to one side of the conductive layer (20). Depending on where the other side is connected, such a conductive trace (40) can perform various functions.

[0034] 1. Connection between the test pin transmitting identical signals and the conductive layers in contact

[0035] As previously explained, the conductive trace (40) is formed on one side of the surface of the guide plate (10), its one side is connected to one side of the conductive layer (20), and the other side can be connected to one side of another conductive layer (20).

[0036] At this time, the conductive layers (20), with which the testing pins (30) of transmitting the same signal are contacted, are connected to each other. For example, as shown in Fig. 3, the plurality of the conductive layers (20), with which the testing pins (30) for ground is contacted, can be connected to each other. Depending on the connection pattern, 2 or several tens or thousands of grounding test pins (30) can be mutually connected.

[0037] As such, the conductive trace (40) according to one embodiment of the present invention mutually connects a plurality of conductive layers (20) in contact with the test pins (30) transmitting identical signals. As shown in FIG. 3, this enables accurate testing even if a contact failure (E) occurs between one of the test pins (30) transmitting identical signals and the corresponding terminal of the space transformer (130).

[0038] 2. Connection between the Conductive Layer and the Main Substrate (or Space Transformer)

[0039] The conductive trace (40), as shown in FIG. 4, can be extended from one side of at least one of the conductive layers (20) from a plurality of the conductive layers (20) to an external area (W), excluding the testing area (T) where the test pins (30) are densely installed.

[0040] In other words, the conductive trace (40) plays a role in extending the contact position between the densely installed test pins (30) in the testing area and the space transformer outside the testing area, which ensures a more convenient connection operation with the space transformer and maintains a stable contact.

[0041] Furthermore, the conductive trace (40) according to one embodiment of the present invention is designed to be directly connected to the main substrate in the external area (W) beyond the testing area (T) without the need for any space transformer. This significantly improves operability and, at the same time, features a shorter signal transmission distance, resulting in lower impedance and greatly enhanced high-frequency performance.

[0042] Additionally, according to one embodiment of the present invention, the conductive trace (40) is extended from the testing area (T) to the external area (W), considerably alleviating spatial constraints in forming the conductive trace (40). This allows for the formation of a conductive trace (40) with a larger area, and the use of thick-wire connections between the conductive trace (40) and the main substrate, thereby further enhancing high-frequency efficiency.

[0043] In one embodiment of the present invention, the test pins (39) transmitting identical signals can be conveniently connected in a confined testing area by grouping a plurality of conductive layers (20) in contact with the test pins (30) transmitting identical signals, along with the trace connecting such conductive layers, and forming each group on the upper surface and the lower surface of the upper plate (11), respectively.

[0044] In one example, as shown in Fig. 5a, a plurality of conductive layers (20) in contact with the grounding test pins (30a) and the conductive traces (40) connecting the same are formed on the upper surface of the upper plate (11). Similarly, as shown in Fig. 5b, a plurality of conductive layers (20) in contact with the power test pins (30b) and the conductive traces (40) connecting the same are formed on the lower surface of the upper plate (12). This allows convenient connection of a plurality of test pins (30) transmitting identical signals without interference with test pins (30) transmitting different signals.

[0045] Furthermore, in one example, it has been described that each group is distinguished and formed only on the upper surface and lower surface of the upper plate (11). However, the present invention is not limited to forming each group only on the upper surface and lower surface of the upper plate (11). Depending on the number of groups, it is possible to form more than one electrically connected group on a single surface, not to mention using both the upper surface and lower surface of the upper plate (11), as well as the upper surface and lower surface of the lower plate (12).

[0046] 3. Connection with the Conductive Layer on the Lower Surface of the Guide Plate

[0047] The conductive trace (40) according to one embodiment of the present invention, as shown in FIG. 6, extends from the testing area (T) to the external area (W) while being connected to the conductive layer (20) on one side of the lower surface of the guide plate (10), i.e., the lower surface of the lower plate (12). The extended conductive trace (40) can be directly connected to the main substrate using a wire.

[0048] Here, the conductive trace (40) plays a role in significantly enhancing high-frequency performance by minimizing the signal transmission route through high-impedance test pins (30) and directly transmitting the signal conveyed by the test pins (30) to the main substrate (120) through thick-diameter wire (J), thereby minimizing noise.

[0049] Fig. 7 is a diagram illustrating a state in which the conductive material according to one embodiment of the present invention is removed using countersinking or counterboring.

[0050] Meanwhile, the conductive layer (20) and the conductive trace (40) according to one embodiment of the present invention can be fabricated using various methods, including the following:

[0051] The first method involves plating or depositing a conductive material on the entire surface of the guide plate (10). Subsequently, from the conductive materials plated or deposited on the guide plate (10), a photo-resister film is formed in areas where the conductive layer (20) and conductive trace (40) are intended to be created. Unnecessary areas of the conductive material formed on the entire surface of the guide plate (10) are then removed through etching solution, resulting in the formation of the desired shapes for the conductive layer (20) and conductive trace (40).

[0052] The second method involves partially forming a photo-resister on the surface of the guide plate (10) where the formation of the conductive layer (20) and conductive trace (40) is unnecessary. Subsequently, the entire surface is plated or deposited with a conductive material, and the conductive material formed on the photo-resister is removed using the lift-off method, resulting in the formation of the desired shapes for the conductive layer (20) and conductive trace (40).

[0053] The third method involves placing a screen on the surface of the guide plate (10) where the formation of the conductive layer (20) and conductive trace (40) is unnecessary. Subsequently, the desired shapes for the conductive layer (20) and conductive trace (40) are formed by depositing a conductive material through the screen.

[0054] Here, a seed layer is formed in the area where the screen is not placed, and the conductive layer (20) and conductive trace (40) can be formed using methods such as electroplating.

[0055] Finally, the entire surface of the guide plate (10) is coated with a conductive material, and the desired shape of the conductive layer (20) and conductive trace (40) can be formed by selectively removing the conductive material from the surface of the guide plate (10) through mechanical processing.

[0056] In one example, when interconnecting ground test pins (30) through the conductive layer (20) and conductive trace (40), a plurality of test pins (30) transmitting identical signals can be connected by removing the conductive material formed at the edge of the guide plate (10), that is the entrance of the guide hole (11a) corresponding to the guide hole where a plurality of test pins (30) are inserted and installed, excluding the grounding test pins (30) using countersinking or counterboring (c), as shown in Fig. 7, ensuring that signal test pins (30) or power test pins (30) other than the grounding test pins (30) are insulated from the grounding test pins (30).

[0057] While the present invention has been described in connection with the preferred embodiments disclosed above, it is evident that various modifications or variations may be made without departing from the abstract and scope of the invention. Therefore, the appended claims are intended to include such modifications or variations that fall within the abstract and scope of the present invention.

Reference Signs List

[0058]

- | | | | |
|------|---------------------------|------|----------------------|
| 1: | Semiconductor test device | 10: | Guide plate |
| 11: | Upper plate | 11a: | 1st receiving groove |
| 11b: | 1st guide hole | 12: | Lower plate |
| 12a: | 2nd receiving groove | 12b: | 2nd guide hole |
| 13: | Fastening member | 20: | Conductive layer |
| 30: | Test pins | 40: | Conductive trace |

Drawings

Fig 1

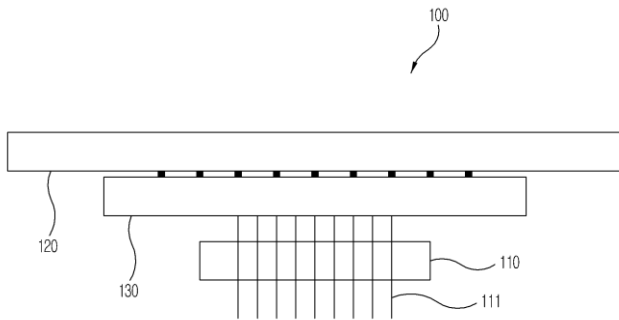


Fig 2

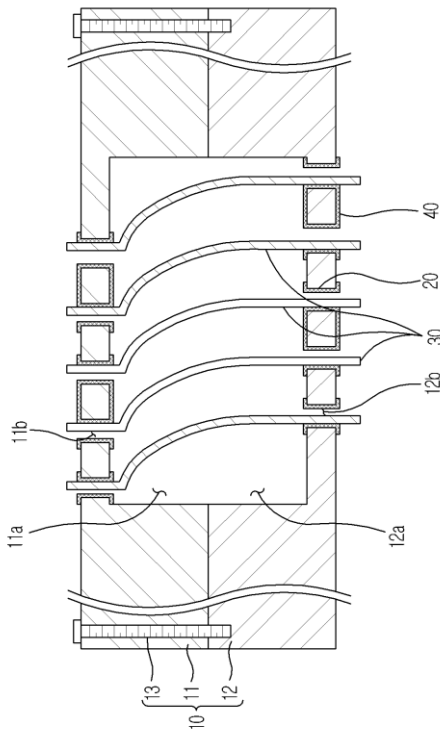


Fig 3

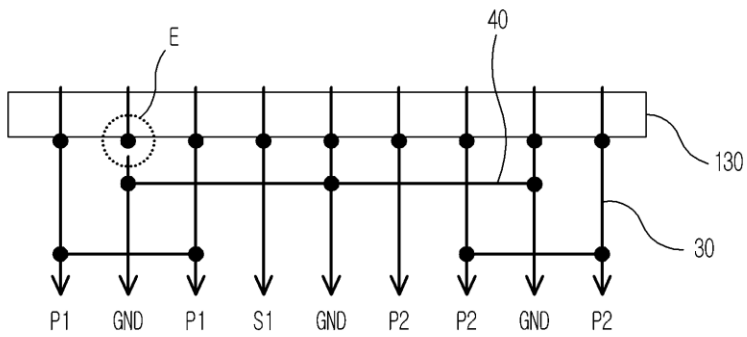


Fig 4

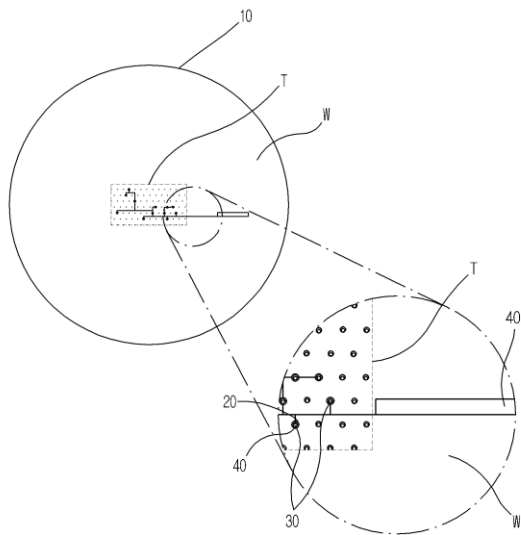


Fig 5a

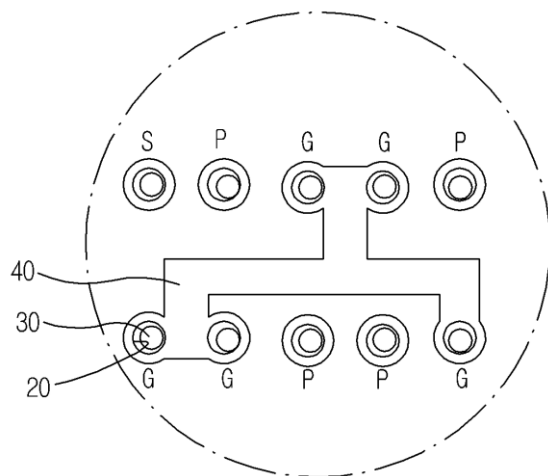


Fig 5b

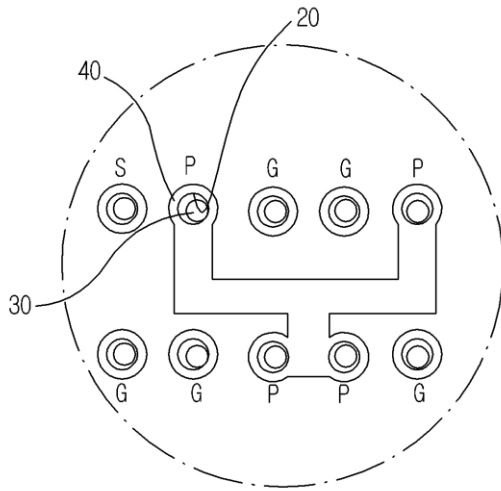


Fig 6

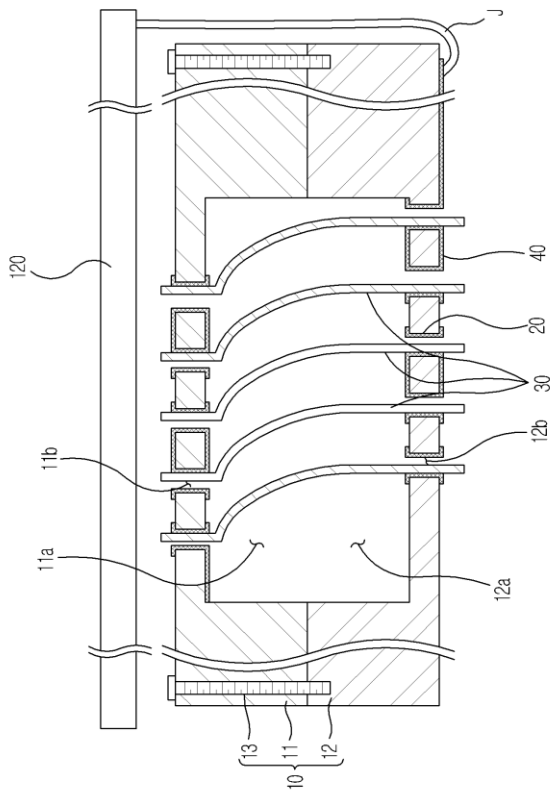


Fig 7

