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G01R 1/067 (2006.01)
G01R 31/26 (2006.01)(72) Inventor: **IL KIM**, Gyeonggi-do (KR)(52) **U.S. Cl.**
CPC **G01R 1/06733** (2013.01); **G01R 31/2601**
(2013.01)(21) Appl. No.: **14/596,762**(57) **ABSTRACT**(22) Filed: **Jan. 14, 2015**

Provided is a semiconductor testing apparatus that a testing pin is rendered to electrically connect to another testing pin or an external substrate through a conductive layer formed in the guide hole, so that it results in enhancement in various characteristics such as poor electrical contact of the testing pin, space efficiency, noise, and high frequency characteristics, thereby improving reliability in testing results.

(30) **Foreign Application Priority Data**

Jan. 14, 2014 (KR) 10-2014-0004576

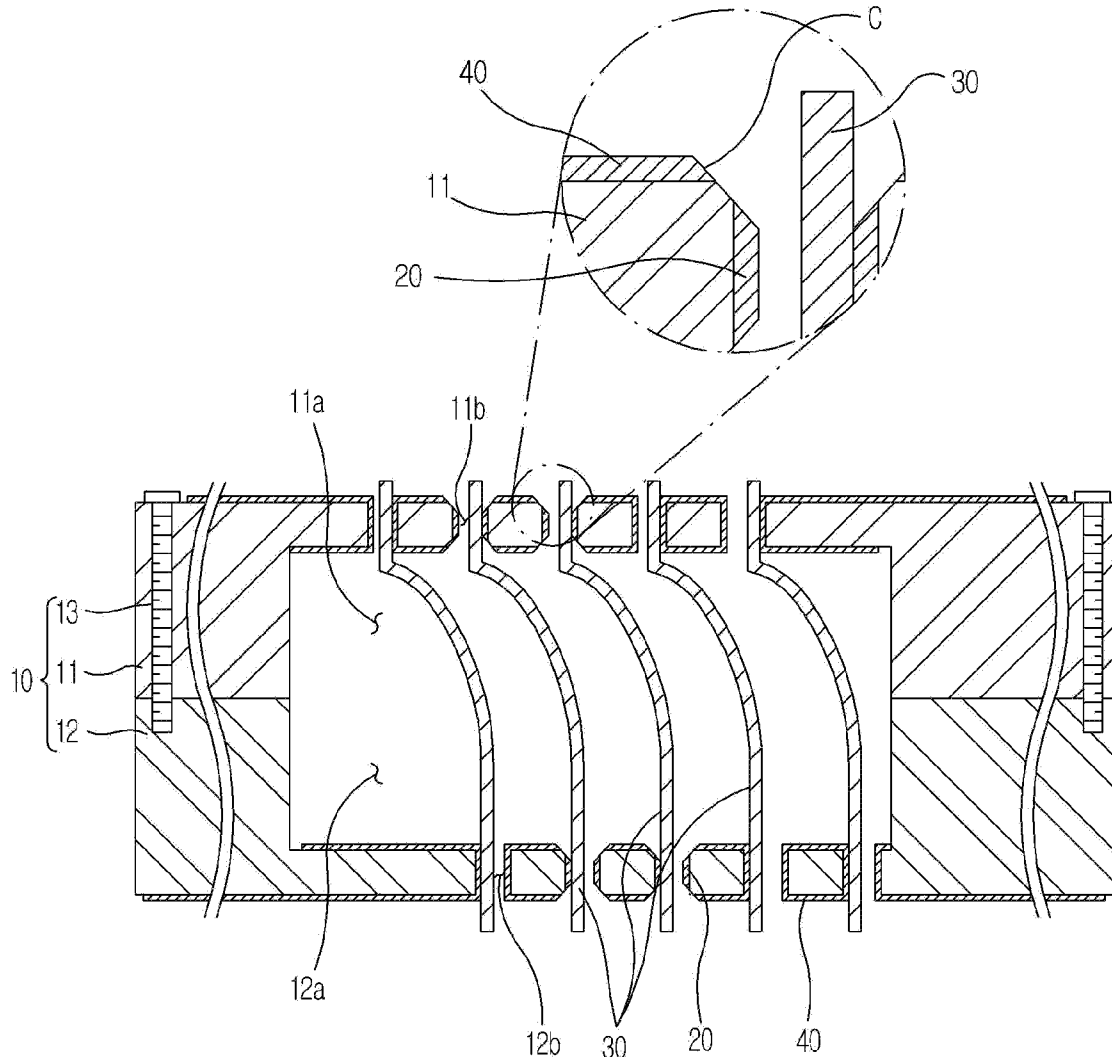


FIG. 1

Prior Art

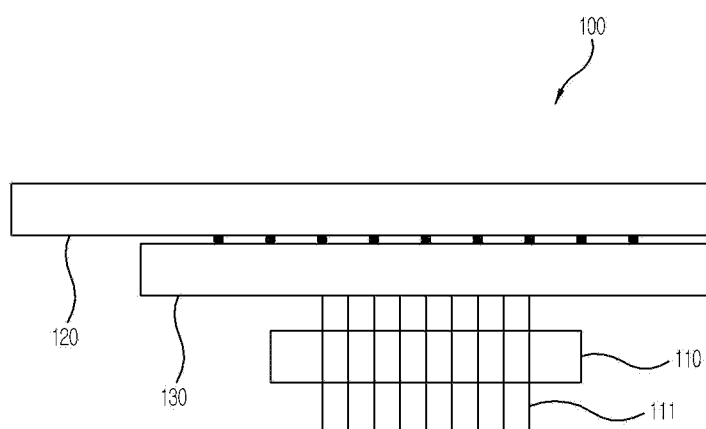


FIG. 2

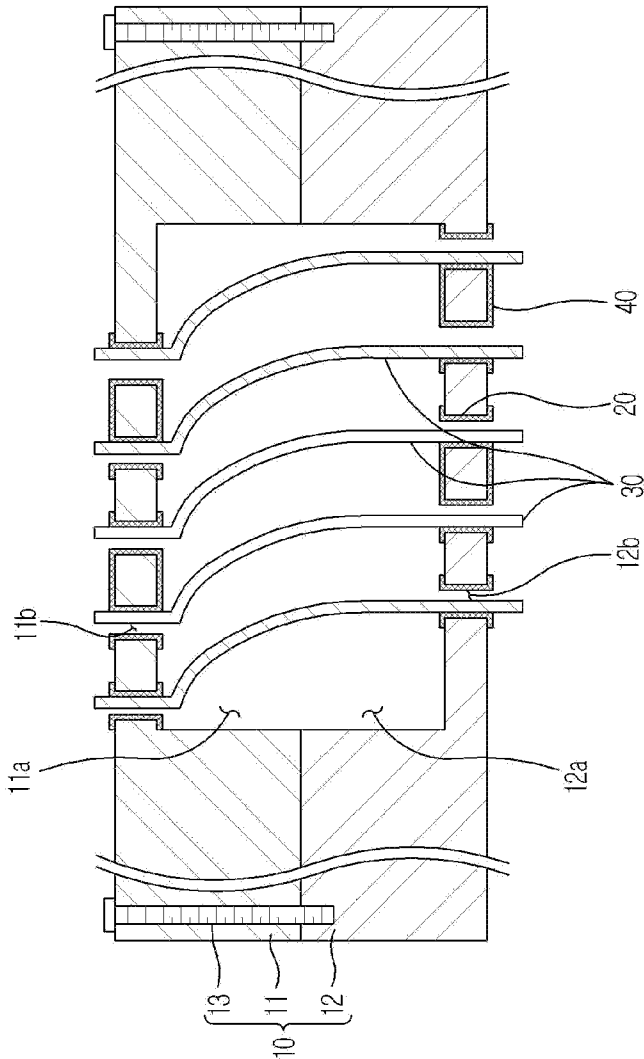


FIG. 4

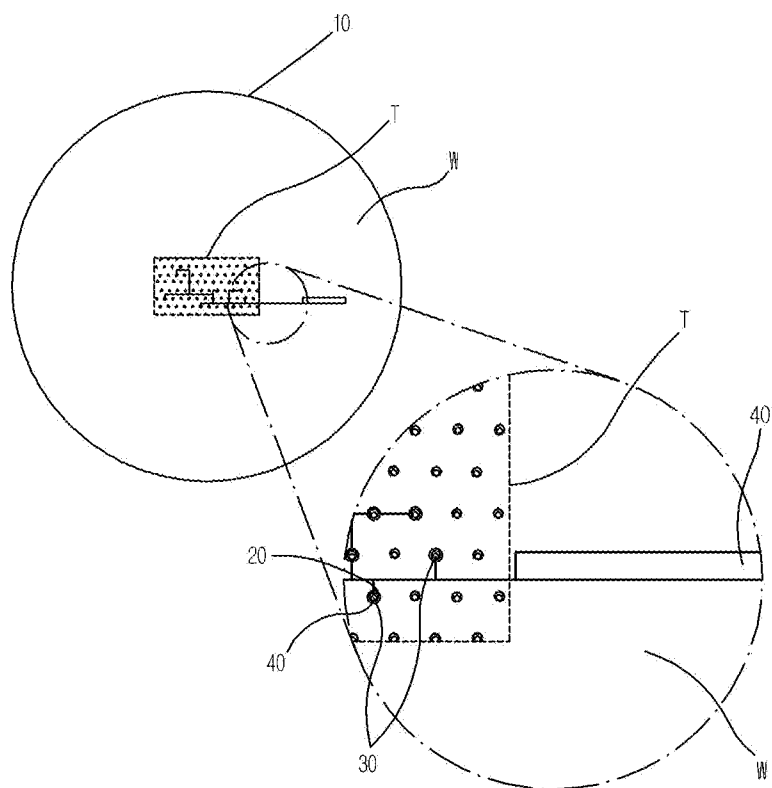


FIG. 5a

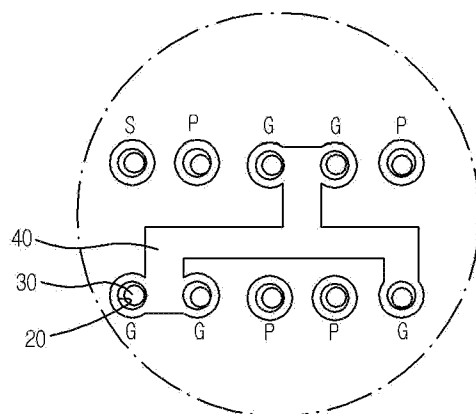


FIG. 5b

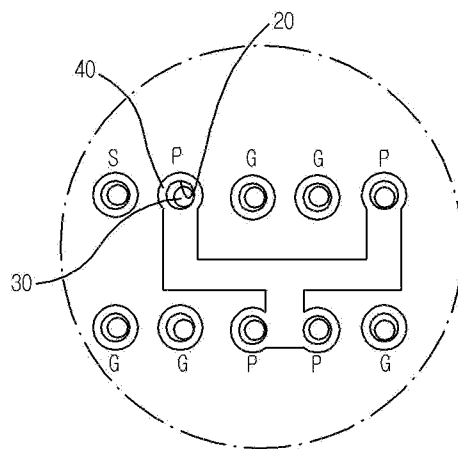
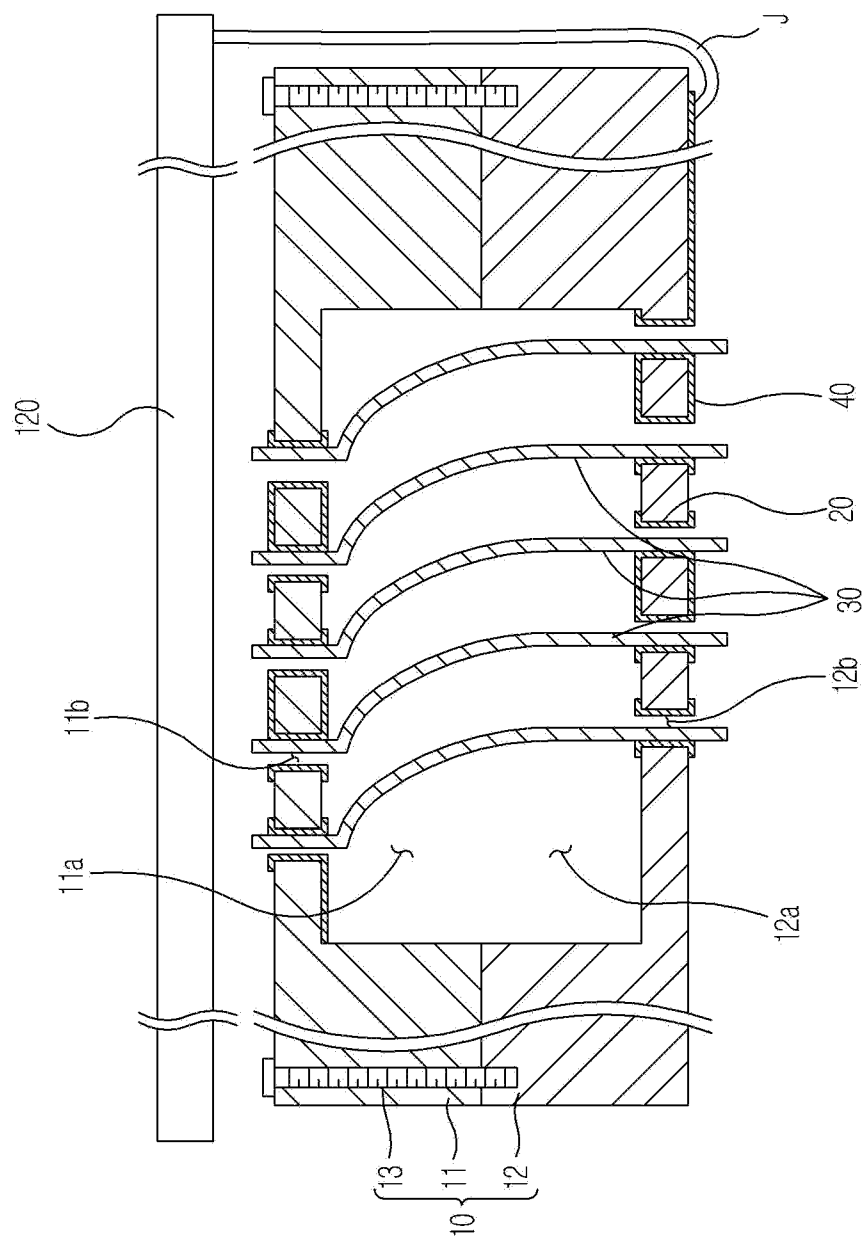


FIG. 6



SEMICONDUCTOR TESTING APPARATUS

CROSS REFERENCE

[0001] The present application claims the benefit of Korean Patent Application No. 10-2014-0004576 filed in the Korean Intellectual Property Office on 14 Jan. 2014, the entire contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a semiconductor testing apparatus, and more particularly, to a semiconductor testing apparatus in that a testing pin is rendered to electrically connect to another testing pin or an external substrate through a conductive layer formed in the guide hole, so that it results in enhancement in various characteristics such as poor electrical contact of the testing pin, space efficiency, noise, and high frequency characteristics, thereby improving reliability in testing results.

[0004] 2. Description of the Related Art

[0005] A semiconductor testing process can divide into a previous process testing, which is an EDS (Electrical Die Sorting) for testing the electrical characteristic of the chip manufactured in the wafer level, and a post-processing test for testing a semiconductor IC manufactured in the package level.

[0006] In the previous process testing, in order to determine the bad chip among chips formed in the wafer, a probe card for applying the electrical signals to the chips and determining the bad chip according to the signal checked through the applied electrical signal is used as the semiconductor testing apparatus. The probe card includes a plurality of testing pins (probe needle) corresponding to the terminal of the wafer.

[0007] In the post-processing test, a test socket for applying the electrical signals to the semiconductor package of IC shape and testing the normal operation condition of the IC is used as the semiconductor testing apparatus. The test socket includes a plurality of pogo pins or conductive rubber sheets corresponding to the terminal of the IC.

[0008] Besides, the semiconductor testing apparatus includes terminals identically with the terminals of the semiconductor formed at one side thereof. In the semiconductor testing apparatus, the terminals are connected to each other or other semiconductor package is extended to one side of the semiconductor package to be connected, thereby performing the test thereof.

[0009] FIG. 1 is a cross-sectional view illustrating a probe card as a previous process testing apparatus according to the conventional semiconductor test apparatus.

[0010] As shown in FIG. 1, the conventional probe card 100 includes a guide plate 110 having a plurality of testing pins 111 electrically contacted with the chips located on the testing stand; a main board 120 separated from the guide plate 110 and formed at the upper portion of the guide plate 110; and a space transformer 130 for spatially matching the electrode pattern of the guide plate 110 having a narrow pitch with the main board 120 having a wide pitch and formed between the guide plate 110 and the main board 120.

[0011] In this conventional probe card 100, when the testing pins 111 are contacted with the semiconductor under test, the electric signal is transmitted to the testing pins 111 from the semiconductor and the electrical signal transmitted to the

testing pins 111 is transmitted to the probe interface board, which is not illustrated therein, through the main board 120.

[0012] Here, in the conventional probe card 100, when the lower end of the test pins 11 is electrically contacted with the semiconductor under test through a DUT (device under test), the upper end of the testing pins 111 is electrically connected to the space transformer 130. At this time, if the electrical contact between one testing pin 111 among many testing pins and the space transformer 130 is unstable, there is a problem in that the result of the DUT test becomes imprecisely. Due to this, the reliability of the test result can be remarkably degraded.

[0013] Since the semiconductor testing device tests the electrical characteristic by applying the electrical signal to the object semiconductor through the testing pins, such problem of the electric contact fault of the testing pin can be identically generated in all semiconductor testing apparatus such as not only the probe card but also the test socket etc.

[0014] Moreover, in the semiconductor testing apparatus, since it is necessary to form the multiple testing pins at the narrow space, there is a problem that the high frequency property is not poor due to the spacious restriction.

SUMMARY OF THE INVENTION

[0015] The present invention has been proposed to solve such problems of the related art, and an object of the invention is to provide a semiconductor testing apparatus in that a testing pin is rendered to electrically connect to another testing pin or an external substrate through a conductive layer formed in the guide hole, so that it results in enhancement in various characteristics such as poor electrical contact of the testing pin, space efficiency, noise, and high frequency characteristics, thereby improving reliability in testing results.

[0016] Another object of the invention is to provide a semiconductor testing apparatus in that a signal transduction length becomes short and an impedance is decreased, so that it can remarkably improve the high frequency performance.

[0017] According to an aspect of the invention to achieve the object described above, there is provided a semiconductor testing apparatus including: a guide plate having at least one or more guide holes formed at one side thereof; a conductive layer formed at one side of an inner surface of the guide hole; at least one testing pin inserted and installed in the guide hole and having one side of an outer surface contacted with one side of the conductive layer and a lower end portion electrically contacted with a semiconductor under test; and at least one or more conductive traces formed at one side of a surface of the guide plate and having one side electrically connected to one side of the conductive layer.

[0018] Preferably, the guide plate includes an upper plate having at least one first guide hole formed at one side thereof and a lower plate coupled to the lower portion of the upper plate and having at least one second guide hole formed at one side thereof; and the conductive trace is formed on at least one surface of upper and lower surfaces of the upper plate or the lower plate.

[0019] Preferably, the conductive trace is electrically connected between the conductive layers with which the testing pins of transmitting the same signal are contacted.

[0020] Preferably, the conductive trace is electrically connected between the conductive layers with which the testing pins for ground are contacted.

[0021] Preferably, the conductive trace is extended and formed toward an area except for a testing area of a side of the

guide plate, on which the testing pins are densely formed, from one side of the conductive layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0022] The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

[0023] FIG. 1 is a cross-sectional view illustrating a probe card as a previous process testing apparatus according to the conventional semiconductor test apparatus;

[0024] FIG. 2 is a schematic cross-sectional view showing a semiconductor testing apparatus according to one embodiment of the present invention;

[0025] FIG. 3 is a conceptual diagram showing a state in that a conductive traces according to one embodiment of the present invention is connected between conductive layers, with which the testing pin of transmitting the same signal is contacted;

[0026] FIG. 4 is a drawing showing a state in that a conductive trace according to one embodiment of the present invention is extended;

[0027] FIG. 5a is a drawing showing an upper surface of an upper plate according to one embodiment of the present invention;

[0028] FIG. 5b is a drawing showing a lower surface of an upper plate according to one embodiment of the present invention;

[0029] FIG. 6 is a drawing showing a state in that a conductive trace according to one embodiment of the present invention is connected to a main board through a wire; and

[0030] FIG. 7 is a drawing showing a state in that the conductive material is removed through a counter sink or a counter bore according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0031] Hereinafter, a preferred embodiment of the invention will be described in detail with reference to the accompanying drawings. Hereinafter, in order to simply make the description, the probe card will be explained as the term called as a semiconductor testing apparatus. However, the present invention is not limited to the probe card. All semiconductor testing apparatus having multiple test pins can be applied thereto.

[0032] FIG. 2 is a schematic cross-sectional view showing a semiconductor testing apparatus according to one embodiment of the present invention; FIG. 3 is a conceptual diagram showing a state in that a conductive traces according to one embodiment of the present invention is connected between conductive layers, with which the testing pin of transmitting the same signal is contacted; FIG. 4 is a drawing showing a state in that a conductive trace according to one embodiment of the present invention is extended; FIG. 5a is a drawing showing an upper surface of an upper plate according to one embodiment of the present invention; FIG. 5b is a drawing showing a lower surface of an upper plate according to one embodiment of the present invention; and FIG. 6 is a drawing showing a state in that a conductive trace according to one embodiment of the present invention is connected to a main board through a wire.

[0033] As shown in the FIG. 2 through FIG. 6, the semiconductor testing apparatus 1 according to one embodiment of the present invention includes a guide plate 10, a conductive layer 20, a testing pin 30, and conductive traces 40.

[0034] The guide plate 10 includes an upper plate 11 having a plurality of first guide holes 11b at a side thereof, a lower plate 12 coupled to the lower portion of the upper plate 11 and having a plurality of second guide holes 12b at a side thereof, and a coupling member 13 for coupling the upper plate 11 to the lower plate 12. The guide plate 10 serves to support the testing pin 30 and provide the forming area of the conductive trace 40 which will be described later.

[0035] The upper plate 11 is in the form of a circular or a rectangular plate shape and has a first containing groove 11a formed on one side of a lower surface thereof and a plurality of first guide holes 11b formed at one side thereof.

[0036] The lower plate 12 is in the form of a circular or a rectangular plate shape corresponding to the upper plate 11 and has a second containing groove 12a formed on one side of an upper surface thereof corresponding to the first containing groove 11a and a plurality of second guide holes 12b formed at one side thereof.

[0037] The upper plate 11 and the lower plate 12 serve to provide the forming area of the conductive trace 40, which will be described later, by means of the outer surfaces thereof and the inner surfaces formed by the first containing groove 11a and the second containing groove 12a.

[0038] The conductive layer 20 is formed at one side of the upper plate 11, in which the first guide holes 11b are formed, or one side of the lower plate, in which the second guide holes 12b are formed, through the coating of the conductive material. The conductive layer 20 serves to electrically connect the testing pin 30 and the conductive trace 40, which will be described later, to each other.

[0039] The testing pin 30 of an approximately rod shape is inserted into the first guide hole 11b and the second guide hole 12b to be arranged. One side thereof is electrically contacted with one side of the conductive layer 20 and it is connected electrically through the conductive layer 20 with the conductive trace 40 which will be described later. The testing pin 30 is electrically contacted with the conductive layer 20 and electrically connected to the conductive trace 40, which will be described later.

[0040] In the meantime, in the present embodiment, a cobra type probe is used as the testing pin 30. However, the present invention is limited to the cobra type probe. The testing pin 30 may be various probes such as a pogo pin or a wire probe etc.

[0041] Also, in the present embodiment, the guide plate includes the upper plate 11 and the lower plate 12. However, the guide plate can be formed with one body like a socket housing of a test socket.

[0042] The conductive trace 40 is formed on the surface of the guide plate 10 by using the conductive material. That is, the conductive trace 40 is formed on at least one surface of the inner and outer surfaces of the upper plate 11 and the lower plate 12. One side of the conductive trace 40 is connected to one side of the conductive layer 20. At this time, the conductive trace 40 can perform various functions depending on where the other side thereof is connected, as described below.

1. Connection Between the Conductive Layers with which the Testing Pin of Transmitting the Same Signal is Contacted

[0043] As described above, the conductive trace 40 is formed on one side of the surface of the guide plate 10. Also, one side of the conductive trace 40 is connected to one side of

the conductive layer 20 and the other side thereof is connected to one side of other conductive layer 20.

[0044] At this time, the conductive layers 20, with which the testing pin of transmitting the same signal is contacted, are connected to each other. For example, as shown in FIG. 3, the plurality of the conductive layers 20, with which the testing pin for ground is contacted, can be connected to each other. Accordingly, two testing pins for ground, several tens of the testing pins for ground, or several thousands of the testing pin for ground can be connected to each other according to the connectivity pattern.

[0045] As described above, since the conductive trace 40 according to one embodiment of the present invention allow the plurality of the conductive layers 20, with which the plurality of testing pin 30 of transmitting the same signal is contacted, to be connected to each other, although the poor contact E between one testing pin among the plurality of testing pins 30 of transmitting the same signal and the corresponding terminals of the space transformer 130 is generated as shown in FIG. 3, the correct test can be performed.

2. Connection Between Main Board (or Space Transformer) and Conductive Layer

[0046] As shown in FIG. 4, the conductive trace 40 can be extended and formed toward the external area W except for the testing area T of the surface of the guide plate 10, on which the testing pins 30 are densely formed, from one side of at least one conductive layer 20.

[0047] That is, since the conductive trace 40 allows the contact position between the testing pins 30 densely formed within the testing area and the space transformer to be extended to the outside of the testing area, the connection work with the space transformer is very easy and the stable contact can be maintained.

[0048] Also, since the conductive trace 40 according to one embodiment of the present invention can be directly connected to the main board without the separate space transformer on the external area W, which is deviated from the testing area T, it can remarkably improve the workability thereof. Also, since the signal transduction length becomes short and the impedance is decreased, it can remarkably improve the high frequency performance.

[0049] Moreover, according to one embodiment of the present invention, the conductive trace 40 can be extended to the external area W from the testing area T, so that the spatial restriction for forming the conductive traces 40 can be considerably solved. Accordingly, the conductive trace 40 has a large area and the conductive trace 40 and the main board are connected to each other by using the wire having a thick diameter, the radio frequency effect can be more improved.

[0050] In the meantime, in one embodiment of the present invention, the plurality of the conductive layers 20, with which the testing pins 30 of transmitting the same signal are contacted, and the conductive traces for connecting them are set to a plurality of groups and each group is formed at the upper surface and the lower surface of the upper plate 11 respectively, so that the testing pins 30 of transmitting the same signal in the narrow testing area can be easily connected.

[0051] For example, the plurality of the conductive layers 20, with which the testing pins 30 of transmitting the same signal are contacted, and the conductive traces 40 for connecting them are formed at the upper surface of the upper plate 11 as shown in FIG. 5a and the plurality of the conduc-

tive layers 20, with which the testing pins 30 for ground are contacted, and the conductive traces 40 for connecting them are formed at the lower surface of the upper plate 11 as shown in FIG. 5b, so that the testing pins 30 of transmitting the same signal can be easily connected without interfering with the testing pin 30 of transmitting the other signal.

[0052] Also, in the drawings, each group is formed at only the upper surface and the lower surface of the upper plate 11. However, the present invention is limited to the position of the groups. That is, each group can be formed at the upper surface and the lower surface of both upper and lower plates 11 and 12 according to the number of the groups. Also, at least one electrical connecting group can be formed on one surface thereof.

3. Connection with Conductive Layer in Lower Surface of Guide Plate.

[0053] In the meantime, as shown in FIG. 6, the conductive trace 40 can be extended to the external area W from the testing area T in a state that one side of the conductive trace 40 is connected to the conductive layer 20 at the lower surface of the guide plate 10, that is the lower surface of the lower plate 12. Then, the extended conductive trace 40 and the main board can be directly connected by using the wire.

[0054] Here, the high conductive trace 40 can minimize the signal transduction route through the testing pin 30 with a high impedance and the signal transmitted to the testing pin 30 can be directly transmitted to the main board 120 through the thick wire J, so that the noise is minimized, thereby remarkably improving the high frequency performance thereof.

[0055] FIG. 7 is a drawing showing a state in that the conductive material is removed through a counter sink or a counter bore according to one embodiment of the present invention.

[0056] In the meantime, the conductive layer 20 and the conductive trace 40 according to one embodiment of the present invention can be manufactured by the following various method.

[0057] In the first method, after the conductive material is plated or deposited on the entire surface of the guide plate 10, a photoresistor film is formed on an area for forming the conductive layer 20 and conductive trace 40 among the plated or deposited conductive materials. Then, unnecessary areas among the conductive materials formed on the entire surface of the guide plate 10 are removed through an etching solution, so that it forms the conductive layer 20 and conductive trace 40.

[0058] In the second method, after a photoresistor is partially formed on the surface of the guide plate 10, in that the forming of the conductive layer 20 and conductive trace 40 is unnecessary, the conductive material is entirely plated or deposited thereon. Then, the conductive materials formed on the photoresistor are removed through a lift-off method, so that it forms the conductive layer 20 and conductive trace 40 in the desiring shape.

[0059] In the third method, after a screen is arranged on the surface of the guide plate 10, in that the forming of the conductive layer 20 and conductive trace 40 is unnecessary, the conductive material is deposited thereon, so that it forms the conductive layer 20 and conductive trace 40 in the desiring shape.

[0060] Here, the seed layer is formed on the area in which the screen is not arranged and the conductive layer 20 and conductive trace 40 can be formed through the electroplating method etc.

[0061] In the last method, the conductive materials are deposited on the entire surface of the guide plate 10 and then, the conductive materials are selectively removed from the surface of the guide plate 10 through the machining, so that it forms the conductive layer 20 and conductive trace 40 in the desiring shape.

[0062] For example, where it is intended to connect the testing pins 30 for ground to each other through the conductive layer 20 and conductive trace 40, as shown in FIG. 7, the conductive materials formed at the corner of the guide plate corresponding to the guide hole, into which the testing pins 30 except for the testing pins 30 for ground are inserted, that is the entrance of the guide hole 11a is removed through the counter sink or the counter bore C, so that the testing pins 30 for signal or the testing pins 30 for power are insulated with the testing pins 30 for ground, thereby connecting the plurality of the testing pins 30 of transmitting the same signal to each other.

[0063] According to the present invention, the testing pin is rendered to electrically connect to another testing pin or an external substrate through the conductive layer formed in the guide hole, thus resulting in enhancement in various characteristics such as poor electrical contact of the testing pin, space efficiency, noise, and high frequency characteristics. Accordingly, increased reliability in testing results may be obtained.

[0064] Also, after the testing pins of transmitting the same signal are electrically connected to each other through a lower surface of the lower plate of the guide plate, the conductive trace 40 is electrically connected to the main board through the external area deviated from the testing area, so that the signal transduction route is minimized through the testing pin and the impedance is decreased, thereby remarkably improving the high frequency performance.

[0065] Although the invention has been described according to the preferred embodiment mentioned above, the inven-

tion can be variously changed and modified without deviating from the essential point and scope of the invention. Accordingly, the accompanying Claims include such change and modification belonging to the essential point of the invention.

What is claimed is:

1. A semiconductor testing apparatus comprising:
 - a guide plate having at least one or more guide holes formed at one side thereof;
 - a conductive layer formed at one side of an inner surface of the guide hole;
 - at least one testing pin inserted and installed in the guide hole and having one side of an outer surface contacted with one side of the conductive layer and a lower end portion electrically contacted with a semiconductor under test; and
 - at least one or more conductive traces formed at one side of a surface of the guide plate and having one side electrically connected to one side of the conductive layer.
2. A semiconductor testing apparatus, as claimed in claim 1, wherein the guide plate comprises an upper plate having at least one first guide hole formed at one side thereof and a lower plate coupled to the lower portion of the upper plate and having at least one second guide hole formed at one side thereof; and the conductive trace is formed on at least one surface of upper and lower surfaces of the upper plate or the lower plate.
3. A semiconductor testing apparatus, as claimed in claim 1, wherein the conductive trace is electrically connected between the conductive layers with which the testing pins of transmitting the same signal are contacted.
4. A semiconductor testing apparatus, as claimed in claim 1, wherein the conductive trace is electrically connected between the conductive layers with which the testing pins for ground are contacted.
5. A semiconductor testing apparatus, as claimed in claim 1, wherein the conductive trace is extended and formed toward an area except for a testing area of a side of the guide plate, on which the testing pins are densely formed, from one side of the conductive layer.

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