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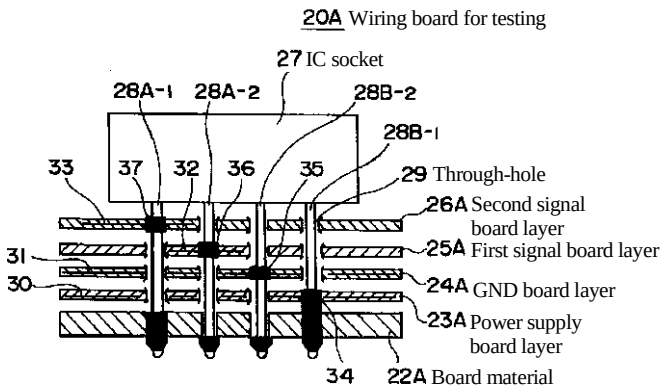
(54) [Title of Invention] WIRING BOARD FOR TESTING

(57) [Abstract]

[Problem] The present invention relates to a wiring board for testing having a structure in which a plurality of a wiring board layer in which a wiring pattern connected to a lead of an IC socket is formed on an insulating board is laminated and formed, and aims to reduce costs as well as improve manufacturing efficiency.

[Resolution Means] In a wiring board for testing having a structure in which a plurality of wiring board layers 23A to 26A are laminated and formed, and to which an IC socket 7 having a lead 28 is mounted, a power supply board layer 23A and a GND board layer 24A which are used in common even when the types of the IC socket 7 are different are utilized as-is, and a first and second signal board layer 25A, 25B are configured so as to be selectable corresponding to the type of the IC socket 7.

A diagram for describing a method for mounting an IC socket on the wiring board for testing that is the first embodiment of the present invention, and a mounted state.



[Scope of Patent Claims]

[Claim 1] A wiring board for testing having a structure in which a plurality of a wiring board layer having a wiring pattern formed on an insulating board is laminated and formed, and having a through-hole formed into which is inserted a lead provided on a socket for a semiconductor device on which a semiconductor device is mounted, wherein the wiring board layer is provided with: a common wiring board layer on which is formed a common wiring pattern connected to a common lead that is common to different types of the socket for a semiconductor device; and a non-common wiring board layer on which is formed a non-common wiring pattern connected to a non-common lead, and having a configuration in which the non-common wiring board layer can be selected corresponding to a type of the IC socket for a semiconductor device.

[Claim 2] The wiring board for testing according to claim 1, further comprising a fixing mechanism for detachably fixing a plurality of the wiring board layer to be laminated.

[Claim 3] The wiring board for testing according to claim 2, wherein the fixing mechanism is a magnet arranged on the wiring board layer.

[Claim 4] The wiring board for testing according to any one of claims 1 to 3, further comprising a positioning mechanism for positioning a plurality of the wiring board layer to be laminated.

[Claim 5] The wiring board for testing according to claim 4, wherein the positioning mechanism is configured by: a positioning base configured having a positioning support erected; and a positioning hole formed in the wiring board so as to correspond to a forming position of the positioning support.

[Claim 6] The wiring board for testing according to any one of claims 1 to 5, wherein a lead-out pattern for leading out a wiring pattern connected to the lead to outside of a disposition region of the IC socket is formed on the wiring board layer.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention] The present invention relates to a wiring board for testing and particularly relates to a wiring board for testing having a structure in which a plurality of a wiring board layer in which a wiring pattern connected to a lead of an IC

socket is formed on an insulating board is laminated and formed. In recent years, various tests have been performed on semiconductor devices in order to improve reliability of the semiconductor devices. These tests are performed by mounting the semiconductor device on the wiring board for testing. The wiring board for testing has a structure in which a socket for a semiconductor device for mounting a semiconductor device on a normal multilayer substrate is arranged.

[0002] However, semiconductor devices of a variety of configurations are provided and, for example, there are semiconductor devices having different properties for each terminal despite having a same shape and same number of terminals. Therefore, it is desirable to test semiconductor devices having such a variety of configurations efficiently and at low cost.

[0003]

[Conventional Art] Conventionally, a reliability test of a semiconductor device (hereinafter referred to as an IC) such as a burn-in test are performed using a wiring board for testing. FIG. 1 to FIG. 3 illustrate a conventional wiring board for testing 1. As illustrated in FIG. 1, a printed wiring board having a multilayer structure are common as a conventionally used wiring board for testing 1.

[0004] In the example of the wiring board for testing 1 illustrated in FIG. 1, a structure is had in which a GND (ground) wiring layer 3 and a first signal wiring layer 4 are laminated on an upper surface side of a board material 2, and a power supply wiring layer 5 and a second signal wiring layer 6 are sequentially laminated on a lower surface side. That is, the wiring board for testing 1 has a four-layer structure as a whole interposing the board material 2. Furthermore, as illustrated in FIG. 2, a plurality of the IC socket 7 is arranged on the wiring board for testing 1, and a prescribed test is performed while the IC is mounted on the IC socket 7. Furthermore, a terminal portion 8 is provided on one end portion of the wiring board for testing 1, and this terminal portion 8 is connected to a tester (IC testing device) to perform testing on the IC.

[0005] FIG. 3 illustrates a method for mounting the IC socket 7 on the wiring board for testing 1. As illustrated in FIG. 3, a lead 9 is provided on a lower surface of the IC socket 7, and a through-hole 10 corresponding to the lead 9 is formed in a socket mounting position of the wiring board for testing 1. The IC socket 7 is equipped on the wiring board for testing 1 by inserting the lead 9 into the through-hole 10 and selectively connecting (soldering) the lead 9 to

prescribed wiring layers 3 to 6.

[0006] Furthermore, when testing the IC, when there is a defect in the wiring board for testing 1 itself, an accurate test cannot be performed. Therefore, testing is performed on the wiring board for testing 1 using the automatic inspection device 11 illustrated in FIG. 4. This automatic inspection device 11 is configured by a board stocker 12 and a device main body 13. The wiring board for testing 1 stored in the board stocker 12 is automatically conveyed from the board stocker 12 to the device main body 13 on which a head for testing is arranged. A configuration is had in which the head for testing is connected to the wiring board for testing 1, and a defect inspection is performed.

[0007]

[Problem to be Solved by the Invention] However, in recent years, with the high integration of ICs, the number of terminals has rapidly increased and the pitch has drastically narrowed. Therefore, the structure of the IC socket 7 for mounting the IC and the wiring board for testing 1 for mounting the IC socket 7 are also becoming complicated. Furthermore, types of ICs are also becoming more diverse, and this also is also a factor in complicating the structure of the wiring board for testing 1.

[0008] Because the conventional wiring board for testing 1 uses a multilayer structure printed wiring board, the layers configuring this cannot be formed independently. Therefore, the wiring board for testing 1 are developed, designed, and produced so as to correspond individually to each type of IC. Thus, there is a problem in that the cost required for the development, design, and production of these becomes enormous and the time required until manufacture becomes long.

[0009] In light of the above points, an object of the present invention is to provide a wiring board for testing that can reduce cost and improve manufacturing efficiency.

[0010]

[Means for Solving the Problem] The present invention is characterized in that the following means are given to solve the problems described above. The invention according to claim 1 is characterized by a wiring board for testing having a structure in which a plurality of a wiring board layer having a wiring pattern formed on an insulating board is laminated and formed, and having a through-hole formed into which is inserted a lead provided on a socket for a semiconductor device on which a semiconductor device is mounted, wherein the wiring board layer is

provided with: a common wiring board layer on which is formed a common wiring pattern connected to a common lead that is common to different types of the socket for a semiconductor device; and a non-common wiring board layer on which is formed a non-common wiring pattern connected to a non-common lead, and having a configuration in which the non-common wiring board layer can be selected corresponding to a type of the IC socket for a semiconductor device.

[0011] Furthermore, the invention according to claim 2 is characterized by the wiring board for testing according to claim 1, further comprising a fixing mechanism for detachably fixing a plurality of the wiring board layer to be laminated. Furthermore, the invention according to claim 3 is characterized by the wiring board for testing according to claim 2, wherein the fixing mechanism is a magnet arranged on the wiring board layer.

[0012] Furthermore, the invention according to claim 4 is characterized by the wiring board for testing according to any one of claims 1 to 3, further comprising a positioning mechanism for positioning a plurality of the wiring board layer to be laminated. Furthermore, the invention according to claim 5 is characterized by the wiring board for testing according to claim 4, wherein the positioning mechanism is configured by: a positioning base configured having a positioning support erected; and a positioning hole formed in the wiring board so as to correspond to a forming position of the positioning support.

[0013] Furthermore, the invention according to claim 6 is characterized by the wiring board for testing according to any one of claims 1 to 5, wherein a lead-out pattern for leading out a wiring pattern connected to the lead to outside of a disposition region of the IC socket is formed on the wiring board layer.

[0014] Each of the means described above has an effect as follows. According to the invention of claim 1, the common wiring board layer configuring the wiring board layer has the common wiring pattern formed that is connected to the common lead that is common to different types of the socket for a semiconductor device, and therefore can be used in common for various types of semiconductor devices.

[0015] Furthermore, the non-common wiring board layer configuring the wiring board layer has the non-common wiring pattern formed that is connected to the non-common lead, and therefore can be applied only to a semiconductor device having a structure corresponding to the non-common lead. Furthermore, because of the configuration in which the non-

common wiring board layer can be selected corresponding to a type of an IC socket for a semiconductor device, when designing and developing the wiring board for testing, it is permissible to only design and develop the non-common wiring board layer, and there is no need to design and develop a common wiring board layer. Thus, it is possible to reduce design and development costs of the wiring board for testing corresponding to a new semiconductor device, and to increase manufacturing efficiency.

[0016] Furthermore, according to the invention of claim 2 and claim 3, by providing the fixing mechanism (for example, a magnet) for detachably fixing a plurality of the wiring board layer to be laminated, each wiring board layer can be easily fixed, and it is possible to replace only a specific wiring board layer. Furthermore, according to the invention of claim 4 and claim 5, by providing the positioning mechanism for positioning the plurality of the wiring board layer to be laminated, a process of laminating each wiring board layer, and in particular, a process of positioning the through-hole, can be easily performed.

[0017] Moreover, according to the invention of claim 6, by forming, on the wiring board layer, the lead-out pattern for leading out the wiring pattern connected to the lead to outside of the disposition region of the IC socket, by connecting a test device of the semiconductor device to this lead-out pattern, it is possible to individually test the semiconductor devices mounted on each IC socket. Accordingly, a defective semiconductor device can be easily and reliably specified.

[0018]

[Embodiments of the Invention] Next, embodiments of the present invention will be described together with drawings. FIG. 5 to FIG. 8 are diagrams for describing a wiring board for testing 20A that is a first embodiment of the present invention. The wiring board for testing 20A is used for reliability testing of a semiconductor device (hereinafter referred to as IC) such as burn-in testing.

[0019] As illustrated in FIG. 5, the wiring board for testing 20A according to the present embodiment has a four-layer structure (five layers when including a board material 22A), and has a structure in which the board material 22A, the power supply wiring board layer 23A (hereinafter referred to as a power supply board layer), a GND wiring board layer 24A (hereinafter referred to as a GND board layer), a first signal wiring board layer 25A (hereinafter referred to

as a first signal board layer), and a second signal wiring board layer 26A (hereinafter referred to as a second signal board layer) are sequentially laminated from a bottom portion.

[0020] FIG. 6 is a diagram for describing a method for mounting an IC socket 27 on the wiring board for testing 20A and a mounted state. As illustrated in FIG. 6, the wiring board for testing 20A has a through-hole 29 that vertically penetrates the board material 22A and each board layer 23A to 26A. A forming position of the through-hole 29 is set to correspond to a forming position of leads 28A, 28B provided on the IC socket 27.

[0021] Furthermore, wiring 30 to 33 is formed on each board layer 23A to 26A as will be described later, and among these wirings 30 to 33, a predetermined wiring is configured to be exposed to the through-hole 29 and connected to the leads 28A, 28B. Note that portions where these wirings 30 to 33 and leads 28A, 28B connect are referred to hereinafter as connecting portions 34 to 37. To mount the IC socket 27 on the wiring board for testing 20A, the leads 28A, 28B of the IC socket 27 and the through-hole 29 are positioned, then the leads 28A, 28B are inserted into the through-hole 29. Then, by performing, for example, a solder dipping process or the like, solder enters into the through-hole 29, and the prescribed wirings 30 to 33 exposed in the through-hole 29 and the leads 28A, 28B are soldered, thereby forming the connecting portions 34 to 37.

[0022] FIG. 7 illustrates the board material 22A and each wiring board layer 23A to 26A that configure the wiring board for testing 20A individually. As illustrated in FIG. 7, a through-hole portion 29a is formed in a prescribed position of the board material 22A and each wiring board layer 23A to 26A, and each through-hole portion 29a communicates in a state in which the board material 22A and each wiring board layer 23A to 26A are laminated to configure the through-hole 29 (see FIG. 6).

[0023] Furthermore, a magnet portion 40 is respectively formed on a peripheral position of the board material 22A and each wiring board layer 23A to 26A. The magnet portion 40 is a thin plate shaped magnet and detachably fixes each board layer 23A to 26A by a magnetic force in a state in which the board material 22A and each wiring board layer 23A to 26A are laminated. Thus, the board material 22A and each wiring board layer 23A to 26A can be easily fixed, and it is also possible to replace only a specific wiring board layer.

[0024] Next, a configuration of the board material 22A and each wiring board layer 23A to 26A will be described. As illustrated in FIG. 7(A), the second signal board layer 26A positioned at a topmost portion has a second wiring pattern 33 of a prescribed shape (pattern) formed on an insulating resin film 38A (hereinafter referred to as a base material) such as polyimide or the like. The second wiring pattern 33 may be obtained by casting a copper foil into a prescribed pattern by using, for example, an etching technique.

[0025] The second wiring pattern 33 is connected to a predetermined through-hole section 29a among a plurality of the formed through-hole portion 29a. Furthermore, the through-hole portion 29a forms the connecting portion 37 by soldering to a non-common lead 28A-1 provided on the IC socket 27. Furthermore, as illustrated in FIG. 7(B), the first signal board layer 25A positioned on a second layer from a top portion has a first wiring pattern 32 of a prescribed shape formed on the base material 38A. The first wiring pattern 32 may also be obtained by casting a copper foil into a prescribed pattern by using, for example, an etching technique. The first wiring pattern 32 is connected to a predetermined through-hole section 29a among the plurality of formed through-hole portions 29a. Furthermore, the through-hole portion 29a forms the connecting portion 36 by soldering to a non-common lead 28A-2 provided on the IC socket 27.

[0026] However, with the first and second signal board layers 25A, 26A described above, when, for example, a terminal property of the IC is changed in conjunction with a design change of the IC, the position of the through-hole portion 29a that connects each wiring pattern 32, 33 also changes. Specifically, when citing the second signal board layer 26A in FIG. 7(A) as an example, there may be a need to provide the connecting portion 37 in the through-hole portion 29a of the position illustrated by arrow B in the figure after the change to an IC where the connecting portion 37 is provided in the through-hole portion 29a of the position illustrated by arrow A in the figure before the change. At this time, the second wiring pattern 33 must be newly reformed. That is, the second signal board layer 26A must be newly designed and developed. The same is true for the first signal board layer 25A.

[0027] Such a board layer that must be newly designed and developed (in the present embodiment, the first and second signal board layers 25A, 26A) in conjunction with a design change or the like of the IC,

in the following description, is particularly called a non-common board layer, and a lead of the IC socket 27 connected to a non-common board layer is particularly called a non-common lead (in the present embodiment, leads 28A-1, 28A-2).

[0028] Meanwhile, as illustrated in FIG. 7(C), the GND board layer 24A positioned on a third layer from the top portion has a GND plane wiring 31 formed on substantially an entire surface of the base material 38A. In this GND plane wiring 31, a non-connecting portion 39 is formed by etching or the like on a periphery of the through-hole portions 29a except for the through-hole portion 29a where the connecting portion 35 is desired to be formed. A common lead 28B-2 provided on the IC socket 27 is inserted through the through-hole portion 29a connected to the GND plane wiring 31 and the connecting portion 35 is formed by soldering.

[0029] Furthermore, as illustrated in FIG. 7(D), the power supply board layer 23A positioned on a fourth layer from the top portion has a power supply plane wiring 30 formed on substantially the entire surface of the base material 38A. In this power supply plane wiring 30, the non-connecting portion 39 is formed by etching or the like on the periphery of the through-hole portions 29a except for the through-hole portion 29a where the connecting portion 34 is desired to be formed. A common lead 28B-1 provided on the IC socket 27 is inserted through the through-hole portion 29a connected to the power supply plane wiring 30 and the connecting portion 34 is formed by soldering.

[0030] However, with the power supply board layer 23A and the GND board layer 24A described above, because a power supply terminal position and GND terminal position of a normal IC are not changed even when a terminal property of the IC is changed in conjunction with, for example, a design change of the IC, the position of the through-hole portions 29a where the connecting portions 34, 35 are formed is not changed. That is, even when the IC design is changed, there is no need for the power supply board layer 23A and the GND board layer 24A to be newly designed and developed.

[0031] Such a board layer that need not be newly designed and developed (in the present embodiment, the power supply board layer 23A and the GND board layer 24A) even when there is a design change or the like of the IC, in the following description, is particularly called a common board layer, and a lead of the IC socket 27 connected to a common board layer is particularly called a common lead (in the present

embodiment, leads 28B-1, 28B-2).

[0032] As described above, the wiring board for testing 20A according to the present embodiment, unlike the conventionally used printed wiring board 1 (see FIG. 1 to FIG. 3) of a laminated structure, has the board material 22A and each board layer 23A to 26A independent of each other, thereby enabling selection and use of any of the board layers 23A to 26A. Specifically, the power supply board layer 23A and the GND board layer 24A, which are common board layers, may be used in common for different types of the IC socket 27 (that is, different types of ICs), and therefore can be used in common even when, for example, the IC is changed.

[0033] In contrast to this, the first and second board layers 25A, 26A, which are non-common wiring board layers, must be newly designed and developed when there is a design change or the like of the IC. However, in the conventional printed wiring board 1 of a laminated structure, because of the configuration in which each of the layers 3 to 6 are integrally laminated as illustrated in FIG. 1, all of the layers 3 to 6, including the GND wiring layer 3 and the power supply wiring layer 5, must be changed in design, whereas in the present embodiment, only the first and second board layers 25A, 26A are designed and developed.

[0034] In this manner, with the wiring board for testing 20A according to the present embodiment, because of the configuration in which the first and second board layers 25A, 26A are selectable, when newly designing and developing the wiring board for testing 20A, it is permissible to only design and develop the first and second board layers 25A, 26A, which are non-common wiring board layers, and there is no need to design and develop the power supply board layer 23A and the GND board layer 24A, which are common wiring board layers. Thus, it is possible to reduce design and development costs of the wiring board for testing 20A corresponding to a new IC, and to improve manufacturing efficiency.

[0035] Next, a wiring board for testing that is a second embodiment of the present invention will be described. FIG. 8(A) illustrates a wiring board for testing 20B that is a second embodiment of the present invention. The wiring board for testing 20B according to the present embodiment is characterized by providing a positioning mechanism that positions a plurality of board layers 23B to 26B (wiring board layers) to be laminated.

[0036] The positioning mechanism is configured by a

positioning base 41 and a positioning hole 43 formed in each board layer 23B to 26B. As illustrated in FIG. 8(C), the positioning base 41 is configured by a frame body 44 having an outer shape that is substantially the same as each board layer 23B to 26B and a plurality of a positioning support 42 erected on the frame body 44. Furthermore, the positioning hole 43 is formed in each board layer 23B to 26B respectively, and the forming position thereof is configured to correspond to the forming position of the positioning support 42 erected on the positioning base 41. Furthermore, the forming position of the positioning hole 43 (that is, of the positioning support 42) is selected in a peripheral position of a base material 38B so as not to interfere with pattern formation of each wiring 30 to 33 as illustrated in FIG. 8(B).

[0037] To position each board layer 23B to 26B using the positioning mechanism configured as above, the positioning hole 43 formed in each board layer 23B to 26B is inserted through the positioning support 42 of the positioning base 41. The forming position of the positioning support 42 and the forming position of the positioning hole 43 are highly accurately provided at a prescribed position. Therefore, as described above, each board layer 23B to 26B to be laminated can be positioned by a process of simply inserting the positioning hole 43 through the positioning support 42. Thus, a through-hole 29b formed in each board layer 23B to 26B can be accurately positioned, and the penetrating through-hole 29 can be easily realized.

[0038] Next, a wiring board for testing that is a third embodiment of the present invention will be described. FIG. 9(A) illustrates a second signal board layer 26C provided on the wiring board for testing that is the third embodiment. Note that other than the second signal board layer 26C illustrated in FIG. 9(A), the configuration is the same as the wiring board for testing 20A according to the first embodiment, and therefore, only the second signal board layer 26C is illustrated and described in the description of the present embodiment.

[0039] The present embodiment is characterized by providing lead-out wiring 46 and a pad for testing 47 on the second signal board layer 26C that is positioned on the topmost layer in a laminated state. This lead-out wiring 46 is formed collectively with the second wiring pattern 33 (not illustrated) and is configured to be led out to an outer side of the IC socket 27 in a state in which the IC socket 27 is mounted.

[0040] That is, when the socket outer shape position of the IC socket 27 is illustrated by a dotted line in FIG.

9(A) (in the figure, illustrated by reference numeral 45), the lead-out wiring 46 is led out to an outer side of a socket outer shape position 45, and the pad for testing 47 is formed on an end portion thereof. Thus, by leading out the lead-out wiring 46 to the outer side of the socket outer shape position 45, it is possible to detect a defect of each IC mounted on the IC socket 27. This will be described below.

[0041] Normally, a plurality of the IC socket 27 is mounted on the wiring boards for testing 20A, 20B, and a prescribed test is collectively performed on the ICs mounted on each IC socket 27. In this case, leads 28A, 28B having the same property of each IC socket 27 are connected by the plurality of IC sockets 27 for simplifying a wiring pattern. Furthermore, as illustrated in FIG. 9(B), in the wiring boards for testing 20A, 20B according to the first and second embodiments, the second wiring pattern 33 formed on the second signal board layers 26A, 26B (the second signal board layer 26A is illustrated in the figure) is formed only on an inner side of the socket outer shape position 45, and is not configured to be lead out to the outer side.

[0042] Therefore, when an abnormality occurs in one among the plurality of ICs mounted on the wiring boards for testing 20A, 20B, with the first and second wiring boards for testing 20A, 20B, it can be detected that an abnormality has occurred in any of the mounted plurality of ICs, but an IC in which an abnormality has occurred cannot be specified. In contrast to this, with the wiring board for testing according to the present embodiment, because the lead-out wiring 46 connected to the through-hole portion 29a (through-hole 29) is led out to the outer side of the socket outer shape position 45, and a pad for testing 47 is formed on the end portion thereof, it is possible to test each IC individually by connecting a terminal of an IC tester to this pad for testing 47. Accordingly, it is possible to easily and reliably specify a defective IC in which an abnormality has occurred.

[0043]

[Effect of the Invention] As described above, according to the present invention, various effects described below can be realized. According to the invention of claim 1, because of a configuration in which a non-common wiring board layer can be selected corresponding to a type of an IC socket for a semiconductor device, when designing and developing a wiring board for testing, it is permissible to only design and develop the non-common wiring

board layer, and there is no need to design and develop a common wiring board layer. Thus, it is possible to reduce design and development costs of the wiring board for testing corresponding to a new semiconductor device, and to increase manufacturing efficiency.

[0044] Furthermore, according to the invention of claim 2 and claim 3, each wiring board layer can be easily fixed, and it is possible to replace only a specific wiring board layer. Furthermore, according to the invention of claim 4 and claim 5, a process of laminating each wiring board layer, and in particular, a process of positioning a through-hole, can be easily performed. Moreover, according to the invention of claim 6, it is possible to individually test a semiconductor device mounted in each IC socket, and therefore, a defective semiconductor device can be easily and reliably specified.

[Brief Description of the Drawings]

[FIG. 1] An exploded view for describing one example of a conventional wiring board for testing.

[FIG. 2] A diagram illustrating a state in which an IC socket is mounted on the conventional wiring board for testing.

[FIG. 3] A diagram for describing a method for mounting an IC socket on the conventional wiring board for testing.

[FIG. 4] A perspective view illustrating an automatic inspection device.

[FIG. 5] An exploded view illustrating a wiring board for testing that is a first embodiment of the present invention.

[FIG. 6] A diagram for describing a method for mounting an IC socket on the conventional wiring board for testing that is the first embodiment of the present invention, and a mounted state.

[FIG. 7] A diagram for describing each board layer configuring the wiring board for testing that is the first embodiment of the present invention.

[FIG. 8] A diagram for describing a wiring board for testing that is a second embodiment of the present invention.

[FIG. 9] A diagram for illustrating an enlarged second signal board layer of the wiring board for testing that is the second embodiment of the present invention.

[Description of Reference Numerals]

20A, 20B Wiring board for testing

22A Board material

23A, 23B Power source board layer

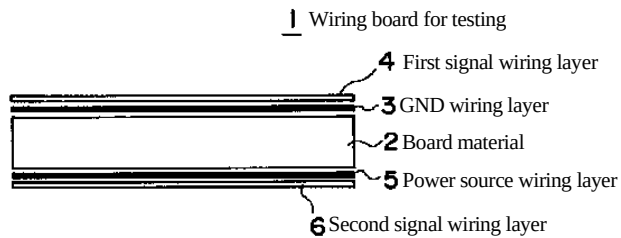
24A, 24B GND board layer

25A, 25B First signal board layer

26A to 26C Second signal board layer
27 IC socket
28 Lead
29 Through-hole
30 Power supply plane wiring
31 GND plane wiring layer
32 First wiring pattern
33 Second wiring pattern
34 to 37 Connecting portion
38A to 38C Base material
39 Non-connecting portion
40 Magnet portion
41 Positioning base
42 Positioning support
43 Positioning hole
45 Socket outer shape position
46 Lead-out wiring
47 Pad for testing

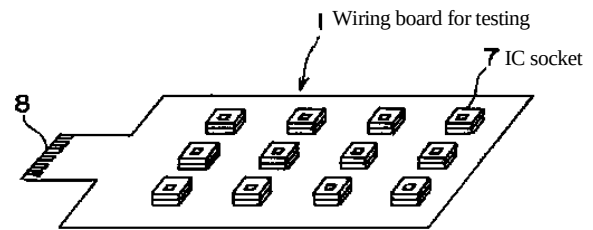
[FIG. 1]

An exploded view for describing one example of a conventional wiring board for testing.



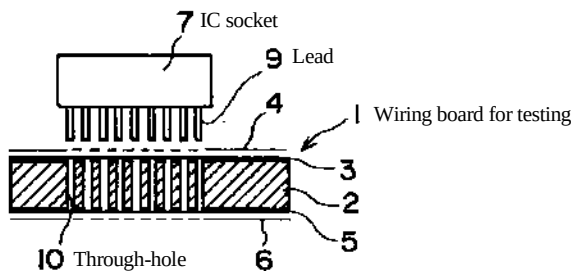
[FIG. 2]

A diagram illustrating a state in which an IC socket is mounted on the conventional wiring board for testing.



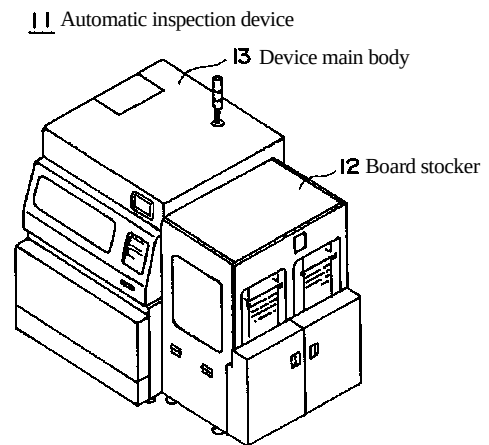
[FIG. 3]

A diagram for describing a method for mounting an IC socket on the conventional wiring board for testing.



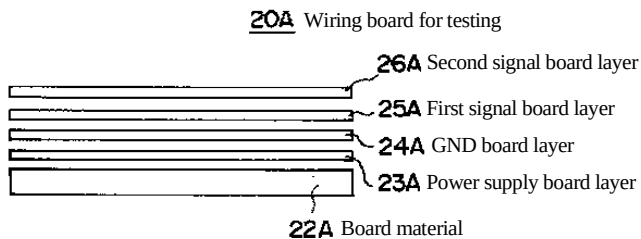
[FIG. 4]

A perspective view illustrating an automatic inspection device.



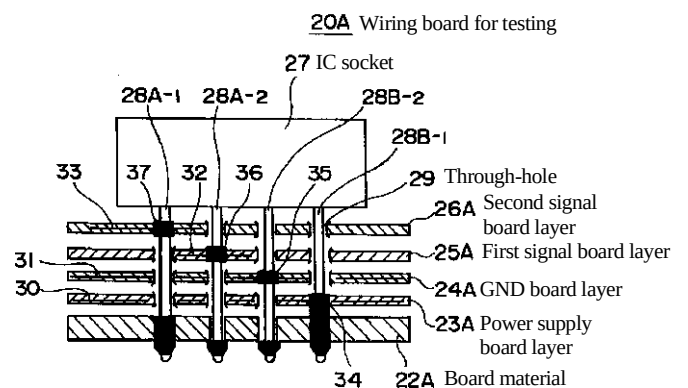
[FIG. 5]

An exploded view illustrating a wiring board for testing that is a first embodiment of the present invention.



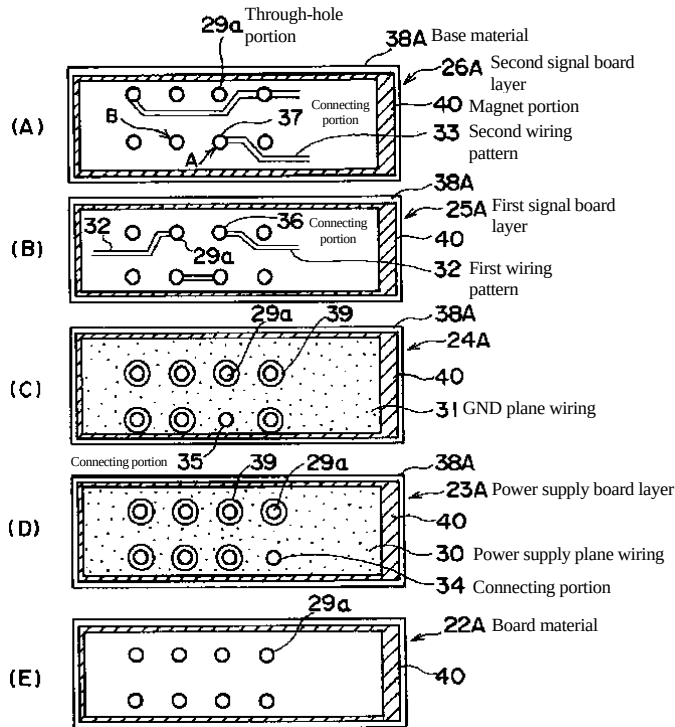
[FIG. 6]

A diagram for describing a method for mounting an IC socket on the wiring board for testing that is the first embodiment of the present invention, and a mounted state.



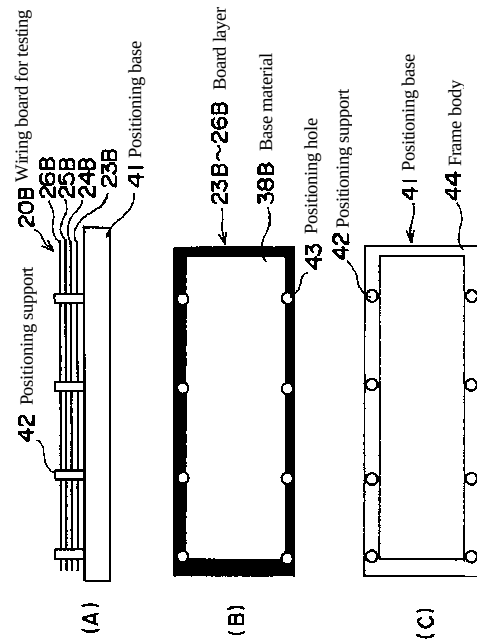
[FIG. 7]

A diagram for describing each board layer configuring the wiring board for testing that is the first embodiment of the present invention.



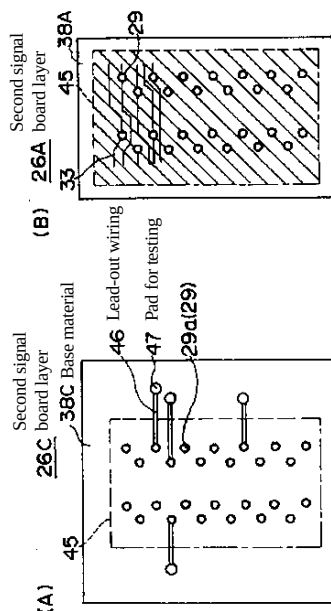
[FIG. 8]

A diagram for describing a wiring board for testing that is a second embodiment of the present invention.



[FIG. 9]

A diagram for illustrating an enlarged second signal board layer of the wiring board for testing that is the second



STATE of NEW YORK)
)
COUNTY of NEW YORK) SS:

CERTIFICATE OF ACCURACY

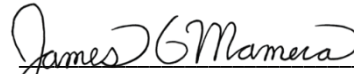
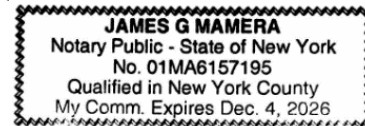
This is to certify that the attached document, "JP1999-352182 (Grouping signal pins)" -
- originally written in Japanese is to the best of our knowledge and belief, a true,
accurate, and complete translation into English.

Dated: 3/13/2024



Heather Cameron
Project Manager
Consortra Translations

Sworn to and signed before ME
This 13th day of March, 2024


Notary Public

Your
legal
translation
partner