

Frederick Taber
Test Technology Consultant
34 Kuchler Drive
LaGrangeville, N.Y. 12540
845-226-7560
taberconsulting@optonline.net

May 28, 2024

Curriculum Vitae – Frederick L. Taber

Education

BSEE, Southeastern Massachusetts University (University of Massachusetts, Dartmouth); 1970

IBM Manufacturing Technology Institute; 1982

Extensive IBM internal technical and management courses and training

Career - Employment

IBM Corporation, Test Engineering; 1970 - 2004

Engineer / Lead Engineer, Sub-product Test Systems Design & Development (for circuit cards); IBM Large Systems Division; 1970 – 1980

Project Engineering Manager, Sub-product Test Systems Design & Development; IBM Large Systems Division (for circuit cards and multi-chip modules); 1980 - 1989

Project Engineering Manager, Wafer Test Systems Design & Development; IBM Microelectronics Division; 1989 - 1992

Senior Engineering Manager for Contacting Systems Development (Wafer Probes and Sockets for Test & Burn-in), IBM Microelectronics; 1992 to 2004

Founder and General Chairman, Burn-in and Test Socket Workshop (BiTS); renamed Burn-in & Test Strategies Workshop in 2011; 2000 – 2014; Chairman Emeritus: 2015-present

Majority owner/partner of BiTS Workshop, LLC; 2003 - 2014

Test Technology Consultant; 2004 – Present

Broad spectrum of projects associated with Wafer Probes and Test & Burn-in Sockets

Career – Industry Engagement

Member of the Technical Meetings Review Committee (IEEE Computer Society's Test Technology Technical Council); 2001 - 2003

Chairman, International SEMATECH's Wafer Probe Council; 2000 – 2004

IBM Microelectronics representative to the Wafer Probe Council

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Program Committee – IEEE Southwest Test Workshop (SWTW); renamed IEEE Semiconductor Wafer Test Workshop in 2008); 2000 – 2017; Committee Emeritus: 2017 – present

Proceedings Coordinator: 2007 – 2014; Tutorials Manual Coordinator: 2015

Board of Advisors for Chip Scale Review magazine; 2004 – 2006

Editorial Advisor for Chip Scale Review magazine; 2011 – 2014

Editorial Board for Advanced Packaging magazine; 2006 – 2009

Member of the Institute of Electrical and Electronics Engineers; 1999 – Present

Golden Core Member – awarded 2003

Life Membership – awarded January, 2024

Member of Computer Society; Test Technology Technical Council

Patents

“Large Area Multiple-Chip Probe Assembly And Method Of Making The Same”; #5,977,787

“Wafer Probe Interface Arrangement With Nonresilient Probe Elements And Support Structure”; # 6,426,636

Patent Application for “System And Method For Assembling A Probe Head”; Application # 13973748

Papers / Articles

“An Introduction To Area Array Probing”; IEEE Southwest Test Workshop – 1998

“An Introduction To Area Array Probing”; International Test Conference – 1998

“The Leading Edge Of Production Wafer Probe Test Technology”; International Test Conference – 2004

Invited Presentation – “International SEMATECH: Wafer Probe Benchmarking Project”; IEEE Southwest Test Workshop – 2001

“A High Performance C4 Probe: TFI™”; IEEE Southwest Test Workshop – 2001; Winner: Most Inspirational Presentation

“Wafer Probe Roadmap – Guidance For Wafer Probe R&D Resources – 2002 Edition”; IEEE Southwest Test Workshop – 2002

“International SEMATECH Wafer Probe Council – Vertical Probing Experiences”; IEEE Southwest Test Workshop – 2003

“Probe Card Tracking Operations Within SEMATECH Probe Council Member Companies”; IEEE Southwest Test Workshop – 2004

“Maximizing The Performance Of An Atypical Cantilever Probe Wire Material”; IEEE Semiconductor Wafer Test Workshop – 2006

“Socket Marketplace Report”; Burn-in & Test Sockets Workshop – 2011

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“Socket Marketplace Report”; Burn-in & Test Sockets Workshop – 2012

“Socket Marketplace Report”; Burn-in & Test Sockets Workshop – 2013

“Socket Marketplace Report”; Burn-in & Test Sockets Workshop – 2014

“Doesn’t Happen Often”; Socket Trends editorial; Advanced Packaging magazine; April 2007

“Snowstorms and Sockets”; Socket Trends editorial; Advanced Packaging magazine; March 2008

“Parallel Universes Draw Closer”; Socket Trends editorial; Advanced Packaging magazine; January/February 2009 (deferred to Solid State Technology magazine May 2009).

“Keeping Pace With the Packaging Evolution”; Market Update editorial; Chip Scale Review magazine, July/August 2014

Industry Reference Material (with SEMATECH Probe Council)

International Technology Roadmap for Semiconductors; Wafer Probe Section; 2001 through 2003 updates

Expert Witness

United States International Trade Commission; In the Matter of: “Certain Probe Card Assemblies, Components Thereof and Certain Tested DRAM And NAND Flash Memory Devices And Products Containing Same”; Phicom & Micronics Japan v. Formfactor; 2007 – 2009; includes tutorial to the court and testimony at trial.

United States District Court, District of Arizona; Integrated Technology Corporation and Nevada Integrated Technology Corporation v. Rudolph Technologies, Inc., et al; 2011; includes testimony at trial.

United States District Court, Northern District of California, Oakland Division; Formfactor, Inc. v. Microprobe; 2011; case settled.

United States District Court, Northern District of California; Interconnect Devices, Inc. v. Johnstech International, 2014-2015; case settled.

United States Patent and Trademark Office – Patent Trial and Appeal Board (PTAB); Formfactor, Inc. (Petitioner) v. Feinmetall, GmbH (Patent Owner); Inter Partes Review; 2018-2019; Termination Decision - Due to Settlement After Institution of Trial (post trial settlement w/o written decision).