



SW Test Workshop
Semiconductor Wafer Test Workshop

A proposal of a new probe head design in vertical probe cards for low crosstalk and PDN impedance



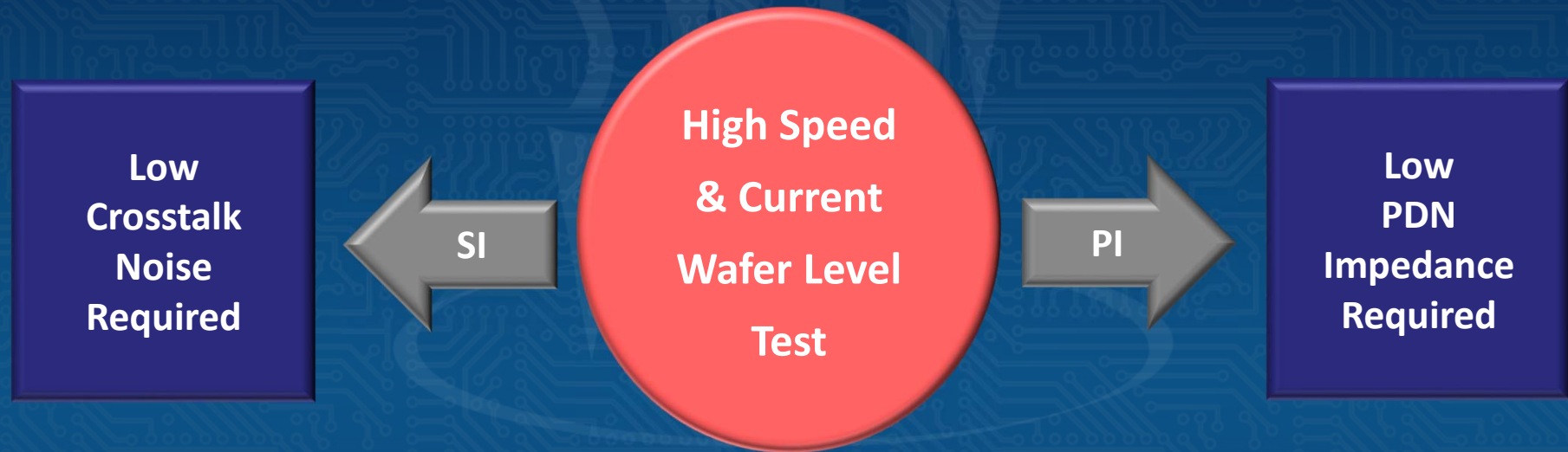
Kyung Hyun Chang
Hyun Min Kim
Willtechnology

June 5-8, 2016

Overview

- **Background**
- **Low Crosstalk Probe Head**
 - Proposed structure of needle for crosstalk reduction
 - Simulation & Measurement result
- **Low – Z Probe Head**
 - Proposed structure of needle for PDN Impedance reduction
 - Simulation & Measurement result
- **Conclusion & Future work**

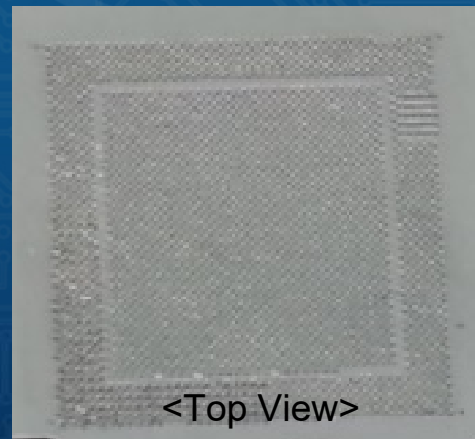
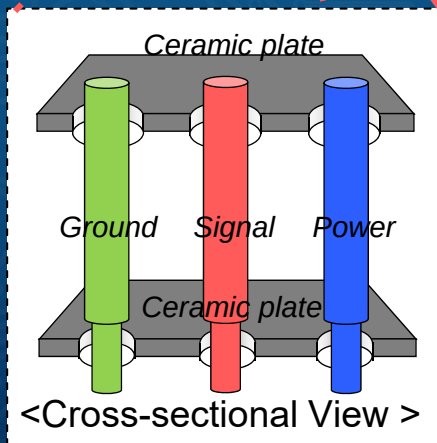
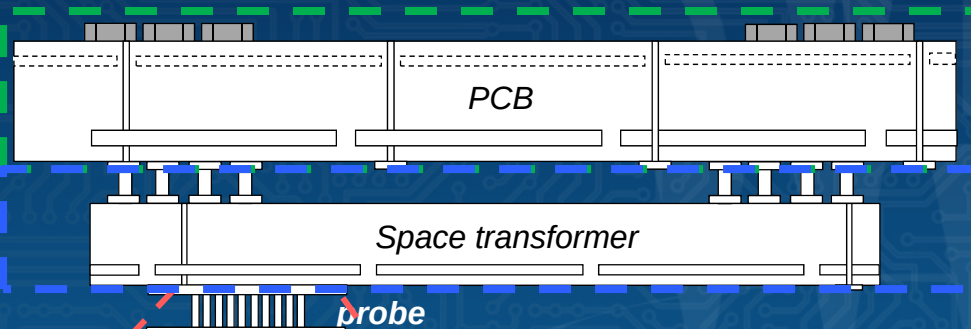
Background



- SI & PI should carefully be considered in high speed / current wafer test.
- Both low crosstalk and PDN impedance are highly desirable for improvements in SI / PI.

Background

- Vertical Probe Card Structure



< Current Probe Head Structure >

SI/PI
Improvement

PCB

- Usage of Low Permittivity Materials (ex. FR4 → Nelco)
- Back drill

STF

- Usage of High Conductivity and Low Permittivity Materials (ex. MLC → MLO)

Probe Head

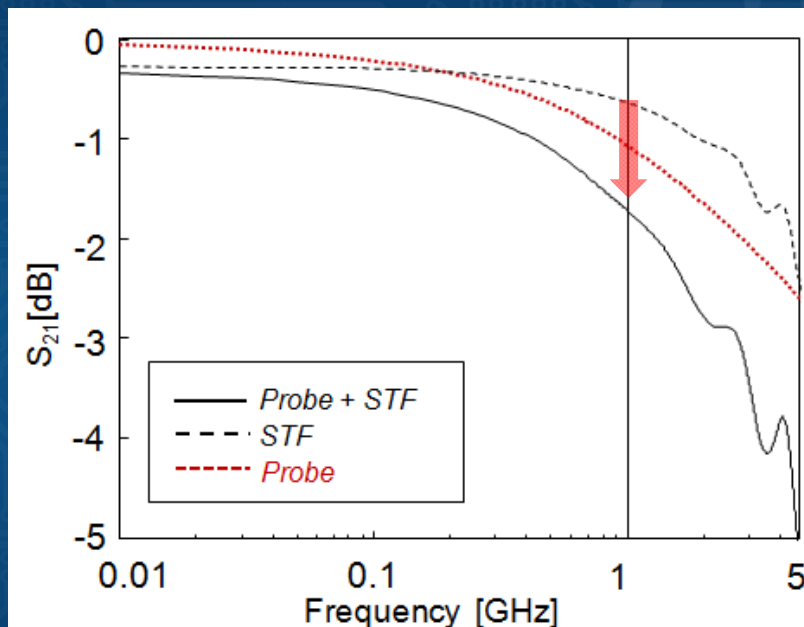
- Difficulties in SI/PI improvement in its current structure

How does a probe head affect SI / PI ?

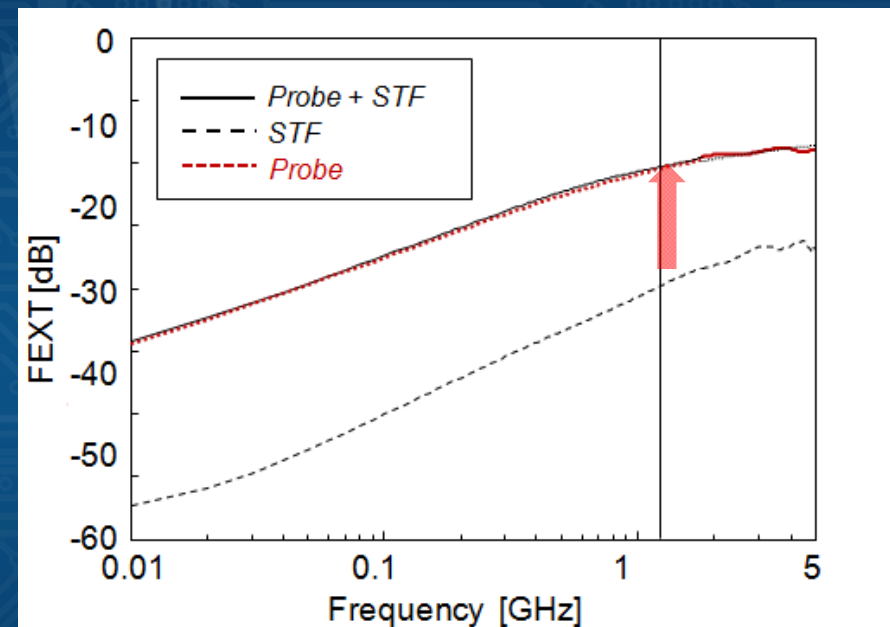
Background

- Degradation of SI due to Probe Head

[Attenuation of probe card]



[Far-end crosstalk of probe card]



- The probe brings about the dominant loss and the far-end crosstalk of the test signals.
- It is necessary to reduce the frequency dependent loss and far-end crosstalk of a probe in test channel of vertical probe card.

Background

- Degradation of PI due to Probe Head

[Z11 of probe card]

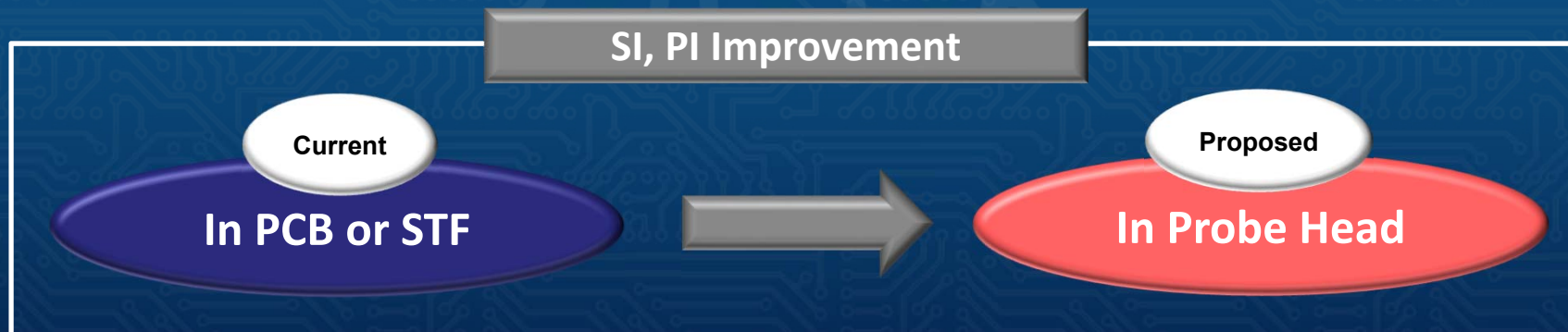
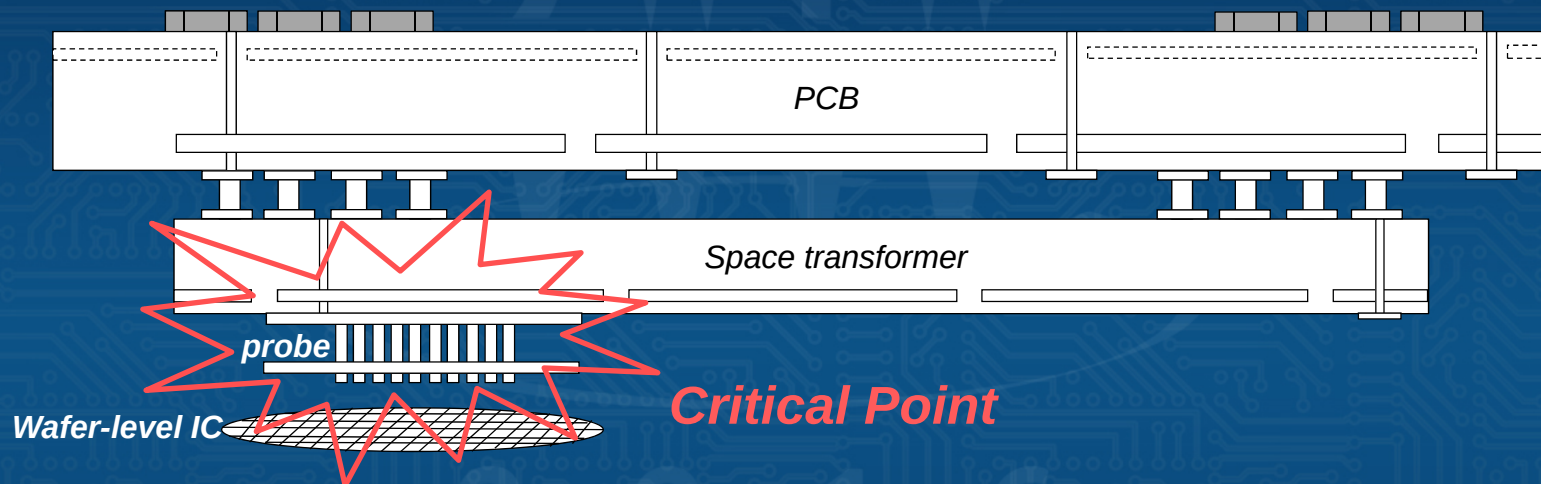


- Increased in inductance by 4nH due to the effect of probe head
- Degradation of PDN impedance from the increased probe inductance

Background

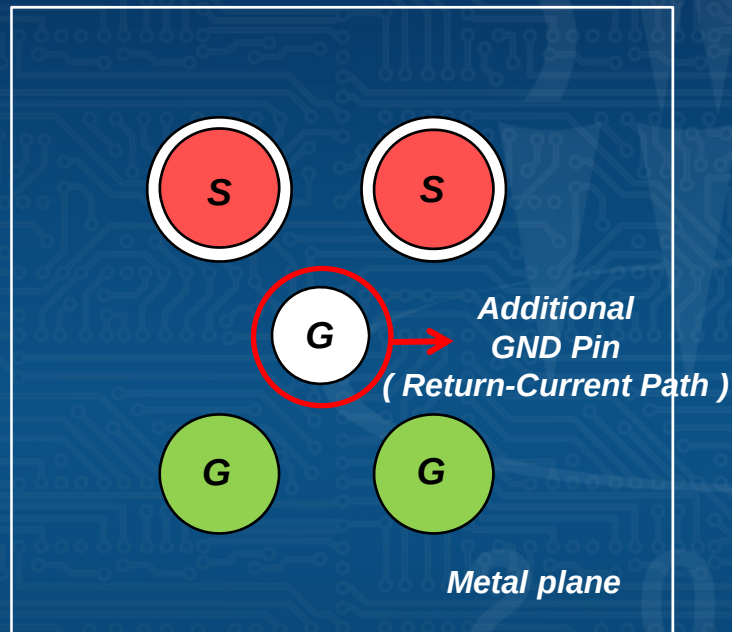
- Room for improvement

< Schematic diagram of the vertical probe cards >

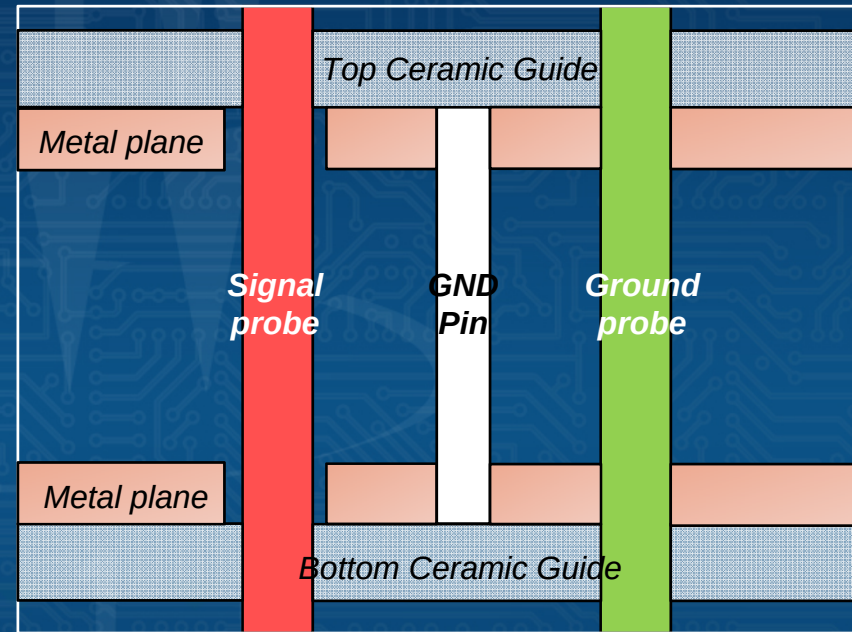


Low X-talk Probe Head

- Proposed structure of probe head for crosstalk reduction



<Top View>



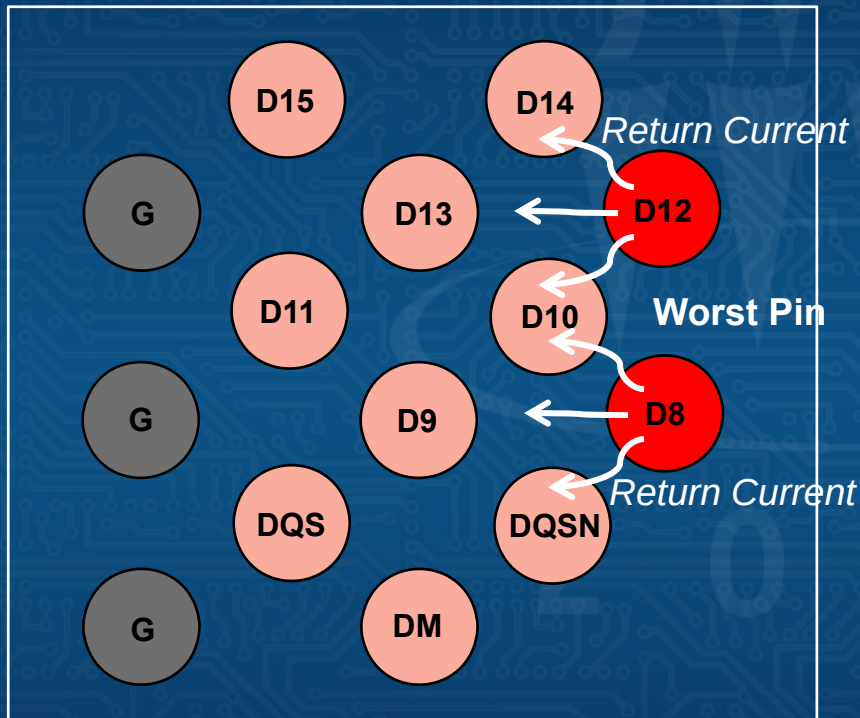
<Cross-sectional View>

- Insertion of metal planes and ground pins for the proposed design
- The ground pins provide return-current paths for signal probes.

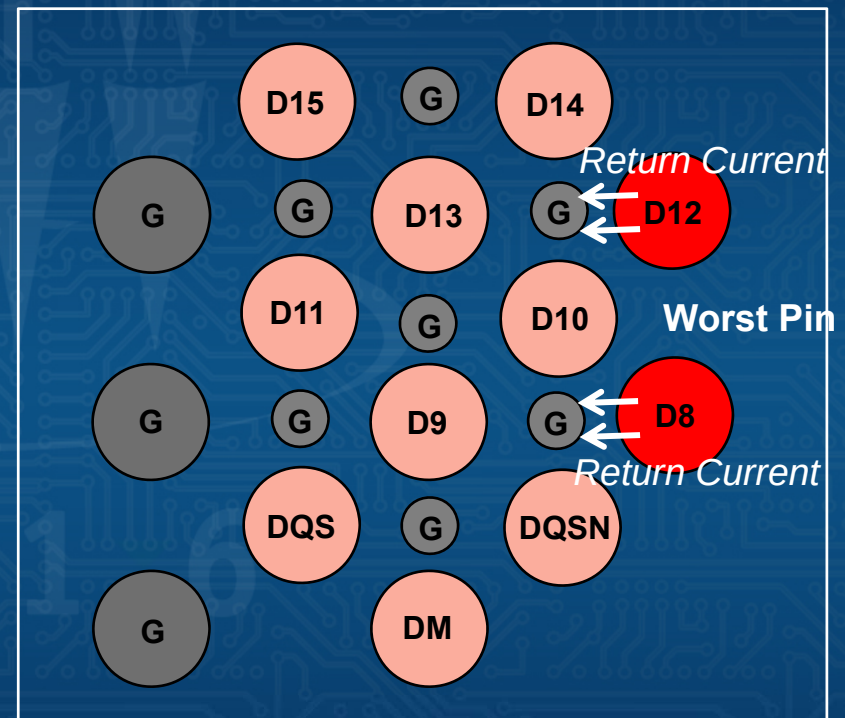
Low X-talk Probe Head

- Proposed structure of probe head for crosstalk reduction

[Pin assignment of AP on wafer]



[Proposed insertion of additional pin on PH]

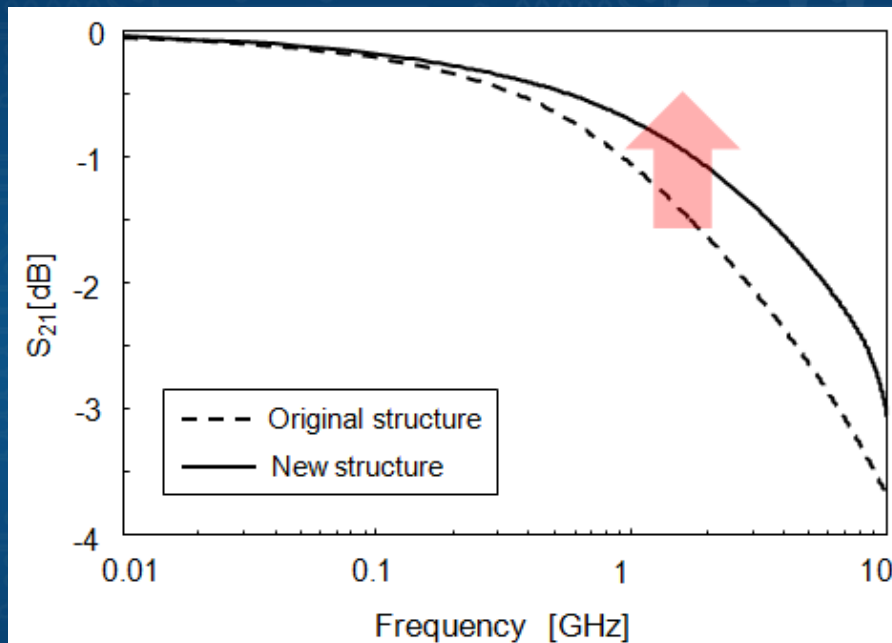


- Signal probes that are far from GND may influence the signal integrity of the others.
- The inserted GND guard pin acts as return-current paths for signal pins
→ Suppressed noise coupling among the signal probes

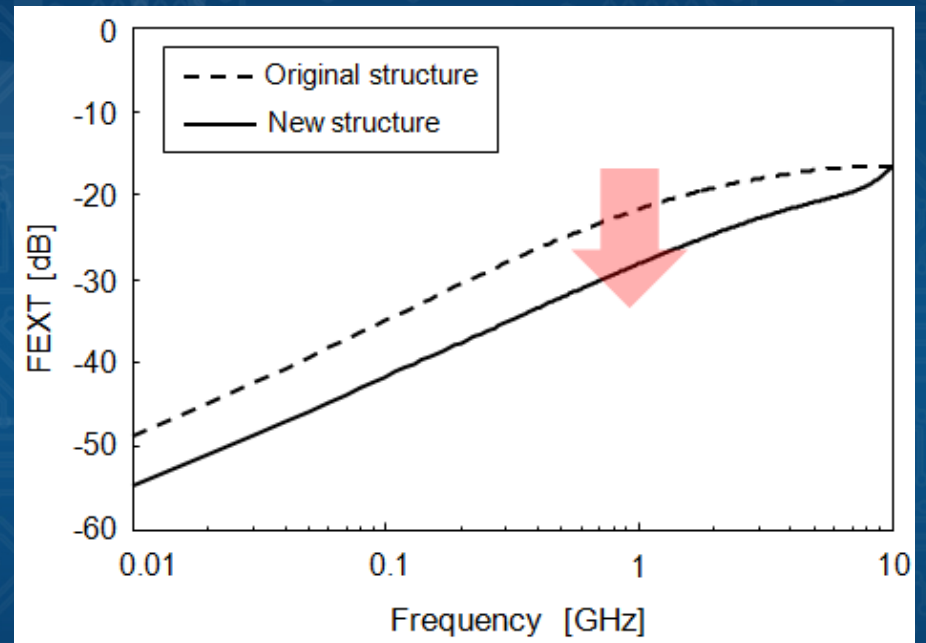
Low X-talk Probe Head

- Comparison Far-end crosstalk (SI Simulation Result)

[Attenuation of probe card]



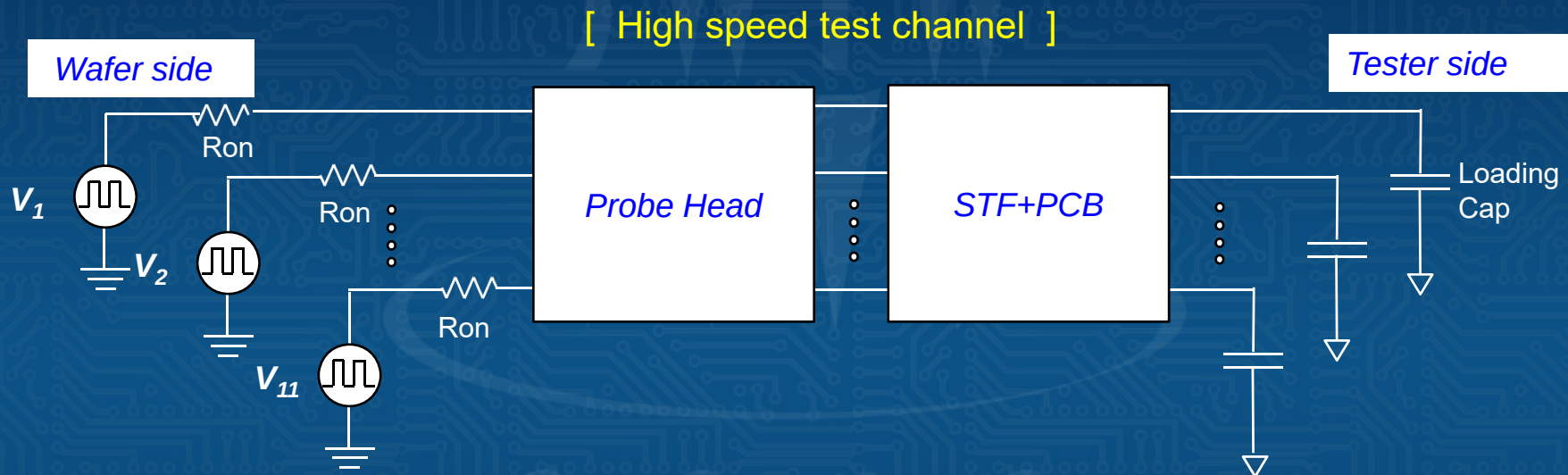
[Far-end crosstalk of probe card]



- Reduced Insertion loss (S₂₁)
- Reduced Far-end crosstalk (FEXT)

Low X-talk Probe Head

- Eye-Diagram Simulation Environment



- Simulation Setup

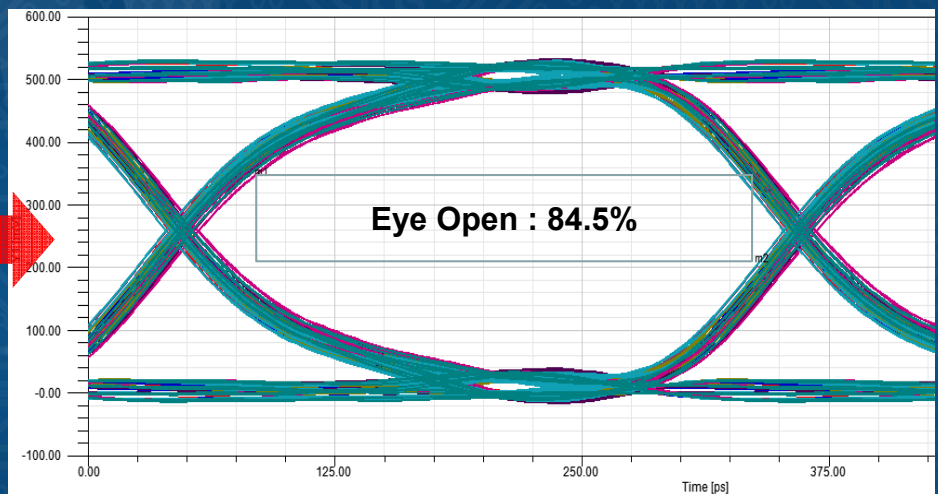
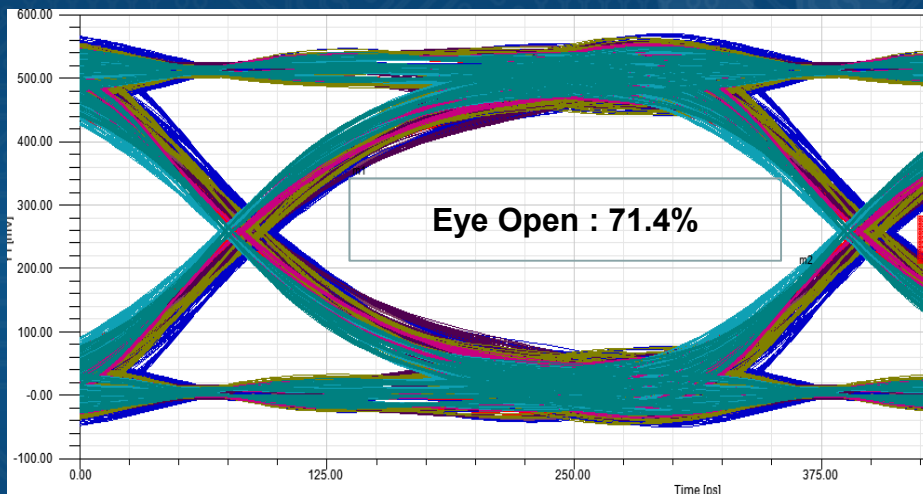
- Input Voltage : 1.1 V
- Data rate : 3200 Mbps
- Rise / Fall Time : $UI/4$

- Turn-on resistance : 50 ohm
- Data pattern : PRBS 2^5
- Loading Capacitance : 2pF

Low X-talk Probe Head

- Comparison Eye Diagram (Eye Simulation Result)

< Eye Diagram of probe card – Data rate : 3.2Gbps >

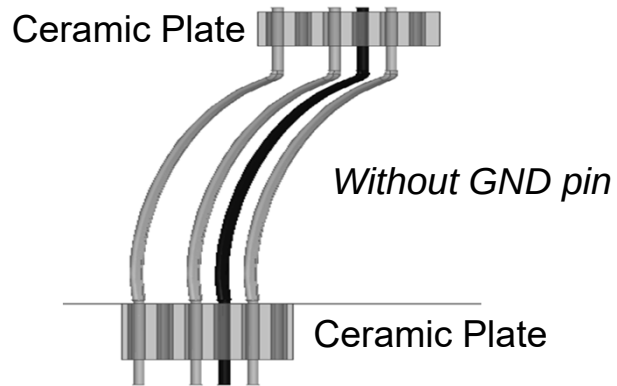


- Larger eye open as a result of reduced crosstalk noise
- The simulation results show that the improvement in SI has been achieved.

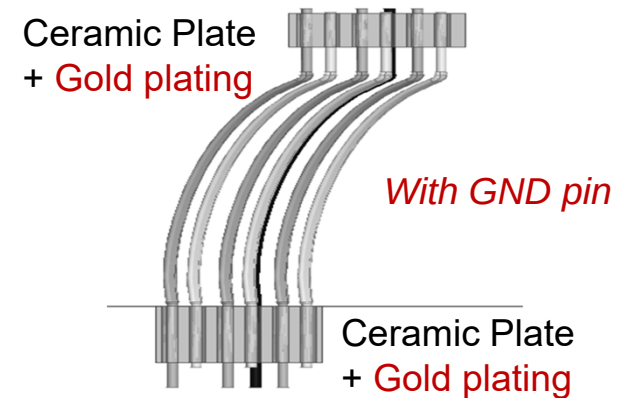
Low X-talk Probe Head

- Probe Head Eye Diagram Measurement Environment

< Original Probe Head >



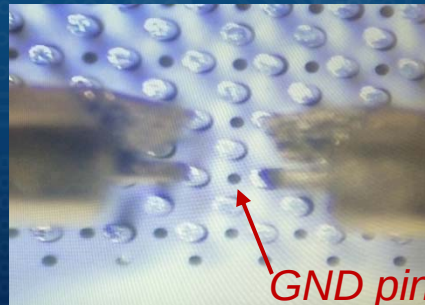
< Low X-talk Probe Head >



< Original PH >



< Low X-talk PH >



Eye-diagram measurement with Crosstalk effects

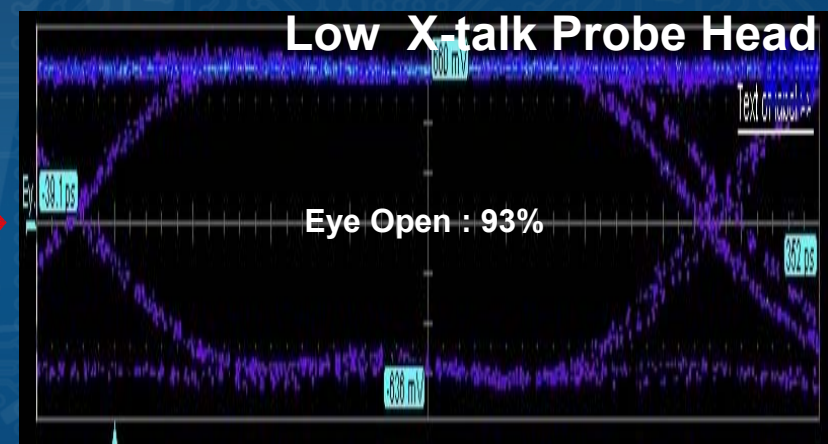
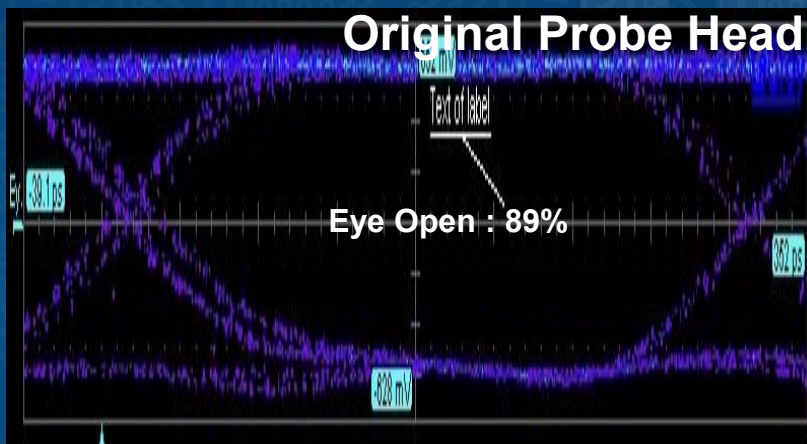
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Low X-talk Probe Head

- Comparison Eye Diagram (Eye Measurement Result)

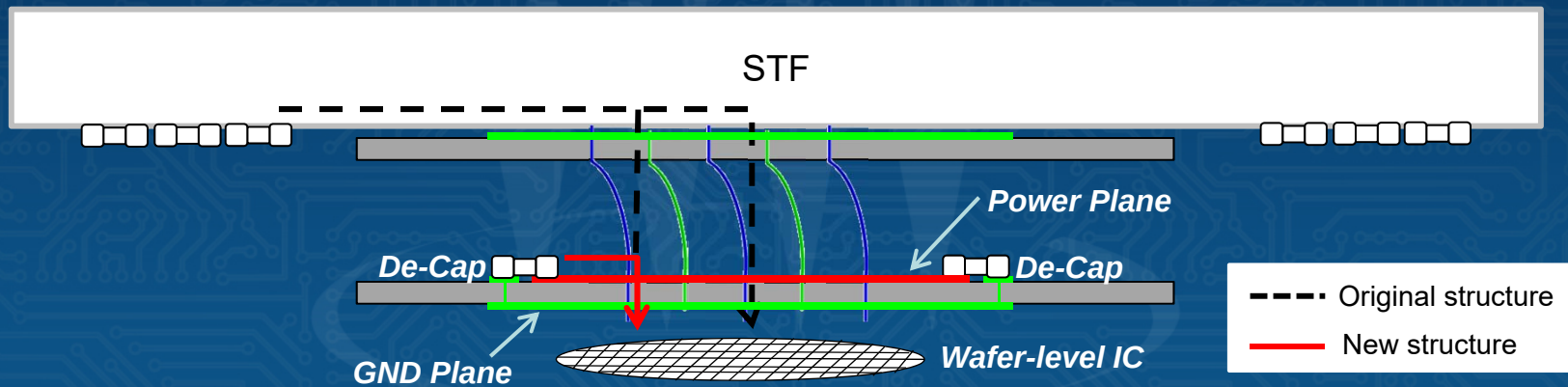
< Eye Diagram of Probe Head – Data rate : 3.2Gbps >



- In measurement, a minor improvement can be seen as compared to the simulation.
- Due to the restrictions, the probes near the GND pins (e.g. D11) can only be measured, which leads to the results only with the partial influence of x-talk.

Low-Z Probe Head

- Proposed structure of PDN Impedance reduction



▪ Power, GND Plane and De-Cap added to Probe Head

PI Improvement

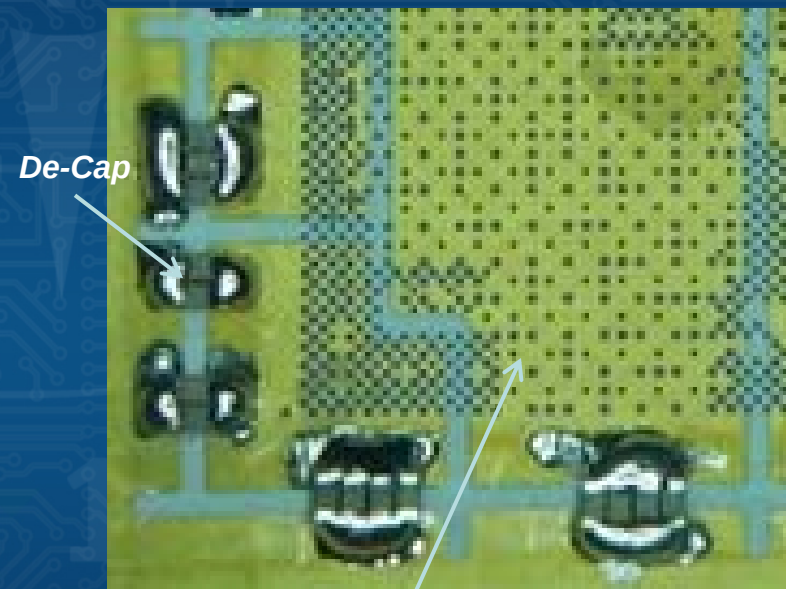
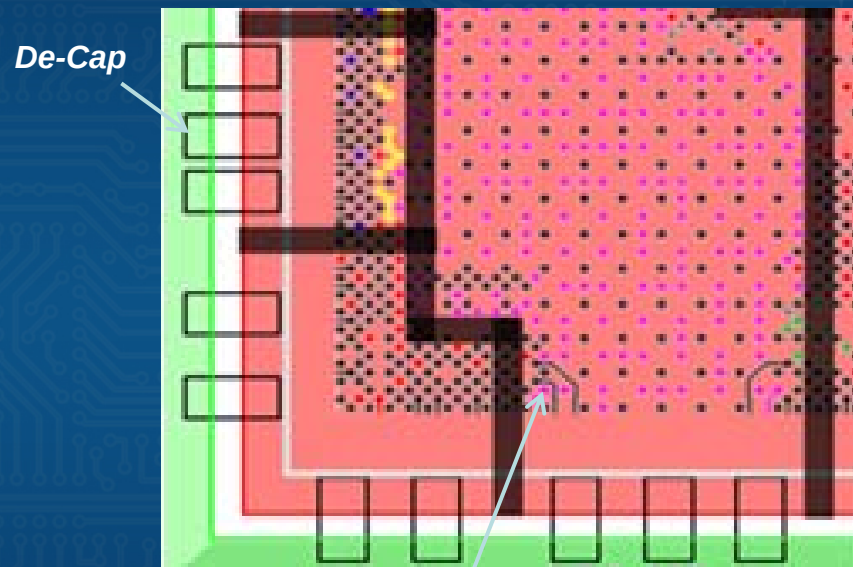
▪ Mitigation effect for increased PDN impedance due to addition of PH

Low-Z Probe Head

- Proposed structure of PDN Impedance reduction

[Low -Z Probe Head Concept]

[Low -Z Probe Head in practice]



- Implementation of Power / GND planes through gold plating
- Capability of applying low-z concept to various powers through splitting the planes

Author

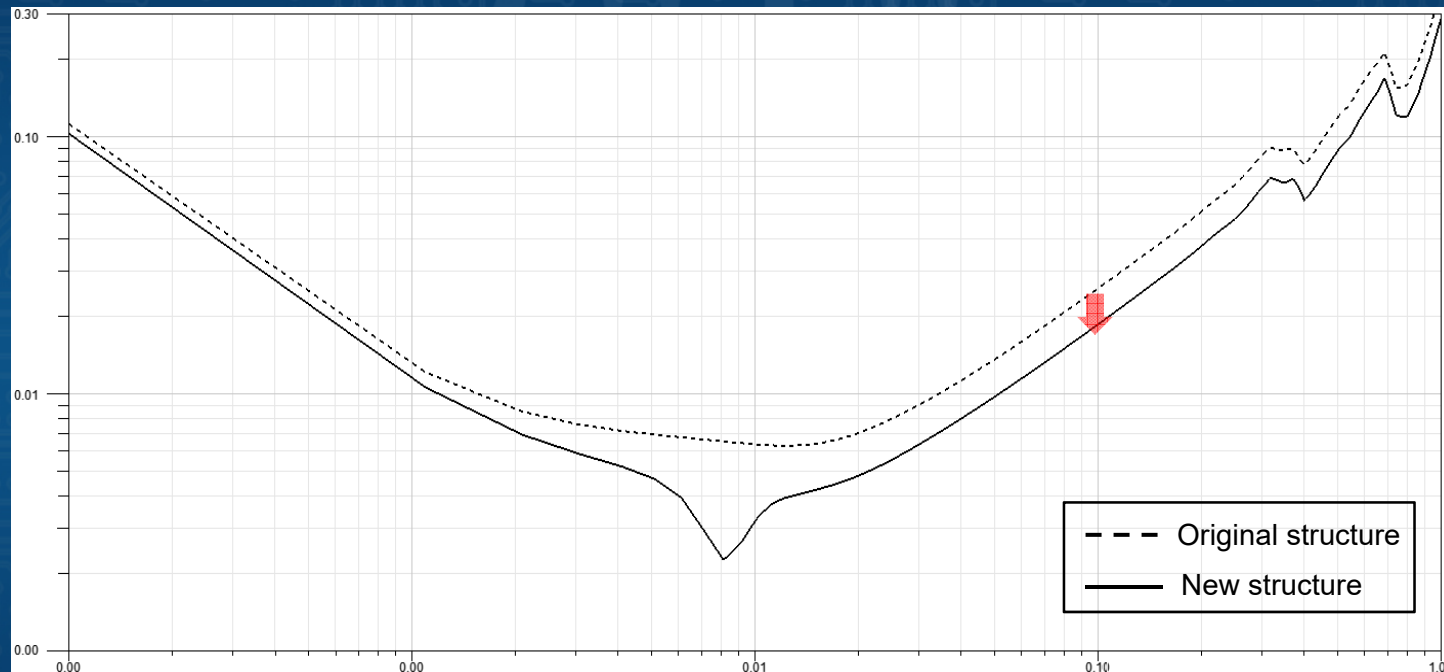
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Low-Z Probe Head

- **Comparison PDN Impedance (PI Simulation Result)**

< Z11 Graph of probe card _Lumped Port PI Simulation >

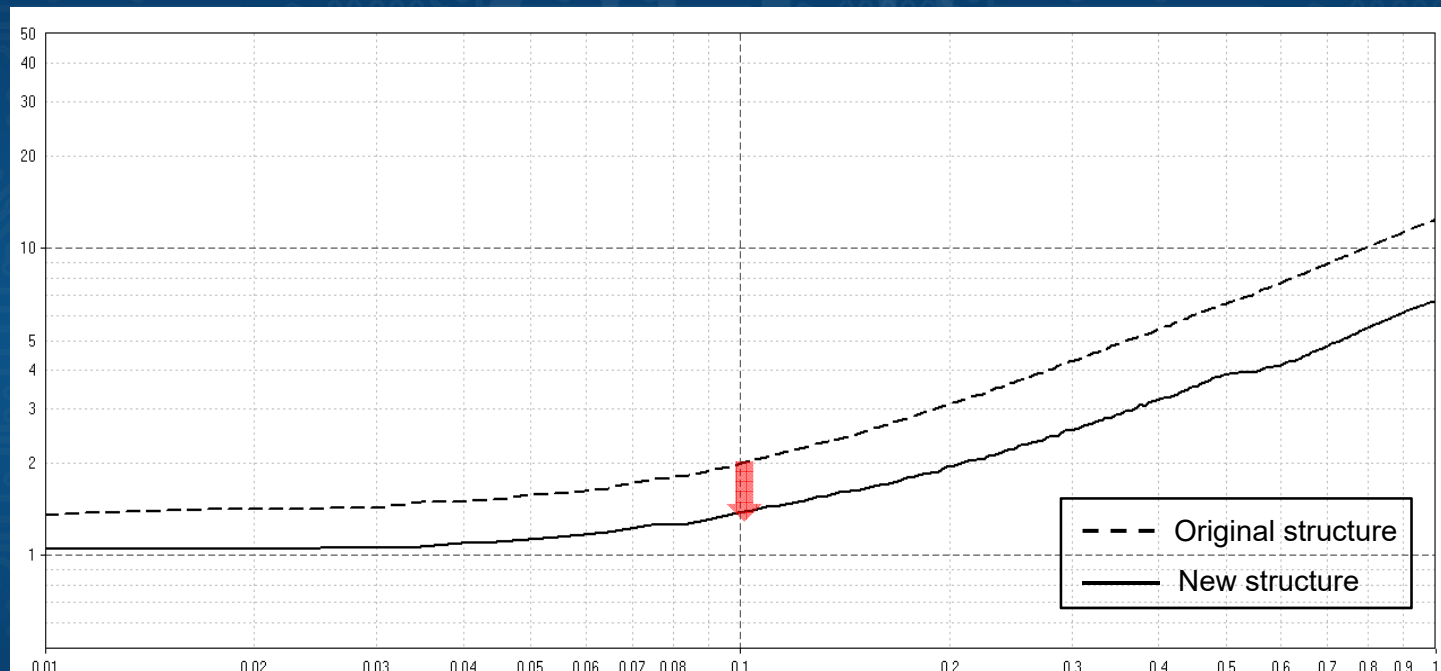


- Result of lumped port PI simulation
- Decrease in PDN Impedance (Z11) of Low-Z structure as compared to original (25% ↓)

Low-Z Probe Head

- Comparison PDN Impedance (PI Measurement Result)

< Z11 Graph of probe card _1pin PI measurement >



- Result of 1-pin PI measurement
- Decrease in PDN Impedance (Z11) of Low-Z structure as compared to original (30% ↓)
- According to the results, decrease in PDN impedance has been observed.

Conclusion & Future work

- SI & PI should carefully be considered in high speed / current wafer level test.
- A new structure with low Z & X-talk is required to compensate the SI & PI loss caused by the probe head
- SI ; Low x-talk among signal probes has been achieved through the new structure with additional GND pins
- PI ; Introducing P/G planes and decaps on probe head leads to lower power impedance
- Further research required to employ such strategy & concept for fine pitch products
- Thanks.