

SWTW

2016

SW Test Workshop

Semiconductor Wafer Test Workshop

Tuesday, June 7, 2016

PROCEEDINGS

June 5-8, 2016
Rancho Bernardo Inn, San Diego, CA

www.swtest.org

FormFactor v. Technoprobe
IPR2024-00933

Chairman's Welcome to SW Test Workshop

Wafer Test Technology

On behalf of the SW Test Executive Team, Program Committee, and Committee Members, it is my great pleasure to welcome you to San Diego and the 26th Annual SW Test Workshop held at the Rancho Bernardo Inn. This is the premier international workshop that focuses on all the aspects of microelectronic wafer and die level testing. Over the past 26-years, we have had over 8000 workshop attendees, many generous corporate sponsors, and more than 500 exhibitors in attendance.

For SW Test 2016, the SW Test Program Committee had a very difficult task of selecting 28 submissions for podium presentation during 9-technical sessions. Attendees will find a diverse technical program that covers many of real-world challenges. We have chosen excellent work from suppliers and end-users with innovative approaches for solving probe challenges associated with the next generation devices and process. Industry leaders in manufacturing detail improved fabrication processes and materials development that facilitate stable testing under the most demanding thermal, electrical, and environmental conditions. Key improvements for test equipment and metrology tools that create enhanced infrastructure to reduce overall cost of test are discussed throughout the program.

To provide attendees with access to key technologies and services, the SW Test EXPO is held in conjunction (but not competing) with the workshop, the top probe card, probe equipment, and related service suppliers showcase the latest products and services. This year, the limited number of exhibits sold-out before the end of April and there is already a waiting list for SW Test EXPO 2017.

From the 2015 Technical Program, the excellent work of Krzysztof Dabrowiecki and Jorg Behr from Feinmetall entitled "*Experience in Applying Finite Element Analysis for Advanced Probe Card Design and Study*" was published in the April 2016 issue of Evaluation Engineering. The presentation made by Rachel Koski and Daniel Frequez of Texas Instruments entitled "*Probe Route Optimization and its Effects on the Efficiency of Test*" has been nominated for the Best ATE Publication of the Year and the award will be presented at Test Vision 2020, held in conjunction with Semicon West July 13/14 in San Francisco, CA.

Additionally, the SW Test Executive Team has worked in collaboration with SEMI.org to gain further recognition for our workshop via the SEMI.org social network that touches over 10,000 professionals. SEMI works with various technical committees, partner organizations, and technologists, to develop programs that cover the latest technology challenges and key solutions in semiconductor manufacturing and testing. For the TechXPOT 2016 at Semicon West, the SW Test Team worked in conjunction with SEMI for their Test Forum track that will feature two "*Best Of ...*" presentations from the 2016 SW Test Technical Program.

I would like to take this opportunity to thank all our sponsors, exhibitors, authors, speakers, session chairs, program committee members, as well as all the volunteers who help make the SW Test Workshop a success. I look forward to another successful Workshop and building some lifelong contacts through a relaxed and friendly atmosphere.

Once again, thank you for being a part of the 26th SW Test.



Jerry Broz, Ph.D.
General Chair
SW Test Workshop

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TECHNICAL PROGRAM AND AGENDA

"AT A GLANCE"

June 5 to 8, 2016

Sunday, June 5

8 a.m. – 12 Noonish	5th Annual SW Test William Mann Golf Tournament
2:00 PM - 4:00 PM	Tutorials – Probe Pad Damage & Early Wear Out (Santiago Ballroom)
4:00 PM - 6:00 PM	REGISTRATION (Aragon South Foyer)
6:00 PM - 7:00 PM	RECEPTION (Aragon Lawn)
7:00 PM - 8:15 PM	Dinner in the Aragon II/III Ballroom
8:15 PM - 8:30 PM	Welcome SW Test 2016
8:30 PM - 9:45 PM	Keynote Presentation by Friedrich Taenzler, Ph.D., RF-Engineering Manager at Texas Instruments, Inc.

Monday, June 6

7:00 AM - 5:00 PM	REGISTRATION / EXHIBITOR CHECK IN (Aragon South Foyer)
7:00 AM - 8:00 AM	CONTINENTAL BREAKFAST (Aragon Lawn)
8:00 AM - 10:00 AM	Test Strategy Innovations (Aragon I/II)
10:00 AM - 10:30 AM	BREAK (Aragon Lawn)
10:30 AM - 12:00 PM	Drilling
12:00 PM - 1:00 PM	LUNCH (Aragon Lawn)
1:00 PM - 3:00 PM	New Test Challenges and Solutions
3:00 PM - 3:30 PM	BREAK (Aragon Lawn)
3:30 PM - 5:00 PM	Bumps and Arrays
5:00 PM - 8:00 PM	EXHIBITS OPEN w/ Dinner Served at RECEPTION STATIONS

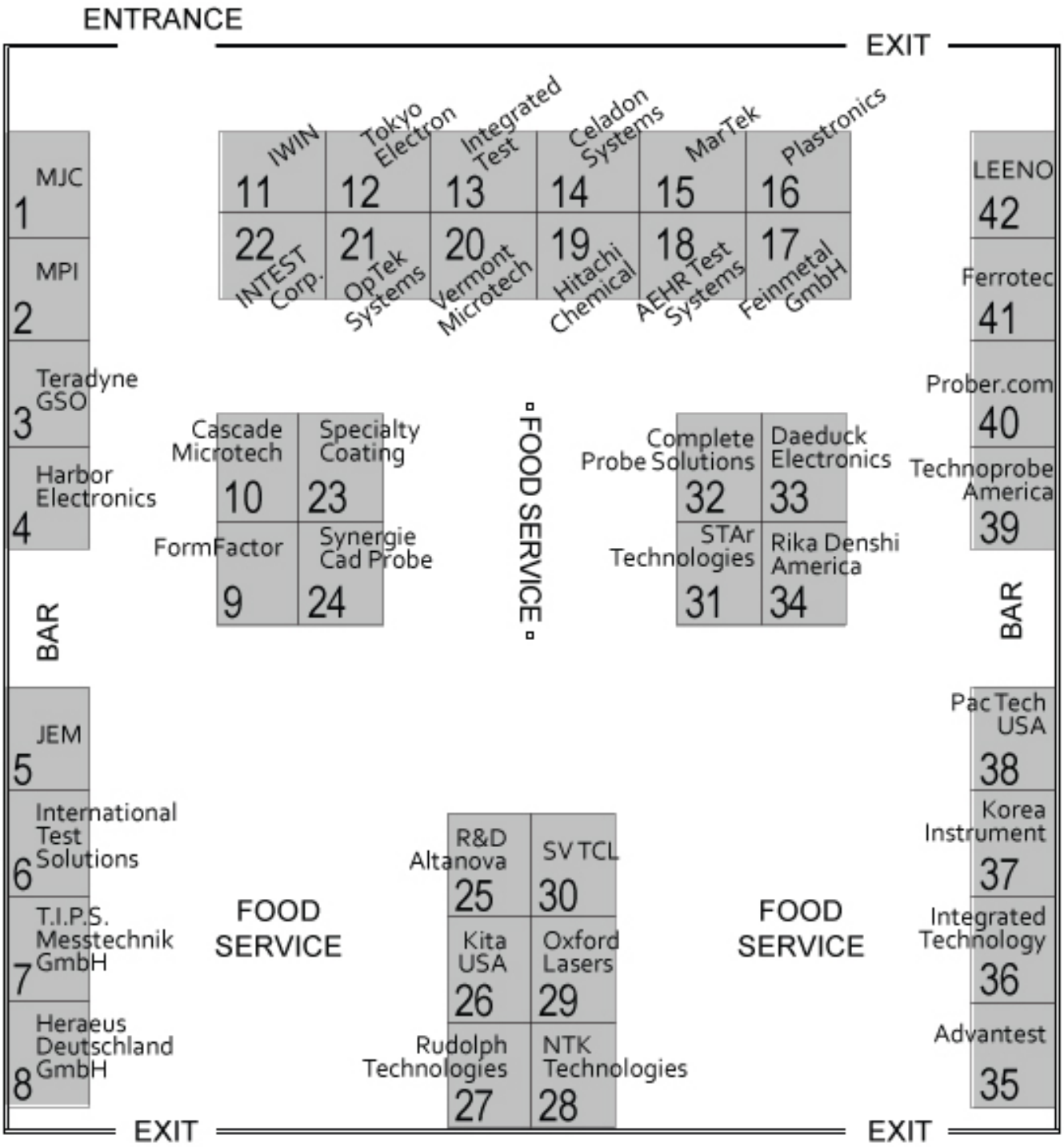
Tuesday, June 7

7:00 AM - 3:00 PM	REGISTRATION (Aragon South Foyer)
7:00 AM - 8:00 AM	CONTINENTAL BREAKFAST (Aragon Lawn)
8:00 AM - 10:00 AM	Moving Forward with Space Transformer Technology (Aragon I/II)
10:00 AM - 10:30 AM	BREAK (Aragon Lawn)
10:30 AM - 12:00 PM	Power Probing at Temperature (Aragon I/II)
12:00 PM - 1:00 PM	LUNCH (Aragon Lawn)
1:30 PM - 3:00 PM	Here is Something Different ...
3:00 PM - 5:00 PM	EXHIBITS OPEN (Refreshments will be served)
6:00 PM - 9:00 PM	WORKSHOP SOCIAL – "Luck be Lady Tonight" Casino Night and Social Event

Wednesday, June 9

7:30 AM - 10:00 AM	REGISTRATION (Aragon South Foyer)
7:00 AM - 8:00 AM	CONTINENTAL BREAKFAST (Aragon Lawn)
8:00 AM - 10:00 AM	Vertical, CU Pillar and ILD Cracking during Probe (Aragon I/II)
10:00 AM - 10:30 AM	BREAK (Aragon Lawn)
10:30 AM - 11:30 PM	Process Improvement (Aragon I/II)
11:30 AM to 12:00 PM	AWARDS and ADJOURNMENT (Aragon I/II)
12:00 PM to 1:00 PM	BOX LUNCH (Aragon Lawn)

SW Test 2016 EXPO Exhibitor Map



SW Test 2016 Exhibitor List

Company	Booth
Advantest	35
AEHR Test Systems	18
Cascade Microtech, Inc.	10
Celadon Systems	14
Complete Probe Solutions, Inc.	32
Daeduck Electronics Co., LTD.	33
Feinmetal GmbH	17
Ferrotec (USA) Corp.	41
FormFactor, Inc.	9
Harbor Electronics, Inc.	4
Heraeus Deutschland GmbH	8
Hitachi Chemical Co., Ltd.	19
Integrated Technology Corporation	37
Integrated Test Corporation	13
International Test Solutions, Inc.	6
Intest Corporation	22
IWIN Co., LTD.	11
JEM America Corp.	5
Kita USA, Inc.	26
Korea Instrument	36
MarTek, Inc.	15
LEENO Industrial, Inc.	42
MJC	1
MPI Corporation	2
NTK Technologies	28
OpTek Systems, Inc.	21
Oxford Lasers	29
PacTech USA	38
Plastronics	16
Prober.com	40
R&D Altanova	25
Rika Denshi America, Inc.	34
Rudolph Technologies	27
Specialty Coating Systems	23
STAr Technologies, Inc.	31
SV TCL - An SV Probe Company	30
Synergie Cad Probe	24
T.I.P.S. Messtechnik GmbH	7
Technoprobe America, Inc.	39
Teradyne Global Services Organization	3
Tokyo Electron Limited	12
Vermont Microtechnologies	20

2016

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PROGRAM SCHEDULE

Program Overview

The 26th Annual SW Test Workshop will be held at the Rancho Bernardo Inn in San Diego, California, from June 5-8, 2016. The Workshop will begin on Sunday morning with a golf tournament and Sunday afternoon with a topical tutorial, followed by a welcome reception, dinner, and a Keynote Speaker. The Technical Program will start Monday morning with 30-minute presentations in theme-oriented sessions. SW Test EXPO 2016 will showcase many of the key suppliers to the wafer probe industry and, as always, there will be ample opportunities for networking. The workshop will conclude on Wednesday at Noon after an awards presentation and lunch. Conference registration includes all meals, refreshments, social activities, and technical program and exhibit attendance, as well as the eProceedings.

June 5, 2016 (Sunday)

7:00 AM - 1:00 PM	**5th Annual SW Test William Mann Golf Tournament**
7:00 - 8:00	Box Breakfast
8:00	Tee Off: Scramble, Reverse Shotgun Format

2:00 PM - 4:00 PM	**Tutorials**
	Tutorial on the Effects of Probe Marks on Wirebonding Priscila Brown (Brigham Young University Idaho – Rexburg, ID, USA), Stevan Hunter (ON Semiconductor – Phoenix, AZ, USA) Presenter: Dr. Stevan Hunter (ON Semiconductor – Phoenix, AZ USA)
	Analysis for Pre-Mature Worn-out of Vertical Probe Needle Wiljelm Carl Olalia (ON Semiconductor Philippines, Inc. – Carmona, Philippines)
	Understanding the Probe Damage Risk thru Determination of Minimum Bond Pad Opening Capability of Different Prober and Needle Type Set-up Wiljelm Carl Olalia (ON Semiconductor Philippines, Inc. – Carmona, Philippines)
	Reducing Probe Needle Damage on Bond Pad Using Six Sigma Methodology Glenn Placido (ON Semiconductor Philippines, Inc. – Carmona, Philippines)

4:00 PM - 6:00 PM	**REGISTRATION OPEN**
6:00 PM - 7:00 PM	**WELCOME RECEPTION**
7:00 PM - 8:15 PM	**BUFFET DINNER**

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Keynote Presentation

8:15 PM - 9:45 PM	Evening Session
8:15 - 8:30	***Opening Remarks for SW Test 2016*** Jerry Broz, Ph.D., General Chair
8:30 - 9:45	***KEYNOTE*** *"Test and Validation in an Analog and Embedded Environment: Challenges, Limitations, and Future in the Test Development Process"* **Friedrich Taenzler, Ph.D.** RF-Engineering Manager Texas Instruments, Inc.



Dr. Friedrich Taenzler is Senior Member of the Technical Staff, Program Manager, Production Test Veteran, and text book author.

His main interests are the developments of low cost test strategies and solutions for Mixed Signal, RF, MCU, and Non-Volatile Memory devices as well as the required ATE systems.

He closely works with a number of universities as a liaison driving test related research projects, and also academia classes on test.

Friedrich obtained his Dipl.-Ing. and Doctoral Degree in Electrical Engineering from Mercator University Duisburg/Germany in 1988 resp. 1994.

In his keynote presentation, Dr. Taenzler will explore and overview the differences and challenges a typical analog test environment is grappling. The diversity of products in the analog, mixed signal, and embedded markets will be discussed. A review regarding probe and package test requirements, followed by the implementation and requirements on the test equipment, infrastructure, and expectations will follow.

One important item within this diversity of test solutions is the people developing, implementing, and maintaining of test solutions. This part of the test implementation, with training, knowledge sharing, and alignment between high numbers of test development and sustaining teams, will also be discussed.

9:45 PM NETWORKING / HOSPITALITY SUITES

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PROGRAM SCHEDULE

June 6, 2016 (Monday)	
7:00 AM - 8:00 AM CONTINENTAL BREAKFAST **7:00 AM - 5:00 PM REGISTRATION**	
8:00 AM - 8:30 AM	**Welcome**
8:00 - 8:30	***Welcome to SWTW-2016*** Jerry Broz, Ph.D., General Chair
8:30 AM - 10:00 AM	**SESSION 1: Test Strategy Innovations** **Session Chair: Jerry Broz**
8:30 - 9:00	***AMD High Pin Count Probing Challenges on Leading Edge GPU: Technoprobe TPEG™ MEMS vs. Cobra*** Presenters: Foo Xin-Reng (AMD – Singapore); and Raffaele Vallauri (Technoprobe Italy)
9:00 - 9:30	***Verification of High-Bandwidth-Memory (HBM) through direct probing on MicroBumps*** Authors: Marc Loranger (Form Factor Inc.); and Sung-wook Moon (SK Hynix) Presenter: Marc Loranger (Form Factor Inc.)
9:30 - 10:00	***Automated Testing of Bare Die-to-Die Stacks*** Authors: Erik Jan Marinissen, Bart De Wachter, Teng Wang, (IMEC – Leuven, Belgium); Joerg Kiesewetter, Jens Fiedler, Karsten Stoll (Cascade Microtech – Germany); Daniel Rishavy (Cascade Microtech – USA) Presenter: Daniel Rishavy (Cascade Microtech –USA)
10:00 AM - 10:30 AM COFFEE BREAK	
10:30 AM - 12:00	**SESSION 2: Drilling** **Session Chair: Joey Wu (MPI Corp - Taiwan)**
10:30 - 11:00	***Advanced Laser Bonding of Ultra Fine Pitch Cantilever Spring Pins for Assembly of Flash, DRAM and Logic Probe Cards*** Thomas Oppert (PacTech-Packaging Technologies - Germany)
11:00 - 11:30	***SMART Laser Drilling for Advanced Vertical Probe Card Manufacturing*** Dr. Alan Ferguson, Dr. Martyn Knowles, Dr. Andrew Kearsley, Michael Gaukroger, Dimitris Karnakis, Riccardo Geremia, Simon Touhy, Michael Cullimore (Oxford Lasers – Didcot, U.K.) Presenter: Dr. Alan Ferguson (Oxford Lasers – Didcot, U.K.)
11:30 - 12:00	***Innovative Laser Processing and Drilling Techniques for Future Probe Card Applications*** Hung-Lung Chen (KJet Laser Tek Inc. – HsinCHu City, Taiwan)
12:00 NOON - 1:00 PM LUNCH ON THE LAWN	

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1:00 PM - 3:00 PM	**SESSION 3 — New Testing Challenges and Solutions** **Session Chair: Clark Liu (PTI – HsiChu, Taiwan)**
1:00 - 1:30	***Thermal Testing of Singulated Devices Get Us Closer to Known-Good Die/Stack*** David Armstrong (Advantest – USA)
1:30 - 2:00	***Robotisation and Test of image sensors*** Philippe Sandri (E2V –France)
2:00 - 2:30	***Achieving Higher Speeds for CMOS Image Sensor Testing*** Minoru Mikami (FormFactor – Yokohama-shi, Japan) Presenter: Larry Levy (FormFactor – Livermore, CA, USA)
2:30 PM - 3:00 PM COFFEE BREAK	
3:00 PM - 4:30 PM	**SESSION 4 — Bump and Array** **Session Chair: Dr. Michael Huebner (FormFactor, Inc.)**
3:00 - 3:30	***Probing for WLP Evaluation*** Clark Liu (PTI – Taiwan)
3:30 - 4:00	***GLOBALFOUNDRIES and MPI Pre-bump probing challenges: MPI inter-changeable pre-bump probe solution*** Qu Yang (GLOBAL FOUNDRIES – Singapore)
4:00 - 4:30	***Managing Hardware Cost for Large Area Array C4 Bump/Cu Pillar SOC Applications using Improved MEMS Methodology*** Michael Chrastecky (BucklingBeam Solutions, LLC)
EXHIBITS OPEN	
5:00 PM RECEPTION & CARVING STATION DINNER IN EXPO HALL	

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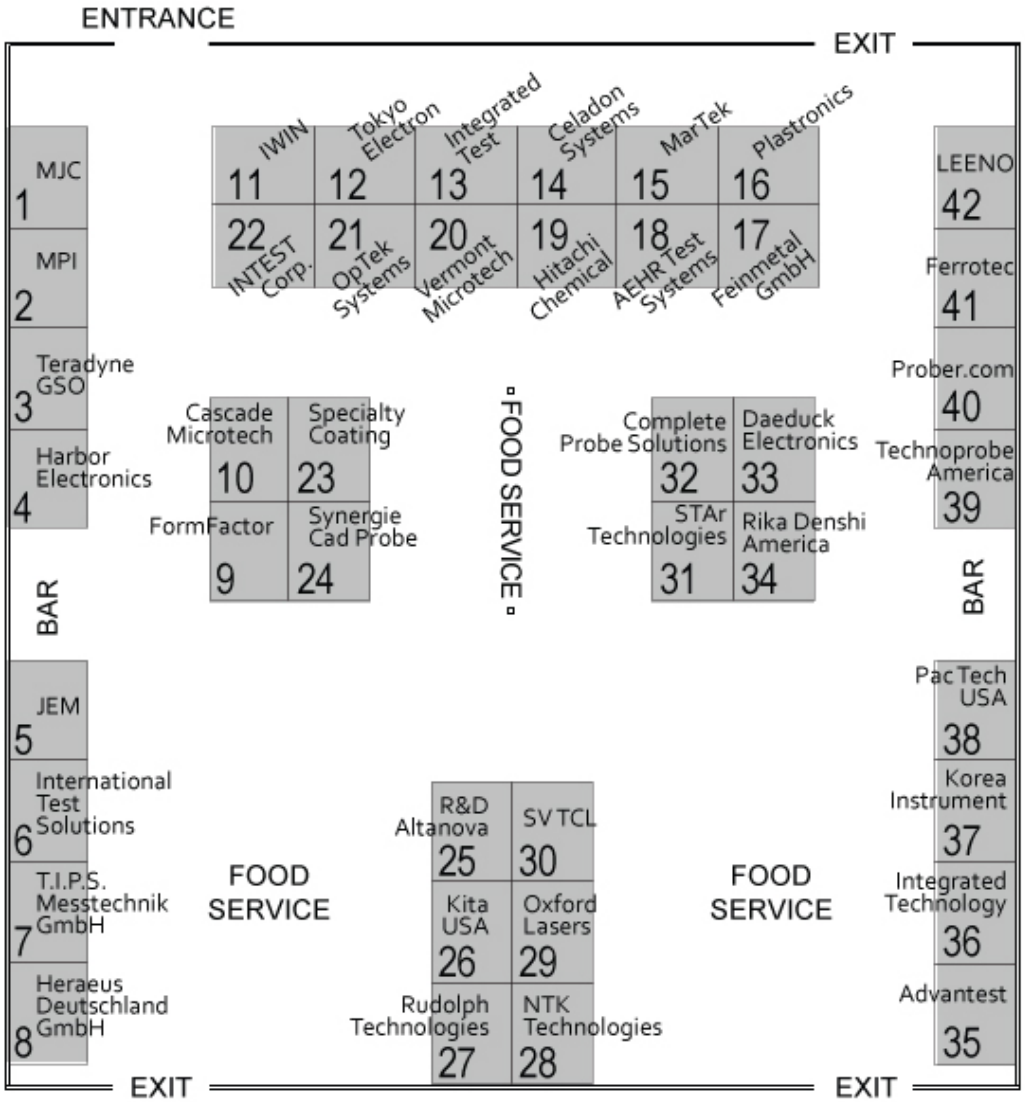
PROGRAM SCHEDULE

SW Test 2016 EXPO

5:00 PM - 8:00 PM	**EXHIBITS OPEN**

5:00 PM RECEPTION & CARVING STATION DINNER IN EXPO HALL

2016 EXHIBITORS



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PROGRAM SCHEDULE

June 7, 2016 (Tuesday)	
7:00 AM - 8:00 AM	**CONTINENTAL BREAKFAST**
7:00 AM – 3:00 PM	**REGISTRATION OPEN**
8:00 AM - 10:00 AM	**SESSION 5 — Moving Forward with Space Transformer Technology** **Session Chair: Mr. Frederick Taber (Taber Consulting – USA)**
8:00 - 8:30	***Optimization for Polyimide Circuit Design of Space Transformer on Probecard*** TAE KYUN KIM (MICROFRIEND INC – Korea)
8:30 - 9:00	***Vertical Probe Card : Probe Head for Improved SI/PI*** Jung Keun Park (Willtechnology – Korea)
9:00 - 9:30	***Production Test RF Calibration for Multi-DUT Probe Cards: How to Get the Most Accurate Measurements*** Daniel Bock (Cascade Microtech – USA)
9:30 - 10:00	**Automated Probe Card Exchange and Docking for RADAR Products** Jory Twitchell (NXP Semiconductor – USA)
10:00 AM - 10:30 AM	**COFFEE BREAK**
10:30 AM - 12:00	**SESSION 6: Power Probing at Temperature** **Session Chair: Rey Rincon (Freescale Semiconductor)**
10:30 - 11:00	***Customized Probe Card for On-Wafer Testing of AlGaN/GaN Power Transistors*** Bryan Root (Celadon Systems, Inc. – USA)
11:00 - 11:30	***GLOBALFOUNDRIES High and Low Temperature Probing Challenges: Technoprobe Probing Solution*** Authors: Joy Chang, Guo Chang Man, Jeffery Lam (Globalfoundries – Singapore), Hellen Kee (Technoprobe – Singapore), Marco Prea (Technoprobe – Italy) Presenters: Raffaele Vallauri (Technoprobe - Italy) and Yah Ean Koh (Globalfoundries - Singapore)
11:30 - 12:00	***High Voltage, High Current, High Temperature – and Sometimes All Come Together at the Same Time…*** Dr. Rainer Gaggl (T.I.P.S. Messtechnik – Austria)
12:00 NOON - 1:00 PM	**LUNCH ON THE LAWN**

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PROGRAM SCHEDULE

1:00 PM - 3:00 PM	**SESSION 7: Probecard Potpourri** **Session Chair: Mark Ojeda (Cypress - USA)**
1:00 - 1:30	***Multi-site Probing of Magnetic Sensors at 175 deg C*** Geert Gouwy (Melexis – Leper, Belgium)
1:30 - 2:00	***General Overview on Pad Damage: Probe Key Parameters and Other Causes*** Riccardo Vettori (Technoprobe – Italy)
2:00 - 2:30	***Automated Thermal Drift Correction of Discrete Probes on Motorized Positioners for Device Characterization*** Joe Frankel and Koby Duckworth (Cascade Microtech – USA)
3:00 PM - 5:00 PM	**EXHIBITS OPEN**
3:00 - 5:00	**PM Break - Refreshments Served in Expo Hall**

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PROGRAM SCHEDULE

Tuesday Evening SOCIAL	
6:00 PM - 9:00 PM	**SOCIAL: "Luck be a Lady Tonight" … Casino Night and Social Club**
6:00 - 9:00	**Cocktail Reception, Dinner, and Entertainment**







9:00 PM NETWORKING / HOSPITALITY SUITES

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PROGRAM SCHEDULE

June 8, 2016 (Wednesday)

7:00 AM - 8:00 AM	**CONTINENTAL BREAKFAST**
7:30 AM – 10:00 AM	**REGISTRATION OPEN**
8:00 AM - 10:00 AM	**SESSION 8: Moving from x1 to x123 SOIC Probe Efficiency Improvements** **Session Chair: Alan Wegleitner (Texas Instruments)**
8:00 - 8:30	***A New Approach to Low Pin Count Products Test Found Vertical Probes to be Superior to Cantilever*** Franz Steger (Texas Instruments Deuschland GmbH – Germany)
8:30 - 9:00	***Probing Cu Pillar Applications w/ Vertical Technologies*** Brandon Mair (Texas Instruments – Dallas)
9:00 - 9:30	***Interlayer Dielectric (ILD) Cracking Mechanisms and Their Effects on Probe Processes*** Daniel Fresquez (Texas Instruments Inc. – Dallas)
9:30 - 10:00	***A Customized Additional Advanced Loopback technology on Vertical Probe Card*** Alex Wei (MPI Corporation – Taiwan)
10:00 AM - 10:30 AM	**COFFEE BREAK**
10:30 AM - 12:00	**SESSION 9: Process Improvement** **Session Chair: Patrick Mui (JEM America)**
10:30 - 11:00	***A Probe Card Metrology Process Enabling Fast Feedback Loops to Reduce Operational and Maintenance Related Cost*** Martin Kunz and Dr. Jörg Nannen (NanoFocus AG – Germany) Presenter: Martin Kunz (NanoFocus AG – Germany)
11:00 - 11:30	***Sustaining and Improving Obsolete Test Systems*** Carl Scharrer (Texas Instruments, Inc – Dallas, TX, USA)
11:30 - 12:00	***Awards Presentations*** Jerry Broz and Rey Rincon (SW Test General Chair and Program Chair) Presenter: Jerry Broz (SW Test General Chair)
12:00 NOON - 12:30 PM	**AWARDS & LUNCH**

SW Test Workshop
Semiconductor Wafer Test Workshop

Technical Program
SW Test 2016

Tuesday, June 7, 2016

June 5-8, 2016

Tuesday, June 7, 2016

8:00 to 10:00 AM – Space Transformer Technology

Optimization for Polyimide Circuit Design of Space Transformer on Probecard

Tae Kyun Kim (MICROFRIEND INC – Korea)

Vertical Probe Card : Probe Head for Improved SI/PI

Jung Keun Park (Willtechnology – Korea)

Production Test RF Calibration for Multi-DUT Probe Cards: How to Get the Most Accurate Measurements

Daniel Bock (Cascade Microtech – USA)

Automated Probe Card Exchange and Docking for RADAR Products

Jory Twitchell (NXP Semiconductor – USA)

SW Test Workshop - June 5-8, 2016

Tuesday, June 7, 2016

10:30 AM to 12:00PM – Power Probing at Temperature

Customized Probe Card for On-Wafer Testing of AlGaN/GaN Power Transistors

Bryan Root (Celadon Systems, Inc. – USA)

GLOBALFOUNDRIES High and Low Temperature Probing Challenges: Technoprobe Probing Solution

Joy Chang, Guo Chang Man, Jeffery Lam (Globalfoundries – Singapore), Hellen Kee (Technoprobe Singapore), Marco Prea (Technoprobe – Italy)

Raffaele Vallauri (Technoprobe - Italy) and Yah Ean Koh (Globalfoundries - Singapore)

High Voltage, High Current, High Temperature – and Sometimes All Come Together at the Same Time…

Dr. Rainer Gaggl (T.I.P.S. Messtechnik – Austria)

SW Test Workshop - June 5-8, 2016

Tuesday, June 7, 2016

1:00 to 3:00 PM – Probecard Potpourri …

Multi-site Probing of Magnetic Sensors at 175 deg C

Geert Gouwy (Melexis – Leper, Belgium) and Josef Mai (JEM Europe)

General Overview on Pad Damage:
Probe Key Parameters and Other Causes

Riccardo Vettori (Technoprobe – Italy)

Automated Thermal Drift Correction of Discrete Probes on Motorized Positioners for Device Characterization

Joe Frankel and Koby Duckworth (Cascade Microtech – USA)

SW Test Workshop - June 5-8, 2016

Tuesday, June 9, 2016

3:00 to 5:00 PM – EXPO 2016

Celebrate at Rancho Bernardo Inn

6:00 to 9:00 PM

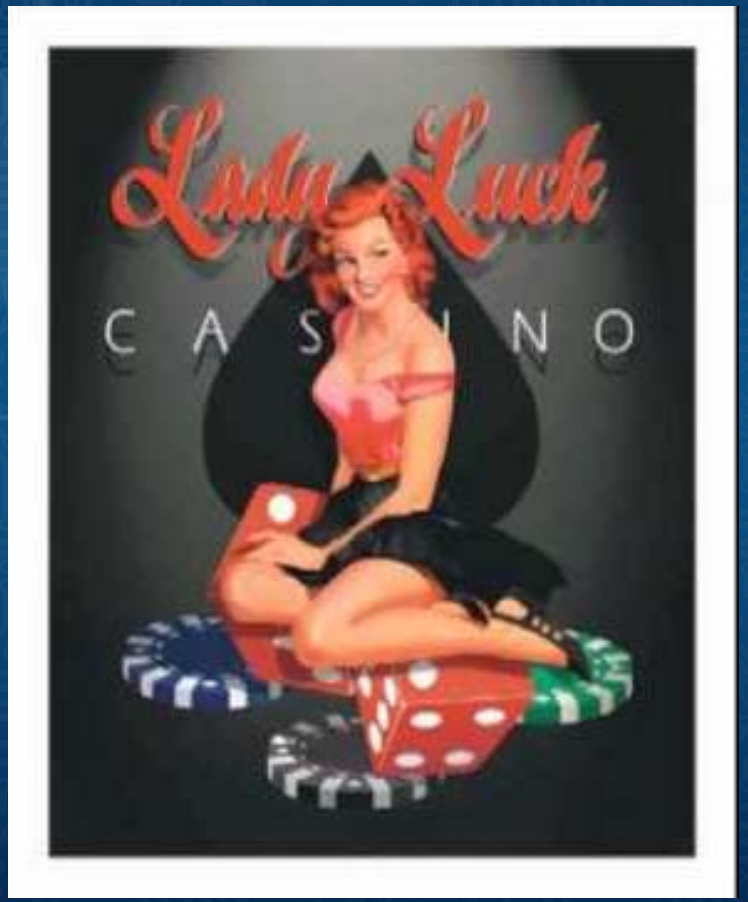


SW Test Workshop - June 5-8, 2016

Tuesday Social Celebrates Las Vegas Style Casino Night

- **Cocktails, Dinner and Gambling, Lounge Singing**





SW Test Workshop - June 5-8, 2016

Thanks for Attending …

See you again … June 4 to 7, 2017 !!!



SW Test Workshop - June 5-8, 2016

Thanks for your Support !

- **Contact the SW Test Team with any questions …**

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SW Test Workshop - June 5-8, 2016

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Save the Dates

Rancho Bernardo Inn, San Diego, CA
June 4-7, 2017

Abstract Submission Date
March 6, 2017

Golf Tournament
June 4, 2017

See You Next Year!

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Technical Program
SW Test 2016

Tuesday, June 7, 2016

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SW Test Workshop
Semiconductor Wafer Test Workshop

Optimization for Polyimide Circuit Design of Space Transformer on Probe Card

Sang-Kyu Yoo
Samsung Electronics

Tae-Kyun Kim, Yong-Ho Cho
Microfriend

Jong-Kwan Yook
Yonsei University

June 5-8, 2016

Overview

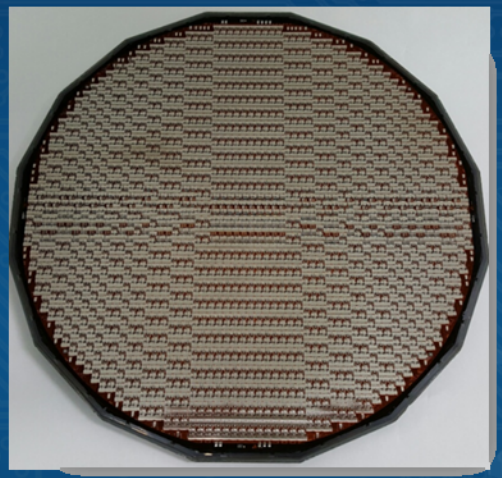
- Introduction of Probe Card Test
- Basic Study for Polyimide Circuit Design
- Signal Integrity on Probe Card
- Summary
- Future Works

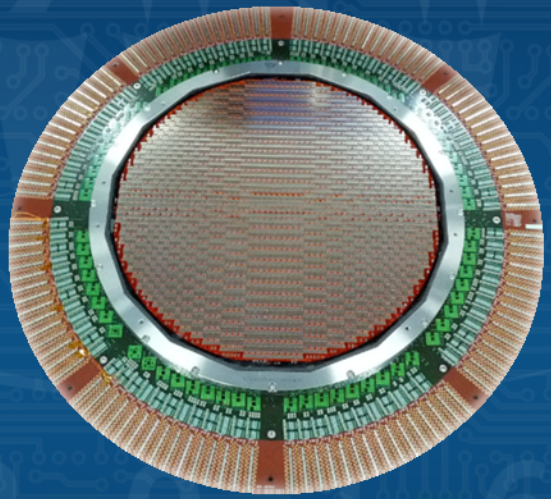
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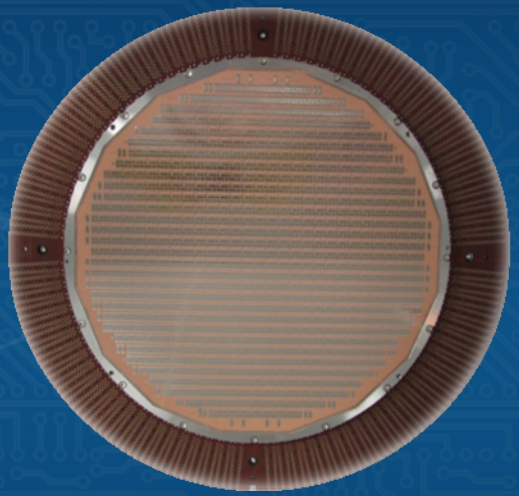
FormFactor v. Technoprobe
IPR2024-00933

Introduction of Probe Card Test

- **Probe Card needs for High Parallel, High Speed and High Density.**







- Probe Card has a Function of Interface between ATE and Device.
- As Test Channels are Increase, Signal Integrity is getting more Important.
- It is necessary for High Parallel, High Density and High Speed on Probe Card.

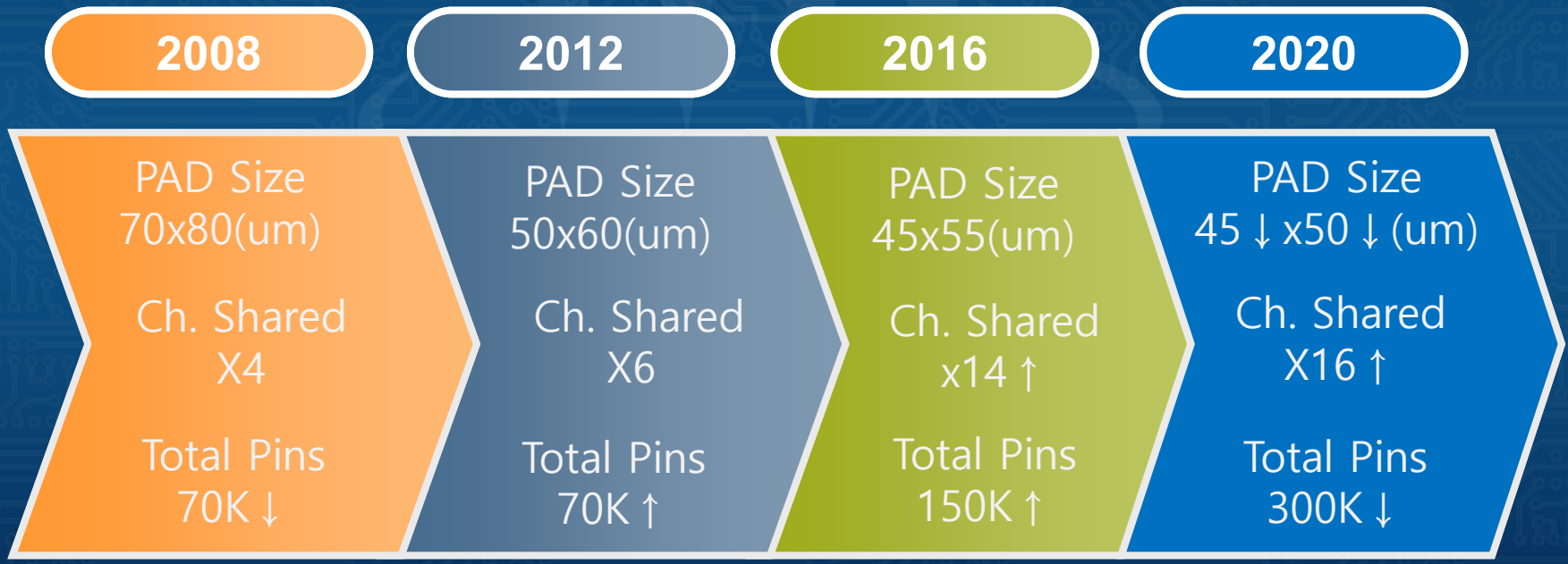
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Introduction of Probe Card Test

- **Test Trends**

- Smaller PAD Size & Fine Pitch and Higher Pin Counts
- Necessity of High Speed Testing Technology on Probe Card
- Higher Circuit Design Density

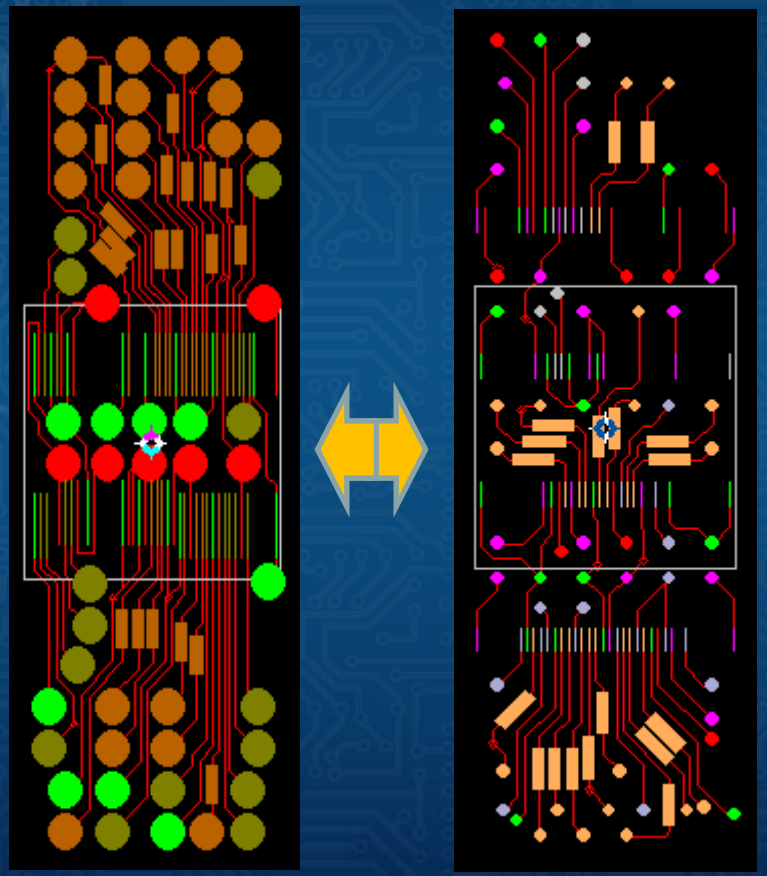


FormFactor Ex. 1031, p. 30

FormFactor v. Technoprobe
IPR2024-00933

Introduction of Probe Card Test

- **Advantage of Polyimide Thin Film**
  - Very Small VIA Hole
  - Highly Denser Circuit
  - Low Relative Dielectric Constant
  - High Propagation Velocity
  - High Speed Digital Circuits
  - Low Cost



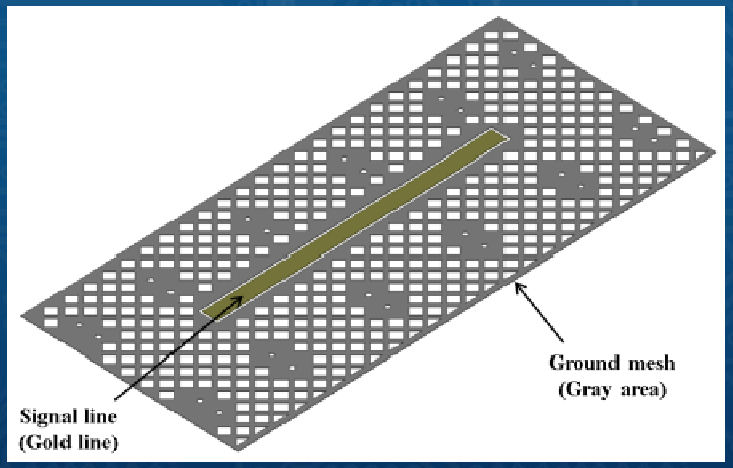
FormFactor Ex. 1031, p. 31

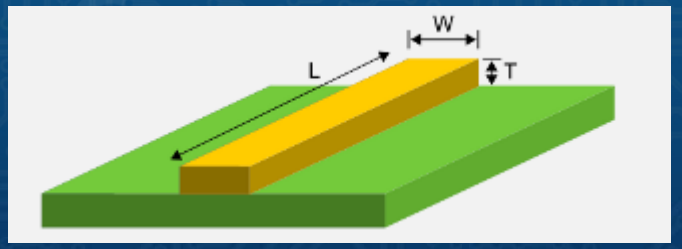
FormFactor v. Technoprobe
IPR2024-00933

Basic Study for PI Circuit Design

- **Needs for Electrical Characteristics of Circuit Trace in Polyimide Thin Film**

  - Dielectric Constant : 3.2
  - Impedance depends on Trace THK., Width, Material, Ground(Mesh & Plane)



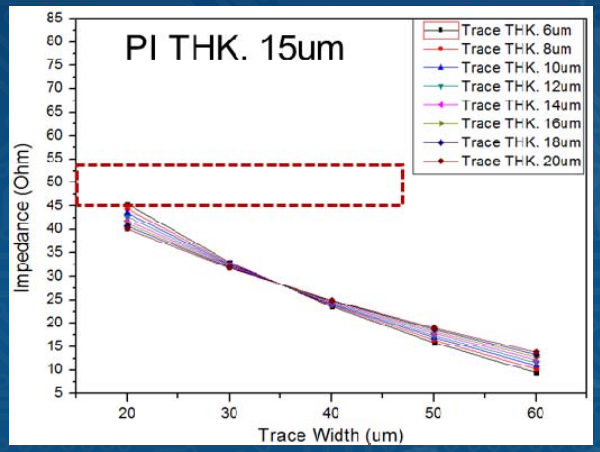


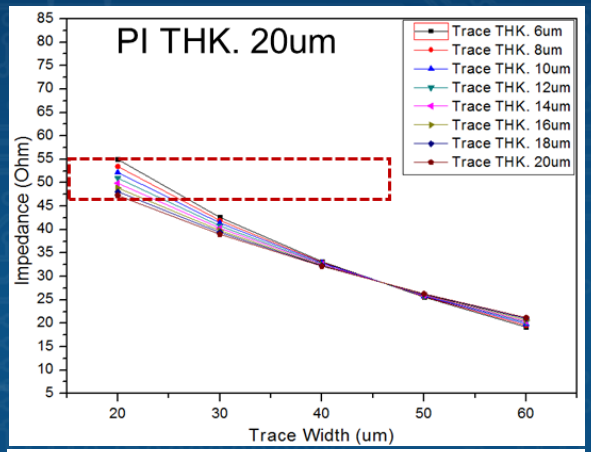
FormFactor Ex. 1031, p. 32

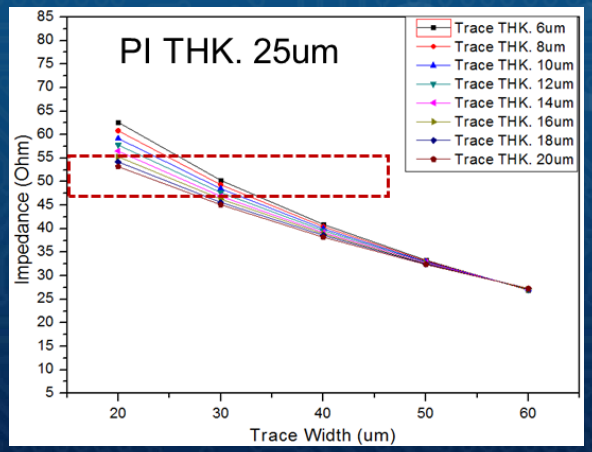
FormFactor v. Technoprobe
IPR2024-00933

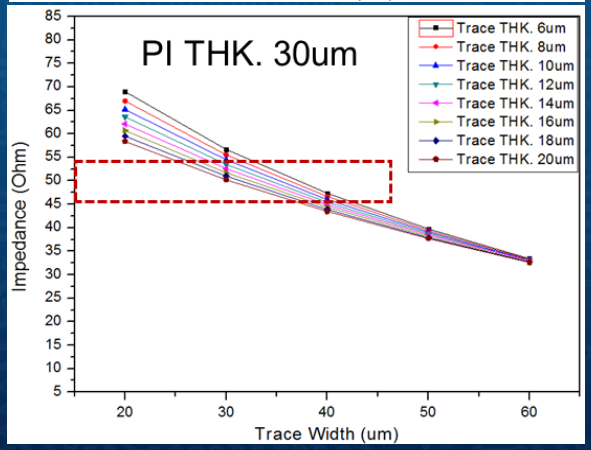
Basic Study for PI Circuit Design

- **Impedance depends on Circuit Trace Width & Thickness and PI Thickness.**



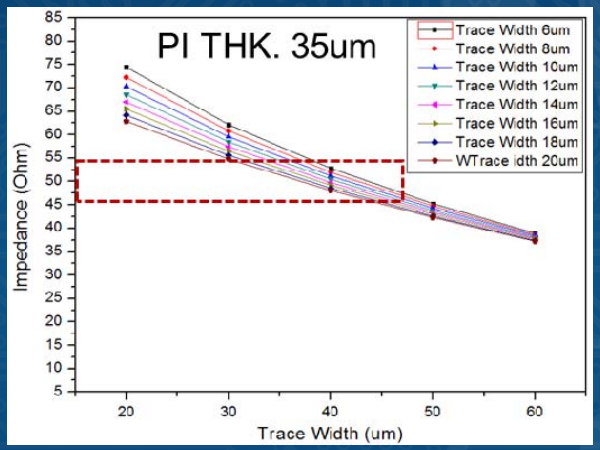


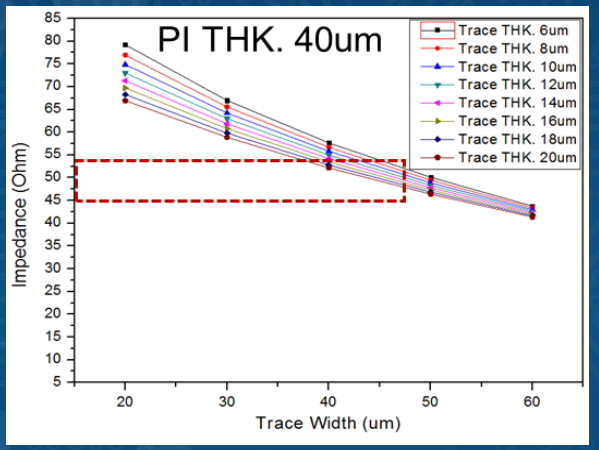




Basic Study for PI Circuit Design

- **Impedance depends on**
  Circuit Trace Width & Thickness and PI Thickness.



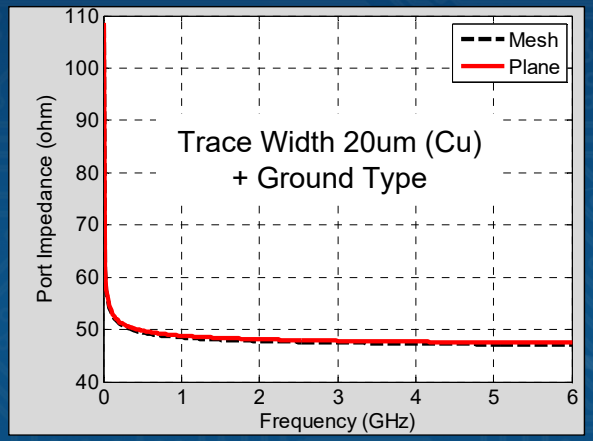


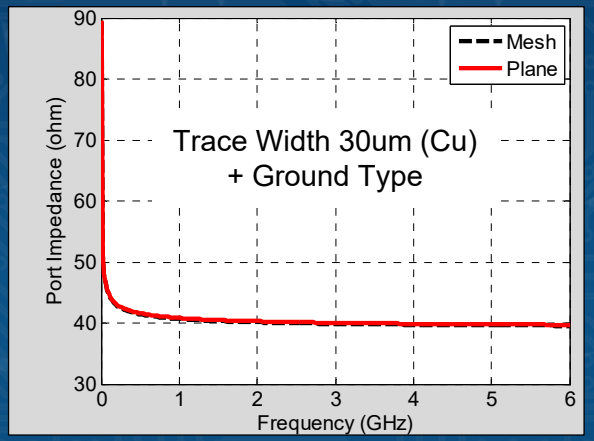
- **Circuit Design on Polyimide Thin Film**
  - Normally, Target Impedance needs for 50±10% Ohm.
  - Impedance mismatching affects poor Signal Quality.

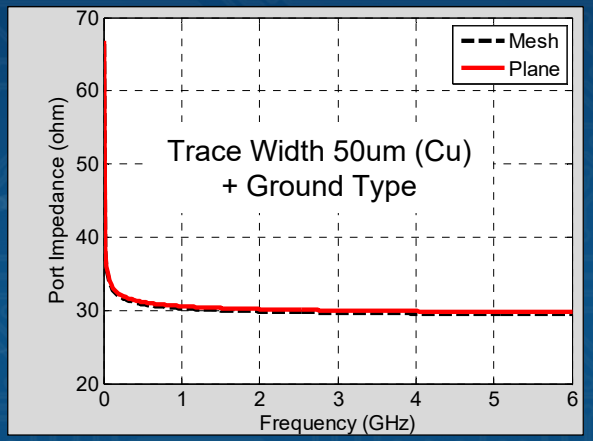
FormFactor Ex. 1031, p. 34
FormFactor v. Technoprobe
IPR2024-00933

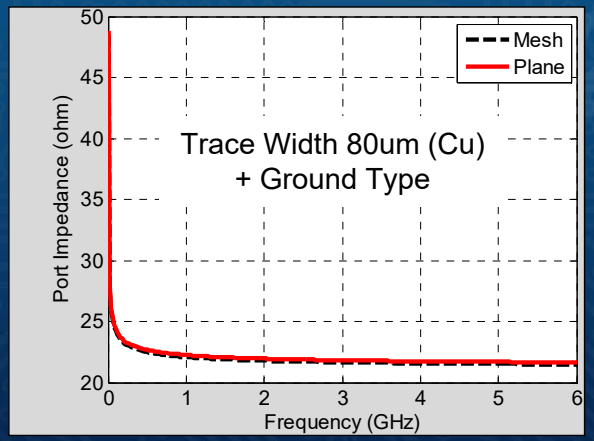
Basic Study for PI Circuit Design

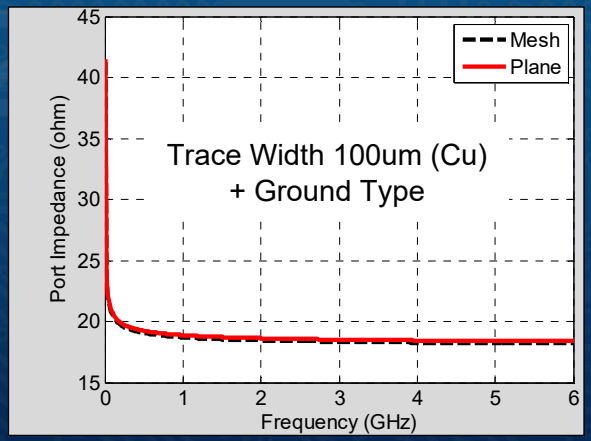
- **Analysis of Impedance for Trace Material (Cu), Width and Ground Type (Mesh or Plane)**

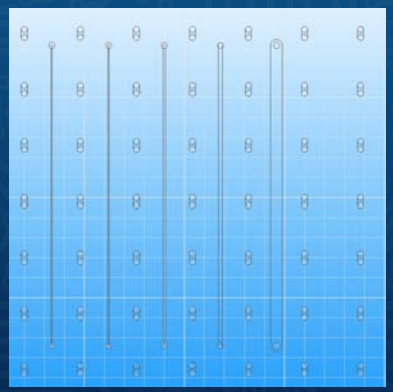








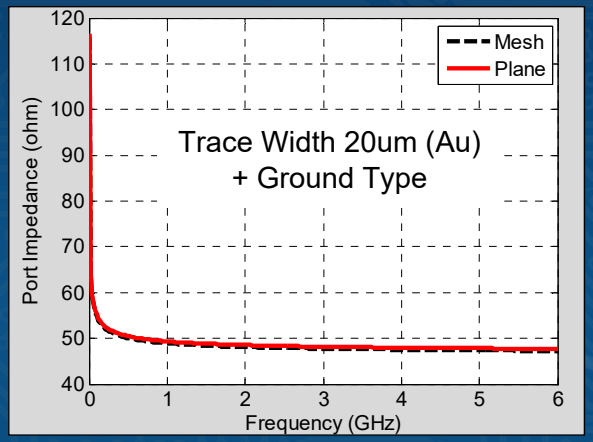


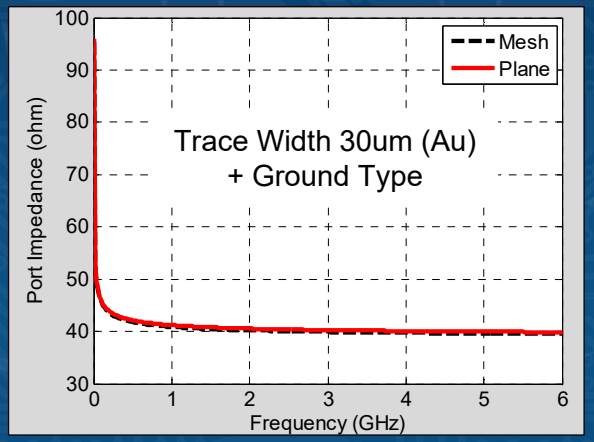


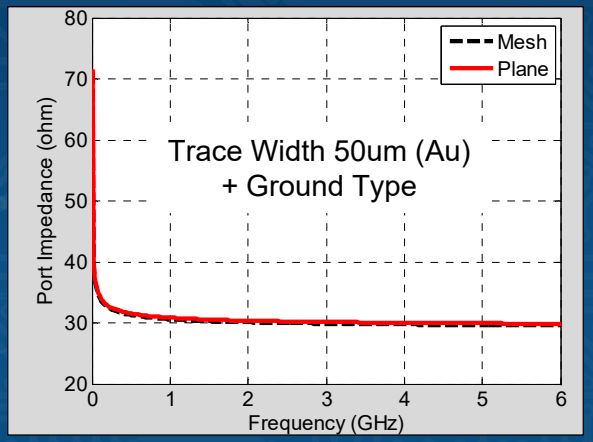
SW Test Workshop - June 5-8, 2016

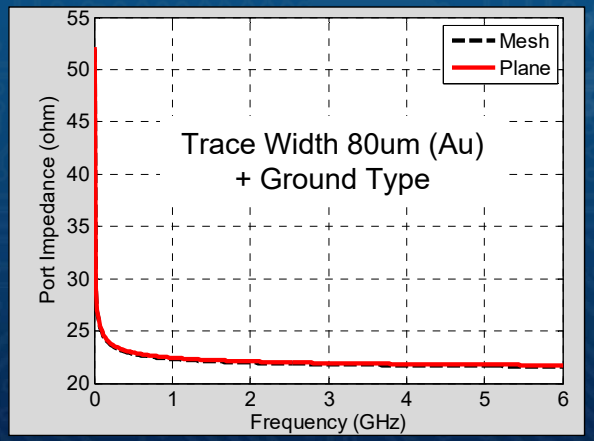
Basic Study for PI Circuit Design

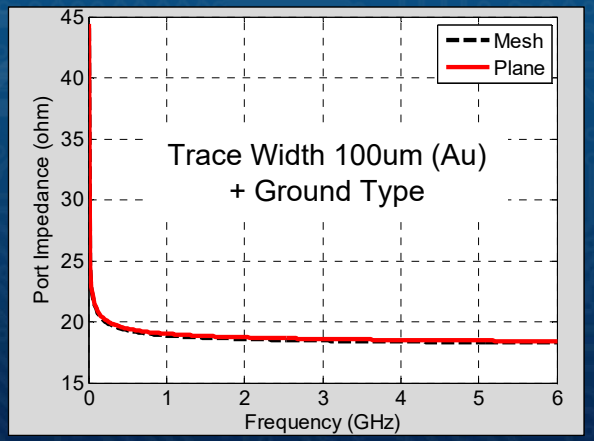
- **Analysis of Impedance for Trace Material (Au), Width and Ground Type (Mesh or Plane)**













SW Test Workshop - June 5-8, 2016

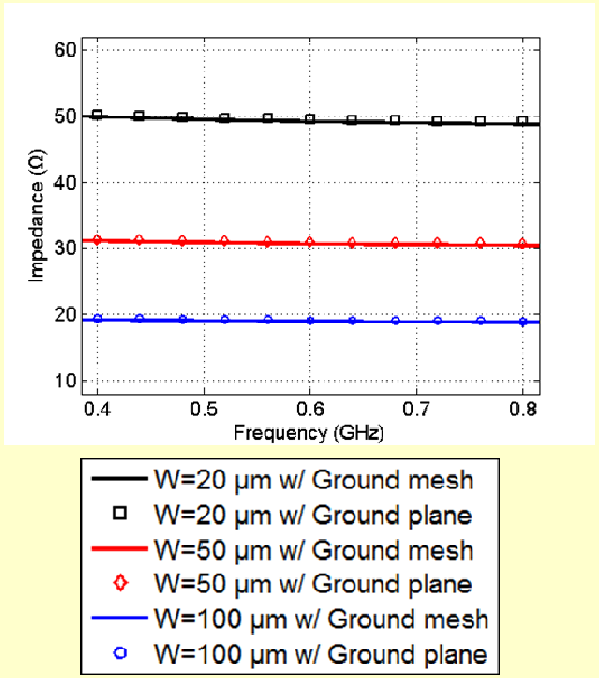
Basic Study for PI Circuit Design

- **Analysis of Impedance for Circuit Trace**

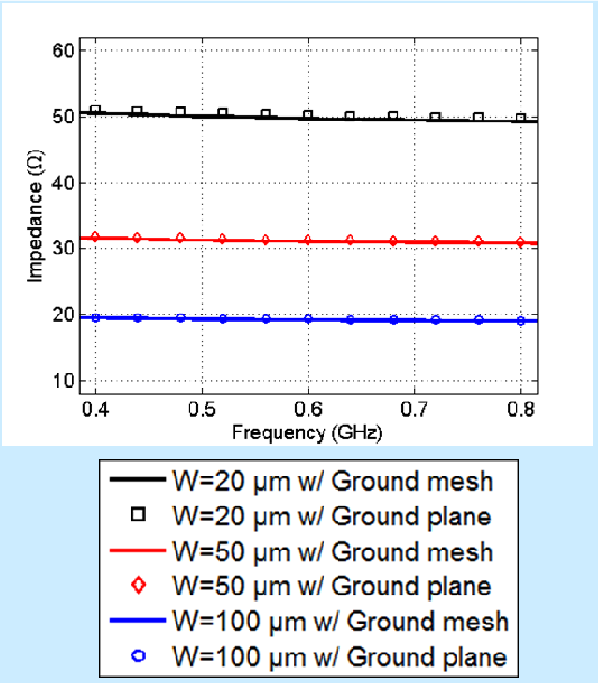
  - Depends on Circuit Material, Width and Ground Type

  - Copper (Cu) vs Gold (Au)

Copper (Cu)



Gold (Au)

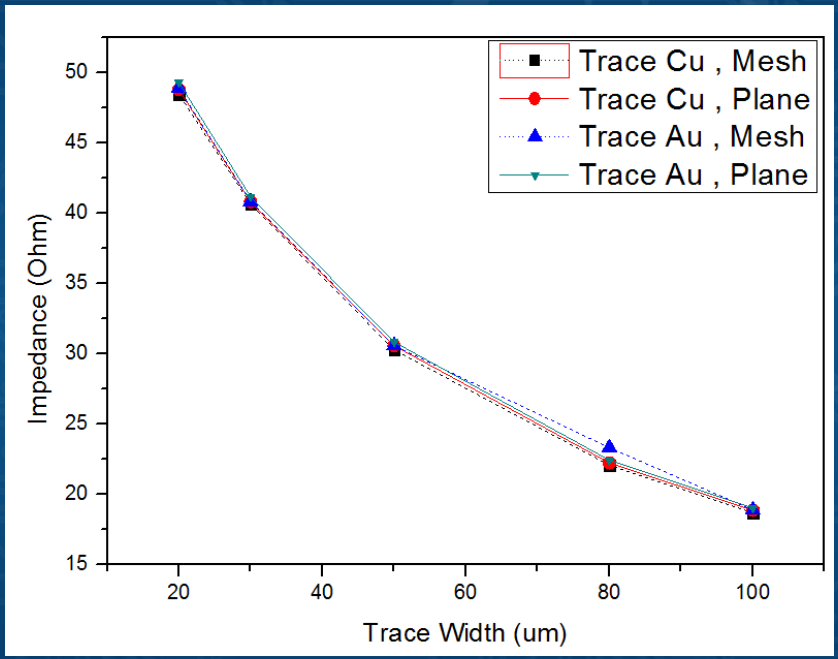


FormFactor Ex. 1031, p. 37

FormFactor v. Technoprobe
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Basic Study for PI Circuit Design

- **Impedance Compared of Copper (Cu) with Gold (Au)**



Resistivity

Cupper (Cu)

: 1.68×10^{-8} Ωm

Gold (Au)

: 2.2×10^{-8} Ωm

- Copper (Cu) vs Gold (Au) , Mesh Ground vs Plane Ground

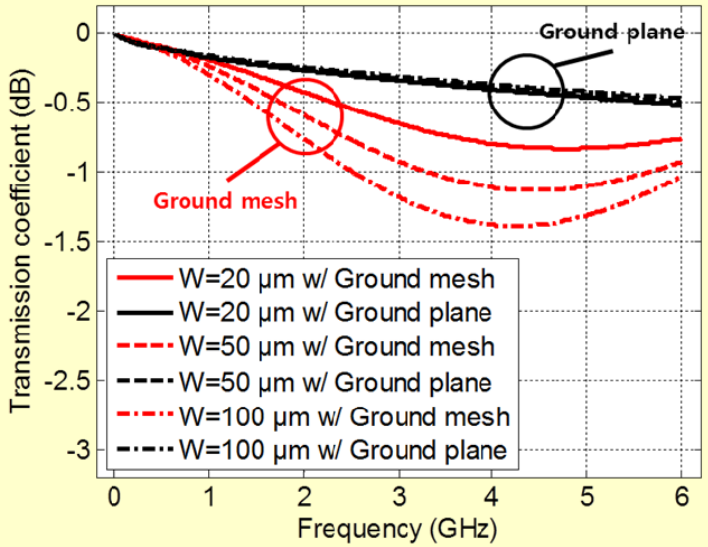
FormFactor Ex. 1031, p. 38

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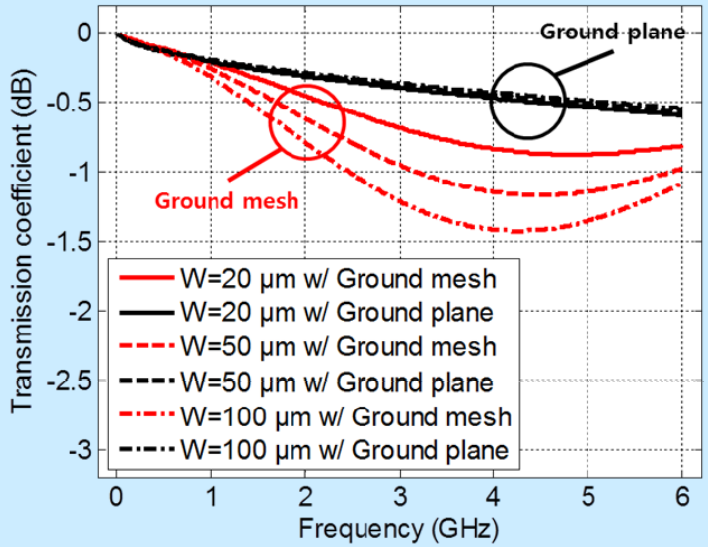
Basic Study for PI Circuit Design

- **Insertion Loss (Transmission coefficient)**
  - Depends on Circuit Material, Width and Ground type(Mesh & Plane)
  - Mesh Ground Insertion Loss Max. -1.5dB @ 4GHz

Copper (Cu)



Gold (Au)

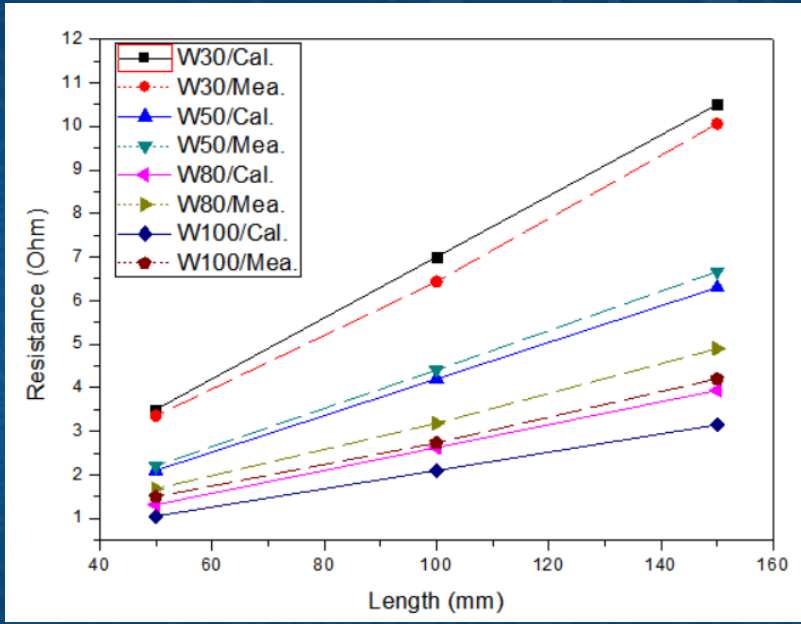


FormFactor Ex. 1031, p. 39

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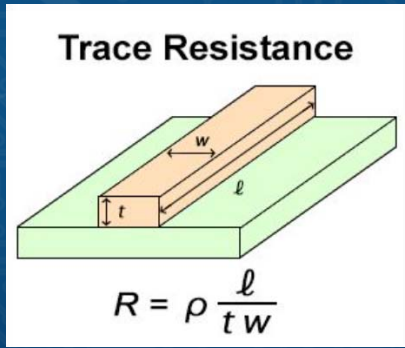
Basic Study for PI Circuit Design

- **Measurement vs Calculation (Trace)**



Copper Resistivity

1.68×10^{-8} Ωm



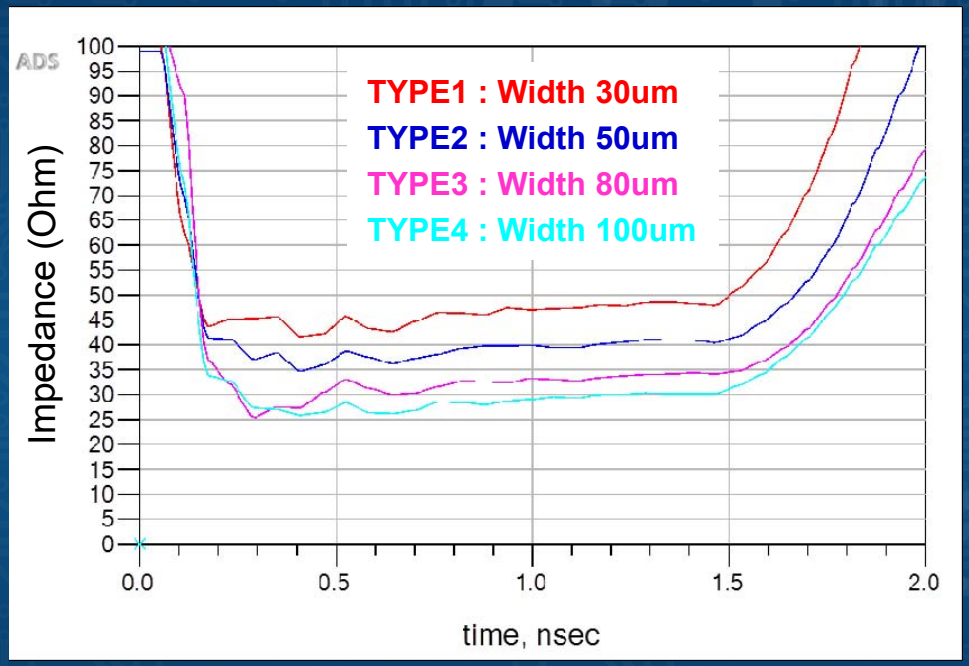
- As Trace Length is Large, the Resistance is getting Higher.
- As Trace Width is Large, the Resistance is getting Lower.

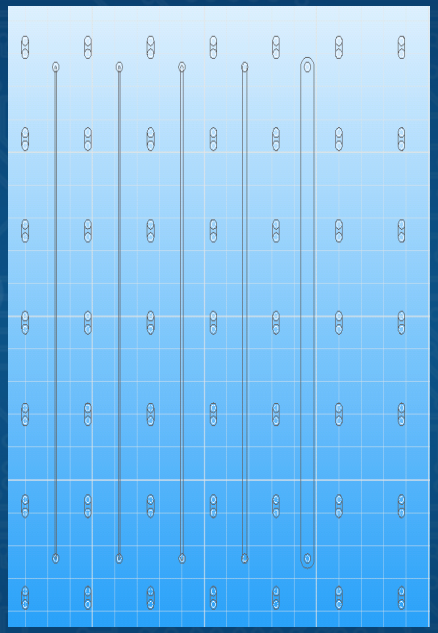
FormFactor Ex. 1031, p. 40

FormFactor v. Technoprobe
IPR2024-00933

Basic Study for PI Circuit Design

- **Measurement (Impedance)**





- As Trace Width is Small, the Impedance is getting Higher.
- Measurement shows impedance for Circuit Trace Width.

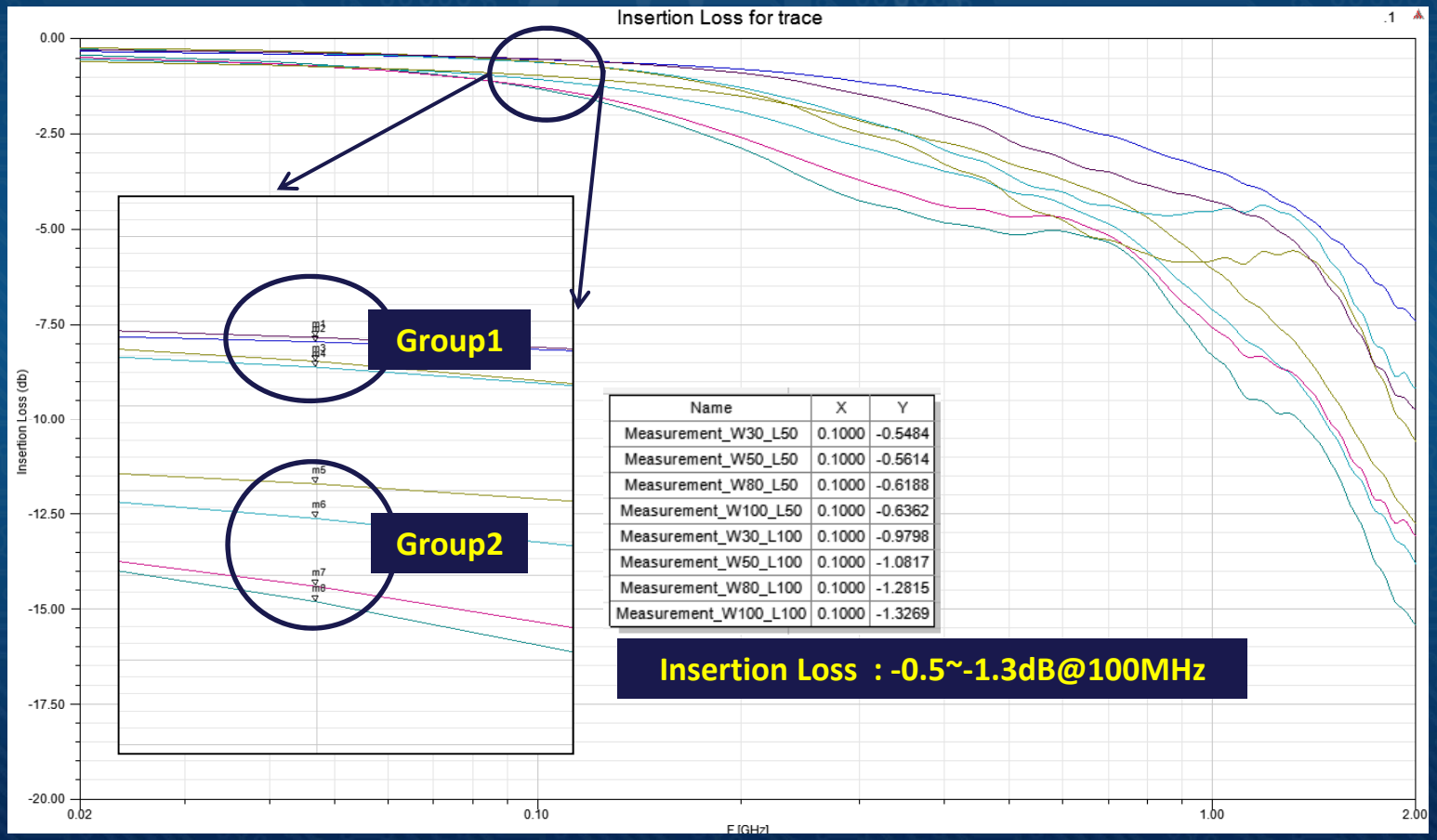
FormFactor Ex. 1031, p. 41

FormFactor v. Technoprobe
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Basic Study for PI Circuit Design

- **Measurement (Insertion Loss)**

  - Analysis of Circuit Trace on Polyimide Thin Film



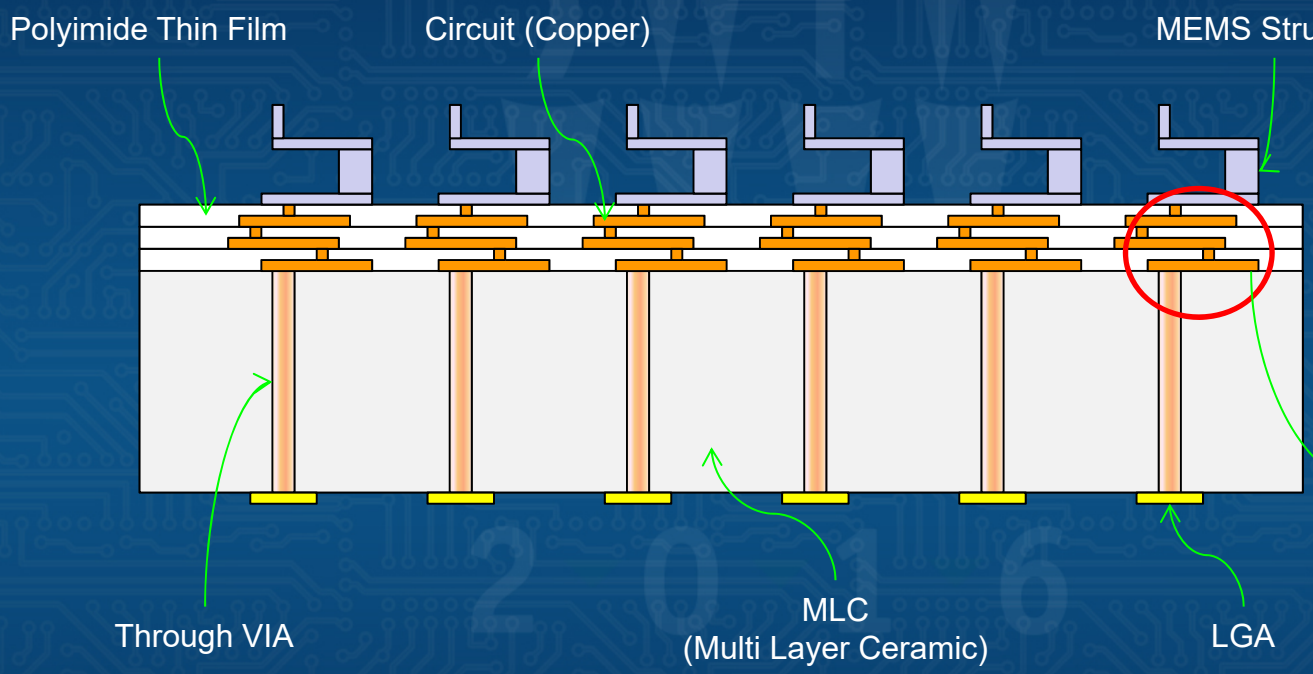
Name	X	Y
Measurement_W30_L50	0.1000	-0.5484
Measurement_W50_L50	0.1000	-0.5614
Measurement_W80_L50	0.1000	-0.6188
Measurement_W100_L50	0.1000	-0.6362
Measurement_W30_L100	0.1000	-0.9798
Measurement_W50_L100	0.1000	-1.0817
Measurement_W80_L100	0.1000	-1.2815
Measurement_W100_L100	0.1000	-1.3269

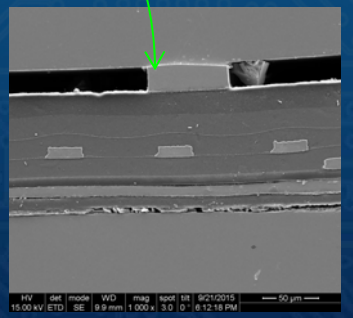
FormFactor Ex. 1031, p. 42

FormFactor v. Technoprobe
IPR2024-00933

Signal Integrity on Probe Card

- **Concept of Circuit Design on Space Transformer (STF)**





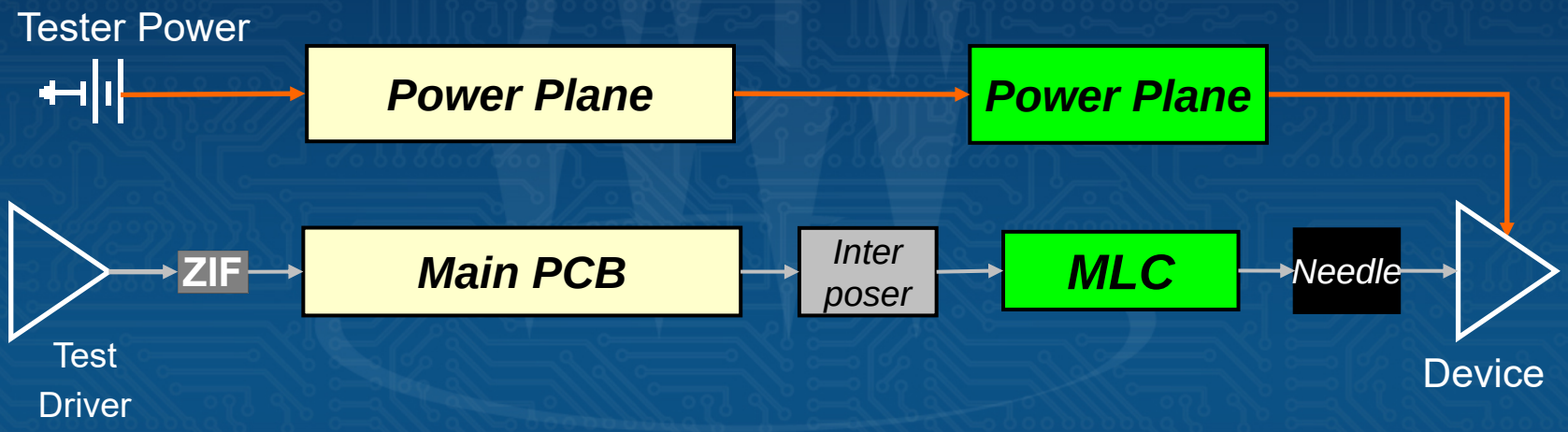
- STF consists of Universal MLC and Polyimide Thin Film.
- Polyimide Circuit is made by MEMS Process.
- MEMS Structure is stacked up after Polyimide Circuit Process.

FormFactor Ex. 1031, p. 43

FormFactor v. Technoprobe
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Signal Integrity on Probe Card

- **Simulation Conditions for Probe Card**



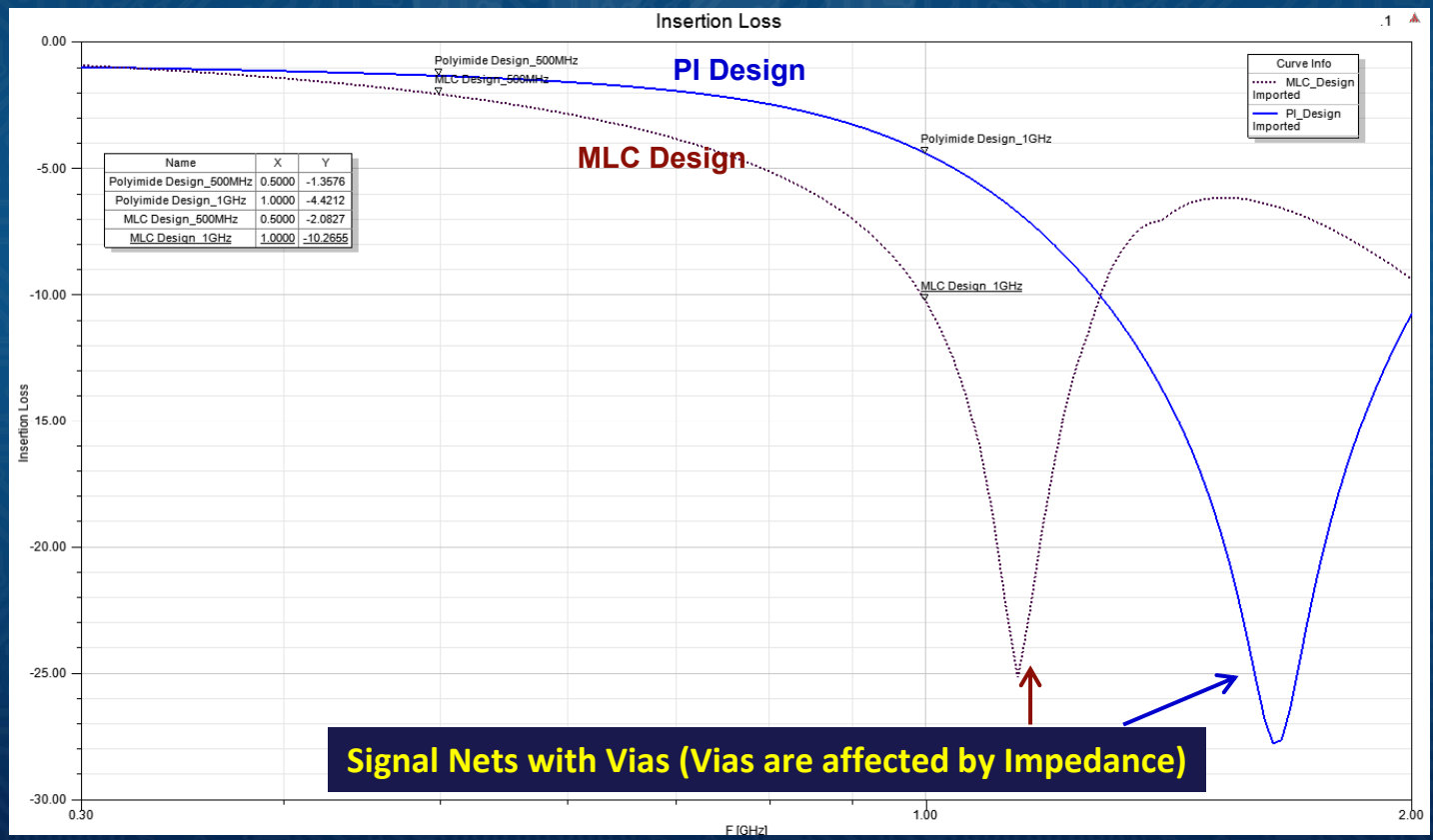
- Input Voltage : 1.1V
- Data : IO Ch.@Memory
- Data Rate : 100Mbps~1000Mbps (50MHz~500MHz)
- Factors : MLC Design vs PI Design on Probe Card
- Simulation Tool : SI Designer @ ANSYS

FormFactor Ex. 1031, p. 44

FormFactor v. Technoprobe
IPR2024-00933

Signal Integrity on Probe Card

- **Insertion Loss (Simulation)**
  - Analysis of MLC Circuit Design vs PI Circuit Design on Probe Card
  - MLC Circuit Design -2.08dB vs PI Circuit Design -1.35dB@500MHz



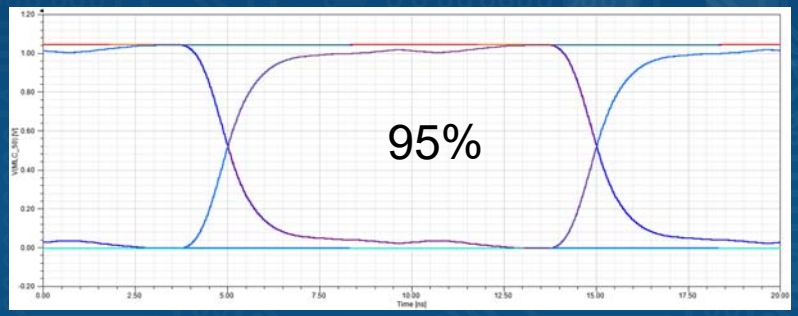
FormFactor Ex. 1031, p. 45

FormFactor v. Technoprobe
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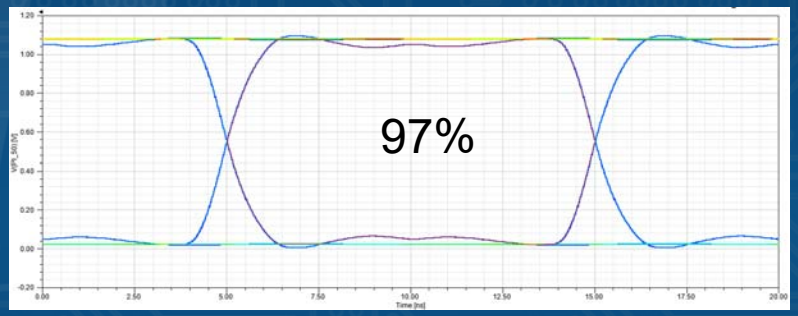
Signal Integrity on Probe Card

- **Eye Diagram (Simulation)**
  - Analysis of MLC Circuit Design vs PI Circuit Design on Probe Card
  - Eye-Opening : 95%~97%@50MHz, 93%~95%@100MHz

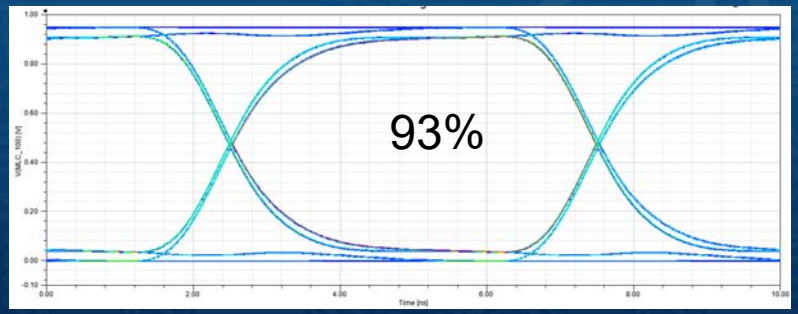
MLC Design : 50 MHz



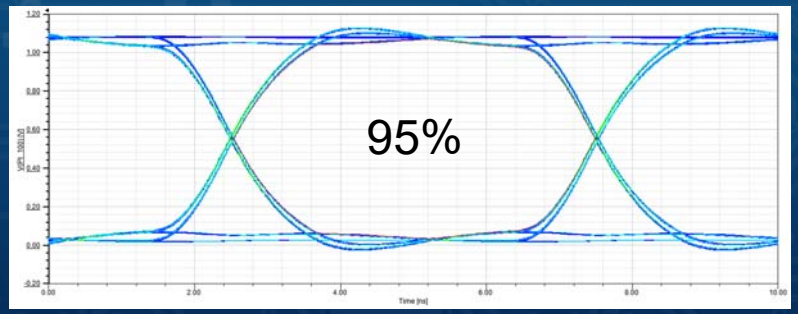
PI Design : 50 MHz



MLC Design : 100 MHz



PI Design : 100MHz



FormFactor Ex. 1031, p. 46

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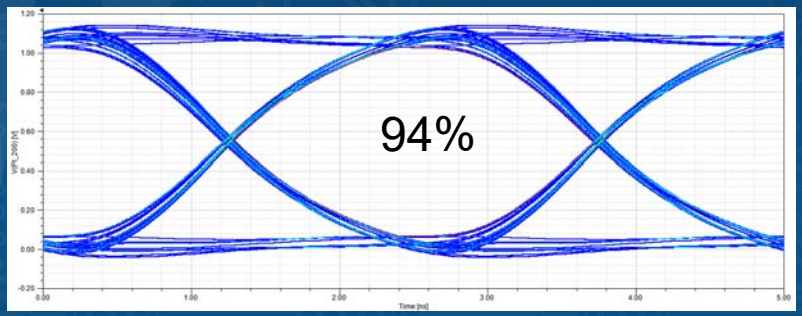
Signal Integrity on Probe Card

- **Eye Diagram (Simulation)**
  - Analysis of MLC Circuit Design vs PI Circuit Design on Probe Card
  - Eye-Opening : 90%~94%@200MHz, 51%~61%@500MHz

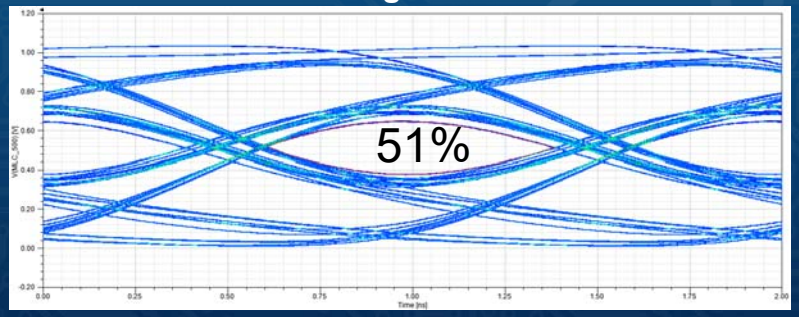
MLC Design : 200 MHz



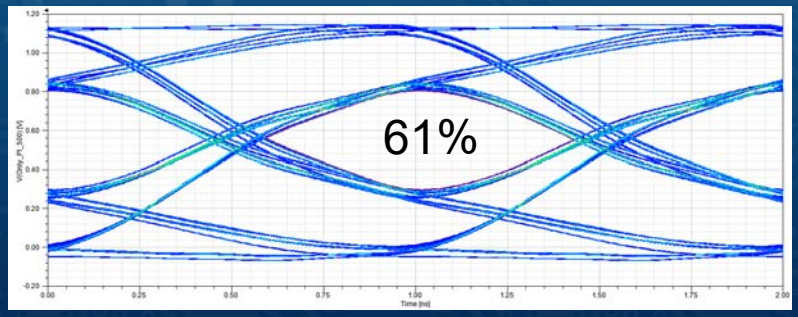
PI Design : 200 MHz



MLC Design : 500 MHz



PI Design : 500 MHz



FormFactor Ex. 1031, p. 47

FormFactor v. Technoprobe
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Summary

- Basic Study for Polyimide Circuit Design was Performed and its Electrical Characteristics have been checked.
- Impedance of Circuit Design using Polyimide Thin Film can be Controlled by changing Trace Geometry.
- Signal integrity was analyzed using two kinds of Design Concept on Probe Card.

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Future Works

- The Electrical Characteristics for Power integrity on Probe Card

- Analysis of Power impedance using Polyimide Thin Film
- Analysis of Effect for Decoupling Capacitor
- Analysis of Power Noise as Ground Type(Mesh & Plane)

FormFactor Ex. 1031, p. 49

FormFactor v. Technoprobe
IPR2024-00933

Acknowledgements



- Sang-Kyu Yoo
- Joon-Yoon Kim



- Yong-Ho Cho
- Sung-Mo Kang



- Jong-Kwan Yook

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Thanks for Your Attention !

FormFactor Ex. 1031, p. 51

FormFactor v. Technoprobe
IPR2024-00933

SW Test Workshop
Semiconductor Wafer Test Workshop

A proposal of a new probe head design in vertical probe cards for low crosstalk and PDN impedance



Kyung Hyun Chang
Hyun Min Kim
Willtechnology

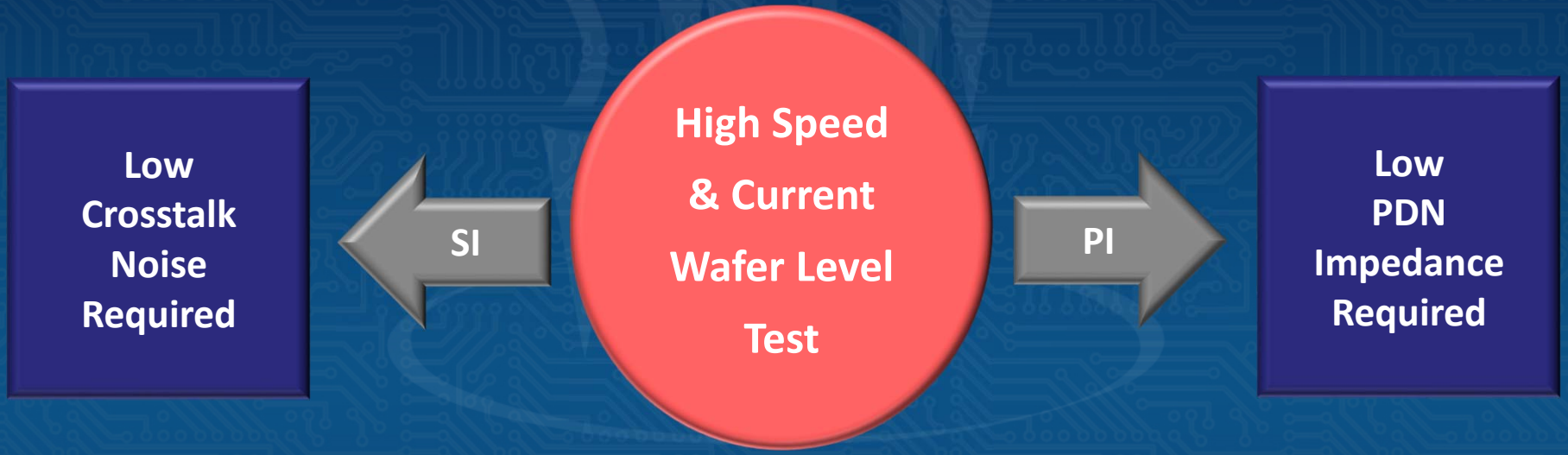
June 5-8, 2016

Overview

- **Background**
- **Low Crosstalk Probe Head**
  - Proposed structure of needle for crosstalk reduction
  - Simulation & Measurement result
- **Low – Z Probe Head**
  - Proposed structure of needle for PDN Impedance reduction
  - Simulation & Measurement result
- **Conclusion & Future work**

FormFactor Ex. 1031, p. 53
FormFactor v. Technoprobe
IPR2024-00933

Background

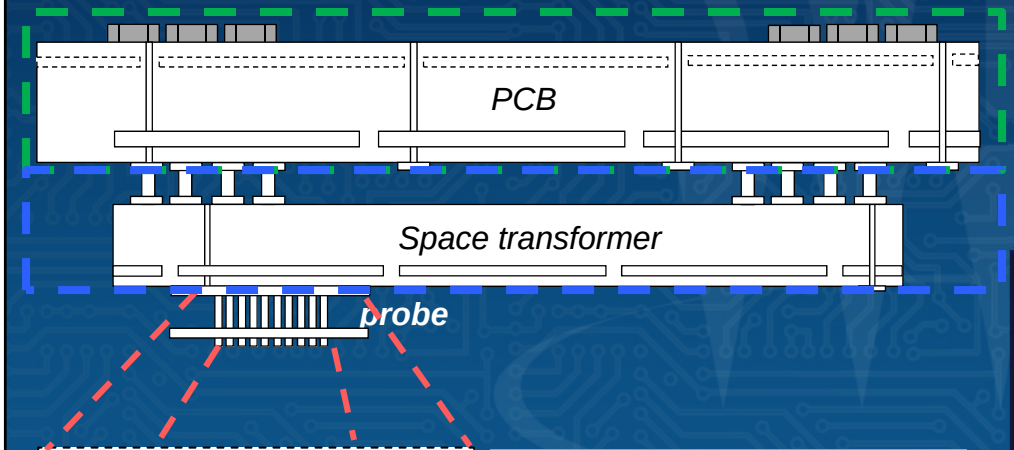


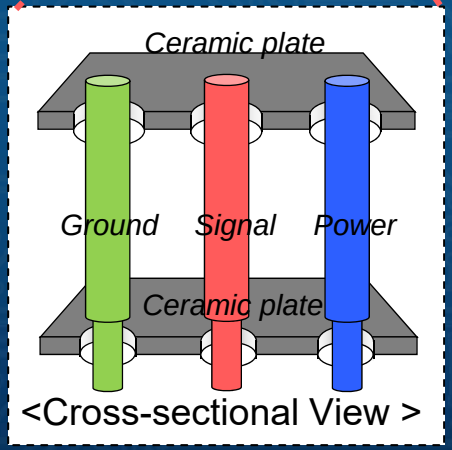
- SI & PI should carefully be considered in high speed / current wafer test.
- Both low crosstalk and PDN impedance are highly desirable for improvements in SI / PI.

FormFactor Ex. 1031, p. 54
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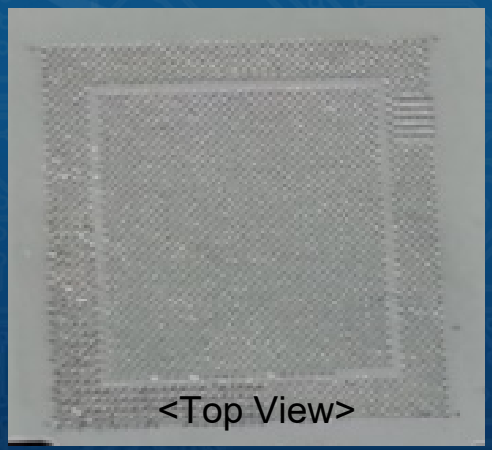
Background

- **Vertical Probe Card Structure**





<Cross-sectional View >



<Top View>

< Current Probe Head Structure >

SI/PI Improvement

PCB

•Usage of Low Permittivity Materials
(ex. FR4 → Nelco)
•Back drill

STF

•Usage of High Conductivity and Low Permittivity Materials
(ex. MLC → MLO)

Probe Head

• Difficulties in SI/PI improvement in its current structure

How does a probe head affect SI / PI ?

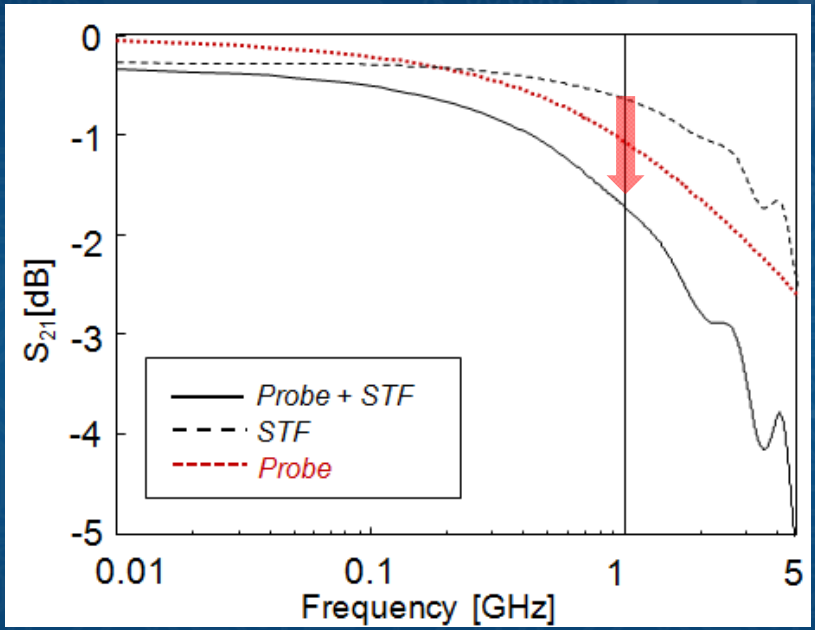
FormFactor Ex. 1031, p. 55

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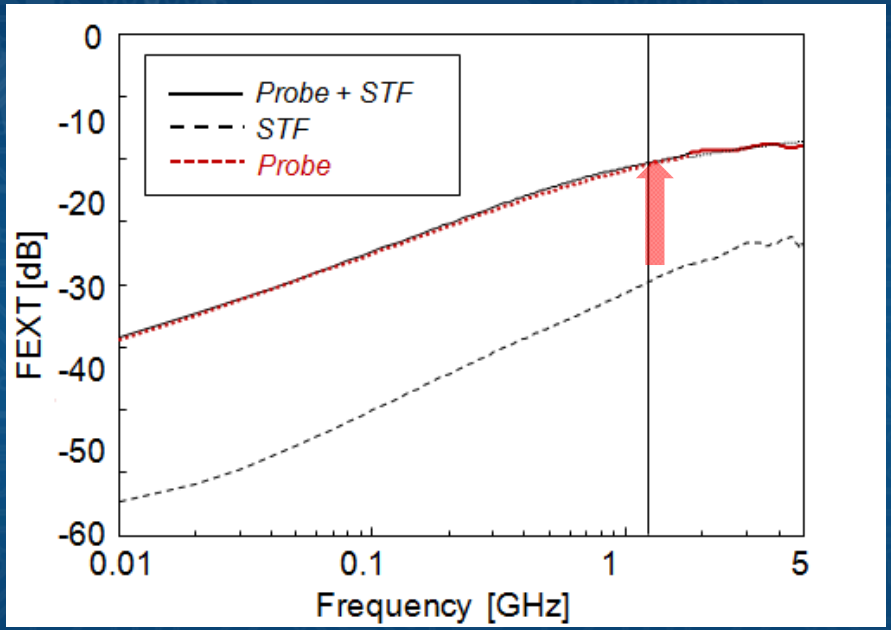
Background

- **Degradation of SI due to Probe Head**

[Attenuation of probe card]



[Far-end crosstalk of probe card]



- The probe brings about the dominant loss and the far-end crosstalk of the test signals.
- It is necessary to reduce the frequency dependent loss and far-end crosstalk of a probe in test channel of vertical probe card.

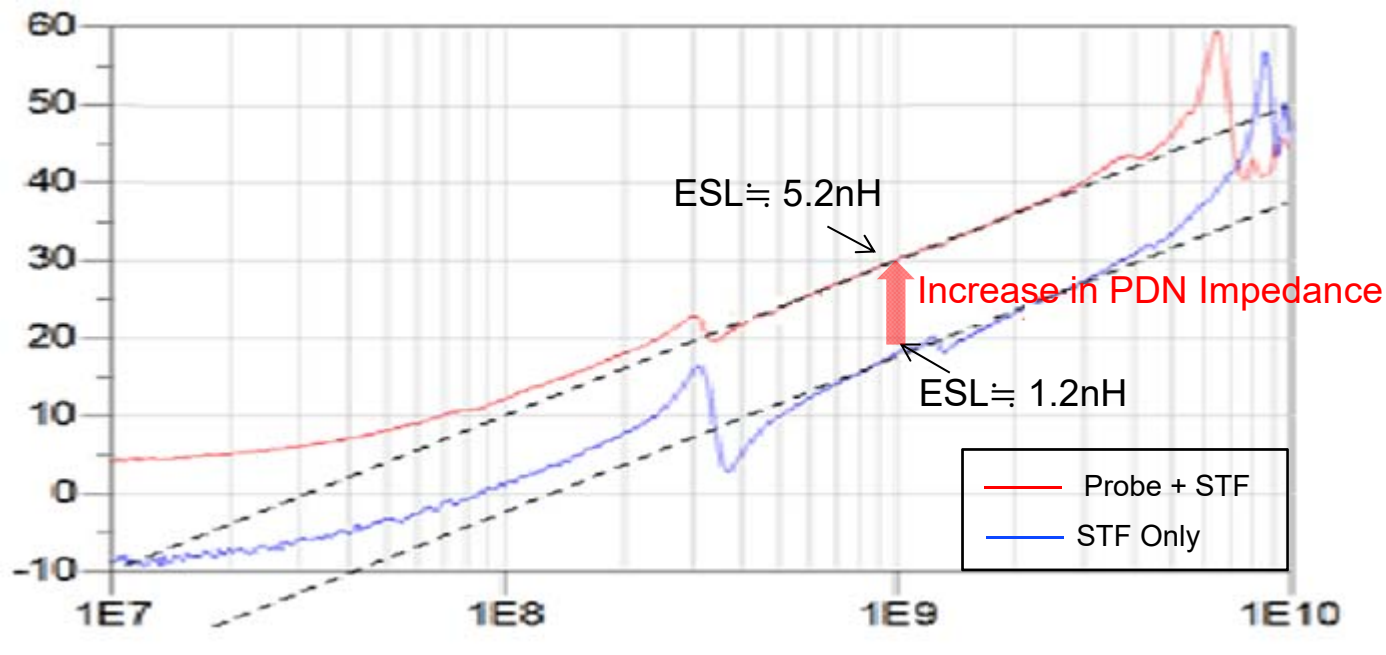
FormFactor Ex. 1031, p. 56

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Background

- **Degradation of PI due to Probe Head**

[Z11 of probe card]



- Increased in inductance by 4nH due to the effect of probe head
- Degradation of PDN impedance from the increased probe inductance

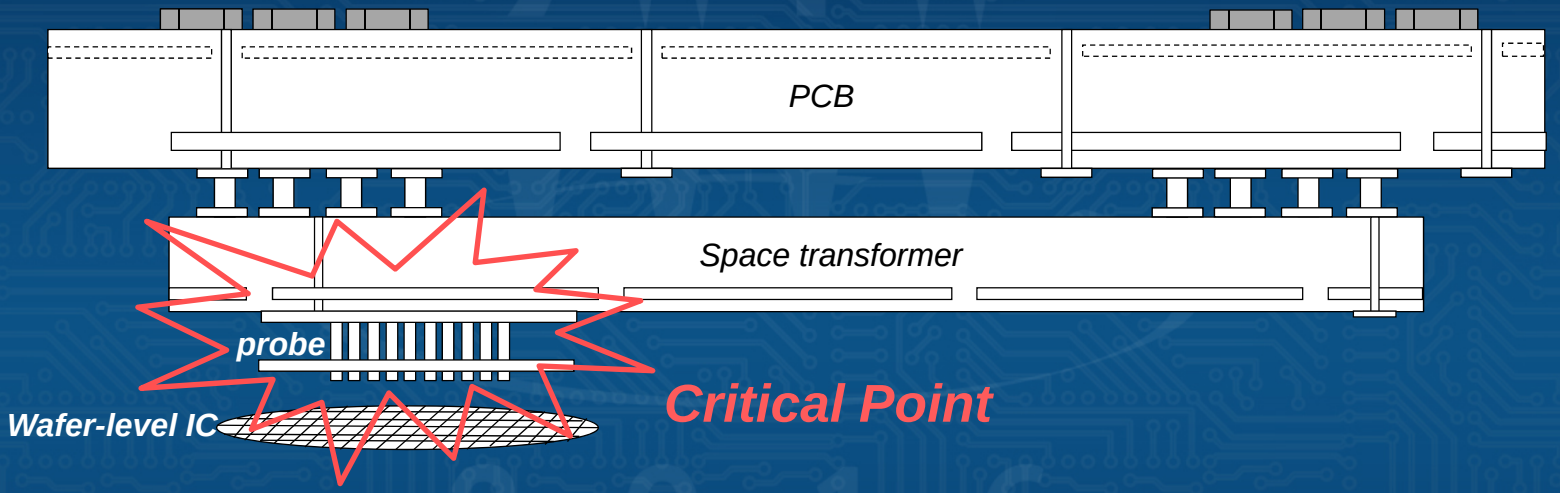
FormFactor Ex. 1031, p. 57

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Background

- **Room for improvement**

< Schematic diagram of the vertical probe cards >

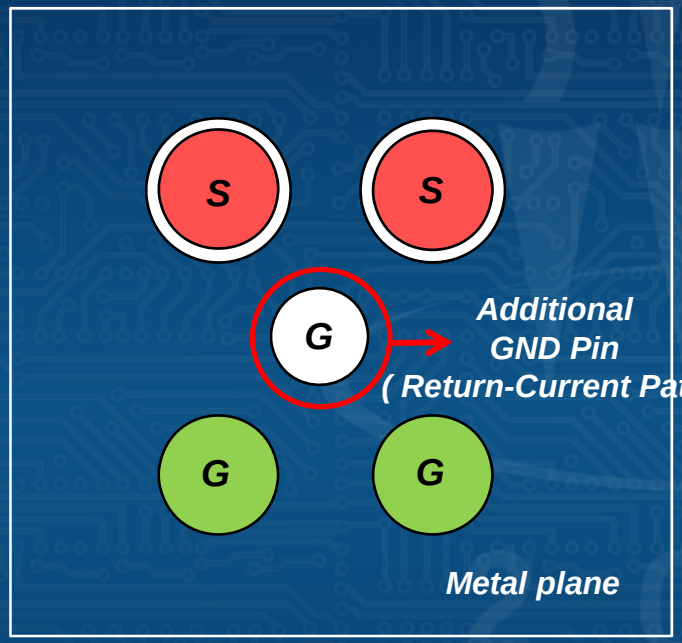




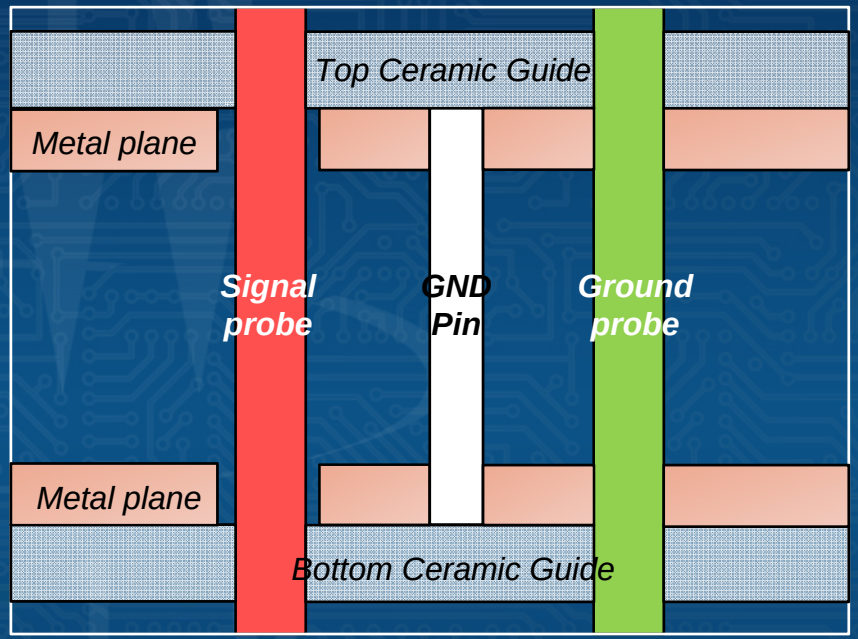
FormFactor Ex. 1031, p. 58
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Low X-talk Probe Head

- **Proposed structure of probe head for crosstalk reduction**



<Top View>



<Cross-sectional View>

- Insertion of metal planes and ground pins for the proposed design
- The ground pins provide return-current paths for signal probes.

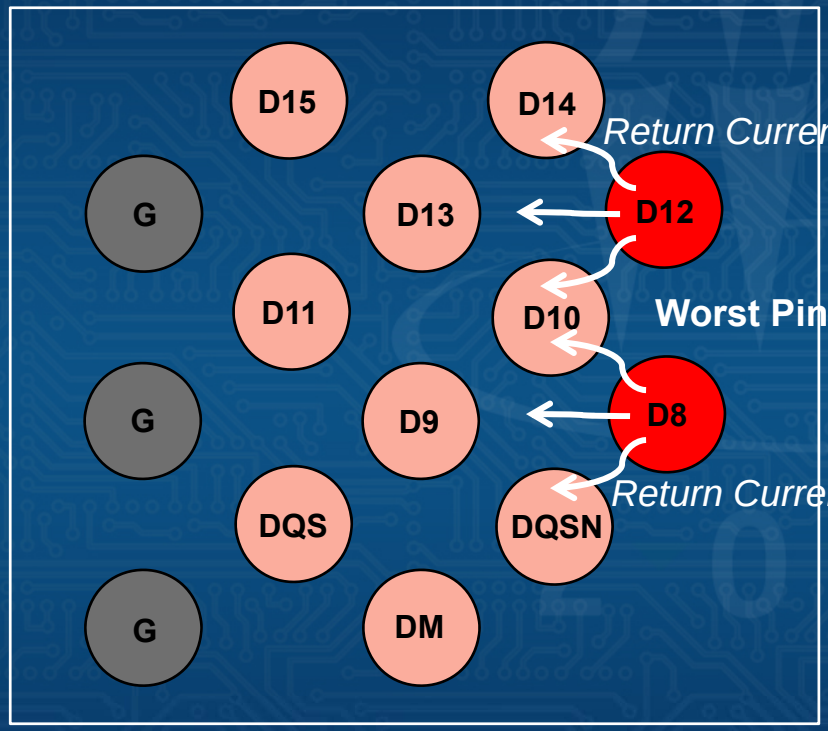
FormFactor Ex. 1031, p. 59

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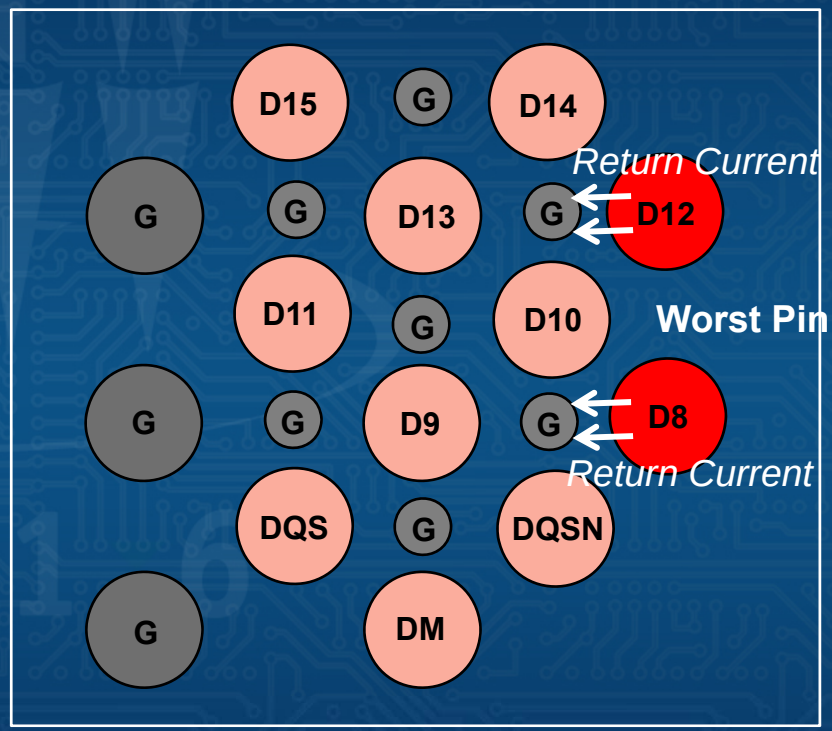
Low X-talk Probe Head

- **Proposed structure of probe head for crosstalk reduction**

[Pin assignment of AP on wafer]



[Proposed insertion of additional pin on PH]



- Signal probes that are far from GND may influence the signal integrity of the others.
- The inserted GND guard pin acts as return-current paths for signal pins

  → Suppressed noise coupling among the signal probes

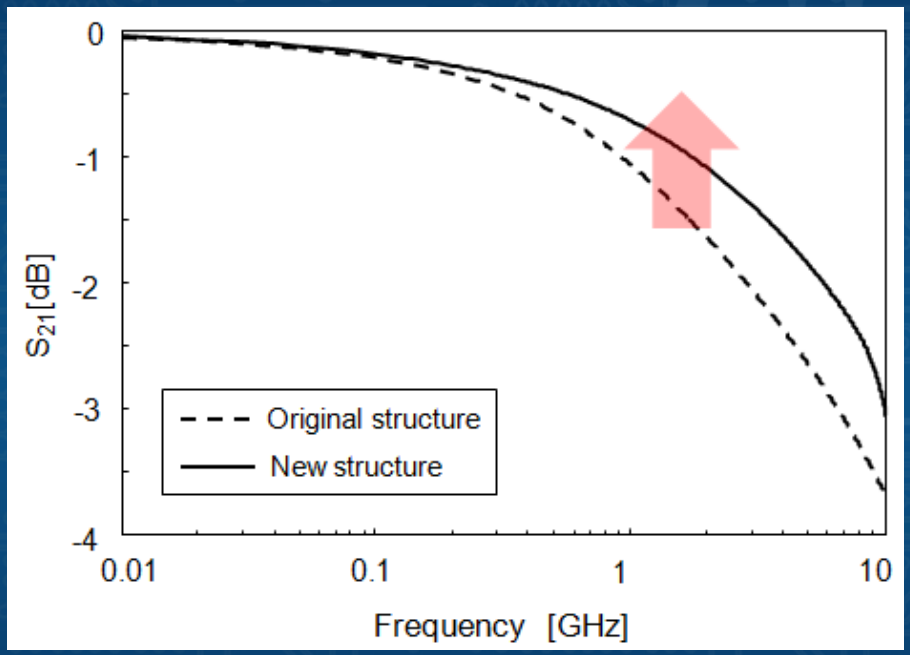
FormFactor Ex. 1031, p. 60

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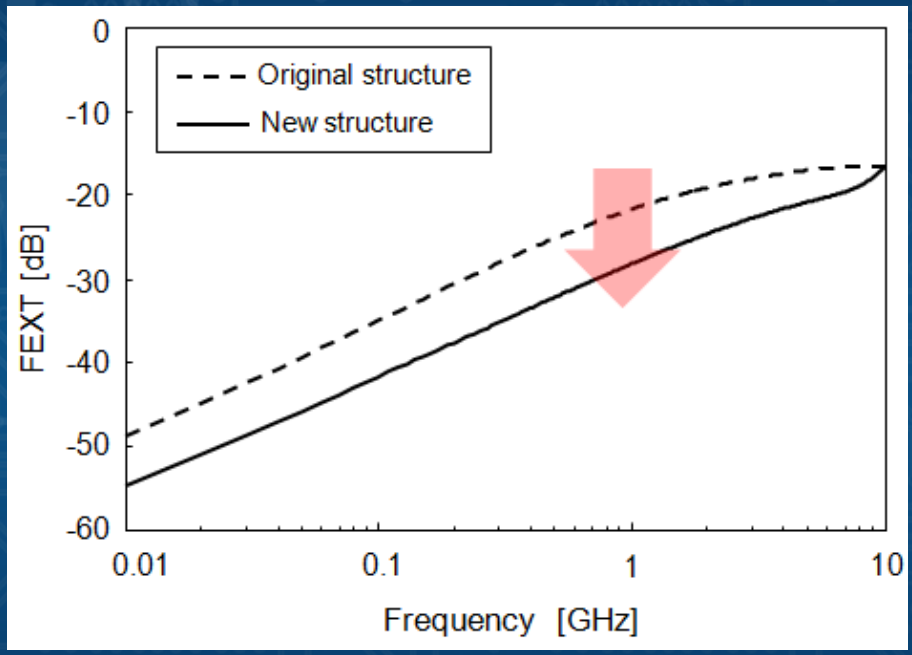
Low X-talk Probe Head

- **Comparison Far-end crosstalk (SI Simulation Result)**

[Attenuation of probe card]



[Far-end crosstalk of probe card]



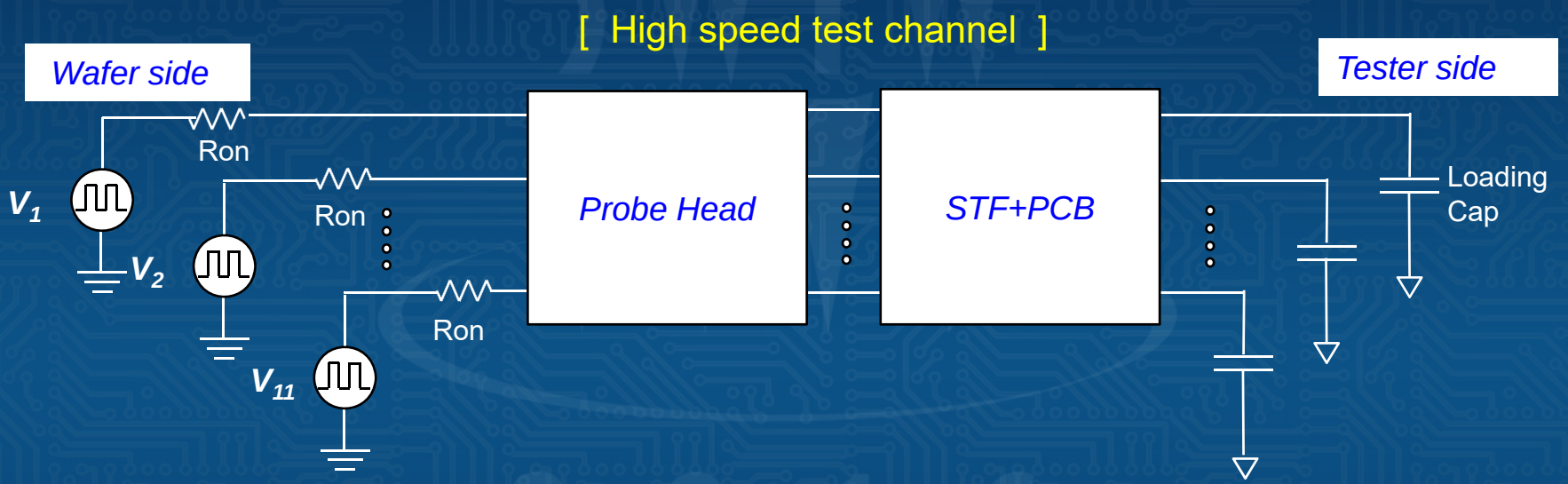
- Reduced Insertion loss (S21)
- Reduced Far-end crosstalk (FEXT)

FormFactor Ex. 1031, p. 61

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Low X-talk Probe Head

- **Eye-Diagram Simulation Environment**



- Simulation Setup

- Input Voltage : 1.1 V
- Data rate : 3200 Mbps
- Rise / Fall Time : UI/4
- Turn-on resistance : 50 ohm
- Data pattern : PRBS 2^5
- Loading Capacitance : 2pF

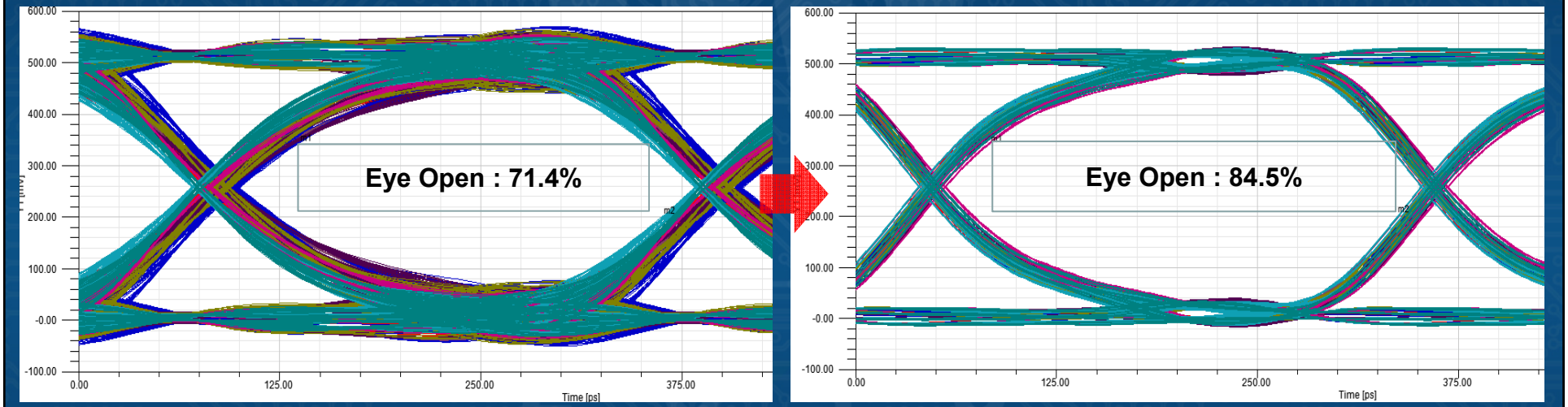
FormFactor Ex. 1031, p. 62

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Low X-talk Probe Head

- **Comparison Eye Diagram (Eye Simulation Result)**

< Eye Diagram of probe card – Data rate : 3.2Gbps >



- Larger eye open as a result of reduced crosstalk noise
- The simulation results show that the improvement in SI has been achieved.

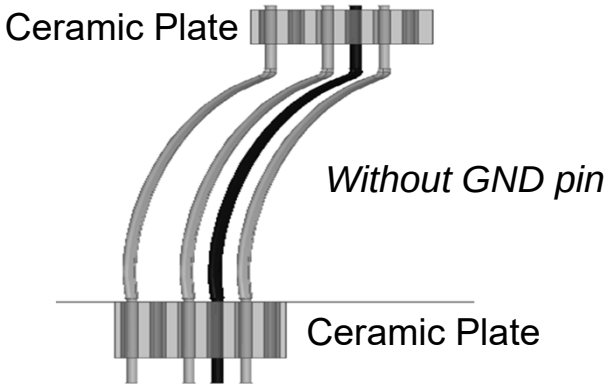
FormFactor Ex. 1031, p. 63

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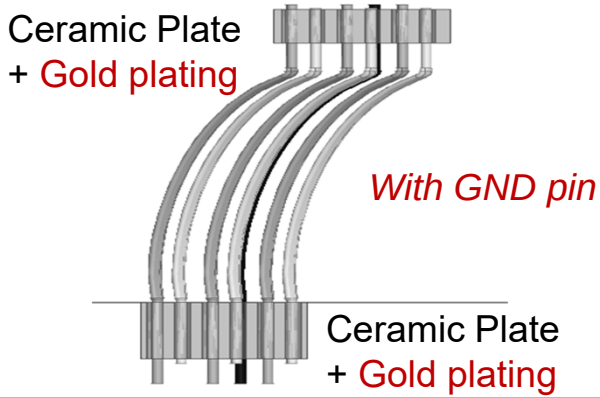
Low X-talk Probe Head

- **Probe Head Eye Diagram Measurement Environment**

< Original Probe Head >



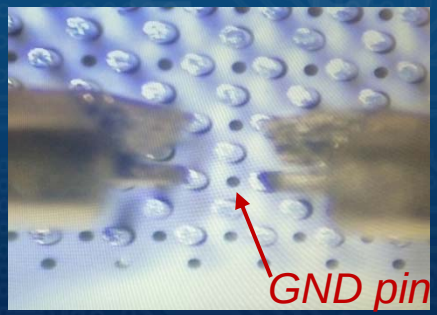
< Low X-talk Probe Head >



< Original PH >



< Low X-talk PH >



Eye-diagram measurement with Crosstalk effects

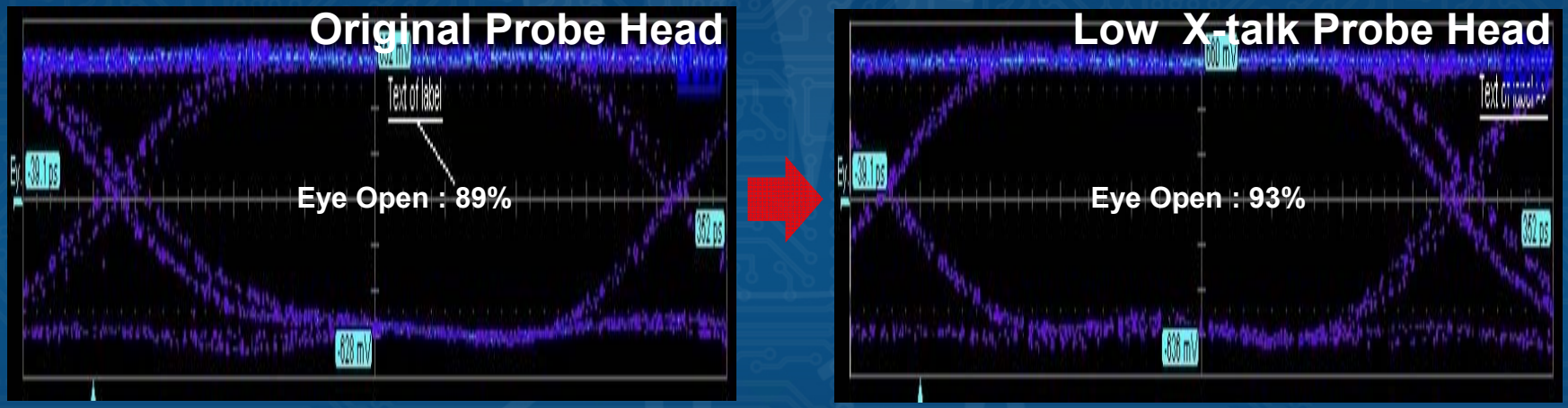
FormFactor Ex. 1031, p. 64

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Low X-talk Probe Head

- **Comparison Eye Diagram (Eye Measurement Result)**

< Eye Diagram of Probe Head – Data rate : 3.2Gbps >



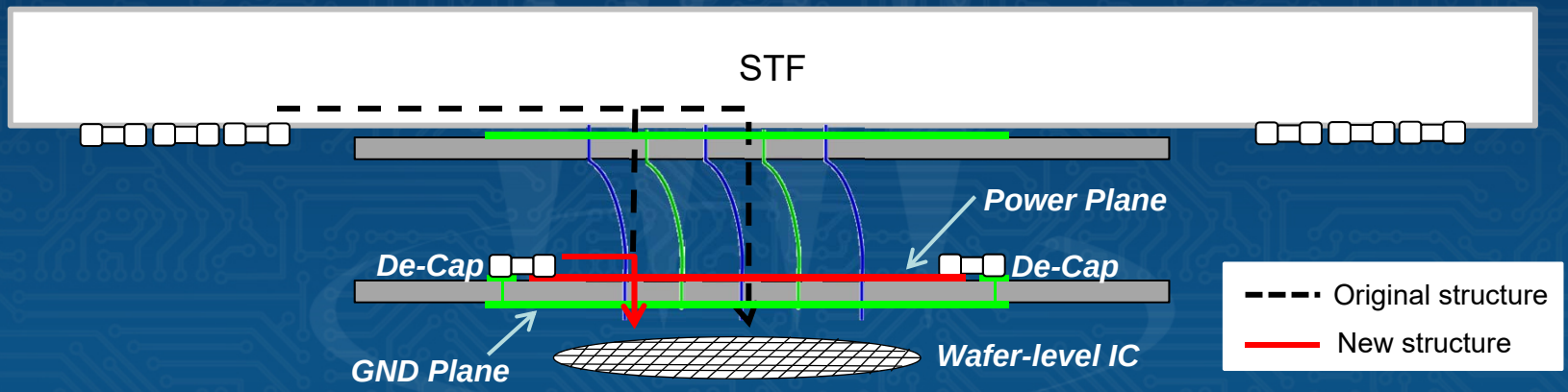
- In measurement, a minor improvement can be seen as compared to the simulation.
- Due to the restrictions, the probes near the GND pins (e.g. D11) can only be measured, which leads to the results only with the partial influence of x-talk.

FormFactor Ex. 1031, p. 65

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Low-Z Probe Head

- **Proposed structure of PDN Impedance reduction**



▪ Power, GND Plane and De-Cap added to Probe Head

PI Improvement

▪ Mitigation effect for increased PDN impedance due to addition of PH

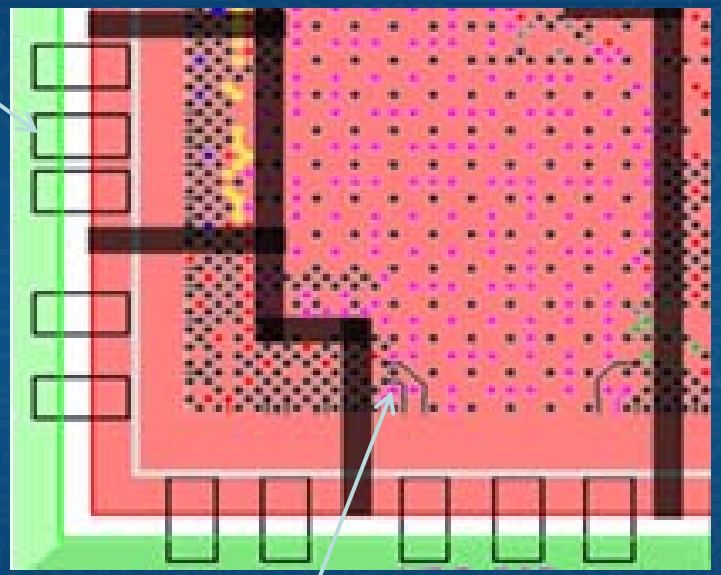
FormFactor Ex. 1031, p. 66

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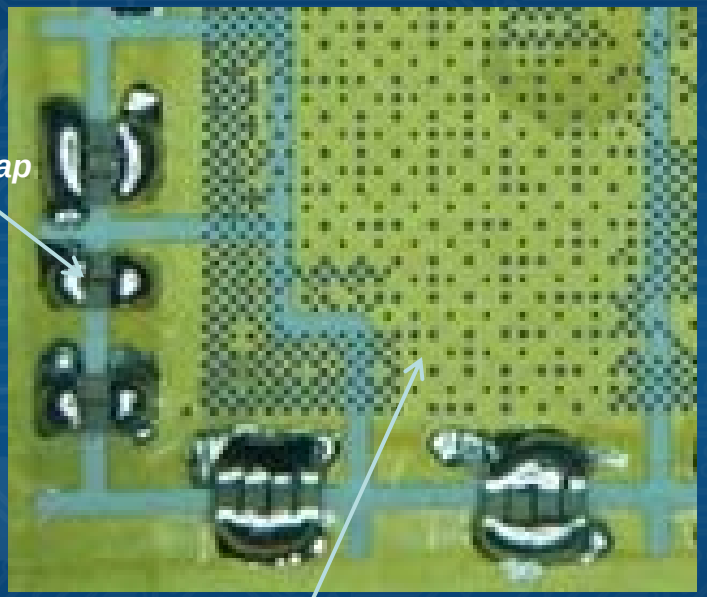
Low-Z Probe Head

- **Proposed structure of PDN Impedance reduction**

[Low –Z Probe Head Concept]



[Low –Z Probe Head in practice]



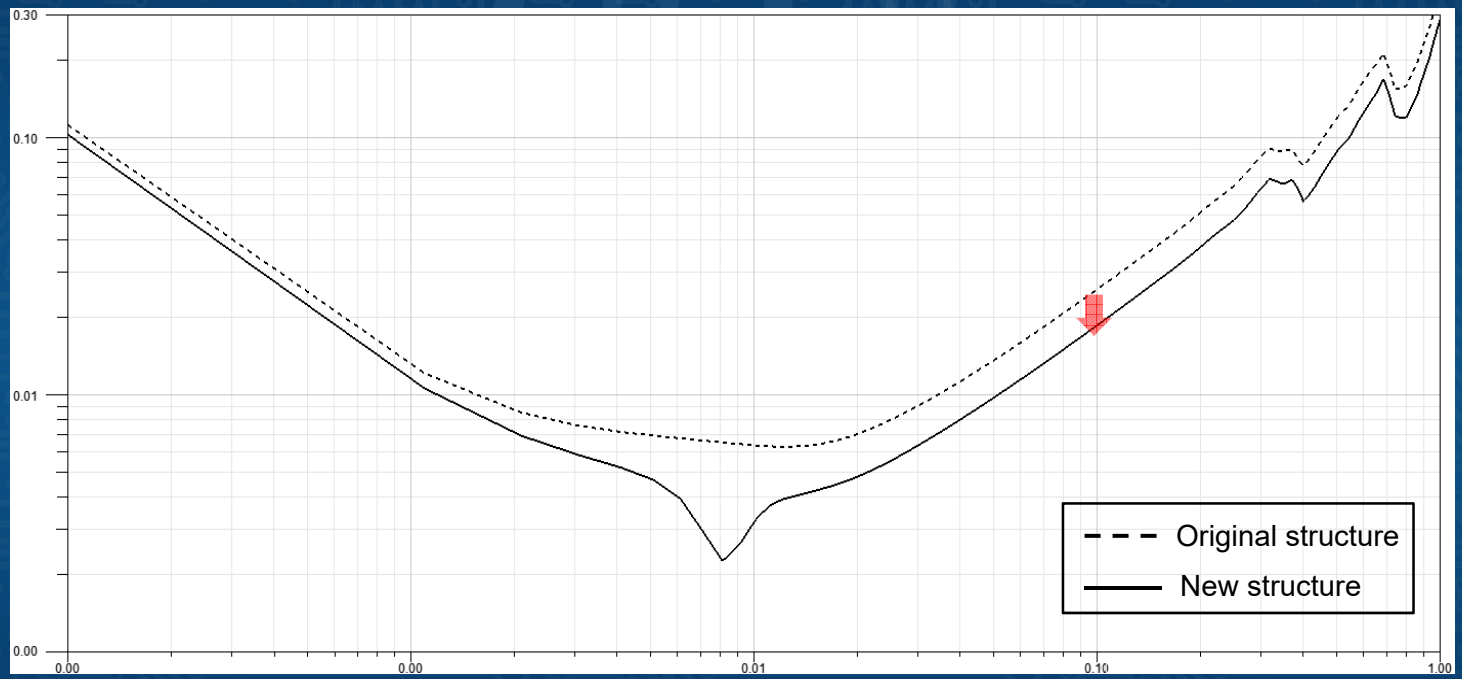
- Implementation of Power / GND planes through gold plating
- Capability of applying low-z concept to various powers through splitting the planes

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Low-Z Probe Head

- **Comparison PDN Impedance (PI Simulation Result)**

< Z11 Graph of probe card _Lumped Port PI Simulation >



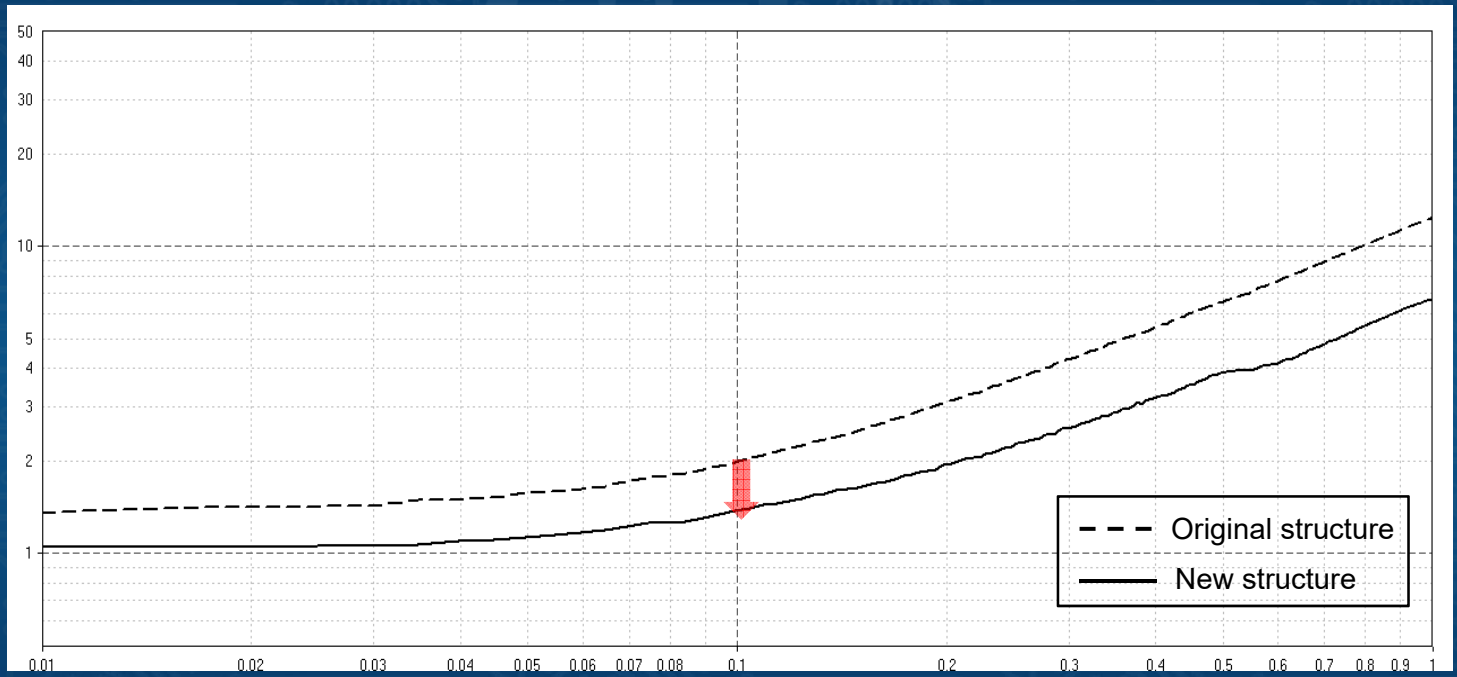
- Result of lumped port PI simulation
- Decrease in PDN Impedance (Z11) of Low-Z structure as compared to original (25% ↓)

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Low-Z Probe Head

- **Comparison PDN Impedance (PI Measurement Result)**

< Z11 Graph of probe card _1pin PI measurement >



- Result of 1-pin PI measurement
- Decrease in PDN Impedance (Z11) of Low-Z structure as compared to original (30% ↓)
- According to the results, decrease in PDN impedance has been observed.

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Conclusion & Future work

- SI & PI should carefully be considered in high speed / current wafer level test.
- A new structure with low Z & X-talk is required to compensate the SI & PI loss caused by the probe head
- SI ; Low x-talk among signal probes has been achieved through the new structure with additional GND pins
- PI ; Introducing P/G planes and decaps on probe head leads to lower power impedance
- Further research required to employ such strategy & concept for fine pitch products
- Thanks.

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SW Test Workshop
Semiconductor Wafer Test Workshop

Production Test RF Calibration for Multi-DUT Probe Cards: How to get the most accurate measurements

Daniel Bock, Ph.D.
Cascade Microtech

June 5-8, 2016

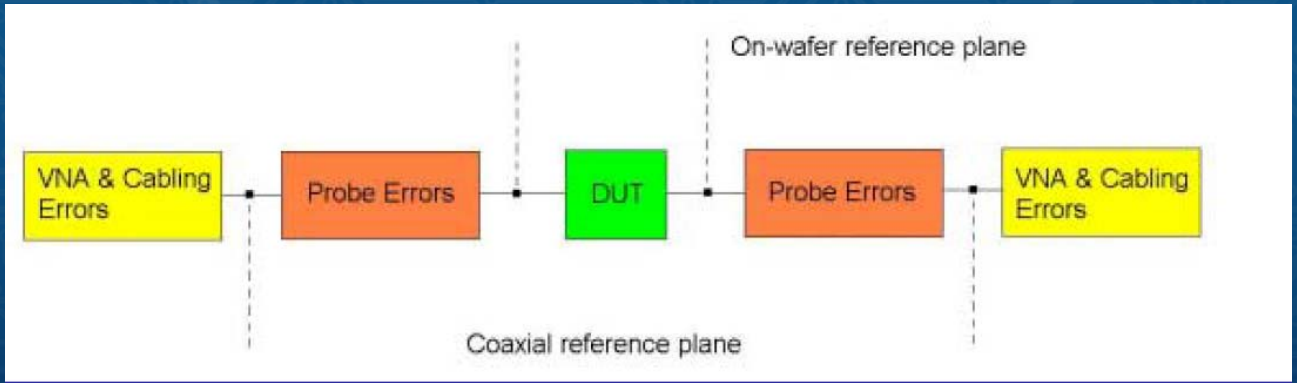
Overview

- What is Calibration?
- What are the differences between single site and multi-site calibration?
- Simulation investigation
- Summary

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Why do you need Calibration?

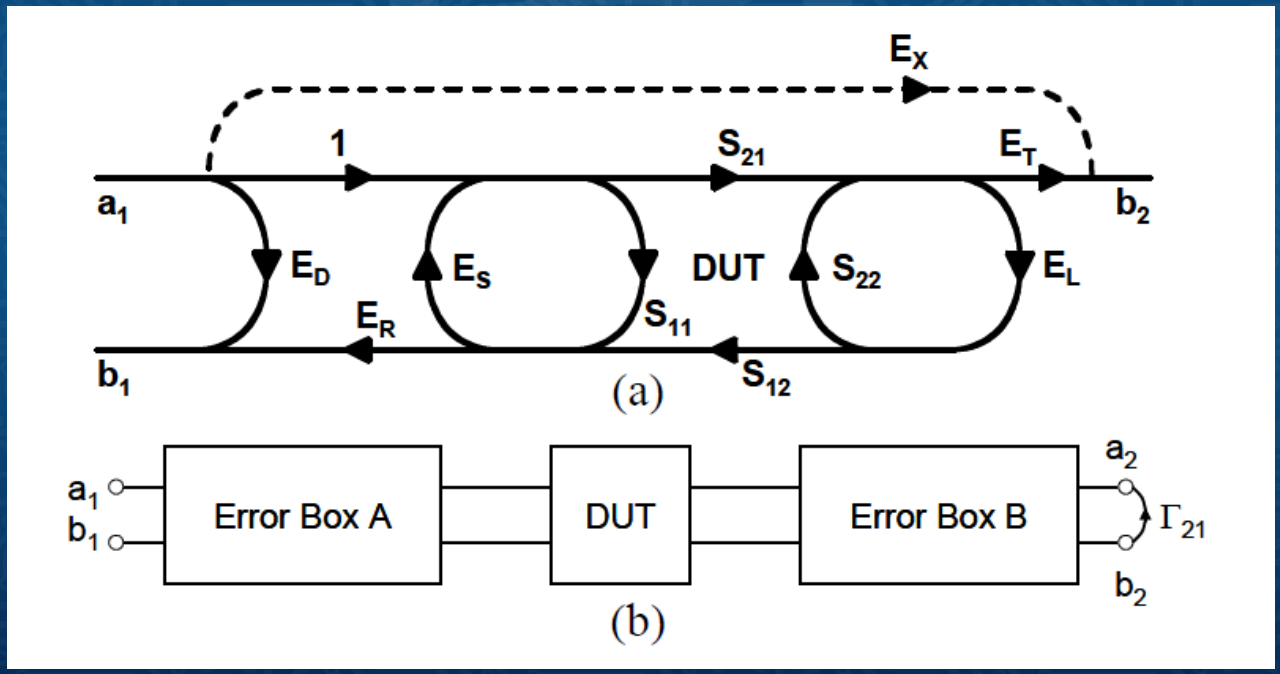
- **You want a guarantee that you are measuring your DUT and NOT your test equipment**
  - The Probes and cabling introduces errors
  - However, Calibration is able to remove those errors



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How does Calibration Work

- It characterizes the RF performance parameters of your test hardware
- Then mathematically remove the parameters



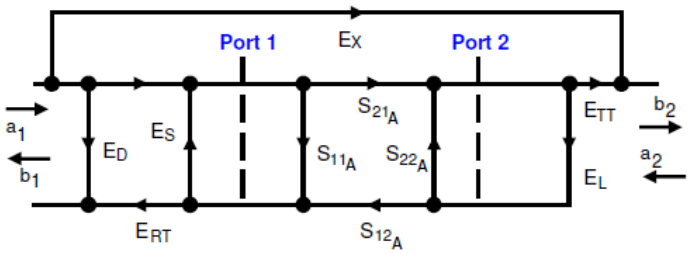
FormFactor Ex. 1031, p. 74

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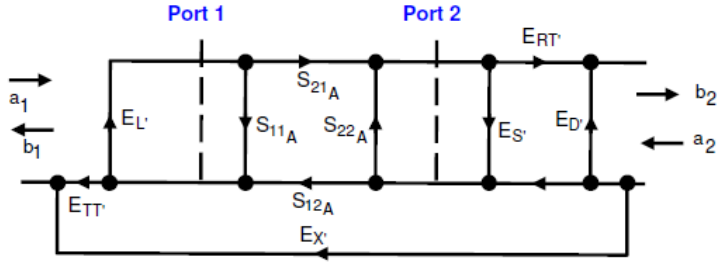
A Little Math….

Two-Port Error Correction

Forward model



Reverse model



E_D	= fwd directivity	E_L	= fwd load match
E_S	= fwd source match	E_{TT}	= fwd transmission tracking
E_{RT}	= fwd reflection tracking	E_X	= fwd isolation
$E_{D'}$	= rev directivity	$E_{L'}$	= rev load match
$E_{S'}$	= rev source match	$E_{TT'}$	= rev transmission tracking
$E_{RT'}$	= rev reflection tracking	$E_{X'}$	= rev isolation

- Each actual S-parameter is a function of all four measured S-parameters
- Analyzer must make forward *and* reverse sweep to update any one S-parameter
- Luckily, you don't need to know these equations to ***use*** network analyzers!!!

$$S_{11a} = \frac{(\frac{S_{11m}-E_D}{E_{RT}})(1+\frac{S_{22m}-E_{D'}}{E_{RT'}}E_{S'})-E_L(\frac{S_{21m}-E_X}{E_{TT}})(\frac{S_{12m}-E_{X'}}{E_{TT'}})}{(1+\frac{S_{11m}-E_D}{E_{RT}}E_S)(1+\frac{S_{22m}-E_{D'}}{E_{RT'}}E_{S'})-E_{L'}E_L(\frac{S_{21m}-E_X}{E_{TT}})(\frac{S_{12m}-E_{X'}}{E_{TT'}})}$$

$$S_{21a} = \frac{(\frac{S_{21m}-E_X}{E_{TT}})(1+\frac{S_{22m}-E_{D'}}{E_{RT'}}(E_{S'}-E_L))}{(1+\frac{S_{11m}-E_D}{E_{RT}}E_S)(1+\frac{S_{22m}-E_{D'}}{E_{RT'}}E_{S'})-E_{L'}E_L(\frac{S_{21m}-E_X}{E_{TT}})(\frac{S_{12m}-E_{X'}}{E_{TT'}})}$$

$$S_{12a} = \frac{(\frac{S_{12m}-E_{X'}}{E_{TT'}})(1+\frac{S_{11m}-E_D}{E_{RT}}(E_S-E_{L'}))}{(1+\frac{S_{11m}-E_D}{E_{RT}}E_S)(1+\frac{S_{22m}-E_{D'}}{E_{RT'}}E_{S'})-E_{L'}E_L(\frac{S_{21m}-E_X}{E_{TT}})(\frac{S_{12m}-E_{X'}}{E_{TT'}})}$$

$$S_{22a} = \frac{(\frac{S_{22m}-E_{D'}}{E_{RT'}})(1+\frac{S_{11m}-E_D}{E_{RT}}E_S)-E_{L'}(\frac{S_{21m}-E_X}{E_{TT}})(\frac{S_{12m}-E_{X'}}{E_{TT'}})}{(1+\frac{S_{11m}-E_D}{E_{RT}}E_S)(1+\frac{S_{22m}-E_{D'}}{E_{RT'}}E_{S'})-E_{L'}E_L(\frac{S_{21m}-E_X}{E_{TT}})(\frac{S_{12m}-E_{X'}}{E_{TT'}})}$$

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Calibration Substrates

- **A calibration substrate is used in order to characterize the measurement path**
  - Measure some combination of
    - Short
    - Open
    - Load
    - Thru



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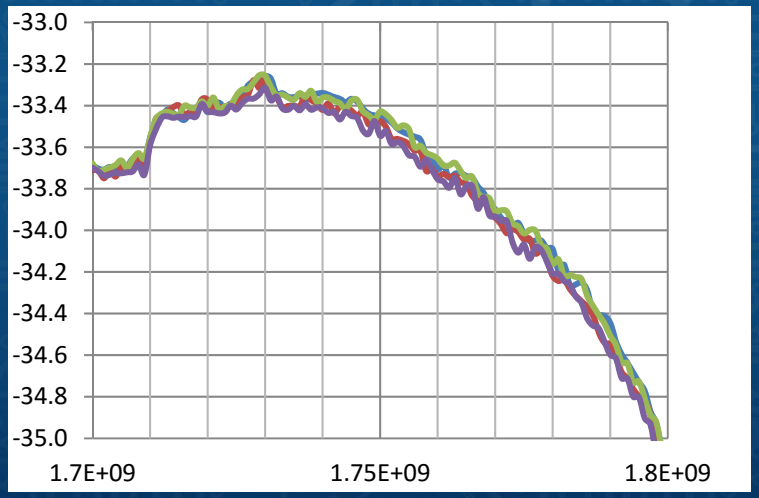
But what about Multi-DUT?

- **In order to improve Cost Of Ownership, many companies are moving to multi-DUT test**
  - Increase number of wafers tested per probe card
  - Increase speed of test with lower number of index steps
- **But now DUT are being tested with different measurement sites, leading to the requirement for site-to-site correlation**

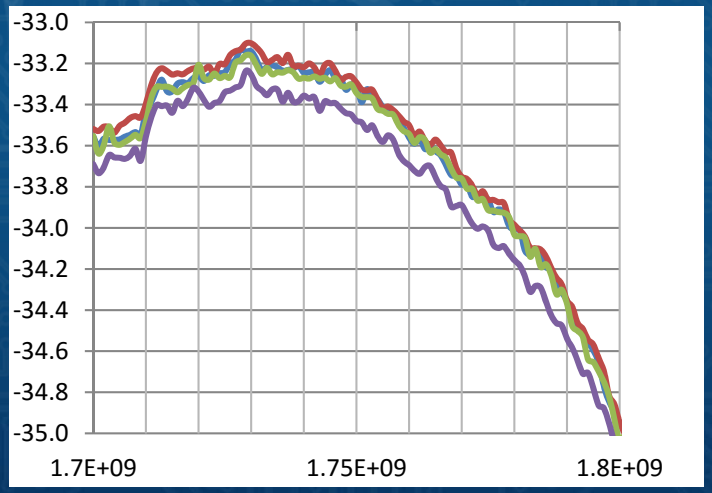
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Single Site Cal vs. Multi-site Cal

- Comparing a single site cal and a multi-site cal shows a bifurcation of the S-parameters
- Data indicates that the ISS using a multi-site cal has better correlation between sites on the same probe card measurement



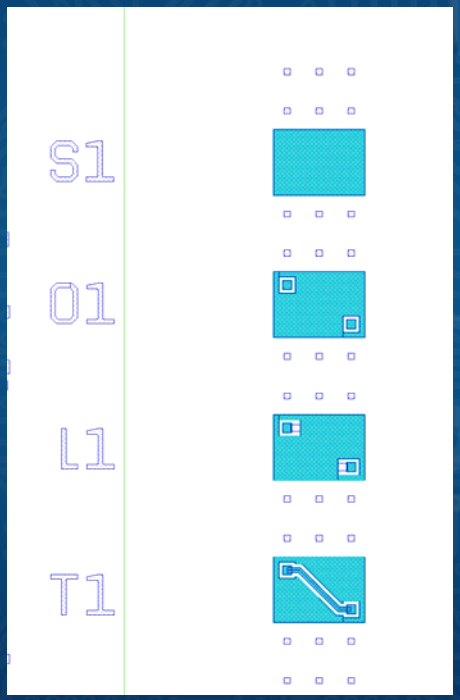
Multi-site Cal



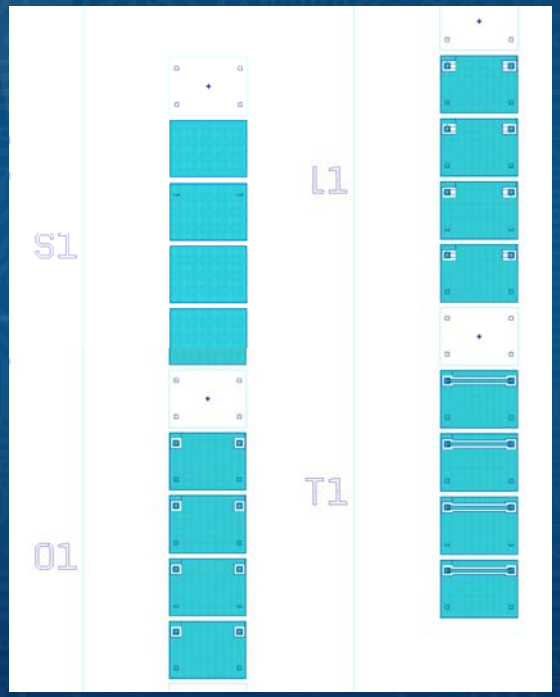
Single Site Cal

What is the difference in a single site layout and multi-site?

- Figure showing the state of the adjacent DIE location



Single Site Standards



4-site Standards

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Simulation Evaluation

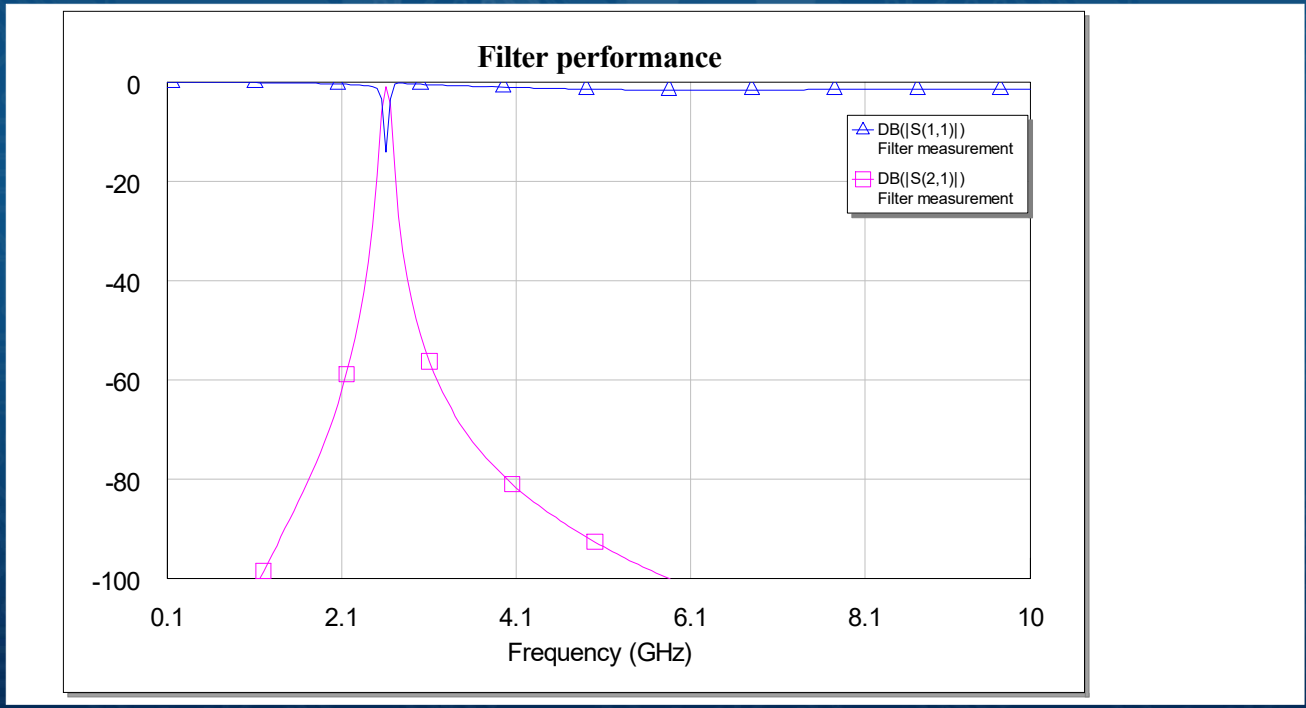
- **In order to investigate further, we used simulation to control all other factors**
- **Simulate two die with same ground return**
  - Comparison between two different scenarios
    - Look at error terms when both ports are controlled (multi-site cal)
    - Look at the error terms when only one port is controlled, but the other can be a random state (single site cal) which includes short, open, load

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Filter measurement data

- The filter is a simple bandpass, with a center frequency of 2.6 GHz, with a 3 dB width of 100 MHz



FormFactor Ex. 1031, p. 81

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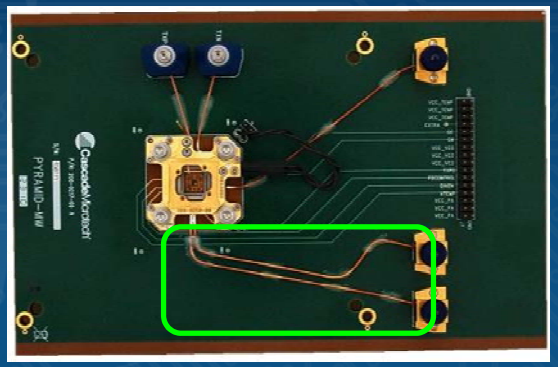
Cal Coefficients

- **In order to properly do SOLT calibration, we need to have cal coeff**
- **They were extracted using LRRM to calculate the values**
  - L-load = 215 pH
  - L-short = 208 pH
  - C-open = 19 fF
  - Thru length = 4.8 ps

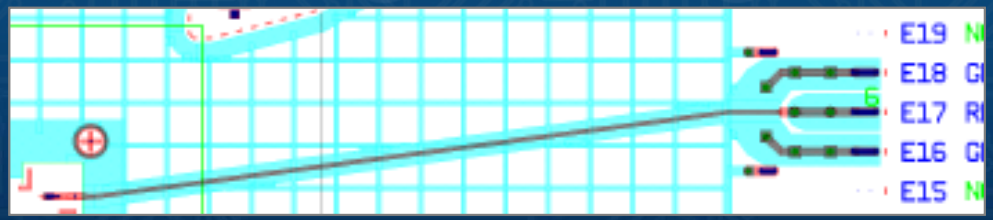
FormFactor Ex. 1031, p. 82
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Probe Card

- **The simulated probe card is modeled after a Pyramid Probe**
  - 50 mm 0.031” semi-rigid coax



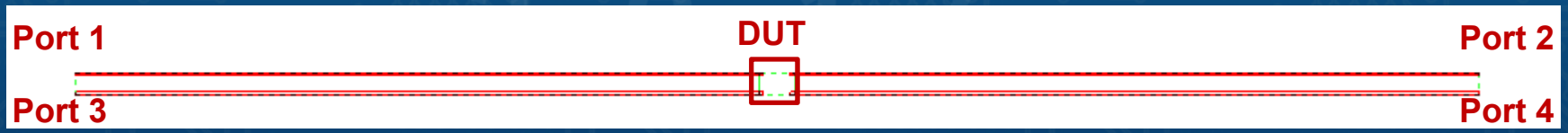
  - 10 mm microstrip transmission line on the Pyramid Probe



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Membrane Layout

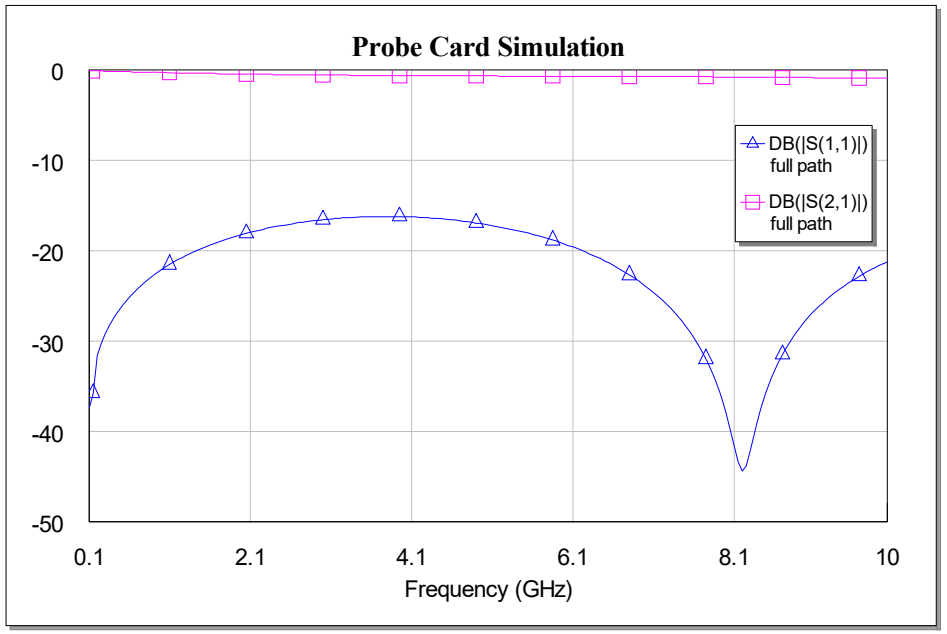
- **The design has a two filter layout**
  - Each filter has a single input/output pair
    - DUT 1 is port 1, 2
    - DUT 2 is port 3, 4
  - Shared ground return



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Simulated performance of a single Channel

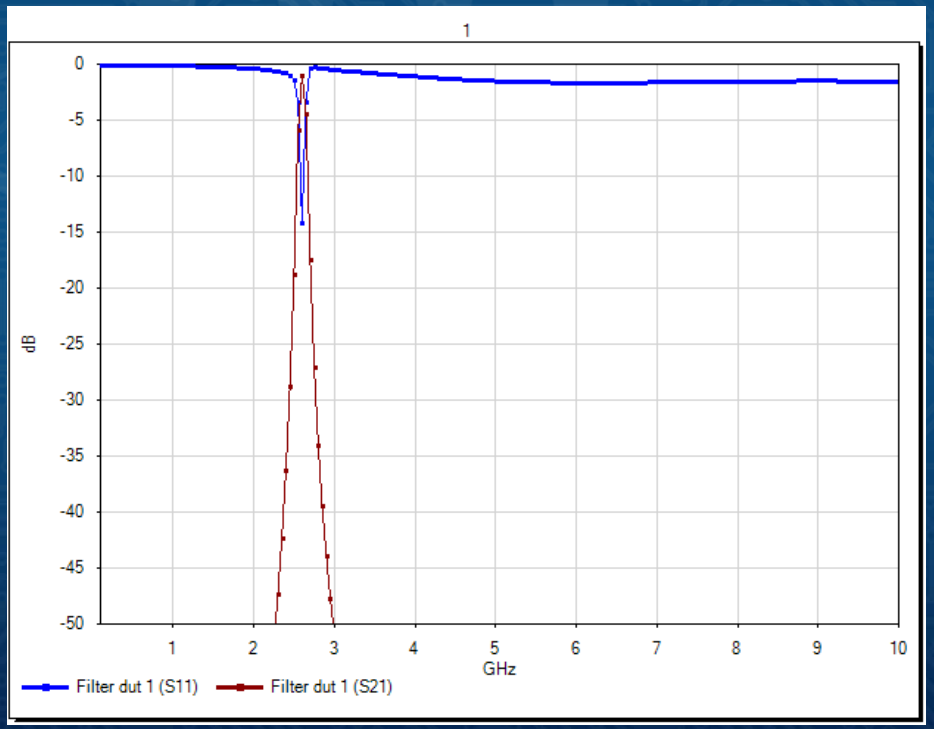
- **The simulated probe card meets the standard specification of a Pyramid Probe:**
  - < 3 dB insertion loss
  - > 10 dB return loss
  - Cross talk is better than 55 dB at 2.5 GHz



FormFactor Ex. 1031, p. 85
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Measurements before Calibration

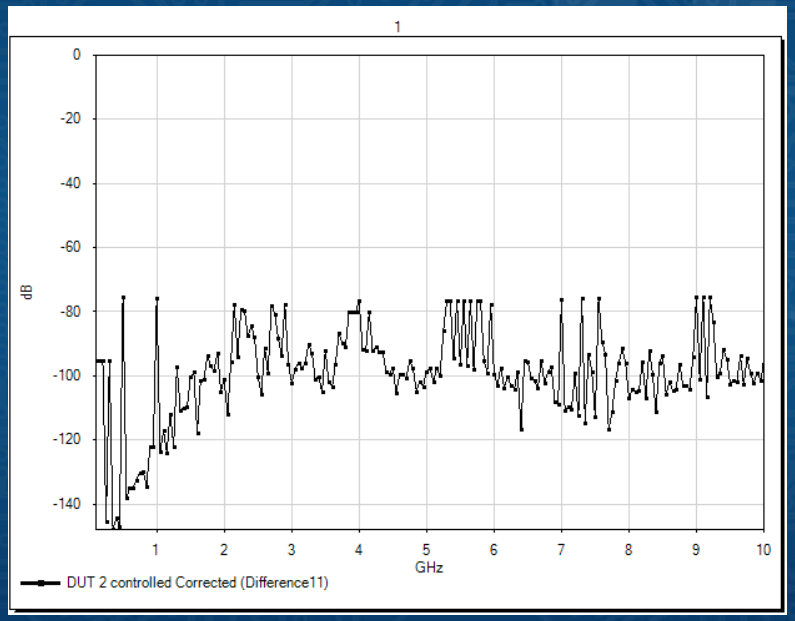
- **The measurements prior to calibration are identical in each DUT**
  - This is ideal scenario



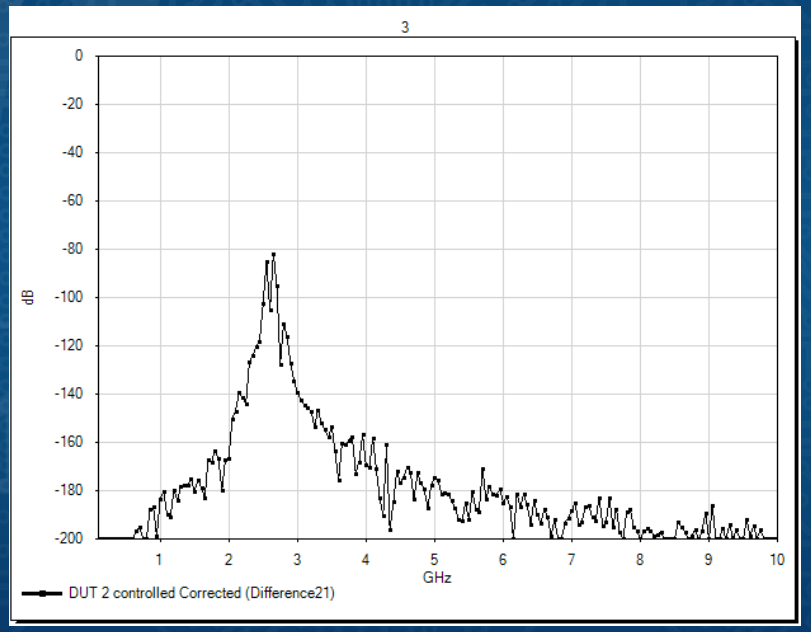
FormFactor Ex. 1031, p. 86
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After Calibration Controlled

- **Looking at the different between DUT 1 and DUT 2, the variation is in the noise**



Δ Return Loss (S11)



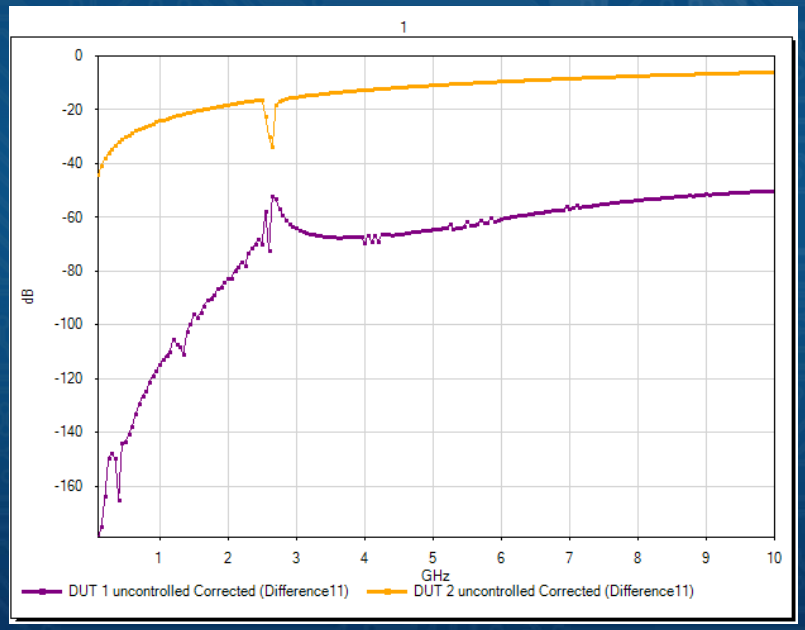
Δ Insertion Loss (S21)

FormFactor Ex. 1031, p. 87

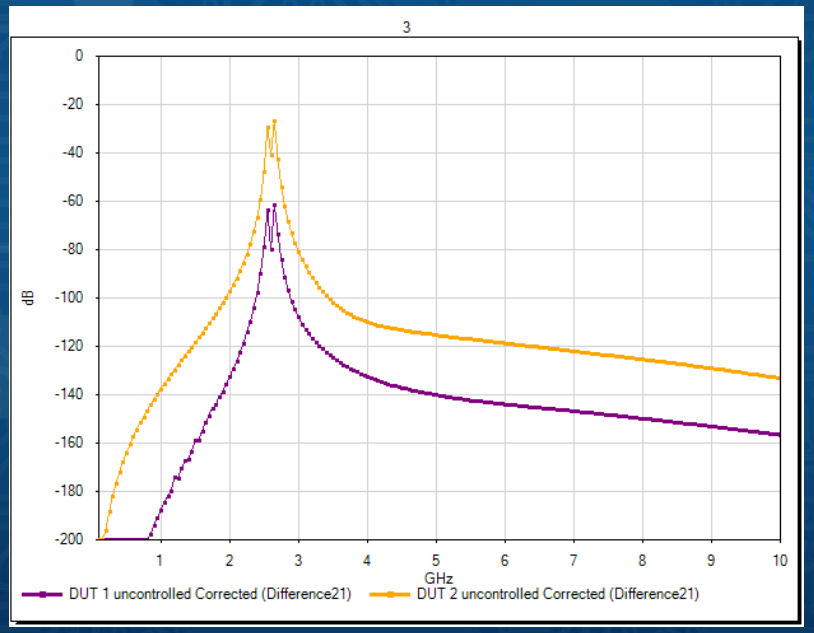
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After Calibration Uncontrolled

- **In the uncontrolled state for the unmeasured lines, it affects both sites, as well as making a bi-modal distribution**
  - Compared to DUT 1 from the controlled state



Δ Return Loss (S11)

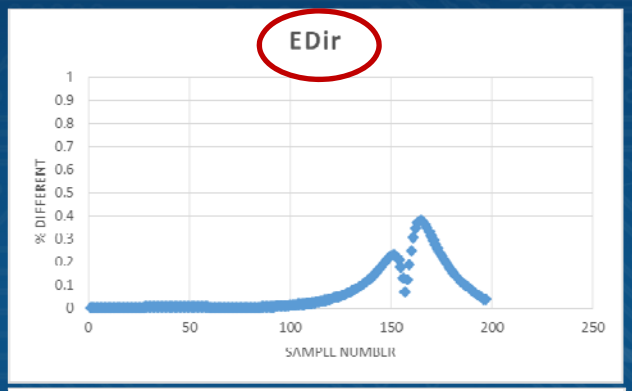


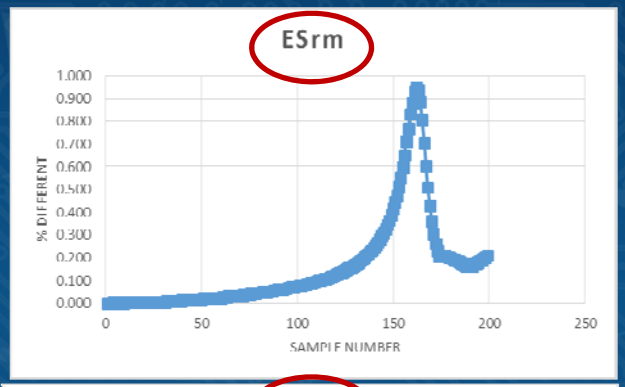
Δ Insertion Loss (S21)

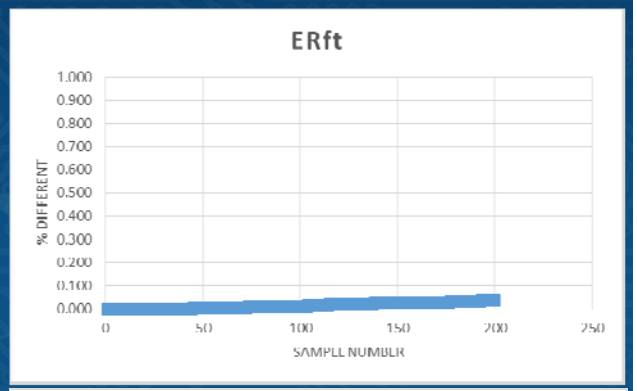
FormFactor Ex. 1031, p. 88

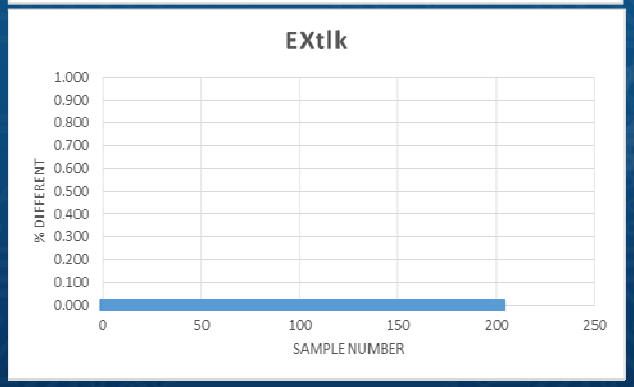
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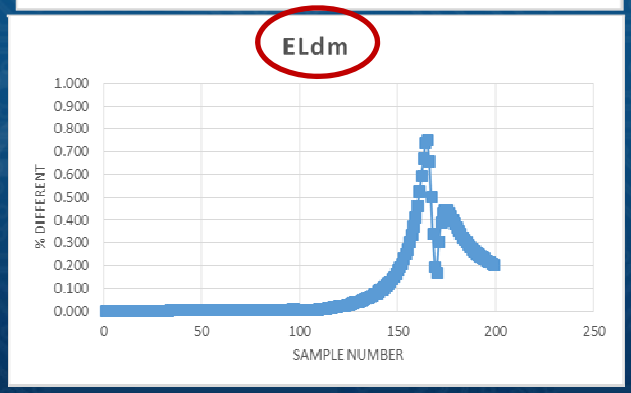
Which Error Terms are Most Affected?

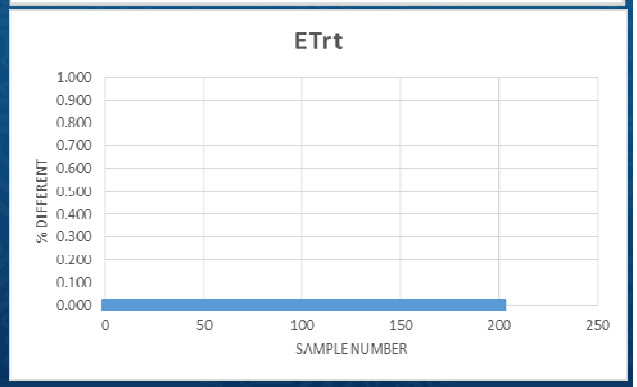








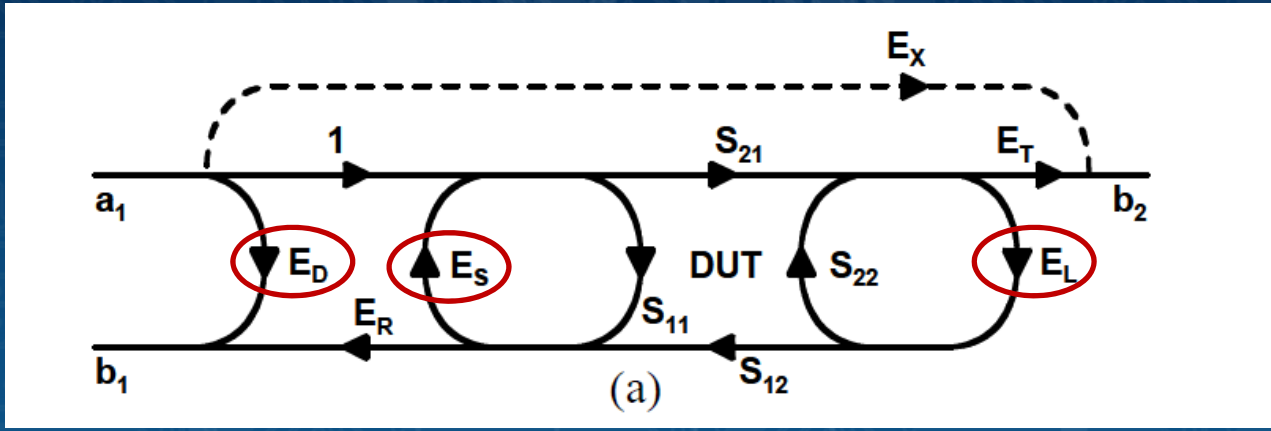




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Which Error Terms are Most Affected?



- ES is most affected (Source match)
- EL is next most (Load match)
- ED is third most (Directivity)
- The rest of the terms are affected less than 5%

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Summary

- **The most accurate measurement in a multi-site application is to make a calibration substrate that mirrors the multi-site layout**
  - Controls all of the RF traces for the highest correlation between sites

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SW Test Workshop
Semiconductor Wafer Test Workshop

2016

Automated Probe Card Exchange and Docking for RADAR Products Running at 40GHz and Beyond

Jory Twitchell
NXP Hardware Eng

June 5-8, 2016

Overview

- Where is RADAR used
- How does NXP RADAR fit in to industry
- Components needed to test
- Is it ready for production
- Show me the data
- Summary of results
- Question and Answer

FormFactor Ex. 1031, p. 93

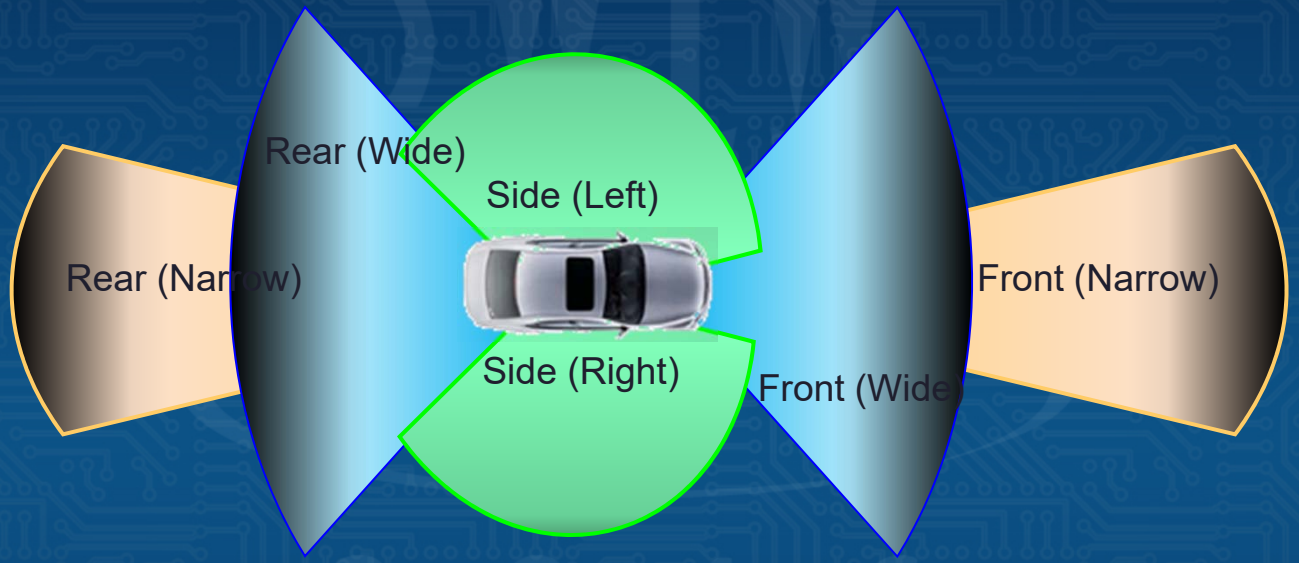
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Where is the RADAR

- **Radar use Past/Present**
  - Radar was developed around the time of WWII. It has traditionally been used in a variety of military and commercial applications such as detecting aircraft, ships, guided missiles and weather formations
  - The modern uses of radar is expanding to be used in antimissile systems, flight control systems, aircraft anti-collision systems, and even geological observations
- **Where does NXP fit into the RADAR space?**
  - Answer: Automotive radar

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NXP RADAR



NXP Chip-Sets designed to sense objects around your vehicle

FormFactor Ex. 1031, p. 95

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NXP RADAR

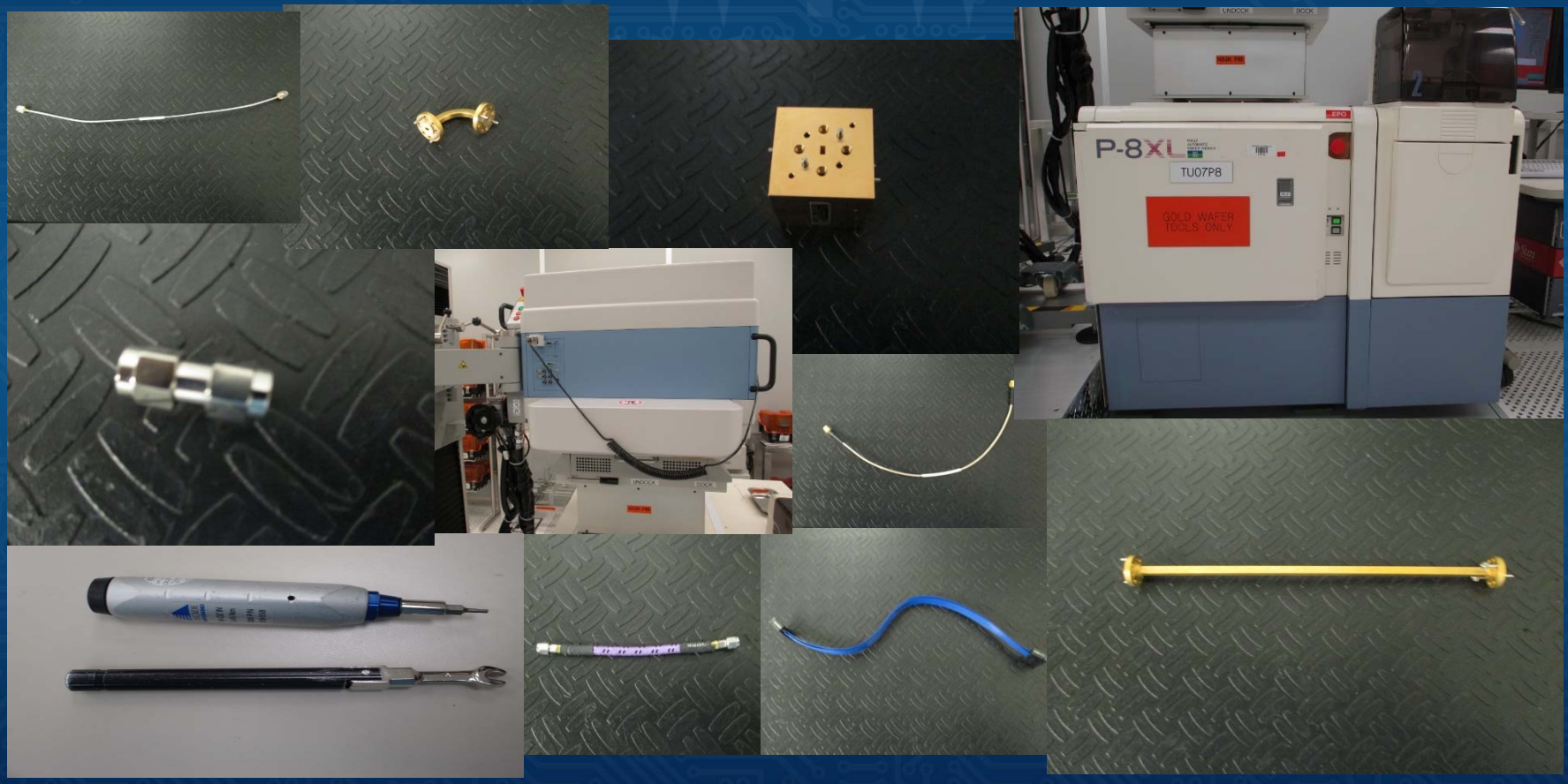
- **NXP produces a 77GHz radar transceiver chipsets which can support the following:**
- **Long-, mid- and short range functionality**
- **High performance and integration capabilities**
- **Multiple safety applications such as:**
  - Adaptive Cruise Control (ACC)
  - Blind Spot Detection (BSD)
  - Emergency Braking
  - Forward Collison Warning (FCW)
  - Headway Alert

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Parts to test

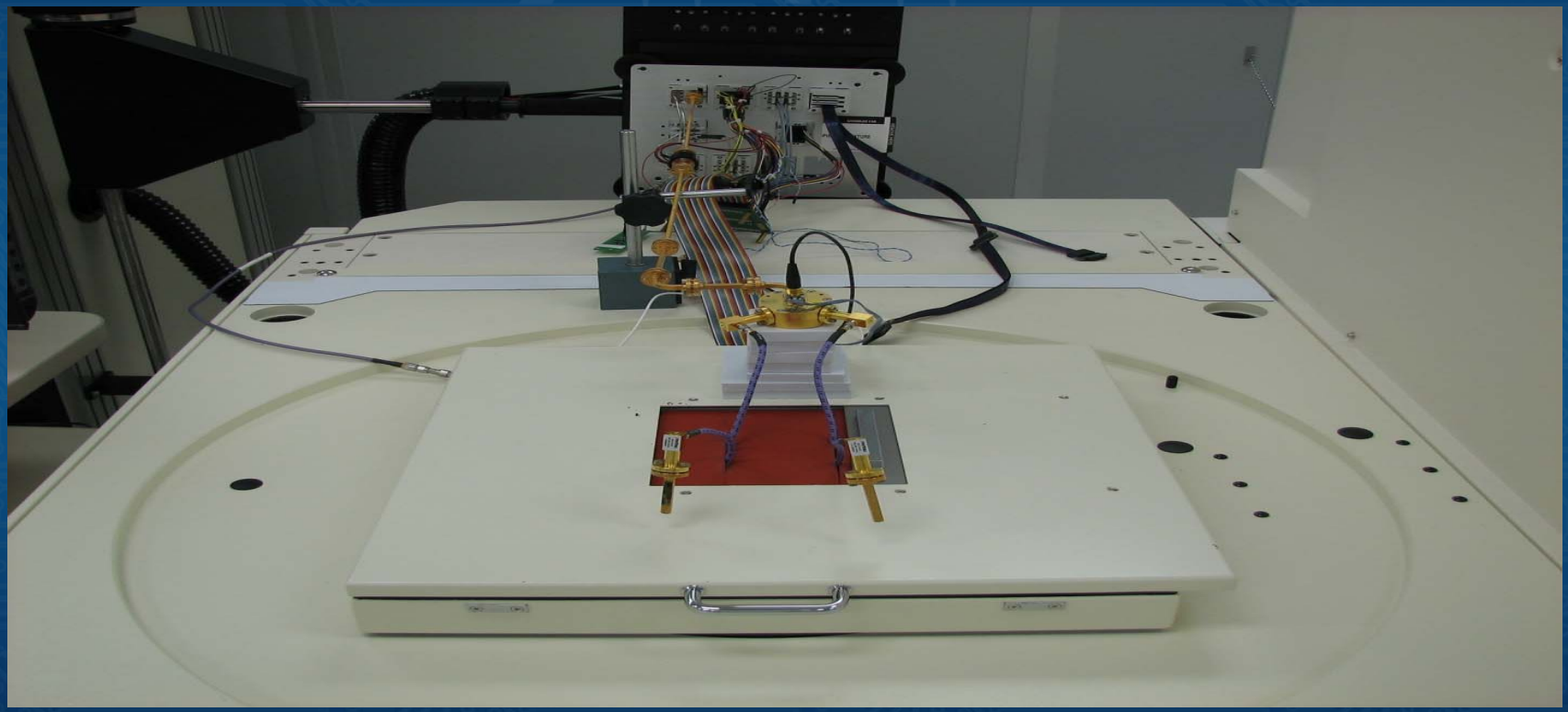
- **Parts required to test product**



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Assembled Parts

- **Parts fit together**

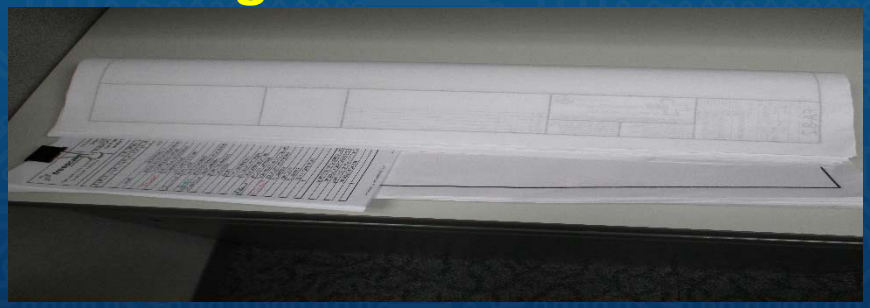


FormFactor Ex. 1031, p. 98

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Production Worthy?

- **Is the previous picture able to be ran by production associates?**
- **Answer: NO!**
  - It takes an engineer/technician hours to set this up. There are too many parts/pieces which have to be correct. Production does not have time to spend hours setting up a device.
- **The part has to be assembled properly with the correct components for each different device. This would be equivalent to a blueprint for testing the wafer.**



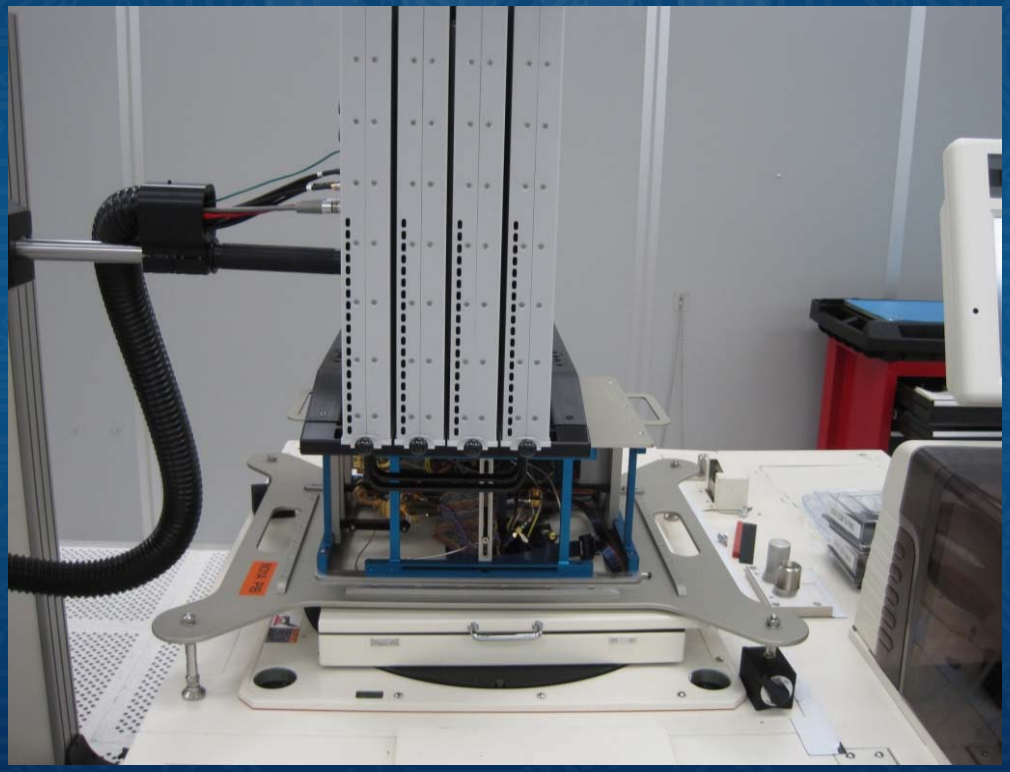
- **We Need a BETTER solution**

FormFactor Ex. 1031, p. 99

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Production Worthy 2nd Attempt

- Recruited some friends at NXP for our 2nd attempt at making the setup production worthy.



FormFactor Ex. 1031, p. 100

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Production Worthy 2nd Attempt

- The wires are now encased in a cage. The test head can be docked from the top. It was a big leap forward for the engineers setting up the tool.

- But did this solve our issue?
- Not quite…..

- The problem was to change the probe card, the cage had to be removed and all the wires detached from the probe card. It is still not ready to be ran by production associates. This process still too time consuming.

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Production Worthy 3rd Attempt

- How to make a production worthy 3rd attempt?
- Recruit some friends!
- Enlisted the help of our friends at inTest Corporation and Cascade MicroTech

inTEST Corporation
reduce the cost of testing

CascadeMicrotech®

FormFactor Ex. 1031, p. 102
FormFactor v. Technoprobe
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Proof of Concept (POC)

- **Stakes are now higher so decided to build a POC before starting the production version**

Test Name	Test	Lower	Upper	Min	Max	Mean	Sdev	Runs
MMW_Loopback_76	5000	-25	5	-22.627	-22.534	-22.568	0.0198	20
MMW_Loopback_38	5001	-25	5	-14.341	-14.267	-14.292	0.0170	20
MMW_Loopback_77	6000	-25	5	-23.576	-23.481	-23.517	0.0229	20
MMW_Loopback_38p5	6001	-25	5	-12.845	-12.760	-12.797	0.0206	20
MMW_Loopback_78	7000	-25	5	-20.271	-20.156	-20.219	0.0236	20
MMW_Loopback_39	7001	-25	5	-15.686	-15.639	-15.655	0.0104	20
MMW_Loopback_79	8000	-25	5	-24.290	-24.191	-24.241	0.0253	20
MMW_Loopback_39p5	8001	-25	5	-14.468	-14.411	-14.449	0.0138	20
MMW_Loopback_80	9000	-25	5	-24.819	-24.705	-24.764	0.0335	20
MMW_Loopback_40	9001	-25	5	-16.295	-16.237	-16.270	0.0136	20

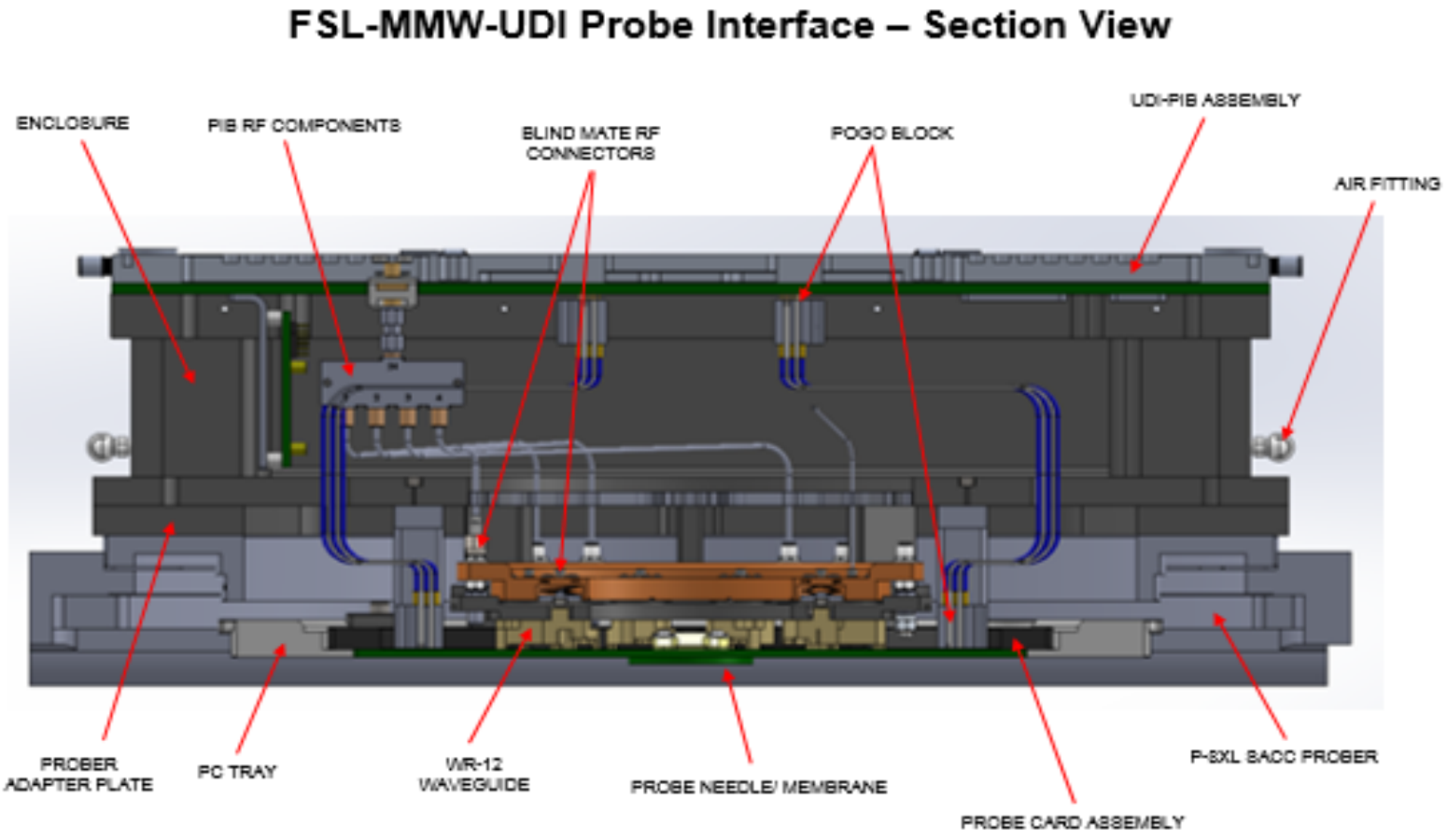
Test Name	Test	Lower	Upper	Min	Max	Mean	Sdev	Runs
MMW_Loopback_76	5000	-25	5	-19.902	-19.827	-19.854	0.0164	20
MMW_Loopback_38	5001	-25	5	-14.396	-14.341	-14.358	0.0119	20
MMW_Loopback_77	6000	-25	5	-20.330	-20.275	-20.306	0.0180	20
MMW_Loopback_38p5	6001	-25	5	-13.363	-13.301	-13.346	0.0172	20
MMW_Loopback_78	7000	-25	5	-17.229	-17.159	-17.203	0.0193	20
MMW_Loopback_39	7001	-25	5	-15.162	-15.121	-15.148	0.0114	20
MMW_Loopback_79	8000	-25	5	-22.229	-22.115	-22.166	0.0311	20
MMW_Loopback_39p5	8001	-25	5	-17.159	-17.120	-17.146	0.0124	20
MMW_Loopback_80	9000	-25	5	-23.414	-23.328	-23.371	0.0211	20
MMW_Loopback_40	9001	-25	5	-15.546	-15.521	-15.538	0.0063	20

- **Data from the loop back connections**

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Universal Hard Dock



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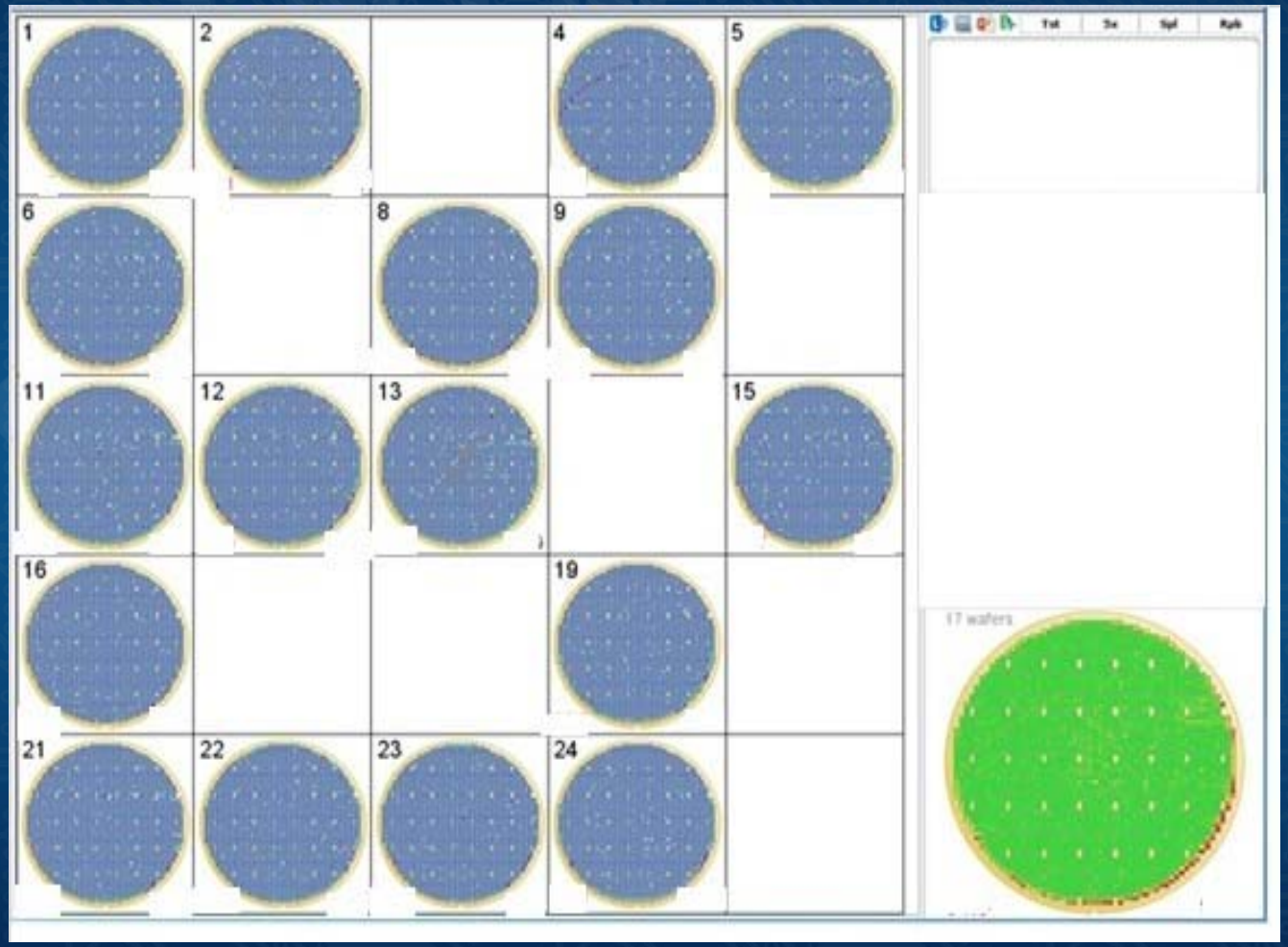
Universal Hard Dock Components

- **The Universal Hard Dock incorporated the following items:**
  - Blind mate connections for the 77GHz and below signals
  - Pogo block for the DC and logic connections
  - PIB RF components
  - Air fitting to allow for testing at temperature other than room
  - WR-12 waveguides for connecting the probe card to the enclosure
  - UDI PIB assembly for docking the test head

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Universal Hard Dock Production Data -40C

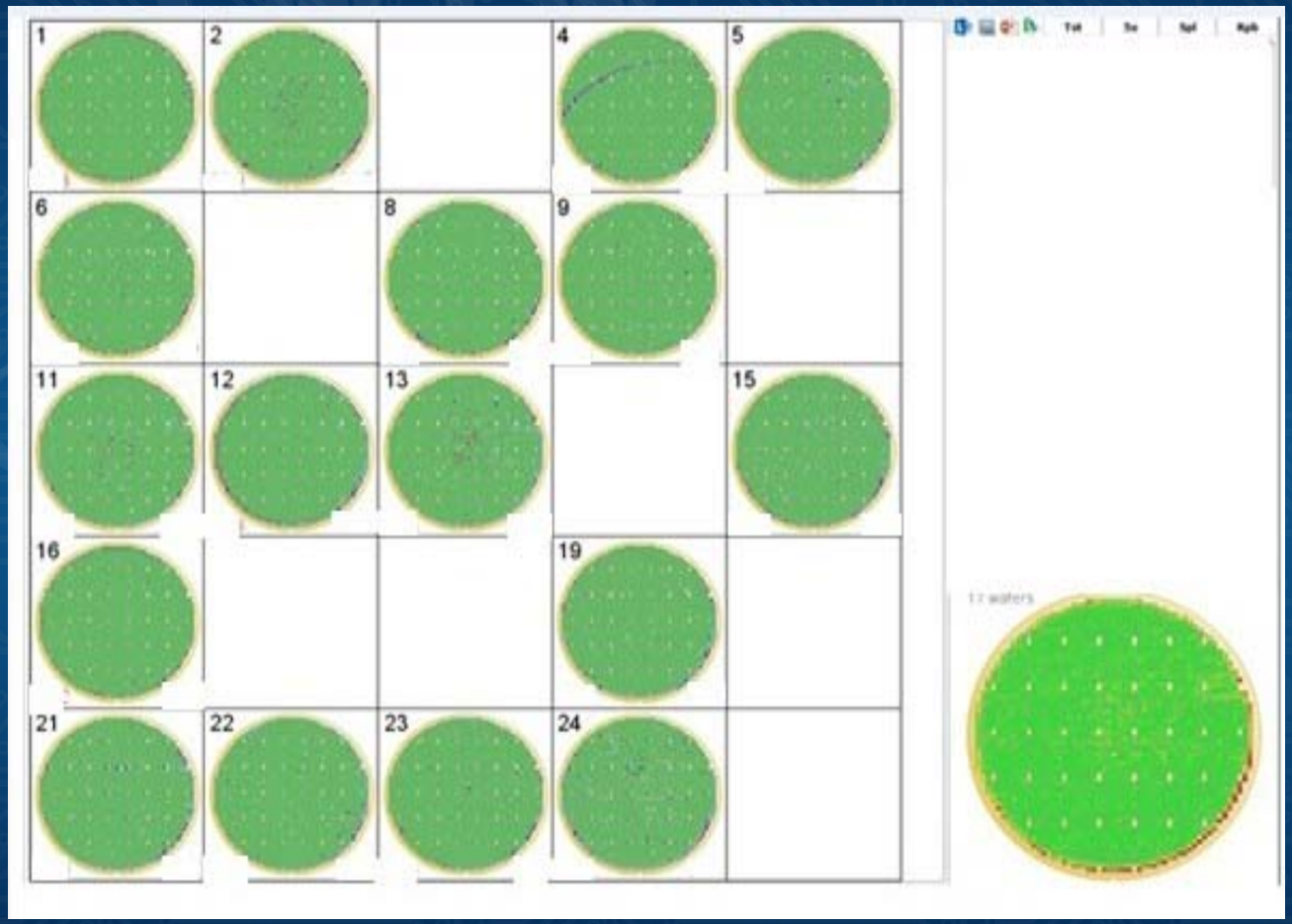
- Test done at -40C
- Wafer splits 2,6,8,11,13, 15,19,22,23
- Wafer splits 1,4,5,9,12,16, 21,24



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Universal Hard Dock Production Data 125C

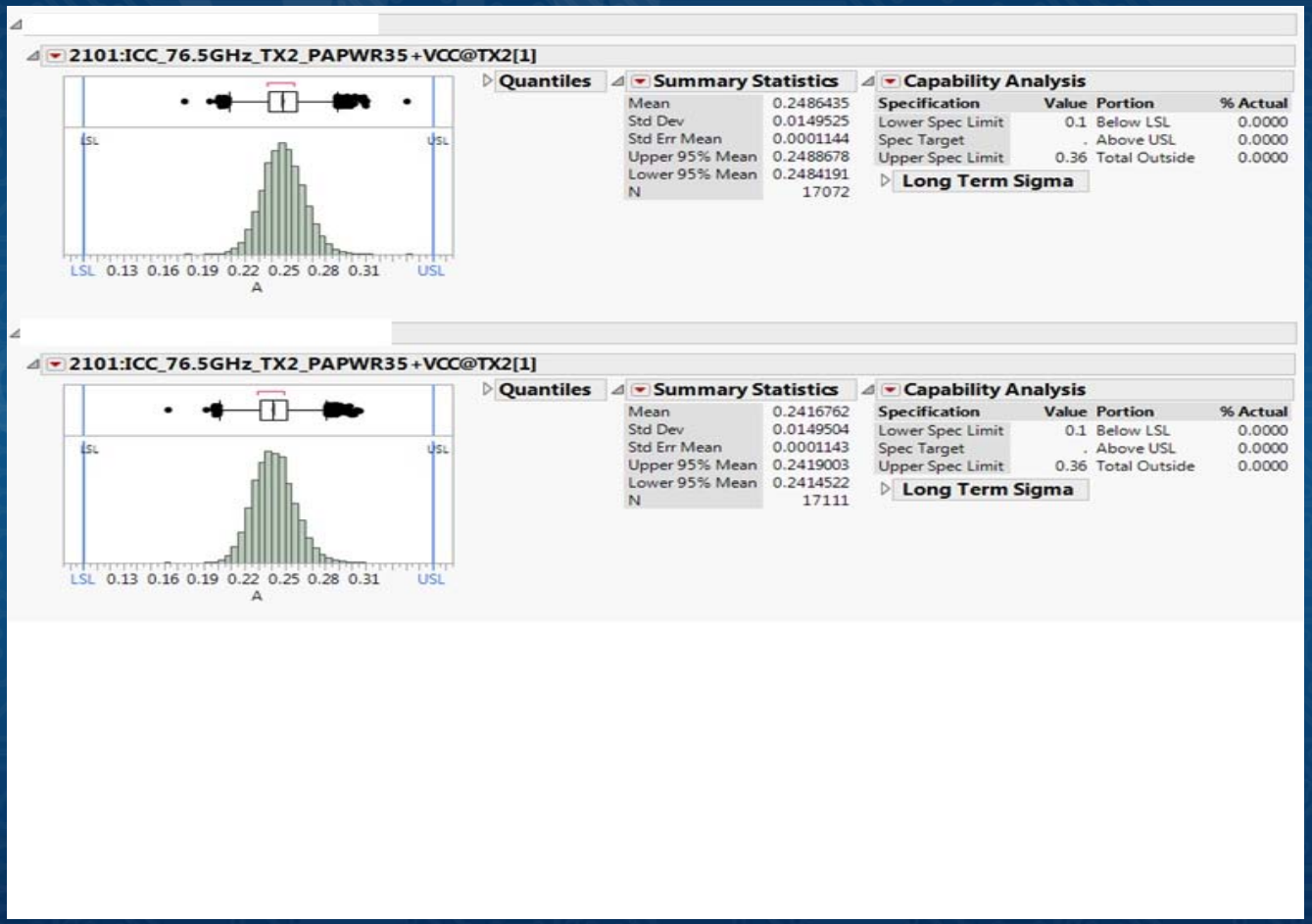
- Test done at 125C
- Wafer splits 2,6,8,11,13, 15,19,22,23
- Wafer splits 1,4,5,9,12,16, 21,24



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Universal Hard Dock Production Data

- ICC test between systems



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Summary

- Time savings of 2x for changeover between products
- Eliminate possible damage to cables, waveguides, and other RF components due to handling
- Critical parameters Pout & Icc Cpk >> 1.67
- Yields are comparable between setups
- The Universal Hard Dock allows manufacturing the ability to change the products running without engineering involvement saving time and engineering resources

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Thanks for the Support !

- **Thank you to the following individuals and their teams for the time and effort in completing this project**
  - Jeff Finder and team at NXP
  - Roy Green and team at inTest
  - Jeff Arasmith and team at Cascade MicroTech



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Question and Answer



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SWTW 2016

SW Test Workshop
Semiconductor Wafer Test Workshop

Customized probe card for on-wafer testing of AlGaN/GaN power transistors

R. Venegas[1], K. Armendariz[2], N. Ronchi[1]

[1]imec, [2]Celadon Systems Inc.

Presented by Bryan Root[2]

CELADON™ ULTRA HIGH PERFORMANCE PROBE CARDS

June 5-8, 2016

Outline

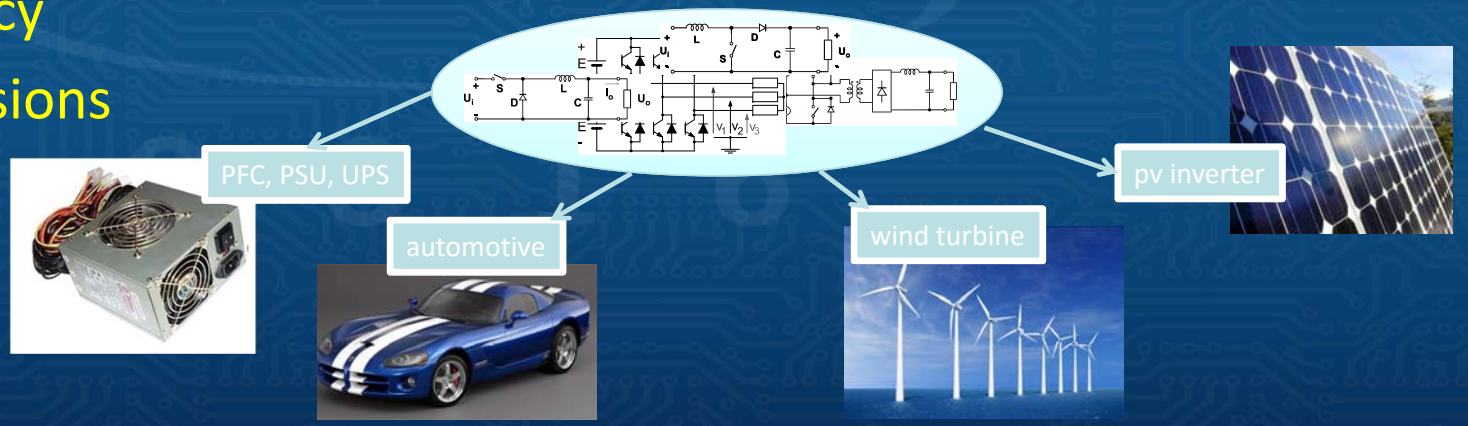
- **Introduction**
  - GaN for power switching applications
- **DC Characterization of GaN power devices**
  - CELADON probe cards
  - Setup
  - Measurements
- **Trapping effects in GaN HEMT**
  - Pulsed I-V
  - Setup
  - Measurements
- **Conclusions**

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Power switching applications

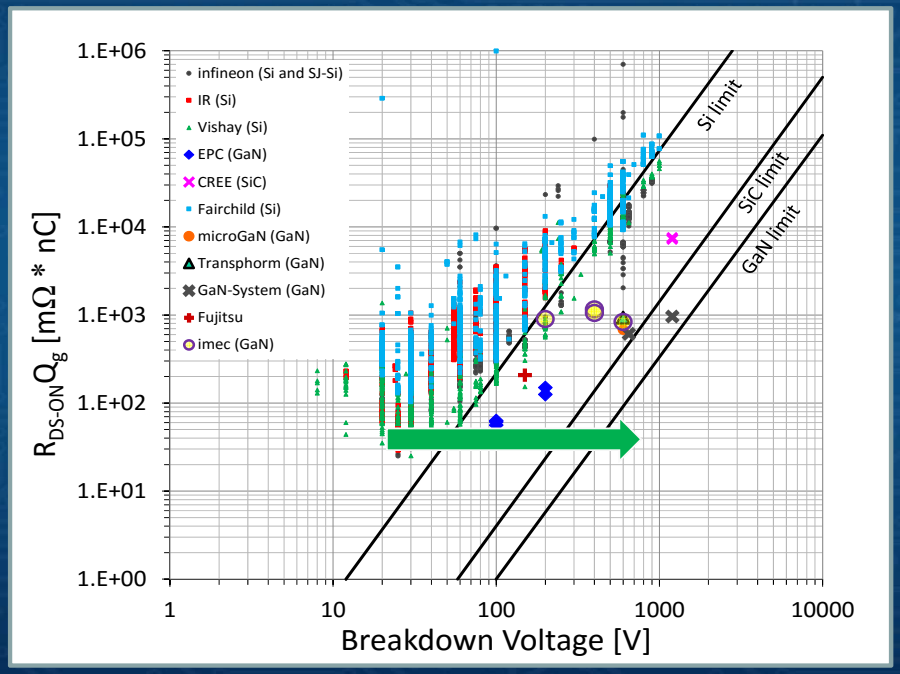
- **Power switching applications are a common presence in our daily-life. Circuit designers and device manufacturers are constantly challenged to improve the present technology, in particular to achieve:**
  - ❖ Higher efficiency
  - ❖ Smaller dimensions
  - ❖ Lower costs



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Figure of Merit

Devices with better $R_{DS\text{-}ON}Q_g$ and higher breakdown are needed to improve the circuit performance.



Silicon has reached its theoretical physical limits.

New technologies, such as GaN and SiC, will soon replace Si-based devices in power switching circuit.

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GaN-based devices

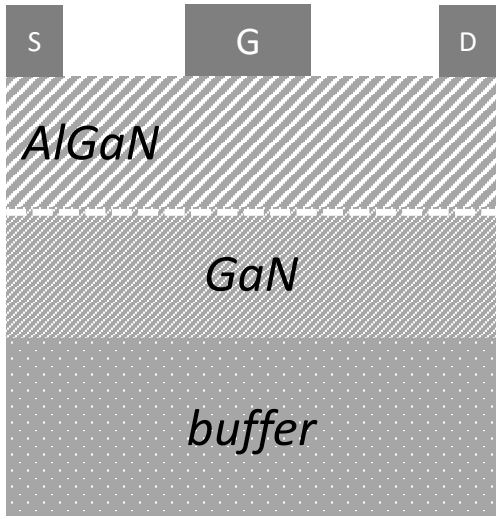
- **AlGaN/GaN High Electron Mobility Transistors (HEMTs) are attractive for power-switching applications due to their excellent properties:**
  - wide energy band-gap (high breakdown)
  - high electron mobility (fast switching speed)
  - good heat conductivity
  - high density electron gas **2DEG** (10^{13} cm^{-2})

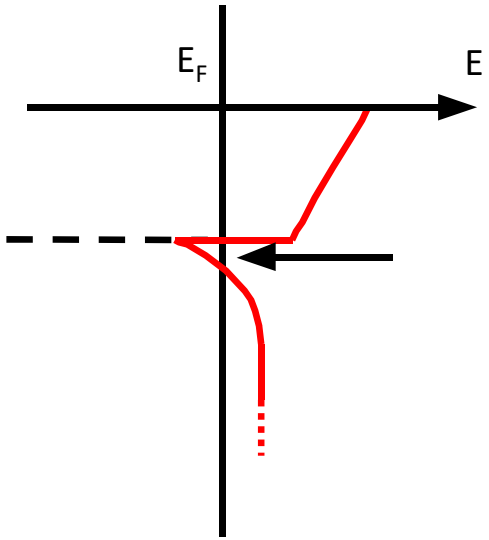
Property	Units	Si	GaAs	4-SiC	GaN
Bandgap	eV	1.1	1.42	3.26	3.39
Relative dielectric constant	-	11.8	13.1	10	9
Electron mobility	cm^2/Vs	1350	8500	700	1200-2000
Breakdown field	10^6 V/cm	0.3	0.4	3	3.3
Saturation electron velocity	-	1	1	2	2.5
Thermal conductivity	K	1.5	0.43	3-3-4.5	1.3

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Depletion mode





Intrinsic normally-on operation (depletion-mode):

- Polarization-induced 2DEG

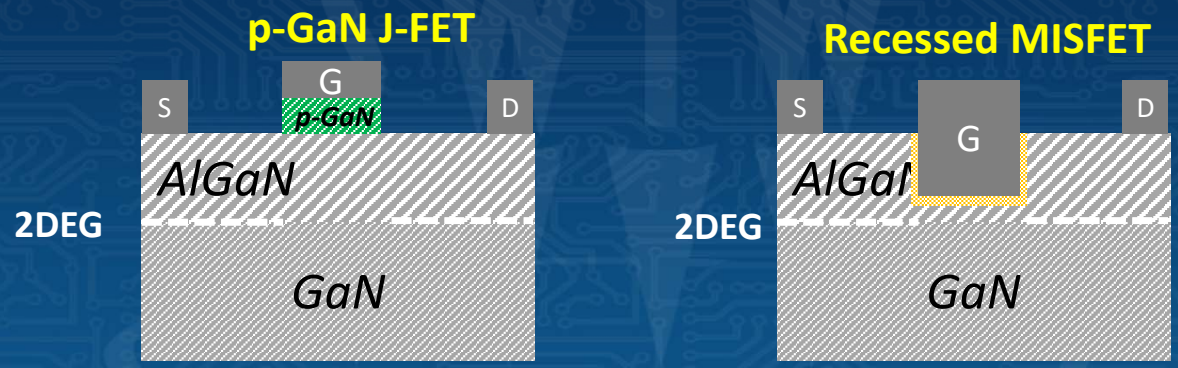
Normally-off operation (enhanced-mode):

- Fail-safe
- simpler gate control circuit

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From d-mode to e-mode



A p-GaN layer below the gate lifts-up the band diagram below the gate to realize e-mode operation.

The AlGaN layer is recessed below the gate, to locally interrupt the 2DEG to realize e-mode operation.

FormFactor Ex. 1031, p. 118

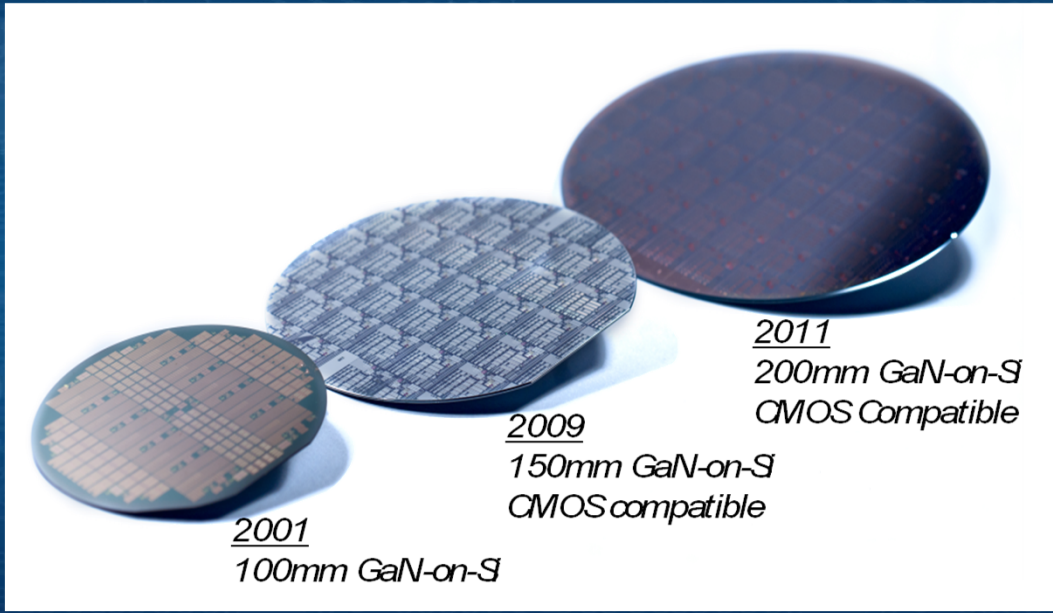
FormFactor v. Technoprobe
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imec

Imec's R&D program on GaN devices-on-Si is meant to develop a GaN-on-Si process and bring GaN technology towards industrialization.

Imec R&D program highlights:

- High current, high V_{BD} devices
- E-mode operation
- 200mm (8 inch) epi-wafers
- CMOS compatible process
- Diodes co-integration
- Gold free ohmic contacts
- Advanced substrates



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A new challenge for characterization

High switching speed, high power and the electrical behavior of the AlGaN/GaN power transistors call for specific characterization techniques in the power domain.





"Traditional" approaches:

- Limited current (for DC needles)
- Poor signal integrity required (for μs pulses)
- Low reliability at high temperature
- Short life time

New techniques are necessary for on-wafer power transistor characterization!

FormFactor Ex. 1031, p. 120

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Customized probe cards



Our solution employs a CELADON VC20 VersaCore™ with multiple needles mounted on a 45E probe card adaptor.

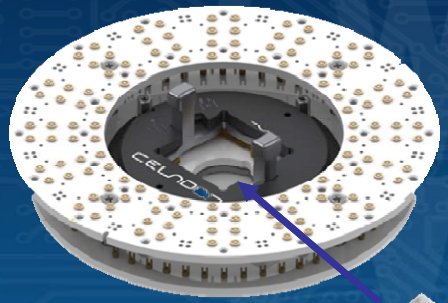
- High current measurements
- Low leakage (for breakdown measurements) less than 5fA’s
- Easy to swap between different probe card cores using Celadon’s insertion tool
- High temperatures (ceramic core) up to 200C

FormFactor Ex. 1031, p. 121

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VersaCore™ Formats

Keithley S600



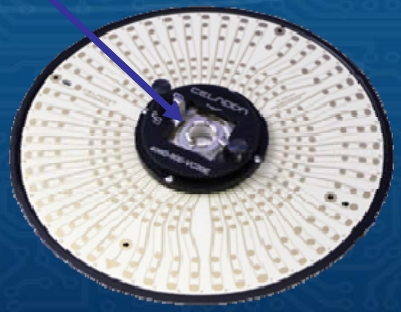


45E Modeling and Characterization



Celadon Indexer





Agilent 407X/408X

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Different cores for different layouts

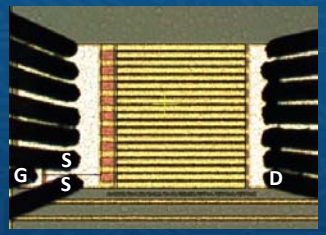
The cores are designed to satisfy the device specifications (layout, position of bond-pads, maximum current expected).

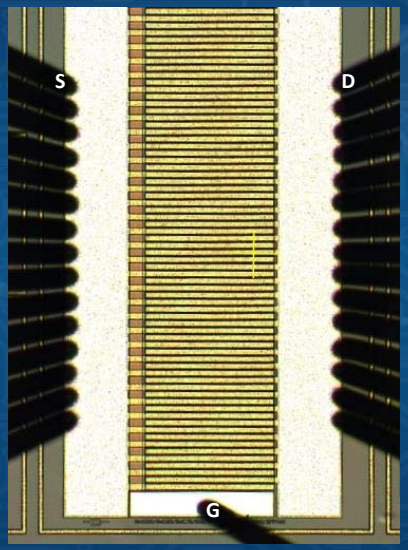
The large number of needles guarantees:

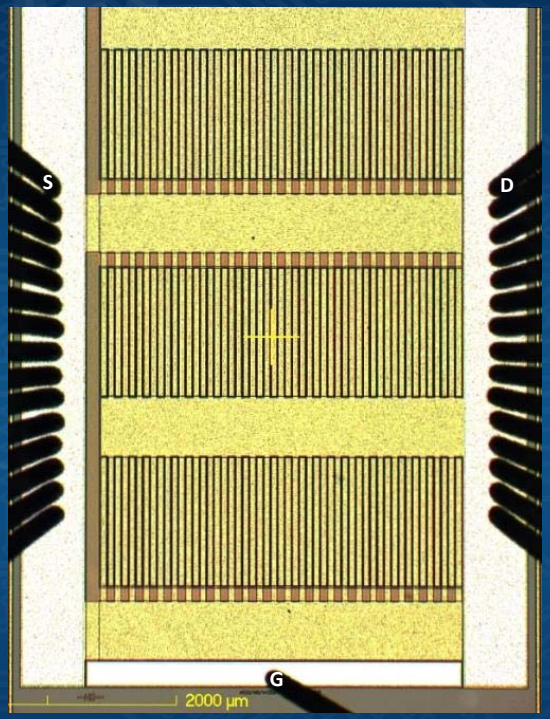
↓ lower contact resistance

↓ lower inductance

↑ higher maximum current



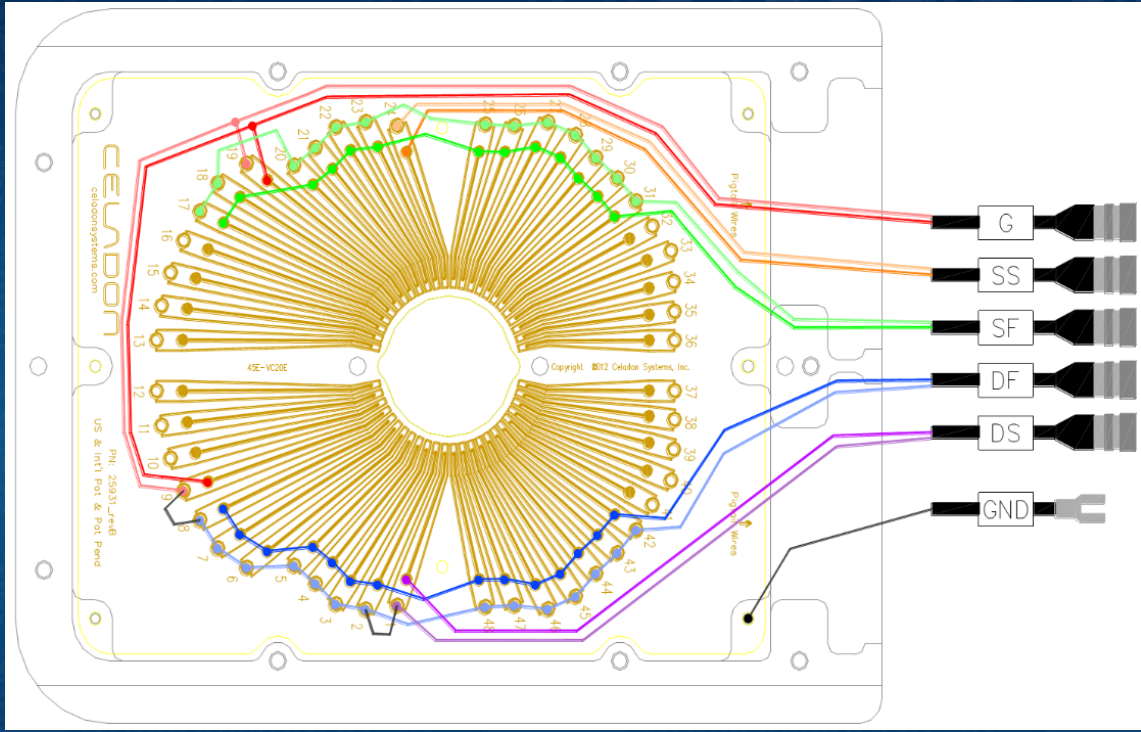




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Internal wiring

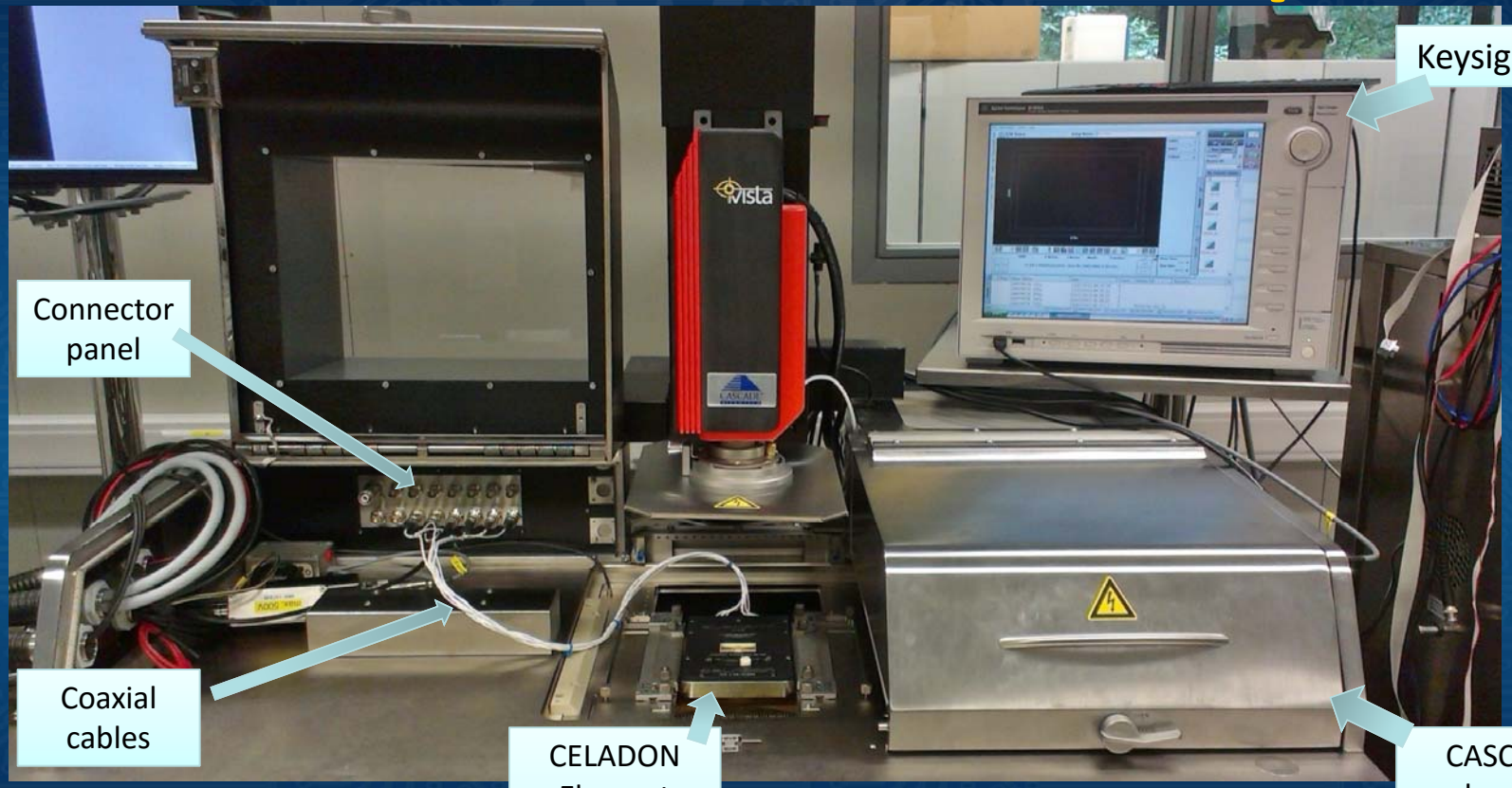


- Coaxial cables are used to contact the instrumentations
- Signal integrity is guaranteed by bringing the cable shield as close as possible to the needles
- Two isolated needles are reserved for the SENSE connections of drain and source
- Input (drain) and output (source) of the current are on distinct cables.

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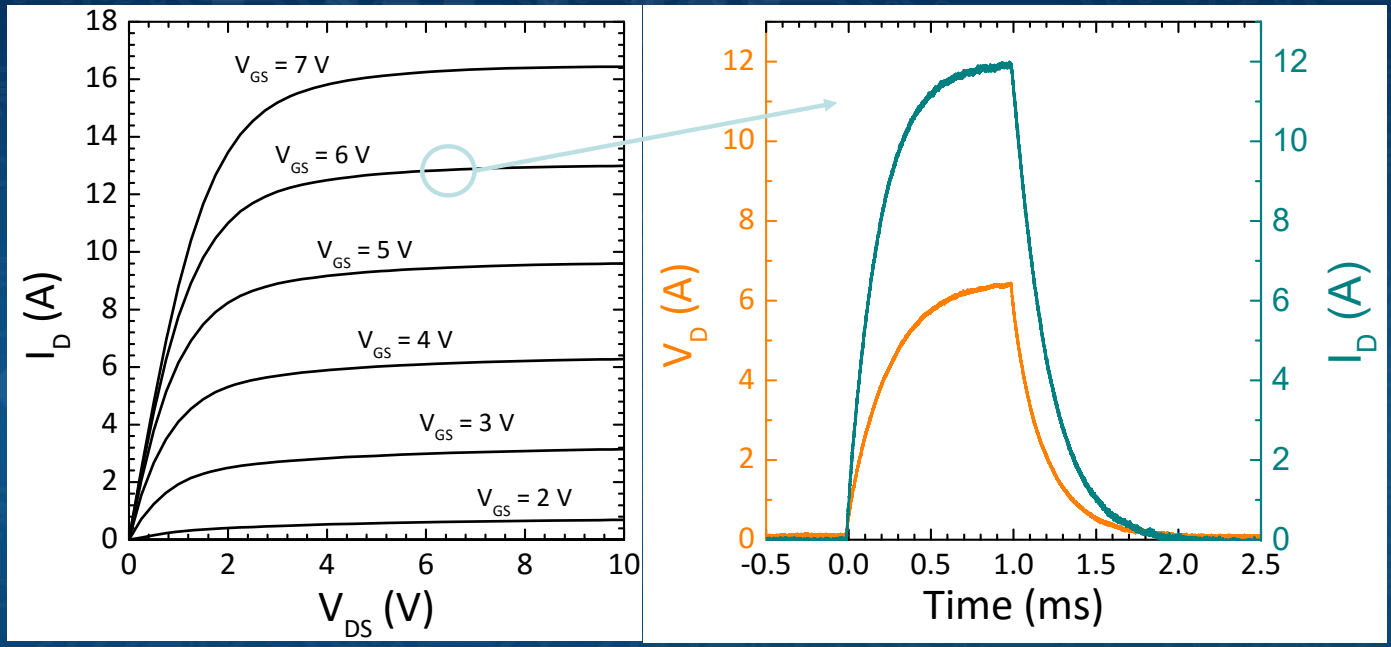
DC-measurement setup



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DC-measurements: I_D-V_{DS}

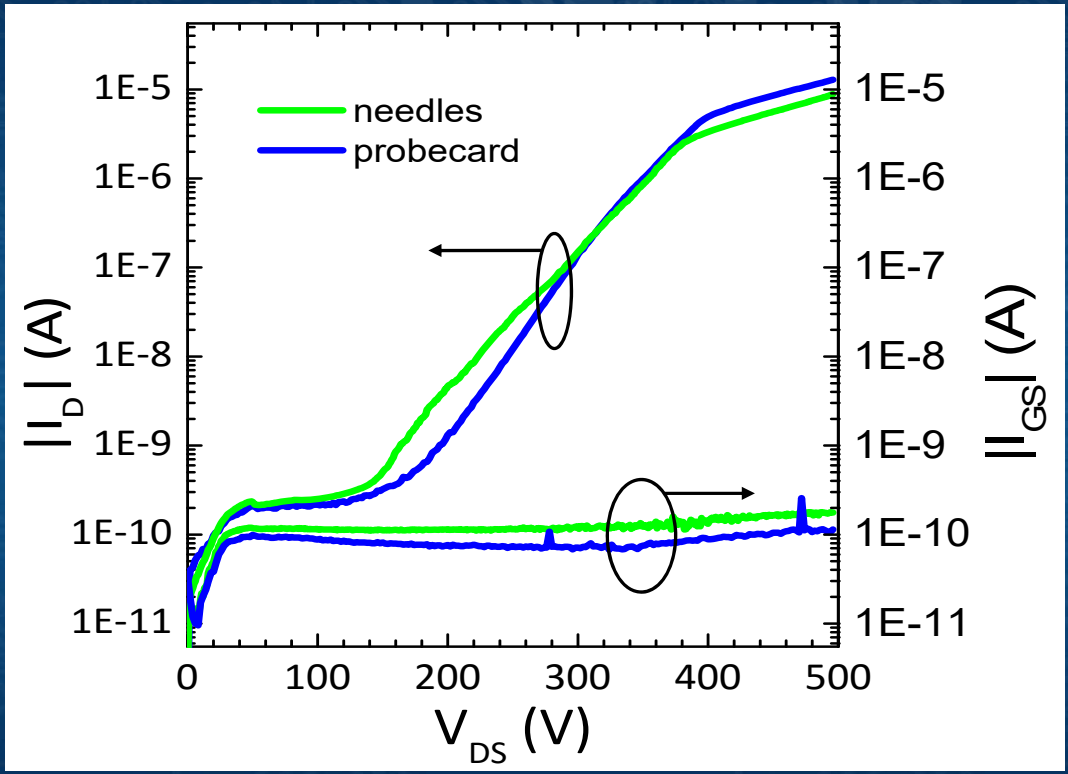
- Output current of an e-mode power devices
- Long-pulses (1ms pulse width, duty cycle 1%)
- Smooth shape of the measured curves



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DC-measurement: leakage



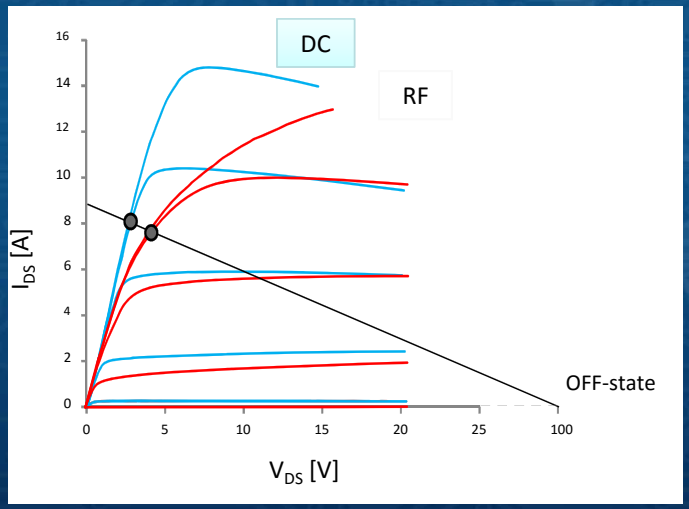
- The probe card does not introduce additional leakage in the measurement

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Trapping effect in GaN-HEMT

GaN technology is not immune to trapping effects. The most detrimental effect of traps for the device behavior is the decrease of the output current (increase of dynamic R_{DS-ON}).
Traps in GaN-HEMT can be at the surface and in the buffer.



The effects of a higher R_{DS-ON} in a switching application are:

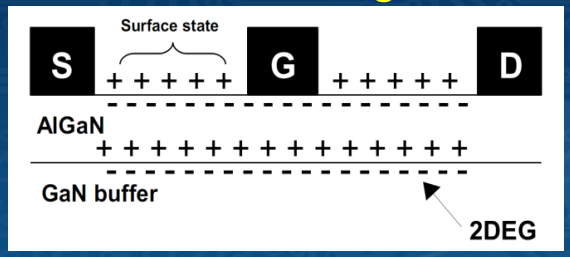
- Higher dissipative power on the transistor
- Higher T_j
- Increased power loss (lower efficiency)
- Distortion of the V_{out}

FormFactor Ex. 1031, p. 128

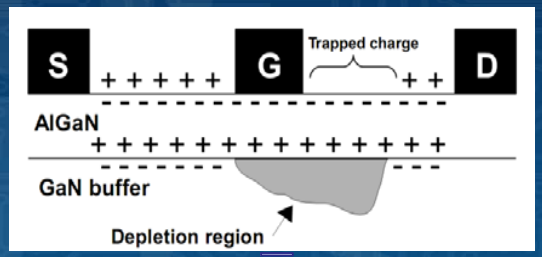
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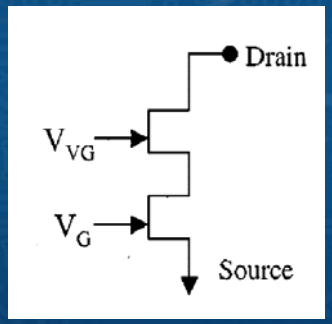
Virtual gate effect

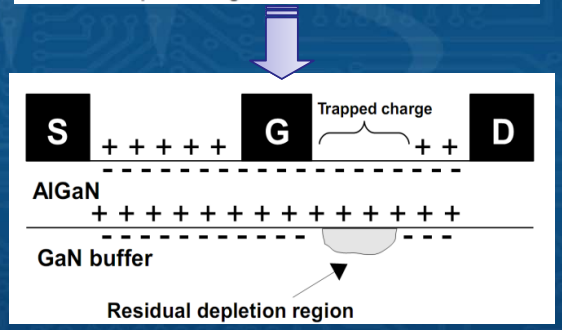
The effect of surface traps is often compared to the presence of a "virtual gate" in series with the "real" gate.











The complete turn-on of the device is linked to the release of the trapped charge.

Vetury, R.; "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs"; IEEE Transactions on Electron Devices 2001

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Avoid trapping in AlGaN/GaN HEMT

For a low dynamic $R_{DS\text{-}ON}$ dispersion, the following points have to be addressed:

- Improve the epitaxial layer quality (buffer-dispersion)
- Decrease the number of trapping states at the surface (passivation/surface cleaning)
- Decrease the intensity of the electric field peak (field plate)

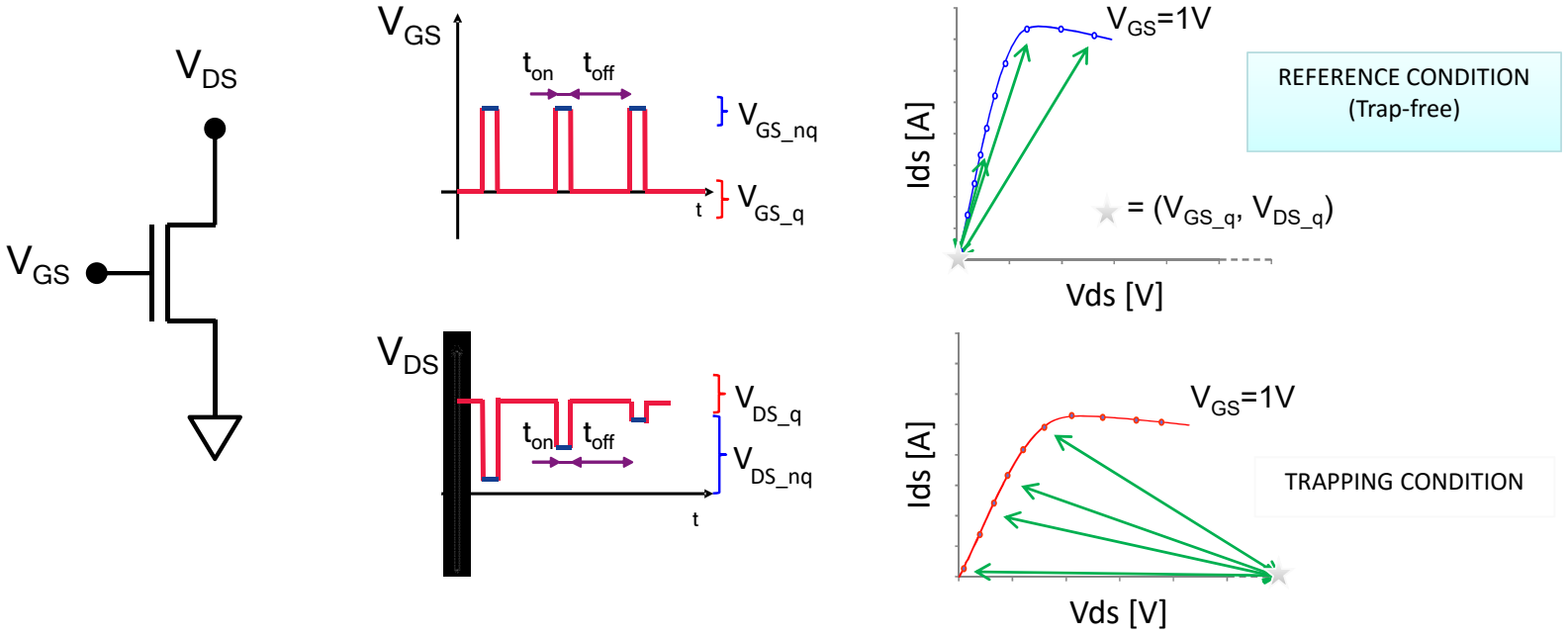
The dynamic $R_{DS\text{-}ON}$ must be measured in a reliable way and in a bias condition similar to the device targeted application.

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Dynamic R_{DS-ON} dispersion

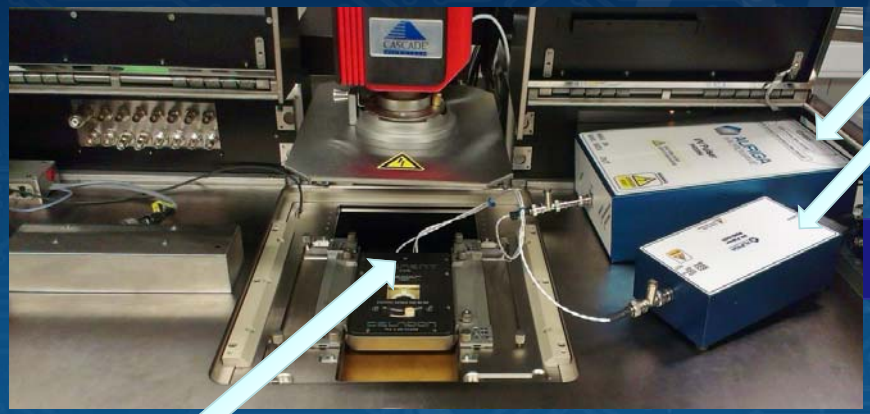
The dynamic R_{DS-ON} is measured from the I_D-V_{DS} characteristic by means of pulsed measurements (with high drain bias applied during the off-state).



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Auriga P-IV system

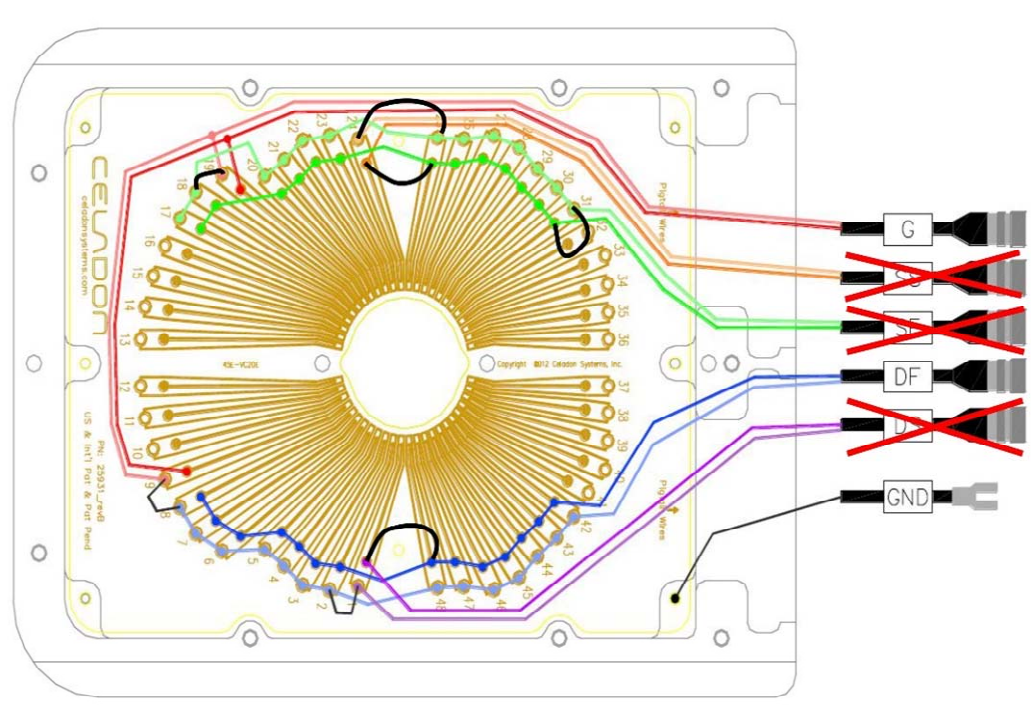






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Probe card connections



For fast switching measurements long current paths and ground loops must be avoided.

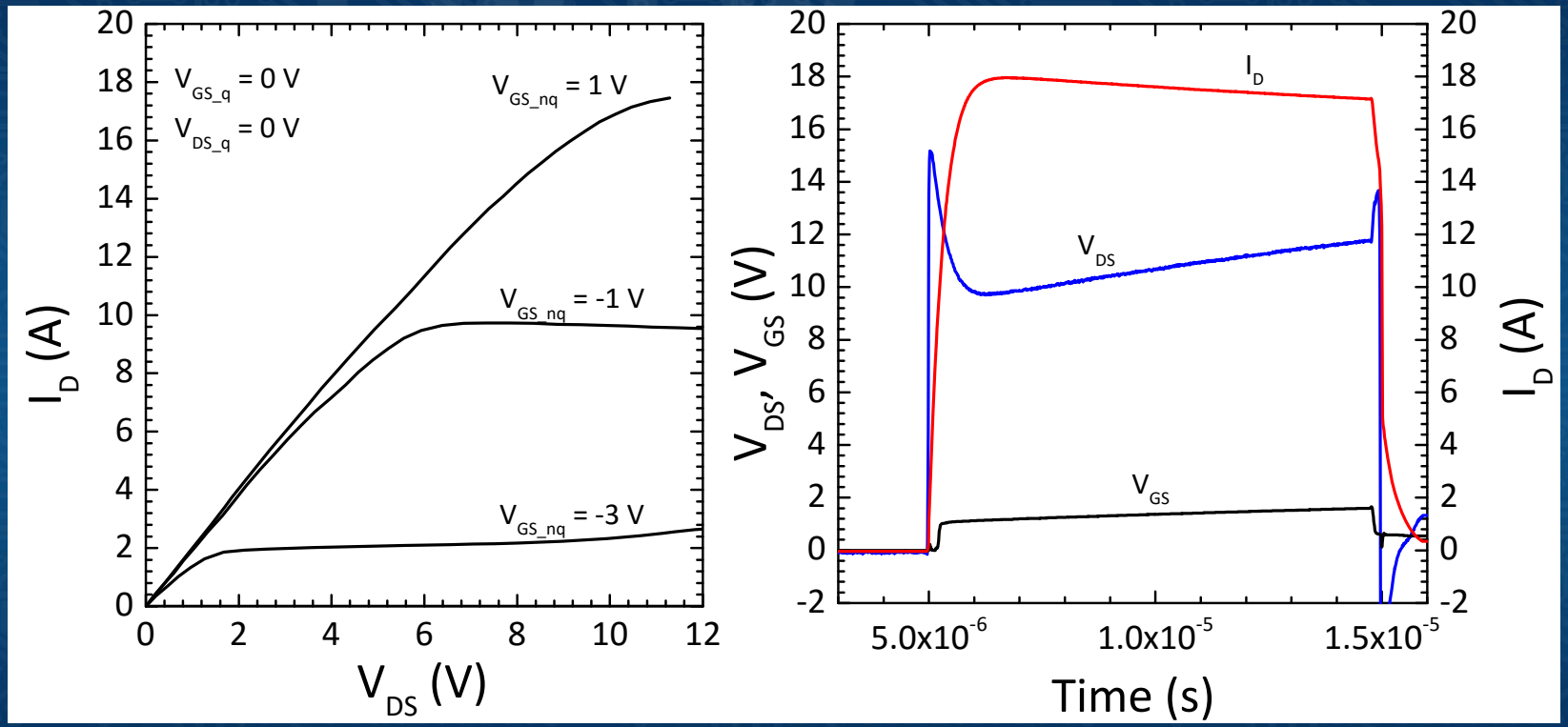
- Source connections are removed
- No sense terminals are needed
- The “return” of the current is through the shield of the drain cable

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P-IV measurements

- Output current of a d-mode power devices
- Short-pulses (10 µs pulse width, duty cycle 10%)
- Limited amplitude of spikes (mainly due to the d-mode operation)

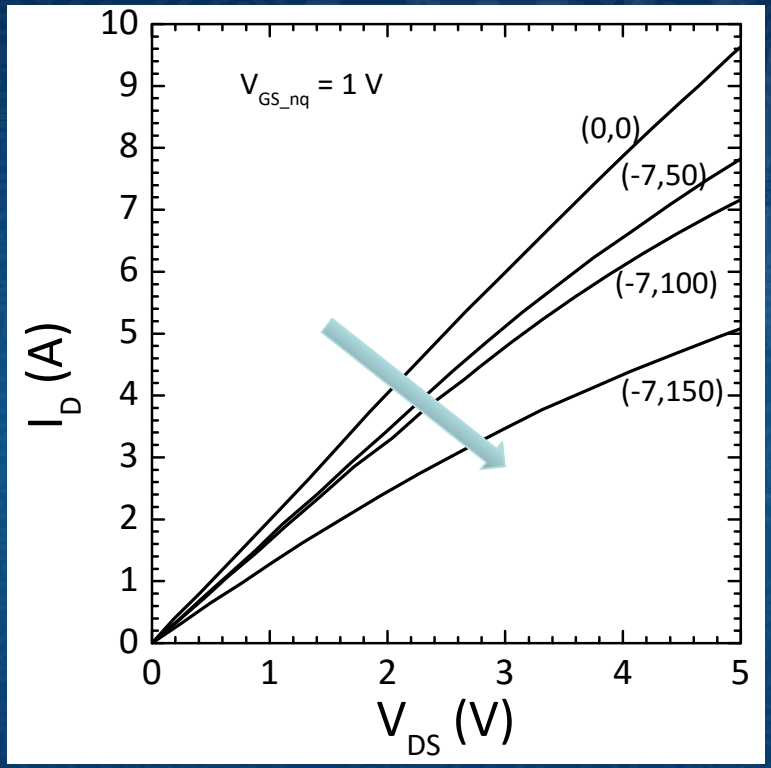


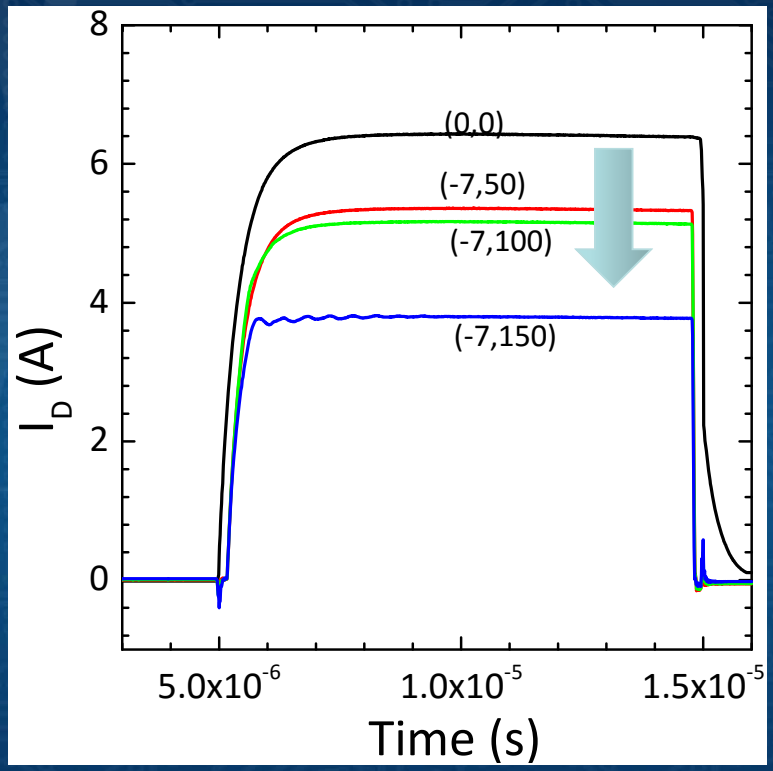
FormFactor Ex. 1031, p. 134

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$R_{DS\text{-}ON}$ dispersion

- Dynamic $R_{DS\text{-}ON}$ degradation for high V_{DS_q}
- Limited amplitude of current spikes





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Conclusions

In this presentation we have demonstrated how the CELADON VC20 VersaCore™ and the 45E probe card holder are successfully used for testing GaN power devices for switching applications.

In particular, we have shown:

- On-wafer high voltage and high current measurements
- Versatility of the interchangeable cores to match the device layout
- Smooth shape of the measured waveforms
- Reliable measurements of fast high-current pulses
- Limited spikes
- Easy to use and reproducible measurement setup

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Acknowledgements

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SWTW 2016

SW Test Workshop
Semiconductor Wafer Test Workshop

High and Low Temperature Wafer Probing Challenges





Presenters: Wei Liang Sio
Emanuele Bertarelli

Authors: Yah Ean Koh
Raffaele Vallauri

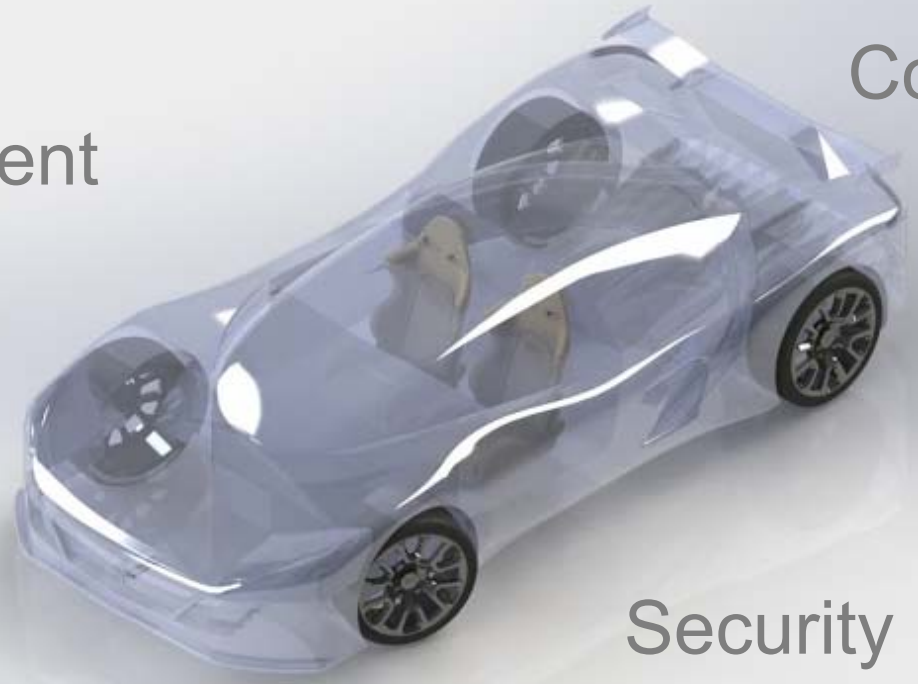
June 5-8, 2016

Overview

- Motivation
- Probing challenges at high/low temperatures
- Production probing issues with reference vendor
- Prober setup optimization
- Technoprobe solution introduction and results
- Conclusions

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Motivation: Automotive Applications



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Probing challenges at high/low temperatures

- **Temperature variation makes everything dynamic, requiring the stabilization of thermal deformation of mechanical setup**
  - Prober and probe card are made of different components and materials, showing different thermal expansion behavior
  - Thermal gradients are also present depending on x,y,z location and are changing during over time (chuck movement during probing, on-line cleaning execution)

→ **Full system to be stabilized in temperature before start probing**

→ **Specific probe card design / probe technology**

→ **Planarity of prober chuck to be under control**

→ **Optimization of chuck movement**

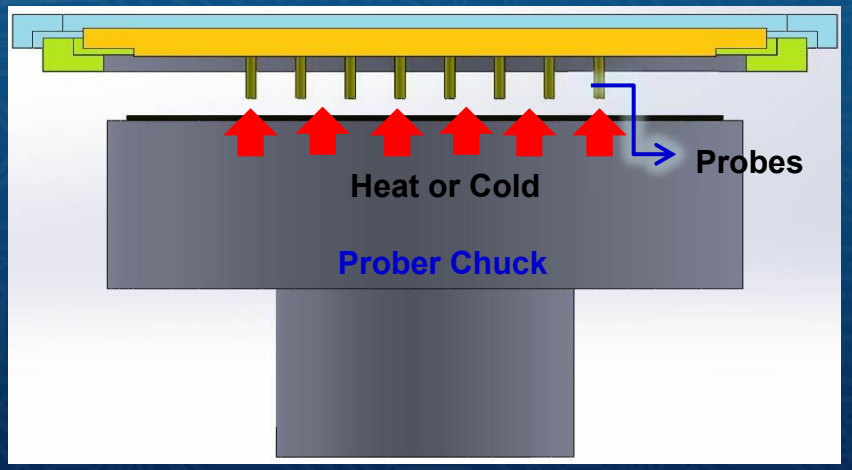
- **At low temperature condensation can occur (dew point)**

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Mechanical Setup Stabilization – Thermal Deformation

- **Chuck temperature affects probe card + prober deformation → x,y,z displacement of tips.**
- **Uneven expansion and contraction causes:**
  - Uneven contact between different probes
  - Incorrect overdrive
  - Pad damage
    - OD out of control (z)
    - Incorrect alignment (x,y)



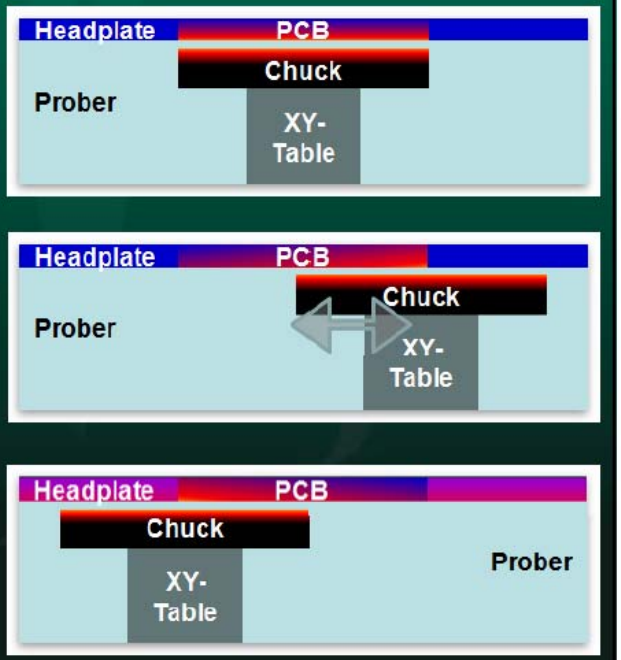


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Ref.: S07_02_Bleyl_Martens_SWTW2011

Continuous thermal stress by moving chuck

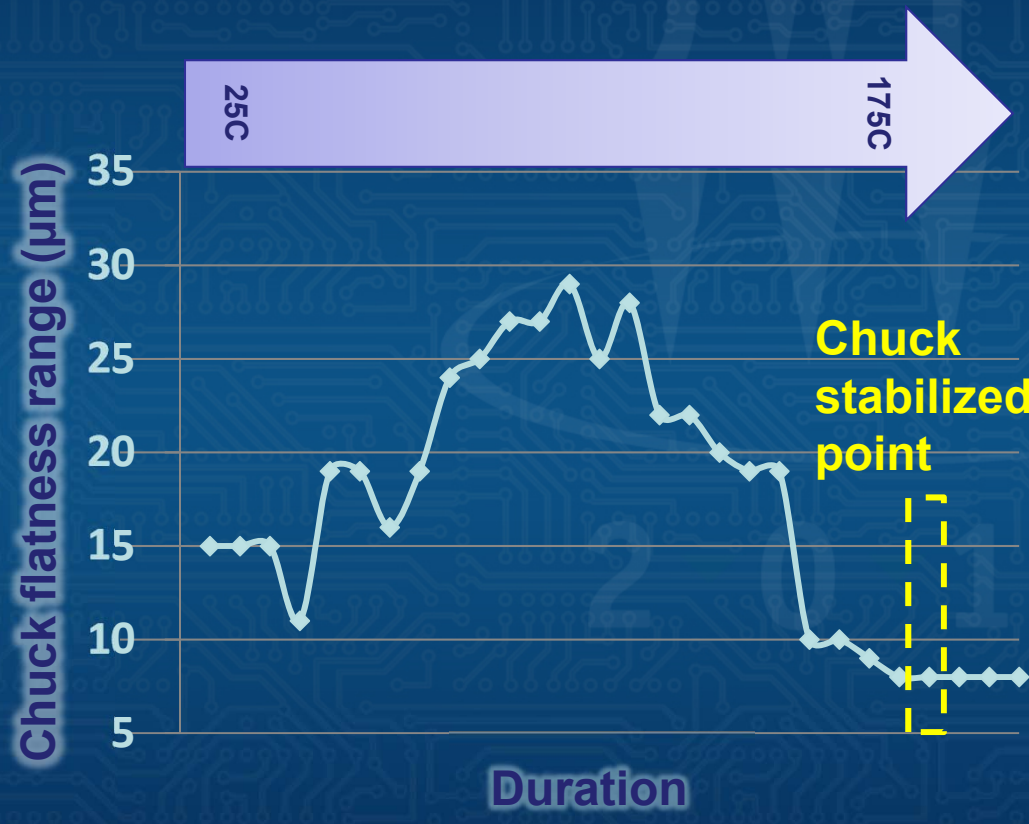
- **Wafer start up**
  - Fast heating of PCB
  - Head plate slow temp. change
- **Moving chuck**
  - Change of thermal gradient in PCB
  - Depends on size and thickness
- **Long term status**
  - Headplate warms up
  - Continuous change of thermal gradient in PCB

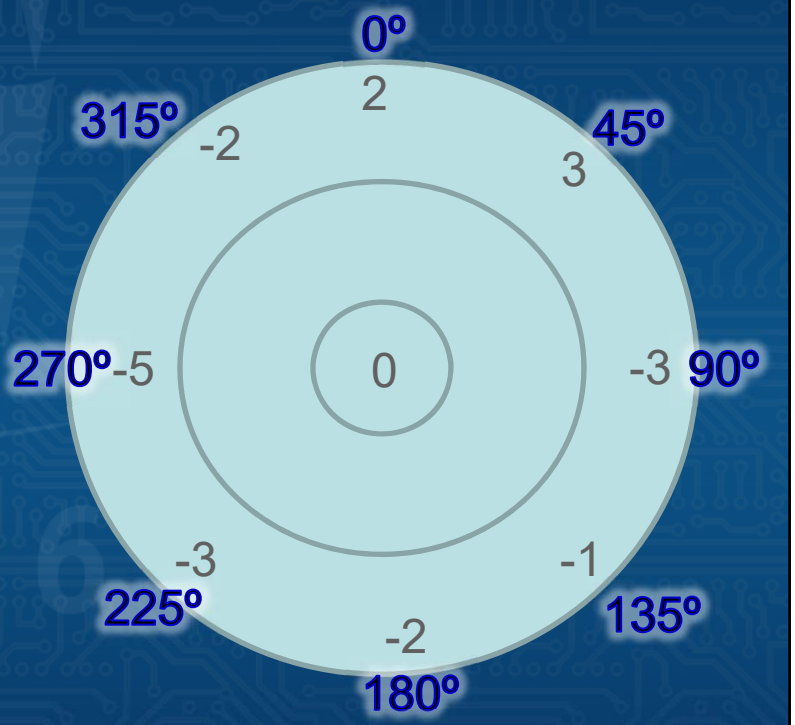


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Chuck Flatness Stability Over Time



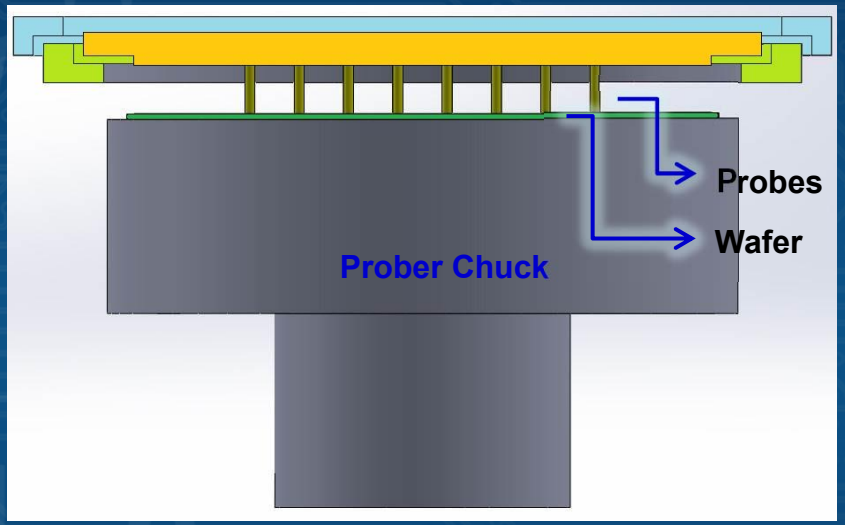


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Soaking Requirement During Probing

- **Stability during test**
  - Preheat first die with contact
  - Require additional soaking for long pauses
  - Realignment after preheat



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Condensation

- **Environment temperature cause condensation**
  - Condensation inside prober and on the probe card
- **Preventive Measures**
  1. Probe card sealing
     - Probe head
     - PCB thru hole
  2. Dry air purge of probe card
     - Dry air displaces humidity around the probe card to prevent condensation during low temperature probing



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Device description

- **Tester platform is Teradyne J750, Aurora tower**
  - PCB is directly in contact with the card holder
  - External stiffener cannot be implemented
- **Product details**
  - Pin count: 159
  - Pad layout: peripheral, 2 rows
  - Array size: 3 mm x 3 mm
  - Min pitch: 100 µm
  - Min pad opening: 60 x 90 µm
  - Pad metallurgy: Al pads

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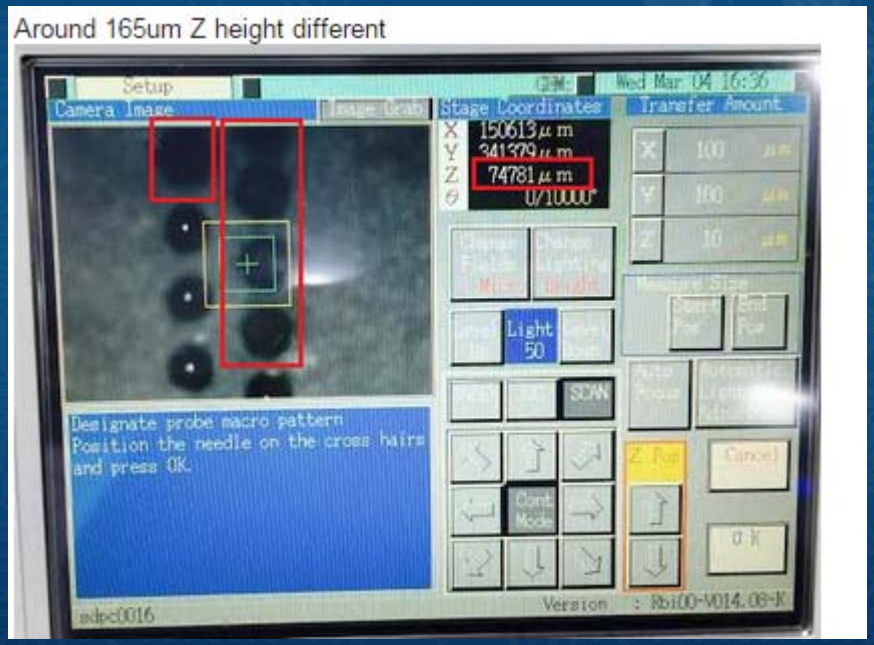
Production probing issues

- **Production was suffering of several issues with reference Vendor PCs**
  - Frequent floating needle issue during extreme high and low temperature testing.
  - Constant probe realignment requirement for high temperature testing.
  - Continuity and yield issues
  - High cost Polisher material to maintain probe's contact resistance during high temperature testing.

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Production probing issues

- **Excessive pin floating: PH mechanical issue**
  - Float issue higher than 150um < happen frequently during high/low temperature testing and exit maximum spec 50um.





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Production probing issues

- **Z height variations at high T**

Uneven probe height cause prober unable to align is magnified at high Temp
After re-seat the probe head, uneven height still exist

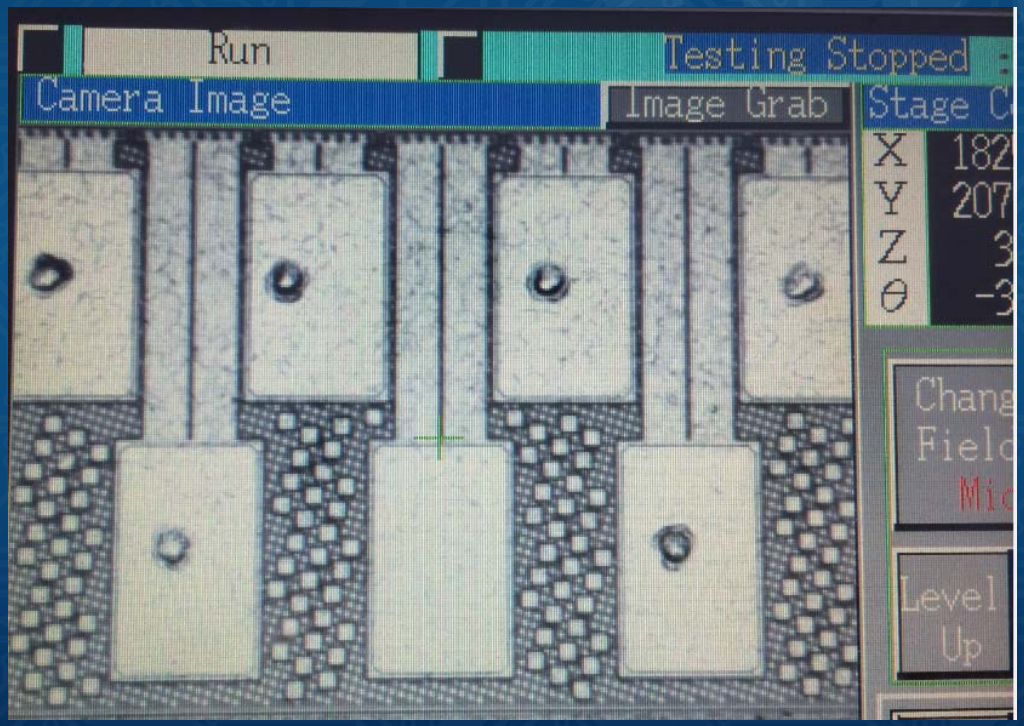


250uM height different

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Production probing issues

- **Missing probe marks**
  - Additional probe alignment required every 5mins to avoid probe mark shift

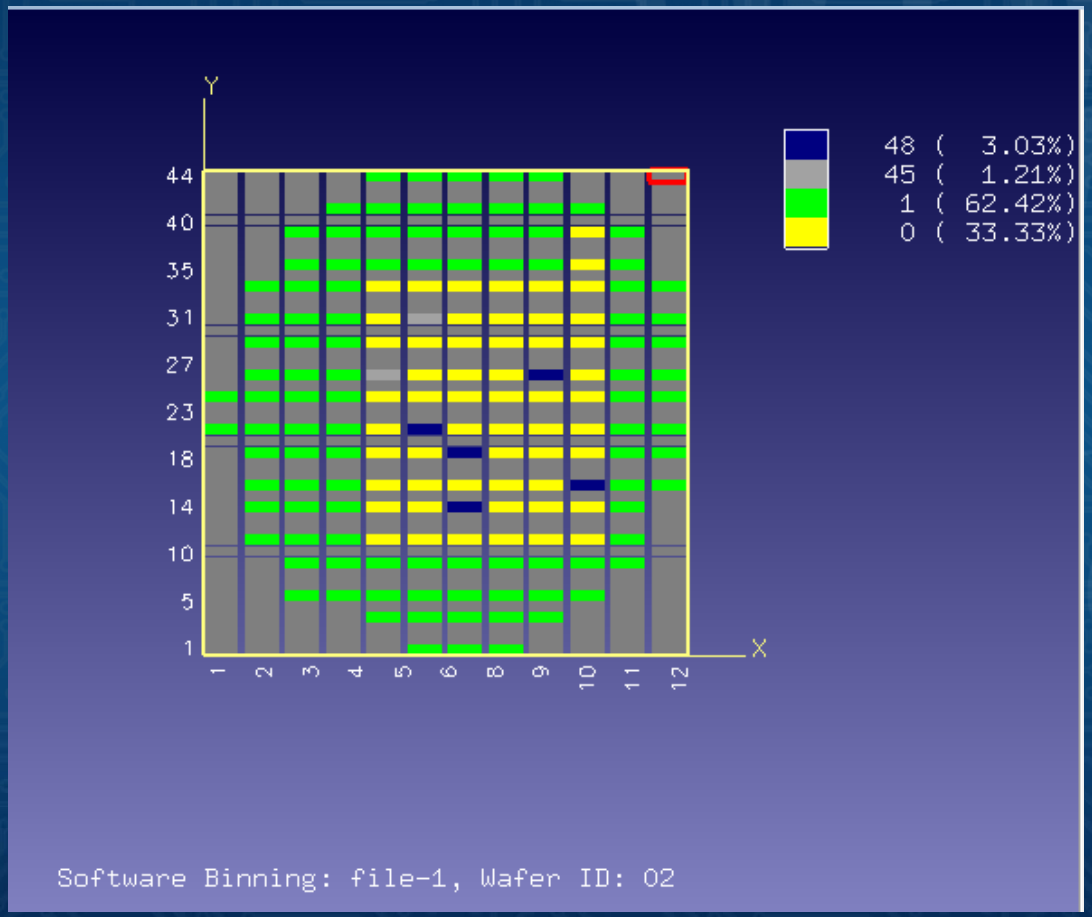


Probe mark with OD 65um

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Production probing issues

- **Contact issues: opens**



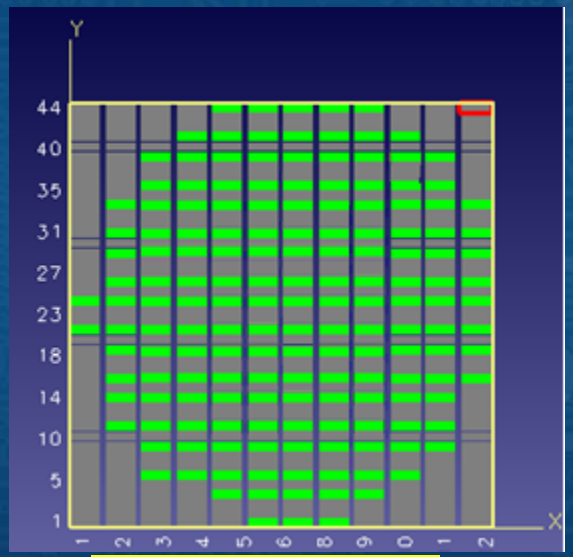
Sbin1 is conti fail dies, all fail OPEN at data_15

FormFactor Ex. 1031, p. 152

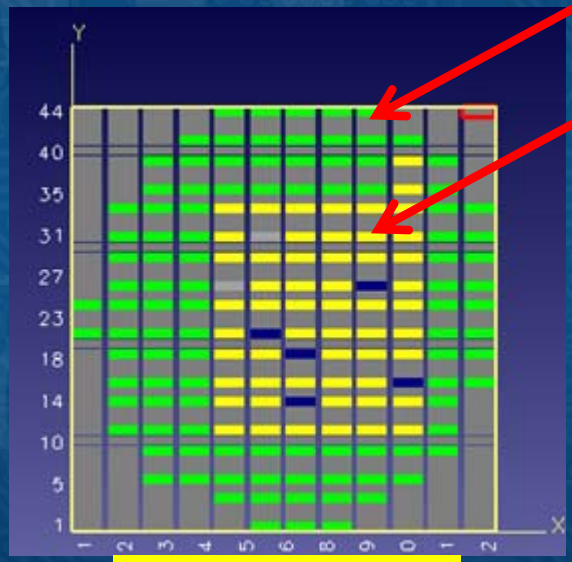
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Production probing issues

- **Observed continuity issue at wafer center from 2nd wafer onwards**



First wafer



Next wafer

Good probemarks

Issue probemarks

Yellow color = continuity failure bin

FormFactor Ex. 1031, p. 153

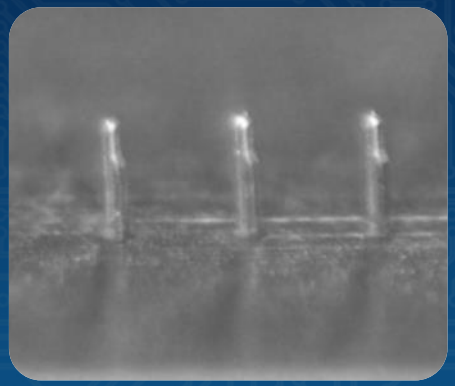
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Technoprobe probe card introduction

- Technoprobe developed a dedicated design, to achieve a weak mechanical interaction between PH mechanics and PCB
- Besides, sealing is applied to isolate prober interior from external environment and prevent condensation during low temperature testing
- PH technology is based on TPEG™ MEMS T1, specifically developed to address probing of Al pads and POAA from -55°C up to + 200°C

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TPEG™ MEMS T1 main features



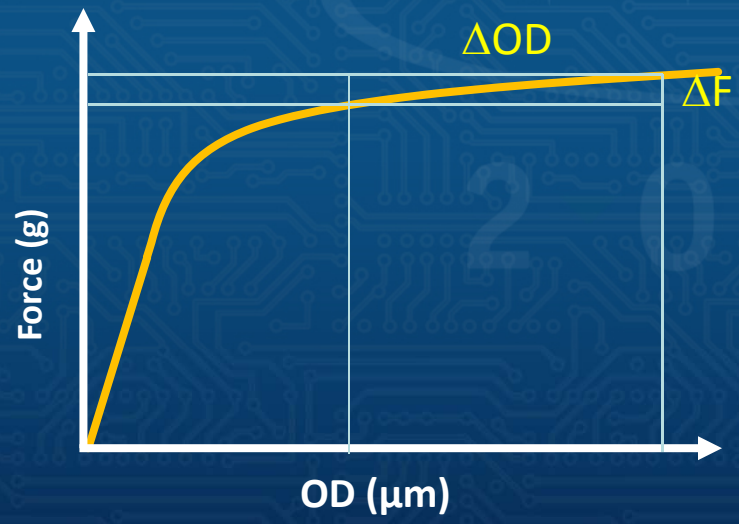
PARAMETER	TPEG™ MEMS T1
Needle diameter	1,5 mils equivalent
Max pin count	> 20.000 pins
X, Y alignment accuracy and Z planarity	X,Y: ± 8 µm; Z plan: Δ 20 µm
Min pitch and configuration	55 µm linear configuration
Pin Current (CCC)	410 mA
Force (at 3 mils OT)	3 g

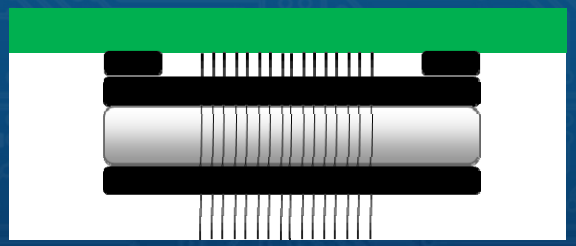
FormFactor Ex. 1031, p. 155

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Buckling Beam Concept

- Technoprobe PH mechanics exploits buckling beam: small force variation (ΔF) vs large OD variation (ΔOD)
- Buckling starts to occur at about 25 µm of actual OD
- Force is almost constant in the working OD range





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PH technology comparison

- **Following table is showing a comparison between Reference Vendor and TP TPEG™ MEMS T1 probing solution**

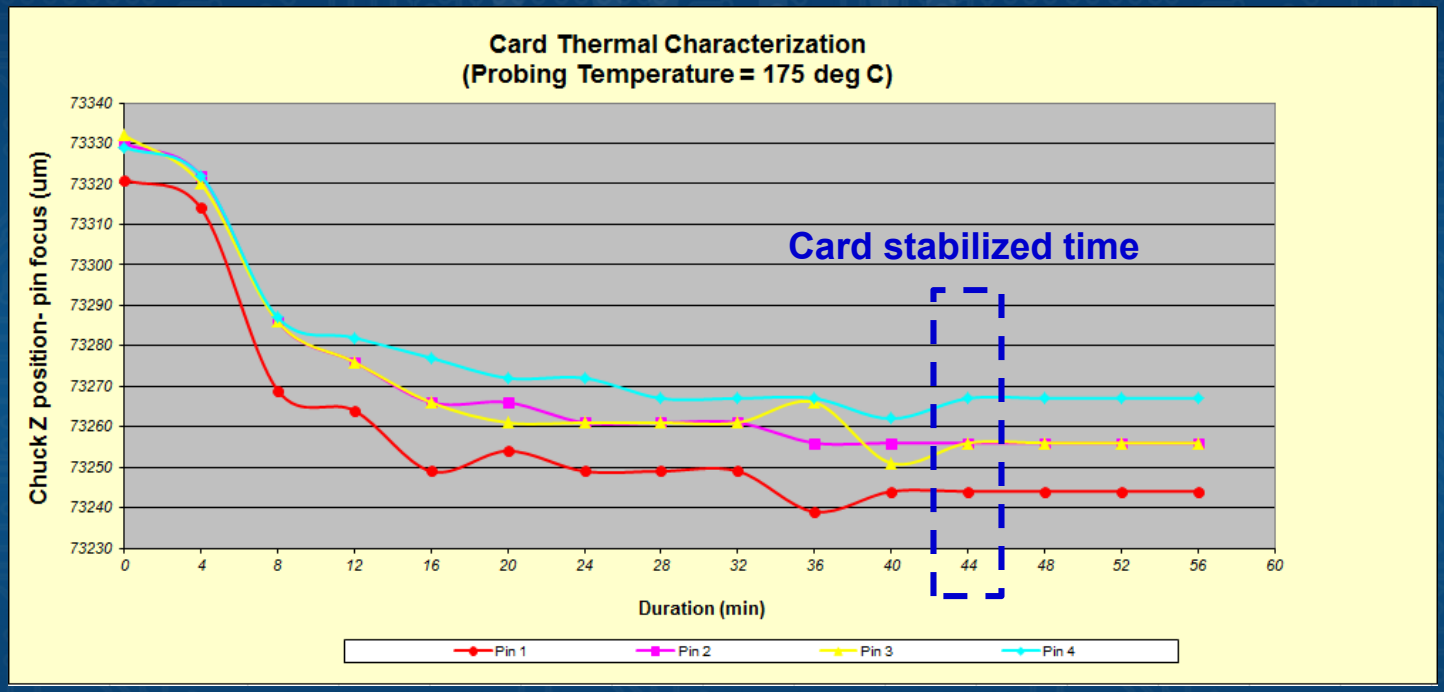
Parameter	Reference Vendor Buckling probe	Technoprobe TPEG™ MEMS T1
Needle diameter	2 mils	1.5 mils equivalent
Max Pin count	1700	> 20K probes
Min Pitch Array	75 um	80 um full array (55 µm linear)
X,Y alignment	±12 um	± 8 um
Z Planarity	20 um	20 um
Force (3 mil OD)	4,5cN with 100um OD	3g
Probe Length	8.5 mm	6.3 mm

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Stabilization at 175 °C

- **Card preheating at 200 µm over the chuck**



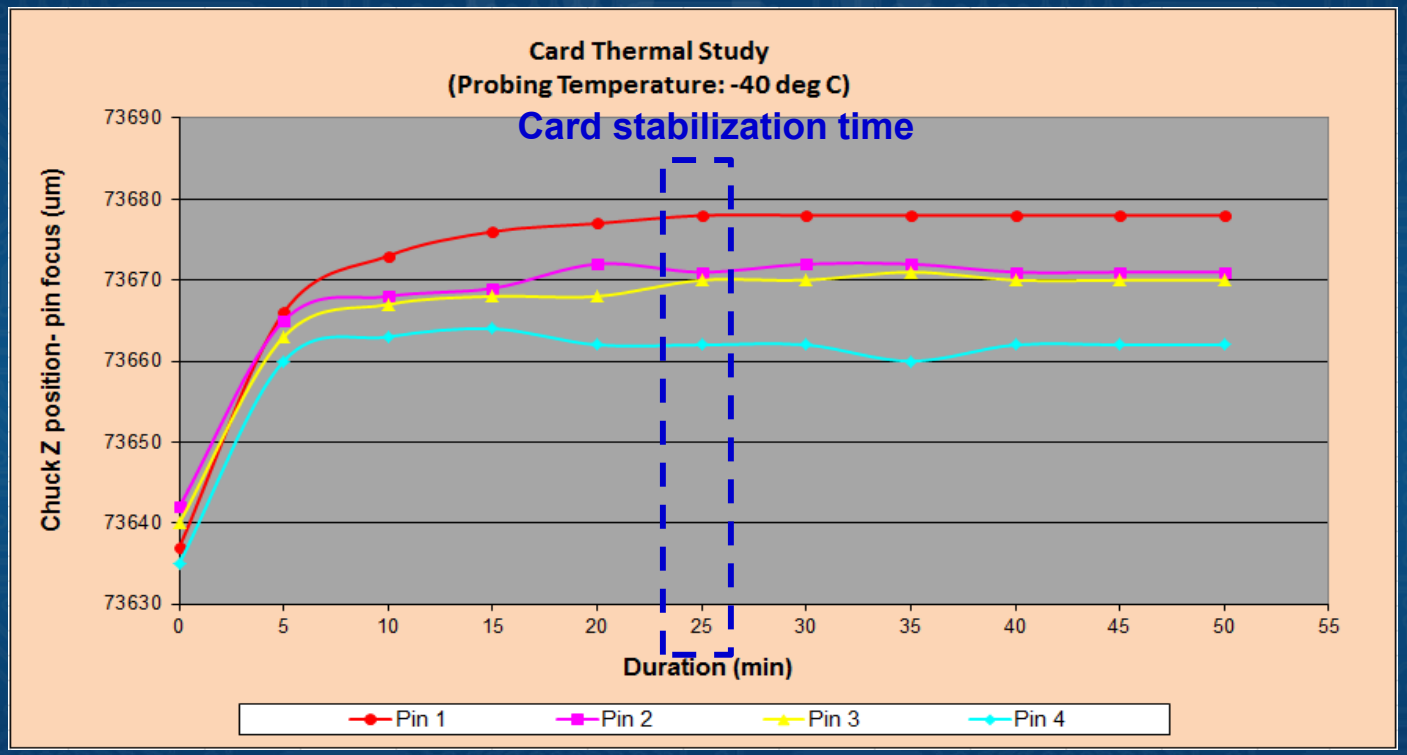
Duration(Min)		0	4	8	12	16	20	24	28	32	36	40	44	48	52	56
Reference Pins (um)	Pin 1	73321	73314	73269	73264	73249	73254	73249	73249	73249	73239	73244	73244	73244	73244	73244
	Pin 2	73330	73322	73286	73276	73266	73266	73261	73261	73261	73256	73256	73256	73256	73256	73256
	Pin 3	73332	73320	73286	73276	73266	73261	73261	73261	73261	73266	73251	73256	73256	73256	73256
	Pin 4	73329	73322	73287	73282	73277	73272	73272	73267	73267	73267	73262	73267	73267	73267	73267

FormFactor Ex. 1031, p. 158

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Stabilization at -40 °C

- **Card precooling at 200 µm over the chuck**

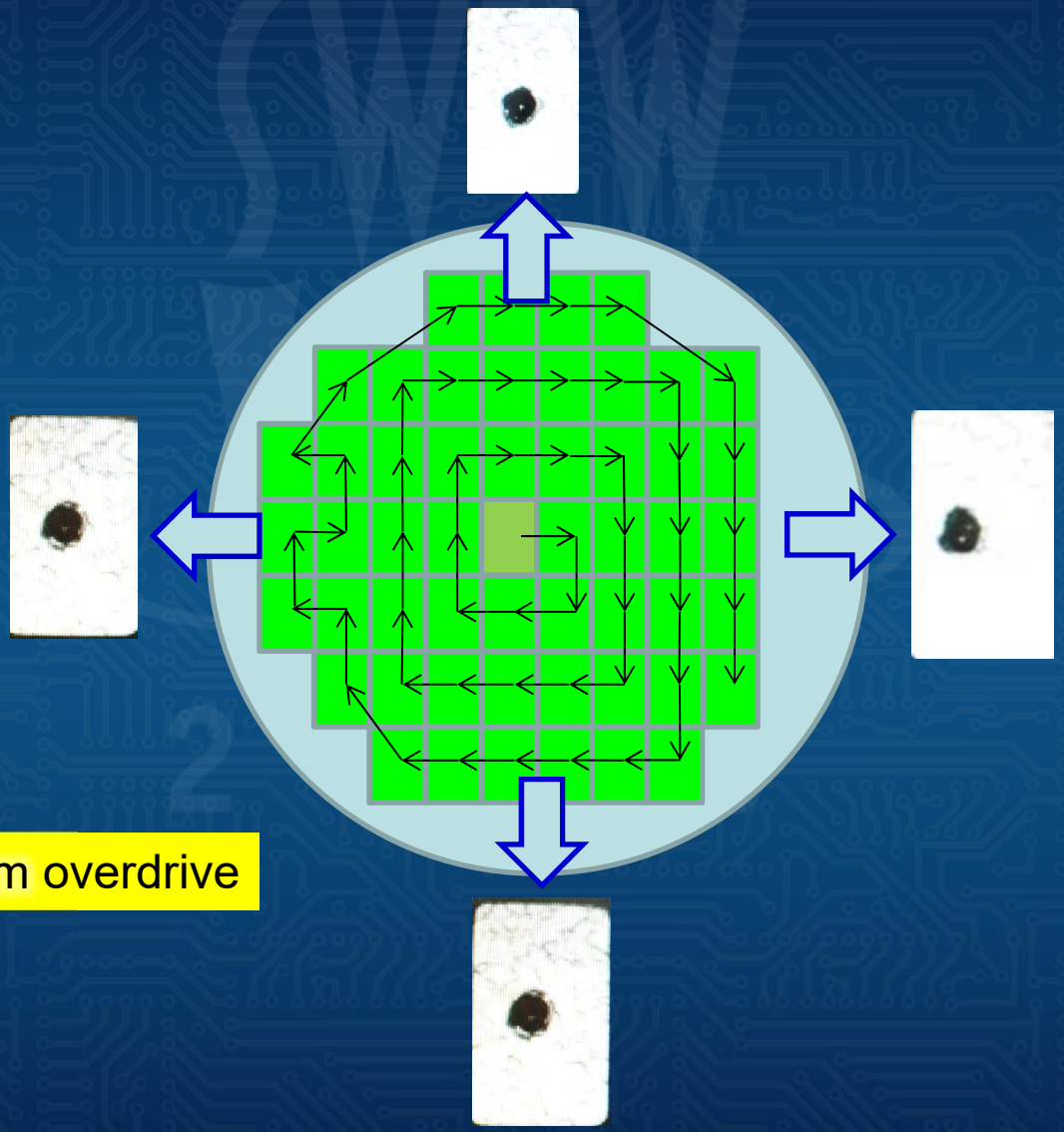


	Duration (min)	0	5	10	15	20	25	30	35	40	45	50
Reference pins (um)	Pin 1	73637	73666	73673	73676	73677	73678	73678	73678	73678	73678	73678
	Pin 2	73642	73665	73668	73669	73672	73671	73672	73672	73671	73671	73671
	Pin 3	73640	73663	73667	73668	73668	73670	73670	73671	73670	73670	73670
	Pin 4	73635	73660	73663	73664	73662	73662	73662	73660	73662	73662	73662

FormFactor Ex. 1031, p. 159

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Probe Mark Profile at 175°C

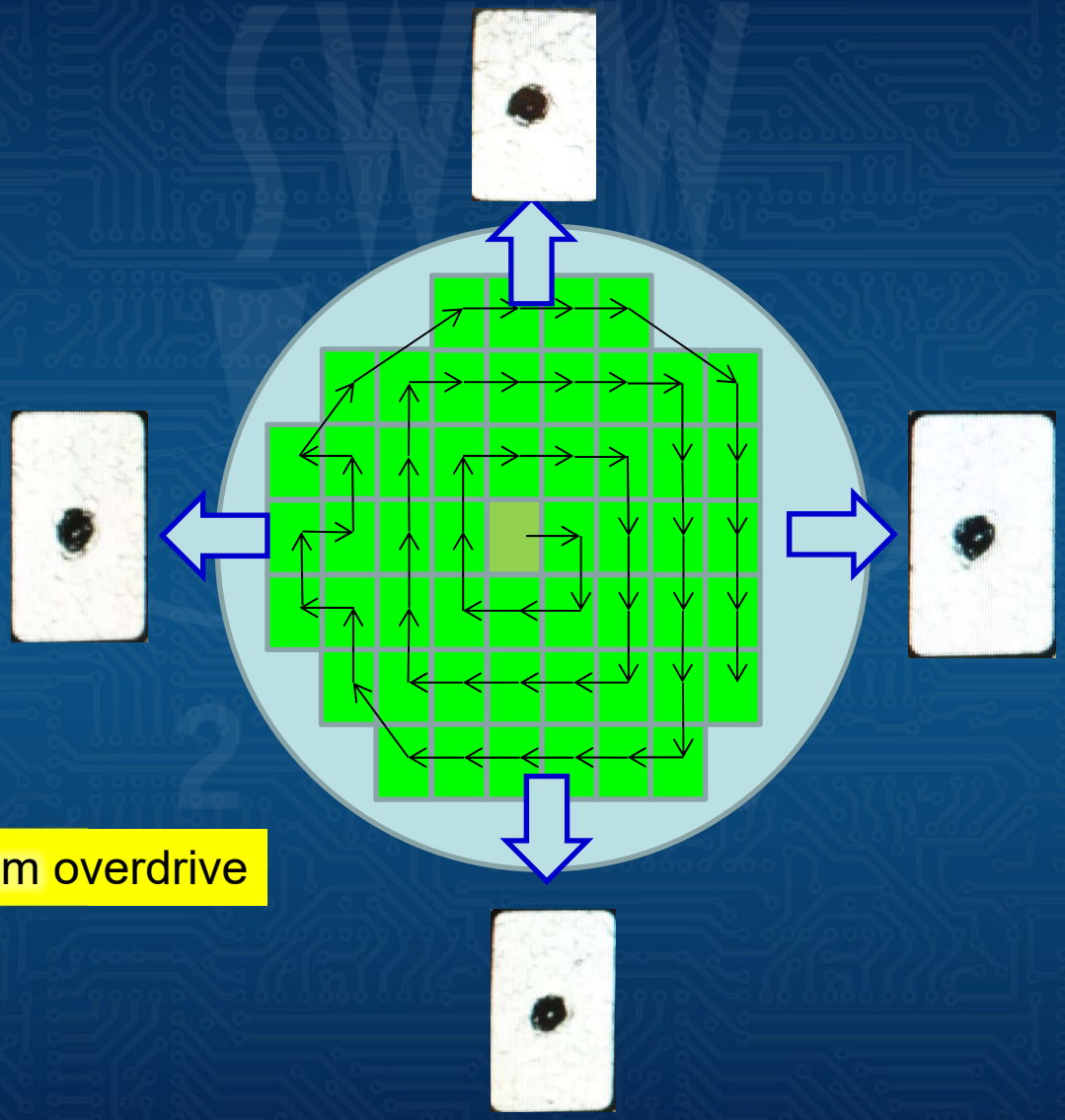


Probing with 50µm overdrive

FormFactor Ex. 1031, p. 160

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Probe Mark Profile at -40°C



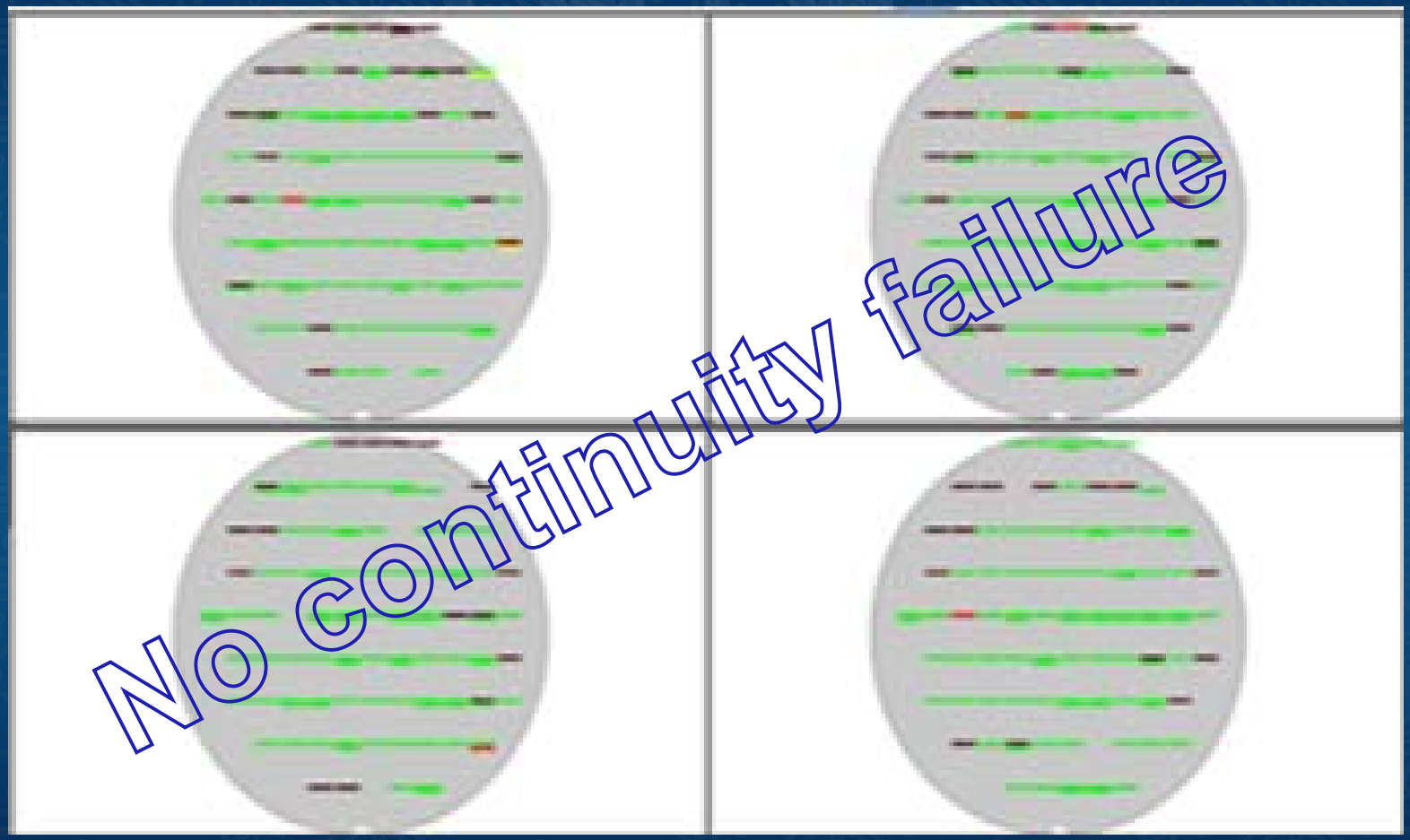
Probing with 50µm overdrive

FormFactor Ex. 1031, p. 161

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Test Results

Continuity failure bin



FormFactor Ex. 1031, p. 162

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Benchmark summary

- **Following table is showing the prober and cleaning setup comparing today reference vendor with respect to Technoprobe probing solution**

Category	Reference Vendor	Technoprobe
Prober Type	TEL P12	TEL P12
Probing OD	70~80 um (max125um)	50 um (max 100 um)
Soaking Time, if any	2 hours	2 hours
Preheat Setting, if any	30 mins	45 mins - HT 25 mins - cold
Cleaning settings:		
Cleaning Media	ITS PP99	Mipox WA6000
Cleaning OD	70~80 um	50 um
Cleaning Frequency	20 index	100 index
Auto Alignment, if any	Every 5 mins	None

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Conclusions

Solutions to extreme temperature probing:

- **Fine tuning soaking recipe**
- **Optimize probing sequence**
- **Avoiding condensation**
- **Additional soaking requirements**
- **Technoprobe probe card design and probe technology demonstrated to be a production worthy solution**

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Acknowledgements

GLOBALFOUNDRIES

- Shi Binglin
- Joy Chang Hui Shan
- Xing Yao
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- Man Guo Chang
- Eddy Lo

TECHNOPROBE

- Raffaele Vallauri
- Emanuele Bertarelli
- Hellen Kee

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SWTW 2016

SW Test Workshop
Semiconductor Wafer Test Workshop

High Voltage, High Temperature, High Current... ...and sometimes all come together at the same time!

Dr. Gerhard Schmidt
Infineon Technologies Austria AG

Georg Franz , Dr. Rainer Gaggl
T.I.P.S. Messtechnik GmbH

June 5-8, 2016

Overview

- High Power Devices - Challenges for Wafer Test
- ...some Physics

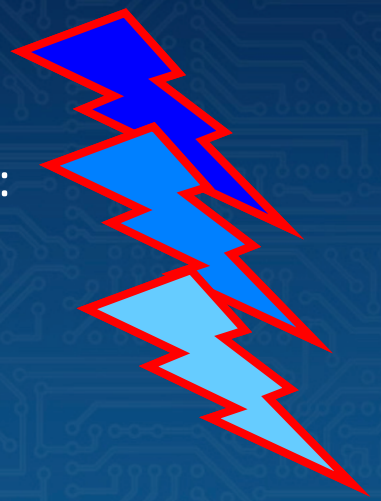
- High Voltage + High Temperature: "Why's that?"
- Lab Test: Full Wafer HV – HT contactor

- Production Test: SiC, GaN and more...
- "Hot-Cold Air Stream" High Voltage Probe Card

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High Voltage on Wafer – Challenges

- **HV Flashovers**
  - If test voltage exceeds insulation strength of atmosphere:



- **known as "arcing", "sparks", "flashovers"**
  - can have unwanted effects for device under test ...

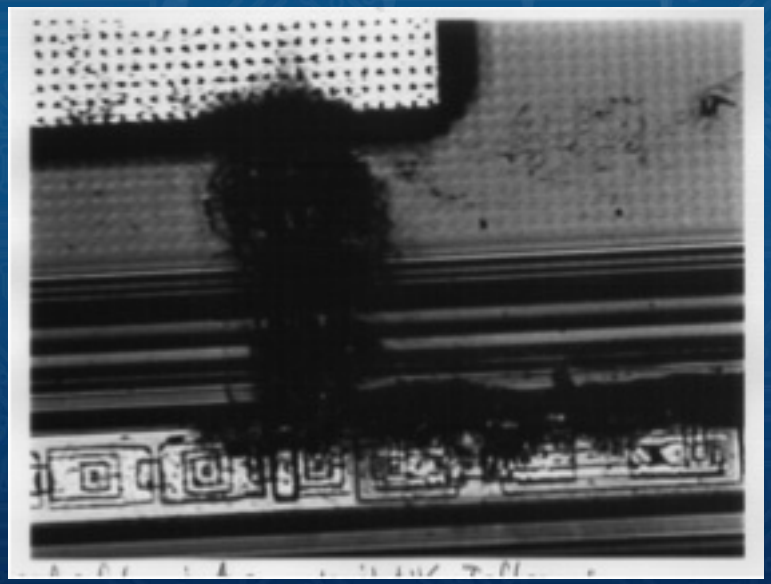


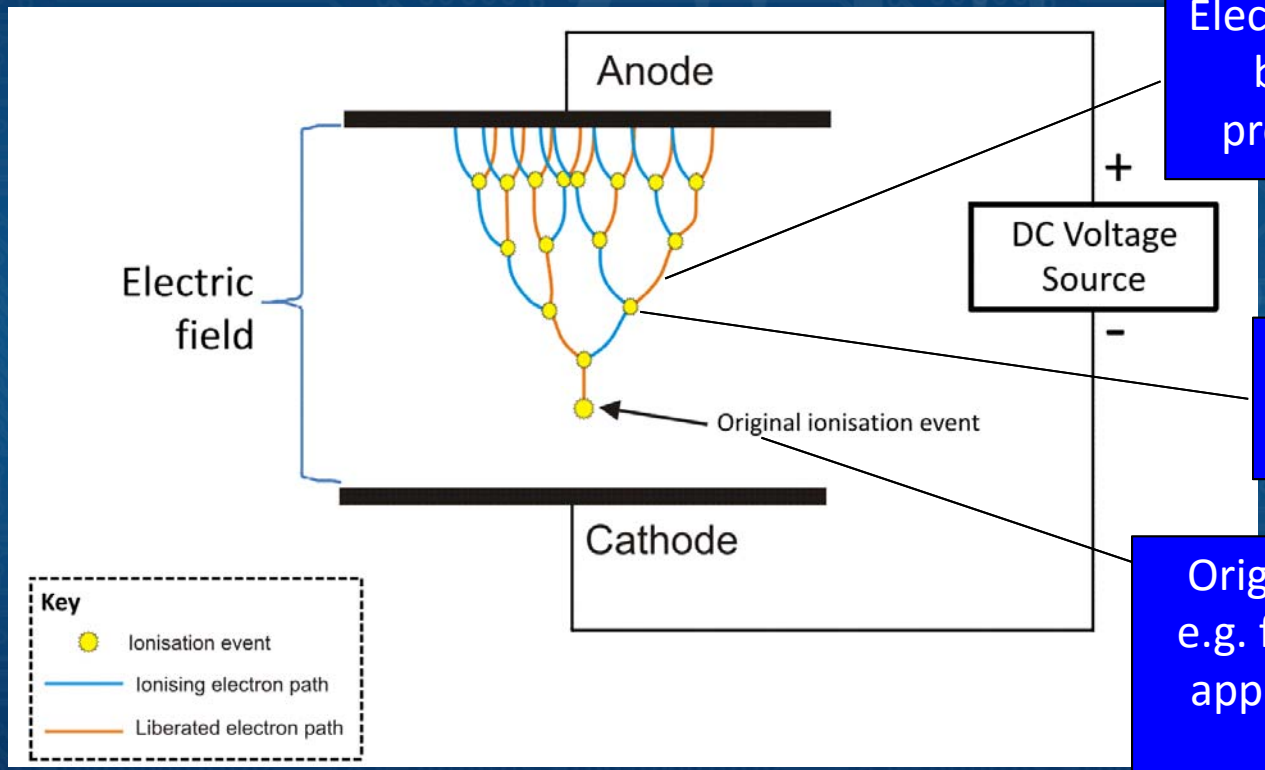
Fig. 1: Damage on wafer surface (IGBT) due to flashover between source-pad and dicing frame structure

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High Voltage – some Physics...

- **Flashover Mechanism: Avalanche Ionization of Gas Molecules, "Arc Discharge"**



Electrons, mean free path between collisions: pressure, temperature

Gas molecules: ionization energy

Original ionization event: e.g. from cosmic radiation, approx. 1 event / second in one cm^3

Fig. 2: Visualisation of a Townsend Avalanche *)

*) picture source: Wikipedia

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...more Physics !

- **Physics of "Gas Discharges"**
  - first described by Friedrich Paschen in his PhD thesis in 1889: [1)]

"Breakdown voltage between two electrodes in a gas is a function of gap distance and pressure" (Paschen's law).

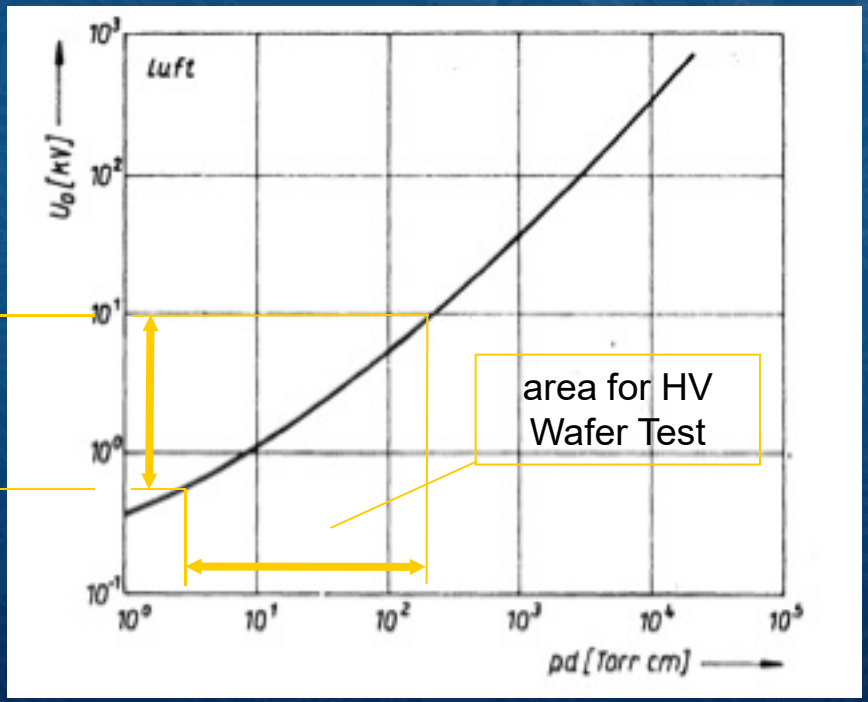


Fig. 3: Paschen Curve for air [2)]



Friedrich Paschen [*)]

*) picture source: Wikipedia

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High Voltage and Temperature...

- **Ideal Gas: Molecule density is temperature dependent**
  - the higher the temperature, the lower the molecule density - and the higher the mean-free path for a given pressure e.g. atmospheric pressure
  - increased mean-free-path length leads to lower flashover voltage
  - mathematical description by the "Ideal Gas Law": $p\,V = n\,R\,T$
- **Thus: Increasing pressure -> increased arcing voltage**
- **Increasing temperature -> decreasing arcing voltage**
  - rules of thumb:
    - ***Doubling (absolute) pressure will double arcing voltage .***
    - ***Increasing test temperature from room temperature 23 °C to 150 °C will decrease arcing voltage by 33 % - or require pressure increased by 50 % (absolute) to compensate for.***

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Case 1: Hot Temp and High Voltage Lab Test... "Why's that?"

- **Characterization of Temperature Dependence of Avalanche Breakdown in IGBT Termination Structures**
  - needed during development of "VLD (variation of lateral doping) termination structure" – Infineon Technologies

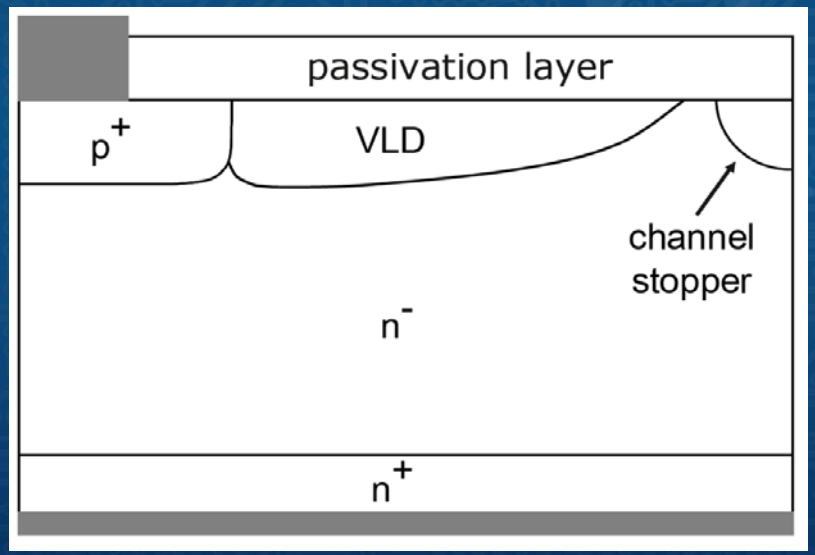


Fig. 4: Schematic cross section of VLD termination structure [3)]

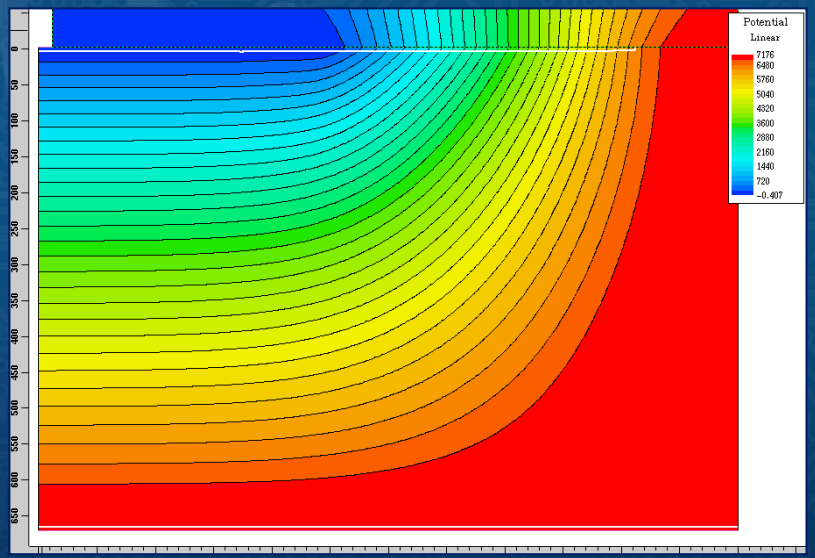


Fig. 5: Simulation of electric field in termination structure at U = 7200 V

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New chip design - HV verification

- **Measurement task: HV blocking capabilities of different chip design versions over temperature**

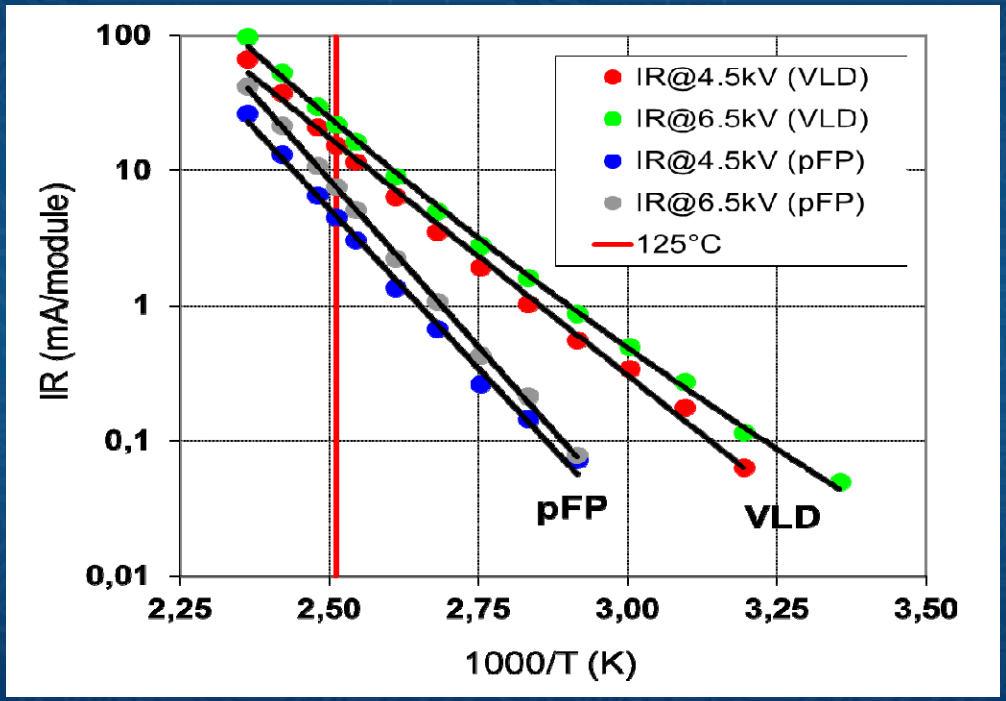


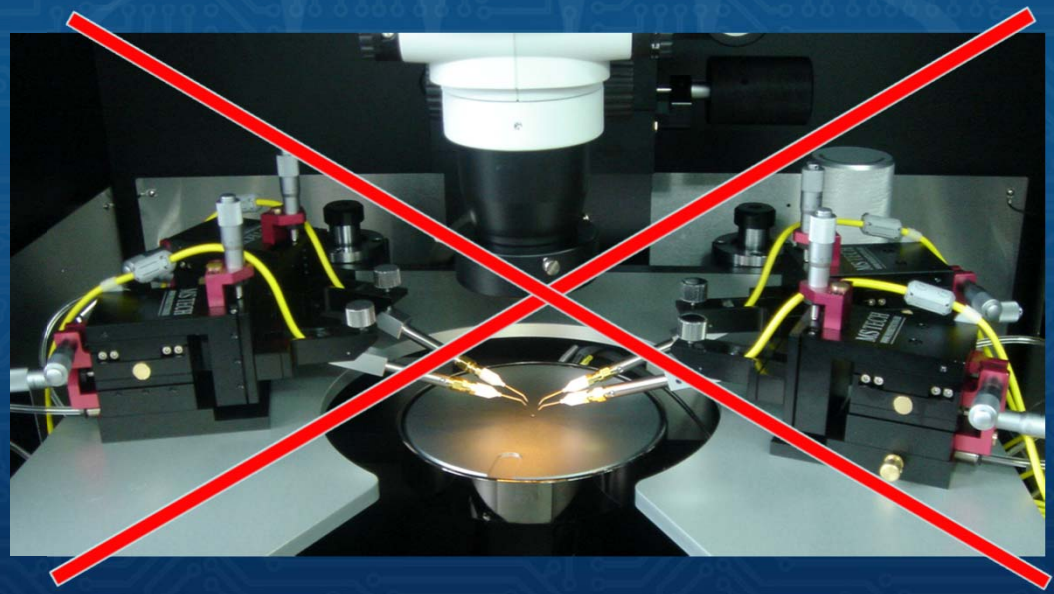
Fig. 6: Leakage current for IGBTs with different termination structures as a function of temperature [3)]

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HV chip design verification

- **High numbers of measurements to be done for good statistical significance**
  - "Classic" laboratory characterization approach with manipulator probes is extremely time consuming due to complicated chip preparation required – wouldn't meet timelines requested...

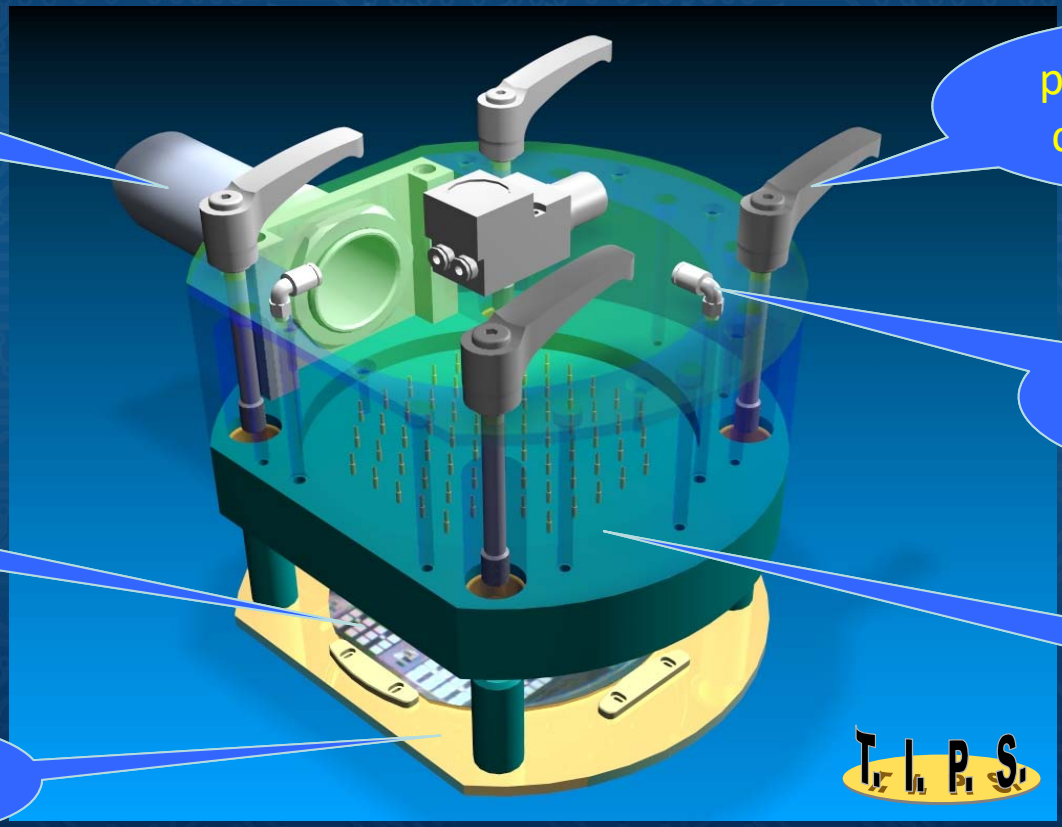


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HV Full Wafer Contactor

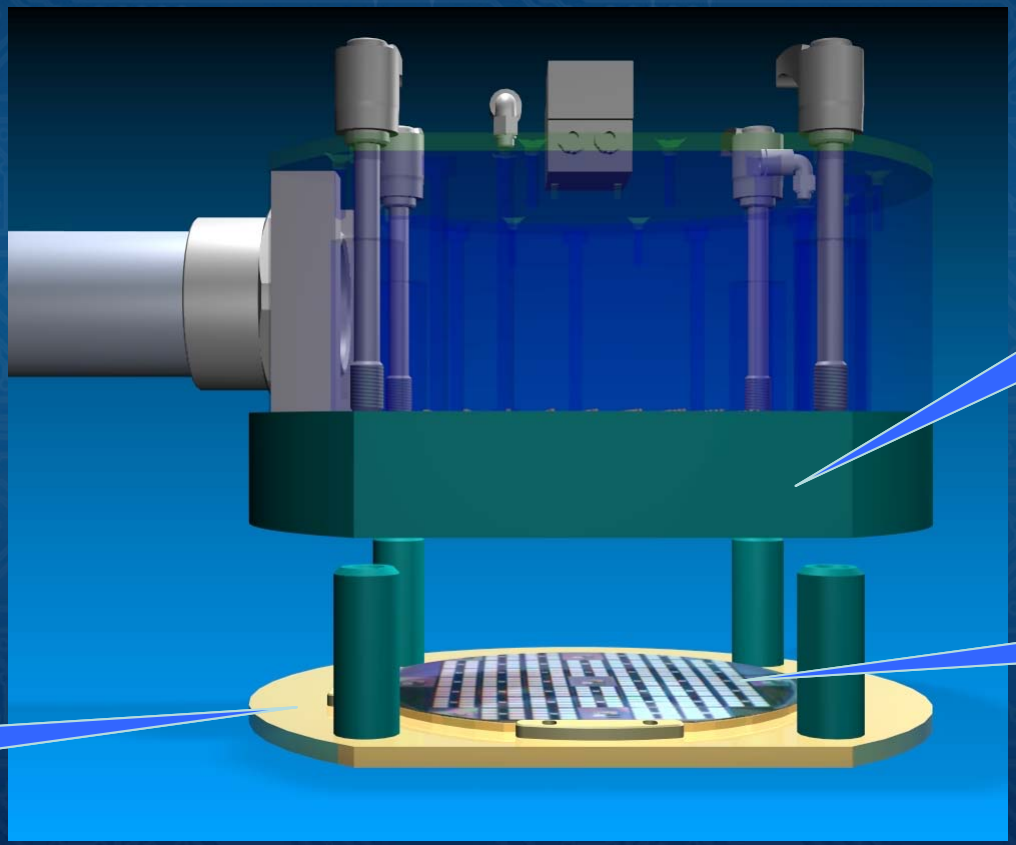
- **6" full wafer wafer single touchdown, 80 x parallel test, 10 kV capable, - 40 °C - 175 °C, max. 4 bar pressure vessel**



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HV Full Wafer Contactor (2)

- "non-gas-loss" design: instead of compressed air also use of compressed HV insulating gas (SF6) is possible



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Summary – Lab Test Setup

- 6" full wafer contactor allows fast high voltage characterization of HV IGBT and diodes and greatly speeds up development for new HV chip designs.
- Full temperature range coverage from – 40 °C – 175 °C,
- lossless pressure vessel allows (restricted) use of insulating gases (e.g. SF6) for most demanding applications
- Very low parasitic current leakage (1 nA @ 10 kV)

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Case 2: Production Wafer Sort

- **Device under test: one of the "exotic" SiC, GaN... specimens**
- **900 V – 20 A – 175 °C – and very narrow HV structures**
  - First proposal: use off-the- shelf TIPS High Voltage "LuPo" probe card with floating air bearing seal, supplied with compressed air at ambient temperature, hot chuck

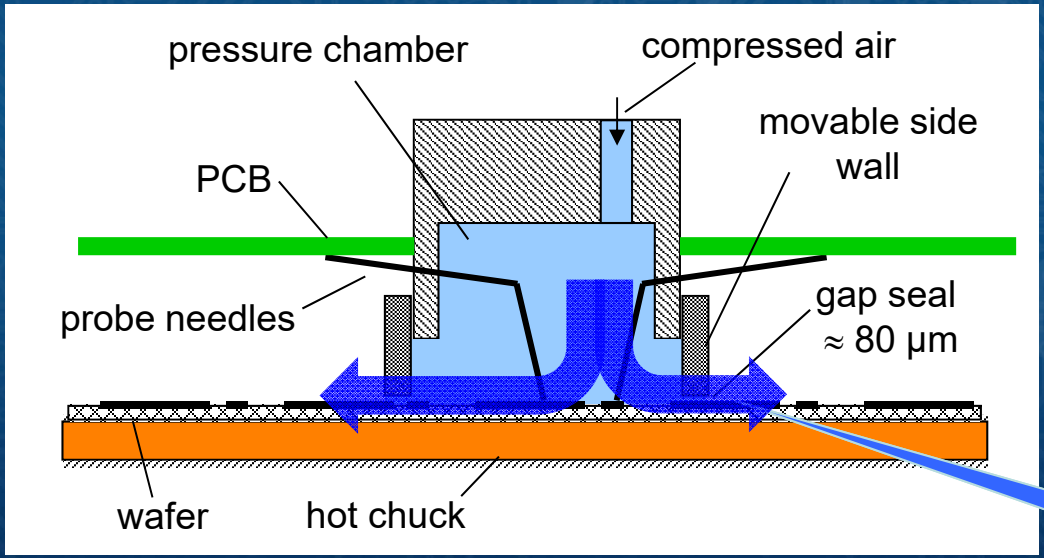


Fig. 7: Schematics of compressed air "LuPo" probe card

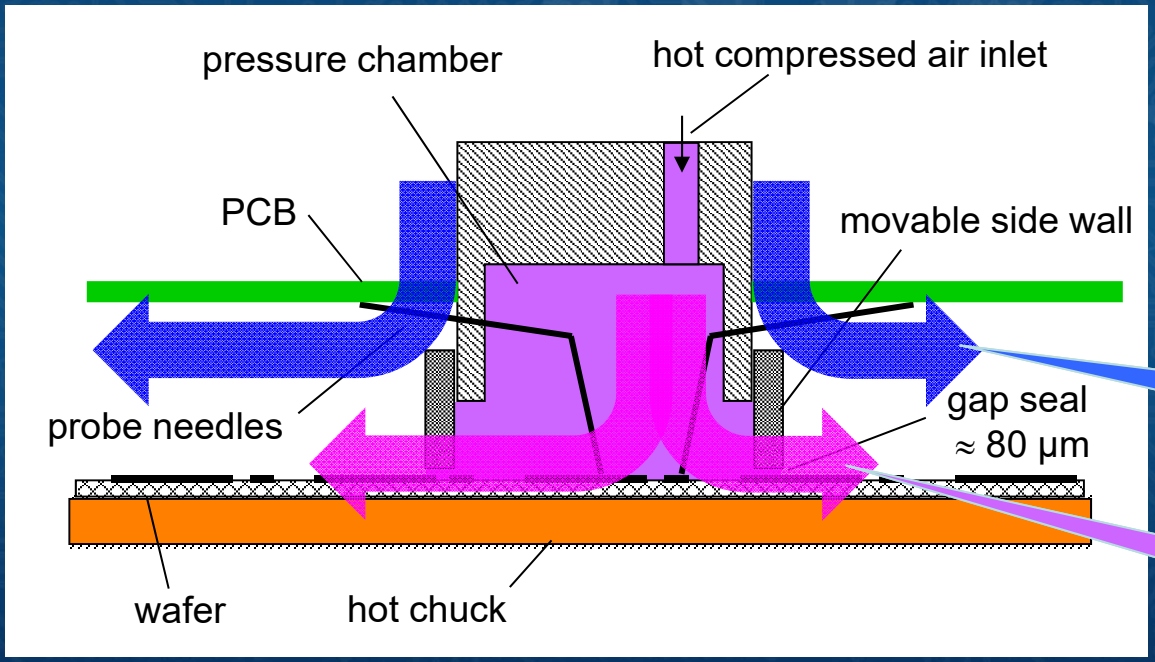
- Air flow causes sharp temperature drop at DUT location
- Thermo-Chuck temperature control "dances polka" when facing local chuck cooling.

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Hot-Cold-Airstream Probe Card

- compressed hot air at chuck temperature to create hot compressed air test emvironment
- cold air stream to insulate probe card components from heat



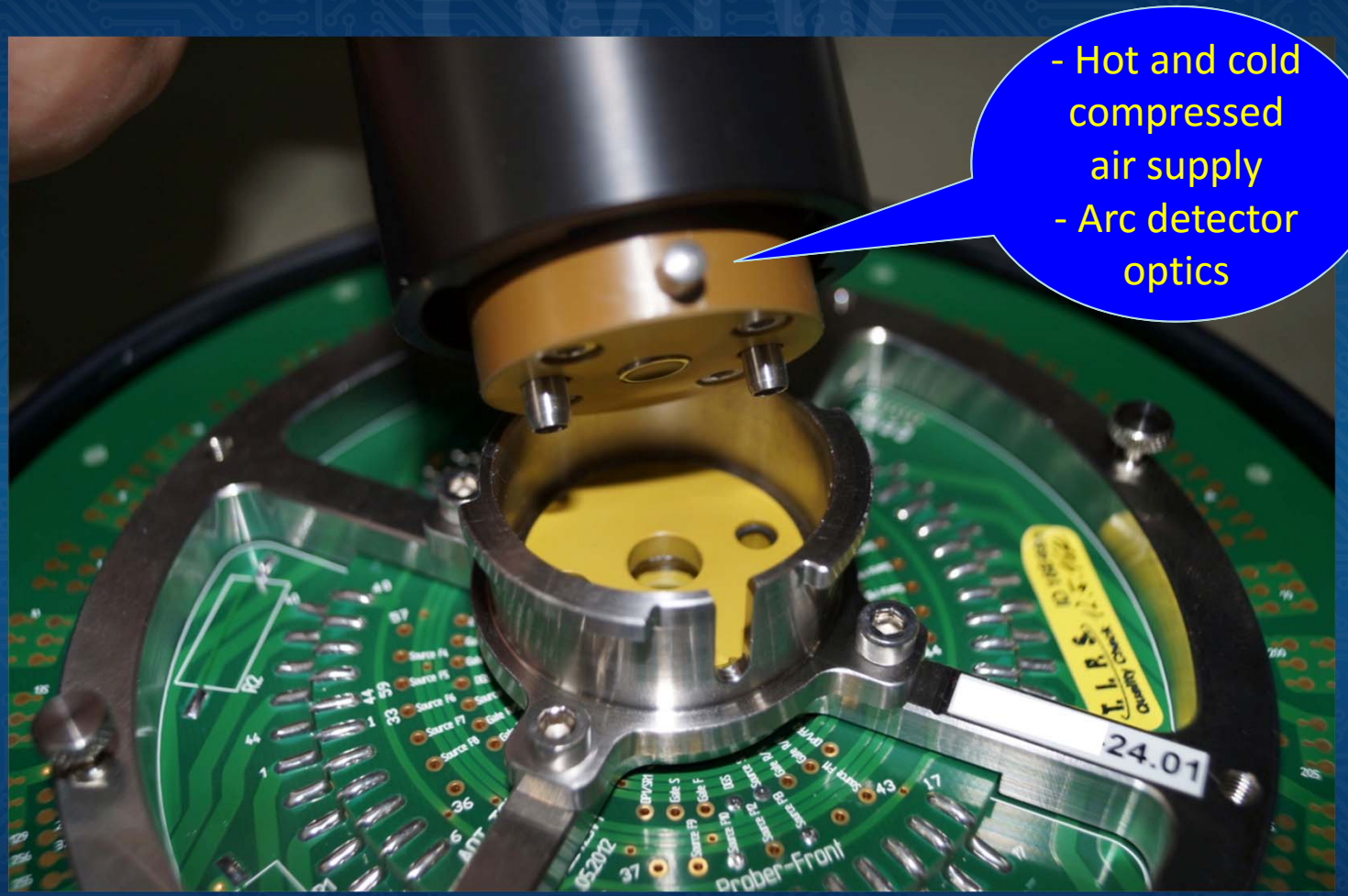
FEM computation used to "tune" thermal gradients during probe card mechanical design

Fig. 8: Schematics of Hot-Cold-Airstream "LuPo" probe card

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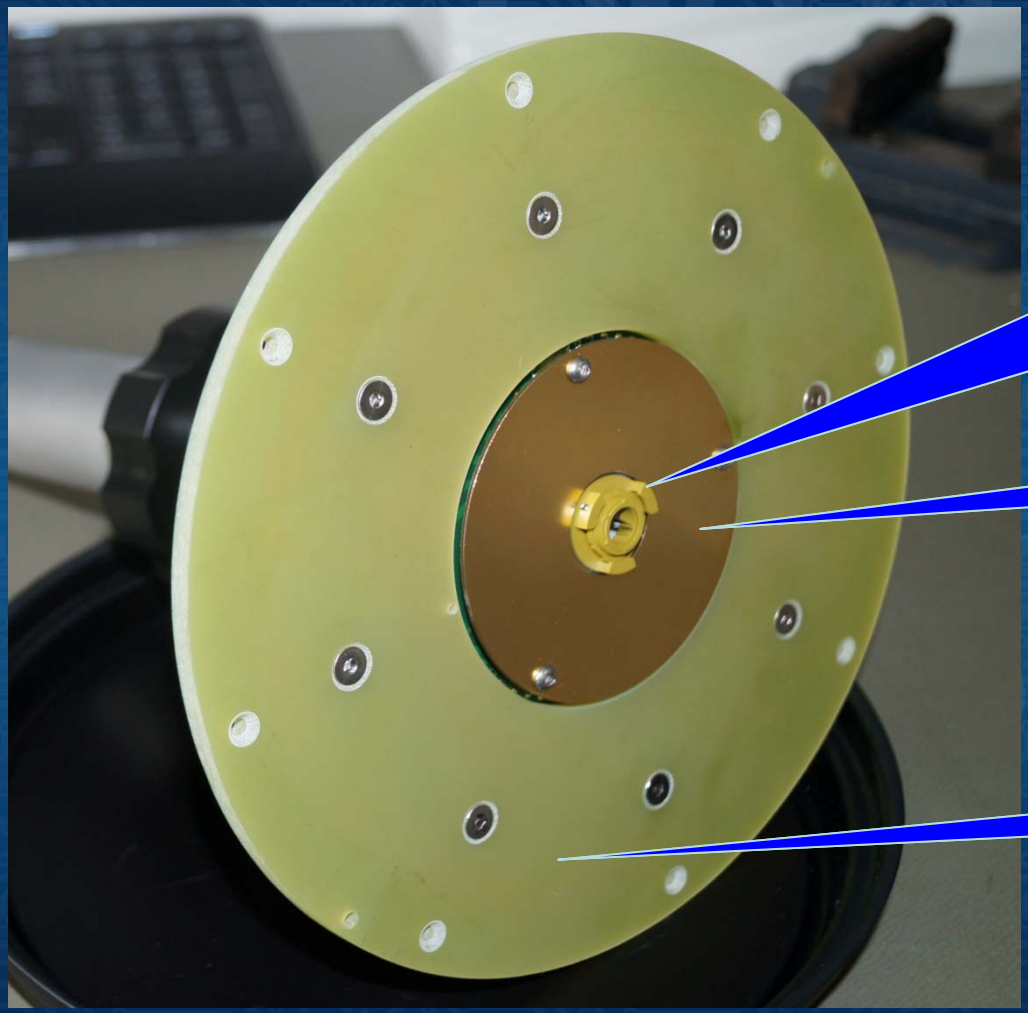
Hot-Cold-Airstream Probe Card (2)



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Hot-Cold-Airstream Probe Card (3)



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Conclusion

- High Voltage – High Current – High Temperature wafer probing is feasible – but with "hard constraints" imposed by physics
- For production test: It's like having a hot air gun inside your prober – So if you can avoid it...
- If you can't avoid it...
  ....at least be careful not to burn your fingers! ☺

Thank you for your attention!

FormFactor Ex. 1031, p. 182
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IPR2024-00933

References

1) **"Ueber die zum Funkenübergang in Luft, Wasserstoff und Kohlensäure bei verschiedenen Drucken erforderliche Potentialdifferenz"**, F. Paschen, Annalen der Physik, vol. 273, no. 5, pp. 69 – 96, 1889

2) **Der elektrische Durchschlag in Gasen**, H.Hess, Vieweg Verlag 1976, ISBN 3528068183 9783528068189

3) **6.5kV IGBT and FWD with Trench and VLD Technology for reduced Losses and high dynamic Ruggedness**, Thomas Duetemeyer1), Josef-Georg Bauer2), Elmar Falck2), Carsten Schaeffer3), G. Schmidt3), Burkhard Stemmer1), PCIM Europe 2008 Conference Proceedings, ISBN: 978-3-89838-605-0

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FormFactor v. Technoprobe IPR2024-00933

SW Test Workshop
Semiconductor Wafer Test Workshop

2016

Multi-site probing of magnetic sensors at 175 deg C

Melexis
Microelectronic Integrated Systems

JEM

Geert Gouwy, Melexis

Josef Mai, JEM

June 5-8, 2016

Agenda

- Melexis company overview
- Basics : magnetic switches, triaxis®
- Test requirements, challenges & test cell considerations
- Concept & system setup
- Flowchart probe card evaluation
- Evaluation criteria & achievements
- Future work

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Melexis supplies worldwide average 7 ICs / car

Sensing

- Speed
- Position
- Current
- Pressure
- Temperature
- Light
- Image

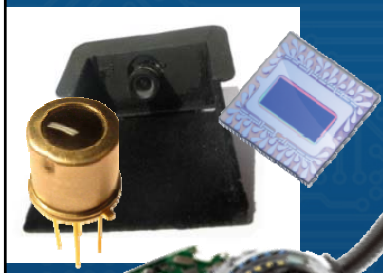


Driving

- BLDC / DC Motor Drivers
- Smart Drivers













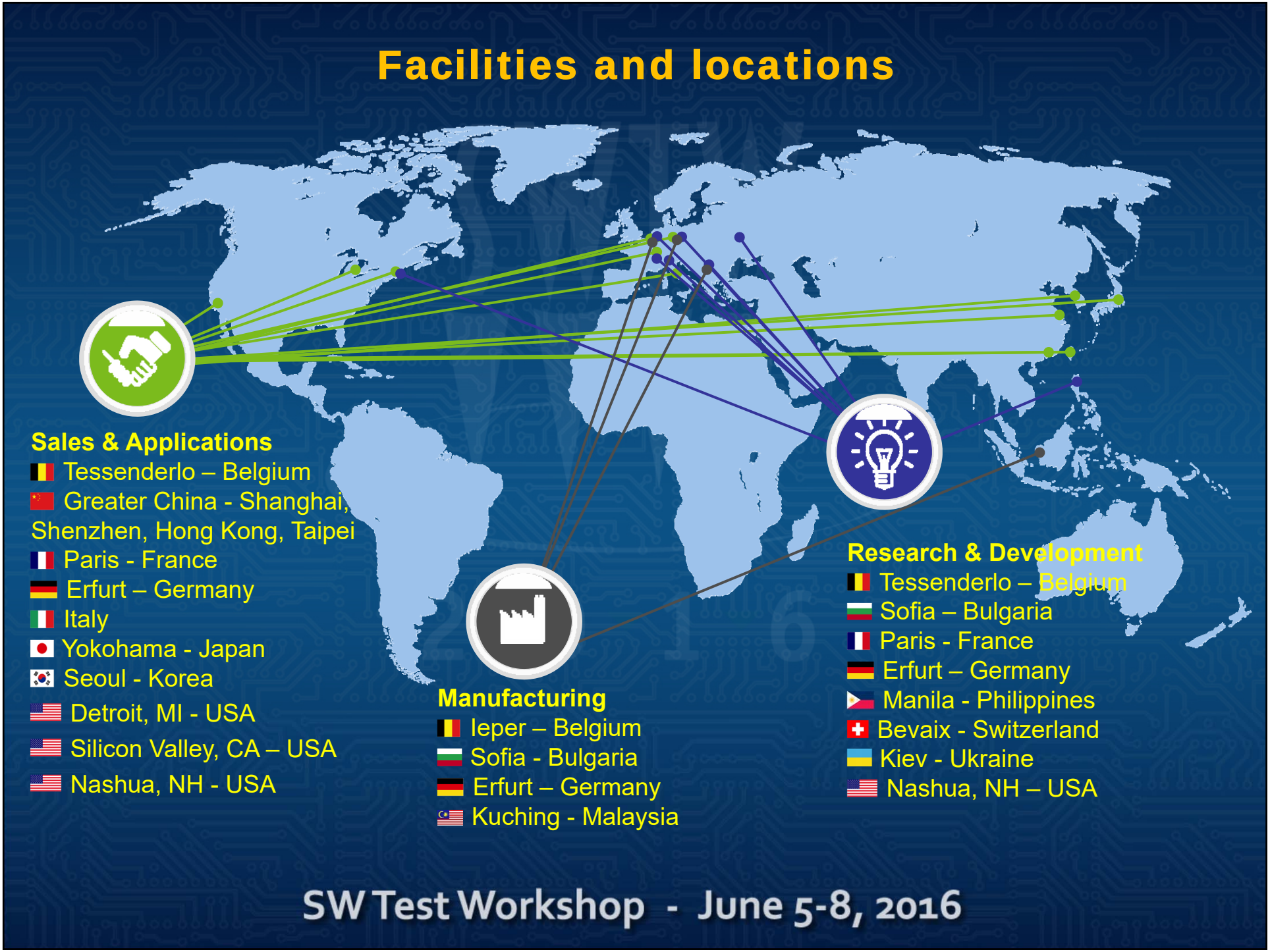
Communicating

- Wired SW CAN, SENT and LIN
- Wireless RF & RFID / NFC

Combining into Systems

SW Test Workshop - June 5-8, 2016

Facilities and locations



SW Test Workshop - June 5-8, 2016

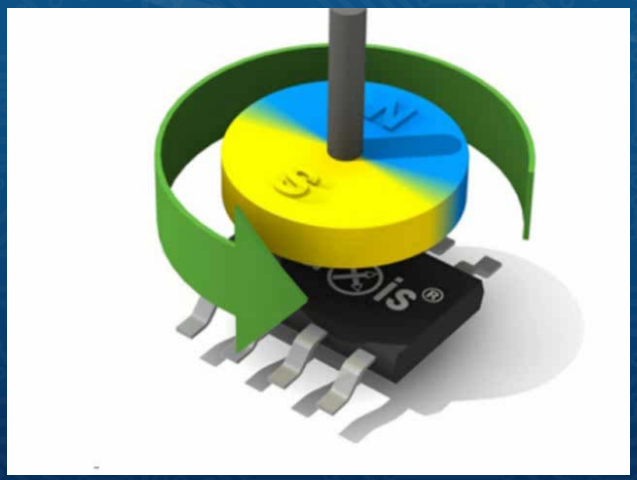
Basics: triaxis® technology

Triaxis® principle:

- 3 axis magnetic field measurement from a single sensor

Triaxis® types:

- Position sensor – rotational, linear, 3D displacement
- Current sensor mounted on a bus bar



Triaxis® characteristics:

- Small size
- High temperature
- Contactless
- Robustness
- Self-diagnostic
- High resolution
- High linearity
- High accuracy

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Test requirements and challenges

Test requirements:

- Rotating magnetic stimulation during electrical test
- Multi-site testing at the wafer level (for efficient throughput)
- Tests at several temperatures from 35 to 175 ° C
- Robust and uniform magnetic fields across all the sites

Challenges:

- Stability of the probe card (and test-cell) over the full temperature range
  → Stable probe-to-pad alignment and minimal pad damage
- Magnetic source as close as possible to the wafer - but the probe card is in the way!
- Minimal magnetic interference from test cell (probe card, prober chuck, etc.)

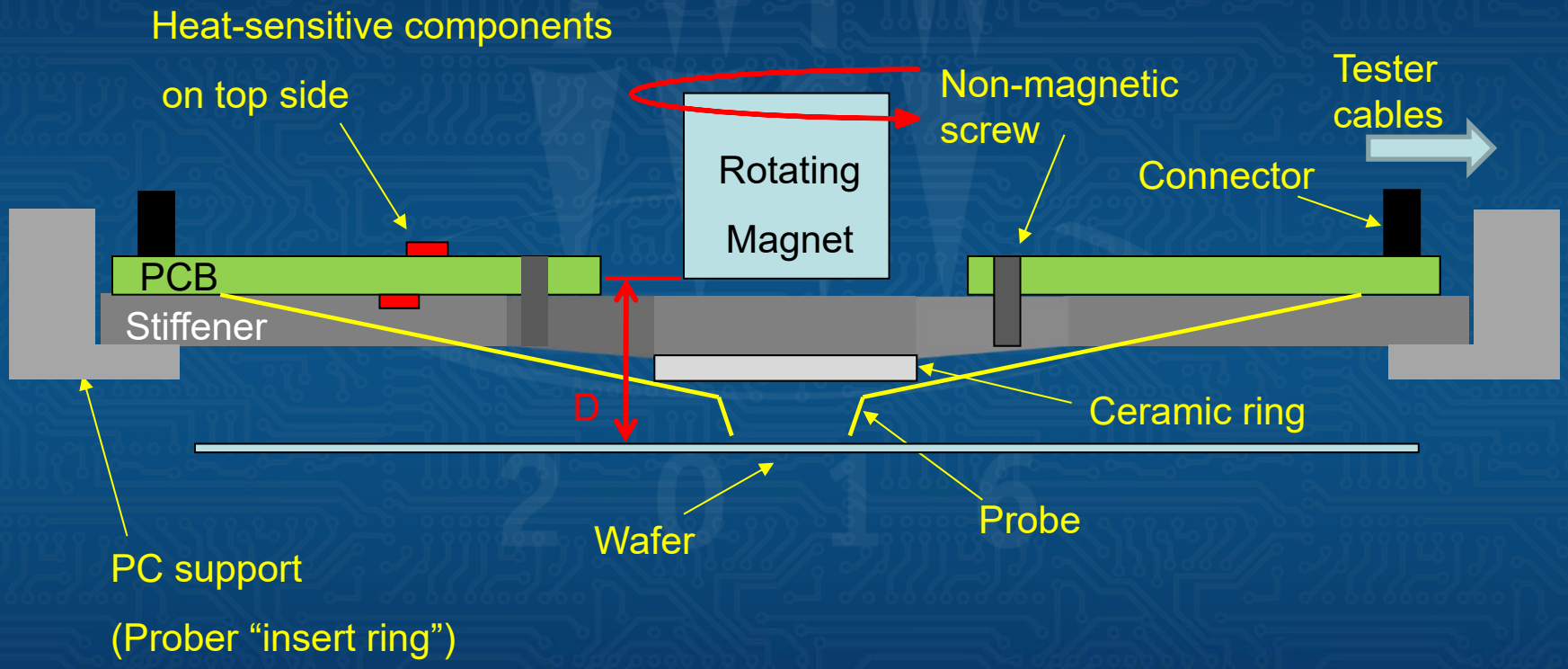
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FormFactor v. Technoprobe
IPR2024-00933

Test-cell considerations

- **Wafer chuck:**
  - High temperature capability with minimal magnetic noise
- **Prober:**
  - High-temperature software options required to ensure good probe-to-pad alignment
  - Modified insert ring for mechanical stability at high temperatures
- **Probe card:**
  - Minimize non-magnetic materials
  - High-temperature materials
  - Stiffener required on bottom (wafer) side
- **Magnetic test head:**
  - Designed for rotation and installation on wafer prober

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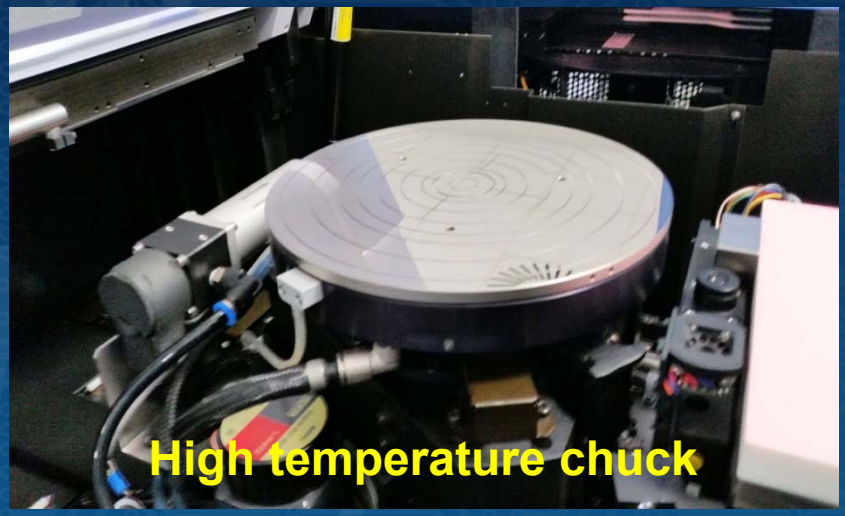
Concept

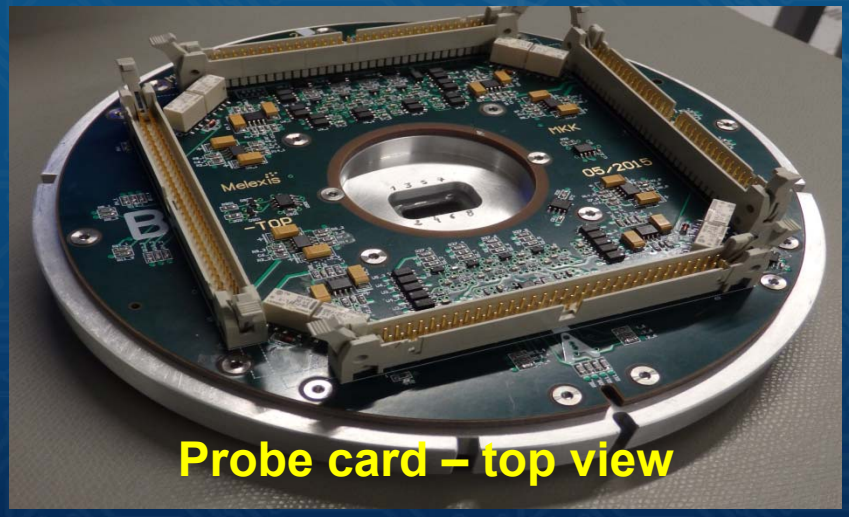


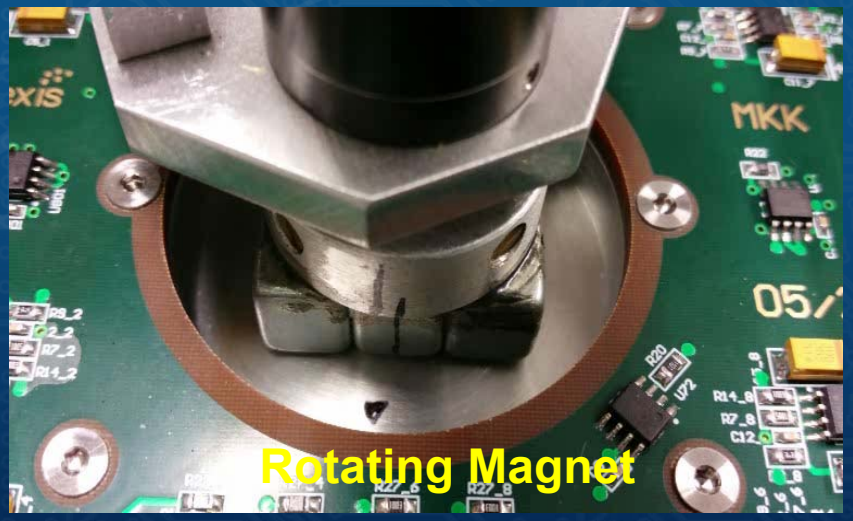
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System setup







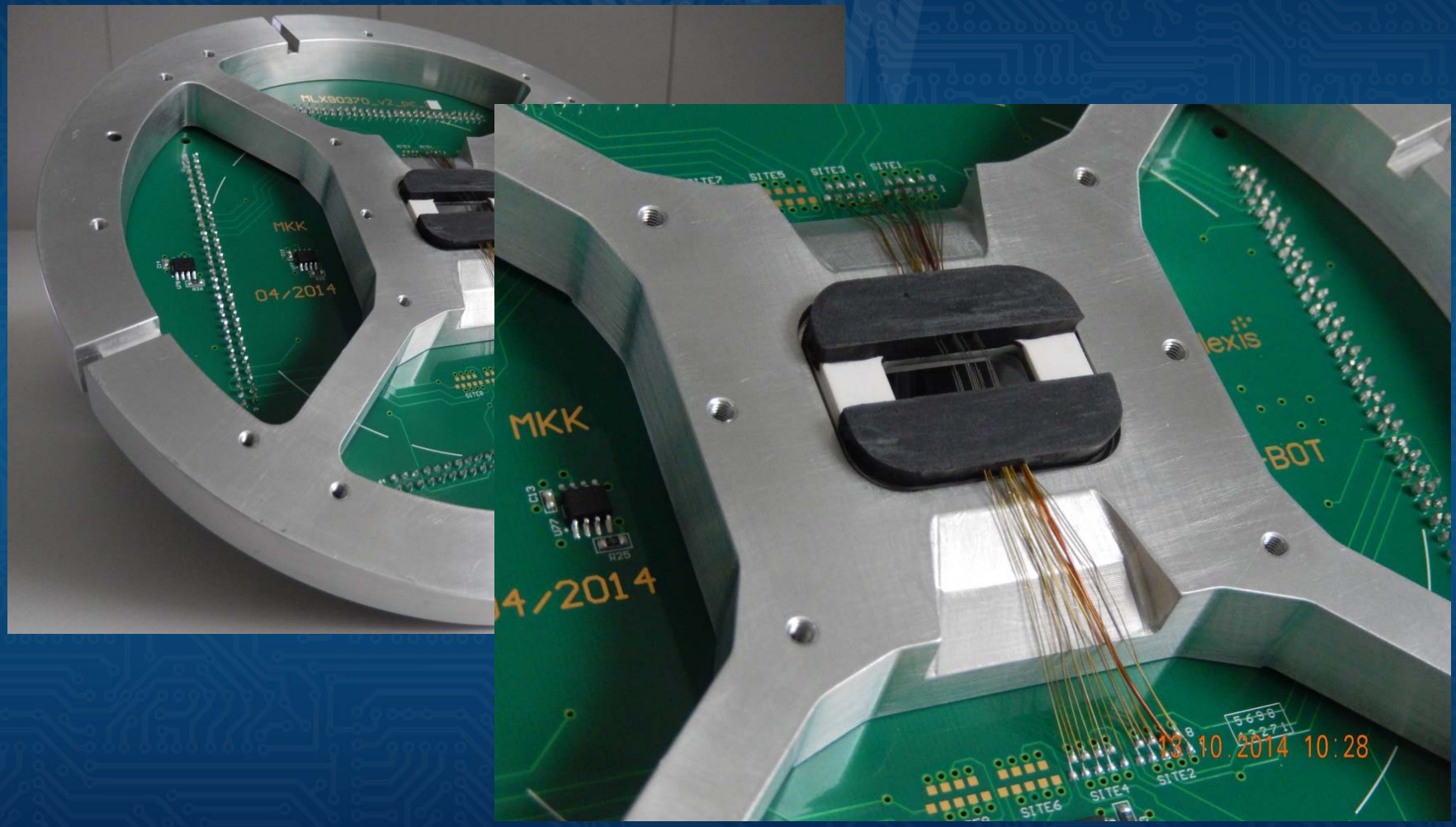


Melexis
Microelectronic Integrated Systems

SW Test Workshop - June 5-8, 2016

JEM

High-temperature probe card (PCB & stiffener)



Melexis
Microelectronic Integrated Systems

SW Test Workshop - June 5-8, 2016

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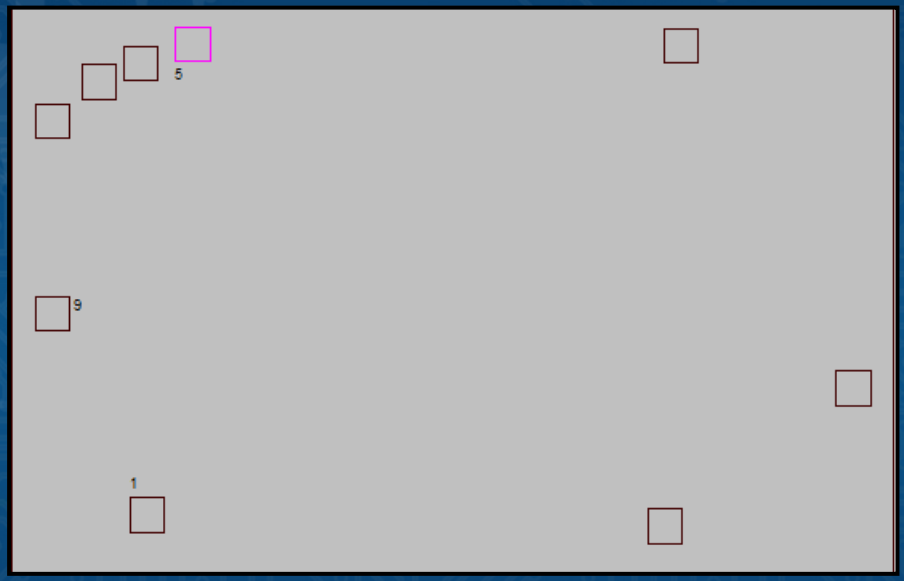
Material selection

Test cell item	Material	Stiffness (Shear modulus) Gpa	Thermal expansion (CTE) um/m-°C	Thermal conductivity W/(m K)	Magnetic susceptibility	Selection result
PC stiffener + PC support (Prober insert ring)	Low-CTE steels	56	2	14	High	✗
	Stainless steels	77	14	16	Med	✗
	Aluminum alloy	27	23	205	Low	✓
PCB	High-Tg epoxy-glass + Cu/Ni/Au plating	Variable	15 (XY plane) 60 (Z-axis)	Low	Low	Weak point
Probe ring	Ceramic	360	5	18	Low	✓
Probe-ring epoxy	High-temp. epoxy	15	10	Low	Low	✓
	Standard Epoxy	Poor	50	Low	Low	✗
Probes	Tungsten-Rhenium	161	4	174	Low	✓
Wafer	Silicon		3			

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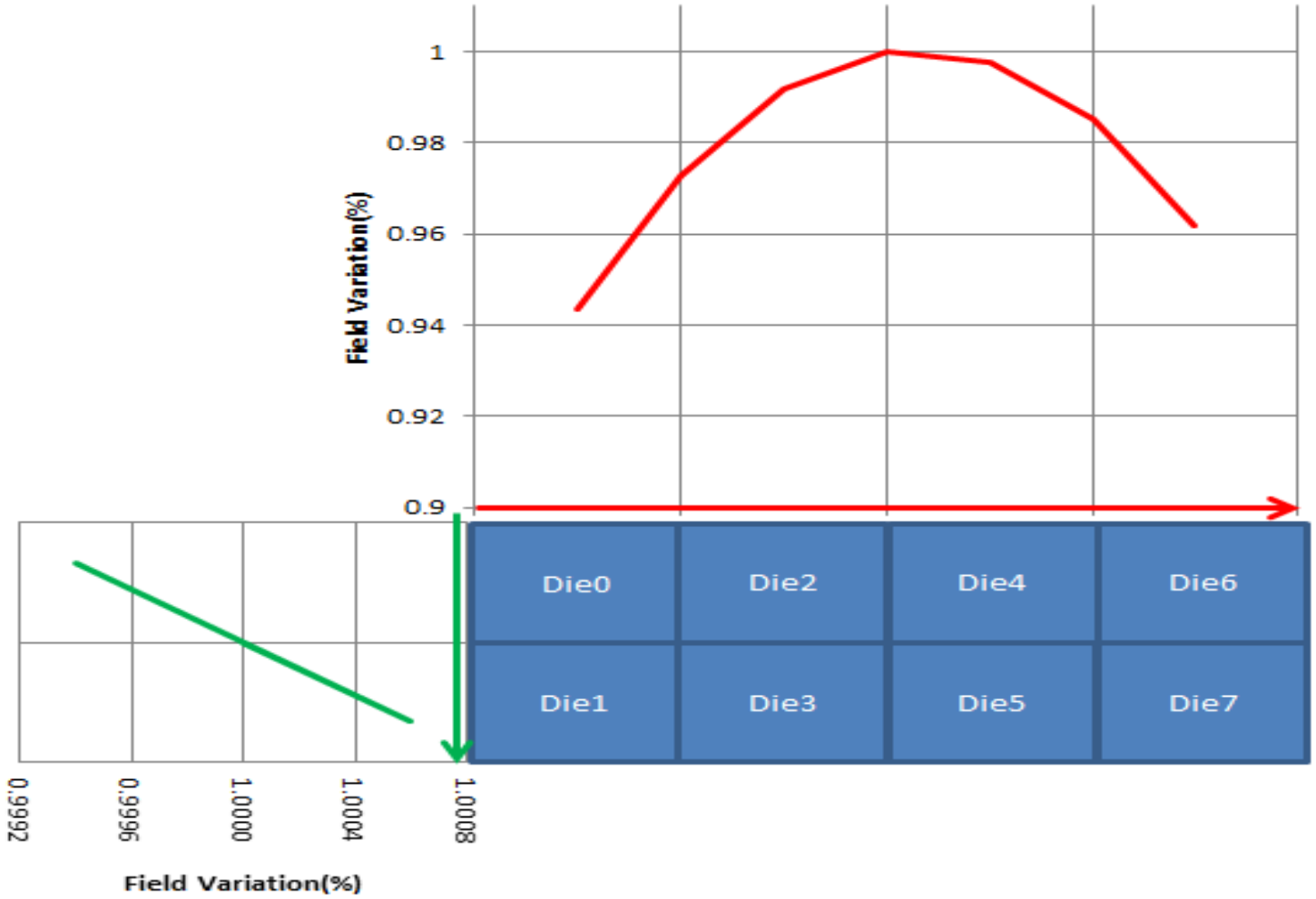
Probing condition

Stepping X (µm) = 2615
Stepping Y (µm) = 1680
Pad Opening (µm) = 101 * 101
Recommended OD (µm) = 75
Alignment Tolerance (µm) = ± 7
Planarity Tolerance (µm) = ± 7
Operating Temperature (˚C) = 35 .. 175
Minimum Pad Pitch (µm) = 133.2
Probe Material = ReW
Tip Diameter (µm) = 25 ± 5
Tip Shape = Semi Radius
Probe Force (g@ODtarget) = 6 ± 20%



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Probing Condition



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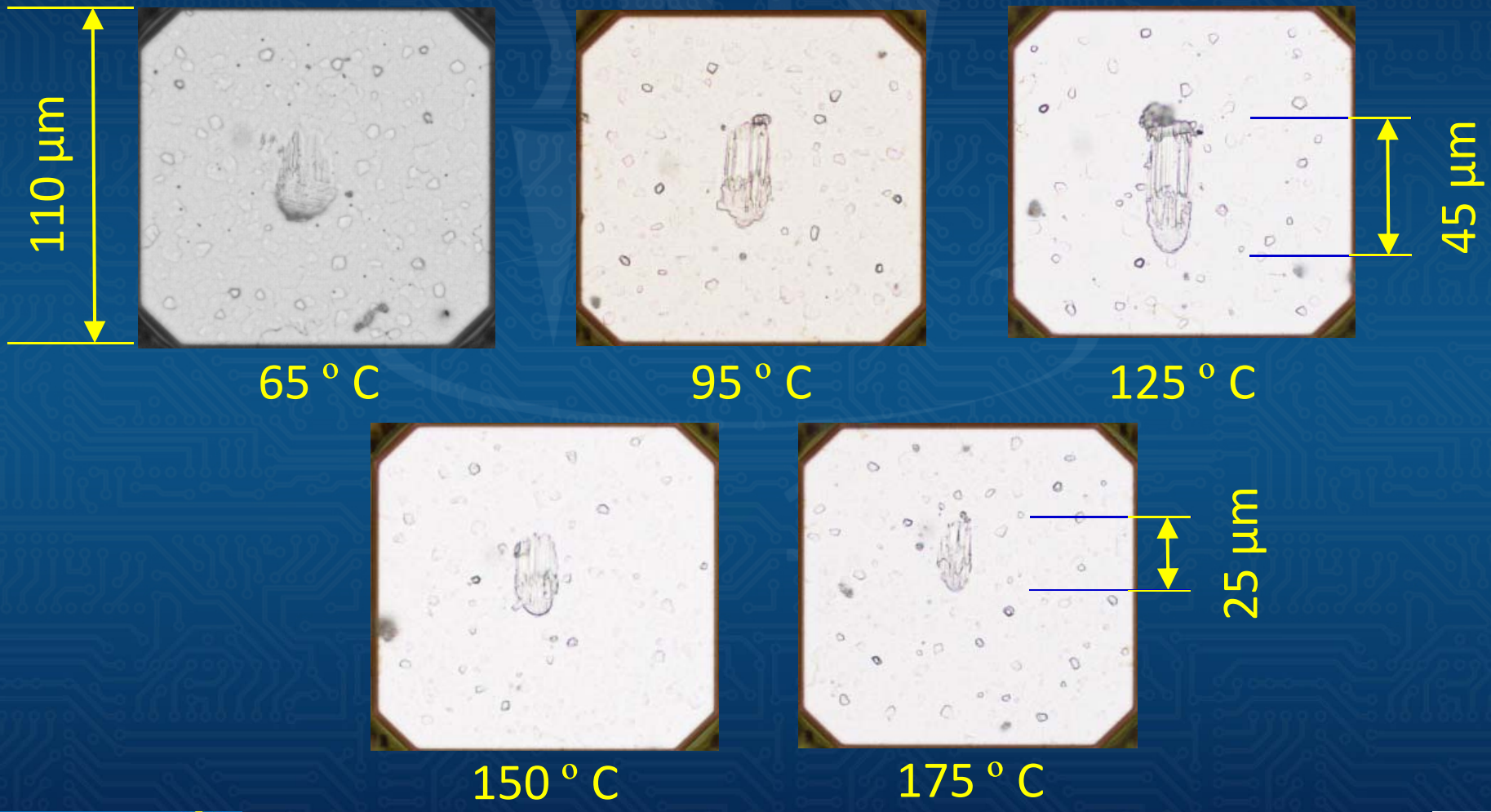
FormFactor v. Technoprobe
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Evaluation criteria - summary

Criteria	Specification	Measured	Assessment
Stable PTPA (probe to pad alignment)			
Alignment tolerance over full temperature range	± 7 µm		
Planarity tolerance over full temperature range	± 7 µm		
Tip diameter (25 µm)	± 5 µm		
Acceptable probe card (system) deflection			
Uniform and stable pad damage (scrub marks)			
Scrub area in specification			
Scrub depth in specification			
Maximum scrub depth not to exceed material thickness			
Stable functionality over operating temperature	35 .. 175 °C		
Stable contact at recommended OD			
Repeatable yields at all temperatures			
Test results uniform among all sites			
Magnetic field uniform among all sites	5% field variation		
Probe card information			
Probe card cost	Low cost		
Probe card technology	Cantilever		
Tip Shape	Semi Radius		
Probe Force (g@ODtarget)	6 g ± 20%		

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Scrub mark size versus temperature @ 60 µm OD

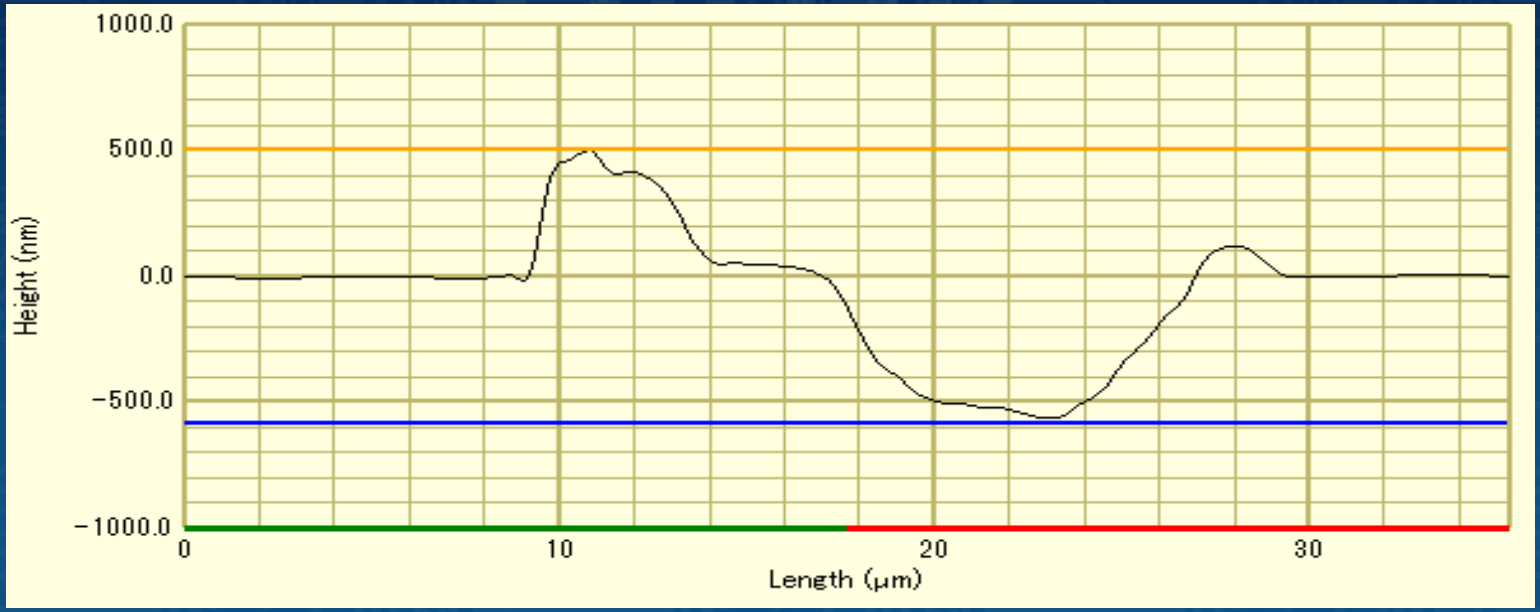


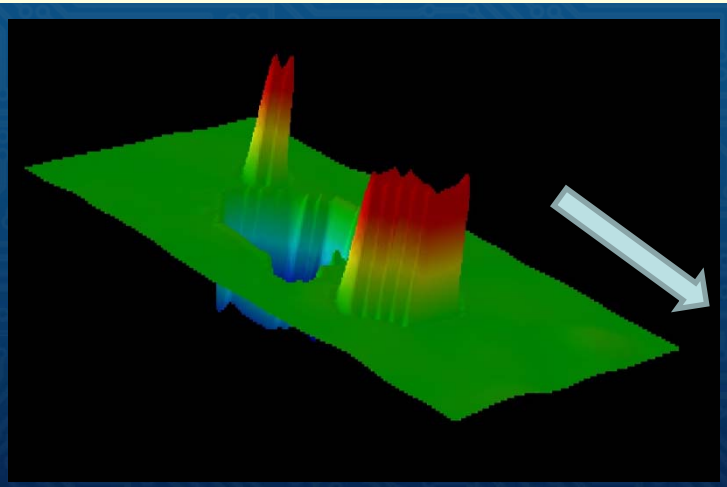
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3D & profile @ 175 ºC (60 µm OD)



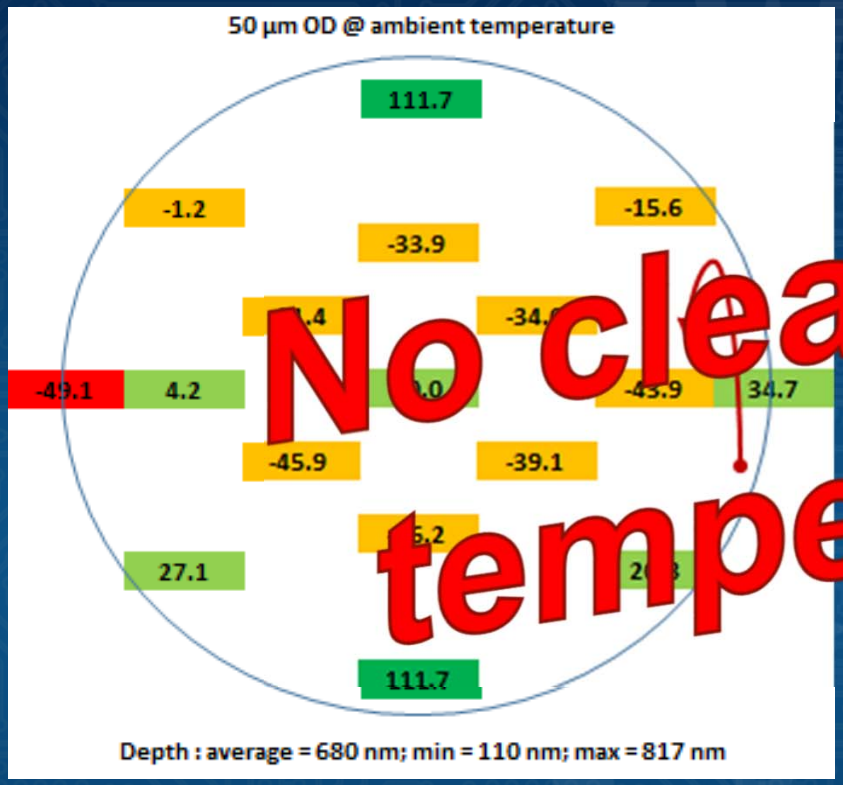


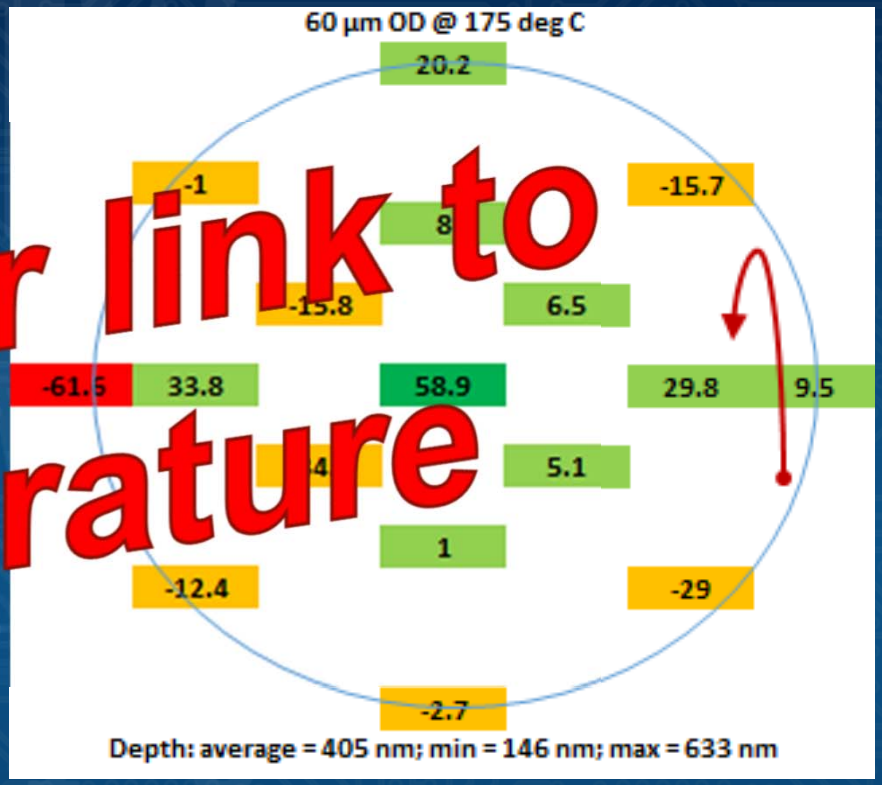
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Scrub profile depth deviation





No clear link to temperature

Highest point	
> Average	
< Average	
Deepest point	

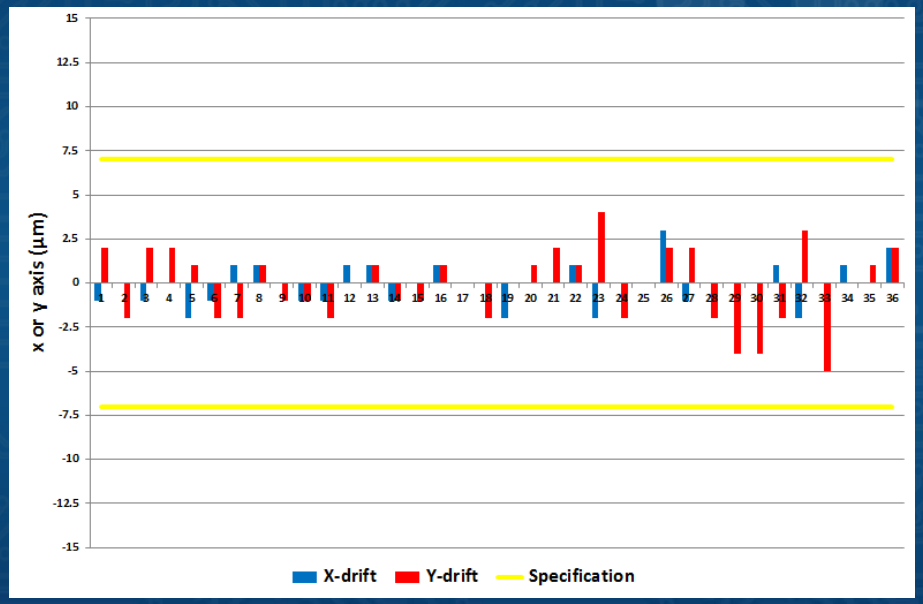
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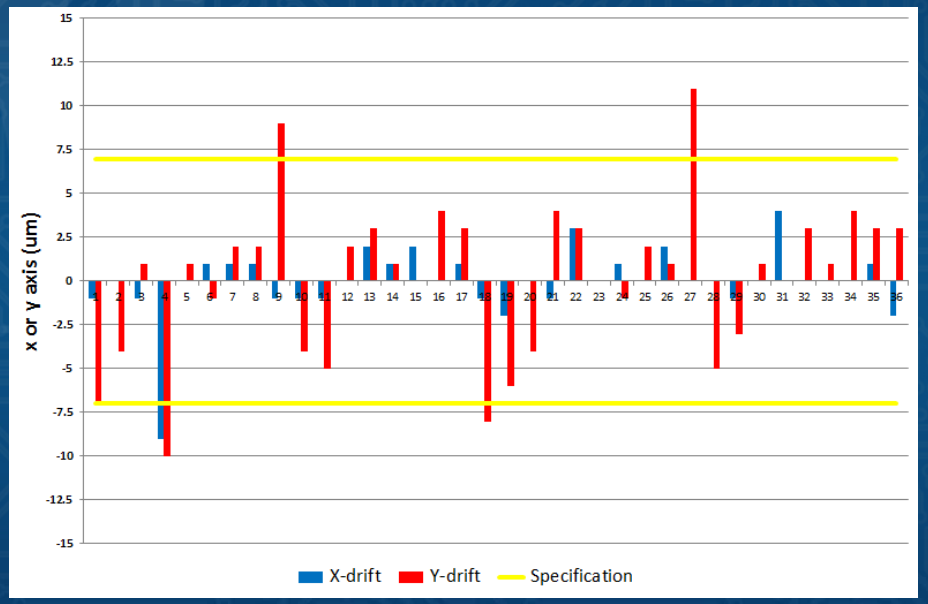
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Needle alignment drift @ 60 µm OD

Ambient



175 deg C



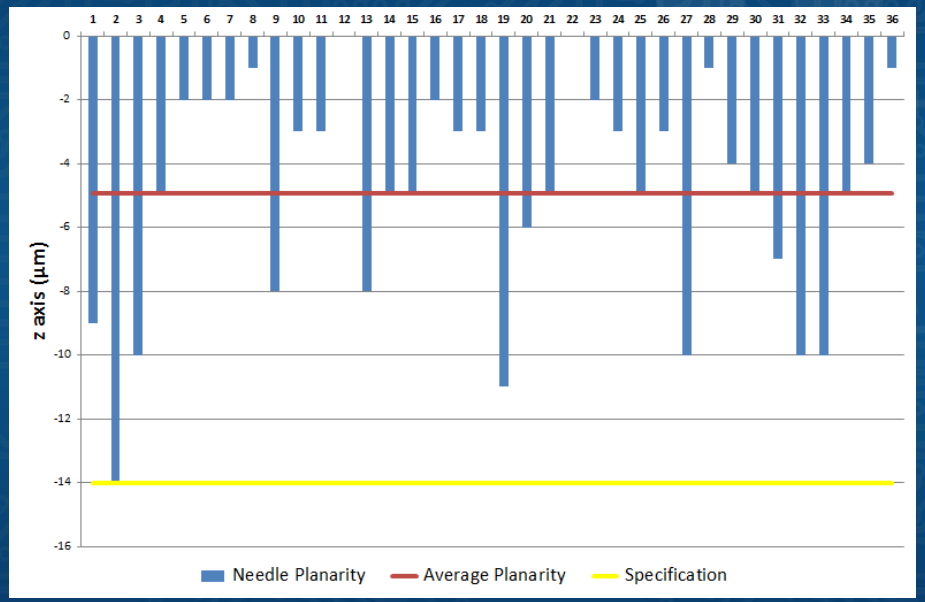
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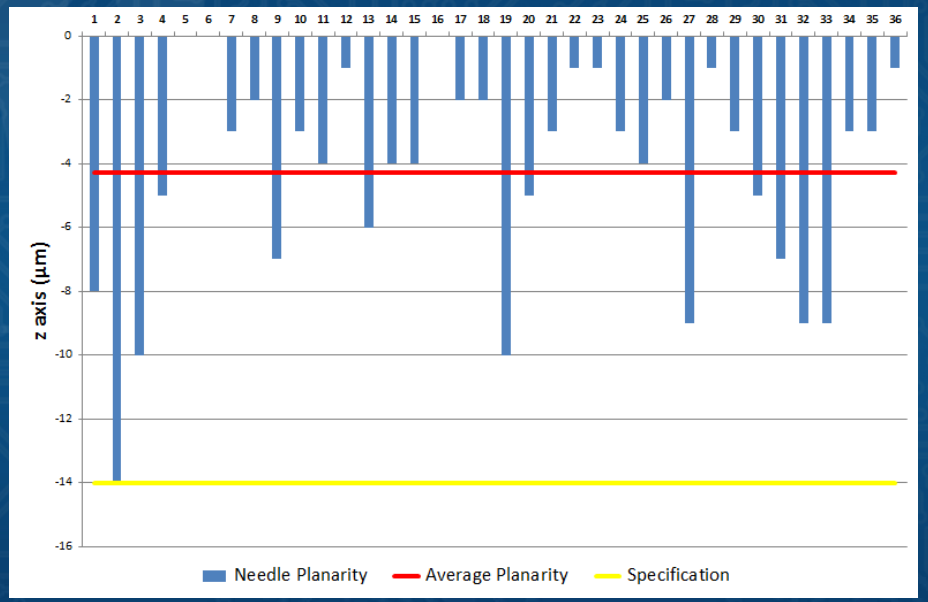
JEM

Probe card planarity @ 60 µm OD

Ambient



175 deg C



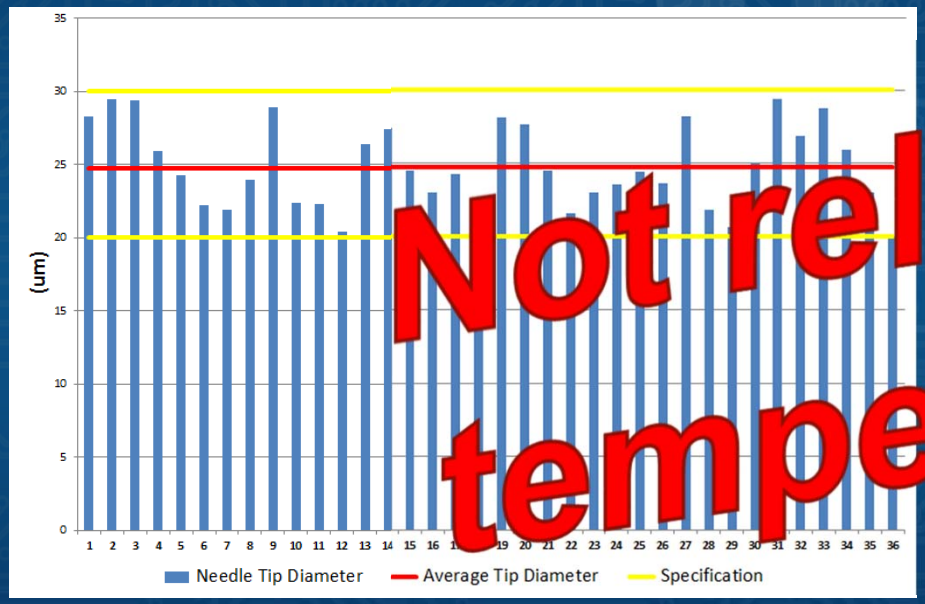
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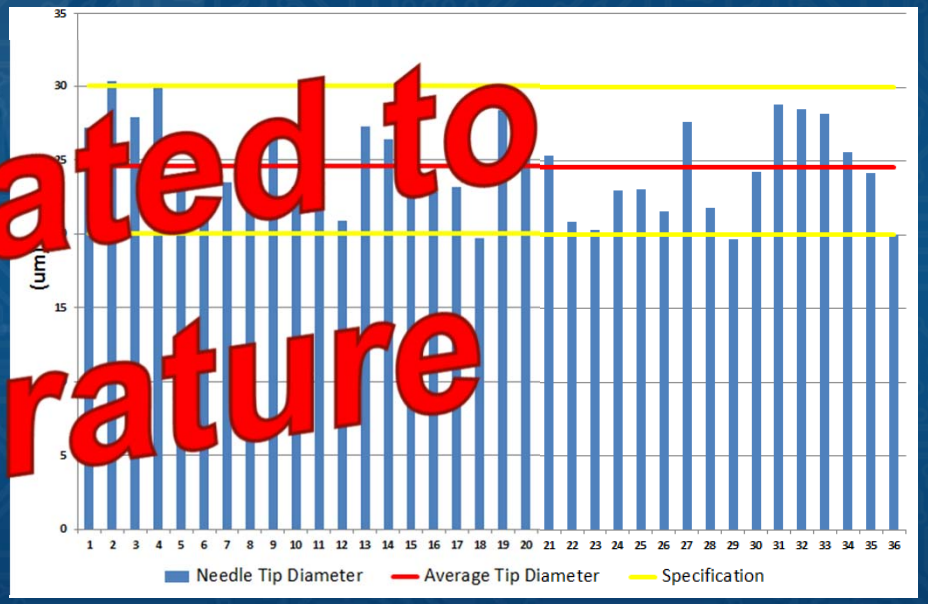
JEM

Tip diameter @ 60 µm OD

Ambient



175 deg C



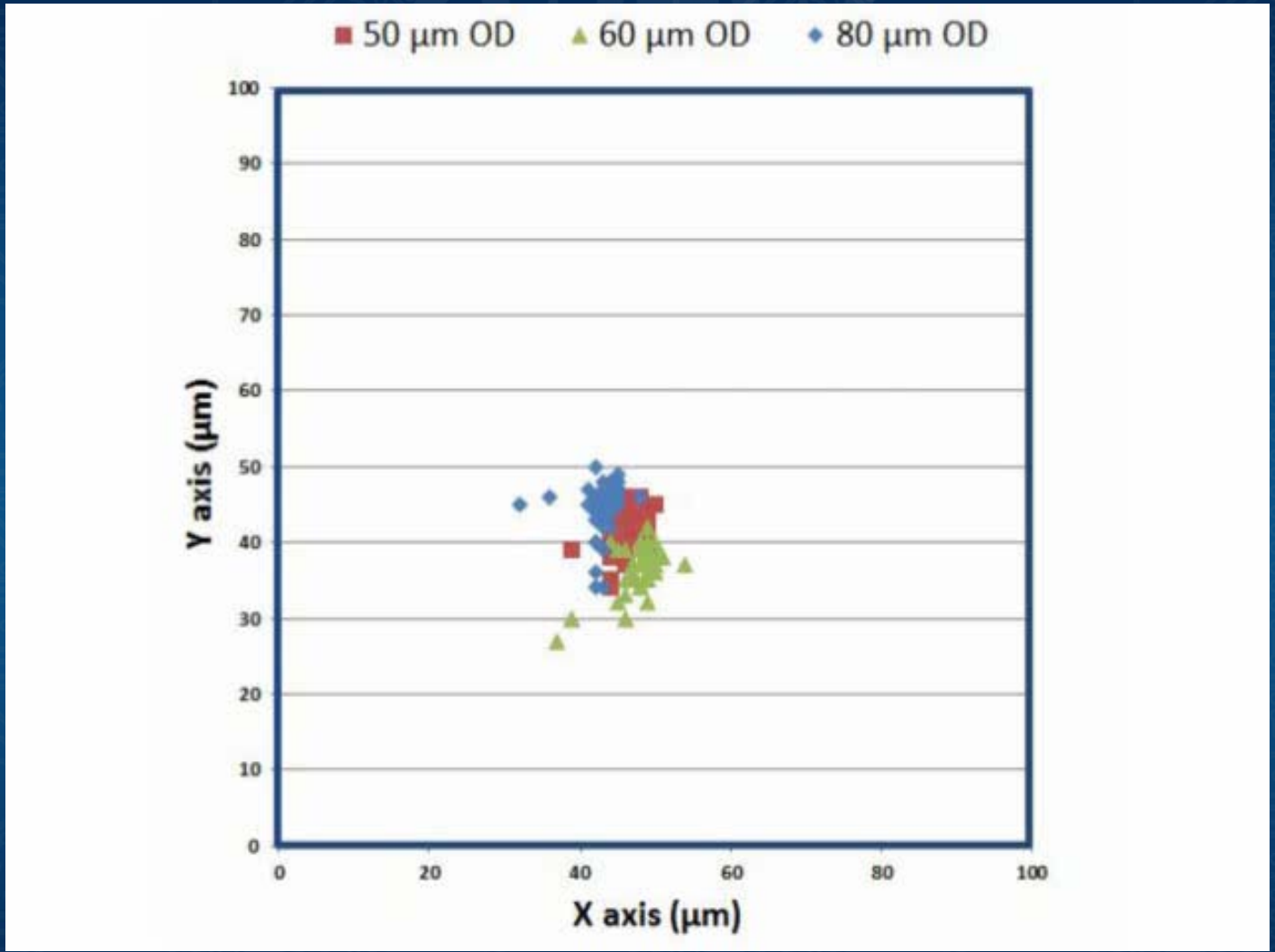
Not related to temperature

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Probe mark position @ ambient

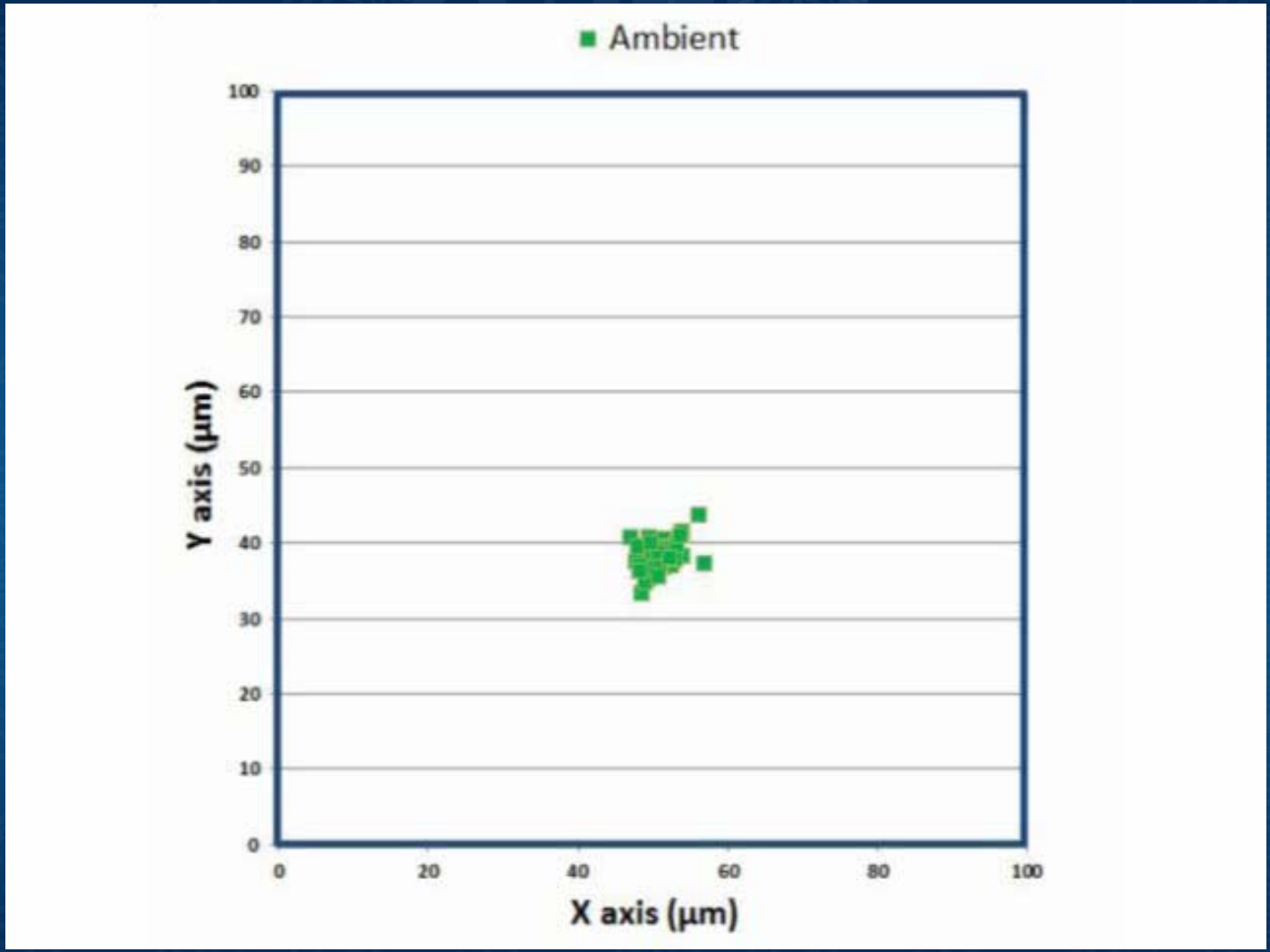


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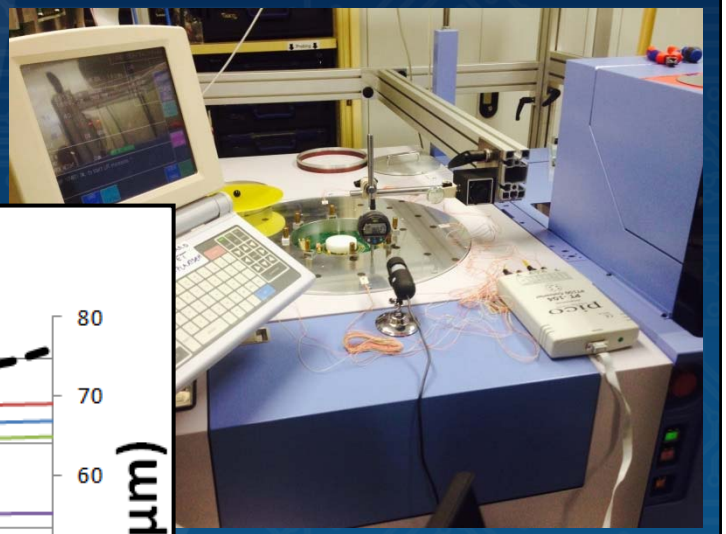
JEM

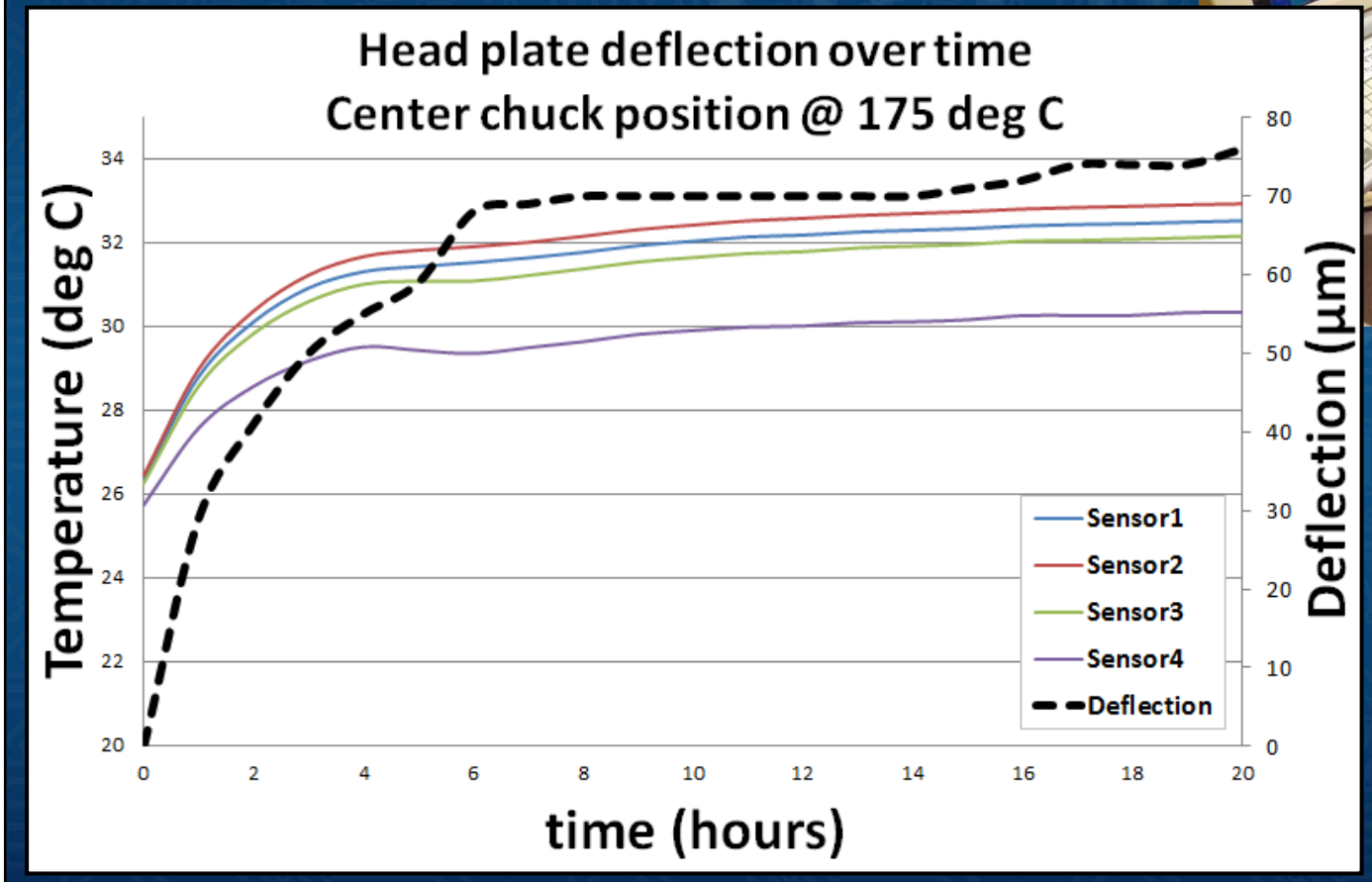
Probe mark position @ 60 µm OD



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Temperature effects



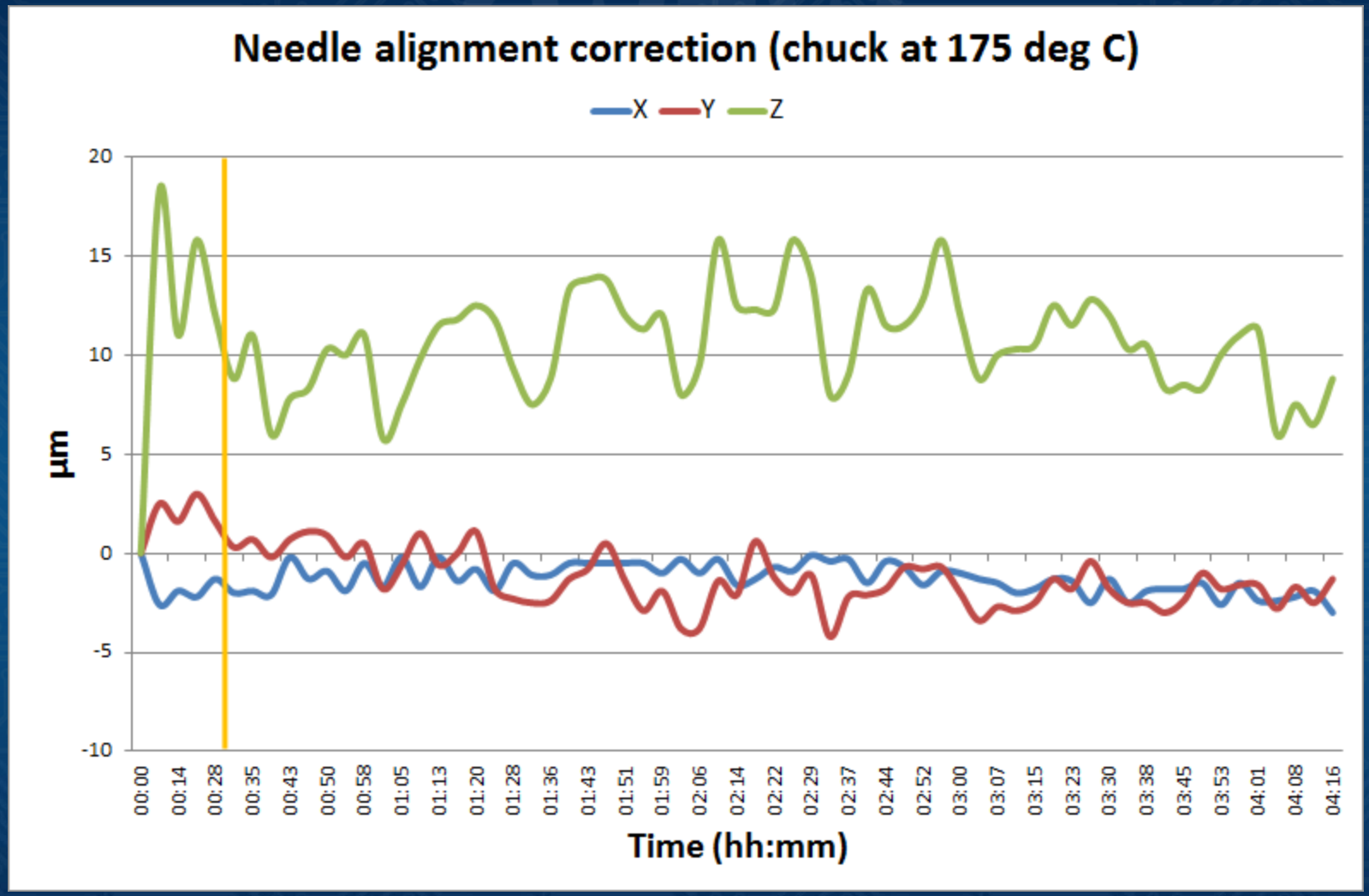


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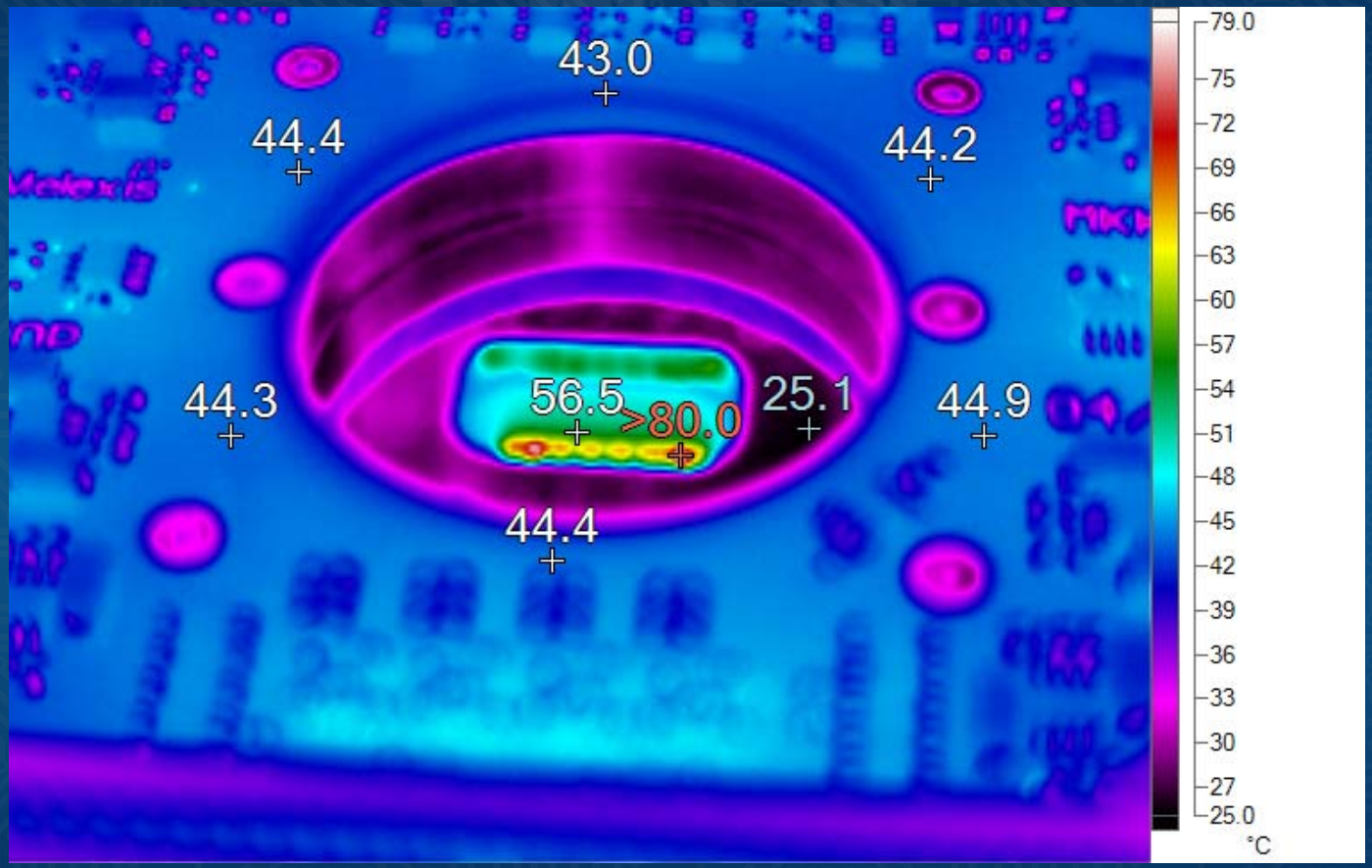
Probe card settling time



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Temperature effects

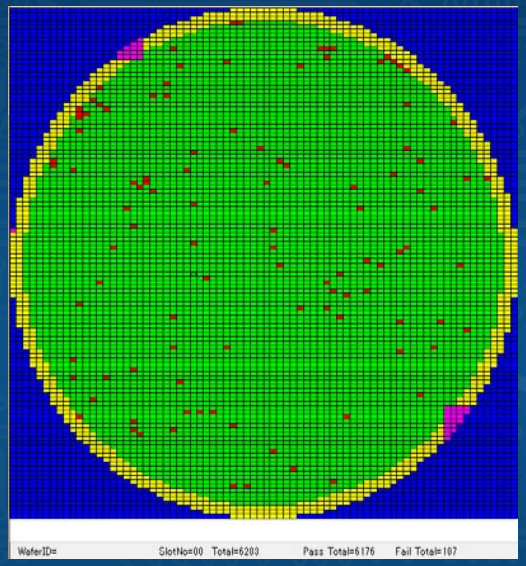


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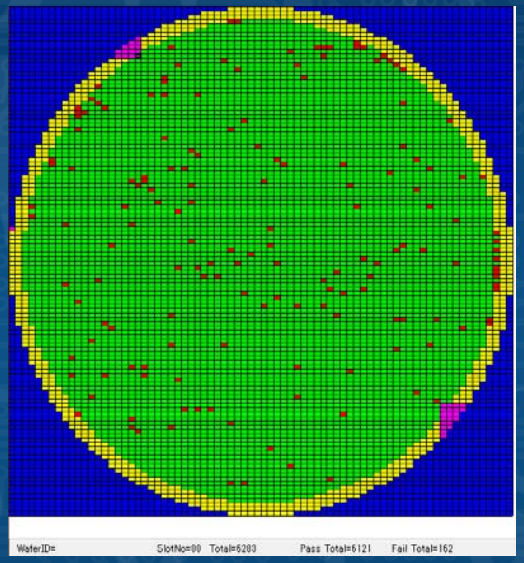
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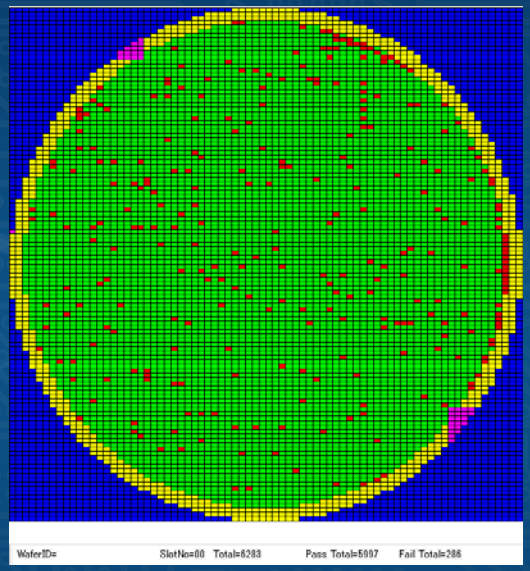
Initial functional test results



35 º C



125 º C



175 º C

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Achievements & conclusions

- The probing hardware builds a proper synergy between the magnetic source, the prober interface, the tester interface and the probe card interface. A carefully designed low-cost cantilever probe card can be used.
- The tests results validate the probing hardware and proves this concept is the best practice for probing over a temperature range from ambient up to 175 ^{o} C for those magnetic devices.
- The applied concept meets the challenging requirements to test on wafer level magnetic sensors in parallel and over a wide temperature range.

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Future work

1. Observe effects of aging of probe cards over many touch downs and repeat tests on successor (in progress).
2. Optimize probe card design and probing parameters, such as cleaning, contacting method and OD, to improve first-pass yield and get more uniform results at the various temperatures.
3. Improve magnetic measurement capabilities.
4. Increase throughput by increasing probing areas.
5. Evaluate the concept over a temperature range from -40 ^{o} C to 200 ^{o} C with ability to mount more components on the PCB and to use different probe head technology.
6. Evaluate the effect of low force probe material on scrub depth.

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Acknowledgements

I would like to thank the following people for their support and input:

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- Peter Schops — Melexis
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Thank you. Questions ?



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SW Test Workshop
Semiconductor Wafer Test Workshop

General Overview on pad damage:
probe key parameters and other causes.

Riccardo Vettori
Technoprobe

June 5-8, 2016

Outline

- **Introduction**
- **Probe action on pads**
- **Scrub mark mechanics**
  - Pressure and shear stress
  - Tip stiffness
  - Lateral force measurements
  - Scrub and temperature
- **Pad damage**
- **Conclusions**

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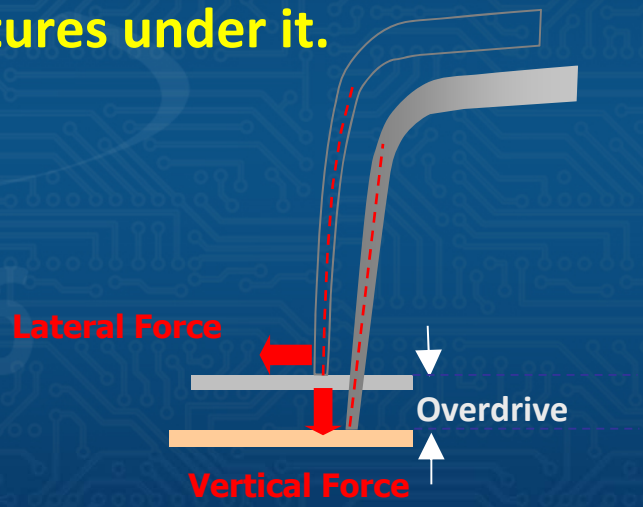
Introduction

- **The wafer probe test aims to evaluate the device electrical performances before assembly.**
- **Probe touch on pad enables breaking the native oxide layer lied on the pad surface, getting a suitable electrical contact.**
- **The probe impact and the sliding motion on pad could cause:**
  - Crack failures in the structures underneath the probing area.
  - Copper, Nickel or other metallization exposure, cause of bonding failure.
  - Problem of bonding reliability due to large scrub.
- **Few options are possible to decrease the failures described above:**
  - Work on the pad structure and layout.
  - Work on the probing process parameters (Overdrive, chuck speed, number of Td, cleaning process, cleaning sheets….)
  - Work on the needle technologies

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Probe action on pad

- **The probing process on pad is composed of 4 phases:**
  - Probe impact on pad
  - Probe sliding forward movement (Cantilever and some MEMS probes)
  - Electrical test with probe under static load on pad
  - Probe sliding backward movement (Cantilever and some MEMS probes)
- **During the probing action the tip digs the pad surface transmitting stress to the stacked interconnected structures under it.**
  The stress transmitted are:
  - Compression stress
  - Shear stress

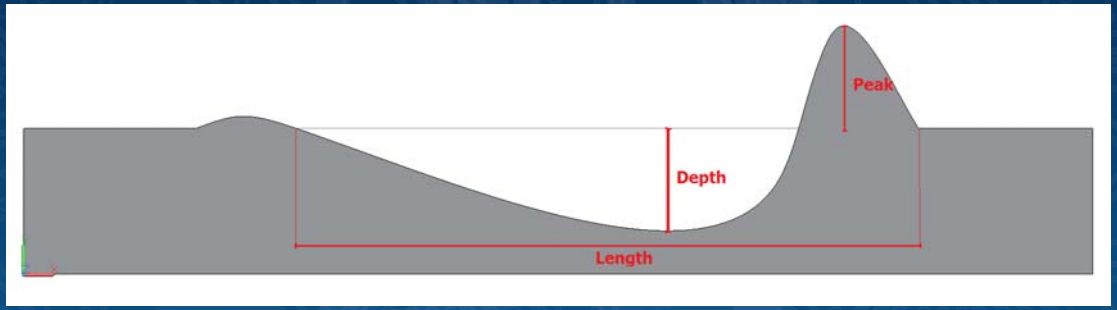


- **Both stresses have to be considered during probe card design, above all the shear stress for cantilever technology**

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Scrub mark description 1/3

- A scrub mark is characterized by 4 elements: length, width, depth and peak.



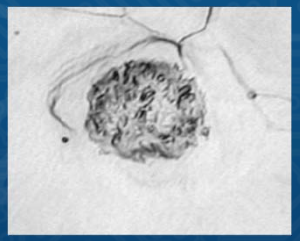
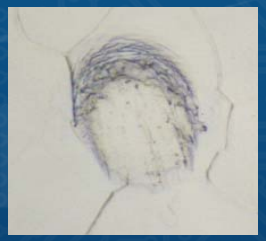
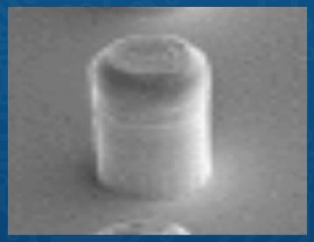
- Cantilever scrub description; 3 comparing cantilever technologies

Key Parameters	STD - flat	Helium	NoScrub
Scrub mark picture			
Notes	• Fat tip shape is used • **Scrub is not deep** • Scrub peak is limited • **Shear stress is high**	• Slim tip shape is used • Scrub quite deep • Scrub peak is taller than STD scrub • Shear stress is low	• NoScrub tip shape is used • **Scrub deeper than STD scrub** • Scrub peak is taller than STD scrub • **Shear stress is low**

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Scrub mark description 2/3

- The table below reports some scrub examples obtained by different TPEG™ MEMS probes

MEMS probe type	TPEG™ Pointed NoScrub	TPEG™ Pointed Scrub	TPEG™ Flat
Scrub mark picture			

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Scrub mark description 3/3

- **Scrub shape depends on the pad contact surface:**
  - Material
  - Hardness
  - Thickness
  - Roughness of the pad surface
  - Native oxide layer
- **One of the most used material for the pad contact surface is Aluminium, but not all the Al pads are the same**
  - Aluminium thickness may change
  - Aluminium grain size and metallurgy may change leading to different hardness
- **The probe action, the scrub shape, the polishing recipe and testing process should change in function of the pad**

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Pressure and Shear Stress 1/2

- **The vertical force alone is not the only leading factor causing cracking and it should be considered tied to another important probe characteristic as the probe contact diameter.**
  - The contact pressure is a key parameter that should be considered since early design phase.
- **The shear stress transmitted by the probe is underestimated but it gives the main contribution to the tensile stress in the inter-metal dielectric.**
  - The tip stiffness has to be considered during cantilever design since the beginning.
- **Vertical probes without scrub action give only compression stress to the structures under pad. As a consequence, vertical probes can work with higher pressure than cantilever.**
  - Some MEMS probes show a scrubbing action on pad. In those cases the shear stress has to be considered.

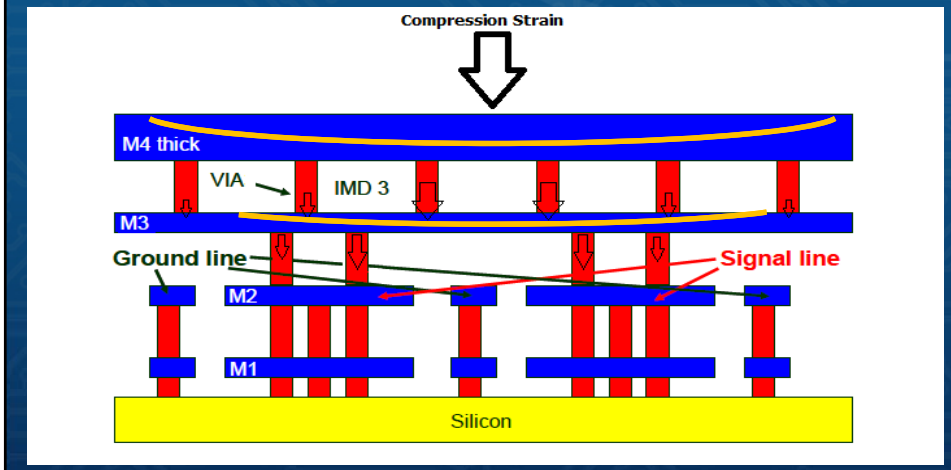
FormFactor Ex. 1031, p. 221

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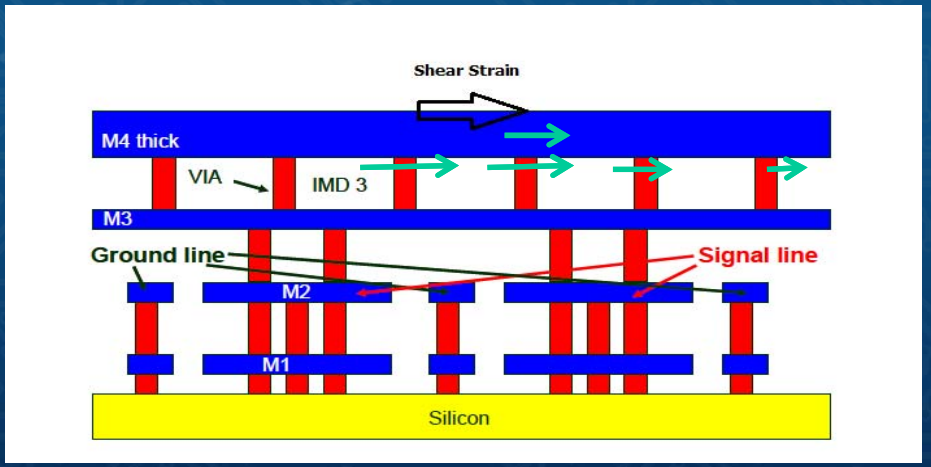
Pressure and Shear Stress 2/2

- Vertical force induces Internal Metals bending deformation and Vias compression.
- Shear stress induces traction in the Internal Metals and Vias deflection.
- Typically, the structures under the pad are more sensitive to shear stress than compression strain.

Compression strain



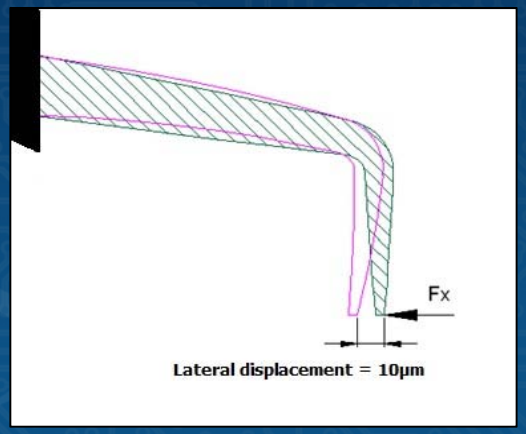
Shear strain



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Cantilever Tip Stiffness

- **The main parameters useful to control the tip stiffness and shear stress are:**
  - Tip length (Cracks appear more often on pads probed by the first level).
  - Tip shape
  - Needle material



- **The tip stiffness can be evaluated measuring the force when a lateral tip displacement is imposed like shown in the picture on side.**

- **Below an example where 2 probes with different tip lengths have been measured.**

Probe	Needle type	Contact Diam (µm)	Tip length (µm)	Force Fx
Probe C	WR4mils	18	180	1,4 g
Probe D	WR4mils	18	270	0,8 g

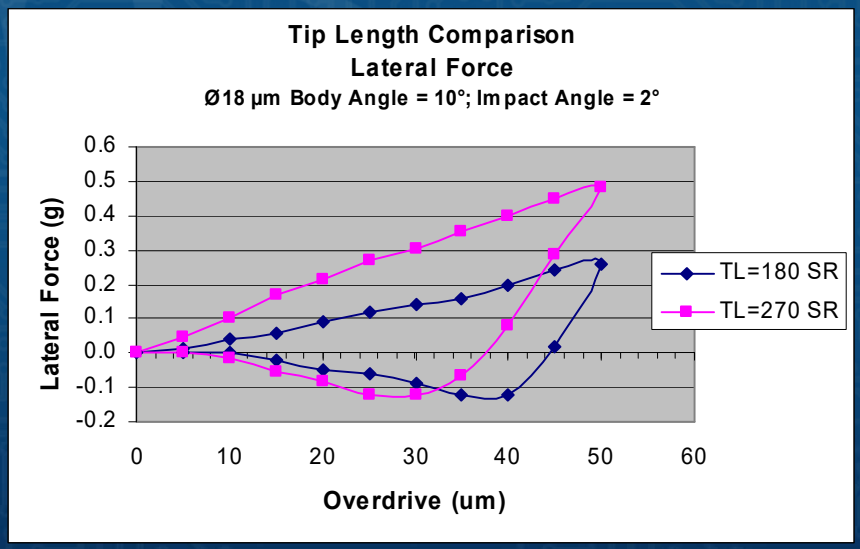
- **The probe with longer tip is less rigid than the shorter one.**

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A lab experience

- In order to investigate the stress transmitted to the pad during the probing action a machine with 2 force gauges has been realised to measure vertical and lateral forces
- The lateral force characteristic will be described in the next slides.
- All the measurement has been performed on little samples of blank wafer with 1,5 µm of Al thickness.



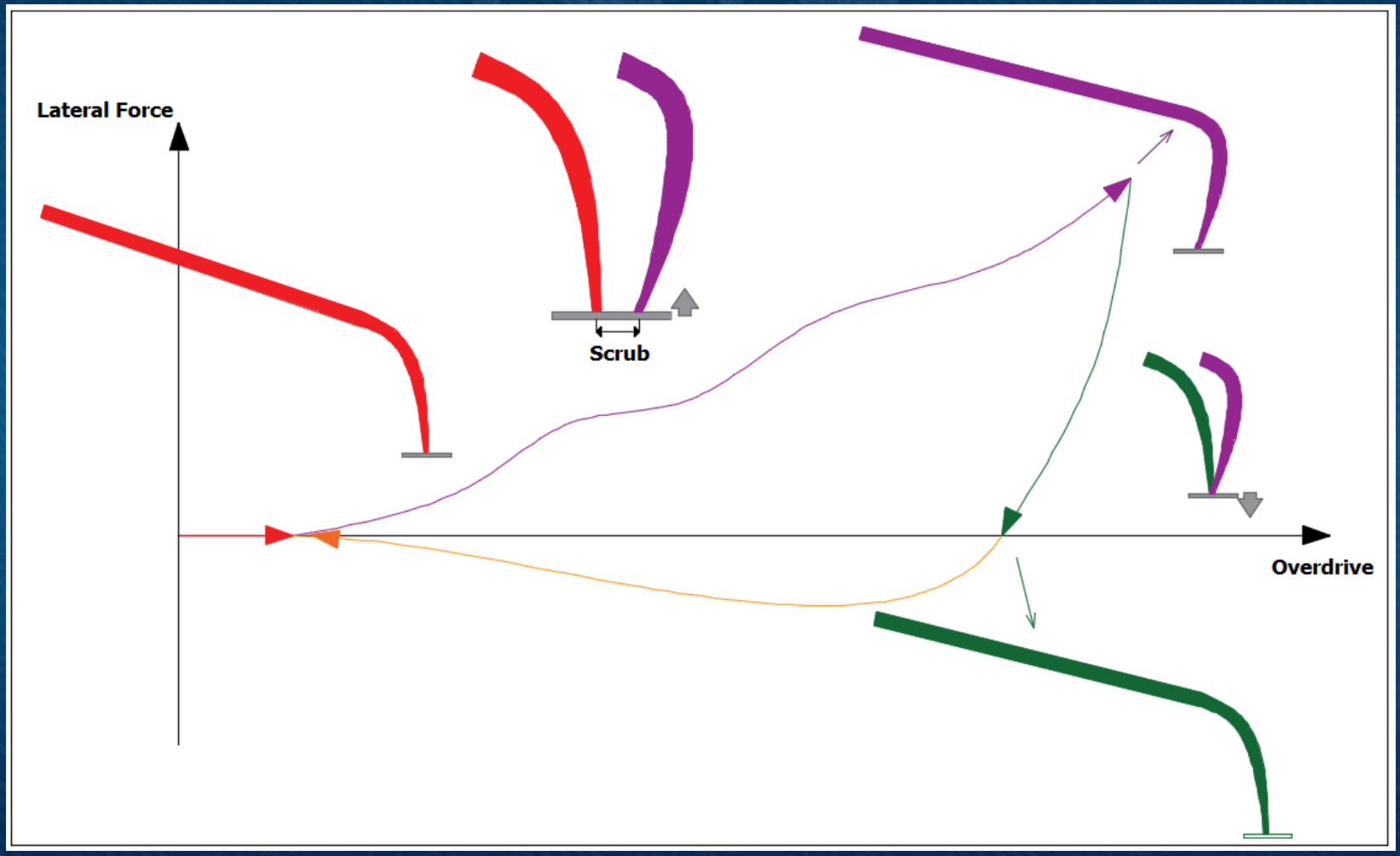


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Lateral force cycle during a TD 1/3

- The picture below shows the cycle described in the previous slide



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Lateral force cycle during a TD 2/3

- **Lateral force cycle description:**

– Red line

The needle slides on the pad surface after the impact with the pad and the lateral force measurement doesn't increase.

Harder the Al pad layer is, longer the tip sliding movement will be.

– Purple trend

The lateral force rise is due to the tip deflection that increases with the overdrive.

The diagram shows a rise wave trend. These waves occur when the tip lateral force achieved enough intensity to overcome the pad friction and the resistance of the aluminium peak formed around the tip. When the probe contact surface is in motion the tip deflection decreases, so the lateral force increment rate decreases slowly too.

If the probe has a stiff tip, all the energy is unload immediately on pad instead of to be accumulated in the tip deflection. The scrub length will be long, the measured lateral force will be low and the pad damage probability will be high.

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Lateral force cycle during a TD 3/3

- **Lateral force cycle description:**

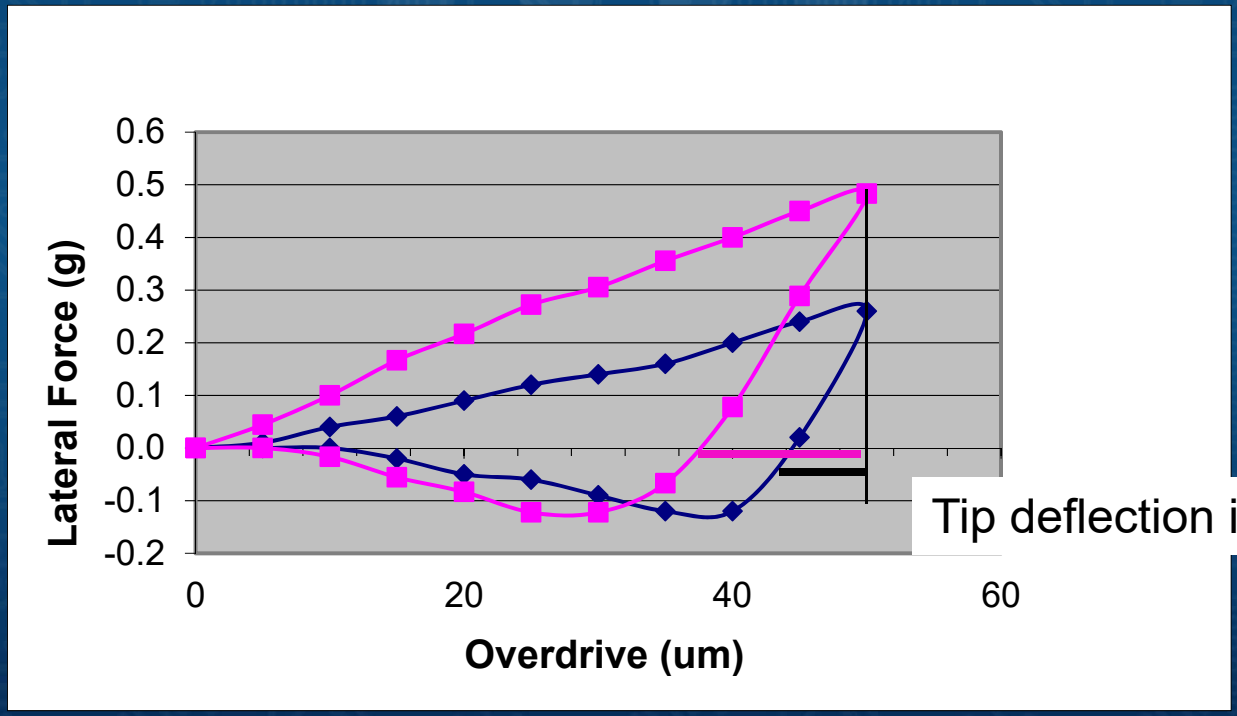
– Green trend
When the chuck starts its return movement, the lateral force decreases quickly to zero. In this phase the tip loses the deflection. The return overdrive necessary to cross the x axes is proportional to the tip deflection and tip rigidity.

– Orange Trend
In this phase the probe move back transmitting to the pad a negative shear stress.

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Lateral Force Vs. Tip length

- The area of the cycle represents the energy accumulated in the probe. More is the energy accumulated in the tip, less is the energy transmitted to the pad structures.
- The plot below shows the Lateral_Force vs. OD for two different probe designs

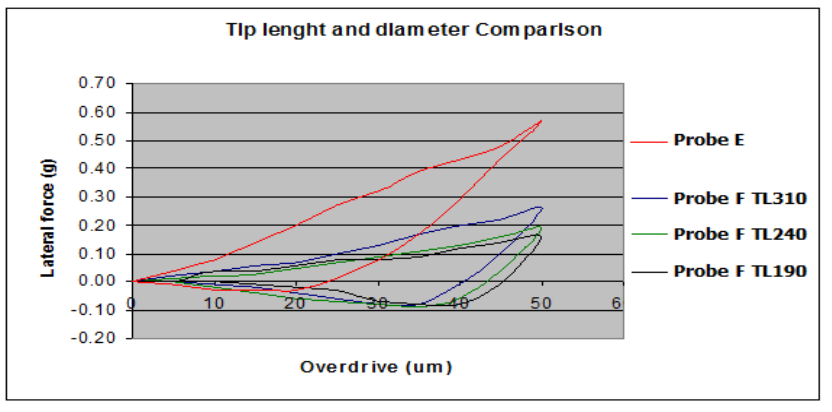


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Lateral Force Vs. Pressure and tip wear

- **The lateral force measurement has been performed on many different probe types.**

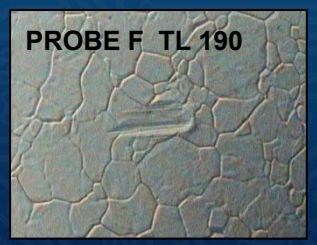
Probe	Needle type	Contact Diam (µm)	Tip length (µm)	Pressure (mg/µm²)
Probe E	WR4mils	15	310	4,8
Probe F	WR4mils	15	310	3
Probe F	WR4mils	15	240	3
Probe F	WR4mils	15	190	3



- The lateral force is proportional to the pressure.
- Probe E scrub is deeper and shorter than Probe F TL310 scrub.
- Probe F –T.L. 310 scrub mark is deeper and shorter than Probe F - T.L. 190 scrub





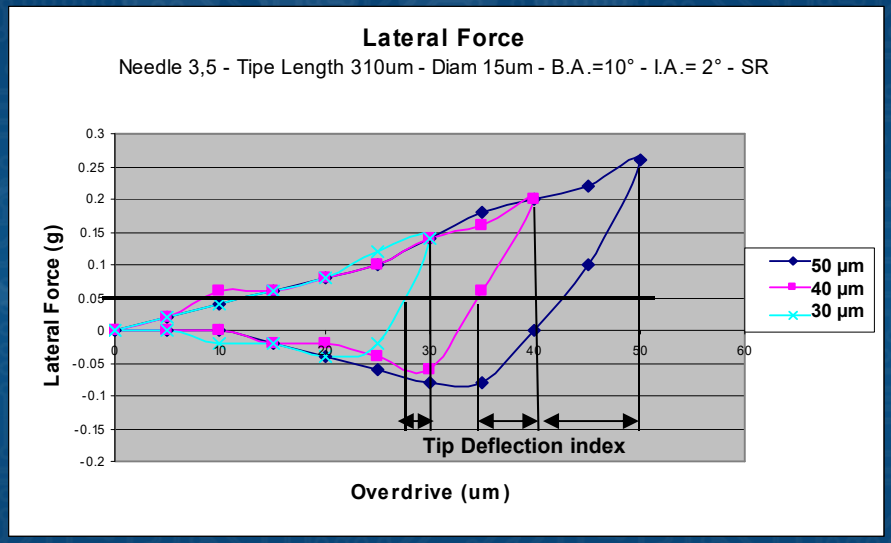


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Lateral Force and Overdrive

- **The lateral force is function of the Overdrive.**

  – Looking at the diagram below it is possible to observe that the tip deflection and the max measured lateral force increase with the overdrive.



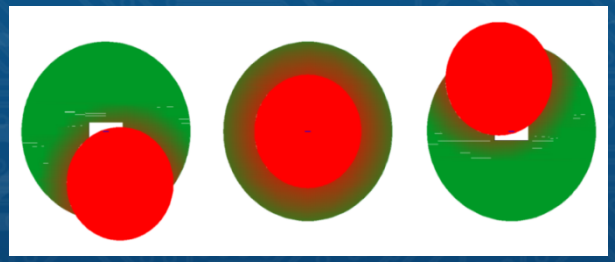
  – The Overdrive can't overtake a max value that is specified by probe card vendors, to avoid the plastic probe deformation.

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Scrub and temperature 1/4

- **Temperature variation makes everything dynamic:**
  - Prober and probe card are made of different components.
  - Each component is made of different materials with different thermal expansion coefficient.
  - When there is a temperature change all the mechanical elements, fixed together, expand with the final result of a structural deflection.
  - Thermal gradients are also present depending over x,y,z location and are changing during probing over time

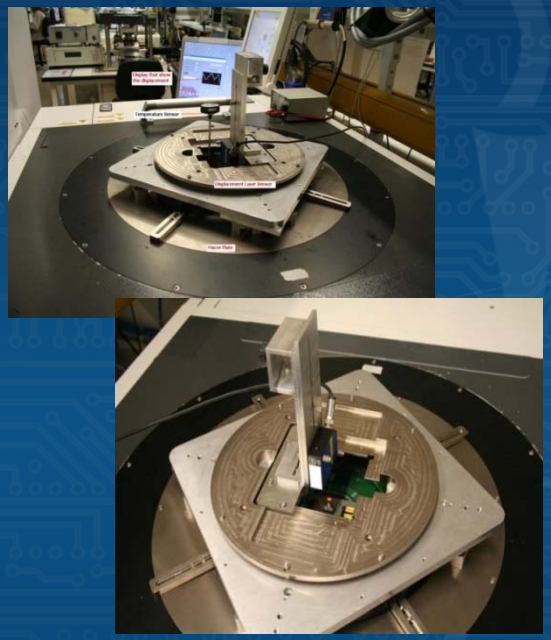


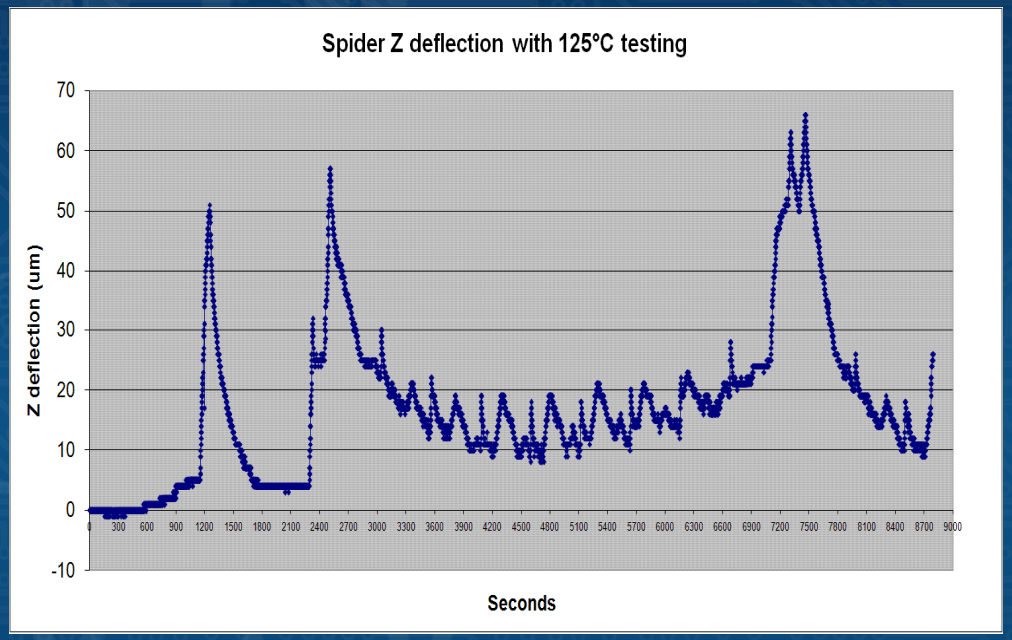
  - On-line cleaning, visual inspection, wafer change and every time that the hot chuck isn't under the card induce a temperature variation of the probe card, which is reflected in the probe head Z position change.

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Scrub and temperature 2/4

- Below a STD probe card Z deflection measured during a full wafer test.





- Test at high temp can increase the pad damage risk due to the probe card deflection and the consequent poor overdrive control.
  The real Overdrive used could be higher than the programmed one.

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Scrub and temperature 3/4

- The Aluminium layer, at high temperature, became softer cushioning the tensile stress transmitted to the structures under pad.
- The scrub mark will thus change especially in terms of scrub depth. Below some measurement obtained with NoScrub Technology on blank wafer with 1,5 µm of Aluminum.

	50 µm OT 30°C	50 µm OT 150°C
x1		
x3		
x6		

Force	1.4 g
Tip diameter	16 µm

N° TDs	50 µm OT 30°C			50 µm OT 150°C		
	Length (± 4 µm)	Width (± 3 µm)	Z (± 0.15 µm)	Length (± 4 µm)	Width (± 3 µm)	Z (± 0.15 µm)
1TD	17	13	0,6	19	15	0,9
3TDs	18	14	0,65	21	16	1
6TDs	19	15	0,75	22	16	1

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Scrub and temperature 4/4

- **Below some experimental scrub measurements on Al Blank wafer with 1,5 µm thickness using TPEG™ MEMS probes.**

	50 µm OT 30°C	50 µm OT 150°C
x1		
x3		
x6		

Force	4,5 g
Tip diameter	14 µm

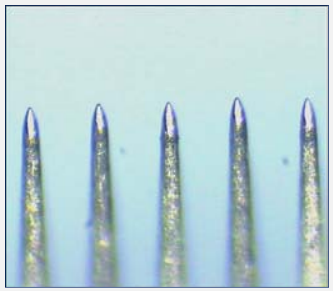
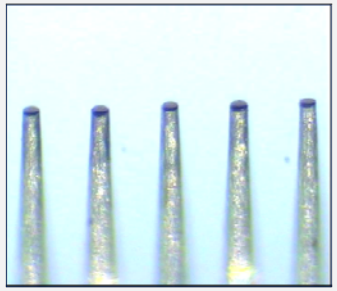
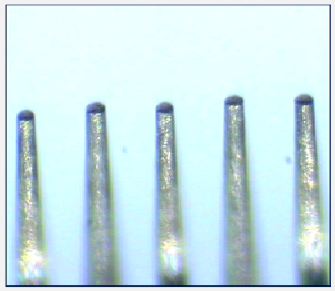
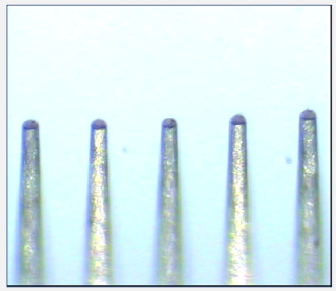
N° TDs	100 µm OT 30°C			100 µm OT 150°C		
	Length (± 4 µm)	Width (± 3 µm)	Z (± 0.15 µm)	Length (± 4 µm)	Width (± 3 µm)	Z (± 0.15 µm)
1TD	23.4	19.8	0.6	27	19.8	0.9
3TDs	25.8	21.3	0.65	28	21.3	0.98
6TDs	26.5	22.0	0.75	28.5	22.0	1.1

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Pad damage and polishing

- Some cleaning sheets normally used for polishing on-line can reduce the contact diameter increasing the pressure on pad.
- Cleaning frequency, overdrive and N°TD have to be set properly to avoid an excessive probe tip dia reduction. The contact surface of the probes doesn't have to become smaller than the diameter specified by probe card vendor for new probe card.

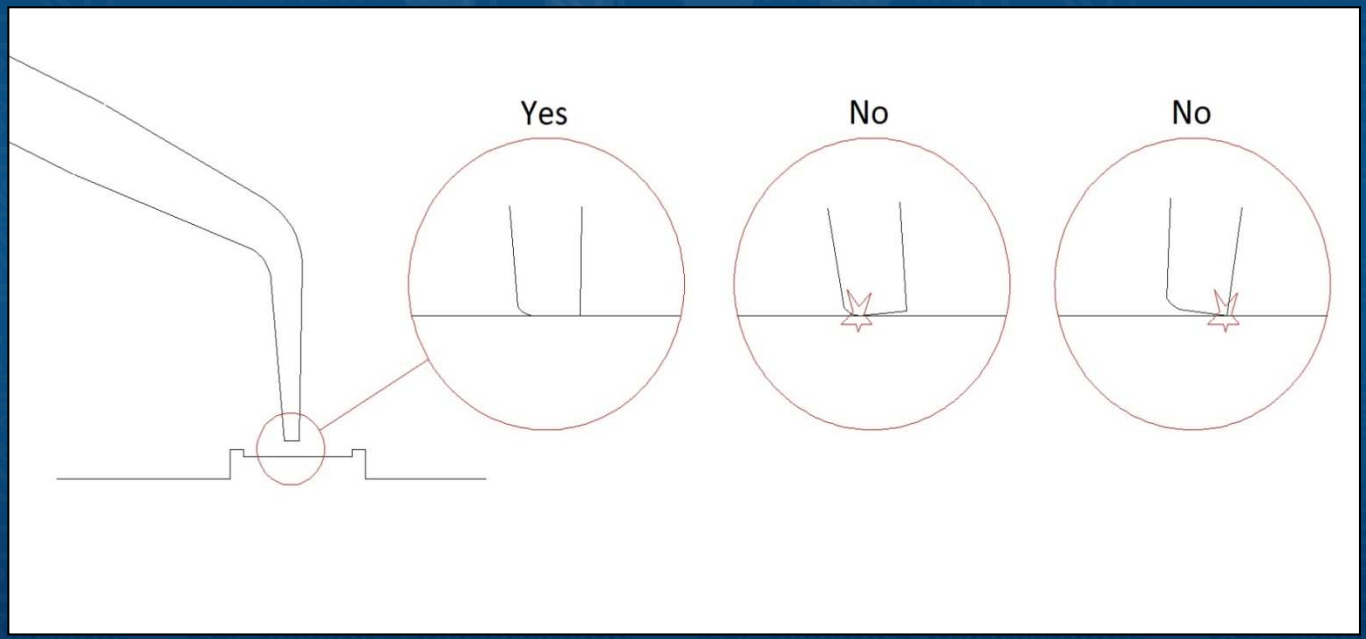
ITS Probe Polish 300, after 37500 TD		MIPOX GC8000 PF3 1µm, after 37500 TD	
Sharpened tips are observed. Similar effect is obtained with **Mipox WA6000 SWE**		Tip shape is maintained. The heels looks rounded.	
ITS Probe Lap 3µm, after 35000 TD		**ITS Probe Scrub 3µm, after 35000 TD**	
Tip shape is maintained, good roughness of the contact surface. Similar effect is obtained with **3M pink paper**		Tip shape is maintained, slightly rounded.	

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Pad and probe contact surfaces parallelism

- **The pad damage risk can increase if the probe contact surface isn't parallel to the pad surface. Every kind of probe damage or serious misalignment could cause cracks due to the high pressure concentrated in a little pad area.**

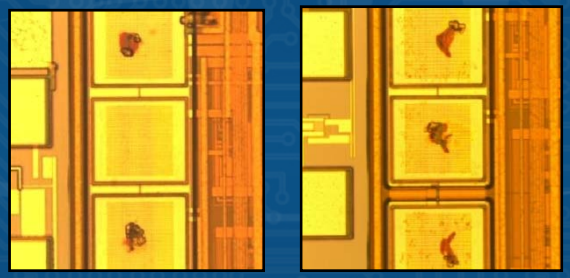


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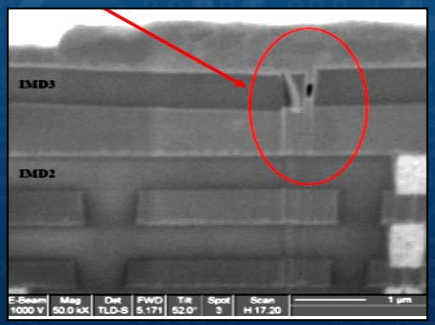
Pad damage analysis

- **Technoprobe has the capability to customise product performances following customer needs. When a new type of pad is developed, it's important to perform some crack test to define the best and reliable solution.**

- **It's common to perform some pad analysis after many TDs, performed on the same pad position, simulating the worst test case.**
  - Physical analysis (Delayering + visual inspection) on probed pad



  - Cross section:



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Conclusions

- **Probe pressure on pad is a better parameter to be considered than just vertical force**
- **The shear stress is an important parameter to be controlled for pad damage in cantilever cards. It can be controlled working on:**
  - Probe pressure on pad
  - Tip shape
  - Tip length
  - Needle material (Young modulus, tensile strength and other mechanical characteristics has to be considered for pad damage).
- **Copper, Nickel or other metallization exposure can be avoided using wide and short tips to decrease the digging action.**
- **Probe contact surface finishing and parallelism with the pad have to be considered**

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Follow-on Work

- It was demonstrated that a control of the chuck movement can decrease the pad damage probability (Soft Touch)
- Some Technoprobe internal trials show that, changing the chuck speed, it is not possible to observe a relevant modification in the scrub marks.
- Further investigations are needed to study the relationship between impact speed and pad damage.

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Thanks for your Support !

Raffaele Vallauri.
R&D Manager
Technoprobe

Marco DiEgidio
R&D Senior Engineer
Technoprobe

Emanuele Bertarelli
R&D Senior Engineer
Technoprobe

SW Test Workshop - June 5-8, 2016

SW Test Workshop
Semiconductor Wafer Test Workshop

Automated Thermal Drift Correction of Discrete Probes on Motorized Positioners for Device Characterization

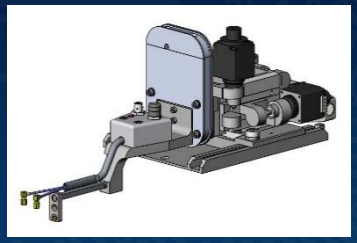
Joe Frankel

Koby Duckworth

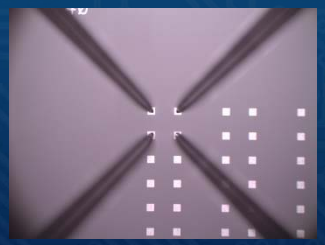
Cascade Microtech, Inc.

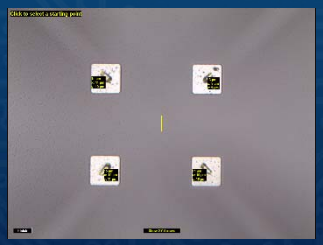
June 5-8, 2016

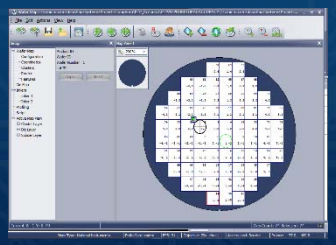
Introduction



- **Problem: As pad sizes shrink from 40um to 30um and smaller, fixed DC probes can no longer make reliable contact over temperature**
- **Approach: Motorize positioners and add controls to enable Unattended Testing at Multiple Temperatures (UT@MT) on Cascade CM300 Probe Stations**
  - Perform probe-to-pad realignment automatically when changing temperature, loading wafer, or stepping to new die
  - Develop fully autonomous operation



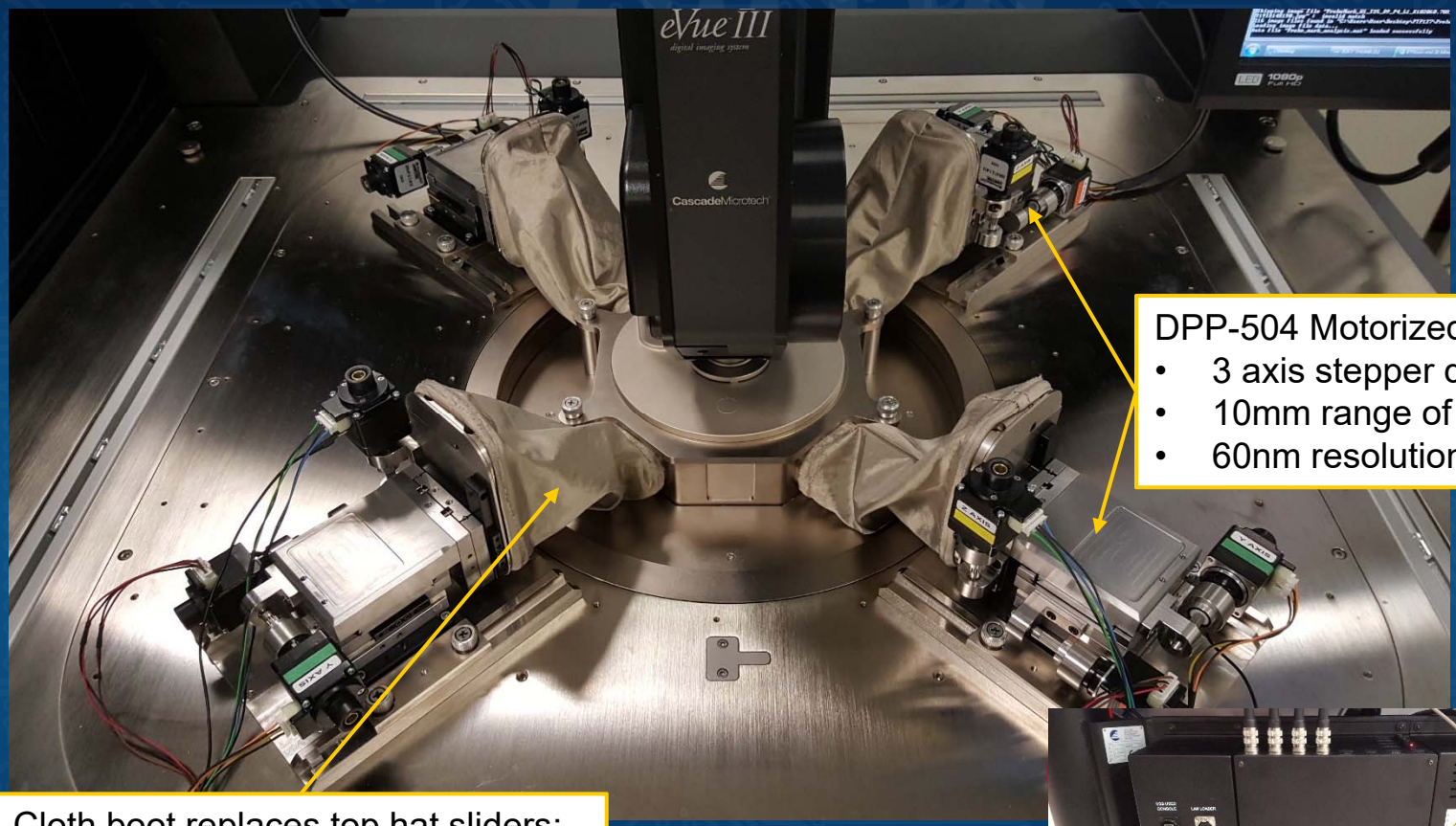




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Motorized Positioner Hardware



DPP-504 Motorized Positioners
- 3 axis stepper drives
- 10mm range of travel
- 60nm resolution



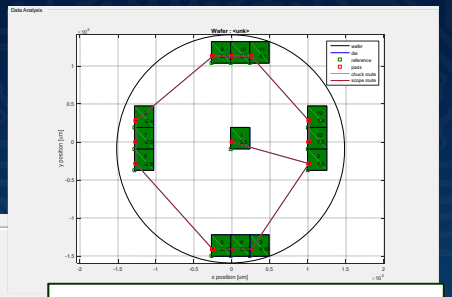
Cloth boot replaces top hat sliders:
- Low friction
- Thermal isolation
- EMI shielding (conductive)
- Light tight

MPX positioner controller installs in back of probe station

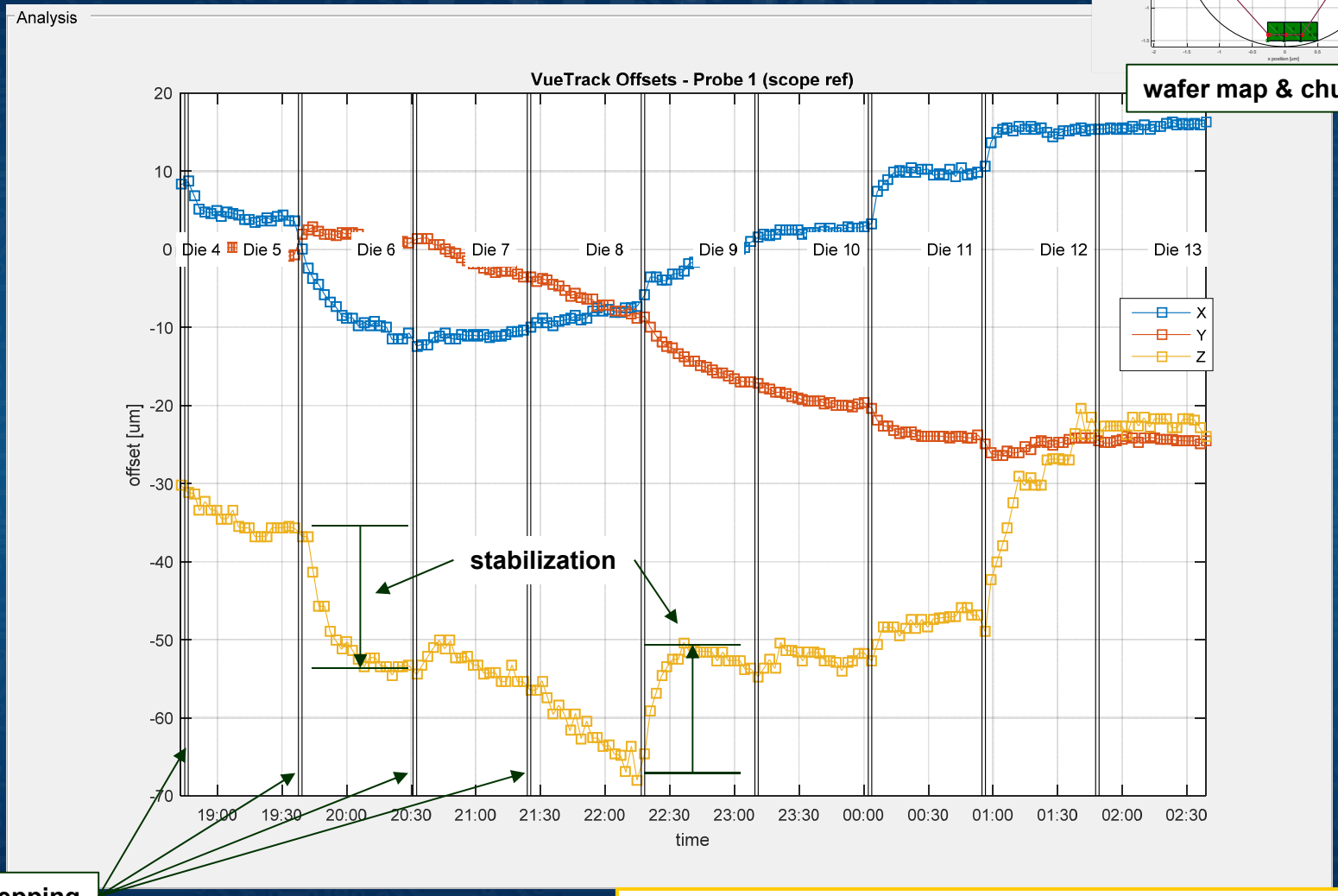
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Stabilization Time



wafer map & chuck route



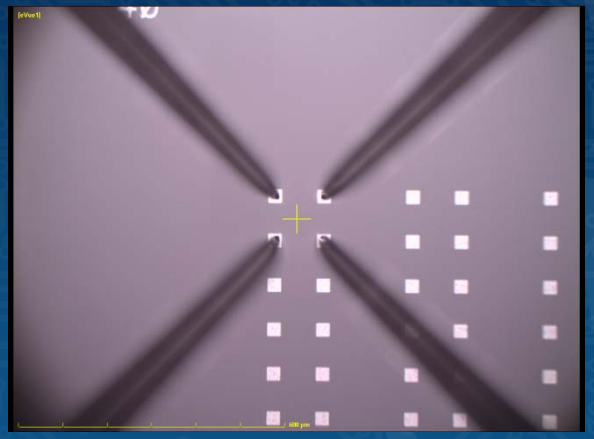
die stepping

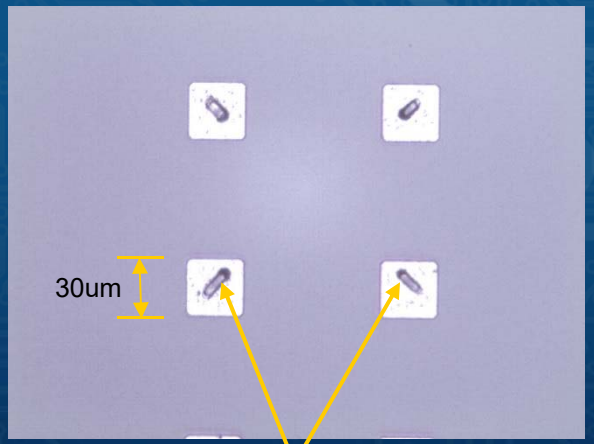
Uncorrected probe-to-pad motion due to die stepping at temperature exhibits well behaved 1st order response, and can be used to optimize die soak time

J. Frankel

SW Test Worksh

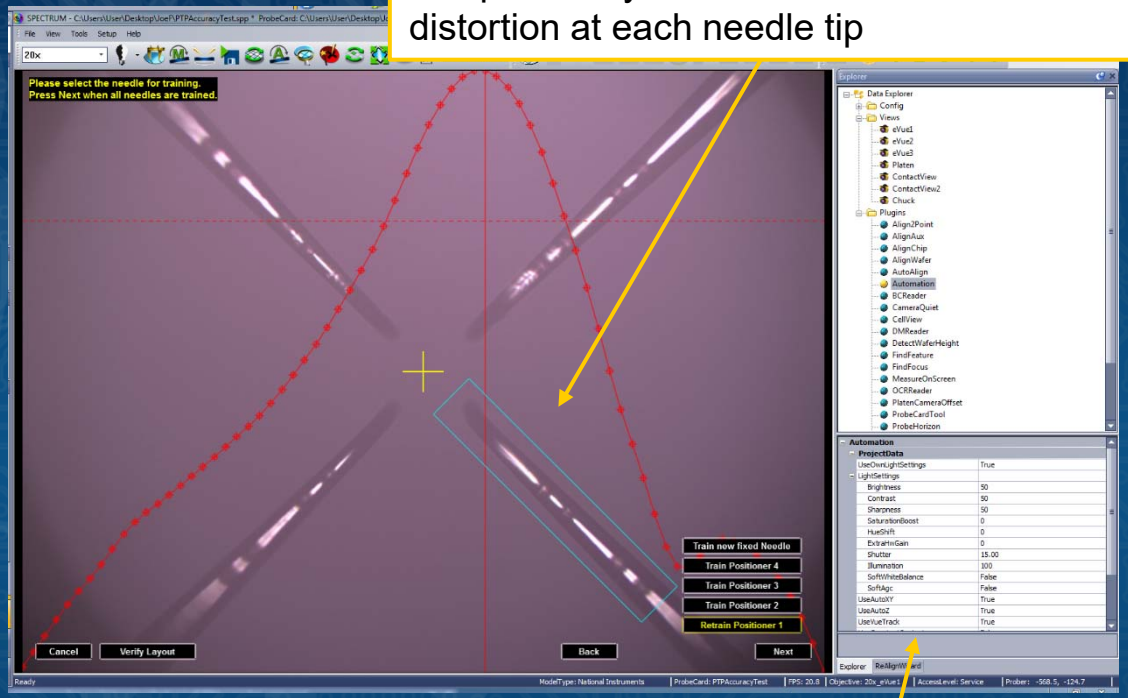
VueTrackPro Software

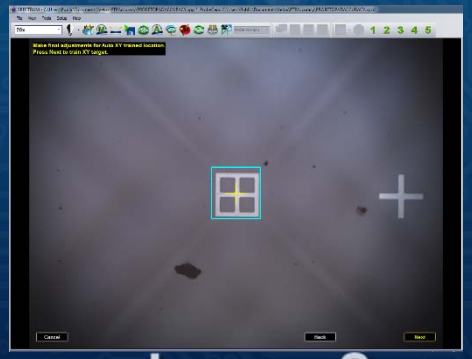




Unattended performance demonstrated over temperature on 30um pads

Vision-based position feedback independently corrects for thermal distortion at each needle tip





New capabilities with VueTrack Automation (*VueTrackPro*) to control motorized positioners

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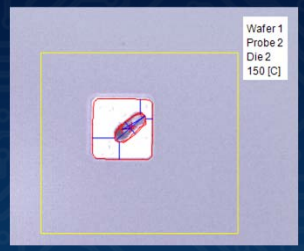
Verification Use Case Parameters

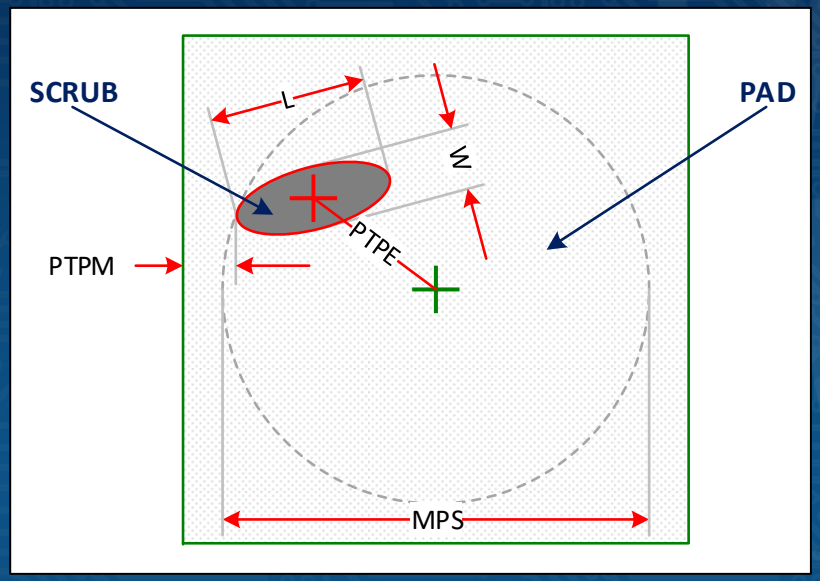
Parameter	Specification
Probe Station	CM300
Probes	DCP-HTR w/fiducial marks
Tip diameter	10 μm
eVue Objective	20X
Scrub Length	15-25 um
Contact Resistance	< 2 Ω
Temperature Range	-60C to +200C
Wafer Soak Time	3 hrs
Die Soak Time	10 min

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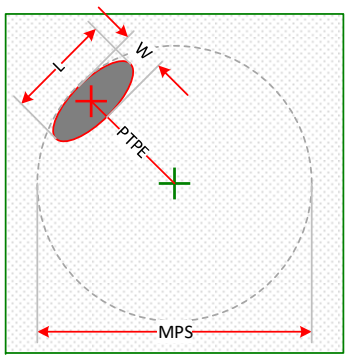
FormFactor v. Technoprobe
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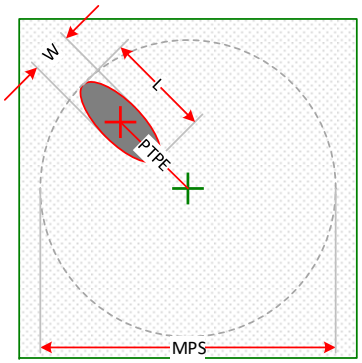
Probe-to-Pad Accuracy Metrics





MPS Constraints





$MPS = 2PTPE + W$ $MPS = 2PTPE + L$

$$2\boldsymbol{PTPE} + \boldsymbol{W} \leq \boldsymbol{MPS} \leq 2\boldsymbol{PTPE} + \boldsymbol{L}$$

Terminology	Unit	Definition
Minimum Pad Size (MPS)	µm	radial distance from center of pad to furthest point on scrub mark
Effective Pad Size (EPS)	µm	EPS = MPS – Tip Diameter
Probe-to-Pad Error (PTPE)	µm	radial distance from center of pad to center of scrub mark
Probe-to-Pad Margin (PTPM)	µm	shortest distance from scrub mark to edge of pad
Scrub Length (L)	µm	length of long axis of scrub mark
Scrub Width (W)	µm	length of short axis of scrub mark
Contact Resistance (CRES)	Ω	Resistance between probe tip and wafer as obtained by Kelvin measurement with B1505A

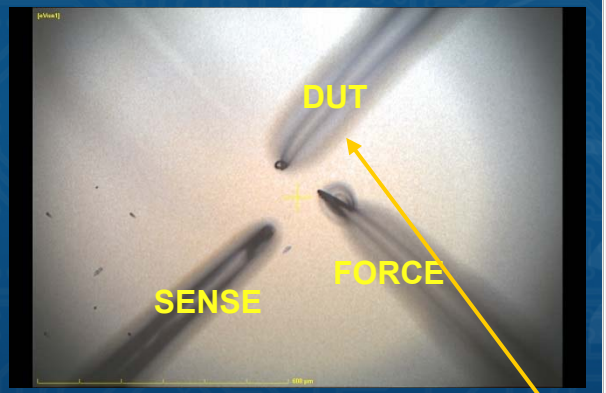
FormFactor Ex. 1031, p. 247

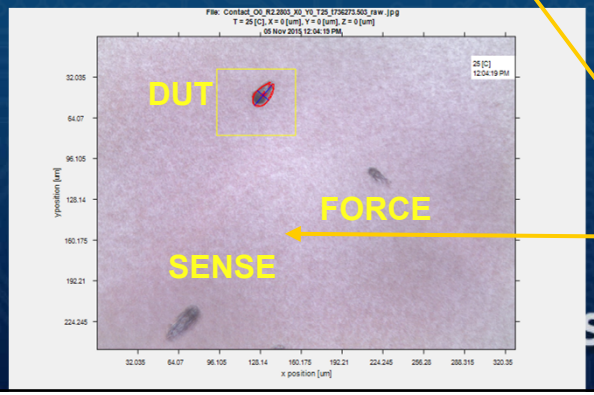
FormFactor v. Technoprobe
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Data File:
CRES003

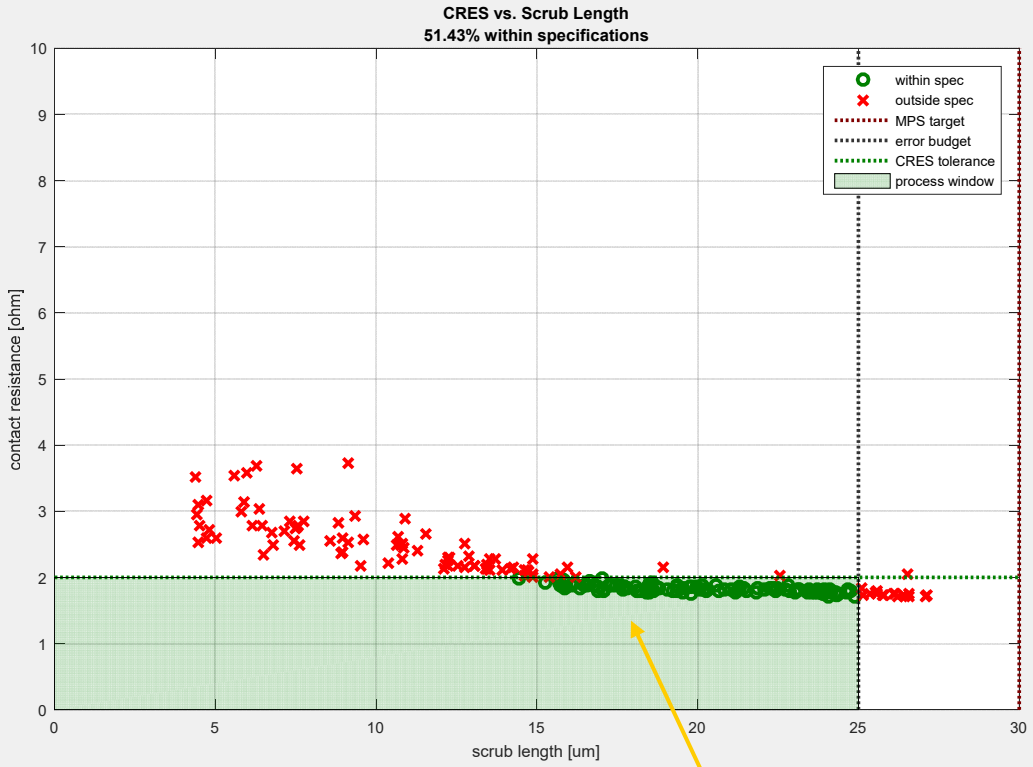
CRES vs. Scrub Length Characterization







Data Analysis

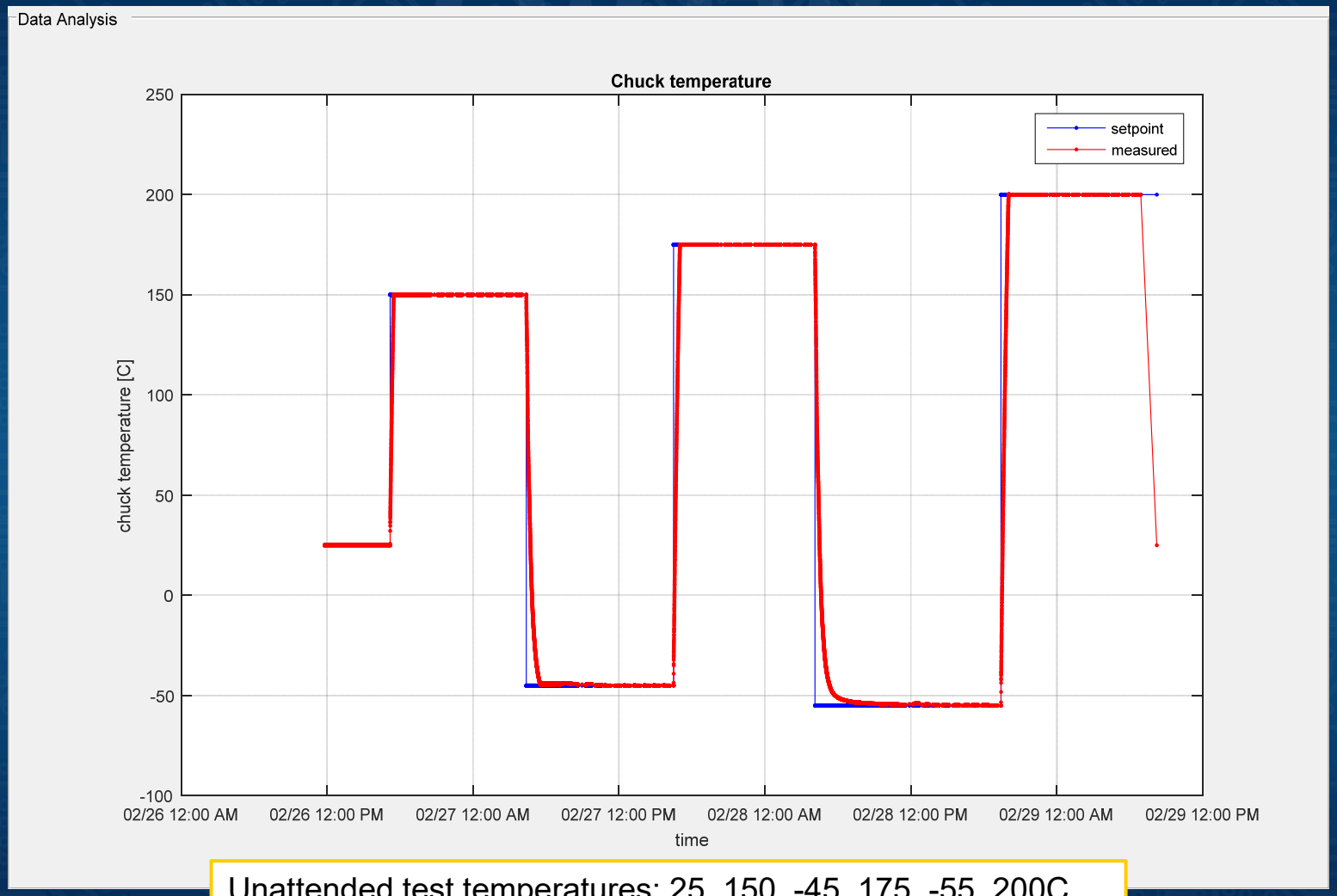


- Contact resistance measured with Keysight B1505A in Kelvin configuration
- Scrub length measured with automated image processing

→ ***Data indicates process window of CRES < 2ohm for scrub length >15um*** *on Cascade test wafer*

Data File:
PTP127

Chuck Temperature vs. Time

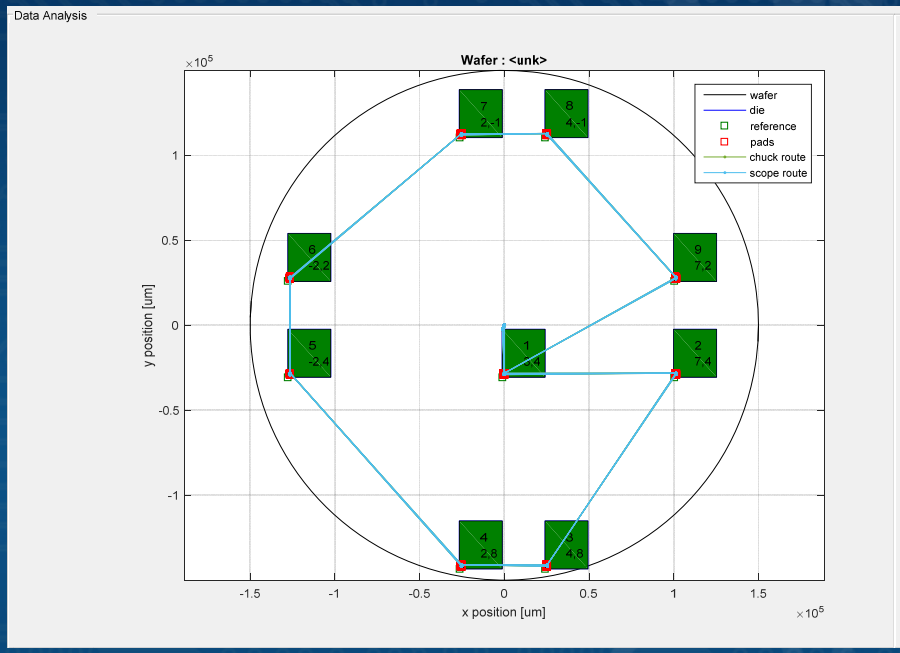


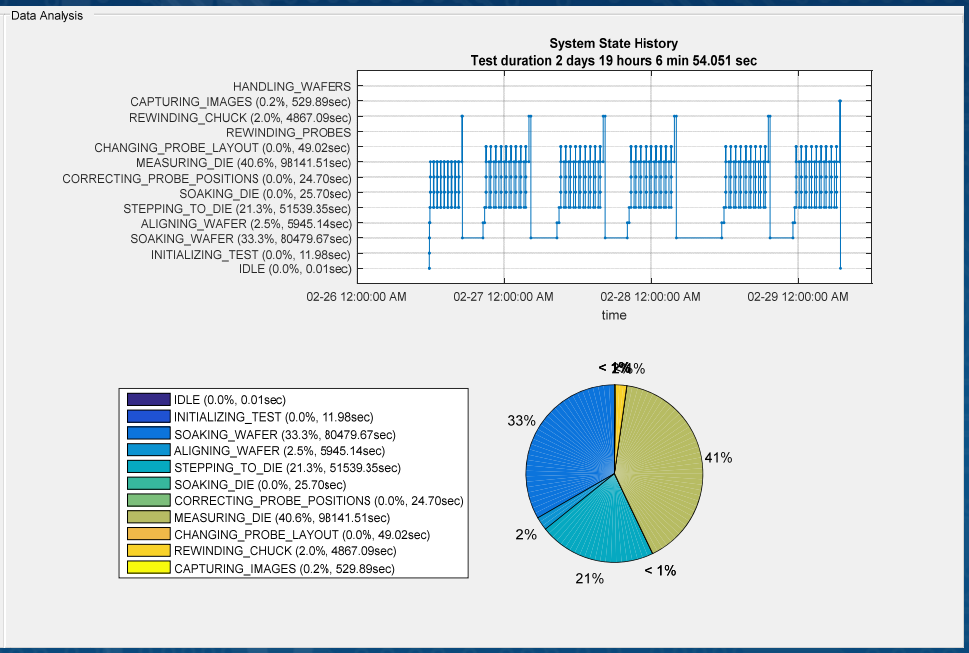
Unattended test temperatures: 25, 150, -45, 175, -55, 200C

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Wafer Map & System State





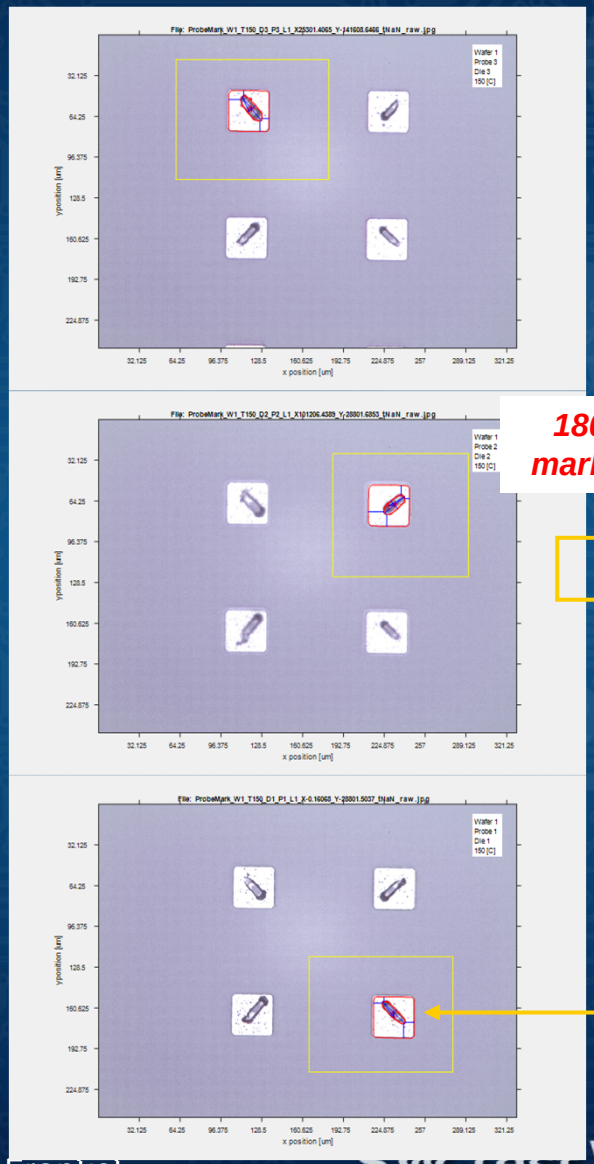
Wafer map illustrates selected die and chuck motion route vs. XY

System state chart illustrates thermal transitions, wafer stepping, and probing over multiple temperatures vs. time, as well as breakdown of system utilization

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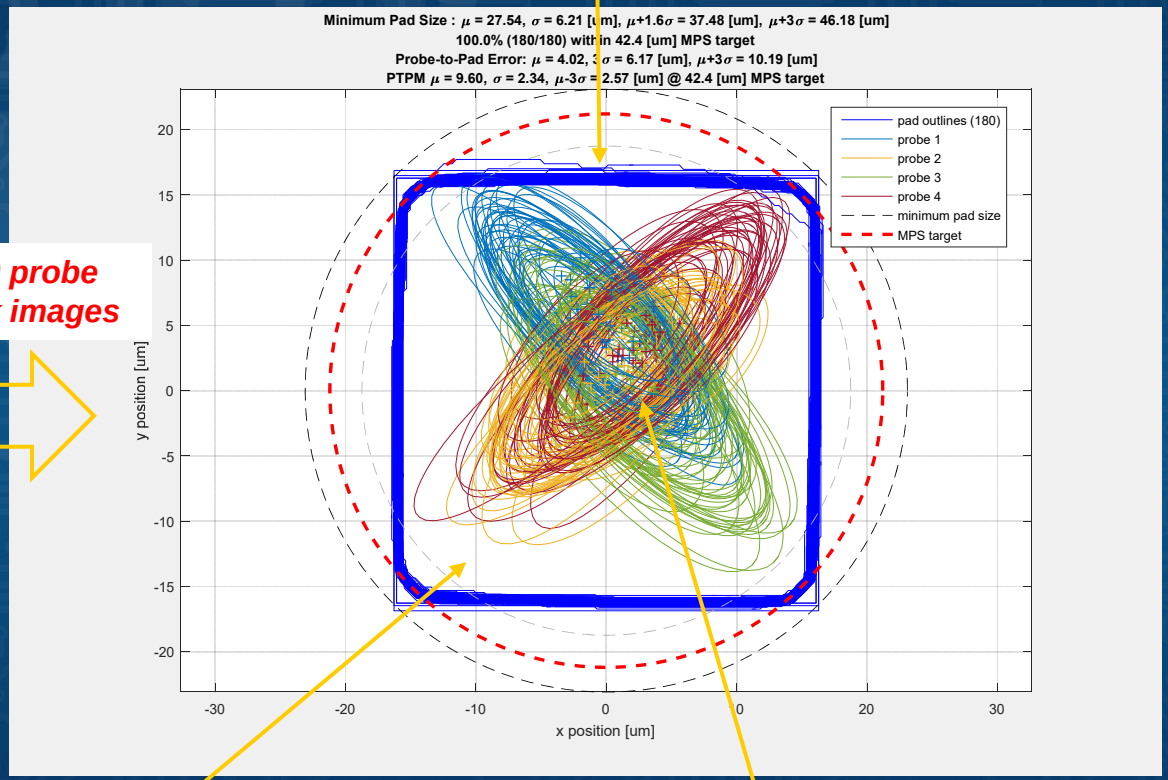
Data File:
PTP126

Probe-to-Pad Accuracy - Spatial



180 probe mark images

Unattended test temperatures: 25, -55, -40, 150, 175C



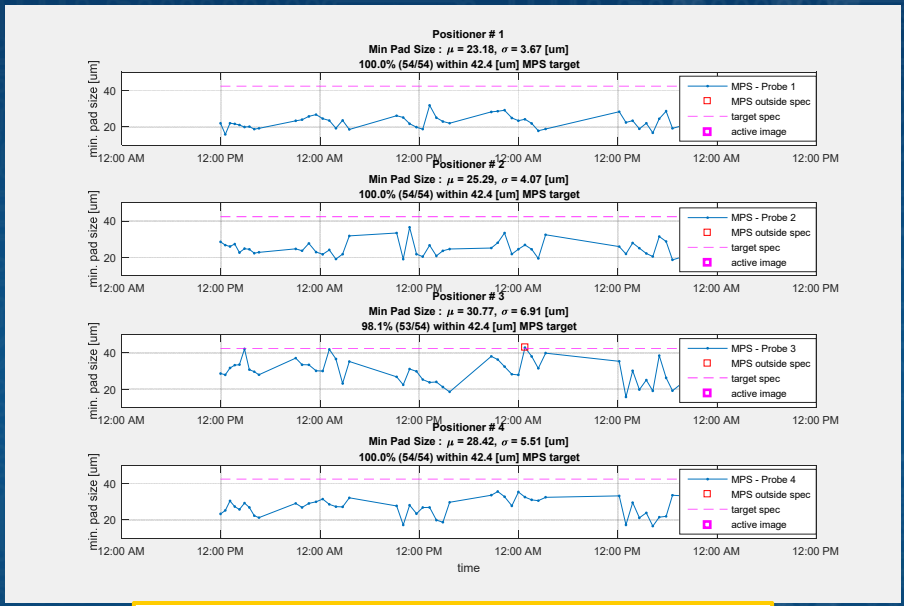
30um pads

Scrub mark measurements
All 180 marks within 30um pads in this example

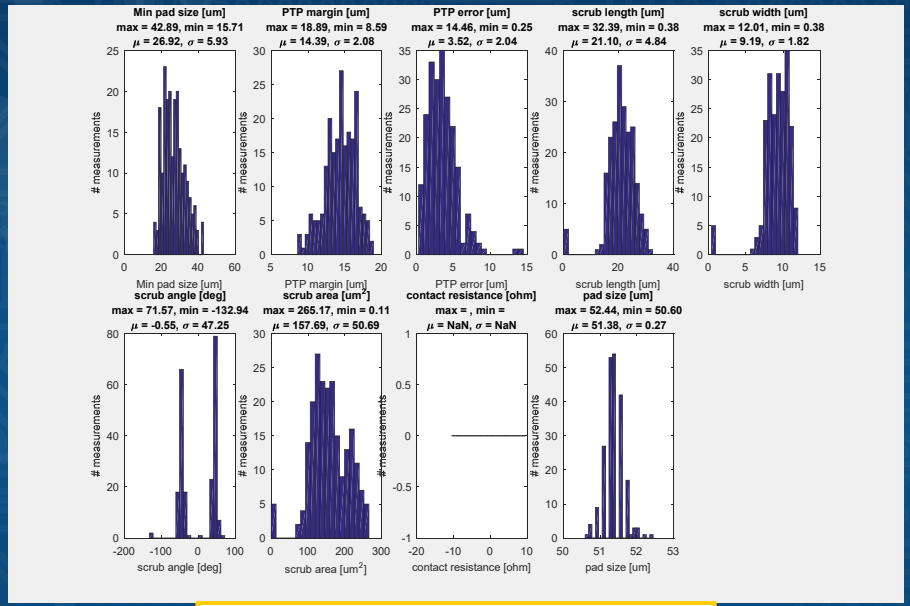
FormFactor Ex. 1031, p. 251

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Probe-to-Pad Accuracy – Temporal & Statistical



Minimum pad size vs. time by probe



Accuracy metric distributions

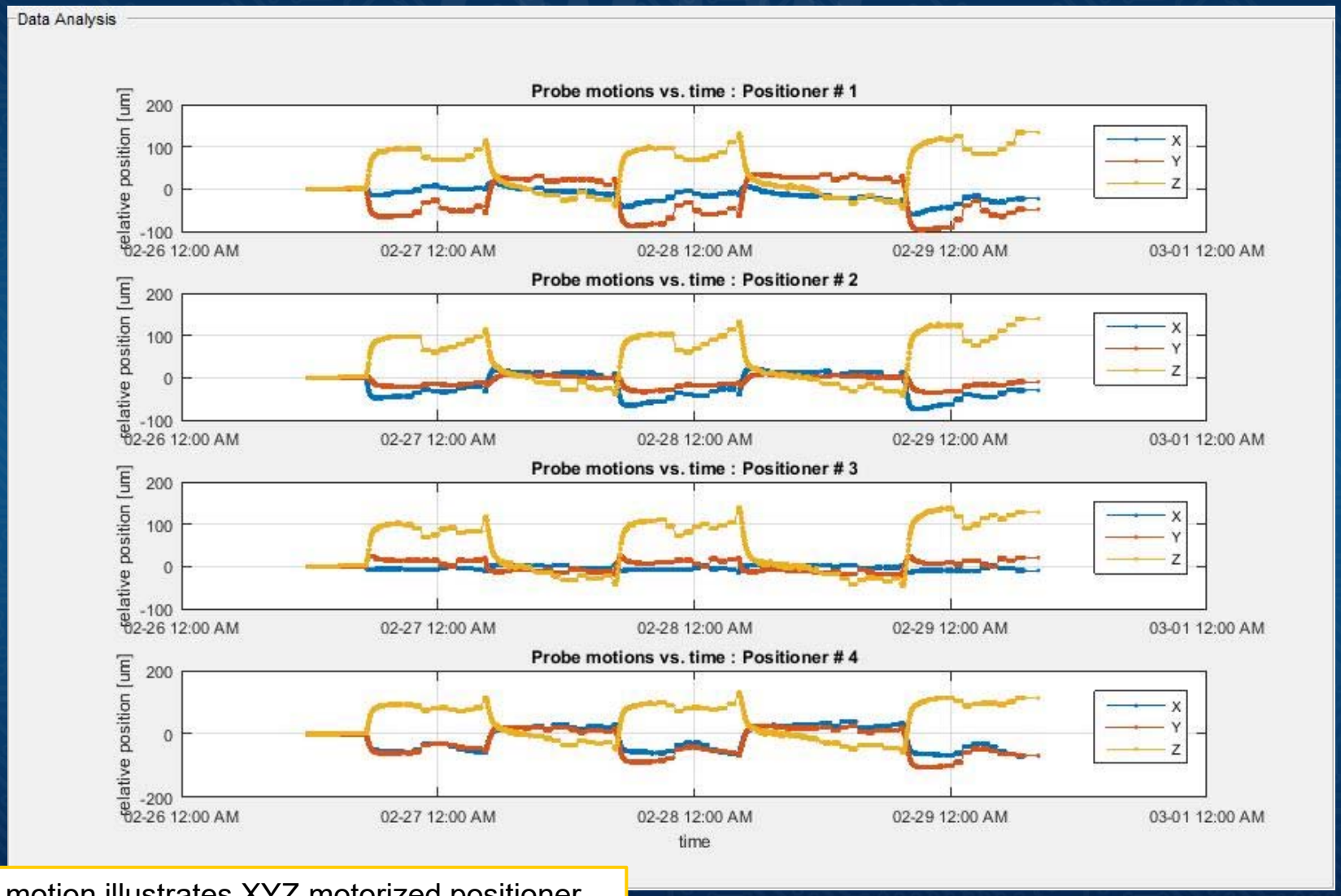
Looking at data from different perspectives provides insights into probing performance and enables troubleshooting

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Data File:
PTP127

Probe Motion vs. Time



Probe motion illustrates XYZ motorized positioner correction at each die step and thermal transition

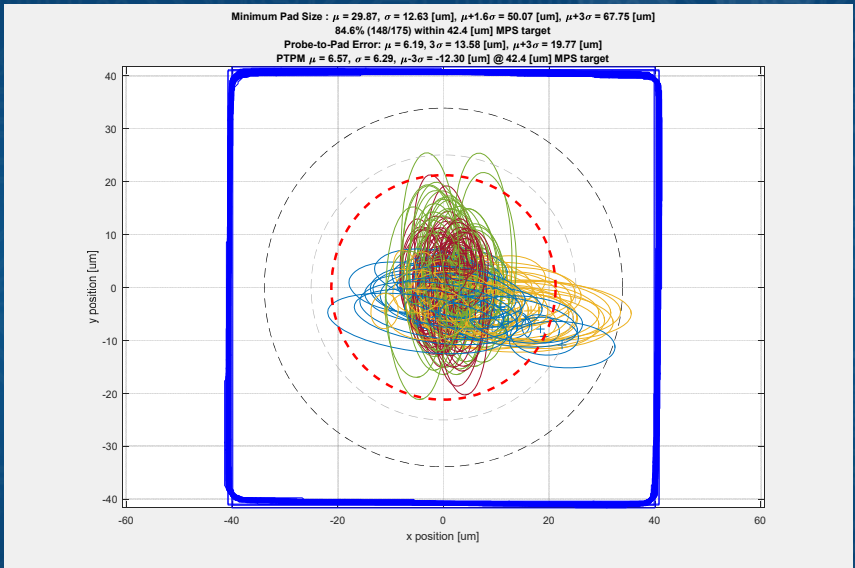
FormFactor Ex. 1031, p. 253

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Motorized vs. Non-Motorized

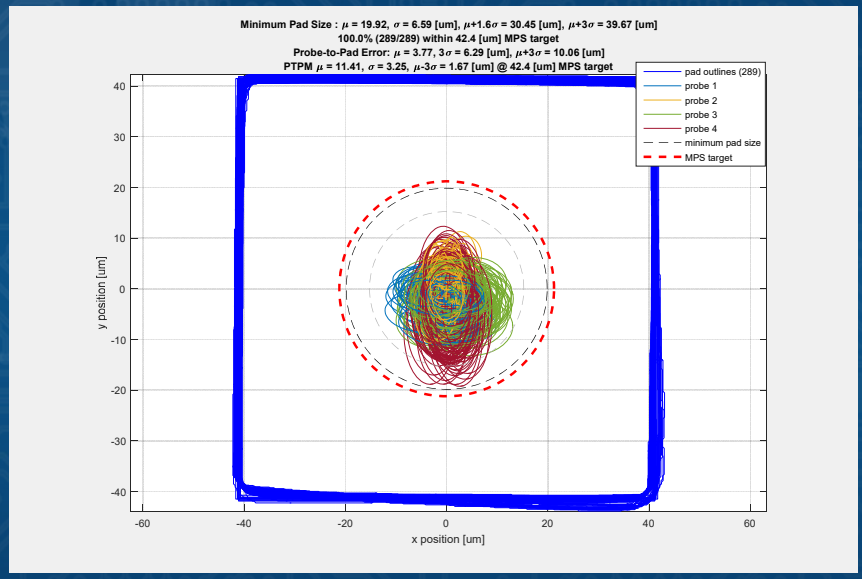
Non-Motorized, Uncorrected

MPS 67.75 um (3σ)



Motorized, Corrected

MPS 39.67um (3σ)



Minimum Pad Size (MPS) metric reduced by motorized correction when stepping and probing at temperature relative to uncorrected case

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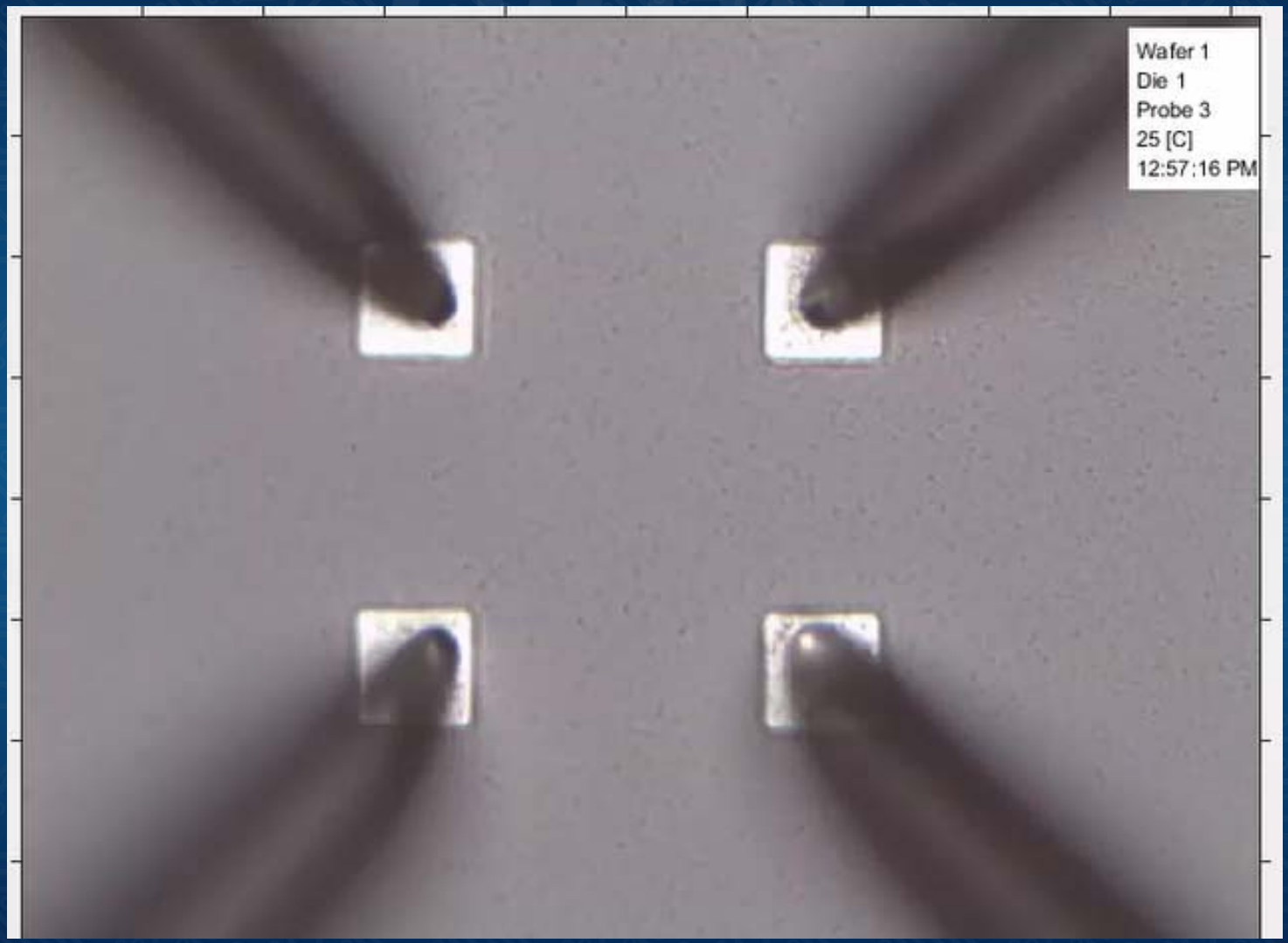
Conclusions

- Vision-based alignment with laser etched tips enables correction of thermal distortion anywhere in the probe-to-pad kinematic loop after stabilization
- Autonomous probing of 30um pads over temperature has been demonstrated at Cascade Microtech in Germany and the US
- Autonomous probing of 30um pads over temperature has also been demonstrated at a key customer site

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Data File:
PTP126

UT@MT Probing Animation



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