

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FORMFACTOR, INC.,
Petitioner,

v.

TECHNOPROBE S.P.A.,
Patent Owner.

Case IPR2024-00933
Patent No. 11,035,885

PATENT OWNER'S RESPONSE

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I. Introduction

The Board should rule in its Final Written Decision that Petitioner fails to show by a preponderance of the evidence that any of Challenged Claims 1-23 of the '885 patent is unpatentable. The '885 patent discloses and claims—through independent and dependent claims of varying scope—detailed configurations of a testing head configured to verify the operation of a device integrated on a semiconductor wafer. To challenge these claims, Petitioner relies on a hodgepodge of seven grounds spanning various combinations of references. These grounds and combinations are flawed because they are missing claim limitations, lack the requisite motivation to combine or modify the references, and are premised on Petitioner's inconsistent positions advanced throughout the Petition.

As one example, Petitioner relies on *Kim* to teach claim 2's requirement that “the first conductive portion is *locally interrupted* by at least one non-conductive zone.” But *Kim* does not disclose this limitation. To compensate, Petitioner advances (a) an implicit construction of “locally interrupted” that contradicts the specification; and (b) a backup obviousness position based on a conclusory “design choice” argument rooted in hindsight. *See infra* Section IV.A.

As another example, Petitioner fails to show that *Kim* renders obvious claim 7's requirement that the “at least one guide includes at least one third conductive portion that includes and electrically connects a third group of the guide

holes to each other and house third contact elements configured to carry *input/output signals*,” because *Kim* does not disclose or suggest electrically connecting pins that carry input/output signals. At times, Petitioner and its expert recognize this deficiency, while relying on vague statements in *Kim* that simply fall short of teaching the claim limitation. *See infra* Section IV.C.

The Petition’s deficiencies continue in Petitioner’s proposed combination of *Kim* with *Schmid* for claims 6 and 23. These claims require that “*the first and second conductive portions [are] formed on a same face* of one of the upper, intermediate and lower guides and [are] physically and electrically separated from each other by at least one non-conductive zone.” But Petitioner fails to point to any prior art teaching where the alleged first and second conductive portions are formed on the same face of a guide plate. Petitioner attempts to compensate for these deficiencies by (a) misreading nebulous portions of *Kim* to infer a teaching that does not exist; and (b) propounding a conclusory obviousness argument that the prior art system “could be implemented” this way. *See infra* Section IV.E.

Similar problems persist throughout the Petition. Petitioner repeats similar “could be” based obviousness assertions for claims 5, 16, and 17. *See infra* Section IV.F. It likewise advances a conclusory “design choice” position for claim 14 that uses that claim as a roadmap. *See infra* Section IV.B. It fails to show that another reference, *Fan*, discloses the limitations of claim 3 and again relies on a conclusory

obviousness stopgap to fill the holes. *See infra* Section IV.G. It does the same for the *Bross* reference and claims 12 and 21. *See infra* Sections IV.H, IV.I. Compounding these problems, Petitioner inconsistently maps the prior art to the independent and dependent claims, undermining its position that the independent claims are unpatentable. *See infra* Section IV.J.

Thus, for the reasons discussed herein and as supported by Patent Owner’s expert, Dr. Souri (Ex. 2001, ¶¶1-160), Patent Owner requests that the Board find Petitioner fails to meet its burden of demonstrating that the claims are unpatentable.

II. Level of Ordinary Skill in the Art

Petitioner contends that a person of ordinary skill in the art (“POSITA”) would have had:

at least a bachelor’s degree in electrical engineering, mechanical engineering, *and* materials engineering or another field applicable to wafer probing technology *with* three to five years of professional experience in designing and/or using probe technologies, or an equivalent level of skill, knowledge, and experience.

Pet., 22 (citing Ex. 1003 ¶¶50–53) (emphases added). The Board adopted this definition in its Institution Decision. Paper 9 at 10. Petitioner’s definition includes typographical errors (emphasized above) that render it unclear. Thus, for purposes

of this response, Patent Owner has used the following definition that fixes those errors:

at least a bachelor's degree in electrical engineering, mechanical engineering, materials engineering, or another field applicable to wafer probing technology, and either three to five years of professional experience in designing and/or using probe technologies, or an equivalent amount of training or work experience.

Souri, ¶¶42-44. Moreover, additional education could substitute for professional experience, and significant work experience could substitute for formal education. *Id.*, ¶44; *see also id.*, ¶45. Patent Owner reserves the right to challenge Petitioner's definition in this or other proceedings, particularly if the record evidence supports a different definition.

III. Claim Construction

The Board construes claims under the standard set forth in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc); 37 C.F.R. § 42.100(b). Under this standard, claims receive their ordinary and customary meaning as would be understood by one of ordinary skill in the art in the context of the specification and the prosecution history. *Phillips*, 415 F.3d at 1314-19.

A. “the first conductive portion is locally interrupted by at least one nonconductive zone” (claim 2)

Claim 2 recites “the first conductive portion is locally interrupted by at least one nonconductive zone.” Petitioner does not propose an express construction for this term, but it implicitly interprets “locally interrupt[]” to mean providing a “gap” in the non-conductive zone. Pet., 39-40. The Board should reject this interpretation because it contradicts the ’885 patent’s disclosures. Instead, the Board should construe the phrase “the first conductive portion is locally interrupted by at least one nonconductive zone” to mean “the first conductive portion encloses at least one non-conductive zone.” This construction comports with the meaning of “locally interrupted” as it would have been understood by one of ordinary skill in the art in the context of the ’885 patent’s specification and prosecution history. *Souri*, ¶¶46-62.

As is “[u]sually” the case, the ’885 patent specification is “dispositive” and “the single best guide to the meaning” of this term. *Phillips*, 415 F.3d at 1315. Specifically, the ’885 patent distinguishes between two exemplary configurations: a first in which at least one conductive portion is *separated* from further conductive portions by at least one non-conductive zone, and a second in which the at least one conductive portion is *locally interrupted* by at least one non-conductive zone. It states: “[a]ccording to an aspect of the present disclosure, the at least one conductive

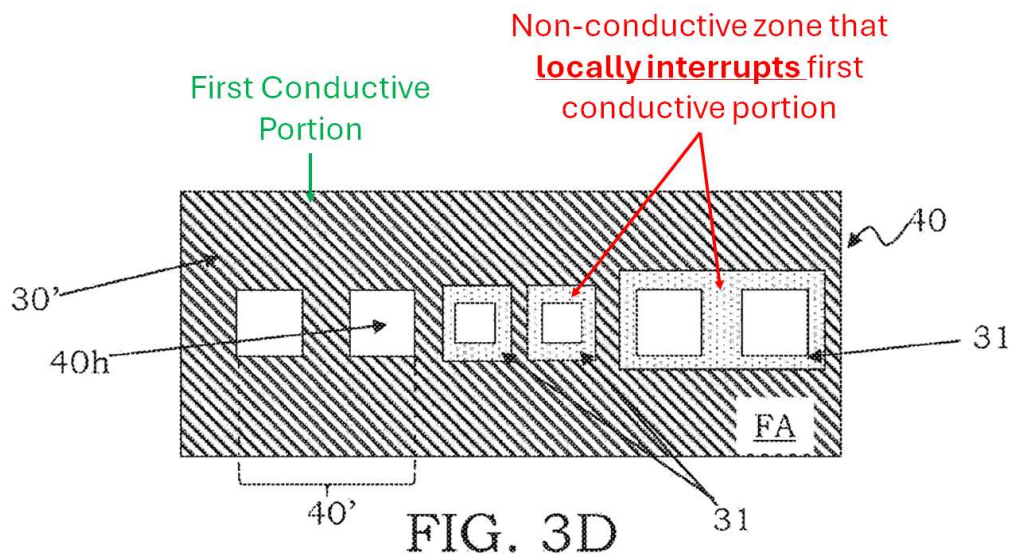
portion can be *separated* from further conductive portions *and/or* can be *locally interrupted* by at least one non-conductive zone.” ’885 patent, 3:56-59 (emphasis added). Claim 2, which recites “locally interrupted,” is directed to the second configuration. Souri, ¶49.

The ’885 patent describes embodiments demonstrating the difference between the conductive portion being “locally interrupted,” as in claim 2, and being “separated.” For example, the ’885 patent describes “locally interrupted” embodiments, explaining that “[i]f the first contact elements 21’ apt to carry ground signals and the second contact elements 21” apt to carry power signals are alternated one after the other, both the conductive portions 30’ and 30” are *locally interrupted* by suitable non-conductive zones 31’ and 31” (similarly to what observed in relation to FIGS. 3A-3D).” ’885 patent, 13:26-31 (emphasis added). It continues to explain the effects of “locally interrup[ting]” the conductive layer:

[E]ach conductive layer may be *locally interrupted* by suitable non-conductive zones 31” in order to not electrically connect contact elements that must not be short-circuited to each other. *In particular, the non-conductive zones 31” of a layer are formed at the holes housing contact elements that must not be short-circuited by said layer*, whereas said layer covers at least partially the walls of the guide holes housing contact elements that must be short-circuited by it.

Id., 14:2-10 (emphases added); Souri, ¶50.

This is precisely what is shown in and described with respect to Figure 3D. For example, the '885 patent explains that as “shown in FIG. 3D, the first conductive portion 30' covers a face of the guide 40 (the face FA in the example), except for areas where guide holes apt to house contact elements that must not be short-circuited are formed.” '885 patent, 10:38-41. It also explains that “the first conductive portion 30' is not formed in areas where the guide holes that do not belong to group 40' are formed.” *Id.*, 10:42-44. The result of this is that the first conductive portion 30' is “locally interrupted” by the non-conductive zones 31 because the first conductive portion 30' encloses the non-conductive zones 31 around those guide holes, as shown below in annotated Fig. 3D of the '885 patent. Souri, ¶¶51-52.



'885 patent, Fig. 3D (annotated).

Patent Owner's interpretation is also consistent with the Examiner's understanding of "locally interrupted" during prosecution. "Because an examiner . . . can be considered one of ordinary skill in the art, his construction of the asserted claims carries significant weight." *St. Clair Intell. Prop. Consultants, Inc. v. Canon, Inc.*, 412 F. App'x 270, 276 (Fed. Cir. 2011); *see also Phillips Petroleum Co. v. Huntsman Polymers Corp.*, 157 F.3d 866, 875-876 (Fed. Cir. 1998) (finding the examiner's understanding of a claim term during prosecution helpful "to elucidate the meaning of the claims"). The Examiner rejected the claim that would issue as claim 2 based on "Fig. 7, zone b" of *Kiyofuji* (US 2008/0139017, Ex. 2002), stating that in *Kiyofuji*, "the first conductive portion 48 is *locally interrupted* by at least one non-conductive zone 50b." Ex. 1002, 60 (emphasis added). *Souri*, ¶53.

Kiyofuji explains that "electrical insulating plate 40 has also a conductive earth pattern 46 on the upside and underside of the electrical insulating plate 40 and a conductive film 48 on the inner surface of each through hole 42." *Kiyofuji*, ¶[0059]. *Kiyofuji* further explains that "earth patterns 46 and conductive film 48 are electrically connected to each other" (*id.*, ¶[0060]). As shown in Fig. 7 of *Kiyofuji*, excerpted below, earth pattern 46 (horizontal hatched portions) is electrically connected to conductive film 48 (vertical hatched portions). Moreover, portion 50b is non-conductive and locally interrupts earth pattern 46, thereby also locally

conductive film 48 is electrically connected to earth pattern 46. Souri, ¶¶54-55.

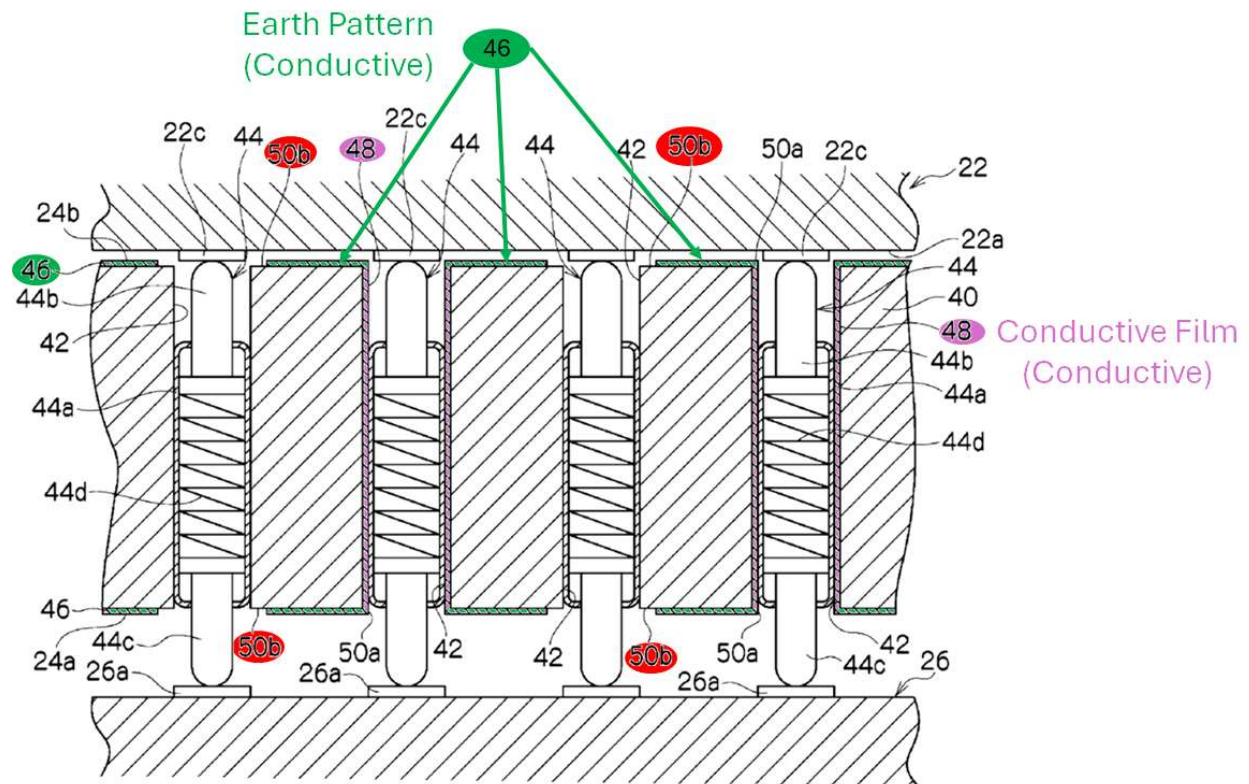


Fig. 7

Kiyofuji, Fig. 7 (annotated).

of the cross-sectional view shown in Fig. 7. *Kiyofuji*, ¶¶[0038]-[0039]; Souri, ¶56.

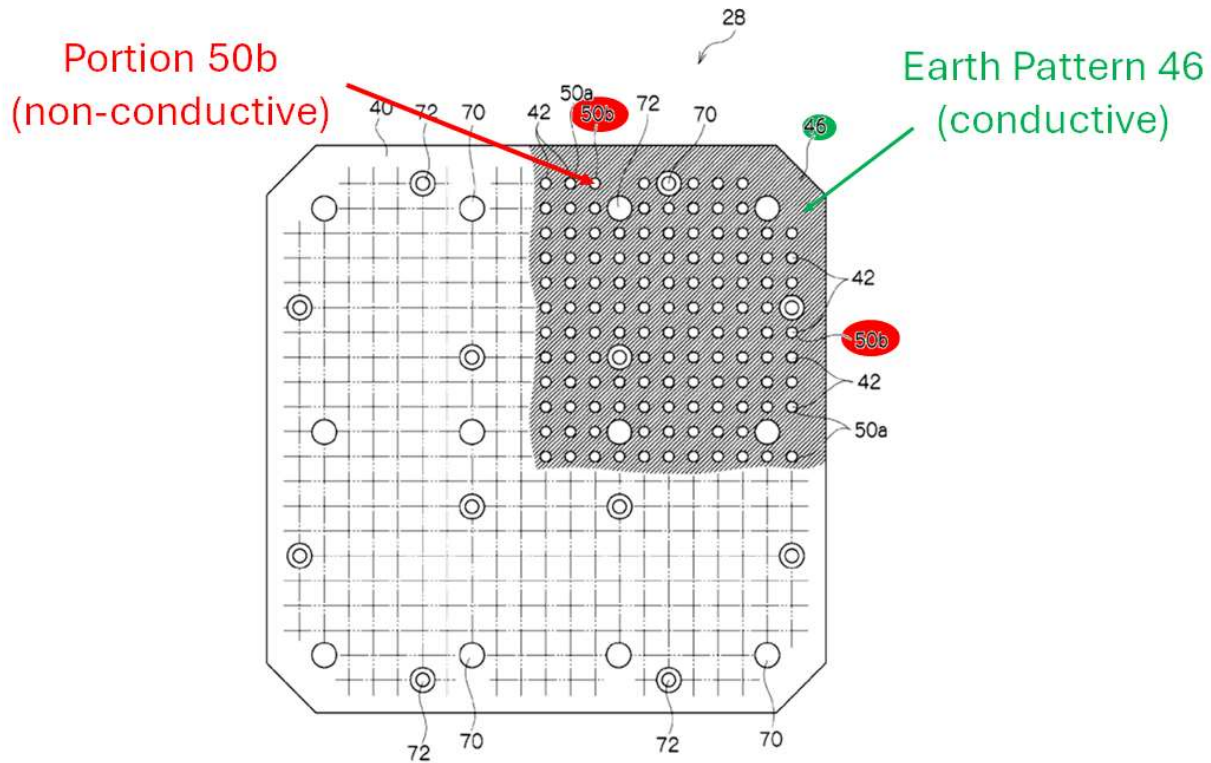
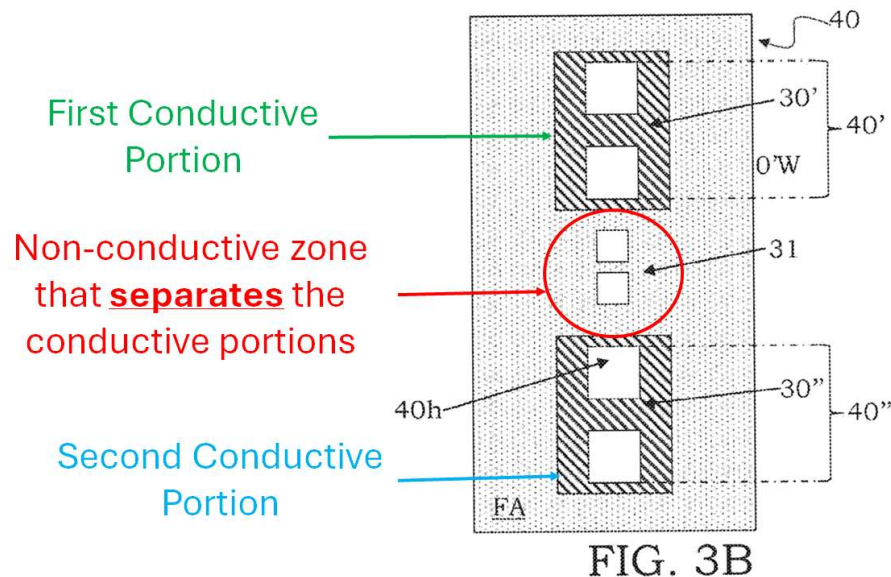


Fig. 6

Kiyofuji, Fig. 6 (annotated). As shown in Fig. 6 above, earth pattern (or conductive portion) 46, which is electrically connected to conductive film 48 (not shown in Fig. 6), encloses the non-conductive portion 50b. *Souri*, ¶57. Thus, consistent with Patent Owner’s interpretation, the Examiner determined that *Kiyofuji* discloses that conductive portion 46 of *Kiyofuji* is “locally interrupted” by non-conductive portion 50b because conductive portion 46 encloses non-conductive portion 50b. *Id.*

As discussed, the ’885 patent distinguishes the “locally interrupted” configuration from other configurations of the first conductive portion, which the ’885 patent describes using the term “separated.” For example, with reference to

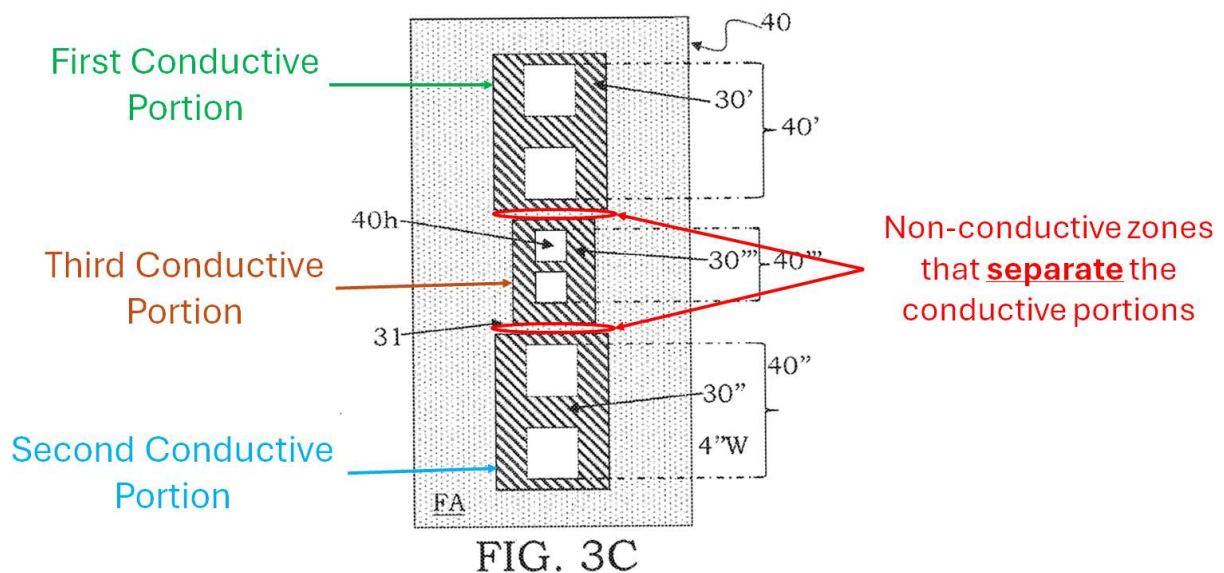
Fig. 3B, the '885 patent explains that the second conductive portion 30'' "is physically and electrically *separated* from the first conductive portion 30' by a non-conductive zone 31 of guide 40." '885 patent, 10:2-10 (emphasis added). Non-conductive zone 31 that *separates* (but does not locally interrupt) the first conductive portion 30' from the second conductive portion 30'' is illustrated in Fig. 3B below. Sourin, ¶58.



'885 patent, Fig. 3B (annotated).

As shown above, when non-conductive zone 31 *separates* the first conductive portion 30' from the second conductive portion 30'', the first conductive portion 30' or the second conductive portion 30'' does not enclose the non-conductive zone 31. Sourin, ¶59. Rather, the non-conductive zone 31 is located between and *forms a gap* between adjacently located conductive portions 30' and 30''. *Id.*

Similarly, with reference to Fig. 3C, the '885 patent discloses that “in addition to the first conductive portion 30' and to the second conductive portion 30”, also the third conductive portion 30''' is formed.” '885 patent, 10:11-13. The '885 patent explains that the third conductive portion 30''' “is physically and electrically *separated* from the conductive portions 30' and 30” by the non-conductive zone 31 of guide 40.” '885 patent, 10:17-19 (emphasis added). Non-conductive zone 31 that *separates* (but does not locally interrupt) the first conductive portion 30' or the second conductive portion 30” from the third conductive portion 30''' is illustrated in Fig. 3C of the '885 patent below. Sourin, ¶60.



'885 patent, Fig. 3B (annotated).

Here again, when the non-conductive zone 31 *separates* the first conductive portion 30' or the second conductive portion 30” from the third conductive portion 30''' , the first conductive portion 30', the second conductive portion 30”, or

even the third conductive portion 30''' does not enclose the non-conductive zone 31. Rather, the non-conductive zone 31 is located between and *forms a gap* between adjacently located conductive portions (e.g., 30' and 30''' or 30'' and 30'''). Souri, ¶61.

Thus, the '885 patent expressly distinguishes between a non-conductive zone that separates (*forms a gap*) between conductive portions from one that “locally interrupts” (*is enclosed by*) a conductive portion. Accordingly, a POSITA would have interpreted the phrase “the first conductive portion is locally interrupted by at least one nonconductive zone” to mean “the first conductive portion encloses at least one non-conductive zone,” based on the specification and figures of the '885 patent. Souri, ¶62.

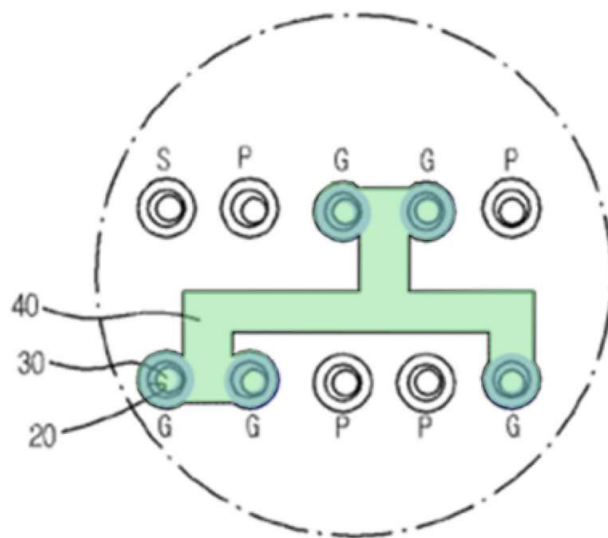
IV. Petitioner Has Not Demonstrated that Any Claim Is Unpatentable

A. *Kim* does not anticipate or render obvious claim 2 (Grounds 1, 2)

Petitioner alleges that *Kim* anticipates claim 2 (Ground 1) or renders it obvious (Ground 2). Pet., 39-40, 52-56. Petitioner’s arguments fail for the following reasons. Souri, ¶¶63-68.

Anticipation: Claim 2 recites “the first conductive portion is locally interrupted by at least one non-conductive zone.” Because claim 2 depends from claim 1, the first conductive portion that Petitioner identified in its analysis of claim 1 must also be the first conductive portion in its analysis of claim 2. *See, e.g.,*

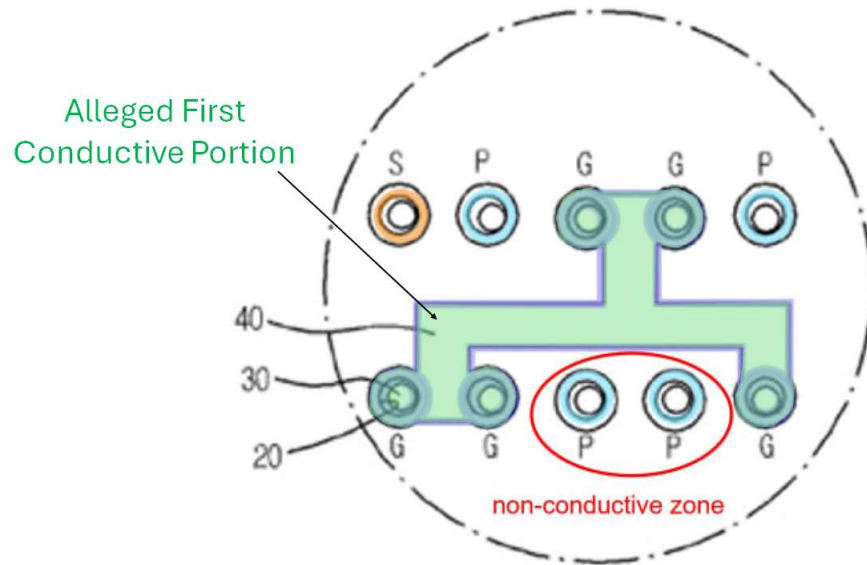
Digital-Vending Servs. Int'l, LLC v. Univ. of Phoenix, Inc., 672 F.3d 1270, 1275 (Fed. Cir. 2012) (A claim term “is presumed to have the same meaning throughout all of the claims.”). In its analysis of claim 1, Petitioner asserted that “[t]wo or more of the conductive layers (20) connected by some or all of the conductive trace (40) collectively constitute the claimed ‘first conductive portion.’” Pet., 31. Thus, according to the Petitioner, some or all of the **shaded portion** in Fig. 5a of *Kim*, excerpted and annotated below from the Petition, corresponds to the claimed “**first conductive portion**.” *Id.*, 34; Souri, ¶65.



Kim, Fig. 5a (excerpted from Pet., 34 and annotated).

In its analysis of claim 2, Petitioner again refers to Fig. 5a of *Kim* and asserts that “[o]n the bottom ‘row’ of test pins, for example, there is a gap in the conductive trace between the second and third ground testing pins, which ‘locally interrupts’

that first conductive portion.” Pet., 39. Petitioner’s annotated Fig. 5a is reproduced below with additional annotations. Sourì, ¶66.



Kim, Fig. 5a, excerpted from Pet., 34 and annotated.

As previously discussed, the phrase “the first conductive portion is locally interrupted by at least one nonconductive zone,” should be construed as “the first conductive portion encloses at least one non-conductive zone.” *See supra* Section III.A. The alleged first conductive portion identified by Petitioner (*see* annotated figure above) does not enclose the non-conductive zone identified by Petitioner. Sourì, ¶67. Quite the contrary, the non-conductive zone identified by Petitioner *separates and forms a gap* between adjacently located portions of the first conductive portion. Pet., 39 (admitting “there is a *gap* in the conductive trace between the second and third ground testing pins, which ‘locally interrupts’ that first conductive portion”).

At best, the *gap* identified by Petitioner is similar to the configurations of Figs. 3B and 3C of the '885 patent in which a non-conductive zone *separates* and forms a *gap* between adjacently located conductive portions. *See supra* Section III.A. Being *separated* by a *gap*, however, does not constitute being “*locally interrupted*.” *See id.* Because the alleged first conductive portion of *Kim* does not enclose Petitioner’s identified non-conductive portion, *Kim* fails to disclose “the first conductive portion is locally interrupted by at least one nonconductive zone.” *Souri*, ¶68. *Kim*, therefore, does not anticipate claim 2.

Obviousness: Petitioner’s backup obviousness position also fails. Petitioner first asserts that “locally interrupting” would have been a “routine design choice[.]” *Pet.*, 53. Petitioner’s “design choice” argument fails because neither Petitioner nor its expert explain why a skilled artisan would have been motivated and found it obvious to choose to locally interrupt the first conductive portion out of the myriad options for patterning allegedly available to the POSITA. *Id.*

Specifically, Petitioner asserts that “Kim explicitly discloses many different methods for forming desired shapes for the conductive layers and the conductive trace on the surface of the guide plate.” *Pet.*, 52-53. Further, Petitioner asserts that “[f]rom all these disclosures and the knowledge of a POSITA, a POSITA would understand that the conductive portion(s) formed on the guide plates could be in singular or multiple groups, and could be arranged, divided, and patterned in

whatever way necessary and best suited to the needs of a particular product or application.” *Id.*, 53. Thus, Petitioner admits that there are myriad ways of forming shapes of the conductive layers. *Id.* Petitioner’s analysis is impermissible hindsight because neither Petitioner nor its expert disclose why a skilled artisan would have been motivated and found it obvious to choose to locally interrupt the first conductive portion out of the myriad options for patterning allegedly available to the POSITA. *InTouch Techs., Inc. v. VGO Commc’ns, Inc.*, 751 F.3d 1327, 1351-52 (Fed. Cir. 2014) (finding that expert’s analysis was impermissible hindsight where she testified only that “one of ordinary skill in the art could combine these references, not that they would have been motivated to do so”).

Here, other than mentioning “routine design choice,” Petitioner provides no evidence, reasons, or bases for why a skilled artisan would have elected “locally interrupting” as the technique out of the plethora of other available techniques. This is insufficient to demonstrate obviousness. As the Board has recognized, under Federal Circuit law, “a statement that a proposed modification ‘is a design choice and is obvious . . . alone is not enough to explain’ a finding of obviousness” and “[t]he Board must offer a reason for why a person of ordinary skill in the art would have made the specific design choice’ at issue.” *FanDuel, Inc. v. Interactive Games LLC*, IPR2017-01491, Paper 38 at 42 (P.T.A.B. Nov. 20, 2018) (quoting *Cutsforth Inc. v. MotivePower, Inc.*, 636 F. App’x 575, 578 (Fed. Cir. 2016)); *see also*

Fanduel, Inc. v. Interactive Games LLC, 966 F.3d 1334, 1344 (Fed. Cir. 2020) (affirming Board’s finding of nonobviousness because “simply calling the addition of a look-up table ‘an obvious design choice’ did not fill that gap [in the reference]”); *Cutsforth*, 636 F. App’x at 578 (“Merely stating that a particular placement of an element is a design choice does not make it obvious.”).

Next, Petitioner asserts that “Kim discloses an example where some conductive material has been removed to ensure that ‘the testing pins 30 for signal or the testing pins 30 for power are insulated with the testing pins 30 for ground.’” Pet., 54. Petitioner further asserts that “locally interrupting the ‘first conductive portion’ would be advantageous to ensure that pins carrying different signals would be electrically isolated.” *Id.* Here again, Petitioner fails to explain why a skilled artisan would have elected to use this specific technique out of the plethora of other available techniques. Thus, Petitioner fails to demonstrate that claim 2 would have been obvious over *Kim*.

**B. *Kim* does not anticipate or render obvious claim 14
(Grounds 1, 2)**

Petitioner alleges that *Kim* anticipates (Ground 1) or renders obvious (Ground 2) claim 14. Pet., 48-49, 52-56. Petitioner’s arguments fail for the following reasons. *Souri*, ¶¶69-86.

Anticipation: Claim 14 depends from claim 1 and recites “at least one conductive track that electrically connects the first and second conductive portions including and electrically connecting the holes of the first and second groups of the guide holes to each other, the contact elements included in the second group being configured to carry the first type of signal.” Petitioner fails to show that *Kim* discloses these features for at least two reasons.

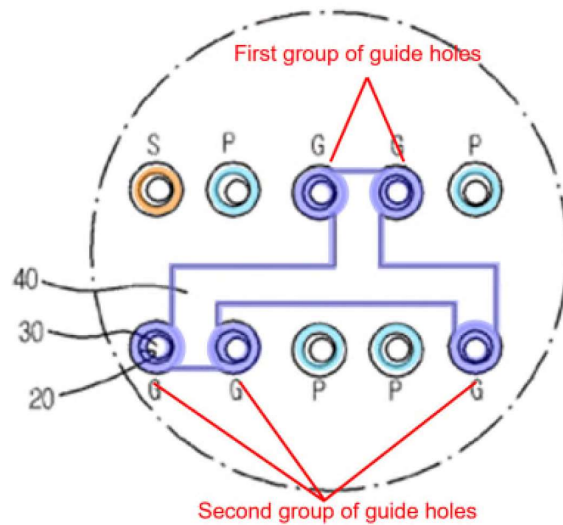
First, the components in *Kim* that Petitioner alleges disclose the first and second conductive portions do not satisfy all of the limitations of the “first conductive portion” and the “second conductive portion,” as recited in claim 14 and claim 1 from which it depends. Specifically, claim 1 recites:

- “a first conductive portion that includes *and electrically connects* a first group of guide *holes* of the plurality of guide holes, *to each other*.” ’885 patent, claim 1 (emphases added); and
- “a second conductive portion that includes *and electrically connects the* holes of a second group of the guide holes *to each other*.” *Id.* (emphases added).

By virtue of its dependency on claim 1, claim 14 therefore requires that the “first conductive portion” electrically connects a first group of guide holes to each other and that the “second conductive portion” electrically connects a second group of guide holes to each other. *See Hartness Int’l Inc. v. Simplimatic Eng’g Co.*, 819 F.2d

1100, 1108 (Fed. Cir. 1987) (dependent claim includes all limitations of its independent claim). *Souri*, ¶¶70-71.

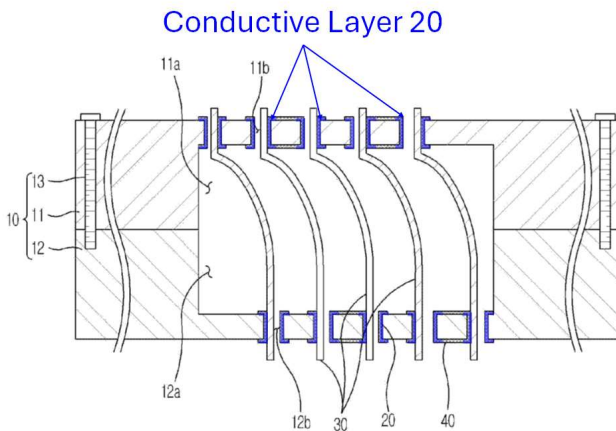
However, neither the first conductive portion nor the second conductive portion that Petitioner identifies in its analysis of claim 14 connect groups of guide holes to each other. *Souri*, ¶¶72-74. Specifically, Petitioner asserts: “The *conductive layers 20* at these ‘first and second group of guide holes’ *are* the claimed ‘first’ and ‘second conductive portions’ of claim 14. Pet., 48-49. Petitioner also asserts that “a ‘conductive track’ (conductive trace 40) electrically connects those ‘first’ and ‘second’ conductive portions.” *Id.*, 49. Thus, Petitioner identifies conductive layers 20, *alone*, as constituting the first conductive portion and the second conductive portion, and conductive trace 40 as corresponding to the claimed conductive track. But as explained below, the conductive layers 20 at each guide hole do not electrically connect one guide hole to another and thus cannot constitute either the “first conductive portion” or the “second conductive portion.” Petitioner’s annotated Fig. 5a from *Kim* is reproduced below.



Pet., 49 (annotating *Kim*, Fig. 5a).

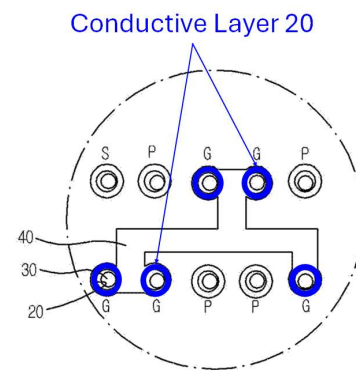
Kim discloses “[t]he conductive layer 20 serves to electrically connect the testing pin 30 and the conductive trace 40.” *Kim*, ¶[0038]. *Kim* also discloses “one side of the conductive trace 40 is connected to one side of the conductive layer 20 and the other side thereof is connected to one side of other conductive layer 20.” *Id.*, ¶[0043]. As Dr. Souri explains, in *Kim*, each guide hole labeled “G” in Fig. 5a of *Kim* has its own conductive layer 20 that is disposed within the guide hole and in the form of an annular ring around the guide hole. Souri, ¶¶75-76. The [conductive layer 20](#) at each guide hole is illustrated in annotated Figs. 2 and 5a of *Kim*, below.

FIG. 2



Kim, Fig. 2 (annotated)

FIG. 5a



Kim, Fig. 5a (annotated)

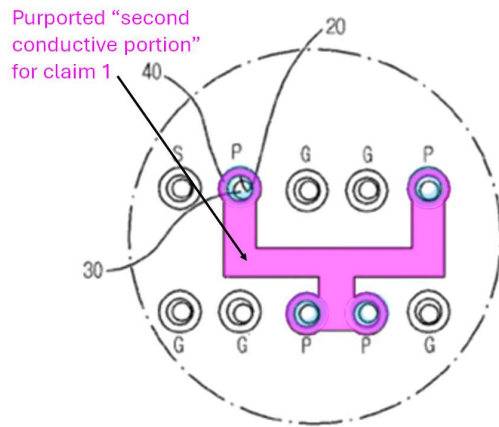
As seen in the cross-sectional view of Fig. 2 and plan view of Fig. 5a above, conductive layers 20 are isolated to each guide hole and do not electrically connect guide holes to each other. *Souri*, ¶76. Thus, conductive layers 20, *alone*, as identified by Petitioner cannot constitute either the “first conductive portion” or the “second conductive portion” of claims 1 and 14 because the conductive layer 20 at each guide hole does not electrically connect that guide hole to another guide hole. Petitioner has therefore failed to demonstrate that *Kim* discloses every element of claim 14 for at least this first reason. *Id.*, ¶¶76-77.

Second, Petitioner advances inconsistent positions regarding the first and second conductive portions recited in claims 1 and 14. When discussing independent claim 1, the Petition asserts that “[t]wo or more of the conductive layers (20) connected by *some or all* of the conductive trace (40) collectively constitute the claimed ‘first conductive portion.’” *Pet.*, 31 (emphasis added); *see also id.*, 32

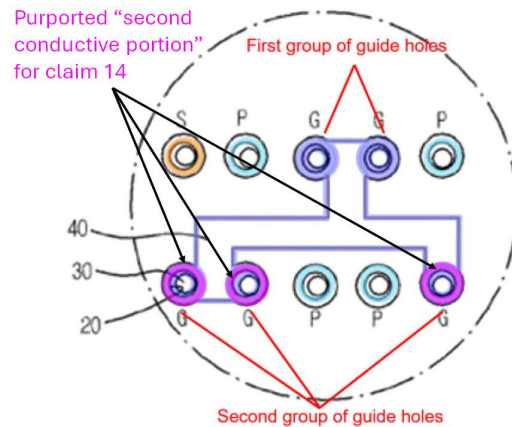
(referring to “conductive layers 20 and conductive trace 40 electrically connect[ing] a group of guide holes” as “this ‘first conductive portion’”). But then Petitioner changes tack when discussing claim 14, arguing that some conductive layers 20 *alone* constitute the claimed “first conductive portion.” *See id.*, 48-49. This is improper because for *Kim* to anticipate claim 14, which includes all the elements of claim 1, the same features of *Kim*’s device must correspond to the “first conductive portion” recited in both claims 1 and 14. *Souri*, ¶¶78-79; *see Hartness Int’l*, 819 F.2d at 1108.

Petitioner similarly takes inconsistent positions regarding the claimed “second conductive portion,” recited in claims 1 and 14. For claim 1, the Petition asserts that “Kim describes and illustrates in Fig. 5b that testing pins carrying power signals (represented by ‘P’) are electrically connected via the conductive layers (20) and conductive trace (40).” *Pet.*, 36. Then, when analyzing claim 14, the Petition again contradicts itself because it asserts that *some* conductive layers 20 *alone* constitute the claimed “second conductive portion.” *Pet.*, 48-49; *Souri*, ¶¶80-81. More importantly, when analyzing claim 1, Petitioner identifies the second conductive portion on a *lower* surface of *Kim*’s guide plate as the alleged second conductive portion. *Pet.*, 36. This is illustrated in Fig. 5b of *Kim* excerpted from the Petition below. But when analyzing claim 14, Petitioner identifies conductive layers 20 on the *upper* surface of *Kim*’s guide plate as the alleged second conductive portion. *Id.*,

48-49. This is illustrated in Fig. 5a of *Kim* excerpted from the Petition and further annotated below. *Souri*, ¶82.



Pet., 36 (claim 1) (annotated)



Pet., 49 (claim 14) (annotated)

This too is improper because for *Kim* to anticipate claim 14, which includes all the elements of claim 1, the same features of *Kim*'s device must correspond to the "second conductive portion" recited in both claims 1 and 14. *See Hartness Int'l*, 819 F.2d at 1108. Specifically, the second conductive portion cannot be on the lower surface of *Kim*'s guide plate 11 for claim 1, while simultaneously being on the upper surface of *Kim*'s guide plate 11 for claim 14. *Souri*, ¶83.

In its decision to institute trial, the Board noted that *Kim* contemplates "the potential for more than one electrically connected group on one surface of a guide plate." Paper 9, 26. The Board relied on *Kim*'s disclosure that "[T]he conductive layers 20, with which the testing pins 30 of transmitting the same signal are contacted, and the conductive traces for connecting them are set to a plurality of

groups and each group is formed at the upper surface and the lower surface of the upper plate 11 respectively.” *Id.* Petitioner did not cite to these portions of *Kim* in its anticipation analysis of claim 14. *See* Pet., 48-49. Nor did Petitioner proffer the rationale included in the Board’s decision. *See id.* “[T]he burden of persuasion is on the petitioner to prove ‘unpatentability by a preponderance of the evidence.’” *In re Magnum Oil Tools Int’l, Ltd.*, 829 F.3d 1364, 1375 (Fed. Cir. 2016) (quoting 35 U.S.C. § 316(e)). The Board may not *sua sponte* modify Petitioner’s inconsistent theories when assessing the patentability of the challenged claims. *Id.* at 1381 (the Board’s “authority is not so broad that it allows the [Board] to raise, address, and decide unpatentability theories never presented by the petitioner and not supported by record evidence.”). It would also be improper for Petitioner to advance this rationale in its reply. *See Wasica Fin. GmbH v. Cont’l Auto. Sys., Inc.*, 853 F.3d 1272, 1286-87 (Fed. Cir. 2017) (introducing reply arguments that “amount to an entirely new theory of [unpatentability] . . . is foreclosed by statute, [Federal Circuit] precedent, and Board guidelines”); *accord* Consolidated Trial Practice Guide at 73 (Nov. 2019) (“Petitioner may not submit new evidence or argument in reply that it could have presented earlier, e.g., to make out a *prima facie* case of unpatentability.”).

Furthermore, one of ordinary skill reading the portion of *Kim* relied on by the Board would understand it to disclose that there may be more than one group of

testing pins 30 on the upper and lower surface of plate 11, and the testing pins 30 in each of those groups may be connected to each other by a conductive trace 40. Souri, ¶¶84-85. As Dr. Souri explains, each of those groups would be similar to the group of testing pins 30 connected to each other shown in Fig. 5a of *Kim*. *Id.*, ¶85. Nothing in *Kim*, however, discloses that the two groups are themselves connected to each other by a conductive trace 40 or in any other manner. *Id.*

Thus, Petitioner fails to demonstrate that *Kim* discloses every element of claim 14 and therefore fails to show that *Kim* anticipates claim 14. Souri, ¶86.

Obviousness: Petitioner’s backup obviousness analysis for claim 14 also fails. Petitioner merely asserts that “the ‘conductive track’ that connects two conductive portions in claim[] . . . 14, to the extent not disclosed in *Kim*, likewise is at most an example of the type of specific pattern of conductive material that would be an obvious design choice to a POSITA implementing *Kim*’s disclosures.” Pet., 56. Petitioner’s conclusory design choice analysis is even more deficient for claim 14 than it is for claim 2. As discussed above, merely calling something a “design choice” is insufficient to show that claimed features would have been obvious. *FanDuel*, Paper 38 at 42; *Cutsforth*, 636 F. App’x at 578. Accordingly, Petitioner fails to demonstrate that claim 14 is obvious over *Kim*.

C. *Kim* does not render obvious claim 7 (Ground 2)

Claim 7 recites “the at least one guide includes at least one third conductive portion that includes and electrically connects a third group of the guide holes to each other and house third contact elements configured to carry input/output signals.” Petitioner fails to identify any teaching in *Kim* that discloses or suggests electrically connecting pins that carry input/output signals. Pet., 57. Instead, Petitioner misreads both *Kim*’s disclosure and Patent Owner’s statements made before the Japanese Patent Office (“JPO”).

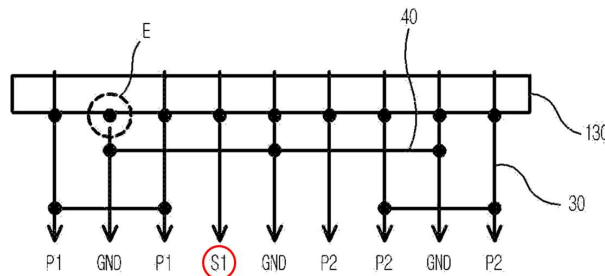
Specifically, Petitioner cites ¶¶[0019], [0025], [0032], [0042], [0044], [0045] of *Kim* as allegedly disclosing that ““testing pins of transmitting the same signal’ may be electrically connected to each other, *without limiting the types of signals.*” and that “Technoprobe also acknowledged *this* to the JPO.” Pet., 57-58 (emphasis added) (citing Ex. 1018, 20). Both assertions are incorrect. *Souri*, ¶¶87-106.

As a preliminary matter, the portions of *Kim* that Petitioner cites never disclose or suggest connecting pins carrying *input/output signals* to each other. Instead, they only disclose connecting pins carrying *ground* signals to each other. For example, while *Kim* generically states that “the conductive trace is electrically connected between the conductive layers with which the testing pins of transmitting the same signal are contacted,” *Kim*, ¶[0019], the very next paragraph explains that “the conductive trace is electrically connected between the conductive layers with

which the testing pins for *ground* are contacted,” *id.*, ¶[0020] (emphasis added). Likewise, in the subsection titled “1. Connection Between the Conductive Layers with which the Testing Pin of Transmitting the Same Signal is Contacted” (*Kim*, ¶[0042], cited at Pet., 58), *Kim* discloses “the plurality of the conductive layers 20, with which the testing pin for *ground* is contacted, can be connected to each other.” *Id.*, ¶[0044] (emphasis added). And ¶[0045] of *Kim* refers back to ¶[0044], stating “[a]s described above,” indicating that “the plurality of testing pin 30 of transmitting the same signal” refer to the testing pins for ground. *Souri*, ¶¶89-90. A skilled artisan therefore would have understood these portions of *Kim* to disclose that testing pins carrying the same type of signal, such as a ground signal, can be connected to each other. *Id.*, ¶90. But this leaves unresolved the question of whether *Kim* discloses connecting input/output pins to one another.

However, *Kim*’s discussion of input/output pins resolves this question and demonstrates that they are *not* connected with each other. For example, Fig. 3 of *Kim*, (referred to in *Kim*, ¶¶[0025], [0032] and cited by Petitioner) includes a single pin labeled “S1” that is not depicted as being connected to any other pin. *Souri*, ¶91.

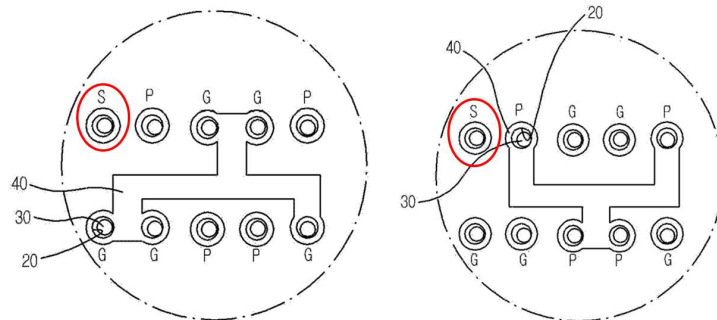
FIG. 3



Kim, Fig. 3 (annotated). Likewise, the pins labeled “S” in Figs. 5a and 5b of *Kim*, which Petitioner alleges refer to a “signal,” are not connected to any other pin. Pet., 57.

FIG. 5a

FIG. 5b



Kim, Figs. 5a and 5b (annotated); Sourì, ¶92. Thus, while *Kim* discloses connecting testing pins carrying a *ground* signal, nothing in *Kim* discloses or suggests connecting testing pins carrying *input/output* signals. Instead, Petitioner’s cited portions of *Kim* confirm that the input/output signals are not connected to each other, as discussed above. Sourì, ¶93.

And while Petitioner relies on *Kim*'s generic disclosure that "'testing pins of transmitting the *same* signal' may be electrically connected to each other," Pet., 57 (quoting *Kim*, ¶[0019]) (emphasis added), a POSITA would have understood that the signals carried by any two input/output pins of *Kim* are unlikely to be the "same" signal. Souri, ¶94. Specifically, the purpose of *Kim*'s probe head is to test the functionality of a chip. *Kim*, ¶[0006]; Souri, ¶95. As Petitioner's expert explains: "Through 'instructions' from the test program, the tester stimulates the input signal I/Os and records the response from the output I/Os (bi-directional I/Os perform either function as required by the test)." Ex. 1003, ¶80. A POSITA would have understood that in such a testing scenario, the different input/output pins in *Kim*'s semiconductor testing apparatus would carry different signals, depending on the test program. Souri, ¶95. In other words, two or more pins associated with input/output signals are likely to carry different signals when simulated with a test program. *Id.*

This is different from pins associated with power and ground that typically carry the same power and ground signals, respectively. Souri, ¶96. Thus, a POSITA would not have understood *Kim*'s statement in ¶[0019] as disclosing or suggesting connecting pins carrying input/output signals. Souri, ¶96. Petitioner's expert agrees, stating "[t]ypically, signal I/Os operate individually, so two or more are not connected together." Ex. 1003, ¶80.

Petitioner's expert goes on to say "however, there may be instances otherwise." Ex. 1003, ¶80. But, Petitioner's expert fails to provide any evidence of instances in which "signal I/Os" would be connected to each other. The Board should disregard such unsupported expert testimony. *See* 37 C.F.R. § 42.65(a) ("Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight."); *Upjohn Co. v. Mova Pharm. Corp.*, 225 F.3d 1306, 1311 (Fed. Cir. 2000) ("Lack of factual support for expert opinion to factual determinations, however, may render the testimony of little probative value in a validity determination.").

Petitioner also asserts that "at minimum it would be obvious to a POSITA that Kim's guide holes housing testing pins carrying input/output signals also *could* be electrically connected via a third conductive portion, forming a third group of guide holes, in the same way as the first and second groups of guide holes are electrically connected." Pet., 58 (emphasis added). Petitioner's conclusory statement fails to explain why a skilled artisan *would* have electrically connected testing pins carrying input/output signals. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.").

Petitioner's expert asserts that "[a] POSITA would have had a reason to electrically connect these signal testing pins in Kim to improve performance in fulfilling certain testing requirements, such as with loop-back testing." Ex. 1003, ¶265. Here again, Petitioner's expert fails to provide any evidence to support this conclusion. Nor does Petitioner's expert explain how connecting signal pins would improve the performance as claimed. *Souri*, ¶97. The Board should disregard such unsupported expert testimony. *See* 37 C.F.R. § 42.65(a); *Upjohn*, 225 F.3d at 1311.

Furthermore, and contrary to Petitioner's assertions, in the JPO proceedings, Patent Owner merely acknowledged that *Kim* discloses test pins for signal, ground, or power. Ex. 1018, 20 ("The test pins are disclosed to be for signal, ground, or power."). However, Patent Owner did not admit that *Kim* discloses or suggests connecting pins carrying input/output signals. *Id.*

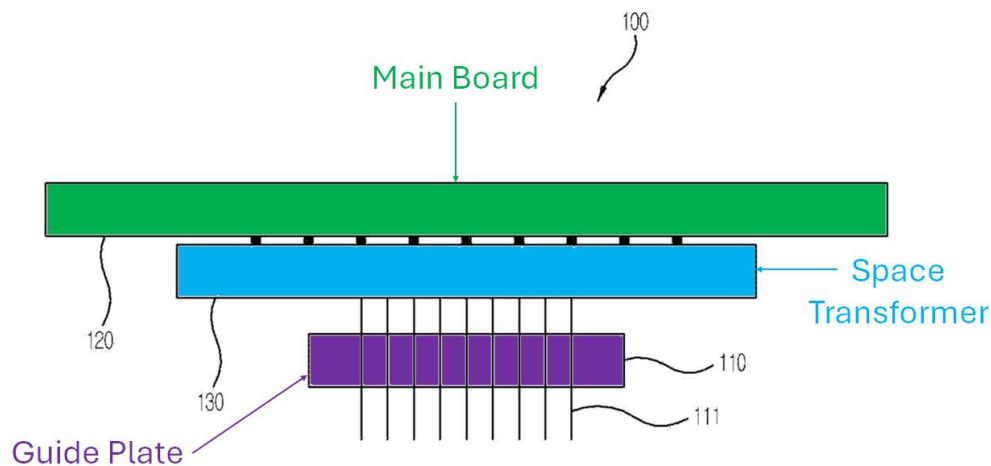
Petitioner next asserts that "it would be obvious" to electrically connect *Kim*'s pins carrying input/output signals and lists purported benefits of doing so. Pet., 58. Specifically, Petitioner asserts that "[a] POSITA would have been motivated to electrically connect these signal testing pins in Kim to achieve the benefits described in Kim, including that 'the signal transduction route is minimized through the testing pin and the impedance is decreased, thereby remarkably improving the high frequency performance.'" Pet., 58 (citing Ex. 1003 ¶¶264-65). Petitioner's rationale

is flawed because the purported benefits Petitioner relies upon are entirely unrelated to electrically connecting input/output signal pins, as discussed below. *Souri*, ¶¶98.

As illustrated in Fig. 1 of *Kim*, excerpted below, a conventional probe card includes a guide plate with testing pins contacting a chip, a main board separated from the guide plate, and a space transformer that helps to increase the narrow pitch of the pins on the guide plate to a wide pitch of the connections on the main board. *Kim*, ¶[0010].

FIG. 1

Prior Art



Kim, Fig. 1 (annotated). In conventional configurations, signals must travel from the main board 120, through the space transformer 130, and through the pins 111 to the chip under test, located at the bottom of the pins 111. *Souri*, ¶¶99-100. Because the length of this path through the wiring in space transformer 130 and through pins 111 can be long, the long path introduces a high impedance, which in turn affects high

frequency performance. *Id.*, ¶¶100-101. *Kim* discloses directly connecting conductive trace 40 to main board 120 through an external wire (J in *Kim*, Fig. 6), bypassing the long length of the wiring in space transformer 120 and the length of pins 111. *Id.*, ¶102. Because the signals no longer have to travel through a long electrical path, but instead travel directly through the wire J, the impedance for signal propagation is low and this consequently improves high frequency performance. *Id.* This is exactly what *Kim* discloses in the portions cited by Petitioner.

For example, *Kim* states: “Another object of the invention is to provide a semiconductor testing apparatus in that *a signal transduction length becomes short and an impedance is decreased*, so that it can remarkably improve the high frequency performance.” *Kim*, ¶[0016] (emphasis). *Kim* also discloses “since the conductive trace 40 according to one embodiment of the present invention *can be directly connected to the main board without the separate space transformer* on the external area W, which is deviated from the testing area T, it can remarkably improve the workability thereof.” *Kim*, ¶[0048] (emphasis added). *Kim* further explains that “since the signal transduction length becomes short and the impedance is decreased, it can remarkably improve the high frequency performance.” *Id.* Notably, these paragraphs disclose nothing about reduction in impedance or improved high frequency performance *due to electrical connection of input/output signals*. Souri, ¶103.

Kim also discloses “after the testing pins of transmitting the same signal are electrically connected to each other through a lower surface of the lower plate of the guide plate, *the conductive trace 40 is electrically connected to the main board through the external area deviated from the testing area, so that the signal transduction route is minimized through the testing pin and the impedance is decreased*, thereby remarkably improving the high frequency performance.” *Kim*, ¶[0064]. As Dr. Souri explains, although *Kim* mentions electrically connecting testing pins transmitting the same signal, here again, *Kim* discloses that impedance is reduced and high frequency performance improves because connection of the conductive portions to the main board bypasses the space transformer and the pins passing through the guide plate. Souri, ¶104. Furthermore, high frequency performance is improved because the signals can travel through the wire J. *Id.* Moreover, contrary to Petitioner’s assertions, the benefits of a minimized signal transduction route, reduced impedance, and improved frequency performance are a result of bypassing the pins and the space transformer, not a result of electrically connecting pins carrying input/output signals. *Id.*, ¶105. *Kim* does not disclose any benefits of connecting input/output signal pins. *Id.*

Thus, Petitioner fails to demonstrate that *Kim* discloses connecting testing pins carrying input/output signals. Furthermore, Petitioner fails to show that a skilled artisan would have been motivated to connect testing pins carrying input/output

signals and, therefore, fails to establish that the skilled artisan would have found claim 7 obvious in view of *Kim*. Souri, ¶106.

D. The combination of *Kim* and *Schmid* does not render obvious claim 18 (Ground 3)

Claim 18 includes recitations similar to those of claim 7. As discussed above, *Kim* fails to disclose or suggest the features of claim 7 also included in claim 18. Petitioner does not rely on *Schmid* for the recitations of claims 7 or 18. Pet., 57-58, 59-67. Indeed, *Schmid* does not disclose or suggest “the at least one guide includes at least one third conductive portion that includes and electrically connects holes of a third group of the guide holes to each other and house third contact elements, of the plurality of contact elements, configured to carry input/output signals between the device under test and a test equipment,” as recited in claim 18. Accordingly, for reasons similar to those discussed above for claim 7, Petitioner fails to demonstrate that claim 18 is obvious over the combination of *Kim* and *Schmid*. Souri, ¶107.

E. The combination of *Kim* and *Schmid* does not render obvious claims 6 and 23 (Ground 3)

Claim 6 recites “the first and second conductive portions being formed on a same face of one of the upper, intermediate and lower guides and being physically and electrically separated from each other by at least one non-conductive zone.” Claim 23 includes similar limitations. Petitioner relies only on *Kim* as allegedly teaching this limitation. Petitioner fails to demonstrate that these claims are

unpatentable because *Kim* does not disclose or suggest these elements of claims 6 and 23. *Souri*, ¶¶108-125.

Quite the contrary, *Kim* discourages forming conductive portions carrying power and ground signals, respectively, on a same face of a guide plate. *Souri*, ¶109. For example, *Kim* discloses forming conductive traces connecting testing pins that carry ground signals on a different surface of the guide plate from conductive traces connecting testing pins carrying other types of signals:

For example, the plurality of the conductive layers 20, with which the testing pins 30 of transmitting the same signal are contacted, and the conductive traces 40 for connecting them are formed at the upper surface of the upper plate 11 as shown in FIG. 5a and the plurality of the conductive layers 20, with which the testing pins 30 for ground are contacted, and the conductive traces 40 for connecting them are formed at the lower surface of the upper plate 11 as shown in FIG. 5b, *so that the testing pins 30 of transmitting the same signal can be easily connected without interfering with the testing pin 30 of transmitting the other signal.*

Kim, ¶[0051] (emphasis added); *Souri*, ¶109. *Kim* stresses the importance of this configuration by explaining that doing so prevents interference between the pins carrying the different types of signals. *Id.*, ¶110. As Dr. *Souri* explains, a POSITA reading *Kim* would not have found it obvious to locate the first conductive portion

carrying ground signals and the second conductive portion carrying power signals on the same face of a guide plate. *Id.*

Petitioner fails to identify any teaching in *Kim* that discloses placing conductive portions carrying power and ground signals on the same face of a guide plate. Pet., 65-66. Instead, Petitioner misreads *Kim*'s disclosure by citing snippets from ¶¶[0050] and [0052] of *Kim* and ¶[0045] of Ex. 1005,¹ and misinterpreting those snippets to argue that *Kim* discloses forming conductive portions carrying power and ground signals on the same face of a guide plate. Souri, ¶111.

As Dr. Souri explains, ¶¶[0050] and [0052] of *Kim* and corresponding ¶¶[0043] and [0045] of Ex. 1005, when interpreted as a whole, do not disclose or suggest forming conductive portions carrying power and ground signals on the same face of a guide plate. Souri, ¶112. Each of these portions of *Kim* and Ex. 1005 is addressed below. *Id.*, ¶113.

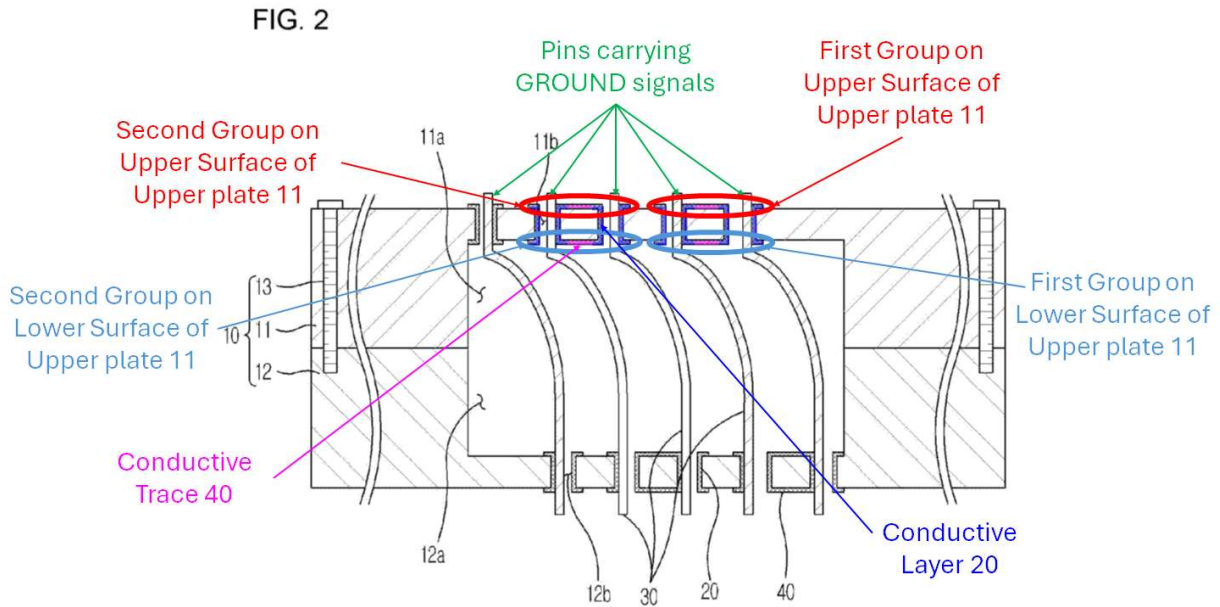
¹ Ex. 1005 is Petitioner's English language translation of Korean Patent Application No. 10-2014-0004576, to which *Kim* claims priority.

Paragraph [0050] of *Kim* and paragraph [0043] of Ex. 1005 state:

<i>Kim, ¶[0050] (emphasis added)</i>	<i>Ex. 1005, ¶[0043] (emphasis added)</i>
In the meantime, in one embodiment of the present invention, <i>the plurality of the conductive layers 20, with which the testing pins 30 of transmitting the same signal are contacted, and the conductive traces for connecting them are set to a plurality of groups</i> and each group is formed at the upper surface and the lower surface of the upper plate 11 respectively, so that the testing pins 30 of transmitting the same signal in the narrow testing area can be easily connected.	In one embodiment of the present invention, <i>the test pins (39) transmitting identical signals can be conveniently connected in a confined testing area by grouping a plurality of conductive layers (20) in contact with the test pins (30) transmitting identical signals, along with the trace connecting such conductive layers, and forming each group on the upper surface and the lower surface of the upper plate (11), respectively.</i>

A POSITA would have understood the italicized portions of these paragraphs as disclosing that conductive layers 20, testing pins 30 carrying the same or identical signal in contact with those conductive layers 20, and conductive traces connecting them could be divided into a plurality of groups. *Souri, ¶114*. Thus, for example, testing pins 30 carrying identical signals (e.g., ground signals) could be divided into a plurality of groups. *Id.* Further, in each such group, conductive traces 40 would connect the conductive layers 20 in contact with the testing pins 30 in that group. *Id.* Moreover, a person of ordinary skill would have understood from these paragraphs that each such group carrying the same signal (e.g., ground signal) could be formed on both the upper surface and on the lower surface of upper plate 11. *Id.* *Kim* illustrates precisely this configuration, including in annotated Fig. 2 below, where two groups of pins are formed on the upper surface of upper plate 11 and also on the

lower surface of upper plate 11. *Id.*, ¶115. Furthermore, the pins in each of the two groups are connected to each other via **conductive traces 40** and **conductive layers 20**.



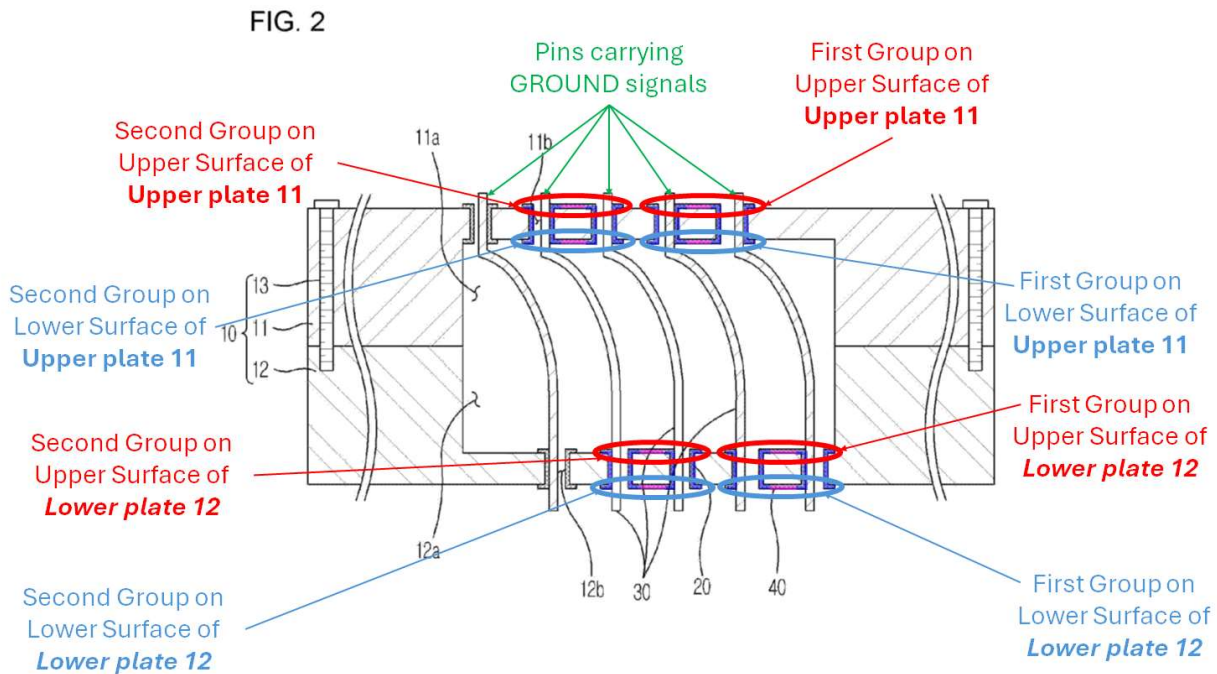
Kim, Fig. 2 (annotated).

Next, referring to those same groups, paragraph [0052] of *Kim* and corresponding paragraph [0045] of Ex. 1005 disclose:

<i>Kim</i>, ¶[0052] (emphasis added)	Ex. 1005, ¶[0045] (emphasis added)
Also, in the drawings, each <i>group</i> is formed at only the upper surface and the lower surface of the upper plate 11. However, the present invention is limited to the position of the groups. That is, each <i>group</i> can be formed at the upper surface and the lower surface of both upper and lower plates 11 and 12 according to the number of the <i>groups</i> . Also, at least one electrical connecting <i>group</i> can be formed on one surface thereof.	Furthermore, in one example, it has been described that each <i>group</i> is distinguished and formed only on the upper surface and lower surface of the upper plate (11). However, the present invention is not limited to forming each <i>group</i> only on the upper surface and lower surface of the upper plate (11). Depending on the number of <i>groups</i> , it is possible to form more than one electrically connected <i>group</i> on a single surface, not to mention using both the upper surface and lower surface of the upper plate (11), as well as the upper surface and lower surface of the lower plate (12).

A POSITA would have understood these paragraphs as disclosing that each of the plurality of groups (e.g., First Group and Second Group illustrated above) could be formed on the upper and lower surfaces, respectively, of upper plate 11, and also on upper and lower surfaces, respectively, of lower plate 12. *Souri*, ¶¶116-117. And as explained above, the First Group and Second Group both carry the same or identical signal (e.g., ground signal). *Id.*, ¶117. *Kim* also illustrates this configuration in annotated Fig. 2 of *Kim*, below, where the first and second groups of pins are formed on the upper surface of upper plate 11 and also on the lower surface of upper plate 11. *Id.*, ¶¶117-118. And those same two groups are also

formed on the upper and lower surfaces of lower plate 12. Furthermore, the pins in each of the groups are connected to each other via **conductive traces 40** and **conductive layers 20**. *Id.*



Kim, Fig. 2 (annotated).

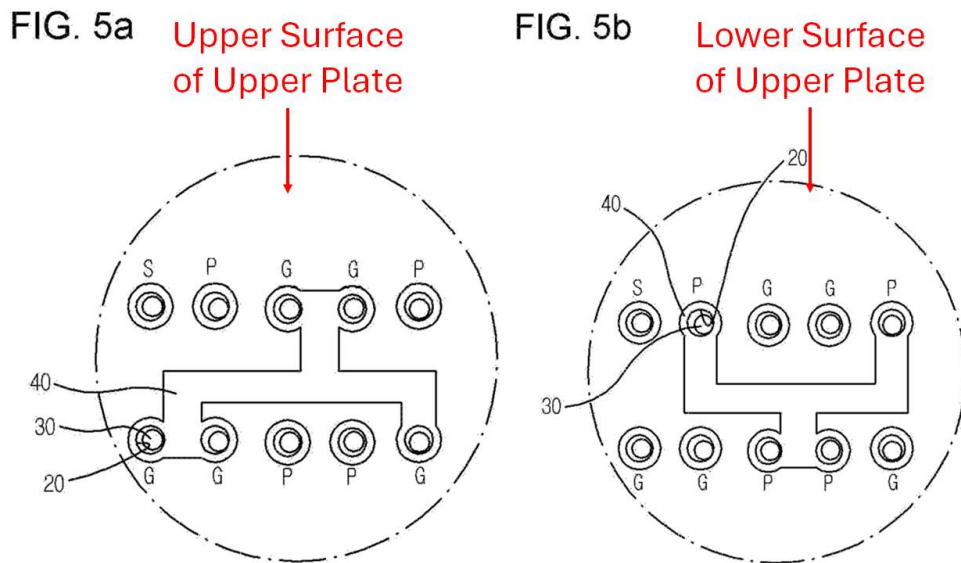
Ex. 1005 also states: “Depending on the number of groups, it is possible to form more than one electrically connected group on a single surface, not to mention using both the upper surface and lower surface of the upper plate (11), as well as the upper surface and lower surface of the lower plate (12).” Ex. 1005, ¶[0045] (partially quoted at Pet., 66). A POSITA would have understood this sentence to mean that if there were too many groups, both surfaces of one or both of upper and lower plates 11 and 12 could be used to accommodate the groups. *Souri*, ¶119. Conversely, if

there were fewer groups, all of the groups could be accommodated on just the upper surface or just the lower surface of only the upper plate 11 or only the lower plate 12. *Id.* No portion of *Kim* or Ex. 1005, however, discloses or suggests forming conductive portions connecting groups of pins carrying ground signals and conductive portions connecting groups of pins carrying power signals on the same surface of either the upper or lower plates 11 and 12 of *Kim*. *Souri*, ¶120. This makes sense because, as discussed, *Kim* expressly discloses that conductive portions connecting groups of pins carrying ground signals and conductive portions connecting groups of pins carrying power signals should be placed on different surfaces to prevent interference. *Id.*; *Kim*, ¶[0051]; Ex. 1005, ¶[0044].

Petitioner asserts that “A POSITA would have understood that Kim’s system could be implemented with both first and second (power and ground) conductive materials on one side of a guide plate, and would have had reason to do so, for instance, when multiple ground and/or power groups are present or to easily follow the layout of the device under test.” Pet., 66. Petitioner cites ¶¶309-311 of its expert’s declaration as support for this conclusory assertion. But Petitioner’s expert merely repeats this conclusory assertion without providing any evidence to support it. Ex. 1003, ¶309. The Board should disregard such unsupported expert testimony. *See* 37 C.F.R. § 42.65(a); *Upjohn*, 225 F.3d at 1311.

Petitioner's expert also improperly relies on the advantages of Patent Owner's own invention, as discussed during prosecution of European Patent Application No. EP3555638, to provide a purported motivation to form power and ground planes on the same face of a guide plate. Ex. 1003, ¶310. The application that issued as the '885 patent and EP3555638 are counterpart applications, include identical disclosures, and derive from International Application No. PCT/EP2017/082180. During prosecution of the European application, Patent Owner explained that "the claimed configuration is particularly advantageous and leads to many technical benefits." Ex. 1016, 455. Patent Owner further explained: "More in particular, the possibility of forming different conductive portions on a same face of the guide allows to easily arrange said conductive portions in the testing head, following the layout of the device under test (DUT)." *Id.* Thus, Patent Owner described the benefits of its own invention, which is also disclosed and claimed in the '885 patent. Accordingly, the knowledge and motivation of a POSITA proffered by Petitioner's expert are based on Patent Owner's own invention. This is improper. *Otsuka Pharm. Co., Ltd. v. Sandoz, Inc.*, 678 F.3d 1280, 1296 (Fed. Cir. 2012) ("The inventor's own path itself never leads to a conclusion of obviousness; that is hindsight."); *Life Techs., Inc. v. Clontech Labs., Inc.*, 224 F.3d 1320, 1325 (Fed. Cir. 2000) ("[T]he path that leads an inventor to the invention is expressly made irrelevant to patentability by statute.")

Petitioner's expert also points to Figs. 5a and 5b of *Kim*. Ex. 1003, ¶311. But Figs. 5a and 5b show the first conductive portion and the second conductive portion formed on different surfaces of upper plate 11. *Kim*, ¶¶[0051], [0027] (“Fig. 5a is a drawing showing an *upper surface* of upper plate,” emphasis added), [0028] (“Fig. 5b is a drawing showing a *lower surface* of an upper plate,” emphasis added); Pet. 31-37. They do not show the first conductive portion and the second conductive portion being formed on the same face of upper plate 11. *Souri*, ¶¶121-122.



Kim, Figs. 5a and 5b (annotated).

Petitioner's expert also cites to ¶[0062] of *Kim*. Ex. 1003, ¶311. There, *Kim* describes an embodiment in which “the conductive materials are deposited on the entire surface of the guide plate 10 and then, the conductive materials are selectively removed from the surface of the guide plate 10 through the machining.” *Kim*, ¶[0061]. *Kim* explains “the conductive materials formed at the corner of the guide

plate corresponding to the guide hole, into which the testing pins 30 except for the testing pins 30 for ground are inserted, that is the entrance of the guide hole 11a is removed through the counter sink or the counter bore C.” *Kim*, ¶[0062]. Thus, here, *Kim* discloses forming one conductive portion connecting pins other than ground pins using a conducting layer. Nothing in this description discloses or suggests forming conductive portions connecting groups of pins carrying ground signals and conductive portions connecting groups of pins carrying power signals on the same surface of either the upper or lower plates 11 and 12 of *Kim*. *Souri*, ¶¶123-124.

The Petition also asserts that “a POSITA would have understood that the conductive portions taught in *Kim* could be arranged and patterned in various ways, including having both the first (ground) and second (power) portions formed on the same face of one guide.” *Pet.*, 65. Petitioner again cites to ¶¶302-305 of its expert’s testimony as support for this conclusory assertion. Petitioner’s expert again repeats the same conclusion with no supporting evidence. The Board should disregard such conclusory expert testimony. 37 C.F.R. § 42.65(a); *Upjohn*, 225 F.3d at 1311.

Thus, Petitioner fails to demonstrate that *Kim* discloses or suggests “the first and second conductive portions being formed on a same face of one of the upper, intermediate and lower guides and being physically and electrically separated from each other by at least one non-conductive zone,” as recited in claims 6 and 23. *Kim* teaches exactly the opposite. *See Kim*, ¶[0051]. Petitioner does not rely on *Schmid*

for these features. Pet., 65-66. Therefore, the combination of *Kim* and *Schmid* does not render obvious claims 6 and 23. Souri, ¶125.

F. The combination of *Kim* and *Schmid* does not render obvious claims 5, 16, and 17 (Ground 3)

Claim 5 recites “the first and second conductive portions being formed on respective faces of the upper, intermediate *and* lower guides” (emphasis added). Claim 16 (and claim 17 which depends therefrom) includes similar recitations. Thus, claims 5, 16, and 17 require the first conductive portion and the second conductive portion to be formed on each of the upper guide, intermediate guide, and the lower guide. Petitioner fails to show that the combination of *Kim* and *Schmid* render obvious at least these features, because Petitioner fails to explain why a POSITA would have been motivated or found it obvious to form the first and second conductive portions on each one of the lower guide, the intermediate guide, and the upper guide. Souri, ¶¶126-131.

But Petitioner asserts “Kim teaches that metalized conductive patterns *can be* formed on the upper or lower plates.” Pet., 61 (emphasis added). Therefore, Petitioner concludes that “[a] POSITA thus would have understood that Kim’s addition of conductive electrical connections to guide plates *could be applied* in a three-guide system like Schmid.” *Id.* (emphasis added). Although the first and second conductive portions *could be* formed on the three guide plates, that alone is

insufficient to demonstrate obviousness of the claimed features. *See Belden*, 805 F.3d at 1073. Petitioner, however, fails to explain why a POSITA *would have formed* the first conductive portion and the second conductive portion on each of the three guide plates as required by claims 5 and 16. Pet., 61-66; Souri, ¶127. Petitioner also fails to explain what benefits if any would have been achieved by forming the first conductive portion and the second conductive portion on each of the three guide plates as required by claims 5 and 16. Pet., 61-66; Souri, ¶127.

As Dr. Souri explains, coating electrically conductive metal on a surface of a guide plate and performing lithography to pattern that conductive material are expensive and time-consuming processes. Souri, ¶128. For example, coating the electrically conductive metal requires one or more of an electro-chemical deposition process, a sputtering process, or some other type of coating process. *Id.* Furthermore, the time required to coat the surface of the guide plate with the metal layer would add to the time required to manufacture the guide plate. *Id.* Performing lithography on the coated material to obtain a desired pattern of conductive portions typically requires a mask for defining the desired pattern. *Id.*, ¶129. Forming the desired pattern typically requires etching of portions of the metal based on the pattern defined by the mask. *Id.* Etching processes in turn may typically involve a chemical etching process, which would further add time to the manufacturing process. *Id.* In addition to the increased manufacturing time, the need for a mask, and materials for

coating and selectively etching the electrically conductive metal would further increase manufacturing costs. *Id.*, ¶130. A POSITA would not have been motivated to incur additional manufacturing costs and/or increase manufacturing time by unnecessarily adding conductive portions on every guide plate. *Id.*

Thus, Petitioner fails to show that the combination of *Kim* and *Schmid* discloses or suggests all the elements of claims 5 and 16. Claim 17 depends from claim 16 and is, therefore, not obvious over the combination of *Kim* and *Schmid* for reasons similar to those discussed above for claim 16. *Souri*, ¶131.

G. The combination of *Kim* and *Fan* does not render obvious claim 3 (Ground 4)

Claim 3 recites “the at least one guide comprises at least one coating dielectric portion that covers the at least one non-conductive zone.” Petitioner relies solely on *Fan* as teaching this limitation. *Pet.*, 68-70. Petitioner is wrong for the reasons discussed below. Moreover, Petitioner and its expert fail to demonstrate that a POSITA would have found it obvious to combine the teachings of *Kim* and *Fan*. *Souri*, ¶¶132-145.

Petitioner asserts that *Fan* discloses that its “guide plate [100] ‘can be made of non-conductive materials’” (*Pet.*, 68), and that “insulating material can be coated on the [plate]” (*Pet.*, 69), and thus concludes that “*Fan* teaches, or at least renders obvious, a testing head that “comprises at least one coating dielectric portion

[insulating layer 600] that covers the at least one non-conductive zone [a portion of guide 100 made of a non-conductive material]” (*id.*). Petitioner misreads *Fan*’s disclosure. *Souri*, ¶133.

Nothing in *Fan* discloses or suggests coating a portion of a guide 100 made with *non-conductive* material with insulating layer 600. Specifically, *Fan* discloses two embodiments, a first embodiment in which the guide plate is made of non-conductive material, and a second embodiment in which the guide plate is made of conductive material. *Souri*, ¶¶134-135. Neither embodiment discloses the limitation of claim 3.

In *Fan*’s first embodiment, the probe head “includes the plate 100, a probe 200, and at least one composite coating layer 300.” *Fan*, 3:5-7. *Fan* discloses that “composite coating layer 300 includes a metal layer 310 and a plurality of lubricating particles 320, which may be made of metal-polymer.” *Id.*, 3:13-15. *Fan* explains that “metal layer 310 is disposed in the through hole 110 of the plate 100 and between the plate 100 and the probe 200.” *Id.*, 3:17-19. Further, *Fan* discloses “the probe head may further include at least one base layer 400 disposed between the metal layer 310 and the plate 100.” *Id.*, 3:64-66; *Souri*, ¶135. Annotated Fig. 2 of *Fan*, illustrating this embodiment, is excerpted below:

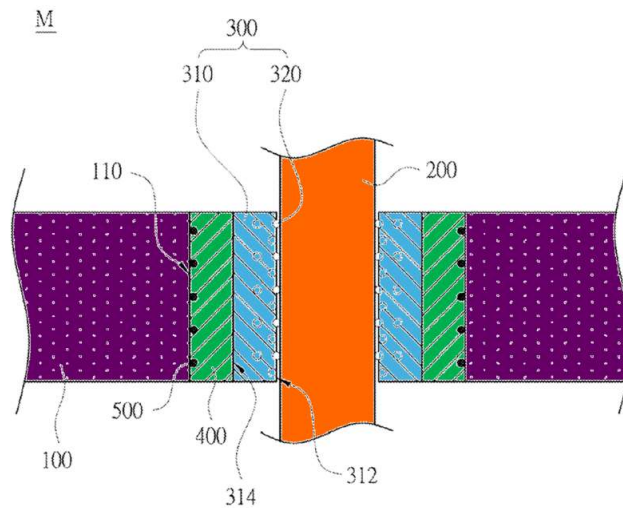


FIG. 2

Fan, Fig. 2 (annotated).

Fan explains that “[i]n this embodiment, the materials of the **base layer 400** and the **metal layer 310** may be the same.” *Id.*, 4:7-8 (emphasis added); Souri, ¶135. Thus, for its first embodiment, *Fan* expressly discloses that **base layer 400** and **metal layer 310** are both metallic. *Id.*, ¶136. With regard to the **plate 100**, *Fan* discloses that the “**plate 100** can be made of non-conductive materials, semiconductor materials, or conductive materials” but that “[i]n this embodiment, the **plate 100** may be made of *ceramics*.” *Fan*, 3:41-42, 3:44-45 (emphasis added).

As Dr. Souri explains, if plate 100 were made of semiconductor or conductive materials, probe 200 would be electrically connected to plate 100 through metallic layers 310 and 400. Souri, ¶137. This in turn would cause all probes passing through plate 100 to be shorted out or connected to each other. *Id.* A POSITA reading *Fan* would have understood that in *Fan*’s first embodiment, plate 100 would have to be

made of a non-conductive material like ceramic to prevent all the probes 200 from being electrically connected to each other. *Id.* More importantly, there is no disclosure or suggestion in *Fan* that any portion of the non-conductive ceramic plate 100 of its first embodiment should be coated with insulating material. *Id.*

Fan discloses a second embodiment for which it expressly states: “The difference between the present embodiment and the embodiment of FIG. 2 relates to additional element of an insulating layer 600.” *Fan*, 5:3-5. *Fan* explains that when “the plate 100 is made of semiconductors or conductors, the surfaces of the plate 100 may be insulated to prevent the probes 200 that inserted to the plate 100 from electrically interrupt from each other.” *Id.*, 5:8-11. Specifically, the “insulating layer 600 may be at least disposed between the metal layer 310 and the plate 100.” *Id.*, 5:11-12; *Souri*, ¶138. Annotated Fig. 4 of *Fan*, illustrating this embodiment is excerpted below.

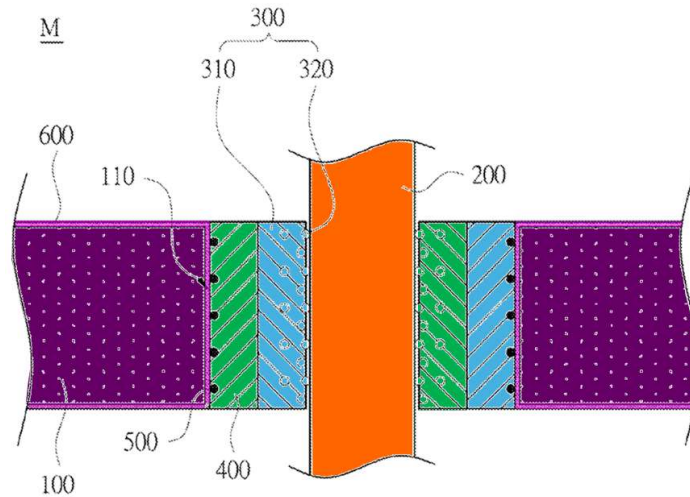


FIG. 4

Fan, Fig. 4 (annotated).

As Dr. Souri explains, adding the insulating layer 600 between plate 100 and base layer 400 and/or metal layer 310 as illustrated in Fig. 4 above makes sense because doing so prevents electrical connection between probe 200 and plate 100 made of a conductive material. Souri, ¶139. However, there is no disclosure or suggestion in *Fan* that insulating layer 600 “covers [a] non-conductive zone,” as recited in claim 3. *Id.*, ¶140. Quite the contrary, layer 600 in this embodiment of *Fan* covers a conductive plate 100. *Id.*

To summarize, *Fan*’s first embodiment does not disclose or suggest covering the surface of the non-conductive guide plate with a dielectric material. Souri, ¶141. And *Fan*’s second embodiment discloses covering the surface of a conductive guide plate with a dielectric material but does not disclose covering a non-conductive portion of the guide plate with dielectric material. *Id.*

Based on these disclosures, a POSITA would not have been motivated to cover a non-conductive portion of the guide plate with a dielectric material. Souri, ¶141. Petitioner and its expert both admit that *Kim*'s guide plate is made of non-conductive material. Pet., 39 (citing *Kim*, ¶[0062] and stating "the material of the upper and lower guide plates is non-conductive material"); Ex. 1003, ¶179 (citing *Kim*, ¶[0062] and stating, "[t]hus, a POSITA would understand that the material composed of the guide (10) including the upper plate (11) and the lower plate (12) is *necessarily non-conductive material*," emphasis added). According to Dr. Souri, because *Kim*'s guide plates 11 and 12 are made of non-conductive material, a skilled artisan would recognize from the first embodiment of *Fan* that there is no need to cover *Kim*'s non-conductive guide plates with an insulating layer. Souri, ¶142.

Petitioner nevertheless asserts: "A POSITA would have found it obvious to coat non-conductive zones on the face of the guide plate disclosed in *Kim* . . . with the insulating material disclosed in *Fan*." Pet., 69. Petitioner asserts that "a POSITA would have understood that applying *Fan*'s teaching to *Kim* by coating non-conductive zones on the guide plate taught in *Kim* with an insulating (dielectric) material would improve *Kim* by helping to ensure that testing pins and conductive portions carrying different signal types remain electrically separated." *Id.*, 70. Petitioner's expert simply repeats these same conclusory assertions. Ex. 1003, ¶¶335-336. But Petitioner and its expert provide no evidence or reasons for why a

POSITA would have been motivated to coat *Kim*'s guide plates with *Fan*'s insulating layer. Souri, ¶143. Although Petitioner and its expert assert in conclusory fashion that adding an insulating layer “would improve Kim,” neither provides any explanation of what in *Kim* would be improved, particularly when *Kim*'s non-conductive guide plates already ensure that testing pins and conductive portions carrying different signal types remain electrically separated. *Id.* Indeed, as Dr. Souri explains, adding dielectric material on the non-conductive zone may produce undesirable capacitance that may distort the test results obtained using *Kim*'s testing apparatus. *Id.*, ¶144. Contrary to Petitioner's assertion, therefore, a POSITA would not have found it obvious to coat portions of *Kim*'s non-conductive guide plate with dielectric material based on the disclosures of *Fan*. *Id.*

Thus, Petitioner fails to show that *Fan* discloses coating non-conductive guide plates with insulating material. Furthermore, Petitioner and its expert fail to demonstrate that a POSITA would have been motivated or found it obvious to coat *Kim*'s non-conductive guide plates with an insulating layer based on the teachings of *Fan*. In sum, Petitioner fails to show that the combination of *Kim* and *Fan* discloses or suggests all the elements of claim 3. Therefore, the combination of *Kim* and *Fan* does not render claim 3 obvious. Souri, ¶145.

H. The combination of *Kim* and *Bross* does not render obvious claim 12 (Ground 5)

Claim 12 recites “wherein the first conductive portion is embedded in the at least one guide.” Petitioner fails to show that the combination of *Kim* and *Bross* discloses or renders obvious at least this limitation. *Souri*, ¶¶146-156.

Petitioner asserts that “[a] POSITA would have found it obvious to select from known manufacturing methods, such as the ones from *Bross*, to form the conductive portion(s) in the guide of *Kim*.” *Pet.*, 70-71. Petitioner also asserts that “a POSITA would be motivated to use the well-known laminating methods described by *Bross*, applied to *Kim*, to embed one or more of the conductive portions within the guide plate and would have reasonably expected success in doing so.” *Id.*, 71. Petitioner, however, provides no reasons or bases for why a POSITA would have replaced *Kim*’s disclosed method of forming the conductive traces on a surface of *Kim*’s guide plate with *Bross*’s method of sandwiching conductive layers between insulating layers. *Id.* Petitioner’s expert repeats the same conclusory statements as Petitioner and also fails to provide any reasons for why a POSITA would have implemented *Bross*’s teachings on *Kim*’s device. *Ex.* 1003, ¶¶338-341. The Board should disregard such conclusory expert testimony. 37 C.F.R. § 42.65(a); *Upjohn*, 225 F.3d at 1311.

Moreover, a POSITA would not have been motivated to replace *Kim*'s relatively simple structure with the more complicated sandwiched structure of *Bross*. Souri, ¶¶147-150. Specifically, *Bross* discloses a probe assembly 20 with a body 22 that includes a multi-layer arrangement comprising "a top insulating layer 23, a first conductive layer 24, a second insulating layer 26, a second conductive layer 28, a third insulating layer 30, a third conductive layer 32, and a fourth or bottom insulating layer 34." *Bross*, 4:41-46. *Bross* also discloses that its "probe element 36 passes through a small, precisely located clearance hole 40 in the second insulating layer 26, through a similar hole 42 in the third insulating layer 30, and through a similar hole 44 in the fourth insulating layer 34." *Id.*, 4:66-5:2. *Bross* explains that "probe element 36 in piercing through the layer of conductive circuitry 32 at the zone 50 makes a mechanically tight and good electrical connection to a respective conductive portion of the layer of circuitry 32." *Id.*, 5:43-47; Souri, ¶¶150-151.

According to Dr. Souri, probe element 36 of *Bross* extends through hole 44, which is a clearance hole. Souri, ¶151. Probe element 36 makes electrical contact with the conductive layers 24, 28, and 32 because these conductive layers extend into clearance hole 44, and probe element 36 pierces through the conductive layers. *Id.* In contrast, in *Kim*, one side of *Kim*'s testing pin 30 "is electrically contacted with one side of the conductive layer 20," which is formed in the guide holes in *Kim*'s guide plate. *Id.*; *Kim*, ¶¶[0038]-[0039]. Thus, *Bross* discloses a completely

different arrangement of insulating and conductive layers as compared to that disclosed by *Kim*. Souri, ¶151.

Bross's structure requires taking a plurality of insulating layers and conductive layers and bonding them to form a multilayer bonded arrangement. *Bross*, 4:41-52. Nothing in *Bross* discloses or suggests any advantages of this method relative to the method of forming conductive traces 40 of *Kim* directly on the surfaces of *Kim*'s guide plate. Souri, ¶152. Petitioner and its expert provide no reasons or bases for why a POSITA would have completely replaced *Kim*'s disclosed guide plate structure with that of *Bross*'s multilayer bonded arrangement. Pet., 70-71; Ex. 1003, ¶¶338-341; Souri, ¶152.

The structure disclosed by *Bross* involves forming multiple insulating and conductive layers and bonding them together. Souri, ¶153. *Bross* discloses that the “various layers of printed circuitry are selectively connected at specially provided ‘via’ locations to respective ones of thin long conductive wires.” *Bross*, 2:10-13, 2:33-38. *Bross* also discloses that the “vias of the multi-layer circuitry are formed in precise pattern.” *Id.*, 2:17-18, 2:38-40. *Bross* explains that “vias are aligned vertically in one plane of view (e.g., the Y direction) and are staggered vertically in a plane of view at right angles.” *Id.*, 2:44-47. A POSITA would have recognized that the requirement of assembling a large number of parts in *Bross*'s structure, the need to precisely align these parts, and the added step of bonding them is likely to result

in greater manufacturing complexity and costs. Souri, ¶154. Furthermore, the requirement to precisely align multiple layers to ensure the vias formed in the different layers are vertically aligned in one direction while being staggered in another direction is also likely to increase manufacturing complexity and costs. *Id.* *Kim*'s structure does not require precise alignment of multiple material layers and does not require any added step of bonding multiple material layers. *Id.*, ¶155. A POSITA, therefore, would not have been motivated to replace *Kim*'s relatively simple structure with the more complicated sandwiched structure of *Bross* particularly because *Bross*'s structure provides no additional structural, manufacturing, or economic benefits over *Kim*'s guide plate arrangement. *Id.*

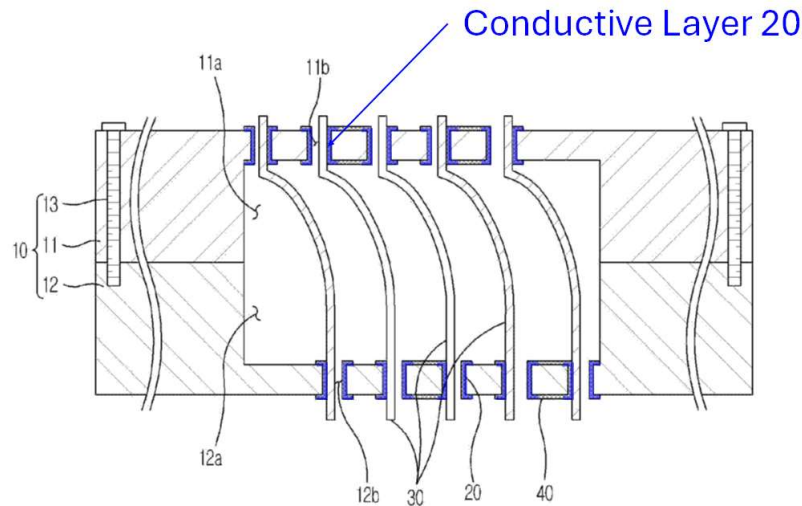
Thus, Petitioner fails to show that a POSITA would have been motivated and found it obvious to replace *Kim*'s structure with that of *Bross*. Souri, ¶156. The only way Petitioner could have arrived at such a combination is through impermissible hindsight. *Otsuka*, 678 F.3d at 1296; *Life Techs.*, 224 F.3d at 1325. Therefore, Petitioner fails to show that the combination of *Kim* and *Bross* renders claim 12 obvious. Souri, ¶156.

Petitioner also asserts in conclusory fashion that “if the claimed term ‘embedded’ can be met just by having the conductive layer formed on the inside of the guide hole, Kim discloses” this feature. Pet., 72. But the analysis provided by Petitioner's own expert belies Petitioner's assertion. Petitioner's expert states that

the “claimed term ‘embedded’ is used to distinguish the term ‘coated’ or ‘coat’ in terms of the process or method for forming conductive portions on the guide.” Ex. 1003, ¶343. Petitioner’s expert further explains that *Kim* discloses *coating* the inner portions of *Kim*’s guide holes, stating: “Kim discloses several methods for forming conductive material on the guide plate including *plating or depositing* using photoresistor film and etching to remove unnecessary conductive materials.” *Id.*, ¶344 (emphasis added).

Thus, Petitioner’s expert admits that *Kim* discloses a coating process that is different from embedding the conductive material in the guide plate. *Id.* Indeed, *Kim* discloses “[t]he conductive layer 20 is formed at one side of the upper plate 11, in which the first guide holes are formed, or one side of the lower plate, in which the second guide holes are formed, through the *coating* of the conductive material.” *Kim*, ¶[0038] (emphasis added). As seen in Fig. 2 of *Kim*, below, [conductive layer 20](#) coats the inner surfaces of the guide holes.

FIG. 2



Kim, Fig. 2 (annotated). Because *Kim* discloses coating conductive material in *Kim*'s guide holes, which Petitioner's expert expressly distinguishes from embedding, *Kim* does not disclose "the first conductive portion is embedded in the at least one guide," as recited in claim 12.

I. The combination of *Kim*, *Bross*, and *Schmid* does not render obvious claim 21 (Ground 7)

Like claim 12, claim 21 recites "wherein the first conductive portion is embedded in the at least one guide." Claim 21 depends from claim 16. Petitioner presents no new arguments for claim 21 but refers to its arguments for claims 12 and 16. Pet., 75. Petitioner does not rely on *Schmid* as disclosing or suggesting the recitations of claim 12. Pet., 70-73. In its analysis of claim 16, Petitioner again does not rely on *Schmid* for the recitations of claim 21. Pet., 66. As discussed above for claim 12, the combination of *Kim* and *Bross* fails to disclose or suggest the

limitations of claim 12. Section IV.H. Accordingly, for similar reasons, Petitioner fails to demonstrate that the combination of *Kim*, *Bross*, and *Schmid* renders obvious claim 21. *Souri*, ¶157.

J. Petitioner fails to demonstrate that independent claims 1, 16, and 23 are unpatentable and has therefore failed to meet its burden for all claims (Grounds 1-7)

1. Petitioner fails to identify with particularity what in *Kim* constitutes the claimed “first conductive portion” and “second conductive portion”

Independent claims 1, 16, and 23 recite “a first conductive portion” and “a second conductive portion.” Petitioner fails to articulate, with particularity, what in *Kim* discloses these claim elements. Compounding this problem, claim 14, which depends from claim 1, also recites the same “first conductive portion” and “second conductive portion,” but Petitioner points to different components in *Kim* for claim 14 than it did for claim 1. The Board has held that inconsistent mappings of the same claim term undermine a finding of unpatentability of the claims based on anticipation grounds. *See Commscope Techs. LLC v. Belden, Inc.*, IPR2023-01056, Paper 7 at 24 (P.T.A.B. Dec. 15, 2023) (“Petitioner’s inconsistent position on the interpretation of the ‘lateral edge’ term among its Grounds 1, 3, and 4 arguments undermines its position as to the interpretation of the term, and undermines its position that *Glew* discloses this limitation under an anticipation standard.”). The

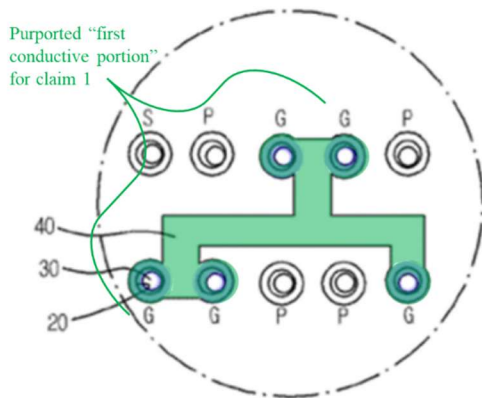
Board should hold the same way here and find that Petitioner fails to show that the independent claims are unpatentable.

When discussing independent claim 1 (the analysis of which is cross referenced for independent claims 16 and 23), Petitioner asserts that “[t]wo or more of the conductive layers (20) connected by *some or all* of the conductive trace (40) collectively constitute the claimed ‘first conductive portion.’” Pet., 31 (emphasis added); *see also id.*, 32 (referring to “conductive layers 20 and conductive trace 40 electrically connect[ing] a group of guide holes” as “this ‘first conductive portion’”). Petitioner’s nebulous description of what constitutes the first conductive portion in the context of claim 1 fails to identify with particularity how *Kim* anticipates claim 1 because it does not show how *Kim* discloses the elements “‘arranged as in the claim.’” *NetMoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1369-71 (Fed. Cir. 2008) (quoting *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

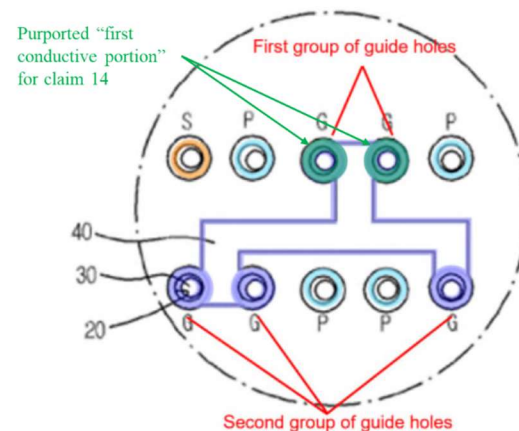
Petitioner’s claim 1 analysis is further exacerbated by its analysis of dependent claim 14, where it takes positions inconsistent with those taken for claim 1. *See supra* Section IV.B. For claim 1, Petitioner asserts that some of the conductive layers 20 “collectively” with “some or all of” the conductive trace 40 constitute the claimed first conductive portion for claim 1. Pet., 31 (emphasis added); *see also id.*, 32. But then it changes tack when discussing claim 14, arguing that

some conductive layers 20 *alone* constitute the claimed “first conductive portion.” *See id.*, 48-49. Specifically, for claim 14, Petitioner asserts that “[t]he *conductive layers 20* at these ‘first and second group of guide holes’ *are* the claimed ‘first’ and ‘second conductive portions.’” *Id.*, 48-49 (emphasis added). Furthermore, in its analysis of claim 14, Petitioner describes the conductive trace 40 of *Kim* as constituting an entirely different claimed feature, namely the “conductive track.” *Id.*, 49.

Thus, when it analyzes claim 1, Petitioner identifies conductive trace 40 of *Kim* as being included in the “first conductive portion” but when analyzing dependent claim 14, it excludes that same conductive trace 40 from the “first conductive portion.” The following figures from the Petition have been further annotated with **green** to illustrate Petitioner’s inconsistent identification of the first conductive portion for claim 1 (Pet., 34) as compared to that for claim 14 (*id.*, 49):



Pet., 34 (claim 1) (annotated)

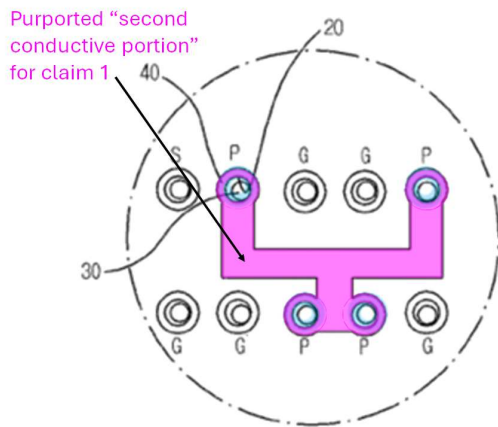


Pet., 49 (claim 14) (annotated)

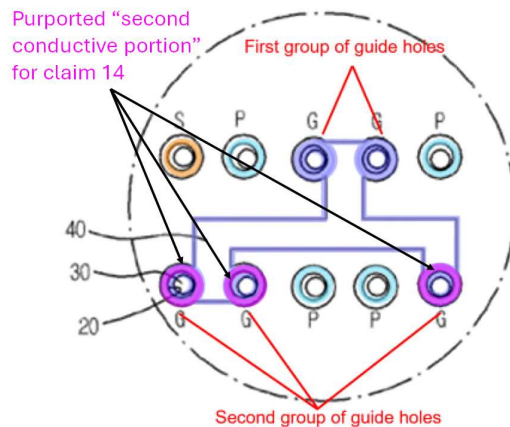
Petitioner also advances inconsistent positions regarding the “second conductive portion” as recited in claims 1 and 14. For claim 1, Petitioner asserts that “Kim describes and illustrates in Fig. 5b that testing pins carrying power signals (represented by ‘P’) are electrically connected via the conductive layers (20) and conductive trace (40).” Pet., 36. While failing to clearly identify the “second conductive portion” in *Kim*, Petitioner implies that the conductive layers 20 and conductive trace 40 of Fig. 5b constitute one of two “conductive portions.” *Id.*, 36-37. It also vaguely states that “[t]he disclosures cited above for limitation [1C] [(which recites the “first conductive portion”)] thus also apply to limitation [1D] [(which recites the “second conductive portion”)] and are incorporated herein.” *Id.*, 35. While it is unclear which parts of that section Petitioner intends to incorporate (because the sections address different conductive portions), this statement further suggests that Petitioner is including both conductive layers 20 and

conductive trace 40 as part of the “second conductive portion,” as it did with the “first conductive portion.”

Then, when analyzing claim 14, Petitioner again contradicts itself because it asserts that *some* conductive layers 20 *alone* constitute the claimed “second conductive portion.” Pet., 48-49. Thus, in its analysis of claim 14, Petitioner not only excludes the conductive trace 40 but also excludes conductive layers 20 associated with pins labeled “P” from its identification of the claimed “second conductive portion.” *Id.* Instead, Petitioner identifies a conductive layer associated with pins labeled “G” as the second conductive portion for claim 14. The following figures from the Petition have been further annotated with pink to illustrate Petitioner’s inconsistent identification of the second conductive portion for claim 1 (*id.*, 36) with that for claim 14 (*id.*, 49):



Pet., 36 (claim 1) (annotated)



Pet., 49 (claim 14) (annotated)

Petitioner’s inconsistent mappings of what in Kim constitutes the “first conductive portion” and the “second conductive portion” are fatal to its anticipation analysis of claim 1. *See Commscope*, IPR2023-01056, Paper 7 at 24. And while Petitioner does not advance an anticipation theory for claims 16 and 23, its obviousness analysis for those claims relies solely on its claim 1 anticipation analysis for the “first conductive portion” and the “second conductive portion.” Pet., 64-67; *see infra* Section IV.J.2. Accordingly, Petitioner’s flawed analysis for claim 1 infects its analysis of claims 16 and 23, undermining all grounds.

“[T]he burden of persuasion is on the petitioner to prove ‘unpatentability by a preponderance of the evidence.’” *In re Magnum Oil*, 829 F.3d at 1375 (quoting 35 U.S.C. § 316(e)). Moreover, the Board is bound by the inconsistent theories advanced by Petitioner and may not *sua sponte* modify any of those theories to determine unpatentability of the challenged claims. *Id.* at 1381. The Board should therefore find that Petitioner fails to meet its burden of identifying with particularity the claimed “first conductive portion” and “second conductive portion.” *See Harmonic, Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1363 (Fed. Cir. 2016).

2. Petitioner’s obviousness arguments do not salvage its flawed anticipation position.

In its obviousness analysis of claim 1, Petitioner focuses on purported “differences in terminology” between *Kim* and the ’885 patent (Pet., 50), the

purported obviousness of combining the teachings of *Kim*'s embodiments (*id.*), and on the purported disclosures of the Korean Patent Application No. 10-2014-0004576 (*id.*, 51). However, Petitioner's obviousness analysis does not address the deficiencies identified above in Section IV.J.1. *See* Pet., 49-52.

Similarly, in the analyses of claim 16 and 23 which cross reference the analyses for claims 5 and 6 (Pet., 66, 67), Petitioner relies on *Schmid* for the purported teaching of three guide plates, (*id.*, 61-64). However, Petitioner's obviousness analysis for claims 16 and 23, based on *Kim* alone or in combination with *Schmid*, also does not address the deficiencies identified above in Section IV.J.1. *See generally* Pet., 61-67.

Accordingly, the Petition has also failed to demonstrate that independent claims 1, 16, and 23 and the claims dependent therefrom are unpatentable.

V. Conclusion

For the foregoing reasons, Patent Owner respectfully requests the Board find that none of Challenged Claims 1-23 are unpatentable.

Respectfully submitted,

Dated: April 18, 2025

/Houtan K. Esfahani/
Houtan K. Esfahani, Reg. No. 41,893
Finnegan, Henderson, Farabow,
Garrett & Dunner, LLP
Lead Counsel for Patent Owner
Technoprobe S.p.A.

CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), I, Houtan K. Esfahani, certify that **Patent Owner's Response** contains 13,977 words, excluding those portions identified in 37 C.F.R. § 42.24(a), as measured by the word-processing system used to prepare this paper.

Dated: April 18, 2025

/Houtan K. Esfahani/
Houtan K. Esfahani, Reg. No. 41,893

CERTIFICATE OF SERVICE

The undersigned certifies that a copy of the foregoing **Patent Owner's Response** was served electronically via email on April 18, 2025, in its entirety on the following:

T. Vann Pearce, Jr.
Jasmine Zhu
Orrick, Herrington & Sutcliffe LLP
2100 Pennsylvania Avenue NW
Washington, DC 20037
TVPPTABDocket@orrick.com
PTABDocketJ3Z8@orrick.com

Anri Nakamoto
Orrick, Herrington & Sutcliffe LLP
Izumi Garden Tower, 28th Floor
6-1 Roppongi 1-Chome
Minato-ku, Tokyo, 106-6028
Japan

Petitioner has consented to service by email.

Dated: April 18, 2025

/William Esper/
William Esper
Legal Assistant and PTAB Coordinator
Finnegan, Henderson, Farabow,
Garrett & Dunner, LLP