

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FORMFACTOR, INC.,
Petitioner,

v.

TECHNOPROBE S.P.A.,
Patent Owner.

Case IPR2024-00933
Patent No. 11,035,885

**DECLARATION OF SHUKRI SOURI, Ph.D.
IN SUPPORT OF PATENT OWNER'S RESPONSE**

TABLE OF CONTENTS

I.	Introduction.....	1
II.	Summary of Opinions.....	1
III.	Qualifications and Background	2
IV.	Materials Considered	6
V.	Legal Standards	8
A.	Level of Ordinary Skill	9
B.	Prior Art.....	10
C.	Anticipation	10
D.	Obviousness.....	11
E.	Claim Construction	16
VI.	Level of Ordinary Skill in the Art	16
VII.	Claim Construction.....	19
A.	“the first conductive portion is locally interrupted by at least one non-conductive zone” (claim 2)	19
VIII.	Petitioner Has Not Demonstrated that Claims 2, 3, 5, 6, 7, 12, 14, 16, 17, 18, 21, and 23 Are Unpatentable	29
A.	<i>Kim</i> does not anticipate or render obvious claim 2 (Grounds 1, 2).....	29
B.	<i>Kim</i> does not anticipate or render obvious claim 14 (Grounds 1, 2).....	32
C.	<i>Kim</i> does not render obvious claim 7 (Ground 2).....	41
D.	The combination of <i>Kim</i> and <i>Schmid</i> does not render obvious claim 18 (Ground 3)	53

E.	The combination of <i>Kim</i> and <i>Schmid</i> does not render obvious claims 6 and 23 (Ground 3).....	53
F.	The combination of <i>Kim</i> and <i>Schmid</i> does not render obvious claims 5, 16, and 17 (Ground 3).....	64
G.	The combination of <i>Kim</i> and <i>Fan</i> does not render obvious claim 3 (Ground 4)	67
H.	The combination of <i>Kim</i> and <i>Bross</i> does not render obvious claim 12 (Ground 5)	75
I.	The combination of <i>Kim</i> , <i>Bross</i> , and <i>Schmid</i> does not render obvious claim 21 (Ground 7)	80
IX.	CONCLUSION.....	81

I. Introduction

1. I, Shukri Sourì, Ph.D., am the investigator for the subject matter in this declaration. Exponent, Inc. (“Exponent”) has been retained by Finnegan, Henderson, Farabow, Garrett & Dunner, LLP on behalf of Technoprobe S.P.A. (“Technoprobe”) for my services as an independent technical expert in connection with an *inter partes* review (“IPR”) of U.S. Patent No. 11,035,885 (“the ’885 patent”) (Ex. 1001) initiated by FormFactor, Inc. (“FormFactor”). I have prepared this declaration in connection with Technoprobe’s Response to FormFactor’s Petition for *Inter Partes* Review.

2. Specifically, this declaration contains my opinions about the technology in certain claims of the ’885 patent and the grounds against these claims that have been asserted by FormFactor. I was not asked to provide any opinions about the ’885 patent that are not expressed herein.

II. Summary of Opinions

3. I was asked by counsel for Technoprobe to consider claims 2, 3, 5, 6, 7, 12, 14, 16, 17, 18, 21, and 23 of the ’885 patent. Below, I set forth the opinions I have formed, the conclusions I have reached, and the bases for these opinions and conclusions. I believe the statements contained in this declaration to be true and correct to the best of my knowledge.

4. Based on my experience, knowledge of the art at the time of the applicable priority date (I was told to assume a priority date of December 16, 2016), it is my opinion that claims 2, 3, 5, 6, 7, 12, 14, 16, 17, 18, 21, and 23 of the '885 patent are patentable over the prior art and prior art combinations identified by FormFactor and as discussed below.

5. I am a salaried employee of Exponent, Inc., which is being compensated at my normal consulting rate. My compensation is in no way contingent upon the nature of my findings, the presentation of my findings in testimony, or the outcome of this proceeding.

III. Qualifications and Background

6. I believe that I am well qualified to serve as a technical expert in this matter based upon my qualifications, discussed in detail below.

7. Based on my education, research, and work experience, I am knowledgeable about the subject matter of the '885 patent and the related prior art.

8. Currently, I am a Principal and a Corporate Vice President at Exponent, an engineering and science consulting firm headquartered at 149 Commonwealth Drive, Menlo Park, California 94025. I am based in, and Director of, Exponent's New York office. I am also the Director of Exponent's Electrical Engineering and Computer Science practice.

9. I received my B.A. (Honors) and M.A. in Engineering Science from Oxford University, United Kingdom, with a focus on semiconductor materials, processing and characterization; my Master's degree in Electrical Engineering ("MSEE") specializing in Integrated Circuit ("IC") design and semiconductor processing from Stanford University, California; and my Ph.D. in Electrical Engineering, also from Stanford University, California.

10. My doctoral research at Stanford, for which I was awarded the Ph.D. degree in 2003, was in 3-dimensional design and fabrication of ICs ("3-D ICs"). In this paradigm, ICs comprise circuits that can be fabricated on multiple layers of active silicon instead of only on the surface of a semiconductor wafer. My contributions included designing and fabricating such circuits as well as identifying and analyzing novel interconnect architectures required to efficiently connect semiconductor devices in 3D arrangement. The goal driving my work was enabling Giga Scale Integration ("GSI") and enhanced speeds in ICs.

11. Throughout my academic and professional career, including my research both at Oxford and Stanford, I acquired skills and expertise in semiconductor processing, IC design, fabrication and characterization. This enabled me to process various semiconductor materials as well as design and fabricate my own semiconductor ICs, using standard process steps including photoresist coating, photolithography, etching, deposition, and ion implantation.

12. I also gained experience designing and implementing test structures in my ICs to allow me to characterize my semiconductor process steps and to perform functional testing of my ICs at the end of fabrication. I performed such characterization and functional testing using probe testing techniques, including manual microprobe test stations as well as automated test equipment (“ATE”) and probe heads.

13. Between my MSEE and Ph.D., I worked as a Research Scientist and a Research Engineer at Raychem Corporation, where I designed semiconductor devices and circuits and the processes to fabricate them. I also designed test parameters to functionally test the devices using probe stations and programmed to control ATE using standard interface buses such as HP-IB/IEEE-488, for example, to acquire and analyze test data.

14. During my Raychem tenure, I also gained experience with different types of electro-ceramic materials and their manufacturing techniques, such as those used for semiconductor protection, electrical capacitors and ceramic Printed Circuit Boards (“PCBs”). My work at Raychem resulted in patents awarded by United States, European, and Japanese patent offices.

15. Exponent’s founding in the late 1960s was based on applying science and scientific method in understanding failures of products. Before renaming, Exponent was known as Failure Analysis Associates. Since joining Exponent more

than 20 years ago, my professional activities have included working with industry members to understand failure modes of their products, whether such failures occur in the field after deployment, during manufacturing and quality assurance, or even earlier in the design and validation phase. The knowledge acquired during such root cause investigations is typically fed back into the manufacturer's product design cycle for purposes of improving yield, quality, reliability, safety and lifetime of the same or new product.

16. Over the years at Exponent, I have led several investigations to identify the root cause of failures involving ICs and PCBs. As examples, such failures have involved interposer boards in Ball Grid Array ("BGA") and multi-chip module ("MCM") packages. Such interposer boards form an electrical bridge between the fine-pitched contacts on ICs and the more spread-out connections on other PCBs such as motherboards. As a result of my investigations, I have worked with industry members on PCB designs.

17. My work on IC failures also involved the use of testing probes to characterize electrical properties of subcircuits and devices. Such IC failures included working with various types of volatile and non-volatile memory chips, as well as processors and controllers. As a result of my investigations, I have worked with industry members on improving IC design.

18. A full list of my patents and journal publications in addition to my academic and industrial experience is further detailed in my curriculum vitae, which is attached to this declaration as Appendix A.

IV. Materials Considered

19. In forming my opinions, I have considered FormFactor's Petition, all the exhibits submitted by FormFactor with the Petition, Patent Owner's Preliminary Response, and the Board's decision to institute trial ("Institution Decision"). In addition, I have considered the exhibits listed in the table below. My opinions are based on my experience, knowledge of the relevant art, the documents identified in the Table below, as well as the documents directly cited in this declaration.

Exhibit	Description
Ex. 2002	U. S. Patent Publication No. 2008/0139017 (" <i>Kiyofuji</i> ")
Ex. 2003	<i>Electrical Engineering Dictionary CRCnetBase 2000</i> 1-4 (Phillip A. Laplante et al. eds., CRC Press LLC 2000)
Ex. 2004	<i>Application Note: Three and Four Port S-parameter Measurements: Calibrations and Mixed-Mode Parameters</i> , Anritsu, Microwave Measurements Division (2002) (" <i>Anritsu</i> ")
Ex. 2005	U. S. Patent No. 6,940,299 (" <i>Lim</i> ")

Exhibit	Description
Ex. 2006	Henry W. Ott, <i>Electromagnetic Compatibility Engineering</i> 194-237 (John Wiley & Sons, Inc. 2009) (“Ott”)
Ex. 2007	Ron Schmitt, <i>Electromagnetics Explained: A Handbook For Wireless/RF, EMC, and High-Speed Electronics</i> 25-49, 139-52 (Elsevier Science 2002) (“Schmitt”)
Ex. 2008	<i>Printed Circuits Handbook</i> , excerpts from chs. 2, 5, 20, 22, 23, 26, 27, 63 (Clyde F. Coombs, Jr. et al. eds., 6th ed., McGraw Hill 2008) (“Coombs”)
Ex. 2009	Gary S. May & Costas J. Spanos, <i>Fundamentals of Semiconductor Manufacturing and Process Control</i> 25-61 (John Wiley & Sons 2006) (“May”)
Ex. 2010	R. Singh & R. K. Ulrich, <i>High and Low Dielectric Constant Materials</i> , ELECTROCHEMICAL SOCIETY INTERFACE 26-30 (1999) (“Singh”)
Ex. 2011	Lee W. Ritchey, <i>Designing a PCB Stackup, Part 1</i> , PCB DESIGN MAGAZINE 12-16, 18-21 (2012) (“Ritchey”)
Ex. 2012	John Levreault, <i>Partner Early for HDI Board Design</i> , PCB DESIGN MAGAZINE 26, 28-31 (2012) (“Levreault”)
Ex. 2013	Happy Holden, <i>A Chronicle of Speed and Density: The TLA Design Winners Through the Years</i> , PCB DESIGN MAGAZINE 38, 40-42, 44-48 (“Holden”)
Ex. 2014	Paul Reid, <i>The Wrap Crack</i> , PCB DESIGN MAGAZINE 78, 80-81 (2012) (“Reid”)

Exhibit	Description
Ex. 2015	Ken Smith and Dean Gahagan, <i>Challenges and More Challenges: SW Test Workshop June 9, 2004</i> (2004) (“Smith”)
Ex. 2016	Chih-Chang Hsu & Hung-Lung Chen, <i>SW Test Workshop: Innovative Laser Processing and Drilling Techniques for Future Probe Card Applications June 5-8, 2016</i> (2016) (“Hsu”)

V. Legal Standards

20. I am not a lawyer. My understanding of the legal standards to apply in reaching the conclusions in this declaration is based on discussions with counsel for Patent Owner, my experience applying similar standards in other patent-related matters, and my reading of the documents submitted in this proceeding. In preparing this declaration, I have tried to faithfully apply these legal standards to the challenged claims.

21. I have been informed that there are two ways in which prior art may render a patent claim unpatentable. First, I have been informed that the prior art may “anticipate” a claim. Second, I have been informed that the prior art may render a claim “obvious” to a person of ordinary skill in the art. I understand that a claim is patentable if it was not anticipated by and would not have been obvious in view of the prior art at the effective filing date of the patent.

22. I have been informed that a dependent claim is a patent claim that refers back to another patent claim. I have been informed that a dependent claim includes all of the limitations of the claim to which it refers.

23. I have been asked to provide my opinions as to whether the identified prior art teaches or renders obvious certain claims of the '885 patent from the perspective of a person of ordinary skill in the art at the '885 patent's earliest claimed priority date in 2016, as described in more detail below.

24. I have been informed that in *inter partes* review proceedings, such as this one, the party challenging the patent bears the burden of proving unpatentability by a preponderance of the evidence. I understand that a preponderance of the evidence means "more likely than not."

25. For purposes of this declaration, I have been asked to provide my opinions on issues regarding patentability. I have been informed of the following legal standards, which I have applied in forming my opinions.

A. Level of Ordinary Skill

26. I have been informed that a person of ordinary skill in the art is determined by considering several factors, including the (i) type of problems encountered in the art; (ii) prior art solutions to those problems; (iii) rapidity with which innovations are made; (iv) sophistication of the technology; and (v) educational level of active workers in the field.

27. I have been instructed to assume a person of ordinary skill in the art is not a specific, real individual, but rather a hypothetical individual having the qualities reflected by the factors discussed above.

B. Prior Art

28. I have been advised and understand the information used to evaluate whether an invention was new and not obvious when made is generally referred to as “prior art.” I understand that prior art includes patents and printed publications that existed before the earliest claimed priority date or the earliest filing date of the patent (which I have been informed is also called the “effective filing date”). I have been informed and understand that a patent or published patent application is prior art if it was filed before the earliest filing date of the claimed invention and that a printed publication is prior art if it was publicly available before the earliest filing date.

C. Anticipation

29. I have been informed that under 35 U.S.C. § 102, a patent claim is unpatentable for anticipation if it is not novel, including if the claimed subject matter was patented or described in a printed publication before the effective filing date of the claimed invention. I have been informed that this is referred to as unpatentability by anticipation. I have been informed that a patent claim is

anticipated under § 102 if a single prior art reference discloses all limitations of the claimed invention.

D. Obviousness

30. I have been informed that under 35 U.S.C. § 103, a patent claim is unpatentable if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious to a person having ordinary skill in the art to which said subject matter pertains at the time the invention was made. I have been informed that this is referred to as unpatentability by obviousness.

31. I have been informed that a proper obviousness analysis includes the following:

- a. Determining the scope and content of the prior art;
- b. Ascertaining the differences between the prior art and the claims at issue;
- c. Resolving the level of ordinary skill in the pertinent art; and
- d. Considering evidence of secondary indicia of non-obviousness (if available).

32. I have been informed that the relevant time for considering whether a claim would have been obvious to a person of ordinary skill in the art is the time of invention. For my obviousness analysis, counsel for Patent Owner instructed me to

assume that the date of invention for the Challenged Claims is December 16, 2016.

My opinions would not change if I assumed a later date of invention.

33. I have been informed that a reference may be modified or combined with other references or with a person of ordinary skill in the art's own knowledge if the person would have found the modification or combination obvious. I have also been informed that a person of ordinary skill in the art is presumed to know all the relevant prior art, and the obviousness analysis may take into account the inferences and creative steps that a person of ordinary skill in the art would employ.

34. I have been informed that whether a prior art reference renders a patent claim obvious is determined from the perspective of a person of ordinary skill in the art. I have also been informed that, while there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, and while a suggestion to combine known elements to achieve the claimed invention may come from the prior art as a whole or individually and may consider the inferences and creative steps a person of ordinary skill in the art would employ, as filtered through the knowledge of one skilled in the art, obviousness grounds cannot be sustained by mere conclusory statements and must include some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.

35. In determining whether a prior art reference could have been combined with another prior art reference or other information known to a person having ordinary skill in the art, I have been informed that the following principles may be considered:

- a. A combination of familiar elements according to known methods is likely to be obvious if it yields predictable results;
- b. The substitution of one known element for another is likely to be obvious if it yields predictable results;
- c. The use of a known technique to improve similar items or methods in the same way is likely to be obvious if it yields predictable results;
- d. The application of a known technique to a prior art reference that is ready for improvement to yield predictable results;
- e. Any need or problem known in the field and addressed by the reference can provide a reason for combining the elements in the manner claimed;
- f. A person of ordinary skill often will be able to fit the teachings of multiple references together like a puzzle; and
- g. The proper analysis of obviousness requires a determination of whether a person of ordinary skill in the art would have a “reasonable expectation of success”—but not “absolute predictability” of

success—in achieving the claimed invention by combining prior art references.

36. I have been informed that, when a work is available in one field, design alternatives and other market forces can prompt variations of it, either in the same field or in another. I have been informed that if a person of ordinary skill in the art could have implemented a predictable variation and would have seen the benefit of doing so, that variation is likely to have been obvious. I have been informed that, in many fields, there may be little discussion of obvious combinations, and in these fields market demand—not scientific literature—may drive design trends. I have been informed that, when there was a design need or market pressure and there are a finite number of predictable solutions, a person of ordinary skill in the art would have had a good reason to pursue those known options.

37. I have been informed that the law permits the application of “common sense” in examining whether a claimed invention would have been obvious to a person skilled in the art. For example, I have been informed that combining familiar elements according to known methods and in a predictable way may suggest obviousness when such a combination would yield nothing more than predictable results. I understand, however, that a claim is not obvious merely because every claim element is disclosed in the prior art and that a party asserting

obviousness must still provide a specific motivation to combine or modify the references as recited in the claims and explain why one skilled in the art would have reasonably expected to succeed in doing so.

38. I have been informed that there is no rigid rule that a reference or combination of references must contain a “teaching, suggestion, or motivation” to combine references. But I also understand that the “teaching, suggestion, or motivation” test can be a useful guide in establishing a rationale for combining elements of the prior art. I have been informed that this test poses the question as to whether there is an express or implied teaching, suggestion, or motivation to combine prior art elements in a way that realizes the claimed invention, and that it seeks to counter impermissible hindsight analysis.

39. I have been informed that, in an obviousness analysis, prior art must be analogous prior art to the patent being considered. I have been informed that a prior art reference is considered to be analogous, or in the same field of art, if the reference is either (1) in the same field of endeavor as the challenged patent, regardless of the problems the challenged patent and the prior art address, or (2) reasonably pertinent to the particular problem being solved by the challenged patent.

E. Claim Construction

40. I have been instructed that the “intrinsic record” includes the patent itself, including the claims, description, and figures, and the patent’s prosecution history—i.e., the record of proceedings at the U.S. Patent and Trademark Office (“Patent Office”) concerning the patent. I understand that, like the claims and written description, the prosecution history provides evidence to a person of ordinary skill in the art of how the inventor intended his patent to be understood, and how the Patent Office understood the patent. I understand that the inventor is permitted to apply a special definition to the terms or to limit the scope of claim terms in his patent claims, which may differ from the term’s plain and ordinary meaning. That special definition or limitation on scope may be provided in the patent’s written description, the patent’s prosecution history, or both.

41. I understand that claim interpretation may also be informed by “extrinsic evidence” (that is, evidence outside of the patent record itself). I have been informed that extrinsic evidence may include dictionaries, technical treatises, and other materials evidencing the meaning of a claim term and the understanding held by a person of ordinary skill in the art in the relevant time period.

VI. Level of Ordinary Skill in the Art

42. In rendering the opinions set forth in this declaration, I was asked to consider the ’885 patent’s claims and the prior art through the eyes of a person of

ordinary skill in the art (which I may also refer to as “one skilled in the art,” “skilled artisan,” “POSITA,” or similar variation). I have considered factors such as the educational level and years of experience of those working in the pertinent art, the types of problems encountered in the art, the teachings of the prior art, patents and publications of other persons or companies, and the sophistication of the technology.

43. I understand that FormFactor provides the following definition of a person of skill in the art:

A POSITA would have had at least a bachelor’s degree in electrical engineering, mechanical engineering, and materials engineering or another field applicable to wafer probing technology with three to five years of professional experience in designing and/or using probe technologies, or an equivalent level of skill, knowledge, and experience.

Pet., 22.

44. In my opinion, FormFactor’s definition is unclear. A POSITA would have had at least a bachelor’s degree in electrical engineering, mechanical engineering, materials engineering, or another field applicable to wafer probing technology, and either three to five years of professional experience in designing and/or using probe technologies, or an equivalent amount of training or work experience. Moreover, additional education could substitute for professional experience, and significant work experience could substitute for formal education.

45. I was at least a person of ordinary skill in the art as of December 16, 2016. In particular, as I explained above, I received a doctoral degree in electrical engineering in 2003 from Stanford University. In addition, in my engineering and scientific consulting career of more than twenty years, I have become intimately familiar with integrated circuit (IC) fabrication processes, printed circuit board assemblies, and semiconductor materials. I have also taught several courses on integrated circuit fabrication and, therefore, I have significant experience in semiconductor and printed circuit board fabrication technologies, including lithography. Additionally, as I described in more detail above, I have significant experience in testing of ICs using micro-scale wafer test probes for functional testing and using Automated Test Equipment to perform parametric testing and process characterization. My experience includes: designing test structures on wafers for process characterization and IC functional testing; using probe stations for sampling specific locations on a semiconductor wafer for testing; generation of test patterns to verify circuit functionality; designing of PCBs for IC packaging and assembly; and application of probe testing for root cause analysis of IC failures. Accordingly, I meet the definition of a person of ordinary skill in the art that I outlined above at least as of December 16, 2016.

VII. Claim Construction

46. Patent Owner's counsel has informed me that in an IPR proceeding such as this one, the Board construes claims using a standard under which claims receive their ordinary and customary meaning as would be understood by a POSITA in the context of the specification and the prosecution history.

A. “the first conductive portion is locally interrupted by at least one non-conductive zone” (claim 2)

47. Claim 2 of the '885 patent recites “the first conductive portion is locally interrupted by at least one non-conductive zone.” Petitioner's expert, Mr. Taber does not propose an express construction for the phrase “locally interrupted,” but instead implicitly interprets the phrase to mean providing a “gap” in the conductive portion. Ex. 1003, ¶¶ 178, 180; *see also* Pet., 39-40. Specifically, Mr. Taber states: “As shown in Figure 5B, the non-conductive zones surround the probes that carry the other type of signal, so there is a gap in the conductive portion, and in that way the non-conductive zones ‘locally interrupt’ the conductive portions.” Ex. 1003, ¶ 178; *see also* Pet., 39. I disagree with Mr. Taber's analysis. As I explain below, a skilled artisan would not have interpreted the phrase “locally interrupted” in claim 2 of '885 patent as referring to any “gap” in a conductive portion.

48. I understand that in this proceeding, Patent Owner proposes that the construction of the phrase “the first conductive portion is locally interrupted by at

least one non-conductive zone” in claim 2, is “the first conductive portion encloses at least one non-conductive zone.” In my opinion, this construction is consistent with how a skilled artisan would have understood the term “locally interrupted” in light of the ’885 patent’s specification and prosecution history.

49. The ’885 patent discloses: “According to an aspect of the present disclosure, the at least one conductive portion can be *separated* from further conductive portions *and/or* can be *locally interrupted* by at least one non-conductive zone.” ’885 patent, col. 3, lines 56-59 (emphases added). Thus, the ’885 patent specification explicitly distinguishes between two exemplary configurations: (1) where at least one conductive portion is *separated* from other conductive portions by at least one non-conductive zone; and (2) where the at least one conductive portion is *locally interrupted* by at least one non-conductive zone. In my opinion, claim 2, which recites “locally interrupted,” is directed to the second configuration disclosed by the ’885 patent.

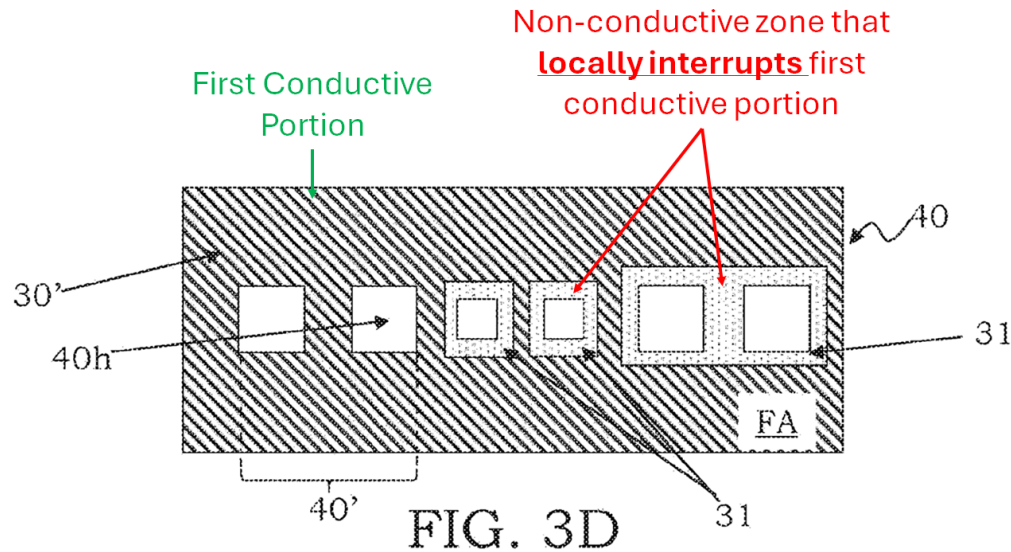
50. The ’885 patent explains the configurations in which a conductive portion is locally interrupted, stating: “If the first contact elements 21’ apt to carry ground signals and the second contact elements 21” apt to carry power signals are alternated one after the other, both the conductive portions 30’ and 30” are *locally interrupted* by suitable non-conductive zones 31’ and 31”.” ’885 patent, col. 13, lines 26-30. Notably, the ’885 patent particularly states that this is similar to what

is “observed in relation to FIGS. 3A-3D.” ’885 patent, col. 13, line 31. The ’885 patent additionally explains:

[E]ach conductive layer may be *locally interrupted* by suitable non-conductive zones 31’’ in order to not electrically connect contact elements that must not be short-circuited to each other. *In particular, the non-conductive zones 31’’ of a layer are formed at the holes housing contact elements that must not be short-circuited by said layer*, whereas said layer covers at least partially the walls of the guide holes housing contact elements that must be short-circuited by it.

’885 patent, col. 14, lines 2-10 (emphases added).

51. The ’885 patent discloses that as “shown in FIG. 3D, the first conductive portion 30’ covers a face of the guide 40 (the face FA in the example), except for areas where guide holes apt to house contact elements that must not be short-circuited are formed.” ’885 patent, col. 10, lines 38-41. The ’885 patent further explains that “the first conductive portion 30’ is not formed in areas where the guide holes that do not belong to group 40’ are formed.” ’885 patent, col. 10, lines 42-44. I have excerpted Fig. 3D of the ’885 patent below.



'885 patent, Fig. 3D (annotated).

52. As illustrated in the above figure, the guide holes that do not belong to the first conductive portion 30' are enclosed by non-conductive zones 31. Further, as shown in annotated Fig. 3D of the '885 patent above, the first conductive portion 30' is "locally interrupted" by the non-conductive zones 31 because the first conductive portion 30' encloses the non-conductive zones 31.

53. This is also consistent with the way in which the Examiner interpreted the phrase "locally interrupted" during prosecution of U.S. Application No. 16/442,385 ("the '385 application"), which issued as the '885 patent. The '385 application included application claim 2, which recited "the first conductive portion is locally interrupted by at least one non-conductive zone." Ex. 1002, p. 395. The Examiner rejected this claim based on U.S. Patent Publication No. 2008/0139017 ("*Kiyofuji*"; Ex. 2001). Ex. 1002, 60. The Examiner stated:

“Kiyofuji et al. disclose wherein the first conductive portion 48 is locally interrupted by at least one non-conductive zone 50b (*see Fig. 7, zone 50b belong to insulated/non-conductive plate see par. 0059*).” Ex. 1002, 60 (emphasis in original).

54. *Kiyofuji* discloses “an electrical connecting apparatus 10 is disposed in a tester (not shown) for testing an integrated circuit as a device under test 12.” *Kiyofuji*, ¶ [0045]. *Kiyofuji* discloses that its apparatus 10 includes a flat-plate like support member 20, a flat circuit board 22 held on the underside of the support member 20, and a flat-plate like electrical connecting device 24 disposed on the underside of the circuit board. *Kiyofuji*, ¶ [0046]. *Kiyofuji* also discloses that “the electrical connecting device 24 includes: an electrical insulating plate 40 formed into a rectangular shape” and “multiple through holes 42 formed to penetrate the insulating plate 40.” *Kiyofuji*, ¶ [0054]. *Kiyofuji* explains that “electrical insulating plate 40 has also a conductive earth pattern 46 on the upside and underside of the electrical insulating plate 40 and a conductive film 48 on the inner surface of each through hole 42.” *Kiyofuji*, ¶ [0059]. *Kiyofuji* further explains that “earth patterns 46 and conductive film 48 are electrically connected to each other.” *Kiyofuji*, ¶ [0060]. I have reproduced an annotated version of Fig. 7 of *Kiyofuji* below, illustrating some of these features.

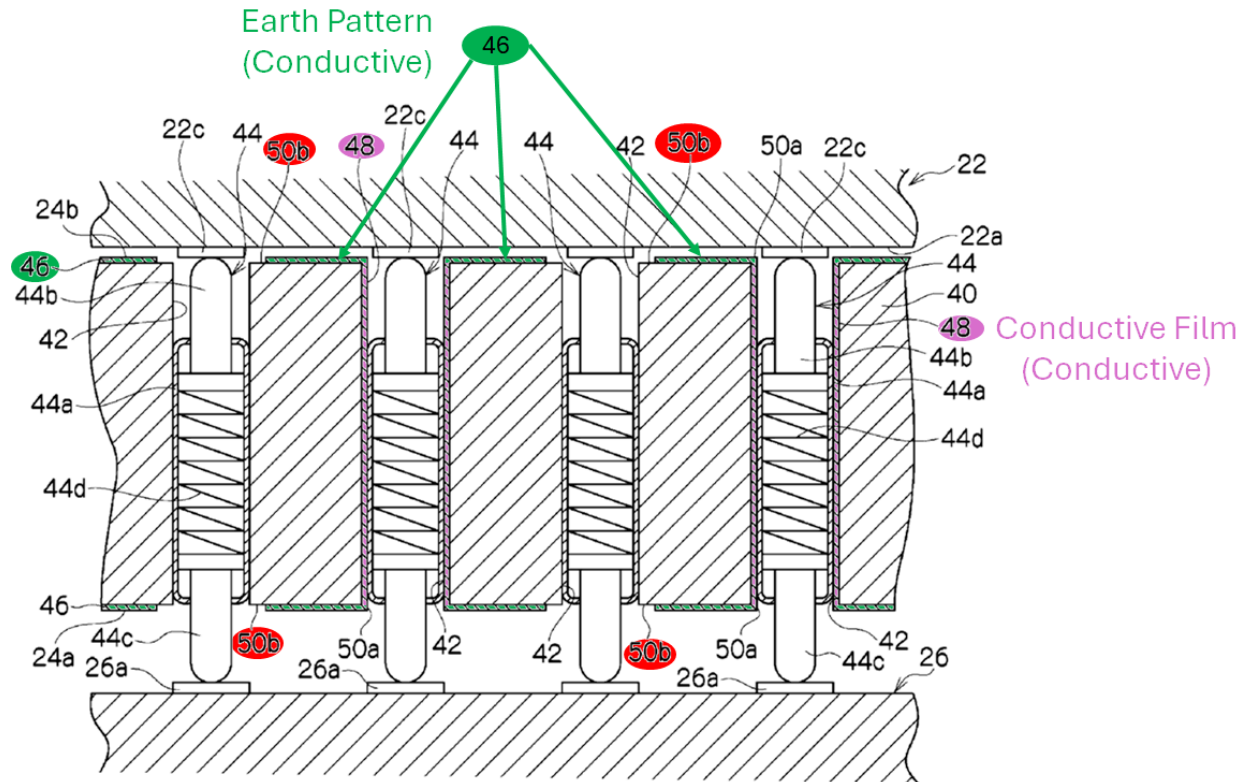


Fig. 7

Kiyofuji, Fig. 7 (annotated).

55. As seen in the above figure, element “50b” of *Kiyofuji* is a part of insulating plate 40. As the Examiner notes, element 50b of *Kiyofuji* locally interrupts element “48.” Because element 48 of *Kiyofuji* is physically and electrically connected to element 46, element 50b of *Kiyofuji* effectively locally interrupts element 48.

56. *Kiyofuji* discloses that Fig. 6 is a bottom view of the cross-sectional view shown in Fig. 7. For example, *Kiyofuji* discloses: “FIG. 6 is a bottom view showing the first embodiment of the electrical connecting device according to the

present invention.” *Kiyofuji*, ¶ [0038]. Further, *Kiyofuji* discloses: “FIG. 7 is an enlarged sectional view of the electrical connecting device shown in FIG. 6.”

Kiyofuji, ¶ [0039]. Although the examiner did not specifically refer to Fig. 6 of *Kiyofuji*, it is instructive to consider both Figs. 6 and 7 of *Kiyofuji* because they show different views of the same device. I have excerpted Fig. 6 of *Kiyofuji* below illustrating the non-conductive portion 50b and the conductive portion identified by the examiner.

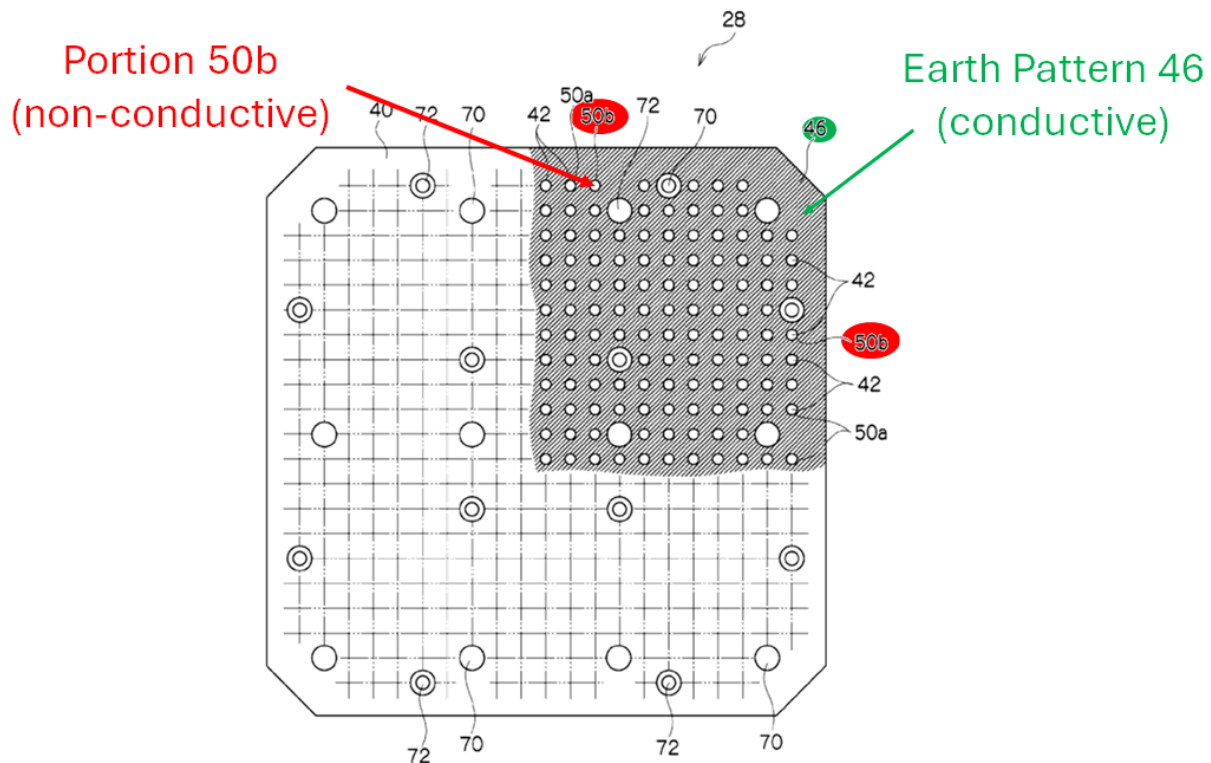


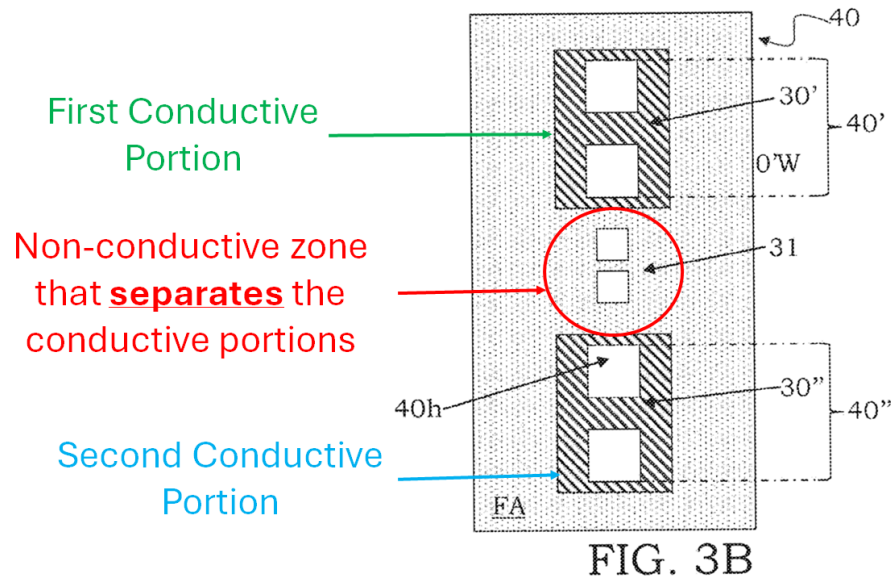
Fig. 6

Kiyofuji, Fig. 6 (annotated)

57. As illustrated in the above figure, *Kiyofuji*’s earth pattern (or conductive portion) 46, which is electrically connected to conductive film 48 (not

shown in Fig. 6), *encloses* the **non-conductive portion 50b**. Thus, the Examiner determined conductive portion 46 (or 48) is “locally interrupted” by **non-conductive portion 50b** because the conductive portion 46 (or 48) encloses **non-conductive portion 50b**. The Examiner’s interpretation is consistent with the interpretation of the phrase “locally interrupted” proposed by the Patent Owner.

58. I further note that the ’885 patent distinguishes the “locally interrupted” configuration from other configurations of the first conductive portion, which the ’885 patent describes using the term “separated.” For example, the ’885 patent explains that the second conductive portion 30’ “is physically and electrically *separated* from the first conductive portion 30’ by a non-conductive zone 31 of guide 40.” ’885 patent, col. 10, lines 8-10 (emphasis added). This configuration is illustrated in Fig. 3B of the ’885 patent. I have reproduced an annotated version of Fig. 3B of the ’885 patent below.

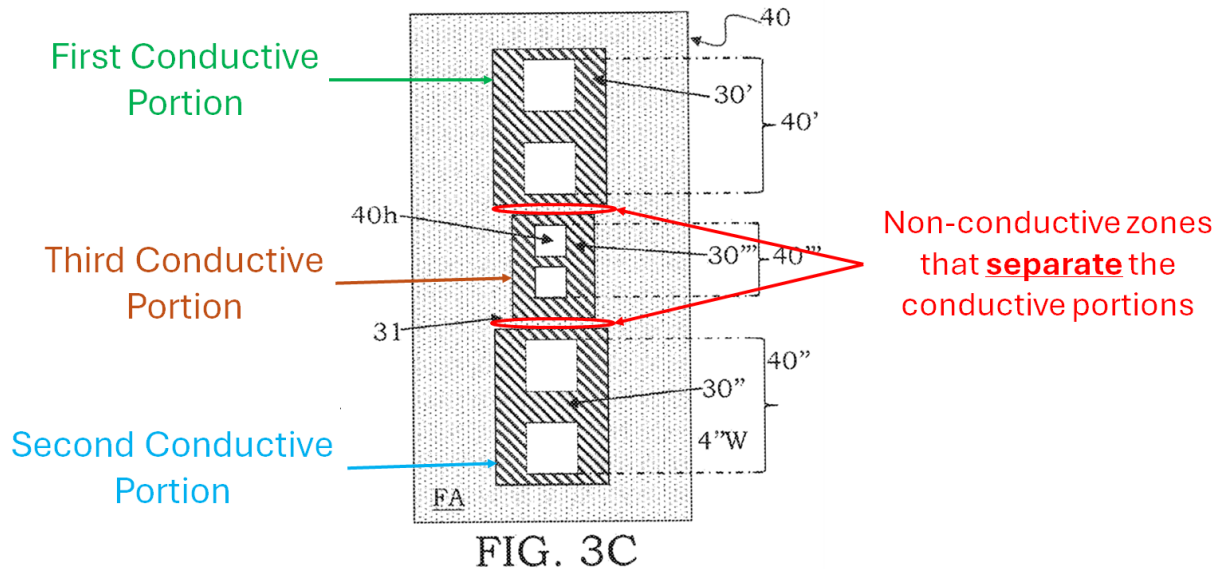


'885 patent, Fig. 3B (annotated).

59. As illustrated in the above figure, when non-conductive zone 31 separates the first conductive portion 30' from the second conductive portion 30'', the first conductive portion 30' or the second conductive portion 30'' does not enclose the non-conductive zone 31. Instead, as shown in the above figure, the non-conductive zone 31 is located between and forms a gap between adjacently located conductive portions 30' and 30''.

60. As another example, the '885 patent discloses that “in addition to the first conductive portion 30' and to the second conductive portion 30'', also the third conductive portion 30''' is formed.” '885 patent, col. 10, lines 11-13. The '885 patent explains that the third conductive portion 30''' “is physically and electrically *separated* from the conductive portions 30' and 30'' by the non-conductive zone 31 of guide 40.” '885 patent, col. 10, lines 17-19 (emphasis added). This configuration

is illustrated in Fig. 3C of the '885 patent. I have reproduced an annotated version of Fig. 3C of the '885 patent below.



'885 patent, Fig. 3C (annotated).

61. As illustrated in the above figure, when the non-conductive zone 31 separates the first conductive portion 30' or the second conductive portion 30'' from the third conductive portion 30''', the first conductive portion 30', the second conductive portion 30'', or even the third conductive portion 30''' does not enclose the non-conductive zone 31. Instead, as illustrated in the above figure, the non-conductive zone 31 is located between and *forms a gap* between adjacently located conductive portions (e.g., 30' and 30''' or 30'' and 30''').

62. In my opinion, a skilled artisan would have understood the difference, as disclosed in the '885 patent, between a non-conductive zone that separates (*forms a gap*) between conductive portions and one that “locally interrupts” (*is*

enclosed by) a conductive portion. Therefore, a skilled artisan would have interpreted the phrase “the first conductive portion is locally interrupted by at least one nonconductive zone” to mean “the first conductive portion encloses at least one non-conductive zone,” based on the disclosure of the ’885 patent and its prosecution history.

VIII. Petitioner Has Not Demonstrated that Claims 2, 3, 5, 6, 7, 12, 14, 16, 17, 18, 21, and 23 Are Unpatentable

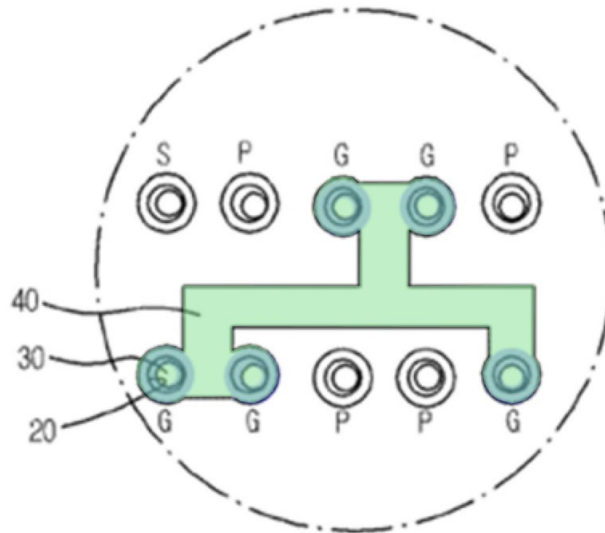
A. *Kim* does not anticipate or render obvious claim 2 (Grounds 1, 2)

63. Mr. Taber asserts that *Kim* anticipates claim 2 (Ground 1) or renders it obvious (Ground 2). Ex. 1003, ¶¶ 177-181, 221-250; *see also* Pet., 39-40, 49-54. I disagree with Mr. Taber for the reasons given below.

64. Claim 2 depends from claim 1 and recites “the first conductive portion is locally interrupted by at least one non-conductive zone.” In my opinion, *Kim* does not disclose or suggest these features of claim 2.

65. Counsel for Patent Owner have informed me that because claim 2 depends from claim 1, the first conductive portion that Mr. Taber identified in his analysis of claim 1 must also be the first conductive portion in his analysis of claim 2. In his analysis of claim 1, Mr. Taber states: “two or more of the conductive layers (20) and some or all of the conductive trace (40) formed on the upper plate (11) for connecting testing pins (30) carrying ground signals constitute

the claimed ‘first conductive portion.’” Ex. 1003, ¶ 168; *see also* Pet., 31. I have reproduced and further annotated a version of Fig. 5a provided by Mr. Taber. *See* Ex. 1003, ¶ 166.

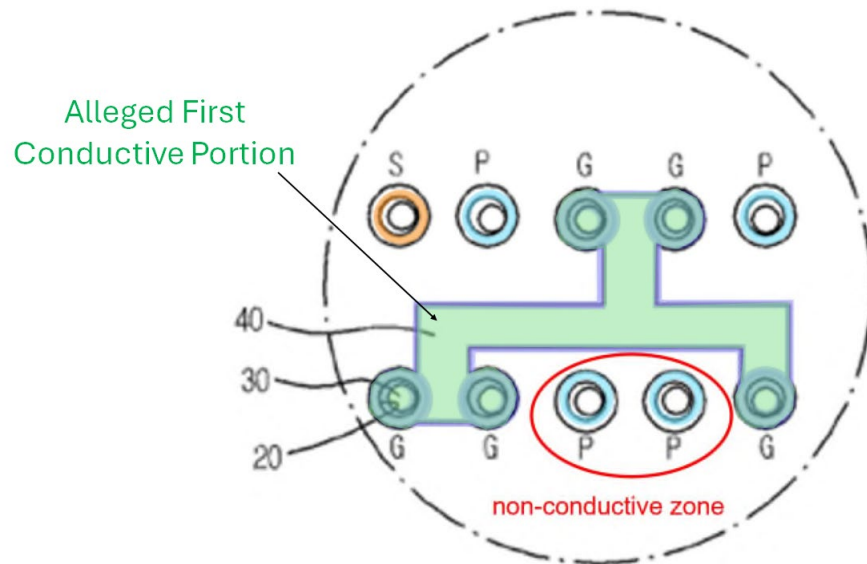


Kim, Fig. 5a (excerpted from Ex. 1003, ¶ 166 and annotated).

Thus, according to Mr. Taber, some or all of the **shaded portion** in Fig. 5a of *Kim*, above, corresponds to the claimed “**first conductive portion**.”

66. In his analysis of claim 2, Mr. Taber again refers to Fig. 5a of *Kim* and states: “On the second or bottom row of the guide holes, for example, the second and the third of the three guide holes referred to as ‘G’ for housing testing pins carrying ground signals are ‘locally interrupted’ because there is a *gap* on the guide plate between the two guide holes metallized by the ‘first conductive portion’ for housing the ground testing pins.” Ex. 1003, ¶ 180 (emphasis added); *see also* Pet.,

39. Below, I have reproduced and further annotated a version of Fig. 5a, provided by Mr. Taber. *See* Ex. 1003, ¶ 180.



Kim, Fig. 5a (excerpted from Ex. 1003, ¶ 180 and annotated).

67. I disagree with Mr. Taber that the *gap* identified in the figure above corresponds to “locally interrupted,” as recited in claim 2 of the ’885 patent. As I discussed above, a skilled artisan would have interpreted the phrase “the first conductive portion is locally interrupted by at least one non-conductive zone,” as “the first conductive portion encloses at least one non-conductive zone.” *See* Section VII.A. As shown in the above figure, however, the alleged first conductive portion identified by Mr. Taber does not enclose the alleged non-conductive zone identified by Mr. Taber. Instead, as illustrated in the above figure, the non-conductive zone identified by Mr. Taber *separates* and *forms a gap* between adjacently located portions of the alleged first conductive portion. Indeed, Mr.

Taber admits this: “the second and the third of the three guide holes referred to as ‘G’ for housing testing pins carrying ground signals are ‘locally interrupted’ because there is a *gap* on the guide plate between the two guide holes.” Ex. 1003, ¶ 180 (emphasis added); *see also* Pet., 39.

68. In my opinion, the *gap* identified by Mr. Taber is similar to the *gap* in the configurations of Figs. 3B and 3C of the ’885 patent in which a non-conductive zone *separates* and forms a *gap* between adjacently located conductive portions. *See* Section VII.A. But, as I explained above, being *separated* by a *gap* does not constitute being “*locally interrupted*.” *See* Section VII.A. Thus, the *gap* identified by Mr. Taber does not “locally interrupt” the first conductive portion of *Kim* identified by Mr. Taber. Therefore, *Kim* does not disclose or suggest “the first conductive portion is locally interrupted by at least one non-conductive zone,” as recited in claim 2 of the ’885 patent.

B. *Kim* does not anticipate or render obvious claim 14 (Grounds 1, 2)

69. Mr. Taber asserts that *Kim* anticipates claim 14 (Ground 1) or renders it obvious (Ground 2). Ex. 1003, ¶¶ 214, 218-220, 221-249; *see also* Pet., 48-53. I disagree with Mr. Taber for the reasons given below.

70. Claim 14 depends from claim 1 and recites “at least one conductive track that electrically connects the first and second conductive portions including and electrically connecting the holes of the first and second groups of the guide

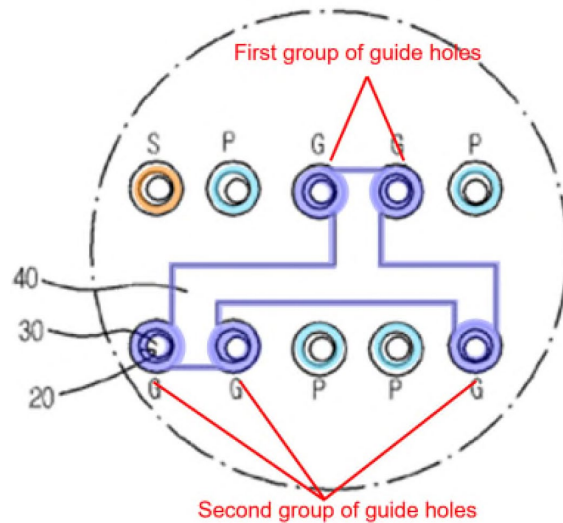
holes to each other, the contact elements included in the second group being configured to carry the first type of signal.” I have been informed by counsel for Patent Owner that because claim 14 depends from claim 1, the first and second conductive portions of claim 14 must be the same as the first and second conductive portions of claim 1.

71. Claim 1 recites “a first conductive portion that includes *and electrically connects* a first group of guide *holes* of the plurality of guide holes, *to each other.*” ’885 patent, claim 1 (emphases added). Claim 1 also recites “a second conductive portion that includes *and electrically connects the* holes of a second group of the guide holes *to each other.*” *Id.* (emphases added). Because claim 14 depends from claim 1, the “first conductive portion” of claim 14 must also electrically connect a first group of guide holes to each other. And similarly, the “second conductive portion” of claim 14 must also electrically connect a second group of guide holes to each other.

72. In his analysis of claim 14, Mr. Taber does not clearly identify what he regards as the “first conductive portion” or the “second conductive portion.” Ex. 1003, ¶¶ 219-220; *see also* Pet., 48-49. For this reason alone, Mr. Taber’s analysis is deficient and fails to demonstrate that *Kim* discloses the elements of claim 14.

73. Mr. Taber asserts: “The plurality of the guide holes constitutes a ‘first’ and ‘second’ group of guide holes, which are electrically connected by the ‘first’

and ‘second’ conductive layers housed within those guide holes, and the contact elements within those guide holes are configured to carry ‘the first type of signal’ (ground).” Ex. 1003, ¶ 219. Next, Mr. Taber asserts: “The two groups of guide holes are electrically connected by a ‘conductive track,’ which is conductive trace 40 (in whole or in part).” Ex. 1003, ¶ 219. Mr. Taber also states that “the conductive trace 40 connecting the conductive portions in and around groups of guide holes is a ‘conductive track.’” Ex. 1003, ¶ 219. Thus, in his analysis of claim 14, Mr. Taber appears to identify the conductive layers housed in the guide holes *alone* as the claimed “first conductive portion” and “second conductive portion,” because he identifies conductive trace 40 as a completely separate element, namely, “conductive track.” *See* Ex. 1003, ¶ 219; *see also* Pet., 48-49. Mr. Taber’s interpretation becomes more apparent from his annotated Fig. 5a, which I have reproduced below.



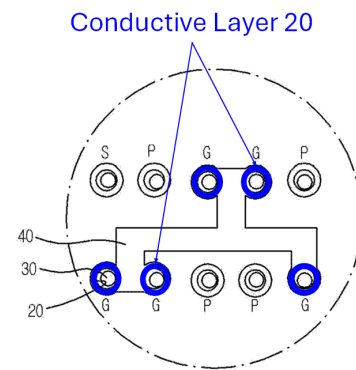
Kim, Fig. 5a (excerpted from Ex. 1003, ¶ 219).

74. I also note that Petitioner expressly states: “The conductive layers 20 at these ‘first and second groups of guide holes’ *are* the claimed ‘first’ and ‘second conductive portions’ of claim 14.” Pet., 48-49 (emphasis added). As I explain below, however, the conductive layers 20 at each guide hole do not electrically connect one guide hole to another. As a result, the conductive layers 20, identified by Mr. Taber in his analysis of claim 14, cannot constitute either the “first conductive portion” or the “second conductive portion.”

75. It is instructive to review *Kim*’s disclosures regarding its “conductive layers 20.” *Kim* discloses: “The conductive layer 20 serves to electrically connect the testing pin 30 and the conductive trace 40.” *Kim*, ¶ [0038]. *Kim* also discloses “one side of the conductive trace 40 is connected to one side of the conductive layer 20 and the other side thereof is connected to one side of other conductive

Kim below.

FIG. 5a



Kim, Fig. 5a (annotated).

In other words, a conductive layer 20 of *Kim* does not connect two or more guide

holes. It only connects the pin 30 passing through a guide hole to the walls of that guide hole.

77. But claim 14 requires that the first conductive portion must electrically connect a first group of guide holes to each other. Because conductive layers 20 of *Kim* do not connect guide holes to each other, the conductive layers 20 of *Kim* cannot constitute the first conductive portion. Similarly, claim 14 requires that the second conductive portion must electrically connect a second group of guide holes to each other. Again, because conductive layers 20 of *Kim* do not connect guide holes to each other, the conductive layers 20 of *Kim* cannot constitute the second conductive portion. Therefore, Mr. Taber and Petitioner fail to demonstrate that *Kim* discloses every element of claim 14.

78. Furthermore, Mr. Taber takes inconsistent positions regarding the first and second conductive portions in his analysis of claims 1 and 14. As I discussed above, because claim 14 depends from claim 1, the first conductive portion of claim 14 must be the same as the first conductive portion of claim 1.

79. In his analysis of claim 1, Mr. Taber asserts that “*two or more* of the conductive layers (20) and *some or all* of the conductive trace (40) formed on the upper plate (11) for connecting testing pins (30) carrying ground signals constitute the claimed ‘first conductive portion.’” Ex. 1003, ¶ 168; *see also* Pet., 31.

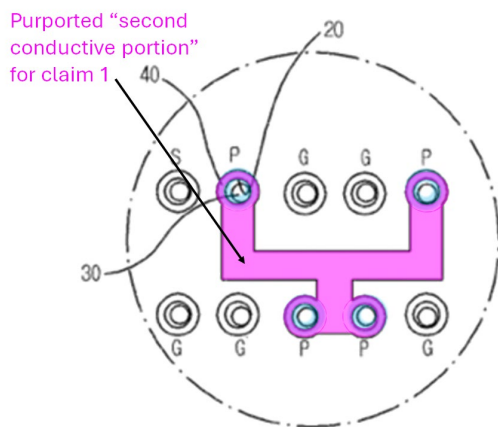
However, as I explained above, when discussing claim 14, Mr. Taber and the

Petitioner assert that some conductive layers 20 *alone* constitute the claimed “first conductive portion.” Ex. 1003, ¶ 219; *see also* Pet., 48-49. In my opinion, because Mr. Taber’s identification of the “first conductive portion” for claim 14 is different from that for claim 1, Mr. Taber fails to demonstrate that *Kim* discloses every element of claim 14.

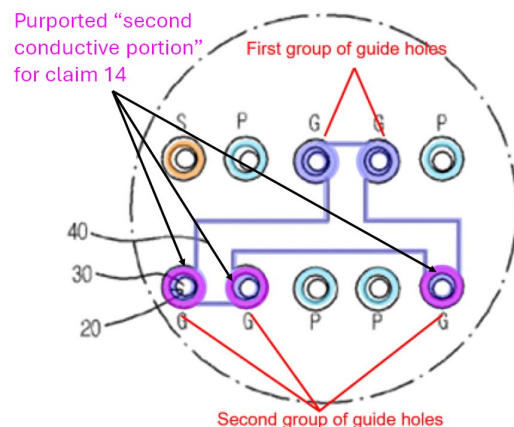
80. Similarly, as I discussed above, because claim 14 depends from claim 1, the second conductive portion of claim 14 must be the same as the second conductive portion of claim 1. However, Mr. Taber identifies two completely different elements of *Kim* as constituting the second conductive portion in his analysis of claims 1 and 14.

81. For claim 1, Mr. Taber asserts that “Kim describes and illustrates in Fig. 5b that testing pins (30) carrying power signals are electrically connected via the conductive layers (20) and conductive trace (40).” Ex. 1003, ¶ 169; *see also* Pet., 36. But, when analyzing claim 14, Mr. Taber again asserts that *some* conductive layers 20 *alone* constitute the claimed “second conductive portion” Ex. 1003, ¶ 219; *see also* Pet. at 48-49. In my opinion, because Mr. Taber’s identification of the “second conductive portion” for claim 14 is different from that for claim 1, Mr. Taber fails to demonstrate that *Kim* discloses every element of claim 14.

82. Mr. Taber's positions include additional inconsistencies. For example, when analyzing claim 1, Mr. Taber identifies conductive layers 20 and conductive trace 40 on a *lower* surface of *Kim*'s guide plate as the alleged second conductive portion. Ex. 1003, ¶ 169; *see also* Pet., 36. But when analyzing claim 14, Mr. Taber identifies conductive layers 20, *alone*, on the *upper* surface of *Kim*'s guide plate as the alleged second conductive portion. Ex. 1003, ¶ 219; *see also* Pet., 48-49. Below, I have reproduced Figs. 5a and 5b of *Kim* as illustrated in Mr. Taber's declaration and further annotated those figures to illustrate Mr. Taber's inconsistent identification of the second conductive portion for claims 1 and 14.



Ex. 1003, ¶ 169 (claim [1d]) (*Kim*, Fig. 5b annotated).



Ex. 1003, ¶ 219 (claim 14) (*Kim*, Fig. 5a annotated).

83. But, because claim 14 depends from claim 1, the same features of *Kim*'s device must correspond to the "second conductive portion" recited in both claims 1 and 14. Specifically, the second conductive portion cannot be on the lower surface of *Kim*'s guide plate 11 for claim 1, while simultaneously being on

the upper surface of *Kim*'s guide plate 11 for claim 14. In my opinion, because Mr. Taber identified different portions of *Kim*, on different surfaces of *Kim*'s guide plate, as the "second conductive portion" for claims 1 and 14, he fails to demonstrate that *Kim* discloses every element of claim 14.

84. I understand that in its decision to institute this trial, the Board stated that *Kim* contemplates "the potential for more than one electrically connected group on one surface of a guide plate." Institution Decision, 26. Even assuming this to be true, in my opinion, there is no disclosure in *Kim* that any such electrically connected group was also connected to another such electrically connected group as required by claim 14 of the '885 patent.

85. Specifically, *Kim* discloses that "the conductive layers 20, with which the testing pins 30 of transmitting the same signal are contacted, and the conductive traces for connecting them are set to a plurality of groups and each group is formed at the upper surface and the lower surface of the upper plate 11 respectively." *Kim*, ¶ [0050]. In my opinion, a skilled artisan would have understood this to disclose that there may be more than one group of electrically connected testing pins 30 on one or both of the upper and lower surfaces of plate 11. For example, there could be a Group 1 of electrically connected testing pins and a Group 2 of electrically connected testing pins. A skilled artisan would have recognized that each of those groups (e.g., Group 1 and Group 2) of

electrically connected testing pins 30 would be similar to the illustration in Fig. 5a of *Kim* showing a group of testing pins 30 connected to each other. In my opinion, however, nothing in *Kim* discloses connecting two or more such groups of electrically connected testing pins 30 to each other, as required by claim 14 of the '885 patent. That is, nothing in *Kim* discloses connecting Group 1 to Group 2, and therefore does not disclose or suggest "at least one conductive track that electrically connects the first and second conductive portions," as recited in claim 14 of the '885 patent.

86. In my opinion, therefore, Mr. Taber's inconsistent positions fail to demonstrate that *Kim* discloses or suggests all the features of claim 14. Furthermore, there is no disclosure in *Kim* regarding connecting more than one electrically connected group of testing pins to each other as required by claim 14. Therefore, *Kim* does not disclose or suggest all the elements of claim 14 of the '885 patent.

C. *Kim* does not render obvious claim 7 (Ground 2)

87. Claim 7 of the '885 patent recites "the at least one guide includes at least one third conductive portion that includes and electrically connects a third group of the guide holes to each other and house third contact elements configured to carry input/output signals between the device under test and a test equipment."

For the reasons explained below, *Kim* does not disclose or suggest at least these elements of claim 7.

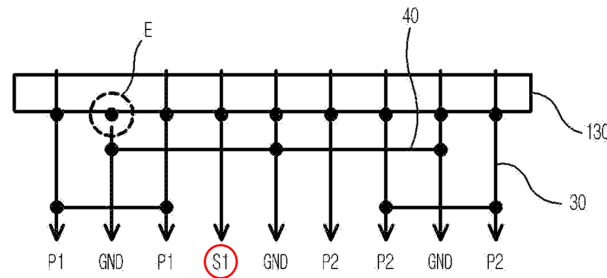
88. In his obviousness analysis for claim 7, Mr. Taber cites ¶¶[0019], [0025], [0032], [0042], [0044], [0045], stating: “*Without limiting as specific type of signal*, Kim explains that it applies to testing pins transmitting *identical* or the *same* signals” and that “pins carrying the same signal can be grouped together via a conductive trace (conductive layer), where the grouping of input/output signals also would be possible.” Ex. 1003, ¶¶ 262-263 (emphases added); *see also* Pet., 57. I disagree with Mr. Taber’s analysis because the portions of *Kim* cited by Mr. Taber do not disclose or suggest connecting pins carrying *input/output signals* to each other. I address each of the paragraphs cited by Mr. Taber below.

89. In particular, in ¶ [0019], *Kim* discloses that “the conductive trace is electrically connected between the conductive layers with which the testing pins of transmitting the same signal are contacted.” *Kim*, ¶[0019]. But in the very next paragraph, *Kim* explains that “the conductive trace is electrically connected between the conductive layers with which the testing pins for *ground* are contacted.” *Kim*, ¶ [0020] (emphasis added). In my opinion, a skilled artisan would have understood ¶¶ [0019]-[0020] of *Kim* as disclosing that testing pins transmitting the same signal, such as a ground signal can be electrically connected.

90. Similarly, *Kim* specifies a section heading “1. Connection Between the Conductive Layers with which the Testing Pin of Transmitting the Same Signal is Contacted.” *Kim*, ¶ [0042]. Within that section, *Kim* discloses “the plurality of the conductive layers 20, with which the testing pin for *ground* is contacted, can be connected to each other.” *Kim*, ¶ [0044] (emphasis added). *Kim* begins ¶ [0045] by saying: “As described above,” referring to previous ¶ [0044] and indicating that “the plurality of testing pin 30 of transmitting the same signal” in ¶ [0045] also refers to the testing pins for ground. A skilled artisan reading ¶¶ [0042]-[0045] of *Kim* would have further understood *Kim* as disclosing that testing pins carrying the same type of signal, such as a ground signal, can be connected to each other. In my opinion, a skilled artisan would not have read *Kim* as disclosing electrically connecting input/output pins to each other. I note that Mr. Taber did not identify a single description or figure in *Kim* that shows input/output pins connected to each other.

91. Contrary to Mr. Taber’s analysis, *Kim*’s discussion of input/output pins and figures demonstrates that *Kim* does not contemplate connecting these pins to each other. For example, Fig. 3 of *Kim*, (referred to in *Kim*, ¶¶ [0025], [0032] and cited by Mr. Taber, Ex. 1003, ¶ 262) includes a single pin labeled “S1” that is not depicted as being connected to any other pin. I have reproduced an annotated version of Fig. 3 of *Kim* below.

FIG. 3

*Kim*, Fig. 3 (annotated).

As illustrated in the above figure, the single pin labeled “S1” is not connected to any other pin.

92. As another example, I have reproduced below annotated versions of Figs. 5a and 5b of *Kim*, also referred to by Mr. Taber. Ex. 1003, ¶ 262. As illustrated in these figures, the pins labeled “S” in Figs. 5a and 5b of *Kim*, which Mr. Taber alleges refer to a “signal,” (Ex. 1003, ¶ 263; *see also* Pet., 57) are not connected to any other pin.

FIG. 5a

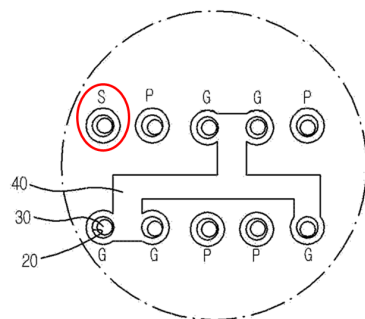
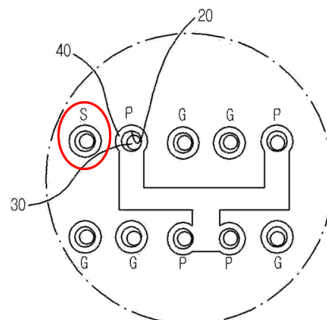


FIG. 5b

*Kim*, Figs. 5a and 5b (annotated).

93. In my opinion, a skilled artisan reading these express disclosures of *Kim* would have understood that while *Kim* discloses connecting testing pins carrying a *ground* signal, nothing in *Kim* discloses or suggests connecting testing pins carrying *input/output* signals.

94. Furthermore, *Kim* discloses that “the conductive trace is electrically connected between the conductive layers with which the testing pins of transmitting the *same* signal are contacted.” *Kim*, ¶ [0019]. Mr. Taber also refers to “pins transmitting *identical* or the *same* signals.” Ex. 1003, ¶ 262. A skilled artisan would have understood that the signals carried by any two input/output pins of *Kim* are unlikely to be the “same” let alone being “identical.”

95. The purpose of *Kim*’s semiconductor testing apparatus is to test electrical characteristics of a chip. During such tests, the test equipment supplies power to the chip through the pins carrying power signals and then runs one or more test programs to activate various pins associated with input/output signals. As Mr. Taber explains: “Through ‘instructions’ from the test program, the tester stimulates the input signal I/Os and records the response from the output I/Os (bi-directional I/Os perform either function as required by the test).” Ex. 1003, ¶ 80. A skilled artisan would have understood that different input/output pins in *Kim*’s semiconductor testing apparatus would carry different signals (not *same* or *identical* signals), depending on the test program. *Anritsu*, 2-8. Thus, two or more

pins associated with input/output signals are likely to carry different signals when stimulated with a test program. *Id.*

96. In my opinion, a skilled artisan would have understood that the behavior of the pins associated with input/output signals is different from that of pins associated with power and ground signals. This is because typically the power and ground pins all carry the same power or ground signals, respectively. *See Lim*, col. 2, lines 46-56. Thus, while a skilled artisan would have found that it makes sense to connect pins carrying the same power signals to each other, or pins carrying the same ground signal to each other, a skilled artisan would not have concluded from *Kim* that it would have been obvious to connect pins carrying different input/output signals to each other. I note that Mr. Taber agrees with this assessment because he states: “Typically, signal I/Os operate individually, so two or more are not connected together.” Ex. 1003, ¶ 80.

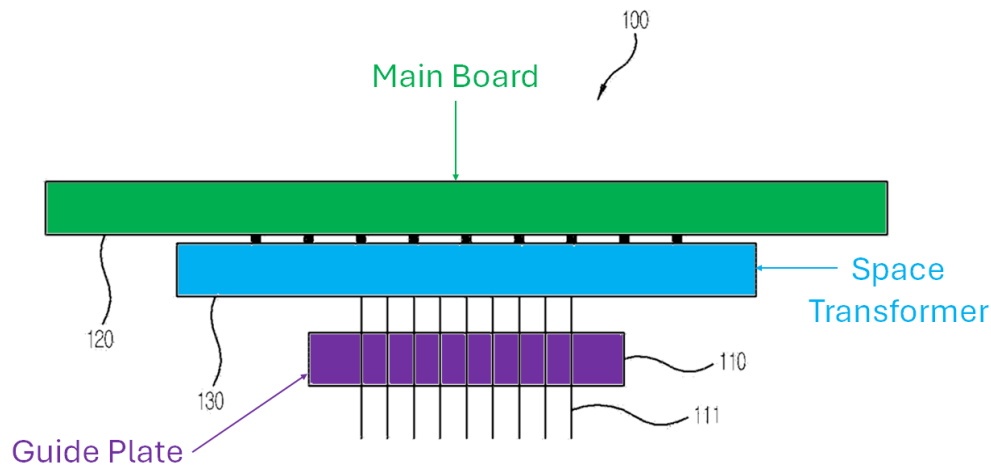
97. Regardless, Mr. Taber asserts that a “skilled artisan would have had a reason to electrically connect these signal testing pins in *Kim* to improve performance in fulfilling certain testing requirements, such as with loop-back testing.” Ex. 1003, ¶ 265. Notably, Mr. Taber does not explain which input/output signal pins would be connected for such testing, or even why connecting signal testing pins would improve performance during such loop-back testing. Ex. 1003, ¶ 265.

98. Mr. Taber also asserts that “[e]lectrically connecting two or more of the input/output testing pins” would “provide a semiconductor testing apparatus in that a signal transduction length becomes short and an impedance is decreased, so that it can remarkably improve the high frequency performance.” Ex. 1003, ¶ 265; *see also* Pet., 58. I disagree with the purported benefits of connecting signal pins touted by Mr. Taber because the purported benefits of reduced length and reduced impedance are not attributable to connecting pins carrying input/output signals together. Rather, as I explain in detail below, those benefits would accrue by connecting pins through an external wire to the main board or test equipment, thereby bypassing the pins and/or a space transformer, as *Kim* describes.

99. To understand what contributes to the impedance in *Kim*’s testing apparatus, it is instructive to review *Kim*’s description of a conventional probe card. *Kim* discloses that a conventional probe card includes a guide plate with testing pins contacting a chip, a main board separated from the guide plate and a space transformer that helps to increase the narrow pitch of the pins on the guide plate to a wide pitch of the connections on the main board. *Kim*, ¶ [0010]. I have reproduced an annotated version of Fig. 1 of *Kim* below to illustrate these features.

FIG. 1

Prior Art

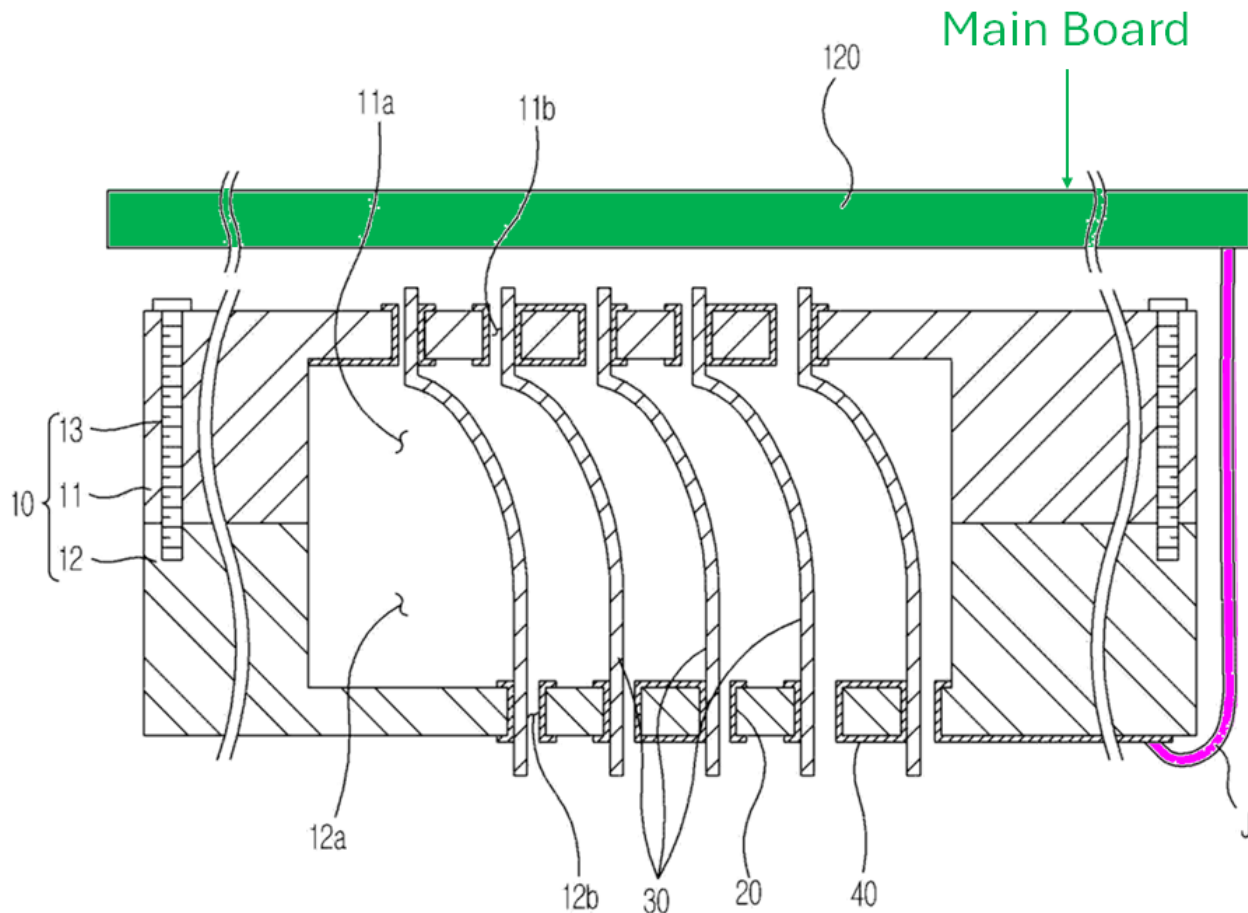
*Kim, Fig. 1 (annotated).*

100. In conventional configurations, signals from the test equipment are supplied through the wiring in the **main board 120**. Those signals then travel through the wiring patterns in the **space transformer 130**, and then through the pins 111 to the chip under test, located at the bottom of the pins 111. Generally, impedance is an electrical property that describes the ability to conduct electrical AC current for a given AC voltage. Ex. 2003, 6. The length of wiring in the **main board 120**, the lengths of wiring patterns in the **space transformer 130**, and the length of pins 111 all contribute to the impedance. In particular, the impedance can be large because of the long length of the wiring in the **main board 120**, wiring in the **space transformer 130**, and pins 111 through which the signals must travel to reach the chip under test.

101. A skilled artisan would have understood that impedance includes electrical resistance, inductance, and capacitance. Ex. 2003, 6. Consequently, impedance will increase with increased length of wiring and performance would be a function of frequency. *Ott*, 208-214. A skilled artisan would have understood that the long path length including the pins and the wiring in the **main board 120** and **space transformer 130** would have resulted in a higher impedance. A skilled artisan would have also understood that high impedance of this electrical path would affect the high frequency performance. *Schmitt*, 146.

102. *Kim* discloses directly connecting conductive trace 40 to **main board 120** through an external wire. This **external wire J** is illustrated in Fig. 6 of *Kim*, which I have reproduced below.

FIG. 6

*Kim*, Fig. 6 (annotated).

As illustrated in the above figure, **wire J** would bypass the length of the wiring in the **space transformer 130**, and the lengths of pins 111. Because **wire J** provides a more conductive path than the wiring in **space transformer 130** as connected to pins 111, the impedance of **wire J** would be smaller than the impedance of the signal path through the wiring in **space transformer 130** and the length of pins 111. The lower impedance provided by **wire J** would also improve high frequency performance. This is what *Kim* discloses.

103. Specifically, *Kim* states: “Another object of the invention is to provide a semiconductor testing apparatus in that *a signal transduction length becomes short and an impedance is decreased*, so that it can remarkably improve the high frequency performance.” *Kim*, ¶ [0016] (emphasis added). *Kim* also discloses “since the conductive trace 40 according to one embodiment of the present invention *can be directly connected to the main board without the separate space transformer* on the external area W, which is deviated from the testing area T, it can remarkably improve the workability thereof.” *Kim*, ¶ [0048] (emphasis added). *Kim* explains that “since the signal transduction length becomes short and the impedance is decreased, it can remarkably improve the high frequency performance.” *Kim*, ¶[0048]. A skilled artisan would have understood from these paragraphs that the impedance provided by **wire J** would be lower than the impedance of the wiring in the space transformer and the pins. A skilled artisan would have also understood that *Kim*’s disclosures say nothing at all about reduction in impedance or improved high frequency performance *due to electrical connection of input/output signals*.

104. *Kim* also discloses “after the testing pins of transmitting the same signal are electrically connected to each other through a lower surface of the lower plate of the guide plate, *the conductive trace 40 is electrically connected to the main board* through the external area deviated from the testing area, *so that the*

signal transduction route is minimized through the testing pin and the impedance is decreased, thereby remarkably improving the high frequency performance.”

Kim, ¶ [0064]. Although *Kim* mentions electrically connecting testing pins transmitting the same signal, here again, *Kim* discloses that impedance is reduced and high frequency performance improves because connecting the conductive portions to the main board bypasses the space transformer and the pins passing through the guide plate. Furthermore, high frequency performance is improved because the signals can travel through the wire J instead of travelling through the combination of the space transformer and the pins.

105. In my opinion, the benefits of a minimized signal path, reduced impedance, and improved frequency performance disclosed in *Kim* are a result of bypassing the full length of pins and the space transformer, not a result of electrically connecting pins carrying input/output signals. More importantly, a skilled artisan would not have understood *Kim* as disclosing any benefits of connecting pins carrying input/output signals to each other.

106. In my opinion, therefore, Mr. Taber fails to demonstrate that *Kim* discloses or suggests connecting testing pins carrying input/output signals. Furthermore, Mr. Taber fails to show that a skilled artisan would have been motivated to connect testing pins carrying input/output signals and, therefore, fails

to establish that the skilled artisan would have found claim 7 of the '885 patent obvious in view of *Kim*.

D. The combination of *Kim* and *Schmid* does not render obvious claim 18 (Ground 3)

107. Claim 18 depends from claim 16 and further includes recitations similar to those of claim 7 of the '885 patent. Mr. Taber relied on the combination of *Kim* and *Schmid* for the recitations of claim 16. Ex. 1003, ¶¶ 313-315; *see also* Ex. 1003, ¶¶ 280-298; *see also* Pet., 59-66. But Mr. Taber did not rely on *Schmid* for the additional limitations of claim 18, relying instead on his analysis based on *Kim*. Ex. 1003, ¶ 319 (referring to analysis for claim 7); *see also* Ex. 1003, ¶¶ 261-266; *see also* Pet., 57-58, 67. As I discussed above, *Kim* does not disclose or suggest the recitations of claim 7, which are similar to the additional recitations in claim 18. Section VIII.C. Therefore, for reasons similar to those I discussed for claim 7, the combination of *Kim* and *Schmid* fails to disclose or suggest all the elements of claim 18 of the '885 patent. Section VIII.C.

E. The combination of *Kim* and *Schmid* does not render obvious claims 6 and 23 (Ground 3)

108. Claim 6 of the '885 patent recites “the first and second conductive portions being formed on a same face of one of the upper, intermediate and lower guides and being physically and electrically separated from each other by at least one non-conductive zone.” Claim 23 of the '885 patent includes similar limitations.

Mr. Taber relies only on *Kim* for these recitations. Ex. 1003, ¶¶ 303-311, 326-327; *see also* Pet., 65-67. I disagree because as explained below, *Kim* does not disclose forming conductive portions carrying power and ground signals on a same face of a guide plate.

109. In fact, *Kim* discourages forming conductive portions carrying power and ground signals on a same face of a guide plate. Specifically, *Kim* discloses:

For example, the plurality of the conductive layers 20, with which the testing pins 30 of transmitting the same signal are contacted, and the conductive traces 40 for connecting them are formed at the upper surface of the upper plate 11 as shown in FIG. 5a and the plurality of the conductive layers 20, with which the testing pins 30 for ground are contacted, and the conductive traces 40 for connecting them are formed at the lower surface of the upper plate 11 as shown in FIG. 5 b, *so that the testing pins 30 of transmitting the same signal can be easily connected without interfering with the testing pin 30 of transmitting the other signal.*

Kim, ¶ [0051] (emphasis added).

110. As made clear by the above excerpt, *Kim* stresses the importance of placing conductive portions connecting pins carrying different types of signals on different faces of the guide plate to prevent interfering between the pins carrying the different types of signals. In my opinion, a skilled artisan reading *Kim* would

not have found it obvious to locate the first conductive portion carrying ground signals and the second conductive portion carrying power signals on the same face of a guide plate.

111. Mr. Taber does not cite anything in *Kim* that specifically discloses forming conductive portions carrying power and ground signals on the same face of a guide plate. Ex. 1003, ¶¶ 303-310; *see also* Pet., 65-67. Instead, Mr. Taber selects disparate portions of *Kim* (e.g., *Kim*, ¶¶ [0050] and [0052]) and Exhibit 1005¹ and misrepresents those snippets to argue that *Kim* discloses forming conductive portions carrying power and ground signals on the same face of a guide plate. Ex. 1003, ¶¶ 303-310; *see also* Pet., 65-67. I disagree with his interpretation of the disclosures he cites.

112. In my opinion, ¶¶ [0050] and [0052] of *Kim* (and corresponding ¶¶ [0043] and [0045] of Ex. 1005), would not have been interpreted by a skilled artisan as disclosing or suggesting forming conductive portions carrying power and ground signals on the same face of a guide plate. I will address each of these portions of *Kim* and Ex. 1005 below.

113. I have excerpted ¶ [0050] of *Kim* and corresponding ¶ [0043] of Ex. 1005 below.

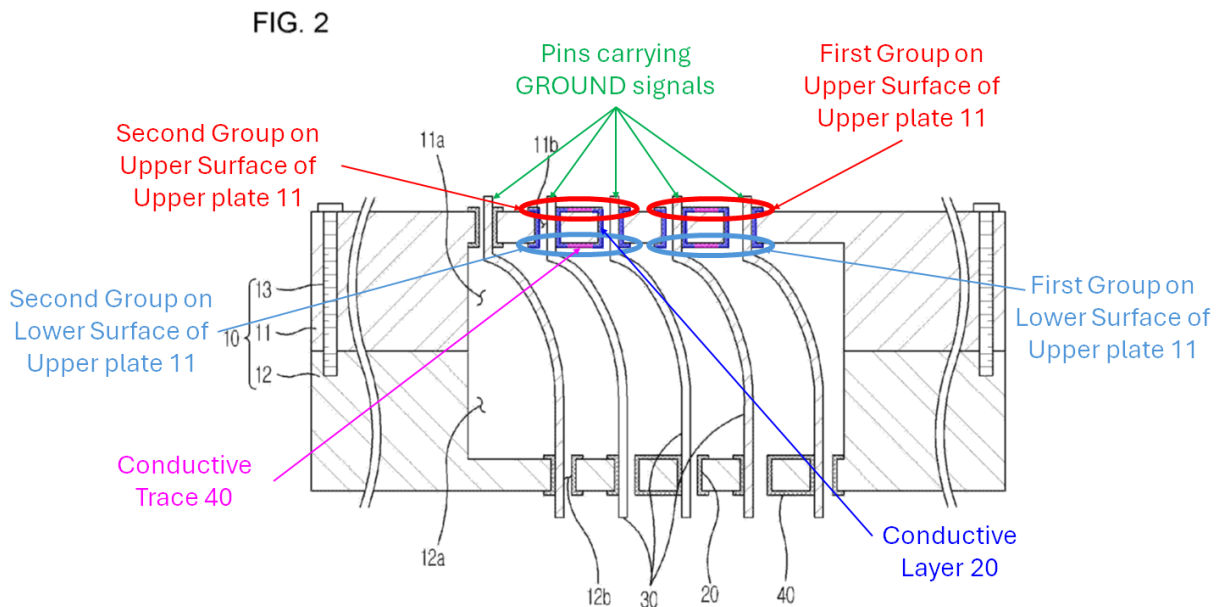
¹ Ex. 1005 is Petitioner's English language translation of Korean Patent Application No. 10-2014-0004576, to which *Kim* claims priority.

<i>Kim, ¶ [0050] (emphasis added)</i>	<i>Ex. 1005, ¶ [0043] (emphasis added)</i>
In the meantime, in one embodiment of the present invention, <i>the plurality of the conductive layers 20, with which the testing pins 30 of transmitting the same signal are contacted, and the conductive traces for connecting them are set to a plurality of groups</i> and each group is formed at the upper surface and the lower surface of the upper plate 11 respectively, so that the testing pins 30 of transmitting the same signal in the narrow testing area can be easily connected.	In one embodiment of the present invention, <i>the test pins (39) transmitting identical signals can be conveniently connected in a confined testing area by grouping a plurality of conductive layers (20) in contact with the test pins (30) transmitting identical signals, along with the trace connecting such conductive layers, and forming each group on the upper surface and the lower surface of the upper plate (11), respectively.</i>

114. In my opinion, a skilled artisan would have understood the italicized portions of these paragraphs as disclosing that conductive layers 20, testing pins 30 carrying the same or identical signal in contact with those conductive layers 20, and conductive traces 40 connecting them could be divided into a plurality of groups. Thus, testing pins 30 carrying identical signals (e.g., ground signals) could be divided into a plurality of groups and within each such group, conductive traces 40 would connect the conductive layers 20 in contact with the testing pins 30 in that particular group. Further, a person of ordinary skill would have understood from these paragraphs that each such group carrying the same signal (e.g., ground signal) could be formed on both the upper surface and on the lower surface of upper plate 11.

115. For example, testing pins 30 carrying ground signals could be divided into two groups (e.g., First Group and Second Group) and in each of those two

groups conductive traces 40 would connect the conductive layers 20 in contact with the testing pins 30. Each of the two groups (e.g., First Group and Second Group) could be formed both on the upper surface and on the lower surface of upper plate 11. *Kim* illustrates precisely this configuration. I have reproduced an annotated version of Fig. 2 of *Kim* below, to show where two groups of pins (e.g., First Group and Second Group) are formed on the upper surface of upper plate 11 and also on the lower surface of upper plate 11. Furthermore, the pins in each of the two groups are connected to each other via **conductive traces 40** and **conductive layers 20**.



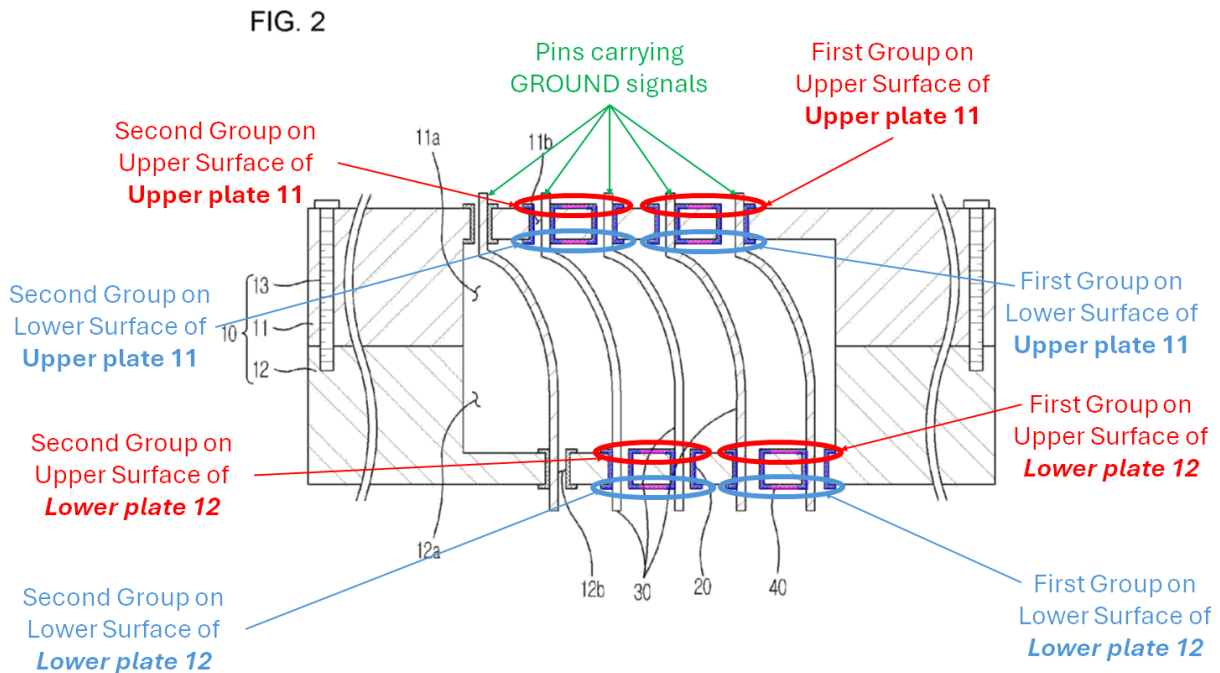
Kim, Fig. 2 (annotated).

116. I have also excerpted ¶ [0052] of *Kim* and corresponding ¶ [0045] of Ex. 1005 below. I note that these portions refer to the same groups discussed above.

<i>Kim</i>, ¶ [0052] (emphasis added)	Ex. 1005, ¶ [0045] (emphasis added)
Also, in the drawings, each <i>group</i> is formed at only the upper surface and the lower surface of the upper plate 11. However, the present invention is limited to the position of the groups. That is, each <i>group</i> can be formed at the upper surface and the lower surface of both upper and lower plates 11 and 12 according to the number of the <i>groups</i> . Also, at least one electrical connecting <i>group</i> can be formed on one surface thereof.	Furthermore, in one example, it has been described that each <i>group</i> is distinguished and formed only on the upper surface and lower surface of the upper plate (11). However, the present invention is not limited to forming each <i>group</i> only on the upper surface and lower surface of the upper plate (11). Depending on the number of <i>groups</i> , it is possible to form more than one electrically connected <i>group</i> on a single surface, not to mention using both the upper surface and lower surface of the upper plate (11), as well as the upper surface and lower surface of the lower plate (12).

117. In my opinion, a person of ordinary skill in the art would have understood these paragraphs as disclosing that each of the plurality of groups (e.g., First Group and Second Group, in my example above) could be formed on the upper and lower surfaces, respectively, of upper plate 11, and also on upper and lower surfaces, respectively, of lower plate 12. In other words, the First Group out of the two groups in my example could be formed on the upper and lower faces of the upper plate and also on the upper and lower faces of the lower plate. Similarly, the Second Group out of the two groups in my example could be formed on the

upper and lower faces of the upper plate and also on the upper and lower faces of the lower plate. As I explained above, each of those two groups (e.g., First Group and Second Group) carries the same or identical signal (e.g., ground signal). *Kim* illustrates this configuration as well. For example, I have reproduced and annotated version of Fig. 2 of *Kim*, below, illustrating this configuration.



118. As illustrated in the above figure, the First Group of pins carrying the same or identical signal (e.g., ground signal) is formed on the upper and lower surfaces of each of upper plate 11 and lower plate 12. Similarly, the Second Group of pins carrying the same or identical signal (e.g., ground signal) is formed on the upper and lower surfaces of each of upper plate 11 and lower plate 12.

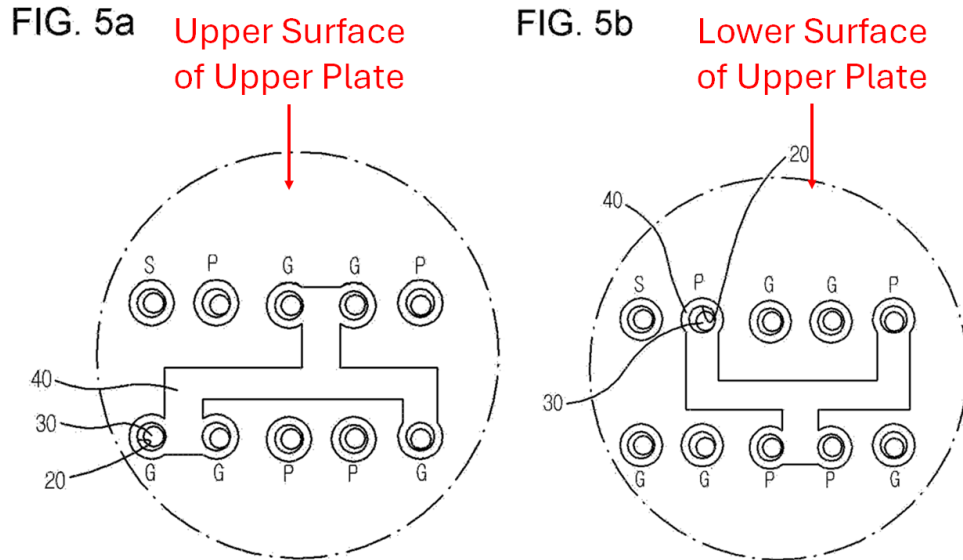
Furthermore, the pins in each of the groups are connected to each other via **conductive traces 40** and **conductive layers 20**.

119. Ex. 1005, ¶ [0045] also states: “Depending on the number of groups, it is possible to form more than one electrically connected group on a single surface, not to mention using both the upper surface and lower surface of the upper plate (11), as well as the upper surface and lower surface of the lower plate (12).” Ex. 1005, ¶ [0045] (partially quoted by Mr. Taber, Ex. 1003, ¶ 308). In my opinion, a skilled artisan would have understood this sentence to mean that if there were too many groups carrying the same signal (e.g., ground signal), both surfaces of one or both of upper and lower plates 11 and 12 could be used to accommodate those groups as shown in the above figure. Conversely, if there were fewer groups carrying the same signal (e.g., ground signal), all of those groups could be accommodated on just the upper surface or just the lower surface of just the upper plate 11 or just the lower plate 12.

120. I note that neither *Kim* nor Ex. 1005 expressly discloses or illustrates forming conductive portions connecting groups of pins carrying ground signals and conductive portions connecting groups of pins carrying power signals on the same surface of either the upper or lower plates 11 and 12 of *Kim*. In my opinion, this makes sense because as *Kim* discloses, forming conductive portions connecting groups of pins carrying ground signals and conductive portions connecting groups

of pins carrying power signals on different surfaces would prevent interference between the ground and power signals. *Kim*, ¶ [0051].

121. Claim 6 also recites that the first and second conductive portions are “physically and electrically separated from each other by at least one non-conductive zone.” In his analysis for this claim limitation, Mr. Taber points to Figs. 5a and 5b of *Kim* and asserts that these figures “show the two conductive portions physically and electrically separated by the guide plate.” Ex. 1003, ¶ 311. As I have explained, however, Figs. 5a and 5b of *Kim* show the first conductive portion and the second conductive portion formed on different surfaces of upper plate 11. For example, *Kim* states: “Fig. 5a is a drawing showing an *upper surface* of upper plate.” *Kim*, ¶ [0027] (emphasis added). Similarly, *Kim* states: “Fig. 5b is a drawing showing a *lower surface* of an upper plate.” *Kim*, ¶ [0028] (emphasis added). I have excerpted these figures below.



Kim, Figs. 5a and 5b (annotated).

122. As seen in the above figures, Figs. 5a and 5b do not show the first conductive portion and the second conductive portion being *formed on the same face* of upper plate 11 and being physically and electrically separated by a non-conductive zone, as recited in claim 14.

123. Mr. Taber also cites to ¶ [0062] of *Kim* and states that “Kim teaches that ‘the testing pins 30 for signal or the testing pins 30 for power are insulated with the testing pins 30 for ground.’ Ex. 1003, ¶ 311. Here again, Mr. Taber misrepresents *Kim*’s disclosure.

124. Specifically, ¶ [0062] of *Kim* refers to the embodiment of Fig. 7, in which “the conductive materials are deposited on the entire surface of the guide plate 10 and then, the conductive materials are selectively removed from the surface of the guide plate 10 through the machining.” *Kim*, ¶ [0061]. *Kim* explains

“the conductive materials formed at the corner of the guide plate corresponding to the guide hole, into which the testing pins 30 except for the testing pins 30 for ground are inserted, that is the entrance of the guide hole 11a is removed through the counter sink or the counter bore C.” *Kim*, ¶ [0062]. A skilled artisan would have understood this embodiment as disclosing forming one single conductive portion on one face of the guide plate to connect ground pins while not connecting pins carrying a signal different from ground using a conducting layer. In this embodiment, there is only one conductive portion on a face of the guide plate. And although non-conductive regions are formed to electrically isolate certain pins in this embodiment, the non-conductive portion does not physically and electrically separate a conductive portion connecting groups of pins carrying ground signals from a conductive portion carrying power signals on the same surface of either the upper or lower plates 11 and 12 of *Kim*.

125. In my opinion, therefore, Mr. Taber fails to demonstrate that *Kim* discloses or suggests “the first and second conductive portions being formed on a same face of one of the upper, intermediate and lower guides and being physically and electrically separated from each other by at least one non-conductive zone,” as recited in claims 6 and 23. Instead, a skilled artisan would have understood that *Kim* teaches exactly the opposite. See *Kim*, ¶[0051]. Mr. Taber does not rely on *Schmid* for the above-identified elements of claims 6 and 23. Ex. 1003, ¶¶ 299-312,

326-327; *see also* Pet., 65-67. Therefore, in my opinion, the combination of *Kim* and *Schmid* does not render obvious claims 6 and 23 of the '885 patent.

F. The combination of *Kim* and *Schmid* does not render obvious claims 5, 16, and 17 (Ground 3)

126. Claim 5 of the '885 patent recites “the first and second conductive portions being formed on respective faces of the upper, intermediate *and* lower guides” (emphasis added). Claim 16 (and claim 17, which depends therefrom) includes similar recitations. Thus, claims 5, 16, and 17 require the first conductive portion and the second conductive portion to be formed on each of the upper guide, intermediate guide, and the lower guide. In my opinion, the combination of *Kim* and *Schmid* does not disclose or suggest these features.

127. Mr. Taber asserts:

A POSITA would have understood that the combination of *Kim* teaching two physically and electrically separated groups of conductive layers (20) and conductive trace (40) in contact with two physically and electrically separated groups of testing pins (30) carrying two different types of signals (*e.g.*, ground and power signals) on the upper and lower guides plates, with *Schmid* teaching three separate guide panels (17, 19, 21) spaced apart from one another with feed through openings (23), would result in conductive portions being formed on respective faces of the upper, intermediate and lower guides - the subject matter in claim 5d.

Ex. 1003, ¶ 297; *see also* Pet., 64-65. But Mr. Taber provides no reasons or bases for why a skilled artisan *would have formed* the first conductive portion and the second conductive portion on each of the three guide plates as required by claims 5, 16, and 17. Ex. 1003, ¶ 297. Mr. Taber also does not explain what benefits if any a skilled artisan would have expected to achieve by forming the first conductive portion and the second conductive portion on each of the three guide plates as required by claims 5, 16, and 17. Ex. 1003, ¶ 297.

128. I disagree with Mr. Taber that merely because *Kim* discloses forming conductive portions on two plates, a skilled artisan would have found it obvious to form the conductive portions on every guide plate of *Kim*'s testing apparatus as modified by *Schmid*. Forming conductive portions on guide plates is an expensive and time-consuming process. For example, forming such a conductive portion typically involves coating the electrically conductive metal on guide plates. *Coombs*, 5.11, 20.10, 22.33. This coating process may involve electro-chemical deposition, sputtering, spin coating, physical vapor deposition, chemical vapor deposition, or some other type of coating process. *Coombs*, 22.33, 23.9, 63.21; *May*, 26, 58-60. Regardless of the process used, a skilled artisan would have understood that coating the conductive metal requires time and a source of the conductive metal material.

129. After coating the guide plate with metal, it is typically necessary to pattern the metal to ensure only certain pins passing through the guide plate are connected to each other. *Coombs*, 5.11. Patterning the metal using lithographic techniques involves application of a photosensitive mask on the metal layer. *Coombs*, 26.2; *May*, 34, 38-40. After coating the mask layer, the mask is exposed and unexposed portions of the mask and the metal disposed below the unexposed portions are etched to form the desired pattern. *Coombs*, 26.2, 26.27; *May*, 34, 38-40, 47-51. A final etching process is typically used to remove the exposed portions of the mask to reveal the desired metal pattern. *Id.* Such etching processes may involve chemical etchants. *May*, 47-51. A skilled artisan would have understood that coating the mask layer and then subsequently etching the mask layer and the underlying metal are process steps that require time and necessitate the use of mask material as well as etching compounds.

130. Thus, a skilled artisan would have understood that forming conductive portions on each guide plate would require time and processing materials used in the forming process. A skilled artisan also would have recognized that forming conductive portions on three guide plates would require more time and materials than that required to form conductive portions on one or two guide plates. Therefore, in my opinion, although conductive portions *could* be formed on each guide plate, as Mr. Taber proposes, a skilled artisan would not have been

motivated to incur additional manufacturing costs and/or increase manufacturing time required to produce the testing apparatus by unnecessarily adding conductive portions on every guide plate. I note that Mr. Taber provides no reasons or bases for why a skilled artisan would have done so. *See* Ex. 1003, ¶¶ 290-298.

131. In my opinion, therefore, Mr. Taber fails to show that the combination of *Kim* and *Schmid* discloses or suggests all the elements of claims 5, 16, and 17. Therefore, the combination of *Kim* and *Schmid* does not render claims 5, 16, and 17 of the '885 patent obvious.

G. The combination of *Kim* and *Fan* does not render obvious claim 3 (Ground 4)

132. Claim 3 of the '885 patent recites “the at least one guide comprises at least one coating dielectric portion that covers the at least one non-conductive zone.” Mr. Taber relies solely on *Fan* as teaching this limitation. Ex. 1003, ¶¶ 329-336; *see also* Pet., 68-70. I disagree for the reasons discussed below.

133. Mr. Taber asserts that *Fan* discloses that its “guide plate ‘can be made of non-conductive materials’” (Ex. 1003, ¶ 333; *see also* Pet., 68), and that “insulating material can be coated on the [plate]” (Ex. 1003, ¶ 332; *see also* Pet., 69). Mr. Taber concludes that “*Fan* teaches, or at least renders obvious, a testing head that ‘comprises at least one coating dielectric portion [insulating layer 600] that covers the at least one non-conductive zone [a portion of guide 100 made of a

non-conductive material].” Ex. 1003, ¶ 334; Pet., 69. I disagree because Mr. Taber has mischaracterized *Fan*’s disclosure.

134. In my opinion, as explained below, nothing in *Fan* discloses or suggests coating a plate 100 made with non-conductive material with insulating layer 600. To the contrary, *Fan* only discloses coating a conductive portion of a plate 100 with insulating layer 600.

135. *Fan* discloses two embodiments: a first embodiment in which the guide plate is made of non-conductive material, and a second embodiment in which the guide plate is made of conductive material. As its first embodiment, *Fan* discloses a probe head that “includes the plate 100, a probe 200, and at least one composite coating layer 300.” *Fan*, col. 3, lines 5-7. *Fan* discloses that “composite coating layer 300 includes a metal layer 310 and a plurality of lubricating particles 320, which may be made of metal-polymer.” *Fan*, col. 3, lines 13-15. *Fan* explains that “metal layer 310 is disposed in the through hole 110 of the plate 100 and between the plate 100 and the probe 200.” *Fan*, col. 3, lines 17-19. Further, *Fan* discloses “the probe head may further include at least one base layer 400 disposed between the metal layer 310 and the plate 100.” *Fan*, col. 3, lines 64-66. *Fan* explains: “In this embodiment, the materials of the base layer 400 and the metal layer 310 may be the same.” *Fan*, col. 4, lines 7-8 (emphasis added). I have

illustrated some of these features of *Fan*'s first embodiment in annotated Fig. 2 of *Fan* excerpted below.

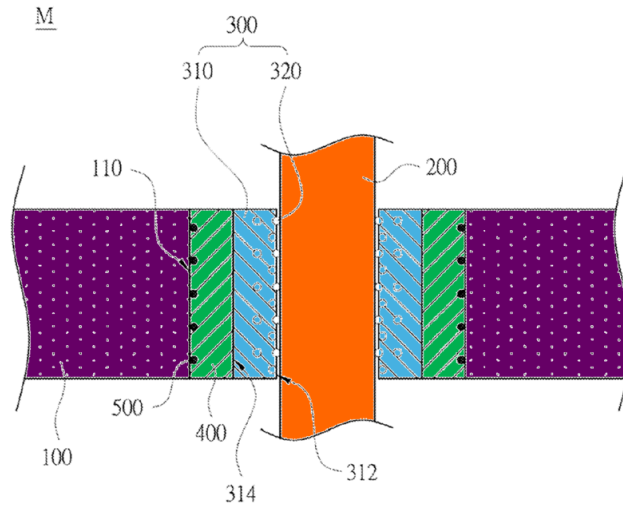


FIG. 2

Fan, Fig. 2 (annotated).

136. For its first embodiment, *Fan* expressly discloses that **base layer 400** and **metal layer 310** are both metallic. With regard to the plate 100, *Fan* discloses that the “plate 100 can be made of non-conductive materials, semiconductor materials, or conductive materials.” *Fan*, col. 3, lines 41-42. But then *Fan* clarifies: “*In this embodiment, the plate 100 may be made of ceramics.*” *Fan*, col. 3, lines 44-45 (emphasis added).

137. If plate 100 in the above embodiment were made of semiconductor or conductive materials, **probe 200** would be electrically connected to **plate 100** through metallic layers **310** and **400**. As a result, all **probes 200** passing through **plate 100** would be shorted out or connected to each other. In my opinion, a skilled

artisan reading *Fan* would have understood that in *Fan*'s first embodiment, **plate 100** would have to be made of a non-conductive material like ceramic to prevent all the **probes 200** from being electrically connected to each other. More importantly, I note that there is no disclosure or suggestion in *Fan* that any portion of the non-conductive ceramic **plate 100** of its first embodiment should be coated with insulating material. Mr. Taber did not identify any such disclosure. Ex. 1003, ¶¶ 329-336; *see also* Pet., 68-70.

138. For its second embodiment, *Fan* expressly states: "The difference between the present embodiment and the embodiment of FIG. 2 relates to additional element of an insulating layer 600." *Fan*, col. 5, lines 3-5. *Fan* explains that when "the **plate 100** is made of semiconductors or conductors, the surfaces of the **plate 100** may be insulated to prevent the **probes 200** that inserted to the **plate 100** from electrically interrupt [sic] from each other." *Fan*, col. 5, lines 8-11. Specifically, the "**insulating layer 600** may be at least disposed between the **metal layer 310** and the **plate 100**." *Fan*, col. 5, lines 11-12. I have illustrated some of these features of *Fan*'s second embodiment in annotated Fig. 4 of *Fan* excerpted below.

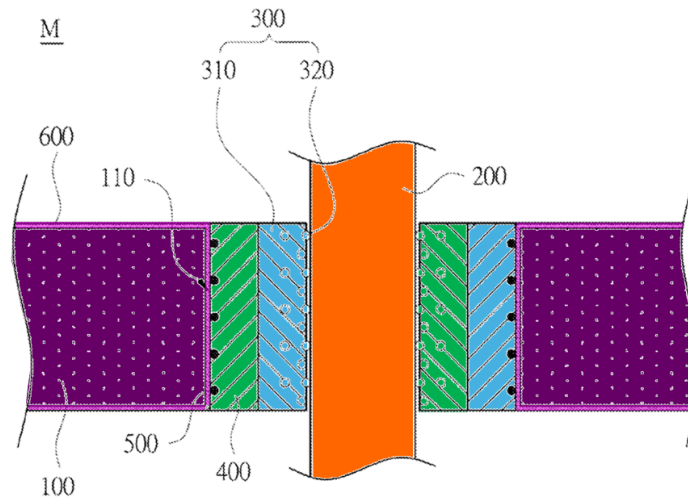


FIG. 4

Fan, Fig. 4 (annotated).

139. In my opinion, adding the **insulating layer 600** between **plate 100** and **base layer 400** and/or **metal layer 310** as illustrated in Fig. 4 above would make sense because doing so would prevent electrical connection between **probe 200** and **plate 100** made of a conductive material. As I explained above, in the absence of the **insulating layer 600**, **probe 200** would be electrically connected to conductive **plate 100** through the metallic (and conductive) **metal layer 310** and **base layer 400**. This would electrically connect or short out all **probes 200** passing through **plate 100**, which would make it impossible to send or detect different electrical signals on different **probes 200**. A skilled artisan would therefore have recognized that **insulating layer 600** would be required to insulate (i.e., electrically disconnect) **probes 200** from conductive **plate 100**.

140. A skilled artisan would also have recognized that no such **insulating layer 600** would be required if **plate 100** were to be non-conductive because in that case, the plate itself would insulate one **probe 200** from another **probe 200**. I further note that there is no disclosure or suggestion in *Fan* that insulating layer 600 “covers [a] non-conductive zone,” as recited in claim 3. Instead, as discussed above and as disclosed by *Fan*, **insulating layer 600** covers a conductive **plate 100**.

141. Thus, contrary to Mr. Taber’s mischaracterizations, nothing in *Fan* discloses covering a non-conductive portion with a dielectric layer. Specifically, *Fan*’s first embodiment does not disclose or suggest covering the surface of the non-conductive guide plate with a dielectric material. And *Fan*’s second embodiment discloses covering the surface of a conductive guide plate with a dielectric material, but does not disclose covering a non-conductive portion of the guide plate with dielectric material. Given the complete lack of disclosure regarding covering a non-conductive portion with a dielectric material in *Fan* or *Kim*, in my opinion, a skilled artisan would not have been motivated to cover a non-conductive portion of *Kim*’s non-conductive guide plate with a dielectric material based on a combination of the teachings of these references.

142. Mr. Taber admits that *Kim*’s guide plate is made of non-conductive material. For example, Mr. Taber cites to *Kim*, ¶ [0062] and states “a POSITA would understand that the material composed of the guide (10) including the upper

plate (11) and the lower plate (12) is *necessarily non-conductive material*.”

Ex. 1003, ¶ 179 (emphasis added). In my opinion, because *Kim*’s guide plate 11 and 12 are made of non-conductive material, a skilled artisan would have recognized from the first embodiment of *Fan* that there is no need to cover *Kim*’s non-conductive guide plates with an insulating layer.

143. Mr. Taber nevertheless asserts: “A skilled artisan would have found it obvious to coat non-conductive zones on the face of the guide plate disclosed in *Kim* with the insulating material disclosed in *Fan*.” Ex. 1003, ¶ 335; *see also* Pet., 69. Mr. Taber further asserts that “a POSITA would have readily understood the benefit of applying *Fan*’s teaching of coating a guide plate with an insulating material to improve *Kim* by coating non-conductive zones on the guide plate of *Kim* and thus helping to ensure that testing pins and conductive portions carrying different signal types remain electrically separated.” Ex. 1003, ¶ 336; *see also* Pet., 70. But Mr. Taber provides no evidence or reasons for why a person of ordinary skill in the art would have been motivated to coat *Kim*’s non-conductive guide plates with *Fan*’s insulating layer. Ex. 1003, ¶¶ 329-336. Nor does he provide any explanation of what in *Kim* would be improved by adding such a dielectric layer when *Kim*’s non-conductive guide plates already ensure that testing pins and conductive portions carrying different signal types remain electrically separated. Ex. 1003, ¶¶ 329-336.

144. I note that adding a dielectric layer between conductive portions can have unintended and detrimental effects. As is well known, conductive portions positioned adjacent to and separated from each other and carrying electrical signals are subject to a capacitance effect due to the relative permittivity of material between the conductive portions. *Schmitt*, 39, 139-143. The amount of capacitance is directly proportional to the relative permittivity. The relative permittivity of a dielectric material can be significantly higher than that of air. *Singh*, Table II. Thus, adding a dielectric material on a non-conductive portion of *Kim*'s guide plate between conductive portions is likely to increase the capacitance, which in turn can affect the magnitude or phase of the electrical signals being transmitted through the conductive portions. *Schmitt*, 38-39, 139-143. Such capacitance may be considered parasitic and undesirable because it can affect the test results when the testing head of *Kim* is used to test an integrated circuit. *Id.* In my opinion, therefore, a skilled artisan would not have found it obvious to add dielectric material between conductive portions already electrically separated by the non-conductive guide plates of *Kim*.

145. To summarize, *Fan* does not disclose or suggest coating any portion of a non-conductive guide plate with insulating material. Moreover, Mr. Taber fails to demonstrate that a skilled artisan would have been motivated or found it obvious to coat *Kim*'s non-conductive guide plates with an insulating layer based on the

teachings of *Fan*. In my opinion, therefore, the combination of *Kim* and *Fan* does not disclose or suggest all the elements of claim 3 and, therefore, does not render claim 3 of the '885 patent obvious.

H. The combination of *Kim* and *Bross* does not render obvious claim 12 (Ground 5)

146. Claim 12 of the '885 patent recites “wherein the first conductive portion is embedded in the at least one guide.” In my opinion, the combination of *Kim* and *Bross* does not disclose or suggest at least these features of claim 12.

147. Citing to ¶¶ [0056]-[0062], Mr. Taber asserts: “Kim discloses various exemplary methods for forming those conductive layers, without limiting its teachings to just those methods.” Ex. 1003, ¶ 338; *see also* Pet., 70-71. Based purportedly on these disclosures, Mr. Taber concludes: “It would have been obvious for a skilled artisan from the teachings of Kim to select a known manufacturing method, such as the one from Bross, to form the claimed conductive portion in the claimed guide.” Ex. 1003, ¶ 338, *see also* Pet., 70-71. Further, Mr. Taber asserts that “a POSITA would be motivated to use the well-known laminating methods described by Bross in Kim to achieve embedding at the time of the invention and would have expected to be successful in doing so following Bross’s teachings.” Ex. 1003, ¶ 340; *see also* Pet., 71. I disagree because here again, Mr. Taber mischaracterizes the disclosures of *Kim*. In its ¶¶ [0056]-[0062], *Kim* discloses various methods of forming a conductive layer on top of a surface of

its guide plate. These methods of *Kim*, however, do not disclose or suggest a single technique that uses lamination or embedding of a conductive layer within a guide plate as recited in claim 12 of the '885 patent.

148. For example, *Kim* discloses a first method in which “the conductive material is plated or deposited on the entire surface of the guide plate 10.” *Kim*, ¶ [0057]. As another example, *Kim* discloses a second method in which “after a photoresistor is partially formed on the surface of the guide plate 10, in that the forming of the conductive layer 20 and conductive trace 40 is unnecessary, the conductive material is entirely plated or deposited thereon.” *Kim*, ¶ [0058]. *Kim* also discloses a third method in which “after a screen is arranged on the surface of the guide plate 10, in that the forming of the conductive layer 20 and conductive trace 40 is unnecessary, the conductive material is deposited thereon.” *Kim*, ¶ [0059]. For the third method, *Kim* explains “the seed layer is formed on the area in which the screen is not arranged and the conductive layer 20 and conductive trace 40 can be formed through the electroplating method.” *Kim*, ¶ [0060]. For its last method, *Kim* discloses “the conductive materials are deposited on the entire surface of the guide plate 10.” *Kim*, ¶ [0061]. A skilled artisan would have understood from these disclosures that every method disclosed in *Kim* is directed to depositing conductive material on a surface of *Kim*'s guide plate. In my opinion, a skilled artisan would not have found it obvious to use the probe assembly

methods of *Bross* for stacking conductive material within *Kim*'s guide plate based on these disclosures of *Kim*.

149. Moreover, while the stacking processes of *Bross could* be used to form the guide plates of *Kim*, Mr. Taber does not explain why a skilled artisan *would* have found it obvious to completely change the structure of *Kim*'s testing apparatus using the stacking methods of *Bross*. See Ex. 1003, ¶¶ 337-345. Similarly, Mr. Taber does not explain why stacking the metal layer in *Kim*'s guide plate would have been more advantageous than coating the conductive layer on a surface of the guide plate as disclosed by *Kim*. See Ex. 1003, ¶¶ 337-345. As explained below, I disagree with Mr. Taber's position that a skilled artisan would have modified *Kim*'s guide plate using the techniques taught by *Bross*.

150. In my opinion, a skilled artisan would not have been motivated to replace *Kim*'s relatively simple structure with the more complicated sandwiched structure of *Bross*. *Bross* discloses a probe assembly 20 with a body 22 that includes a multi-layer arrangement comprising "a top insulating layer 23, a first conductive layer 24, a second insulating layer 26, a second conductive layer 28, a third insulating layer 30, a third conductive layer 32, and a fourth or bottom insulating layer 34." *Bross*, col. 4, lines 41-46. *Bross* also discloses that its "probe element 36 passes through a small, precisely located clearance hole 40 in the second insulating layer 26, through a similar hole 42 in the third insulating layer

30, and through a similar hole 44 in the fourth insulating layer 34.” *Bross*, col. 4, line 66 to col. 5, line 2. *Bross* explains that “probe element 36 in piercing through the layer of conductive circuitry 32 at the zone 50 makes a mechanically tight and good electrical connection to a respective conductive portion of the layer of circuitry 32.” *Bross*, col. 5, lines 43-47.

151. *Bross* discloses that probe element 36 extends through clearance hole 44. *Bross* further disclose that probe element 36 makes electrical contact with the conductive layers 24, 28, and 32 because these conductive layers extend into elements of clearance hole 44 and probe element 36 pierces through the conductive layers 24, 28, and 32. *Bross*, col. 4, line 66 to col. 5, lines 2, 43-47. In contrast, in *Kim*, one side of *Kim*’s testing pin 30 “is electrically contacted with one side of the conductive layer 20,” which is formed in the guide holes in *Kim*’s guide plate. *Kim*, ¶¶ [0038]-[0039]. Thus, *Bross* discloses a completely different arrangement of insulating and conductive layers as compared to that disclosed by *Kim*.

152. Furthermore, *Bross*’s structure requires taking a plurality of insulating layers and conductive layers and bonding them to form a multilayer bonded arrangement. *Bross*, col. 4, lines 41-52. Nothing in *Bross* discloses or suggests any advantages of this method relative to the method of forming conductive traces 40 of *Kim* directly on the surfaces of *Kim*’s guide plate. Mr. Taber also provides no reasons or bases for why a person of ordinary skill in the art would have

completely replaced *Kim*'s unitary guide plate structure with that of *Bross*'s multilayer bonded arrangement. *See* Ex. 1003, ¶¶ 337-345.

153. The structure disclosed by *Bross* involves forming multiple insulating and conductive layers and bonding them together. *Bross*, col. 4, lines 41-52. *Bross* also discloses that the "various layers of printed circuitry are selectively connected at specially provided 'via' locations to respective ones of very thin relatively long conductive wires." *Bross*, col. 2, lines 10-13; col. 2, lines 33-38. *Bross* also discloses that the "vias of the multi-layer circuitry are formed in a precise pattern." *Bross*, col. 2, lines 17-18; col. 2, lines 38-40. *Bross* explains that "vias are aligned vertically in one plane of view (e.g., the Y direction) and are staggered vertically in a plane of view at right angles." *Bross*, col. 2, lines 44-47.

154. A skilled artisan would have recognized that the assembly of a large number of parts (insulating layers and printed circuitry layers) in *Bross*'s structure, precise alignment of these parts, and the added step of bonding the parts is likely to result in greater manufacturing complexity and costs. *Ritchey*, 12-15; *Levreault*, 29; *Holden*, 44; *Reid*, 78-81; *Coombs*, 2.14, 27.22-25; *Smith*, 21; *Hsu*, 6, 14. A skilled artisan would have also recognized that the requirement to precisely align multiple layers to ensure the vias formed in the different layers are vertically aligned in one direction while being staggered in another direction would increase manufacturing complexity and costs. *Id.*

155. In contrast, *Kim*'s structure does not require precise alignment of multiple material layers and also does not require any added step of bonding multiple material layers. A skilled artisan, therefore, would not have been motivated to replace *Kim*'s relatively simple structure consisting of a single plate with through holes with the more complicated sandwiched structure of *Bross* particularly because *Bross*'s structure provides no additional structural, manufacturing, economic, or performance benefits over *Kim*'s guide plate arrangement, given the increased complexity of *Bross*. Indeed, Mr. Taber did not identify any such benefits of using *Bross*'s structure over the unitary guide plate structure of *Kim*. See Ex. 1003, ¶¶ 337-345.

156. In my opinion, therefore, Mr. Taber fails to show that a skilled artisan would have been motivated and found it obvious to replace *Kim*'s structure with that of *Bross*. As a result, Mr. Taber has also failed to show that the combination of *Kim* and *Bross* discloses or suggests the elements of claim 12 of the '885 patent. In my opinion, therefore, the combination of *Kim* and *Bross* does not render claim 12 of the '885 patent obvious.

I. The combination of *Kim*, *Bross*, and *Schmid* does not render obvious claim 21 (Ground 7)

157. Like claim 12, claim 21 of the '885 patent also recites "wherein the first conductive portion is embedded in the at least one guide." Claim 21 depends from claim 16. Mr. Taber presents no new arguments for claim 21 but refers to his

arguments for claims 12 and 16. Ex. 1003, ¶ 358; *see also* Pet., 75. Furthermore, Mr. Taber does not rely on *Schmid* as disclosing or suggesting the recitations of claim 12. Ex. 1003, ¶¶ 337-345; *see also* Pet., 70-72. In his analysis of claim 16, Mr. Taber again does not rely on *Schmid* for the recitations of claim 16. Ex., 1003, ¶¶ 313-315; *see also* Pet., 66. As I discussed above for claim 12, the combination of *Kim* and *Bross* fails to disclose or suggest the limitations of claim 12. Accordingly, for similar reasons, Mr. Taber fails to demonstrate that the combination of *Kim*, *Bross*, and *Schmid* renders obvious claim 21 of the '885 patent.

IX. CONCLUSION

158. For the reasons set forth in Section VIII, it is my opinion that claims 2, 3, 5, 6, 7, 12, 14, 16, 17, 18, 21, and 23 of the '885 are patentable over the prior art and prior art combinations identified by FormFactor.

159. In signing this declaration, I understand that the declaration will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I acknowledge that I may be subject to cross-examination in this case and that cross-examination will take place within the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

160. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Date: April 17, 2025

Respectfully submitted,



Shukri Sourì, Ph.D.

Appendix A



Exponent®

Engineering & Scientific Consulting

Shukri Sourì, Ph.D.

Corporate Vice President, Practice/Office Director and Principal | Electrical Engineering and Computer Science

New York

+1-212-895-8126 | ssouri@exponent.com

Professional Profile

Dr. Sourì's expertise is in microelectronics and computing systems. His professional activities involve advising industrial and legal clients as well as government entities on science and technology matters addressing issues related to intellectual property, product reliability, and failure analysis.

Dr. Sourì has led complex investigations involving electronics, computer communications, and software controls for safety-critical applications in the medical device, automotive, aviation and process controls industries.

Dr. Sourì's experience in the area of microelectronics systems includes technical investigations into computer memories, device physics, integrated circuit (IC) fabrication processes, and esoteric semiconductor material systems for solid-state lighting. He also has broad experience with power electronic devices, circuit protection, IC packaging, and printed circuit board assemblies and display technologies as used in various industries including consumer appliances.

In computing systems, Dr. Sourì has worked extensively with embedded controls systems for automotive applications, computer hard disk drives and for drug delivery and implantable devices. He also has expertise in telephony, secure mobile and Internet communications, microprocessor architectures particularly for mobile computing and has analyzed audio/video/image processing software and developed digital asset delivery technologies.

Dr. Sourì received his Ph.D. in Electrical Engineering at Stanford University on 3-Dimensional integration of ICs and has taught several courses on IC fabrication, optical fiber communications, TCP/IP networking, and communications protocols and implementation of systems on 3-D chips. He also read Engineering Science at Balliol College, Oxford, where he specialized in photoreflectance microscopy of semiconductor materials. His current research interests include: cloud computing, information security and privacy; financial portfolio optimization, and trading algorithms and software.

Academic Credentials & Professional Honors

M.A., University of Oxford, UK, 2007

Ph.D., Electrical Engineering, Stanford University, 2003

M.S., Electrical Engineering, Stanford University, 1994

B.A., Engineering Science, University of Oxford, UK, 1992

Prior Experience

Founder, Merenga Inc., 2000-2002

Co-Founder and Engineering Manager, arcadiaOne, Inc., 1999-2000

Research Engineer, Circuit Protection Division, Raychem, 1996-1997

Research Scientist, Corporate Research & Development, Raychem, 1994-1996

Professional Affiliations

Institution of Engineering and Technology—IET (member)

Institute of Electrical and Electronic Engineers (senior member)

Oxford University Society (life member)

Oxford Union (member)

Patents

Patent 6,188,556: Two-Terminal Transistor PTC Circuit Protection Devices, WO0024126, 2001 (with C. McCoy, H. Duffy, A. Cogan, and R. Bommakant).

Patent 6,181,541: Transistor-PTC Circuit Protection Devices, WO0024105, 2001 (with H. Duffy, A. Cogan, M. Munch, and N. Nickols).

Patent 6,153,948: Electronic Circuits with Wide Dynamic Range of On/Off Delay Time, WO001249, 2000 (with A. Cogan).

Patent 5,569,495: Method of Making Varistor Chip with Etching to Remove Damaged Surfaces, CA2220931, EP0826225, WO963978, JP11505375T, 1996 (with A. Evans, T. Tsukada, and R. Dupon).

Publications

H. K. Kytomaa, P. Boehm, J. Osteraas, B. Haddad, J. Hacker, L. Gilman, E. Jampole, P. Murphy, S. Souri. An integrated method for quantifying and managing extreme weather risks and liabilities for industrial infrastructure and operations. Process Safety Progress 2019, American Institute of Chemical Engineers. July 2019. <https://doi.org/10.1002/prs.12087>

D'Andrade B, Kattamis AZ, Murphy PF, McNulty J, Souri S. Arcing enabled by tin whiskers. IEEE: Reliability Society 2010 Annual Technical Report, 2010.

Fu J, Souri S, Harris J. Temperature and humidity dependent reliability analysis of RGB LED chip. Proceedings, ISTFA 2006: Discretes, Passives, MEMS, and Optoelectronics, pp. 137-141, 2006.

Saraswat K, Kapur P, Souri S. Performance limitations of metal interconnects and possible alternatives. 203rd Meeting of the Electrochemical Society, Paris, France, April 2003.

Saraswat K, Kapur P, Chandra G, Chiang T-Y, Souri S. Scaling induced performance limitations of metal interconnects. IEEE ISSCC Microprocessor Design Workshop, San Francisco, CA, February 2002.

Chiang T, Souri S, Chui C, Saraswat K. Thermal analysis of heterogeneous 3-D ICs with various integration scenarios. IEEE IEDM, December 2001.

Banerjee K, Souri S, Kapur P, Saraswat K. 3-D Heterogeneous ICs: A technology for the next decade and beyond. 5th IEEE Workshop on Signal Propagation on Interconnects, Venice, Italy, May 2001.

Banerjee K, Souri S, Kapur P, Saraswat K. 3-D ICs: A novel chip design for improving deep-submicrometer interconnect performance and systems-on-chip integration. Proceedings, IEEE: Special Issue on Interconnections, Vol. 89, No. 5, pp. 602-633, May 2001.

Davis J, Venkatesan R, Kaloyeros A, Bylansky M, Souri S, Banerjee K, Saraswat K, Rahman A, Reif R, Meindl J. Integration limits on Gigascale Integration (GSI) in the 21st Century. Proceedings, IEEE: Special Issue of Limits to Semiconductor Technology, Vol. 89, No. 3, pp. 3-05-324, March 2001.

Saraswat K, Banerjee K, Joshi A, Kalvade P, Kapur P, Souri S. 3-D ICs: Motivation, performance analysis and technology. Proceedings, 26th European Solid-State Circuits Conference (ESSCIRC), Stockholm, Sweden, September 19-21, 2000.

Souri S, Banerjee K, Mehrotra A, Saraswat KC. Multiple Si layer ICs: Motivation, performance analysis, and design implications. 37th ACM Design Automation Conference (DAC), pp. 213-220, Los Angeles, CA, June 5-9, 2000.

Saraswat K, Banerjee K, Joshi A, Kalavade P, Souri S, Subramanian V. 3-D ICs with multiple Si Layers: Performance analysis, and technology. 5th International Symposium on Low and High Dielectric Constant Materials: Materials Science, Processing, and Reliability Issues, 197th Meeting of the Electrochemical Society, Toronto, Canada, May 14-19, 2000.

Saraswat K, Souri S, Subramanian V, Joshi A, Wang A. Novel 3-D structures. Proceedings, IEEE International SOI Conference, pp. 54-55, 1999.

Subramanian V, Toita M, Ibrahim N, Souri S, Saraswat K. Low-leakage germanium-seeded laterally-crystallized single-grain 100nm TFTs for vertical integration applications. IEEE Electron Device Letters, Vol. 20, pp. 341-343, 1999.

Souri S, Saraswat K. Interconnect performance modeling for 3D integrated circuits with multiple Si layers. IEEE International Interconnect Technology Conference, pp. 24-26, 1999.

Haskell B, Souri S, Helfand M. Varistor behavior at twin boundaries in ZnO. Journal of the American Ceramic Society, Vol. 82, No. 8, August 1999.

Chu A, Souri S, Melfand M, Kinsman K, Dupon R. Superior electrical performance of Raychem ZnO Varistor through advanced processing. Proceedings, 1st Asian Meeting on Ferroelectricity, Xian, China, October 5-8, 1995.

Books

A. Arora, S. Arun Lele, N. Medora, S. Souri. Lithium-Ion Battery Failures in Consumer Electronics. Artech House, 2019.

Souri S, Chiang T, Kapur P, Banerjee K, Saraswat KC. 3-D ICs deep submicron interconnect performance modeling and analysis. In: Interconnect Technology and Design for Gigascale Integration. Davis J and Meindl J (eds), Kluwer Academic Publishers, October 2003.