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Sixth Edition

- Lead-free PCB design and manufacturing techniques
- Lead-free materials
- Lead-free reliability models
- High-Density Interconnection (HDI) best practices

Clyde F. Coombs, Jr.

PRINTED CIRCUITS HANDBOOK

Clyde F. Coombs, Jr. Editor-in-Chief

Sixth Edition



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CHAPTER 2

ELECTRONIC PACKAGING AND HIGH-DENSITY INTERCONNECTIVITY*

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2.1 INTRODUCTION

All electronic components must be interconnected and assembled to form a functional and operating system. The design and the manufacture of these interconnections have evolved into a separate discipline called *electronic packaging*. Since the early 1950s, the basic building block of electronic packaging is the printed wiring board (PWB), and it will remain that into the foreseeable future. This book outlines the basic design approaches and manufacturing processes needed to produce these PWBs.

This chapter outlines the basic considerations, the main choices, and the potential trade-offs that must be accounted for in the selection of the interconnection methods for electronic systems. Its main emphasis is on the analysis of potential effects that the selection of various printed wiring board types and design alternatives could have on the cost and performance of the complete electronic product.

2.2 MEASURING THE INTERCONNECTIVITY REVOLUTION (HDI)

The continuing increase in component performance and lead density, along with the reduction in package sizes, has required that PWB technology find corresponding ways to increase the interconnection density of the substrate. With the introduction and continued refinement of such packaging techniques as the ball grid array (BGA), chip-scale packaging (CSP), and chip-on-board (COB), traditional PWB technology has approached a point where alternative ways of providing high-density interconnection have had to be developed. (See Chaps. 3 and

* Adapted from Coombs, Clyde F. Jr., *Printed Circuits Handbook* (4th ed.), chap. 1, "Electronic Packaging and Interconnectivity," (McGraw-Hill, New York, 1996.)

The importance of the rigorous cost trade-off analysis during the design of electronic products is underscored by the fact that about 60 percent of the manufacturing costs are determined in the first stages of the design process, when only 35 percent of the total design effort has been expended.

Attention to manufacturing and assembly requirements and capabilities (so-called design for manufacturability and assembly [DFM/A]) during product design can reduce assembly costs by up to 35 percent and PWB costs by up to 25 percent.

The elements that must be considered for the most cost-effective electronic packaging designs are:

- Optimization of the PWB design and layout to reduce its manufacturing cost
- Optimization of the PWB design to reduce its assembly cost
- Optimization of the PWB design to reduce testing and repair costs

The following sections provide some guidelines on how to approach such optimization of PWB designs. Basically, the costs of the electronic assemblies are directly related to their complexity and there are a number of measurements relating the effects of various PWB design elements to their costs to guide the design engineer in selection of the most cost-effective approach.

2.5 ICS AND PACKAGES

The most important factors influencing PWB design and layout are the component terminal patterns and their pitches, especially those of ICs and their packages, since these dictate the density of the interconnecting substrates. Thus, this element will be considered first.

Driven by the need for improved cost and performance, the complexity of ICs is constantly increasing. Due to relentless progress in IC technology, the gate density on a chip is increasing by about 75 percent per year, resulting in the growth of IC chip I/O terminals by 40 percent per year, which places ever increasing demands on the methods of their packaging and interconnection.

As a result, the physical size of electronic gears keeps shrinking by 10 to 20 percent per year, while the surface area of substrates is being reduced by about 7 percent per year. This is accomplished by continuously increasing wiring densities and reducing linewidths, which has severely stressed PWB manufacturing methods, reduced processing yields, and increased the costs of the boards.

2.5.1 IC Packages

Since their inception, IC chips have been placed within ceramic or plastic packages. Until about 1980, all IC packages had terminal leads that were soldered into plated through-holes (PTHs) of the PWBs. Since then, an increasing number of IC packages have their terminals made in a form suitable for surface-mounting technology (SMT), which has become the prevailing method of component mounting.

There has been a proliferation of IC package types, both for through-hole assembly as well as for surface mounting, varying in their lead configurations, placement, and pitches. Also, IPC-SM-782³ provides a good catalog of the available SMT packages and of the PWB footprint formats they require for their assembly.

Basic I/O termination methods of IC packages include the following:

- *Peripheral*, where the terminations are located around the edges of the chip or package
- *Grid-array*, where the terminations are located on the bottom surface of the chip or package

Most IC packages have peripheral terminations at their edges. The practical limit on the peripheral lead pitches on packages is about 0.3 mm, which permits locating, at most, 500 I/Os on a large IC package, as shown in Table 2.2. It has also become evident that, in typical board assembly operations, the yields plummet as the lead pitches go below 0.5 mm.

TABLE 2.2 Various Array Package Body Sizes, Configurations, and Lead Pitches

Body size (mm)	Number of I/Os	Minimum pitch (mm)
8 × 8	24	0.5
9 × 9	68	0.5
10 × 10	144	0.5
13 × 13	154	0.65
23 × 23	168	1.27
23 × 23	208	1.27
23 × 23	217	1.27
23 × 23	240	1.27
23 × 23	249	1.27
27 × 27	225	1.27
27 × 27	256	1.27
27 × 27	272	1.27
27 × 27	292	1.27
27 × 27	300	1.27
27 × 27	316	1.27
31 × 31	304	1.50
31 × 31	329	1.27
31 × 31	360	1.27
31 × 31	385	1.27
35 × 35	313	1.27
35 × 35	352	1.27
35 × 35	388	1.27
35 × 35	420	1.27
35 × 35	456	1.27
37 × 37	676	0.8
42.5 × 52.5	1247	1.0
52.5 × 52.5	2577	1.0

Various area array components come with a large variety of body sizes, numbers of I/Os, and I/O pitches. These components are called chip-scale packages (CSPs), plastic ball grid arrays (PBGA), ceramic ball grid arrays (CBGAs), plastic pin grid arrays (PPGAs), and ceramic column grid arrays (CCGAs).

It is expected that chips with terminal counts below 150 to 200 will continue to use packages with peripheral leads, if these can be soldered within practical assembly yields. But for IC packages with over 150 to 200 I/Os, it is very attractive to use the grid-array terminations, since in such a case the entire bottom surface area can be utilized for terminations, which makes it possible to place large numbers of I/Os within a limited area.

This consideration has led to the development of a number of area array solder-bumping termination methods for IC and multichip module (MCM) packages, variously called pad grid, land grid, or ball grid arrays (BGAs) with terminal grids set at 1 mm (0.040 in), 1.27 mm (0.050 in), and 1.50 mm (0.060 in), respectively.

Use of grid arrays provides a number of benefits. The most important is the minimal footprint area on the interconnecting substrate, but grid arrays also offer better electrical performance due to low electrical parasitics in high-speed operation, simplified adaptation into SMT

component placement lines, and better assembly yields, despite the impossibility of direct visual inspection of the joints.

Due to continuous decrease of the terminal pitches on packages, it is important that PWB designers carefully assess the manufacturing and assembly capabilities of PWB substrates requiring such fine-pitch terminations, to ensure the greatest yields and lowest cost of the product.

2.5.2 Direct Chip Attach

The relentless pressures of size, weight, and volume reduction of electronic products have resulted in a growth in interest in direct chip attach (DCA) methods, where bare IC chips are mounted directly to the substrate. These methods are extensively used on chip-on-board (COB) and multichip module (MCM) assemblies, as shown in Fig. 2.4.

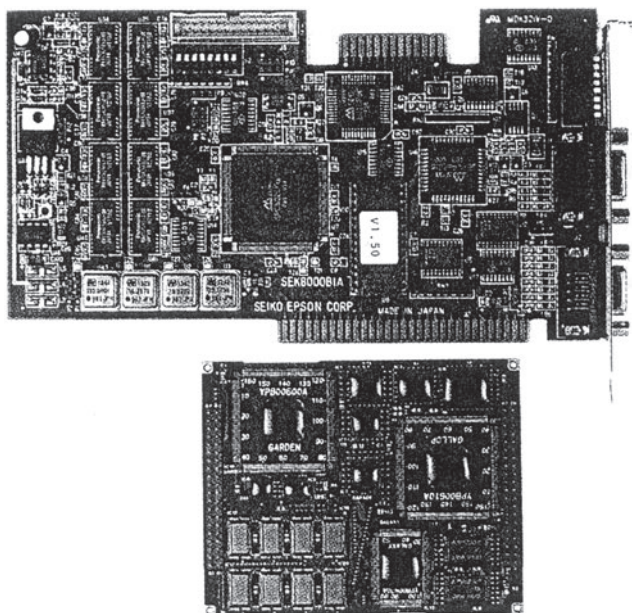


FIGURE 2.4 COB and MCM assemblies.

Three methods of bare chip attachment to the substrate are as follows:

1. *Wire-bonding* is the oldest and the most flexible and widely used method. (More than 96 percent of all chips today are wire-bonded.)
2. *Tape-automated bonding* (TAB) is useful with small I/O pitches and provides the ability to pretest the chips before assembly.
3. *Flip-chipping* is used for its compactness and improved electricals, typical of which is the C4 process of IBM.

The problems of thermal coefficient of expansion (TCE) mismatch between silicon chips that are directly flip-chipped onto a laminate substrate have been effectively eliminated by using a filled epoxy underfill encapsulation technique between the chip and the substrate (see

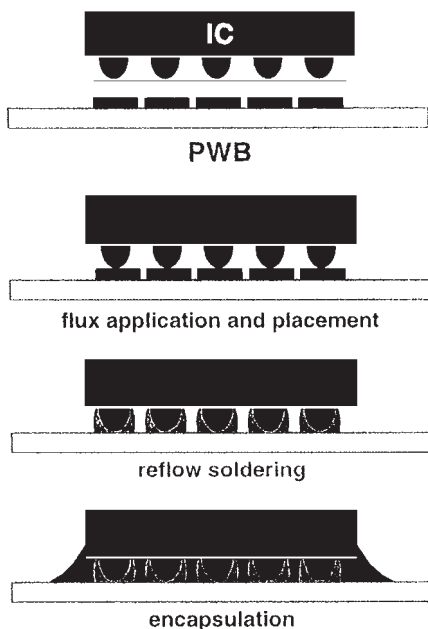


FIGURE 2.5 Underfill between the chip and PWB on flip-chip on board.

Fig. 2.5). This method distributes stresses over the entire area of the chip and thus significantly improves the reliability performance of this assembly method.

While the chips that need area array or flip-chip terminations—i.e., those with high pin counts—are the fastest-growing category of ICs, they still represent only a very small percent of all ICs used. Designers must, therefore, ascertain which of the DCA methods will be the most cost beneficial for a particular application.

2.5.3 Chip-Scale Packages (CSPs)

When mounting unpackaged chips on these interconnecting substrates, it is not always possible to ascertain that only properly operating chips have been assembled. By now, there are a number of methods proposed to solve this known good die (KGD) problem.

As one of the ways to resolve this problem, a number of manufacturers have developed a set of miniature packages, only slightly larger than the chip itself, which protect the chip and redistribute the chip termination to a grid array. These miniature packages permit testing and burning in of chips prior to their final assembly. A typical example of such chip scale packages is shown in Fig. 2.6. There are a number of such packages on the market.

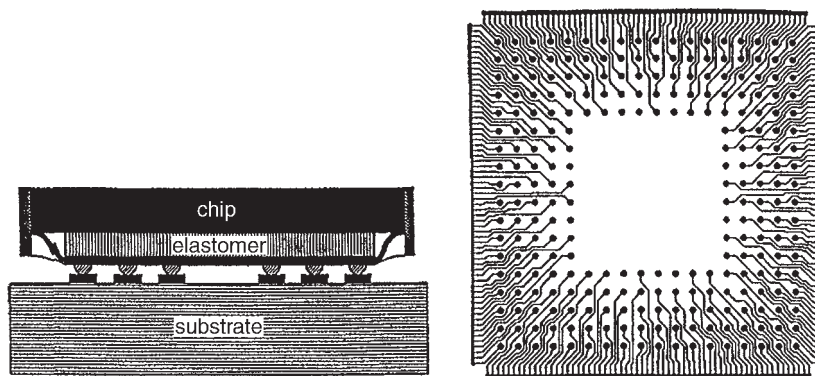


FIGURE 2.6 CSP by Tessera, Inc., San Jose, California.

The designer, however, must analyze the termination pitches of these new CSPs because some use very tight grids, such as 0.5 mm (0.020 in) or less, which need special PWB techniques to permit signal redistribution from these packages to the rest of the board.

In general, the current PWB technology is adequate to provide direct chip terminations if wire-bonding or TAB techniques are used for interconnecting bare chips to the substrate. It requires placing suitable bonding pads spaced by the required pitch in one or two rows around the chip site. While this somewhat reduces the packaging efficiency of the board, it is still an effective method for DCA assemblies.

With grid array, the situation is more difficult because the signals from internal rows of area grid terminations must be routed between the terminals located closer to the edge, which

do not permit more than one, or at most two, conductors to pass through. In most cases, these signals from internal rows are brought down into internal layers of MLBs.

The conventional PCB constructions today cannot handle any grid arrays with pitches below 0.020 in, while some flip-chip ball grid arrays go below 0.010-in pitch. In cases when grid distances of the area terminations are below 0.50 mm (0.040 in), special redistribution layers are frequently used, which distribute signals to the conventionally made PTHs in supporting MLB.

Such layers consist of unsupported dielectric layers where small vias or blind holes are formed by laser or plasma etching or are photoformed and then plated using additive or semi-additive metallization processes. While this approach requires some extra area beyond the chip perimeter to complete the signal transfer and increases the costs of substrates, it permits the mounting of flip-chips and CSPs on PWBs. A typical method for forming such redistribution layers, called surface laminar circuit (SLC),⁴ has been developed at IBM's Yasu plant.

2.6 DENSITY EVALUATIONS

2.6.1 Component Density Analysis

Because the components and their terminations exert a major effect on the design of the PWB, a number of metrics have been developed to establish the relationships between component density and PWB density. A major analysis of these relationships has been made by H. Holden⁵ and some of his charts and derivations are provided here to guide the design engineers during the development of a rational PWB design.

This information is very useful in determining where the designed product will fit in the component density spectrum and what, therefore, is to be expected for PWB density.

Figure 2.7 provides a generalized view of the relationships among the component density, their terminal density, and the necessary wiring density that will be required to accommodate the selected degree of component complexity. The definition of the wiring connectivity W_f is provided.

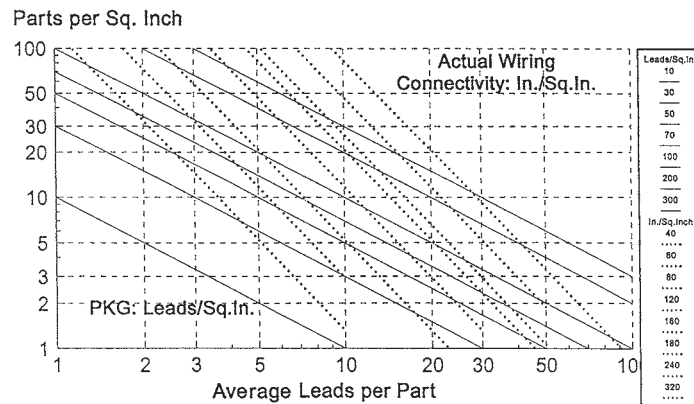


FIGURE 2.7 Plot of general relations between component and wiring density.

2.6.2 PWB Density Metrics

It is essential for the proper design of PWBs to determine the density requirements and then analyze alternative methods of board construction for the most cost-effective design. There are a number of basic terms and equations used for the calculation and analysis of PWB wiring density.

CHAPTER 5

TYPES OF PRINTED WIRING BOARDS

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5.1 INTRODUCTION

Since the invention of printed wiring technology by Dr. Paul Eisner in 1936, several methods and processes have been developed for manufacturing printed wiring board (PWBs) of various types. Most of these have not changed significantly over the years; however, some specific trends continue to exert major influences on the types of PWBs required and the processes that create them:

1. Computers and portable telecommunications equipment require higher-frequency circuits, boards, and materials, and also use more functional components that generate considerable amounts of heat that need to be extracted.
2. Consumer products have incorporated digital products into their design, requiring more functionality at ever-lower total cost.
3. Products for all uses continue to get smaller and more functional, driving the total circuit package itself to become more dense, causing the PWBs to evolve to meet these needs.

These trends have led to the larger use of nonorganic base substrates, such as aluminum and soft iron. In addition, alternate ways to create boards have been developed. These will be discussed in this chapter, along with the traditional board structures and processes. The terms *printed wiring board*, *PWB*, and *board* will be used synonymously. Also, the words *laminate*, *substrate*, and *panel* will be used interchangeably.

5.2 CLASSIFICATION OF PRINTED WIRING BOARDS

PWBs may be classified in many different ways according to their various attributes. One fundamental structure common to all of them is that they must provide electrical conductor paths which interconnect components to be mounted on them.

5.2.1 Basic PWB Classifications

There are two basic ways to form these conductors:

5.1

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5.7 MOLDED INTERCONNECTION DEVICES

Three-dimensional circuit technology was of great interest in the early to mid-1980s. The proponents for this technology, however, realized the mistake of trying to make it directly competitive with conventional flat circuits and have developed a niche where the substrate also offers other functional uses, such as structural support for the product.

Manufacturers of three-dimensional circuits prefer to call them *molded interconnection devices* (MIDs). In many applications of MIDs, the number of components to interconnect the electronic and electrical components can be reduced, thus making the total assembly cost cheaper and the final structure more reliable.

5.8 PLATED-THROUGH-HOLE (PTH) TECHNOLOGIES

In 1953, the Motorola Corporation developed a PTH process called the *Placir* method,¹ in which the entire surface and hole walls of an unclad panel are sensitized with SnCl_2 and metallized by spraying on silver with a two-gun spray. Next, the panel is screened with a reverse conductor pattern, using a plating resist ink, leaving metallized conductor traces uncovered. The panel is then plated with copper by an electroplating method. Finally, the resist ink is stripped and the base silver removed to complete the PTH board. One problem associated with the use of silver is the migration caused by silver traces underneath the copper conductors.

The Placir method was the forerunner of the semiadditive process, which is discussed in Chap. 31.

In 1955, Fred Pearlstein² published a process involving electroless nickel plating for metallizing nonconductive materials. This catalyzer consists of two steps. First, the panel is sensitized in SnCl_2 solution, and then it is activated in PdCl_2 solution. This process presented no problem for metallizing nonconductive materials.

At the same time that Pearlstein's paper was published, copper-clad laminates were starting to become popular. Manufacturers of PWBs applied this two-step catalyzing process to making PTHs using copper-clad laminates. This process, however, turned out to be incompatible with the copper surface. A myriad of black palladium particles called *smads* were generated between copper foil and electrolessly deposited copper, resulting in poor adhesion between the electroless copper and the copper foil. These smads and electroless copper had to be brushed off with strong abrasive action before the secondary electroplating process could begin. To overcome this smad problem, around 1960 researchers began attempting to develop better catalysts; the products of their research were the predecessors of modern palladium catalysts.³

The mid-1950s was a busy time in the area of electroless copper-plating solutions. Electrolessly deposited nickel is difficult to etch. But since it adheres somewhat better to the base than does electroless copper, research for the development of stable electroless copper-plating solutions was quite natural. Many patent applications for these solutions were filled in the mid-1950s. Among the applicants were P. B. Atkinson, Sam Wein, and a team of General Electric engineers, Luke, Cahill, and Agens. Atkinson won the case, and a patent⁴ teaching the use of Cu-EDTA as a complexing agent was issued in January 1964 (the application had been filed in September 1956).

5.8.1 Subtractive and Additive Processes

Photocircuits Corporation was another company engaged throughout the 1950s in the development of chemicals for PTH processes. Copper-clad laminates were expensive, and a major

portion of expensive copper foil had to be etched (*subtracted*) to form the desired conductor pattern. The engineers at Photocircuits, therefore, concerned themselves with plating (*adding*) copper conductors wherever necessary on unclad materials for the sake of economy. Their efforts paid off. They were successful in developing not only the essential chemicals for reliable PTH processes but also the fully additive PWB manufacturing technology known as the CC-4* process. This process is discussed in detail in Chap. 31.

With the use of SnCl_2 - PdCl_2 catalysts and EDTA-base electroless copper-plating solutions, the modern PTH processes became firmly established in the 1960s. The process of metallizing hole walls with these chemicals for the subsequent formation of PTHs is commonly called the *copper reduction process*. In the subtractive method, which begins with copper-clad laminates, pattern plating and panel plating are the two most widely practiced methods of making PTH boards. These methods are discussed in the following subsections.

5.8.2 Pattern Plating

In the pattern-plating method, after the copper reduction process, plating resist layers of the reverse conductor image are formed on both sides of the panel by screening resist inks. In most fineline boards, photosensitive dry film is used instead. There are some minor variations in the pattern-plating method (see Fig. 5.6):

1. Catalyzing (preparing the nonconductive surface to cause copper to come out of solution onto that surface)
2. Thin electroless copper (0.00001 in) followed by primary copper electroplating; thick electroless copper (0.0001 in)
3. Imaging (application of a plating resist in the negative of the desired finished circuit)
4. Final electroplating copper
5. Solder plating (as etching resist) 0.0002 or 0.0006 in
6. Stripping plating resist
7. Etching of base copper
8. Solder etching (0.0002-in case); solder reflow (0.0006-in case)
9. Solder mask followed by hot-air solder coater leveler if solder etching is used
10. Final fabrication and inspection

Most manufacturers of DSBs with relatively wide conductors employ thick electroless copper plating. However, thin electroless copper followed by primary electroplating is preferred for boards having fine-line conductors, because a considerable amount of surface is brushed off for better adhesion of dry film. This provides a higher reliability for PTHs. Solder reflow boards had been preferred by many customers, particularly in military and telecommunications applications, until the emergence of hot-air solder coater levelers. Although the solder-over-copper conductors protect the copper from oxidization, solder reflow boards have some limitations. Solder mask is hard to apply over reflowed solder, and it tends to wrinkle and peel off in some areas when the boards go through component soldering. A more serious problem is the solder bridging that occurs when the conductor width and clearance become very small.

In step 9, the entire surface of the board except for the pads is covered by solder mask, and then the board is immersed into the hot-air solder coater leveler, resulting in a thin coating of

* CC-4 is a registered trademark of Kollmorgen Corporation.

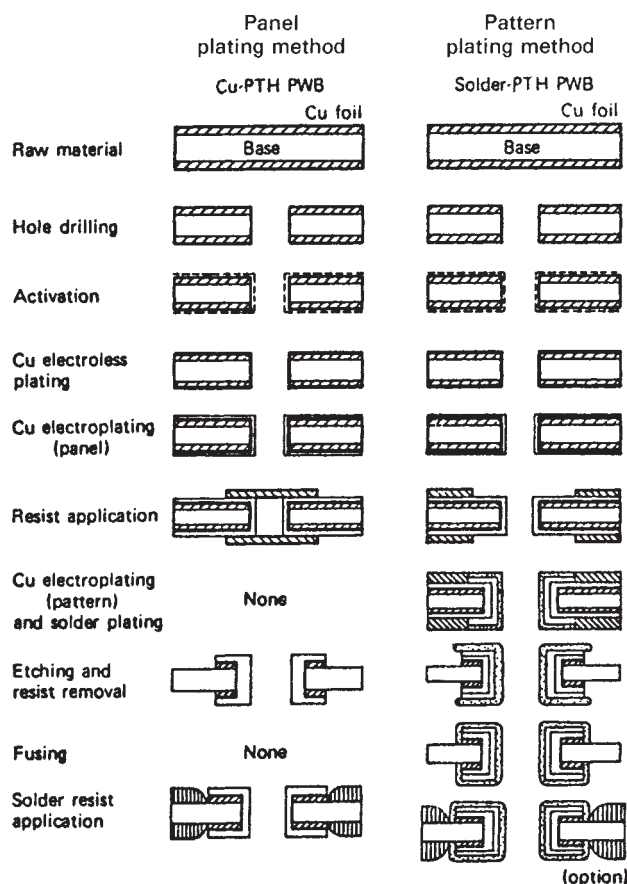


FIGURE 5.6 Key manufacturing steps in panel plating and pattern-plating methods.

solder over the pads and the hole walls. The operation sounds simple, but it requires constant fine-tuning and maintenance of the hot-air solder coater leveler; otherwise, some holes may become heavily clogged with solder and are then useless for component insertion.

One advantage of the pattern-plating method over the panel-plating method is in etching. The pattern-plating method needs to etch only the base copper. The use of ultrathin copper foil (UTC), which is usually $\frac{1}{8}$ or $\frac{1}{4}$ oz thick, offers a real advantage. However, as long as electroplating is used, the pattern-plating method cannot escape from a current distribution problem, regardless of the thickness of the base foils. The panel-plating method by electroplating suffers from the same problem but to a lesser degree. Good current distribution is very difficult to achieve when the boards are not of the same size or type, and particularly if some have large ground planes on the outer faces being plated. When the board has a few holes in an isolated area remote from the bulk of the circuitry, these tend to become overplated, making component lead insertion difficult during assembly. To minimize this current distribution problem, various countermeasures are practiced, such as special anode position, anode masking, agitation, and plating thieves. But none of these offers a decisive solution to the distribution problem, and they are extremely difficult to implement flexibly and effectively in a large plating operation, where a large number of product mixes have to be handled all the time.

CHAPTER 20

MANUFACTURING INFORMATION, DOCUMENTATION, AND TRANSFER INCLUDING CAM TOOLING FOR FAB AND ASSEMBLY

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20.1 INTRODUCTION

The manufacturing of printed circuit boards (PCBs) and assemblies (PCAs) begins with the soft-tooling process. This process is the transformation of customer computer-aided design (CAD) data and specifications into the necessary tools required for manufacturing the bare printed circuit board and populating the assembly. The typical tools required for manufacturing printed circuit boards include artwork for photoprinting of inner conductive layers, outer conductive layers, and solder mask patterns. Artwork is also created for screen-printing patterns for nomenclature and via-plugging layers. Additional tools required include drill and routing numerical controlled (NC) programs, electrical testing netlists and fixtures, and CAD reference soft-tools.

The tooling process for assembly requires assembly drawings, bills of materials (BOM), and schematic or logic diagrams, and includes the solder-paste stencil design, assembly array layout, and the resulting computer numeric control (CNC) programs for component placement, in-circuit test program creations, and possibly the creation of a functional test program. Many of these procedures will be covered in subsequent chapters in the “Assembly” section of this Handbook.

During the tooling process, the customer part numbers are analyzed to determine the compatibility of the design features with the manufacturing process capabilities. Additionally, attempts to optimize the manufacturing of the product at the lowest cost are a primary goal. However, the majority of the costs have been defined before the design is transmitted to the manufacturing site by the PCB designer. An early investment in time by the PCB design team and the manufacturing tooling team can result in the most significant savings in overall product cost.

20.1

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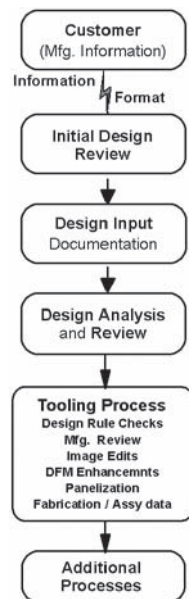


FIGURE 20.1 The soft-tooling process (computer-aided manufacturing [CAM]) for PCB fabrication and assembly.

This chapter describes the PCB tooling process, as defined in Fig. 20.1, including the transfer of information, design reviews, optimization of materials, definition of BOM and routings, tool creation, and additional processes that are required.

20.2 MANUFACTURING INFORMATION

The tooling process begins with the receipt of information from the customer. Unfortunately, although the time required to send information to the manufacturer has decreased to minutes or hours from day(s), a significant issue with the provision of packages to manufacturers is the completeness of the information provided. The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has a new document, IPC-2610, that defines a complete documentation package, including the following:

- IPC-2611, “Generic Requirements for Electronic Product Documentation”
- IPC-2612, “Sectional Requirements for Electronic Diagramming Documentation (Schematic and Logic Descriptions)”
- IPC-2613, “Sectional Requirements for Assembly Documentation (Electronic Printed Board and Module Assembly Descriptions)”
- IPC-2614, “Sectional Requirements for Board Fabrication Documentation (Printed Circuit Board Description Including Embedded Passives)”
- IPC-2615, “Sectional Requirements for Dimensions and Tolerances”
- IPC-2616, “Sectional Requirements for Electrical and Mechanical Part Descriptions (Specification and Source Control Part Descriptions)”
- IPC-2617, “Sectional Requirements for Discrete Wiring Documentation (Wire Harness, Point to Point and Flexible Cable Descriptions)”
- IPC-2618, “Sectional Requirements for Bill of Material Documentation (Complete Listing of Parts, Materials, and Procurement Documents)”

Timely tooling of a part number depends on having the correct information. All features required to exist on the PCB must be defined for the manufacturer. The information is defined via design data, drawings, and textual information. Automated data are encouraged whenever possible.

20.2.1 Required Information

The information and common data formats required to permit the tooling of the PCB include the following:

- Part number information
 Information: This information defines the part number to be built, including revision number, releases, dates, etc.
 Format: This information is typically provided in the part drawing or may be provided as an additional text file.

20.2.2.4 IPC-2581. This is the new IPC coordinated data transfer format. Started in the late 1990s, it is available on some CAD systems. A description is available in Sec. 18.3.4.2.

20.3 INITIAL DESIGN REVIEW

The purpose of the initial design review is to determine the potential fit of the product to the manufacturing facility, determine general cost information, and prepare for tooling. Proper upfront analysis of a product prior to manufacturing or tooling saves time and materials.

It is the responsibility of the manufacturing site to determine the fit of a given product to its capabilities. PCB manufacturing sites should monitor and maintain a list of manufacturing capabilities and a technology roadmap of where the facility is developing additional process capabilities. This list of capabilities defines the acceptability of a product for manufacturing or whether the product is a research and development project.

20.3.1 Design Review

Reviewing the incoming package for design and performance requirements (e.g., line width and spacing, impedance) versus the PCB manufacturing capabilities will define the capability for manufacturing and provide a prediction of the resulting yield. Among the design characteristics that should be reviewed against process capabilities are the following:

Item	Issue
Maximum number of layers	Higher-layer-count products require greater control of processes and tooling tolerances.
Board thickness	Some process or handling equipment may have limitations on board thickness (either too thin or too thick).
Minimum feature width	Finer line widths require better control of artwork and process tolerances. In addition, the relationship of line width to copper weight is significant in providing a well-defined line. Fine lines with lower copper weights are easier to manufacture than fine lines with higher copper weights. For normal impedances, like 50 ohm, thinner lines will require thinner dielectrics.
Minimum feature spacing	Finer feature spacing requires better control of artwork and process tolerances. In addition, the relationship of feature spacing to copper weight is significant. Fine spaces with lower copper weights are easier to manufacture than fine spaces with higher copper weights. Minimum feature spacings affect electrical cross-talk. Closer spacing to reference ground will minimize this cross-talk.
Minimum finished hole size	Smaller holes require higher manufacturing process capabilities and imply (due to design characteristics) finer tolerances on tooling and internal registration systems. The aspect ratio (AR) of diameter to board thickness is a major process concern.

Maximum aspect ratio	Small holes and thick boards result in difficulty during the plating processes and can result in defective products that may or may not pass electrical testing. Plating high-AR holes requires chemistry and process parameter enhancements.
PCB dimensional tolerances	Fine PCB profile or cutout tolerances may result in punching/blanking requirements versus routing, or changes in the routing parameters or programming.
Feature-to-feature tolerances	The location of features on the PCB relative to other features may require alternative materials or process changes to reduce the tolerances.
Hole size tolerances	Consistency in the plating process versus selected drilling hole size and plating densities has significant impact on the capability to control hole tolerances. Adjustments to the PCB design, drill hole size selection, or process parameters may be required to produce an acceptable product with tighter tolerances.
Impedance requirements	The multilayer stack-up thicknesses and tolerances, along with the copper thickness and line widths, must match the nominal impedance and the upper-and lower-acceptability limit. Often, various impedances cannot be fabricated on the same layer.

20.3.2 Material Requirements

Determination of the bill of materials is required during the initial analysis of the design. The determination of the BOM and other material-processing requirements will define the manufacturing facility's capability to produce and its material cost structure. In addition, the definition of the material requirements will be the basis for the generation of the process traveler requirements.

The primary materials requiring definition are those included in the BOM, including laminates, prepregs, copper foil, solder mask, and gold. The materials may be explicitly defined by the PCB customer (e.g., usage of a specific solder mask), or may be implied in the drawings or specifications provided with the tooling package.

Several factors impact the selection of the raw materials, including the following:

- Customer-defined physical constraints, for example, the definition of the physical dimensions between conductive layers
- Customer specification of electrical properties, for example, the definition of the impedance requirements on certain layers
- Manufacturing process capabilities related to lamination thicknesses and tolerances
- Specification of material dielectric requirements, for example, the usage of FR-4 or polyimide
- Specifications of physical operating parameters, for example, the minimum requirements of the glass transition temperature

The determination of the laminates, prepregs, and copper foils are based on the following:

- Standard constructions for the PCB manufacturer of a defined PCB layer count, final thickness, copper weight, and dielectric spacing.

- Custom constructions based on defined physical constraints (e.g., minimum dielectric spacing). These custom constructions are defined through knowledge of the lamination pressing thickness of materials versus copper circuitry densities and the availability of materials from suppliers.
- Custom constructions based on defined electrical property constraints, such as controlled impedances, cross-talk, or capacitance. These custom constructions are typically defined via equations or software models provided with certain product parameters.

The determination of solder mask is based on the customer specifications and drawings. Once the acceptability of the solder masks is defined, the PCB manufacturer selects the acceptable masks based on either preferred process (due to volume or cost) or the design characteristics' interaction with the solder mask. These design characteristics include the following:

- **Tenting or plugging of vias** A hole plugging epoxy may be preferred over liquid photoimageable solder mask with a secondary via plugging process.
- **Platable area densities/higher external copper weights** Thin solder masks may not be able to ensure coverage of high plating.
- **Secondary processes** Post-solder-mask processes may chemically or mechanically alter the appearance of certain solder masks.

The determination of gold requirements is based on the thickness and area of the gold. These factors can be used to calculate the requirement of gold per PCB product.

20.3.3 Process Requirements

The selection of the proper product routing (or traveler) is critical to the upfront analysis of the product acceptability to manufacturing. Considering a typical multilayer PCB product, the product routings can be broken into two parts: the innerlayer pieces and the outerlayer piece.

The product routings of the innerlayer pieces are fairly standard, and are typically as follows:

Step	Typical process requirements
Layer cleaning	Cleaning of the laminate surface via either mechanical or chemical cleaning processes
Imaging	Coating of the laminate with photoresist material and the exposure of the photoresist with artwork defining the innerlayer pattern
Develop-etch-strip (DES)	Developing of the photoresist, etching of the exposed copper, and stripping of the remaining photoresist
Innerlayer inspection	Inspection of the innerlayer piece to the PCB design intent
Oxide	Coating of the innerlayer piece with an oxide layer prior to lamination

One of the few decision points in innerlayer manufacturing is whether the product will require inspection. This decision can be based on the manufacturing facility's process capabilities and the design of the specific innerlayer piece. For example, if the process capability for innerlayer manufacturing of designs at 0.008 in. lines and spaces is 100 percent yield, and the product has been designed at or above 0.008 in. lines and spaces, then the product may not require inspection. Typically, the design package will identify the design technologies (e.g., line width and spacing); however, these should be confirmed during the design analysis and review stage.

The product routings of the outerlayer pieces define the finished product appearance and, as a result, are more complex. Assuming a pattern plating process, the typical outerlayer

process routings for a solder-mask-over-bare-copper (SMOBC)/hot-air-solder-level (HASL) product is as follows:

Step	Typical process requirements
Lamination	Lamination of innerlayer pieces with prepreg and copper foils to create the outerlayer piece
Drilling	Addition of the holes providing pathways for electrical conductivity between outer layer and innerlayer pieces and for other PCB design purposes
Electroless copper plating	Deposition of copper on the surface and in the holes of the product, providing the conductivity necessary for electroplating
Imaging	Coating of the panel with photoresist material, the exposure of the photoresist with artwork defining the outerlayer pattern, and the developing of the outerlayer pattern
Electroplate copper tin plating	The plating of the final circuitry of the product Sacrificial plating over the final circuitry of the product
Strip-etch-strip (SES)	Stripping of the remaining photoresist, etching of the exposed copper, and stripping of the sacrificial plating
Solder mask	Coating of the bare copper product with either dry film or liquid photoimageable solder mask, exposing of the panel with the PCB customer-supplied artwork pattern, developing of the pattern (exposing the sites requiring solder), and curing of the solder mask
Nomenclature	Screening of the nomenclature onto the panel and curing
HASL	Coating of the exposed copper sites with solder, leveling to the customer's requirements of thickness
Depanelization	NC routing of the PCB products from the manufacturing panel
Electrical testing	Electrical testing of the product for conformance to the PCB design
Inspection	Verification of product conformance to specifications prior to shipment to the PCB customer

After the electroplate copper operation, the process may change to meet the surface finish requirements. Some of the alternative steps affecting the outerlayer product routing include the following:

Item	Typical process requirements
Selective gold plating	Before the SES process, the panel is coated with additional resist and the selective sites are exposed. These exposed sites are then plated with nickel and gold. The panel will then proceed through the SES process. The HASL step would be omitted.
NPTH in planes without annular ring	A secondary drilling operation will be required to drill the holes, if the hole is to be located through the copper or the hole/feature size is beyond the process capabilities of tenting. This step may occur at the depanelization step.

CHAPTER 22

INTRODUCTION TO HIGH-DENSITY INTERCONNECTION (HDI) TECHNOLOGY

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22.1 INTRODUCTION

The use of more complex components with very high input/output (I/O) counts has pushed the board fabricator to reexamine techniques for creating smaller vias, and many new or redeveloped processes have appeared on the market. These processes include revised methods of creating holes, such as laser drilling, micro-punching, and mass etching; new methods for additively creating dielectric with via holes using photosensitive dielectric materials; and new methods for metallizing the vias such as conductive adhesives and solid post vias. All of these methods share some common traits. They all allow the designer to increase significantly routing density through the use of vias in surface-mount technology (SMT) pads, to reduce size and weight of product, and to improve the electrical performance of the system. These types of boards are generically called high-density interconnects (HDI). An HDI board typically will have, as an average, over 110 to 130 electrical connections per square inch (20 connections per sq. cm) on both sides of the board.

22.2 DEFINITIONS

Printed wiring boards (PWBs) with microvia hole structures are called different names, such as HDI, SBU (sequential build-up), and BUM (build-up multilayer). However, HDI covers a broader range of high-density wiring boards such as extremely high-layer-count multilayer boards (MLBs) without microvia holes. MLBs with microvia holes are not necessarily built sequentially, nor do they necessarily have build-up structures. These definitions are not appropriate for the discussions in this chapter, and therefore we shall address MLBs with microvia holes simply as *microvia hole boards* (all microvia hole boards are essentially multilayer boards).

Some trade and academic organizations define the microvia hole to be a hole of a certain diameter or less. For example, IPC defines a microvia hole as a hole with a diameter equal to or less than 150 μm . However, when a surface blind via (SBV) hole is formed between layer 1 (L1)

22.3

22.5.3.2.7 Resin-Coated Foil (RCF). Similar to the potential problems faced with photoimageable dielectrics, there is a divergence between the material characteristics required for hole filling and the characteristics that are desirable for an innerlayer dielectric-copper material. Nonetheless, it is likely that the RCF foil materials will prove to be acceptable for filling vias in the limited range of specific applications that exhibit a low-aspect ratio between hole diameter and core thickness.

Liquid dielectric resin is coated more or less the same way as in photovia. However, there is a fundamental difference between photovia and laser via dielectric. In laser via processing, the resin is fully cured before laser drilling (microvia formation). This is a big advantage over photovia materials since the resin movement after hole formation is much more stable than in the case of photovia processing in which resin is fully cured after holes are formed. This resin (hole) movement makes pattern-imaging registration difficult for photovia processing.

22.6 HDI MANUFACTURING PROCESSES

This section discusses processes that employ non-drilling via-hole formation techniques. Through-via drilling is possible below 0.20 mm (0.008 in.), but cost and practicality discourage this. Below 0.20 mm (0.008 in.), laser and other via-formation processes are more cost-effective. Each of the five major via-hole formation processes used for printed circuits is discussed in the following sections.

- Photovia
- Plasma via
- Laser via
- Solid (paste) via
- Insulation displacement via

The manufacturing process for each microvia technology begins with a base core, which may be a simple double-sided board carrying power and ground planes or a multilayer board carrying some signal pattern in addition to power and ground planes. The core usually has plated through holes (PTHs). These PTHs become BVHs. Such a core is often called an *active core*.

22.6.1 Photovia Process

Prior to dielectric material coating by any of the methods described previously, the copper surface of the base core must be treated by an adhesion promotion process to ensure good adhesion of dielectric material to the copper surface. Today, very few manufacturers use oxide treatment for this purpose. The most popular adhesion promotion treatment is a special etching process offered by many suppliers of chemicals. This step is common to all microvia processes.

Dielectric resin is semicured after coating to eliminate tackiness, and then the hole pattern is exposed by photoexposure processing. The usual photodeveloping process creates microvia holes and the dielectric is fully cured, typically at 160°C for about 1 hour. Then, the panel goes through a permanganate etching process to remove any residual resin at the bottom of the hole and simultaneously create microporous surfaces that act as an anchor and ensure desirable peel strength after copper plating.

The level of peel strength is controversial. Minimum peel strength required for chip package substrates is about 600 g/cm², but motherboard users, particularly cell phone makers, demand a minimum of 1.0 kg/m² or more in order for cell phone handsets to withstand drop tests. Laser via materials usually yield stronger peel strength because of fillers that can be added to dielectric resin. When etched, these fillers generate a superior microporous surface structure needed for strong peel strength.

After permanganate etching, the panel is catalyzed and metallized in an electroless copper bath and panel-plated galvanically to desired thickness. Some photovia process practitioners roughen the resin surface mechanically by brushing or liquid honing prior to catalyzing. Then, the conductor pattern is formed by dry-film tenting and etching. Some manufacturers prefer to use the pattern-plating method for this purpose. Very few microvia board manufacturers use direct metallization methods for metallizing holes prior to galvanic plating. Several Japanese manufacturers use electroless copper all the way to the desired thickness in panel plating and use a positive electrodeposited (ED) system to achieve fine lines and very small annular rings.

One important step in microvia hole board fabrication when resin is the dielectric choice, whether the process is photovia or laser via, is the removal of residual catalysts (normally palladium) entrapped in a microporous surface that can cause migration. The process used in this step is normally a trade secret.

Photovia processing is now used primarily to fabricate semiconductor chip package substrates because a large number of holes can be formed in one photoexposure and development step. However, as mentioned previously, photovia processing suffers more from material shrinkage than laser via processing after full cure, and hole locations tend to move randomly, which makes subsequent registration for patterning difficult. Because of this problem, photovia users limit the size of the panel to be much smaller than the usual panel size prevalent in motherboard fabrication to about 400 mm × 400 mm. Small hole formation is also difficult with the photovia process. As a result, even makers of package substrates are now resorting more to laser via processes as the laser-drilling speed is being improved. Photovia process users engaged in mass production are found only in Japan today. All photodielectric processes have certain characteristics in general. Table 22.11 lists the typical processing factors. A standard photovia process sequence is described in Fig. 22.18a.

TABLE 22.11 Four Typical Photodielectrics (Three Epoxy and One Polyimide) and the Processing Parameters for Coating, Exposure, Developing, Desmears, and Metallization

	Product A	Product B	Product C	Product D
Product	L-PID, negative	L-PID, negative	L-PID, negative	DF-PID, negative
Material	Epoxy	Epoxy	Polyimide	Epoxy
Preclean	Chemical clean	Pumice jet	Br. oxide	Chemical clean
Apply PID	Curtain coat 150–400 cps	Curtain coat 200–600 cps	Extrusion coat 12,000–25,000 cps	Vac. lam. 60 s @ 65°C
Thickness	50 μm	50 μm	37 μm	63 μm
Drying	15 h @ 90°C	6 h @ 25/40°C 3 h @ 140°C	5 h @ 25°C 15 h @ 125°C	N/A
Exposure	800–1,200 mJ/cm ²	800–1,600 mJ/cm ²	2,000–3,000 mJ/cm ²	700–1,200 mJ/cm ²
Heat bump	15 h @ 90°C	12 h @ 125°C	N.R.	20 h @ 85°C
Development	Aqueous proprietary 75 min @ 35°C	Organic GBL 60 min @ 30°C	Organic proprietary 150 min @ 30°C	Aqueous proprietary 60 min @ 35°C
Final cure	UV: 1.0 J/cm ² + 60h @ 145°C	60 h @ 150°C	120 h @ 175°C	UV: 2 J/cm ² + 60h @ 150°C
Roughen				
Swell	4 h @ 65°C	4 h @ 75°C	2 h @ 65°C	5 h @ 60°C
Etch	4 h @ 80°C	8 h @ 75°C	1 h @ 75°C	10 h @ 75°C
Neutralize	6 h @ 50°C	6 h @ 50°C	3 h @ 45°C	3 h @ 25°C
Metallize: electroless Cu	0.3–0.5 μm	0.7–1.0 μm	0.3–0.5 μm	0.4 μm
Bake	20 h @ 90°C	60 h @ 150°C	60 h @ 150°C	15 h @ 90°C
Electroplate				

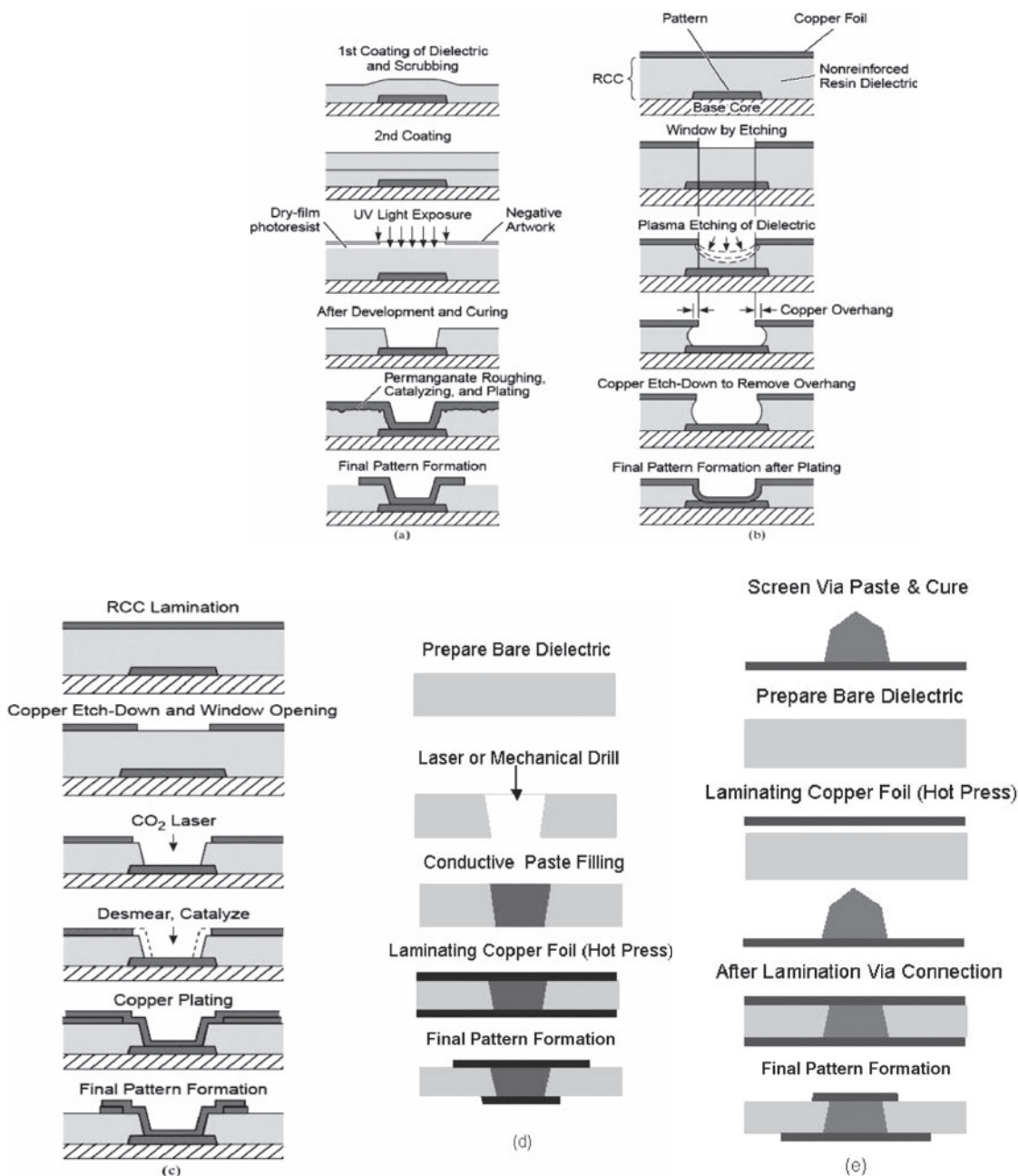


FIGURE 22.18 Standard HDI manufacturing processes: (a) a typical photovia process with liquid resin dielectric; (b) the standard plasma via process with RCC; (c) the semiconformal laser via process; (d) the standard conductive (paste) solid via process; (e) the insulation displacement via formation process.

22.6.2 Plasma Via Process

Plasma via processing was developed by a Swiss PWB maker, Dyconex. Products made with the plasma via process are called DYCOstrate.

There are many variations to the plasma via process, one of which is illustrated in Fig. 22.18b. Today, it is mainly used to fabricate sophisticated flex and flex-rigid wiring boards in small quantities.

First, an opening or window is made through copper foil by a normal etching process. When plasma etching is applied through this window, the shape of holes tends to be like a bowl (as shown in Fig. 22.28b), which is not suitable for reliable plating (although new plasma-etching equipment claims to have solved this problem).^{7,8} Another problem is related to how the microvia hole is formed. The copper edge of the window hangs out over the hole, which results in poor reliability after panel plating. Therefore, to ensure reliable plated holes, a secondary etching is necessary to remove this copper overhang. One good thing results from this secondary etching, however: Since surface copper is thinned, formation of finer conductors is made easier. Nevertheless, by the time the panel is ready for plating for subsequent conductor pattern formation, it takes several times longer than other processes in a mass-production environment.

Plasma via processing is effective for forming through holes on flexible materials since holes are formed by plasma etching from both sides of the film and the bowl effect is minimized.

Plasma via etching evolved from the traditional process of plasma desmearing of through holes. Different gas, magnetrons, and equipment fixturing are employed by current plasma via-etching equipment. The plasma is generated in a partial vacuum filled with a mixture of oxygen, nitrogen, and chlorofluoro (CF_4) gasses. Microwave magnetrons create the plasma field and special low-frequency kilowave units help provide rapid etching of organics.

22.6.3 Laser Via Process

Laser via processing is by far the most popular microvia hole formation process. But it is not the fastest via formation process. In Fig. 22.19, the chemical etching of small vias is the fastest, with an estimated rate of 40,000 to 50,000 vias per second. This is also true of plasma via

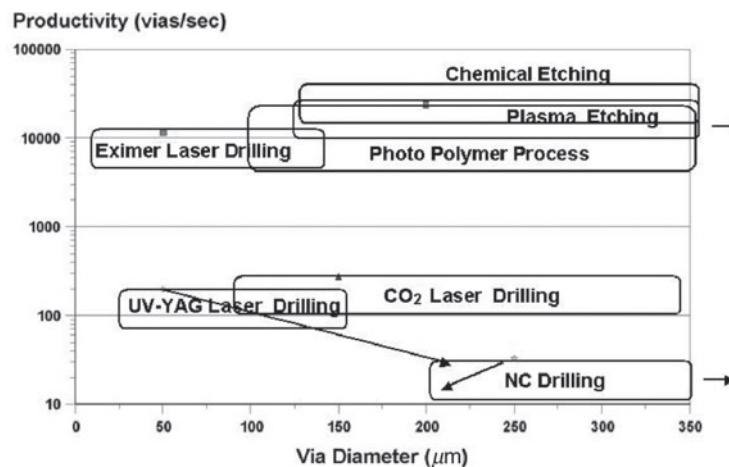


FIGURE 22.19 The various rates of via formation based on diameter and method of via ablation, from chemical, plasma, photo and laser techniques.

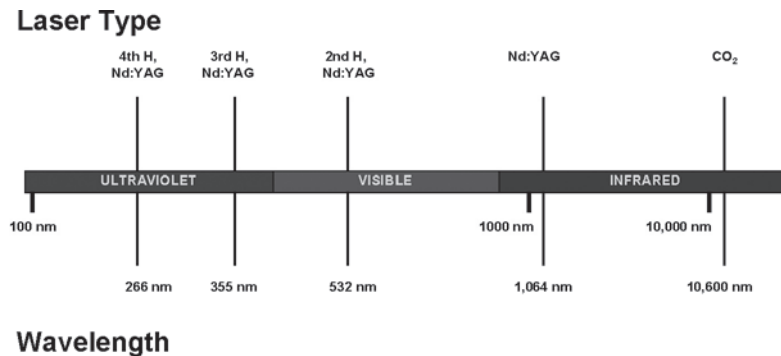


FIGURE 22.20 The wavelengths used by laser via drilling from infrared to ultraviolet region, including the harmonics of Nd:YAG lasers.

formation and photovia formation. These are all *mass-via-formation* processes. Laser drilling is one of the oldest microvia generation techniques.⁹ The wavelengths for laser energy are in the infrared and ultraviolet region. Figure 22.20 shows the five major wavelengths used in current laser drills. The absorption curves of many organic dielectrics epoxy, polyimide, matte copper, and glass fibers are shown in Fig. 22.21. Laser drilling requires programming the beam fluence size and energy. High-fluence beams can cut metal and glass, whereas low-fluence beams cleanly remove organics but leave metals undamaged. A beam spot size as small as approximately 20 microns (<1 mil) is used for high-fluence beams and about 100 microns (4 mil) to 350 microns (14 mil) for low-fluence beams.^{10,11}

However, there are many variations. For the purpose of drilling microvia holes, there are four laser systems: UV/Yag laser, CO₂ laser, Yag/CO₂, and CO₂/CO₂ combinations. Then there are three dielectric materials: RCC, resin only (dry-film or liquid resin), and reinforced prepreg. Therefore, the number of ways to make microvia holes by laser systems is driven by the permutation of four laser systems and these three dielectric materials.

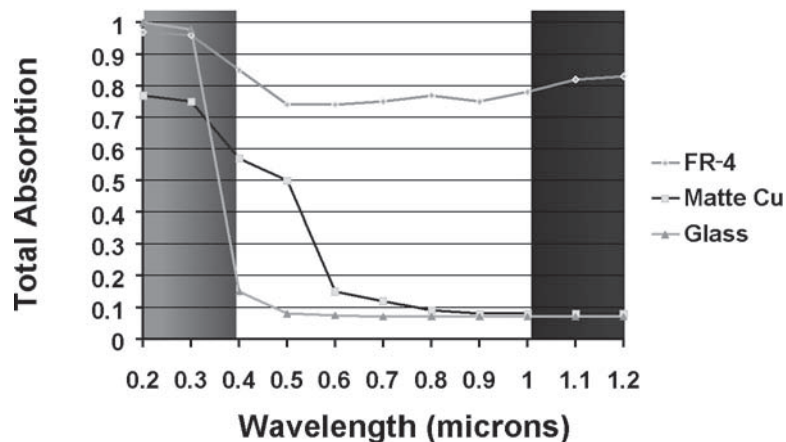


FIGURE 22.21 The absorption wavelength of different materials respond to different wavelength of laser energy. Epoxy, copper and glass of laminate are ablated by the UV wavelength but only the resin is ablated by the CO₂ wavelengths.

There are several factors to observe in laser via processing: position accuracy of lased holes (microvia holes), uneven diameters of holes, dimensional change of the panel after curing dielectric, dimensional change of the panel due to temperature and humidity variations, alignment accuracy of the photoexposure machine, unstable nature of negative artwork, and so on. These should be carefully monitored and are important for all microvia hole processes.

22.6.3.1 UV/Yag Laser. A Yag laser can penetrate copper; therefore, it is not necessary to pre-etch the window when the choice of dielectric is RCC or a copper-foil/prepreg combination.

Positioning accuracy in relation to the capture pad is good, but there are weaknesses associated with the Yag laser. The speed of drilling (ablation) is slower than the CO₂ laser, particularly when a hole diameter is equal to or larger than 125 μm , because the laser beam is very small. Therefore, it is necessary to do trepanning (spiral drilling pattern), which results in longer drilling time. Another weakness is the Yag laser's sensitivity to the thickness of dielectric material. If the thickness of the RCC's resin is not even, the Yag laser beam, the power of which is adjusted to remove the thicker part of the resin, may damage the capture pad. If adjusted to the thinner part, it may not reach the capture pad.

Although the Yag laser can penetrate copper and glass-reinforced prepreg, the situation is worse in this material than with RCC. The laser power must be adjusted to penetrate through the crossover part of woven glass. Then, when the laser beam hits the part of prepreg where there is now a glass bundle (opening), the beam can really damage the capture pad. To avoid this problem, the operator must reduce the laser power and apply laser ablation for a longer duration, which increases drilling time considerably. Depending on the construction of the dielectric layer through which the Yag laser beam must penetrate, the drilling speed must be adjusted to about 3 to 50 holes per second when glass-reinforced dielectric is used.

When the dielectric is RCC, the speed of the currently available UV/Yag laser is somewhere around 100 to 300 holes per second.

When the dielectric is resin without copper foil, a CO₂ laser is the best since a CO₂ laser can offer much faster drilling speed (a single-head CO₂ laser can drill as many as 25,000 holes per minute, including overhead such as loading a panel onto the drilling table and registering the panel).

The best feature of the UV/Yag laser drilling machine is its ability to drill a very small hole (down to 20 to 30 μm , whereas the smallest hole a CO₂ laser can drill is 50 μm in a mass-production environment) and its superior position accuracy through RCC.

For higher-speed drilling, even Yag laser users are now etching copper foil down to 6 to 9 μm , the process more frequently seen in CO₂ drilling.

22.6.3.2 CO₂ and Twin CO₂. A CO₂ laser beam cannot penetrate copper foil unless the foil is very thin, less than 5 μm , and the surface is treated to be dark to absorb the CO₂ laser beam (this process is called CO₂ laser direct drilling and will be treated later).

When the surface is resin only, a single-headed CO₂ laser machine can drill holes at the rate of 20,000 to 25,000 per minute depending on hole density and distribution. The drilling speed continues to increase. The denser the hole, the faster the drilling speed because time lost by table motion is minimized. A dual-head CO₂ machine can boost drilling productivity by about 70 percent compared to a single-head machine.

Manufacturers of dielectric resins mix fillers in the resins to enhance peel strength. Some fillers can slow down the drilling speed of a CO₂ laser beam (beam absorption is weaker in this case). For example, when the required dielectric thickness is 60 μm , resin is coated twice, which is a frequent practice to produce a thick coating. The first coating is made with resin without filler (40 μm), and the second coating (20 μm) is resin with filler. Since the laser beam goes through a thin layer of filled resin, the speed degradation is minimized.

The most desirable shape of drilled microvia holes is tapered, which is accomplished by pulse drilling. Normally, two to three pulses are used. When three pulses are applied on the same spot continuously, the capture pad may be overheated and excessive epoxy smear may result. Therefore, when three pulses are to be applied, the entire panel is drilled first by two

pulses and then the third pulse is once again applied to all holes. This way, the quality of the holes is ensured, although it takes longer to drill.

When the choice of dielectric is RCC, the opening or window must be formed first on copper foil, as in the case of plasma via. Prior to window formation, an etching process thins the surface copper, usually down to 6 to 7. This process is sometimes called *half-etching*.

Half-etching yields a few benefits. Window formation is made easier, and formation of fine-line conductors is also made easier. $\text{H}_2\text{O}_2/\text{H}_2\text{SO}_4$ etchant is often used for this purpose for even thickness. As mentioned previously, this half-etching procedure is also becoming common for Yag laser users.

There are two variations to CO_2 laser drilling through a window opening. One is called *conformal* and the other *semiconformal* (see Fig. 22.18c).

In the conformal method, a laser beam with a diameter larger than the window opening is used. Straight ablation of dielectric results in a bowl-shaped hole, as in the case of plasma via. Therefore, improved systems use laser beam diameters slightly larger than the window opening, and beams are pulsed to minimize the bowl effect.

In the semiconformal method, a laser beam with a diameter slightly smaller than the window opening is used. This results in a slight step when plated afterward, as shown in Fig. 22.18c. To minimize this step, half-etching is important in semiconformal drilling.

Some manufacturers using CO_2 drilling etch down copper completely after RCC lamination. The dielectric surface below copper is already microporous, which generates good adhesion except prior to the RCC stage. Therefore, some special treatment is applied to the resin surface, such as electrolessly plated nickel layer, prior to copper plating, but such treatment is kept secret.

The RCC approach suffers from misregistration of window opening to capture pad when the surface and capture pad diameter becomes less than $250\text{ }\mu\text{m}$, which causes serious defects (see Fig. 22.22). Laser via process practitioners have several solutions to this problem. They can use liquid resin or resort to a Yag or Yag/ CO_2 laser. Since a Yag laser can break through copper foil, the beam can be directed to the capture pad position accurately. Another choice is to use laser direct imaging (LDI) for window etching in order to benefit from the speed of the CO_2 laser.

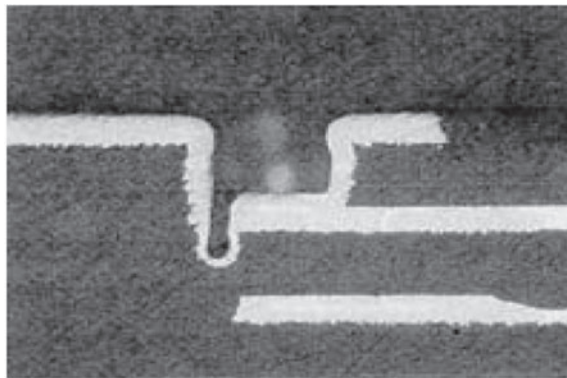


FIGURE 22.22 Misregistration of laser hole to capture pad.
(Courtesy of *Ibidem*.)

Another solution is to use CO_2 laser direct drilling. The advantage of using RCC is the pre-established peel strength. Manufacturers go through delicate steps to establish the appropriate peel strength when using liquid resin. The degree of resin cure, permanganate etching, control, and regeneration of the permanganate solution affects the resultant peel strength as well as cost.

In this laser direct drilling method, copper foil is etched down to about 5 μm and its surface goes through oxide treatments such as black oxide or other methods, typically as alternatives to oxide treatment, which is normally an etching process. The copper thickness is further reduced by 1 μm , and the surface color becomes dark, allowing the CO_2 beam to penetrate.

Alternatively, ultrathin copper RCC may be used. Carrier foil, usually copper foil of 70- μm thickness (2 oz.), is coated with a very thin layer (10 to 20 μm) of current conductive release film, and a thin foil of 3 to 5 μm is plated. After such RCC is laminated to the core, the carrier film is peeled off and the surface condition is the same as etched-down copper. Drilling speed in this direct CO_2 laser drilling method is degraded by 30 to 40 percent compared to that of straight resin drilling, but the registration to the capture pad is ensured.

22.6.3.3 Yag/ CO_2 . This combination is particularly useful for a copper/prepreg structure. The Yag laser offers good position accuracy and cuts through copper, but it tends to leave glass fibers sticking out in the hole after prepreg drilling. And as mentioned before, it is sensitive to dielectric thickness variation. The CO_2 laser beam cuts through glass fiber more cleanly than the Yag. In this combination laser drilling, the power of the Yag laser beam is adjusted to cut through copper and remove a portion of glass fiber and leaves the finishing to the CO_2 laser. The speed of drilling is governed by the speed of the Yag laser and is therefore slower than a pure CO_2 laser. However, this is the preferred laser-drilling machine for fabricating infrastructure types of PWBs, such as ones used for servers, network routers, and base stations that typically have copper/prepreg surface structures. The size of the panels used to fabricate such boards is usually large; therefore, the positioning accuracy of the Yag laser is preferred. Microvia hole boards used by the automotive industry also have this copper/prepreg structure.

The speed of drilling by a Yag/ CO_2 machine is much slower than that of a CO_2 laser. However, the number of microvia holes to be drilled for infrastructure boards is normally one magnitude less than that seen in cell phone applications, in which the number of microvia holes can reach as many as 650,000 to 700,000 per m^2 . Furthermore, the price of infrastructure boards is much more than that of mass-produced cellular phone motherboards. Therefore, slower speed of drilling, which means higher drilling cost, does not affect the total cost of manufacturing.

Residual glass fibers in the hole that can affect reliability may be removed chemically or mechanically. Mechanical removal is preferred. Blasting with aluminum oxide (about 20 μm diameter particles) is commonly used to remove glass fibers and smears as well. An excimer laser is also used to remove smears in the hole by a sweeping motion through the copper opening. In both cases, it takes about 30 sec. to desmear one side of the panel.

22.6.4 Dry Metallization (Conductive Inks, Conductive Paste, and Insulation Displacement)

Three types of dry metallization are covered: conductive ink, conductive paste, and insulation displacement. Conductive ink describes a single-layer dielectric with microvias formed by photoimaging, laser, or insulation displacement. A conductive paste is used to fill the microvias and act as the conductive path between layers. Surface metallization may be accomplished either by laminating copper foil onto the dielectric surface or by chemical deposition. This process is shown in Fig. 22.18d.

Insulation displacement is a unique process in that the silver conductive paste is screened on copper foil and cured. The conductive paste forms a "pointed" via that penetrates conventional prepregs during lamination and adheres to the copper foil on the reverse side, forming a via. Figure 22.18e shows this via formation process.

Standard activities concentrate on the use of photoimaging and screen printing while overcoming the limitations and expense associated with processes such as plating and etching. The concept is built on the use of a photoimageable dielectric to produce both vias and circuit

CHAPTER 23

ADVANCED HIGH-DENSITY INTERCONNECTION (HDI) TECHNOLOGIES

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23.1 INTRODUCTION

Since the introduction of HDI in the mid-1980s (HP-Finstrate, Siemens's MicroWiring, and IBM's Surface Laminar Circuit [SLC] technology; see Figs. 22.1, 22.2, and 22.3), many variations of making high-density interconnect (HDI) wiring boards have been developed and implemented for mass production. However, if one technology is to be judged in terms of volume produced and picked as a winner, laser-drilling technology is the one. Other methods are still used by a number of printed wiring board (PWB) manufacturers, but on a much smaller scale.

The purpose of this chapter is to examine a variety of HDI fabrication processes as seen in Fig. 23.1. However, a greater emphasis will be placed on the laser-drilling process (hereinafter *laservia*) since it is the most popular process today and it seems its popularity will grow in the future. It must be understood that interconnect via hole (IVH) formation is just one element of fabricating HDI wiring boards. The other two important factors are the various dielectric materials and the methods of metallization. Fabrication of HDI wiring boards with microvia holes involves many new processes not common to conventional board fabrication. Therefore, additional emphasis will be placed upon these new fabrication processes that are common to other microvia technologies.

23.2 DEFINITIONS OF HDI PROCESS FACTORS

The 21 different HDI processes shown in Fig. 23.1 have three basic fabrication factors in their process makeup:

- Dielectric materials
- IVH formation
- Methods of metallization

23.1

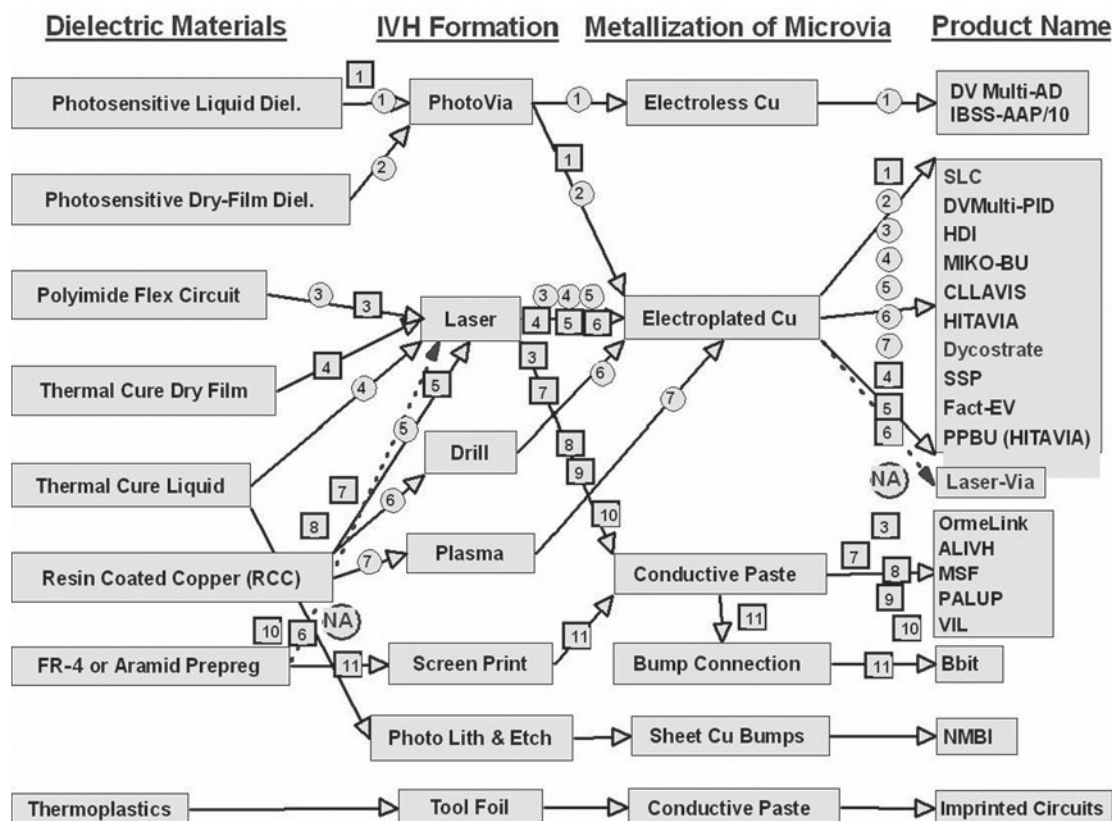


FIGURE 23.1 The HDI technologies in use today are made up of three factors: the dielectric materials, the methods of IVH formation, and the method of metallization of those z-axis via connections. In recent years up until now, 21 different HDI processes have been used.

23.2.1 Dielectric Materials

Eight different general dielectric materials have been used in the current or past HDI processes. IPC slash sheets such as IPC-4101B and IPC-4104 cover many of these, but many are not yet specified by IPC standards. The materials are:

- Photosensitive liquid dielectrics
- Photosensitive dry-film dielectrics
- Polyimide flexible film
- Thermally cured dry films
- Thermally cured liquid dielectrics
- Resin-coated copper (RCC) foil
- Conventional FR-4 cores and prepregs
- Thermoplastics

23.2.2 Interconnect Via Hole Formation

Seven different methods of forming the IVHs have been used in current or past HDI processes. Laser drilling is the most prominent, but the other six come into use also. The methods are:

- Photo processes to define vias in photodielectrics
- Various laser-drilling methods, including UV-Yag, UV-Eximer, and CO₂
- Mechanical drilling
- Plasma drilling
- Screen printing of via pastes
- Photo and etch of solid vias
- Toolfoil

23.2.3 Method of Metallization

Four different methods of metallizing the IVHs have been used in the current or past HDI processes. The methods are:

- Fully additive electroless copper
- Conventional electroless and electroplating copper
- Conductive pastes
- Fabricating solid metal vias

23.3 HDI FABRICATION PROCESSES

The three basic and original HDI processes are laser drilling laminate (Finstrate) and flexible materials (microwiring), photodielectrics with SLC and plasma-etching polyimide (Dycos-trate). These and the other 18 HDI processes have been integrated into standard printed circuit manufacturing flows. There is no standard way to organize these processes, but the method of IVH formulation is the most unique characteristic of each process and will be used for this purpose.

23.3.1 Photo-Via Technologies^{1,2}

23.3.1.1 IBSS-AAP10 System. The Interpenetrating Polymer Network Build-Up Structure System (IBSS) is a new photodielectric. This photo-imageable dielectric (PID) is a proprietary photodielectric developed by Ibiden of Japan. It complements Ibiden's older epoxy type of photo-redistribution layer technology, IP-10.

23.3.1.1.1 Structure. IBSS is specifically formulated for integrated circuit and flip-chip packages and has a high T_g and flexibility. The bismaleimide-triazine (BT) core also provides high-temperature resistance. A typical IBSS structure and its features are illustrated in Fig. 23.2.

23.3.1.1.2 Manufacturing Process. IBSS is a liquid system applied by roller coater to a rigid core, typically BT. The coating is cured and photodeveloping creates the vias. The IBSS requires an aggressive swell-and-etch because of the higher-temperature nature of the photo-dielectric (PD). The metallization is fully additive copper, also proprietary to Ibiden.

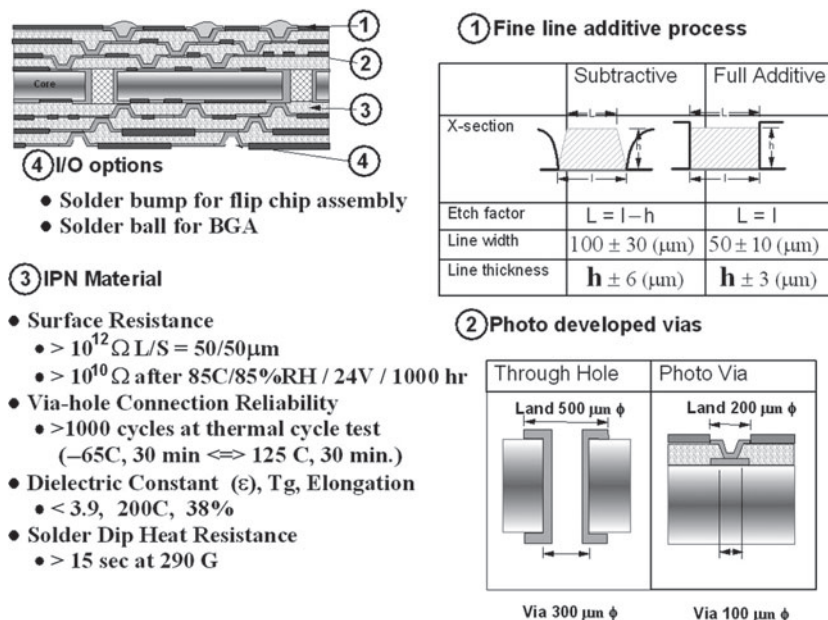


FIGURE 23.2 The IBSS/AAP10 multilayer substrate structure.

The imaging for additive metalization uses a permanent dry-film photoresist. For additional layers of dielectric, an adhesion promoter is applied to the surface copper. Figure 23.3 outlines the IBSS process.

23.3.1.2 Surface Laminar Circuits. SLC technology was the first of the PID microvia, build-up technologies to reach the interconnect market in high volume. Development of SLC technology began during the late 1980s at IBM (Yasu, Japan), and the first product was introduced in 1990.¹ The first flip-chip, direct-chip-attach (FC/DCA) product employing SLC technology was shipped from Yasu in 1992, and in 1995 IBM Endicott, New York, shipped its first printed wiring boards that utilized SLC technology.² Used by many original equipment manufacturers (OEMs) in Japan, the SLC process provided the high-density interconnect technology for Sony's first digital Camcorder, the DCR-PC7, seen in Fig. 23.4. This eight-layer build-up structure had two SLC layers on each side of a four-layer core. The assembly density of this was over 612 pins per sq. in. due to the wall-to-wall 0.5 mm. pitch chip scale package (CSP) used.³

The most suitable photosensitive dielectric was the photo-imageable solder masks, due to their proven compatibility with printed circuit assembly processes, ability to withstand exposure to service environments, and possession of the necessary via-imaging characteristics. SLC technology was originally developed and implemented with a liquid PID solder mask applied by curtain coating. In 1995, it was also qualified with a dry-film PID with virtually identical electrical properties. The dry-film version did not require the extensive surface grinding processes that the liquid PID process required.

PID technology is based on photoimageable polymeric systems to form blind microvias in dielectric material between layers of circuitry. The use of PIDs allows all microvias on a panel to be formed simultaneously, with no incremental-per-via cost. Its use is particularly advantageous on applications with high densities of vias (e.g., more than 50,000 on an 18 in. $\times$ 24 in. panel).

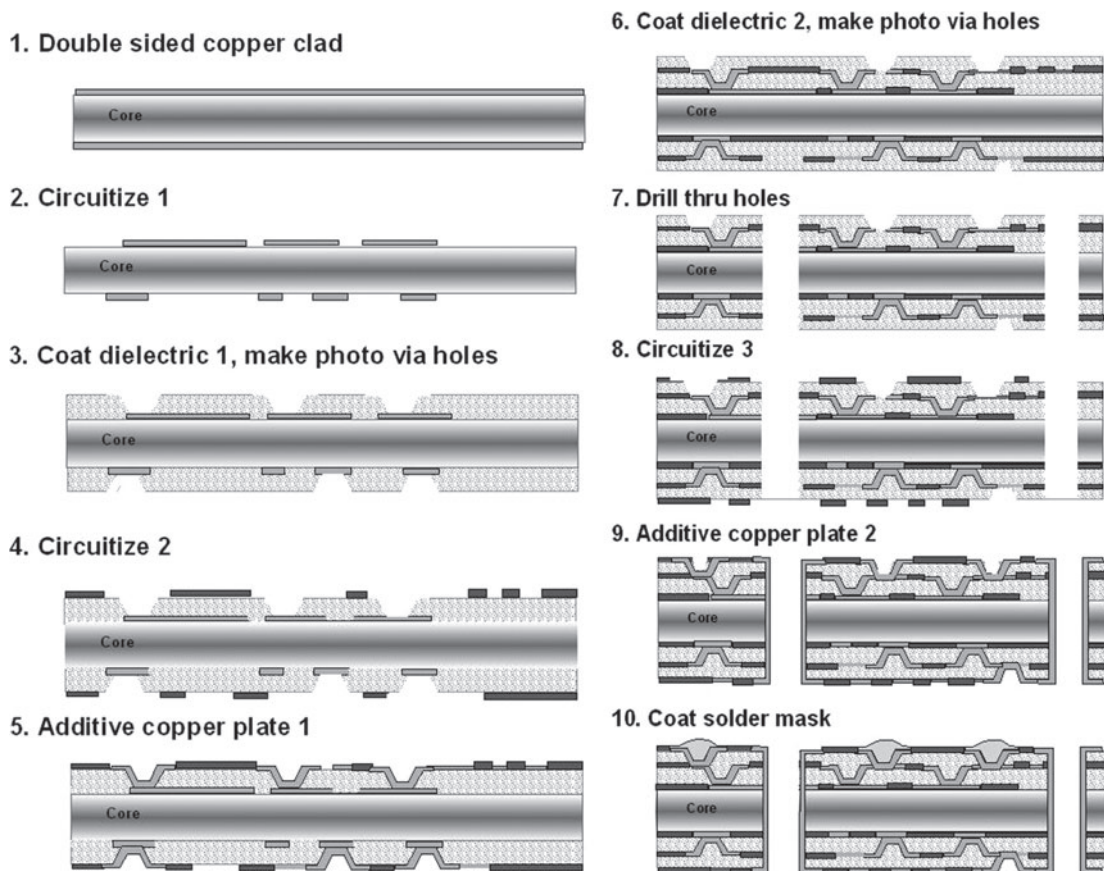


FIGURE 23.3 The IBSS/AAP10 multilayer substrate fabrication process.

23.3.1.2.1 Liquid Versus Dry PID. A typical flowchart of the PID technology fabrication process, including options for multiple build-up layers and a multilayer core, is shown in Fig. 23.5. At this level in the process, PID technology is the same whether a liquid or dry-film PID is used.

Liquid and dry-film PIDs do provide slightly different via wall profiles. The liquid PID has tapered via walls, whereas the dry-film PID has essentially vertical via walls. The tapered via walls provide good plating coverage on the via walls and base. Vertical walls allow for a smaller via top opening, and correspondingly smaller capture land for a given via bottom diameter.^{4,5}

23.3.1.2.2 Tools. The use of a liquid PID requires two unique pieces of equipment: a coater of some variety, either curtain, slot, roller coater or screen printer (with associated drying ovens), and a leveling tool (surface sander). A leveling tool is required to planarize the surface of the cured liquid PID to accommodate fine-line photolithography on the surface. Liquid PID provides a conformal coating over underlying circuit features, producing nonuniform planarity. The leveling operation also removes a lip of exposed PID that overhangs the via openings in these processes. Many liquid PIDs have a self-leveling characteristic and do not require any other leveling.

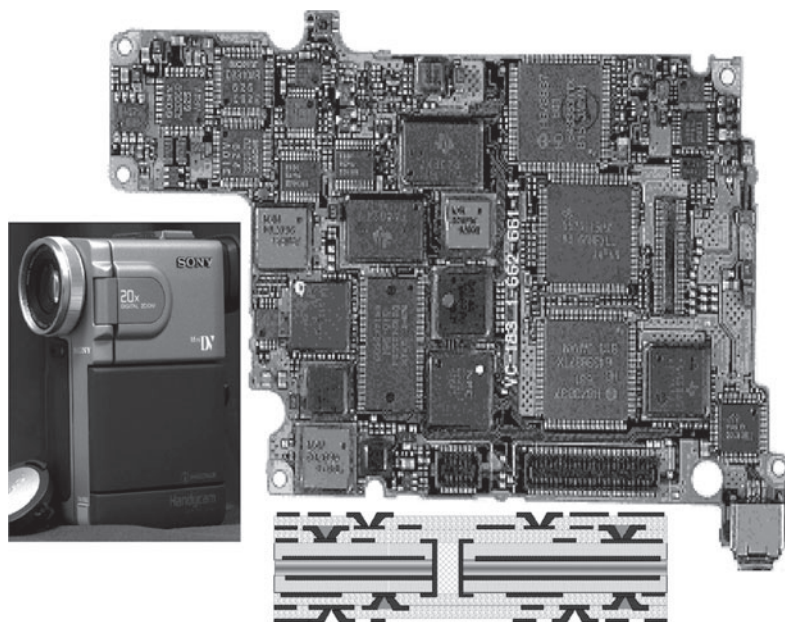


FIGURE 23.4 The Sony DCR-PC7 digital camcorder utilized the SLC process for the 2+4+2 build-up structure and 0.5 mm CSPs to achieve over 600 connections (pins) per sq. in.

The use of a dry-film PID requires only one unique piece of equipment: a vacuum laminator. Vacuum laminators are common at printed circuit fabrication shops; in addition, the capital to obtain one is significantly less than for a curtain or slot coater. The dry-film PID has excellent planarization and does not require a leveling process due to the film's low solvent content, low shrinkage, and vacuum lamination process.^{6,7}

PID technologies were originally conceived as an alternative to multilayer lamination as a way to make multilayer PWBs. PID technology builds up each surface signal layer on top of the previous layers in a sequential fashion. The base under all of the outer build-up layers is a conventional double-sided or multilayer circuit board containing voltage, ground planes, and even signal layers. Mechanically drilled and plated holes are used only in the core layers, to make connections to the backside of the laminate base and accommodate mounting pinned components. There is greater wiring density to use plated through holes (PTHs), which extend only through the base printed circuit structure and not through the build-up layers, especially when two or more build-up layers are used. Figure 23.6 provides additional details of the SLC manufacturing process of multilayer printed circuit boards.^{8,9}

23.3.1.3 DV Mult-PID. DV Mult-PID is from NEC. This structure uses a PID primarily as an integrated circuit (IC) substrate and for high-density electronic products. It is capable of three build-up layers per side. Figure 23.7 shows a typical NEC high-density board. The use of a dry-film PID requires only one unique piece of equipment: a vacuum laminator. Vacuum laminators are common at printed circuit fabrication shops; in addition, they cost much less than a curtain or slot coater. The dry-film PID has excellent planarization, does not require a leveling process due to the film's low solvent content, low shrinkage, and vacuum lamination. The modified structure of DV Multi-AD uses laminates and RCC for the build-up layers and fully additive electroless plating. Figure 23.8 illustrates this structure and manufacturing process.

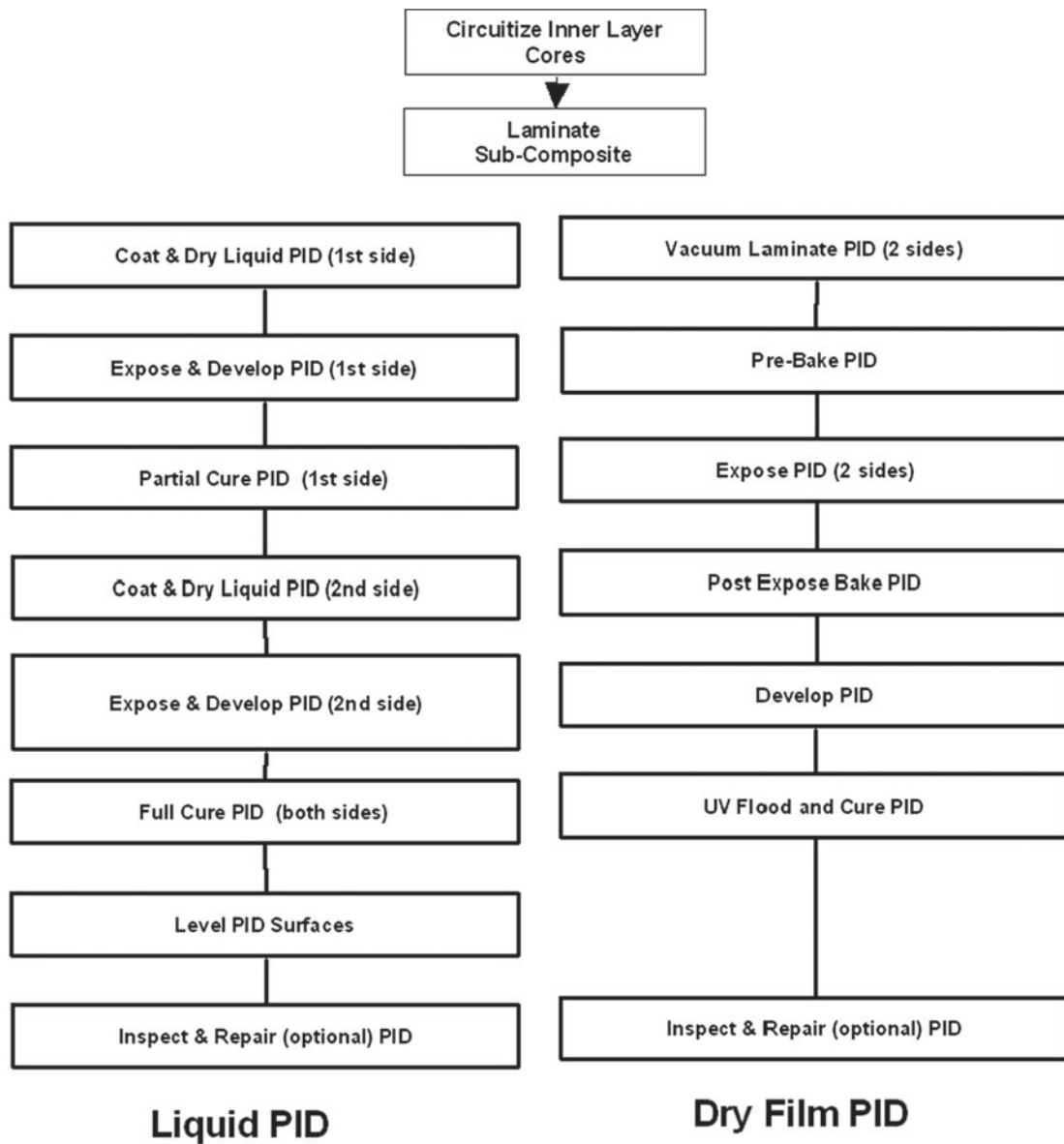


FIGURE 23.5 The manufacturing flows for the two-major SLC manufacturing processes.

23.3.2 Laser Via Technologies^{(3-5), [3-6], [7-10]}

Circled processes 3, 4, and 5, as well as squared 3 through 10 in Fig. 23.1, utilize a laser drill via generation technique. This process was first used in the late 1970s to drill small holes in G-10 laminate for buried vias in mainframe computer boards by IBM for its 3081 system and by Burroughs. (Attempts to find pictures of these products proved unfruitful.) The Hewlett

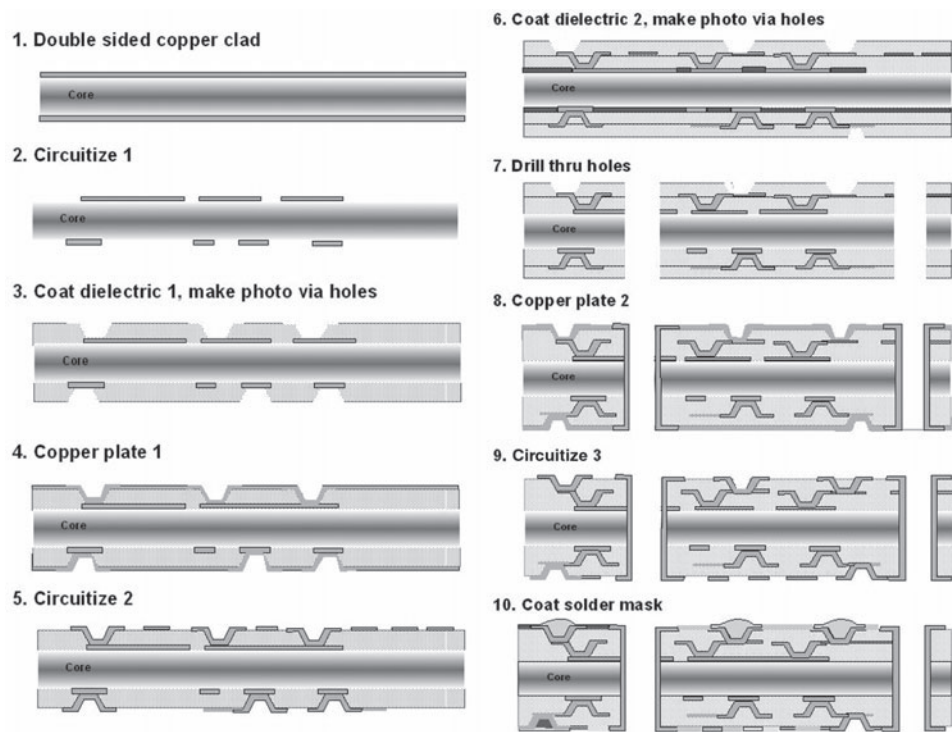


FIGURE 23.6 Additional details of the SLC manufacturing process.

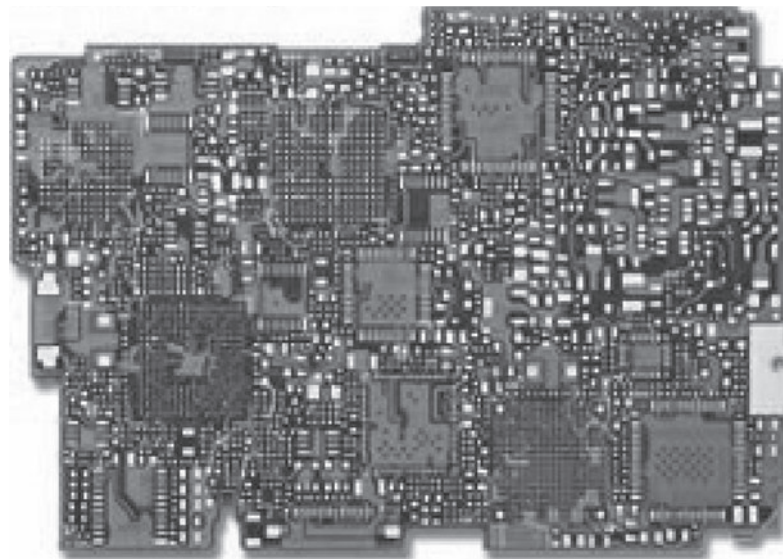


FIGURE 23.7 A typical high-density DV Mult-PID board from NEC.

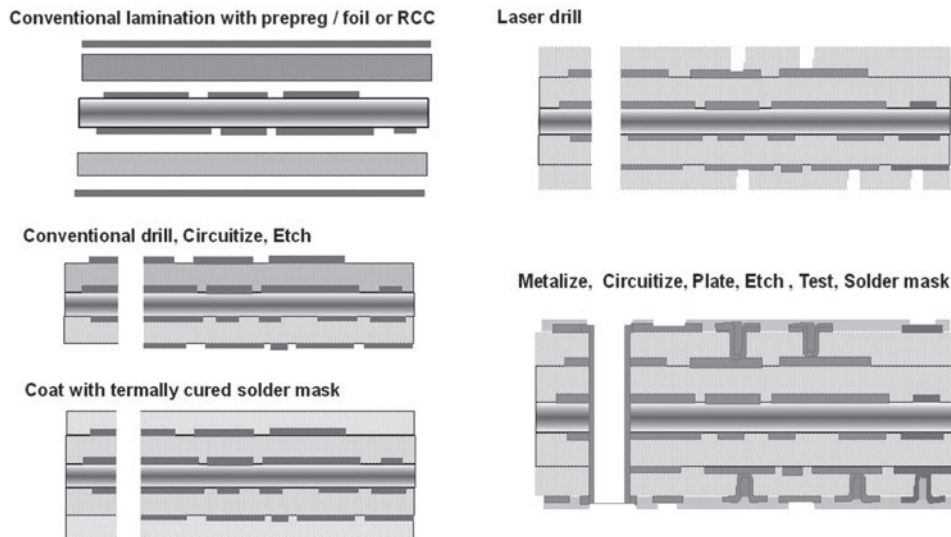


FIGURE 23.8 The DV Mult-PID board manufacturing process.

Packard laser-drilled Finstrate family of boards, first produced in 1983, is shown in Chapter 22. Siemens' laser-drilled microwiring was produced since 1987.

23.3.2.1 High-Density Interconnect (HDI). The HDI process developed by General Electric and now owned by Lockheed Martin is the one most similar to IC processes. This process is what is called a “chips first,” as the assembly is done before the substrate is completed and the IC bonding is direct to the substrate. It does not use flip-chip or wire bonding, but can utilize unmodified chips directly. A number of build-up layers and very fine geometry are possible. There are obvious advantages in making multichip modules and in using standard chips. The materials and bonding technologies have proven to be very reliable and suitable for military applications. The disadvantage is the maximum panel that can be sputtered. Future use of PVD/CVD metallization may make this process more cost-effective.

23.3.2.1.1 Structure. The circuit structure of HDI consists essentially of common conventional flex circuits or more advanced microvia flex structures. These are purchased for this process. The polyimide film is usually 25- or 50-micron adhesiveness. The laser ablates away the polyimide to produce blind and through vias. The through vias are stopped by the aluminum bonding pads of the integrated circuits. By doing this, integrated circuits designed for wire bonding can be directly attached. Figure 23.9 shows a typical HDI structure.

23.3.2.1.2 Manufacturing Process. The process starts with a finished single-sided, double-sided, or multilayer polyimide flex circuit. An adhesive is applied to the flex circuit. All the ICs and components are bonded to the polyimide film layer pair flex circuitry and cured. The assembly is turned over and a laser drills down through the flex circuitry to make blind and through vias including opening up the bonding pads on the IC chip. Gold, under-bump metallurgy, or C4 bumps are not required. The panel goes through tungsten sputtering to metalize the vias and seed the top layer. Circuit pattern can be applied, plated, and then etched to complete the circuit. The process is diagrammed in Fig. 23.10.^{10,11}

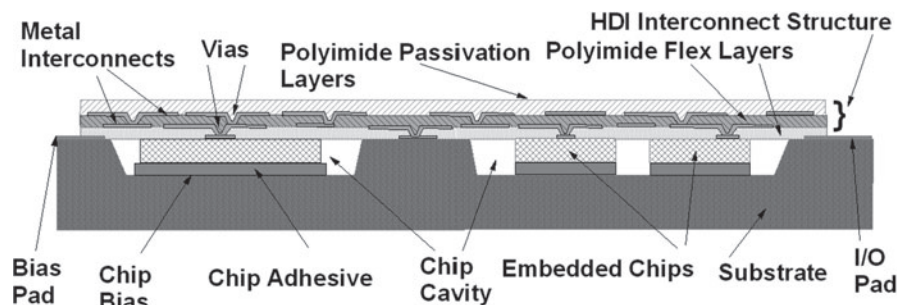


FIGURE 23.9 Structure for the HDI multilayer substrate with lasered blind vias and direct connection to the ICs.

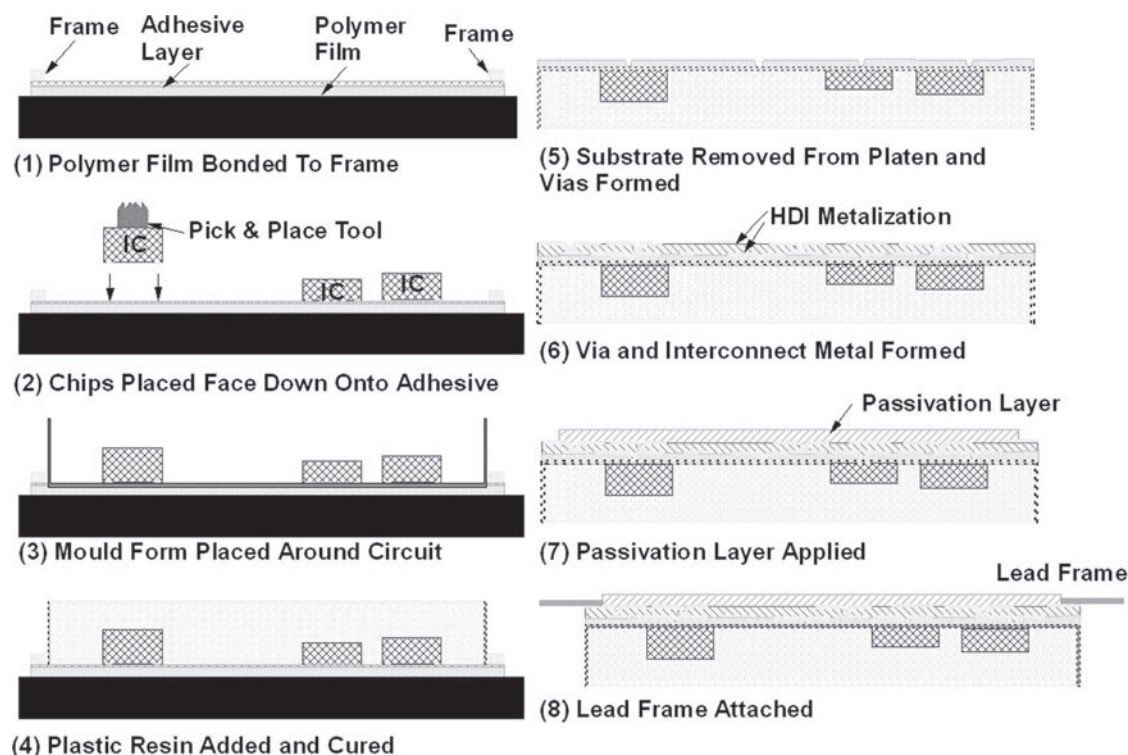


FIGURE 23.10 Manufacturing sequence for the HDI multilayer substrate with lasered blind vias.

23.3.2.2 Meiko-BU. Meiko Circuits of Japan takes a photoresist and coats it onto a stainless steel panel. This starts the process to produce high density interconnect structures (HDIS) in a remarkable way. The advantages of this process is that surface geometries are not determined by etching or full additive metallization, the vias are under the surface lands, and the circuits are all flush with the dielectric, permitting the elimination of solder masks. On the negative side, this is a more expensive process that involves carriers.

CHAPTER 26

IMAGING

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26.1 INTRODUCTION

Imaging is the process that patterns the metal conductor to form the circuit. This process involves a multistep integration of imaging materials, imaging equipment, and processing conditions with the metallization process to reproduce the master pattern on a substrate. Large features (200 μm and greater) can be very economically formed by screen printing. Feature sizes smaller than 200 μm , however, are formed using a photolithographic process, which is the main discussion of this chapter. As circuit densities have increased over the years, the imaging process has continually evolved to enable commercial production of finer features. This need for high-density interconnect (HDI) is driving the industry to feature sizes of 10 μm or lower. Imaging equipment and materials have been developed to meet this challenge.

To achieve a reproducible high-yield/low-cost imaging process for a given feature size, various factors must be carefully balanced. This chapter outlines the chemistry and equipment options for the photolithographic imaging process, highlighting trade-offs that must be considered so that process engineers, designers, and procurers of printed wiring boards (PWBs) and HDI structures have an overview of the process considerations that can enable a manufacturable product.

Printing is an alternate process for imaging. Screen printing is used to print resist on foil and silver inks on polyester. Ink jet printing has been used to pattern resist, legend, and silver conductors. Recently an ink jet system has been introduced that prints a UV-curable catalyst layer to electroless plate copper at thicknesses of 0.05 to 5 microns.¹ Significant development work is underway on organic transistors patterned by ink jet and other printing methods. These techniques are beyond the scope of this chapter.

The photolithographic process sequence for imaging is given in Fig. 26.1. Basically the process

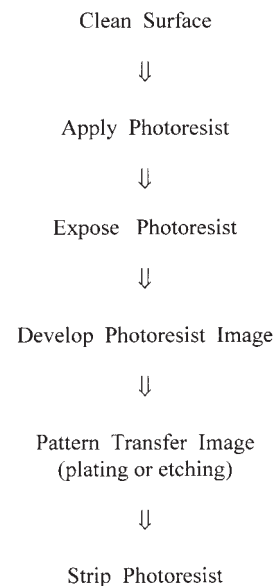


FIGURE 26.1 The photolithographic process sequence.

26.1

involves applying a light-sensitive polymeric material (photoresist) onto the substrate of interest, exposing this photoresist to light with the desired pattern, and developing the exposed pattern. This developed pattern is used for either subtractive (etching) or additive (plating) metal pattern transfer. Details of these metallization processes are given in subsequent chapters. After metallization, the photoresist is stripped from the surface and the panel is ready for further processing.

26.2 PHOTSENSITIVE MATERIALS

The photosensitive polymeric systems used as photoresists in the interconnect industry are either liquids or dry films formed from a liquid solution. Dry-film photoresists are the industry standard, but liquid photoresists have become widely used, particularly for fine-feature circuits. Both types of photoresist can be used for a variety of processing requirements.

26.2.1 Positive- and Negative-Acting Systems

Photoresists may function in a photographic sense in either a positive or negative tone. The difference, illustrated in Fig. 26.2, is a result of the specific chemical reactions that occur on exposure to light. For the common negative-acting systems, exposure initiates cross-linking

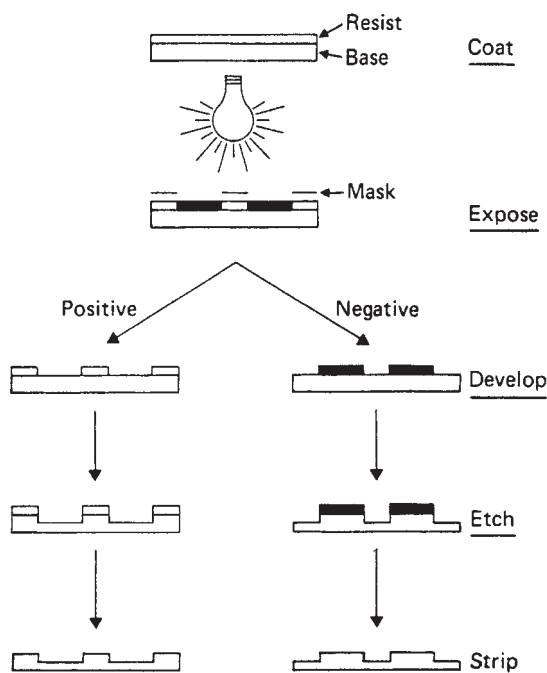


FIGURE 26.2 The photolithographic process sequence for positive and negative tone photoresists. (Reprinted by permission of C.G. Willson, Introduction to Microlithography, Theory, Materials and Processing, ACS Symposium Series 219, Washington, D.C., 1983, p. 89.)

between one or more of the components in the polymeric matrix, reducing the photoresist's solubility in the developing solution. The exposed regions remain after development of the image. For positive-acting photoresists, the chemistry is often the novalac resin-based materials utilized by the semiconductor industry. Upon exposure, an acid-catalyzed reaction occurs that increases the solubility of the photoresist in the developer solution. In this case, it is these exposed regions that are removed in the developer solution.

Photographic tone can have an effect on product yield caused by contamination between the phototool with the master image and the photoresist. For a negative-acting photoresist, contamination blocks the light and prevents cross-linking, leading to a mousebite (partial reduction in line width) or an open circuit in the conductor after etching. For a positive-acting photoresist, contamination blocks the light and prevents the acid-catalyzed solubilization, leaving excess metal and a possible short after etching. Since circuit patterns often have a greater area of spaces than lines, there is a lower probability of a contaminant causing an actual defect with the positive-acting photoresist. However, negative-acting photoresists are the most widely used since many other factors impact yield and contamination must be minimized in any photolithographic process.

26.2.2 Decision Factors

The large variety of commercially available photoresists makes it a challenge to determine which one is likely to perform best for a given application. Key technical and economic factors that must be considered are summarized in Fig. 26.3. The primary consideration is the end use of the pattern.

- The photoresist must be chemically compatible with the subsequent pattern transfer steps (i.e., can withstand the chemical environment such as the solution pH) for it to function as an accurate mask for pattern transfer.

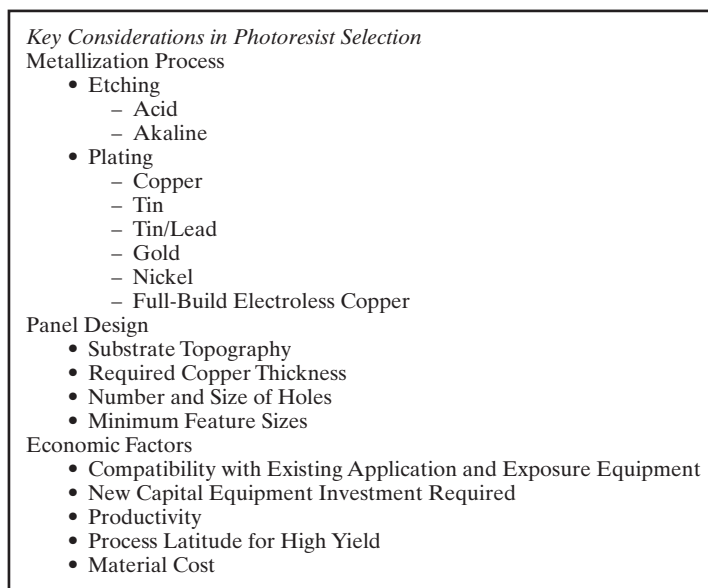


FIGURE 26.3 Criteria for selection of photoresist materials.

- The nature of the substrate itself in terms of topography and surface features must also be considered. Is the photoresist required to cover or tent plated through holes or tooling features, and must it conform to existing circuitry? This consideration will dictate if dry-film or liquid photoresists are appropriate and, in some instances, the required tone.
- The required product feature dimensions are equally important. They are usually specified in terms of line width and spacing with a given allowable variation. Since these product specifications are for the final conductor features, the impact of photoresist processing on the critical dimensions must be established. Each photoresist has an inherent contrast (i.e., the rate of change of solubility on exposure to light). This contrast, combined with the resist thickness, phototool, light source used for exposure, and developing conditions, determines the finest feature that can be imaged. For photoresists used in the PWB industry, the minimum line width achievable in production is usually 10 to 25 μm greater than the photoresist thickness. Novel process sequences have demonstrated it is possible to overcome this traditional barrier.²
- The adhesion of the photoresist is another key attribute. The chosen photoresist must have good adhesion to the underlying substrate during pattern transfer but must also be able to release cleanly from the substrate during stripping.

26.3 DRY-FILM RESISTS

Dry-film photoresists are generally used for pattern formation prior to both plating and etching.

These films have a three-layer structure, with the photosensitive material sandwiched between a polyester coversheet and a polyethylene separator sheet (see Fig. 26.4). The photoresist thickness is typically 25 to 50 μm , but thinner and thicker films are used for special applications. The photoresist is applied to the printed wiring board (PWB) substrate using lamination: The polyethylene separator is removed, and the photoresist flows under the heat and pressure from the laminating rolls to adhere to the substrate. The polyester coversheet

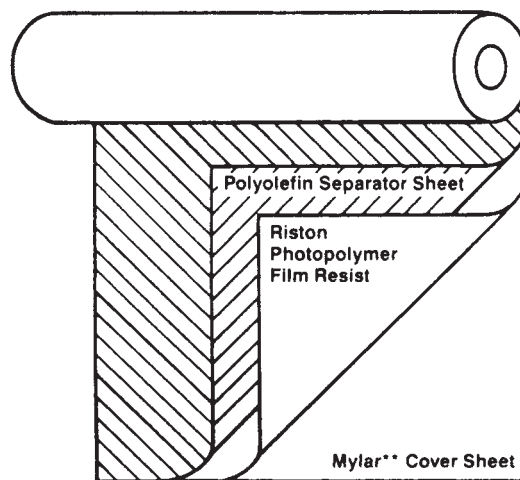


FIGURE 26.4 Dry-film photoresist components. (Reprinted with permission of DuPont Electronics, DuPont Technical Literature.)

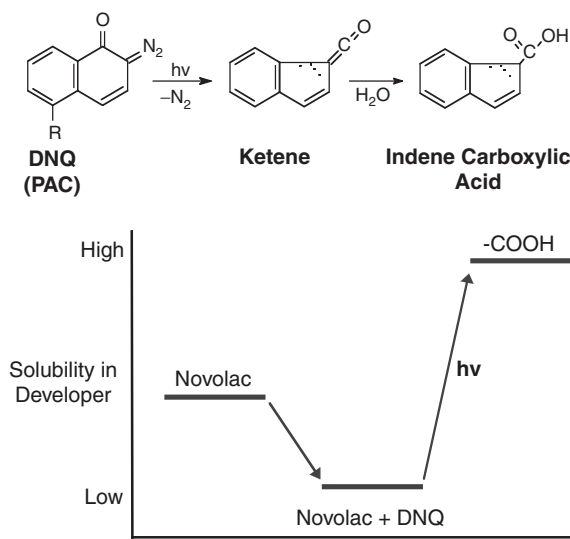


FIGURE 26.5 Chemistry mechanism of positive-acting liquid photoresists.

plating). The chemistry involves the conversion of a base-insoluble diazonaphthalquinone to the base-soluble indene acid. Thus, this photo-driven conversion alters the solubility of the base material in alkaline solutions, allowing for image formation (see Fig. 26.5).

26.5 ELECTROPHORETIC DEPOSITABLE PHOTORESISTS

Electrophoretic depositable (ED) photoresists^{12,13} were introduced in the late 1980s with expectations of broad adoption by the interconnect industry. The early materials were modifications of those used for coating automobiles and appliances. These fast-coating processes provide a defect-free film of high durability on conductive substrates and are well suited to large-volume production. Anodically and cathodically deposited materials that are both positive and negative acting have been introduced but have achieved limited market penetration in the interconnect industry. Advances in dry-film photoresists and liquid photoresists reduced the interest in implementing a new photoresist process. (A detailed discussion of electrophoretic depositable photoresists is included in Sec. 17.1.6 of the fourth edition of this handbook.)

26.6 RESIST PROCESSING

Imaging is a sequential process, and the various steps are very interdependent. Equipment and processing conditions play a large role in the image quality, yield, and productivity that can be achieved. The choice among the numerous options for each step depends on the type of substrate to be imaged, the feature sizes to be produced, the existing equipment, the type of photoresist, and the productivity and economics of the production line. Alternatives for each process step are described and compared.

26.6.1 Cleanliness Considerations

Cleanliness is an issue throughout the entire photolithography process, including yellow room contamination level (cleanliness class), solution filtration, equipment cleanliness class, and product handling. Its importance increases as feature size decreases. The level of cleanliness needed to give acceptable yield for the finest features must be established and maintained.

Sticky rollers, either as free-standing equipment or as handheld items, are one type of equipment used to remove contamination from flat surfaces, either panels or equipment.

26.6.2 Surface Preparation

Good adhesion between the photoresist and the substrate is essential for the remainder of the process to be successful. All laminates arrive at the imaging area, dirty, and the exact process sequence for surface preparation is chosen based on the nature of the contamination. Epoxy dust generated during trimming and processing of the laminate is removed by mechanical cleaning. The copper surface is either foil or foil with electroless or electroplated copper. Foil typically has an antitarnishing agent of chromium and zinc that must be removed for reproducible imaging results. During cleaning, the texture or surface roughness of the copper is altered, promoting mechanical adhesion between the copper and the photoresist. The extent of this texturing is measured by the usual parameters for surface roughness, the height and spacing of the topography measured by profilometry (see Fig. 26.6).

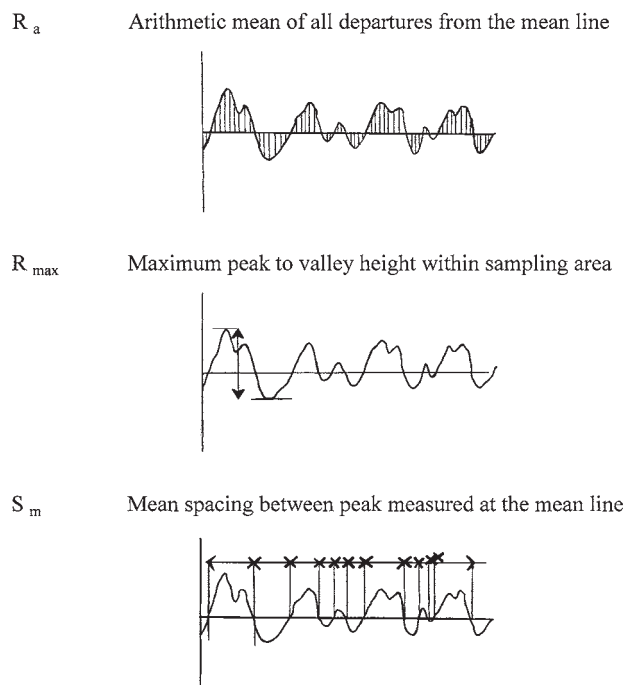


FIGURE 26.6 Surface roughness parameters.

TABLE 26.2 Copper Surface Chemical Composition as Measured by X-Ray Photoelectron Spectroscopy (XPS)

Sample	% Cu	% O	% C	% N	% Zn	% Cr
Initial		46	24		16	12
Preclean 1	12	19	68			
Preclean 2	6	10	70	14		

Chemical cleanliness can be determined in a variety of ways. Wetting is often tested using a *water break test* or more analytically in terms of contact angle, with a low value being desirable.

In addition, analytical techniques (Auger and x-ray photoelectron spectroscopies) can be used to evaluate the chemical composition of the surface (see Table 26.2).¹⁴

26.6.2.1 Mechanical Cleaning. Most mechanical cleaning equipment physically abrades the copper surface using a pumice or aluminum oxide slurry either directly (scrubbing or vapor blasting) or impregnated into brushes. Scrubbing provides an even final surface texture, whereas brushing creates grooves (see Fig. 26.7). The copper thickness must be sufficient to provide the desired final conductor height after cleaning. Mechanical cleaning is more difficult for very thin flexible panels.

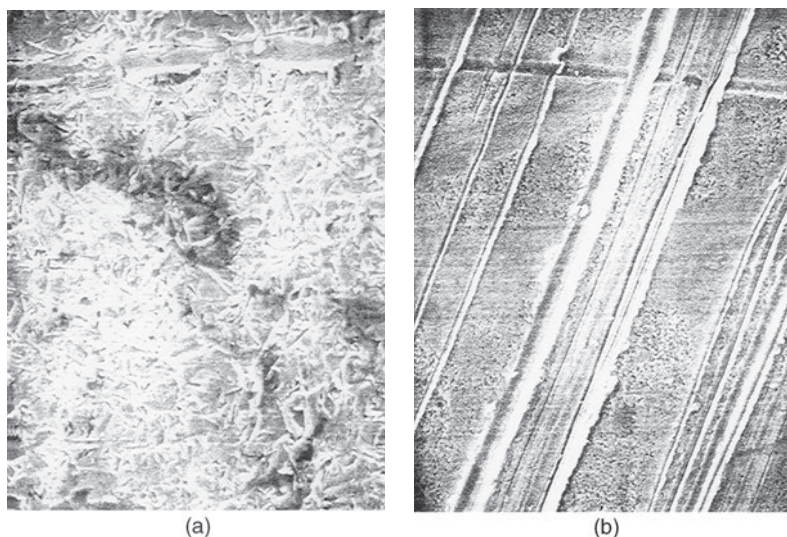


FIGURE 26.7 Comparison of the pumice cleaned (a) and mechanically abraded copper surfaces (b), 1200X. (Reprinted with permission of D. P. Seraphim, R. C. Lasky, and C-Y Li, *Principles of Electronic Packaging*, McGraw-Hill, 1989, p. 383.)

The texture of the mechanically cleaned surface affects the adhesion between the photoresist and the copper. The resist should conform to the topography, and thus, the extent and type of texture must be tailored to the type of photoresist. If the gouges are too deep, a dry film applied with traditional lamination will have difficulty conforming to the surface and create defects: near or full opens after etching, and underplating or shorts after pattern plating. Thus, the cleaning process, photoresist type, and application method must be matched to image at high yields.

Conveyorized equipment is used that passes the panels through the brushes or slurry and then to rinse chambers before exiting through a dryer section. If rinsing is insufficient, residual

TABLE 26.3 Cleaning Solutions Used to Remove Various Contaminants

Cleaning technique	Process chemistry	Contaminant removed
Abrasion	Pumice, Al oxide	All
Plasma	CF ₄ /O ₂ , O ₂ /H ₂ O	Organic
Chemical solutions (aqueous etchants)	H ₂ SO ₄ , HCl, etc.	Inorganic
Chemical solutions (nonaqueous)	Alcohols, etc.	Organic
Thermal	N ₂	H ₂ O

Source: Adapted from *Introduction to Microlithography*, 1st ed., L. F. Thompson and M. J. Bowden, American Chemical Society Symposium Series 219, Washington, D.C., 1983, p. 184.

pumice can remain on the copper surface. Maintaining proper functioning of the mechanical parts that contact the product is essential since brushes and slurry deteriorate with use. Equipment designs that isolate the abrasive from the majority of the tool are more durable.

26.6.2.2 Chemical Cleaning. Chemical cleaning includes a variety of solutions since the solubility of contaminants can be quite different (see Table 26.3). Grease and fingerprints require a soap solution or solvent to dissolve them. Antitarnish treatment removal and copper roughening is done with mild etchants for the copper, such as ammonium persulfate, sodium persulfate, or peroxide/sulfuric acid. Depending on the oxidation level and the amount of antitarnish treatment, there is often an induction time for copper removal. Solutions used can be common chemicals or proprietary mixtures in which surfactants and other additives have been included. Alternatively, the oxide and antitarnish treatment can be removed initially, followed by a surface roughening. In this case, the oxide removal is accomplished with mild acidic cleaning solutions such as sulfuric acid.

The selection of the cleaning solution also depends on the copper thickness. Thin “seed” layers used for electrolytic pattern plating can tolerate very little etching, and extremely dilute solutions or dry methods are used. Thus, chemical adhesion can be more important than mechanical.¹⁵ Selection of the proper process chemicals and sequence depends on the overall conductor formation process and the photoresist to be used.

Chemical cleaning sequences are often contained in conveyORIZED spray equipment with rinsing between each step. Batch processing in a tank system is also used, with a hoist for basket movement between solutions. Uniformity of the etching of panels within a basket must be measured, but is generally quite good and reproducible as long as the immersion time is short and the bath’s chemical composition is consistent.

26.6.2.3 Electrolytic Cleaning. A unique inline conveyORIZED tool built by Atotech uses electrolytic cleaning.^{16,17} The antitarnish is removed electrolytically along with oils and fingerprints in a uniform process with very little copper removal. The surface texture is then altered by microetching and passivated prior to dry-film photoresist lamination or other coatings.

26.6.3 Photoresist Application

The technique used to apply the photoresist to the substrate depends on the type of photoresist selected. The various techniques used with dry-film and liquid photoresists are discussed.

For any of these techniques, the cleanliness of the operation—both the equipment and the room—and the handling of the product are critically important, especially for high density. It is also advisable to minimize handling at this stage by using automated inline equipment for the preclean step and automatic loading and unloading.

26.6.3.1 Dry-Film Hot Roll Lamination. In this process, both temperature and pressure are used to laminate the dry-film photoresist to the panels. After stripping off the polyethylene

separator sheet, the photoresist is contacted to the substrate in a nip between two heated rolls. Heat reduces the viscosity of the photoresist and pressure causes it to flow, conforming to the irregularities of the copper surface.

The weave of the laminate affects the topography of the substrate and how much flow is required to achieve good conformation, an essential condition for high yield. Dry-film photoresists are tailored to have rheology that maximizes flow during lamination while preventing flow in the roll prior to lamination, which could cause edge fusion. Panels are often heated with heated rolls and infrared heaters prior to lamination to improve photoresist conformation. The key process parameters affecting conformation are laminator speed, laminating roll temperature, and rigidity of the rolls with respect to the core material and rubber durometer. For aqueous-developable materials, wet lamination has proven to be effective in improving conformation and yield for innerlayers. By using a water-alcohol mixture, wet lamination can also be applied to tent and etch inner via holes to minimize the land diameter.¹⁸

Both automatic and manual tools are available for film lamination (see Fig. 26.8). With manual tools, the panel is placed in the nip and pulled through by the rotation of the rollers.

The continuous film of photoresist must be trimmed for each panel on at least two sides. This technique is labor-intensive and extremely dirty due to the chips of resist generated by trimming.

However, it is useful for very thin materials and nonstandard-size panels in small lot sizes. With automatic equipment, the basics are the same but the panel enters from an automatic loader or a conveyORIZED preclean tool directly into and through the dry-film laminator.

This is a relatively clean operation with little handling of the panels since the photoresist is automatically trimmed to the appropriate size and placed within the board edge.

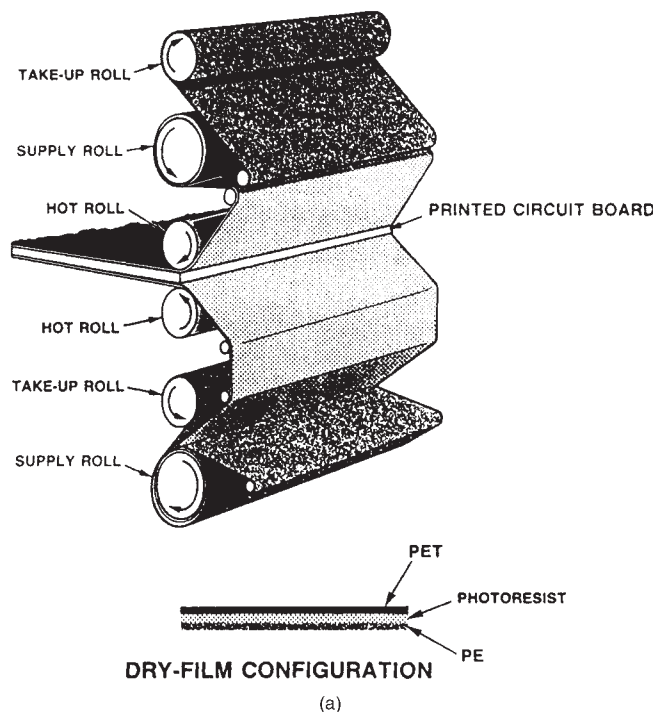


FIGURE 26.8 Configuration of a hot roll laminator: (a) three-dimensional schematic; (b) two-dimensional schematic. (Reprinted with permission of E. S. W. Kong, *Polymers for High Technology*, ACS Symposium Series 346, Washington, D.C., 1987, p. 280.)

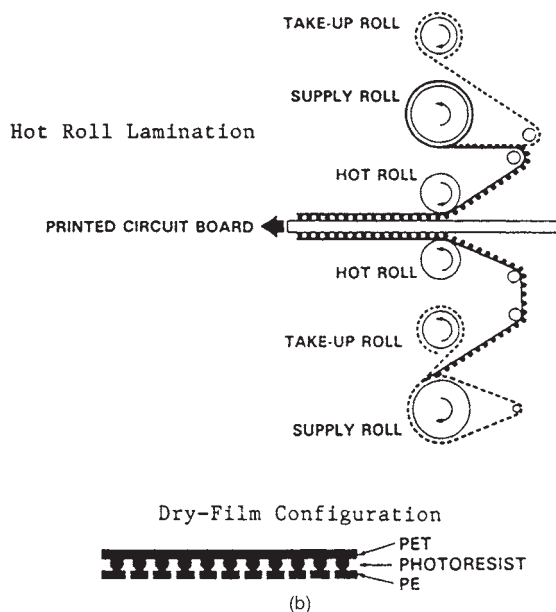


FIGURE 26.8 (Continued)

Equipment is available to convey even very thin panels. Panels are often heated, wetted (wet lamination), or cleaned before the actual lamination.

26.6.3.2 Dry-Film Vacuum Lamination. This method is similar to hot roll lamination but the temperature and pressure used to adhere the photoresist to the substrate is applied by a heated vacuum platen instead of laminating rolls. Vacuum lamination is useful for products with tall or closely spaced features that make it difficult for the photoresist to conform. The vacuum removes the air that would be trapped and pulls the photoresist into tight spaces, providing conformal coverage. This equipment is also used for material that will deform nonuniformly under the pressure of laminating rolls, such as thin unreinforced polyimides. With vacuum lamination, the pressure is evenly distributed over the panel, improving dimensional stability control.

26.6.3.3 Liquid Coating. A great variety of methods are used to apply liquid photoresist to panels. Roller, spray, electrostatic, and electrophoretic coating provide double-sided application and are well suited to high-volume manufacturing. Curtain coating is single-sided, requiring either two passes of the panel through the equipment with slight drying between coatings or an inline equipment layout with two coating and drying units. This causes a difference in the solvent content of the two sides. Screen-coating equipment is available for either single-side or double-side coating. In all instances, the cleanliness of the surroundings, equipment, and solutions is essential for high-yield processing. Most equipment is designed to minimize material consumption by collecting and filtering excess liquid so it can be recycled to the feed tank.

26.6.3.4 Roller Coating. This method places liquid photoresist on the board by transferring the liquid from one set of rollers to another (see Fig. 26.9). The exact number, physical configuration, and surface of the rollers vary, as well as how the material is metered. Often, gravure roller coating is used. Grooves or crosshatches in the rollers that contact the panel determine the amount of liquid deposited on the substrate and are set with a measured overlap or interference so that the board is squeezed between the rollers.¹⁹ Photoresist viscosity also influences the coating thickness applied. Improvements in panel handling and in confining the solution to

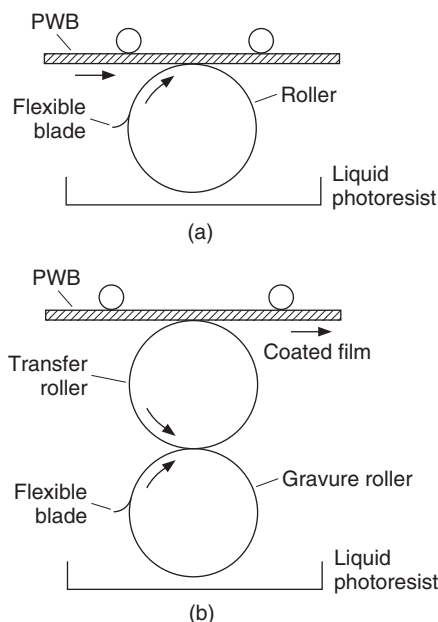


FIGURE 26.9 Configuration of a roll coater: (a) direct coating; (b) indirect coating.

the center of the panel allow for simultaneous two-sided “postage stamp” coverage similar to that obtained with dry-film photoresists, leaving the tooling and location holes clear of material. In commercial systems, the coater is conveyorized, with panels entering a clean oven immediately after coating. The throughput of these systems can be as high as 240 panels per hour.

26.6.3.5 Spray Coating. Although very thin and uniform coatings are possible with this method, its use in resist imaging has been limited due to concerns about waste caused by overspray.

The spray head traverses a larger area than the substrate to be coated, and the amount of liquid photoresist that becomes overspray can be significant. Exact characteristics of the coating in terms of thickness and topographical coverage depend on spray-head configuration, nozzle backpressure, droplet size, and conveyor speed.²⁰

26.6.3.6 Electrostatic Coating. This method is similar to spray coating except that the rotation spray head is charged and the panel is grounded. Since the atomized photoresist is attracted to the substrate, there is less material waste than with spray coating.²¹ Electrostatic coating is used for solder mask since it provides good coverage of conductor sidewalls. However, its use with photoresist is limited to innerlayers. It is unsuitable for outerlayers because it deposits a thicker coating on the rim of a plated through hole while leaving its interior uncoated.

26.6.3.7 Electrophoretic Coating. This method requires materials specially formulated for anodic or cathodic deposition. The equipment schematic in Fig. 26.10 illustrates the process sequence: preclean, coat, permeate rinse, rinse, and dry.²² Panels are placed in the photoresist solution wet or are often sprayed with solution to ensure wetting, especially if the parts have blind or through vias. Voltage is applied, and within 20 sec. to 3 min. an insulating film forms.

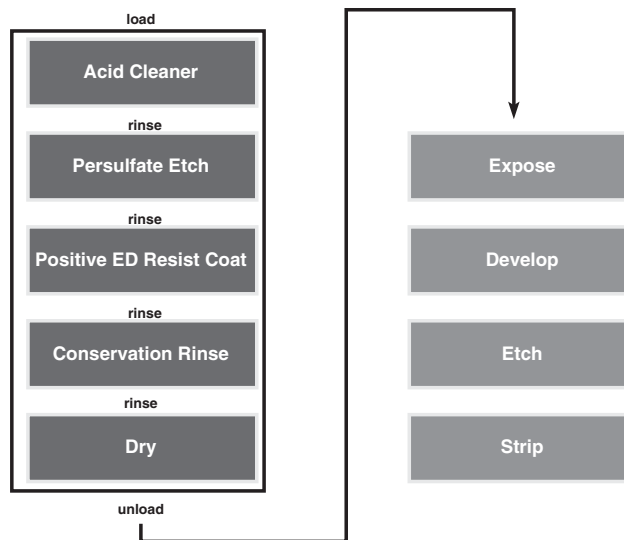


FIGURE 26.10 Configuration of an electrophoretic photoresist coater. (Reprinted with permission of J. Dubrava et al., "Development of a Novel Positive-Working Electrodeposited Photo Resist Process for the Production of High Density PWB Outerlayers," presentation at the IPC Conference, San Diego, California, Spring 1995.)

Rinsing removes loosely bound material that is returned to the plating cell after ultrafiltration to separate the photoresist and the counterion. This aids in maintaining the ionic balance.

After a final water rinse, the panel is dried to remove water and consolidate the film. The film is now tack-free and can be imaged.

The chemical composition of the photoresist determines whether the equipment components are made from polyvinyl chloride (PVC), polypropylene, or polyethylene. Electrodes are made of stainless steel and encased in an ion-selective membrane that is flushed to prevent the build-up of counterion migrating there during deposition. The permeate and ultrafiltration unit is important for long-term stability of the coating solution. The coating unit is often enclosed in a clean environment to reduce the amount of particles found in solution or resting on the panel as the process proceeds.

26.6.3.8 Curtain Coating. This method is commonly used to coat liquid solder mask materials. The panel is conveyed at high speed through a vertically falling curtain of the liquid photoresist. The coating width can be adjusted so that the edges are not covered. Temperature and viscosity are controlled for reproducible coatings, and coating thickness is determined by the conveyor speed and the solution flow rate.²³ Material in the curtain is returned to the sump and reused, giving very efficient material utilization. This method is one-sided, and the first-side photoresist coating must be partially dried before coating the reverse side. Due to the extra handling required to coat one side at a time and the inability to convey very thin panels through the curtain at high velocity, this method has seen only limited use with photoresist.

26.6.3.9 Screen Coating. Another common method for coating solder mask with either a pattern or flood coverage is screen coating. The screen mesh size and the liquid solution viscosity set the wet coating thickness. The screen is placed above the panel to be coated, and the material is forced through the openings in the screen onto the panel surface, where it forms a film.

Equipment is available for either single-side or double-side coating. With single-sided screen printers, the coating must be partially dried before the reverse side is coated. This causes a difference in the solvent content between the two sides that would result in nonuniformity for very precise lithography. In addition, the sequential nature of the coating allows debris and contaminants to be embedded into the first coating. Double-sided screen printers eliminate a drying step and minimize panel handling. The advantages of screen coating are that the equipment is relatively inexpensive to purchase and operate, “postage stamp” (small embedded areas) coating is possible, and waste is minimized.

26.6.4 Expose

Expose is the actual imaging step, reproducing the master pattern in the photoresist. The relief image is created after subsequent development. The expose process elements are phototool generation, registration of the phototool to the panel, and exposure through the phototool by the light source. Light-source alternatives include contact printing, either collimated or uncollimated; proximity printing; projection printing; and laser direct imaging. The noncontact methods separate the phototool from the substrate, reducing yield losses caused by contamination between the phototool and photoresist. With laser direct imaging, there is no phototool and the design data file of the master pattern drives the laser beam to expose the photoresist.

Phototools are generated on either film or glass substrates, depending on the feature sizes that are being patterned and the durability required. The panel is either mechanically aligned, with pins holding the phototool with respect to the product, or optically aligned, with alignment features dictating the movement of the phototool and product. The alignment requirements are interrelated to those achieved at composite lamination and drilling. The registration scheme is contained within the exposure equipment.

26.6.4.1 Conventional Imaging

26.6.4.1.1 Artwork Generation. Polyester and glass are the substrates used for phototools. They differ in optical properties, dimensional stability, and durability. Silver halide on polyester is used to create first-generation phototools on a laser plotter. This image is often contact printed onto diazo on polyester to make the copies used in production. Optical absorbance of the different phototool materials versus wavelength is plotted in Fig. 26.11.

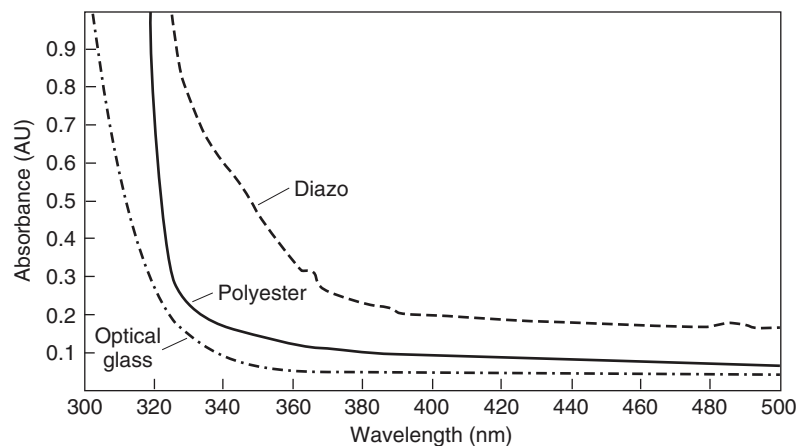


FIGURE 26.11 Optical absorbance of common phototool materials in the spectral region of PWB photoresist exposure.

Diazo phototools are the least expensive, and glass is the most expensive. Although the less-expensive materials have poorer transmission, this property is generally not limiting, except for applications requiring high intensity. Table 26.4 illustrates the impact on exposure time. Edge definition is a major difference among the options, as shown in Fig. 26.12. The photos illustrate that chromium on glass gives the sharpest edge definition. Edge definition is also affected by the pixel size of the phototool plotter and the spot's addressability (see the section on LDI). For applications that use a low-contrast photoresist and poor light collimation, these differences are not measurable on the printed photoresist image or in the patterned conductor. However, for high-density imaging, edge definition is important, as is the dimensional stability of the phototool.

TABLE 26.4 Comparison of the Optical Transmission of Various Phototool Materials

Property	Diazo	Polyester	Glass
Absorbance at 365 nm	0.271	0.107	0.047
Transmission at 365 nm	54%	54%	90%
% increase in exposure time vs. glass	40	13	0

Film dimensions change more rapidly with temperature than glass and are also affected by humidity. Careful control of both temperature and humidity is required throughout the life of a phototool (see Table 26.5).

TABLE 26.5 Dimensional Stability of Phototool Substrate Materials with Respect to Temperature and Relative Humidity

Substrate	Expansion coefficient, ppm/°C	Expansion coefficient, %RH/°C
Soda lime glass	9.2	0
Low-expansion glass	3.7	0
Pyrex	3.2	0
Quartz	0.5	0
Polyester	18	9

Source: Kodak Technical Literature (ACCUMAX 2000) for polyester film; *Tables of Physical and Chemical Constants*, Longman, London, 1973, p. 254; H. J. Fischbeck and K. H. Fischbeck, *Formulas, Facts and Constants*, Springer-Verlag, Berlin, 1987, for glass data.

The durability of the phototool is also important, especially for use in a manual contact printer. Damage depends on phototool handling, the exposure tool, the cleanliness level of the operation, and the surface of the product being contacted. Commonly, glass artwork is usable for 100 to 400 contacts with repair, while film artwork is usable for 20 to 50. For large numbers of the same part, number cost per contact may actually be lower with glass artwork, while for prototype parts, film artwork is ideal. However, the majority of production panels are exposed with film artwork. High-density applications such as chip scale packaging and multichip modules using laminate (MCM-L) may require glass artwork. The requirements of the product determine the type of phototool that should be used.

26.6.4.1.2 Registration. The image is placed on the panel with respect to a point of reference so that the image is well aligned to previous and future features. In multilayer construction, the innerlayer images are aligned front to back for successful lamination and drilling of the plated through holes (PTHs). The outerlayer image is then aligned to the drilled holes. The same considerations are relevant for single-layer boards. Thus, accurate alignment

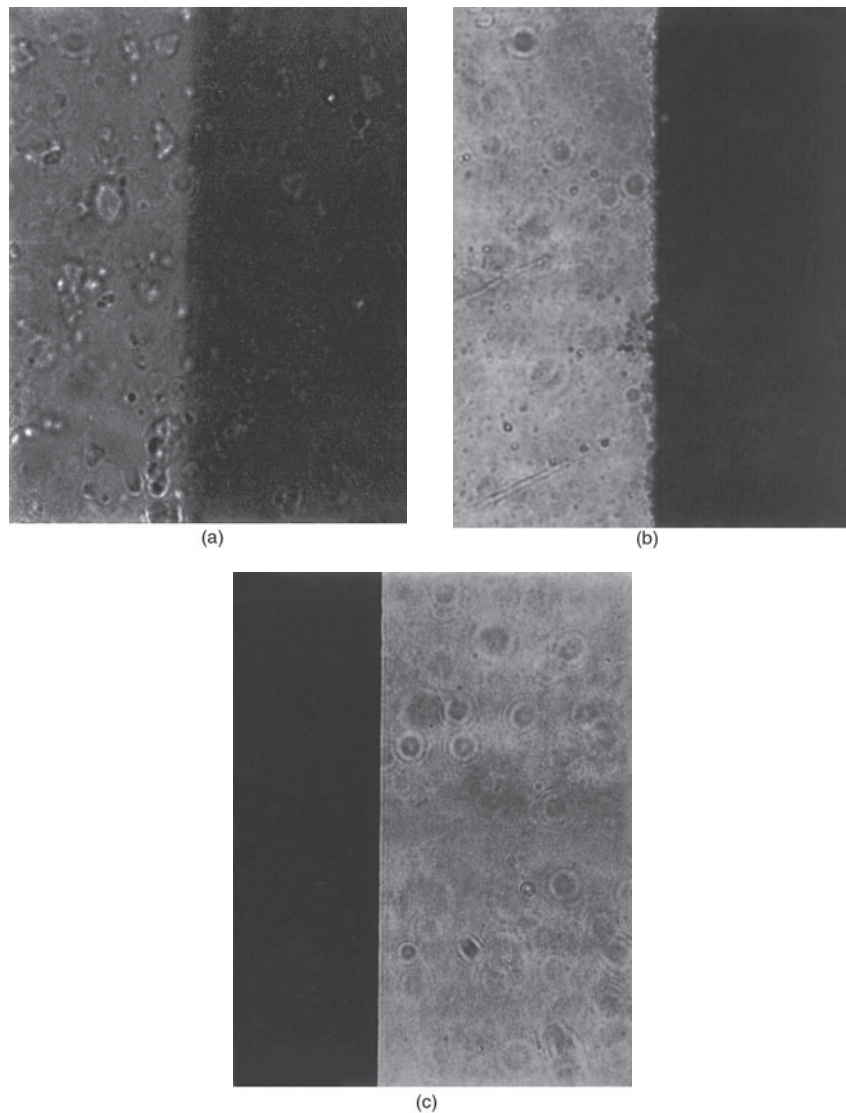


FIGURE 26.12 Optical micrograph of the image edge of common phototool materials, 1600 $\times$: (a) diazo on polyester; (b) silver on polyester; (c) Cr on glass.

is clearly part of the imaging process and also depends on knowledge and control of the dimensional stability of the product. The image must be scaled to match the dimension of the board at the exposure step; for multilayer structures with several photolithographic steps, a series of dimensional measurements are required prior to product manufacture.

Mechanical registration entails the use of fixed pins or other mechanical devices to hold the phototool and the panel in place during exposure. The actual configuration of the pins and their shape varies. Both two- and three-point systems are used. The three-point systems well define the center location since they are located at the extremes of the area to be patterned.

The shapes of the pins are either round or elongated with one flat side. In the latter case, the flat side defines the edge, while round pins center within the hole in the panel and phototool.

Film artwork alignment holes are punched with respect to the product pattern by plotting alignment targets as part of the product pattern and optically aligning and punching a slot or hole. The edges of the punched feature wear, and registration will deteriorate with use. For glass artwork, the glass is drilled at the alignment locations and a bushing is placed at the center of the hole. The pin is then inserted through the bushings in top and bottom artwork and through the panel. With use, the bushings do move and must be reset for maximum reproducibility.

Optical alignment systems operate either manually or automatically. In both instances, the phototool is plotted with alignment targets—usually an opaque dot that is smaller than a drilled or punched hole in the panel. With backlighting, the dot (phototool) is aligned to the center of the hole (product). Often, three locations at the edges of the panel are used. In manual systems, micrometers are used to move either the part or artwork. In automatic equipment, a vision system calculates the necessary movement, and motors then move either the phototool or the product into alignment. Since there is no wear on the phototool, when it is optically registered the accuracy is maintained with usage. The absolute accuracy achieved with optical methods is superior to mechanical registration, with the best accuracy and reproducibility obtained with automatic optical systems. The extra expense for automated equipment is warranted if it is needed to meet stringent product requirements.

26.6.4.1.3 Exposure Control and Measurement. The role of exposure is to change chemically the photoresist and its solubility in the developer solution. The appropriate energy dose is determined experimentally by measuring the combination of dose and development that is needed to produce features with straight sidewalls. The photoresist is coated on an optically clear substrate and exposed from the backside. Contrast curves, plots of the log of the exposure dose versus the thickness of the film remaining, are used to identify the functional cure point—for example, the dose that loses thickness less than 10 percent (see Fig. 26.13).

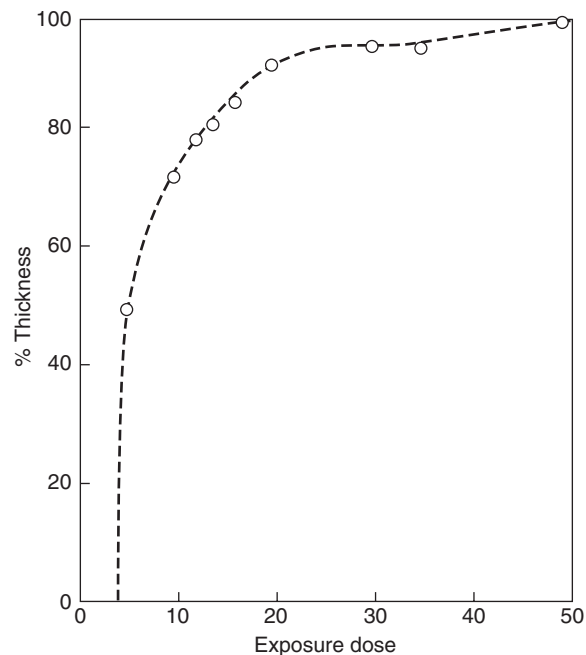


FIGURE 26.13 Contrast curve for a negative-acting dry-film photoresist, percent film thickness remaining versus exposure dose (mJ/cm^2).

Exposure in the region of stability ensures that the base of the material has reacted. Step wedges, film strips with a series of neutral density filters, are also used to determine appropriate exposure doses. The dose is varied to obtain photoresist residue on the area with the manufacturer's recommended step value. This technique depends on appropriate and consistent developer conditions.

Step wedges are often used to control the expose or expose-and-develop processes.

The energy incident on the photoresist is the product of the lamp intensity and the time of exposure:

$$\text{energy} = \text{intensity} \times \text{time} \quad (26.1)$$

Thus, the exposure dose can either be measured directly by using an integrating radiometer or indirectly by measuring exposure time and light intensity with a radiometer. The radiometer response must be matched to the spectral output of the light used so that representative measurements are made (see Fig. 26.14). Most exposure equipment provides the option of using either direct energy or time measurement. With a stable light source, both approaches are equally reproducible.

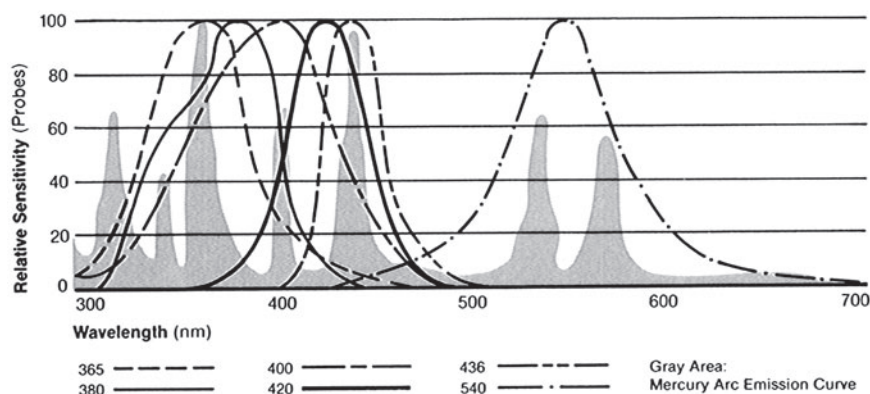


FIGURE 26.14 Output of Hg/Xe light source and radiometers. (Reprinted with permission of Optical Associates, Inc., Milpitas, California, Technical Literature.)

26.6.4.1.4 Contact Exposure Tools. This equipment places the phototool and the panel in direct contact and draws a vacuum between the pieces for hard contact. A range of light wavelengths is used, often from a mercury or mercury/xenon light source, which is stable and has a high intensity output at ultraviolet and visible (UV/Vs) wavelengths (see Fig. 26.14). The light is distributed over the area to be exposed by placing the board at a distance from the source, either noncollimated or collimated by the use of optical elements, as shown in Fig. 26.15. Collimation refers to the angle of incidence of the light onto the photoresist, and it is critically important for fine-line images. Defining fine spaces is the challenge for both additive and subtractive conductor formation, and exposure under the opaque areas cannot be tolerated. The lamp intensity for noncollimated sources is greater, and therefore less time is required to expose the panel. Process throughput is noticeably enhanced for photoresists requiring a large dose.

In addition to collimation, good contact between the phototool and the panel is the most important factor to control in fine-line formation. Any gap will allow exposure under the

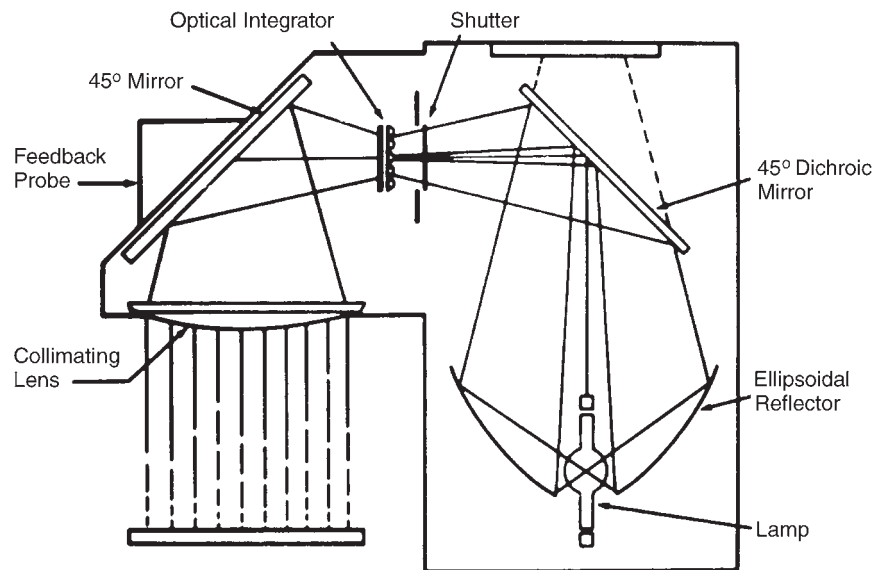


FIGURE 26.15 Configuration of lamp and optics for a collimated contact printer. A noncollimated source is identical except for the collimation lens in the lower left. (Reprinted with permission of Optical Associates, Inc., Milpitas, California, Technical Literature.)

opaque, resulting in poor linewidth control and reduced resolution. The sensitivity to off-contact exposure varies among photoresists, and newer resists are formulated with increased off-contact latitude.²⁴ Since the lamp's spectral output degrades over time, the lamp must be routinely replaced to maintain a stable photoprocess. The exact frequency for replacement depends on the line and space definition required, but the lamp life is typically 1,000 hours.

Failure to replace a lamp can result in it exploding and damaging the optical elements in the exposure unit, which is far more costly than routine maintenance.

26.6.4.1.5 Noncontact Exposure Equipment. Semiconductor imaging demonstrated the yield limitations in using contact-exposure equipment. Noncontact methods had to be developed to achieve acceptable conductor yield as critical dimensions decreased to $0.18\ \mu\text{m}$ and below.

The PWB industry is following this evolution, driven by the increased demand for products with fine features of $25\ \mu\text{m}$ and less. Semiconductor tool concepts cannot be used directly due to important differences between IC and PWB products, namely the physical size of the substrate and features to be imaged and the flatness of the substrate. The key to noncontact methods is the use of appropriate optics for clear image placement in the photoresist (Fig. 26.16), even if the image transfer function has degraded. For PWB applications, this includes the depth of focus to allow for panel warpage and the resolving power, given the contrast of the resist. The following approaches address these concerns and are viable alternatives to contact printing.

26.6.4.1.6 Proximity Printing. This is the oldest method for off-contact printing and requires no modification to the equipment optics. The phototool is held out of contact from 125 to $500\ \mu\text{m}$. The image in the photoresist suffers from the distance between the phototool and the part allows exposure under the opaque area and imaging of debris on the phototool. Nevertheless, resolution as fine as $75\ \mu\text{m}$ has been reported for proximity printing with thin coatings of liquid resist.²⁵

26.6.4.1.7 Projection Printing. Three approaches are possible for this technique: scanning, stitching, and magnified projection printing. Scanning and stitching evolved from semiconductor

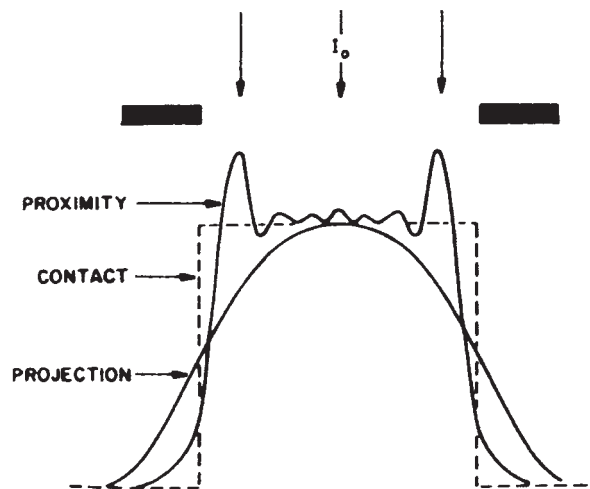


FIGURE 26.16 Image transfer for contact, proximity, and projection printing.

and MCM-D thin-film technology, where smaller, flatter substrates are used. They require movement of the phototool and/or the substrate during exposure. Magnified projection imaging is unique to the PWB application and has no moving optical components. A schematic of all three systems is given in Fig. 26.17.

- The scanning printer requires the synchronized movement of the part and the phototool during exposure. Precise alignment of the two pieces must be maintained during the motion. Periodic adjustment for flatness is usually required since this equipment has a small depth of focus. For typical PWB formats, a large phototool is needed, requiring expensive glass phototools for their flatness, rigidity, and sharp line definition. This exposure technique has demonstrated high resolution over a large, relatively flat area using a high-contrast resist.²⁶ Few PWB applications exist, but the technique is useful for flat panel display manufacture.
- Stitcher projection printers are step-and-repeat tools that use a repeating image or “stitch” together several images. The artwork generation and management in the equipment are complicated, which has hampered these printers widespread use for large panels. The usual active area size as defined by the optics is approximately 6 in. × 6 in. Thus, for a standard 18 in. × 24 in. panel, 12 artwork changes are required to expose one side. These systems have very high resolving capability and large depth of focus. Again, glass artwork is used, but these smaller plates are easier to generate and use than in a scanning projection printer.
- The magnified projection imaging concept was first demonstrated in the late 1980s with the SeriFLASH exposure tool, utilizing 436 nm illumination and a 5 in. × 5 in. liquid crystal display as the phototool. The image was magnified six times to expose an 18 in. × 24 in. panel, but demonstrated photoresist definition was limited to 125 μm since the liquid crystal features were one-sixth of the final conductor width. The equipment was subsequently modified for 365 nm exposure with a glass phototool to improve resolution. Fifty- μm line and 63 μm space resolution has been demonstrated.²⁷ The exposure time required is similar to that of contact exposure equipment. With optimized optics, this may become a high-resolution tool that utilizes conventional photoresist and phototools.

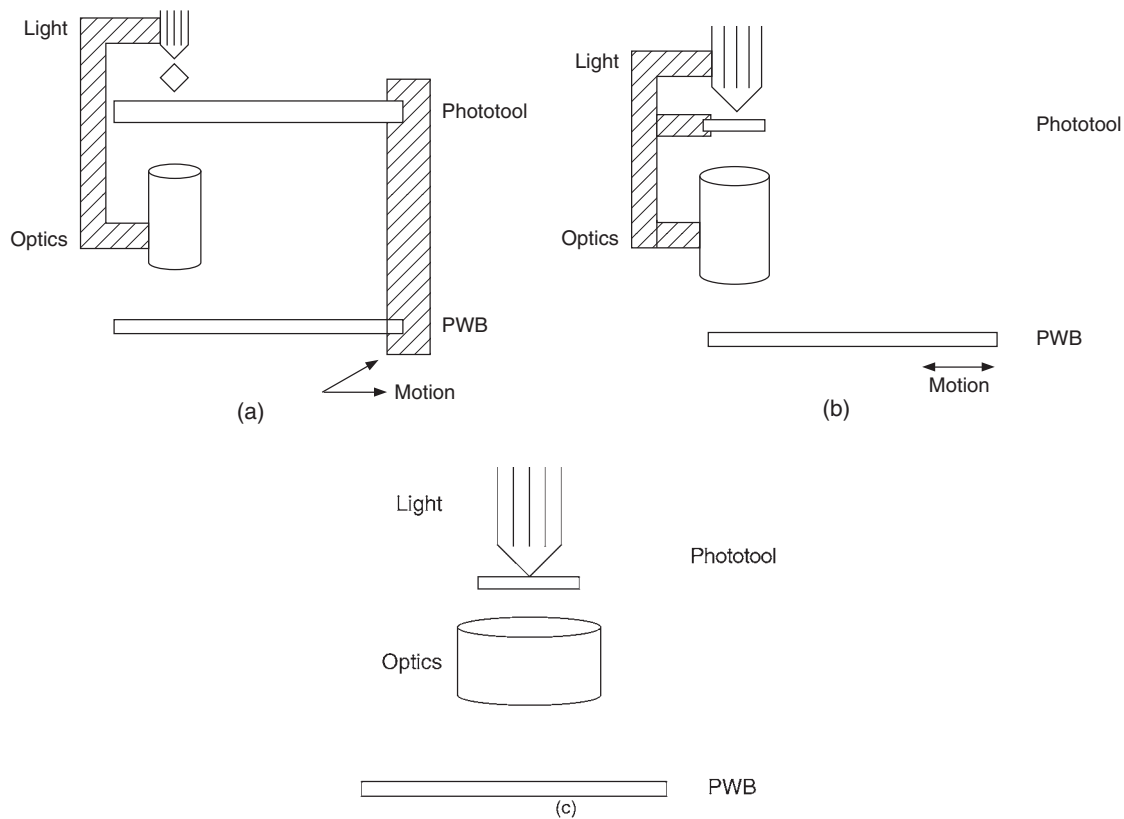


FIGURE 26.17 Configuration for projection imaging equipment: (a) scanning, (b) stitching, and (c) magnified.

26.6.4.2 Laser Direct Imaging. The LDI method of exposure provides the ultimate in flexibility for customized pattern compensation factors and for engineering changes to the product design since it does not require a phototool. Systems introduced in the 1980s used an Ar^+ laser with visible optics, requiring specialized photoresists that were sensitive to visible light. Improved Ar^+ systems relied on the UV wavelengths, making it compatible with conventional photoresists. However, high-speed photoresists were needed to achieve the productivity for high-volume production. Concerns about the lifetime (3,000 to 5,000 hours) and power consumption (60 to 80 kW) of gas lasers led to development of solid-state laser systems at various wavelengths.^{28,29,30} The initial solid-state laser systems used 355 nm with a polygon mirror to scan the panel. Recently developed LDI systems have used digital mirror devices (DMD) instead of polygon mirrors and image at a wavelength of 405 nm. Filters are used to block 355 nm light, extending the lifetime of the DMD device. Due to the small size of the individual mirrors, about 1.5 microns, DMD technology provides better resolution than an 8,000 dpi polygon mirror system. However, the area coverage is smaller and several DMDs working in parallel are needed to expose a PWB panel. Systems have also been introduced that use no photoresist at all, laser ablating either tin for use as an etch resist or physical vapor deposition (PVD) copper on polyimide for use as a plating base.^{31,32} In addition to varying in laser type and wavelength, specific equipment designs differ in optics, either single- or multiple-beam operation; platen design; single- or double-side exposure; pixel shape; and spot size and resolution.

Multiple-beam operation increases exposure productivity, a key requirement for economic feasibility in large-volume manufacturing. Target production rates for the various systems ranged from 60 to 180 panels per hour (18 in. $\times$ 24 in. with 50 μm features). However, installed LDI systems have been used primarily for prototype and small-lot, quick-turn production of high-density boards. For these applications, savings are achieved due to artwork elimination and reduced setup time. For volume production of medium- to high-technology boards, it is possible to achieve an economic return through yield savings and the ability to produce designs that had not been technically or economically possible with conventional imaging.³³ LDI technology makes it possible to scale the electronic data and compensate for dimensional changes in sequential build-up (SBU) structures. Although the UV systems can expose conventional photoresist, use of high-speed photoresist is needed to maximize tool throughput. Most LDI systems use a flatbed platen design and can image both innerlayers and outerlayers.

Systems with an external drum architecture, similar in design to laser photo plotters, are limited to innerlayers because the panel must have sufficient flexibility to conform to the drum (Fig. 26.18). The pixel shape can be either square or gaussian. Square pixels are made up

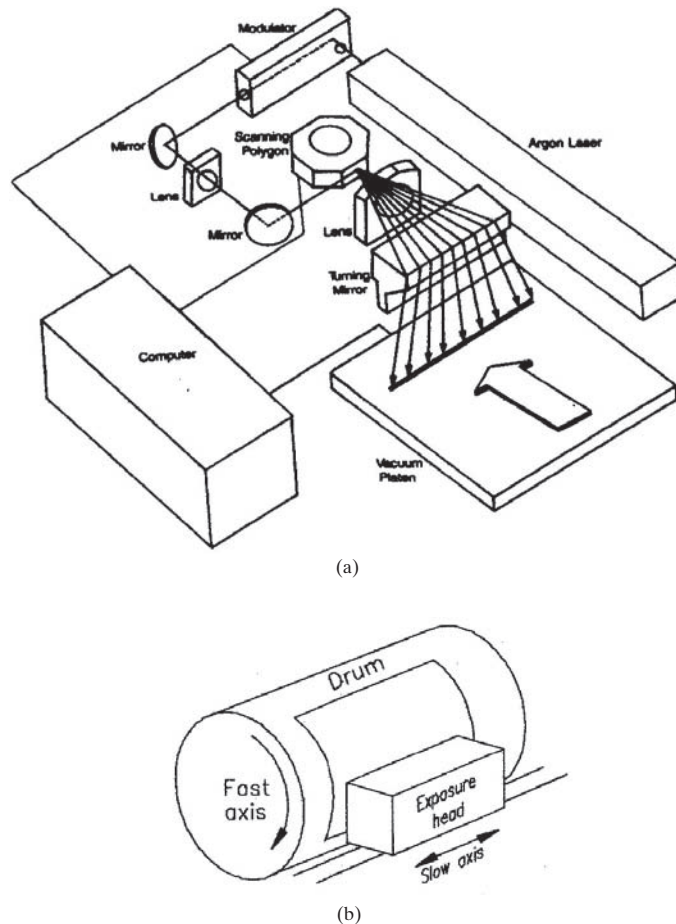


FIGURE 26.18 Schematics of laser direct imaging equipment: (a) flatbed platen; (b) external drum.

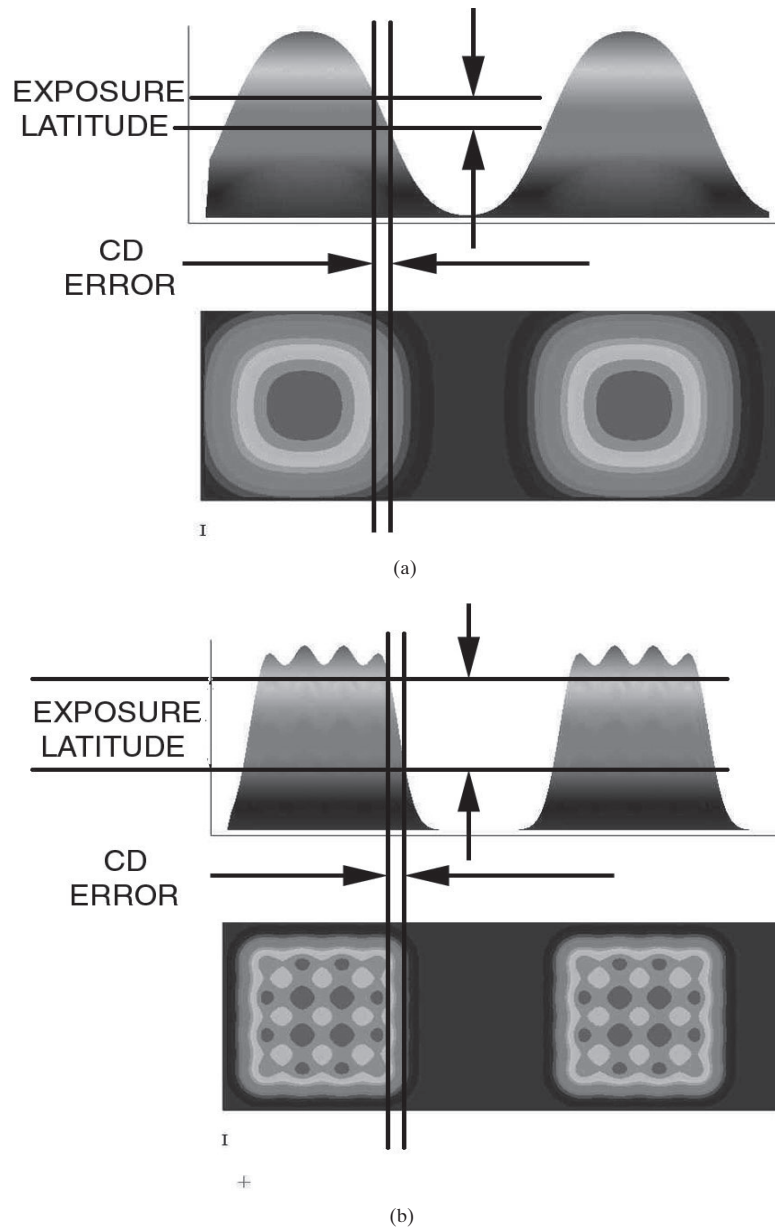


FIGURE 26.19 Computer simulation of aerial image for a $25\ \mu\text{m}$ feature: (a) four $12.5\ \mu\text{m}$ laser spots on $6.25\ \mu\text{m}$ pixel spacing; (b) four $6.25\ \mu\text{m}$ laser spots on $6.25\ \mu\text{m}$ pixel spacing.

of many point sources of light and can theoretically achieve perfect stitching. However, in real systems there is intensity variation due to mechanical vibration and edge rounding. Gaussian pixels use a single-point source and may have less intensity variation. Due to the diffraction-limited nature of light, greater depth of focus can be achieved.³⁴ Figure 26.19 illustrates that

LASER PARAMETERS	PLOT for 2 mil line	PLOT for 2.5 mil line
Addressability 1.0 mils Spot Size 1.0 mils		Not Possible
Addressability 0.5 mils Spot Size 1.0 mils		
Addressability 0.5 mils Spot Size 0.5 mils		

FIGURE 26.20 Final image dimension as governed by spot size and addressability of a laser plotter or laser direct exposure tool.

imaging with a smaller laser spot size gives steeper aerial image sidewalls, increasing process latitude.³⁵ In addition to spot size, addressability of the beam is important in determining the system resolution, as shown in Fig. 26.20.

In selecting an LDI system, you must consider both the capital cost and operating cost. However, the critical factor is that the equipment combined with the photoresist material is capable of achieving both the resolution needed for the product mix and the productivity needed for the production volume. Photoresists for LDI are available that are compatible with the various metallization processes.³⁶

26.6.5 Develop

In this process step, the solubility difference between the exposed and unexposed areas of the photoresist creates a relief image of the master pattern. The panel is immersed in an appropriate solvent, and the process conditions are adjusted to control the clearing time for dissolving the unexposed areas for negative photoresists or exposed areas for positive ones. Total dwell time is set to approximately double the time to clear, commonly called a 50 percent breakpoint. Solution concentration, temperature, and agitation are key variables. The resulting photoresist images should be distinct, with vertical sidewalls. Failure to achieve this indicates that one of the previous steps requires adjustment. For images larger than the phototool dimension, the cause is either incomplete development, overexposure, or poor contact during exposure. For images that are smaller than expected, either the exposure dose is too low or development is too aggressive. Distorted images can be caused by problems with preclean, application, or exposure. The common equipment for developing is spray conveyorized, either horizontally or vertically.

Additives are used in the developer solution to prevent foaming. The solution is filtered to remove resist particles and either replenished with fresh solution to maintain a consistent dissolved resist content and solution concentration or operated continuously for a certain amount of product and then replaced. Waste-developer solution is treated (aqueous and semi-aqueous) or distilled and reused (solvent). Rinsing is important in stopping the dissolution and, for aqueous photoresists, water with a high-mineral content often improves the resist image and the conductor yield. Tank systems can also be used with photoresists that have a wide-process latitude. Ultrasonic agitation is often used to aid in the dissolution.

There are additional steps that improve the resist removal in the line channels and the conductor formation yield. Plasma treatment has been used effectively to improve product yield, especially with respect to shorts in a print-and-etch process. In addition, for some aqueous-developable dry films, a heat treatment after exposure has improved the space definition, and spaces equal to or smaller than the resist height have been resolved. Thus, these process steps ensure that tight resolution requirements can be met.

26.6.6 Strip

After the pattern transfer has been completed, the photoresist is removed from the substrate using equipment similar to that used for development. The stripping solution swells and dissolves the photoresist, stripping it either in sheets or as small particles. The equipment design must effectively remove and separate the skins. Often, brushes and ultrasonic agitation are added to aid in the resist removal. As with developing, filtration is important to keep the spray nozzles clean and keep fresh solution reaching the panel. For stripper chemistries that oxidize the copper, an antitarnishing agent is often added either to the stripping solution or as part of the rinsing.

26.7 DESIGN FOR MANUFACTURING

As design features are continually reduced to produce higher-density interconnects, tighter control of every step in the conductor formation process is required to achieve high yield. The maximum possible yield with an etching or plating process depends on the conductor dimensions such as the conductor pitch in terms of line and space, the conductor thickness, and the size and shape of the capture pads around plated through-holes (PTH) and vias.

26.7.1 Process Sequence: Etching versus Plating Considerations

For a specific circuit design, there is often a question of the appropriate process sequence. Although the capabilities of imaging and the pattern transfer step dictate the overall limitations, the decision depends on the unique capabilities of the manufacturing line to be used. Some general considerations can clarify the true issues for most production situations.

Photoresist patterning has different constraints for etching and plating. For etching, a thin photoresist is desirable to maximize the etchants' attack in the channel developed in the photoresist. Resolution does not limit the process, since very small spaces can be resolved in either liquid or thin dry-film photoresists. The etching process itself is key to conductor formation.

Etching the copper from the channel becomes increasingly difficult as feature size is reduced, particularly for thicker metal layers. Therefore, the key criteria defining the capabilities of the print-and-etch process is the minimum space cleared, constrained by the final conductor height and the etchant chemistry and equipment.

For pattern plating, the photoresist thickness must be greater than or equal to the final thickness of the conductor, and it must be possible to develop a photoresist channel equal to the final conductor width. As conductor thickness increases, it becomes more challenging to produce channels with a higher aspect ratio. Since photoresist resolution is on the order of its thickness, it would be difficult to resolve smaller than a 38 μm photoresist channel for 25 μm thick plating, irrespective of the final conductor spacing. Thus, the challenge for pattern plating is to resolve and develop fine channels in thicker photoresist materials and then ensure that the plating solution wets the bottom of the narrow photoresist channels.

Thus, in choosing the conductor formation process, the thickness of the conductor and the linewidth and spacing are the key parameters. A generalized relationship between them is

CHAPTER 27

MULTILAYER MATERIALS AND PROCESSING

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27.1 INTRODUCTION

Printed circuit board (PCB) structures and processes continue to be driven by device miniaturization, functional densification, and speed. The choice of components, actives and passives, and connectors are primary determinants of layer count and layer options, such as copper foil weights. Reductions in chip voltages are matched by an increase in current demand; this in turn causes increases in the number and thickness of the plane layers. More device leads combined with decreasing pitch increases the number of vias and interconnecting layers, while miniaturization and weight reduction at the product level forces reduction in the physical package for the product.

New structures or advancements on existing structures are then needed to make these interconnections. These structures—such as blind and buried vias, multi-lamination (sub-laminations), and build-up technologies—directly impact multilayer processing. Deeper blind vias and buried vias have caused a major increase in the demand for reliable via filling materials and methods. Relatively new materials, equipment, and processes have and are being developed to address this need. A new section in this chapter, “Filled Via Processing and Sequential Lamination,” addresses filled vias internal to the PCB.

Ever increasing frequencies continue to shift demand to materials with lower attenuation and propagation delay. To guarantee the electrical performance requirements of this product type and to benefit from the increased raw material and processing costs, the industry is specifying each element in the construction more so than in the past, and with less latitude. For instance, requirements for post-pressed thickness tolerance on a prepreg fill section, or surface roughness of the treatment side of the copper foil, or percent resin of the prepreg or core are much more likely to find their way onto fabrication prints.

Globalization of sourcing for PCBs continues to have a major impact on the physical design or the fabrication processes for the PCB construction. Mass lamination techniques have scaled to higher layer counts, and alternate tooling methods and panelization approaches

27.1

have contributed to increases in material utilization and throughput. These technologies increase production volumes and reduce costs and are discussed in this chapter in Secs. 27.4.4 and 27.4.6.

The latest challenge to the physical PCB is coming from regulatory bodies and consumers who demand products that are less damaging to the environment. Materials developed to meet these demands are known colloquially as either lead-free or RoHS-compliant (that is, in accordance with the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment Directive). This chapter will not deal at length in the specific requirements of this directive, but will address the major impacts to the PCB materials (see Section 27.2.3) and subsequent processing (see Secs. 27.5.5 and 27.6.2).

Lead-free joints, which have no appreciable lead content (for what “appreciable” means in this context, refer to the appropriate directive; see also Chapter 10) reflow at temperatures 30 to 40°C higher than the melt point of eutectic solder. These temperature increases have necessitated the development of newer resins or blends, different curing agents, and fillers to provide a laminate system that can survive and remain reliable after these elevated heat excursions. The changes to the laminates themselves are covered elsewhere in more detail (see Chapters 6 and 7), but those properties directly applicable to the performance of the PCB are discussed in this chapter in Sec. 27.2.2.

In some market segments, particularly the consumer market, “green” technology is an important product differentiator or even a market requirement. This chapter also introduces halogen-free laminates in Sec. 27.2.

27.1.1 Relevant Specifications, Standards, and Test Methods

Industry standards groups such as the IPC have defined properties requirements and performance specifications to facilitate the choice of laminates. Design standards are available to inform the material selection process to achieve a desirable form, fit, or function. Standardized property tests have been developed to provide a common method to test for property values and to interpret results. Some of the most commonly used are:

- IPC-2221, “Generic Standard on Printed Board Design”
- IPC-4101, “Specification for Base Materials for Rigid and Multilayer Printed Boards”
- IPC-4104, “Specification for High Density Interconnect (HDI) and Microvia Materials”
- IPC-4652, “Metal Foil for Printed Wiring Applications”
- IPC-TM-650, “Test Methods Manual”

Table 27.1 lists some laminate tests covered in IPC-TM-650.

TABLE 27.1 IPC-TM-650 Laminate Tests

Test Method #	Title
2.4.24C	“Glass transition temperature and Z-axis thermal expansion by TMA”
2.4.24.1	“Time to delamination (TMA method)”
2.4.24.2	“Glass transition temperature of organic films—DMA method”
2.4.24.3	“Glass transition temperature of organic films—MA method”
2.4.24.4	“Glass Transition and Modulus of Materials Used in High Density interconnection (HDI) and microvias—DMA method”
2.4.24.5	“Glass transition temperature and thermal expansion of materials used in high density interconnection (HDI) and microvias—TMA method”
2.4.24.6	“Decomposition temperature (T_d) of laminate material using TGA”
2.4.25C	“Glass transition temperature and cure factor by DSC”
2.6.25	“Conductive anodic filament (CAF) resistance test: X-Y axis”

27.3 MULTILAYER CONSTRUCTION TYPES

The construction of the rigid multilayer ML-PWB can take on many variations. To help categorize the various constructions, the IPC has developed industry PWB design specifications, defining them by class and type. Grouping the ML-PWB into categories facilitates the ability of designers and fabricators to communicate using a common format.

27.3.1 IPC Classifications

IPC classifications specify generic PBC design and rigid organic printed board structure.

27.3.1.1 IPC-2221: Generic Standard on Printed Board Design. There are many ML-PWB structures. This section discusses the methods and materials for the basic and several of the advanced structures. The IPC has two comprehensive standards for the design of rigid printed circuits, IPC-2222 and IPC-2226. The classification system within these standards for the ML-PWB by structure is shown. The distinction between the two is the focus on microvias in the later standard.

27.3.1.2 IPC-2222: Rigid Organic Printed Board Structure Design. This standard covers products with conventional feature sizes:

- **Type 3** This is a multilayer board without blind or buried vias (see Fig. 27.4)
- **Type 4** This is a multilayer board with blind and/or buried vias (see Fig. 27.5)

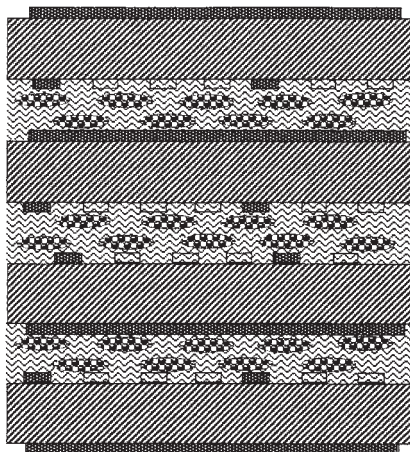


FIGURE 27.4 Type 3 (eight-layer ML-PWB) multilayer board without blind or buried vias.

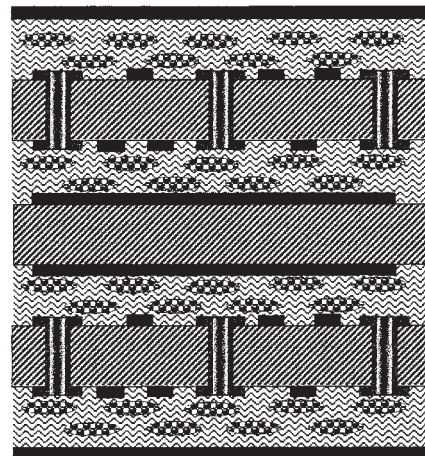


FIGURE 27.5 Type 4 (eight-layer-B/V MLPWB) multilayer board with buried vias.

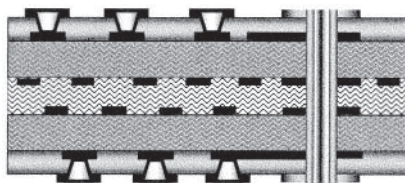


FIGURE 27.6 Type I (six-layer HDI MLPWB) high-density multilayer board with blind vias from top and bottom layers and through vias connecting the outerlayers.

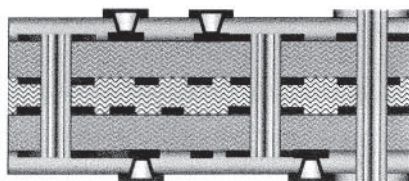


FIGURE 27.7 Type II (six-layer HDI MLPWB) high-density multilayer board with vias as well as buried vias in the core and through vias connecting the outerlayers.

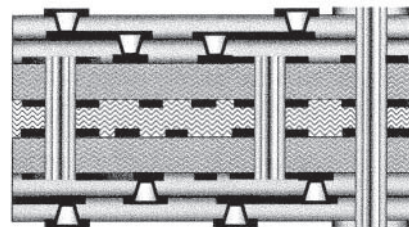


FIGURE 27.8 Type III (eight-layer HDI MLPWB) high-density multilayer board with blind vias as well as buried vias in the core and through vias connecting the outerlayers.

27.3.1.3 IPC-2226: Design Standard for High-Density Interconnect (HDI) Printed Boards.

This covers products with high-density feature sizes:

- **Type I** 1[C]0 or 1[C]1 has through vias connecting the outerlayers (see Fig. 27.6).
- **Type II** 1[C]0 or 1[C]1 has buried vias in the core and may have through vias connecting the outerlayers (see Fig. 27.7).
- **Type III** >2[C]>0 may have buried vias in the core and may have through vias connecting the outerlayers (see Fig. 27.8).

27.3.2 Basic Type 3 ML-PWB Stack-Ups

The type 3 construction can be said to be the most basic of PWB multilayer technologies. An ML-PWB is fabricated by the bonding (laminating) of copper-clad details consisting of imaged and etched laminates (typically double-sided). The bonding medium, known as prepreg, is a B-staged (partially cured) reinforced resin. The imaged details consist of C-staged (fully cured) laminate. These material components are arranged by layering according to the design documentation. This layering method in fabrication, known as the stack-up, follows the layer numbering order of the design. The stack-up formation method is often loosely defined in the design documentation; therefore, a good understanding of the lamination options is necessary. The lamination options described in this discussion refer to methods used to form the outerlayers and to form layer pairs. The material resin system should be defined on the design documentation. Refer to IPC-2221/2222 for minimum suggested design documentation requirements.

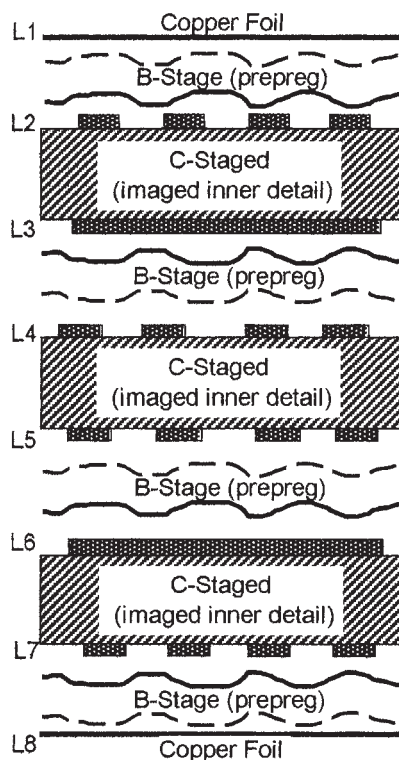


FIGURE 27.9 Foil outer stack-up (eight-layer ML-PWB), a typical stack-up for a foil board.

The basic ML-PWB stack-up can be constructed with two options to produce the outerlayers and to form layer pairs. A third option that employs single-sided “capped” clads is rarely used and is not discussed. Often, in the case of designs having an odd number of layers, a combination of these methods is employed. The following three-layer stack-up methods are discussed:

- **Foil outerlayer construction (foil outer)** In this stack-up, the outerlayers are formed by using a sheet of copper foil per side.
- **Clad outerlayer construction (clad outer)** A clad detail provides the copper for the outerlayer.
- **Odd-layer construction** This stack-up method balances a construction consisting of an odd number of layers.

27.3.2.1 Foil Outer Stack-Up. A board produced with copper foil outers is fabricated from one or more patterned innerlayer details and two copper sheets. The copper sheets form the outerlayers of the fabricated ML-PWB. This stack-up is the least expensive way to fabricate an ML-PWB and is by far the most popular design option. Figure 27.9 shows a typical stack-up for a foil outer board consisting of eight layers.

The stack-up shown contains three imaged clad details bonded with two sheets of prepreg at each opening and having two sheets of copper foil on the outside. When possible, the higher resin content prepreg ply should face the signal layer side. This is especially important when the signal is a heavyweight copper (2 oz. or more). The copper layers, numbered from L1 to L8, begin with the top foil layer (typically called the primary side). In the design pictured, the layers L2, L4, L5, and L7 represent signal layers. Layers L3 and L6 represent power/ground layers. When the final imaged patterned is produced, it can provide another signal layer pair or a set of ground layers, or a “pads-only” pattern to support vias and component holes, as well as the device footprints of the electrical components and their associated fan-out patterns. Some of the advantages of this bonding method are:

- **Lower raw material cost** Loose sheet copper foil and prepreg sheets are more economical than clad laminate.
- **Lower consumable material cost** The reduction in imaging resist and chemistry results in a cost savings.
- **Lower labor cost** The reductions in material handling and in the processes of imaging and pre-lamination result in less total labor.

27.3.2.2 Clad Outer Stack-Up. Figure 27.10 depicts the same eight-layer design as Fig. 27.9, except the outerlayers are formed with a clad laminate. This stack-up arrangement requires four clad details, as compared to only three for the foil-stacked board shown in Fig. 27.9. This makes the clad outer board more expensive than the more commonly used foil outer construction.

However, the clad outer design has one less B-stage opening and no copper foil. In addition, the clad outer boards are patterned on only one side prior to lamination. These factors partially offset the higher cost of this design. In Fig. 27.10, notice how the layer pairs have changed position placement. Layers L3 and L6 are now paired with a signal layer, which may

be advantageous for controlling the dielectric thickness. See Sec. 27.3.3 for a discussion on controlled impedance. Some of the advantages of using the clad outer bonding method include:

- **Improved surface topography** When surface flatness is critical, the clad outer construction provides a smoother surface. When a signal layer of heavyweight copper is the first layer down, it is possible for weave texture imprinting to occur. This topography condition, sometimes referred to as “telegraphing,” can sometimes imprint the circuit pattern when using a foil build-up.
- **Improved handling** Depending on the layer pairing, sometimes additional copper can be retained, as in a case where a signal-to-signal imaged detail can be avoided. This is mostly the case when the layer pair details are being produced on very thin core laminate.
- **Improved dielectric thickness control** Sometimes, it is necessary to control the thickness at a specific layer pair tightly. This could be due to high-voltage considerations or to aid in the precision spacing of a signal plane to a ground plane where controlled impedance is necessary. This is possible because the C-staged (fully cured) clad laminate typically has an improved thickness tolerance.

The chief disadvantage with a clad outer layer design is in the potential for lower yield. This is because the external copper foil must be protected by the image mask during all the internal layer image, etch, strip, and oxide processing steps; then the mask must be removed at a later point in the process so that the external details can be fabricated. The potential exists to scratch the photomask during all the handling steps, which will result in shorts or opens (depending at which point in the process the scratch occurs).

27.3.2.3 Odd-Layer Stack-Up. Sometimes, due to signal routing or the need to have a greater dielectric space, an odd-layer circuit is formed. Similar in characteristics to the clad stack-up, the odd-layer construction technique employs a non-imaged single-sided clad laminate. Material can be procured with a single side, but a warning is associated with its use due to a lack of bondability. When this material is manufactured at the laminator supplier with only copper on one side, a release sheet is used against the non-copper side. The release sheet produces a slick, smooth surface. The non-copper surface thus requires an aggressive surface preparation to promote bondability. One alternative to gain the same benefit of the single-sided clad is to etch the copper off one side of a double-sided clad. The etched side becomes the bond surface, which has greater adhesion due to the copper tooth imprint left behind. See Fig. 27.11 for an example of a balanced odd-layer construction.

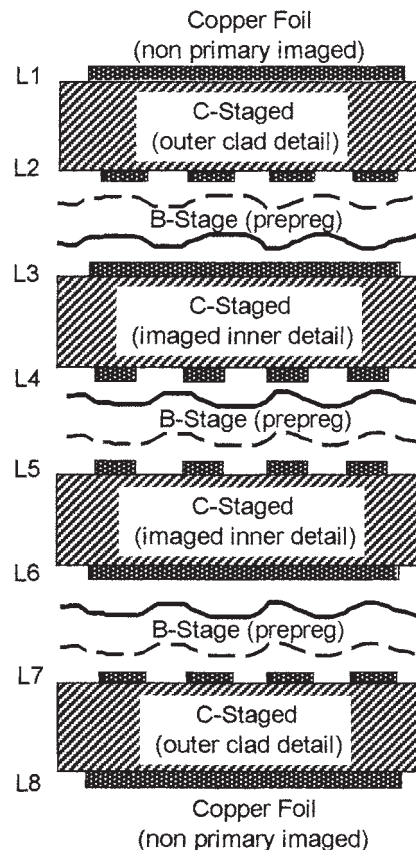


FIGURE 27.10 Clad outer stack-up (eight layer ML-PWB) multilayer board design with the out-layers formed with a clad laminate.

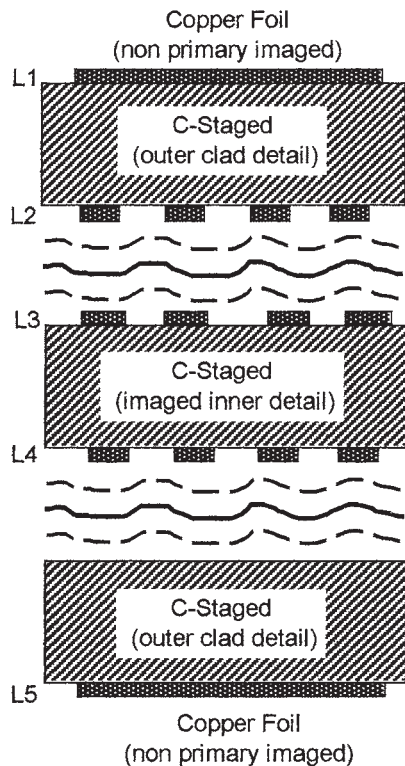


FIGURE 27.11 Odd-layer clad stack-up (five-layer ML-PWB), an example of a balanced odd-layer construction.

Some of the uses of the single-sided odd-layer stack-up are:

- **Odd-layer construction option** The single-sided construction technique allows an opportunity to supply a layer for circuit designs having an odd layer count.
- **Odd-layer core balance** One of the problems associated with a build-up of odd-layer circuits is the ability to maintain a balanced construction of the cores. Depending on the overall design thickness and layer count, this can become a major concern to reduce warping. Figure 27.11 depicts an example of an odd-layer stack-up with three equal core thicknesses.

27.3.3 Controlled-Impedance Stack-Up

The number of ML-PWBs containing controlled impedance signals is significant. The signal lines in an ML-PWB have a characteristic impedance value expressed in ohms (Ω). Active devices, connectors, and transmission lines also have characteristic impedance. In a high-speed circuit environment (typically starting at 2 to 3 MHz and above), if the signal energy is reflected rather than transmitted, the signal impedance mismatch is known to have discontinuity. This means that, to avoid signal losses due to reflections, all impedance characteristics must be matched. The physical relationship between a signal line and the surrounding power/ground layers determines the impedance of that signal line.

The controlled-impedance stack-up requires specific manufacturing discipline that must be adhered to in order to maintain the integrity of the designed circuit. An ML-PWB design requiring a controlled-impedance fabrication for a design for manufacturing (DFM) discussion between the designer and manufacturer in order to avoid producibility traps and induced error. Several resources are available to assist in developing the

proper manufacturing parameters to ensure that the product meets the specified tolerance. IPC-2141, "Controlled Impedance Circuit Boards and High Speed Logic Design," and IPC-317, "Design Guidelines for Electronic Packaging Utilizing High-Speed Techniques," are two of the industry standard documents that contain formulas and examples of various impedance configurations.

Typical producible process tolerances for common impedance values are as follows:

- 50 Ω traces typically have a tolerance around 5 to 7 percent.
- 75 Ω traces typically have a tolerance around 12 to 15 percent.
- 100 Ω traces typically have a tolerance around 17 to 20 percent.

When tolerances are required to be tighter than this, it places more significance on the stack-up and etch of the circuit. The design requirement should be clearly specified in the ML-PWB documentation. The preferred way to specify an impedance requirement is in a drawing note rather than by applying dimensional boundaries. Firm dimensional boundaries do not allow the manufacturer freedom to meet the end requirement based on process knowledge.

It is recommended that during the design process software modeling be performed and then confirmed with the manufacturer before fabrication. Several excellent simulation software tools are available commercially. Some also exist as freeware and shareware. However, it is best to

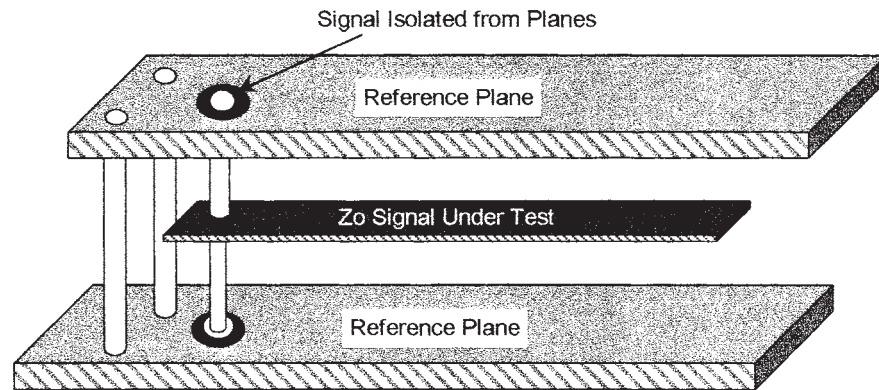


FIGURE 27.12 Example of impedance test coupon design and layout.

confirm the models' predicted values by actual process verification. The most versatile method of verification is with a test coupon. The test coupon should accurately represent the construction configuration of the stack-up, except it requires a few special prerequisites in order to yield reliable test data. Figure 27.12 shows a typical impedance test coupon stack-up. Note that the signal reference planes of the coupon are shorted together. Also, the simulated signal line is isolated and open-ended; the signal lines are usually at least 6 in. long. The footprint of the coupon via holes that feed through to the surface should be verified to match to the spacing of the time domain reflectometry (TDR) instrument probe. This will reduce the risk of rendering the specimen not testable or necessitating the use of expensive adjustable probes. The IPC test method IPC-TM-650 2.5.5.7 contains suggested spacing, but it is best to confirm this with the manufacturer's preference. Examples of some common impedance types are shown in Fig. 27.13.

The factors most influential on characteristic impedance are:

- **Dielectric separation (H)** The separation of the signal line between the reference planes has a significant influence on characteristic impedance. The variability of the dielectric layering must be reduced to minimize the effect on tolerance. This is where stack-up selection becomes critical when determining whether the signal-to-plane opening will be made with a clad laminate or within the bondable area of the B-staged (prepreg) resin. This is also where glass

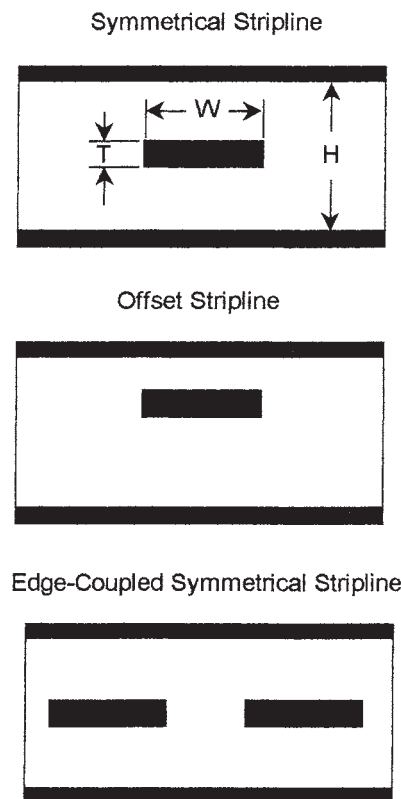


FIGURE 27.13 Examples of common impedance stacks.

style selection becomes important. The glass style and subsequent resin content will have different effects on the nominal thickness obtained.

- **Conductor width (W)** The finished width of the conductor can produce variance, which is likely to occur from lot to lot. Therefore, process control measures are necessary when producing controlled impedance circuits. The density of neighboring circuits will have an effect on the final etch. Often it is advantageous to modify the artwork line width at phototool generation for predicted variance.
- **Dielectric constant (D_k)** Choosing a laminate resin system with a consistent dielectric constant has an influence on characteristic impedance over higher frequencies. The influence of dielectric constant becomes most critical when the ML-PWB design is a high-layer-count design. The lower the D_k value of the resin system, the thinner the overall board can be. Typically, the manufacturer has little opportunity to affect the dielectric constant, because the material type is specified by the design. Here, it is important that the designer/manufacturer know the D_k value range of the laminate supplier's resin system. Caution: Do not use the D_k value of the neat resin, but that of the composite laminate, which will vary somewhat with glass style. This is sometimes referred to as effective D_k (Eff D_k).
- **Conductor thickness (T)** The conductor thickness or copper weight can also affect the final impedance value. Here, as with conductor width, manufacturing process variations can have an inverse effect on the precision of the impedance value. Some modern software simulation tools, such as those from Polar Instruments, Inc., allow values for conductor profile (area) to be included in the simulation. This is more significant when lines are of heavy copper. It is best to avoid routing of impedance lines on plated subcores due to the added variability.

For external impedance tracks and internal plated-up tracks such as on subcores, autothieving patterns will minimize large variations in plating height between tracks in dense areas and those in uncongested areas. This will increase the fabricator's ability to produce impedance values consistently within a smaller range.

27.3.4 Sequential Laminations

When a design includes buried and/or blind vias, it typically requires a set of sequential lamination and plating cycles. These technologies are defined in the industry design standard IPC-2221/2222 and are known as Type 4 ML-PWBs. These build types, when employing industry standard feature sizes, are mature in the industry. Complementing technologies, employing use of sequential processes for ML-PWB designs containing microvias less than 0.15 mm, are considered as build-up technologies. The terminology of build-up technologies encompasses many design stack-up variations; they can take on many forms and employ a multitude of methods. The build-up technologies defined in IPC-2315 and IPC-2221/2226 include categories named Type I, II, III, IV, V, and VI. The advanced build-up technologies use the materials found in IPC-4104. These include materials for layer forming, dielectric insulation, and interconnectivity. Included are photo-imageable and non-photo-imageable materials (liquid, paste, or dry-film nonreinforced dielectric); adhesive-coated dielectrics (reinforced and nonreinforced); and conductive foils and paste (coated and non-coated, photo-imageable). For a detailed discussion of these processes, see Chap. 22 and 23. This discussion will limit itself to addressing processes for standard technology Type 4 and advanced technology build-up Types I, II, and III, which can be manufactured with conventional processes.

27.3.4.1 The Buried Via Stack-Up. To avoid hopelessly complex routing, each signal net is generally routed using only one pair of layers with what is called *Manhattan geometry*. This means that diagonal routing is avoided and all signal lines run in a horizontal or a vertical direction. To avoid blockage and side-to-side cross-talk problems, horizontal lines are run on

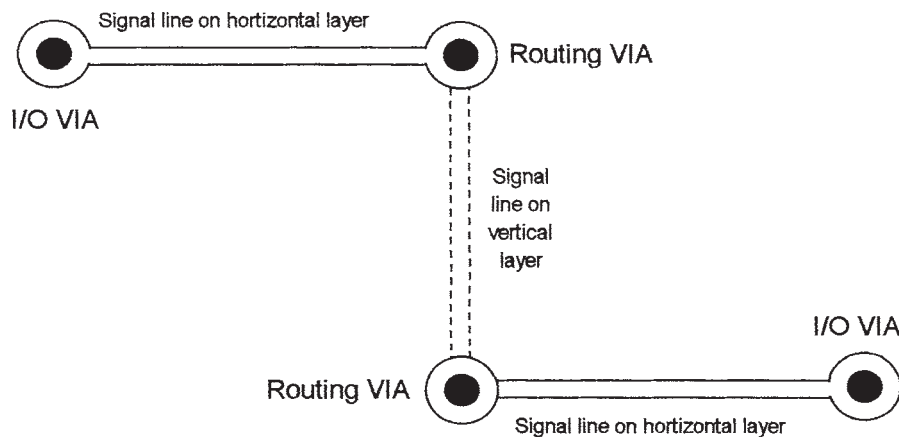


FIGURE 27.14 An example of a net routing using Manhattan geometry.

one layer and vertical lines on the other. This means that, in addition to a via at each end of the net (I/O via), most nets need one or two additional vias (routing vias) to change direction from horizontal to vertical. Figure 27.14 shows an example of Manhattan geometry.

The net shown in Fig. 27.14 has two I/O vias and two routing vias. The I/O vias connect the signal lines to the board surface, where the net connects to an input or output point of an active circuit. The routing vias are used to change directions from horizontal to vertical. With through-hole vias, the routing vias pass through all layers, consuming valuable routing space. A high-layer-count board with many signal layer pairs can run out of via sites. In this case, additional layers will not improve routing completion and the board is said to be via-starved. One solution to a via-starved board is to use buried vias. The buried via connects two adjacent signal layers and provides routing vias without affecting routing on other layers. Figure 27.15 shows an eight-layer board with two buried via layers.

Buried vias do not pass through the board, so they do not congest the routing on other layers. In addition, the same via site can be used simultaneously on different layer pairs. Since buried vias are drilled and plated in the thin laminate prior to lamination, they can be very small and positioned very accurately, saving additional routing space. In some applications, buried vias are placed where needed with no reference to a predetermined grid. This gridless routing approach gives very high computer-aided design (CAD) autoroute completion.

To benefit from buried vias, signal layer pairs must be routed on opposite sides of the same C-stage component. In Fig. 27.15, L4 and L5 are the only buried via candidates. In Fig. 27.10, no signal layers can benefit from buried vias. The design shown in Fig. 27.15 is able to use buried vias on two layer pairs because a power/ground layer pair separates them. In non-buried via designs, it is best to use one power/ground plane between each signal layer pair. This gives cross-talk isolation and impedance reference. A buried via design uses a second redundant layer to force the next signal layer pair onto the same imaged detail. In other words, for a high-layer-count design to use buried vias on all signal layer pairs, power/ground plane pairs must be inserted between each signal layer pair. This increases the number of layers in the board and increases cost. Another disadvantage of buried vias is the cost associated with the extra drilling and plating operations.

27.3.4.2 The Blind Via Stack-Up. Another via option is the blind via, which connects the surface layer to one or more internal layers but does not go through the board to the opposite outside layer. Figure 27.16 shows an example of an eight-layer ML-PWB with both blind and

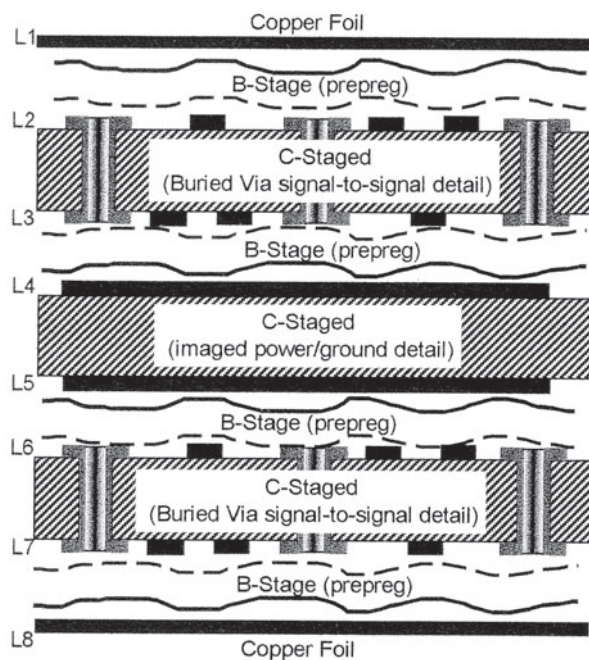


FIGURE 27.15 Type 4 (eight-layer B/V ML-PWB), an eight-layer board with two buried via layers.

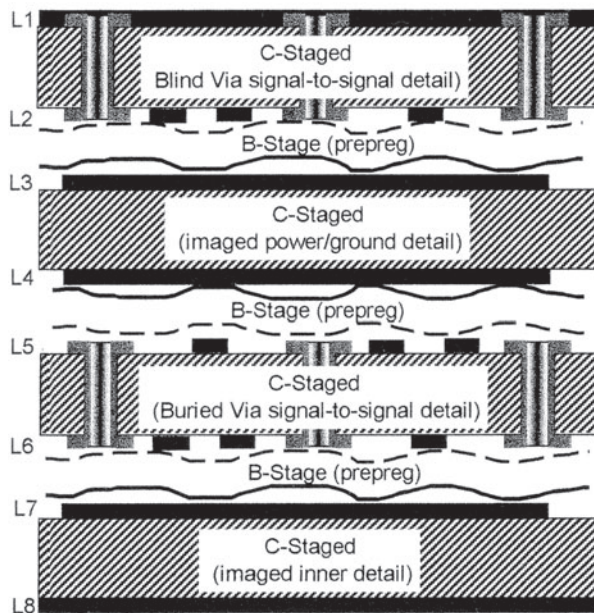


FIGURE 27.16 Type 4 (eight-layer blind and buried via ML-PWB). The design contains buried vias connecting L5 and L6. Blind vias connect layers L1 and L2.

buried vias. The design shown in Fig. 27.16 contains buried vias connecting L5 and L6. Blind vias connect layers L1 and L2. The buried vias can be fabricated in layer details as described earlier or can be fabricated by blind drilling. Blind vias may become very important in very dense double-sided surface-mount designs that have interference between I/O vias from opposite sides on the board. If this is particularly troublesome, a via-in-pad (VIP) approach or dog-bone escape pattern is used. The VIP approach places a blind hole directly in the device I/O pad. The dog-bone approach places a blind hole in an adjacent pad next to the solderable land.

A second application for buried vias is to ensure complete side-to-side electrical isolation. This is particularly important in wireless designs where the RF circuits must be shielded from other circuits. Through vias allow RF electric fields to escape from a shielded region. A blind via eliminates this problem and allows RF functions to be combined with logic and control functions on the same board.

The ultimate use of blind vias is effectively to convert a dense double-sided surface-mount design to a pair of less-dense single-sided surface-mount designs. To see how this is possible, visualize an ML-PWB with fine-pitch SMDs on both sides as two separate boards with some level of side-to-side interconnection. If the board is manufactured as two separate subassemblies, the I/O connections on one side will not interfere with the I/O connections on the opposite side. For example, consider a 16-layer board fabricated as two 8-layer subassemblies. The subassemblies are laminated, drilled, plated, and patterned like a standard ML-PWB, with the exception that the sides that will become the board exterior are blanket-metallized. After patterning, the two subassemblies are laminated together and then processed as a standard ML-PWB. This process is another form of sequential lamination. The only through holes required in this design are the relatively few that provide side-to-side interconnection. Since each via site is used twice, a 100 mil. grid may replace a 50 mil. grid, providing a significant increase in innerlayer routing resources. This type of ML-PWB structure is very costly and has mostly been replaced with the routing features of the high-density design.

27.3.4.3 The High-Density Stack-Up. The buried via stack-up design came about for a solution to gain signal routability when CAD routing solutions were pressed to the limit. Early on, Type 4 designs were considered specialty products and utilized standard-feature-size characteristics. With the advent of more sophisticated CAD routing tools, it became possible to auto-route with greater efficiency, sometimes avoiding the necessity and cost of buried vias. Soon high-I/O, full-matrix components created new interconnectivity demands. Today buried via sections defined as cores in IPC-2221/2226 are used for the central starting point of manufacture, and then build-up layers are applied to complete the design as an HDI structure. As noted earlier, the common discriminator that separates the high-density design from a conventional Type 4 is mainly the feature size. For example, the HDI Type II, as shown in Fig. 27.7, uses a conventionally processed ML-PWB Type 3 board as the core (L2 to L5) and the PTHs become buried after the high-density features of L1 and L6 are added. Microvias are used to form a connection to L2 and L5; then through holes are formed to tie L1 through L6. The microvias and holes are now metallized in one cycle. The build-up layers in the example use thin dielectrics to provide a close proximity to the adjacent layer. This is required to accommodate the microvia connection and maintain producibility for metallization.

Figures 27.17 to 27.19 show a comparison of the HDI build-ups for Types I, II, and III. In each case, complexity is added by building add-on layers sequentially. The build-up layers are typically for signal routing and contain low copper weight. Dielectric-coated (nonreinforced) microfoils (as thin as 9 to 12 μm) are employed to provide a low-profile thickness after copper plating. This is needed to facilitate the image of fine-line widths typically associated with HDI. These styles of circuits offer some economy through use of a variety of dielectrics. The use and style of construction type must be matched with the product's expected application environment and operating life. Often the need for CTE match of area array components compels the application of a non-woven aramid layer at the surface. The resin system selection should be based on the expected CTE mismatch concerns, such as when a ceramic device is surface-mounted to the assembly. Thermal cycling of power on and off can cause earlier failure when a large mismatch is present.

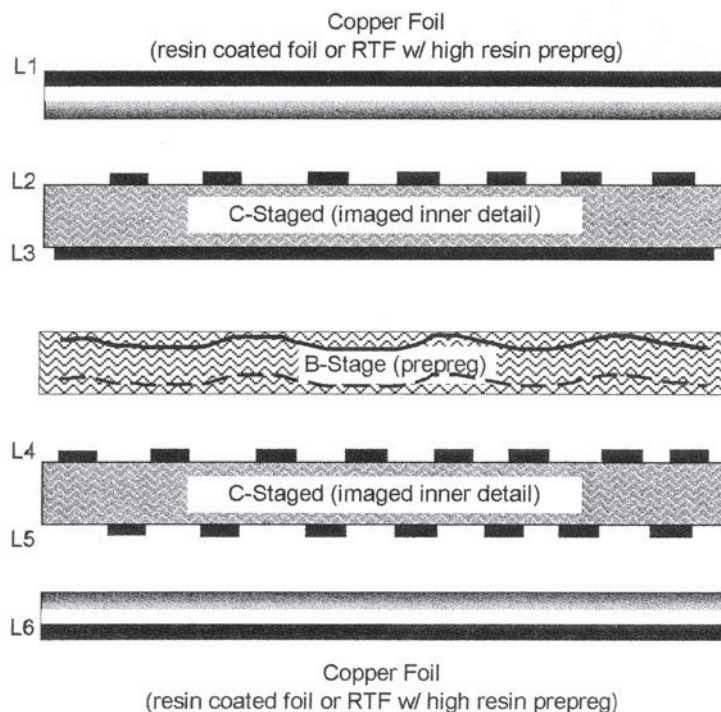


FIGURE 27.17 Type I (six-layer HDI stack-up) shows one example of how to stack up an ML-PWB with HDI features.

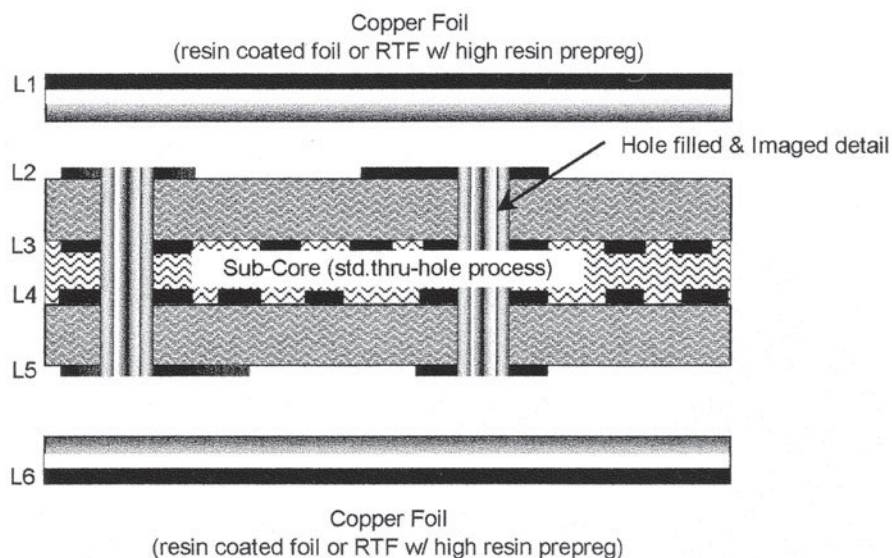


FIGURE 27.18 Type II six-layer stack-up having at its core a four-layer board with through holes, which later become buried.

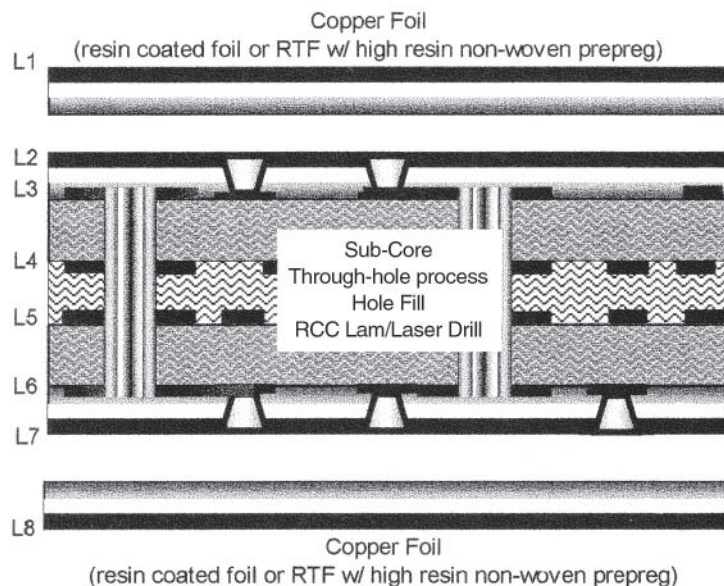


FIGURE 27.19 Diagram showing how an HDI Type III (eight-layer HDI stack-up) might be produced employing conventional lamination techniques.

Manufacturing capability becomes critical when targeting HDI features. The IPC has taken the responsibility of developing industry standards to assist in benchmarking and quantifying capability limits. Manufacturing features such as imaging, etching, hole formation, plating, and lamination registration are all strained and must be optimized. Other processes that are equally challenged are the end-product continuity testing to access the high-density features.

27.3.4.3.1 HDI Type I Stack-Up. Figure 27.17 shows one example of how to stack up an ML-PWB with HDI features. The economies of this design are obvious because it requires only one lamination cycle. The density push in this level of HDI focuses on imaging and microvia routing. By routing at a high circuit density, the surface area of the board is better utilized. The outerlayers are typically formed with a low height dielectric. When utilizing conventional lamination, this is usually a resin-coated foil or a microfoil bonded with a high-flow non-woven aramid prepreg. Special non-woven series of aramid fiber laminates have been developed to yield an equivalent dielectric thickness of 1.9 mil.

Special handling is required for the microfoils, which are usually 9 to 12 μm thick. To facilitate handling, a sacrificial carrier foil is sometimes cohered to the microfoil externally for added stiffness. After lamination, one option is to process the microvias through laser drilling and conventional through-hole drilling. Sometimes a clad outer construction may be best, depending on the laser technology chosen. For example, infrared (IR) (CO_2) laser ablation using an etched mask (small etched openings the size of the via) in the outer copper can be performed at primary print. This process helps reduce possible misregistration error. One metallization cycle is required to tie in all vias electrically. This reduces costs compared to sequential cycles.

27.3.4.3.2 HDI Type II Stack-Up. Density demands, when not met by the single lamination approach of Type I, must then address the use of sequential processing when employing standard ML-PWB techniques. The Type II stack-up shown in Fig. 27.18 has at its core a four-layer board with through holes, which later become buried.

27.3.4.3.3 HDI Type III Stack-Up. The use of a Type III structure may be employed when routing densities are greatly pressed. At this point of complexity and above, alternative

CHAPTER 63

MANUFACTURING OF FLEXIBLE CIRCUITS

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63.1 INTRODUCTION

Basically, it is possible to produce the standard constructions of single- and double-sided flexible circuits and multilayer rigid/flex for small volume—if there is a set of manufacturing facilities for multilayer rigid circuit boards. However, it is not easy to achieve high productivity, with high process yield, for volume production of flexible circuits using these facilities, as they are not designed to deal with the unique issues of flexible circuits, such as their thin, flexible material. Therefore, manufacturing facilities for high volume flexible circuits must be designed to take advantage of these differences, including specific equipment and process conditions, as discussed in this chapter.

Table 63.1 shows the specialties for processing the flexible circuit materials. Most of the issues are caused by their complicated structures and fragile materials. The coverlay structures and the stiffener constructions require supplemental manufacturing processes, making process yields lower. The varieties of outer shapes make material yields and productivity lower. Thin, fragile materials can easily incur serious mechanical damage due to rough handling. Thin materials can also undergo significant dimensional changes in the manufacturing processes. They cause a pattern shift between the processes and make the process yields lower. High-level automation has basic barriers, discussed later, when applied to the manufacturing process for flexible circuits, because of its unstable materials. Many processes must be conducted by manual methods, which are, of course, labor intensive.

Process elements particular to flexible circuits are required to achieve a high manufacturing yield. Also, an appropriate total process design is required to achieve high productivity with high yield.

A roll-to-roll (RTR) manufacturing system is a high-productivity solution for volume production of flexible circuits. However, the RTR lines are not flexible for a non-standard construction, and they are available for only the early steps of the long manufacturing processes. Also, RTR processes have many limitations to apply.

63.2 SPECIAL ISSUES WITH HDI FLEXIBLE CIRCUITS

High-density flexible circuits, which have been developed since the mid-1990s, have special constructions and therefore require supplemental processes. In addition, high-grade manufacturing technologies are required to generate finer circuits. Sometimes, they are called HDI

63.1

63.3.10 Etching

Ferric chloride or cupric chloride solution is recommended for use as the etching chemicals for flexible circuits, especially for high-density circuits. An alkaline solution has a higher process speed, but is not good on fine circuits because of unstable etching rates. As an alkaline solution makes some chemical attacks on polyimide surfaces, it should not be used for fine line requirements.

There are appropriate correction factors for the etching rates of each combination. Between conductors, patterns, thickness, and etching, solutions should be introduced for the photo masks, based on the actual trials, especially for the multiple parallel fine lines very common to high density flexible circuits. Usually, there are remarkable differences in etching factors between middle conductors and edge conductors, as shown in Fig. 63.13.

A set of dummy conductor patterns helps to minimize the difference of the etching factors.

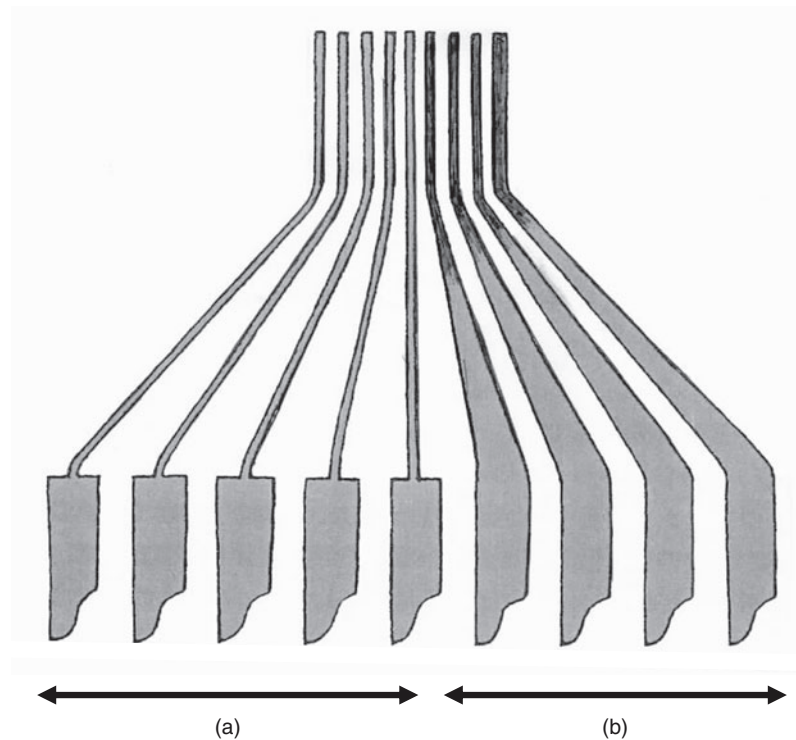


FIGURE 63.13 Pattern correction for the etching factors (a) Unacceptable (b) Preferred.

63.4 NEW PROCESSES FOR FINE TRACES

The generation of fine lines is the most basic process in building high-density flexible circuits. Three basic manufacturing concepts have been developed:

1. Advanced subtractive
2. Semi-additive
3. Full-additive

These methods have many variations to cover different construction concepts and specifications.

Innovative technologies have been developed for each unit process, such as the collimated light source exposure machine and the laser direct imaging system.

63.4.1 Advanced Subtractive Process

The subtractive (etching) process is the most common technology for generating copper-based circuitry on flexible film substrates. It is basically the same method used for rigid boards, but there are several differences in the process. An example is that it may be automated for use with a roll-to-roll process.

Subtractive technology with traditional equipment and materials cannot produce high-density traces with pitches smaller than 150 μm . However, many new technologies have been introduced for each key item, as shown in Table 63.6. The most advanced subtractive process with adhesiveless laminates can generate 30- μm -pitch traces on 9- μm copper foil for the single-side circuits using roll-to-roll manufacturing systems. A 50 micron pitch trace circuit is shown in Fig. 63.14 .

TABLE 63.6 New Technologies Needed to Generate Fine-Line Traces on Flexible Substrates

Processes	New technologies
Surface treatment	New soft etching chemicals (organic) Sputtering of seed layer
Resist coating	High-resolution liquid etching resist and plating resist (spray coater, dipping coater, etc.) Thin dry film ($\sim 15 \mu\text{m}$) High-sensitivity dry film with high resolution ($10 \text{ mJ}/\text{cm}^2$) Wet laminator
Exposure	Collimated light source with glass mask ($\sim 15\text{-}\mu\text{m}$ line/space) Autoalignment system for double-sided circuits (with accurate dimension compensation system, $\sim 5 \mu\text{m}$) Roll-to-roll conveyor system with low tension Laser direct imaging system ($30\text{--}40 \mu\text{m}$ line/space)
Etching	High-resolution etchant (cupric chloride, ferric chloride)

It is possible to produce 20- μm -pitch traces by subtractive process (as shown in Fig. 63.15), but the process will have relatively low yields.. The advanced subtractive process can produce 60- μm -pitch traces on double-sided flexible circuits with thin copper foil plated to 20- μm -thick.

Processes New technologies Surface treatment New soft etching chemicals (organic) Sputtering of seed layer Resist coating High-resolution liquid etching resist and plating resist (spray coater, dipping coater, etc.)

Thin dry film ($\sim 15 \mu\text{m}$) High-sensitivity dry film with high resolution ($10 \text{ mJ}/\text{cm}^2$) Wet laminator Exposure Collimated light source with glass mask ($\sim 15\text{-}\mu\text{m}$ line/space) Autoalignment system for double-sided circuits (with accurate dimension compensation system, $\sim 5 \mu\text{m}$) Roll-to-roll conveyor system with low tension Laser direct imaging system ($30\text{--}40 \mu\text{m}$ line/space) Etching High-resolution etchant (cupric chloride, ferric chloride)

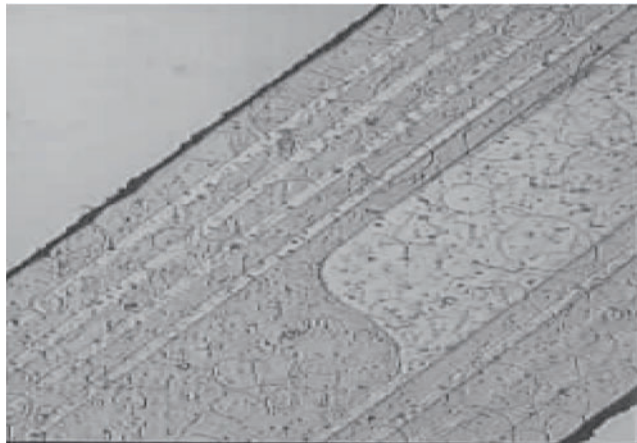


FIGURE 63.14 Fifty micron pitch trace produced by advanced subtractive process. (*DKN Research.*)

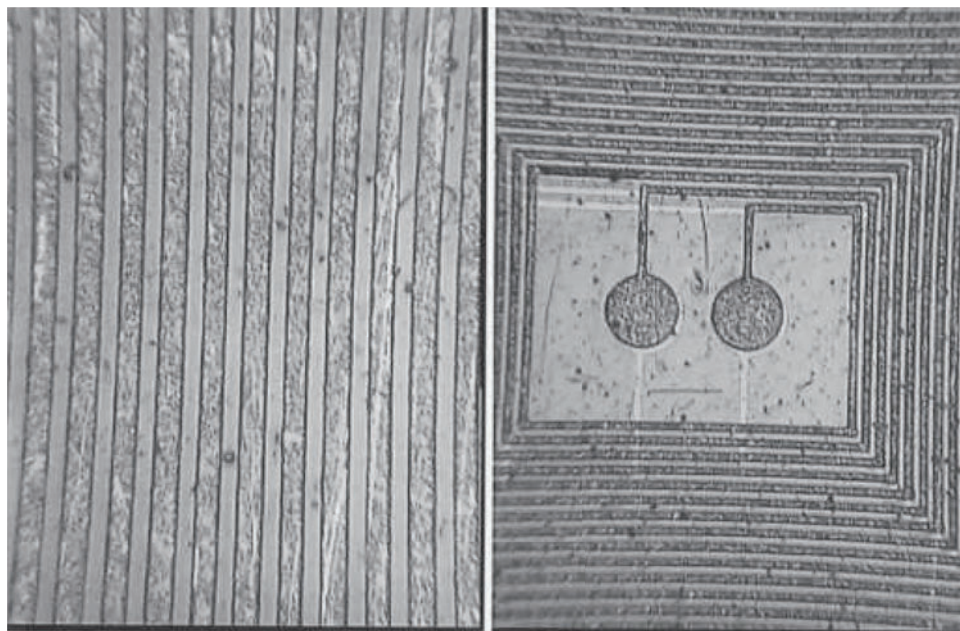


FIGURE 63.15 Twenty micron pitch traces made by advanced subtractive process. (*DKN Research.*)

63.4.2 Semi-Additive Processes

The first candidate to produce fine traces instead of subtractive process could be the semi-additive process. Several kinds of semi-additive processes—including thin copper laminates and sputtering—were developed to generate fine-line traces on specific polyimide substrate materials. An advantage of these processes is that the conductor layers can have

varying thicknesses. Both processes create suitable electroless plating processes to achieve reliable bond strength on the substrates.

The first idea of the semi-additive process is that the chemical and electrical deposition makes the copper layers after the drilling on the plain base film followed by traditional imaging and etching process as illustrated in Fig. 63.16.

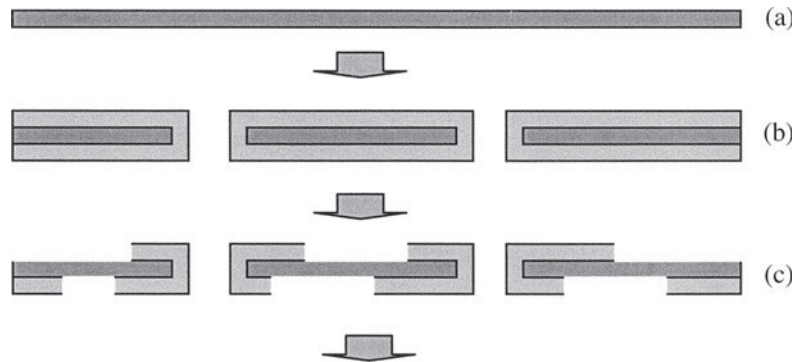


FIGURE 63.16 Basic high density circuit generation process flow for semi-additive method, (a) Plain film substrate, (b) Drilling via holes and plating of copper layers, (c) Etching of copper layer.

The thin copper laminate process does not need special technology such as sputtering, therefore it is relatively easy to design the manufacturing process. Figure 63.17 illustrates a typical manufacturing process for the double-side circuits.

1. It starts from double-side laminates with very thin copper layers.
2. The first step is drilling to form the via holes. Most of the drilling technologies are available to generate the small holes. Mechanical process including micro punching works for larger holes than 60 microns diameters. Chemical etching and plasma etching could be the low cost solutions for the high hole counts designs. But they need supplemental photolithography and copper etching process. Excimer laser and UV YAG laser are capable to generate smaller holes than 50 micron diameters for both through holes and blind via holes.
3. Copper layers are plated on the whole surface to build the conductive layer in the via holes, by both electroless and electrolytic processes, using, standard copper plating process. It is important that the processes are controlled well enough to make the thin copper layers with uniform thickness.
4. A negative pattern of conductor traces for the plating resist is formed on the copper surface by a high-resolution photolithography process.
5. Further electro plating is conducted to build the required copper thickness. The plating conditions should be well controlled to have a uniform thickness for whole circuits. A smaller panel size is recommended for an easy control of the plating conditions.
6. The plating resist is removed by standard stripping process.
7. As the final process, the seed layers between the conductor traces are removed by appropriate etching process. A supplemental metal plating is conducted as the protection layer for the process, prior to the stripping process of the plating resist.

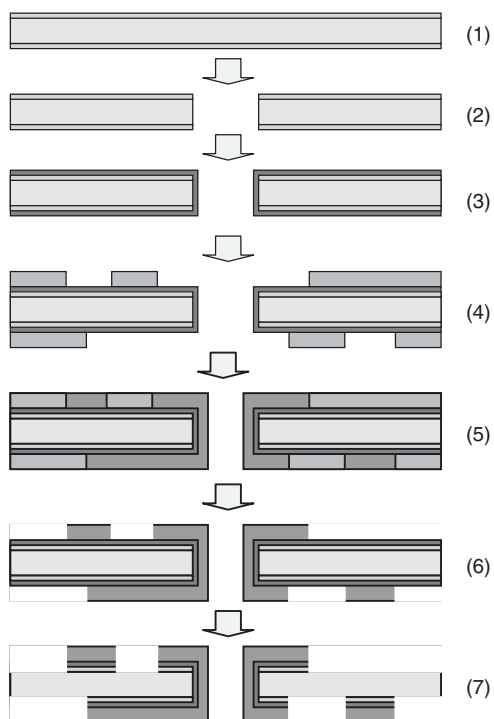


FIGURE 63.17 Semi-additive process with thin copper laminates.

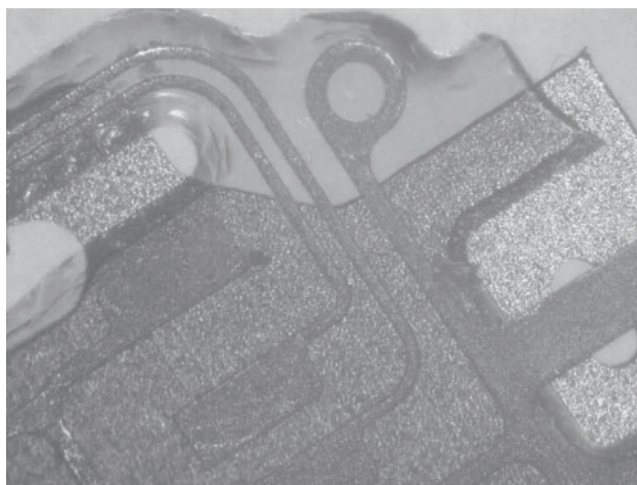


FIGURE 63.18 Twenty micron traces on double sided flexible circuits made by semi-additive process.

Figure 63.18 and Fig. 63.19 show examples made by the semi-additive process. The sputtering process has been developed to have thin seed layer for the semi-additive process with finer trace densities as shown in Fig. 63.20.

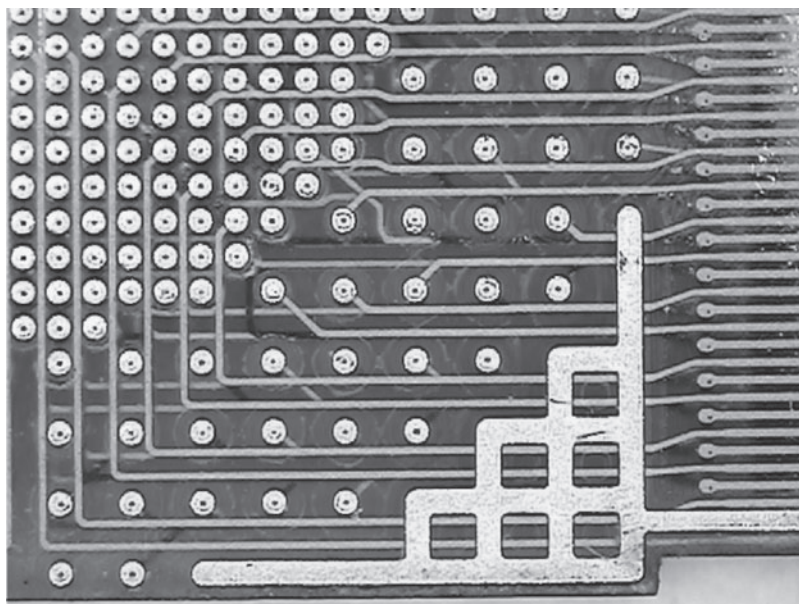


FIGURE 63.19 Fifteen micron traces with 20 micron holes for 10 layer circuits. (Source: MicroCommex.)

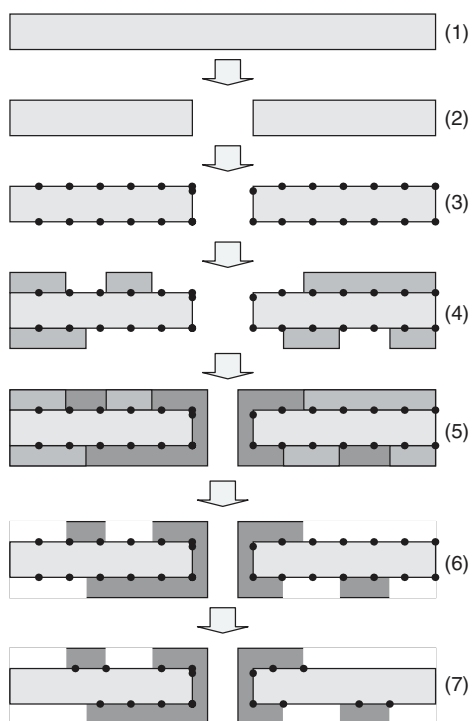


FIGURE 63.20 Semi-additive process with sputtering.

1. Because it's a plain plastic film, polyimide film is typically the starting material for the manufacturing process.
2. The small size holes are generated by mechanical processes or laser process. It needs supplemental photolithography process to use chemical etching and plasma etching for this process.
3. A set of sputtering processes is employed to form the electrically conductive thin seed layer, typically thinner than one micron. To have a reliable bond strength between organic layers and conductors, appropriate conditioning including surface treatment should be conducted.

The following processes are used for plating resist formation:

- Electro-forming of the copper conductors
- Stripping of the plating resist
- Etching of the seed layers
- A process that is basically the same as the previous semi-additive process, but is able to provide finer pitches with higher aspect ratios because of extremely thin seed layers. An optimized condition of the process can produce smaller than 5 micron pitches and larger aspect ratios than 1:5.

Figure 63.21 shows two examples of fine trace produced by sputtering/electro-forming process.

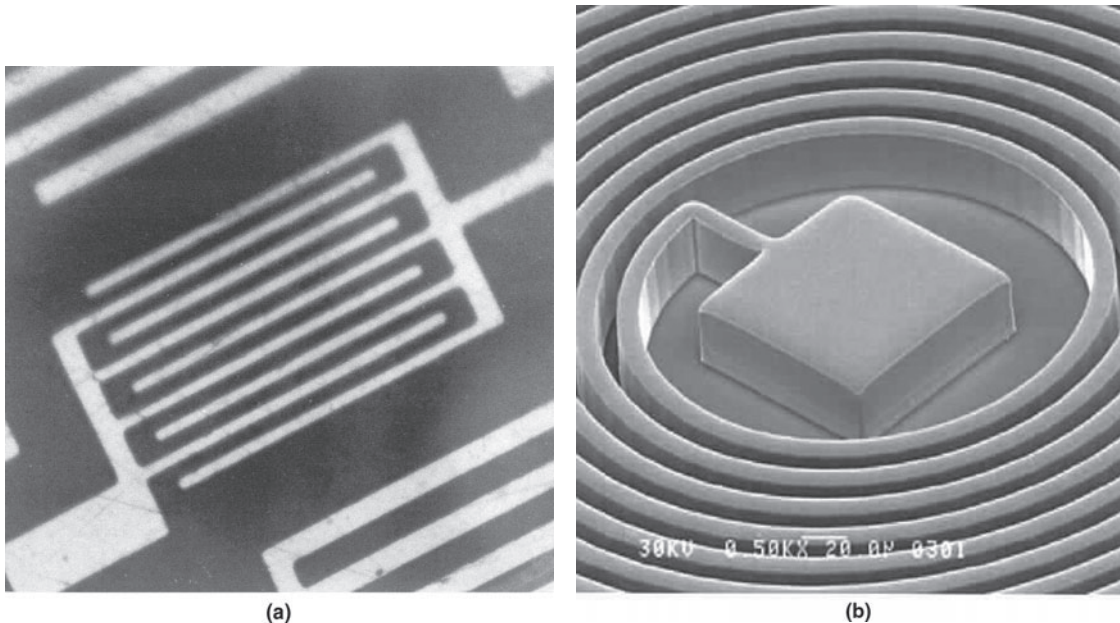


FIGURE 63.21 Ultra thin patterns made by semi-additive process with sputtering, (a) Ten micron pitch traces with one micron thick trace, (b) Ten micron wide traces with 25 micron thick traces. (Dynamic Research.)

A combination of the semi-additive process with a casting technology of the polyimide resin provides a capability to build multi-layer constructions with ultra fine traces and micro via holes. But the layer constructions and the manufacturing process could be very different from the traditional flex circuits. The manufacturing process starts from the preparation of the base layer. A commercialized polyimide film is available as the starting material for the process.

A casting of the liquid polyimide on a suitable carrier plate is another choice to have a thinner base layer than 12 microns. A glass or a stainless steel plate is recommended to use to manage the dimensions stable.

1. A seed layer is formed on the base layer by a series of sputtering processes.
2. A negative pattern of conductor traces is formed with plating resist by a high resolution photolithography process. The selection of the photo resist could be the key of the technology. A spin coating of the liquid photo resist is recommended for the high resolution.
3. An electrical forming of copper or other suitable metals is conducted to generate the fine conductor traces with necessary aspect ratios.
4. A set of process for stripping and etching of the seed layer between conductor traces is conducted to have isolated circuits. A gold plating on the conductors prior to the stripping process is recommended for the chemical protection of the traces.
5. A polyimide resin is coated on the circuits as the insulation layer for the next conductor layer. A photo-sensitive polyimide resin is recommended to coat to generate via holes by photolithography process. A combination of non-photo sensitive polyimide and Excimer laser is another choice. It has a flexible capability to form reliable insulation layers. But its productivity is low and processing cost per unit area is relatively high.
6. The second seed layer is formed by the same sputtering process as shown previously in process 2. A difference is that the thin seed layer have to cover the different surfaces in the via holes.
7. The same processes of photolithography of plating resist, electro forming of the conductors, stripping of the resist and etching of seed layer are conducted to build the second conductor layer.

An example of the processes is illustrated in Fig. 63.22.

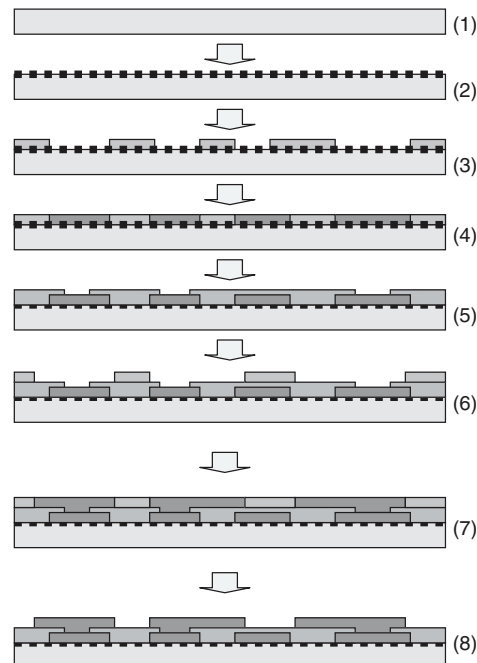


FIGURE 63.22 Semi-additive process with polyimide (PI) casting.

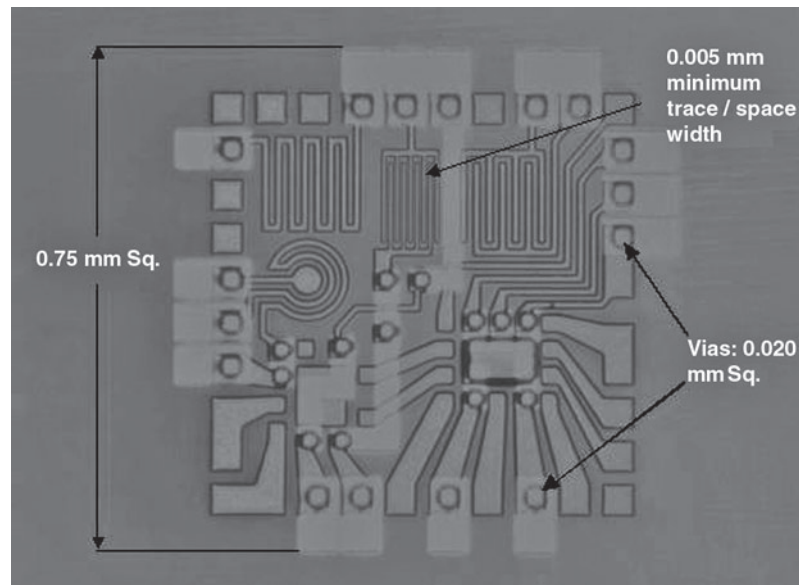


FIGURE 63.23 Ten micron pitch with 20 micron diameter via holes on the three layer flexible circuits made by semi-additive process with casting. (Source: Dynamic Reaserch.)

The same processes can be repeated to form more conductor layers. Figure 63.23 shows an example of ultra high density multi-layer flexible circuits with 10 micron pitch and 20 micron diameter via holes.

63.4.3 Fully Additive Processes

Several full-additive processes that can produce extremely fine traces on flexible substrate materials have been developed.

Several combinations of chemical deposition process of the conductor materials and photo-sensitive resists have been tried. Unfortunately, there is no good combination that satisfies the needs for both high-resolutions and physical performances. Further improvement is required to have practical high density flexible circuits.

Screen-printing has had a remarkable progress to generate fine resolutions. An appropriate combination of the screen printer and screen mask can provide smaller pitch traces than 20 microns as shown in Fig. 63.24. It could be the low cost solution for the volume production for the high density flexible circuits. The process is capable for both conductor materials and insulation materials. A screen printable conductive material could be the key of the process.

63.4.4 Process Comparison

A comparison of the fine line generation technologies is shown in Fig. 63.25. The advanced subtractive process can provide the best cost-performance solution when building a high-density circuit at pitches larger than 30 μm for single-side circuits and 50 μm for double-side circuits. The process does not need very different technologies from the traditional etching process, therefore the technical hurdles are relatively low and it minimizes the investment for the manufacturing equipment.