High and Low Dielectric Constant Materials

by R. Singh and R. K. Ulrich

Silicon-based dielectrics (SiO_2, Si_3N_4, SiO_xN_y etc.) have been widely used as the key dielectrics in the manufacturing of silicon integrated circuits (ICs) and virtually all other semiconductor devices. Dielectrics having a value of dielectric constant k x 8.854 F/cm more than that of silicon nitride (k > 7) are classified as high dielectric constant materials, while those with a value of k less than the dielectric constant of silicon dioxide (k < 3.9) are classified as the low dielectric constant materials. The minimum value of (k) is one for air. The highest value of k has been reported for relaxor ferroelectric (k = 24,700 at 1 kHz).[1] In this paper, we present several important applications of both high- and low-k dielectrics in microelectronics, optoelectronics and cryoelectronics. Special emphasis has been placed on emerging applications of high- and low-k dielectrics that can avoid physical limits imposed by silicon-based dielectrics.[2] An example of such an application is the use of high-k dielectrics as the gate dielectric material for the fabrication of sub-100 nm metal-oxide-silicon (MOS) Si ICs as well as organic transistors fabricated on plastic. Realizing the importance of high- and low-k dielectrics, an ECS Symposium Series (International Symposium on Low and High Dielecric Constant Materials: Materials Science, Processing and Reliability Issues) was started in 1996 and appeared as the Fourth Symposium in the Spring 1999 ECS meeting. The high-k dielectrics are discussed first, followed by low-k dielectrics. Manufacturing and processing issues, including low temperature processing, high throughput, low defects and low thermal and residual stress etc., are presented next followed by some concluding remarks.

High Dielectric Constant Materials

As shown in Table I, a large variety of materials have been used for a number of applications. High-k dielectric materials have recently become important mainly in three areas: memory cell dielectrics, gate dielectrics, and passive components.

Memory chips use the presence or absence of charge in a capacitor to represent a "1" or "0". For a modern-day 64M DRAM, fitting 64 million capacitors (along with 64 million accompanying transistors and associated housekeeping circuitry) onto about 1 cm^2 of Si requires that each capacitor occupy no more than a few tenths of a square μm. The situation will get even more crowded as IC density trends continue. The number of components per chip has grown at an exponential rate for almost 40 years, doubling about every 18 months. This observation, known as Moore's law, is not only the record of a remarkable rate and duration of growth but is also a self-fulfilling prophecy. The microelectronics industry is aware of how long this trend has been valid and believes that it will continue for a decade or more. Therefore, the industry is aggressively developing a variety of technologies necessary to stay on this curve.

The area of individual capacitors on DRAMs is shrinking rapidly while, at the same time, operating voltages are falling from 5 V a few years ago to around 3 V today and, maybe, about a volt in couple of years. However, charge storage requirements for each memory cell are not relaxing at a significant rate remaining at about 30 fF/cell. Until recently the approach to this problem has been to employ thinner layers of traditional silicon dioxide and silicon nitride dielectrics. But, as memory chips surpass about 64 Mb, this approach is no longer adequate because, to achieve the required cell capacitance, these materials must become so thin (less than 1 nm), that they would suffer from unacceptable levels of leakage current or would suffer catastrophic breakdown even with the reduced operating voltage

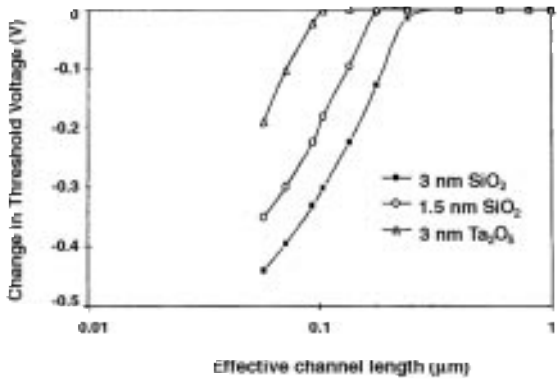


FIG. 1. Effect of decreasing channel length on threshold voltage variation.

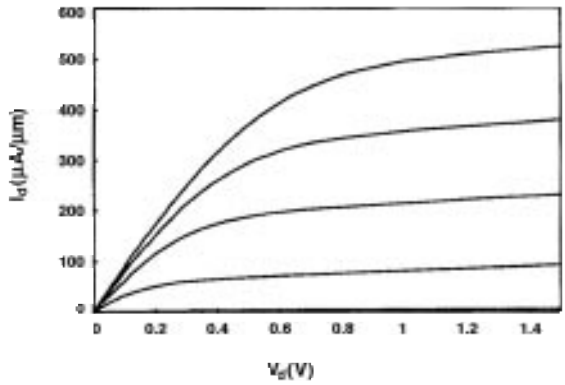


FIG. 2. I_d-V_d characteristics of a 4.0 nm equivalent SiO_2 thickness Ta_2O_5 for 0.15 μm MOS transistors @V_{dd} = 1.5V (© 1998 IEEE. Reprinted with permission, IEEE/SEMI Advanced Semiconductor Manufacturing Conference, *Boston, MA, 434, 1988).*

Technoprobe Exhibit 2010, Page 1 of 5
FormFactor v. Technoprobe - IPR2024-00933

of modern-day chips. Clearly, if one looks at the capacitor equation, the only factor left to adjust is the dielectric constant. Then the solution is to develop higher-k materials to enable the capacitor dielectric to maintain a robust thickness while still providing sufficient charge storage with a continuously shrinking area and storage voltage.

Depending on their composition and morphology, SiO_2 and Si_3N_4 have dielectric constants between about 4 and 7. Looking at the list of candidate materials shows that Al_2O_3, (k = 9) is not an improvement but Ta_2O_5 (k = 25) can meet the requirement for the next generation of DRAMs. Certainly, the industry has had long-term experience with Ta_2O_5 and it can be deposited in a variety of ways including chemical vapor deposition (CVD), metalorganic chemical vapor deposition (MOCVD), sputtering and anodization. In very thin film form, less than a nm, anodization provides higher yields because it is insensitive to the roughness of the underlying base plate. When a thin dielectric film is deposited by chemical or physical deposition methods, any peaks or valleys in the underlying metal which are about the same vertical size as the dielectric's final thickness can result in a point of excessive leakage or even a short. But, with anodization, an excess of metal such as Ta, can be deposited and converted to oxide to provide the needed dielectric. This requires a carefully controlled electrochemical process to achieve just the right amount of capacitance.

However, Ta_2O_5 does not provide enough of an improvement in dielectric constant for memory generations of 1 Gb or above, expected in a year or so. The long-term solution seems to lie in the various ferroelectric or near-ferroelectric materials such as various combinations of barium and strontium with titanate (BST), lead magnesium niobate (PMN), and other perovskite metal oxides. These types of materials can exhibit dielectric constants from a few hundred to several thousand enabling them, in principle, to provide sufficient capacitance for DRAMS into the foreseeable future. These materials can be deposited using almost any method by which a thin film can be formed and come in a wide variety of compositions and morphologies. The dielectric constants tend to be a strong function of the specific elemental ratios and crystal structures which, in turn, are a function of the deposition method. The selection of a particular dielectric material and the design of the DRAM cell depend on a number of complex factors, including the process simplification leading to cost-reduction.

As a memory cell dielectric, the application of high-k dielectrics in the fabrication of non-volatile ferroelectric random access memory (FeRAM) is an emerging area. Ferroelectric dielectrics such as lead zirconium titanate (PZT) or strontium bismuth tantalate (SBT) have a perovskite structure and are unique in that their crystal structure maintains its "memory" without power. The capacitor structure in FeRAMs controls read/write, speeds, data storage lifetime, device layout, and packing density. The early FeRAM device (manufactured by Ramtron Corp.) is being used in game cartridges, where memory is maintained without the use of a battery.[3]

Both for DRAMs and FeRAMs, the interfacial reaction and thermal stability of the electrodes in capacitor and developing plasma etching processes that provide critical dimensions of the devices are challenging problems. Polysilicon as an electrode material has the problem of forming a silicon oxide layer at the poly-Si/high k- interface. A number of other electrode materials including, Al, Ir, Pt, Ru., TaN, TiN and W are being considered for the manufacturing of cell capacitors for DRAMs and FeRAMs. Each electrode material has unique processing problems. As an example, Pt has adhesion and etch residue problems while Ru forms RuO_4 as toxic by-product and is also susceptible to pinholes and notching because of its ease of oxidation.[3]

From the MOS transistor performance point of view, the thickness of silicon-based dielectrics as the gate dielectric material poses a fundamental limitation. As discussed in a companion article in this issue, for oxides less than about 2 nm, significant direct tunneling currents start to flow. In order to overcome the fundamental limitations of SiO_2 as the gate dielectric, as early as 1980, one of the authors proposed the use of high-k dielectrics as the gate dielectric material.[4] Figure 1 shows the influence of thickness and dielectric constant on the threshold voltage of a MOSFET at submicron channel lengths. As can be seen from Fig. 1, the use of high-k dielectric provides less variation in threshold voltage. Similar consideration of sub-threshold swing values shows that a value of 50 mV/decade (highly desirable for optimum performance of the circuit) can be obtained for high-k gate dielectric materials. For any given generation of Si MOSFETs, there is an optimum gate dielectric capacitance value. This optimum value of the capacitance is dependent on the supply voltage, oxide thickness and other parameters specific to the fabrication process. It has been shown[5] that for a dielectric thickness of 5 nm, the optimum dielectric constant is 25 which corresponds to the k-value of Ta_2O_5. For MOSFETs, there is thus a certain dielectric constant for a given dielectric thickness for which the circuit performance is optimum.

In the context of high-k dielectrics and silicon-dielectric interface, there are two extreme cases. In one case epitaxial dielectrics (e.g., II-A fluorides) can provide the required clean interface. In the other case, an ultrathin layer of Si based dielectric (generally SiO_x) can provide the required clean interface. The second approach is currently being investigated vigorously by researchers throughout the world. The development of high-k gate dielectric material is a relatively new approach; the initial, results however, are promising. Using thermal CVD

TABLE I. Important High-k Dielectric Materials

	Dielectric Constant	Application
$PbMgNbO_3$+$PbTiO_3$	22,600	B
$PbLaZrTiO_3$	1000	B
$BaSrTiO_3$	300	B
TiO_2	50	A,C
Ta_2O_5	25	A, B
CeO_2	20	A
$BaZrTiO_3$	17.3	E
Al_2O_3	9	B
$(Bz,Ca,Sr)F_2$	7.3	D

A: Gate dielectrics B: Capacitor dielectrics C: Photoelectrochemical cells
D: Epitaxial dielectrics E: Gate dielectrics for organic transistors on plastic

Technoprobe Exhibit 2010, Page 2 of 5
FormFactor v. Technoprobe - IPR2024-00933

for the deposition of Ta_2O_5, a feasibility study was performed[6] on the incorporation of Ta_2O_5 as the gate dielectric in a sub-180 nm CMOS process. Figure 2 shows the transistor current-voltage characteristics of 150 nm MOS transistors using 4.0 nm equivalent thickness of Ta_2O_5.[6] We have shown,[7] that the leakage current density of PLZT films deposited directly on Si by rapid phothermal processing assisted MOCVD (in-situ cleaning, and deposition followed by in-situ annealing), is lower than reported for any non-silicon-based inorganic dielectric. Similarly, the use of high energy photons, in cleaning, deposition and annealing low-temperature deposited diectrics, gives improved performance and reliability.[7]

Another interesting application of high-k gate dielectric is in the fabrication of low-cost field-effect transistors using organic (e.g., pentacene) semiconductor as the starting semiconductor deposited on plastic substrates.[8] Recently, researchers at IBM have used room temperature deposited barium zirconate (k = 17.3) as the gate dielectric material in place of SiO_2. As shown in Fig. 3, the source-drain current of transistors based on high-k as the gate dielectric material can be changed by five orders of magnitude by a gate voltage change of just a few volts. In case of SiO_2 based transistors, few hundred volts were required to get the same change in the source-drain current. These results are very promising for the practical realization of all-plastic based display systems.

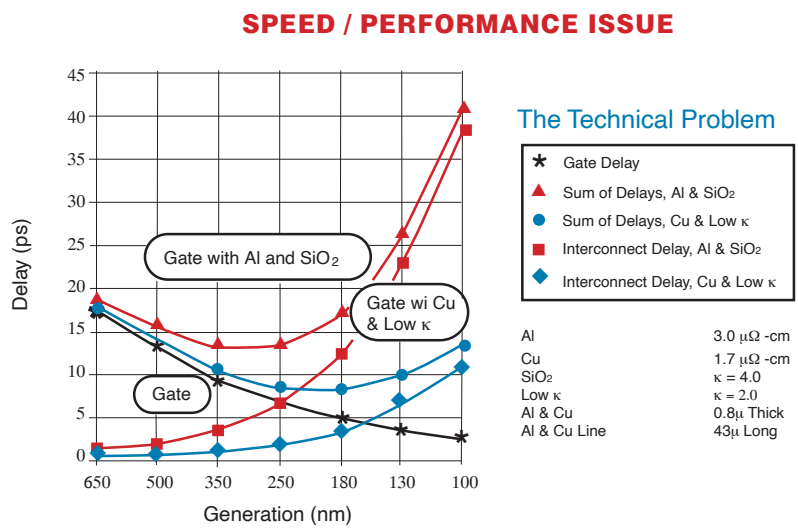
In the area of passive components, high-k materials are finding increased application in capacitors for decoupling, timing, filtering, and many other functions. Passive components, including capacitors, usually outnumber active components in almost any consumer or industrial application and occupy a significant fraction of circuit board space. This is particularly true in rapidly growing applications such as cell phones, global positioning systems, receivers, and other wireless devices. Therefore, there is a strong desire to place capacitors in the circuit board in the form of integrated passive components thus freeing up more real estate for ICs. Therefore, almost every microelectronics manufacturer and research center now has a program on depositing and processing thin high-k films in between layers of flex, ceramic or as build-up

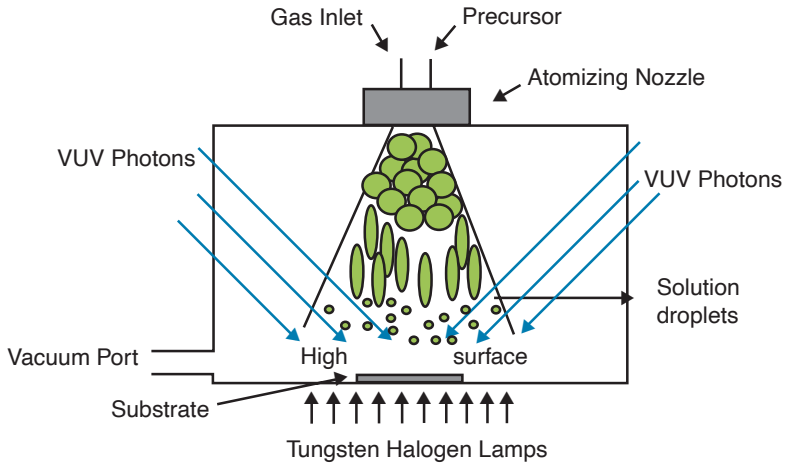
FIG. 3. (right) Plot of I_D versus V_D at various V_G from an organic IGFET on polycarbonate (Reprinted with permission from Science, *Volume 283, Paper 824 (1999) American Association for the Advancement of Science).*

FIG. 4. (center) Calculated gate and interconnect delay versus technology generation (Reprinted with permission of the Semiconductor Industry Association. The National Technology Roadmap for Semiconductors: Technology Needs, *1997 edition. Austin: SEMATECH (1997).)*

FIG. 5. (bottom) Direct liquid injection and rapid photothermal chemical vapor deposition system. (Reprinted with permission from the American Institute of Physics, *68, 3, (1997).)*

Due to copyright restrictions, we are unable to reproduce this figure online.





Technoprobe Exhibit 2010, Page 3 of 5
FormFactor v. Technoprobe - IPR2024-00933

on silicon. As in the case of high-k materials for DRAMs, the film deposition methods include just about every method that there is including sputtering, anodization, CVD, spin-on, and thick-film deposition techniques.

For example, decoupling capacitors are mounted on the circuit board near just about any active device with fast edge rates in order to provide low-impedance power during the short periods of high current demand. When the clock cycles, there may be millions of gates changing states at once. This demands so much current that, without a nearby capacitor between power and ground, the local voltage could be forced to sag to the point that false triggering would occur. The decoupling capacitor can be viewed as a small, fast-response battery. Discrete decoupling capacitors are mounted on almost any board that has an IC chip and they are even finding their way into the chip packages themselves. Integrating these into the layers of the circuit board would not only free up more space for higher chip density but would have the added effect of performing better. Integrated capacitors exhibit much less lead inductance, which, in turn, gives them a higher operating frequency. Finally, an integrated capacitor does not have solder joints that will break.

These are the promises of integrated high-k materials but there are many challenges between here and there. What materials will be used and how will they be processed? Certainly, the same high-k materials making their way into DRAMs are candidates, but integrated capacitors will probably lag DRAM dielectric technology by at least several years. Right now alumina and some tantalum oxides are finding their way into high-performance multiple chip modules (MCM) assemblies and will eventually trickle down into consumer products as the demands for higher functionality per volume increases.

Low Dielectric Constant Materials

As stated before, any dielectric material with a k value less than the conventionally used SiO_2 (k = 3.9) is termed as a low dielectric constant material. The communication revolution (microsystems operating at 1 V) and the technological thrust toward portable, high circuit density, and low power electronic microsystems, have necessitated the use of low-k dielectrics as the interlevel dielectric (ILD) material. As shown in Fig. 4,[9] only the use of Cu as a conductor and low-k dielectric as the dielectric material can provide the lower delay time required for advanced circuits. It is worth mentioning here that from the interconnection performance point of view, the use of low-k dielectric material in place of currently used dielectric (SiO_2) has more to offer than what replacement of copper as a conductor can deliver. Table II shows the list of a number of low-k dielectric materials that are currently being investigated for interconnect applications.

The term, "interlevel dielectric (ILD)" is commonly used for the dielectric isolation both between layers and within an individual layer of conducting lines. The dielectric within an individual layer is sometimes known as the "gap-fill." Some researchers use the term "intermetal dielectric (IMD)" to signify the insulator between and within metal lines, using ILD to signify the insulator associated with polysilicon conducting lines. Thus, IMD is a subset of ILD.

The use of Si-O-F based low-k dielectric materials for interconnect application has been a relatively straightforward issue. However, this is not the case for polymer-based low-k-dielectrics or other low-k inorganic dielectrics. The main problem is that currently available low-k dielectrics cannot withstand the high processing temperature inherent is currently used metal deposition techniques. Thus, from a process integration point of view, two different approaches are being explored. In one case, new materials are being invented that can allow the use of high processing temperatures. In another approach, the temperature of metal and low-k dielectric processing is reduced to accommodate the currently available low-k dielectrics. Another important issue in low-k dielectrics is that the thermal conductivity of organic polymers is much lower than the thermal conductivity of SiO_2. The thermal conductivity of SiO_2 is about 1.2 W/K.m. On the other hand, the thermal conductivity of typical polymers is about 0.24-0.37 W/K.m. The low thermal conductivity is highly undesirable, since high-speed circuits generate heat that must be dissipated.

Spin coating followed by furnace annealing and chemical vapor deposition are the two most common deposition techniques used for processing low-k dielectrics. For the processing of low-k dielectrics, we have stressed the importance of reduction of processing temperature and processing time.[10] The use of fast heating and cooling rates in rapid thermal processing reduces the processing time. For obtaining optimum performance of the low-k dielectrics, both heating and cooling rates of the thermal cycle need to be optimized. Due to lower microscopic defects, the use of rapid photothermal processing of dielectrics provides the best performance and the reliability.[7] As compared to spin-on coated films, the performance of CVD deposited films is better. This is due to the fact that CVD provides better control of microstructure than is possible

Table II. Various Low-k Dielectric Materials

Dielectric	Value of k (@ 1 MHz)
$SiO_x F_y$	3.2 - 3.5
Hydrogen silsesquioxane	3.0
Polysiloxane	2.89
Fluropolyimide	2.8
Benzo-cyclo-butane	2.7
Black diamond	2.7
Polyethylene	2.4
Polypropylene	2.3
Fluoropolymer	2.24
Perylene	2.2
Dupont PTFE-based copolymer AF 2400	2.06
Xerogels	1.2
Air	1.0
Carbon dioxide	1.0

Technoprobe Exhibit 2010, Page 4 of 5
FormFactor v. Technoprobe - IPR2024-00933

with spin-on coated films. However, the cost of conventional CVD films is higher than the cost of spin-coated films. For low-k dielectrics, we have developed a low-cost direct liquid injection (DLI) assisted rapid photothermal chemical vapor deposition (RPCVD) system.[11] Figure 5 shows the schematic diagram of such a system.

Due to the low thermal conductivity problem of organic dielectrics, it is possible that initially low-k materials will be introduced as an embedded material. Texas Instruments has demonstrated the viability of low-k materials with Cu. It is possible that in future Cu plugs, Cu conductor, combined with low-k dielectrics can eventually be used in the manufacturing. Air gaps as well as carbon dioxide have also been studied as potential low-k dielectrics.[12,13] However, due to the low thermal conductivity of air, it is highly unlikely that air or other gases will find practical applications.

In addition to the fundamental problems of low thermal conductivity and optical anisotropy, a major concern of non-uniformity in microstructure also exists for porous materials. Thus for a fully integrated Cu and low-k interconnect system, we expect the possibility of new failure modes. In place of currently used DC reliability tests, AC reliability tests will become very important.

Manufacturing Considerations

With shrinking dimensions and increased aspect ratios, new defect classes will limit the yield of new generations of semiconductor products involving high- and low-k dielectrics. Due to new processes and new materials, the defect complexity will also increase. Atomic roughness of the interfaces will play a critical role in determining the defect type and distributions. The traditional concept of a defect (defects largely tied to particle contamination) may not be sufficient to predict the actual yield of a product.[14] In addition to macroscopic defects, microscopic defects, and their role in leading to the development of macroscopic defects may be a major issue. Due to small dimensions, the edge definition of an etching step which, in current technology is an acceptable variance, may itself be a defect issue. Microstructural homogeneity is the most important parameter that improves performance and reliability for all materials. In light of discussion of defect and structural properties, the absence of microstructural homogeneity in a region results in increase of stress. Stress in the film after a processing step is directly related to the number of defects present in the film.

Scaling devices to accommodate shrinking linewidths is driving a trend toward thinner layers (< 200 nm) and more stacks to engineer the electrical and mechanical properties and speed the fabrication process. The layering of thin films, both metal and dielectrics, provides the flexibility to balance and optimize numerous parameters such as stresses, adhesion, conductivity, and diffusivity. Precise control over deposition processes, patterning, etching, and chemical mechanical polishing (CMP), is critical for meeting desired performance levels and yield.

Conclusion

In this paper, we have presented the current status and future directions in the materials and processing of high- and low-k dielectrics. The results presented in this paper show that reduction of thermal stress of the dielectric film, homogenous microstructure, and reduction of interface roughness are the most important requirements for a particular processes to be acceptable for manufacturing.

Acknowledgement

The authors acknowledge the help of Dr. Vijay Parihar in the preparation of this manuscript. ■

References

1. R. Kyoung, K. Sojin and J. H. Koo, *J. Am. Ceram. Soc.*, 81, 2998 (1998).
2. R. Singh, *Microelectronics Reliability*, 38, 1471 (1998).
3. S. P. DeOrnellas and A. Cofer, *Solid State Technology*, 41, 53 (1998).
4. R. Singh and K. Rajkanan, *J. Vac. Sci. Technol.*, 17, 376 (1980).
5. H. Shimada, and T. Ohmi, *IEEE Trans. Electron. Devices*, 43, 431 (1996).
6. T. Devoivre, C. Papadas, M. Setton, N. Sandler, L. Vallier, and I. Bouras, *Proc. 1998 IEEE/SEMI Advanced Semiconductor Manufacturing Conf.*, p. 434 (1988).
7. R. Singh, S. V. Nimmagadda, V. Parihar, Y. Chen, and K. F. Poole, *IEEE Trans. Electron. Devices*, 45, 643 (1998).
8. C. D. Dimtrakopoulos, S. Purushothaman, J. Kymissis, A. Callegari, and J. M. Shaw, *Science*, 283, 822 (1999).
9. *The National Technology Roadmap for Semiconductors*, Semiconductor Industry Association, p. 11, 1997.
10. M. A. Wait, J. Mavoori, R. Singh, J. E. Harriss, K. F. Poole, J. W. Kolis, R. P. S.Thakur, and A. A. Ogale, *Appl. Phys. Lett.*, 64, 3264 (1994).
11. R. Sharangpani and R. Singh, *Rev. Sci. Instruments*, 68, 1564 (1997).
12. B. Shieh, K. Saraswat, M. Deal, and J. McVittie, *Solid State Technology*, 42 (2), 51 (1999).
13. P. Singer, *Semiconductor International*, 22 (3), 38 (1999).
14. R. Singh, V. Parihar, K. F. Poole, and K. Rajkanan, *Semiconductor Fabtech.*, 9, 223 (1999).

About the Authors

Rajendra Singh *is D. Houser Banks Professor in the Holcombe Department of Electrical and Computer Engineering and Director of the Center for Silicon Nanoelectronics at Clemson University in Clemson, SC. He has worked in the areas of dielectrics, rapid thermal processing, solar cells and semiconductor manufacturing. In 1998, Dr. Singh was awarded the Thomas D. Callinan Award of the Dielectric Science and Technology Division of The Electrochemical Society.*

Richard K. Ulrich *is a Professor of Chemical Engineering at the University of Arkansas and a founding member of the High Density Electronics Center. His primary research interest is in the area of high dielectric constant materials for various electronic applications.*

Technoprobe Exhibit 2010, Page 5 of 5
FormFactor v. Technoprobe - IPR2024-00933