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P R E M I E R I S S U E

HIGH-SPEED DESIGN



Designing a PCB Stackup, Part 1



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SPEEDING EDGE

SUMMARY: *The challenge in designing a PCB stackup is to satisfy its many demands. Information in this document is drawn from experience gained designing more than 2,000 PCB stackups for products as simple as video games and as complex as the highest-performance backplanes used in supercomputers and routers.*

The practice that has worked in the past of allowing the fabricator to design a PCB stackup no longer works. Speeds have increased to the point where signal integrity and power delivery considerations make it necessary to employ far

more discipline in the choice of materials and arrangement of the layers in the stackup – both of which are outside the skill set of virtually all PCB fabricators. A common part of the vendor selection process has been to submit each design for a quote to several fabricators and make the choice based on price only. This is very often a fatal method of vendor selection because the lowest bidder often takes shortcuts in order to achieve the lowest price and/or may not possess the skills necessary to manufacture quality PCBs of the given complexity.

Among the demands placed on stackup design are:

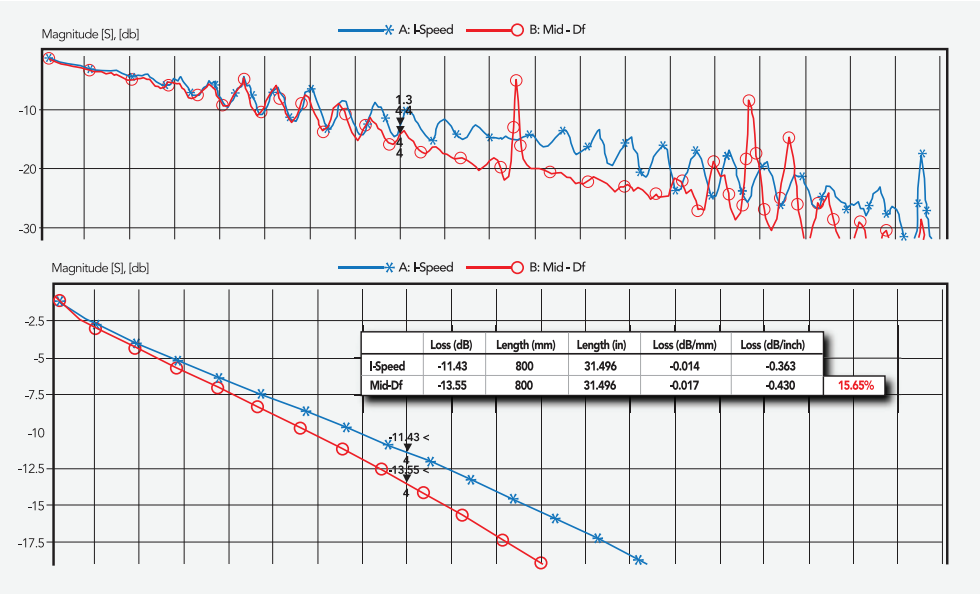
- Providing enough signal layers to allow successful routing of all signals to signal integrity rules.
- Creating copper thickness in planes and signal layers that meets the conductivity demands of signals and power and, at the same time, be reasonable to manufacture.
- Providing enough power and ground layers to meet the needs of the power delivery system.
- Specifying dimension trace widths and dielectric thicknesses that allow impedance targets to be met.
- Ensuring that the spacing between signal layers and their adjacent planes is thin enough to satisfy crosstalk needs.
- Specifying dielectric materials that are economical to manufacture and readily available.
- Avoiding the use of expensive techniques such as blind and buried vias and build up processing if possible.
- Providing for prototype manufacture in one factory or country and production manufacture in another factory or country.



The Next Generation High Speed Product from Isola

- Global Constructions available in all regions
- Optimized Constructions to improve lead free performance
- I-Speed delivers 15-20% lower insertion loss over competitive products through reduced copper roughness and dielectric loss
- Improved Z-axis CTE 2.70%
- I-Speed – IPC 4101 Rev. C /21 /24 /121 /124 /129
- Offer spread and square weave glass styles (1067, 1086, 3313, etc.) for laminates and prepregs
 - Minimizes micro-Dk effects of glass fabrics
 - Enables the glass to absorb resin better and enhances CAF capabilities
 - Improves yields at laser and mechanical drilling
- A low Df product with a low cost of ownership

Effective Loss @ 4 GHz on a 32 inch line



I-Speed delivers 15-20% lower insertion loss over competitive low Df products.

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Supplying the base for innovation

DESIGNING A PCB STACKUP, PART 1 *continues*

Information needed to design a successful PCB stackup is scattered among many documents and specifications, many of which are not in the public domain. This document is intended to bring all of the necessary information into one document to improve the design process.

How a Typical Multilayer PCB is Built

In order to understand the choices that must be made when designing a PCB stackup, it is useful to review how a typical multilayer PCB is fabricated. Figure 1 is a diagram showing the components that make up a six-layer PCB. The manufacturing method shown in the figure is referred to as foil lamination. This refers to the fact that the two outer layers begin as sheets of foil copper with no images etched into them. This is the most cost-effective way there is to manufacture a multilayer PCB and should be the objective of the stackup design process. There are other methods available, such as cap lamination, that forms the outer layers as part of a two-sided piece of laminate and build up processing that involves blind and buried vias. These choices always result in more expensive PCBs and should be considered only as a last resort.

It should be noted that PCB layers are built in pairs. Therefore, PCBs normally have an even

number of layers. As a result, when additional layers are needed they will be added one pair at a time along with an additional pre-preg layer. Designing a stackup with an odd number of layers when only one additional layer is needed does not result in a PCB that is cheaper than if a pair of layers had been added. The reason for this is that the fabricator will need to purchase a piece of laminate for the added layer that has copper foil on both sides. The copper foil that is not needed will be etched away when the necessary foil side is etched.

As can be seen from Figure 1, three main components make up a multilayer PCB. These are:

- Sheets of laminate that have a sheet of copper foil bonded to each side which have the patterns for either signal layers or plane layers etched into the copper foils. These are often referred to as details. (Laminate is a combination of woven glass cloth and a resin system such as epoxy or polyimide.) The thickness of the copper on each side of this laminate can vary from ½ ounce to 2 ounces. (Copper foil thickness is specified in ounces per square foot of surface area. 1 ounce is approximately 1.4 mil or 36 microns thick.)

- Sheets of uncured laminate called pre-preg placed between the details and between details and the outer foil sheets. This pre-preg is a woven glass material coated with the same resin system that is used in the laminates. Unlike the laminates, the resin is only partially cured. During lamination heat will cause this resin to melt and flow into the voids in the adjacent copper layers, serving as the glue to bond the layers together and then cure it to the same rigid state as the resin in the laminate. After lamination pre-preg is indistinguishable from laminate.

- Sheets of copper foil to form the outer layers. The reason the two outer layers are solid copper at this stage instead of etched with the outer layer patterns is to provide a path for the current required to plate copper into the holes drilled through the PCB for vias and component leads. The task of the stackup designer is to select combinations of pre-preg, laminate and foils that provide the desired electrical charac-

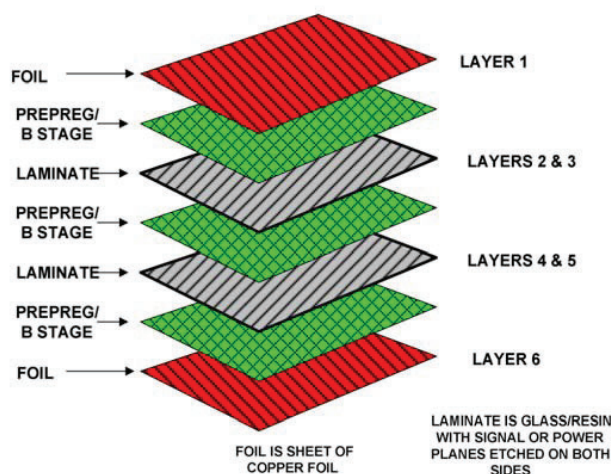


Figure 1: A typical six-layer PCB stackup using foil lamination.

DESIGNING A PCB STACKUP, PART 1 *continues*

teristics while satisfying cost and manufacturability goals.

Alternative PCB Fabrication Methods

Figure 2 is an illustration of the cap lamination method of manufacturing a multilayer PCB. As can be seen, there are three pieces of laminate each with two conductor layers in this version of a six-layer PCB. The most obvious difference between this and foil lamination for this six-layer PCB is that only two pieces of laminate or details must be processed using foil lamination while three are required with cap lamination. This represents a cost increase over foil lamination. This was the method used to fabricate PCBs in the early days of multilayer fabrication.

A third method for creating a multilayer PCB is by the use of buried and blind vias. In one version of this method, the internal $n-2$ layers are fabricated using either of the two methods shown above, resulting in a complete sub-PCB with plated through holes running from layer 2 to layer $n-1$. Then, a piece of pre-preg and a piece of foil are added to each side and the combination is laminated into a final PCB of n layers. After this second lamination step, holes are drilled through the entire stackup and plated.

It is also common to drill blind vias from layer 1 to layer 2 and layer n to layer $n-1$ as well. It is easy to see that this method will result in

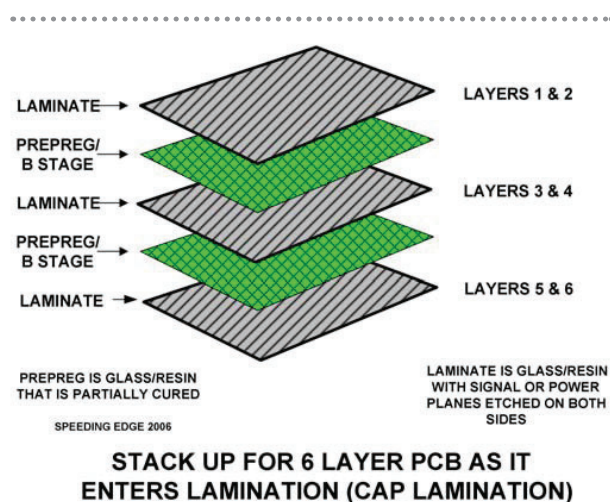


Figure 2: Typical six-layer PCB using cap lamination.

a significantly more expensive PCB that takes longer to manufacture than either of the above choices. (In some cases PCBs designed to use buried vias can cost as much as twice what the same number of layers would cost using only through-hole vias.)

Choosing a Fabricator as a Design Partner

One of the secrets to creating PCB stackups that are right the first time is to select a PCB fabricator to work with while trading off manufacturability of the final PCB stackup against signal integrity and cost goals. The right fabrication engineer can provide valuable insight into the manufacturability of proposed stackups as well as advice on how to improve a stackup. Clearly, for this to work, the fabricator must have experience manufacturing PCBs of the complexity being designed. The design engineering department must have a clear, direct path to the engineering department of the fabricator. The classic method of allowing the purchasing or materials department to select fabricators based on cost does not work well with modern designs.

My first criterion in choosing fabricators is "Are they building PCBs like mine every day or will my design represent a stretch for them?" As always, selecting fabricators that demonstrate recent capability with the class of PCB being designed goes a long way toward ensuring success on the first try. The best way to determine that there is a match is to conduct a vendor survey by visiting the factory and viewing the production line itself. Look for PCBs of your complexity being manufactured in real time. (It is common for fabricators to display complex PCBs in conference rooms that do not represent the actual capability of the fabrication process as a way to impress customers.)

This is the standard method used by companies such as Cisco to ensure suppliers are matched to the need. These visits are conducted by a team of people who represent manufacturing, engineering and purchasing, to make sure all areas are covered. Failing that, the next best way is by checking references to see how satisfied current customers are; ask for references who are willing to discuss their experiences with the supplier. If no references are forthcoming, it is well to beware.

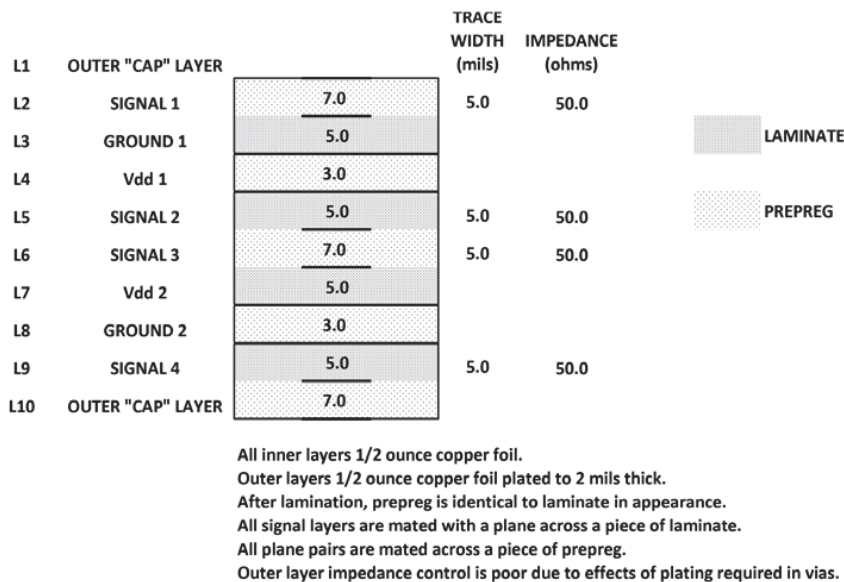
DESIGNING A PCB STACKUP, PART 1 *continues***Figure 3:** A typical 10-layer PCB stackup.**Types of Signal Layers**

Figure 3 is a typical 10-layer PCB stackup. This example has three types of signal layers: surface microstrip (L1 & L10), buried microstrip (L2 and L9) and off-center or dual stripline (L5 & L6).

There is a fourth type of signal layer—centered or symmetrical stripline: a single stripline layer centered between two planes. The reason that dual stripline is used more often than single stripline is that each time a single stripline layer is added to a stackup, a plane must also be added to isolate signal layers from each other, resulting in higher layer counts for a given number of signal layers. The method used to keep the two signal layers in the dual stripline configuration from interfering with each other (crosstalk) is to route signals on one layer horizontal and on the other vertical.

In this example, the two outer layers are not used for signals. The reason is impedance uniformity on these layers is difficult to control accurately due to the uneven plating of copper that often results when plating is done to plate copper in the holes that conduct current such as vias and power leads.

Alternate Ways to Stack Layers

Figure 4 shows two different ways to arrange the layers in a ten-layer PCB. The short bars represent signal layers and the long bars represent planes. The stacking on the left appears to have two more signal layers than the one on the right due to the fact that the top and bottom layers on the right are not available for signals and this is true. The disadvantages of the stackup on the left are power delivery related. Most high-speed designs require plane capacitance to support fast switching edges. In order to create plane capacitance, pairs of planes must be close to each other (less than 4 mils, 100

microns). The stackup shown in Figure 4 has only one plane pair close together while the stackup on the right has two plane pairs.

A second benefit of the stackup on the right in Figure 4 is that the plane pairs are separated by pre-preg which can be made very thin, less than 3 mils, as shown in Figure 3. This is of significant value when designing a power delivery system.

A third benefit of the stackup on the right is that each signal layer is paired with a power plane across a piece of laminate. The benefit here is that during lamination, the thickness of the laminate does not change and this makes it possible to achieve tightly controlled impedances on the transmission lines. When a signal layer is mated with a plane across a piece of prepreg, impedance control is more difficult as the prepreg thickness can change significantly during the press cycle.

For all the reasons given above, the layer stacking on the right in Figure 4 represents the best compromise between power delivery and impedance accuracy. If two more signal layers are needed, they would be added along with two more planes resulting in a 14-layer PCB. If four more signal layers are needed then four

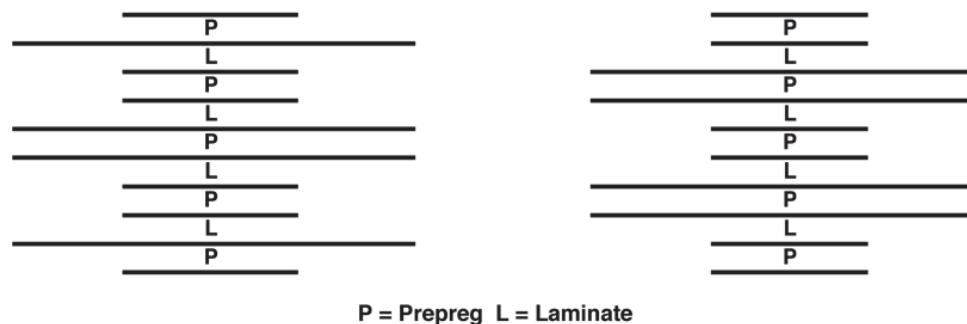
DESIGNING A PCB STACKUP, PART 1 *continues*

Figure 4: Two ways to arrange plane and signal layers in a 10-layer PCB.

more signal and four more plane layers would be added, resulting in an 18-layer PCB and so on for 22 and 26 layers.

Selecting an Impedance

The starting point for most PCB stackup design is determining what impedance or impedances to use in each signal layer. A number of impedances have been used for controlled impedance PCBs. Among these are 62 or 65 ohms for PCI buses, 72 or 75 ohms for video signals, 50 ohms for ECL and high-speed CMOS, 28 ohms for Rambus and an assortment of differential impedances for various differential signaling protocols.

Attempting to design stackups that accommodate more than one impedance value has proven to be difficult. A reasonable question to ask is whether or not multiple impedances are really necessary. The most common impedance found in multilayer PCBs is 50 ohms. It turns out that this impedance represents a happy medium between impedance value and ease of manufacture when more than two controlled impedance signal layers are needed. Therefore, it is worth examining the protocols that specify other impedance values to see if they will operate successfully with a 50-ohm transmission line.

The most common PCB impedance is 50 ohms. This impedance is achieved on stripline layers with a trace width that is about the same as the dielectric thickness. In order to make a 62-ohm line for the PCI bus, the trace width has to be made very narrow in stripline layers.

Reference 1 explains how this impedance came into existence and demonstrates that the PCI bus works properly with 50-ohm transmission lines. A similar analysis will show that the Rambus protocol also works properly with 50-ohm transmission lines. (To make a 28-ohm line, the trace width must be so wide that it will not fit between pins on a BGA.)

This leaves 72-ohm video and the various differential protocols. In almost all cases, the 72-ohm video requirement is to match 72-ohm coaxial cable bringing a signal onto a PCB or taking it off the PCB. Building a stackup that allows both 50 ohms and 72 ohms in the same signal layer is very difficult, if not impossible. Is that really necessary? I have found that if the IC using the video signal is located close to the edge of the PCB, as most are, a very short trace of 50 ohms is not going to significantly degrade the video signal. This can be easily validated using any good SI simulator.

The 100-ohm differential impedance requirement is an artifact of the need to provide two 50-ohm lines each parallel terminated in 50 ohms^[2]. It can be seen that the optimum way to route differential signals in a PCB is so that neither member of a pair interacts with the other. This is achieved by separating them from each other far enough so that one does not drive down the impedance of the other. When this is done, it is no longer necessary to specify differential impedance. As a result, all of the signals that need controlled impedance can be routed with the same impedance. The question is, what impedance?

DESIGNING A PCB STACKUP, PART 1 *continues*

From all of this, it can be seen that 50 ohms is a very good compromise impedance. It also happens to be in the sweet spot of the PCB fabrication process as well as of all the tools used to measure impedance and other characteristics of transmission lines. Therefore, it is wise to construct stackups that have a nominal impedance of 50 ohms.

In spite of what might be called out in some applications notes, every modern logic family fast enough to require controlled impedance and terminations is capable of driving a 50-ohm transmission line so there is no need to design complex stackups that require complex routing rules in order to make all of the nets fit into the space available in the signal layers.

Making All Layers the Same Impedance

Sometimes, in an attempt to provide more than one impedance on the same PCB, there is the temptation to make some layers of the stackup one impedance and others a different impedance. Examples of this are to make the PCI bus at 65 ohms and other signals 50 ohms. If this is done it is likely that the layers containing one impedance may be used sparsely while layers containing the other impedance may be overcrowded. Therefore, it is wise to make all layers the same impedance so the task of routing is easy.

Selecting Laminates

PCB material systems are defined by the resin systems used to make the laminate and prepreg. To a lesser extent, the type of glass is also part of how a laminate system is differentiated from its competition. For the most part, a glass composition known as "E" glass is used.

Resin systems used to manufacture laminate include:

- Epoxy-based systems (sometimes called FR-4)
- Polyimide
- PPO-polyphenylene oxide
- PPE-polyphenylene ester
- BT-bismalamine triazine
- CE-cyanate ester
- Phenolic cured epoxy
- Cyanate ester modified epoxy
- Filled phenolic cured epoxy

For a detailed discussion of the merits and drawbacks of each of these resin systems, see Chapter 5^[2].

In the early years of PCB manufacture the resin system choices were epoxy and polyimide. Polyimide has very good high temperature characteristics, but is very difficult to process and absorbs moisture to a level that causes it to fail leakage tests unless it is baked dry and then waterproofed. Epoxy-based systems are very easy to process and do not fail leakage tests, but don't tolerate the temperatures required to solder well. All of the other resin systems on the above list were developed in the hopes of achieving the ease of processing of epoxy and withstanding the high temperatures associated with soldering and rework achieved with polyimide. The results have been mixed. The work horses of PCB fabrication are still variations of epoxy and polyimide.

In the United States, the resin systems of choice have been Isola Corporation's FR406 and FR408 and Nelco Corporation's N4000 series. When selecting a resin system for a project it is advisable to check with the probable fabricators and determine which laminate system in their production inventory works best. It is also advisable to choose a resin system that has an equivalent with both suppliers in order to avoid creating a single-source situation.

Most projects designed in the U.S. are destined for volume manufacture off shore in China, Taiwan, Japan or South Korea. The resins systems listed above are available in all of those countries. However, there are laminate manufacturers in all four countries that manufacture laminate locally. Among these are Mitsubishi, Panasonic, Matsushita and TUC. All of these suppliers have laminates that are equivalent to the main stream laminates used in the U.S. When designing a stackup that will be prototyped in the U.S. and manufactured in volume offshore it is advisable to obtain the materials information from the offshore supplier and make sure the materials needed are available off shore.

Laminate systems are created in two parts. These are the cured laminate with copper foil on each side and partially cured laminate (prepreg) that will serve as the glue layers during

DESIGNING A PCB STACKUP, PART 1 *continues*

lamination. When creating a stackup, it is necessary to get the specifications for both types of material in order to create a stackup that can be built with available materials. Figure 5 is this information for Isola's IS620i. Notice that each thickness of laminate is made with woven glass cloth and resin. The standard construction column specifies what type of glass cloth is used for each thickness. These numbers refer to a particular glass weave with precisely specified numbers of threads per inch and thread diameter. For more details on each glass style see Chapter 5^[4].

Notice that the relative dielectric constant (ϵ_r) varies in two ways. First, it varies with the ratio of glass to resin. Second, it varies with frequency. Therefore, it is necessary to specify

both in order to achieve accurate impedance calculations. It is easy to determine which ϵ_r to use based on ratio of glass to resin. The big question is what frequency should be used for a given design. Virtually all modern designs will have components on them with 200 pSec or faster edges that must be properly controlled. It has been shown that the equivalent frequency for this rise time is approximately 2 GHz. Therefore, using the ϵ_r value at 2-2.5 GHz will result in accurate impedance calculations.

As can be seen in the above tables, a wide variety of glass styles are used to manufacture laminate and pre-preg. Prior to the advent of multigigabit differential signaling protocols, the glass style had little effect on signal quality. Since then, it has been shown that certain glass

Core Thickness	Standard Constructions	Resin Content	Dk at 100 MHz	Dk at 500 MHz	Dk at 1 GHz	Dk at 2.0 GHz	Dk at 5.0 GHz	Dk at 10.0 GHz
0.0020	1-106	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0027	1-1080	60	3.52	3.51	3.51	3.51	3.47	3.47
0.0030	1-1080	63	3.45	3.45	3.44	3.44	3.40	3.40
0.0035	2-106	66	3.39	3.38	3.38	3.37	3.33	3.33
0.0035	1-2113	51	3.74	3.74	3.73	3.73	3.70	3.70
0.0040	2-106	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0040	1-3070	49	3.80	3.79	3.79	3.78	3.75	3.75
0.0040	1 - 3313	55	3.64	3.64	3.63	3.63	3.59	3.59
0.0043	106/1080	62	3.48	3.47	3.47	3.46	3.42	3.42
0.0045	106/1080	63	3.45	3.45	3.44	3.44	3.40	3.40
0.0050	2-1080	57	3.59	3.59	3.58	3.58	3.54	3.54
0.0050	106/2113	55	3.64	3.64	3.63	3.63	3.59	3.59
0.0050	1-1652	43	3.96	3.95	3.93	3.94	3.92	3.92
0.0055	1-1652	47	3.85	3.84	3.84	3.84	3.81	3.81
0.0060	1080/2113	54	3.67	3.66	3.66	3.65	3.62	3.62
0.0060	106/ 1080	70	3.30	3.29	3.29	3.28	3.24	3.24
0.0065	1080/2113	57	3.59	3.59	3.58	3.58	3.54	3.54
0.0070	1080/2116	58	3.57	3.56	3.56	3.55	3.52	3.52
0.0070	2-2113	52	3.72	3.72	3.71	3.70	3.67	3.67
0.0075	2 - 3313	52	3.72	3.72	3.71	3.70	3.67	3.67
0.0080	2-3070	49	3.80	3.79	3.79	3.78	3.75	3.75
0.0100	2-1652	43	3.96	3.95	3.93	3.94	3.92	3.92
0.0100	3-1080	66	3.39	3.38	3.38	3.37	3.33	3.33
0.0100	2-2116	54	3.67	3.66	3.66	3.65	3.62	3.62
0.0120	2-2113/ 1652	48	3.82	3.82	3.81	3.81	3.78	3.78
0.0140	2-2116/1652	47	3.85	3.84	3.84	3.84	3.81	3.81
0.0160	3-1652	46	3.88	3.87	3.87	3.86	3.83	3.83
0.0180	2-3070/2-1652	46	3.88	3.87	3.87	3.86	3.83	3.83
0.0210	2-2116/2-1652	50	3.77	3.76	3.76	3.76	3.72	3.72

ISOLA IS 620I LAMINATE INFORMATION

Prepreg	Resin Content	Thickness (in)	Df at 100 MHz	Df at 500 MHz	Df at 1 GHz	Df at 2.0 GHz	Df at 5.0 GHz	Df at 10.0 GHz
106	75	0.0025	0.0046	0.0050	0.0056	0.0058	0.0066	0.0073
1080	65	0.0033	0.0049	0.0052	0.0057	0.0059	0.0066	0.0072
2113	58	0.0042	0.0051	0.0054	0.0058	0.0060	0.0066	0.0071
3313	54	0.0036	0.0052	0.0055	0.0059	0.0060	0.0066	0.0071
3070	55	0.0046	0.0051	0.0055	0.0059	0.0060	0.0066	0.0071
2116	55	0.0052	0.0051	0.0055	0.0059	0.0060	0.0066	0.0071
1652	51	0.0061	0.0053	0.0055	0.0059	0.0060	0.0066	0.0070

Prepreg	Resin Content	Thickness (in)	Df at 100 MHz	Df at 500 MHz	Df at 1 GHz	Df at 2.0 GHz	Df at 5.0 GHz	Df at 10.0 GHz
106	75	0.0025	0.0046	0.0050	0.0056	0.0058	0.0066	0.0073
1080	65	0.0033	0.0049	0.0052	0.0057	0.0059	0.0066	0.0072
2113	58	0.0042	0.0051	0.0054	0.0058	0.0060	0.0066	0.0071
3313	54	0.0036	0.0052	0.0055	0.0059	0.0060	0.0066	0.0071
3070	55	0.0046	0.0051	0.0055	0.0059	0.0060	0.0066	0.0071
2116	55	0.0052	0.0051	0.0055	0.0059	0.0060	0.0066	0.0071
1652	51	0.0061	0.0053	0.0055	0.0059	0.0060	0.0066	0.0070

ISOLA IS 620I PREPREG INFORMATION**Figure 5:** Typical resin information.

DESIGNING A PCB STACKUP, PART 1 *continues*

weaves can result in differential skew and excessive jitter in differential signal paths operating at or above 2.4 Gb/S^[5].

It has since been shown that three weaves which exhibit this problem are 106, 1080 and 7628. Avoiding the use of these weaves in a high-speed design obviates this problem. Of all those listed, 3313 has been shown to be the most uniform weave. For this reason, I use this weave between all my signal layers and their nearest planes.

As mentioned earlier, all of the common laminates use a glass known as "E" glass formulated to spin well and allow good adherence of resin. This glass happens to have a relatively high loss tangent. There is an alternate glass referred to as "S" glass that has a lower loss tangent. At least one laminate supplier, Nelco, uses this glass to create a low-loss laminate known as N4000-13SI. This material does have a low loss, but at the expense of creating a single-sourced PCB design. The Isola IS620i shown here has proven to be a drop-in replacement for N4000-13SI if the need for lower-loss laminate is encountered.

Considerations When Selecting a Laminate System

There are a number of properties of laminates that must be taken into account when selecting a laminate system. Among these are:

- Does the PCB require lead free assembly?
- Does the PCB require a high T_g (ability to withstand high temperatures)?
- Does the design require a low-loss laminate?
- Can the program tolerate a single-source laminate?
- Will production volumes be manufactured in a different shop or country than the prototypes?

When most of these conditions must be met, many of the laminate types listed above will be eliminated from consideration.

Obtaining Laminate Information

In order to properly design a PCB stackup it is necessary to obtain laminate information

of the quality shown in Figure 5. There are two places to get this information. These are the fabricator and the laminate manufacturer. My first choice is to ask the fabricator for this data. Often, the engineering departments of fabricators do not have it. This is a sign that the fabricator is not up to the skill level required to successfully participate in designs of this complexity.

In the event the fabricator does not possess this information, the second choice is to contact the materials manufacturer directly. Laminate manufacturers accustomed to supplying materials to the high performance market will have their materials characterized in this manner and will openly share the data. There are laminate manufacturers who do not have this data. They have been supplying materials to the low-performance market and should be avoided.

In Part 2, we will investigate methods for calculating and testing impedance, and discuss the steps required for proper PCB stackup. **PCBDESIGN**

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