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P R E M I E R I S S U E

HIGH-SPEED DESIGN





A Chronicle of Speed and Density: The TLA Design Winners Through the Years

by **Happy Holden**
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SUMMARY: *Since 1988, Mentor's Technology Leadership Awards have honored the PCB designers working on the veritable edge of the cutting edge. Happy Holden tracks some of the trends he's seen in 12 years judging TLA designs.*

Printed circuit design is a complex, challenging endeavor that often goes unrecognized. There are no university degrees in PCB design, but the skills required for modern, high-speed electronics layout and design require just as much study and lab work as a university degree. Fortunately, Mentor Graphics sponsors an ongoing program to recognize the best efforts by printed circuit board designers and organizations: the Technology Leadership Awards (TLA).

The TLA was created in 1988 by Russ Henke, then GM of Mentor's Board Station Division. For 24 years, Mentor has asked companies and individuals to submit entries that they feel are examples of the best in technology of PCB design. The electronics world has responded with some of the most challenging PCBs ever seen.

The TLA entries offer a unique look at the evolution of PCB designs over nearly a quarter century, particularly in the ever-changing areas of speed and density.

Entries are accepted for six categories of applications. This is a fluid definition that can change if new applications develop or existing categories are extinguished. The categories are:

- Computers, Blade & Servers, Memory Systems
- Consumer Electronics & Handheld
- Industrial Controls, Instrumentation & Medical
- Military & Aerospace
- Telecom, Network Controllers & Line Cards
- Transportation & Automotive

The most hotly contested categories are usually Industrial Controls, Instrumentation & Medical, Military & Aerospace, and Telecom. The majority comes from the U.S., the UK, China, and India. But 31 countries have submitted entries including Germany, South Africa, Finland, Israel, Hungary, Canada, Turkey, Singapore, Austria, Poland, Belgium, Spain, Norway, Sweden, Slovakia, France, the Russian Federation, Japan, South Korea, Taiwan, Pakistan, Italy, the Netherlands, Poland, Switzerland, Mexico, Egypt, Italy and Portugal. This list includes entries from universities in those countries.

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A Brief History of TLA Entries

I have been a judge for TLA since 2001, and in that time I have seen enormous changes in design complexity. Figure 1 tracks the TLA designs over this period. Each point was an entry from 2001 through 2012, with the larger triangles and squares showing the average for that year. The two diagonal dashed lines are the minimum HDI entries and the maximum through-hole multilayer entries. This is a logarithmic chart, with dispersal showing the enormous variety of entries over the years.

Figure 2 offers another way to look at these entries. I have plotted the average number of pins per square inch of substrate over the years for through-hole multilayers and microvia HDI. There has been a steady growth in the density of components from 52 (TH) and 173 (HDI) average connections per square inch in 2001 to the peak occurring in 2010 at 187 (TH) and 413 (HDI) average connections per square inch. And 2012 follows the general trend, with 180 (TH) and 330 (HDI) average connections per square inch.

The wide variations of MAX and MIN are due to the diversity of designs; typical entries range from single-sided boards to 42-layer telecom backplanes with only connectors. In 2001, only 18% of entries were HDI, but there was a steady increase of HDI entries to a level of over 40% for the last three years. HDI is also increasingly represented among the winning design, with 30% in 2001 to greater than 70% by 2010.

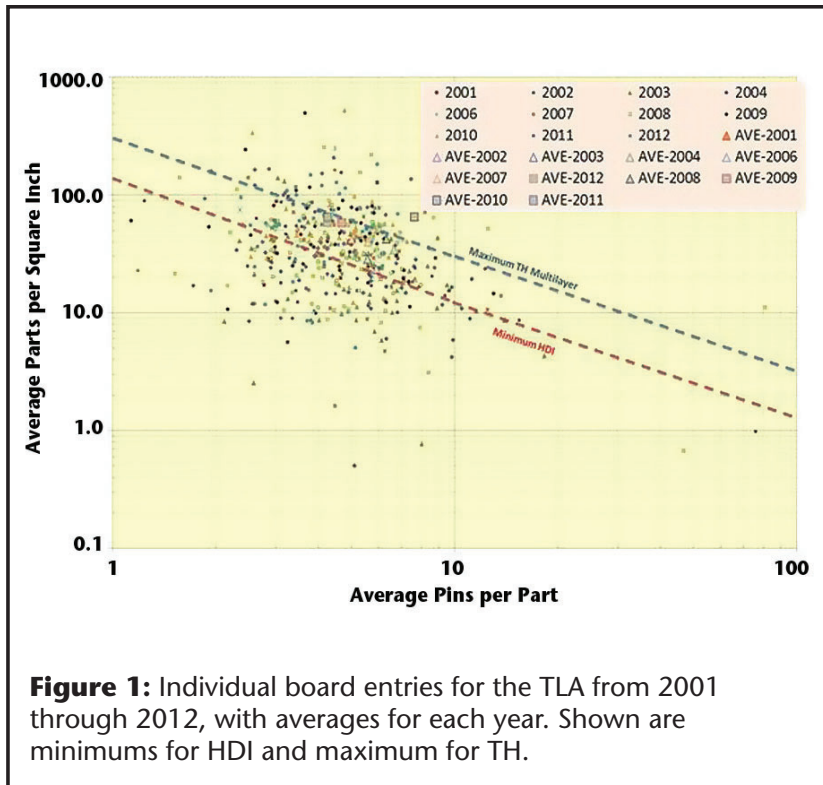


Figure 1: Individual board entries for the TLA from 2001 through 2012, with averages for each year. Shown are minimums for HDI and maximum for TH.

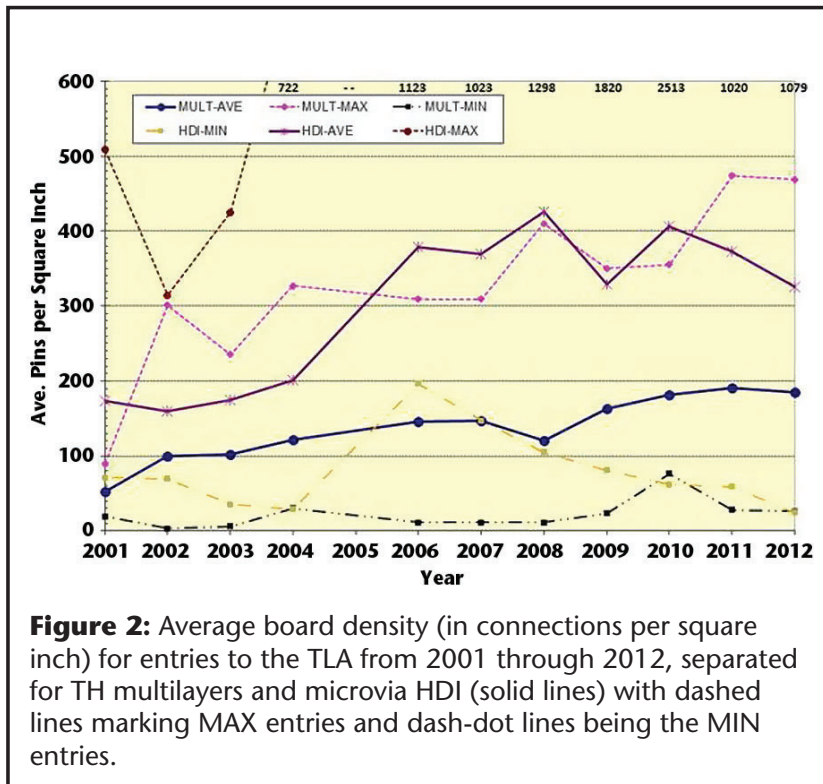


Figure 2: Average board density (in connections per square inch) for entries to the TLA from 2001 through 2012, separated for TH multilayers and microvia HDI (solid lines) with dashed lines marking MAX entries and dash-dot lines being the MIN entries.

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Mentor has automated much of the technical data for submission with EDA tool scripts. These scripts collect the physical information from the design database much like a standard design report would do. Information such as size, thickness, layers, number of nets, design rules, vias, routing distances, etc., provide data needed for Mentor to create a large spreadsheet of these technical details for the judges.

When screen captures of layers routed, 3D images, thermal maps, SI and PI simulations, and photos of the finished board or assembly are provided, the judges have a much clearer understanding of the challenges the designers and engineers faced, as well as their solutions. These are important parts of an entry that cannot be found in the design tool database – the problems that this team faced in terms of high-speed logic, critical nets, placement issues, signal integrity and noise challenges, as well as power integrity, PDN, thermal, manufacturing and cost issues.

The entry statistics for the 2012 TLA program are typical:

- Biggest board: 16.75" x 14.0"
- Smallest board: 2.67" x 2.11"
- Most layers: 28 HDI (5+16+5)
- Average traces/spaces: 4/4
- Most vias: 45,673
- Most nets: 8,057
- Most connections: 23,316
- Most components: 8,635
- Most FPGAs: 45
- Largest percentage of high-speed nets: 88%
- Highest passive/active ratio: 205:1

To better view some of the average characteristics, Figure 3 compares some averages of 2012 and 2007 with 2000 and 1995 entries. In 1995, clocks were around 66MHz and signals had nanosecond edge rates, and RAM averaged 64MB. DIP through-hole still predominated, but SMT was increasing. Mobile phones were

Design Trend	17 years ago	12 years ago	2007	2012
Min. trace/spacing (th)	6.5/6.4	5/5	4.7/4.4	2.5/2.5
Total metal layers	8	10	16	14.3
Total area (in ²)	101	76	90	58
# Nets	1465	1544	3559	1913
# Pin-to-pin connections	5190	7661	10939	6717
# Components	649	1120	2711	2217
# Component pins	4214	5790	14666	9093
Average leads / part	18	5	5	4.2
Average leads / in ²		89	212	244

Figure 3: Entry averages from 2007 and 2012 are compared to averages from 2000 and 1995.

just coming out and there were no HDI entries. By 2000, there were 750MHz processors with 100MHz clocks and rise times at 0.5ns. BGAs were small at 100-200 pins, and 18% were HDI.

To make the judging as unbiased as possible, Mentor removes the identity of each entry's designers. Each design is given an entry number, and until the winners are announced, judges have no idea who is responsible for the design, or even where it originated. We are, however, provided with the designers' written explanations of challenges they faced, which can be very interesting when dealing with non-English speaking design teams.

Figure 4 is typical of the drawings, figures and photos attached to a design entry. A verbal

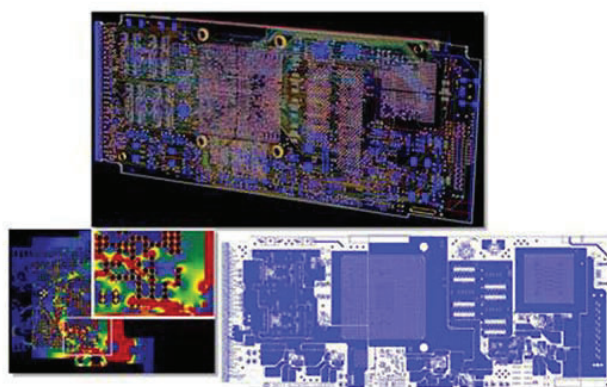


Figure 4: One of the 2012 TLA submissions featuring additional details about the power integrity of the design.

A CHRONICLE OF SPEED AND DENSITY *continues*

description is essential, as well as all the technical data and layer routings, but a finished board and a 3D image can be very helpful in putting it all into perspective!

Recent TLA Winners

To help us better gauge the caliber and trend lines of the winning designs over the years, Figures 5-10 offer a summary of the winners of the Best Overall Design awards for the last six years, followed by each team's details of the challenges associated with that design.

The 2012 Best Overall Design winner (Figure 5): Selex-Galileo's semi-active laser system:

- Complex due to unique shape and reliability concerns during use.
- Connecting two fine-pitch parts (LQFP @ 0.4 mm) without the use of microvias and large power module.
- Plated-through and cap-plated via-in-pad employed with close fabricator involvement.

- Placement and routing was done in an orthogonal fashion, then rotated to the proper 3D angle.
- EDA Tools: Expedition PCB, Dx Designer, DMS, IO Designer & Valor NPI.

The 2011 Best Overall Design winner (Figure 6): Wipro Technologies, for its single-box BTS housing transport, baseband and RF circuits:

- Digital & RF circuits – tight constraints; managed within limited board space.
- High-speed routing is done using HDI and needed strict length matching and verified using SI and timing (pre- and post-layout) simulations.
- 210 diff pairs.
- Multiple DDR3 devices.
- Serial interfaces: SGMII, SRIO-II, RP3, USB2.0.
- Power integrity: 12 major rails; 20 minor rails (lots of split planes).
- Dissipate 280W – temperature-sensitive



Figure 5: The 2012 TLA Best Overall Design from UK-based Selex-Galileo.

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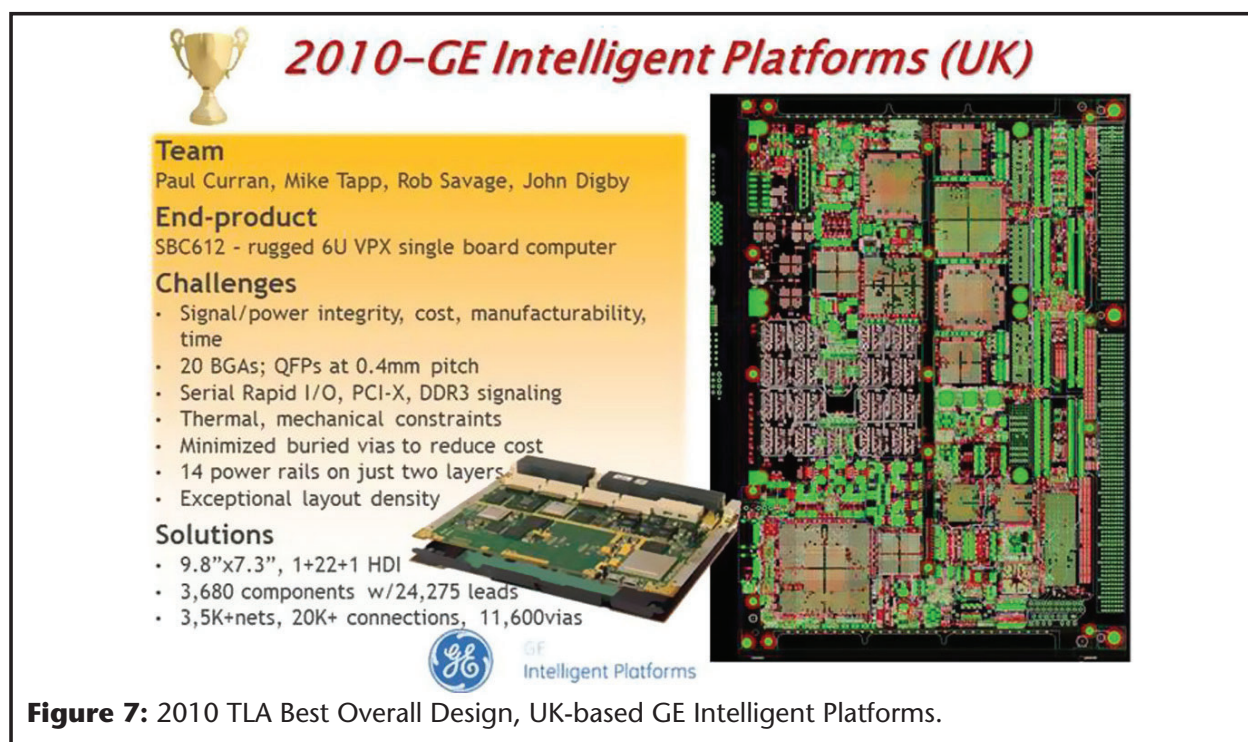
Figure 6: The 2011 TLA Best Overall Design from India-based Wipro Technologies.

devices – resolved using heat towers & thermal ground vias

- Managed tight component & routing density while minimizing crosstalk.
- Tight DfX constraints – broad test coverage required.
- SI and timing analysis on parallel buses; SI/timing and channel analysis on SERDES/differential lines
- Power integrity on power distribution planes.
- EDA Tools: Agilent ADS – RF circuit analysis and simulations; Ansoft HFSS – 3D EM simulation for RF resonance analysis; Flotherm – board-level and system-level thermal simulations; Valor – DfX review; XtremePCB – Concurrent PCB layout work.
- Concurrently, designers were working on the single database across different locations. We were able to change/modify the constraints online and work on different sections. Since the data is updated dynamically, all the designers were able to see the progress and plan accordingly.

The 2010 Best Overall Design winner (Figure 7): General Electric Intelligent Platforms' SBC612 rugged 6U VPX single-board computer:

- Aimed at high-performance mil/aero applications. 6U form factor.
- Complexity: 3,500+ nets; 20,000+ connections; 11,600+ vias; total 20 BGAs placed on both sides – several quad flat packs with 0.4mm pitch also used.
- Thermal management: Processor was low power (30W), but still needed to be placed close to a cold wall due to operation at temperatures up to 85°C. All components had to be rated for -45°C to 85°C for ruggedization.
- Mechanical: Mezzanine plug-in cards dictated low profile placement regions.
- Buried vias: Reduced buried via pairs to cut costs, which increased routing challenge.
- High-speed signaling: Serial Rapid I/O, PCI-X, DDR3 – significant constraints with tight tolerances. Placed solid continuous ground layers on either side of over 500 diff pairs to minimize impedance discontinuities.



- Power: Managed trade-offs between power consumption and thermal management. Ensured that the PCB could deliver the required 30A current.
- Significant effort taken in placement to ensure thermal efficiency, effective power delivery, and sufficient routing channels including tuning space.
- 14 power rails placed on two internal layers shielded signals from power noise with ground plane on either side. Manually increased power trace widths wherever possible to increase current capacity for critical devices.
- The stackup created for this design has been successfully used for other designs and has become the new standard. Design was completed two weeks under schedule.
- EDA tools: Expedition PCB; I/O Designer: The major design challenge was routing the processor and connecting components. Because the number of routing channels and layers was limited, it was important to reduce the number of crossover connections between the devices. I/O

Designer was used extensively to manage the unraveling of these connections. By maintaining consistency between the PCB and schematic data the team could quickly perform the necessary pin-swaps to optimize the routing without compromising the FPGA internal design.

The 2009 Best Overall Design winner (Figure 8): Tellabs Operations, for its sonnet switch module for an optical transport product:

- Tight timing margins requiring extensive constraint formulas – with tons of diff pairs, ground shielding and curved traces.
- Constraints evolved as the layout was underway.
- 120+ power rails supplying filtered power throughout the design.
- Time constraints, so two layout designers worked simultaneously with XtremePCB. Also worked concurrently with engineering.
- EDA tools: ExpeditionPCB, XtremePCB, CES, DXDesigner, FablinkXE. The use of XtremePCB and cluster attributes to group

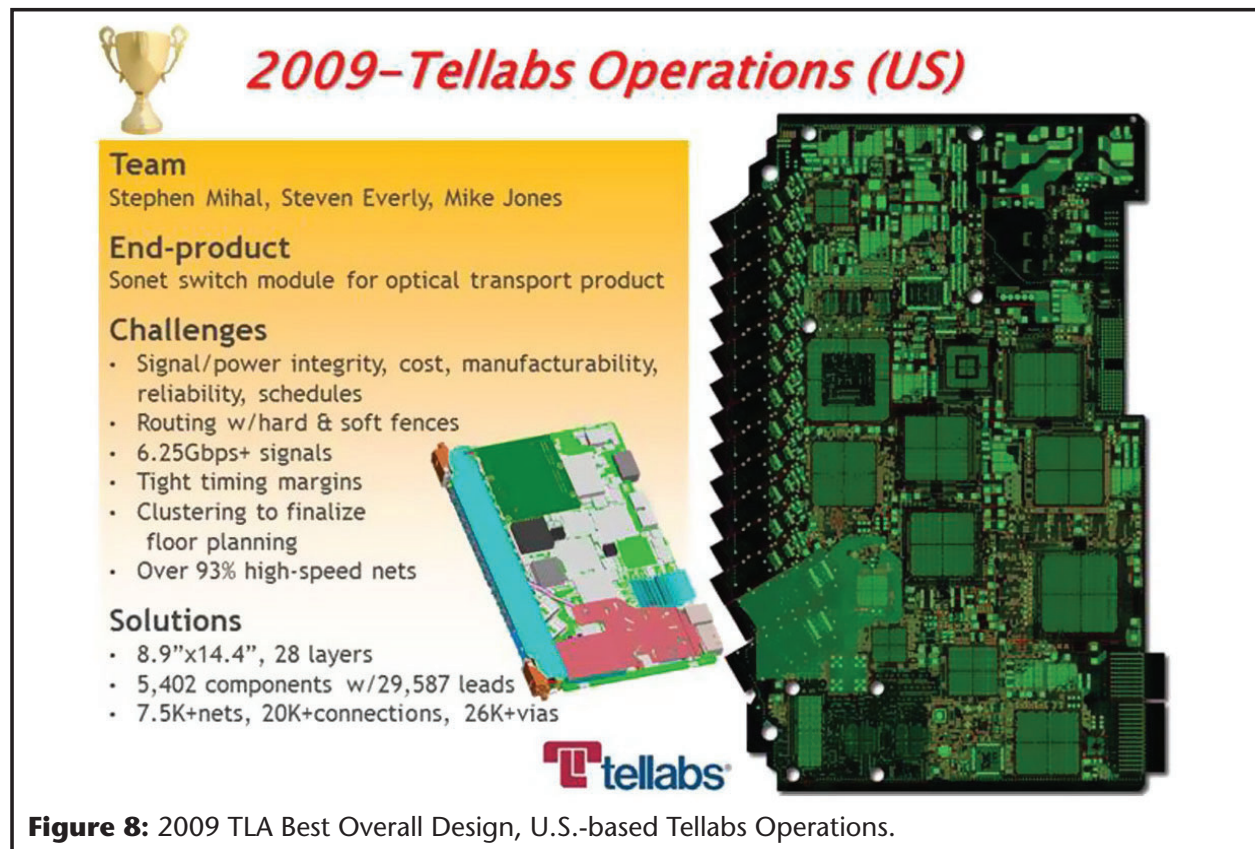
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Figure 8: 2009 TLA Best Overall Design, U.S.-based Tellabs Operations.

components quickly to finalize the design floorplan, and the ability to cross-probe between the design and schematic or CES database was crucial to our success. We utilized XtremePCB to double-team during the entire layout design phase, including floorplan, placement, fanout, defining power layers, routing and trace tuning. During the layout phase we maintained a design source for engineering changes, and if running XtremePCB was not feasible we worked through design copies and utilized the export/import functions to work in tandem throughout the floorplan and placement phase. This was instrumental in reducing the time-to-market of this product. Concurrent design techniques were followed which allowed for seamless engineer changes to the design; HyperLynx Simulation was run to model design considerations. Static signals were

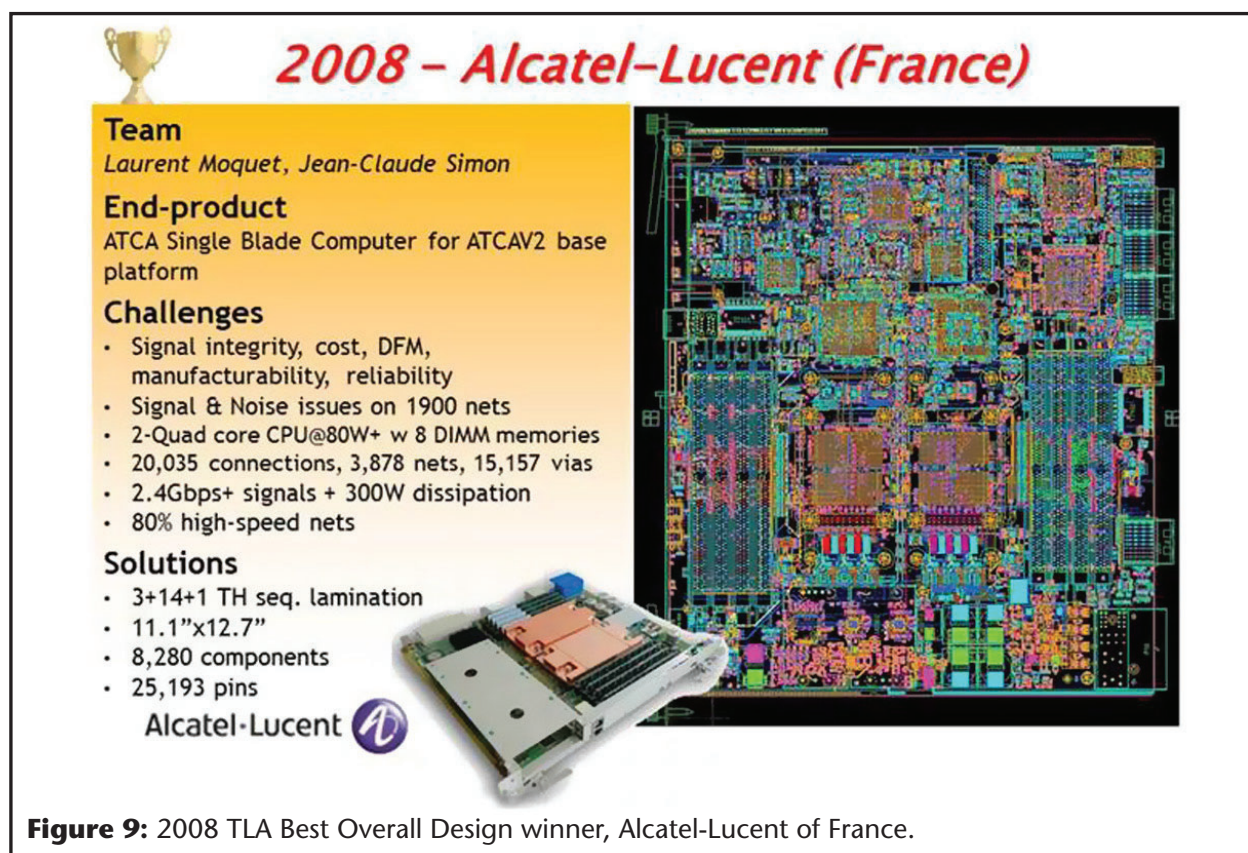
autorouted using both hard and soft routing fences.

The 2008 Best Overall Design winner (Figure 9): Alcatel-Lucent, for its optical router telecom switch module:

- Blind vias, eight power planes, two 4-layer TH MULT laminated to a 10-layer.
- 4/4 geometry, 0.010" FHS with 18:1 AR.
- Signal and noise problems for 1,900 high-speed nets.

The 2007 Best Overall Design winner (Figure 10): Siemens, for its reconfigurable FPGA-based signal processing platform on PCI-X (1.5 TeraMAC/s):

- According to Xilinx, this is the most powerful signal processing board in the world. With 16 Virtex 4 SX55 (BGA 1148 pins), DDR2-533 DRAM (BGA 0.8 mm pitch).



- Board dimensions and board thickness is limited to the PCI-X standard. The manufacturer was undefined at project start, so we needed a very common PCB technology definition. Huge estimated power dissipation (220W, 100A@1.2V, 30A transients) requires thermo simulations.
- One of the challenges was the time schedule; we had only 10 weeks for the first layout.
- All 16 FPGAs on the board had to be connected to the 128-bit cascade bus and each FPGA had its own DDR2 memory bus.
- PCI specification allows a maximum of 1.6 mm board thickness, and it was very difficult to keep the layers low! Each FPGA also has to be connected to four DDR2-533 DRAMs. Each section of the buss had 3,406 high-speed nets.
- The system performance went down

badly when we added the power layers and area fills, so we decided to switch from Solaris to Linux computers and to use a faster HW platform.

- When we started our design, the Mentor I/O-Designer did not support the Xilinx Virtex-4, so an experimental patch was added. To avoid voids during the soldering process, we found a completely new solution to via-in-pads by placing the microvias concentric to the BGA pads.
- EDA Tools: Boardstation, HiSpeed Option, Boardstation RE (partially autorouting, fanout generation), HyperLynx; AutoTherm, 3D Thermal analysis (FloTherm/Flomerics); Power integrity (PowerSI/Sigrity).

Challenges of the Future

A study of TLA design winners reveals several trends. More functionality is being supplied by semiconductor integration, with ever-in-

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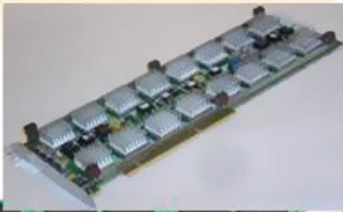
2007 – Siemens (Germany)

Team: Helmut Riedl, Manfred Hofstatter, Michael Heider, Alfred Fuchs

End-product: Reconfigurable FPGA-based signal processing platform on PCI-X (1,5 TeraMAC/s)

Challenges:

- Signal-Noise, cost, DFM-manufacturability, reliability, schedule
- 12.3"x4.7", 18 Layers, 1+16+1 HDI, 4,186 components w/ 25,203 pins
- 19,913 connections, 5,488 nets
- 80/110 micron geometry,
- 38,701 vias
- 60% high-speed nets

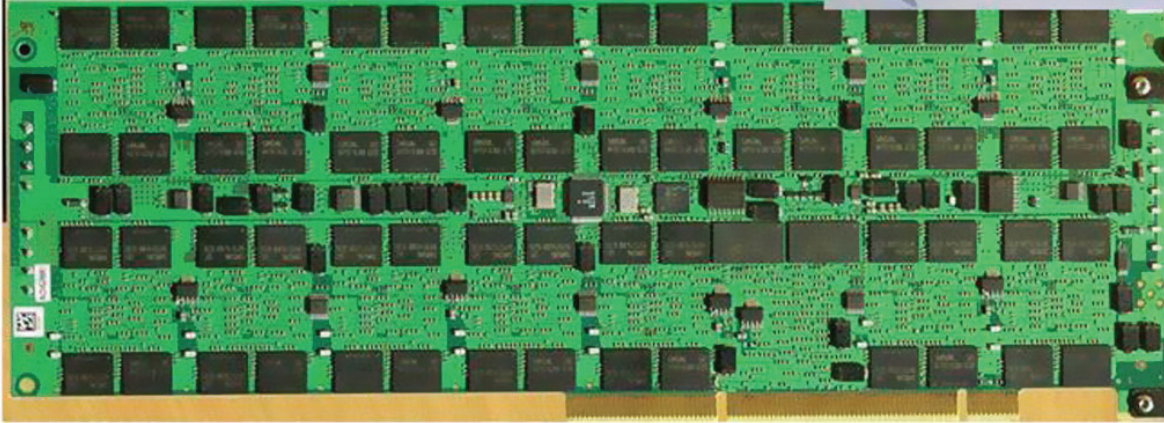


Figure 10: 2007 TLA Best Overall Design, Siemens of Germany.

creasing finer-pitch BGAs featuring more pins, busses and memory channels with their associated problems of signal and power integrity, and more passives, with thermal and manufacturing issues. Time-to-market pushes schedules, while cost controls are driving more design planning and DFM. Fortunately, there seem to be more simulation tools being used to optimize designs and solve tricky problems.

How does your work compare? If your designs are challenging, or if you have a more innovative solution to these design challenges, then you should enter the Technology Leadership Awards next year. There are few programs that show the work of our best PCB designers

and engineers, while recognizing the best designers for that work. For information about the 2013 program, click [here](#).

I hope to see one of your designs next year! **PCBDESIGN**



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