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Designing a PCB Stackup,
Part 1 p.12

Partner Early for HDI
Board Design p.26

A Chronicle of Speed and
Density: The TLA Design
Winners Through the
Years p.38

P R E M I E R I S S U E

HIGH-SPEED DESIGN



The Wrap Crack

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PWB INTERCONNECT SOLUTIONS

SUMMARY: *In the process of plating copper on the initial core, we produce a wrap of copper that goes through the barrel of the hole, and over the copper foil on its surface, producing what is called the wrap. A wrap crack is similar to a corner crack in a plated through-hole, and the focus of this column.*

Buried vias and microvias are created by a sequential lamination process, which is the number of lamination steps that the board is exposed to during fabrication. The first lamination is used to make the core that includes the buried via. It is processed just like a normal circuit board, by making internal layers with discreet innerlayer circuits, laminating the stack together, and drilling the laminated stack. The board is then subjected to desmear and hole preparation, electroless and electrolytic copper plating in the hole and etching to produce discreet circuits. After that, the board is subjected to one or more lamination steps in which other structures, like microvias, are formed.

In the process of plating copper on the initial core, we produce a wrap of copper that goes through the barrel of the hole, and over the copper foil on the surface around the hole. This copper produces what is called the wrap. A wrap crack is similar to a corner crack in a PTH.

There are two styles of microvias or buried vias: those with copper caps and those without copper caps. If there is no need for a copper cap, say with staggered microvias, the core is ready

to have the holes filled with epoxy or have the B-stage epoxy fill the hole during lamination. Frequently, the B-stage epoxy is used to automatically fill the microvia or buried via. There are occasions when the buried via is too large or too long for the B-stage epoxy to adequately fill the buried via during the lamination process. In those cases, a third-party epoxy may be used to fill the drilled holes. The third-party fill may be conductive epoxy or not, as the electrical current is carried by the copper plating in the wall of the buried via.

If a copper cap is required, as in stacked microvias, then the core may be put through a process called planarization or skiving. Sometimes the copper on the surface of the core is so thick that, with the copper cap, the dielectric spacing between the top of the buried via and the layer above is reduced. With ½-ounce copper foil, the thickness is typically 15.2 µm (.0006") of copper, 30.5 µm (.0012") of plating in the hole on the surface of the plated hole

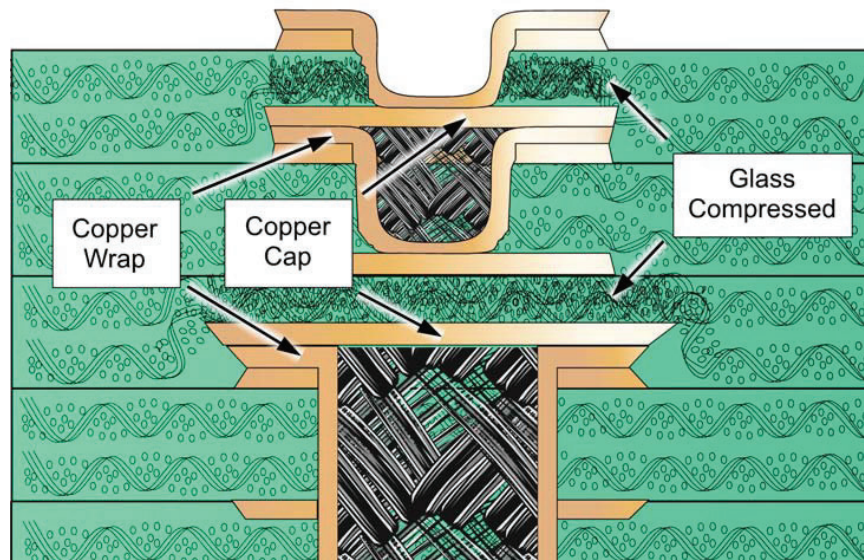


Figure 1: Planarization of the cap, wrap and glass compression.

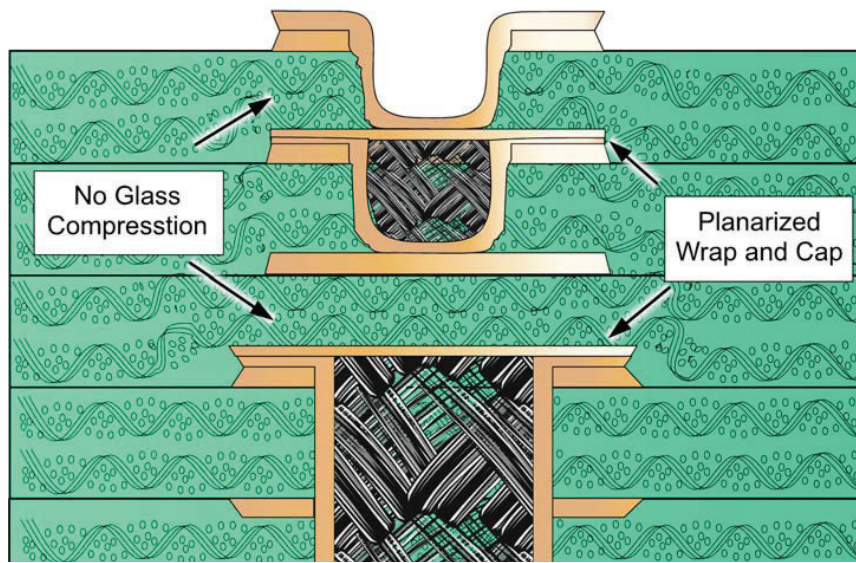
THE WRAP CRACK *continues*

Figure 2: Planarization of the cap and wrap.

and $30.5\text{ }\mu\text{m}$ of copper for the copper cap. In this case, we have a total of $76.2\text{ }\mu\text{m}$ (.003") of copper sticking up into the dielectric. If we use $127\text{ }\mu\text{m}$ (.005") of dielectric after lamination, a post of copper sticks up into the dielectric $76.2\text{ }\mu\text{m}$, thus reducing the dielectric spacing down to $50.8\text{ }\mu\text{m}$ (.002"). This means that the glass in the dielectric will be compressed during the

problem is that the core may have variation in the copper plating thicknesses due to current distribution problems. Although the copper is supposed to be $30.5\text{ }\mu\text{m}$ (.0012") thick, it may be as low as $20.3\text{ }\mu\text{m}$ (.00079") thick in some areas or on the opposite site of the board. So the planarization step needs to be controlled to skive aggressively on the $30.5\text{ }\mu\text{m}$ (.0012") circuit and less aggressively on the circuit that has $17.8\text{ }\mu\text{m}$ (.0007") of copper plating.

lamination step. The compression of the glass fibers makes an area between layers that has reduced amount of resin. This compression of the glass fibers can be described as glass lock or in extreme cases can produce a glass crack.

To eliminate this condition of glass lock or glass crack, the fabricator frequently planarizes, or skives, the copper circuits before the cap is plated. This is done to reduce the copper thickness of the wrap and produce a smooth surface. Planarization is done on both sides of the core. The

Next, the core is subjected to electroless and electrolytic copper plating and the cap is produced. After etching, the core may be planarized or skived again to produce a smooth surface and reduce the thickness of the cap. One study showed that a wrap that is $5.0\text{ }\mu\text{m}$ (.0002") thick is robust where as a wrap of less than $5.0\text{ }\mu\text{m}$ is prone to early failure. Based on this, I think a wrap of $10.1\text{ }\mu\text{m}$ (.0004") is adequate to provide a guard band. The same is true for the cap. A



Figure 3: Photo showing wrap crack.

cap of $5.0\text{ }\mu\text{m}$ seems to be robust in most applications, so I would make the requirement to be $10.1\text{ }\mu\text{m}$ as a guard band. IPC-6012 specifies that the wrap and cap will be a minimum of $12\text{ }\mu\text{m}$ (.00047") and the cap will be $12\text{ }\mu\text{m}$. Add to that the thickness of the foil, in this case $15.2\text{ }\mu\text{m}$ (.0006"). This makes the minimum copper sticking up into the dielectric a total of $38.1\text{ }\mu\text{m}$ (.0015").

To understand the role of the cap in circuits we have to understand how the electricity flow through the buried via (see [Reid on Reliability: Lifted Pad Stacked Microvia Failure](#)). What we find is that if the cap forms the target pad for a microvia, it becomes an integral part of the circuit and a crack between the cap and the wrap will produce an open. A cap that is not part of a stacked microvia can have a crack and it will not cause an open. If the cap is not part of a stacked structure it can come completely off of the microvia or buried via and the electrical path will still be intact.

A microvia or buried via which has a wrap crack type of failure presents itself as an accelerated or a wear out type damage accumulation. Usually the cycles to failure are reduced to between 100 to 200 cycles. This failure mode starts with a crack from the corner of the dielectric. The crack progresses up the face of the copper foil and then across the knee of the wrap, usually at a 45° angle. The crack can then propagate horizontally between the wrap and the cap. In Figure 4, note that the crack has trapped moisture, resulting in oxidation between the cap and the wrap.

The fill in the buried or microvia is very important. The cap on top of the buried via produces what can be best described as a "pipe bomb." The cap traps the fill inside the buried

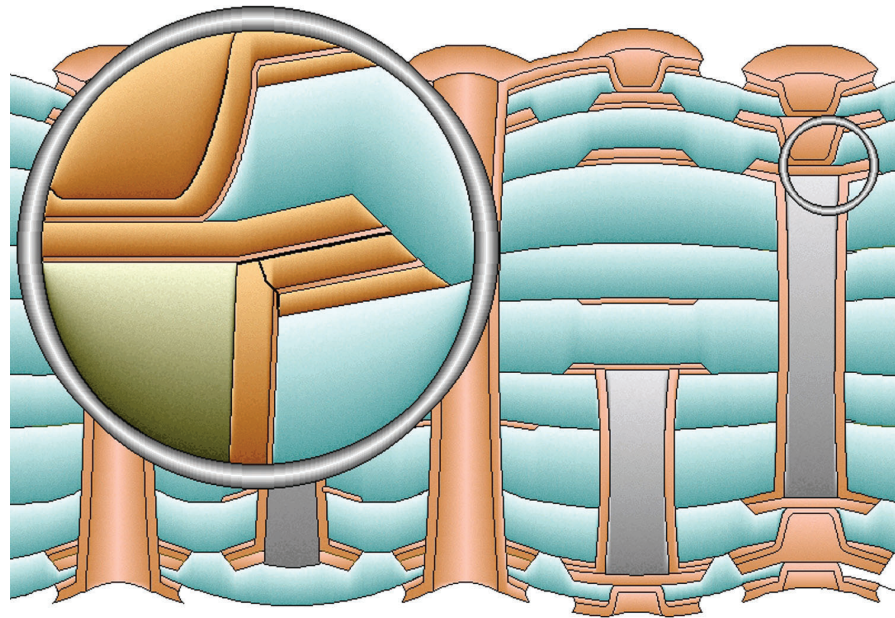


Figure 4: Animation of a wrap crack. Click [here](#) for animation.

via. Unlike the dielectric the fill is not constrained with X- or Y-axis glass fibers. The fill is expanding to all directions, X, Y and Z. Because there is more dielectric in the Z-axis the amount of pressure pushing up on the cap is greater than the X- and Y-axis pressure.

One of the factors of concern is the coefficient of thermal expansion of the fill as compared to the dielectric. While this is an important factor I believe the T_g of the fill is a bigger factor. With a T_g mismatch, the dielectric in the hole of the buried via can expand at a significantly higher rate than the surrounding dielectric until the T_g of the surrounding dielectric is reached.

The best fill is the A-stage fill of the dielectric. If one can get the A-stage dielectric and use this as the fill, the T_g will be matched and the whole buried via will have the same thermal expansion at a given temperature. **PCBDESIGN**



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