

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of: David F. Sorrells, et al Attorney Docket No.: 12189-0091IP1
U.S. Patent No.: 7,496,342
Issue Date: February 24, 2009
Appl. Serial No.: 10/972,133
Filing Date: October 25, 2004
Title: DOWN-CONVERTING ELECTROMAGNETIC SIGNALS,
INCLUDING CONTROLLED DISCHARGE OF CAPACITORS

DECLARATION OF IAN GALTON, PH.D.

Table of Contents

I.	Assignment	7
II.	Background and Qualifications	7
III.	Materials Reviewed and Considered	11
IV.	Legal Understanding.....	12
A.	Anticipation.....	12
B.	Obviousness	13
C.	Claim Construction	14
1.	ParkerVision’s Proposed Constructions	16
2.	TI’s Constructions	17
3.	PTAB’s Constructions	18
V.	The Person of Ordinary Skill in the Art	19
VI.	Summary of Opinions.....	20
VII.	TECHNOLOGY BACKGROUND.....	20
A.	Superheterodyne Receivers.....	21
B.	Direct Conversion Receivers	23
C.	Mixers	23
4.	Synchrony	24
D.	Amplifiers	25

1. Differential Circuits	25
2. Low-pass filter or Antialiasing filter	27
VIII. THE '342 PATENT	34
A. Brief Description.....	34
B. Prosecution History.....	35
C. PTAB History	36
D. Litigation history.....	38
IX. Overview of the Prior art	40
1. DeMaw.....	40
2. DeMaw Simulation.....	43
3. Tayloe	45
4. Macnally	51
5. Macnally Simulation.....	53
X. THE CHALLENGED CLAIMS ARE UNPATENTABLE.....	55
A. GROUND 1A – DeMaw Renders Claims 18-21, 23 Obvious	55
1. Analysis	55
B. GROUND 1B – the DeMaw-Tayloe Combination Renders Claims 22-23 Obvious.....	73
1. The DeMaw and Tayloe Combination	73

2. Motivation to Combine DeMaw with Tayloe	74
3. Analysis	76
C. GROUND 2 – Macnally Renders Claims 18-23 Obvious.....	79
4. Analysis	79
XI. ADDITIONAL REMARKS	101

LISTING OF CLAIM TERMS

Claim No.	Claim Element
18.P	A method for down-converting an electromagnetic signal, comprising the steps of:
18.1	(1) receiving an information signal;
18.2	(2) inverting the information signal to generate an inverted information signal;
18.3	(3) electrically coupling the information signal to a first capacitor and the inverted information signal to a second capacitor;
18.4	(4) controlling a charging and discharging cycle of the first and second capacitors with first and second switching devices electrically coupled to the first and second capacitors, respectively; and
18.5	(5) performing a plurality of charging and discharging cycles of the first and second capacitors to generate first and second down-converted information signals across first and second impedance devices, respectively;
18.6	wherein the information signal is used to store a charge on the first capacitor when the first switching device is closed and the inverted information signal is used to store a charge on the second capacitor when the second switching device is closed.
19.	The method of claim 18, wherein the first capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the second switching device is open.
20.	The method of claim 18, wherein the first capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between ten percent to

	twenty-five percent of the total charge stored therein during a period of time that the second switching device is open.
21.	The method of claim 18, wherein the first capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the second switching device is open.
22.	The method of claim 18, further comprising the step of: amplifying the first and second down-converted information signals.
23.	The method of claim 18, further comprising the step of: removing a carrier signal from the first and second down-converted information signals.

I, Dr. Ian Galton of La Jolla, CA, declare that:

I. ASSIGNMENT

1. I have been retained by Fish & Richardson P.C. as an independent expert on behalf of Petitioner Texas Instruments (“TI”). I understand that TI is petitioner in an *inter partes* review (“IPR”) of U.S. Patent No. 7,496,342 (“the ’342 patent”) (EX1001) before the Patent Trial and Appeal Board (“PTAB” or “Board”). I understand the ’342 patent is assigned to Patent Owner ParkerVision, Inc. (“ParkerVision”). I have been asked to provide my independent analysis of the ’342 patent in light of the materials cited below and my knowledge and experience in this field during the relevant period. I have been asked to consider what a person of ordinary skill in the art (POSITA) at the time of the alleged invention of the ’342 patent would have understood from the teachings of the ’342 patent, including scientific and technical knowledge related to the ’342 patent

2. I am not, and never have been, an employee of TI. I am being compensated at my standard consulting rate for my time providing my independent analysis, plus reasonable out-of-pocket expenses. I have received no additional compensation for my work in this matter, and my compensation does not depend upon the content of my opinions, any testimony that I may provide, or the ultimate outcome of the matter. All of the opinions set forth in this declaration are my own.

II. BACKGROUND AND QUALIFICATIONS

3. I am currently a Professor of Electrical Engineering at the University of California at San Diego (UCSD) where I manage the Integrated Signal Processing Group. My qualifications for formulating my analysis on this matter are summarized here with full descriptions of my educational background, professional work, qualifications, and publications set forth more fully in my curriculum vitae, which is attached to this declaration as Appendix A.

4. I received my Bachelor of Science in Electrical Engineering from Brown University in Providence, RI in 1984. I received my Masters and Ph.D. in Electrical Engineering from the California Institute of Technology in 1989 and 1992, respectively.

5. After receiving my B.S. degree, I worked as a design engineer at Mindset Corporation in Sunnyvale, CA, which was an early innovator in the personal computer market, from 1984 to 1985. I then worked as a design engineer at Mead Data Central in Menlo Park, CA, a leading database service responsible for services such as LEXIS and NEXIS, from 1985 to 1986. From 1986 to 1988 I worked as a design engineer for Acuson, Inc. in Mountain View, CA which leveraged current developments in computing technology to improve diagnostic ultrasound technology.

6. After receiving my Ph.D. in 1992 I began teaching at the University of California at Irvine as an Assistant Professor of Electrical Engineering before

moving to UCSD in 1996, initially joining as a tenured Associate Professor of Electrical Engineering prior to my current position as a tenured Professor of Electrical Engineering. I currently hold the “Skyworks Endowed Chair in High Performance Communications Devices and Circuits.” My work at UCSD includes teaching and conducting research in the field of mixed-signal integrated circuits and systems for communications. My work with the Integrated Signal Processing Group at UCSD includes leading graduate and post-doctorial students in developing enabling technology for highly-integrated, high-performance, low-cost, communication systems. The research involves the invention, development, analysis, and proof-of-principle integrated circuit (IC) implementation of key communication system blocks such as data converters and frequency synthesizers. The emphases of the research are on the development of new digital signal processing techniques and new digital-like analog circuits that exploit the strengths of advanced IC technology to mitigate the effects of non-ideal analog circuit behavior in mixed-signal and radio frequency ICs.

7. In addition to my teaching and academic research responsibilities at UCSD, I regularly consult at several semiconductor companies and teach industry-oriented short courses on the design of mixed-signal integrated circuits. I am a Fellow of the IEEE, and have served on a corporate Board of Directors, on several corporate Technical Advisory Boards, as the Editor-in-Chief of the IEEE

Transactions on Circuits and Systems II: Analog and Digital Signal Processing, as a member of the IEEE Solid-State Circuits Society Administrative Committee, as a member of the IEEE Circuits and Systems Society Board of Governors, as a member of the IEEE International Solid-State Circuits Conference Technical Program Committee, and as a member of the IEEE Solid-State Circuits Society Distinguished Lecturer Program.

8. I have authored or co-authored well over 100 scientific papers in peer-reviewed academic journals and conferences. I am also a named inventor on 25 issued U.S. Patents. I have received numerous awards from leading organizations in the area of Electrical Engineering, including IEEE. A complete list of my publications, patents, awards, and recognitions is included in my CV (Appendix A).

9. In addition to gaining expertise via my academic training, professional experiences, and research accomplishments described above, I have kept abreast of the field of RF and other mixed-signal integrated circuits specifically and electrical engineering in general by reading technical literature, attending and presenting at conferences, and attending and presenting at symposia. I have been invited to participate in the peer review process for various technical journals, and conferences, and have reviewed manuscripts submitted by other engineers relating

to integrated circuit design and communications technology. Furthermore, I have collaborated with or have communicated with many other engineers in the field.

III. MATERIALS REVIEWED AND CONSIDERED

10. In forming the opinions expressed in this Declaration, I relied upon my education and experience in the relevant field of the art, and have considered the viewpoint of a POSITA at the time of the alleged invention. I have also reviewed and considered the documents listed in the Exhibit List of this declaration. Although this declaration refers to selected portions of the cited references for the sake of brevity, it should be understood that these are examples, and that a POSITA would have viewed the references cited herein in their entirety and in combination with other references cited herein or cited within the references themselves. The references used in this declaration, therefore, should be viewed as being considered herein in their entireties.

11. Specifically, I have analyzed the following publications and materials, in addition to other materials I cite in my declaration:

- DeMaw (TI-1016)
- U.S. Patent No. 6,230,000 (“Tayloe”) (TI-1004)
- International Publication No. WO 00/16492 (“Macnally”) (TI-1023)

12. Each of these foregoing article references indicate on their face that they were published in journals or conference proceedings that I am familiar with,

and which would have been available to and disseminated to members of the general technical community prior to April 14, 2000.

IV. LEGAL UNDERSTANDING

13. I understand that issues such as invalidity and claim construction are analyzed based on certain legal standards. Counsel for TI has provided me with an understanding of these standards, and I have applied them in my analysis set forth in this declaration.

A. Anticipation

14. I have been informed that a patent claim is invalid as anticipated under 35 U.S.C. § 102 if each and every element of a claim, as properly construed, is found either explicitly or inherently in a single prior art reference. Under the principles of inherency, if the prior art necessarily functions in accordance with, or includes the claimed elements, it anticipates.

15. I have been informed that a claim is invalid under 35 U.S.C. § 102(a) if the claimed invention was known or used by others in the U.S., or was patented or published anywhere, before the Applicant's invention. I further have been informed that a claim is invalid under 35 U.S.C. § 102(b) if the invention was patented or published anywhere, or was in public use, on sale, or offered for sale in this country, more than one year prior to the filing date of the patent application (critical date). And a claim is invalid, as I have been informed, under 35 U.S.C. §

102(e), if an invention described by that claim was described in a U.S. patent granted on an application for a patent by another that was filed in the U.S. before the date of invention for such a claim.

B. Obviousness

16. I have been informed that a patent claim is invalid as “obvious” under 35 U.S.C. § 103 in light of one or more prior art references if it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention (“POSITA”), taking into account (1) the scope and content of the prior art, (2) the differences between the prior art and the claims, (3) the level of ordinary skill in the art, and (4) any so called “secondary considerations” of non-obviousness, which include: (i) “long felt need” for the claimed invention, (ii) commercial success attributable to the claimed invention, (iii) unexpected results of the claimed invention, and (iv) “copying” of the claimed invention by others. For purposes of my analysis here, I have applied a date of April 14, 2000, as the date of the alleged invention in my obviousness analyses, although in many cases the same analysis would hold true even if the date of the alleged invention occurred earlier than April 14, 2000 (especially given the earlier publication or filing dates of the prior art in Exhibits TI-1004, TI-1016, and TI-1023 as described below).

17. I have been informed that a claim can be obvious in light of a single prior art reference or multiple prior art references. To be obvious in light of a

single prior art reference or multiple prior art references, there must be a reason that would have prompted a POSITA to modify the single prior art reference, or combine two or more references, in a manner that provides the elements of the claimed invention. This reason may come from a teaching, suggestion, or motivation to combine, or may come from the reference(s) themselves, the knowledge or “common sense” of a POSITA, or from the nature of the problem to be solved, and this reason may be explicit or implicit from the prior art as a whole. I have been informed that, under the law, the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand it is improper to rely on hindsight in making the obviousness determination.

C. Claim Construction

18. I have been informed by counsel that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and custom meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. I understand that the structure of the claims, the specification, and the file history also may be used to better construe a claim insofar as the plain meaning of the claims cannot be understood. Moreover, treatises and dictionaries may be used, albeit under limited

circumstances, to determine the meaning attributed by a POSITA to a claim term at the time of filing. I have followed this approach in my analysis.

19. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time the alleged invention was made (not today).

20. I have been informed by counsel that, for purposes of my analysis in this *inter partes* review proceeding, the terms appearing in the patent claims should be interpreted according to their “ordinary and customary meaning.” In determining the ordinary and custom meaning, the words of a claim are first given their plain meaning that those words would have had to a POSITA. In that regard, I understand that the best indicator of claim meaning is its usage in the context of the patent specification as understood by a POSITA. I also understand that the words of the claims should be interpreted as they would have been interpreted by a POSITA at the time of the invention was made (not today). Because I do not know at what date the invention as claimed was made, I have used the earliest priority date of U.S. Patent No 7,496,342 as the point in time for claim interpretation purposes. That date was April 14, 2000.

21. In the co-pending litigation between ParkerVision and Texas Instruments, I have been informed that the parties have proposed claim

constructions for certain terms in the 342 patent. The terms and constructions are as follows:¹

Term	ParkerVision’s Proposed Construction	TI’s Proposed Construction
“controlling a charging and discharging cycle”	Plain-and-ordinary meaning	“controlling a cycle of charging and then discharging”
“switching device”	Plain-and-ordinary meaning wherein the plain-and-ordinary meaning is “an electronic device for opening and closing a circuit as dictated by an independent control input”	No construction necessary/ Plain and ordinary meaning, or if construction is necessary, an electronic device which opens and closes to break or complete an electrical path in a circuit

22. These claim constructions are described in more detail below. While Petitioner endorses TI’s interpretations of the claims, the prior art analyzed here is invalidating under either parties’ constructions.

1. ParkerVision’s Proposed Constructions

¹ *E.g.*, TI-1029, 13.

23. ParkerVision proposes a plain-and-ordinary meaning construction for “controlling the charging and discharging cycle” because the “language of the term is straightforward” and there are “no words that are unclear.” TI-1010, 1.

According to ParkerVision, the claim limitation “does not impose a sequential order of events,” but rather, the language of the claim term “simply means there is a switching device for each capacitor—a first switching device controls a charging/discharging cycle of a first capacitor, and a second switching device controls a charging/discharging cycle of a second capacitor.” *Id.*

24. ParkerVision proposes a plain-and-ordinary meaning construction for “switching device,” but also proposes that, if a construction were necessary, that the plain-and-ordinary meaning be “an electronic device for opening and closing a circuit as dictated by an independent control input.” ParkerVision notes that the court considered this term in another patent and adopted ParkerVision’s constructions. ParkerVision also points to the ’342 patent specification as showing that “there is always a second input (i.e., an independent control input) coming into each switch.” *Id.*, 7.

2. TI’s Constructions

25. TI proposes that “controlling a charging and discharging cycle” means “controlling a cycle of charging and then discharging.” TI points to the ’342 patent specification’s description of the invention that “repeatedly describes the

‘charging’ and ‘discharging’ portions of the cycle recited in method claim 18 as separate and distinct events.” Defendant Texas Instruments Inc.’s Claim Construction Brief, ParkerVision, Inc. v. Texas Instruments, Inc., 6:23-cv-00384 at 7. TI points out that charging occurs “when a switch is closed” and discharging occurs “when the switch is opened.” *Id.* According to TI, in the ’342 patent specification, “the alleged invention is always either charging or discharging, and never simultaneously both charging and discharging.” *Id.*

26. TI’s proposes no construction / plain-and-ordinary meaning of “switching device”; but if a construction is necessary, TI proposes “an electronic device which opens and closes to break or complete an electrical path in a circuit.” *Id.*, 9. TI’s proposal does not require that the switching device include an independent control input. *Id.* First, TI notes that the other constructions ParkerVision points to are not for the ’342 patent, and therefore are inapposite. *Id.*, 10. Second, TI argues that adding the requirement of an independent control input adds ambiguity to an otherwise unambiguous term. *Id.*, 11. Specifically, “nothing in ParkerVision’s definition explains what the control signal is independent of.” *Id.* In support of its construction, TI points to definitions of a switch or switching device from general purpose and technical dictionaries, none of which require an independent control input. *Id.*, 10.

3. PTAB’s Constructions

27. In addition to the parties’ proposed constructions, the PTAB has previously construed certain terms as follows:²

Claim Term	Construction
“electrically coupling”	“indirectly or directly connecting such that an electrical signal can flow between”
“impedance device”	“a device that exhibits an impedance”

As will be discussed in more detail below, the prior art renders the Challenged Claims unpatentable under ParkerVision’s, TI’s, and the PTABs constructions of the aforementioned terms.

V. THE PERSON OF ORDINARY SKILL IN THE ART

28. I understand that a Person of Ordinary Skill in the Art (“POSITA”) is a hypothetical person who is presumed to be aware of all pertinent prior art, thinks along conventional wisdom in the art, and is a person of ordinary creativity—not an automaton.

29. I understand the level of ordinary skill in the art is evaluated based on various factors, including: the level of education and work experience of persons in the field; the type of problems encountered in the field; and the sophistication of the technology at issue.

²TI-1030, 8-13.

30. As of the '342 patent's alleged priority date (April 14, 2000), a POSITA would have had at least a bachelor's degree in electrical engineering or a related subject and two or more years of experience in the field of electromagnetic (EM) circuit design. Less work experience may be compensated by a higher level of education, such as a master's degree.

VI. SUMMARY OF OPINIONS

31. This expert Declaration explains the conclusions that I have formed based on my analysis. To summarize those conclusions:

- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 18-21, and 23 of the '342 patent are obvious in view of DeMaw.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that claims 22-23 of the '342 patent are obvious in view of DeMaw and Tayloe.
- Based upon my knowledge and experience and my review of the prior art publications listed above, I believe that I believe that claims 18-23 of the '342 patent are obvious in view of Macnally.

VII. TECHNOLOGY BACKGROUND

32. In this section, I provide a high-level overview of technical concepts and design principles underlying direct conversion technology and the '342 Patent.

A. Superheterodyne Receivers

33. A received radio frequency (RF) signal has a frequency spectrum that is centered at the signal's carrier frequency, e.g., 900 MHz, and is non-zero over a band of frequencies, e.g. 5 MHz, centered about the carrier frequency. The objective of the down-conversion process in a wireless receiver is to shift the spectrum of the RF signal so that it is centered about zero-frequency, a process which is sometimes, albeit infrequently, referred to as "removing the carrier." The down-converted signal is typically referred to as the baseband signal. As the frequency spectrum of the RF signal has real and imaginary parts that are not necessarily conjugate symmetric about the carrier frequency, usually the baseband signal must be represented as a pair of signals, one corresponding the baseband signal's real component and one corresponding to the baseband signal's imaginary component. These two signals are typically called the in-phase and quadrature baseband signal components.

34. Unwanted RF signals with different carrier frequencies are usually present in the signal captured by the antenna, so it is necessary for a receiver to filter out these unwanted signals in addition to performing frequency down-conversion. Furthermore, the power of the signal at the antenna is usually extremely low, so the receiver must provide a large amount of amplification in addition to down-conversion and filtering operations.

35. Practical circuits used to process analog information-bearing signals often have small unwanted DC components arising from non-ideal circuit behavior. However, despite these DC components being small, they are often much larger than the received signal at the receiver's antenna output. Unfortunately, the large gains required in radio receivers have the potential to amplify these offsets so much that they overload the circuitry within the receiver, thereby rendering the receiver non-functional. This was a significant problem ever since the early days of wireless receivers, and it was solved in the early part of the 20th century by Edwin H. Armstrong with an invention called the superheterodyne receiver. The gist of the idea is to first perform frequency down-conversion to a non-zero intermediate frequency (IF) along with filtering and amplification. As the desired signal after this initial frequency down-conversion step, known as the IF signal, occupies a frequency band centered at the IF and does not overlap zero-frequency, any DC offset can be removed without affecting the desired signal. Typically, the IF signal is passed through a so-called bandpass filter centered at the IF to suppress unwanted received signals above and below the spectrum of the desired signal (including the DC component), and the result is frequency down-converted from the IF to generate the in-phase and quadrature baseband signals mentioned above, along with additional amplification. Lowpass filtering is generally applied to the baseband signals to further suppress unwanted components.

B. Direct Conversion Receivers

36. Superheterodyne receiver architectures are still used, and were extremely widely used until the 1990s. The shift away from superheterodyne receivers arose because high-quality, low-power, low-noise, and low-area bandpass filters are not amenable to integrated circuit (IC) implementation. Therefore, IC-based superheterodyne receivers generally require off-chip bandpass filters, typically surface acoustic wave (SAW) bandpass filters, to perform the necessary bandpass filtering. Such filters are expensive and their use requires dedicated IC input and output pins which are also expensive. These issues induced significant research and development efforts to develop direct conversion receivers, i.e., receivers that down-convert the received RF signal directly to baseband without first down-converting to a non-zero IF. The benefit of doing this is that lowpass filters, which are amenable to IC implementation can be applied to the baseband signals to remove unwanted signals without the need for bandpass filters.

C. Mixers

37. The term mixer in the context of wireless receivers refers to a class of circuits that perform the above-mentioned frequency shift operation. The classic communication system textbook definition of a mixer is a circuit that multiplies an input signal by a sinusoidal oscillator signal and filters the result. However, most modern practical mixer circuits perform multiplication by “squared-up” oscillator

signals, i.e., by oscillator signals which resemble square waves that ideally have the same mid-point crossing times as the corresponding sinusoidal oscillator signals. In this case the multiplication function is equivalent to multiplying the sign of the mixer's input signal by 1 or -1 as a function of the sign of the mixer's squared-up oscillator signal and can be implemented using simple transistor switches as in the prior art discussed below. Not only are such switch-based ± 1 multipliers far easier to implement than precise analog multipliers, but the use of squared up oscillator signals greatly improves noise performance. *See, e.g., I. Galton and C. Weltin-Wu, "Understanding Phase Error and Jitter: Definitions, Implications, Simulations, and Measurement," IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 1, pp. 1-19, Jan. 2019.

38. The in-phase and quadrature baseband signals mentioned above are generated by applying the RF input signal or the IF input signal to the inputs of a pair of such mixers, where the squared up oscillator signals applied to the two mixers differ in phase by 90 degrees. Lowpass filtering is always required following the mixer multiplication process, but engineers sometimes refer to just the ± 1 multiplication process as the mixing process. Either way, by the 1990s it was commonly understood that lowpass filtering is essential following the ± 1 multipliers in the baseband down-conversion process.

4. Synchrony

39. A well-known way to avoid the need to create two baseband signals, i.e., in-phase and quadrature baseband signals, is to use a single mixer that multiplies by ± 1 with a frequency and phase which precisely matches those of the carrier of the received signal. In such cases, the required oscillator signal is generated by a carrier synchronization circuit (also known as a carrier recovery circuit). The carrier synchronization circuit's input is the RF or IF signal, and its output is an oscillator signal with a frequency and phase that ideally match those of the input signal.

D. Amplifiers

40. As mentioned above, amplification is essential to the wireless reception process. The overall amplification gain from the antenna through to a receiver's baseband signals is typically many orders of magnitude. Amplifier nonlinearity has the potential to convert power from unwanted signals to distortion components that land within the frequency band of the desired signal, thereby corrupting the desired signal. As the distortion components grow disproportionately with the power of the unwanted signals and the unwanted signals often have much higher power than the desired signal, the amplifiers in wireless receivers must be designed to have a high degree of linearity.

1. Differential Circuits

41. IC implementations of circuit blocks such as amplifiers are often differential, meaning that they process pairs of signals wherein the signal information is represented as the difference between the two signals of each pair. For example, suppose the differential inputs to an amplifier circuit are denoted as v_{in+} and v_{in-} . Then the so-called differential-mode signal, defined as $v_{in} = v_{in+} - v_{in-}$, conveys the desired information content of the differential signal. Note that this definition implies $v_{in+} = v_{in-cm} + v_{in}/2$ and $v_{in-} = v_{in-cm} - v_{in}/2$, where $v_{in-cm} = (v_{in+} + v_{in-})/2$. The v_{in-cm} signal is called the common-mode signal. Therefore, the differential-mode signal is the difference between the two voltages and the common-mode signal is the average of the two voltages. As the signal information is conveyed by the differential-mode signal and differential circuits are designed not to process the common-mode signal (e.g., a differential amplifier amplifies its differential-mode input signal but does not significantly amplify its common-mode input signal), differential circuits are not sensitive to noise and distortion that equally affects the two signals which make up each of its differential signals.

42. Differential circuits are designed and laid out on an IC as symmetrically as possible, so it is the case that much of the inevitable non-ideal circuit behavior which corrupts any given differential signal, does so in the same way to both of the differential signal's two constituent signals. For example, even order nonlinear distortion corrupts each signal nearly equally, so differential

circuits tend to be insensitive to even order nonlinear distortion. However, this benefit requires good symmetry between the two halves of a differential circuit. For example two inputs of a differential amplifier must have matching input impedances for the above-mentioned benefit to occur.

43. Another benefit of a differential circuit is that it has twice the signal range as that of a comparable non-differential circuit. This quadruples the signal power, whereas it only doubles power of the noise introduced by the circuit, which corresponds to a signal-to-noise ratio (SNR) improvement of 3 dB. Modifying the non-differential circuit to improve its SNR by 3 dB would typically double its power consumption. As differential circuits typically consume less than twice the power of corresponding non-differential circuits with comparable SNRs, differential circuits are generally more efficient than non-differential circuits in terms of power consumption.

44. For the above reasons, differential circuits that are designed and laid out to be as symmetrical as possible are generally preferable to non-differential circuits in IC implementations.

2. Low-pass filter or Antialiasing filter

45. Lowpass filters are essential components in direct-conversion receivers as described above. In applications where the baseband signals are to be

subsequently sampled, lowpass filters are also sometimes called an antialiasing filters.

46. One particular differential lowpass filter is shown in Fig. 1. It is the antialiasing filter presented in Macnally, which, as explained in Macnally, is a fourth-order Butterworth filter implemented as a cascade of two of the differential Rauch biquads. TI-1021, 7:14-29. Each antialiasing filter described in Macnally has this form, although Macnally does not specify the component values. Instead, Macnally states that the filter is a Butterworth low-pass filter with a -3 dB bandwidth (also known as a cutoff frequency) of 2.4 MHz, and a gain of 15.6 dB. TI-1021, 7:17-19. The purpose of this section is to analyze the circuit shown in Fig. 1 and choose component values, i.e., values of R_1 , R_2 , R_3 , R_4 , C_1 , C_2 , C_3 , and C_4 , which cause Fig. 1 to achieve the same -3 dB bandwidth and gain as the corresponding filter presented in Macnally under the constraint that the component values are appropriate for integration in a 0.6 micron CMOS process (the IC technology in which the circuit presented in Macnally was implemented)

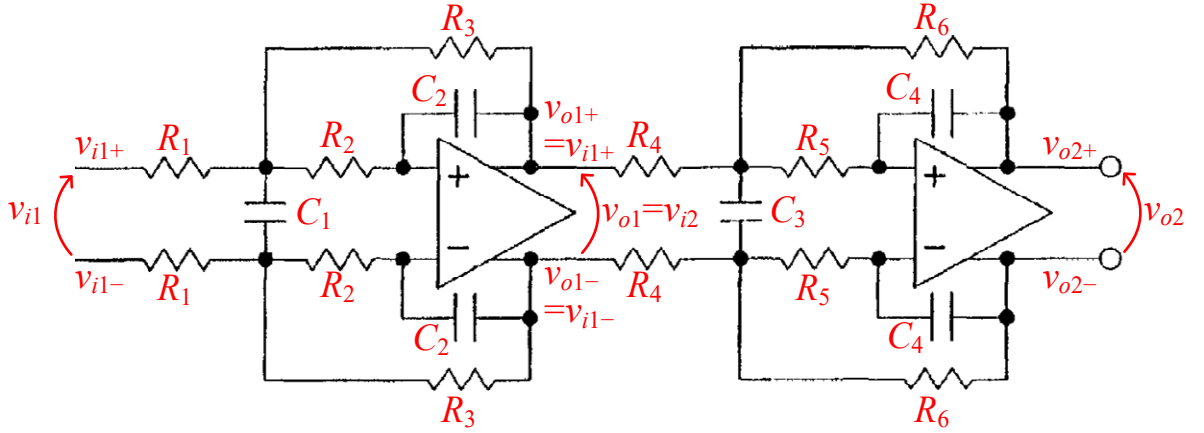


Figure 1: Annotated copy of the antialiasing filter shown in Fig. 3 of Macnally.

47. A POSITA would recognize that differential-mode behavior of the circuit of Fig. 1 can be analyzed via the differential-mode half circuit shown in Fig. 2, and that each stage can be analyzed in isolation from the other stage. *See, e.g.,* K. R. Laker, W. M. C. Sansen, “Design of Analog Integrated Circuits and Systems,” First. Ed., McGraw-Hill, 1994; E. Foster, “Active low-pass filter design,” *IEEE Transactions on Audio*, vol. AU-13, no. 5, pp. 104-111, September-October 1965. A POSITA would also recognize that each operational amplifier in such a circuit would be designed to have an open loop DC gain that is much higher than the closed-loop gain of each filter stage over the bandwidth of the filter, and, consequently, that

$$v_{m1}(s)=0 \quad \text{and} \quad v_{m2}(s)=0, \tag{1}$$

to a good approximation.

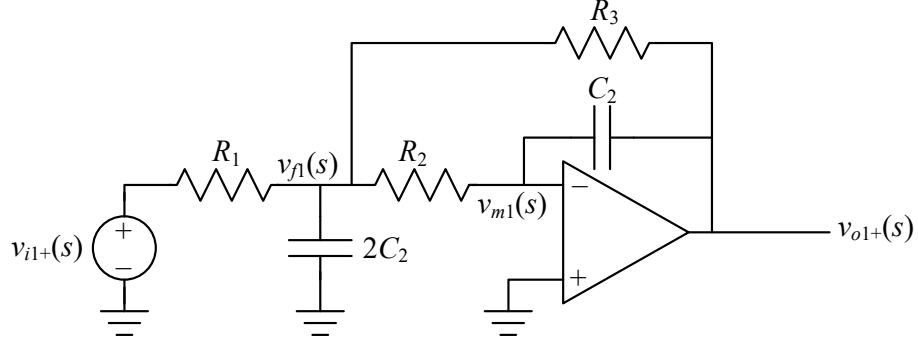


Figure 2: Differential-mode half-circuit corresponding to the first stage of Figure 1.

48. Applying Kirchoff's Current Law with (1) to the node at the negative terminal of the first op-amp and to the $v_{f1}(s)$ node in Fig. 1 yields

$$v_{ol+}(s)sC_2 + \frac{v_{f1}(s)}{R_2} = 0, \quad (2)$$

and

$$\frac{v_{f1}(s) - v_{il+}(s)}{R_1} + v_{f1}(s)2sC_1 + \frac{v_{f1}(s) - v_{ol+}(s)}{R_3} + \frac{v_{f1}(s)}{R_2} = 0, \quad (3)$$

respectively. Equation (3) can be rearranged as

$$v_{f1}(s) \left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + 2sC_1 \right] - \frac{v_{il+}(s)}{R_1} - \frac{v_{ol+}(s)}{R_3} = 0, \quad (4)$$

Solving (2) for $v_{f1}(s)$ and substituting the result into (4) gives

$$-v_{ol+}(s)sR_2C_2 \left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + 2sC_1 \right] - \frac{v_{il+}(s)}{R_1} - \frac{v_{ol+}(s)}{R_3} = 0, \quad (5)$$

Rearranging (5) gives

$$\frac{v_{ol+}(s)}{v_{il+}(s)} = - \frac{1}{s^2 (2R_1C_1R_2C_2) + s \left(R_1 + R_2 + \frac{R_1R_2}{R_3} \right) C_2 + \frac{R_1}{R_3}}, \quad (6)$$

By symmetry, it follows that

$$\frac{v_{ol-}(s)}{v_{il-}(s)} = \frac{v_{ol+}(s)}{v_{il+}(s)}, \quad (7)$$

49. By definition, the differential-mode input and output signals of the first filter stage are $v_{i1}(s) = v_{i1+}(s) - v_{i1-}(s)$ and $v_{o1}(s) = v_{o1+}(s) - v_{o1-}(s)$, respectively, $v_{i1-}(s) = -v_{i1+}(s)$, and $v_{o1-}(s) = -v_{o1+}(s)$ (this is a small-signal analysis, so the common-mode voltages are taken to be zero). As this implies $v_{i1+}(s) = v_{i1}(s)/2$, and $v_{i1-}(s) = -v_{i1}(s)/2$, it follows from (7) that the differential-mode gain of the first stage, i.e., $A_1(s) = v_{o1}(s)/v_{i1}(s)$, is given by the right side of (6), i.e.,

$$A_1(s) = -\frac{1}{s^2(2R_1C_1R_2C_2) + s\left(R_1 + R_2 + \frac{R_1R_2}{R_3}\right)C_2 + \frac{R_1}{R_3}}, \quad (8)$$

50. By identical reasoning, the differential-mode gain of the second filter stage, i.e., $A_2(s) = v_{o2}(s)/v_{i2}(s)$, is

$$A_2(s) = -\frac{1}{s^2(2R_4C_3R_5C_4) + s\left(R_4 + R_5 + \frac{R_4R_5}{R_6}\right)C_4 + \frac{R_4}{R_6}}, \quad (9)$$

51. Therefore, the differential-mode frequency response of the filter shown in Fig. 1 is given by the product of (8) and (9) with s replaced by $j2\pi f$, i.e.,

$$A(j2\pi f) = A_1(j2\pi f)A_2(j2\pi f), \quad (10)$$

where f denotes frequency in Hz and j is the unit-magnitude imaginary number.

As shown in [Foster], the circuit with

$$R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = R \quad (11)$$

for any positive value of R implements a Butterworth filter with a -3 dB bandwidth of f_0 and unity gain provided the capacitor values are chosen as:

$$C_1 = \frac{1}{2} \cdot \frac{3.91969}{2\pi f_0 R}, \quad C_2 = \frac{0.25512}{2\pi f_0 R}, \quad C_3 = \frac{1}{2} \cdot \frac{1.62359}{2\pi f_0 R}, \quad \text{and} \quad C_4 = \frac{0.61592}{2\pi f_0 R}. \quad (12)$$

52. Given that $f_0 = 2.4$ MHz, choosing $R = 1000 \, \Omega$ in (12) yields capacitor values which are easily realizable in the 0.6 micron CMOS technology used in [1], and large enough that the circuit's noise performance is unlikely to be problematic. The resulting capacitor values are:

$$C_1 = 130 \, \text{pF}, \quad C_2 = 17 \, \text{pF}, \quad C_3 = 53.8 \, \text{pF}, \quad \text{and} \quad C_4 = 40.8 \, \text{pF}. \quad (13)$$

53. While these component values in the circuit of Fig. 1 yield a Butterworth filter with the desired -3 dB bandwidth, its DC gain is 0 dB whereas the target DC gain of the overall filter is 15.6 dB. Therefore, it is necessary to modify these component values. A generally good design choice is to have each filter stage contribute half the DC gain, i.e.,

$$A_1(0) = A_2(0) = A_0 \quad \text{where} \quad A_0 = 10^{\frac{15.6/2}{20}} = 2.4547. \quad (14)$$

54. Setting $s = 0$ in (8) and (9) shows that the DC gains of the first and second filter stages are given by $-R_3/R_1$ and $-R_6/R_4$, respectively. For good noise performance, it is preferable to increase the DC gain of the two stages by increasing R_3 and R_6 rather than decreasing R_1 and R_4 . Therefore, setting $R_3 = R_6 = 2454.7 \, \Omega$ and keeping the other resistors at $1000 \, \Omega$ gives the desired DC gain.

However, to maintain the same frequency response, the capacitor values must be changed to maintain the original pole frequencies. This can be done by ensuring that the coefficients of s^2 and s in (8) and (9) change by the same factor of A_0^{-1} by which the new values of R_3 and R_6 caused the s^0 coefficients to change. Inspection of (8) and (9) shows that this requirement is achieved if C_2 and C_4 are changed to

$$C_2 \frac{R_1 + R_2 + \frac{R_1 R_2}{R_3} A_0}{A_0 \left(R_1 + R_2 + \frac{R_1 R_2}{R_3} \right)}, \quad \text{and} \quad C_4 \frac{R_4 + R_5 + \frac{R_4 R_5}{R_6} A_0}{A_0 \left(R_4 + R_5 + \frac{R_4 R_5}{R_6} \right)}, \quad (15)$$

respectively, and C_1 and C_3 are changed to

$$C_1 \frac{R_1 + R_2 + \frac{R_1 R_2}{R_3}}{R_1 + R_2 + \frac{R_1 R_2}{R_3} A_0}, \quad \text{and} \quad C_3 \frac{R_4 + R_5 + \frac{R_4 R_5}{R_6}}{R_4 + R_5 + \frac{R_4 R_5}{R_6} A_0}, \quad (16)$$

respectively. Therefore, the revised component values are

$$R_1 = R_2 = R_4 = R_5 = 1000\Omega \quad \text{and} \quad R_3 = R_6 = 2454.7\Omega \quad (17)$$

and

$$C_1 = 104.3 \text{ pF}, \quad C_2 = 8.6 \text{ pF}, \quad C_3 = 43.2 \text{ pF}, \quad \text{and} \quad C_4 = 20.7 \text{ pF}. \quad (18)$$

55. The above shows that circuit of Fig. 1 with the component values given by (17) and (18) implements the desired filter. It also shows that the filter's frequency response is given by (10) with $A_1(s)$ and $A_2(s)$ given by (8) and (9), respectively, with component values given by (17) and (18) and s replaced by $j2\pi f$. Fig. 3 shows a plot of the magnitude of the filter's frequency response in dB, i.e., a plot of $20\log(|A(j2\pi f)|)$, versus frequency in Hz on a log scale. As can be seen from

the plot, the DC gain of the filter is 15.6 dB and the filter's -3 dB frequency is 2.4 MHz, as intended.

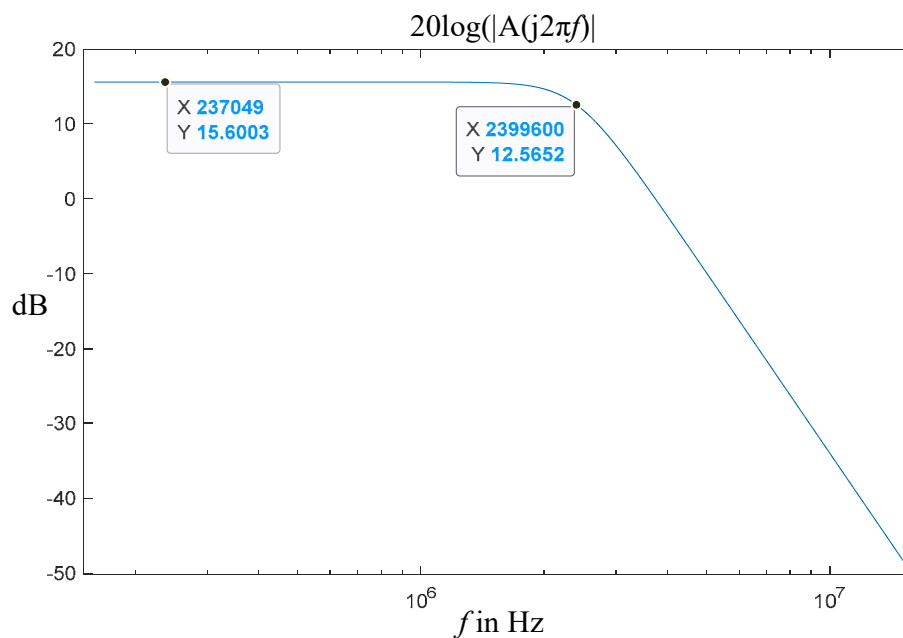
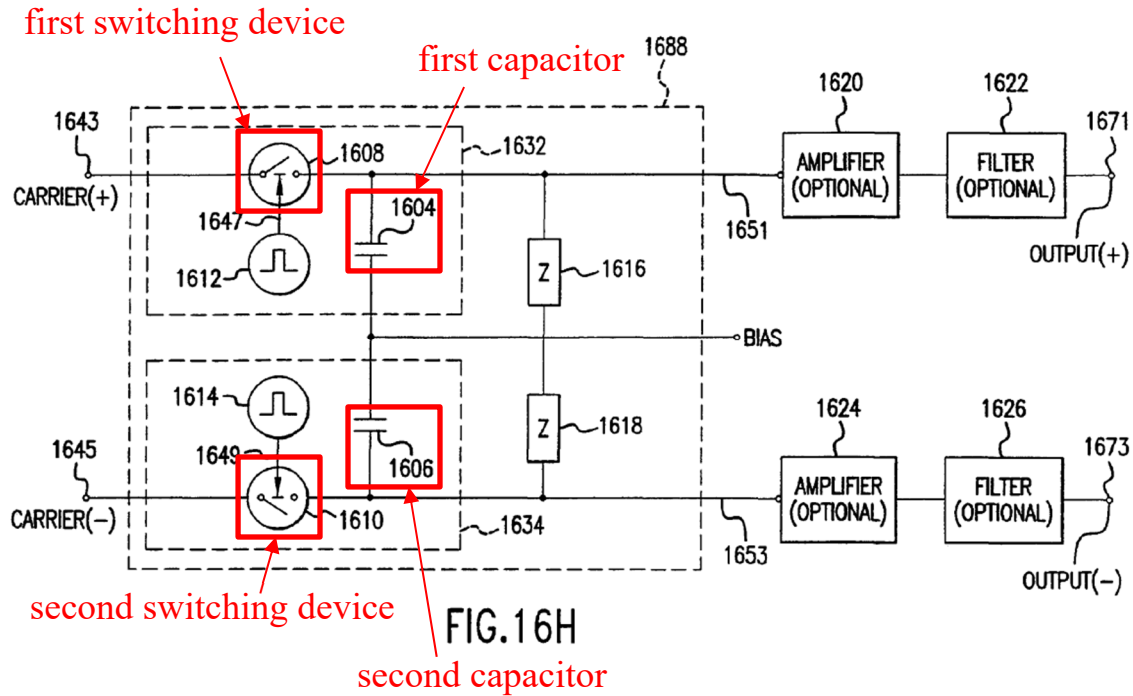


Figure 3: Magnitude of the differential-mode frequency response of the filter shown in Fig. 1 with component values given by (17) and (18).

VIII. THE '342 PATENT

A. Brief Description

56. The '342 Patent is directed to “down-converting and up-converting an electromagnetic (EM) Signal.” TI-1001, Abstract. The '342 patent generally relates to the down-conversion of an electromagnetic (“EM”) signal. TI-1001, 1:43-45, 6:25-29. Figure 16H of the '342 patent, reproduced below, illustrates an example of a receiver with two switches. TI-1001, 3:47-48, 18:6-9, 20:33-39.



The Challenged Claims are limited to a method of down-conversion using particular circuit elements, including first and second switching devices, first and second capacitors and first and second impedance devices. *See, e.g.*, TI-1001, 52:37-57. This invention is not disclosed in Application No. 09/550,644 (“the ‘644 application”). The materials describing differential embodiments in the ‘342 specification discussed above were new matter added in the ‘851 application.

B. Prosecution History

57. As mentioned briefly above, the ‘342 patent resulted from application No. 10/972,133 (the ‘133 Application). The ‘133 Application is a Division of Application No. 09/855,851 (the ‘851 Application, now US 7,010,286), filed on May 16, 2001. The ‘851 Application is a Continuation-in-Part of U.S. Application

No. 09/550,644 (the '644 Application), filed on April 14, 2000. The '133 Application claims the benefit of several provisional applications,³ but the '644 Application is the earliest claimed priority date (the so-called Critical Date). Thus, this Petition treats April 14, 2000 as the Critical Date for purposes of prior art.

58. During prosecution, the claims were the subject of an obviousness-type double patenting rejection. The pending claims were otherwise allowed. The application filed a terminal disclaimer to overcome the double patenting rejection. The claims were subsequently issued.

C. PTAB History

59. Claim 18 of the '342 patent was previously challenged in a Petition for IPR by RPX, whose petition was denied institution. *See, e.g.*, Denial of Institution, PTAB-IPR2014-01107, January 8, 2015. Institution in that proceeding was denied, not due to faults in the disclosures of Oxner, but rather due to RXP's failure as a petitioner to adequately convey how the circuit of Oxner implemented each method step of claim 18. DDI, PTAB-IPR2014-01107, 17. The present petition is distinguishable over the prior RXP proceeding in that none of the prior

³ Provisional application No. 60/272,043, filed on Mar. 1, 2001, provisional application No. 60/213,363, filed on Jun. 21, 2000, provisional application No. 60/204,796, filed on May 16, 2000.

art relied on during that petition is being asserted here. Although DeMaw (TI-1016), was discussed in connection with the Oxner reference in the petition's claim construction section (due to DeMaw being the subject of an invalidity analysis of claim 18 raised by Qualcomm in the district court), DeMaw was not considered with respect to claim 18 in the prior RPX proceeding. *See* §II.D, *infra*.

60. In discussing DeMaw, RPX noted that the circuit of Figure 6.7 “had a similar configuration to FIG. 16H of the ’342 patent, which the switches upstream of the capacitor.” Petition, PTAB-IPR2014-01107, 17-18. DeMaw, itself, notes that Figure 6.7 is similar (but not identical) to a circuit suggested in Oxner. DeMaw, 196.

61. The PTAB, in evaluating Oxner, agreed with RPX that “Oxner expressly describes all the structural features required to implement each method step recited in independent claim 18.” DDI, PTAB-IPR2014-01107, 17. However, the PTAB concluded that RPX had not presented sufficient evidence “to support a finding that Oxner expressly or inherently describes how these structural features perform the functions associated with each method step.” *Id.*

62. Here, DeMaw is a different circuit than Oxner. As discussed below, DeMaw includes all of the structural features required to implement each method step recited in independent claim 18. *See also*, §II.D (discussing DeMaw in the Qualcomm litigation and Federal Circuit appeal).

63. In addition to evaluating RPX's petition, the PTAB also made a determination of which terms to construe. The PTAB's claim construction are summarized above, in §I.C.3.

D. Litigation history

64. Claim 18 has previously been found invalid by the Federal Circuit as the result of an appeal from *ParkerVision Inc. v. Qualcomm Inc.*, 3-11-cv-00719 (MDFL) (complaint filed July 20, 2011). Prior to this finding by the Federal Circuit, the jury in the district court proceeding held claim 18 valid and infringed. TI-1031, 5, 25-26. Qualcomm moved for judgment as a matter of law of invalidity in view of DeMaw of claim 18 (among other things) based on the expert witness's testimony concerning DeMaw's circuit operation. *Id.*, 6, 11, 25-26; TI-1039. In response, ParkerVision argued that the expert witness "failed to establish that DeMaw satisfies the 'generating' limitation of claim 18." TI-1040, 17 (claim 18 requires "performing a plurality of charging and discharging cycles of the first and second capacitors to generate first and second down-converted information signals *across* first and second impedance devices, respectively"). Instead, ParkerVision argued, the expert showed that the down-converted signals were generated before the impedance devices at the output of the switches. *Id.* The analysis of DeMaw in the instant petition clearly shows that the down-converted signals are generated across the impedance devices.

65. ParkerVision also argued that the expert witness’s simulation of the DeMaw circuit was flawed because the expert used his own values for the circuit components. TI-1040, 17-18. Contrary to this assertion by ParkerVision, and in agreement with the findings of the Federal Circuit, the simulations provided herein for DeMaw use values that conform to the circuit’s intended operational parameters.

66. The court denied Qualcomm’s motion for judgment as a matter of law regarding invalidity. TI-1031, 6. Qualcomm appealed the district court’s denial of JMOL to the Federal Circuit. *ParkerVision, Inc. v. Qualcomm Inc.*, 3-11-cv-00719, dkt 553 (July 15, 2014).

67. The Federal Circuit ***reversed the district court’s denial of*** Qualcomm’s JMOL on invalidity, finding that there was “***no basis on which a reasonable jury could reject the evidence that DeMaw anticipates claim 18 of the ’342 patent.***” TI-1031, 28-29. The Federal Circuit found that “even though Figure 6.7 of DeMaw does not expressly state that the capacitors engage in ‘charging and discharging’ to generate a baseband signal,” the expert testimony “regarding the DeMaw circuit established that charging and discharging is ‘implicit’ in that reference.” *Id.*, 28. The Federal Circuit noted that ParkerVision had not been able to undermine the expert’s explanations of “the operation of the DeMaw circuit and how Figure 6.7 of DeMaw corresponds to Figure 16H of the ’342 patent.” *Id.*

Furthermore, the Federal Circuit rejected ParkerVision's arguments concerning the lack of component values in DeMaw. *See, id.* Patent Owner's present day position that the '342 Patent is somehow valid, through assertion against Petitioner, flies directly in the face of the clear finding by the Federal Circuit.

68. In agreement with the findings of the Federal Circuit, this Petition details how claim 18 is unpatentable in view of DeMaw. As discussed below, DeMaw's circuit shown in FIG. 6.7 corresponds to FIG. 16H of the '342 patent, and the simulations of DeMaw's circuit show that the operations include charging and discharging to generate a baseband signal across impedance devices, as claimed in claim 18.

IX. OVERVIEW OF THE PRIOR ART

1. DeMaw

69. DeMaw is a textbook titled, "Practical RF Design Manual," and was first published in 1982 by Prentice-Hall. DeMaw describes a dual field effect transistor (FET) balanced mixer, as shown in FIG. 6.7, reproduced below. This circuit takes two inputs, V_{RF} and V_{LO} , and generates the output V_{IF} . In the explanation of the circuit operation that follows, V_{LO} can be considered a periodic waveform with fundamental frequency f_{LO} (DeMaw 3.A.1) (or a squared-up version of a sinusoid thereof, as described in Section VII), and V_{RF} can be a

modulated sinusoidal carrier of frequency f_{RF} . DeMaw's circuit can be part of a superheterodyne receiver.

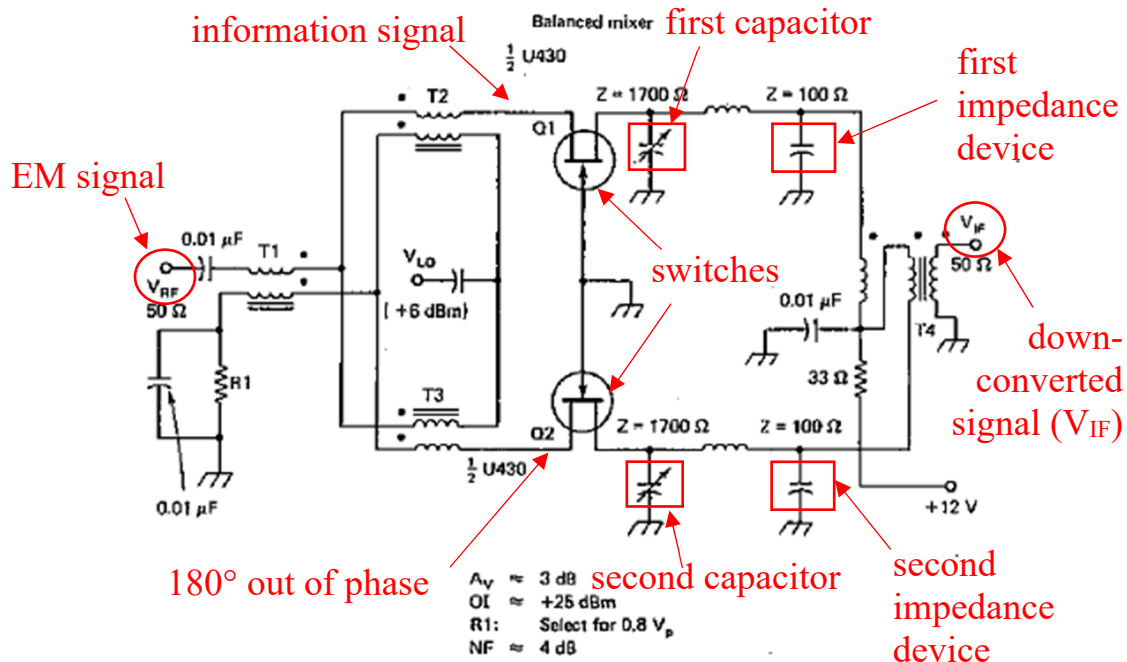


Figure 6.7 Dual FET balanced mixer using a Siliconix U430 device.

DeMaw, FIG. 6.7 (annotated)

The three transformers T1, T2, and T3 are arranged in a configuration known as a 180° hybrid coupler. This achieves three goals:

- 1) The quiescent operating point of Q1 and Q2 can be set via the resistor R1.
- 2) The RF signal, V_{RF} , is electrically coupled in-phase at the source (left terminal) of Q1 and 180° out-of-phase at the source (left terminal) of Q2.
- 3) The local oscillator signal, V_{LO} , is electrically coupled in-phase at the sources of both Q1 and Q2.

70. Next, observe that the circuit formed by Q1, the upper capacitor-inductor-capacitor (C-L-C) network, and one winding of transformer T4 is identical to the circuit formed by Q2, the lower C-L-C network, and another winding of transformer T4. Thus, the right-half of this circuit starting at Q1 and Q2 form a differential circuit, symmetric along the horizontal midpoint axis. The value of R1 is selected “to give a V_{GS} of 0.8 the pinchoff voltage.” DeMaw, 196. This bias point, along with the large swing of V_{LO} (DeMaw, 194-195), causes the signals at the sources of Q1 and Q2 to traverse a highly nonlinear region of its V_{GS} - I_{DS} transfer characteristic. This nonlinearity causes intermodulation between the components of the signals at the sources of Q1 and Q2. As discussed above, the source of Q1 is driven by a signal which contains components proportional to $+V_{LO}$ and $+V_{RF}$, while the source of Q2 is driven by a signal which contains components proportional to $+V_{LO}$ and $-V_{RF}$. The aforementioned nonlinearity in the transistor V_{GS} - I_{DS} transfer characteristic results in the drain currents of Q1 and Q2 containing signals proportional to the products V_{LO}^2 , V_{RF}^2 , and $V_{LO}V_{RF}$. Transistors Q1 and Q2 are switches because they turn off and on periodically as a function of V_{LO} .

71. Using trigonometric identities, we can compute that the drain currents of Q1 and Q2 contain many different frequency components. The C-L-C networks which follow the drains of Q1 and Q2 are known as a π -matching networks. They

are bandpass impedance matching networks that are tuned to the frequency $|f_{LO} - f_{RF}|$, which is called the intermediate frequency, f_{IF} . Therefore, we can make the following statements about the voltages across the second impedance devices:

- 1) The signal components whose frequencies are far from f_{IF} are rejected by the π -matching network.
- 2) The signal components across the respective impedance devices at frequency f_{IF} are 180 out of phase.
- 3) There are signal components at frequencies $2f_{LO}$, $2f_{RF}$, etc., that are in-phase.

The transformer T4 is wound in a manner that the differential signal across the second impedance devices is transferred to its output terminal, while the common mode signal is suppressed. Thus, the output of this circuit, V_{IF} , is dominated by the signal proportional to $V_{LO}V_{RF}$, which is the goal of the mixer.

2. DeMaw Simulation

72. The analysis of DeMaw includes a simulation of the above circuit using LTspice XVII (17.2.4), a freely available SPICE-compatible simulator. The LTspice XVII simulator is a well-known simulator, with a long history and many

regarded among those practicing in this technology area. Waveform data is not modified or post-processed in any way except where noted in the plots.

73. For the DeMaw circuit simulations, parameter values that were described in DeMaw were used, with minor adjustments. For example, the exact parameters of the transformers were not provided; only the physical description was given. Reasonable values were calculated based on the expected circuit operating conditions. In particular, the transformer coupling ratio is ideal, however using a realistic (non-ideal) coupling ratio would not affect the presented results. A SPICE model was found for the exact JFET specified in the book, the Siliconix U430.

74. The DeMaw circuit was simulated for 400 μ s. The LO signal used is a square wave of 150MHz and amplitude of 1.2V peak. While using a square wave for the LO of this circuit is an idealization, it does not alter the circuit behavior in any way relevant to the presented results. It was chosen to be able to clearly see the transition between switch ON and OFF states.

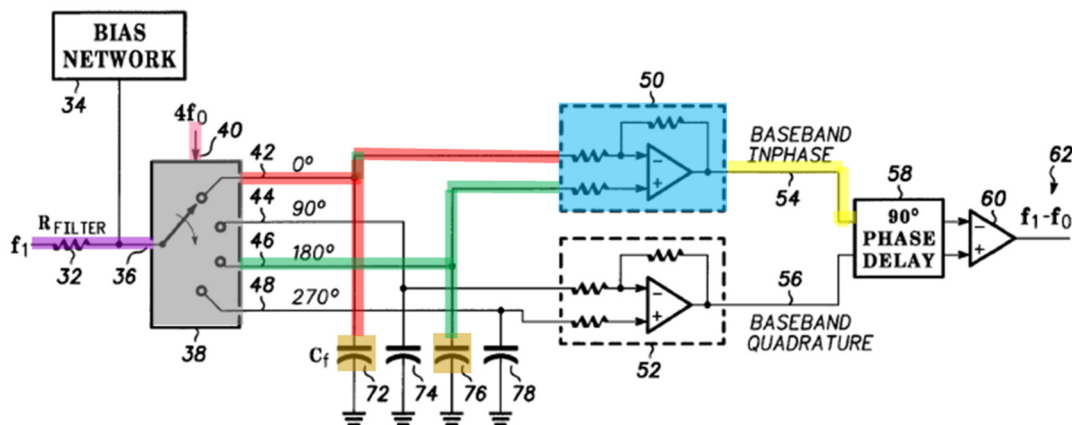
3. Tayloe

75. Tayloe is directed to a direct conversion receiver (also referred to as a “product detector”) “for converting a signal to baseband.” TI-1004, Abstract, 1:51-52. Tayloe’s direct-conversion circuitry operates to down-convert a radio frequency (RF) or intermediate frequency (IF) signal to baseband. *See, e.g.,*

Tayloe, 2:13-14 (“In operation, an RF or IF signal f_1 is received at resistor 32.”); see also TI-1001, 1:60-63 (describing that “the invention down-converts the electromagnetic signal to a demodulated baseband information signal”). Tayloe explains that its direct conversion receiver includes a commutating switch that “serves to sample an RF waveform four times per period at the RF frequency.” *Id.*, Abstract. “The samples are integrated over time to produce an average voltage at 0 degrees, 90 degrees, 180 degrees and 270 degrees” *Id.* “The average voltage at 0 degrees is the baseband in-phase signal, and the average voltage at 90 degrees is the baseband quadrature signal.” *Id.*

76. Tayloe describes that, “to increase gain, the 0 degree average can be differentially summed with the 180 degree average to form the baseband in-phase signal.” *Id.* Tayloe achieves this differential summation using a summing amplifier that amplifies the difference between 0 and 180 degree baseband signals. *Id.*, 2:56-67. Tayloe states that “[d]irect conversion receivers are desirable in part because they convert signals of interest directly to baseband (or near zero hertz) from a radio frequency (RF) or an intermediate frequency (IF).” *Id.* at 1:10–13.

77. In more detail, Tayloe discloses an example of a direct conversion receiver in FIG. 3:



30 **FIG. 3**

TI-1004, Figure 3 (annotated).

78. The receiver receives an RF input signal f_1 and down-converts this signal to produce signal of interest 62. *Id.*, 2:13-67 (“[A]n RF ... signal f_1 [purple] is received at resistor 32.... After passing through resistor 32, the input signal is received by commutating switch 38 [gray] at input 36. Commutating switch 38 switches input 36 to outputs 42 [red], 44, 46 [green], and 48.... As commutating switch 38 cycles through the four outputs, capacitors 72-78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants.... The outputs of commutating switch 38 are input to summing amplifiers 50 [light blue] and 52. Summing amplifier 50 [light blue] differentially sums the 0 degree output [42 (red)] and the 180 degree output [46 (green)], thereby producing baseband in-phase signal 54 [yellow]. The resulting

signals are then summed by summing amplifier 60 to produce the signal of interest 62”).

79. Tayloe’s receiver has four frequency down-conversion circuits, the outputs of which are labeled “0°,” “90°,” “180°,” and “270°,” each including a switch and a storage element (*e.g.*, capacitor).

80. The 0° frequency down-conversion module provides a 0° down-converted signal 42 (red). TI-1004, 2:13-18 (“[A]n RF ... signal f_1 [purple] is received at resistor 32.... After passing through resistor 32, the input signal is received by commutating switch 38 [gray] at input 36. Commutating switch 38 switches input 36 to output 42 [red]....”), 2:46-48 (“Output 42 [red] represents the average value of the [RF] input signal [f_1 (purple)] during the first quarter wave of the period [of the input signal f_1], and is termed the 0 degree output.”).

81. The 0° frequency down-conversion module includes a commutating switch 38 (gray), which periodically couples the input signal f_1 (purple) to the output 42. TI-1004, 2:16-26. Moreover, the rate at which the commutating switch 38 periodically couples the input signal f_1 at input 36 (purple) to the output 42 is determined by a control signal ($4f_0$, pink) supplied to a control input 40 of the switch. *Id.*, 2:18-20 (“The rate at which commutating switch 38 operates is controlled by a signal present at control input 40.”). At the start of each successive cycle of the $4f_0$ control signal, the commutating switch changes which of its four

outputs, 42, 44, 46, and 48, is connected to its input 36. As there are four outputs, this means that each of the commutating switch outputs, 42, 44, 46, and 48, is successively connected to input 36 at a frequency of f_0 Hz for a duration of $1/(4f_0)$ seconds.

82. The 0° frequency down-conversion module also includes a capacitor 72 (brown). “During the time that [the commutating] switch 38 connects input 36 [receiving the RF input signal f_1] to output 42, charge builds up on capacitor 72.” TI-1004, 2:32-33. The voltage across the capacitor 72 corresponding to this charge constitutes the average value of the RF input signal f_1 during first quarter of the period of the signal f_1 and is output from the 0° degree frequency down-conversion module as the 0° down-converted signal 42 (red). *Id.*, 2:46-48 (“Output 42 [red] represents the average value of the input signal during the first quarter wave of the period, and is termed the 0° degree output.”), 2:18-26.

83. Similarly, the 180° frequency down-conversion module provides a 180° down-converted signal 46 (green). TI-1004, 2:13-18 (“After passing through resistor 32, the [RF] input signal [f_1] is received by commutating switch 38 [gray] at input 36. Commutating switch 38 switches input 36 to output[] ... 46 [green]....”), 2:50-53 (“Output 46 [green] represents the average value of the input signal [f_1 (purple)] during the third quarter wave of the period [of the input signal f_1], and is termed the 180° degree output.”), 2:18-26.

84. The 180° frequency down-conversion module includes the commutating switch 38 (gray) and a capacitor 76 (brown). When the commutating switch 38 couples the input signal f_1 (purple) to the output 46, charge builds up on the capacitor 76 (brown). TI-1004, 2:18-38 (“During the time that commutating switch 38 connects input 36 to output 42, charge builds up on capacitor 72.... The same principle holds true for capacitor[] 76 ... when commutating switch 38 connects input 36 to output[] 46....”).) Thus, voltage across the capacitor 76 constitutes the average values of the RF input signal f_1 during the third quarter of the period of the signal f_1 and is output from the 180° frequency down-conversion module as the 180° down-converted signal 46 (green). *Id.*, 2:50-53 (“Output 46 [green] represents the average value of the input signal during the third quarter wave of the period, and is termed the 180 degree output.”), 2:18-26.

85. The 90° and 270° frequency down-conversion modules each have a similar operation and structure. TI-1004, 2:35-39 (“Likewise, during the time commutating switch 38 connects input 36 to output 44, charge builds up on capacitor 74. The same principle holds true for capacitors 76 and 78 when commutating switch 38 connects input 36 to outputs 46 and 48 respectively.”). “As commutating switch 38 cycles through the four outputs, capacitors 72–78 charge to voltage values substantially equal to the average value of the input signal during their respective quadrants” *Id.*, 2:39-43. “Output 44 represents the average

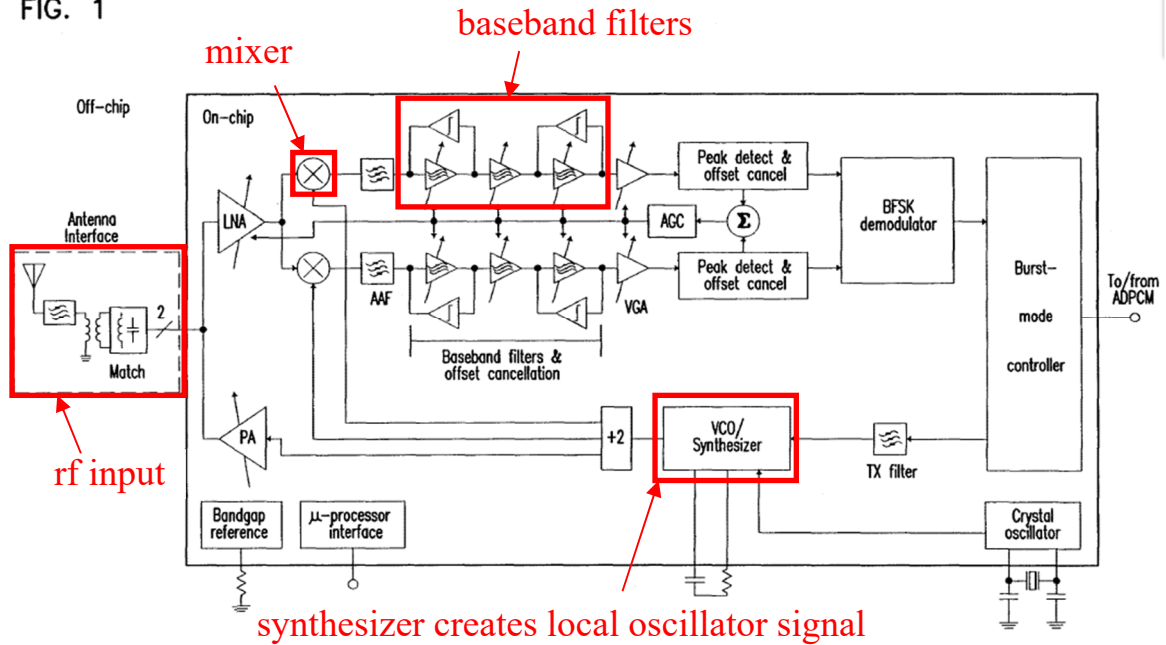
value of the input signal during the second quarter wave of the period, and is termed the 90 degree output.” *Id.*, 2:48-50. “Output 48 represents the average value of the input signal during the fourth quarter wave of the period, and is termed the 270 degree output.” *Id.*, 2:53-55.

4. Macnally

86. Macnally, titled A Single-Chip CMOS Direct-Conversion Transceiver, is an International Patent Publication No. 00/16492 published on March 23, 2000. Macnally claims the benefit of priority to U.S. Provisional Patent Application No. 60/099,723, filed on September 10, 1998.

87. Macnally describes “[a] single-chip CMOS direct conversion transceiver [including] a receiver having a baseband filter, and a demodulator.” Macnally, Abstract, 1:5-6. Macnally’s fully-integrated transceiver, shown in FIG. 1, “incorporates RF circuits 102, 104, synthesizer 106, baseband filters 108, demodulator 110, and digital signal processing.” Macnally, 8:22-24. FIG. 1 is shown below:

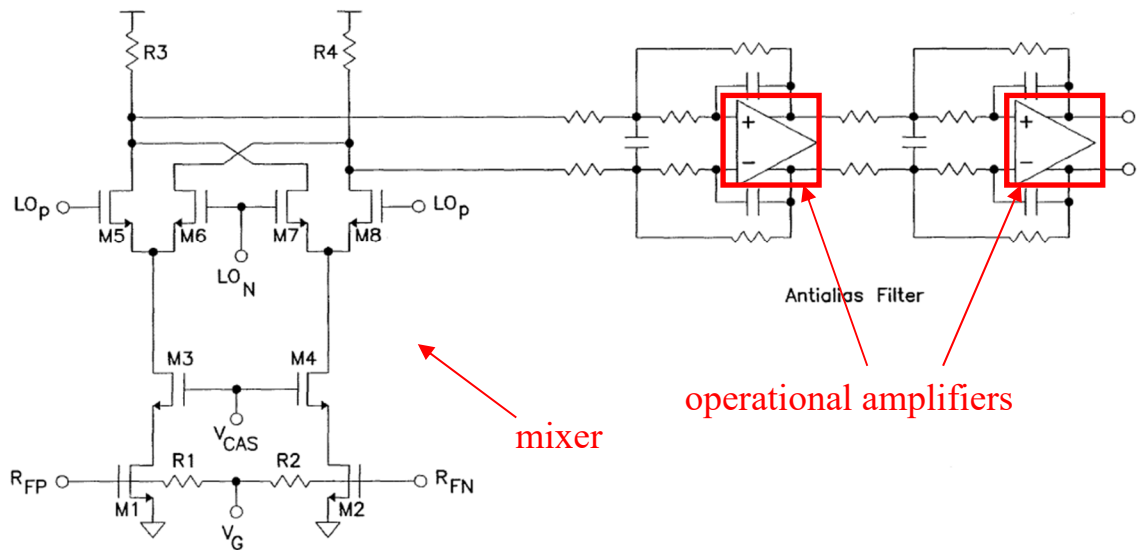
FIG. 1



Macnally, FIG. 1 (annotated)

88. For the receiver, Macnally shows a “diagram of a mixer 142 and an antialiasing filter 144,” as annotated below. *Id.*, 12:15.

FIG. 3



TI-1014, FIG. 3 (annotated).

89. Macnally discloses “[t]he output of the mixer 142 is fed to a four-pole Butterworth antialiasing filter 144.” TI-1014, 7:7-16,17-29 (“Two biquad stages form the four-pole Butterworth antialias filter”), FIG. 1 (full diagram). Macnally describes a Butterworth lowpass filter with a 2.4 MHz cutoff frequency and nominal gain of 15.6 db. Macnally,

90. Noteworthy, Macnally’s system includes certain “off-chip” components, including “an ISM band filter 112, a balun 114, an RF matching network 116, an RC loop filter for the [phase-locked loop] PLL 118, a crystal resonator 120, and a resistor 122 for biasing.” Macnally, 8:24-26.

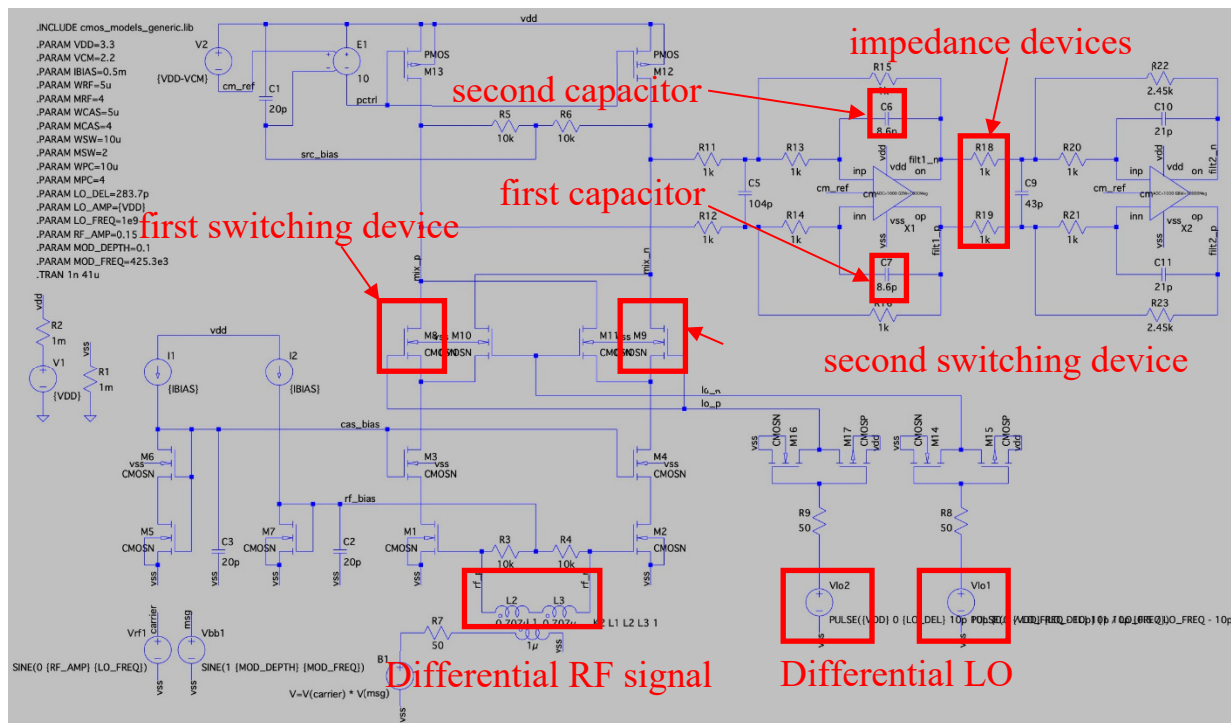
91. I have provided a discussion of Macnally’s differential amplifiers that are part of its antialiasing circuitry in §VII.D above.

5. Macnally Simulation

92. I have also provided a simulation of Macnally’s mixer and antialiasing circuitry. The circuit was built using the limited descriptive text available in the patent. The SPICE technology library models a generic CMOS process with 0.6um gate lengths, using a 3.3V supply voltage. Reasonable choices were made for device W/L ratios to make the circuit work as intended. This circuit was not optimized in any way; however, further optimization (for noise and power, for example) would not affect the presented results in any way. As no details of the biasing circuits were given for the mixer core, simple bias circuits and controllers

were created. In places, these circuits rely on ideal elements such as voltage-controlled voltage sources. The usage of these devices is limited to non-critical areas that do not affect the presented results. Within the antialiasing filters, an op-amp (short for operational amplifier) macromodel was used that emulates an op-amp with 60dB of DC gain. The choice of a macromodel accelerates simulation time, but does not affect the presented results. As I discussed above, the LTspice XVII simulator is a well-known simulator, with a long history and many refinements over the years (it was first released in 1999). Furthermore, the results identified here are within the expected results for this circuit and therefore align with how I would expect the circuit of Macnally to operate based on my own analysis of the circuit.

93. The entire Macnally simulation testbench is shown in MACNALLY-SIM-FIG. 1, below:

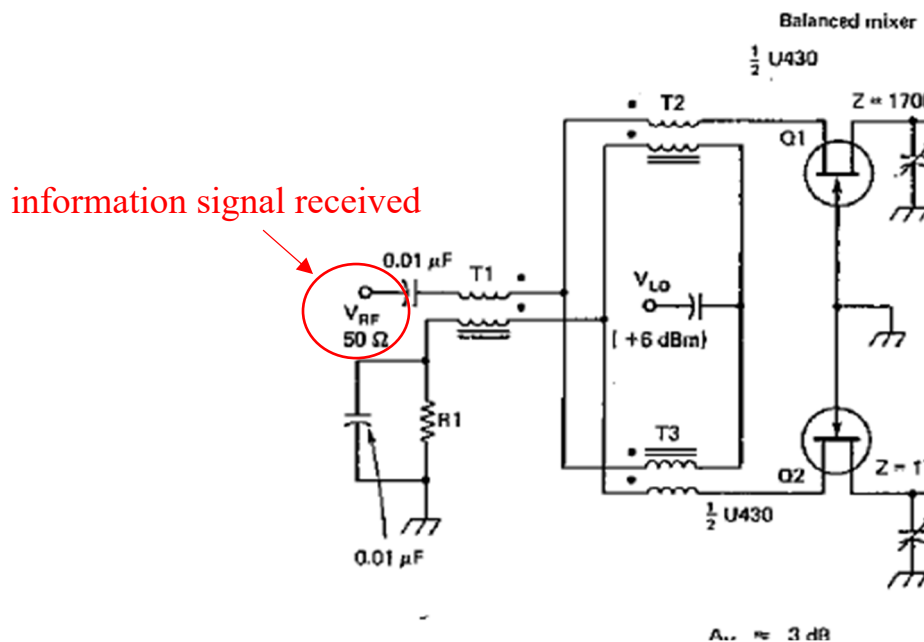


18.P A method for down-converting an electromagnetic signal, comprising the steps of

95. As explained above, and will be shown through simulation, DeMaw describes a balanced mixer that down-converts an electromagnetic signal (an RF signal) to generate an intermediate frequency (IF) signal. DeMaw, 196-197. The method steps are described below using the FIG. 6.7 circuit provided by DeMaw. Simulation waveforms are also provided for each method step (as appropriate) to show the performance of the method steps by the circuit.

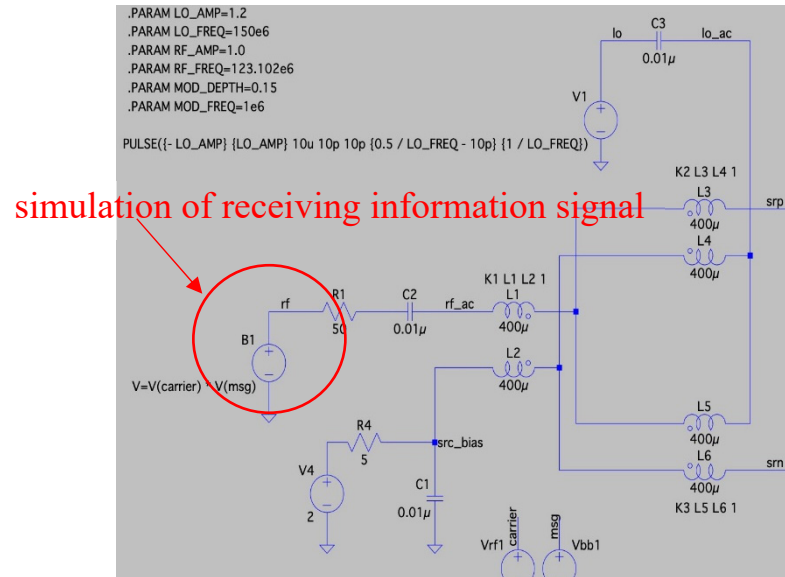
18.1 (1) receiving an information signal;

96. DeMaw describes receiving an information signal. Specifically, DeMaw's balanced mixer receives an RF information signal into a single-ended (meaning non-differential) input, as shown in FIG. 6.7 below:



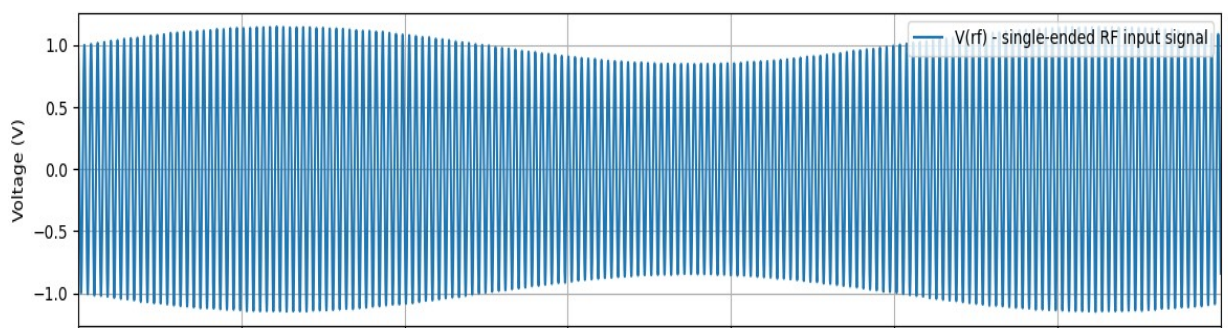
DeMaw, FIG. 6.7 (partial, annotated)

In simulation, V_{RF} was generated with a 1.0 volt, 123.102MHz sinusoidal carrier AM modulated with a 0.15 volt, 1 MHz sinusoidal “message signal.” This V_{RF} source is shown in DEMAW-SIM-FIG. 1:



DEMAW-SIM-FIG. 1 (partial, annotated)

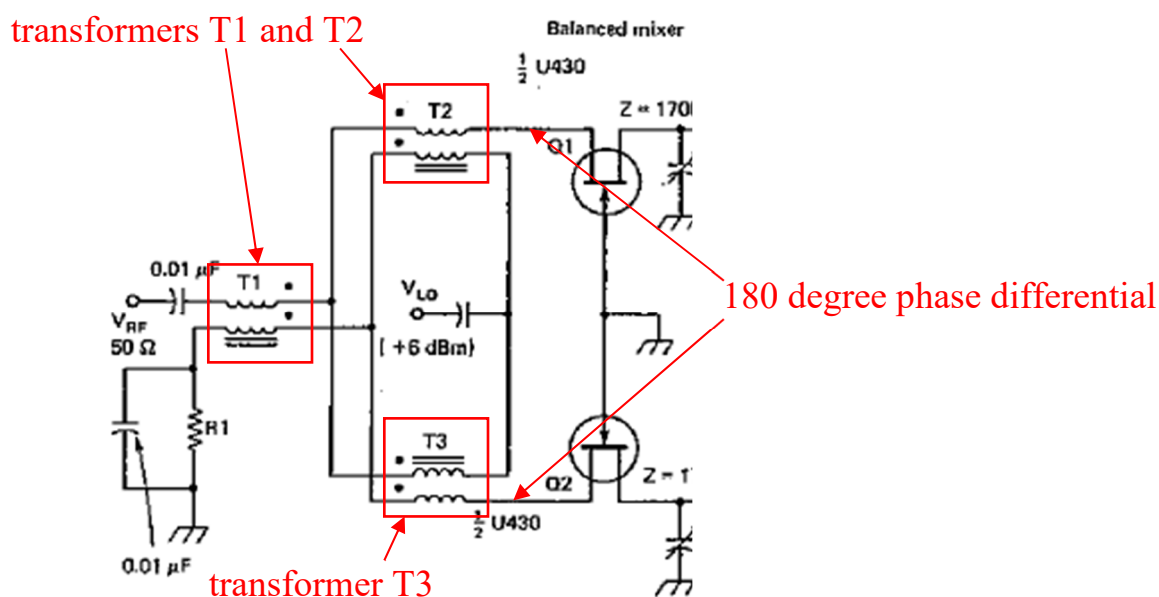
The single-ended RF input signal is illustrated by DEMAW-SIM-FIG. 2:



DEMAW-SIM-FIG. 2 (RF Input Signal)

18.2 (2) inverting the information signal to generate an inverted information signal;

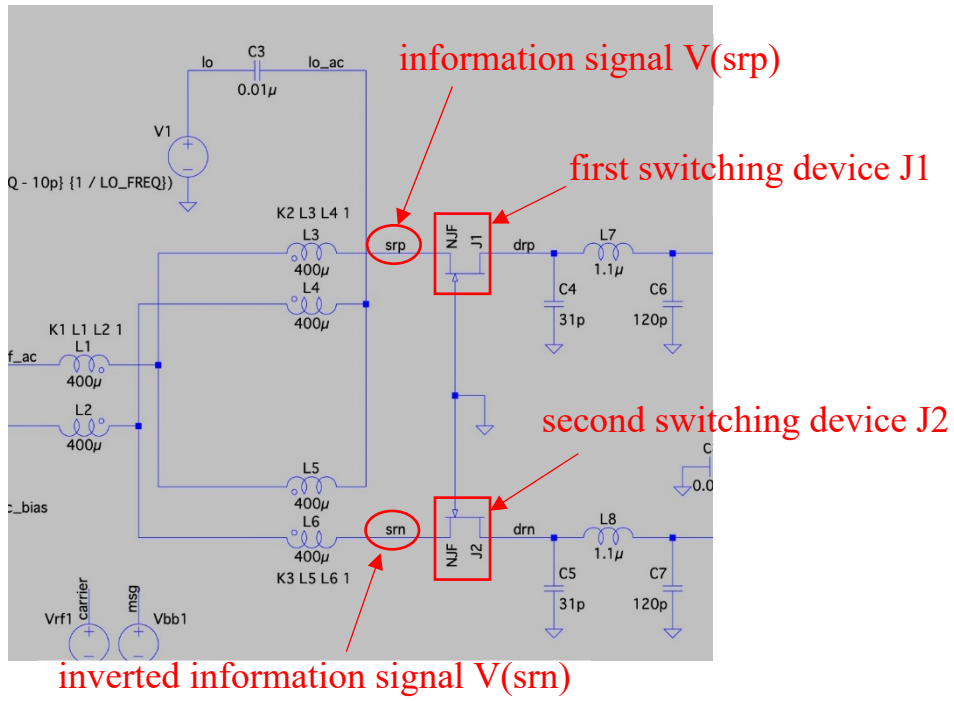
97. DeMaw's circuit uses the trio of transformers T1, T2, and T3 operating as a 180° hybrid coupler described above, to create “a 180° phase differential between the sources of switching devices Q1 and Q2.” (DeMaw, 196-197). The inverted information signal is shown below:



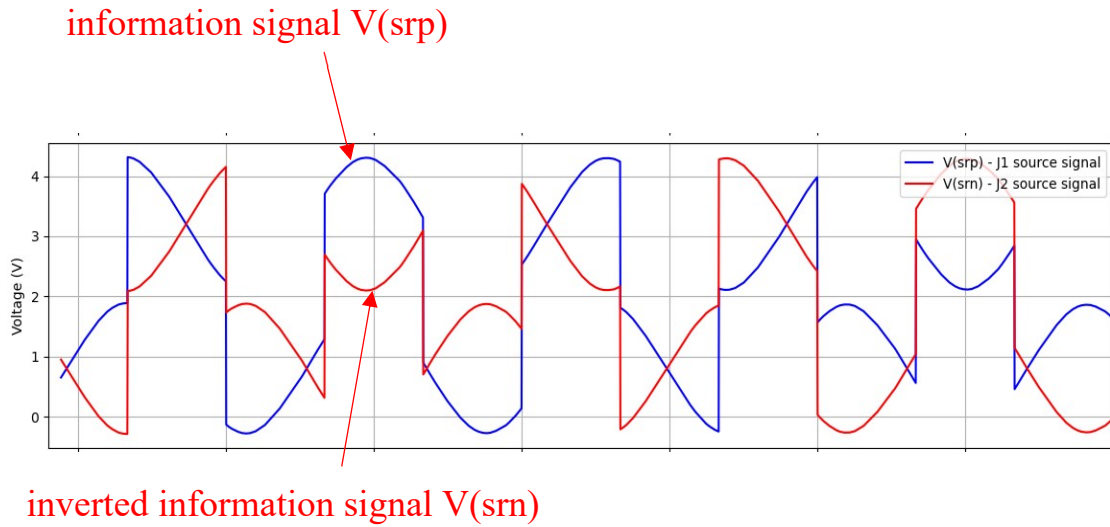
DeMaw, FIG. 6.7 (partial, annotated)

A POSITA would have recognized that the creation of a differential signal with a 180° offset includes inverting the information signal.

98. The simulation is used to plot the voltages at nodes *srp* and *srn*, which are connected to the sources of the first and second switching devices J1 and J2, respectively. These are labeled in DEMAW-SIM-FIG. 3:



DEMAW-SIM-FIG. 3, (partial, annotated)



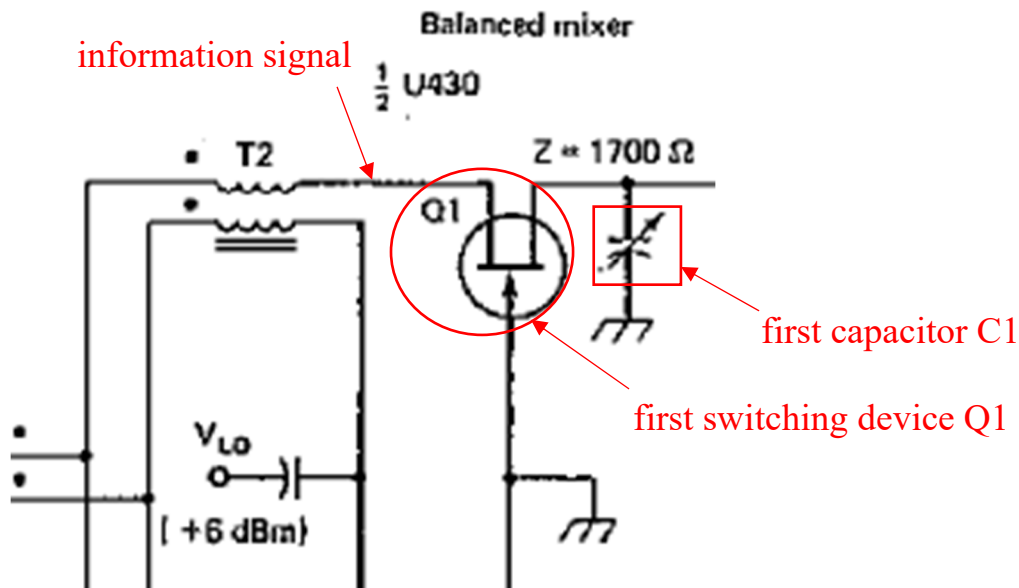
DEMAW-SIM-FIG. 4, inverted information signal

DEMAW-SIM-FIG. 4 shows the information signal $V(srp)$ (in blue) at the source of the first switching device J1. Likewise, DEMAW-SIM-FIG. 4 shows the

inverted information signal $V(srn)$ (in red) at the source of the second switching device J2. This plot demonstrates the hybrid coupler operation, whereby the information signal and inverted information signals are superimposed upon an in-phase LO signal, appearing at the first and second switching devices, respectively.

18.3 (3) electrically coupling the information signal to a first capacitor and the inverted information signal to a second capacitor;

99. In DeMaw, in operation, when switch Q1 is closed (i.e., turned on), the information signal is electrically coupled to the first capacitor. This is shown in DeMaw FIG. 6.7 below:

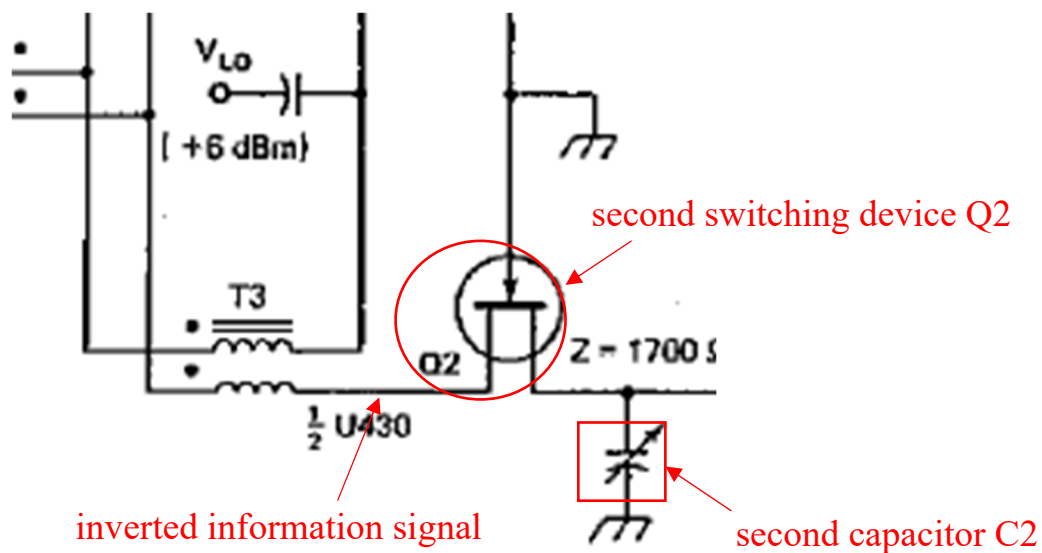


DeMaw, FIG. 6.7 (partial, annotated)

100. The first switching device Q1 “electrically couples” the information signal to the first capacitor C1 when it is closed. More precisely, the current that

flows through the drain of Q1 is substantially proportional to the voltage at the source of Q1, which contains the information signal. This current causes charge to accumulate in capacitor C1. Therefore, the amount of charge present on Q1 (and therefore the voltage across it) is a function of the information signal present at the other side of the switch.

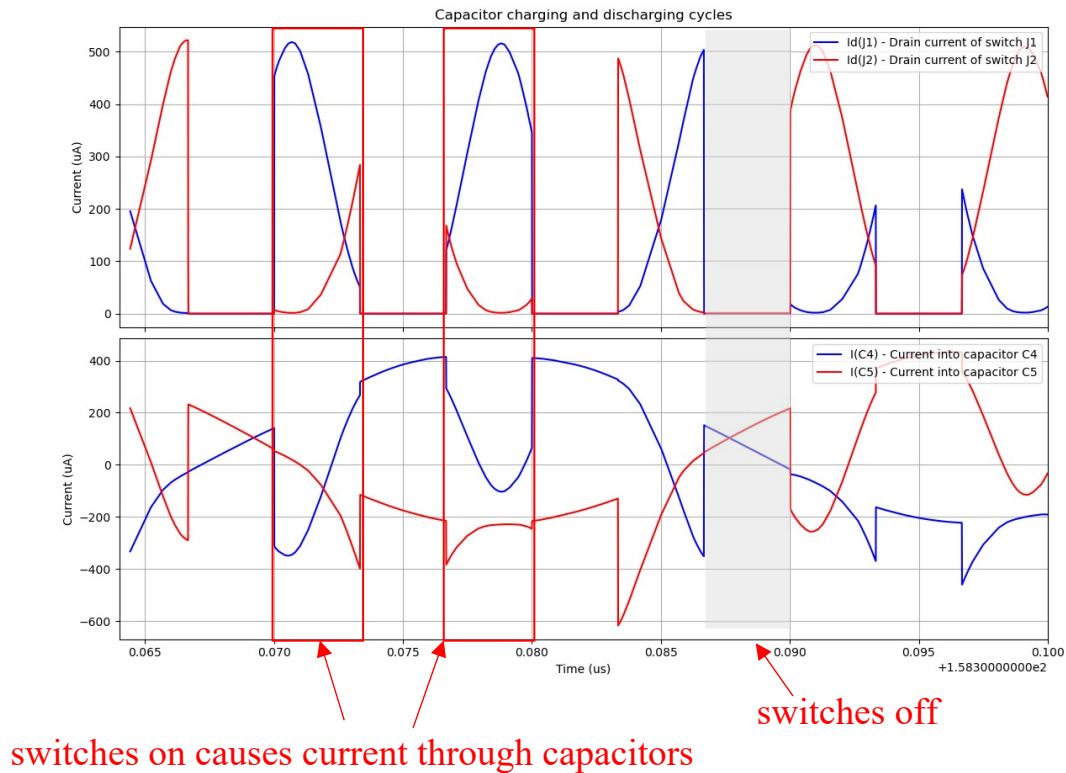
101. By invoking the differential symmetry of this portion of the circuit that was explained in the previous section, the preceding paragraph can be used to demonstrate that this circuit electrically couples the inverted information signal to a second capacitor.



DeMaw, FIG. 6.7 (partial, annotated)

102. DEMA-SIM-FIG. 4, below, shows the drain current through the first and second switching devices J1 and J2 (corresponding to Q1 and Q2,

respectively, in DeMaw Fig. 6.7), indicating that the switches electrically couple the information signal and inverted information signal to the first (C4) and second (C5) capacitors, respectively:



DEMAW-SIM-FIG. 4 (annotated)

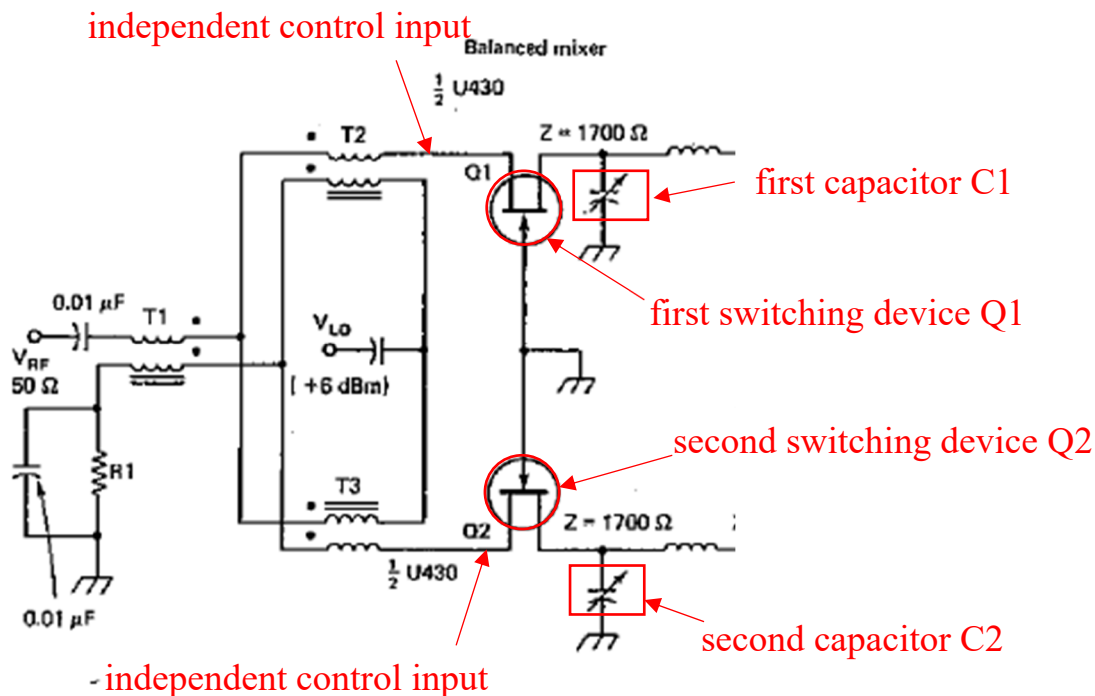
103. The switches are off when their drain currents are zero and on when their drain currents are non-zero. An example of one such off-period is annotated (gray) in DEMAW-SIM-FIG. 4. Examples of two such on-periods are also annotated in the figure. Specifically, the figure shows that the drain current of the first switching device J1 becomes non-zero when the switching device J1 is on, indicated by the red boxes surrounding portions of the waveform. The current in

the first capacitor C4 reacts when the first switching device is turned on, visibly influenced by the current through J1.

104. Likewise, DEMAW-SIM-FIG. 4 shows identical electrical coupling between the inverted information signal to the second capacitor C5 by turning on the second switching device J2.

18.4 (4) controlling a charging and discharging cycle of the first and second capacitors with first and second switching devices electrically coupled to the first and second capacitors, respectively; and

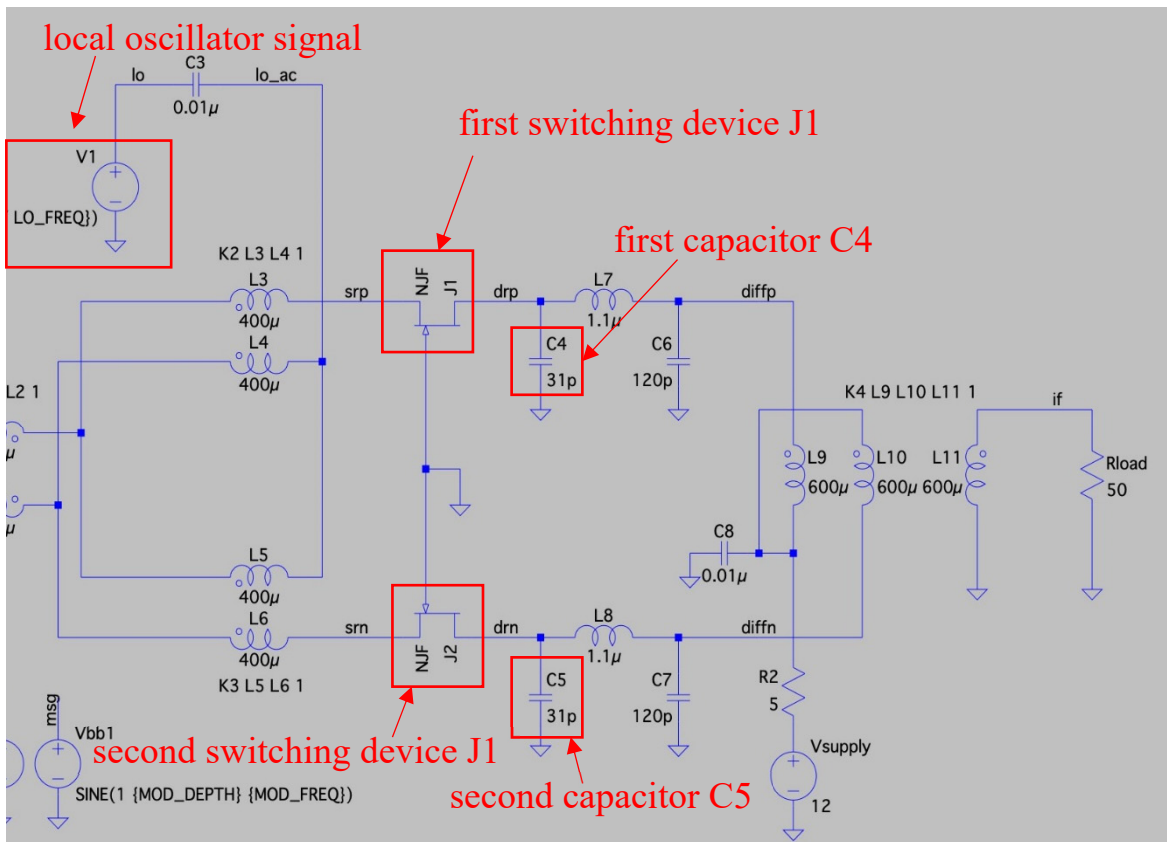
105. The DeMaw circuit includes a first switching device Q1 that controls the charging and discharging of the first capacitor C1 based on a control signal. The first switching device Q1 includes an independent control input (transistor source) and is controlled by a control signal based on V_{LO} , as shown in FIG. 6.7:



DeMaw, FIG. 6.7 (partial, annotated)

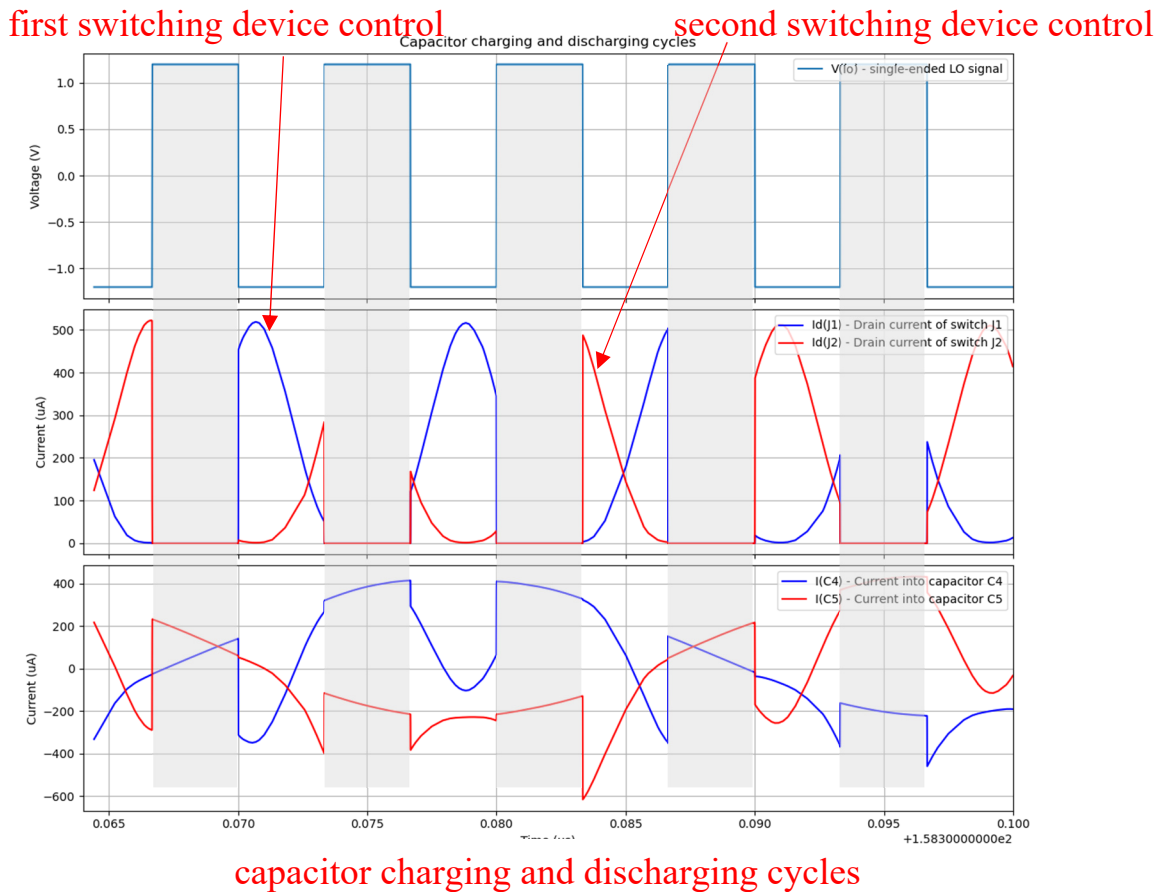
106. Likewise, the DeMaw circuit includes a second switching device Q2 that controls the charging and discharging of the second capacitor C2 based on a control signal. The second switching device Q2 includes an independent control input (transistor source) and is controlled by a control signal based on V_{LO} , as shown in FIG. 6.7, above.

107. DEMAW-SIM-FIG. 1 shows the simulation setup to demonstrate this claim. Specifically, it will be shown that the LO signal controls the periodic charging and discharging of first and second capacitors C4 and C5, respectively, through switching devices J1 and J2.



DEMAW-SIM-FIG. 1, (partial, annotated)

108. DEMAW-SIM-FIG. 5 shows the controlling of the charging and discharging cycles of the first and second capacitor by the first and second switching devices, respectively, where the open and close times of the switches are aligned with the low and high levels, respectively, of the LO signal. The grayed-out regions are aligned to intervals of time where the LO signal is high, and during these intervals no current flows through switches J1 or J2.

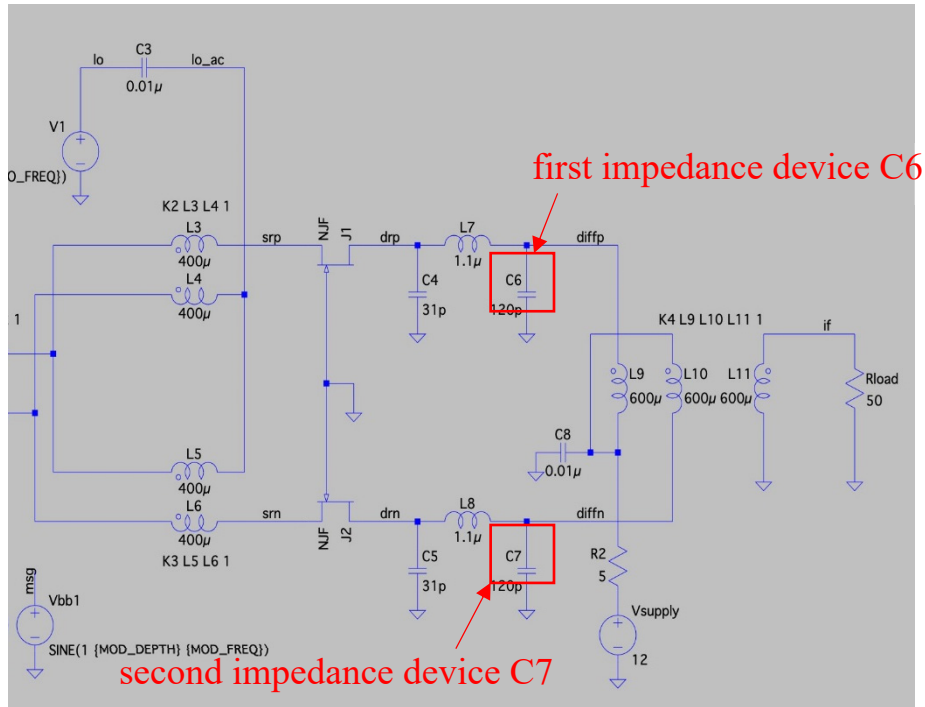


DEMAW-SIM-FIG. 4 (annotated)

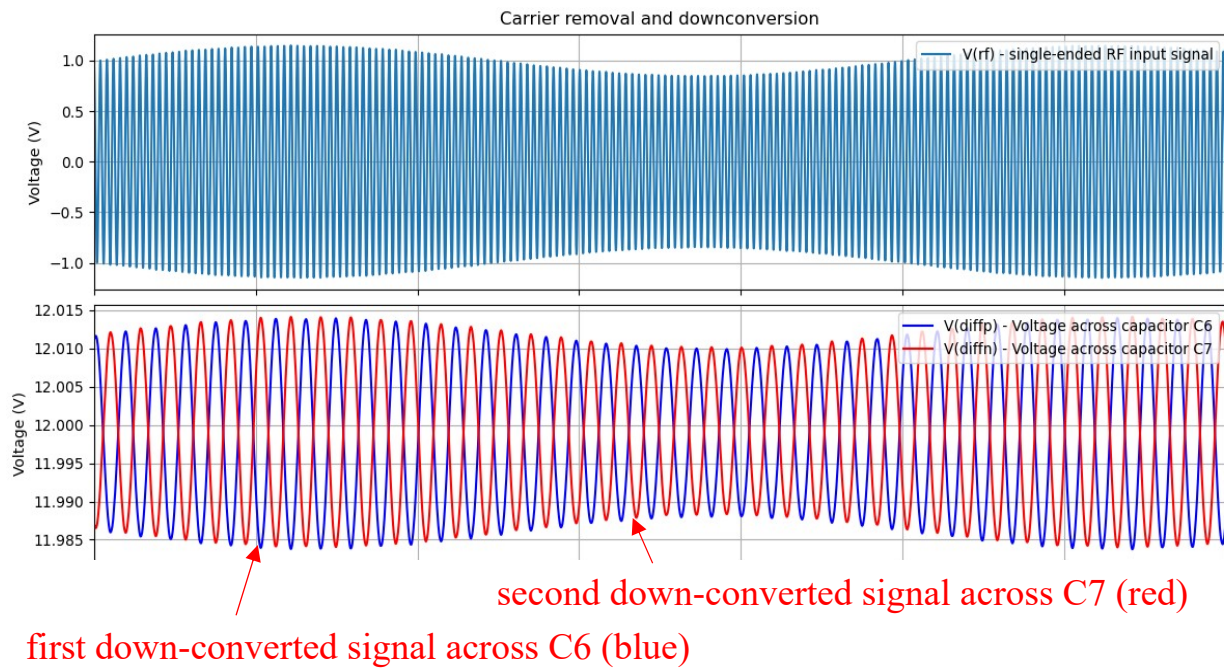
109. Because switch J1 and J2 are controlled by local oscillator V_{LO} , the charging and discharging occurs in cycles. These cycles occur sequentially, and thus, DeMaw's operation would satisfy TI's constructions. DeMaw's circuit structure already satisfies ParkerVision's constructions because "a first switching device [J1] controls a charging/discharging cycle of a first capacitor [C4]" and "a second switching device [J2] controls a charging/discharging cycle of a second capacitor [C5]." Plaintiff ParkerVision, Inc.'s Responsive Claim Construction Brief, 6:23-cv-00384, 2.

18.5 (5) performing a plurality of charging and discharging cycles of the first and second capacitors to generate first and second down-converted information signals across first and second impedance devices, respectively;

110. As already seen from simulation, the DeMaw circuit performs a plurality of charging and discharging cycles of the first and second capacitors, which are impedance devices under any construction. These first and second capacitors are coupled to first and second impedance devices capacitors C6 and C7, respectively, as shown in DEMAW-SIM-FIG. 1:



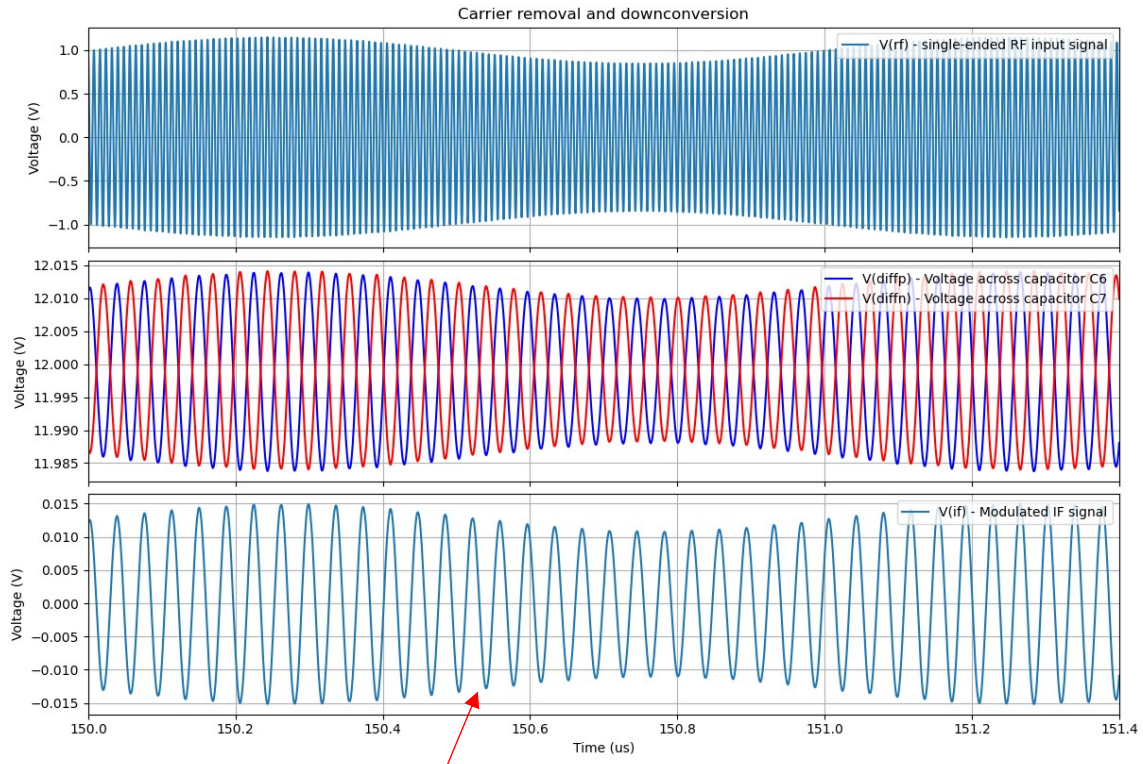
DEMAW-SIM-FIG. 1, (partial, annotated)



DEMAW-SIM-FIG. 5 (annotated)

111. As shown in DEMAW-SIM-FIG. 5 a first down-converted signal $V(\text{diffp})$ is generated across first capacitor C6 due to performing a plurality of charging and discharging cycles of the first capacitor C4. Likewise, a second down-converted signal $V(\text{diffn})$ is generated across second capacitor C7 due to performing a plurality of charging and discharging cycles of the second capacitor C5. As can be seen by DEMAW-SIM-FIG. 5, the first down-converted signal $V(\text{diffp})$ and the second down-converted signal $V(\text{diffn})$ are at a lower frequency than the RF input signal, as they have been translated to f_{IF} .

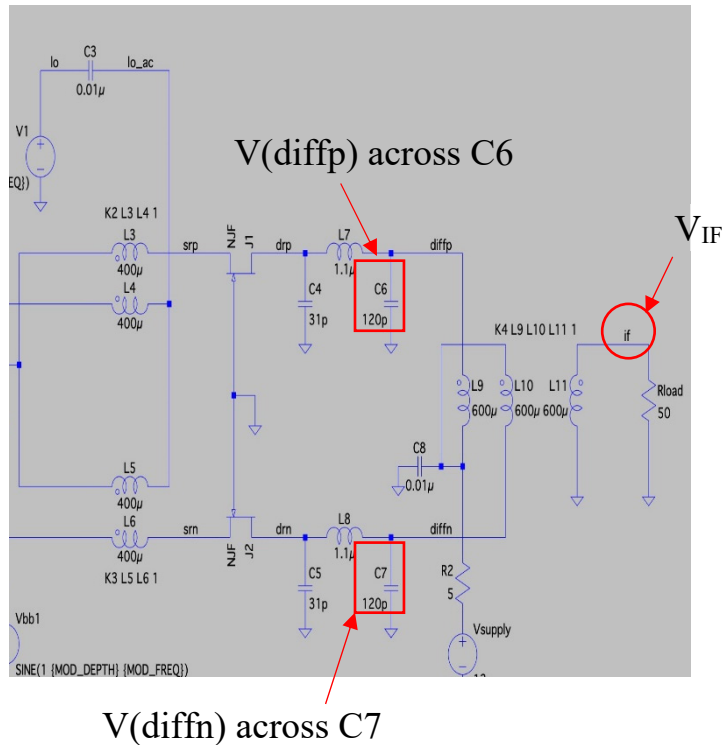
112. DeMaw also combines the first and second down-converted signals into a single IF signal $V(\text{if})$, via the differential to single-ended transformer as shown in DEMAW-SIM-FIG. 6:



V(if) – combined down-converted signal

DEMAW-SIM-FIG. 6

The points in the circuit corresponding to $V(diffp)$, $V(diffn)$, and $V(if)$ are shown in DEMAW-SIM-FIG. 1:



DEMAW-SIM-FIG. 1, (partial, annotated)

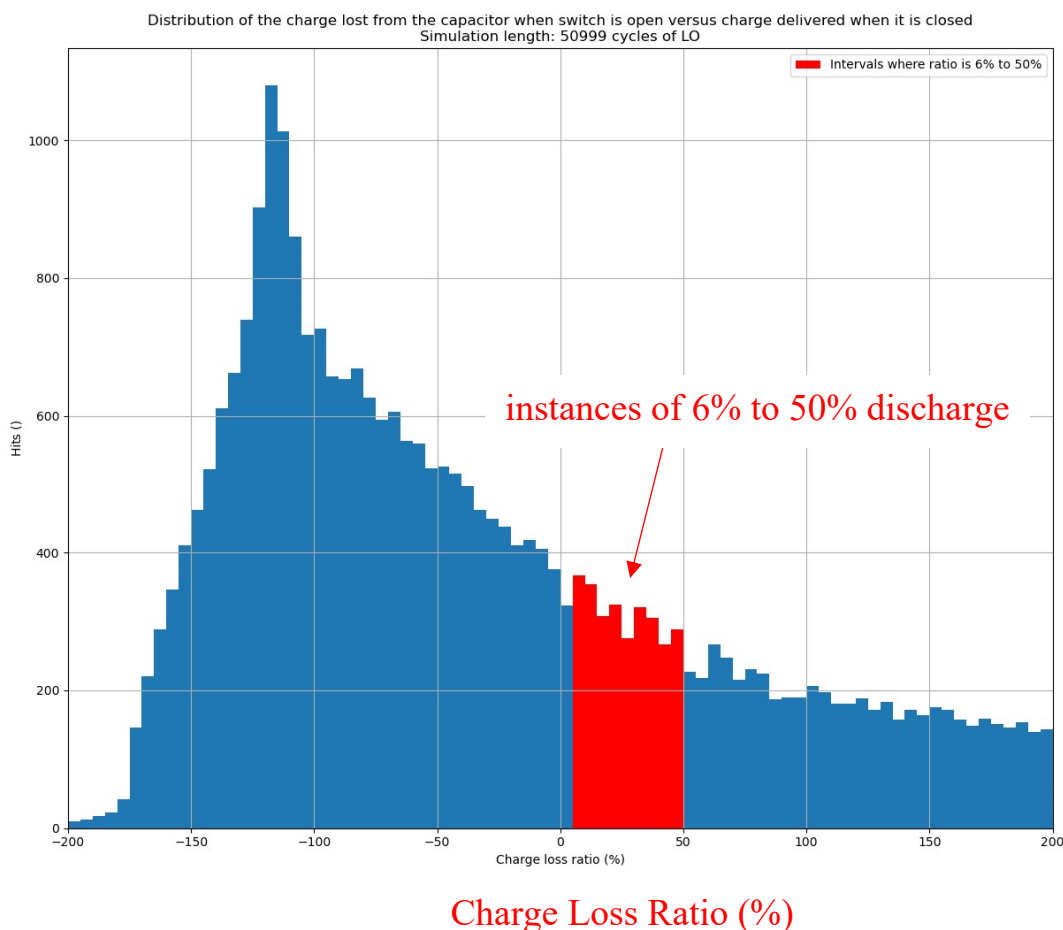
18.6 wherein the information signal is used to store a charge on the first capacitor when the first switching device is closed and the inverted information signal is used to store a charge on the second capacitor when the second switching device is closed.

113. As was already explained for claim limitation 18.3, the currents through switches J1 and J2 when closed are functions of their source voltages, $V(srp)$ and $V(srn)$, respectively. These voltages contain the information signal and inverted information signal, respectively. Therefore, the charge delivered to first and second capacitors C4 and C5 while switches J1 and J2 are closed are functions of the information signal and inverted information signal, respectively.

19. The method of claim 18, wherein the first capacitor discharges between six percent to fifty percent of the total charge stored therein during a period

of time that the first switching device is open, and wherein the second capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the second switching device is open.

114. DeMaw teaches claim 19. Specifically, using the transition edges of the LO signal, and the knowledge that the switch opening and closing is dictated by the LO signal amplitude, we can compute on a cycle-by-cycle basis the charge ratio described in claim 19. This ratio is collected for 50,999 simulation cycles and plotted as a histogram, shown in DEMAU-SIM-FIG. 7.



DEMAU-SIM-FIG. 7 (annotated)

It is evident that the DeMaw circuit generates a continuum of these ratios, many of which are within the 6% to 50% range specified in the claim.

20. The method of claim 18, wherein the first capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the second switching device is open.

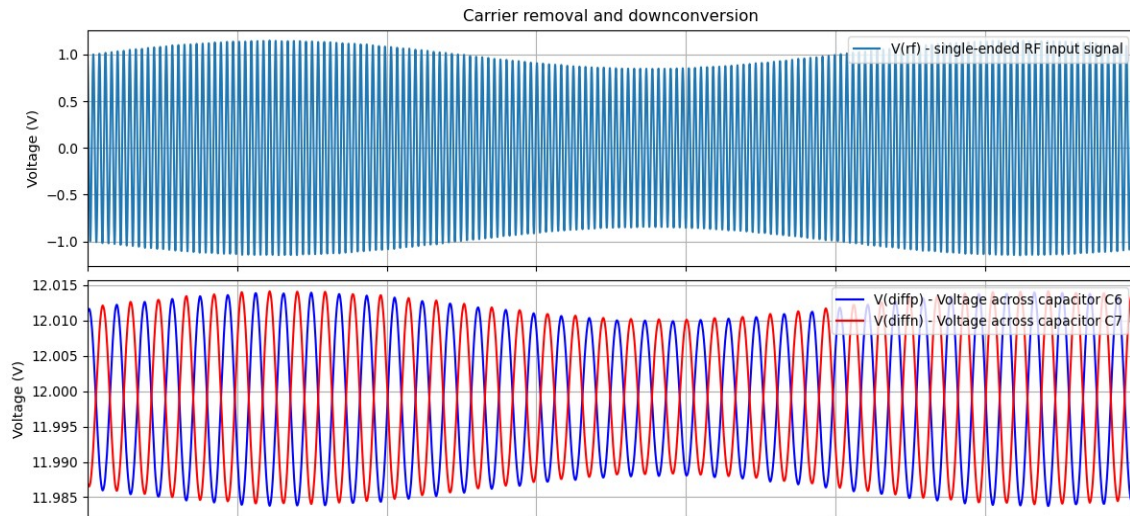
115. From DEMAW-SIM-FIG. 7, the histogram shows a continuum of occurrences of discharging ratio that includes the claim's 10-25% discharging rate.

21. The method of claim 18, wherein the first capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the second switching device is open.

116. From DEMAW-SIM-FIG. 7, the histogram shows a continuum of occurrences of discharging ratio that includes the claim's 15-30% discharging rate.

23. The method of claim 18, further comprising the step of removing a carrier signal from the first and second down-converted information signals.

117. DeMaw teaches claim 23. Specifically, DeMaw's balanced mixer receives an RF signal input that has a carrier frequency, and outputs an intermediate frequency, where the carrier frequency is removed. This removal of the carrier frequency from each of the first and second down-converted signals is illustrated by DEMAW-SIM-FIG. 5:



carrier frequency remove from first (blue) and second (red) down-converted signals

DEMAW-SIM-FIG. 5 (annotated)

As shown in the above plot, the RF input signal is a 123.102MHz AM-modulated carrier. The differential signal across the first and second impedance devices is a 26.898MHz IF signal with the same modulation as the input. Hence, it is shown that the input 123.102MHz carrier has been removed. A POSITA would have recognized that to fully recover the baseband signal, this mixer would be part of the first down-conversion stage in a superheterodyne receiver. Additionally, the claim is satisfied in that a carrier was removed from the first and second down-converted information signals.

B. GROUND 1B – the DeMaw-Taylor Combination Renders Claims 22-23 Obvious

1. The DeMaw and Taylor Combination

118. DeMaw describes a receiver that uses a balanced mixer for communications circuits that down-converts a radio frequency (RF) signal into an intermediate frequency (IF) signal. *See, e.g.*, DeMaw, 197. The DeMaw balanced mixer circuit does not down-convert the IF signal to baseband. In the combination, the IF signal of DeMaw is further down-converted to baseband by removing the carrier signal from the first and second down-converted (IF) signals, in a manner identical to that described by Tayloe.

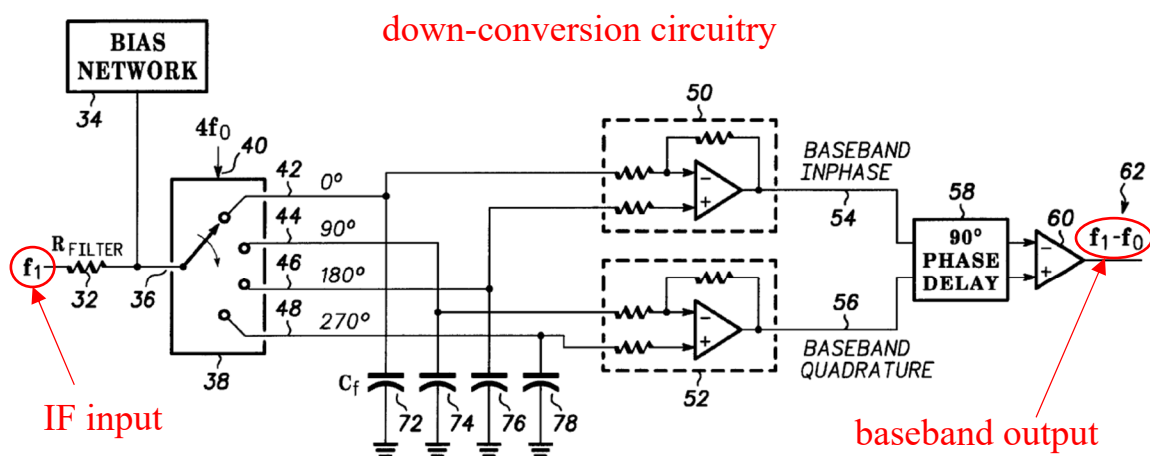
2. Motivation to Combine DeMaw with Tayloe

119. As I previously described, a POSITA would have understood that DeMaw's balanced mixer produces first and second down-converted signals at an intermediate frequency (IF). DeMaw, FIG. 6.7 (outputting V_{IF}). A POSITA would have understood that further circuitry would have been required to obtain a baseband signal from the IF signal. Therefore, a POSITA implementing DeMaw's balanced mixer would have sought out down-conversion circuitry to further down-convert the IF signal to baseband, like the circuitry in Tayloe.

120. DeMaw's balanced mixer outputs a single-ended IF output, produced by the combination of the first and second down-converted signals. A POSITA implementing DeMaw, therefore, would have sought a second down-converting circuit that was already configured to receive a single-ended IF input to produce a baseband signal, which is what Tayloe describes. Tayloe's down-conversion

circuitry “is applicable anywhere signals need to be converted to baseband, such as in the last stage of a superheterodyne receiver,” such as is the case for the output signal of DeMaw. Tayloe, 6:2-5.

121. The circuitry of Tayloe is reproduced below, which shows a single ended IF input and a baseband output:



30 **FIG. 3**

Tayloe, FIG. 3 (annotated)

Tayloe describes that, in operation, “an RF or IF signal f_1 is received at resistor 32.” Tayloe, 2:13-14 (emphasis added). Tayloe also explains that “the carrier signal frequency is exactly equal to f_0 .” *Id.*, 3:50-52; *see also id.*, 1:9-21

(describing local oscillator signal f_0 and that the signal of interest $f_1 - f_0$ is produced at baseband). The output of Tayloe’s down-conversion circuitry is a baseband signal. *See, e.g.*, Tayloe, 1:9-21, 1:65-67, 2:2-3, 2:65-67, 3:54-59, 4:1-8.

Therefore, a POSITA would have recognized that Tayloe provides a circuit that can receive the single-ended IF input from DeMaw and output a baseband signal.

122. A POSITA would have recognized that Tayloe provided benefits over other down-conversion circuit designs. For example, Tayloe's down-conversion circuitry addresses signal losses that occur in other designs during the down-conversion process. Tayloe, 1:35-42 (describing conversion loss from 6-8 dB). By contrast, Tayloe's circuitry exhibits less than 1 dB of conversion loss, which is a 6-7 dB improvement over other designs. Tayloe, 3:6-10. In addition, Tayloe's design has the ability to be configured for different bandwidth detection scenarios, exhibiting narrowband detection characteristics. Tayloe, 3:21-27. These advantages, in addition to Tayloe's single-ended input, provide multiple reasons for why a POSITA would be motivated to use Tayloe to down-convert DeMaw's IF signal to baseband.

123. A POSITA would have had a reasonable expectation of success using Tayloe's down-conversion circuitry to further down-convert DeMaw's IF signal to obtain a baseband signal. Tayloe describes experimental results that describe possible implementations of its circuitry. *See, e.g.*, Tayloe, 5:30-60. The experimental results are illustrative to a POSITA to configure Tayloe's down-conversion circuitry to obtain a baseband signal from DeMaw's IF signal.

3. Analysis

22. The method of claim 18, further comprising the step of amplifying the first and second down-converted information signals.

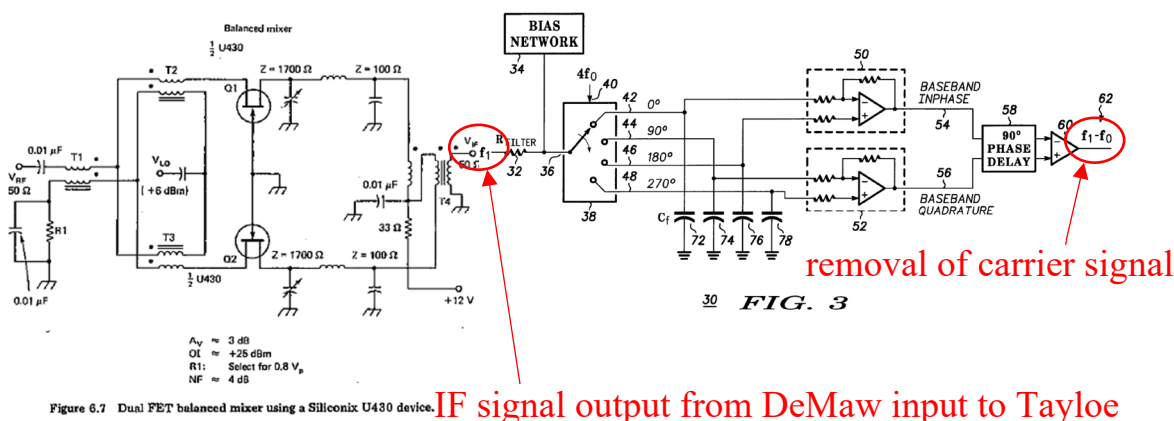
124. The DeMaw-Tayloe combination renders claim 22 obvious. In the combination, Tayloe amplifies the first and second down-converted information signals. For example, in Tayloe, the output of each capacitor represents the average value of the input signal during respective quarter waves of the period. Tayloe, 2:46-55. The in-phase outputs are input to a summing amplifier that amplifies the difference between the 0 and 180 degree signals to produce a baseband in-phase signal likewise, the quadrature outputs are input to a summing amplifier that amplifies the difference between the 90 and 270 degree signals to create a baseband quadrature signal. Tayloe, 2:56-67.

125. DeMaw outputs a singled ended IF signal that is representative of individual first and second down-converted signals. Tayloe receives the single-ended IF signal as an input and further down-converts it to baseband in-phase and base-band quadrature signals. Tayloe then amplifies each of the baseband in-phase and baseband quadrature signals. The amplification of the baseband in-phase signal, for example, is mathematically equivalent to amplification of the first down-converted signal because the components to the right of the switches in the DeMaw circuit, the components in Tayloe, and amplification are all linear operations, so their order can be interchanged without changing the behavior of the circuit to the extent that linearity holds. Likewise, the amplification of the

baseband quadrature signal, for example, is mathematically equivalent to the amplification of the second down-converted signal.

23. The method of claim 18, further comprising the step of removing a carrier signal from the first and second down-converted information signals.

126. The DeMaw-Taylor combination renders claim 23 obvious. In the combination, Tayloe's direct-conversion circuitry removes the carrier frequency from the first and second down-converted (IF) signals from DeMaw's balanced mixer circuit. The combined circuit is provided below in DeMaw, FIG. 6.7 and Tayloe, FIG. 3:



DeMaw, FIG. 6.7 with Tayloe, FIG. 3 (annotated).

In operation, Tayloe receives the IF signal from DeMaw at resistor 32. Tayloe, 2:13-14. The commutating switch 38 is controlled by a control signal $4f_0$, where f_0 is the carrier frequency. Tayloe, 2:15-27. The commutating switch 38 “remains closed at each of the four outputs for substantially 90 degrees at the frequency of

the input signal.” Tayloe, 2:27-32. During the time that commutating switch 38 is closed, charge builds up on a capacitor. Tayloe, 2:33-34. “Each of the capacitors functions as a separate integrator, each integrating a separate quarter wave of the input signal.” *Id.*, 2:41-45.

127. The output of each capacitor represents the average value of the input signal during respective quarter waves of the period. Tayloe, 2:46-55. The in-phase outputs are input to a summing amplifier that amplifies the difference between the 0 and 180 degree signals to produce a baseband in-phase signal. Likewise, the quadrature outputs are input to a summing amplifier that amplifies the difference between the 90 and 270 degree signals to create a baseband quadrature signal. Tayloe, 2:56-67. A POSITA would have recognized that such frequency down-conversion to (zero-frequency) baseband removes the carrier signal from the first and second down-converted information signals.

C. GROUND 2 – Macnally Renders Claims 18-23 Obvious

4. Analysis

18.P A method for down-converting an electromagnetic signal, comprising the steps of

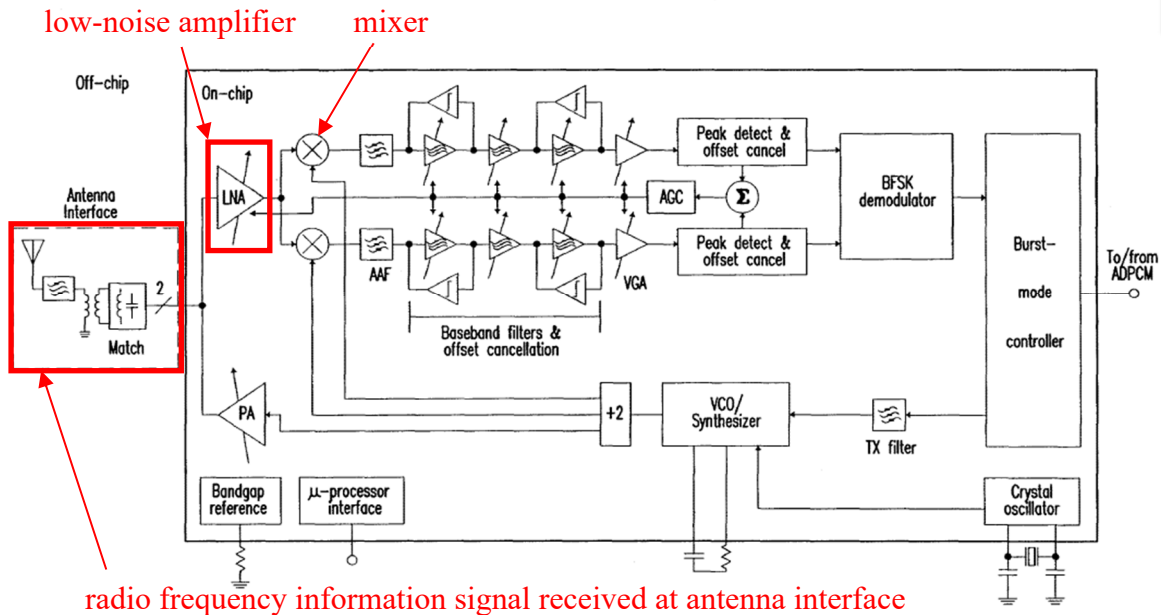
128. To the extent the preamble is limiting, Macnally describes a direct conversion transceiver circuit that when operated performs a set of steps, including down-converting an RF signal to baseband. *See, e.g.*, Macnally, 8:18-24 (describing the direct-conversion transceiver with RF circuits and baseband filters),

Abstract (describing a direct conversion transceiver), 1:5-6 (“This invention relates in general to communication systems, and more particularly to a single-chip CMOS direct-conversion transceiver.”), 2:19-25 (describing a single-chip CMOS direct-conversion transceiver that includes a receiver having a baseband filter). A POSITA would have understood that a direct-conversion transceiver includes circuitry that when operated performs down-conversion of an electromagnetic signal into a baseband signal.

18.1 (1) receiving an information signal;

129. Macnally teaches receiving an information signal (a radio frequency (RF) electromagnetic signal) at an antenna interface of the direct-conversion receiver. *See, e.g.*, Macnally, 10:20-24, FIG. 1. In operation, an RF information signal is received by Macnally’s antenna interface, as illustrated in FIG. 1, reproduced below:

FIG. 1



Macnally, FIG. 1 (annotated)

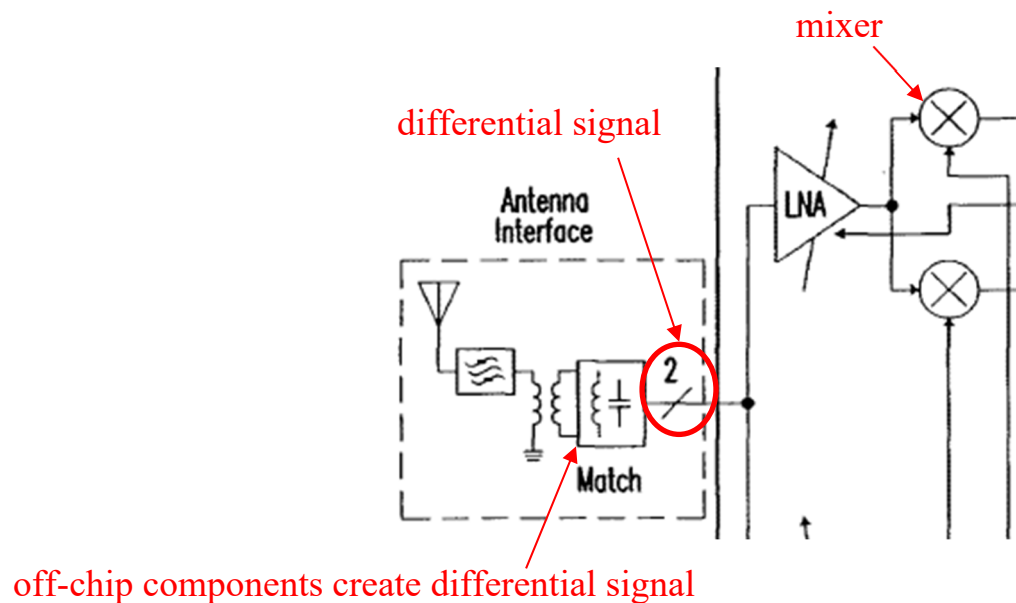
As explained by Macnally, the direct-conversion transceiver is “attached to the filter/antenna port of a radio transceiver.” Macnally, 10:22-24. In addition, Macnally explains that radio transceivers “usually require” a “Low Noise Amplifier or (LNA) for clear reception.” *Id.*, 10:25-26.

130. A POSITA reading Macnally would have understood that the direct-conversion transceiver, in operation, received an RF information signal at the antenna.

18.2 (2) inverting the information signal to generate an inverted information signal;

131. Macnally teaches inverting the information signal to generate an inverted information signal. As shown in FIG. 1 below, after the RF information

signal is received by the antenna, the information signal is passed through off-chip components, including an ISM band bandpass filter, a balun (which converts the signal to fully-differential form), and a matching network, the result of which is a fully-differential signal, indicated by the circled “2” in FIG. 1:

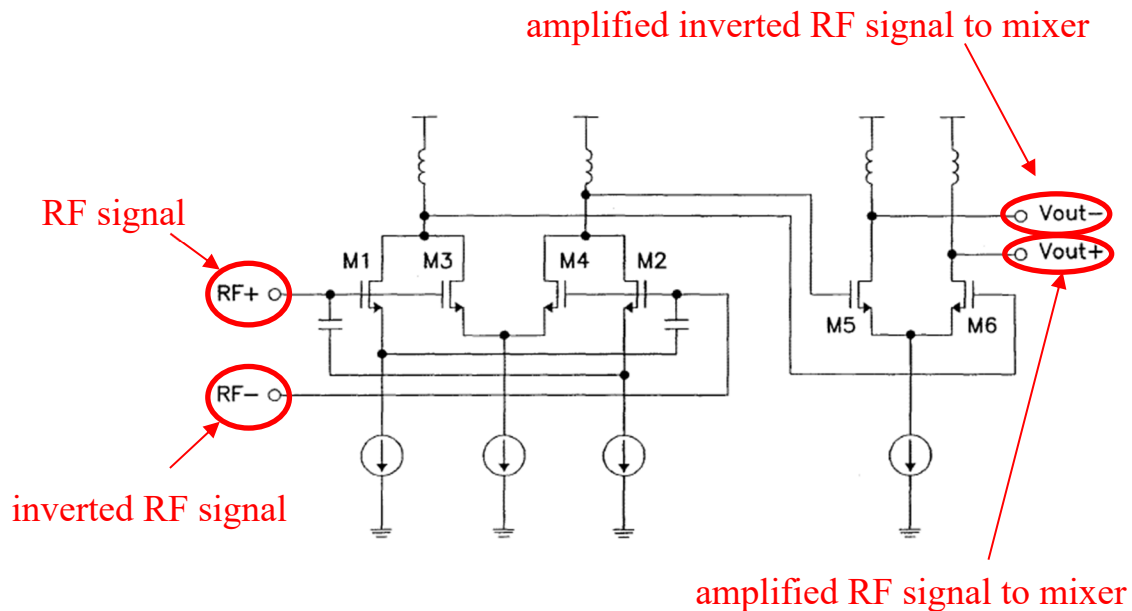


Macnally, FIG. 1 (annotated)

As noted by Macnally, a “fully-differential analog signal path minimizes supply and substrate noise coupling.” Macnally, 10:11-12. The creation of a fully differential signal involves “off-chip” circuitry that determines the difference between two single-ended signal values to create differential output, where the maximum values of the differential output are 180 degrees out of phase. A POSITA would have recognized that the creation of a fully differential signal includes inverting the single-ended signal received at the antenna.

132. That the received information signal is inverted is readily apparent from the positive and negative RF signals input to the LNA, as shown in FIG. 2, and into the mixer, shown in FIG. 3:

FIG. 2



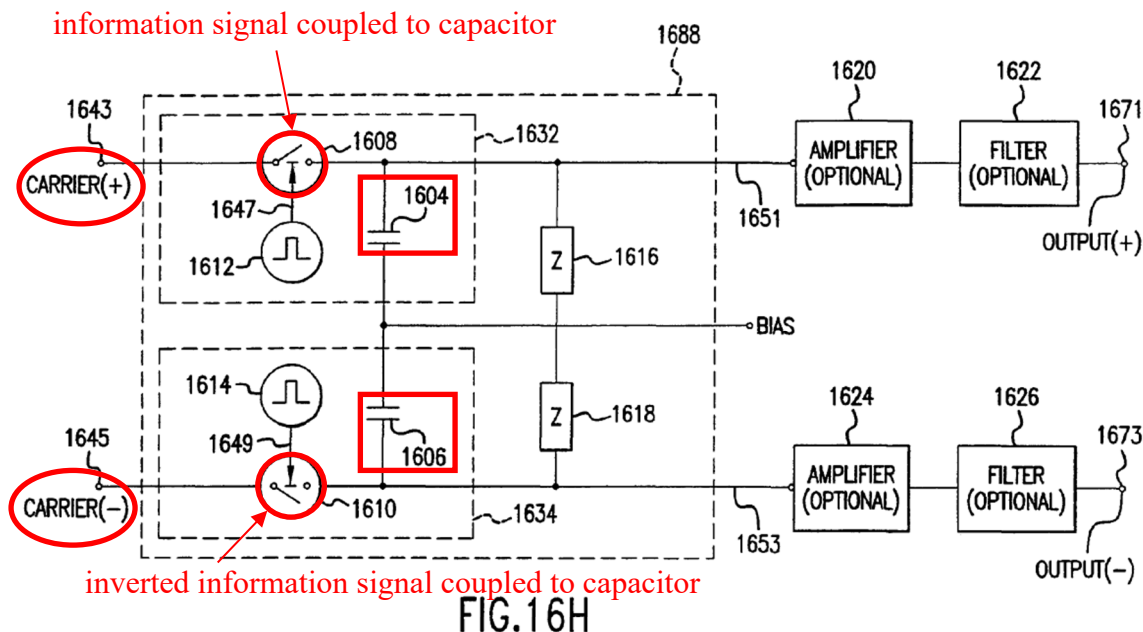
Macnally, FIG. 2 (annotated)

The LNA includes a first stage that “employs a capacitively cross-coupled input pair, M1 and M2, that provides both gain and impedance matching in parallel with a differential pair, M3 and M4, for additional gain.” Macnally, 12:3-6. “The second stage of the LNA 138 is also a differential pair.” *Id.*, 6-7.

mixer



device 1608.” *Id.* “Similarly, the inverted RF signal is coupled to capacitor 1606 through switching device 1610.” *Id.* FIG. 16H is shown below:



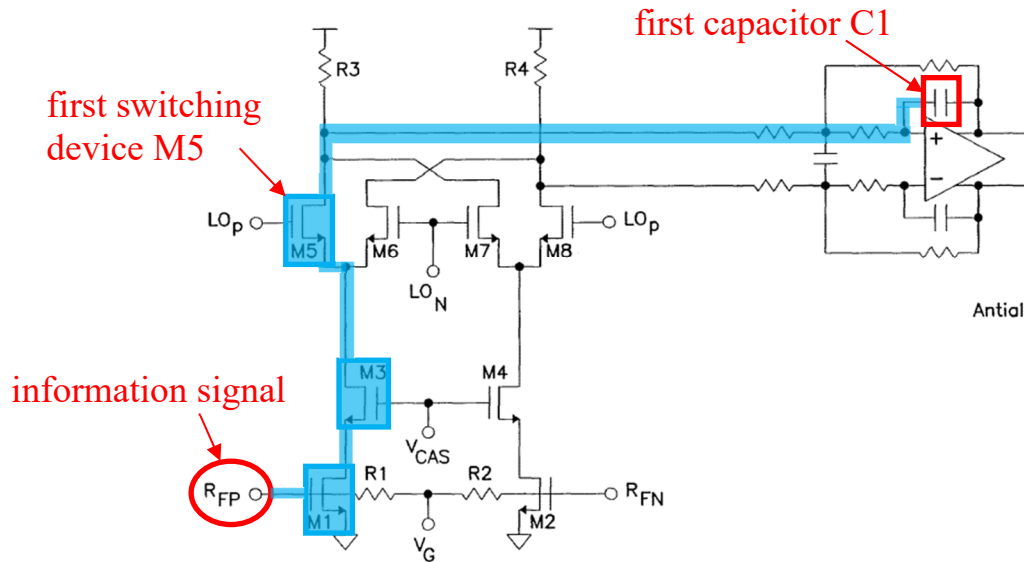
TI-1001, FIG. 16H (annotated)

Accordingly, electrically coupling the information signal to the first capacitor includes coupling the RF signal to a capacitor through a switching device.

134. Macnally’s mixer and antialiasing circuit includes a first capacitor electrically coupled to the information signal through the mixer. *See, e.g.,* Macnally, 12:19-20 (“The LO input transistors operate as switches that steer a process and temperature independent current.”). Specifically, the R_{FP} input is connected to capacitor C1 through first switching device M5 that is controlled by

the independent control input coupled to local oscillator LOp. This electrical coupling is shown in FIG. 3 below:

FIG. 3



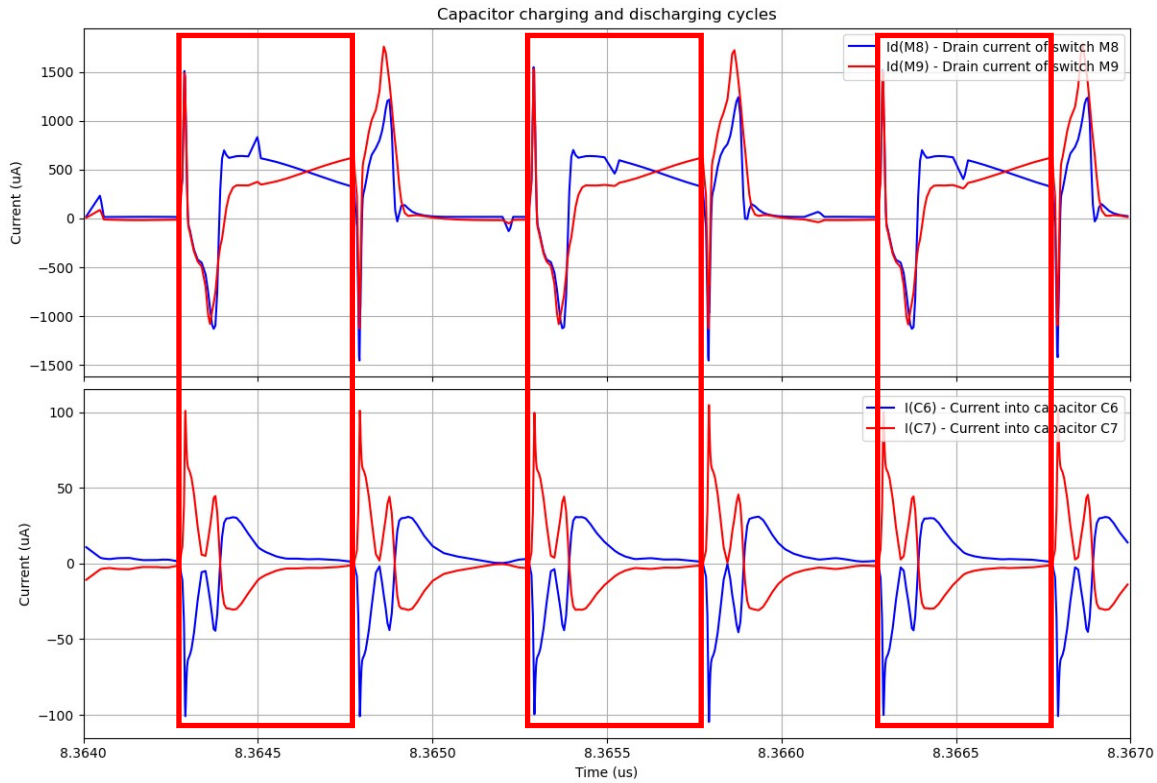
Macnally, FIG. 3 (partial, annotated)

The R_{FP} information signal input to the mixer is a version of the received information signal that is transformed and amplified. *See, e.g.*, Macnally, 8:18-25 (describing off-chip processes), 10:20-25 (describing low noise amplifier). However, the substance of the received information signal is preserved through those pre-processing steps. Specifically, the information carried by the information signal is preserved. *Id.* Thus, the input R_{FP} is the claimed information signal. *Id.* The R_{FP} input is connected to the first capacitor C1 through a set of transistors and resistors, as shown above in light blue.

Specifically, the inverted information signal R_{FN} is electrically coupled to the capacitor C2 through second switching device M8.

138. The inverted information signal R_{FN} is directly connected to the first capacitor C2 in the sense that, when switching device M8 is closed, there is a direct conductive path between the R_{FP} input and the second capacitor C2. In operation, when switching device M8 is closed (M8 being controlled by the control signal LOp), a conductive path is connects the inverted information signal R_{FN} input to the capacitor C2.

139. Electrically coupling the information signal to a first capacitor and the inverted information signal to a second capacitor is also shown by simulation:



MACNALLY-SIM-FIG. 2 (annotated)

It is the nature of mixers and modulated signals that the information (encoded in the modulated carrier) varies much more slowly than the carrier signal. In particular, the Macnally circuit operates at a 10x higher carrier frequency than DeMaw, for the same baseband signal bandwidth. Therefore, although it is not possible to see the information signal present in the capacitor current waveforms of figure MACNALLY-SIM-FIG. 2 due to the narrow time plotting range. This plot shows that switches M8 and M9 are indeed electrically coupled to capacitors C6 and C7, e.g., the clock feedthrough current spikes in the switch currents appear in the capacitor currents. That the information signal is electrically coupled is by deduction, as this circuit produces the downconverted information signal at its output, and the only path between input and output passes through switches M8 and M9.

18.4 (4) controlling a charging and discharging cycle of the first and second capacitors with first and second switching devices electrically coupled to the first and second capacitors, respectively; and

140. Macnally teaches controlling a charging and discharging cycle of the first capacitor with the first switching device electrically coupled to the first capacitor. *See, e.g.,* Macnally, 12:19-20 (“The LO input transistors operate as switches that steer a process and temperature independent current.”). The LO signal is a periodic waveform, and therefore the switches M5 and M8 are

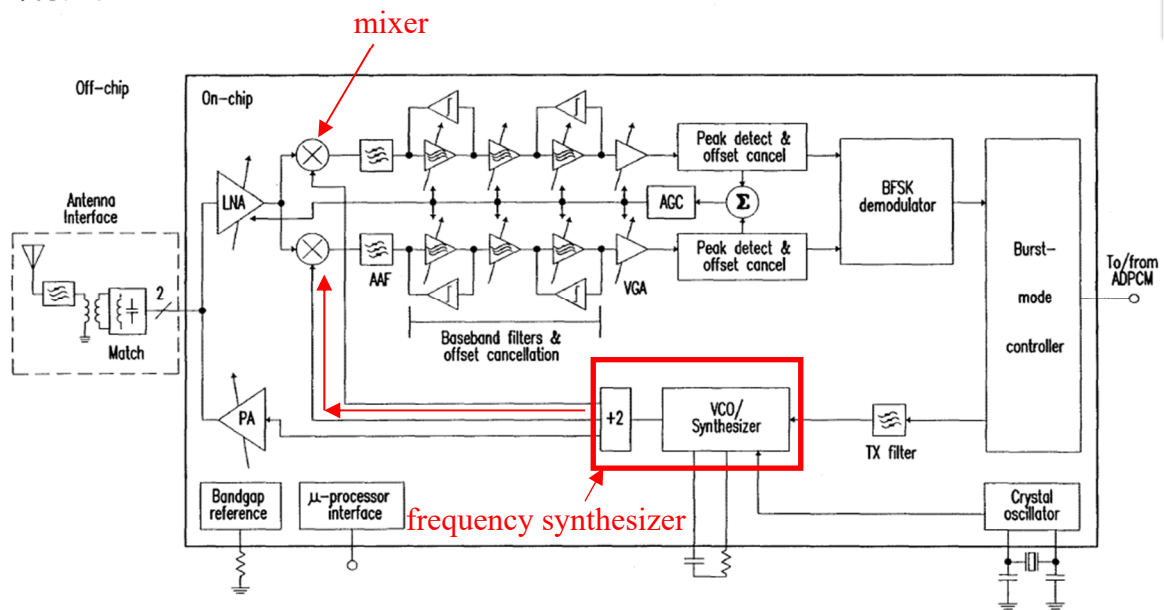
controlled cyclically. As shown in the previous claim limitation, switches M5 and M8 are electrically coupled to capacitors C1 and C2. Therefore, the information signal which is connected to the gates of M1 and M2 appear as a differential current at the drains of M1 and M2. Properly biased, the cascode devices M3 and M4 simply convey this current to the switches, which include M5 and M8. Therefore, not only do the switches M5 and M8 control charging and discharging cycles of capacitors C1 and C2, respectively, they do so with a current proportional to the information signal and inverted information signal, respectively. Each of M5 and M8 include their own independent control inputs, making them switching devices under any construction.

141. Because switches M5 and M8 are controlled by local oscillator signal LOp, the charging and discharging occurs in cycles. These cycles occur sequentially, and thus, Macnally's operation would satisfy TI's constructions. Macnally's circuit structure already satisfies ParkerVision's constructions because "a first switching device [M5] controls a charging/discharging cycle of a first capacitor [C1]." TI-1009, at 2. Transistors M5 and M8 have independent control inputs that cause them to complete (on) or break (off) a circuit, making them switching devices under any construction.

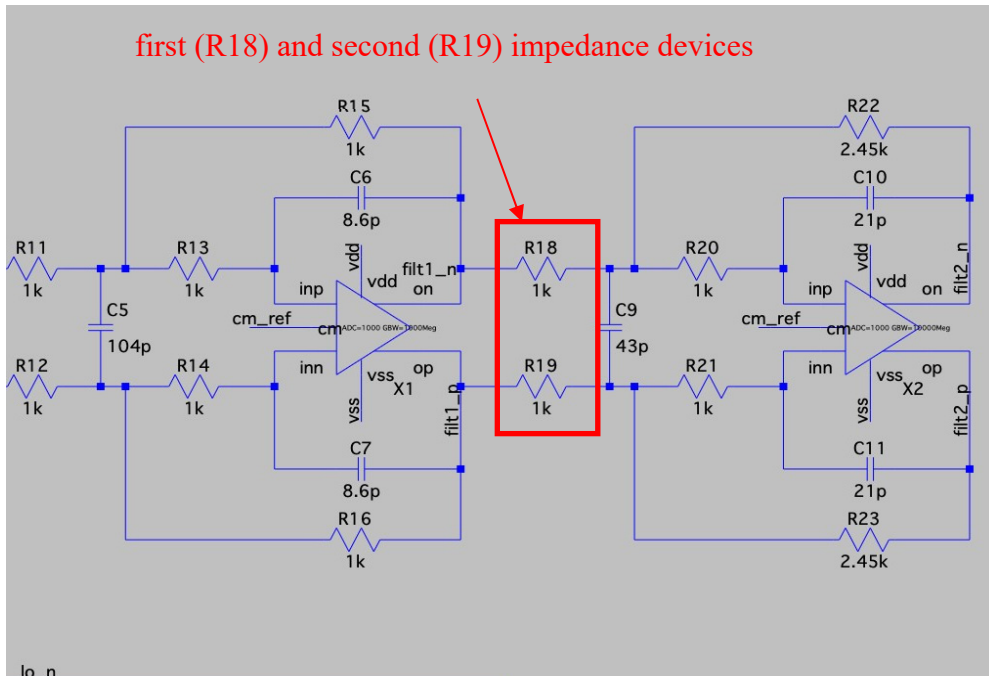
18.5 (5) performing a plurality of charging and discharging cycles of the first and second capacitors to generate first and second down-converted information signals across first and second impedance devices, respectively;

142. Macnally teaches element 18.5. Examining the block diagram shown below, it is understood that the signals LOp and LOn are generated by an on-chip frequency synthesizer. A POSITA would recognize that the design intention is to operate the mixers with a continuous sequence of clock cycles, thereby performing a plurality of the charging and discharging cycles previously described.

FIG. 1

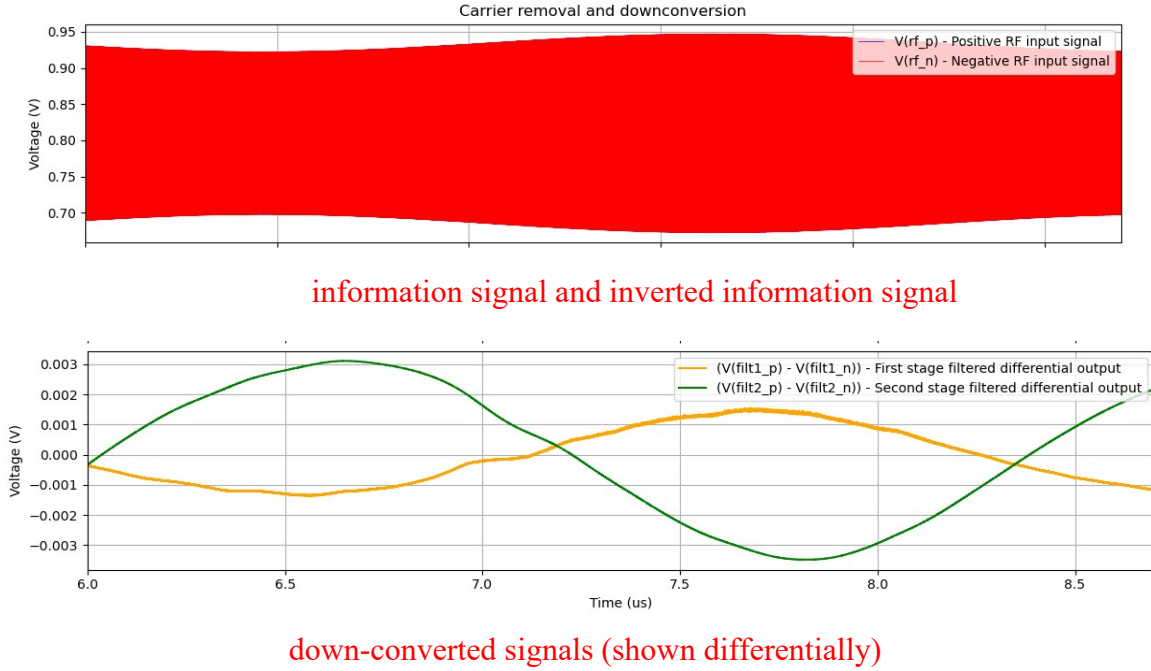


143. To demonstrate via simulation that this operation results in the down-converted information signal appearing across first and second impedance devices, we plot the differential signal across resistors R18 (first impedance device) and R19 (second impedance device), the locations of which are shown in MACNALLY-SIM-FIG. 1 below.



MACNALLY-SIM-FIG. 1 (partial, annotated)

144. The top pane of the waveform plot shows the input RF signal. Its frequency is so high relative to the down-converted information signal that the waveform appears as a solid band with this plot resolution. The trace $V(filt1_p)$ — $V(filt1_n)$ shows the down-converted information signal, with the carrier clearly removed.



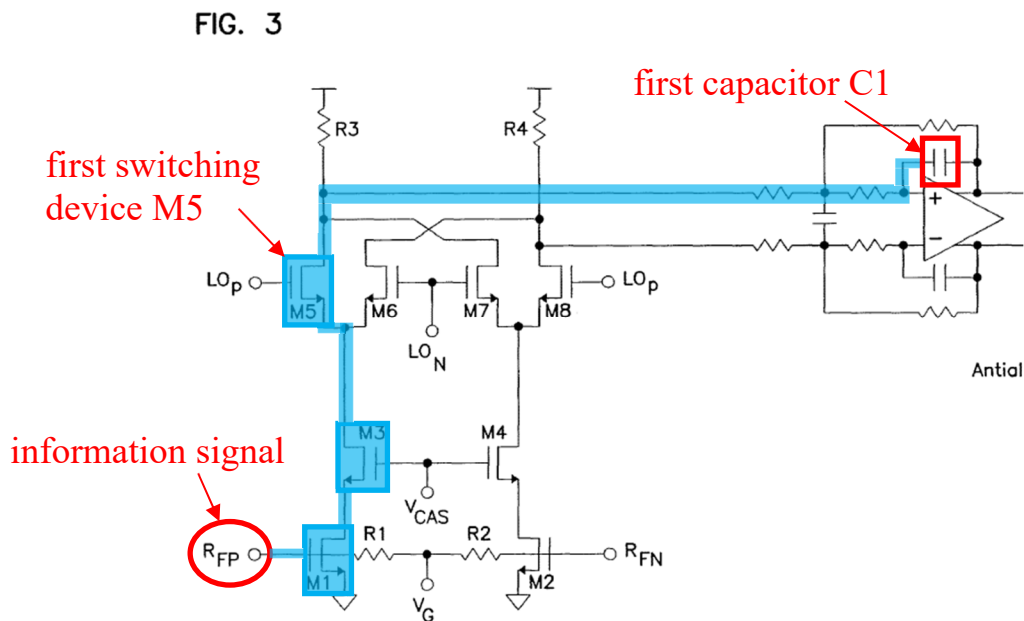
MACNALLY-SIM-FIG. 3 (annotated)

The use of differential signaling in this circuit would be recognized by a POSITA as advantageous to reject common-mode impairments of the mixer circuit, in particular clock leakage. Nevertheless, a POSITA would also recognize that if the Rauch biquad filter were properly designed, e.g., using the values presented in the analysis of Section VII-D, then the dominant signal components present across the individual impedance devices R18 and R19 would be the down-converted information signal and down-converted inverted information signal, respectively.

18.6 wherein the information signal is used to store a charge on the first capacitor when the first switching device is closed and the inverted information signal is used to store a charge on the second capacitor when the second switching device is closed.

145. *See, supra*, Ground 2, 18.3-4 (describing the operation of the Macnally circuit and how the operation of the switches causes charge to be stored on the capacitors).

146. In operation, when the first switching device M5 is closed, the RF information signal is directed to the capacitor C1 so that charge is stored on the first capacitor C1. This is shown by FIG. 3 below:

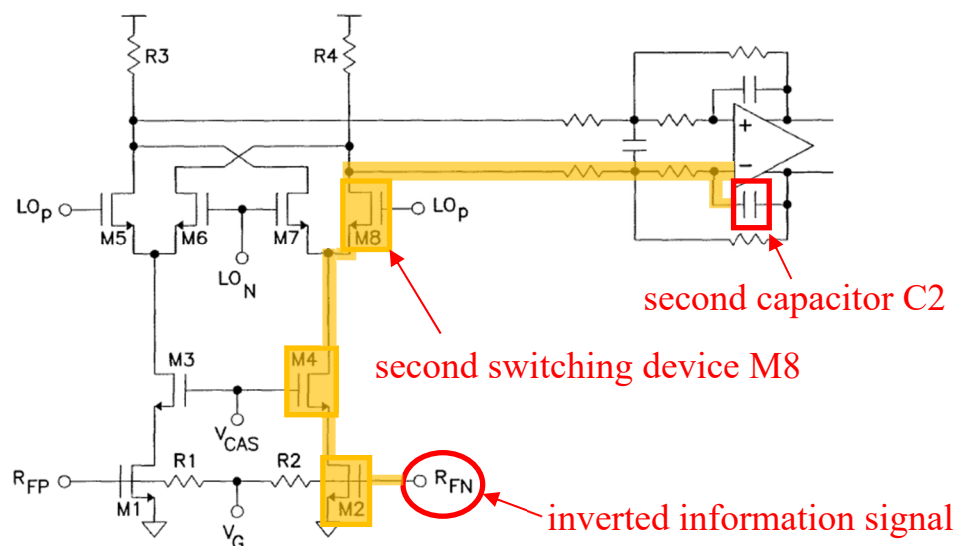


Macnally, FIG. 3 (annotated)

147. In operation, when switching device M5 is closed, the information signal R_{FP} is directed to the first capacitor C1, thereby delivering charge to the first capacitor C1. The first capacitor C1 stores the charge.

148. Likewise, Macnally's second capacitor that is electrically coupled to the inverted information signal, as shown in FIG. 3 below:

FIG. 3



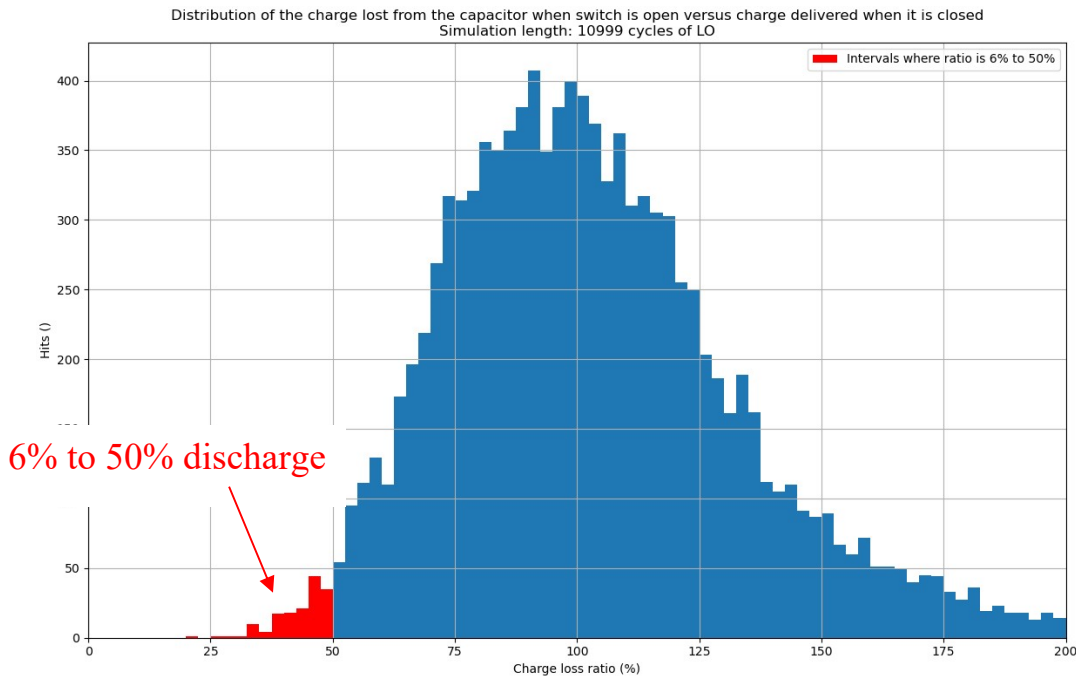
Macnally, FIG. 3 (partial, annotated)

During operation, when the switching device M8 is closed, the inverted information signal is directed to the capacitor C2, the inverted information signal delivering charge to the capacitor C2, which stores charge. Thus, in Macnally, the inverted information signal R_{FN} is used to store a charge on the second capacitor C2 when the second switching device M8 is closed.

19. The method of claim 18, wherein the first capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between six percent to fifty percent of the total charge stored therein during a period of time that the second switching device is open.

149. Macnally teaches claim 19. As the mixer switches are driven by the full-swing LO clock signal, it is possible to compute the intervals of time when the switches are open versus closed. The identical post-processing script that was used

to generate figure DEMA-W-SIM-FIG. 7 was used to generate MACNALLY-SIM-FIG. 4, below. The region of occurrences within the 6% to 50% range is marked in red.



MACNALLY-SIM-FIG. 4 (annotated)

20. The method of claim 18, wherein the first capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between ten percent to twenty-five percent of the total charge stored therein during a period of time that the second switching device is open.

150. There are a non-zero number of cycles where the charge loss ratio is just under 25%, which satisfies the claimed range of 10% to 25%.

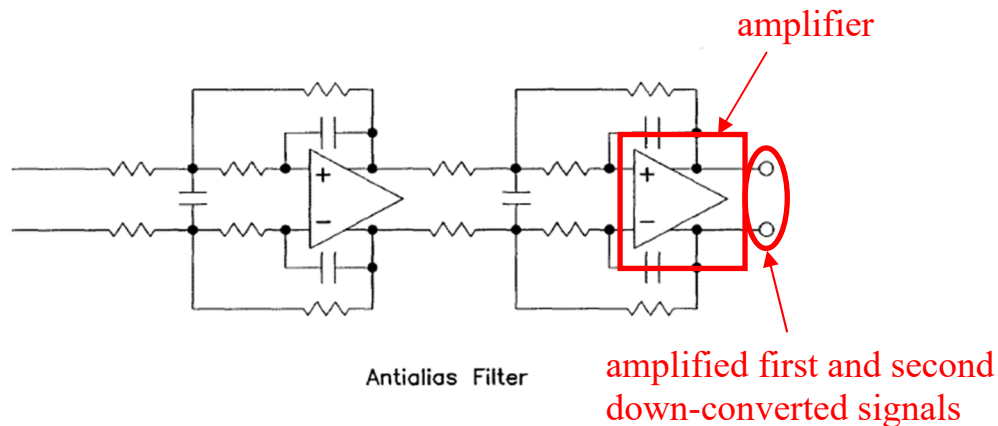
21. The method of claim 18, wherein the first capacitor discharges between fifteen percent to thirty percent of the total charge stored therein during a period of time that the first switching device is open, and wherein the second capacitor discharges between fifteen percent to thirty percent of the total

charge stored therein during a period of time that the second switching device is open.

151. There are a non-zero number of cycles where the charge loss ratio is 25%, which satisfies the claimed range of 15% to 30%.

22. The method of claim 18, further comprising the step of amplifying the first and second down-converted information signals.

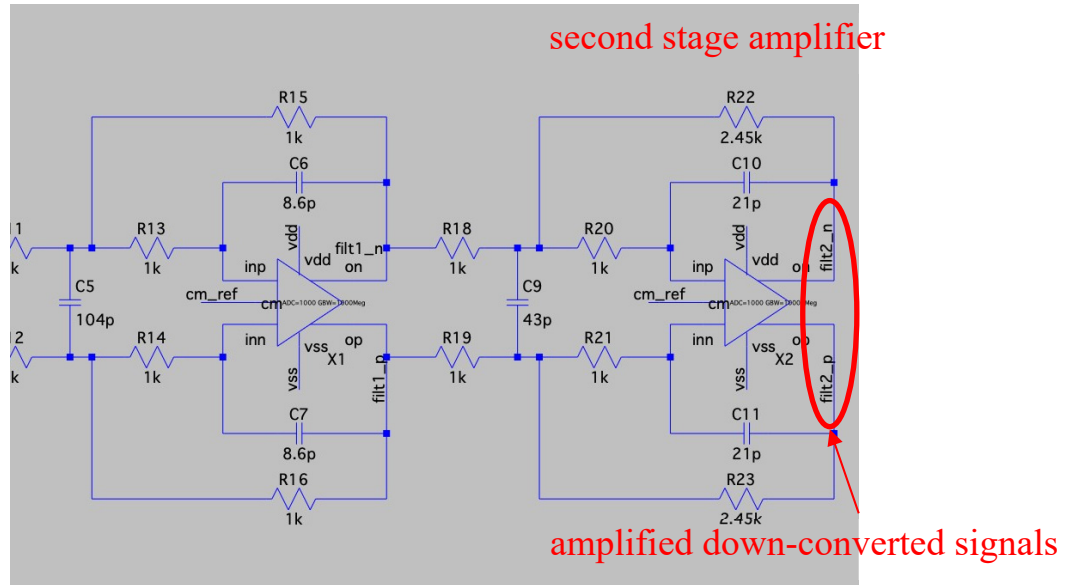
152. Macnally teaches the step of amplifying the first and second down-converted information signals. For example, as shown in FIG. 3, first and second down-converted information signals are differential signals, which are amplified by the two stages of the antialiasing filter as specified in the text of the patent, “Two biquad stages form the four-pole butterworth antialias filter with a nominal gain of 15.6dB...” Macnally, 12:22-26.



Macnally, FIG. 3 (partial, annotated)

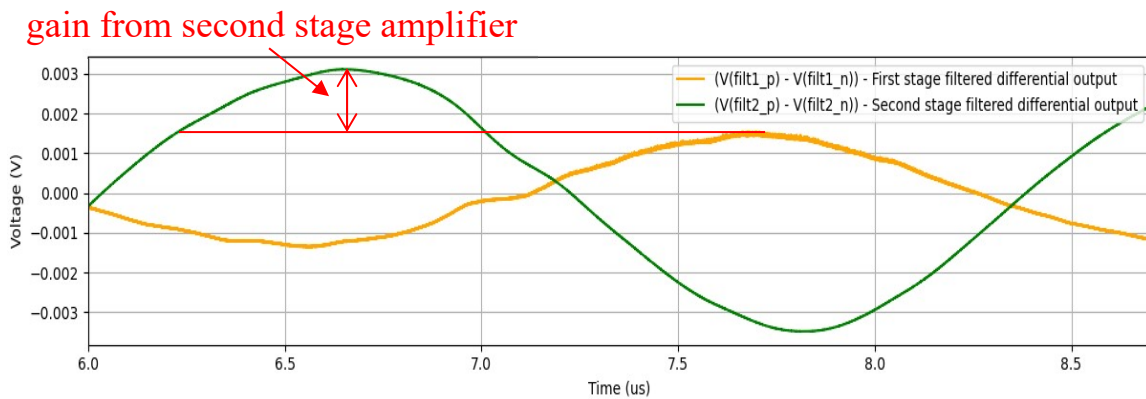
According to the analysis performed in this document (Section VII-D), each biquad stage delivers a portion of the total 15.6dB gain. Therefore, if the first and

second down-converted information signals are defined across resistors R18 and R19, or equivalently the differential first stage output, then the amplified information signals are defined at the output of the second stage.



MACNALLY-SIM-FIG. 1 (partial, annotated)

The simulation shows that in operation, the first and second down-converted signal are amplified by the second stage amplifier:

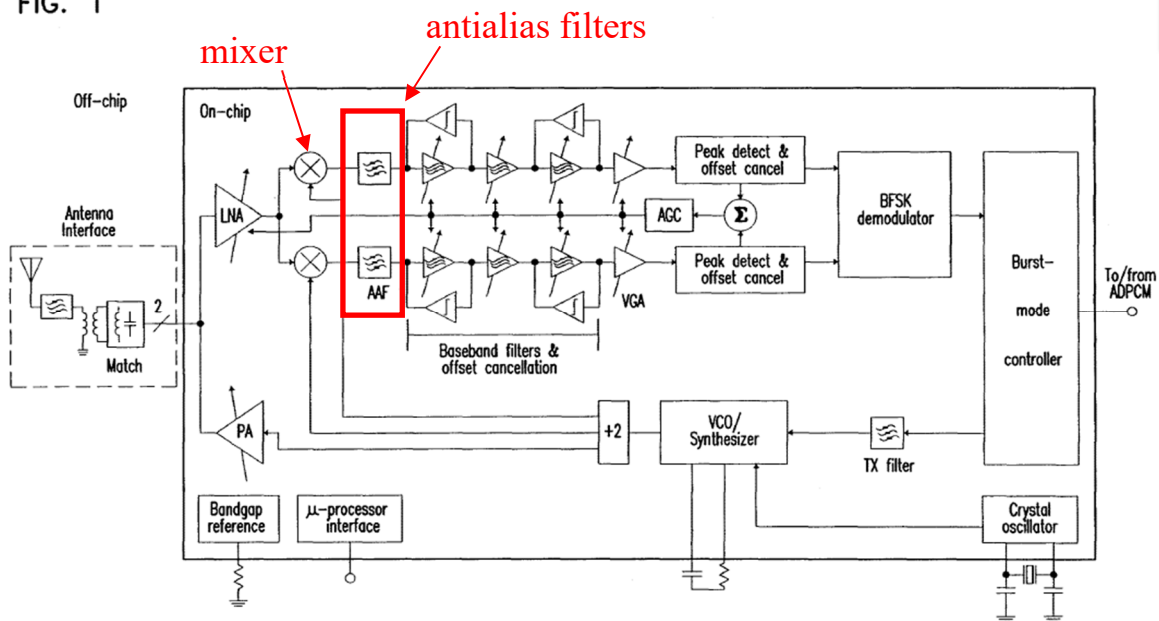


Macnally-SIM-FIG. 5

23. The method of claim 18, further comprising the step of removing a carrier signal from the first and second down-converted information signals.

153. Macnally teaches the step of removing a carrier signal from the first and second down-converted information signals. As mentioned above, Macnally is a direct-conversion transceiver, which a POSITA would have recognized as including circuitry that down-converts a radio frequency signal to baseband, which inherently removes the RF carrier. Furthermore recall that the direct-conversion transceiver circuitry includes antialias filters downstream of the mixer, as shown in FIG. 1:

FIG. 1



Macnally, FIG. 1 (annotated)

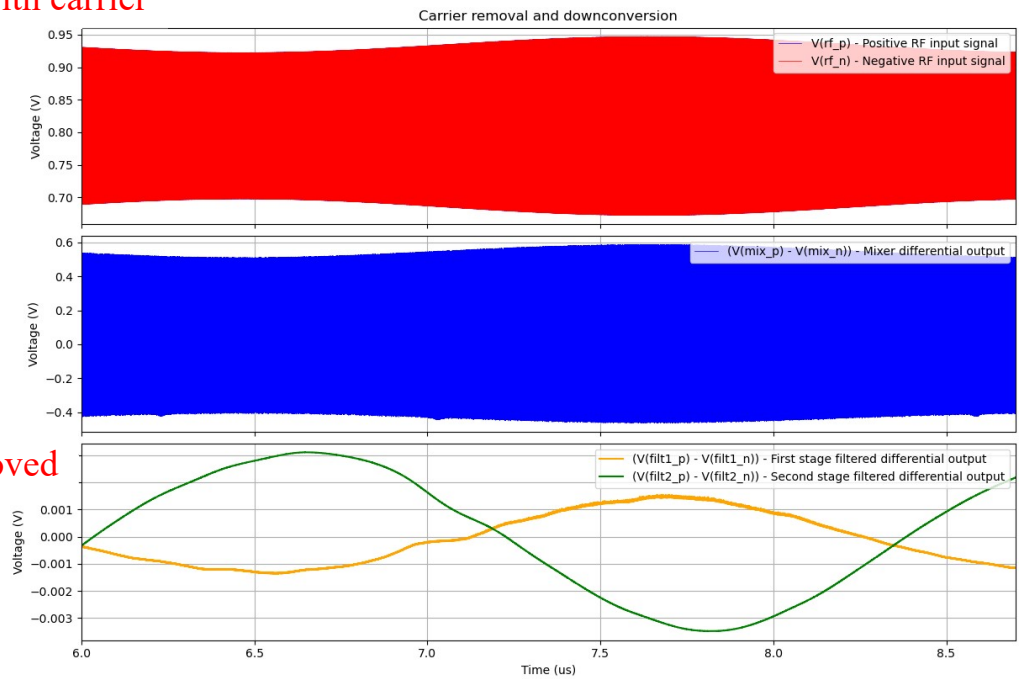
Therefore, even if some of the RF carrier were to leak into the outputs of the mixers as a result of non-ideal circuit behavior, the lowpass antialias filters would

remove it (because the cutoff frequency of the antialias lowpass filters is 2.4 MHz whereas the RF carrier frequency is 900 MHz).

154. In operation, the simulation results also show the removal of the carrier signal from the first and second down-converted signals:

RF signal with carrier

carrier removed



MACNALLY-SIM-FIG. 6

As can be seen by MACNALLY-SIM-FIG. 6, operation of the Macnally circuit down-converts the RF input signal and removes the carrier frequency (otherwise the bottom plot waveforms would show the same high-frequency “blur” that can be seen in the top-two plots).

XI. ADDITIONAL REMARKS

155. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

156. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code.

Dated: May 18, 2024

By: /Dr. Ian Galton/
Dr. Ian Galton

APPENDIX A

Ian Galton

Education

Brown University , Providence, RI	ScB in Electrical Engineering	1984
California Institute of Technology , Pasadena, CA	MS/PhD in Electrical Engineering	1989/1992

Employment

Professor of Electrical Engineering, University of California at San Diego , La Jolla, CA	7/02 – present
Associate Professor of Electrical Engineering, University of California at San Diego , La Jolla, CA	11/96 – 6/02
Assistant Professor of Electrical Engineering, University of California at Irvine , Irvine, CA	7/92 – 10/96
Design Engineer, Acuson, Inc. , Mountain View, CA	8/86 – 9/88
Design Engineer, Mead Data Central , Menlo Park, CA	2/85 – 8/86
Design Engineer, Mindset Corporation , Sunnyvale, CA	7/84 – 1/85

UCSD Research Overview

Ian Galton manages the Integrated Signal Processing Group at the University of California, San Diego (UCSD). The group develops enabling technology for highly-integrated, high-performance, low-cost, communication systems. The research involves the invention, development, analysis, and proof-of-principle integrated circuit (IC) implementation of key communication system blocks such as data converters and frequency synthesizers. The emphases of the research are on the development of new digital signal processing techniques and new digital-like analog circuits that exploit the strengths of advanced IC technology to mitigate the effects of non-ideal analog circuit behavior in mixed-signal and radio frequency ICs.

Selected Accomplishments, Activities, Honors, and Awards

- Author or co-author of ~100 scientific papers in peer-reviewed academic journals and conferences
- Inventor or co-inventor on ~22 U.S. Patents
Holder of the “Skyworks Endowed Chair in High Performance Communications Devices and Circuits”
- Fellow of the Institute of Electrical and Electronics Engineers (IEEE)
- Recipient of the 2015-2016 and the 2016-2017 UCSD Electrical and Computer Engineering Department “Best Graduate Teacher” award
- Co-recipient of the 2015 IEEE International Solid-State Circuits Conference (ISSCC) Lewis Winner Award
- Recipient of the Brown Engineering Alumni Medal, 2012
- Co-recipient of the 2008 IEEE Transactions on Circuits and Systems Darlington Award
- Co-recipient of the 2008 IEEE ISSCC Jack Kilby Award
- Member of the IEEE Solid-State Circuits Society Distinguished Lecturer Program, 2007-2010
- Organizer of the IEEE ISSCC Short Courses, 2007-2010
- Member of the IEEE ISSCC Technical Program Committee, 2005-2011
- Recipient of the 2005-2006 UCSD Electrical and Computer Engineering Department “Best Teacher Award”
- IEEE Solid State Circuits Society Administrative Committee, 2002-2005
- IEEE Circuits and Systems Society Board of Governors, 1998-2001, 2002-2005
- Editor-in-Chief of the *IEEE Transactions on Circuits and Systems II: Analog to Digital Signal Processing*, 2001-2003
- Board of Directors of innoCOMM Wireless, San Diego, CA, through its 2001 purchase by National Semiconductor Corporation
- Technical consultant and/or Technical Advisory Board member for several semiconductor and communications companies
- Instructor in over 80 industry-oriented short courses on the design of data converters, PLLs, and wireless transceivers at IEEE conferences and through Mead Education
- Recipient of the California Institute of Technology Charles Wilts PhD Thesis Prize, 1992

2023

H. Tan, A. Paulk, B. Stedelin, D. Cleary, C. Nerison, Y. Tchoue, E. C Brown, A. Bourhis, S. Russman, J. Lee, K. Tonsfeldt, J. C Yang, H. Oh, Y. Ro, K. Lee, M. Ganji, I. Galton, D. Siler, S. Han, K. Collins, S. Ben-Haim, E. Halgren, S. Cash, S. Dayeh, A. Raslan, “Intraoperative application and early experience with novel high-resolution, high-channel-count thin-film electrodes for human microelectrocorticography,” in *Journal of Neurosurgery*, vol. 1, Sept. 2023.
S. Kim and I. Galton, “Adaptive Cancellation of Inter-Symbol Interference in High-Speed Continuous-Time DACs,” in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 11, pp. 4309-4322, Nov. 2023.

[\[PDF\]](#)

P. Asbeck et al., “Integrated Circuits for Wireless Communications: Research Activities at the University of California, San Diego: Circuits Research for Wireless Communications at the University of California, San Diego,” in *IEEE Microwave Magazine*, vol. 24, no. 5, pp. 30-44, May 2023.

[\[PDF\]](#)

2022

E. Helal, A. I. Eissa and I. Galton, “DTC Linearization via Mismatch-Noise Cancellation for Digital Fractional- N PLLs,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 69, no.12, pp. 4993-5006, Dec. 2022.

[\[PDF\]](#)

Y. Tchoue, A. Bourhis, D. Cleary, B. Stedelin, J. Lee, K. Tonsfeldt, E. Brown, D. Siler, A. Paulk, J. Yang, H. Oh, Y. Ro, K. Lee, S. Russman, M. Ganji, I. Galton, S. Ben-Haim, A. Raslan, and S. Dayeh, “Human Brain Mapping With Multithousand-Channel PtNRGrids Resolves Spatiotemporal Dynamics,” *Science Translational Medicine*, vol. 14, issue 628, Jan. 2022.

J. Remple, A. Panigada, and I. Galton, “An ISI Scrambling Technique for Dynamic Element Matching Current-Steering DACs,” *IEEE Journal of Solid State-Circuits*, vol. 57, no. 2, pp. 465-479, Feb. 2022.

[\[PDF\]](#)

2021

E. Alvarez-Fontecilla, E. Helal, A. I. Eissa, and I. Galton, “Spectral Breathing and its Mitigation in Digital Fractional- N PLLs,” *IEEE Journal of Solid State-Circuits*, vol. 56, no. 10, pp. 3191-3201, Oct. 2021.

[\[PDF\]](#)

E. Helal, E. Alvarez-Fontecilla, A. I. Eissa, and I. Galton, “A Time Amplifier Assisted Frequency-to-Digital Converter Based Digital Fractional- N PLL,” *IEEE Journal of Solid State-Circuits*, vol. 56, no.9, pp. 2711-2723, Sept. 2021.

[\[PDF\]](#)

E. Alvarez-Fontecilla, A. I. Eissa, E. Helal, C. Weltin-Wu and I. Galton, “Delta-Sigma FDC Enhancements for FDC-Based Digital Fractional- N PLLs,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 3, pp. 965-974, March 2021.

[\[PDF\]](#)

2020

D. Kong and I. Galton, “MSE Analysis of a Multi-Loop LMS Pseudo-Random Noise Canceller for Mixed-Signal Circuit Calibration,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 9, pp. 3084-3098, Sept. 2020.

[\[PDF\]](#)[\[ADDITIONAL MATERIAL\]](#)[\[CORRECTION\]](#)

2019

A. Rovinski, C. Zhao, K. Al-Hawaj, P. Gao, S. Xie, C. Torng, S. Davidson, A. Amarnath, L. Vega, B. Veluri, A. Rao, T. Ajayi, J. Puscar, S. Dai, R. Zhao, D. Richmond, Z. Zhang, I. Galton, C. Batten, M. B. Taylor and R. G. Dreslinski, “Evaluating Celerity: A 16-nm 695 Giga-RISC-V Instructions/s Manycore Processor With Synthesizable PLL,” *IEEE Solid-State Circuits Letters*, vol. 2, no. 12, pp. 289–292, Dec. 2019.

[\[PDF\]](#)

A. Rovinski, C. Zhao, K. Al-Hawaj, P. Gao, S. Xie, C. Torng, S. Davidson, A. Amarnath, L. Vega, B. Veluri, A. Rao, T. Ajayi, J. Puscar, S. Dai, R. Zhao, D. Richmond, Z. Zhang, I. Galton, C.

Batten, M. B. Taylor and R. G. Dreslinski, “A 1.4 GHz 695 Giga RISC-V Inst/s 496-Core Manycore Processor With Mesh On-Chip Network and an All-Digital Synthesized PLL in 16nm CMOS,” *Symposium on VLSI Circuits (VLSIC)*, 2019.

[\[PDF\]](#)

D. Kong and I. Galton, “Subsampling Mismatch Noise Cancellation for High-Speed Continuous-Time DACs,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 8, pp. 2843–2853, Aug. 2019.

[\[PDF\]](#)

D. Kong, K. Rivas-Rivera and I. Galton, “A 600 MS/s DAC with over 87dB SFDR and 77dB peak SNDR Enabled by Adaptive Cancellation of Static and Dynamic Mismatch Error,” *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2219–2229, Aug. 2019.

[\[PDF\]](#)

I. Galton and C. Weltin-Wu, “Understanding Phase Error and Jitter: Definitions, Implications, Simulations, and Measurement,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 1, pp. 1–19, Jan. 2019.

[\[PDF\]](#)

2018

E. Alvarez-Fontecilla, C. Venerus and I. Galton, “Multi-Rate DEM With Mismatch-Noise Cancellation for DCOs in Digital PLLs,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 10, pp. 3125–3137, Oct. 2018.

[\[PDF\]](#)

D. Kong and I. Galton, “Adaptive Cancellation of Static and Dynamic Mismatch Error in Continuous-Time DACs,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 2, pp. 421–433, Feb. 2018.

[\[PDF\]](#)

2017

T. Ajayi, K. Al-Hawaj, A. Amarnath, S. Dai, S. Davidson, P. Gao, G. Liu, A. Lotfi, J. Puscar, A. Rao, A. Rovinski, L. Salem, N. Sun, C. Torng, L. Vega, B. Veluri, X. Wang, S. Xie, C. Zhao, R. Zhao, C. Batten, R. G. Dreslinski, I. Galton, R. K. Gupta, P. P. Mercier, M. Srivastava, M. B. Taylor and Z. Zhang, “Celerity: An Open-Source RISC-V Tiered Accelerator Fabric,” *Symp. on High Performance Chips (Hot Chips)*, 2017.

[\[SLIDES\]](#)

E. Familier and I. Galton, “Second and Third-Order Successive Requantizers for Spurious Tone Reduction in Low-Noise Fractional- N PLLs,” *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, 2017, pp. 1–4.

[\[PDF\]](#)[\[SLIDES\]](#)

J. Remple and I. Galton, “The Effects of Inter-Symbol Interference in Dynamic Element Matching DACs,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 1, pp. 14–23, Jan. 2017.

[\[PDF\]](#)[\[CORRECTION\]](#)

2016

C. Venerus, J. Remple, and I. Galton, “Simplified Logic for Tree-Structure Segmented DEM Encoders,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 11, pp. 1029–1033, Nov. 2016.

[\[PDF\]](#)

E. Familier and I. Galton, “Second and Third-Order Noise Shaping Digital Quantizers for Low Phase Noise and Nonlinearity-Induced Spurious Tones in Fractional- N PLLs,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 6, pp. 836–847, Jun. 2016.

[\[PDF\]](#)

2015

C. Weltin-Wu, G. Zhao, and I. Galton, “A Highly-Digital Frequency Synthesizer Using Ring-Oscillator Frequency-to-Digital Conversion and Noise Cancellation,” *IEEE International Solid-State Circuits Conference (ISSCC)*, 2015, pp. 1–3.

[\[PDF\]](#) [\[SLIDES\]](#) **Lewis Winner Award for Outstanding Paper**

C. Weltin-Wu, G. Zhao, and I. Galton, “A 3.5 GHz Digital Fractional- N PLL Frequency

Synthesizer Based on Ring Oscillator Frequency-to-Digital Conversion,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 2988–3002, Dec. 2015.

[\[PDF\]](#)

C. Weltin-Wu, E. Familier, and I. Galton, “A Linearized Model for the Design of Fractional- N Digital PLLs Based on Dual-Mode Ring Oscillator FDCs,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 8, pp. 2013–2023, Aug. 2015.

[\[PDF\]](#)

C. Venerus and I. Galton, “Quantization Noise Cancellation for FDC-Based Fractional- N PLLs,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 12, pp. 1119–1123, Dec. 2015.

[\[PDF\]](#)[\[CORRECTION\]](#)

C. Venerus and I. Galton, “A TDC-Free Mostly-Digital FDC-PLL Frequency Synthesizer With a 2.8–3.5 GHz DCO,” *IEEE Journal of Solid-State Circuits*, vol. 50, no. 2, pp. 450–463, Feb. 2015.

[\[PDF\]](#)[\[CORRECTION\]](#)

2013

C. Venerus and I. Galton, “Delta-Sigma FDC Based Fractional- N PLLs,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1274–1285, May 2013.

[\[PDF\]](#)

G. Taylor and I. Galton, “A Reconfigurable Mostly-Digital Delta-Sigma ADC With a Worst-Case FOM of 160 dB,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 4, pp. 983–995, Apr. 2013.

[\[PDF\]](#)

N. Rakuljic and I. Galton, “Suppression of Quantization-Induced Convergence Error in Pipelined ADCs With Harmonic Distortion Correction,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 3, pp. 593–602, Mar. 2013.

[\[PDF\]](#)

E. Familier, C. Venerus, and I. Galton, “A Class of Quantizers With DC-Free Quantization Noise and Optimal Immunity to Nonlinearity-Induced Spurious Tones,” *IEEE Transactions on Signal Processing*, vol. 61, no. 17, pp. 4270–4283, Sep. 2013.

[\[PDF\]](#)

E. Familier and I. Galton, “A Fundamental Limitation of DC-Free Quantization Noise With Respect To Nonlinearity-Induced Spurious Tones,” *IEEE Transactions on Signal Processing*, vol. 61, no. 16, pp. 4172–4180, Aug. 2013.

[\[PDF\]](#)

2012

G. Taylor and I. Galton, “A Reconfigurable Mostly-Digital Delta-Sigma ADC With a Worst-Case FOM of 160dB,” *Symposium on VLSI Circuits (VLSIC)*, 2012, pp. 166–167.

[\[PDF\]](#) [\[SLIDES\]](#)

2011

K. J. Wang and I. Galton, “A Discrete-Time Model for the Design of Type-II PLLs With Passive Sampled Loop Filters,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 58, no. 2, pp. 264–275, Feb. 2011.

[\[PDF\]](#)[\[CORRECTION\]](#)

2010

G. Taylor and I. Galton, “A Mostly-Digital Variable-Rate Continuous-Time Delta-Sigma Modulator ADC,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 12, pp. 2634–2646, Dec. 2010.

[\[PDF\]](#)

G. Taylor and I. Galton, “A Mostly-Digital Variable-Rate Continuous-Time ADC Delta-Sigma Modulator,” *IEEE International Solid-State Circuits Conference (ISSCC)*, 2010, pp. 298–299.

[\[PDF\]](#) [\[SLIDES\]](#)

N. Rakuljic and I. Galton, “Tree-Structured DEM DACs with Arbitrary Numbers of Levels,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 57, no. 2, pp. 313–322, Feb. 2010.

[\[PDF\]](#)

I. Galton, “Why Dynamic-Element-Matching DACs Work,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 57, no. 2, pp. 69–74, Feb. 2010.

[\[PDF\]](#)

2009

A. Panigada and I. Galton, "A 130mW 100MS/s Pipelined ADC with 69dB SNDR Enabled by Digital Harmonic Distortion Correction," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2009, p. 162–163,163a.

[\[PDF\]](#) [\[SLIDES\]](#)

A. Panigada and I. Galton, "A 130 mW 100 MS/s Pipelined ADC With 69 dB SNDR Enabled by Digital Harmonic Distortion Correction," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, pp. 3314–3328, Dec. 2009.

[\[PDF\]](#)

2008

K. J. Wang, A. Swaminathan, and I. Galton, "Spurious Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4 GHz Fractional- N PLL," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2787–2797, Dec. 2008.

[\[PDF\]](#)

K. J. Wang, A. Swaminathan, and I. Galton, "Spurious-Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4GHz Fractional- N PLL," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2008, pp. 342–618.

[\[PDF\]](#) [\[SLIDES\]](#) **Jack Kilby Award for Outstanding Student Paper**

K. L. Chan, J. Zhu, and I. Galton, "Dynamic Element Matching to Prevent Nonlinear Distortion From Pulse-Shape Mismatches in High-Resolution DACs," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 9, pp. 2067–2078, Sep. 2008.

[\[PDF\]](#)

K. L. Chan, N. Rakuljic, and I. Galton, "Segmented Dynamic Element Matching for High-Resolution Digital-to-Analog Conversion," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 11, pp. 3383–3392, Dec. 2008.

[\[PDF\]](#)

2007

A. Swaminathan, K. J. Wang, and I. Galton, "A Wide-Bandwidth 2.4GHz ISM-Band Fractional- N PLL with Adaptive Phase-Noise Cancellation," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2007, pp. 302–604.

[\[PDF\]](#) [\[SLIDES\]](#)

A. Swaminathan, K. J. Wang, and I. Galton, "A Wide-Bandwidth 2.4 GHz ISM Band Fractional- N PLL With Adaptive Phase Noise Cancellation," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2639–2650, Dec. 2007.

[\[PDF\]](#)

A. Swaminathan, A. Panigada, E. Masry, and I. Galton, "A Digital Requantizer With Shaped Requantization Noise That Remains Well Behaved After Nonlinear Distortion," *IEEE Transactions on Signal Processing*, vol. 55, no. 11, pp. 5382–5394, Nov. 2007.

[\[PDF\]](#)

S. Pamarti, J. Welz, and I. Galton, "Statistics of the Quantization Noise in 1-Bit Dithered Single-Quantizer Digital Delta-Sigma Modulators," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 3, pp. 492–503, Mar. 2007.

[\[PDF\]](#)

S. Pamarti and I. Galton, "LSB Dithering in MASH Delta-Sigma D/A Converters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 54, no. 4, pp. 779–790, Apr. 2007.

[\[PDF\]](#)

K. L. Chan, J. Zhu, and I. Galton, "A 150MS/s 14-bit Segmented DEM DAC with Greater than 83dB of SFDR Across the Nyquist band," *IEEE Symposium on VLSI Circuits (VLSIC)*, 2007, pp. 200–201.

[\[PDF\]](#)

2006

J. Rode, A. Swaminathan, I. Galton, and P. M. Asbeck, "Fractional- N Direct Digital Frequency Synthesis with a 1-Bit Output," *IEEE MTT-S International Microwave Symposium Digest*, 2006, pp. 415–418.

[\[PDF\]](#)

A. Panigada and I. Galton, "Digital Background Correction of Harmonic Distortion in Pipelined ADCs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 53, no. 9, pp. 1885–1895, Sep. 2006.

[PDF] **Darlington Best Paper Award**

K. L. Chan and I. Galton, "A 14b 100MS/s DAC with Fully Segmented Dynamic Element Matching," *IEEE International Solid State Circuits Conference (ISSCC)*, 2006, pp. 2390–2399.

[PDF] [SLIDES]

2005

M. Y. Li, I. Galton, L. E. Larson, and P. M. Asbeck, "Nonlinearity Estimation and Spectral Regrowth Prediction of Power Amplifiers Using Correlation Techniques," *The IEEE Annual Conference Wireless and Microwave Technology*, 2005, pp. 170–173.

[PDF]

J. L. Ceballos, I. Galton, and G. C. Temes, "Stochastic Analog-to-Digital Conversion," *48th Midwest Symposium on Circuits and Systems*, 2005, p. 855–858 vol. 1.

[PDF]

2004

S. Ye and I. Galton, "Techniques for Phase Noise Suppression in Recirculating DLLs," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 8, pp. 1222–1230, Aug. 2004.

[PDF]

J. Welz and I. Galton, "A Tight Signal-Band Power Bound on Mismatch Noise in a Mismatch-Shaping Digital-to-Analog Converter," *IEEE Transactions on Information Theory*, vol. 50, no. 4, pp. 593–607, Apr. 2004.

[PDF]

E. Siragusa and I. Galton, "A Digitally Enhanced 1.8-V 15-bit 40-MSample/s CMOS Pipelined ADC," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2126–2138, Dec. 2004.

[PDF]

S. Pamarti, L. Jansson, and I. Galton, "A Wideband 2.4-GHz Delta-Sigma Fractional- N PLL with 1-Mb/s In-Loop Modulation," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 1, pp. 49–62, Jan. 2004.

[PDF]

M. Y. Li, I. Galton, L. E. Larson, and P. M. Asbeck, "Correlation Techniques for Estimation of Amplifier Nonlinearity," *IEEE Radio and Wireless Conference*, 2004, pp. 179–182.

[PDF]

E. Siragusa, I. Galton, "A Digitally Enhanced 1.8 V 15 b 40 MS/s CMOS Pipelined ADC," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2004, pp. 452 – 538, Feb. 2004.

[PDF] [SLIDES]

2003

S. Ye, L. Jansson, and I. Galton, "Techniques for In-Band Phase Noise Suppression in Recirculating DLLs," *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, 2003, pp. 297–300.

[PDF]

S. Pamarti and I. Galton, "Phase-Noise Cancellation Design Tradeoffs in Delta-Sigma Fractional- N PLLs," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 50, no. 11, pp. 829–838, Nov. 2003.

[PDF]

I. Galton, "Delta-Sigma Fractional- N Phase-Locked Loops", *Phase-Locking in High-Performance Systems: From Devices to Architectures* (ed. Behzad Razavi), Wiley-IEEE Press, 2003.

[PDF]

2002

S. Ye, L. Jansson, and I. Galton, "A Multiple-Crystal Interface PLL with VCO Realignment to Reduce Phase Noise," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2002, vol. 2, pp. 58–401.

[PDF] [SLIDES]

S. Ye, L. Jansson, and I. Galton, "A Multiple-Crystal Interface PLL with VCO Realignment to Reduce Phase Noise," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1795–1803, Dec.

2002.

[\[PDF\]](#)

J. Welz and I. Galton, "Necessary and Sufficient Conditions for Mismatch Shaping in a General Class of Multibit DACs," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 49, no. 12, pp. 748–759, Dec. 2002.

[\[PDF\]](#)

J. Welz and I. Galton, "A Necessary and Sufficient Condition for Mismatch Shaping in Multi-Bit DACs," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 2002, vol. 1, p. I-105-I-108.

[\[PDF\]](#)

J. Keyzer, R. Uang, Y. Sugiyama, M. Iwamoto, I. Galton, and P. M. Asbeck, "Generation of RF Pulsewidth Modulated Microwave Signals Using Delta-Sigma Modulation," *IEEE MTT-S International Microwave Symposium Digest*, 2002, vol. 1, pp. 397–400.

[\[PDF\]](#)

J. Grilo, I. Galton, K. Wang, and R. G. Montemayor, "A 12-mW ADC Delta-Sigma Modulator with 80 dB of Dynamic Range Integrated in a Single-Chip Bluetooth Transceiver," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 3, pp. 271–278, Mar. 2002.

[\[PDF\]](#)

I. Galton, "Delta-Sigma Data Conversion in Wireless Transceivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 1, pp. 302–315, Jan. 2002.

[\[PDF\]](#)

A. Fishov, E. Siragusa, J. Welz, E. Fogleman, and I. Galton, "Segmented Mismatch-Shaping D/A Conversion," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 2002, vol. 4, p. IV-679-IV-682.

[\[PDF\]](#)

G. Chang, L. Jansson, K. Wang, J. Grilo, R. Montemayor, C. Hull, M. Lane, A. X. Estrada, M. Anderson, I. Galton, S. V. Kishore, "A Direct-Conversion Single-Chip Radio-Modem for Bluetooth," *IEEE International Solid-State Circuits Conference (ISSCC)*, 2002, vol. 1, pp. 88–448.

[\[PDF\]](#)

P. Asbeck, I. Galton, K.-C. Wang, J. F. Jensen, A. K. Oki, and C. T. M. Chang, "Digital Signal Processing-Up to Microwave Frequencies," *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 900–909, Mar. 2002.

[\[PDF\]](#)

2001

J. Welz and I. Galton, "The Mismatch-Noise PSD From a Tree-Structured DAC in a Second-Order Delta-Sigma Modulator With a Midscale Input," *Proceedings of the IEEE International Conference on Acoustics, Speech, and Signal Processing*, 2001, vol. 4, pp. 2625–2628.

[\[PDF\]](#)

P.M. Asbeck, I. Galton, L.E. Larson, X. Zhang, M. Iwamoto, J. Hinrichs and J. Keyzer, "Digital Control of Power Amplifiers for Wireless Communications," *31st European Microwave Conference*, 2001, pp. 1-4, vol. 4, pp. 2625–2628.

[\[PDF\]](#)

P. M. Asbeck, L. E. Larson and I. G. Galton, "Synergistic Design of DSP and Power Amplifiers for Wireless Communications," in *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, no. 11, pp. 2163-2169, Nov 2001.

[\[PDF\]](#)

J. Welz, I. Galton, and E. Fogleman, "Simplified Logic for First-Order and Second-Order Mismatch-Shaping Digital-to-Analog Converters," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 11, pp. 1014–1027, Nov. 2001.

[\[PDF\]](#)

J. Keyzer, J. Hinrichs, A. Metzger, M. Iwamoto, I. Galton, and P. Asbeck, "Digital Generation of RF Signals for Wireless Communications with Band-Pass Delta-Sigma Modulation," *IEEE MTT-S International Microwave Symposium Digest*, 2001, vol. 3, pp. 2127–2130 vol. 3.

[\[PDF\]](#)

J. Grilo, I. Galton, K. Wang, and R. Montemayor, "A 12 mW ADC Delta-Sigma Modulator with 80

dB of Dynamic Range Integrated in a Single-Chip Bluetooth Transceiver,” *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, 2001, pp. 23–26.

[\[PDF\]](#)

E. Fogleman and I. Galton, “A Dynamic Element Matching Technique for Reduced-Distortion Multibit Quantization in Delta-Sigma ADCs,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 2, pp. 158–170, Feb. 2001.

[\[PDF\]](#)

E. Fogleman and I. Galton, “A Digital Common-Mode Rejection Technique for Differential Analog-to-Digital Conversion,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 48, no. 3, pp. 255–271, Mar. 2001.

[\[PDF\]](#)

E. Fogleman, J. Welz, and I. Galton, “An Audio ADC Delta-Sigma Modulator with 100-dB Peak SINAD and 102-dB DR Using a Second-Order Mismatch-Shaping DAC,” *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 339–348, Mar. 2001.

[\[PDF\]](#)

2000

E. J. Siragusa and I. Galton, “Gain Error Correction Technique for Pipelined Analogue-to-Digital Converters,” *Electronics Letters*, vol. 36, no. 7, pp. 617–618, Mar. 2000.

[\[PDF\]](#)

I. Galton, “Digital Cancellation of D/A Converter Noise in Pipelined A/D Converters,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 47, no. 3, pp. 185–196, Mar. 2000.

[\[PDF\]](#)

E. Fogleman, J. Welz, and I. Galton, “An Audio ADC Delta-Sigma Modulator with 100 dB SINAD and 102 dB DR Using a Second-Order Mismatch-Shaping DAC,” *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, 2000, pp. 17–20.

[\[PDF\]](#)

E. Fogleman, I. Galton, W. Huff, and H. Jensen, “A 3.3-V Single-Poly CMOS Audio ADC Delta-Sigma Modulator With 98-dB Peak SINAD and 105-dB Peak SFDR,” *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 297–307, Mar. 2000.

[\[PDF\]](#)

1999

E. Fogleman, I. Galton, and H. Jensen, “A Dynamic Element Matching Technique for Reduced-Distortion Multibit Quantization in Delta-Sigma ADCs,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1999, vol. 2, pp. 290–293.

[\[PDF\]](#)

E. Fogleman, I. Galton, W. Huff, and H. Jensen, “A 3.3 V Single-Poly CMOS Audio ADC Delta-Sigma Modulator With 98 dB Peak SINAD,” *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, 1999, pp. 121–124.

[\[PDF\]](#)

E. Fogleman, I. Galton, and H. Jensen, “An Area-Efficient Differential Input ADC With Digital Common Mode Rejection,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1999, vol. 2, pp. 347–350.

[\[PDF\]](#)

1998

E. T. King, A. Eshraghi, I. Galton, and T. S. Fiez, “A Nyquist-Rate Delta-Sigma A/D Converter,” *IEEE Journal of Solid-State Circuits*, vol. 33, no. 1, pp. 45–52, Jan. 1998.

[\[PDF\]](#)

H. T. Jensen and I. Galton, “A Reduced-Complexity Mismatch-Shaping DAC for Delta-Sigma Data Converters,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1998, vol. 1, pp. 504–507 vol. 1

[\[PDF\]](#)

H. T. Jensen and I. Galton, “An Analysis of the Partial Randomization Dynamic Element Matching Technique,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 12, pp. 1538–1549, Dec. 1998.

[\[PDF\]](#)

H. T. Jensen and I. Galton, "A Low-Complexity Dynamic Element Matching DAC for Direct Digital Synthesis," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 45, no. 1, pp. 13–27, Jan. 1998.

[\[PDF\]](#)

W. Huff and I. Galton, "Nonuniform-to-Uniform Decimation for Delta-Sigma Frequency-to-Digital Conversion," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1998, vol. 1, pp. 365–368 vol. 1.

[\[PDF\]](#)

I. Galton, W. Huff, P. Carbone, and E. Siragusa, "A Delta-Sigma PLL for 14 b 50 kSample/s Frequency-to-Digital Conversion of a 10 MHz FM Signal," *IEEE International Solid-State Circuits Conference (ISSCC)*, 1998, pp. 366–367.

[\[PDF\]](#)

I. Galton, W. Huff, P. Carbone, and E. Siragusa, "A Delta-Sigma PLL for 14-b, 50 kSample/s Frequency-to-Digital Conversion of a 10 MHz FM Signal," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2042–2053, Dec. 1998.

[\[PDF\]](#)

1997

H. T. Jensen and I. Galton, "Yield Estimation of a First-Order Noise-Shaping D/A Converter," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1997, vol. 1, pp. 441–444.

[\[PDF\]](#)

H. T. Jensen and I. Galton, "A Performance Analysis of the Partial Randomization Dynamic Element Matching DAC Architecture," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1997, vol. 1, pp. 9–12.

[\[PDF\]](#)

I. Galton, "Spectral Shaping of Circuit Errors in Digital-to-Analog Converters," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 10, pp. 808–817, Oct. 1997.

[\[PDF\]](#)

1996

H. T. Jensen and I. Galton, "A Hardware-Efficient DAC for Direct Digital Synthesis," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1996, vol. 4, pp. 97–100.

[\[PDF\]](#)

I. Galton, "Noise-Shaping D/A Converters for Delta-Sigma Modulation," *Proceeding of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1996, vol. 1, pp. 441–444.

[\[PDF\]](#)

I. Galton, D. A. Towne, J. J. Rosenberg, and H. T. Jensen, "Clock Distribution Using Coupled Oscillators," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1996, vol. 3, pp. 217–220.

[\[PDF\]](#)

I. Galton and H. T. Jensen, "Oversampling Parallel Delta-Sigma Modulator A/D Conversion," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 43, no. 12, pp. 801–810, Dec. 1996.

[\[PDF\]](#)

1995

H. T. Jensen and I. Galton, "A Robust Parallel Delta-Sigma A/D Converter Architecture," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1995, vol. 2, pp. 1340–1343.

[\[PDF\]](#)

I. Galton, "A Practical Second-Order Delta-Sigma Frequency-to-Digital Converter," *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1995, vol. 1, pp. 5–8.

[\[PDF\]](#)

I. Galton, "Analog-Input Digital Phase-Locked Loops for Precise Frequency and Phase Demodulation," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal*

Processing, vol. 42, no. 10, pp. 621–630, Oct. 1995.

[\[PDF\]](#)

I. Galton and H. T. Jensen, “Delta-Sigma Modulator Based A/D Conversion Without Oversampling,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 773–784, Dec. 1995.

[\[PDF\]](#)

I. Galton and P. Carbone, “A Rigorous Error Analysis of D/A Conversion with Dynamic Element Matching,” *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 42, no. 12, pp. 763–772, Dec. 1995.

[\[PDF\]](#)

1994

E. King, F. Aram, T. Fiez, and I. Galton, “Parallel Delta-Sigma A/D Conversion,” *Proceedings of the IEEE Custom Integrated Circuits Conference (CICC)*, 1994, pp. 503–506.

[\[PDF\]](#)

I. Galton, “Higher-Order Delta-Sigma Frequency-to-Digital Conversion,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1994, vol. 5, pp. 441–444.

[\[PDF\]](#)

I. Galton, “Granular Quantization Noise in a Class of Delta-Sigma Modulators,” *IEEE Transactions on Information Theory*, vol. 40, no. 3, pp. 848–859, May 1994.

[\[PDF\]](#)

P. Carbone and I. Galton, “Conversion Error in D/A Converters Employing Dynamic Element Matching,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1994, vol. 2, pp. 13–16.

[\[PDF\]](#)

1993

I. Galton, “One-Bit Dithering in Delta-Sigma Modulator-Based D/A Conversion,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1993, pp. 1310–1313 vol. 2.

[\[PDF\]](#)

I. Galton, “Granular Quantization Noise in the First-Order Delta-Sigma Modulator,” *IEEE Transactions on Information Theory*, vol. 39, no. 6, pp. 1944–1956, Nov. 1993.

[\[PDF\]](#)

I. Galton and G. Zimmerman, “Combined RF Phase Extraction and Digitization,” *Proceedings of the IEEE International Symposium on Circuits and Systems (ISCAS)*, 1993, pp. 1104–1107 vol. 2.

[\[PDF\]](#)

1989

I. Galton, “An Efficient Three-Point Arc Algorithm,” *IEEE Computer Graphics and Applications*, vol. 9, no. 6, pp. 44–49, Nov. 1989.

[\[PDF\]](#)

PATENTS

I. Galton, E. Alvarez-Fontecilla, A. Eissa, “Frequency to Digital Converter, Asynchronous Phase Sampler, and Digitally Controlled Oscillator Methods,” U.S. Patent No. 11,437,980, September 6, 2022.

I. Galton, E. Alvarez-Fontecilla, “Multi-rate DEM with mismatch noise cancellation for digitally-controlled oscillators,” U.S. Patent No. 10,735,005, February 27, 2020.

I. Galton, C. Weltin-Wu, “Digital fractional-N PLL based upon ring oscillator delta-sigma frequency conversion,” U.S. Patent No. 10,158,366, December 18, 2018.

I. Galton, M. Pedrali-Noy, “Fast Frequency Throttling and Re-Locking Technique for Phase-Locked Loops,” U.S. Patent No. 9,602,113, March 3, 2016.

I. Galton, “Foreground and Background Bandwidth Calibration Techniques for Phase-Locked Loops,” U.S. Patent No. 9,461,657, October 4, 2016.

G. Taylor, I. Galton, “Mostly-Digital Open-Loop Ring Oscillator Delta-Sigma ADC and Methods for Conversion,” U.S. Patent No. 9,397,691, July 19, 2016.

A. Swaminathan, I. Galton, “VCO With Linear Gain Over a Very Wide Tuning Range,” U.S. Patent No. 9,054,687, June 9, 2015.

G. Taylor, I. Galton, “Ring Oscillator Delta Sigma ADC Modulator With Replica Path Nonlinearity Calibration,” U.S. Patent No. 8,542,138, September 24, 2013.

A. Swaminathan, I. Galton, “Adaptive Phase Noise Cancellation for Fractional-N Phase Locked Loop,” U.S. Patent No. 7,999,622, August 16, 2011.

A. Swaminathan, I. Galton, “Nonlinearity Robust Successive Requantizer,” U.S. Patent No. 7,986,250, July 26, 2011.

P. Asbeck, I. Galton, “Radio Transmission Frequency Digital Signal Generation,” U.S. Patent No. 7,953,174, May 31, 2011.

M. Li, P. Asbeck, I. Galton, L. Larson, “Correlation Method for Monitoring Power Amplifier,” U.S. Patent No. 7,652,532, January 26, 2010.

A. Panigada, I. Galton, “Digital Background Correction of Nonlinear Error in ADCs,” U.S. Patent No. 7,652,532, October 13, 2009.

I. Galton, “Digital Background Cancellation of Digital to Analog Converter Mismatch Noise in Analog to Digital Converters,” U.S. Patent No. 7,006,028, February 28, 2006.

E. Fogleman, H. T. Jensen, I. Galton, “Analog-to-Digital Converters With Common-Mode Rejection Dynamic Element Matching, Including as Used in Delta-Sigma Modulators,” U.S. Patent No. 6,816,100, November 9, 2004.

I. Galton, “Digital Cancellation of D/A Converter Noise in Pipelined A/D Converters,” U.S. Patent No. 6,734,818, May, 2004.

I. Galton, J. A. Grilo, and K. J.-N. Wang, “Partial Mismatch-Shaping Digital-to-Analog Converter,” U.S. Patent No. 6,697,004, February, 2004.

S. Ye, I. Galton, "CMOS Phase Locked Loop With Voltage Controlled Oscillator Having Realignment to Reference and Method for the Same," U.S. Patent No. 6,683,506, January, 2004.

I. Galton, "Method and Apparatus for Cyclic Return to Zero Techniques for Digital to Analog Convertors," U.S. Patent No. 6,476,748, November, 2002.

I. Galton, "Spectral Shaping of Circuit Errors in Digital-to-Analog Converters," U.S. Patent No. 5,684,482, November, 1997.

I. Galton, "Combined Angle Demodulator and Digitizer," U.S. Patent No. 5,369,404, November, 1994.

S.H. Maslak, H.G. Larsen, J.S. Chaffin, P.E. Chandler, I. Galton, and M. Karmali, "Variable Origin-Variable Acoustic Scanning Method and Apparatus," U.S. Patent No. 5,261,408, November 16, 1993.

S.H. Maslak, H.G. Larsen, J.S. Chaffin, P.E. Chandler, I. Galton, and M. Karmali, "Variable Origin-Variable Angle Acoustic Scanning Method and Apparatus for a Curved Linear Array," U.S. Patent No. 5,235,986, August 17, 1993.

Galton, "Analog-to-Digital Converter Using Parallel Delta-Sigma Modulator," U.S. Patent No. 5,196,852, March 23, 1993.

S.H. Maslak, H.G. Larsen, J.S. Chaffin, P.E. Chandler, I. Galton, and M. Karmali, "Variable Origin-Variable Angle Acoustic Scanning Method and Apparatus," U.S. Patent No. 5,148,810, September 22, 1992.