

MICROELECTRONICS

AN INTEGRATED APPROACH

Roger T. Howe

*Department of Electrical Engineering and Computer Sciences
University of California at Berkeley
Berkeley, California*

Charles G. Sodini

*Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, Massachusetts*

Prentice Hall Electronic and VLSI Series
Charles G. Sodini, Series Editor



Prentice Hall, Upper Saddle River, New Jersey 07458

Library of Congress Cataloging-in-Publication Data

Howe, Roger Thomas.
Microelectronics : an integrated approach / Roger T. Howe,
Charles G. Sodini.
p. cm.
Includes bibliographical references and index.
ISBN 0-13-588518-3
1. Microelectronics. 2. Solid state electronics. I. Sodini,
Charles G. II. Title.
TK7874.H688 1997
621.3815--dc20

96-17867
CIP

Acquisitions editor: Eric Svendsen
Production service: TKM Productions
Editorial/production supervision: Sharyn Vitrano
Copy editor: TKM Productions
Interior design: Lisa Delgado
Cover design: Joseph Sengotta
Art director: Amy Rosen
Managing editor: Bayani Mendoza DeLeon
Editor-in-chief: Marcia Horton
Director of production and manufacturing: David W. Riccardi
Manufacturing buyer: Julia Meehan
Editorial assistant: Kathryn Cassino



© 1997 by Prentice-Hall, Inc.
Simon & Schuster / A Viacom Company
Upper Saddle River, New Jersey 07458

All rights reserved. No part of this book may
be reproduced, in any form or by any means,
without permission in writing from the publisher.

The author and publisher of this book have used their best efforts in preparing this book. These efforts
include the development, research, and testing of the theories and programs to determine their effective-
ness. The author and publisher make no warranty of any kind, expressed or implied, with regard to these
programs or the documentation contained in this book. The author and publisher shall not be liable in any
event for incidental or consequential damages in connection with, or arising out of, the furnishing, perfor-
mance, or use of these programs.

Printed in the United States of America

10 9 8 7 6 5

ISBN 0-13-588518-3

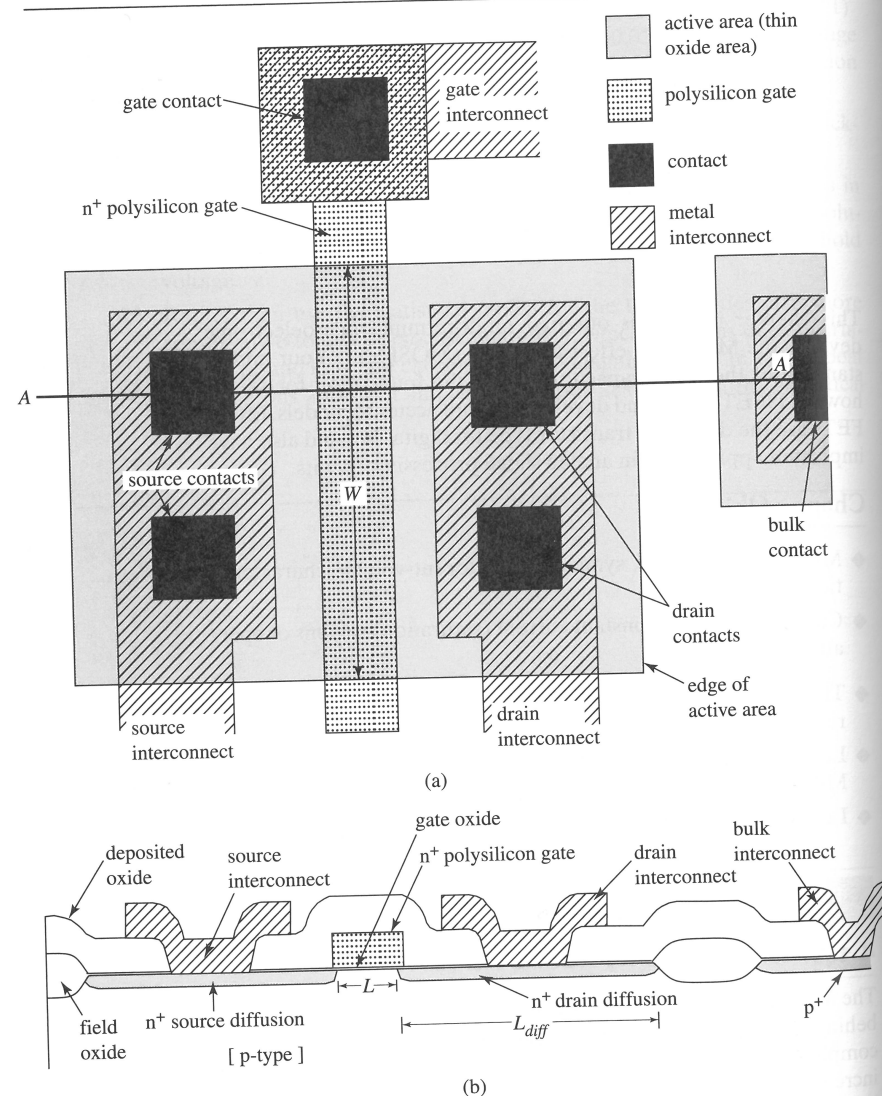
Prentice-Hall International (UK) Limited, London
Prentice-Hall of Australia Pty. Limited, Sydney
Prentice-Hall Canada Inc., Toronto
Prentice-Hall Hispanoamericana, S.A., Mexico
Prentice-Hall of India Private Limited, New Delhi
Prentice-Hall of Japan, Inc., Tokyo
Simon & Schuster Asia Pte. Ltd., Singapore
Editora Prentice-Hall do Brasil, Ltda., Rio de Janeiro

To our families,

Jenny
Nathan, Julie, Debbie and Greg
R. T. H.

Anne
Maria and John
C. G. S.

modern n-channel MOSFET is shown in Fig. 4.1. The basic structure is identical to that of the simple MOSFET whose fabrication process was described in detail in Chapter 2. The **gate** of the transistor is a film of n^+ polycrystalline silicon (polysilicon). Underlying the gate is the **gate oxide** which is a layer of thermally grown silicon dioxide (SiO_2).



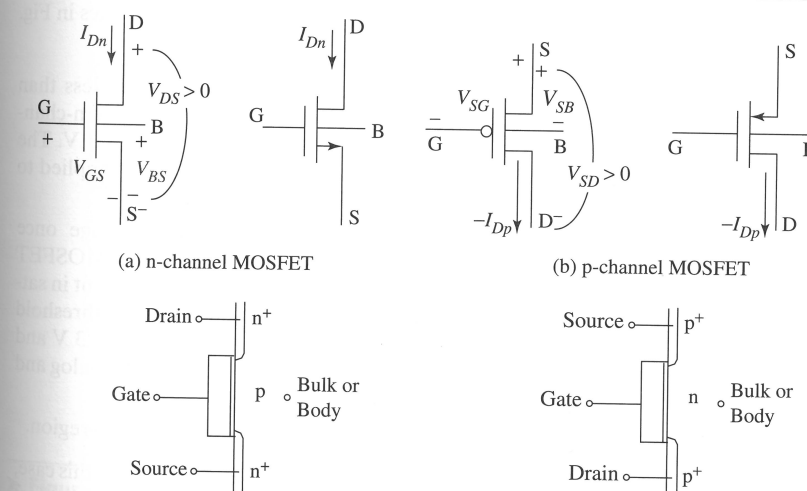
► **Figure 4.1** (a) Four-mask layout and (b) cross section of an integrated n-channel MOSFET.

The **channel** is formed under the polysilicon gate between the two n^+ regions as shown in Fig. 4.1 (b). The **channel length** L of the MOSFET as is defined in Fig. 4.1 (b) as the gap between the n^+ diffusions. On the layout in Fig. 4.1(a), the **channel width** W of the MOSFET is defined as the width of the active area. One n^+ diffusion is called the **source**, the other is called the **drain**. The potentials on the diffusions will be the basis for differentiating the source from the drain, as discussed in the next section. The source and drain diffusions have a length L_{diff} and the same width W as the channel. Metal interconnections make ohmic contacts to the gate, source, and drain. In addition, the underlying p-type bulk region (the substrate or a deep p-type diffusion) is contacted with a fourth metal interconnection called the **bulk** or **body**.

MOSFET Circuit Symbol and 4.1.2 Terminal Characteristics

Before introducing the current-voltage characteristics of the MOSFET, it is helpful to have a symbol for this device. Unfortunately, there are two common symbols for each MOSFET type. Figure 4.2 shows the circuit symbols and basic structure for an **n-channel MOSFET** (shown in Fig. 4.1) and for the complementary **p-channel MOSFET** that has p^+ source and drain diffusions in an n-type bulk region. In this text we will use the symbols without arrows for digital circuits and the symbols with arrows for analog circuits. The cross sections for the two MOSFETs have been rotated 90° in order to illustrate the close correspondence between the symbols and the physical structure.

The MOSFETs are oriented as they often appear in circuit schematics: the drain for the n-channel MOSFET and the source for the p-channel MOSFET are on top—toward the positive voltage supply. Voltages between terminals are labeled by an ordered pair of subscripts such as $V_{GS} = V_G - V_S$. By IEEE convention, the reference



► **Figure 4.2** (a) n-channel MOSFET symbols and structure and (b) p-channel MOSFET symbols and structure.

directions for currents are defined as positive *into* the device terminals. Since the drain current for the p-channel device is negative, it is convenient to use $-I_{Dp} > 0$, which is positive leaving the drain terminal. For the n-channel MOSFET in Fig. 4.2(a), the drain and source terminals are selected so that $V_{DS} > 0$, which is equivalent to defining the source as the one with the *lower* potential. As shown in Fig. 4.2(b), the labeling convention is opposite for the p-channel MOSFET. Its source and drain are identified so that $V_{SD} > 0$, which means its source is defined as the one with the *higher* potential.

The n-channel MOSFET's static (DC) terminal characteristics can be measured with voltage sources and ammeters. Since the MOSFET is a four terminal device, we need to experiment and discover which voltages are most important. For our initial investigation, we short the bulk to the source to set $V_{BS} = 0$ V. Since the voltage *differences* between the drain and source and gate and source are most important, we ground the source ($V_S = 0$ V) for convenience. Since the gate terminal is insulated, the only current of interest is that into the drain terminal I_{Dn} .

Figure 4.3(a) is a schematic of the circuit used to find the drain current's functional dependence on the two voltages under our control: the gate-source voltage V_{GS} and the drain-source voltage V_{DS} . The conventional way to graph the measured data is to plot a family of curves $I_{Dn}(V_{GS}, V_{DS})$, with V_{GS} as a parameter. The drain current versus drain-source voltage curves for a selected set of gate-source voltages are called the MOSFET **drain characteristics**.

Figure 4.3(b) shows measured drain characteristics for an n-channel MOSFET in a digital CMOS process. Although the voltage and current ranges can vary with the technology and device layout, the ranges in Fig. 4.3(b) are typical. In this graph, the drain current I_D is measured as a function of drain-source voltage V_{DS} for eight gate-source voltages

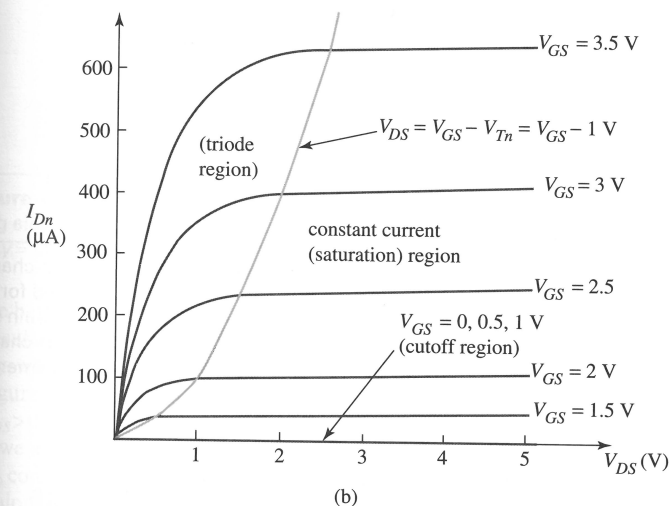
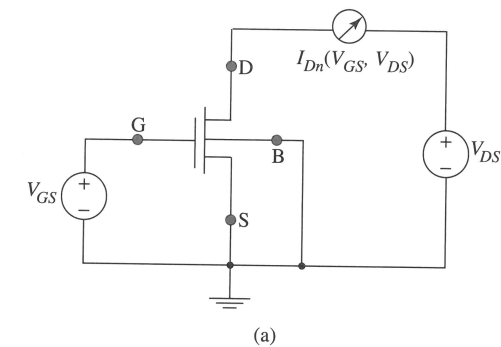
$$I_{Dn}(V_{GS} = 0, 0.5, 1, 1.5, 2, 2.5, 3, 3.5 \text{ V}, V_{DS}), \text{ for } 0 \text{ V} < V_{DS} < 5 \text{ V} \quad (4.1)$$

Several observations can be made from studying the drain characteristics in Fig. 4.3(b).

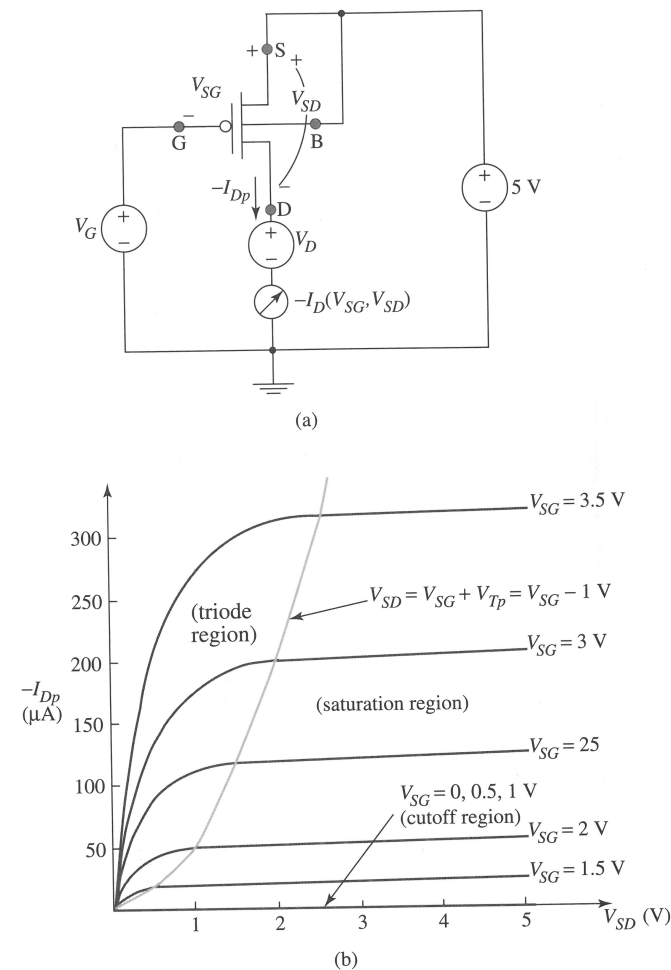
1. The MOSFET is **cutoff** ($I_{Dn} = 0$ A) for gate-source voltages that are less than some critical voltage, which is defined as the **threshold voltage** V_{Tn} of the n-channel device. A typical value for the n-channel threshold voltage is $V_{Tn} = 1$ V. The n^+ source and drain are electrically isolated until sufficient voltage is applied to the gate to create an n-type inversion layer or **channel** between them.
2. The drain current is nearly independent of the drain-source voltage once $V_{DS} > V_{GS} - V_{Tn}$. In this region of operation, called **saturation**, the MOSFET behaves like a current source. Further study reveals that the drain current in saturation is proportional to the square of the gate-source voltage above threshold $(V_{GS} - V_{Tn})^2$. This can be seen from the ratios of drain current for $V_{GS} = 3$ V and for $V_{GS} = 2$ V. This constant-current behavior will be exploited in both analog and digital circuit design.
3. The region where I_{Dn} depends on both V_{GS} and V_{DS} is termed the **triode** region.

The p-channel MOSFET's drain characteristics are shown in Fig. 4.4. In this case, the source and n-type bulk terminals are both connected to a 5 V supply. The effect of varying the drain voltage and gate voltage on the drain current can be investigated. The shape of the drain characteristics are identical to those of the n-channel MOSFET

if $-I_{Dp}$ (which is positive) is plotted against the source-drain drop $V_{SD} = 5 \text{ V} - V_D$ as a function of the source-gate voltage $V_{SG} = 5 \text{ V} - V_G$. The drain current is zero unless the source-gate voltage $V_{SG} > -V_{Tp}$, where V_{Tp} is the p-channel threshold voltage. A typical value for the p-channel threshold voltage is $V_{Tp} = -1$ V.



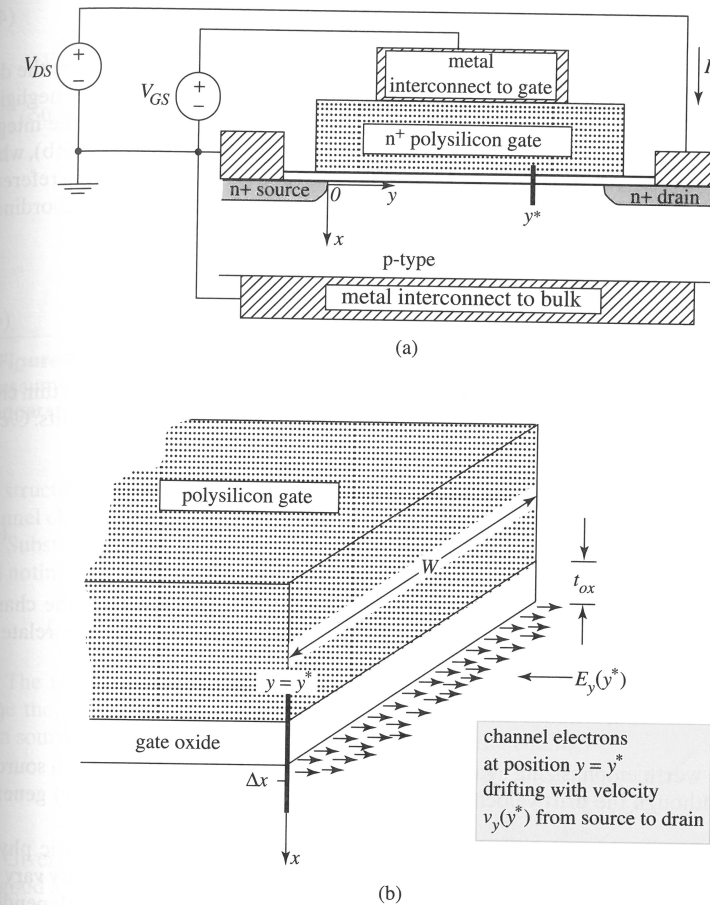
► **Figure 4.3** n-channel MOSFET drain characteristics: (a) test circuit and (b) measurements of drain current as function of drain-source voltage, with gate-source voltage as a parameter for a typical integrated device.



► **Figure 4.4** (a) Test circuit and (b) measured drain characteristics of a p-channel MOSFET with the same geometric dimensions as the n-channel device used for Fig. 4.3. The negative of the drain current $-I_{Dp}$ (> 0) is plotted against the source-drain drop V_{SD} , with the source-gate drop V_{SG} as a parameter. The drain current for the p-channel is about half that of the n-channel device for identical geometries and complementary threshold voltages $V_{Tp} = -V_{Tn} = -1$ V.

► 4.2 DEVICE PHYSICS OF THE MOSFET: DRAIN CURRENT AND CHANNEL CHARGE

We are now prepared to quantify how the drain current varies with the terminal voltages for the n-channel MOSFET. As a starting point, we will build upon the electrostatics of the MOS capacitor that were discussed in Chapter 3. Once the channel forms, an inversion layer of electrons exists between source and drain. An applied

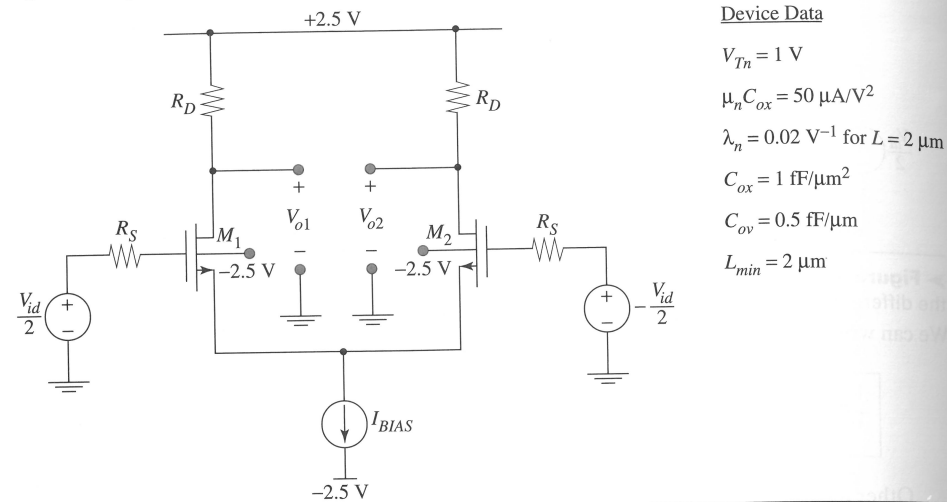


► **Figure 4.5** (a) MOSFET biased with $V_{GS} > V_{Tn}$ and $V_{DS} > 0$. (b) Cutaway view of drifting electrons in the channel at position y^* (see (a)) between the source ($y = 0$) and drain ($y = L$).

voltage between the drain and source will impose an electric field across the channel that results in a drift current density. A good first step is to relate this drift current density, which is the origin of the drain current I_D , to the charge in the inversion layer.

Figure 4.5(a) illustrates an n-channel MOSFET with applied voltages $V_{GS} > V_{Tn}$ and $V_{DS} > 0$. For simplicity, we again short the bulk to the source so $V_{BS} = 0$. Furthermore, we assume that a channel extends from the source to the drain. The drain current I_D consists of electrons drifting from source to drain along the channel. At any point along the channel, the electron drift current must equal the drain current I_D since there is no current to the substrate or through the insulating oxide to the gate.

Figure 4.5(b) shows a perspective view of a portion of the channel at position y^* between the source and drain. From basic semiconductor physics, the drift current density J_y at any point (x, y) in the channel is given by



► Figure Ex11.2

$$\text{So } R_D = \frac{2 \cdot 2.5 \text{ V}}{I_{BIAS}} = \frac{5 \text{ V}}{50 \mu\text{A}} = 100 \text{ k}\Omega$$

Since we know $R_D = 100 \text{ k}\Omega$, we can find the required g_m needed to achieve a differential-mode gain of -50 . From the value of g_m we calculate W/L .

$$a_{dm} = -g_m (R_D \parallel r_o) \approx -g_m R_D = -50, \text{ thus } g_m = -\frac{a_{dm}}{R_D} = \frac{50}{100 \text{ k}\Omega} = 0.5 \text{ mS}$$

$$g_m = \sqrt{2 \left(\frac{W}{L} \right)_{1,2} \mu_n C_{ox} \frac{I_{BIAS}}{2}}, \text{ so}$$

$$\left(\frac{W}{L} \right)_{1,2} = \frac{g_m^2}{\mu_n C_{ox} I_{BIAS}} = \frac{(0.5 \text{ mS})^2}{(50 \mu\text{A/V}^2) (50 \mu\text{A})} = 100$$

We will choose the minimum length of $L = 2 \mu\text{m}$ to achieve the best frequency response. Therefore, $(W/L)_{1,2} = 200/2$.

Note: a typical value of λ_n for $L = 2 \mu\text{m}$ is 0.02 V^{-1} which yields an output resistance

$r_o = 1/\lambda_n I_{BIAS} = 1 \text{ M}\Omega$. Our gain estimate neglected this resistance.

$$C_{gs} = \frac{2}{3} W L C_{ox} = \frac{2}{3} \cdot 200 \mu\text{m} \cdot 2 \mu\text{m} \cdot 1 \text{ fF}/\mu\text{m}^2 = 0.27 \text{ pF}$$

$$C_{gd} = W C_{ov} = 200 \mu\text{m} (0.5 \text{ fF}/\mu\text{m}) = 0.1 \text{ pF}$$

The 3 dB frequency can be estimated using the Miller Approximation.

$$C_M \approx g_m R_D C_{gd} = 50 (0.1 \text{ pF}) = 5 \text{ pF}$$

Device Data

$$V_{Tn} = 1 \text{ V}$$

$$\mu_n C_{ox} = 50 \mu\text{A/V}^2$$

$$\lambda_n = 0.02 \text{ V}^{-1} \text{ for } L = 2 \mu\text{m}$$

$$C_{ox} = 1 \text{ fF}/\mu\text{m}^2$$

$$C_{ov} = 0.5 \text{ fF}/\mu\text{m}$$

$$L_{min} = 2 \mu\text{m}$$

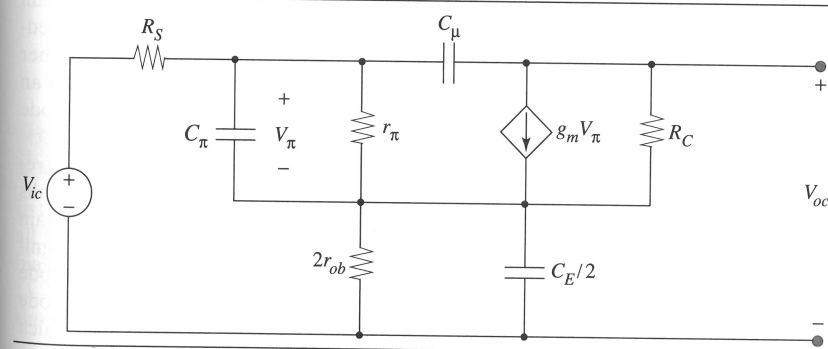
$$f_{3dB} = \frac{\omega_{3dB}}{2\pi} = \frac{1}{2\pi R_S (C_{gs} + C_M)} = \frac{1}{2\pi (5 \text{ k}\Omega) (5.27 \text{ pF})} = 6.04 \text{ MHz}$$

11.4.2 Common-Mode Frequency Response

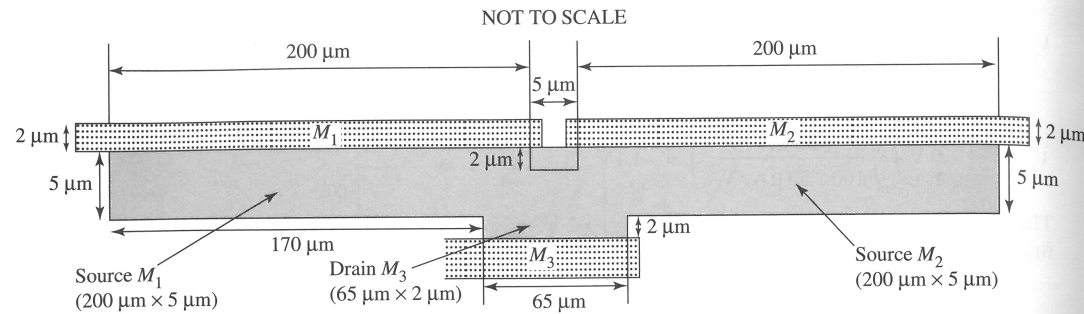
In this section we analyze the frequency response of the common-mode output voltage given a purely common-mode input voltage. Since the circuit is perfectly symmetrical, we can again use the half-circuit technique. The half-circuit for the purely common-mode frequency response is shown in Fig. 11.17.

The contribution of the internal resistance of the bias current source to the common-mode half-circuit is twice its actual value. We use a resistor equal to $2r_{ob}$ to account for this fact. A capacitor C_E , in parallel with the bias current source represents the parasitic capacitance at this node. Since this capacitance has the dominant effect on the frequency response of the common-mode voltage gain, we must take this parasitic capacitance into account. The contribution of the impedance of this capacitor to the common-mode half circuit is twice its actual impedance. Therefore, we place a capacitor of value $C_E/2$ in the common-mode half-circuit to account for this impedance.

We begin the analysis by solving for the common-mode voltage gain at DC by open-circuiting all the capacitors. The amplifier looks exactly like the common-emitter amplifier with an emitter degeneration resistor that was analyzed in Chapter 8. The value of the emitter degeneration resistor is $2r_{ob}$. Since the emitter degeneration resistor is large, the input resistance of this amplifier is large and the effect of the



► Figure 11.17 Common-mode half-circuit small-signal model to analyze the common-mode frequency response of the differential amplifier.



► Figure Ex11.3B

perimeter is very small since the drain of M_3 is shared with the sources of M_1 and M_2 . The perimeter that bounds field oxide is only $(2\ \mu\text{m} + 2\ \mu\text{m})$.

$$C_{sb1} = C_{sb2} = (200\ \mu\text{m} \cdot 5\ \mu\text{m}) C_{jn} + (5\ \mu\text{m} + 170\ \mu\text{m}) C_{jsw} = 188\ \text{fF}$$

$$C_{db3} = (65\ \mu\text{m} \cdot 2\ \mu\text{m}) C_{jn} + (2\ \mu\text{m} + 2\ \mu\text{m}) C_{jsw} = 15\ \text{fF}$$

So the total capacitance is

$$C_E = C_{gd3} + C_{sb1} + C_{sb2} + C_{db3} \approx 32.5\ \text{fF} + 188\ \text{fF} + 188\ \text{fF} + 15\ \text{fF} = 425\ \text{fF}.$$

The $CMRR$ has a magnitude that is $-3\ \text{dB}$ below its low frequency value at

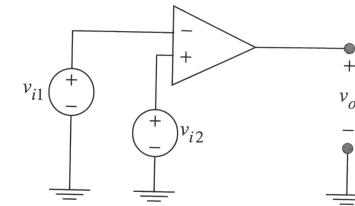
$$f_{3dB} \approx \frac{1}{2\pi r_{o3} C_E} = \frac{1}{2\pi (2.5\ \text{M}\Omega) (425\ \text{fF})} = 150\ \text{kHz}$$

► 11.5 DIFFERENTIAL AMPLIFIERS WITH SINGLE-ENDED OUTPUTS

It is often important to convert a differential signal into a single-ended signal. A **single-ended signal** is defined as one that is referenced to ground. Many operational amplifiers have this function built into the amplifier as indicated by the symbol for an operational amplifier. The input has two voltage sources that can have both differential and common-mode components, while the output is a single-ended voltage referenced to ground as shown in Fig. 11.19. The easiest way to make a differential-to-single-ended conversion is to take just one output from the differential amplifier analyzed in the previous section, as shown in Fig. 11.20.

The differential- and common-mode gain of this circuit can be analyzed from the results in Section 11.2. Recall in Eq. (11.20) that the expression for v_{o2} was written in terms of the purely differential- and common-mode signals as

$$v_o = v_{o2} = a_{cm} v_{ic} - a_{dm} \frac{v_{id}}{2} \quad (11.38)$$



► Figure 11.19 Many operational amplifiers require a differential-to-single-ended conversion.

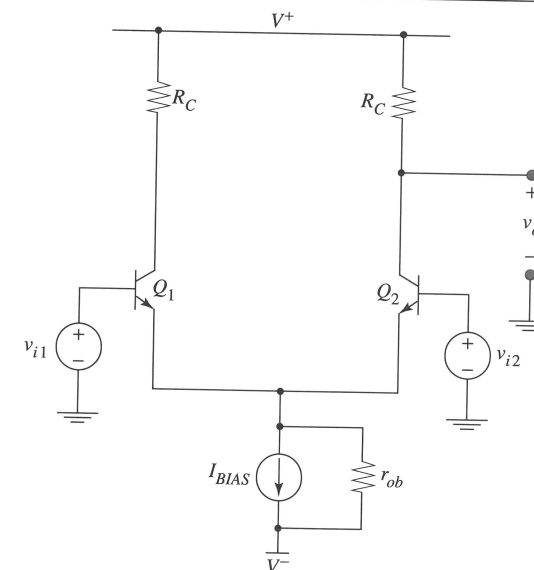
where $a_{dm} = -g_m R_C$ and $a_{cm} = \frac{-g_m R_C}{1 + 2g_m r_{ob}}$.

Using Eq. (11.38) the differential-mode gain for a purely differential input signal for this single-ended amplifier is

$$\frac{v_o}{v_{id}} = -\frac{a_{dm}}{2} = \frac{g_m R_C}{2} \quad (11.39)$$

The common-mode gain for a purely common-mode input signal is

$$\frac{v_o}{v_{ic}} = a_{cm} = \frac{-g_m R_C}{1 + 2g_m r_{ob}} \quad (11.40)$$



► Figure 11.20 Differential amplifier with single-ended output.