

Transcript of Ian Galton, Ph.D.

Date: April 14, 2025
Case: Texas Instruments Incorporated -v- Parkervision, Inc. (PTAB)

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WORLDWIDE COURT REPORTING & LITIGATION TECHNOLOGY

ParkerVision Exhibit 2039
TI v. ParkerVision - IPR2024-00934

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

- - - - - - - - - - - - - - x

TEXAS INSTRUMENTS :

INCORPORATED, :

Petitioner, : IPR2024-00934

v. : U.S. Patent 7,496,342 B2

PARKERVISION, INC., :

Patent Owner. :

- - - - - - - - - - - - - - X

Videotaped Deposition of IAN GALTON, Ph.D.

Conducted Virtually

Monday, April 14, 2025

12:02 p.m. EDT

Job No.: 578938

Pages 1 - 56

Reported by: Debra A. Whitehead

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Videotaped Deposition of IAN GALTON, Ph.D., conducted virtually.

Pursuant to notice, before Debra Ann Whitehead, E-Notary Public in and for the Commonwealth of Virginia.

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ALSO PRESENT:

PARKER SIMPSON, Video Specialist

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C O N T E N T S

EXAMINATION OF IAN GALTON, Ph.D. PAGE

By Ms. Mandir 7

E X H I B I T S

(Attached to the Transcript)

GALTON EXHIBIT PAGE

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P R O C E E D I N G S

VIDEO SPECIALIST: Here begins the videotaped deposition of Ian Galton, Ph.D.; in the matter of Texas Instruments Incorporated versus ParkerVision, Incorporated; in the United States Patent and Trademark Office, before the Patent Trial and Appeals Board; Case Number IPR2024-00934. 12:01:52 12:01:53 12:01:58 12:02:00 12:02:04 12:02:08 12:02:12

Today's date is 4/14/2025. The time on the video monitor is 12:02 eastern time. The remote videographer for today is Parker Simpson, representing Planet Depos. All parties of this video deposition are attending remotely. 12:02:13 12:02:17 12:02:20 12:02:25 12:02:28

Would counsel please voice-identify themselves and state whom they represent. 12:02:29 12:02:31

MS. MANDIR: This is Stephanie Mandir from Daignault Iyer, on behalf of ParkerVision. 12:02:31 12:02:34

MR. MAGEE: This is Robert Magee from Blue Peak Law Group, on behalf of Petitioner Texas Instruments. Also attending today are Josh Griswold and Rishi Gupta from Fish & Richardson. 12:02:38 12:02:40 12:02:43 12:02:46

VIDEO SPECIALIST: The court reporter 12:02:50

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today is Debbie Whitehead, representing Planet Depos. 12:02:50

The witness will now be sworn. 12:02:50

IAN ANDREW GALTON, Ph.D., 12:02:50

having been duly sworn, testified as follows: 12:03:03

EXAMINATION BY COUNSEL FOR PATENT OWNER 12:03:03

BY MS. MANDIR: 12:03:03

Q Good morning, Dr. Galton. Can you please state your full name, for the record. 12:03:06 12:03:08

A Ian Andrew Galton. 12:03:10

Q And do you have any documents in front of you today? 12:03:12 12:03:15

A I do not. 12:03:17

Q And do you agree not to communicate with anyone else while questions are being asked in today's deposition? 12:03:17 12:03:21 12:03:23

A I do. 12:03:27

Q Is there any reason that you can't give truthful and accurate testimony today? 12:03:27 12:03:29

A No. 12:03:31

Q So you provided two different declarations in IPR2024-00934. Correct? 12:03:31 12:03:35

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A Yes. 12:03:42

Q And you understand that this is an IPR related to U.S. Patent Number 7,496,342. Correct? 12:03:42 12:03:47

A Yes. 12:03:52

Q And you submitted a first declaration in support of the petition which was marked as TI-1003. Correct? 12:03:52 12:03:56 12:04:04

A I did submit a first deposition. I'd have to check the number, but that sounds right. 12:04:07 12:04:11

Q And you were deposed regarding that first declaration. Correct? 12:04:13 12:04:16

A Yes. 12:04:18

Q And after that deposition you provided patent owner with a second declaration. Correct? 12:04:18 12:04:21

A Yes. 12:04:24

Q And the purpose of today's deposition is to ask you about that second declaration and the simulations included. 12:04:24 12:04:28 12:04:32

Do you understand? 12:04:33

A I do. 12:04:34

MS. MANDIR: I'm now going to be providing you with a document entitled Second 12:04:39 12:04:42

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Declaration of Ian Galton, Ph.D. It should be provided in the chat momentarily, and please just let me know when you have that in front of you. 12:04:45 12:04:47 12:04:51

A Okay. It has not some through yet. 12:04:54

Q A little bit larger, so maybe it's taking a second. 12:05:07 12:05:10

A There. It just came through. 12:05:12

Q The document entitled Second Declaration of Ian Galton, Ph.D., will be Exhibit 1 to your deposition today. 12:05:17 12:05:19 12:05:23

(Galton Deposition Exhibit 1 marked for identification and is attached to the transcript.) 12:05:23 12:05:25

Q And Exhibit 1 is a copy of your second declaration in IPR2024-00934 that you submitted and prepared for the purposes of this proceeding. 12:05:25 12:05:29 12:05:34

Correct? 12:05:37

A Correct. 12:05:38

Q And Exhibit 1 provides additional simulations that were performed beyond those described in your originally submitted declaration. Correct? 12:05:38 12:05:42 12:05:44 12:05:46

A Yes. 12:05:50

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Q And if we scroll through your second declaration, Section 2 is a section entitled DeMaw Circuit with Siliconix U430 JFET Models. Correct? 12:05:50 12:05:52 12:06:00

A Siliconix, yes. 12:06:09

Q And in your first declaration you stated that the DeMaw circuit had been simulated with Siliconix U430 JFET models; however, you realized later that it was actually inadvertent simulated with the default generic LTspice JFET models instead. Correct? 12:06:11 12:06:12 12:06:16 12:06:18 12:06:23 12:06:28

A Correct. 12:06:29

Q And if you go to Paragraph 3 of your second declaration, it states that the simulations in Section 2, Part A, of your second declaration correspond to the same circuit and inputs as the DeMaw simulations in your original declaration, but just using the U430 JFET model instead. 12:06:30 12:06:33 12:06:37 12:06:42 12:06:46 12:06:48

Correct? 12:06:51

A Correct. 12:06:52

Q So if you go to Page 6 of your second declaration, you'll find a figure DeMaw-SIM-Figure 1, Revised, and this is a graphical representation 12:06:52 12:07:05 12:07:11

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of the LTspice simulation of the original DeMaw Figure 6.7 circuit, just using the corrected U430 JFET model. Correct? 12:07:15 12:07:19 12:07:25

A Correct. 12:07:27

Q So just to clarify, there is nothing changed from this circuit as shown on Page 6 of your second declaration in your simulated DeMaw circuit in your first or original declaration other than the corrected JFET model? 12:07:27 12:07:29 12:07:34 12:07:43 12:07:45

A The circuit is the same. But as we describe in this document, we tightened the tolerances of the simulator. So we took some steps to make the simulation more accurate. And those are indicated in the text in the upper left corner of the figure we're looking at. 12:07:51 12:07:54 12:07:59 12:08:03 12:08:06 12:08:09

Q So you said that there were steps taken to make the stimulation more accurate in the DEMAW-SIM-FIG. 1 Revised. 12:08:19 12:08:22 12:08:24

Can you point to where in this figure -- 12:08:28

A Yes. 12:08:34

Q -- that can be shown? 12:08:35

A So if you look at the very top line of 12:08:37

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text, it says .OPTIONS. And then it says, numdgt equals 12 plotwinsize equals zero reltol equals .0001. And each of those improves the accuracy of the simulation. 12:08:39 12:08:44 12:08:50 12:08:54

So I start with reltol, which is the last of the three. The default value is .001, and we changed it to .0001. And internally the simulator is solving a set of matrix equations which approximate a system of differential equations. But because computers can only sample or -- or process sampled data and not continuous time data, it makes an approximation, it does numerical integration. And that reltol parameter offers a trade-off. 12:08:55 12:08:58 12:09:04 12:09:09 12:09:13 12:09:17 12:09:21 12:09:23 12:09:25 12:09:28

If you make that parameter smaller, the accuracy of the numerical integrations gets higher, at the expense of taking longer to simulate. And so the default value was higher than it is in this -- in this diagram, and we made it smaller to make it more accurate. 12:09:29 12:09:33 12:09:36 12:09:39 12:09:44 12:09:52

Plotwinsize equals zero turns off a compression algorithm. So as I'm sure you've 12:09:54 12:09:58

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noticed from the data we sent you, the output files are enormous from these simulations. And the simulator has a built-in feature that's on by default which compresses the data. And it does so by deciding which points it feels it can throw out without causing too much inaccuracy, and it throws them out. 12:10:00 12:10:03 12:10:06 12:10:10 12:10:14 12:10:17 12:10:20

And we -- we found that in the case of Macnally that was actually degrading the accuracy, so we just disabled it for all of our simulations. 12:10:21 12:10:24 12:10:28

And then numdgt specifies the number of decimal places that the data is written out to the files. And before it had been significantly lower; and because of that, we were getting significant round-off error. 12:10:32 12:10:37 12:10:42 12:10:45 12:10:47

None of these changes made much of a difference for DeMaw, but they made a significant difference for Macnally. 12:10:49 12:10:52 12:10:54

Q So outside of these parameters in the U430 JFET model, there are no other changes from your original simulated DeMaw circuit to the circuit shown in DEMAW-SIM-FIG. 1 Revised here. 12:10:56 12:11:04 12:11:10 12:11:14

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Is that correct? 12:11:18

A Well, I mean it is, but I need to clarify that a bit. 12:11:19 12:11:22

So originally we decided what -- I mean, we told the simulator what data to store in output files by clicking on wires and basically saying Store this value, store that value. And then when we ran the simulation, it wrote whatever we told it to write to a file. But later when you guys wanted to see all of our files, we decided that would be very cumbersome to explain and would lead to a lot of confusion. 12:11:23 12:11:30 12:11:34 12:11:38 12:11:40 12:11:44 12:11:49 12:11:52 12:11:54

So if you look at the second line in the -- in the file there that we've been looking at -- sorry, the figure that we've been looking at, the .SAVE, what that line does is it tells the simulator to save those specific voltages and/or currents. 12:11:55 12:11:59 12:12:01 12:12:03 12:12:10 12:12:14

And so we didn't have that in the original circuit simulation because we did it by hand. So that .SAVE directive doesn't actually change the circuit or the simulation in any way; 12:12:16 12:12:19 12:12:25 12:12:29

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it just change -- it just -- it just specifies what output values are written. 12:12:32 12:12:34

And then the .TRAN just tells it how long to simulate. And offhand I don't remember if we simulated it for exactly that amount of time or a little bit less or a little bit more. So that might be different, I just don't know. I don't remember. 12:12:37 12:12:41 12:12:44 12:12:47 12:12:49 12:12:51

Q So outside of the .SAVE parameters, the first line of parameters, and the U430 JFET models, the rest of the circuit simulated in the Figure 1 revised figure here is the exact same as the originally simulated DeMaw circuit. 12:12:51 12:12:58 12:13:03 12:13:07 12:13:13

Is that correct? 12:13:17

A I believe so, yes. 12:13:17

Q And you said that when -- strike that. 12:13:18

You said that when you reran the simulations using the U430 JFET models, you observed a significant increase in the mixer gain. 12:13:27 12:13:29 12:13:34

Is that correct? 12:13:38

A Yes. 12:13:39

Q What contributed to that mixer gain? 12:13:39

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A The parameters of those JFETs are significantly different, and so they offer a higher trans-conductance, for example. And that gave rise to a higher gain. 12:13:43 12:13:48 12:13:50 12:13:55

Q And the simulations in Section 2, Part B, of your second declaration are the results of the same circuit as the original declaration, but with a U430 model and with a smaller input signal amplitude. Correct? 12:13:56 12:14:04 12:14:08 12:14:11 12:14:15

A Hold on, I just want to go to my table of contents just so I'm -- we're literally on the same page. 12:14:17 12:14:20 12:14:22

So -- I'm so sorry, would you mind just repeating that, that question? 12:14:23 12:14:26

Q Sure. The simulations in part -- strike that. 12:14:27 12:14:31

The simulations in Section 2, Part B, of your second declaration are the results of the same circuit as your original declaration for DeMaw, but with a U430 JFET model and with a smaller input signal amplitude. 12:14:31 12:14:34 12:14:37 12:14:42 12:14:46

Is that correct? 12:14:48

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A Yeah, but let me clarify what you said just to make sure we're saying the same thing. 12:14:51 12:14:53

So what we just looked at was the -- was the circuit corresponding to 2A. And then we subsequently ran the same circuit with a 6 dB lower input signal, and that's Figure 2 -- I mean Section 2B. 12:14:56 12:15:02 12:15:08 12:15:14 12:15:16

So the answer is yes, but I just want to make sure that I'm saying what you're saying. 12:15:18 12:15:19

Q And Figure 1.1 in your second declaration, which is on Page 14, shows that same circuit as Figure 1, but just with a smaller input signal amplitude. 12:15:22 12:15:28 12:15:33 12:15:35

Is that correct? 12:15:36

A Give me one second to check it out. 12:15:38

Yes. 12:15:50

Q And you ran the simulations with a smaller input signal amplitude to correct for the mixer gain? 12:15:50 12:15:56 12:15:59

Is that correct? 12:15:59

A No. 12:16:01

Q Why did you run simulations with a 12:16:03

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smaller input signal amplitude? 12:16:07

A We wanted to make sure that the mixer was operating in its linear region. And so we reduced the signal, input signal, by 6 dB and observed that the output reduced correspondingly. And, therefore, we knew from that that the mixer was in its -- in its linear region. So it was just a sanity check. 12:16:10 12:16:15 12:16:20 12:16:26 12:16:29 12:16:32 12:16:35

Q So just to confirm the Figure 1.1, in your second declaration nothing changed from your originally simulated DeMaw circuit other than the U JFET models and the input signal amplitude. 12:16:36 12:16:50 12:16:55 12:16:58

Is that correct? 12:17:03

MR. MAGEE: Objection to form. 12:17:05

A When you said the -- are you comparing the results from Part 2A or my original declaration? 12:17:07 12:17:09 12:17:14

Q Let me reask the question. Strike that. 12:17:14

Nothing changed from your originally simulated DeMaw circuit other than the U430 JFET model and the input amplitude in Figure 1.1 of your second declaration, outside of the parameters 12:17:23 12:17:26 12:17:32 12:17:40

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illustrated in the .SAVE and .OPTIONS lines of the upper left-hand corner of the figure. 12:17:45 12:17:54

Is that correct? 12:17:56

A And possibly the .TRAN. I don't remember. But that is correct. 12:17:58 12:18:01

Q So turning to Paragraph 10 of your declaration here. 12:18:02 12:18:14

You state that your original declaration included one histogram of the charge loss ratio percentages for Capacitors C4 and C5, which was DEMAW-SIM-FIG. 7. Correct? 12:18:18 12:18:21 12:18:25 12:18:29

A Yes. 12:18:33

Q And you say in your second declaration that you've created separate histograms, one for Capacitor C4 and one for Capacitor C5. Correct? 12:18:33 12:18:35 12:18:39

A Yes. 12:18:43

Q Did you use the same calculation methodology to generate the histograms in your second declaration as you did in your first declaration? 12:18:43 12:18:45 12:18:48 12:18:50

A No. 12:18:53

Q What changes did you make? 12:18:54

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A Well, the changes are described later in this document. But we had been using -- we had been using current into the capacitors, and integrating that current to determine the charge, which is a valid method. So there's nothing wrong with that method. 12:19:00 12:19:01 12:19:07 12:19:10 12:19:13 12:19:17

But we decided that if we used voltage instead, it would be -- it's just a different way of doing it. And since we're relying on the internal accuracy of LTspice to do that calculation, we believed it would be more accurate. 12:19:18 12:19:22 12:19:27 12:19:29 12:19:33 12:19:36

So our goal is to just improper accuracy. We also believed it would be easier for your expert to follow if we -- if we relied on LTspice to do the integration, as opposed to doing it in Python. 12:19:36 12:19:39 12:19:42 12:19:46 12:19:49

Q Did you provide the Python script for the calculations used to generate the histograms in the first declaration? 12:19:49 12:19:57 12:20:02

A Yes. And the first -- no, not in the first declaration, only in the second declaration. 12:20:04 12:20:07

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Q And so you said that in the calculations used in the first declaration you were using the current into the capacitors, and integrating that current to determine the charge. Now in the second declaration your calculations were using the voltage instead of integrating the current. 12:20:13 12:20:17 12:20:21 12:20:23 12:20:26 12:20:29

Is that correct? 12:20:33

A That is correct. 12:20:34

MR. MAGEE: Objection to form. 12:20:34

THE WITNESS: Sorry, Bobby. 12:20:34

A Yes, that is correct. 12:20:38

Q Were there any other changes to your calculation outside of the integration of current to voltage? 12:20:39 12:20:40 12:20:43

A Well, it's not as if we just -- everywhere we saw current we replaced it with the voltage. I mean, the calculation is a little different. Because the current through a capacitor is equal to the capacitance times the derivative of the voltage. And so we made corresponding changes to calculate it correctly. 12:20:48 12:20:51 12:20:55 12:20:56 12:20:59 12:21:03 12:21:09

The two methods in principle are 12:21:13

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identical. It's just that the internal operation of the -- of LTspice gives it essentially higher accuracy to let it -- to do it in terms of voltage and then current. 12:21:15 12:21:20 12:21:26 12:21:29

It made almost no difference in the circuits, but we just thought this would be a cleaner way of doing it. And since we -- you had requested and we complied to give you all of our documentation, we decided to do it in a way that we felt was cleaner and easier to read and provided more accuracy. 12:21:31 12:21:36 12:21:38 12:21:41 12:21:45 12:21:49 12:21:52

Q I'm now going to provide you with a document labeled Exhibit 2. This will be Exhibit 2 to your deposition. And this will be a Word formatted version of the Python script titled Comp, or C-O-M-P, dot PY, which you produced to us. 12:22:03 12:22:05 12:22:09 12:22:14 12:22:17 12:22:23

So we simply copied the Python script into a Word document so that it was readable to everyone, and that's what's going to be provided as Exhibit 2. 12:22:23 12:22:26 12:22:29 12:22:31

(Galton Deposition Exhibit 2 marked for 12:22:31

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identification and is attached to the transcript.) 12:22:31

Q Let me know when you have that document in front of you. 12:22:33 12:22:34

A Okay. Okay, I have the document. Give me a second, though. I'm just looking through it. 12:22:36 12:22:50

Okay. Got it. 12:23:07

Q So, Dr. Galton, do you recognize Exhibit 2? 12:23:09 12:23:13

A I do. It's in a kind of weird format, but -- but it appears to be equivalent to the comp.PY document we sent you. 12:23:16 12:23:19 12:23:25

Q And specifically if you could scroll down to the line starting at 654. 12:23:28 12:23:32

A Six fifty -- my copy doesn't have line numbers on it, so I don't know where you want me to go. 12:23:40 12:23:42 12:23:52

Q To the right of the lines there's not numbers? 12:23:52 12:23:55

A There are not numbers in mine. Oh, I'm sorry. There are. I'm so sorry. It was off screen. Give me a second, I'm going to adjust this. 12:23:55 12:24:01 12:24:05 12:24:07

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Okay. What line number do you want me to go to? 12:24:08 12:24:10

Q Please turn to Line 654. 12:24:11

A I'm scrolling down. Give me a second. 12:24:21

Q Just let me know when you're at Line 654. 12:24:32

A I'm there. 12:24:35

Q Starting at Line 654 of Exhibit 2, it starts the function of the histogram plots. 12:24:36 12:24:41

Correct? 12:24:45

A Yes. 12:24:46

Q And will you describe from this code how you plotted the histograms? 12:24:46 12:24:54

A Okay. Well, so the actual function starts at 658 def cap histogram. And if we scroll down through the docstring, which is the thing inside the triple quotes, we get to Line 687. 12:24:56 12:25:01 12:25:09 12:25:15

So the first thing we do is we take the data -- okay. Let's back up for a minute. Let's go up to the Line 658. 12:25:22 12:25:30 12:25:33

So -- excuse me -- dat is -- well, fd is the output file destination. Fn is the name of the file. And then dat is a Python dictionary 12:25:37 12:25:47 12:25:51

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which contains the simulation data. 12:25:55

LO is the LO waveform name. And CAP is a 12:25:59

string, which is just the capacitor to be plotted; 12:26:07

for instance C6 or C7. And then tstart is the 12:26:11

start time. And t end is the end time. And 12:26:15

number of points is -- sorry, npts is number of 12:26:21

points. 12:26:24

So if we go down now to 688, what trim is 12:26:25

doing is just taking this dictionary, which you 12:26:36

can think of as an array or a set of arrays that 12:26:38

are indexed by name. 12:26:48

And so what we're doing first off is 12:26:53

trimming so that the time data starts at tstart 12:26:59

and ends at tend. Okay? 12:27:05

And -- excuse me. So then we calculate 12:27:09

the LO, the vlo, as being the difference between 12:27:21

lo0 and lo1. Excuse me. And this allow us to 12:27:27

optionally use a differential LO or a 12:27:38

nondifferential LO. And then vlo is -- hold on 12:27:42

one second. Let me back up, because I -- because 12:27:52

I skipped over a few things. 12:27:54

So first of all, if there are two LO 12:27:56

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sequences, that means it's a differential LO. If on the other hand there's one LO sequence, then it's a single-ended LO. And so this if statement determines which of the two cases is the case and loads this list vlo with that data. Okay. 12:28:05 12:28:08 12:28:12 12:28:16 12:28:24

And then once again, depending on whether it's differential or single-ended, we determine the cap signal in Line 699. And then we use the LO to divide up the interval. 12:28:34 12:28:36 12:28:44 12:28:50

So if the LO is turning the switches on, that's our so-called charging period. And if it's turning the switches off, that's our so-called discharging period. 12:28:52 12:28:58 12:29:01 12:29:04

And then -- let's see. Give me one second here. Okay. So then what we do is we figure out the number of periods there are. And since we're always looking at two at a time, so we're looking at the current period and the next period, and then we move on to the current period and the next period after that and so forth, we have to subtract one off so we don't run past the end of our array, that's 706. 12:29:09 12:29:12 12:29:22 12:29:27 12:29:31 12:29:33 12:29:35 12:29:37 12:29:40

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And then in 708, if the number of points that's been requested to the function is less than the number of events we have, we shorten it. And then we compute the total charge delivered to the capacitor when the switch is on, and the charge lost from the capacitor when the switch is off is indicated in the comment. So we calculate qin and qout. 12:29:44 12:29:48 12:29:50 12:29:55 12:29:58 12:30:03 12:30:06 12:30:10

So the first thing we do is we set up lists that have the right number of values; those are in 712 and 713. And then we get the time indices for the start of the first on period, or the current on period, the end of the current on period and the end of the next off period. So that's idx0, idx1, idx2. 12:30:11 12:30:16 12:30:19 12:30:29 12:30:32 12:30:34 12:30:41

And then we use the capacitor voltage, which is already integrated by spice, which I mentioned before. So the -- the charge stored on a capacitor is C times delta-v, where delta-v is the change in voltage and C is the capacitance. 12:30:45 12:30:47 12:30:49 12:30:56 12:31:02

So qin, the charge stored during the time when the switch is on, is calculated in 719. And 12:31:07 12:31:15

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the charge that's lost compared to what was stored in -- when the switch was on, is calculated in 720. 12:31:23 12:31:27 12:31:31

Now, I should point out here that what we're calling qin and qout at this stage are actually voltage changes, because we're going to take a ratio. And so if we wanted them to be actually charge values, it would be C times qin and C times qout. But because we're taking a ratio of qin and qout subsequently the C cancels out. 12:31:32 12:31:35 12:31:38 12:31:41 12:31:43 12:31:46 12:31:49 12:31:54

And so when we look at qloss, Line 727, you can see that qloss is qout divided by qin. And we multiply it by 100 to turn it into a percent from a fraction. And then we just call the histogram function from NumPy, and then we just add some labels and we're done. 12:31:54 12:32:00 12:32:08 12:32:12 12:32:14 12:32:17

Q Let's go back through some of those things that you just explained. 12:32:19 12:32:27

If you go to Line 718, it says use capacitor voltage, already integrated by spice. 12:32:31 12:32:36

Correct? 12:32:38

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A Yes. 12:32:39

Q And where is the voltage I guess being integrated? 12:32:42 12:32:46

A So in a capacitor, I equals C times the derivative of the voltage. Okay? So if we integrate both sides of that equation, we get the integral of current equals C times the change in voltage. 12:32:52 12:32:58 12:33:01 12:33:03 12:33:06

And the integral of current is charge, because current is charge per unit time. So when you integrate current, you get charge. 12:33:09 12:33:14 12:33:18

And previously in our -- in my original declaration we were in Python integrating the current to calculate the charge. But LTspice does that integration when it calculates the voltage across the capacitor. 12:33:21 12:33:25 12:33:28 12:33:34 12:33:38

So we decided that it would be more accurate and it would cause less confusion and perhaps less contention in depositions if we instead just used the voltage across the capacitor to determine the charge. Because, as I said, charge is proportional to voltage change across 12:33:39 12:33:41 12:33:43 12:33:46 12:33:50 12:33:58

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the capacitor. 12:34:01

Q And you said that the LTspice already 12:34:03
does the integration when it calculates voltage. 12:34:09
Can you point to somewhere in the code that shows 12:34:14
that? 12:34:16

MR. MAGEE: Objection to form. 12:34:19

A LTspice, I don't have the code for 12:34:20
LTspice. I mean, that's internal to the way that 12:34:24
LTspice works. 12:34:26

You know, it's like saying, you know -- 12:34:28
I'm looking at Word right now, and it's 12:34:31
underlining certain words that are misspelled. 12:34:35
And if you ask me, Can you point to where in the 12:34:37
code it figures out which word is misspelled, I'd 12:34:40
have to say I can't do that. I don't have the 12:34:43
source code for Microsoft Word. 12:34:45

And in the same way I don't have the 12:34:48
source code for LTspice. It's done internally. 12:34:49

Q Is there a function or variable in the 12:34:55
script that indicates that spice is doing some 12:34:59
sort of integration to find the voltage? 12:35:03

A No. But there doesn't need to be, 12:35:08

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because a fundamental principle of electronic circuits that POSITAs are taught when they're in their freshman or sophomore year in college, is that -- is that the equation of current through a capacitor is equal to -- is that the current through a capacitor equals the capacitance times the derivative of the voltage. And, therefore, if you -- if you know the voltage change across the capacitor, you -- and you know the capacitance, you know the amount of charge that was changed on that capacitor. 12:35:11 12:35:16 12:35:20 12:35:24 12:35:27 12:35:31 12:35:36 12:35:41 12:35:44 12:35:49 12:35:54

And any circuit simulator that calculates voltage across a capacitor has to be doing that integration, because at every node it keeps track of current and voltage. And the only way that it can know the voltage across the capacitor is if it has ultimately integrated the current, or done the equivalent of integrating the current. 12:35:58 12:36:01 12:36:06 12:36:10 12:36:13 12:36:17 12:36:23

Q On Line 719 of the code the variable qin[ii] is -- strike that. 12:36:25 12:36:44

On Line 719 the variable qin[ii] is computed. 12:36:55 12:37:01

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Do you see that? 12:37:02

A Yes. 12:37:03

Q What is qin[ii]? 12:37:03

A So qin is a list, or you can think of it as an array, ii is the index. So it -- qin[ii] points to the ii'th element in that list. And cap_sig I-X -- [idx1] is the voltage at one of the capacitor nodes. And cap_sig[idx0] is the voltage at the other capacitor node. 12:37:11 12:37:16 12:37:25 12:37:32 12:37:43 12:37:48

And so qin[ii] is actually the voltage change across the capacitor when the switch is closed. 12:37:51 12:37:56 12:38:03

And as I mentioned, it's a little bit of -- qin we -- we're using it as if it's charge; but in reality to make it charge, we would have to multiply by C. But since we didn't multiply by C, it's actually the voltage change across the capacitor. 12:38:06 12:38:08 12:38:15 12:38:17 12:38:24 12:38:26

But when we divide subsequently in Line 727 qout by qin, it doesn't matter whether C is there or not. Because -- because if it had been there, it would have cancelled. So we just don't 12:38:28 12:38:31 12:38:35 12:38:38

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bother multiplying by C because subsequently it gets cancelled out anyway. 12:38:40 12:38:43

Q So qin refers to the change in voltage across a capacitor when the switch is closed? 12:38:49 12:39:03

Is that correct? 12:39:08

A Yes. 12:39:09

Q And another way to put that would be the charge delivered to the capacitor while the switch -- or strike that. 12:39:09 12:39:14 12:39:20

Another way to put that would be the charge delivered to the capacitor during a charging cycle? 12:39:21 12:39:28 12:39:31

Is that correct? 12:39:32

MR. MAGEE: Objection. Form. 12:39:33

A It's proportional to the charge delivered to the capacitor when the switch is closed. 12:39:34 12:39:37

Q So qin would be proportional to the charge delivered to the capacitor during a charging cycle. 12:39:44 12:39:50 12:39:53

Is that correct? 12:39:54

A Yes. 12:39:56

Q And -- 12:39:56

A I'm so sorry. Can I just amend that? I want to make sure we're very precise. If we define the charging cycle to be the period of time when the switch is closed, then the answer is yes. 12:40:00 12:40:04 12:40:07 12:40:09

Q So can we say that it is the -- strike that. 12:40:11 12:40:19

Can we say that it is the -- refers to -- strike that. 12:40:19 12:40:23

Can we say that qin is proportional to the charge delivered to the capacitor when the switch is on during one cycle? 12:40:23 12:40:26 12:40:29

A Yes. 12:40:33

MR. MAGEE: Object to form. 12:40:33

Q And can you explain what the variable qout means in Line 720? 12:40:35 12:40:40

A It is the same thing for when the switch is open -- when the switch is subsequently open in the next -- in the next cycle, but the negative of that. 12:40:46 12:40:50 12:40:56 12:40:57

Because if the -- if qin corresponds to charging, then we have the negative, so that corresponds to discharging. 12:40:58 12:41:01 12:41:04

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Q And Line 720 uses the cap_sig[idx2] minus cap_sig[idx1], whereas qin uses cap_sig[idx1] minus cap_sig[idx0]. 12:41:05 12:41:05 12:41:27

Can you explain what idx0, idx1, and idx2 mean in this context? 12:41:27 12:41:33

A Yes. So idx stands for index. So remember, we've got an array of variables. And the index allows us to select specific elements out of the array. 12:41:34 12:41:38 12:41:44 12:41:49

So we're going through a loop here. And for each portion of time when the switch closes, and then followed by the portion of time when the switch opens, we're doing our calculation. 12:41:50 12:41:54 12:42:01 12:42:03

So idx0 is the index value corresponding to the time at which the switch closes; that is, becomes conductive. 12:42:06 12:42:10 12:42:15

Idx1 is an index corresponding to the time at which the switch opens, which means it becomes nonconductive. And idx2 is the -- is the index corresponding to the time that marks the end of the region of time during which the switch is open. 12:42:17 12:42:20 12:42:24 12:42:33 12:42:36 12:42:40

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So therefore, qin[ii] is looking at the voltage -- is the voltage change across the capacitor during the current switch close time interval. And qout is the negative of the voltage change across the capacitor during the subsequent switch open time interval. 12:42:45 12:42:50 12:42:54 12:43:00 12:43:06 12:43:09

Q So would qout be the change in voltage during the period of time when the switch is off during a discharge cycle? 12:43:11 12:43:30 12:43:36

MR. MAGEE: Objection to form. 12:43:39

A It is the negative of the change in voltage over the period of time when the switch is turned off. 12:43:40 12:43:43 12:43:47

Q And that would be over one cycle of the switch? 12:43:51 12:43:58

A I don't know what you mean by "one cycle of the switch," I'm sorry. 12:44:02 12:44:03

Q Let me rephrase that question. Strike that. 12:44:04 12:44:09

This would be over one cycle of the RF signal. Correct? 12:44:10 12:44:16

A Not necessarily. It would be the -- the 12:44:19

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time between idx0 and idx2 corresponds to one cycle of the local oscillator, one period of the local oscillator. 12:44:29 12:44:36 12:44:38

Q In Line 727, qloss is how you calculated the percentage, which is 100 times qout divided by qin. Correct? 12:44:43 12:44:49 12:44:54

A Yes. 12:44:55

Q So would you say that the percentage discharge would be proportional to the charge loss during one discharge cycle divided by the charge delivered to the capacitor during the charge cycle? 12:44:55 12:44:59 12:45:04 12:45:08 12:45:12

A Yes. 12:45:12

MR. MAGEE: Objection to form. 12:45:13

Q Is this -- strike that. 12:45:14

The script that we just looked at to generate the histogram plotting, was that used for all of the histograms generated in your second declaration? 12:45:23 12:45:26 12:45:30 12:45:35

A Yes. 12:45:36

Q So that would be all the histograms generated for DeMaw as well as all the histograms 12:45:36 12:45:41

generated for the Macnally circuit. Correct? 12:45:45

A Yes. 12:45:48

Q And you can put Exhibit 2 away. And if we can turn back to Exhibit 1, which is your second declaration. And turn to Section 3. 12:45:48 12:45:56 12:45:59

A Just give me a second. Sorry. 12:46:05

Okay. I'm there. Go where? I'm sorry. 12:46:11

Q If you could turn to Section 3, which starts on Page 19 of your second declaration. It is entitled DeMaw Circuit Modified to Match DeMaw Figure 6.7 With A Squared-Up LO. Let me know when you're there. 12:46:13 12:46:15 12:46:19 12:46:23 12:46:27

A Yep, I'm there. 12:46:27

Q And your original DeMaw circuit simulations used -- 12:46:29 12:46:37

A I don't know if I lost you. Are you there? 12:46:51 12:46:53

Q Yeah, sorry. Strike that last question. DeMaw -- strike that. 12:46:53 12:46:58

In Paragraph 18 you write that "The set of simulation results presented in this section correspond as closely as possible to the circuit 12:47:01 12:47:06 12:47:09

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shown in Figure 6.7 given the information provided in the figure and associated text of DeMaw." 12:47:11 12:47:14

Do you see that? 12:47:17

A Yes. 12:47:23

Q How did you change the simulations in this section from Section 2 so that it would more closely correspond to the circuit shown in Figure 6.7 and the information provided in DeMaw? 12:47:23 12:47:33 12:47:38 12:47:43

A Okay. I'd like to put up two copies of this so I can -- so I can look at them side by side, just so I can point out the differences. 12:47:49 12:47:52 12:47:54

Give me one second. Let me see if I can do that. Well, let me go through DEMAW-SIM-FIG. 1.2, and I'll do it from memory, and then we'll go back and see if I missed anything. 12:47:57 12:48:00 12:48:15 12:48:18

Okay. So one of the things that we changed was, if you look at -- if would be really better if we -- if we could look at both at the same time. I'm trying to think best how to do this. 12:48:20 12:48:26 12:48:33 12:48:36 12:48:40

I'm going to just take a screen shot, if you don't mind, of the -- of the other circuit. 12:48:42 12:48:44

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I'm sorry. 12:48:49

Q I don't mean to interrupt you. If I send you another Exhibit 1 would you be able to pull that up and then share -- look at two pages at the same time? 12:48:50 12:48:54 12:48:56 12:48:59

A Yeah, the problem is that my stupid PDF reader doesn't -- doesn't do that. I can -- I can do it. Just give me a second. I can do it a different way. I'm just going to take a screen shot of one and put it next to the other. Sorry about that. 12:48:59 12:49:04 12:49:08 12:49:11 12:49:13 12:49:17

Q All right. Just to clarify, you're putting a screen shot of DEMAW-SIM-FIG. 1 Revised in your second declaration versus a screen shot of DEMAW-SIM-FIG. 1.2? 12:49:25 12:49:26 12:49:33 12:49:36

A Yeah, I was going to do a different one, but I can do that. Give me a second. 12:49:38 12:49:40

Q Just so we know what we're looking at. 12:49:44

A So I'm going to do, just as you said, I'm going to do a screen shot of DeMaw-FIG -- DEMAW-SIM-FIG. 1 Revised Annotated, so I'm going to take that screen shot. Give me a second. 12:49:47 12:49:49 12:49:56 12:50:02

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Okay. Let me open that. Sorry about this. 12:50:12

MS. MANDIR: Why don't we go off the record for a second. I think I have a better way to figure this out. 12:50:21 12:50:22 12:50:24

THE WITNESS: Okay. 12:50:26

VIDEO SPECIALIST: Okay. We are going off the record. The time is 12:50. 12:50:28 12:50:29

(A recess was taken.) 12:50:31

VIDEO SPECIALIST: And we are back on the record. The time is 12:59. 12:59:21 12:59:28

BY MS. MANDIR: 12:59:32

Q So, Dr. Galton, did you speak with anyone about the substance of your deposition during the break? 12:59:32 12:59:35 12:59:37

A No. I made coffee. 12:59:38

Q Okay. 12:59:41

(Galton Deposition Exhibit 3 marked for identification and is attached to the transcript.) 12:59:41 12:59:43

Q And I shared with you a document that will be Exhibit 3 to your deposition. 12:59:43 12:59:45

And Exhibit 3 is a snippet of DEMAW-SIM-FIG. 1 (revised, clean) of your second 12:59:49 12:59:53

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declaration and a snippet of DEMAW-SIM-FIG. 1.2 of your second declaration. 12:59:59 13:00:05

Do you see that? 13:00:07

A I do. 13:00:08

Q And you said that you made some changes to the simulation in Section 2, which is where we find DEMAW-SIM-FIG. 1 of your second declaration to the figure DEMAW-SIM-FIG. 1.2 which is in Section 3 of your declaration. Correct? 13:00:08 13:00:21 13:00:26 13:00:32 13:00:38

A Yes. 13:00:44

Q And can you walk me through the differences between DEMAW-SIM-FIG. 1 to DEMAW-SIM-FIG. 1.2? 13:00:44 13:00:46 13:00:51

A Sure. Okay. So one of the changes is, if you look in the lower left where you see on the original figure, the top figure, a V4 voltage generator and R4, which is a resistor. 13:00:54 13:00:59 13:01:02 13:01:11

We've replaced the original resistor in that voltage generator with a bigger resistor. And that -- and we adjusted the resistance value of R4 to get the correct bias that was indicated in DeMaw. 13:01:17 13:01:19 13:01:23 13:01:26 13:01:31

Previously what we were doing was just using the voltage source to get that correct bias. And from a circuit point of view, there's -- or from a functionality point of view, there is very little difference; it's just that the voltage method was more convenient. 13:01:32 13:01:34 13:01:37 13:01:43 13:01:45 13:01:47

But whether -- in the POPR, when I was criticized for -- or accused of choosing values to get the numbers that I wanted, I realized it would be good to just do it exactly like as described in the -- in the document. So that's one of the changes. 13:01:49 13:01:53 13:02:00 13:02:05 13:02:09 13:02:11

Another change was in the V supply down in the lower right, above that is a 33-ohm resistor in the new circuit and a 5-ohm resistor in the other circuit. And -- yeah. So that -- that is what's called a decoupling network for the supply. And we just chose different values. It doesn't really change anything. But we put it to exactly what was specified in DeMaw Figure 6.7. 13:02:11 13:02:16 13:02:20 13:02:23 13:02:31 13:02:35 13:02:38 13:02:40

And I think we also changed -- give me one second. I want to just look at the numbers. 13:02:47 13:02:51

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Yeah. We changed the LO frequency and the RF frequency. Let me just double-check this. Yeah, to better match what was described in DeMaw figure -- in DeMaw. 13:02:54 13:03:01 13:03:06 13:03:09

So I believe those are all the changes. I don't recall any others. Oh, wait. Hold -- no. Oh, yeah. We also, if you look up at the top voltage supplies sources that the LO -- the LO voltage V2, we have a different resistor. We have a 50-ohm resistor feeding into a .01-microfarad capacitor in the second diagram and not in the first. Again it doesn't make much of a difference, but we wanted to hew as closely as possible to what was described in DeMaw. 13:03:11 13:03:14 13:03:19 13:03:24 13:03:29 13:03:34 13:03:39 13:03:42 13:03:44 13:03:50

Q Okay. So just to go through those points again. 13:03:52 13:03:55

In Figure 1.2 you replaced the bias voltage V4 and Resistor R4 which had a 5-ohm resistance, with a 1.6-kilohm resistor, R4. 13:03:57 13:04:05 13:04:14

Correct? 13:04:21

A Yes. 13:04:29

Q And you also -- strike that. 13:04:29

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In Figure 1.2 you increased the VDD supply resistor V2 from 5 ohms to 33 ohms. Correct? 13:04:31 13:04:38 13:04:41

A It's R2, but yes. 13:04:42

Q Sorry. Let me correct that. Strike that. 13:04:44 13:04:50

In Figure 1.2 you increased the VDD supply resistor R2 from 5 ohms to 33 ohms. 13:04:52 13:04:56

Correct? 13:04:59

A Yes. 13:05:00

Q And in Figure 1.2 you added R3, which is a 50-ohm source impedance at the LO input. 13:05:00 13:05:15

Correct? 13:05:19

A That is correct. 13:05:20

Q And in Figure 1.2 you changed the RF frequency from originally 123 megahertz to 150 megahertz. 13:05:20 13:05:32 13:05:45

Is that correct? 13:05:47

A Yes. It's 123.102, but yes. 13:05:48

Q So in Figure 1.2 you changed the RF frequency from 123.102 megahertz to 150 megahertz. 13:05:53 13:06:00

Correct? 13:06:07

A That is correct. 13:06:07

Q And you also changed the LO frequency 13:06:08

from 150 megahertz to 119.8 megahertz. Correct? 13:06:14

A Yes. 13:06:22

Q And looking at the difference between 13:06:23

Figure 1 and Figure 1.2 -- 13:06:32

A Can I stop you for one second? I'm so 13:06:35

sorry. I just remembered one other change. Can 13:06:38

I -- can I say it, or do you want to continue? 13:06:40

Q Let me continue my question, and I 13:06:42

probably will bring up the change that you're now 13:06:44

seeing. So strike that. 13:06:47

In Figure 1.2 it looks like you changed 13:06:48

the LO amplitude from 1.2 volts to .785 volts. 13:06:51

Is that correct? 13:06:59

A Give me one second. Yes. 13:07:01

Q And in Figure 1.2 compared to Figure 1, 13:07:11

it also looks like you changed the values of 13:07:18

Inductors 1, L1, L2, L3, L4, L5, and L6 from 400 13:07:23

microhenries to 4 microhenries. 13:07:32

Is that correct? 13:07:34

A Yes, that is correct. I forgot about 13:07:36

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that change. 13:07:39

So yeah, sorry for not noticing that, or 13:07:41

not remembering that. 13:07:44

And then the one additional change which 13:07:45

is, if you look at the transformers, so the 13:07:47

transformers are L1 and L2. That's one of the 13:07:54

transformers. L3-L4 is another. L5-L6 is 13:07:57

another. And L9-L10 11 -- L9-L10, and 11 is 13:08:01

another transformer. 13:08:09

And in all those cases we changed the 13:08:11

last value of the parameter -- parameters at the 13:08:12

top in text from 1 to .99. And that makes no 13:08:15

substantial difference, but by making them ever so 13:08:19

slightly nonideal it just -- it just made the 13:08:22

simulator converge better. 13:08:25

So -- so there are some cases when you 13:08:27

run circuit simulations where when you have ideal 13:08:29

components it occasionally doesn't -- doesn't 13:08:33

converge. And then you have to change initial 13:08:36

conditions and run it again. 13:08:39

So we just -- we just found that making 13:08:41

it .99, which is actually more realistic anyway, 13:08:43

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reduced that problem. 13:08:46

Hold on. We're having an earthquake. 13:08:49

Give me a second. 13:08:53

VIDEO SPECIALIST: Should we go off the 13:08:58

record? 13:08:59

MS. MANDIR: Yeah, let's go off the 13:09:00

record. 13:09:01

VIDEO SPECIALIST: We are going off the 13:09:01

record. The time is 13:09. 13:09:03

(A recess was taken.) 13:09:05

VIDEO SPECIALIST: And we are back on the 13:14:05

record. The time is 13:14. 13:14:07

BY MS. MANDIR: 13:14:11

Q Dr. Galton, before the earthquake 13:14:11

happened we were discussing some of the changes 13:14:14

that you've made between the DeMaw Figure 1 13:14:17

revised in your declaration and DeMaw Figure 1.2 13:14:23

in your second declaration. Correct? 13:14:29

A Yes. 13:14:30

Q And I think we had gone through most of 13:14:30

the changes, but we were interrupted by the 13:14:33

earthquake. 13:14:35

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Do you remember specifically we were talking about the parameters of the transformers being .99 instead of the ideal 1. Correct? 13:14:38 13:14:41 13:14:44

A Yes. Yes. 13:14:49

Q Were there any other changes or modifications made to Fig 1 Revised in your second declaration to Fig 1.2 that we have not already discussed? 13:14:51 13:14:57 13:15:02 13:15:08

A I do not believe so. 13:15:09

Q Let's see. So it looks like in Fig 1.2 of DeMaw on your second declaration you replaced the inductors LO9, LO10, and -- strike that. 13:15:10 13:15:28 13:15:35

In Fig 1.2 of your second declaration you replaced inductors L9, L10, and L11, which were originally 600 microhenries, to inductors with 4 microhenries. 13:15:43 13:15:46 13:15:51 13:15:57

Is that correct? 13:15:58

MR. MAGEE: Objection to form. 13:15:59

A They're not inductors; they're windings on the transformer. But they -- but they do have different values. 13:16:00 13:16:02 13:16:05

Q And those values changed from 600 13:16:14

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microhenries to 4 microhenries. Correct? 13:16:17

MR. MAGEE: Objection to form. 13:16:20

A The transformer windings changed from 600 microhenries to 4 microhenries, that is correct. 13:16:22 13:16:25

Q And in Section 4 of your second declaration, which is Exhibit 1. If you can turn back to Exhibit 1 of your deposition today. 13:16:28 13:16:35 13:16:42

Section 4 of your second declaration is titled DeMaw Circuit Modified to Match DeMaw Fig 6.7 with the Sinusoidal LO. 13:16:46 13:16:48 13:16:54

Do you see that? 13:16:57

A You said -- give me one second. What page is that on, I'm sorry? 13:16:58 13:17:00

Q This is Exhibit 1 of your deposition, which is your second declaration. And this would be Section 4 of your second declaration, which is entitled DeMaw Circuit Modified to Match DeMaw's Fig 6.7 with the Sinusoidal LO. 13:17:01 13:17:02 13:17:06 13:17:10 13:17:15

A Right. Can you just give me a page number so it's easier for me to find it? 13:17:17 13:17:19

Q Page 50 of your second declaration. 13:17:24

A Okay, I'm there. 13:17:30

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Q And in Section 4 of your second declaration, you use a sinusoidal LO in place of a squared-up LO to simulate the circuit behavior of the DeMaw circuit. Correct? 13:17:31 13:17:36 13:17:40 13:17:48

A Yes. 13:17:49

Q And as shown in DEMAW-SIM-FIG. 1.7, you use the same modified circuit that we just went through in Section 3, but replaced the squared-up LO with a sinusoidal LO. Correct? 13:17:50 13:17:58 13:18:01 13:18:05

A Yes. 13:18:08

Q And each of the variations of Section 3 and Section 4 have the same modified circuit outside of different input signals. Correct? 13:18:08 13:18:33 13:18:40

A Yes. 13:18:45

Q Where in your second declaration do you show a waveform of the charging and discharging of the capacitors? 13:18:45 13:18:56 13:19:00

A Give me one second. 13:19:04

MR. MAGEE: Objection to form. 13:19:11

A Well, we show the discharge ratios, the charge loss ratios, on the histograms. We show the -- give me one second here. 13:19:19 13:19:24 13:19:29

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We show the voltages at the J1 source and J2 source in Figure 4.7. But I don't think -- I don't think we actually have a plot of the charge and discharge waveforms, if memory serves. Let me just look for one other thing. 13:19:35 13:19:42 13:19:49 13:19:51 13:19:57

No, we don't actually plot those wave forms. But what we do plot is the current into the capacitor. 13:19:59 13:20:03 13:20:06

So, for example, in DEMAW-SIM-FIG. 5.8 on Page 59 we show the current into Capacitor C4 and the current into Capacitor C5. And so the integral of those two waveforms is the charge going into the capacitors. 13:20:06 13:20:11 13:20:15 13:20:18 13:20:26

MS. MANDIR: I don't believe I have any more questions for you, Dr. Galton. I appreciate your time. Sorry about the earthquake. And I turn my time over to Bobby if he has any questions. 13:20:53 13:20:56 13:20:57 13:21:01 13:21:04

MR. MAGEE: Can we take just maybe a five-minute break real quick just to let me double-check my notes? 13:21:04 13:21:06 13:21:08

VIDEO SPECIALIST: We are going off the 13:21:10

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record. The time is 13:21. 13:21:11

(A recess was taken.) 13:21:13

VIDEO SPECIALIST: We are back on the record. The time is 13:26. 13:25:56 13:26:01

MR. MAGEE: I don't have any questions, so we'll go ahead and read and sign. 13:26:05 13:26:06

VIDEO SPECIALIST: If there's nothing further, this concludes the deposition of Ian Galton, Ph.D. The time is 13:26. 13:26:09 13:26:10 13:26:14

(Off the record at 1:26 p.m. EDT.)

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ACKNOWLEDGMENT OF DEPONENT

I, IAN GALTON, Ph.D., do hereby acknowledge that I have read and examined the foregoing testimony, and the same is a true, correct and complete transcription of the testimony given by me, and any corrections appear on the attached Errata sheet signed by me.

_____ _____

(DATE) (SIGNATURE)

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C E R T I F I C A T E

I, Debra Ann Whitehead, E-Notary Public in and for the Commonwealth of Virginia, do hereby certify:

That IAN GALTON, Ph.D., the witness whose deposition is hereinbefore set forth, was duly sworn by me before the commencement of such deposition and that such deposition was taken virtually and is a true record of the testimony given by such witness.

I further certify that the adverse party, TEXAS INSTRUMENTS INCORPORATED, was represented by counsel at the deposition.

I further certify that the deposition of IAN GALTON, Ph.D., occurred virtually, on Monday, April 14, 2025, from 12:02 p.m. to 1:26 p.m. EDT.

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I further certify that I am not related to any of the parties to this action by blood or marriage, I am not employed by or an attorney to any of the parties to this action, and that I am in no way interested, financially or otherwise, in the outcome of this matter.

IN WITNESS WHEREOF, I have hereunto set my hand this 14th day of April, 2025.

My commission expires:

October 31, 2027



E-NOTARY PUBLIC IN AND FOR THE

COMMONWEALTH OF VIRGINIA

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EXHIBIT 1

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	David F. Sorrells, et al	Attorney Docket No.: 12189-0090IP1
U.S. Patent No.:	7,496,342	IPR2024-00934
Issue Date:	February 24, 2009	
Appl. Serial No.:	10/972,133	
Filing Date:	October 25, 2004	
Title:	DOWN-CONVERTING ELECTROMAGNETIC SIGNALS, INCLUDING CONTROLLED DISCHARGE OF CAPACITORS	

SECOND DECLARATION OF IAN GALTON, PH.D.

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I, Dr. Ian Galton, declare:

I. Overview

1. This document provides an overview of additional simulations performed beyond those described in my original Declaration (TI-1003) in support of the ’342 patent IPR petition. All additional circuits and configurations that have been simulated to support my analysis of the prior art for the ’342 patent beyond those presented in my original Declaration are described in the document, and none of the results change the conclusions presented in my original Declaration regarding the alleged invention disclosed in the ’342 patent.

2. All of the files necessary to duplicate the results presented below along with additional text files that provide relevant instructions and information are being provided with this Second Declaration.

II. DeMaw Circuit With Siliconix U430 JFET Models

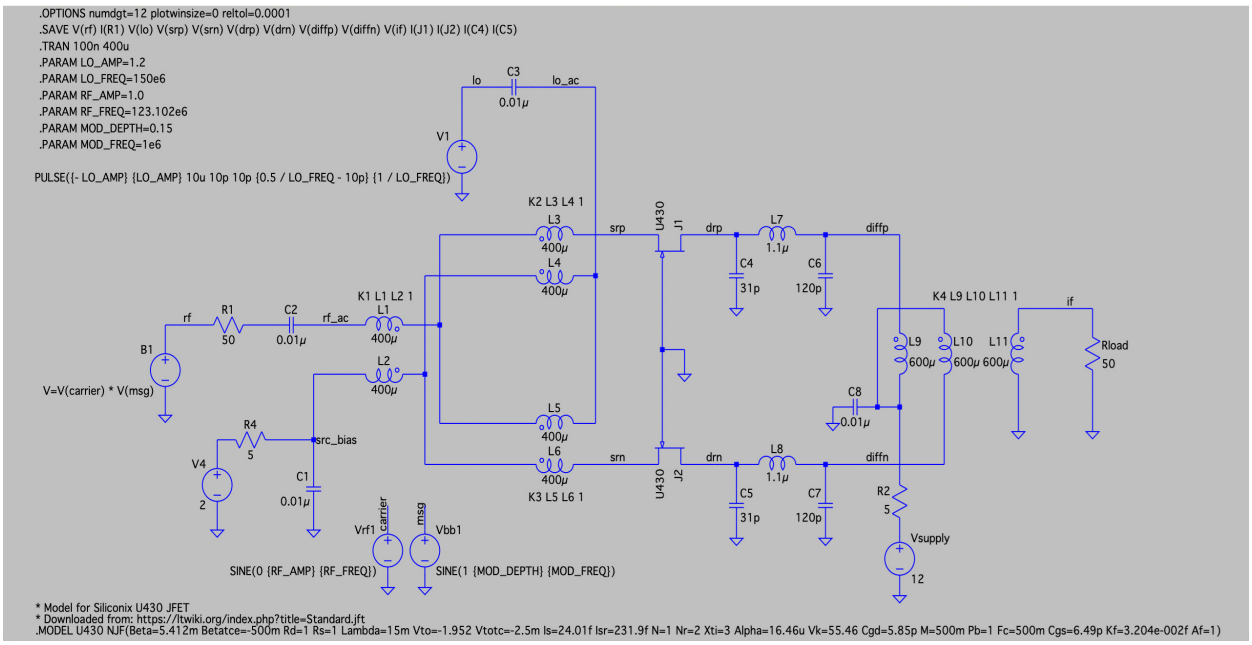
3. My original Declaration mentioned that the DeMaw circuit had been simulated with Siliconix U430 JFET models. However, the circuit was inadvertently simulated with default, generic LTspice JFET models. The first set of simulation results shown in **Part A** of this section correspond to the same version of the DeMaw circuit, the same input, and the same local oscillator (LO) signals that were described in my original Declaration, except with the Siliconix U430 JFET models.

4. Using the Siliconix U430 JFET models in place of the generic LTspice

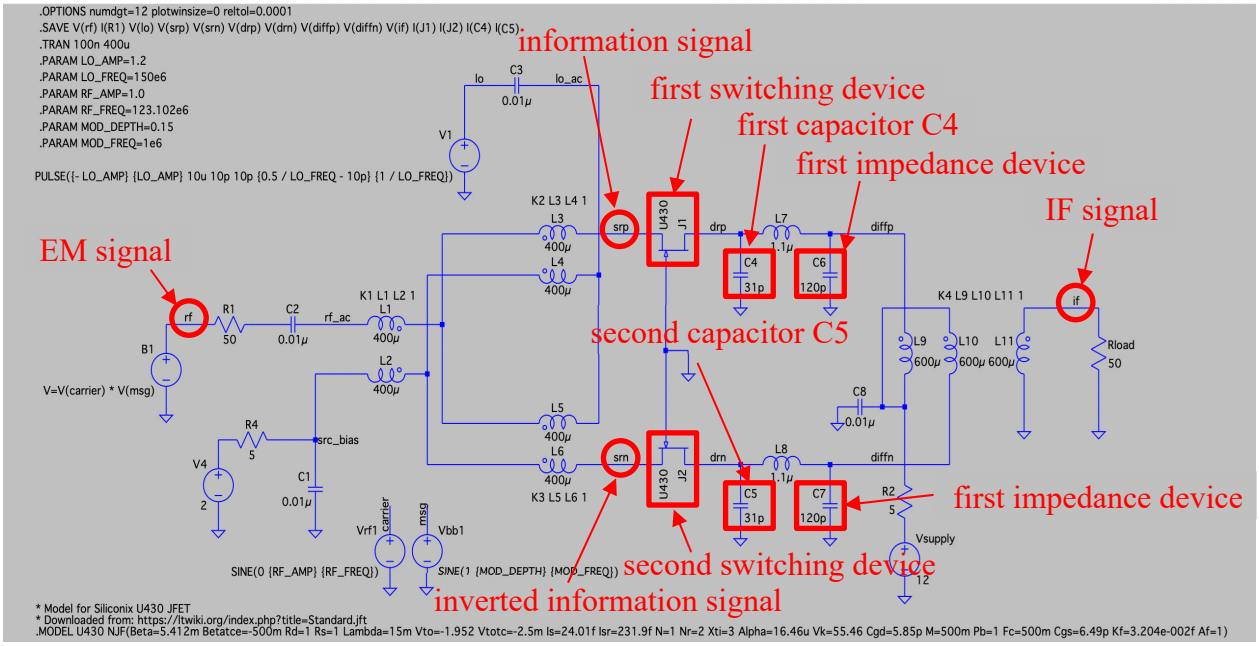
JFET models resulted in a significant increase in mixer gain. To ensure that the increase in mixer gain did not cause the mixer to operate above its compression point (i.e., outside of its linear region), the second set of simulation results shown in **Part B** of this section correspond to exactly the circuit configuration and LO signal as in the simulation results shown in **Part A** except with a 6 dB lower-power input signal. As can be seen from the results presented below, using the 6 dB lower-power input signal reduced the mixer's output signal power by 6 dB, thereby indicating that the mixer was not operating above its compression point when simulated to generate the Part A results.

A. Simulation of DeMaw Circuit Using Siliconix U430 JFET Models

5. DEMAW-SIM-FIG. 1 (revised, clean), below, is a graphical representation of the LTspice simulation of the DeMaw Figure 6.7 circuit using the Siliconix U430 JFET models. DEMAW-SIM-FIG. 1 (revised, annotated) is an annotated version that identifies the elements of claim 18 and corresponds to DEMAW-SIM-FIG. 1 in my original Declaration. Everything I wrote in my original Declaration about DEMAW-SIM-FIG. 1 is true of DEMAW-SIM-FIG. 1 (revised).



DEMAW-SIM-FIG. 1 (revised, clean). DeMaw circuit as described in the original Declaration but with U430 JFET models (highlighting two capacitors).

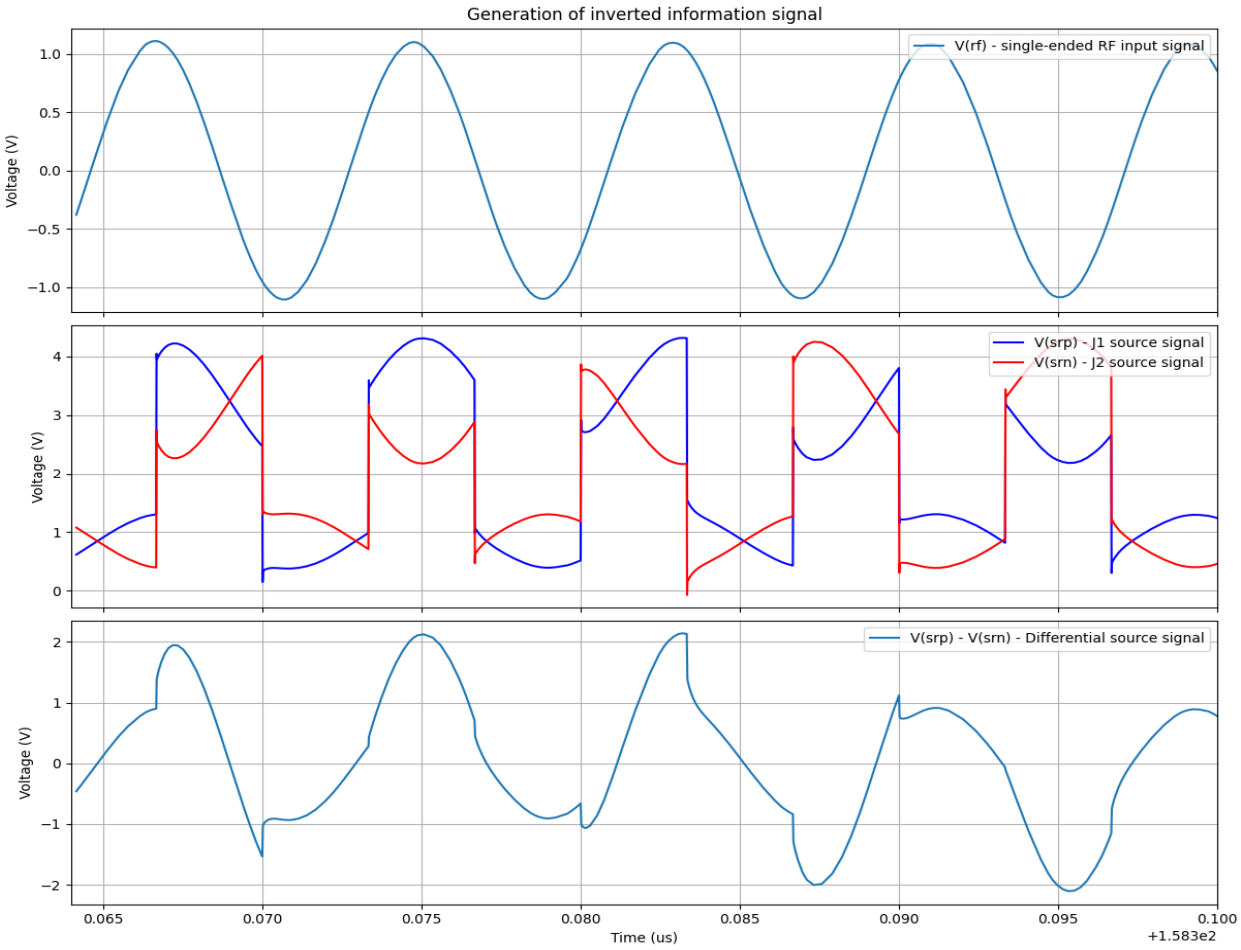


DEMAW-SIM-FIG. 1 (revised, annotated).

6. As I mentioned already, the circuit simulation above is structurally the

same as the simulation I provided in my previous declaration. Therefore, I only provide one annotation to the updated DeMaw circuit simulation graphic showing the structural elements (including the U430 JFETs), even though I also provide further simulations using different input values and circuit component values.

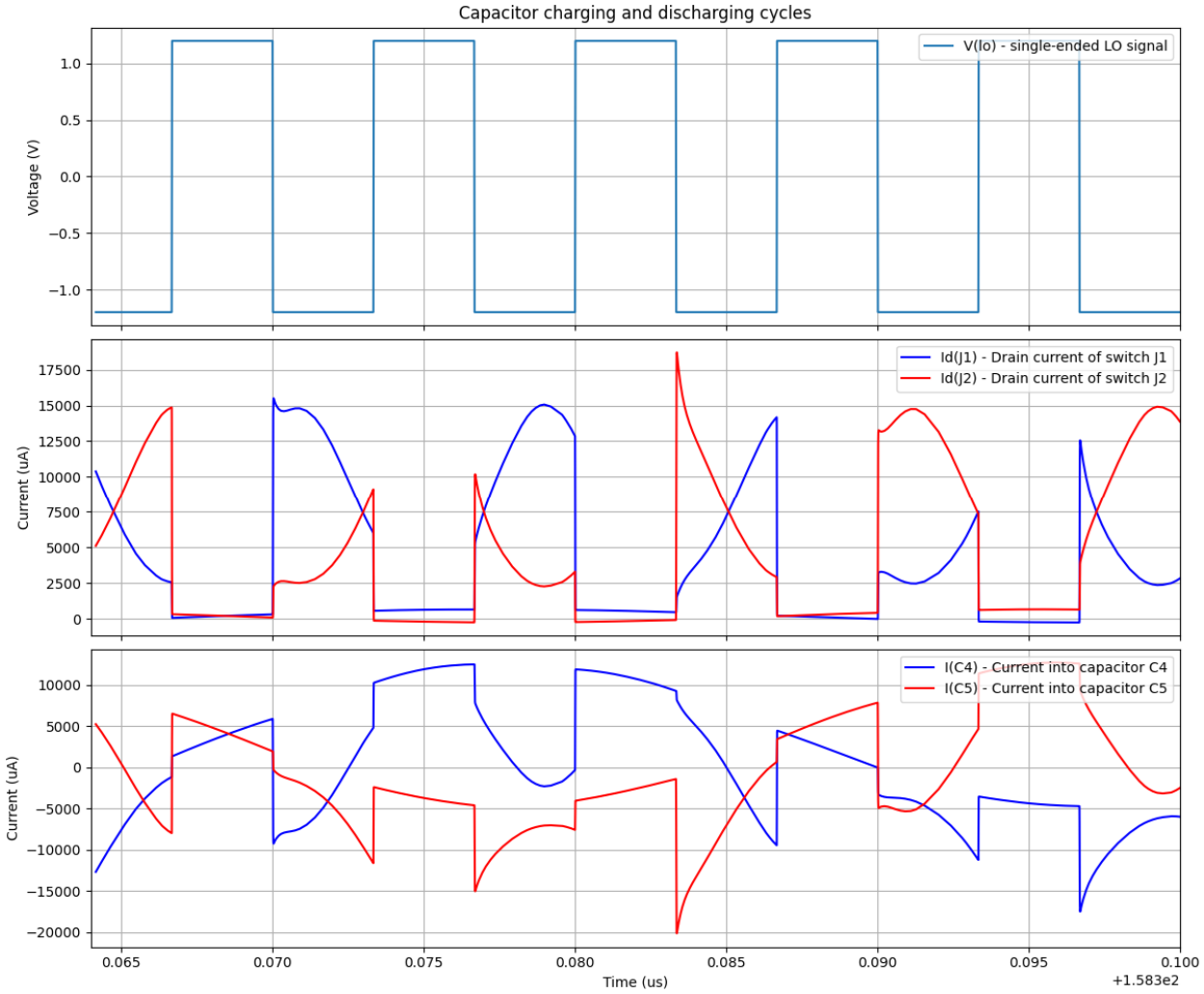
7. DEMAW-SIM-FIG. 4 (revised) is a graphical representation of the generation of the inverted information signal of the DeMaw circuit simulation of DEMAW-SIM-FIG. 1 (revised). The revised version additionally shows V(rf), the single ended RF input signal, and V(srp)-V(sm), the differential source signal. The information signal and inverted information signal correspond to claims 18.1-18.2. Everything I wrote in my original Declaration about DEMAW-SIM-FIG. 4 is true of this revised version.



DEMAW-SIM-FIG. 4. Graphical representation of the generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1 (revised)).

8. DEMAW-SIM-FIG. 5 (revised) is a graphical representation of the charging and discharging cycles of both of the capacitors C4 and C5 highlighted in the DeMaw circuit of DEMAW-SIM-FIG. 1 (revised). DEMAW-SIM-FIG. 5 (revised) is applicable to elements 18.3-18.6, as well as claims 19-21. Everything I wrote in my original Declaration about DEMAW-SIM-FIG. 5 is true of this revised version. I noticed a typographical error in paragraphs 102-104 of the original Declaration where it mistakenly refers to “DEMAW-SIM-FIG. 4” when it should

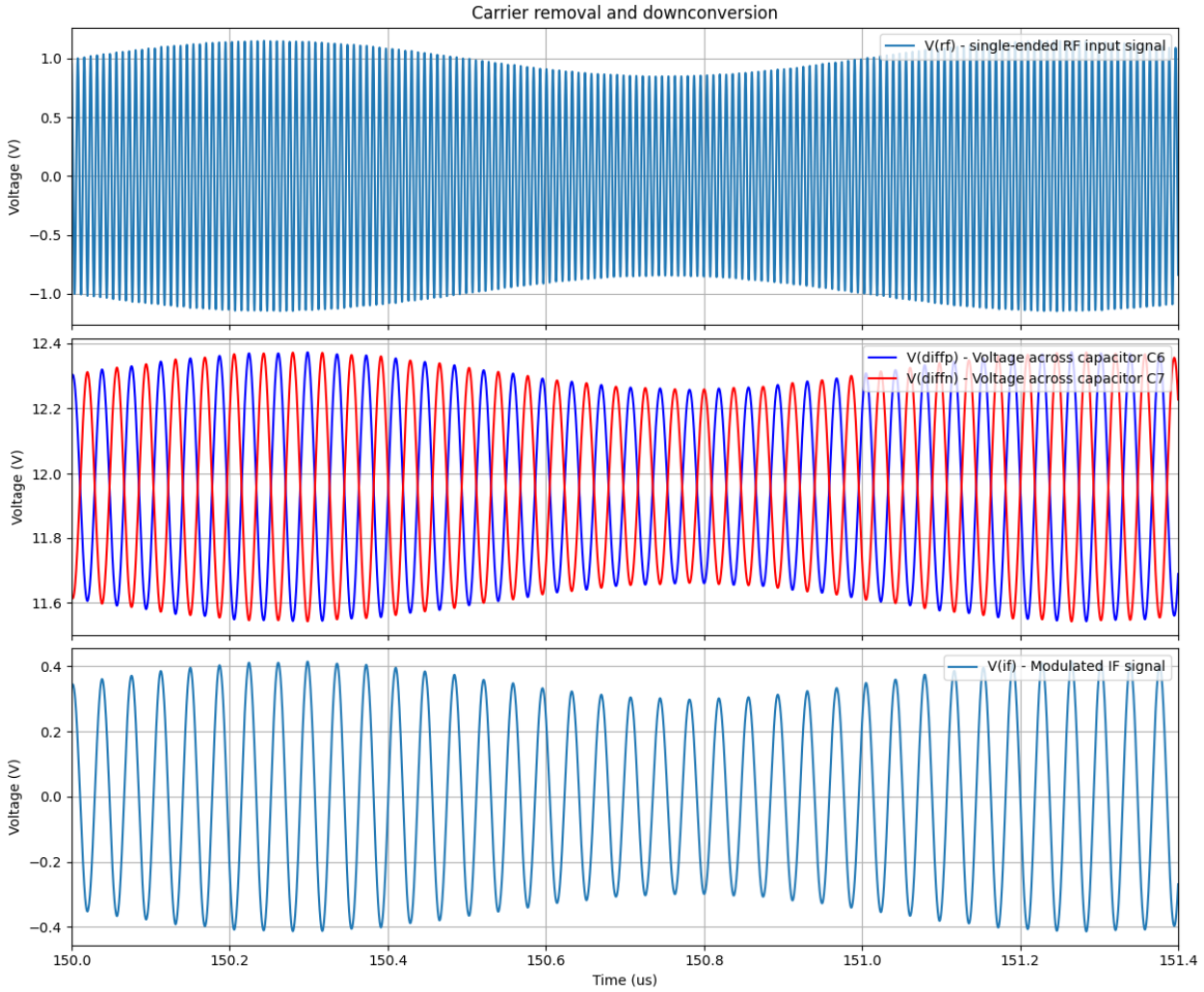
have referred to DEMAW-SIM-FIG. 5, because paragraphs 102-104 describe and reproduce the content of DEMAW-SIM-FIG. 5, not DEMAW-SIM-FIG 4. Additionally, in paragraph 108, an annotated version of DEMAW-SIM-FIG. 5 is mislabeled as "DEMAW-SIM-FIG 4 (annotated)."



DEMAW-SIM-FIG. 5 (revised). Graphical representation of the charging and discharging cycles of both of the capacitors highlighted in the DeMaw circuit of DEMAW-SIM-FIG. 1 (revised).

9. DEMAW-SIM-FIG. 6 (revised) is a graphical representation showing

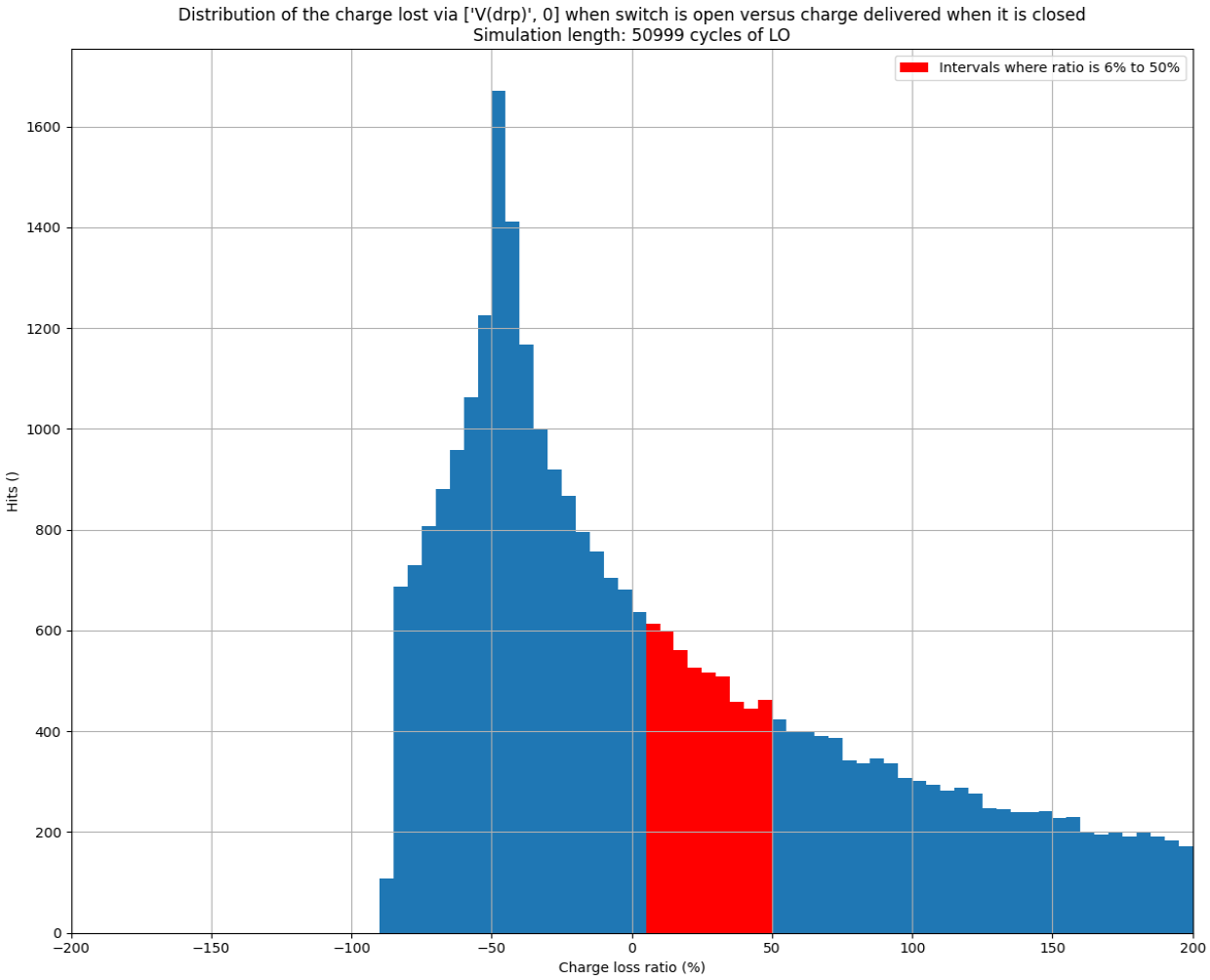
the carrier removal and down-conversion. DEMAW-SIM-FIG. 6 (revised) is applicable to claims 18.5 and 23 (both of which I understand are statutorily disclaimed. Everything I wrote in my original Declaration about DEMAW-SIM-FIG. 6 is true of this revised version. I noticed a typographical error in paragraph 110 of the original Declaration where it mistakenly reproduces a portion of DEMAW-SIM-FIG. 6 labeled as "DEMAW-SIM-FIG. 5." The correction to the mistake is clear, however, because the graph mislabeled as DEMAW-SIM-FIG. 5 is clearly a portion of DEMAW-SIM-FIG. 6.



DEMAW-SIM-FIG. 6 (revised). Graphical representation of the carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1 (revised)).

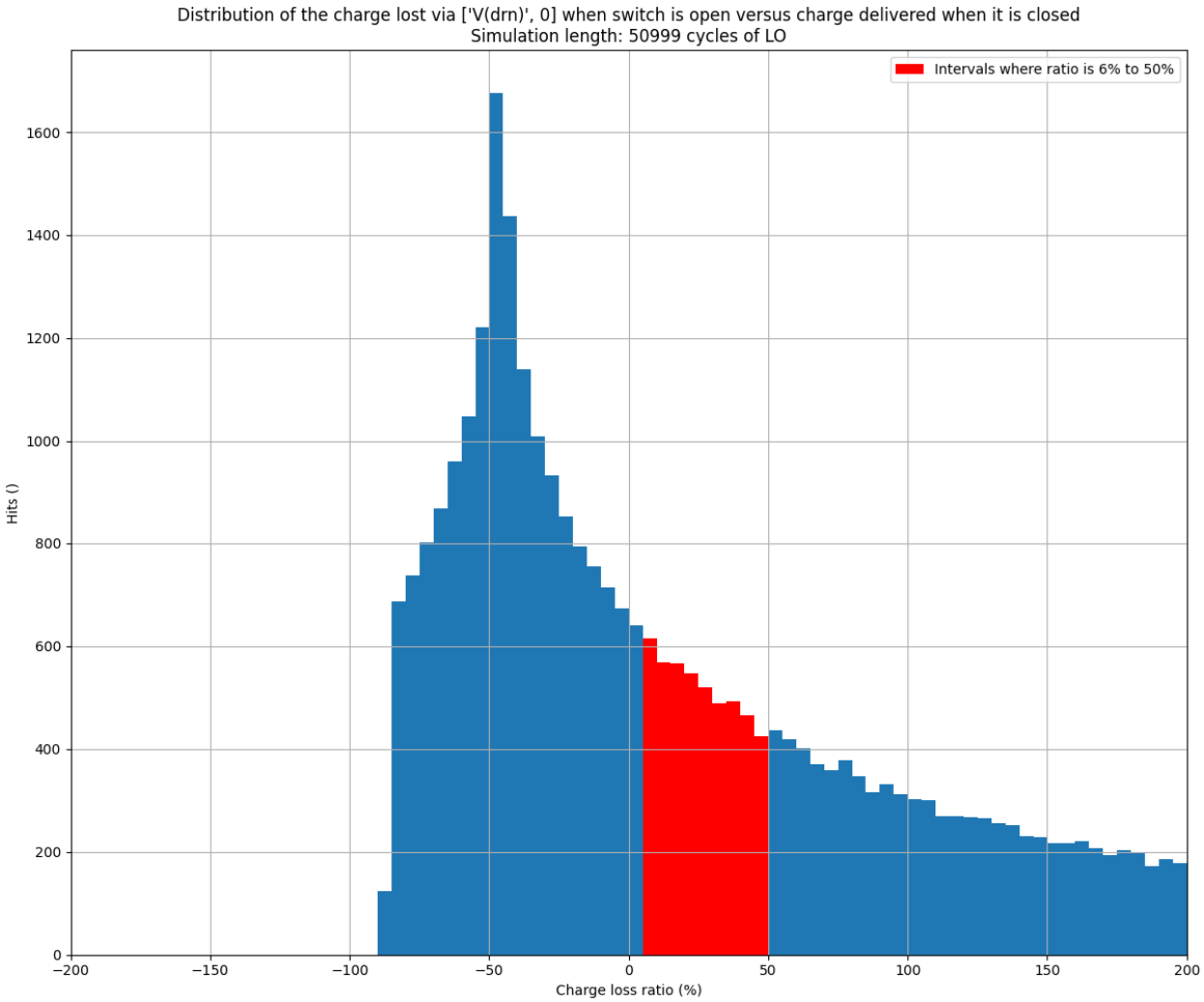
10. In my original Declaration, I provided one histogram of the charge loss ratio percentages that was representative of capacitors C4 and C5 (DEMAW-SIM-FIG. 7). I have generated two histograms here; one for each capacitor DEMAW-SIM-FIG. 7A and 7B. Everything I wrote in my original Declaration about DEMAW-SIM-FIG. 7 is true of DEMAW-SIM-FIG. 7A and 7B (revised). DEMAW-SIM-FIG. 7A (revised) is a histogram showing the charge loss ratio percentages for

the first capacitor C4 of the circuit of DEMAW-SIM-FIG. 1 (revised).



DEMAW-SIM-FIG. 7A (revised). Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1 (revised)).

11. DEMAW-SIM-FIG. 7B (revised) is a histogram of the charge loss ratio percentages for the second capacitor C5 of the circuit of the circuit of DEMAW-SIM-FIG. 1 (revised).

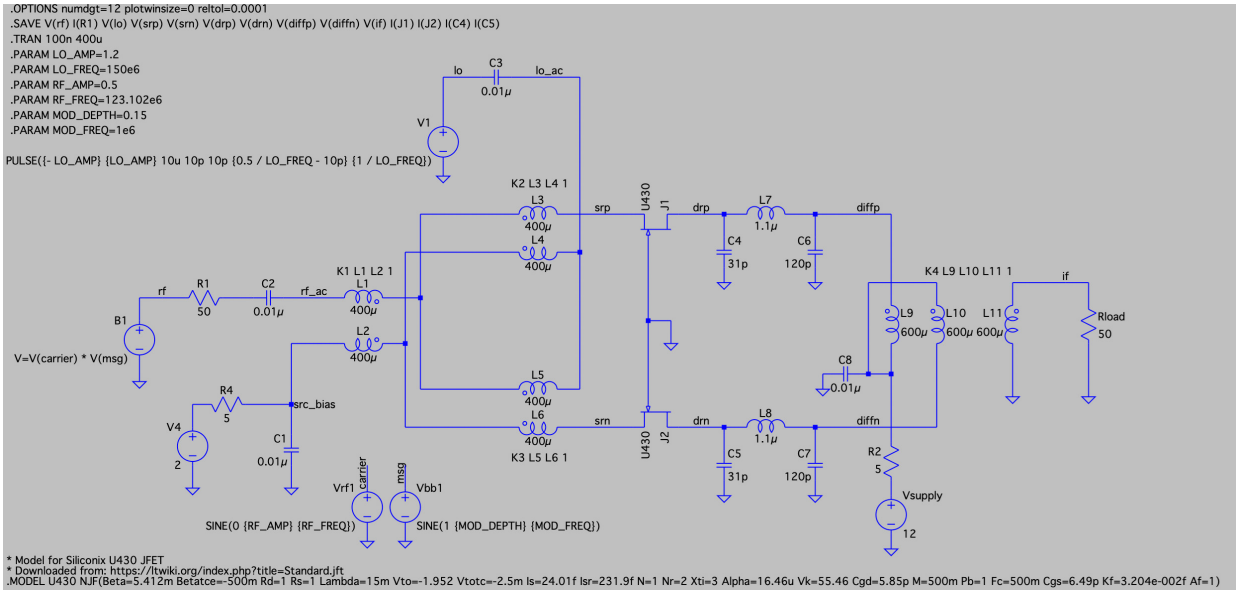


DEMAW-SIM-FIG. 7B (revised). Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1 (revised)).

B. DeMaw Circuit Simulation of DEMAW-SIM-FIG. 1 (revised) Using Smaller Input Signal

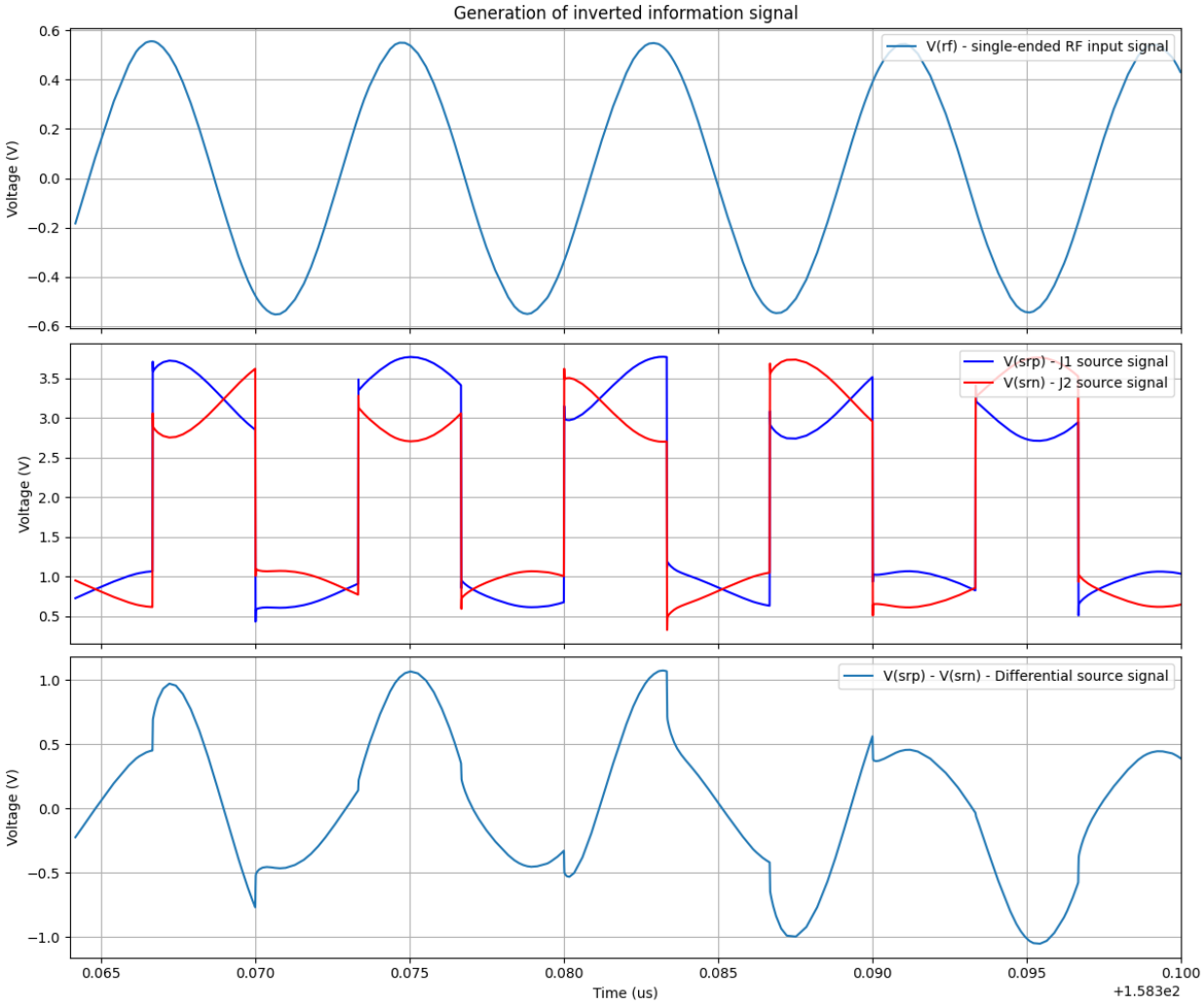
12. DEMAW-SIM-FIG. 1.1 is a graphical representation of the LTspice simulation of the DeMaw Figure 6.7 circuit using the Siliconix U430 JFET models (as shown in DEMAW-SIM-FIG. 1 (revised)), but with a smaller input signal amplitude. I have created additional figures DEMAW-SIM-FIGS. 4.1, 5.1, 6.1, 7.1A

and 7.1B based on simulation output from DEMAW-SIM-FIG. 1.1. DEMAW-SIM-FIGS. 4.1, 5.1, 6.1, 7.1A and 7.1B respectively show the same simulation output from DEMAW-SIM-FIG. 1.1 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIGS. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.1, 4.1, 5.1, 6.1, 7.1A and 7.1B.



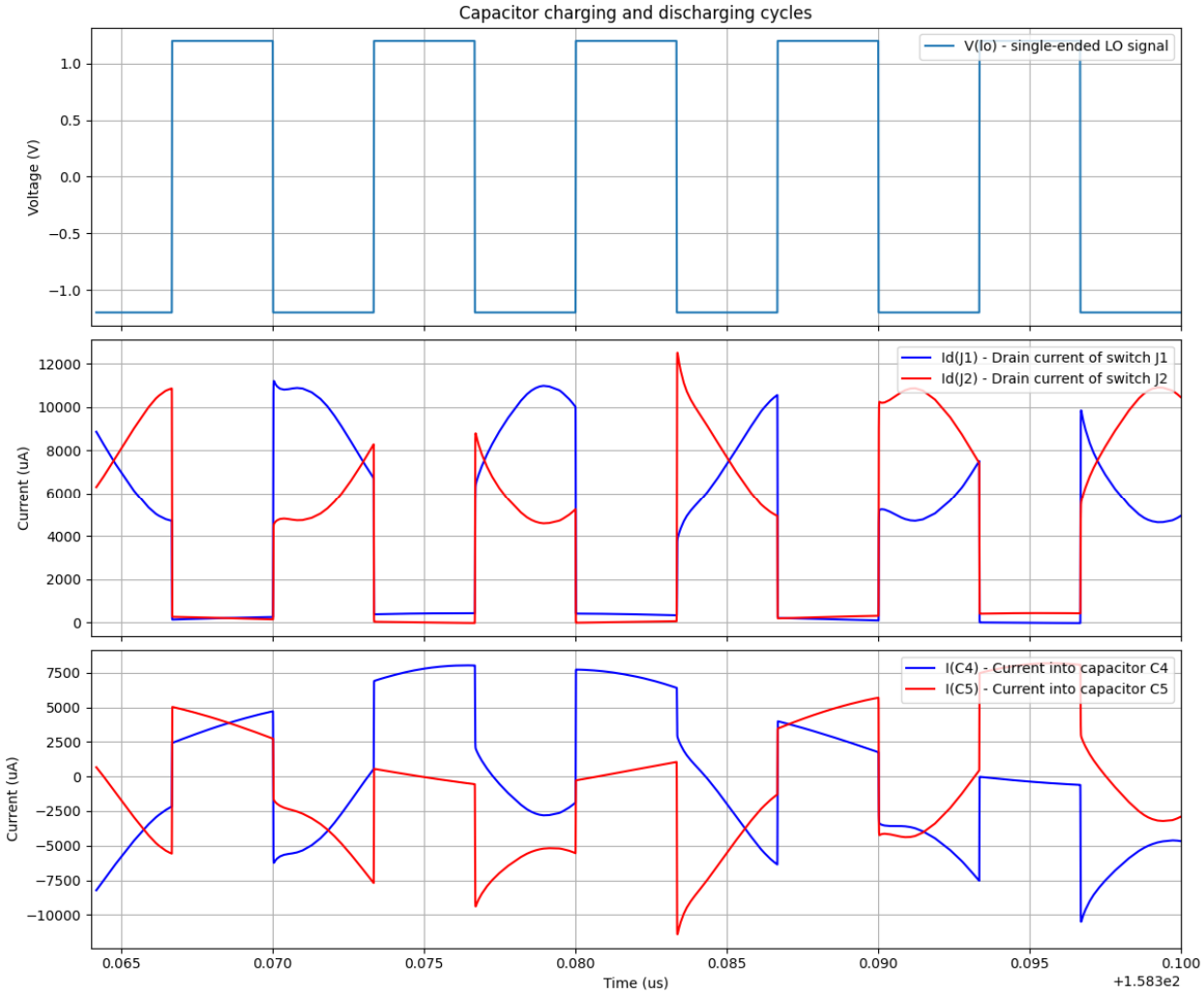
DEMAW-SIM-FIG. 1.1. DeMaw circuit as described in the original Declaration except with U430 JFET Models and reduced input signal amplitude.

13. DEMAW-SIM-FIG. 4.1 is a graphical representation of the generation of the inverted information signal of the DeMaw circuit simulation of DEMAW-SIM-FIG. 1.1.



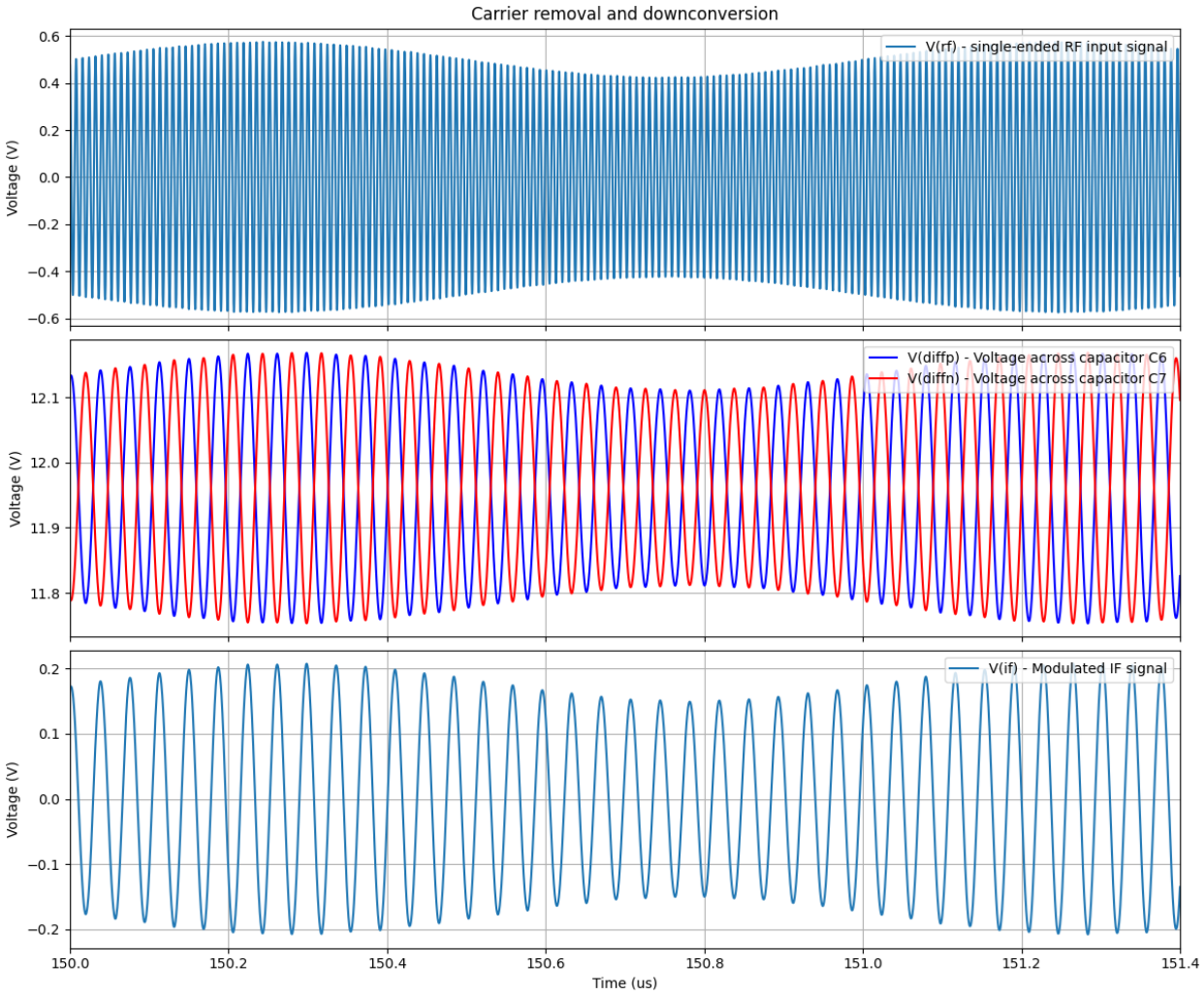
DEMAW-SIM-FIG. 4.1. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.1).

14. DEMAW-SIM-FIG. 5.1 is a graphical representation of the charging and discharging cycles of both of the capacitors C4 and C5 highlighted in the DeMaw circuit of DEMAW-SIM-FIG. 1.1. My conclusions regarding claim elements 18.3-18.6, as well as claims 19-21, based on DEMAW-SIM-FIG. 5 (revised) are likewise supported by DEMAW-SIM-FIG. 5.1.



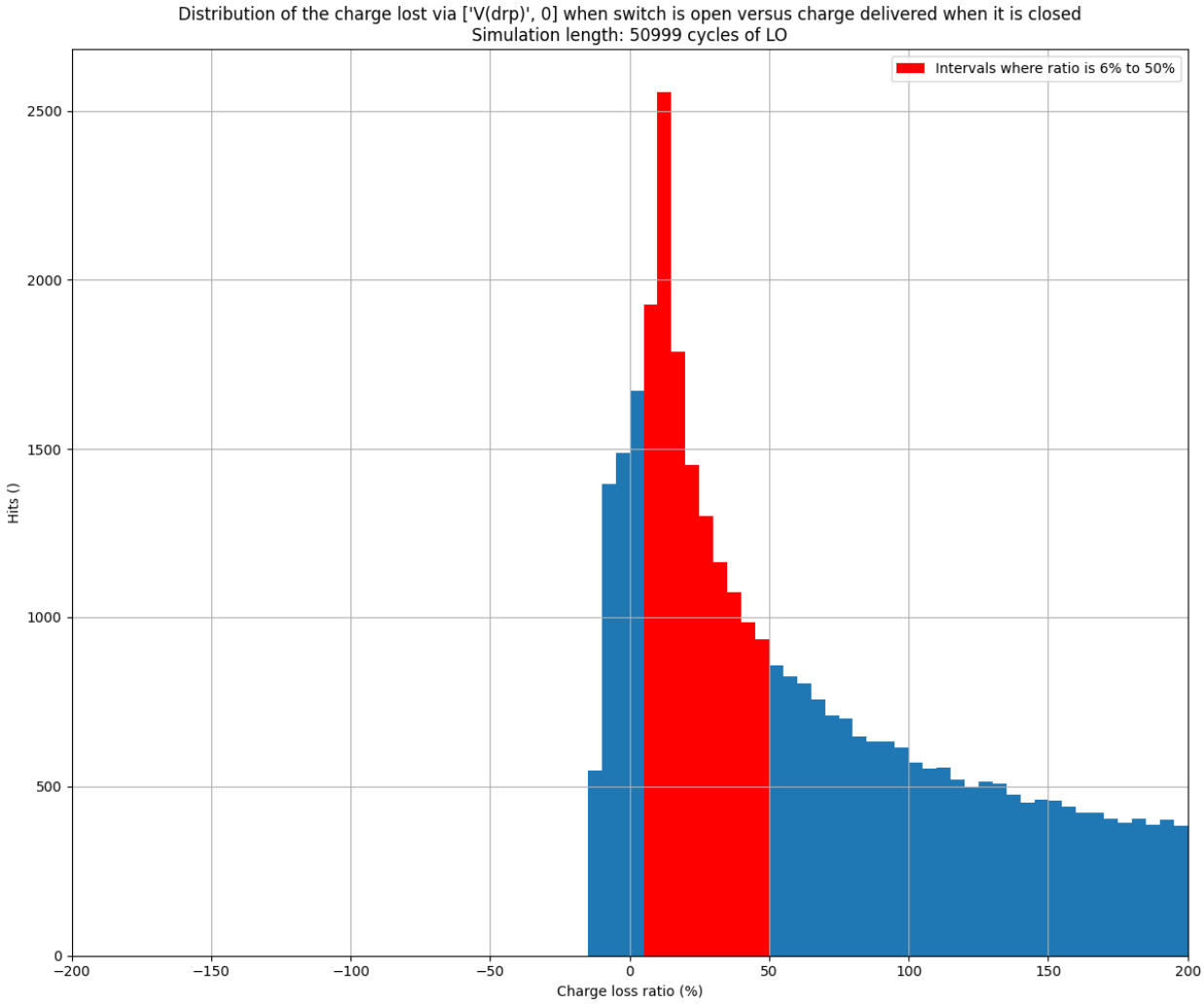
DEMAW-SIM-FIG. 5.1. Graphical representation of the charging and discharging cycles of capacitors C4 and C5 in the DeMaw circuit of DEMAW-SIM-FIG. 1.1.

15. DEMAW-SIM-FIG. 6.1 is a graphical representation showing the carrier removal and down-conversion. My conclusions regarding claim element 18.5 and claim 23 based on DEMAW-SIM-FIG. 6 are likewise supported by DEMAW-SIM-FIG. 6.1.



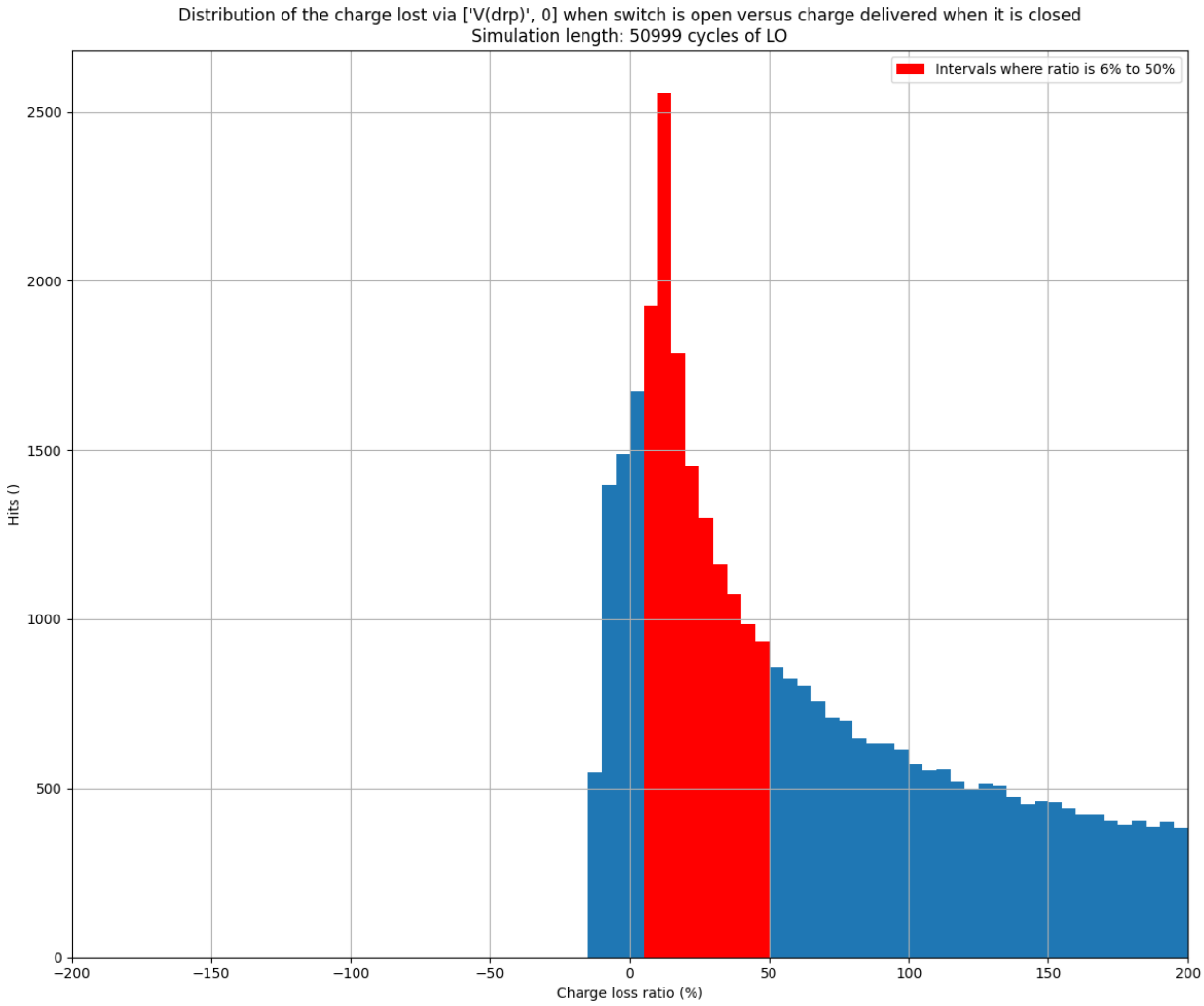
DEMAW-SIM-FIG. 6.1. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.1).

16. DEMAW-SIM-FIG. 7.1A is a histogram showing the charge loss ratio percentages for the first capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.1.



DEMAW-SIM-FIG. 7.1A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.1).

17. DEMAW-SIM-FIG. 7.1B is a histogram of the charge loss ratio percentages for the second capacitor C5 of the circuit of the circuit of DEMAW-SIM-FIG. 1.1.



DEMAW-SIM-FIG. 7.1B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.1).

III. DeMaw Circuit Modified to Match DeMaw FIG. 6.7 With a Squared-Up LO

18. As explained in my original Declaration, the simulated DeMaw circuit had some minor differences relative to the circuit shown in FIG. 6.7 of DeMaw. Although my original Declaration explained why these differences are not significant to the conclusions presented in the original Declaration, the Patent

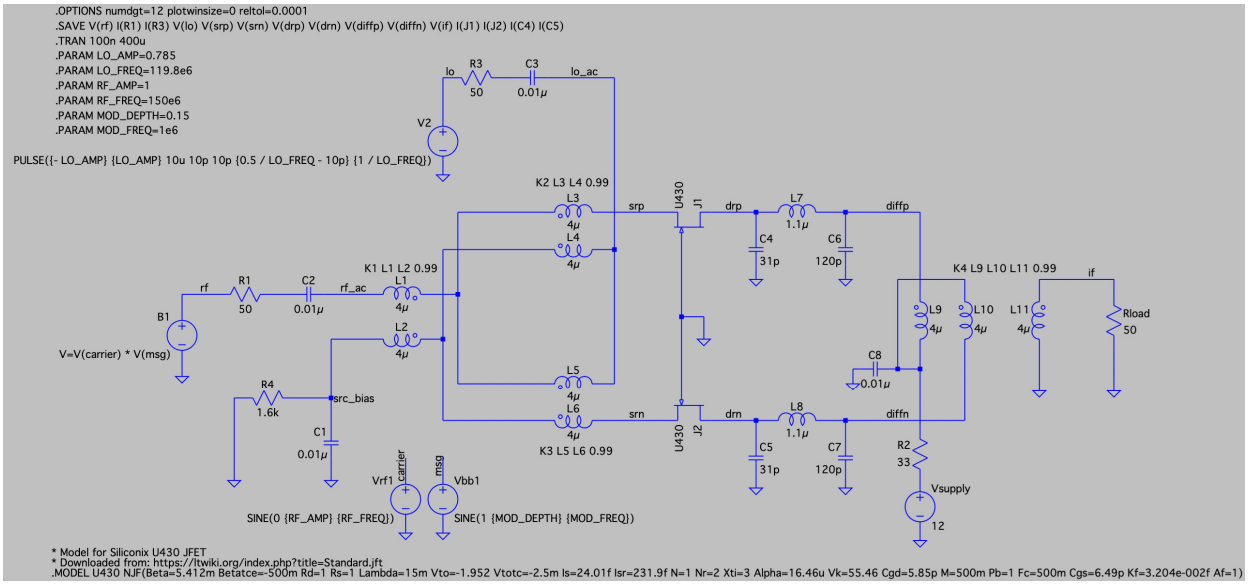
Owner's Preliminary Response (POPR) accused me of having made the circuit different than that shown in FIG. 6.7 of DeMaw to "get the results [that TI] needed." To address this criticism, the set of simulation results presented in this section correspond as closely as possible to the circuit shown in FIG. 6.7 given the information provided in the figure and associated text of DeMaw. Five sets of simulation results are presented which differ only in the power of the RF input to the mixer.

19. The POPR falsely claims that DeMaw "specifically teaches a sinusoidal LO." As I explained in my deposition, it is common practice to use LO signals that approximate square waves (also known as "squared-up" LO signals), so the simulations below use a squared-up LO.

A. Simulation Results For a Large Input Signal

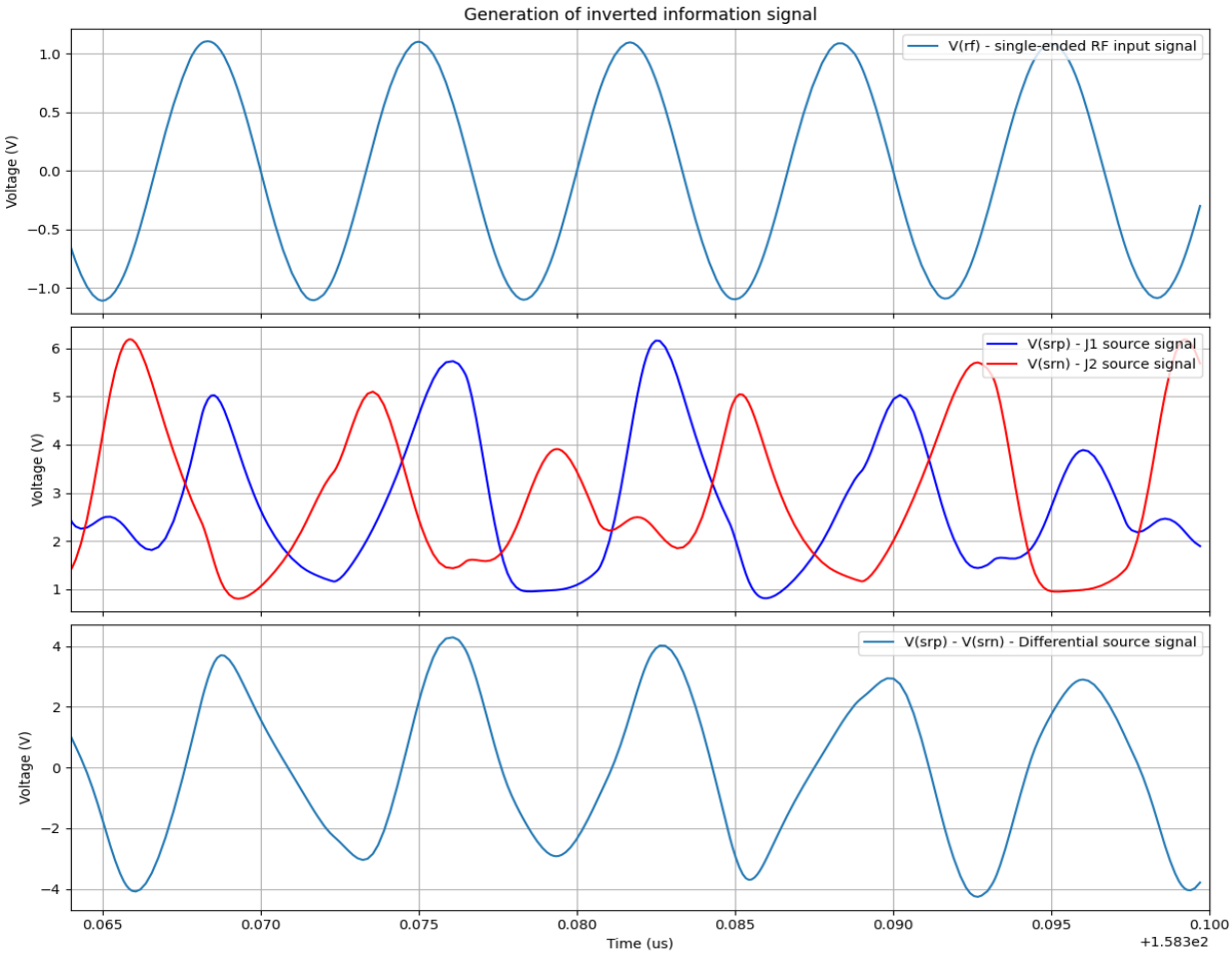
20. DEMAW-SIM-FIG. 1.2 is a schematic representation of the simulated DeMaw Figure 6.7 circuit using a large input signal and a squared-up LO. I have created additional figures DEMAW-SIM-FIGS. 4.2, 5.2, 6.2, 7.2A and 7.2B based on simulation output from DEMAW-SIM-FIG. 1.2. DEMAW-SIM-FIGS. 4.2, 5.2, 6.2, 7.2A and 7.2B show the same simulation output from DEMAW-SIM-FIG. 1.2 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.2, 4.2,

5.2, 6.2, 7.2A and 7.2B.



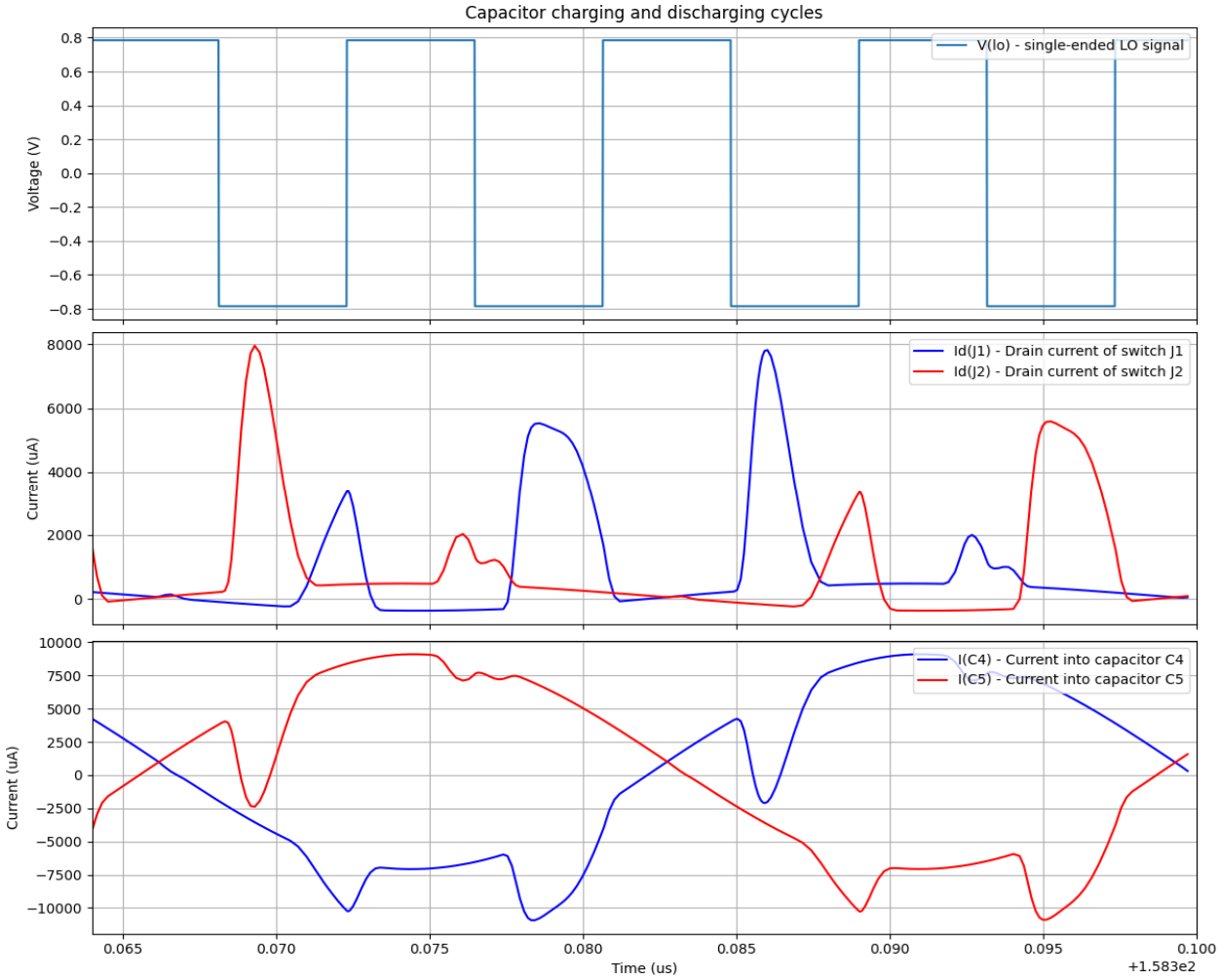
DEMAW-SIM-FIG. 1.2. DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and a large input signal.

21. DEMAW-SIM-FIG. 4.2 is a graphical representation of the generation of the inverted information signal of the DeMaw circuit simulation of DEMAW-SIM-FIG. 1.2.



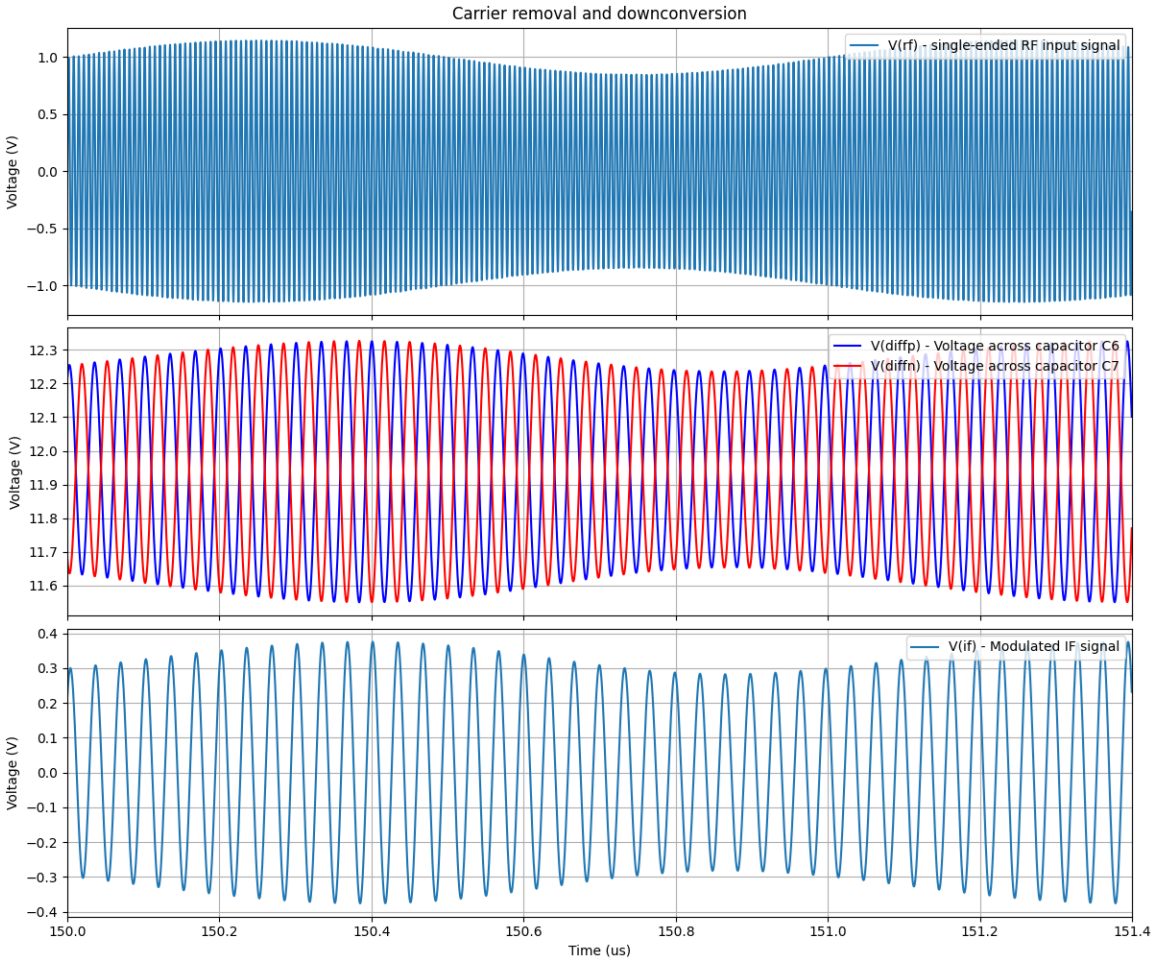
DEMAW-SIM-FIG. 4.2. Generation of information signal and inverted information signal (circuit of DEMAW-SIM-FIG. 12).

22. DEMAW-SIM-FIG. 5.2 is a graphical representation of the capacitor charging and discharging cycles of capacitors C4 and C5 of the circuit of DEMAW-SIM-FIG. 1.2.



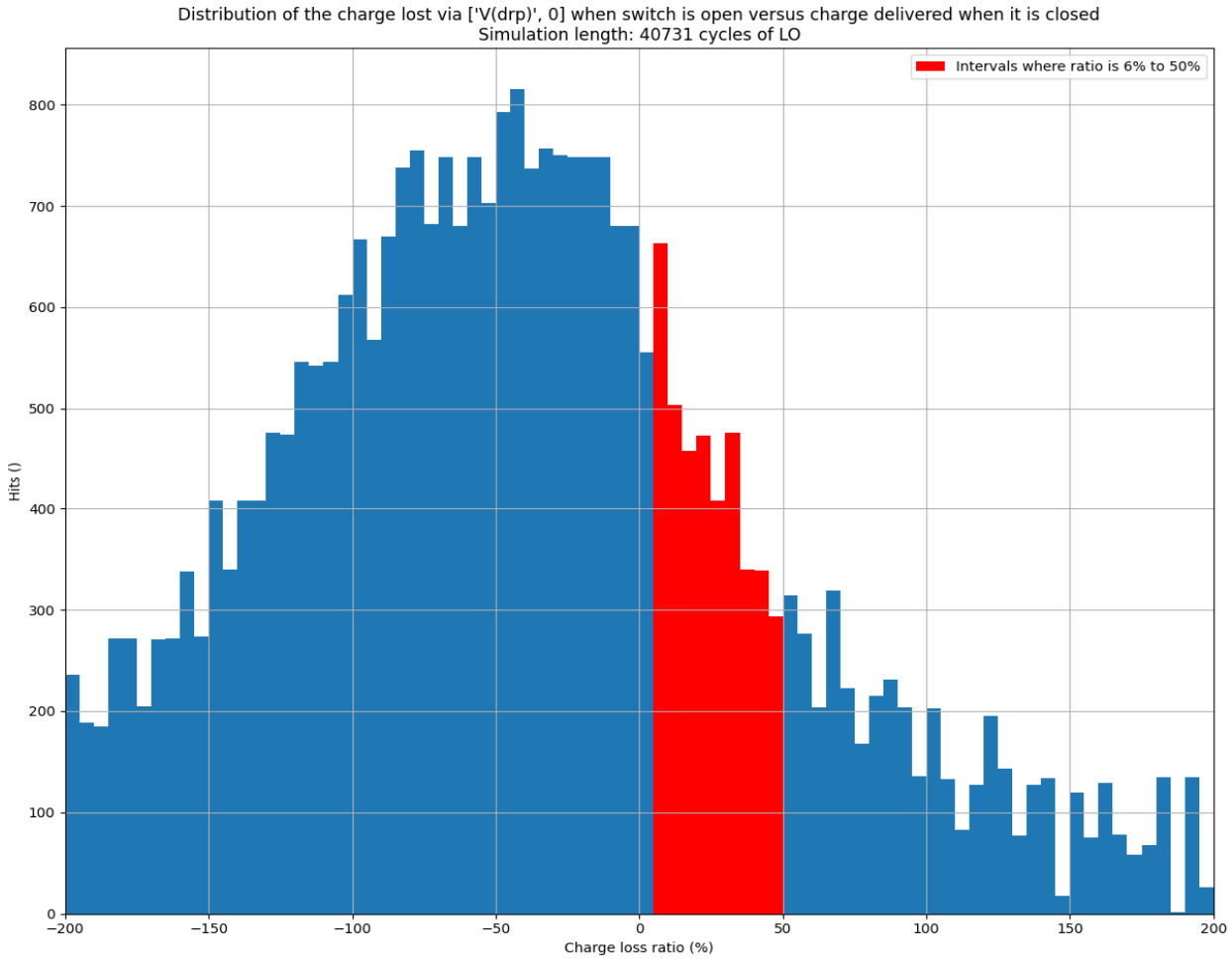
DEMAW-SIM-FIG. 5.2. Capacitors C4 and C5 charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.2).

23. DEMAW-SIM-FIG. 6.2 is a graphical representation of the carrier removal and down-conversion of the circuit of DEMAW-SIM-FIG. 1.2.



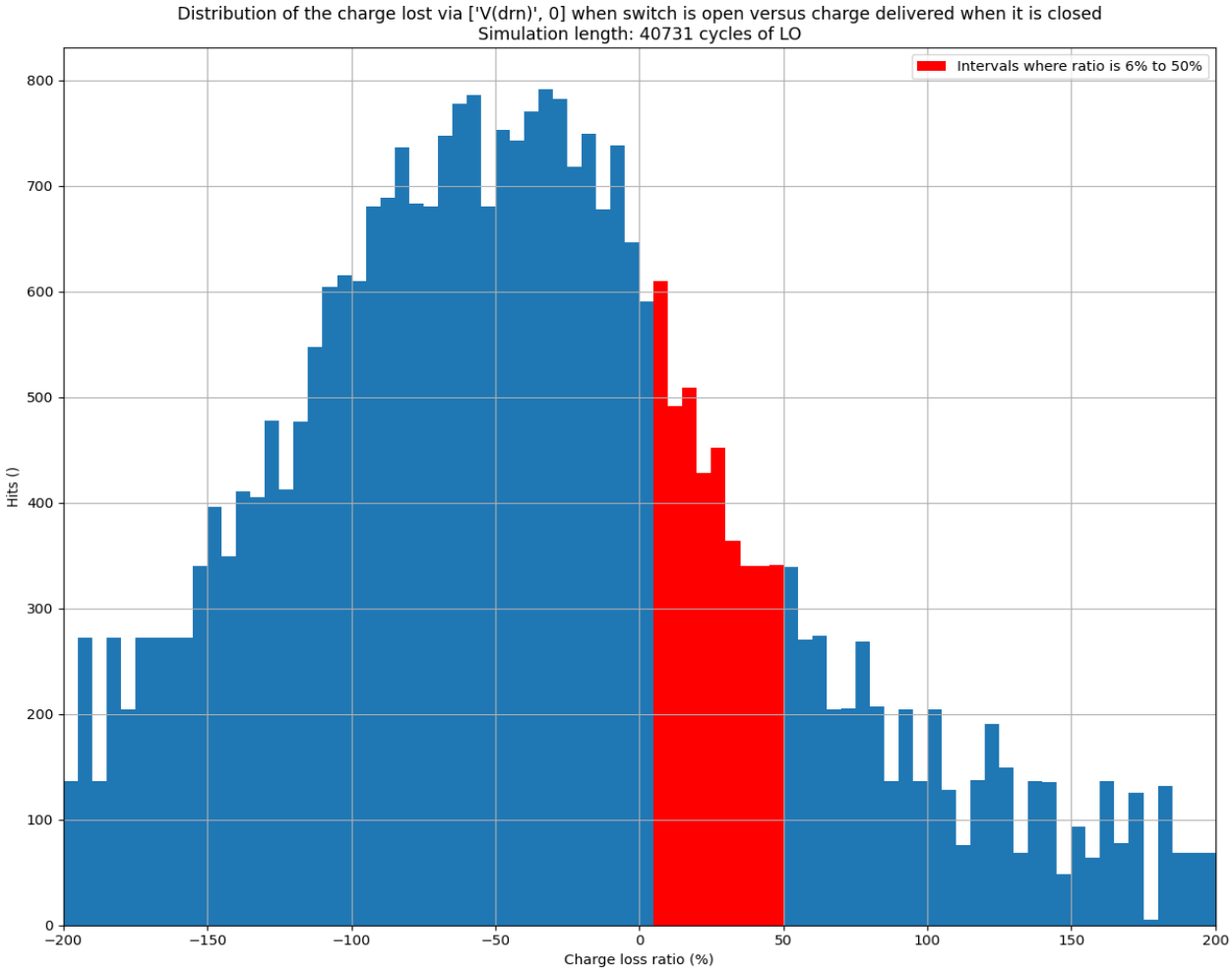
DEMAW-SIM-FIG. 6.2. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.2).

24. DEMAW-SIM-FIG. 7.2A is a histogram showing the charge loss ratio percentages for capacitor C4 in the circuit of DEMAW-SIM-FIG. 1.2.



DEMAW-SIM-FIG. 7.2A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.2).

25. DEMAW-SIM-FIG. 7.2B is a histogram of the charge loss ratio percentages for capacitor C5 of the circuit of DEMAW-SIM-FIG. 1.2.

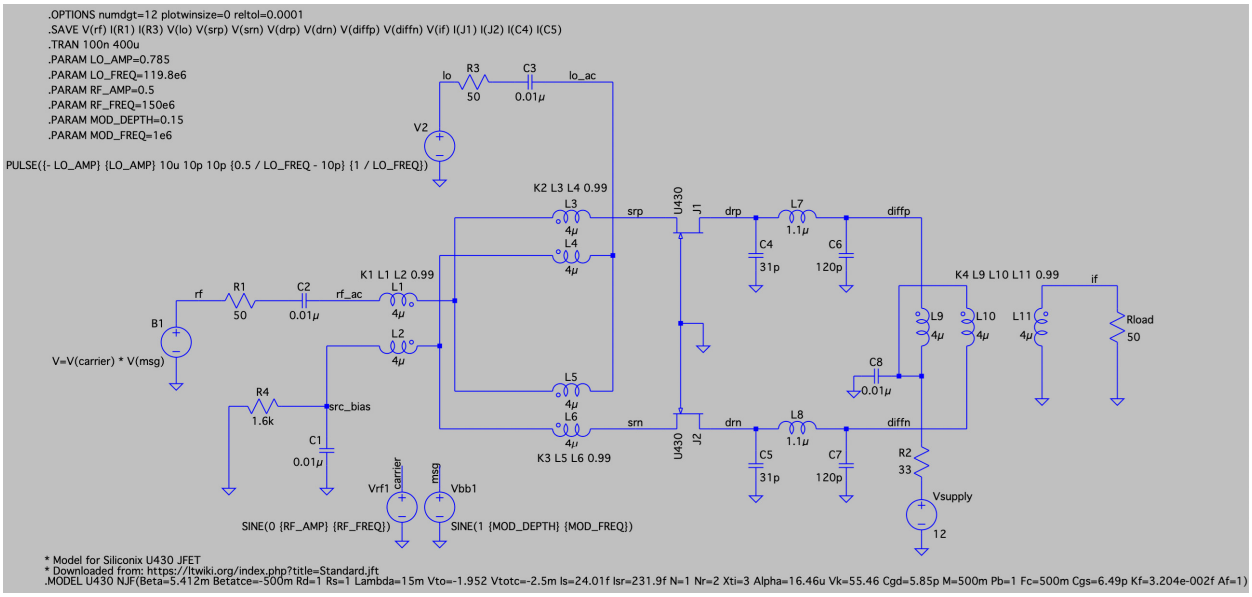


DEMAW-SIM-FIG. 7.2B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.2).

B. Simulation Results For an Input Signal Reduced by 6 dB

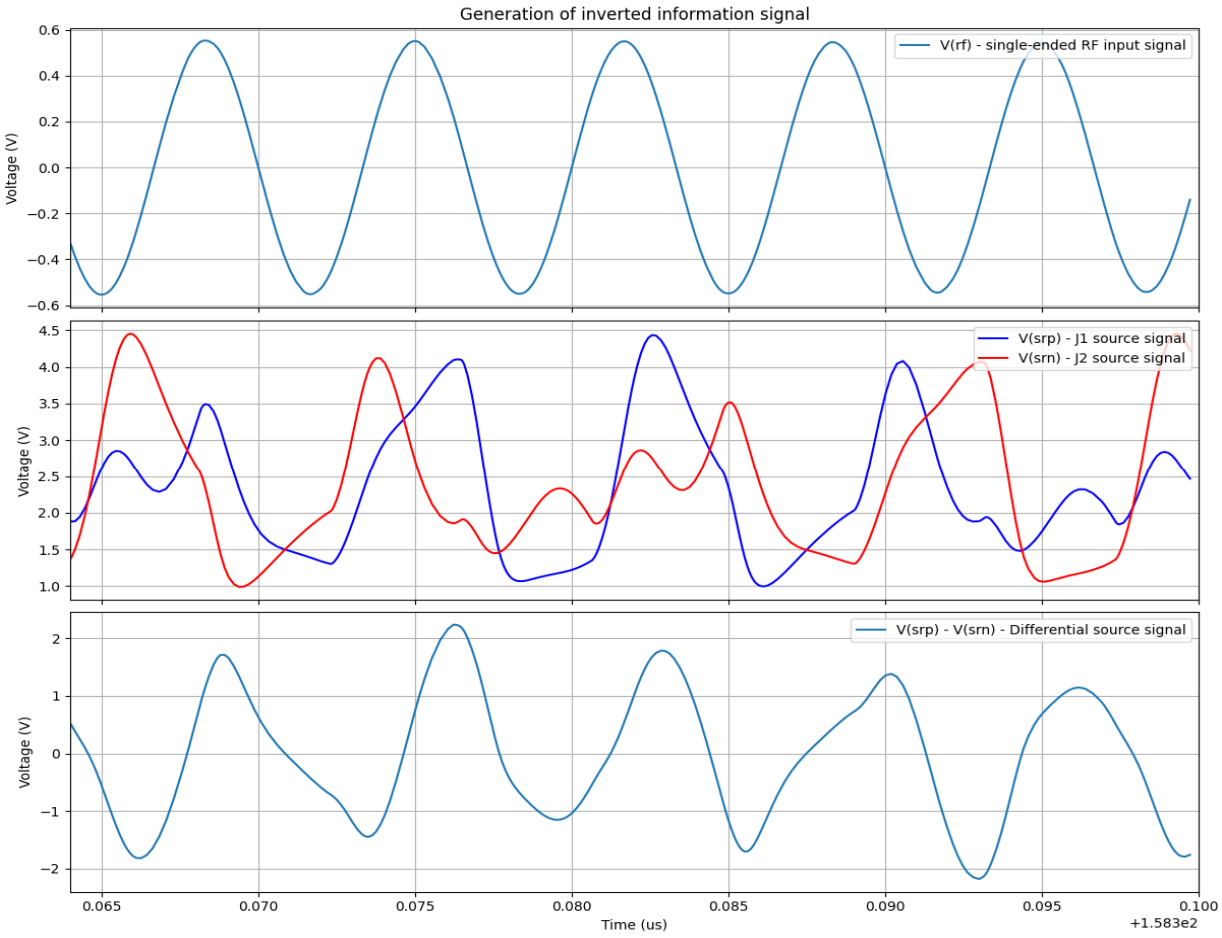
26. DEMAW-SIM-FIG. 1.3 is a schematic representation of the DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 6 dB. I have created additional figures DEMAW-SIM-FIGS. 4.3, 5.3, 6.3, 7.3A and 7.3B based on simulation output from DEMAW-SIM-FIG. 1.3. DEMAW-SIM-FIGS. 4.3, 5.3, 6.3, 7.3A and 7.3B show the same simulation output

from DEMAW-SIM-FIG. 1.3 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIGS. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.3, 4.3, 5.3, 6.3, 7.3A and 7.3B.



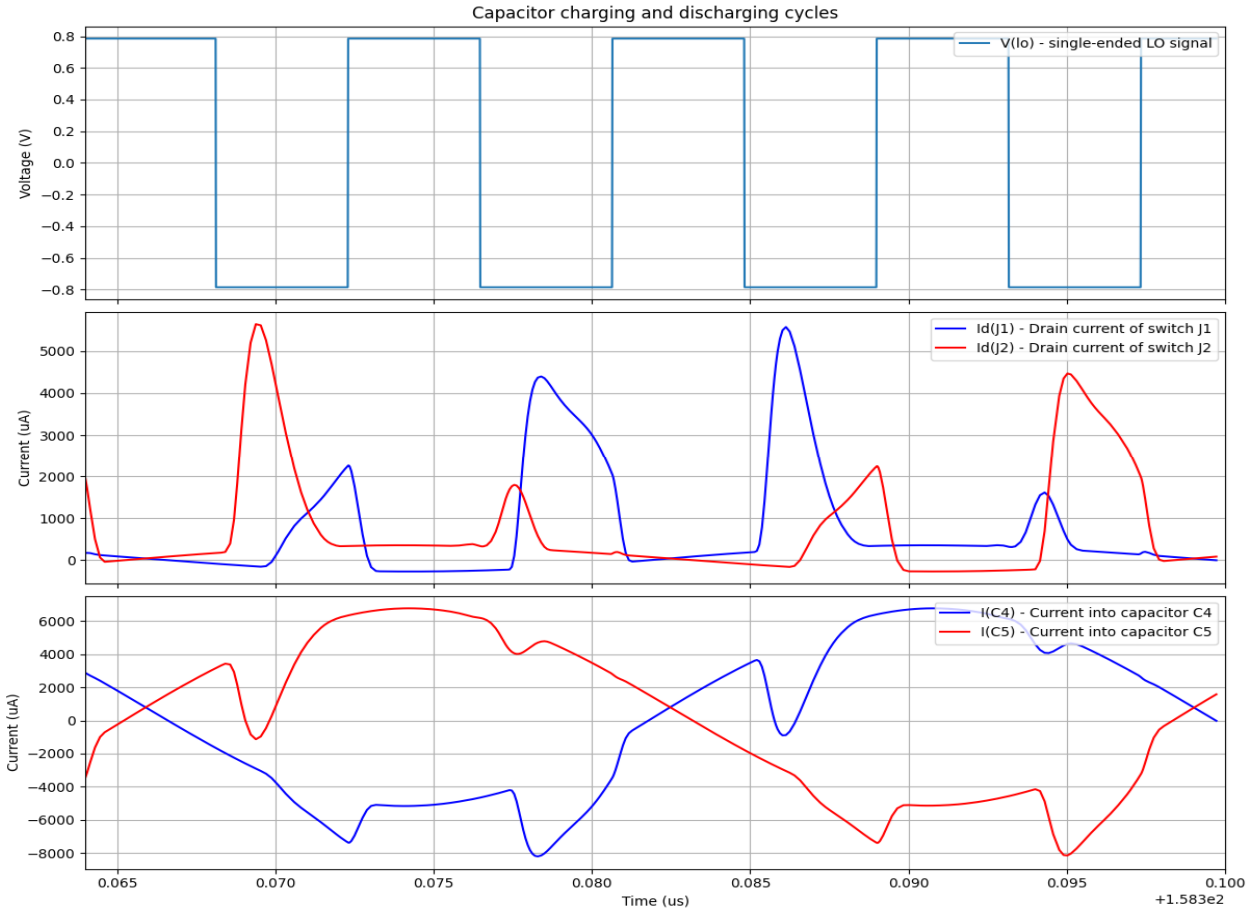
DEMAW-SIM-FIG. 1.3. DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 6 dB.

27. DEMAW-SIM-FIG. 4.3 is a graphical representation of the generation of the information signal and the inverted information signal in the circuit of DEMAW-SIM-FIG. 1.3.



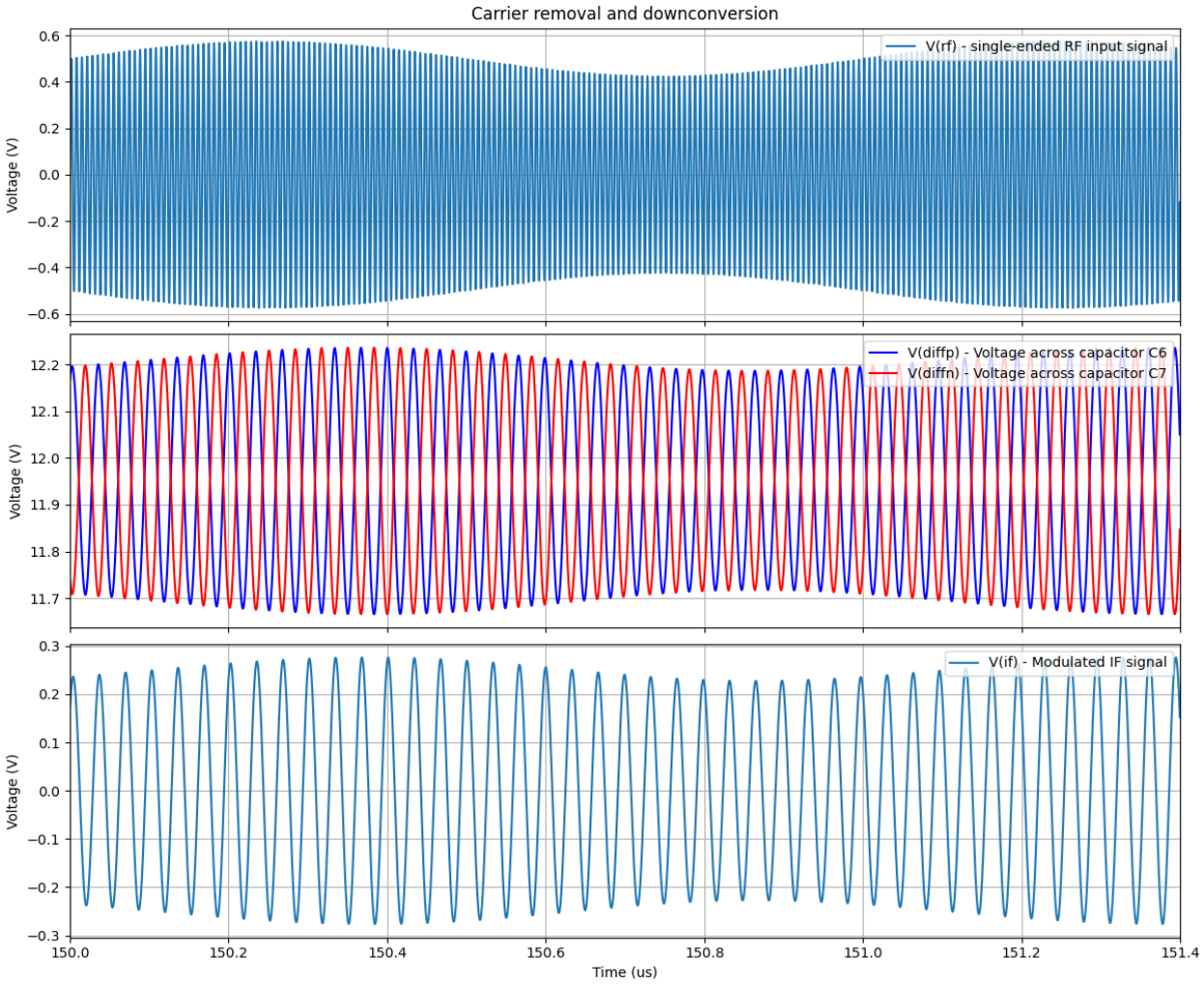
DEMAW-SIM-FIG. 4.3. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.3).

28. DEMAW-SIM-FIG. 5.3 is a graphical representation showing the charging and discharging cycles of the capacitors C4 and C5 in circuit of DEMAW-SIM-FIG. 1.3.



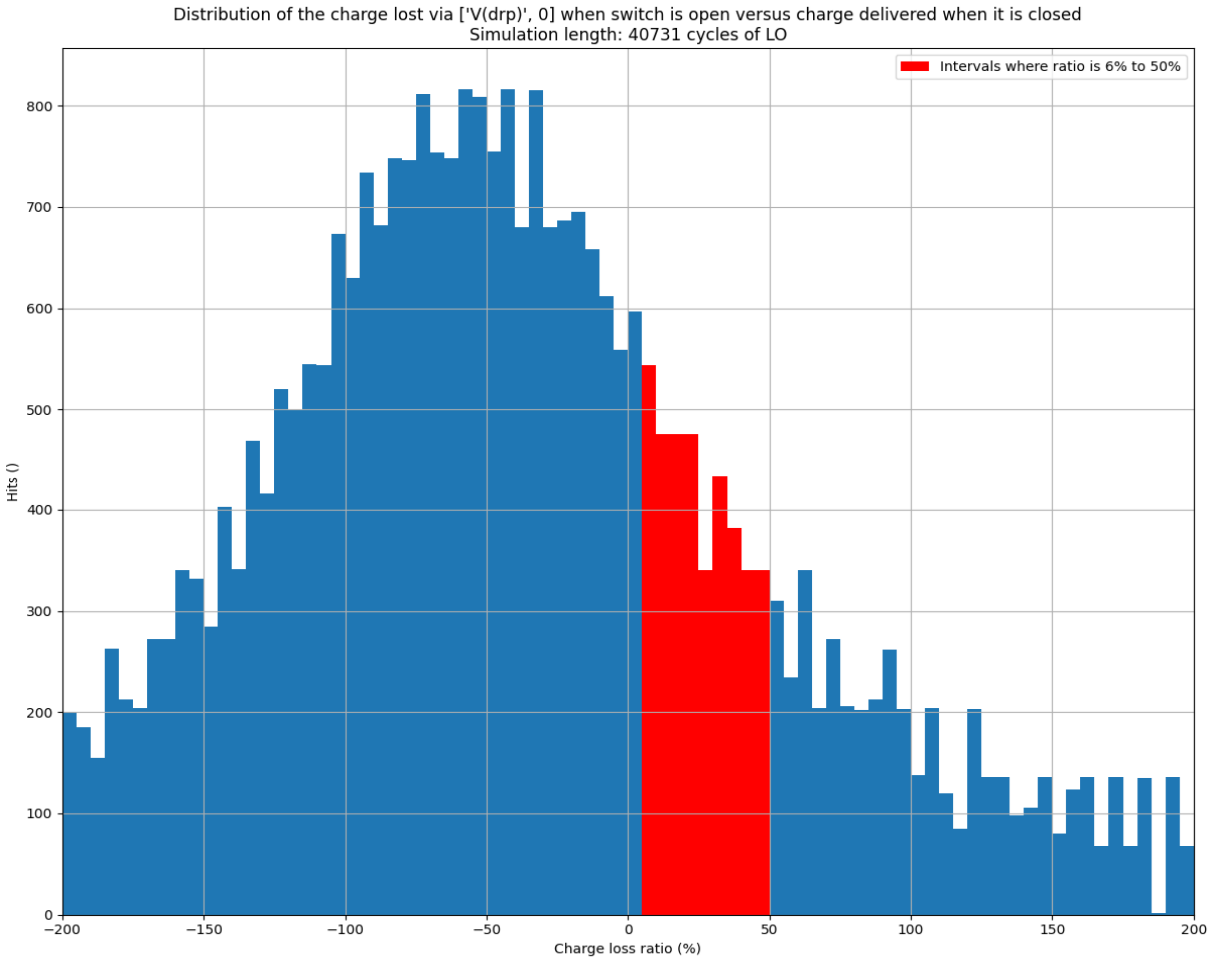
DEMAW-SIM-FIG. 5.3. Charging and discharging cycles of capacitors C4 and C5 (circuit of DEMAW-SIM-FIG. 1.3).

29. DEMAW-SIM-FIG. 6.3 is a graphical representation of the carrier removal and down-conversion of the circuit of DEMAW-SIM-FIG. 1.3.



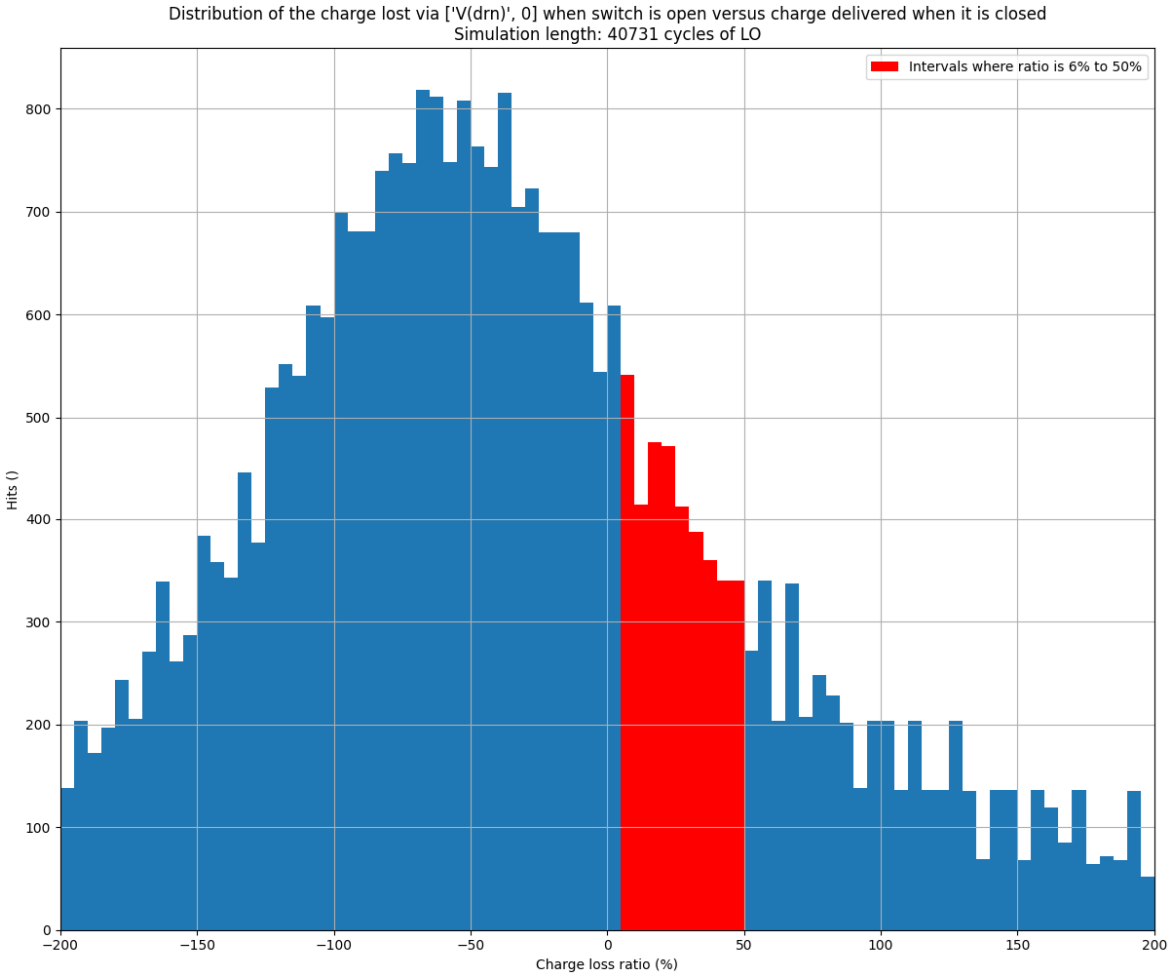
DEMAW-SIM-FIG. 6.3. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.3).

30. DEMAW-SIM-FIG. 7.3A is a histogram of the charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.3.



DEMAW-SIM-FIG. 7.3A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.3).

31. DEMAW-SIM-FIG. 7.3B is a histogram showing the charge loss ratio percentages for capacitor C5 of the circuit of DEMAW-SIM-FIG. 1.3.

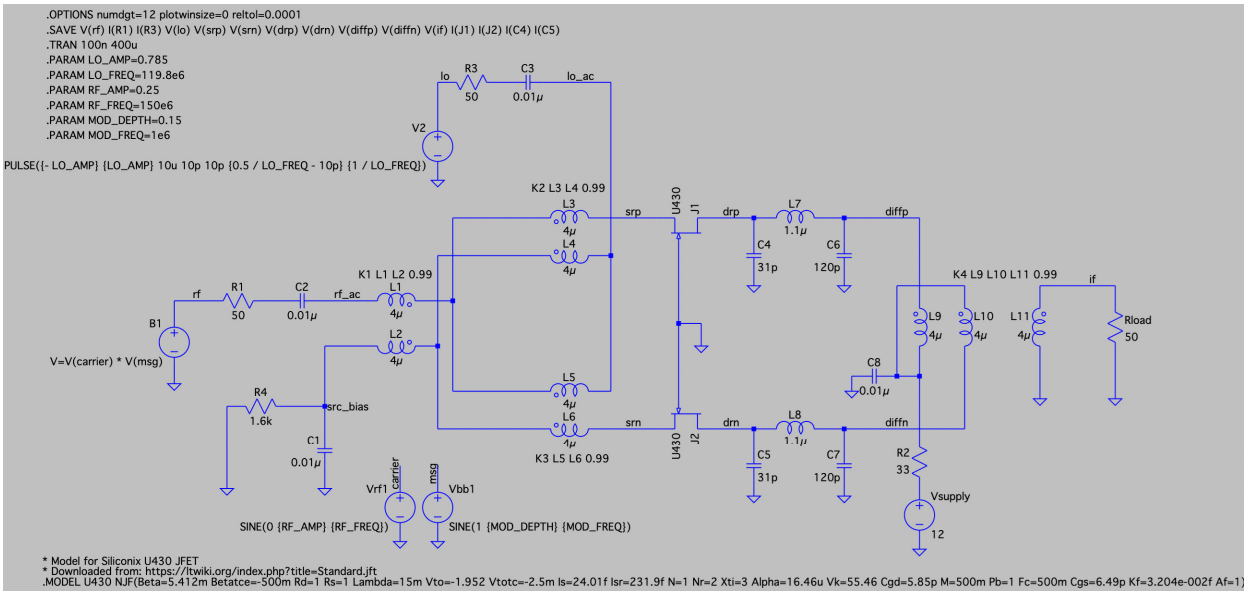


DEMAW-SIM-FIG. 7.3B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.3).

C. Simulation Results For an Input Signal Reduced by 12 dB

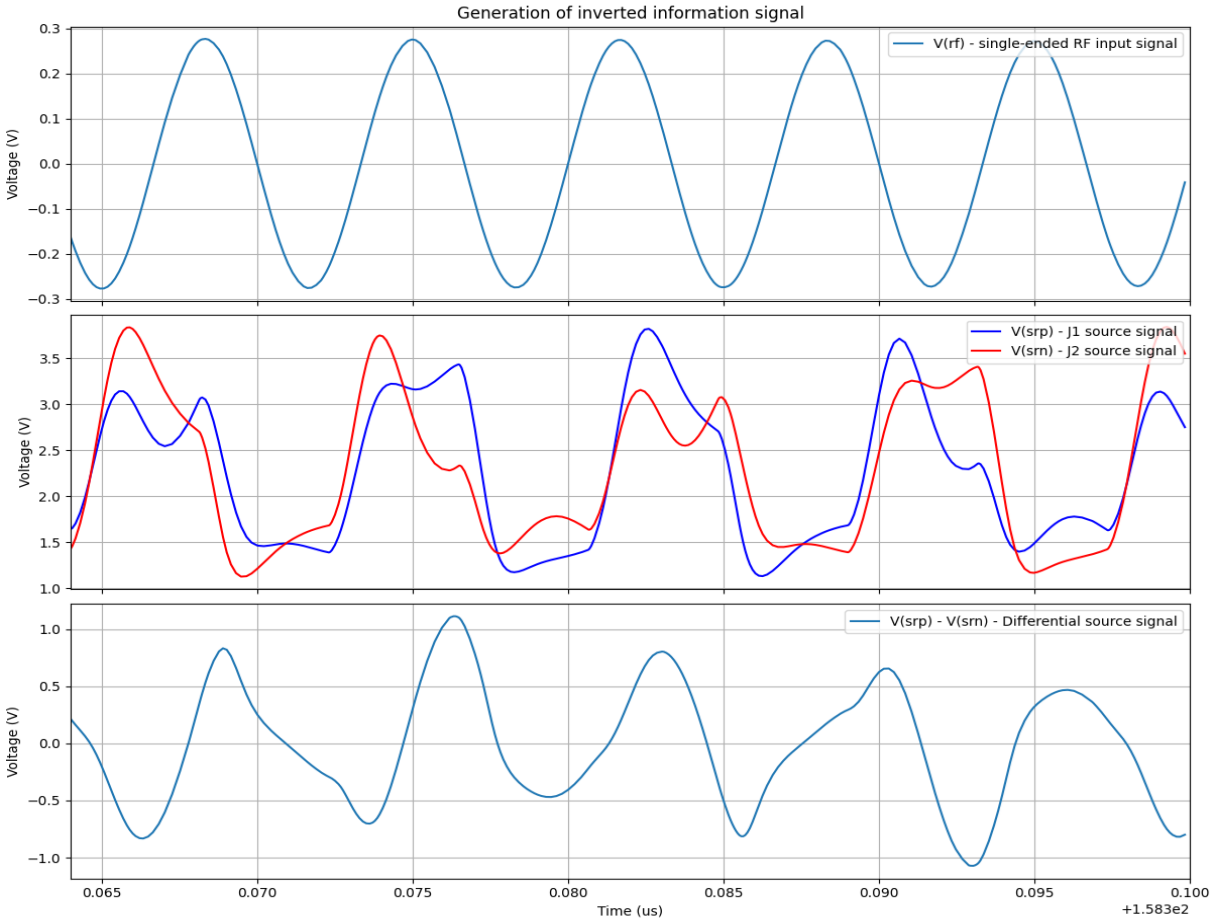
32. DEMAW-SIM-FIG. 1.4 is a schematic representation of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 12 dB. I have created additional figures DEMAW-SIM-FIGS. 4.4, 5.4, 6.4, 7.4A and 7.4B based on simulation output from DEMAW-SIM-FIG. 1.4. DEMAW-SIM-FIGS. 4.4, 5.4, 6.4, 7.4A and 7.4B show the same simulation output from DEMAW-SIM-FIG. 1.4 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from

DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIGS. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.4, 4.4, 5.4, 6.4, 7.4A and 7.4B.



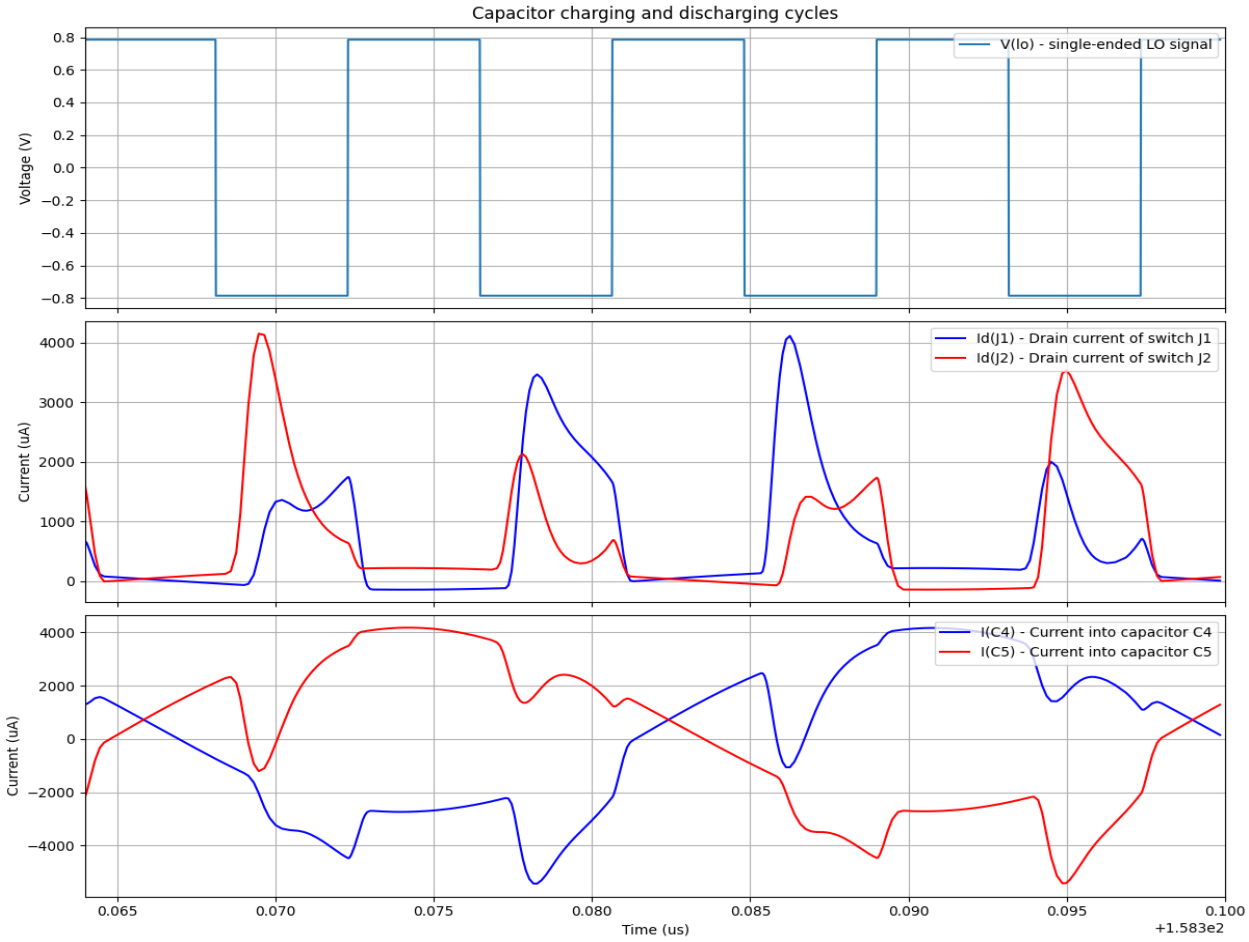
DEMAW-SIM-FIG. 1.4. Simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 12 dB.

33. DEMAW-SIM-FIG. 4.4 is a graphical representation of the generation of inverted information signal of the circuit of DEMAW-SIM-FIG. 1.4.



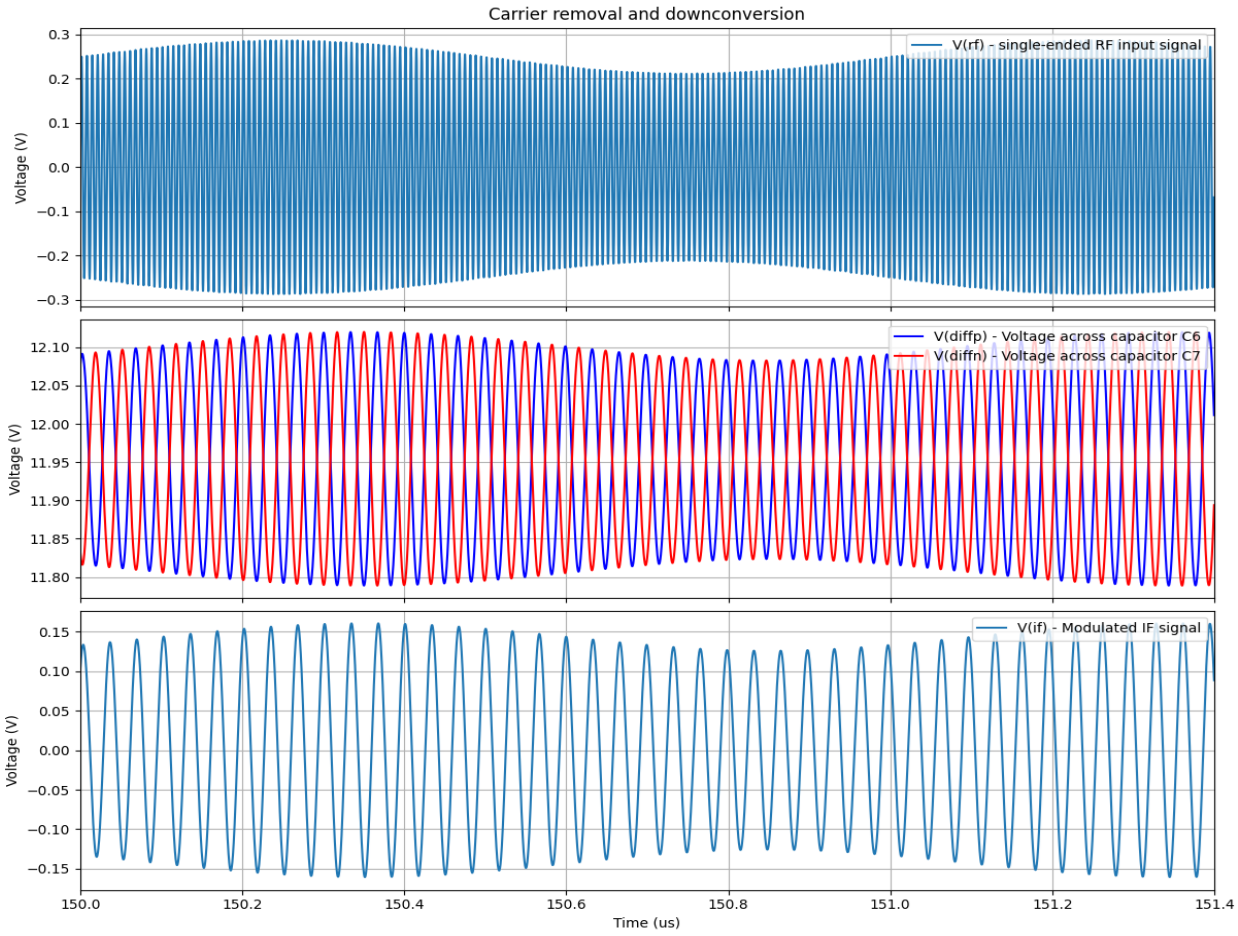
DEMAW-SIM-FIG. 4.4. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.4).

34. DEMAW-SIM-FIG. 5.4 is a graphical representation of the charging and discharging cycles of capacitors C4 and C5 of the circuit of DEMAW-SIM-FIG. 1.4.



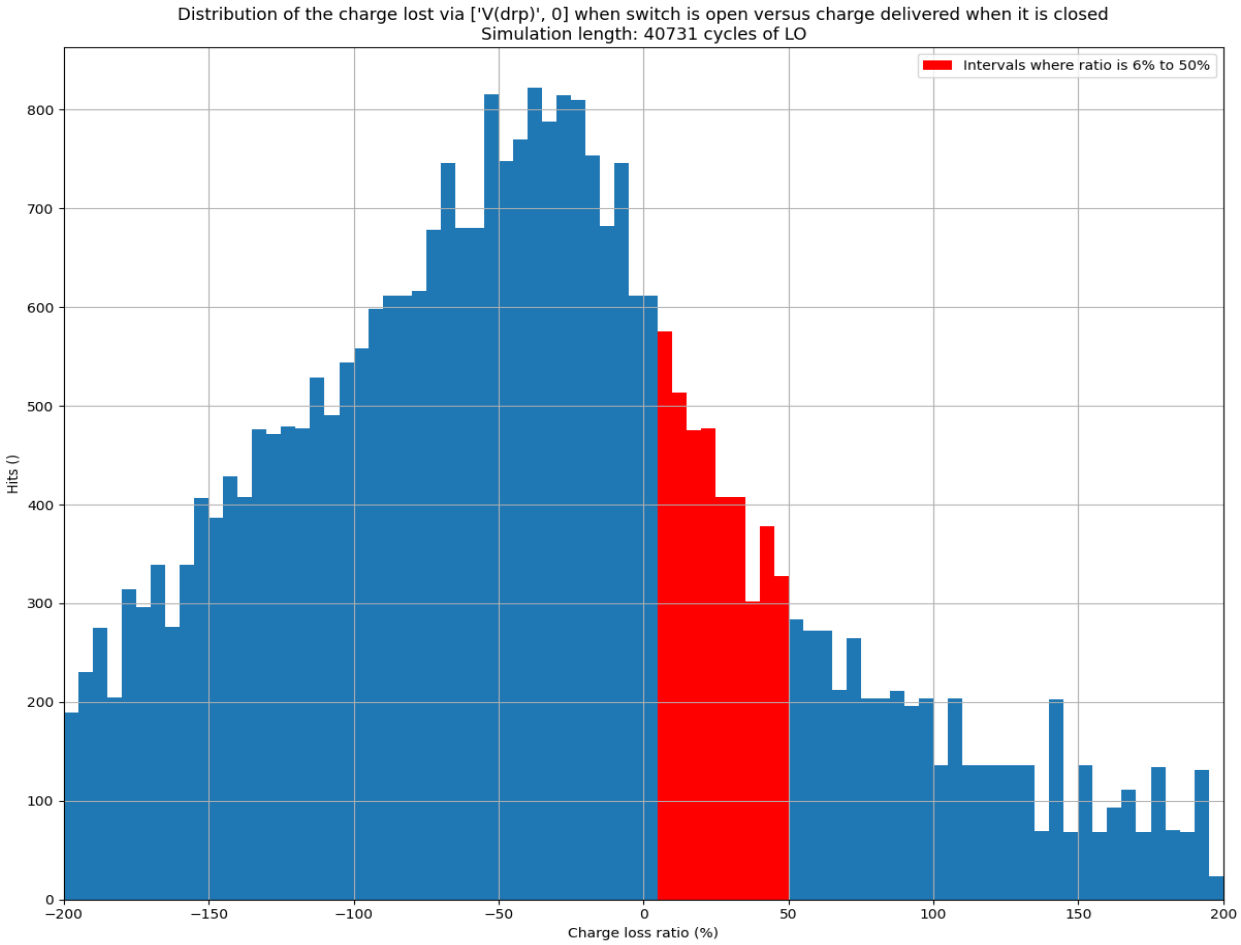
DEMAW-SIM-FIG. 5.4. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.4).

35. DEMAW-SIM-FIG. 6.4 is a graphical representation showing the carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.4.



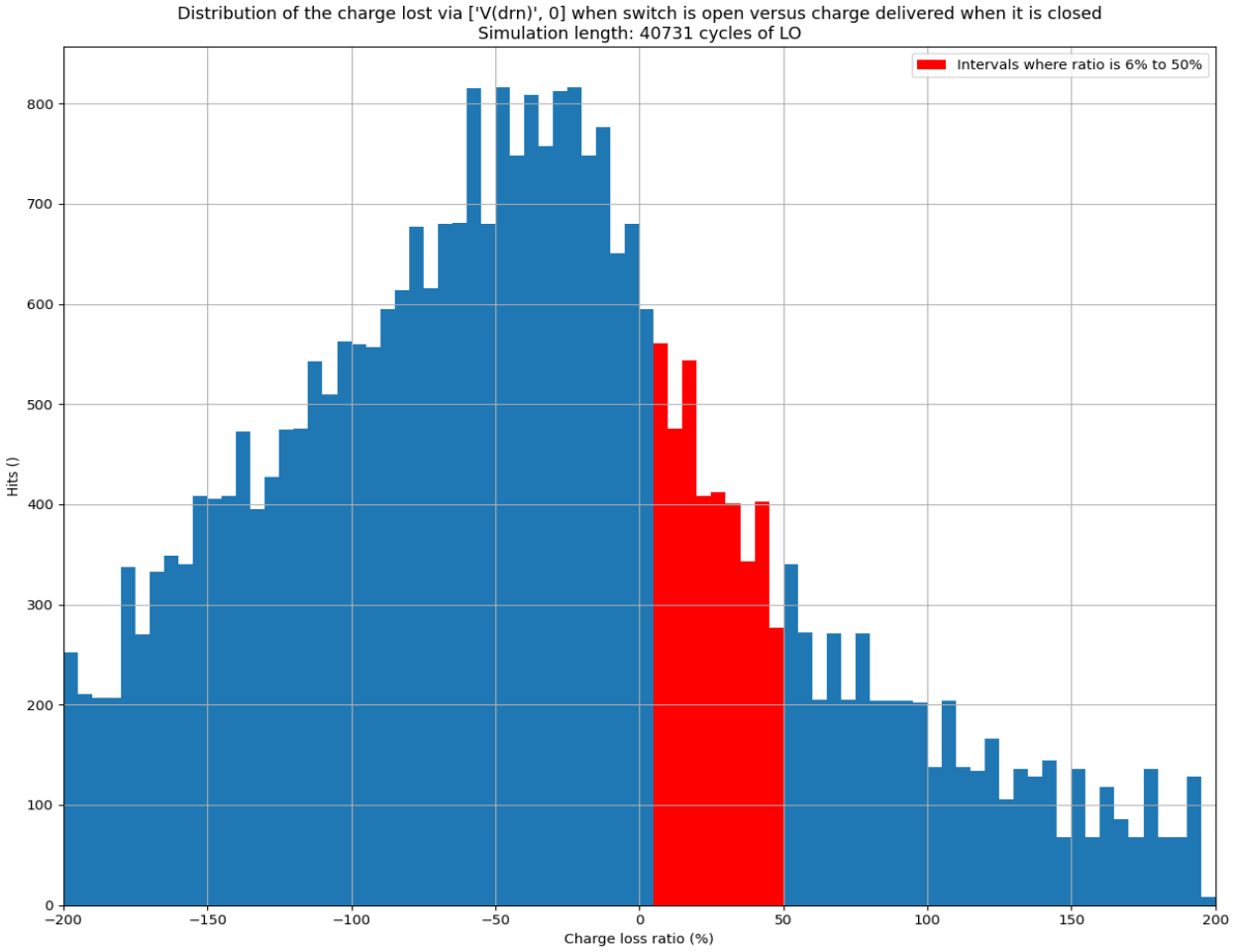
DEMAW-SIM-FIG. 6.4. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.4).

36. DEMAW-SIM-FIG. 7.4A is a histogram of the charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.4.



DEMAW-SIM-FIG. 7.4A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.4).

37. DEMAW-SIM-FIG. 7.4B is a histogram of the charge loss ratio percentages for capacitor C5 of the circuit of DEMAW-SIM-FIG. 1.4.

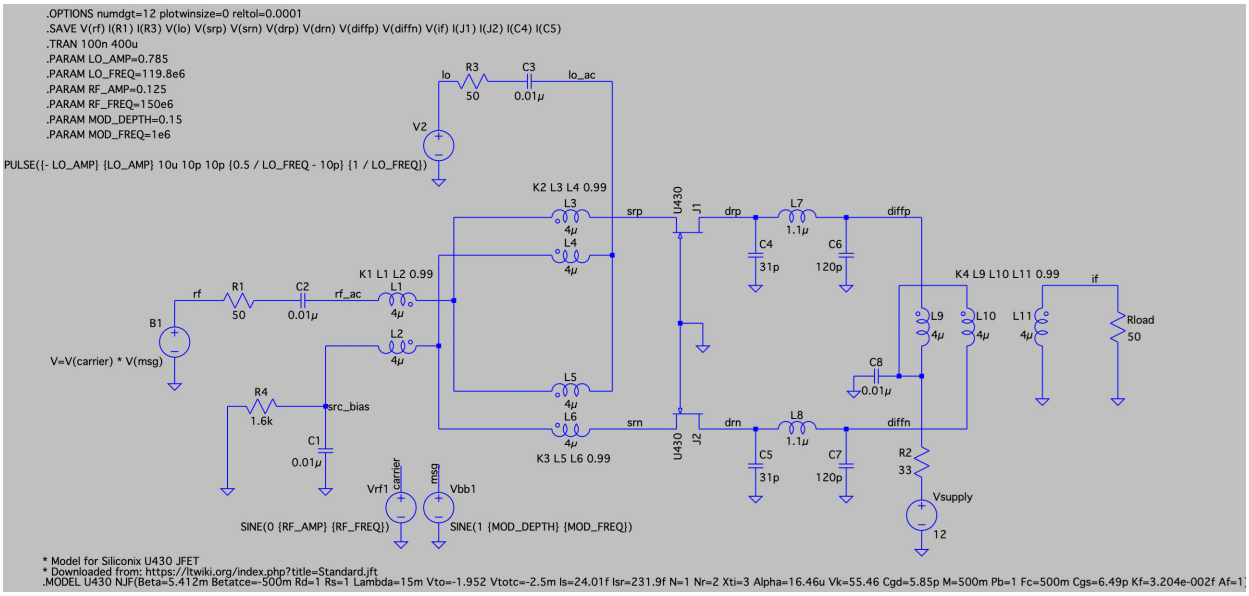


DEMAW-SIM-FIG. 7.4B. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.4).

D. Simulation Results For an Input Signal Reduced by 18 dB

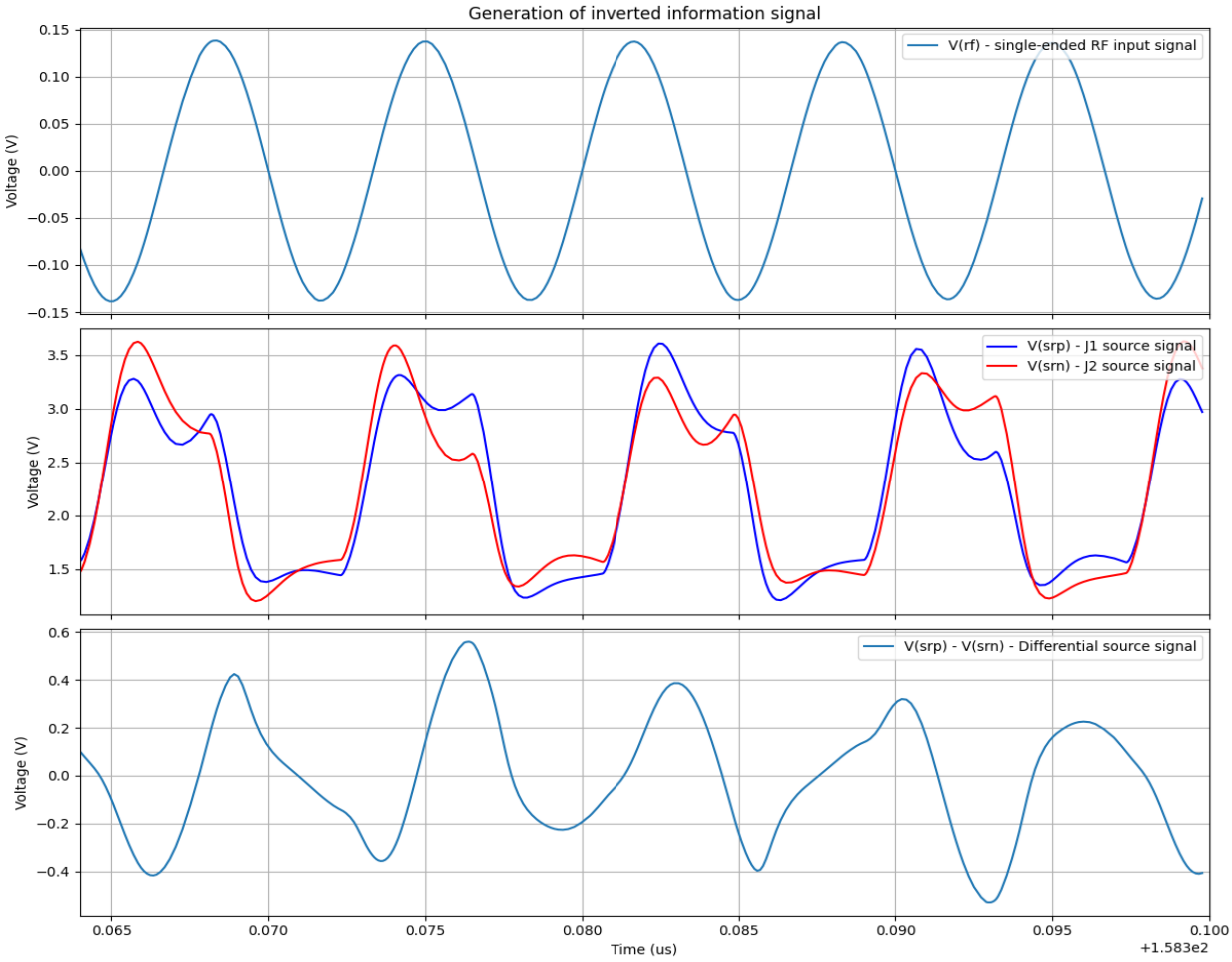
38. DEMAW-SIM-FIG. 1.5 is a schematic diagram of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 18 dB. I have created additional figures DEMAW-SIM-FIGS. 4.5, 5.5, 6.5, 7.5A and 7.5B based on simulation output from DEMAW-SIM-FIG. 1.5. DEMAW-SIM-FIGS. 4.5, 5.5, 6.5, 7.5A and 7.5B show the same simulation output from DEMAW-SIM-FIG. 1.5 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from

DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.5, 4.5, 5.5, 6.5, 7.5A and 7.5B.



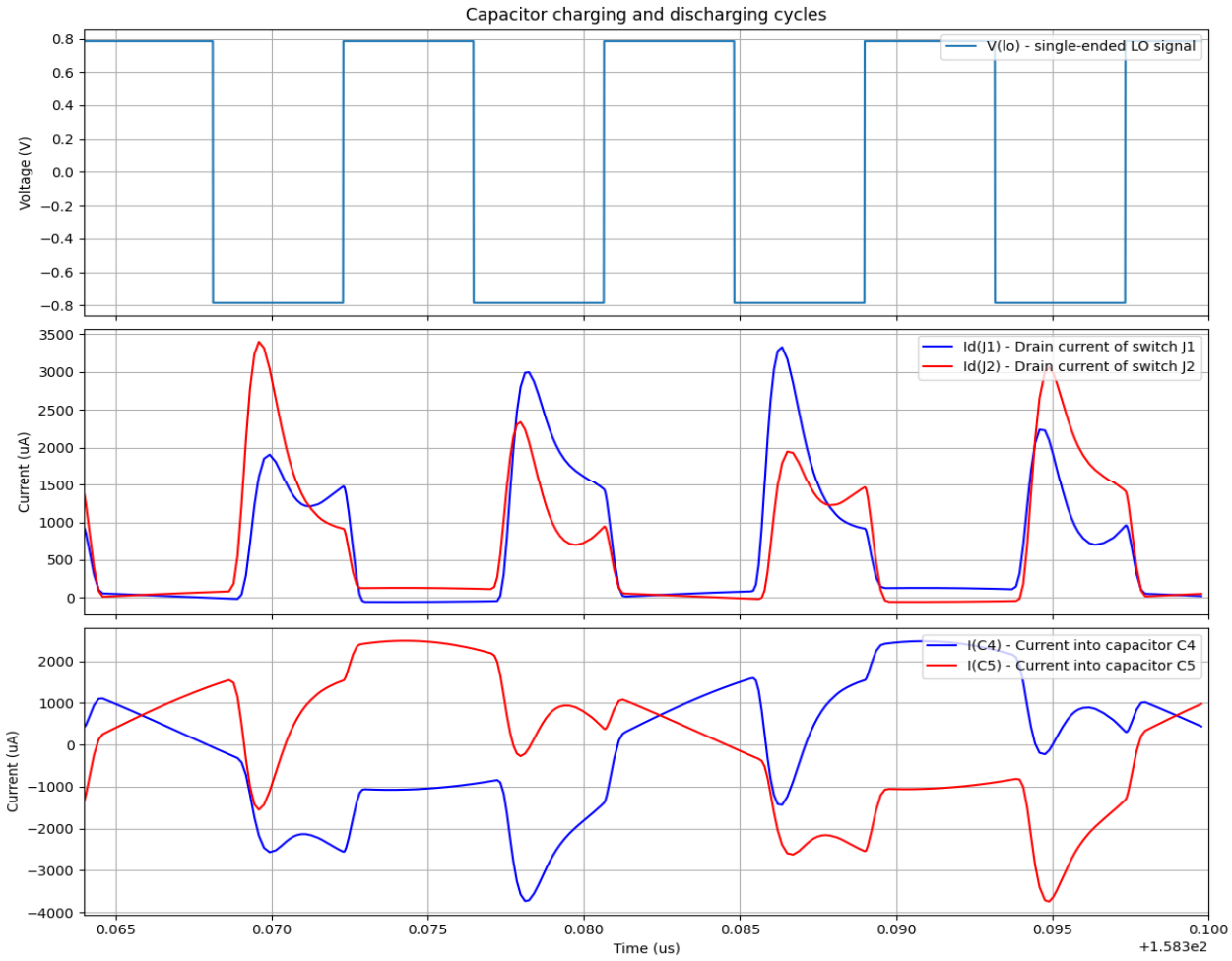
DEMAW-SIM-FIG. 1.5. DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 18 dB.

39. DEMAW-SIM-FIG. 4.5 is a graphical representation illustrating the generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.5).



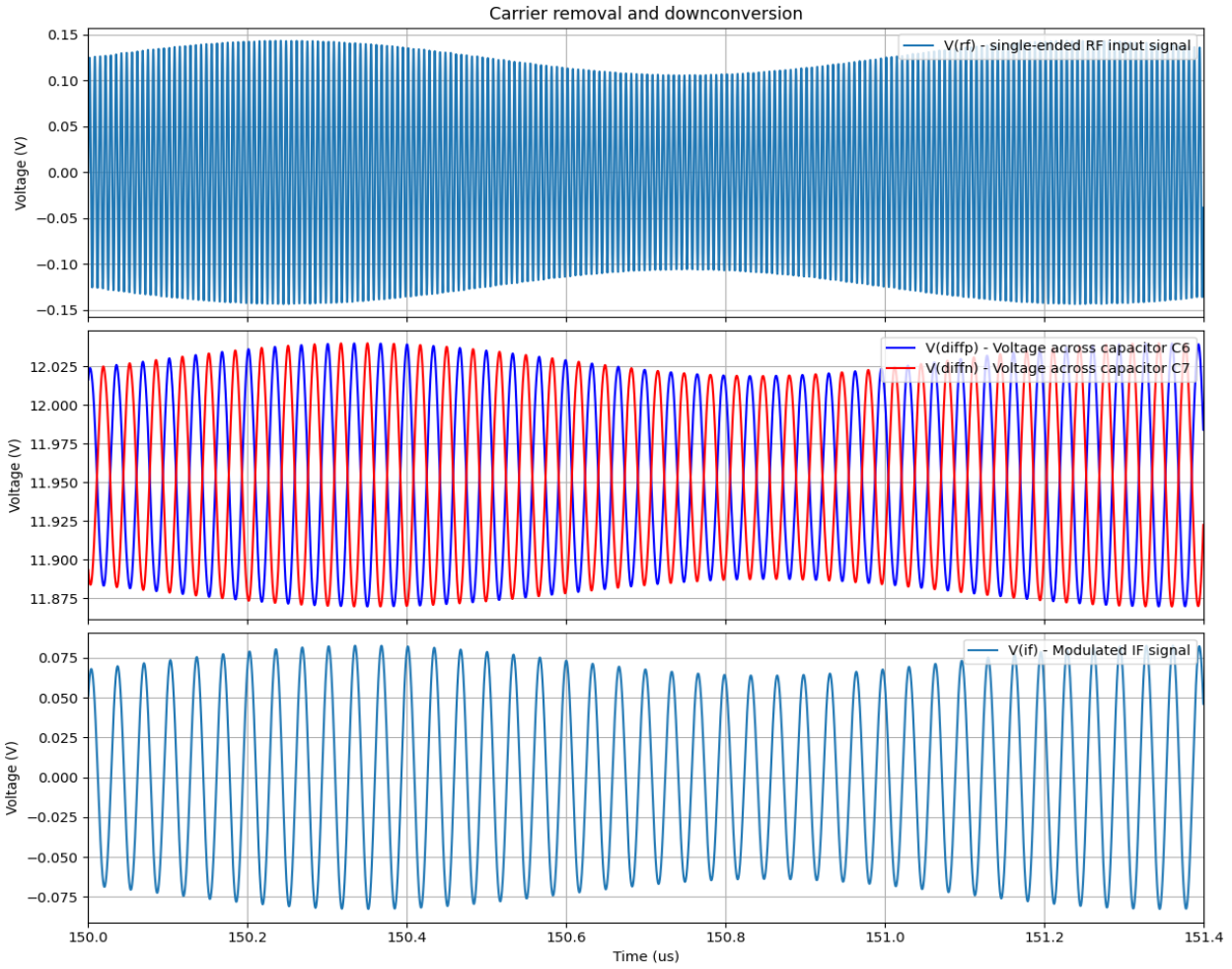
DEMAW-SIM-FIG. 4.5. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.5).

40. DEMAW-SIM-FIG. 5.5 is a graphical representation illustrating the charging and discharging cycles of the capacitors C4 and C5 of the circuit of DEMAW-SIM-FIG. 1.5.



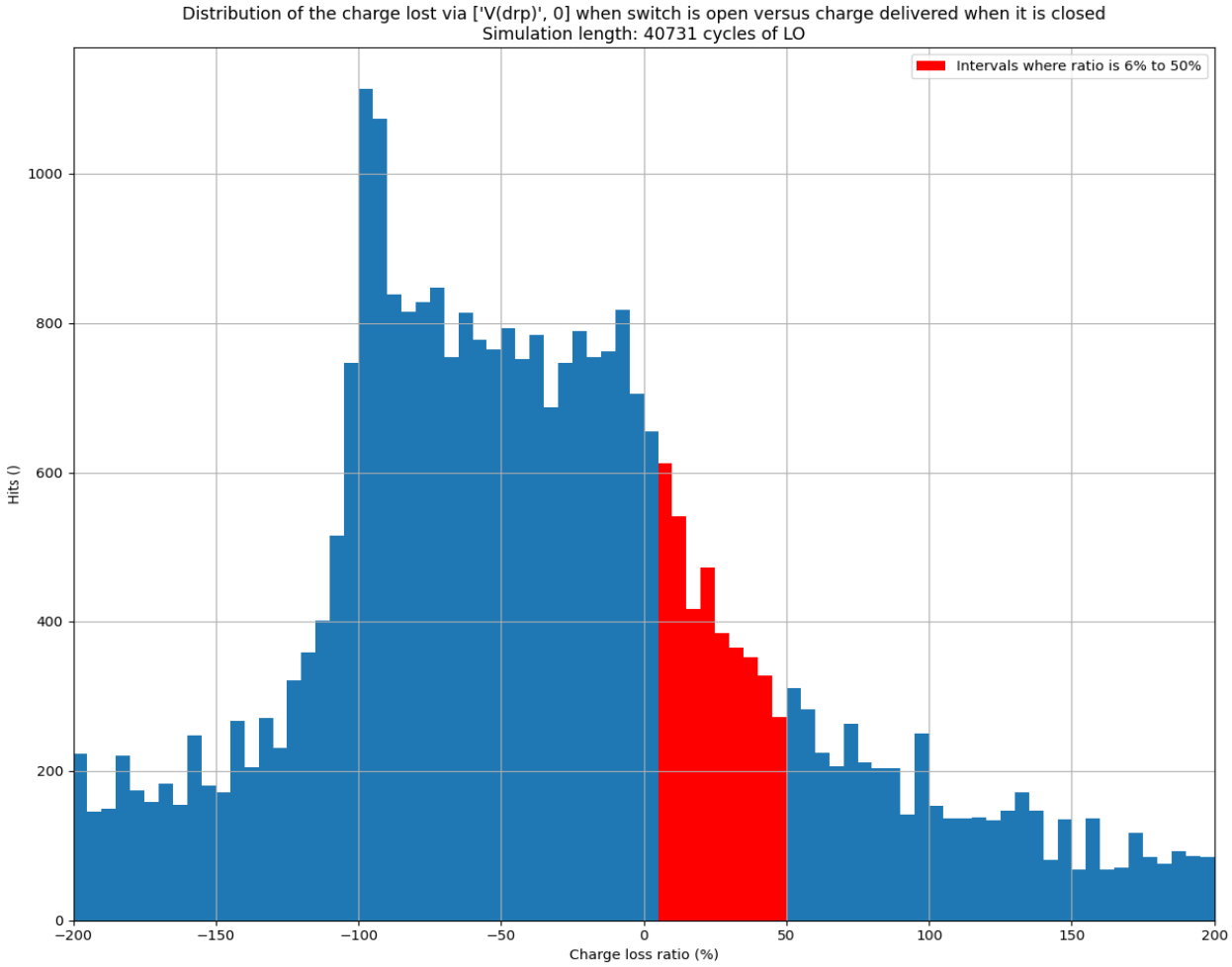
DEMAW-SIM-FIG. 5.5. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.5).

41. DEMAW-SIM-FIG. 6.5 is a schematic representation illustrating the carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.5.



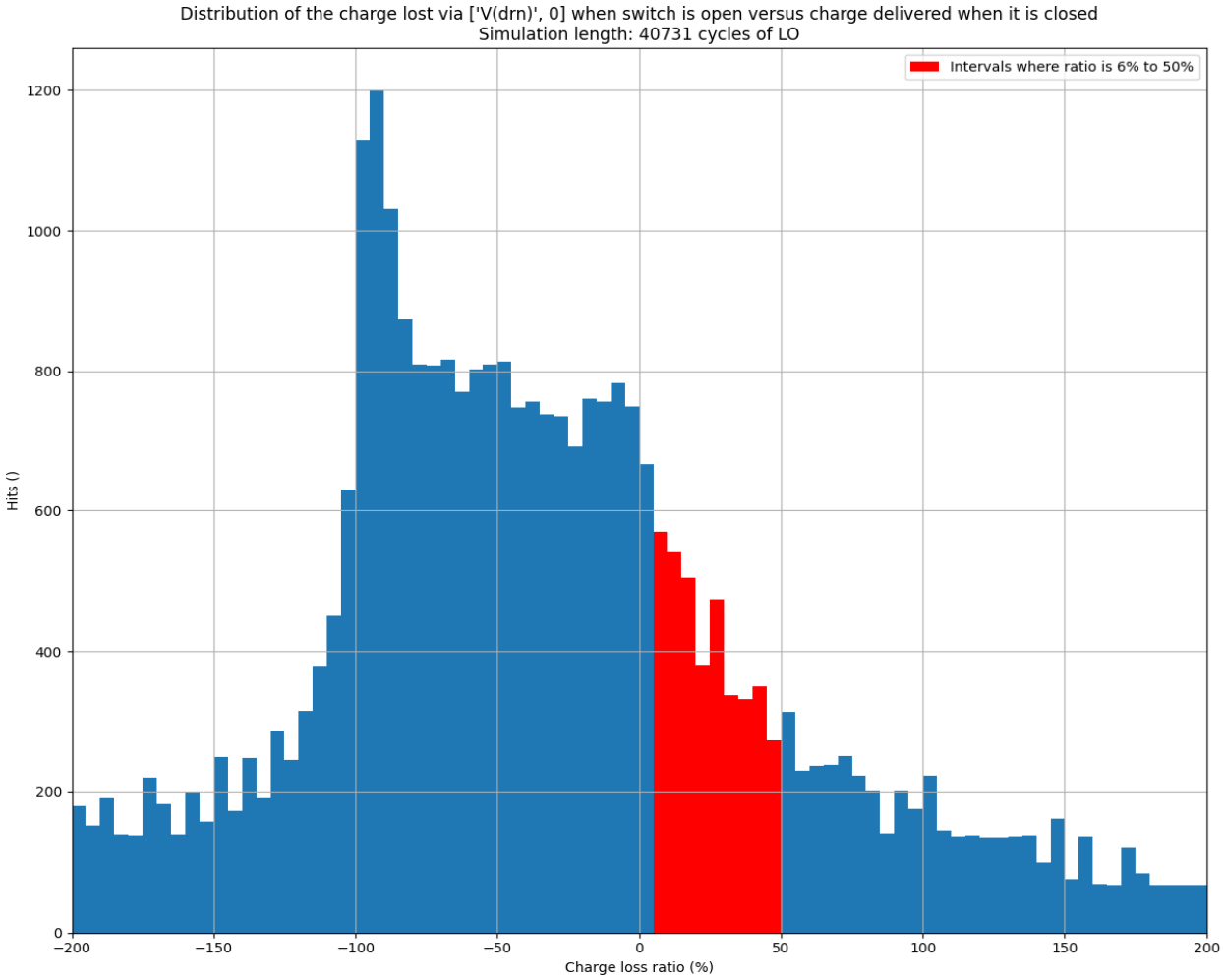
DEMAW-SIM-FIG. 6.5. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.5).

42. DEMAW-SIM-FIG. 7.5A is a histogram illustrating the charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.5.



DEMAW-SIM-FIG. 7.5A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.5).

43. DEMAW-SIM-FIG. 7.5B is a histogram showing the charge loss ratio percentages for capacitor C5 of the circuit of DEMAW-SIM-FIG. 1.5.

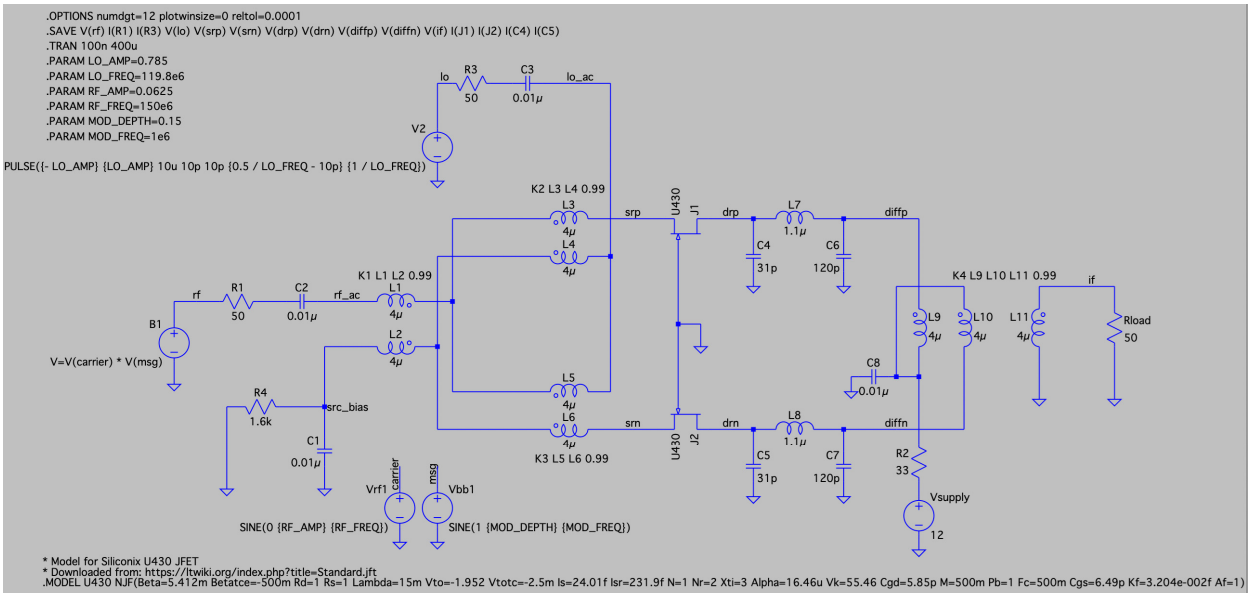


DEMAW-SIM-FIG. 7.5B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.5).

E. Simulation Results For an Input Signal Reduced by 24 dB

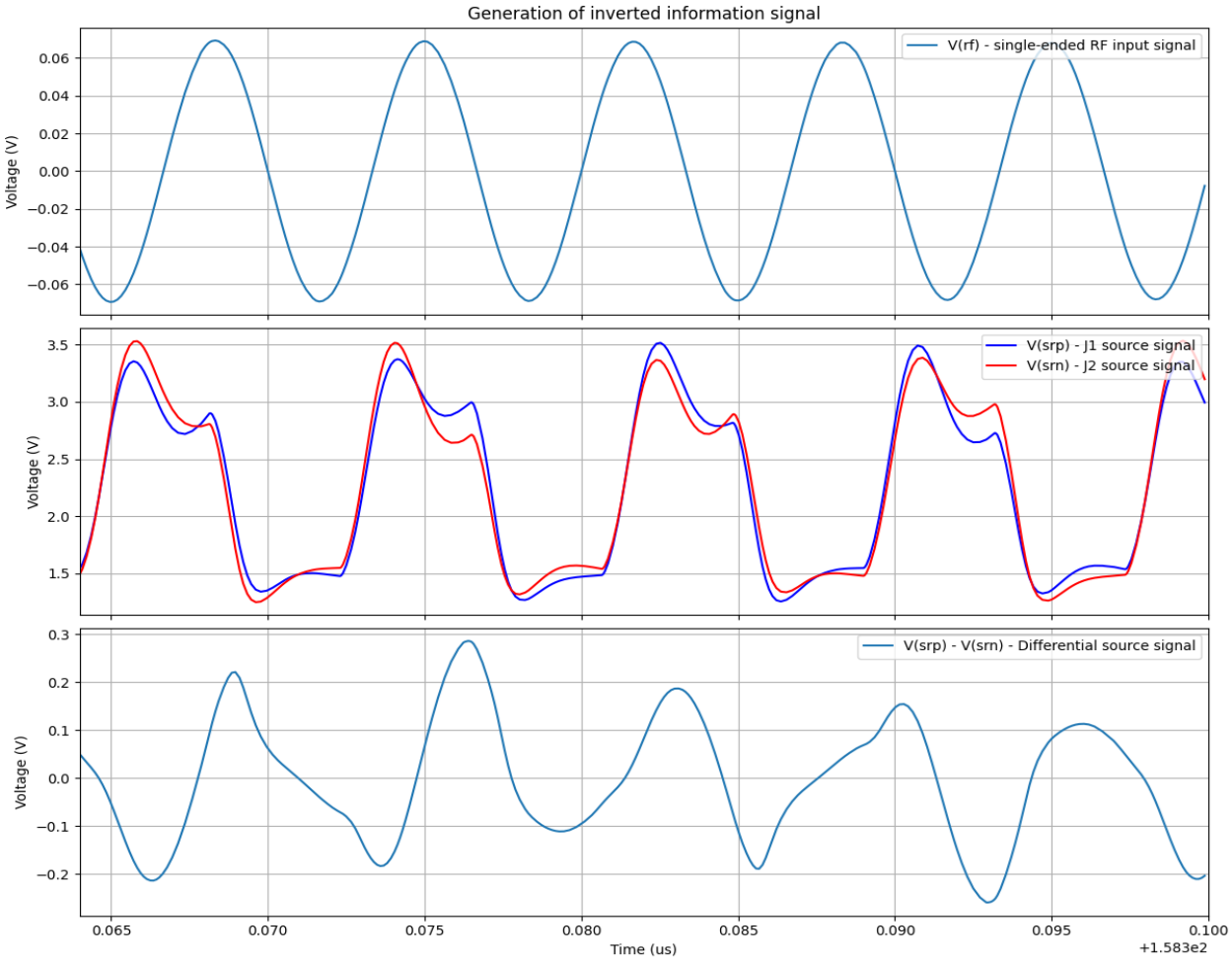
44. DEMAW-SIM-FIG. 1.6 is a schematic representation of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 24 dB. I have created additional figures DEMAW-SIM-FIGS. 4.6, 5.6, 6.6, 7.6A and 7.6B based on simulation output from DEMAW-SIM-FIG. 1.6. DEMAW-SIM-FIGS. 4.6, 5.6, 6.6, 7.6A and 7.6B show the same simulation output

from DEMAW-SIM-FIG. 1.6 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.6, 4.6, 5.6, 6.6, 7.6A and 7.6B.



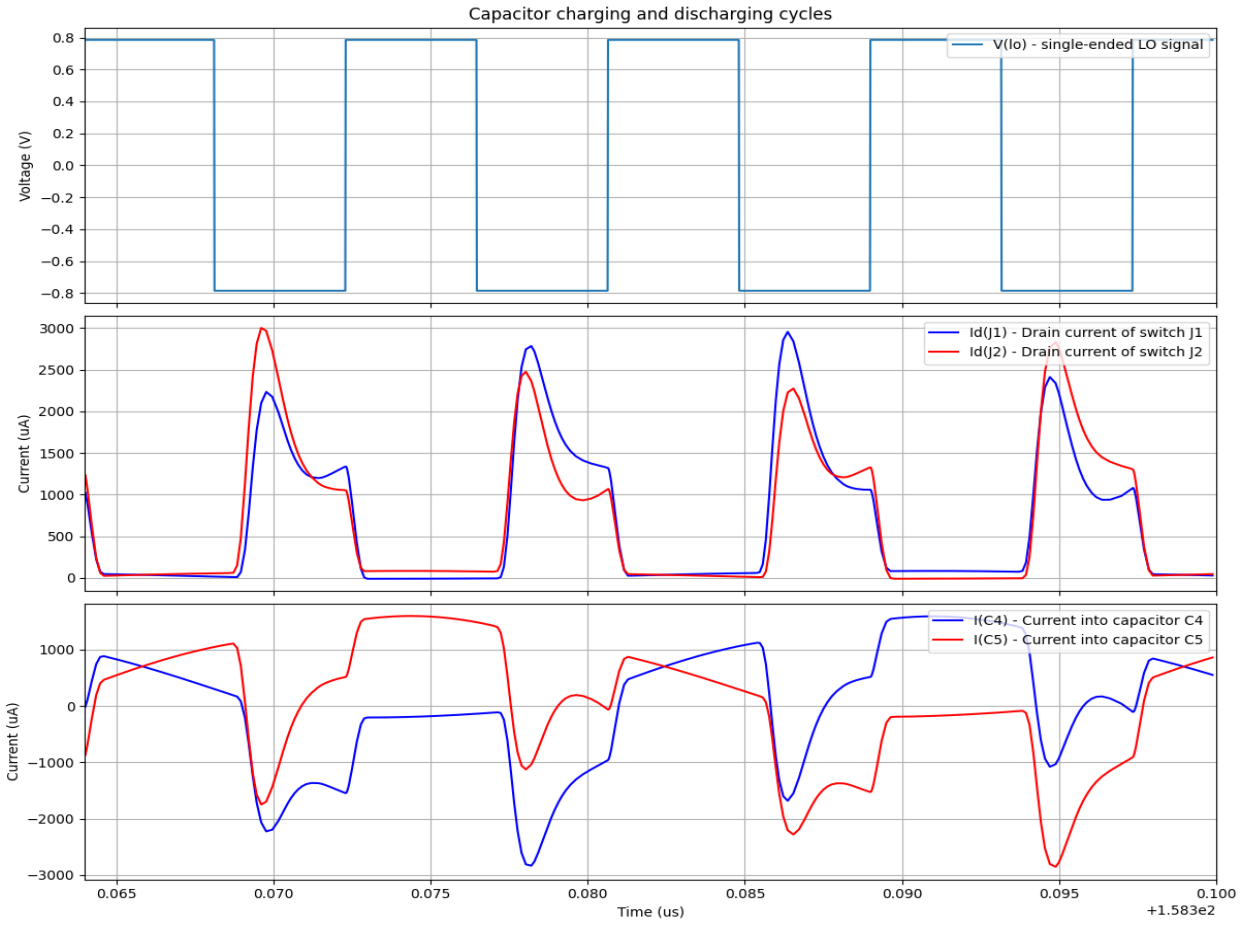
DEMAW-SIM-FIG. 1.6 is a schematic representation of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 24 dB.

45. DEMAW-SIM-FIG. 4.6 is a graphical representation of the generation of inverted information signal in the circuit of DEMAW-SIM-FIG. 1.6.



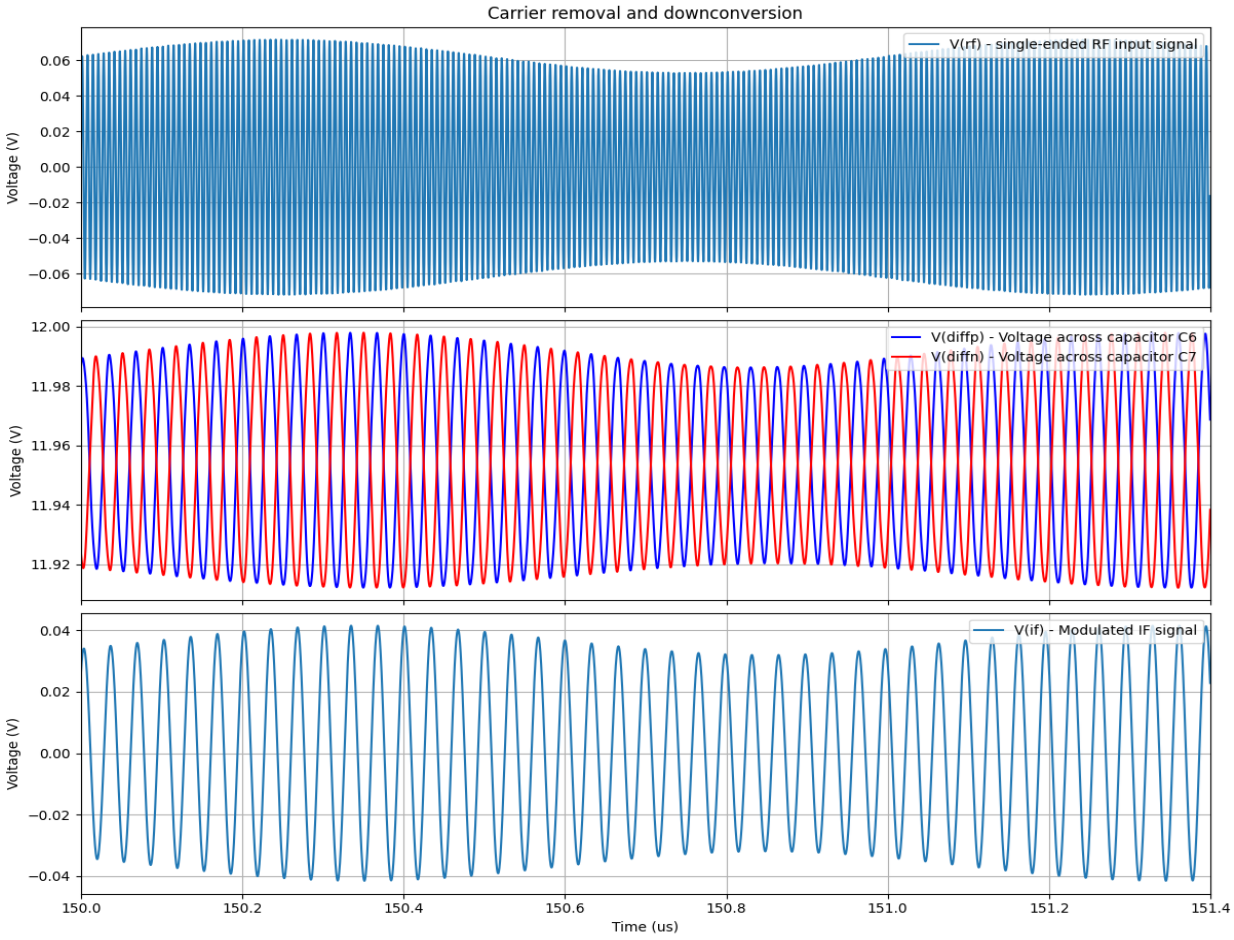
DEMAW-SIM-FIG. 4.6. Graphical representation of the generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.6).

46. DEMAW-SIM-FIG. 5.6 is a graphical representation of the charging and discharging cycles for capacitors C4 and C5 in circuit of DEMAW-SIM-FIG. 1.6.



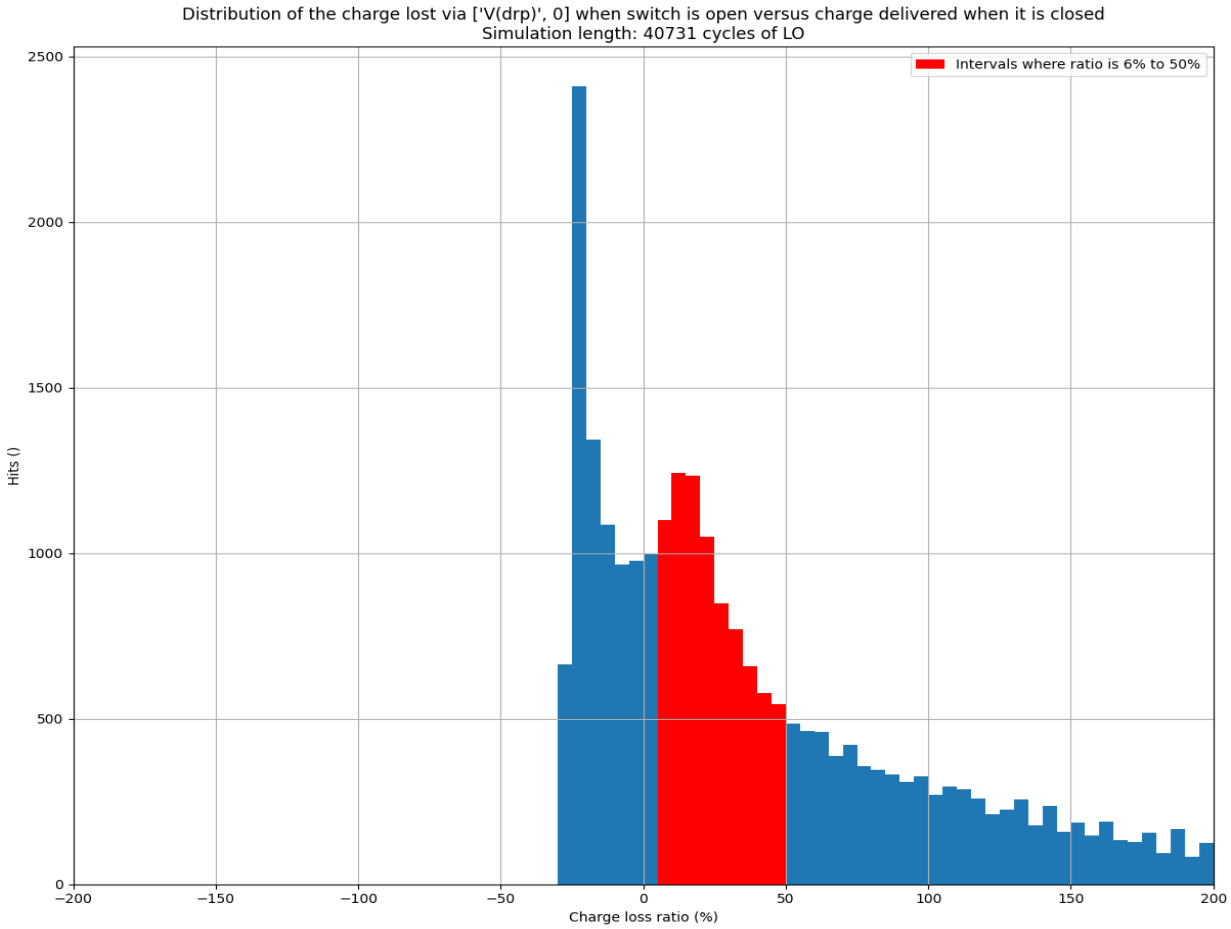
DEMAW-SIM-FIG. 5.6. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.6).

47. DEMAW-SIM-FIG.6.6 is a graphical representation of carrier removal and down-conversion for circuit of DEMAW-SIM-FIG. 1.6.



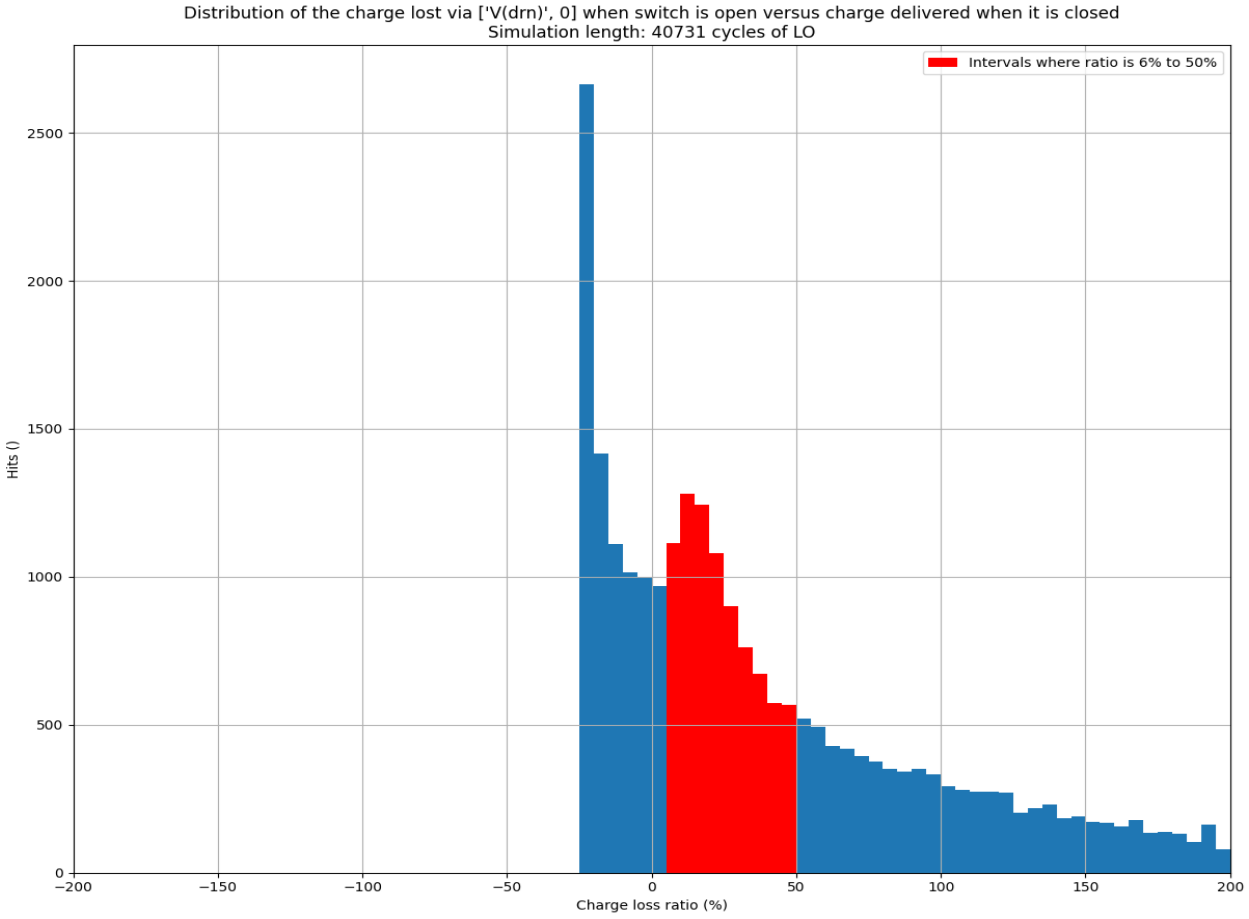
DEMAW-SIM-FIG. 6.6. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.6).

48. DEMAW-SIM-FIG. 7.6A is a histogram showing charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.6.



DEMAW-SIM-FIG. 7.6A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.6).

49. DEMAW-SIM-FIG. 7.6B is a histogram of the charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.6.



DEMAW-SIM-FIG. 7.6B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.6).

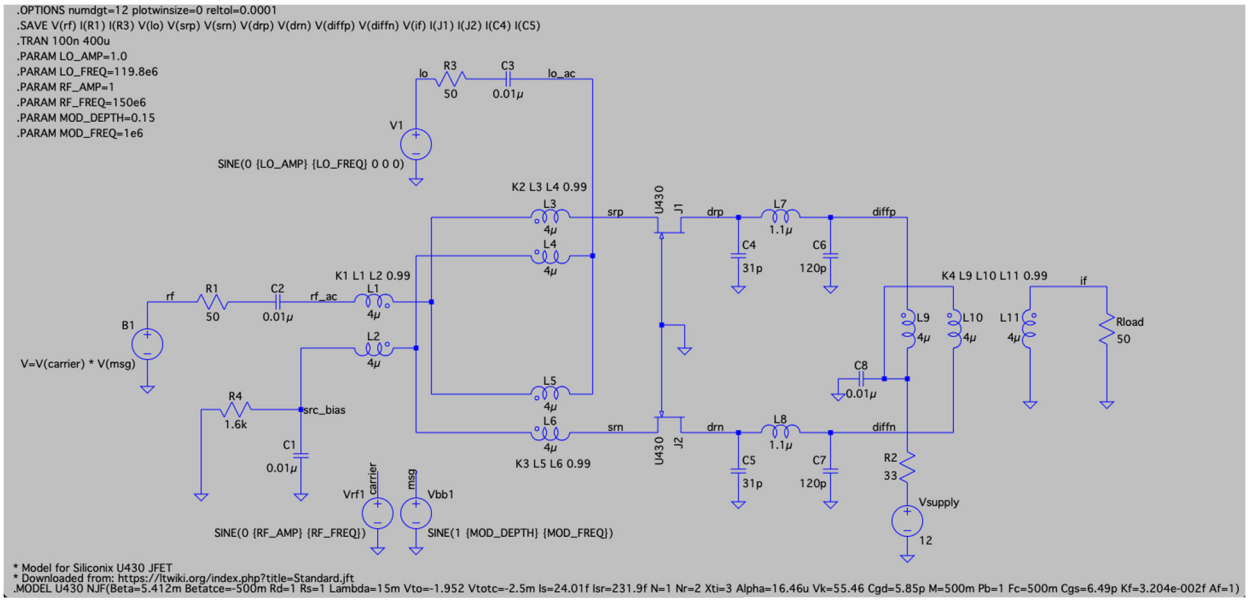
IV. DeMaw Circuit Modified to Match DeMaw FIG. 6.7 With a Sinusoidal LO

50. As I testified in my deposition, using sinusoidal LO signals in place of squared-up LO signals would not result in circuit behavior that would lead to different conclusions than those presented in my original Declaration, despite the POPR's false claims to the contrary. The simulation results presented in this section support my testimony. They correspond to the same circuit and input conditions as those for the simulation results presented in Section **Error! Reference source not**

found. except with a sinusoidal LO in place of a squared-up LO.

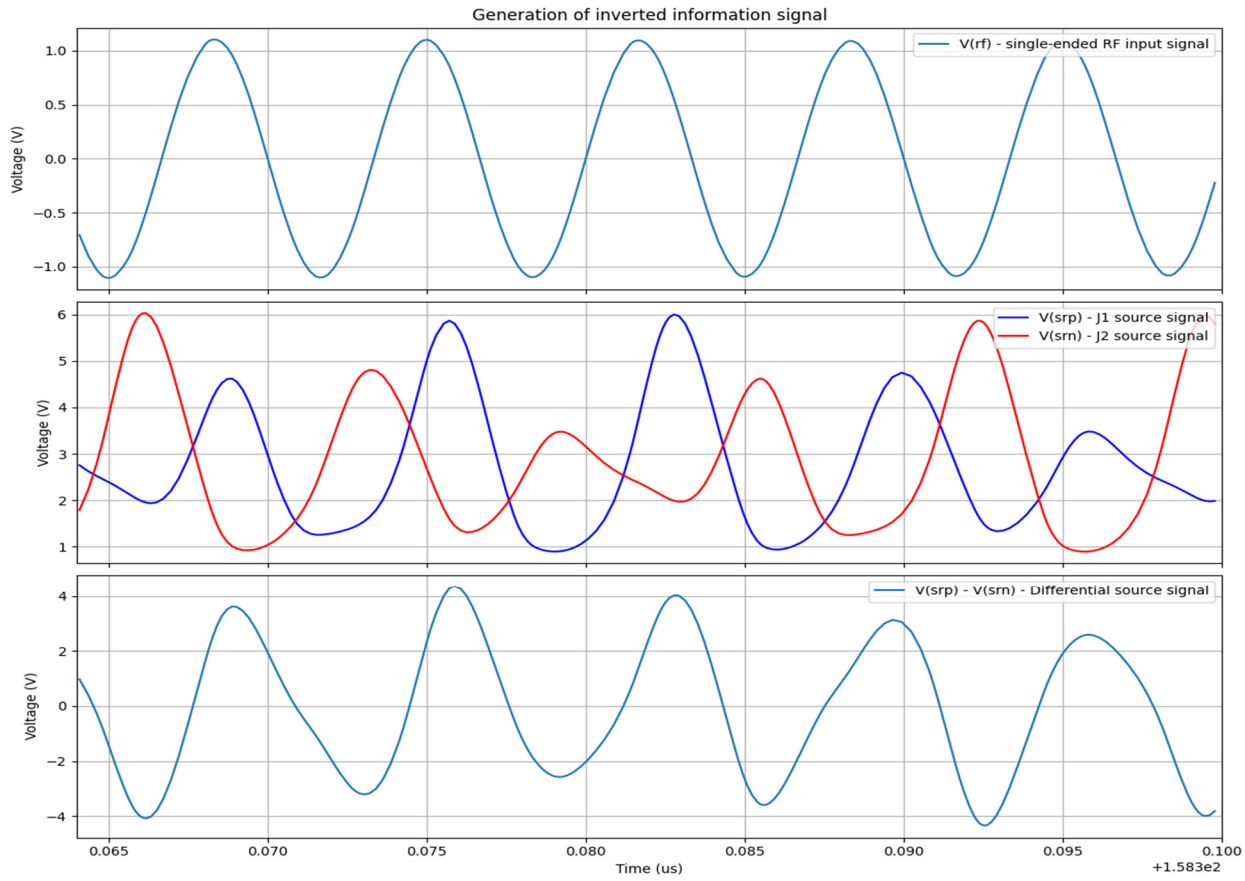
A. Simulation Results For a Large Input Signal

51. DEMAW-SIM-FIG. 1.7 is a schematic illustration of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and a large input signal. I have created additional figures DEMAW-SIM-FIGS. 4.7, 5.7, 6.7, 7.7A and 7.7B based on simulation output from DEMAW-SIM-FIG. 1.7. DEMAW-SIM-FIGS. 4.7, 5.7, 6.7, 7.7A and 7.7B show the same simulation output from DEMAW-SIM-FIG. 1.7 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.7, 4.7, 5.7, 6.7, 7.7A and 7.7B.



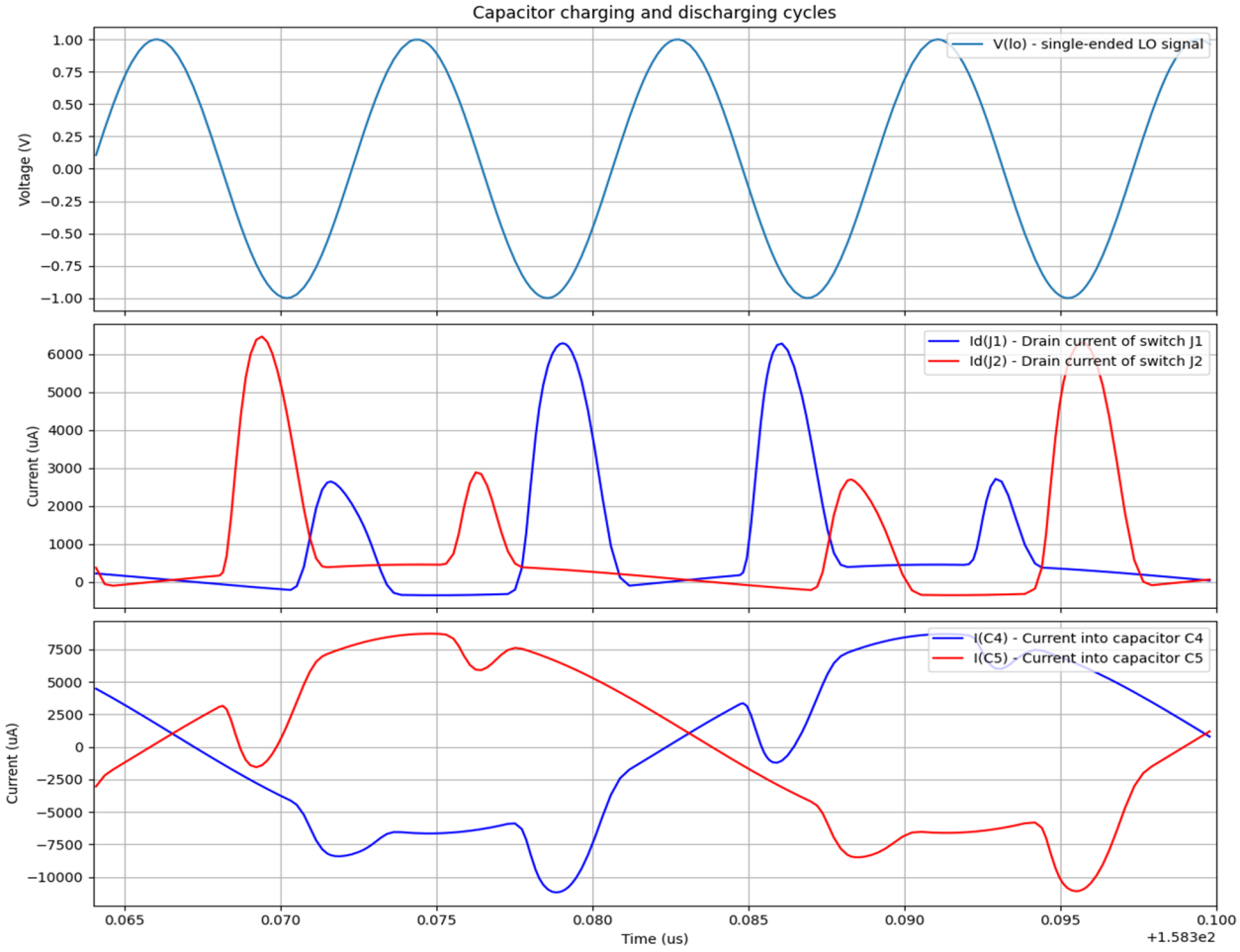
DEMAW-SIM-FIG. 1.7. DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and a large input signal.

52. DEMAW-SIM-FIG. 4.7 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.7.



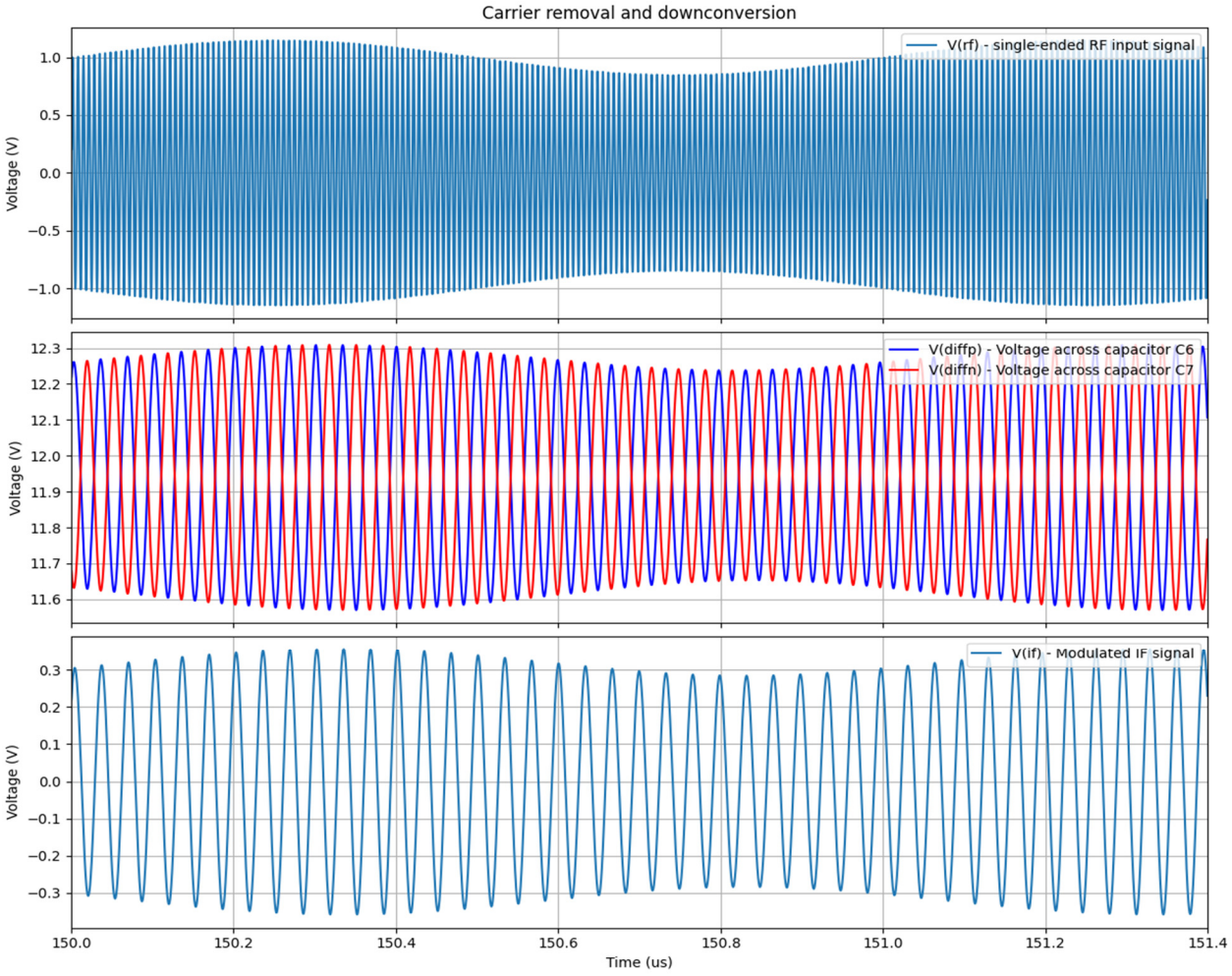
DEMAW-SIM-FIG. 4.7. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.7).

53. DEMAW-SIM-FIG. 5.7 is a graphical representation of the charging and discharging cycles of capacitors C4 and C5 for circuit of DEMAW-SIM-FIG. 1.7.



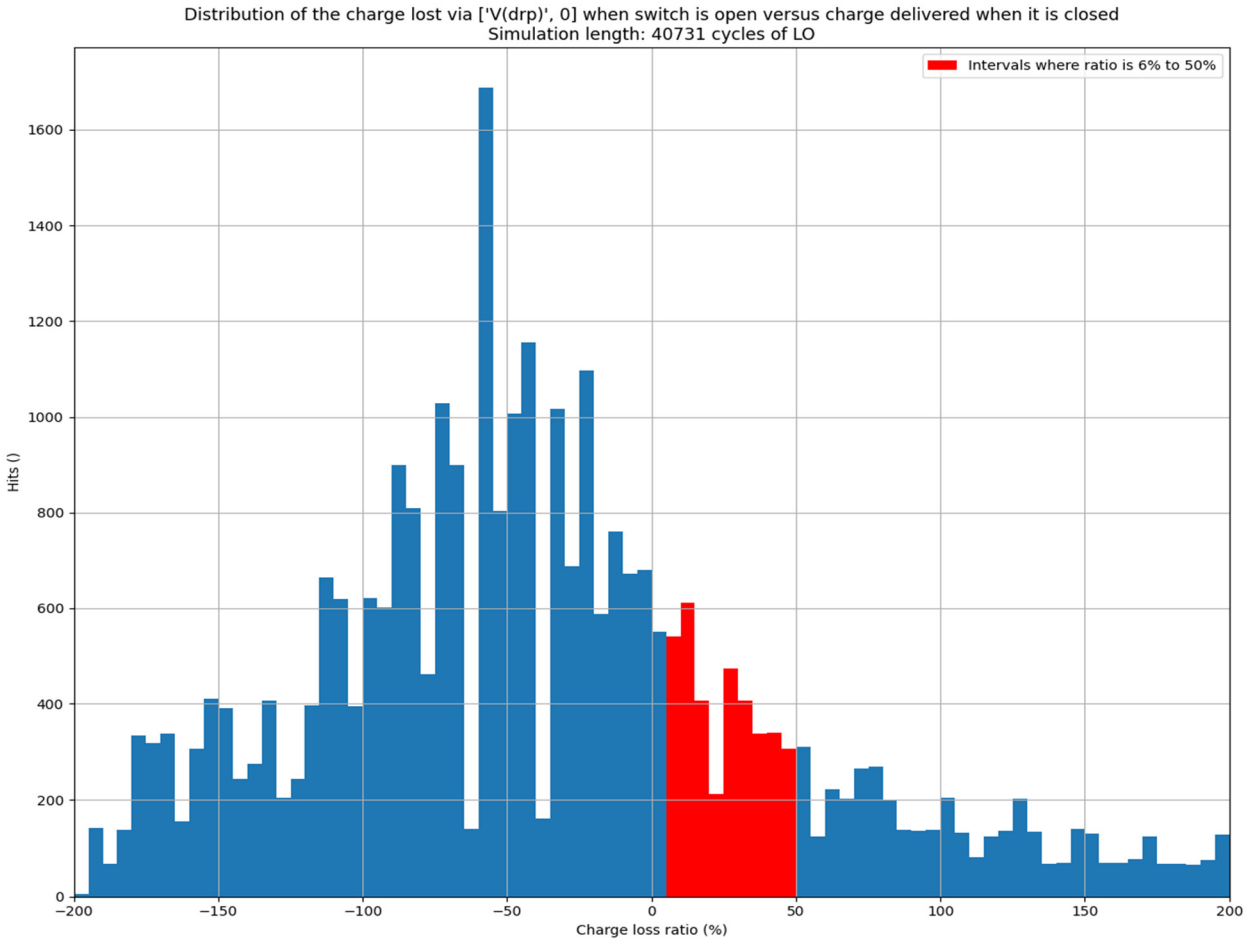
DEMAW-SIM-FIG. 5.7. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.7).

54. DEMAW-SIM-FIG. 6.7 is a graphical representation showing carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.7.



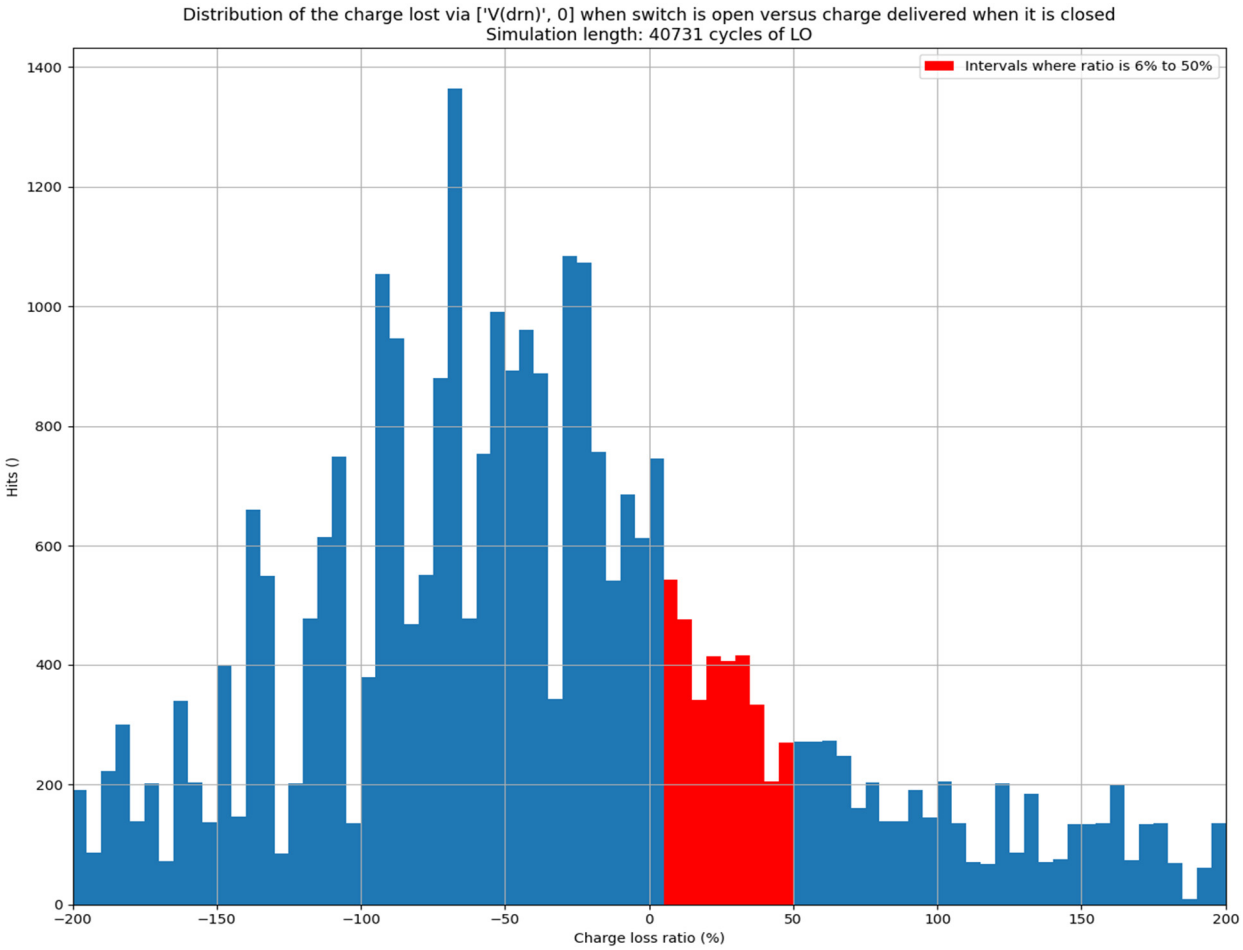
DEMAW-SIM-FIG. 6.7. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.7).

55. DEMAW-SIM-FIG. 7.7A is a histogram of the charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.7.



DEMAW-SIM-FIG. 7.7A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.7).

56. DEMAW-SIM-FIG. 7.7B is a histogram of the charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.7.

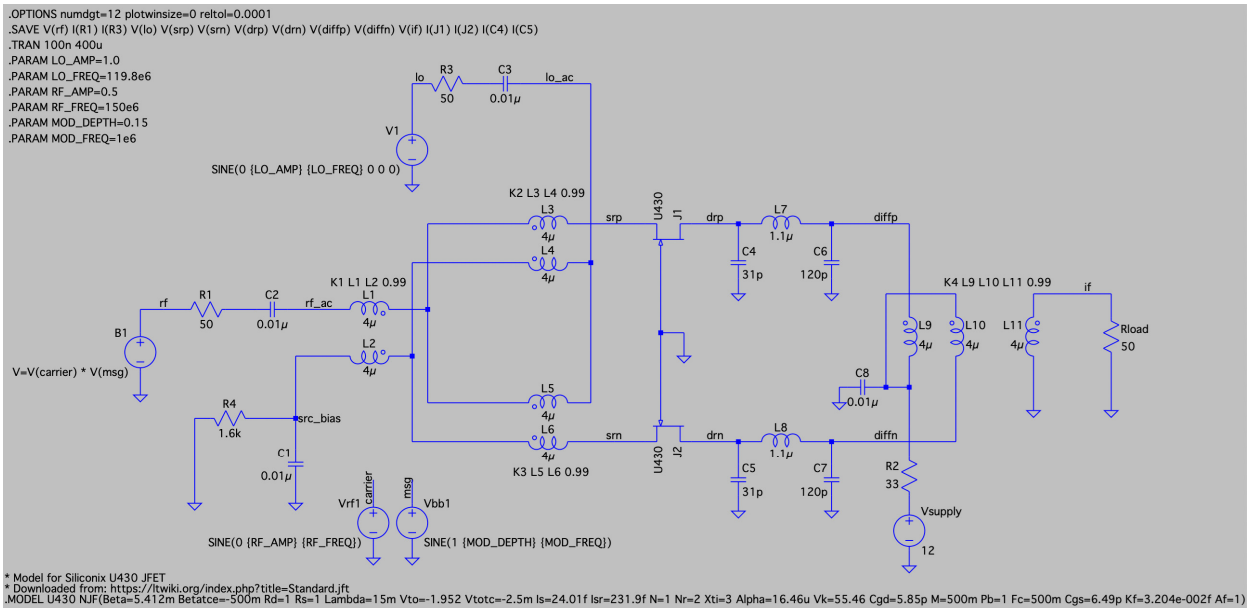


DEMAW-SIM-FIG. 7.7B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.7).

B. Simulation Results For an Input Signal Reduced by 6 dB

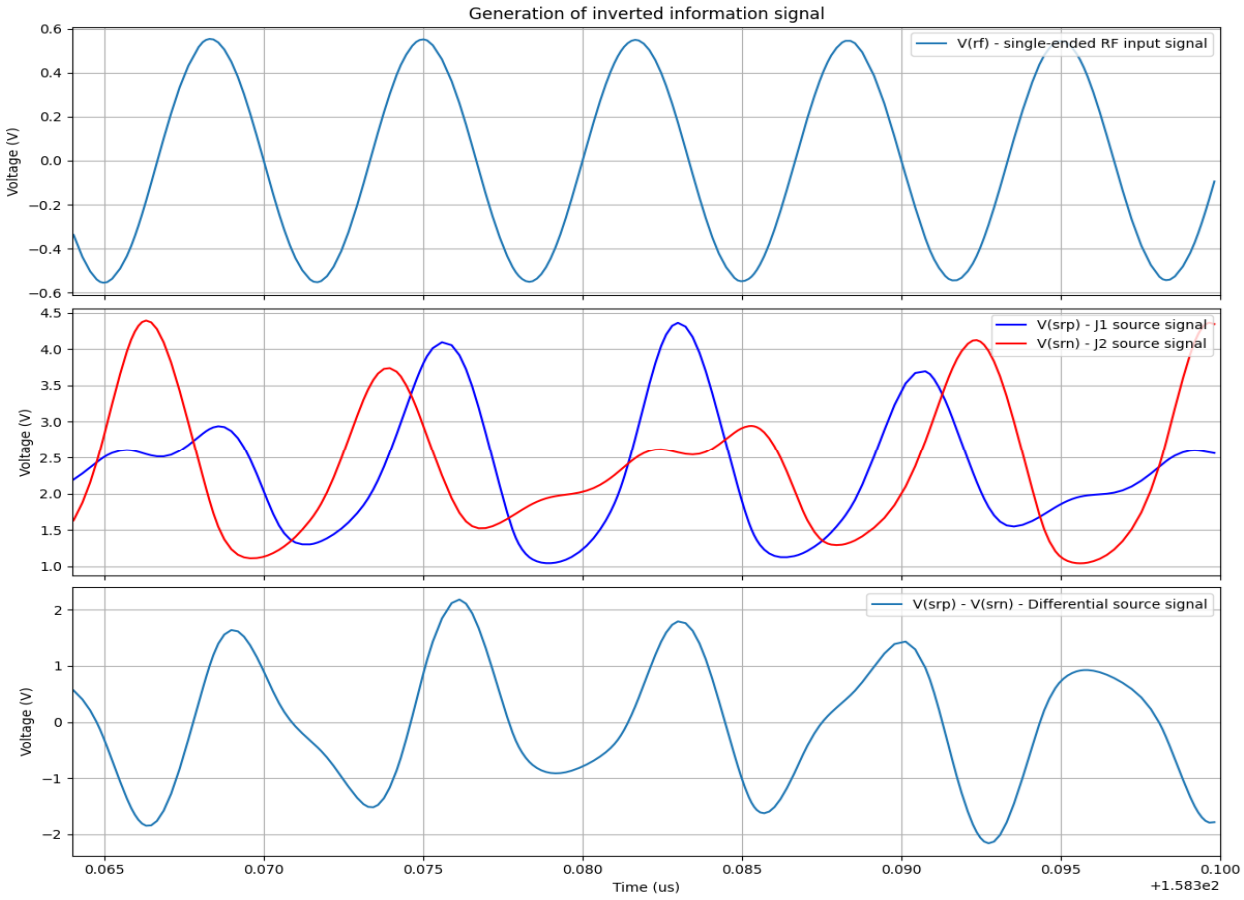
57. DEMAW-SIM-FIG. 1.8 is a schematic illustration of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 6 dB. I have created additional figures DEMAW-SIM-FIGS. 4.8, 5.8, 6.8, 7.8A and 7.8B based on simulation output from DEMAW-SIM-FIG. 1.8. DEMAW-SIM-FIGS. 4.8, 5.8, 6.8, 7.8A and 7.8B show the same simulation output from DEMAW-SIM-FIG. 1.8 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from

DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.8, 4.8, 5.8, 6.8, 7.8A and 7.8B.



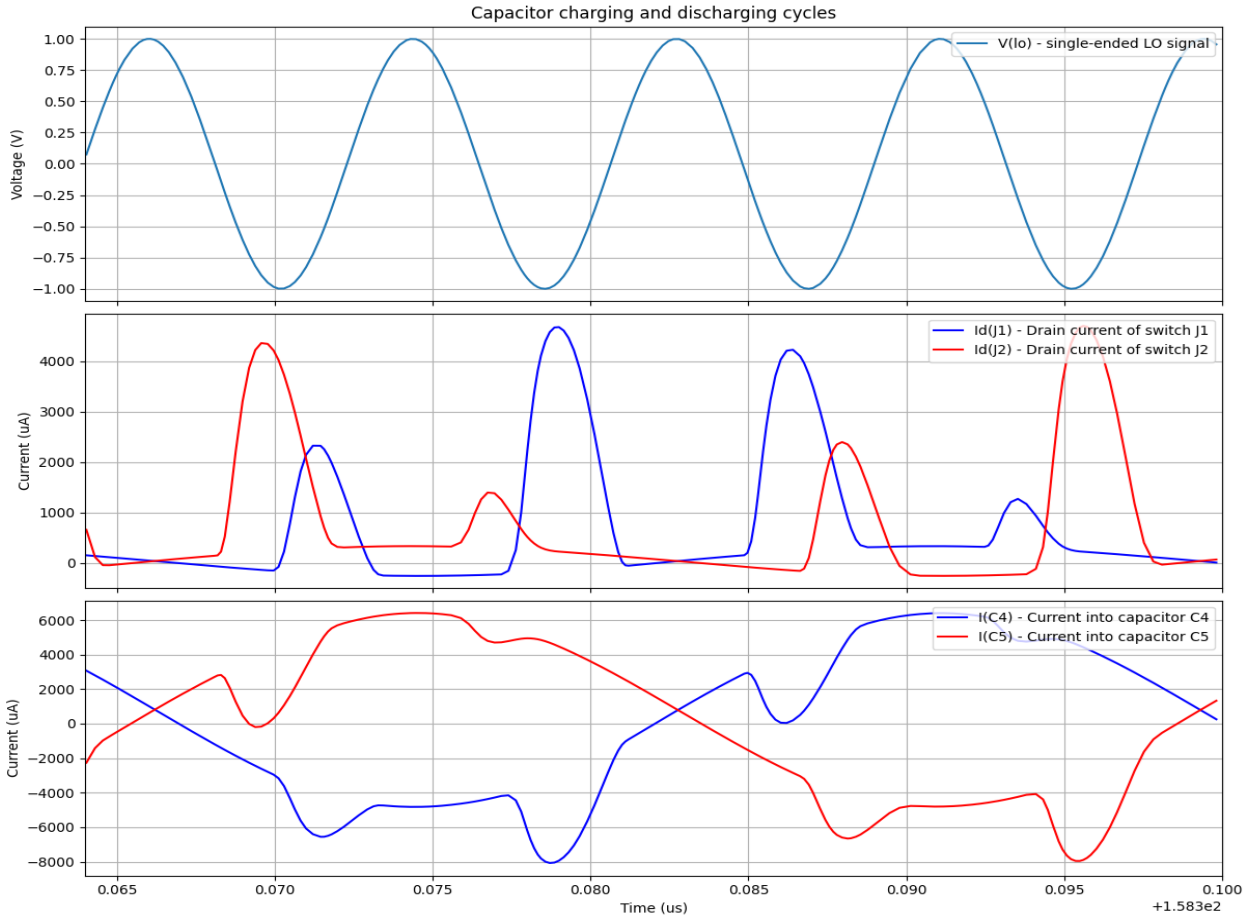
DEMAW-SIM-FIG. 1.8. DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 6 dB.

58. DEMAW-SIM-FIG. 4.8 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.8.



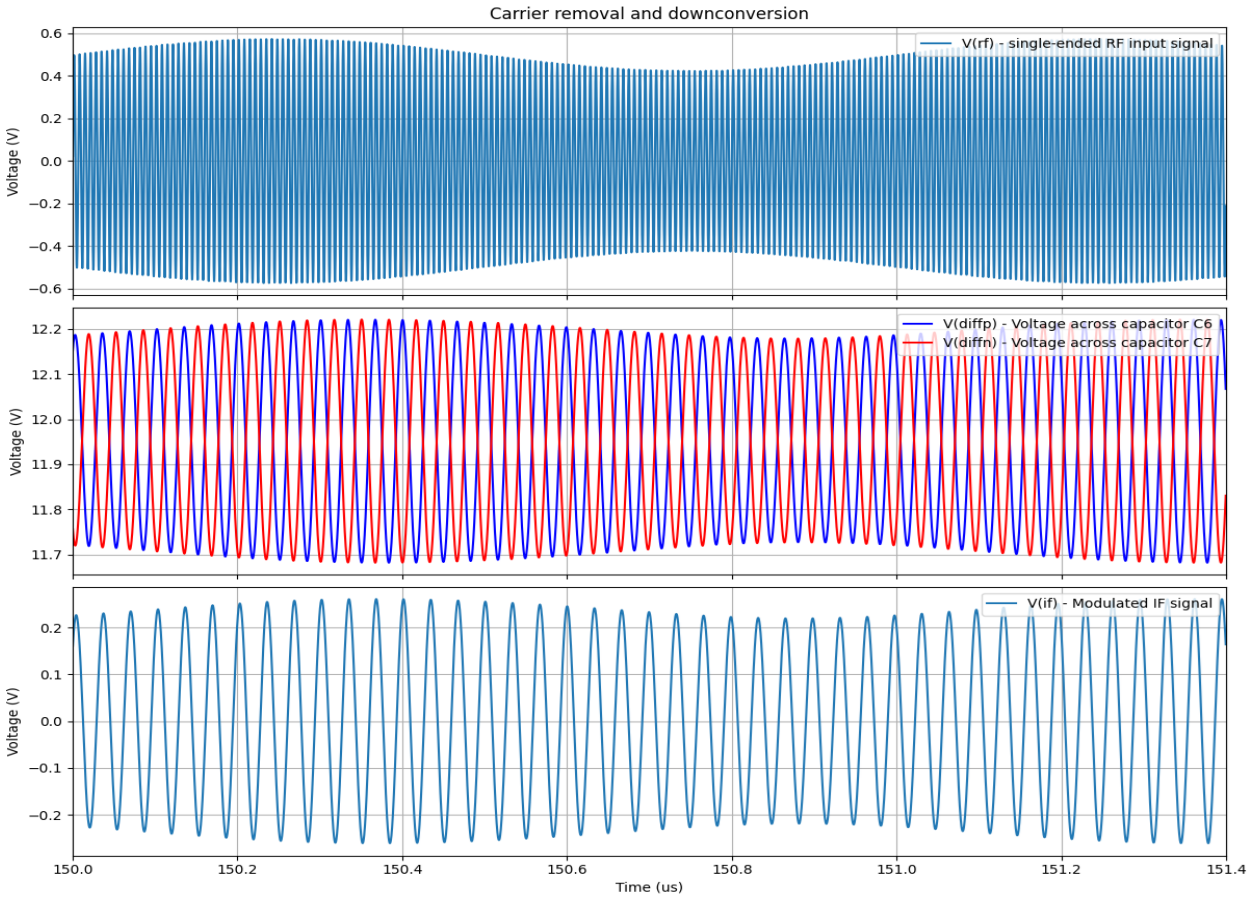
DEMAW-SIM-FIG. 4.8. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.8).

59. DEMAW-SIM-FIG. 5.8 is a graphical representation of the charging and discharging cycles for capacitors C4 and C5 of the circuit of DEMAW-SIM-FIG. 1.8.



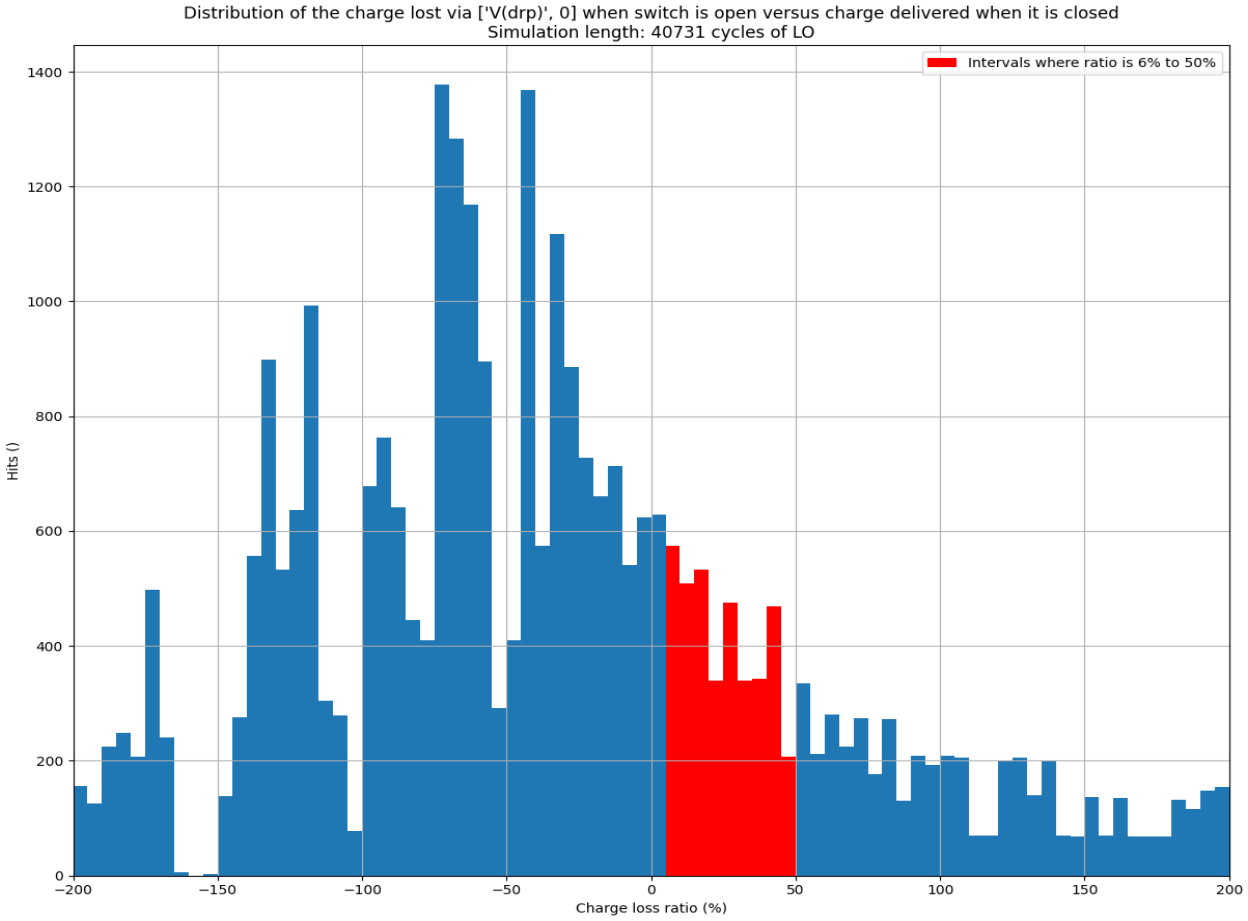
DEMAW-SIM-FIG. 5.8. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.8).

60. DEMAW-SIM-FIG. 6.8 is a graphical representation of the carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.8.



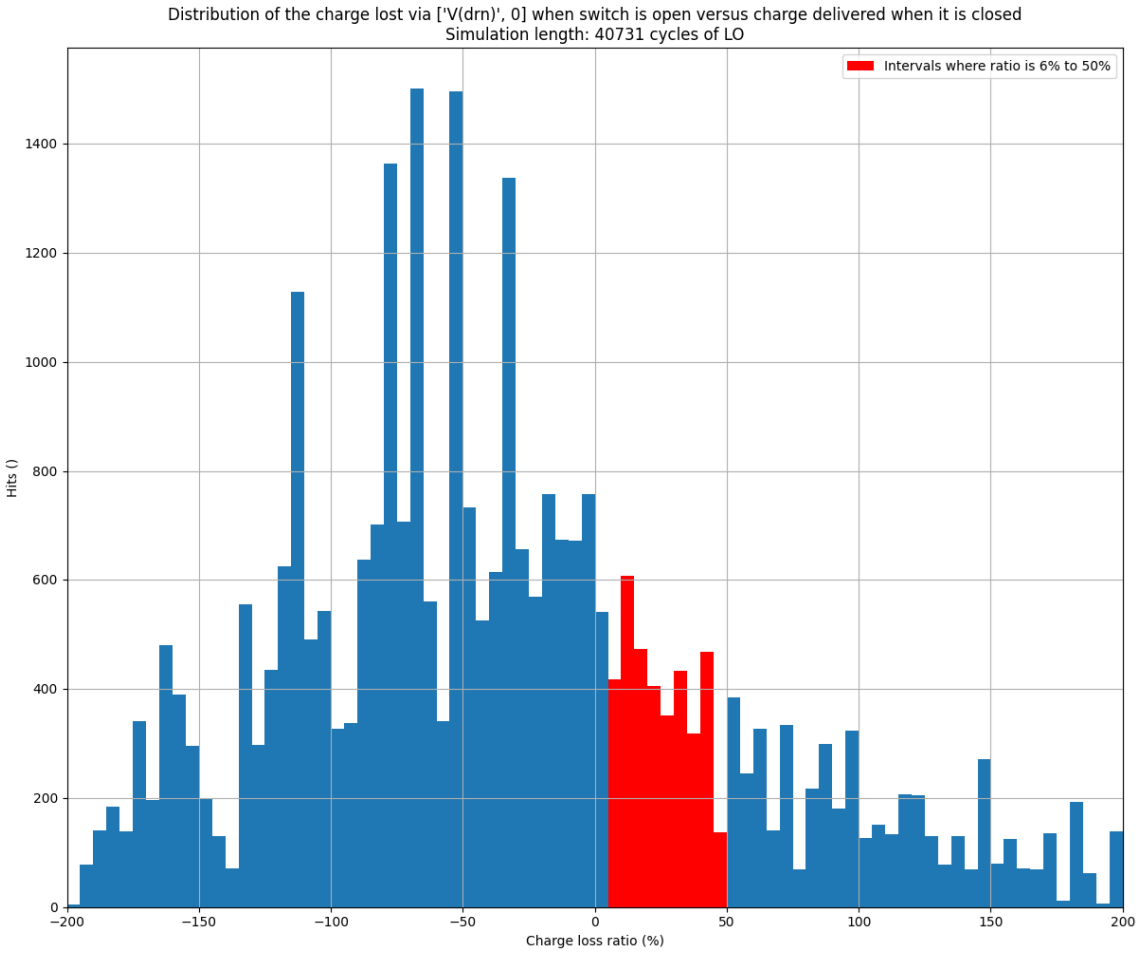
DEMAW-SIM-FIG. 6.8. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.8).

61. DEMAW-SIM-FIG. 7.8A is a histogram of the charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.8.



DEMAW-SIM-FIG. 7.8A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.8).

62. DEMAW-SIM-FIG. 7.8B is a histogram of the charge loss ratio percentages for capacitor C5 of the circuit of DEMAW-SIM-FIG. 1.8.

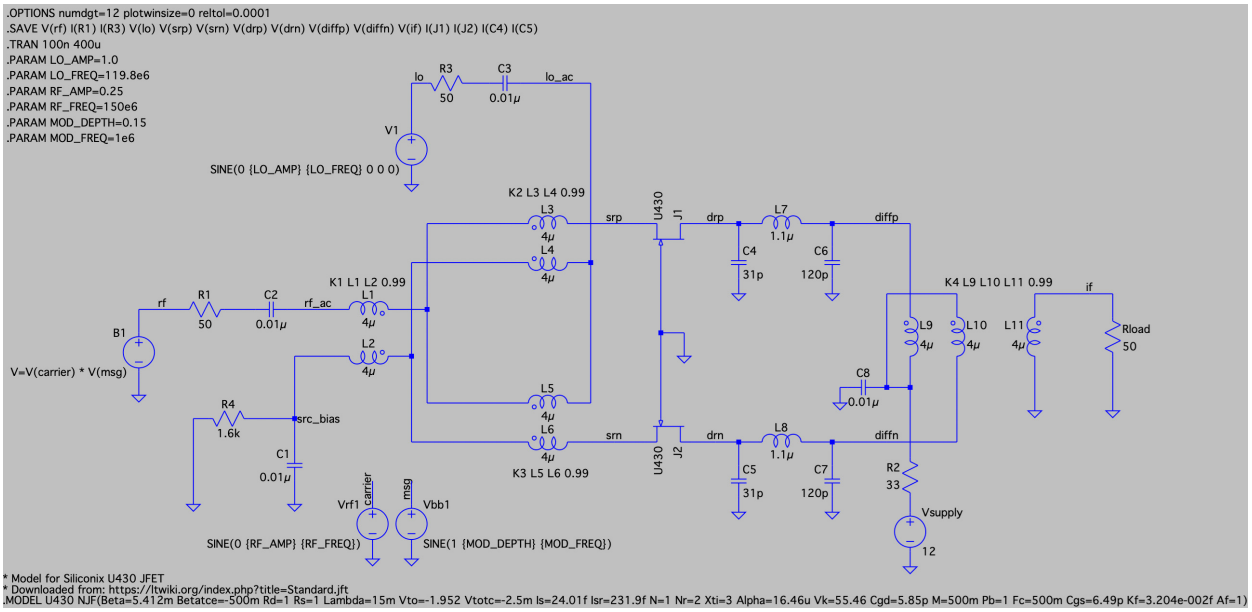


DEMAW-SIM-FIG. 7.8B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.8).

C. Simulation Results For an Input Signal Reduced by 12 dB

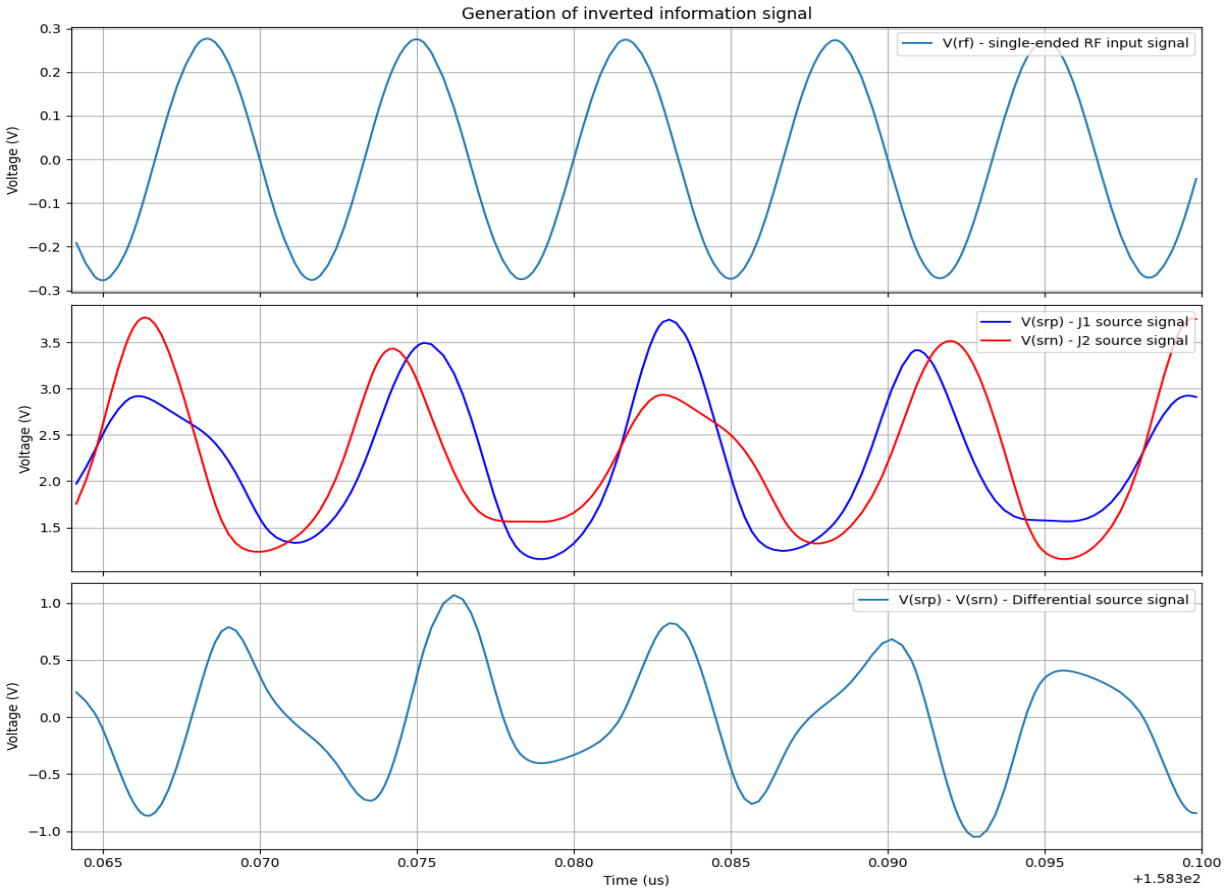
63. DEMAW-SIM-FIG. 1.9 is a schematic representation of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 12 dB. I have created additional figures DEMAW-SIM-FIGS. 4.9, 5.9, 6.9, 7.9 and 7.9B based on simulation output from DEMAW-SIM-FIG. 1.9. DEMAW-SIM-FIGS. 4.9, 5.9, 6.9, 7.9A and 7.9B show the same simulation output from DEMAW-SIM-FIG. 1.9 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from

DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.9, 4.9, 5.9, 6.9, 7.9A and 7.9B.



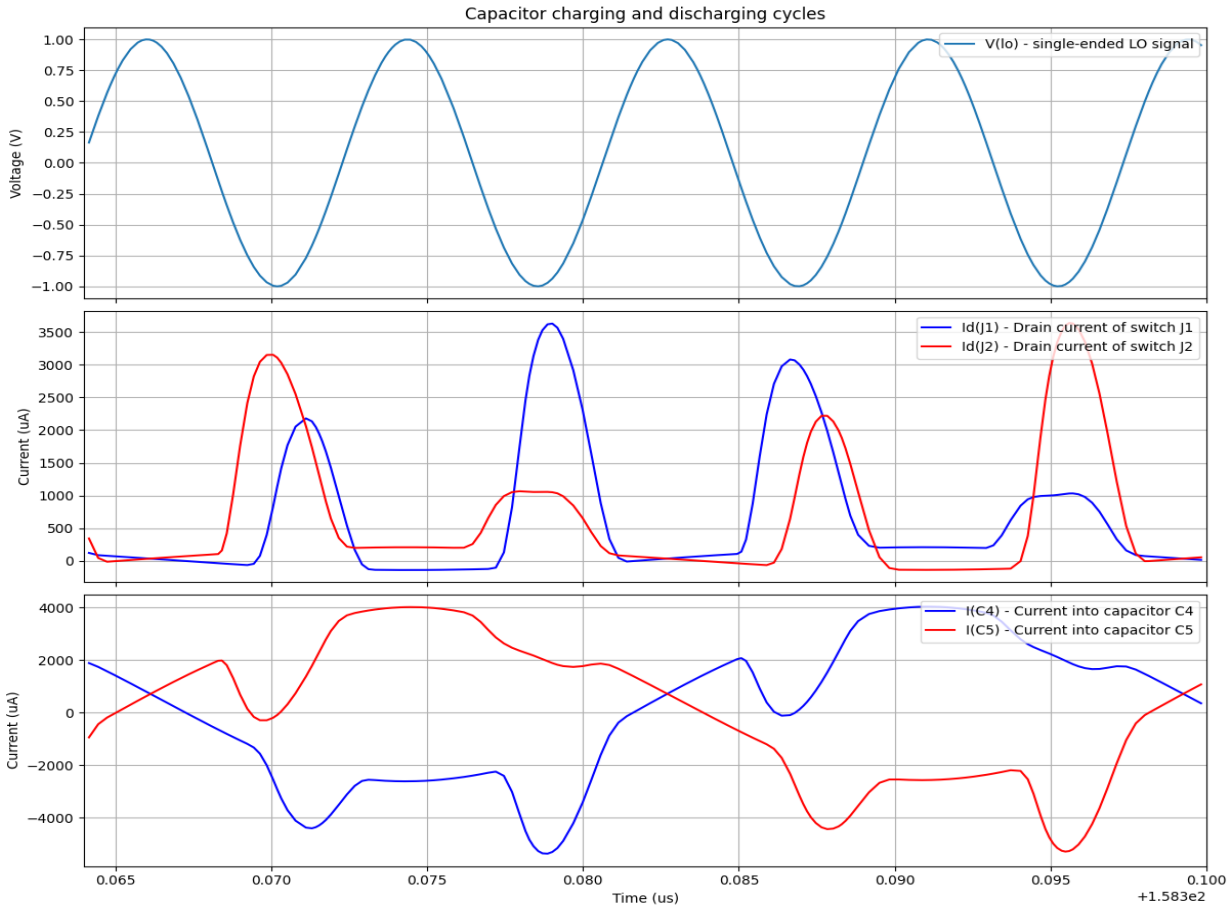
DEMAW-SIM-FIG. 1.9. DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 12 dB.

64. DEMAW-SIM-FIG. 4.9 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.9.



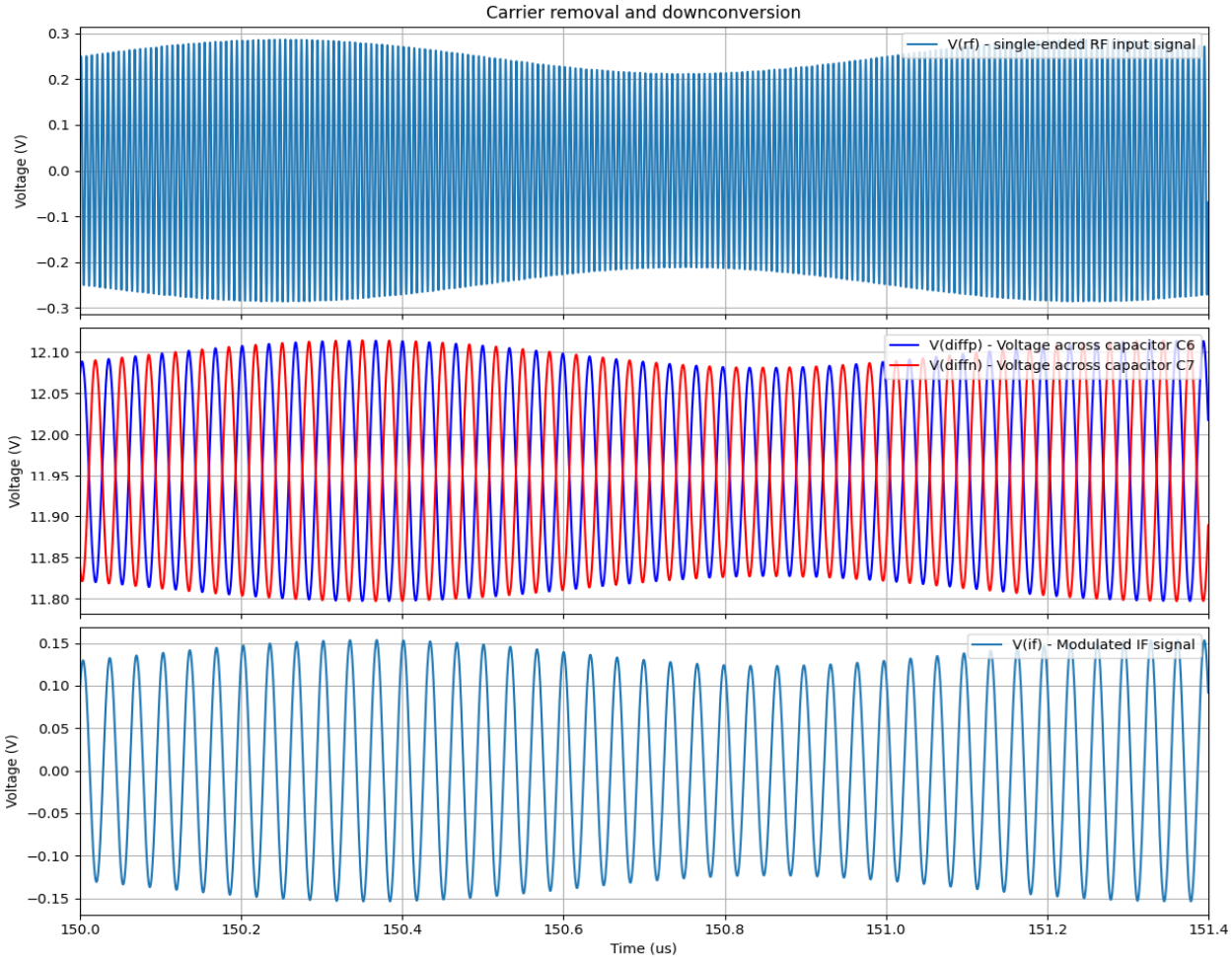
DEMAW-SIM-FIG. 4.9. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.9).

65. DEMAW-SIM-FIG. 5.9 is a graphical representation of the charging and discharging cycles for capacitors C4 and C5 of the circuit of DEMAW-SIM-FIG. 1.9.



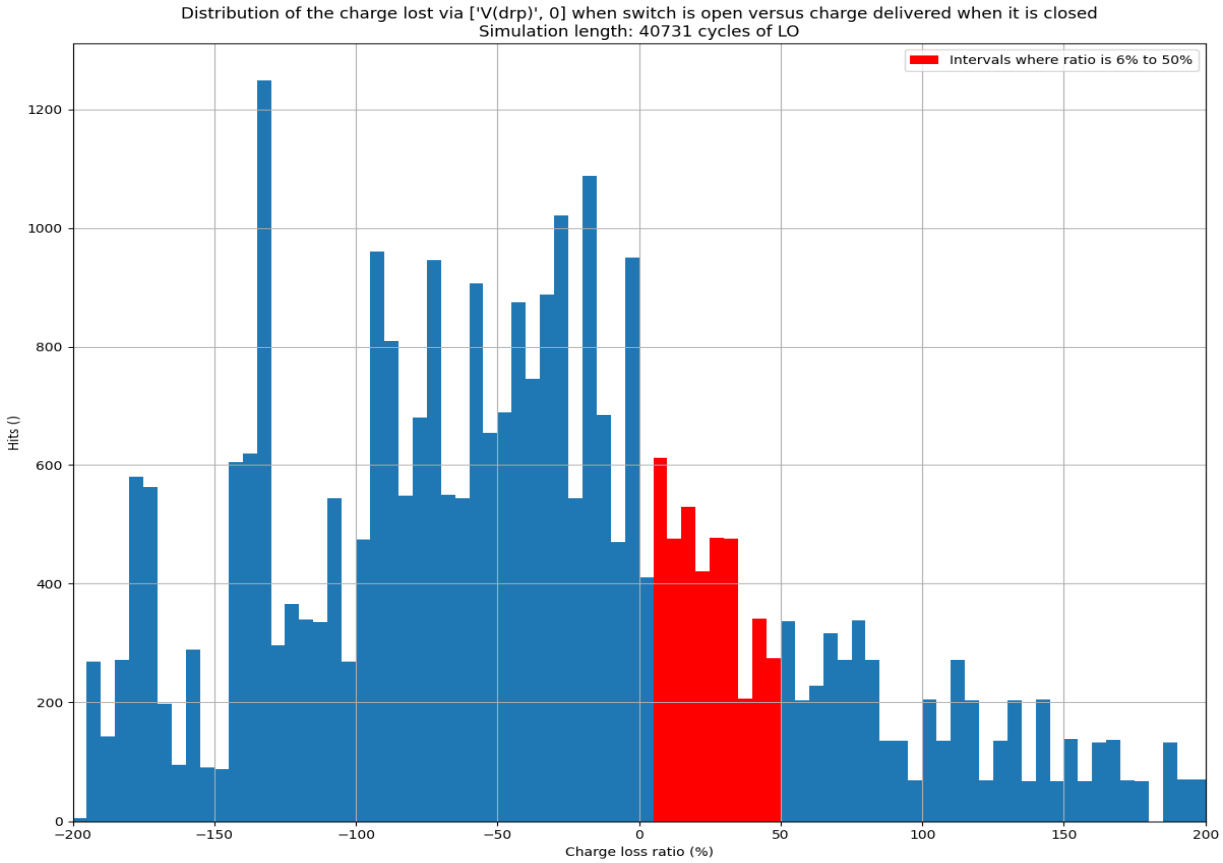
DEMAW-SIM-FIG. 5.9. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.9).

66. DEMAW-SIM-FIG. 6.9 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.9.



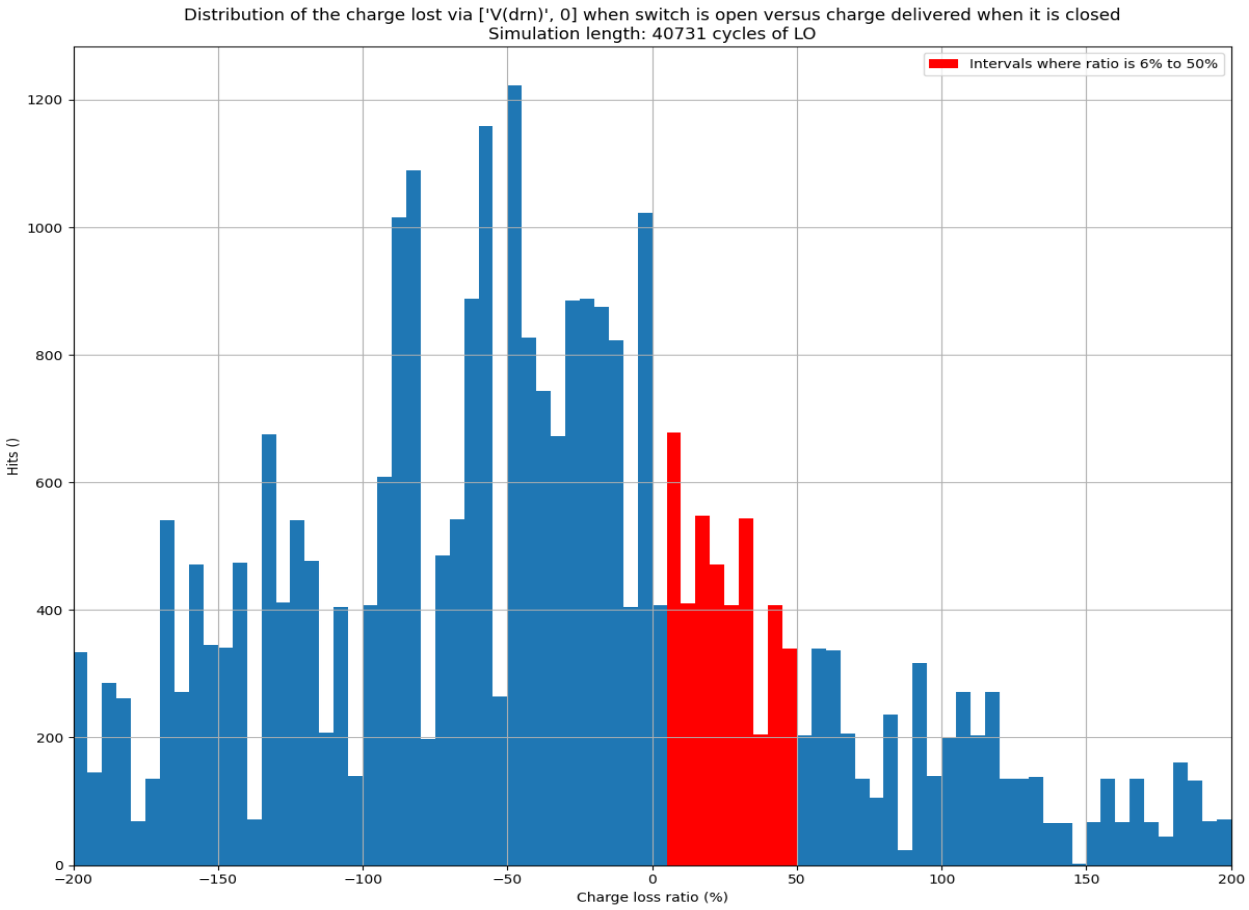
67. DEMAW-SIM-FIG. 6.9. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.9).

68. DEMAW-SIM-FIG. 7.9A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.9.



DEMAW-SIM-FIG. 7.9A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.9).

69. DEMAW-SIM-FIG. 7.9B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.9.

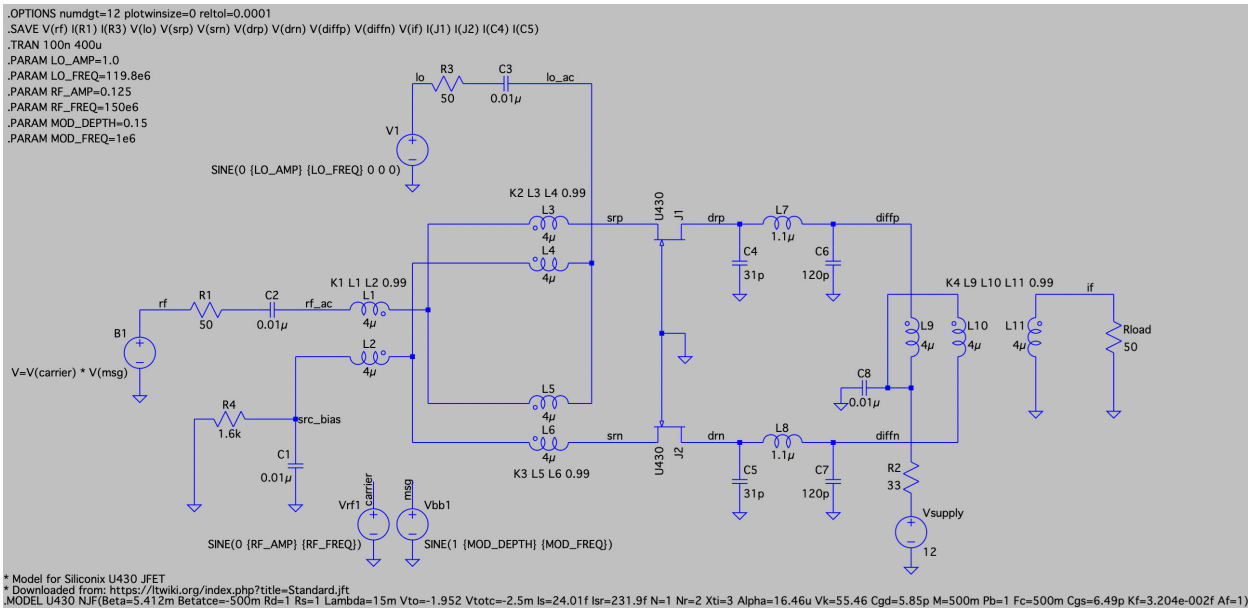


70. DEMAW-SIM-FIG. 7.9B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.9).

D. Simulation Results For an Input Signal Reduced by 18 dB

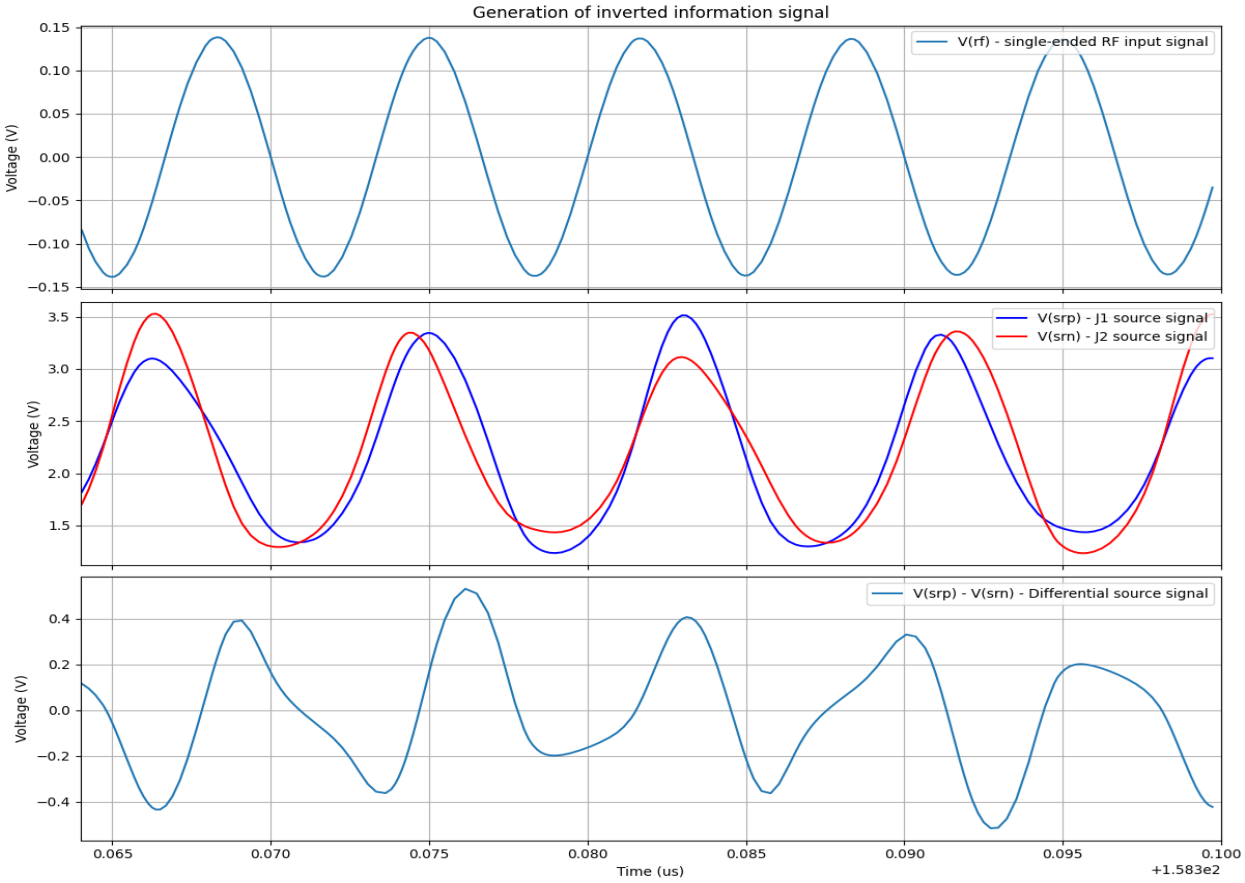
71. DEMAW-SIM-FIG. 1.10 is a schematic illustration of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 18 dB. I have created additional figures DEMAW-SIM-FIGS. 4.10, 5.10, 6.10, 7.10A and 7.10B based on simulation output from DEMAW-SIM-FIG. 1.10. DEMAW-SIM-FIGS. 4.10, 5.10, 6.10, 7.10A and 7.10B show the same simulation output from DEMAW-SIM-FIG. 1.10 as DEMAW-SIM-FIGS. 4, 5, 6,

and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.10, 4.10, 5.10, 6.10, 7.10A and 7.10B.



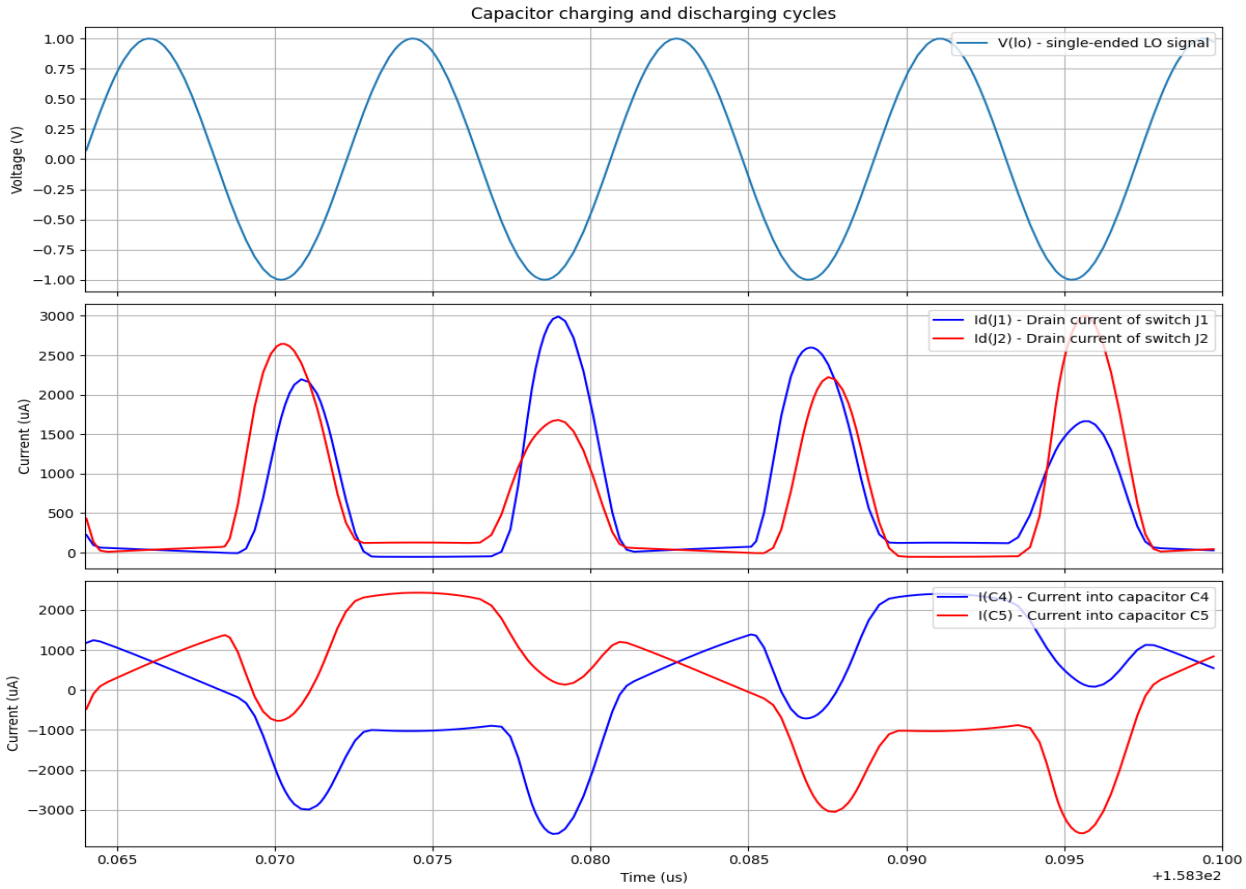
DEMAW-SIM-FIG. 1.10. DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 18 dB.

72. DEMAW-SIM-FIG. 4.10 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.10).



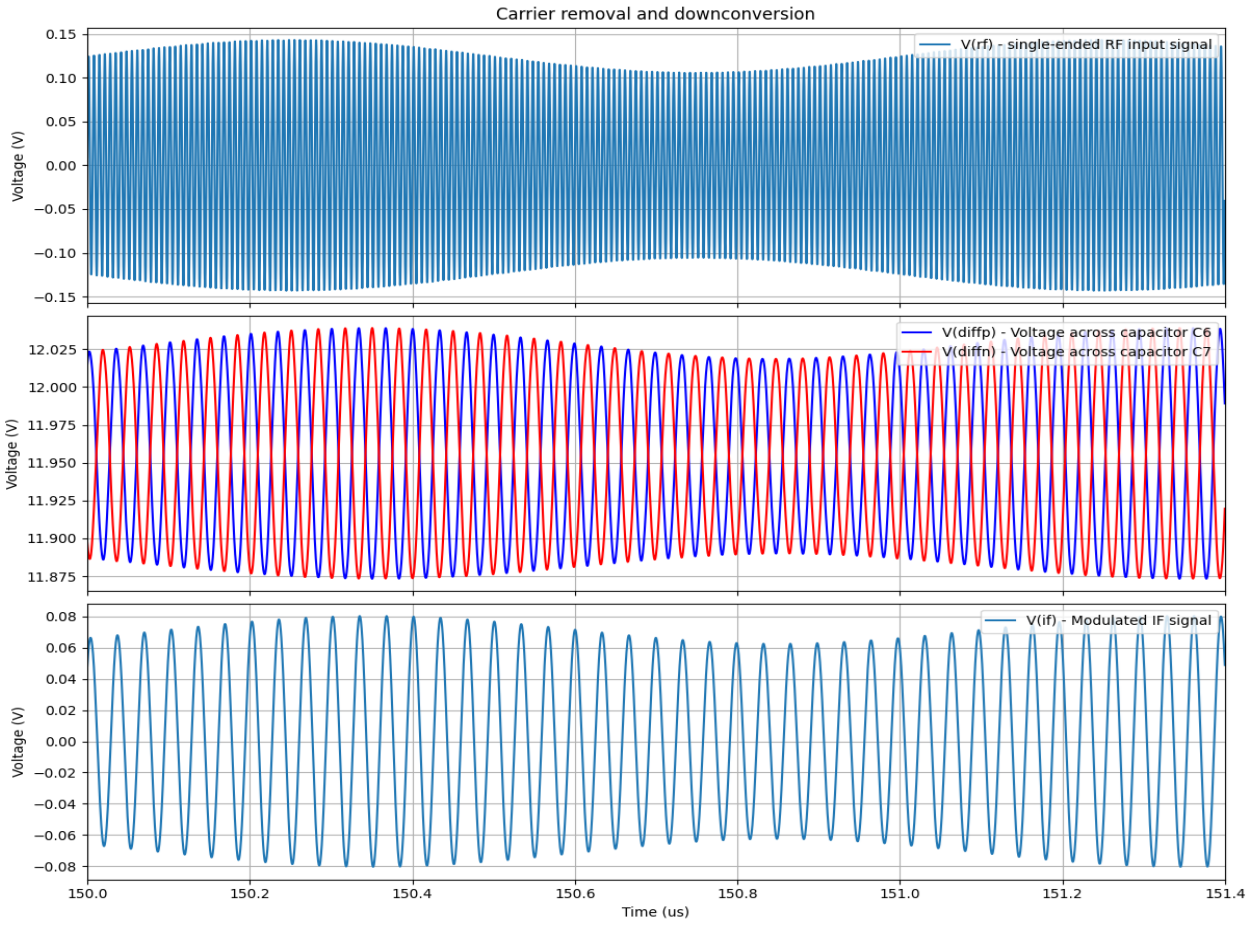
DEMAW-SIM-FIG. 4.10. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.10).

73. DEMAW-SIM-FIG. 5.10 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.10.



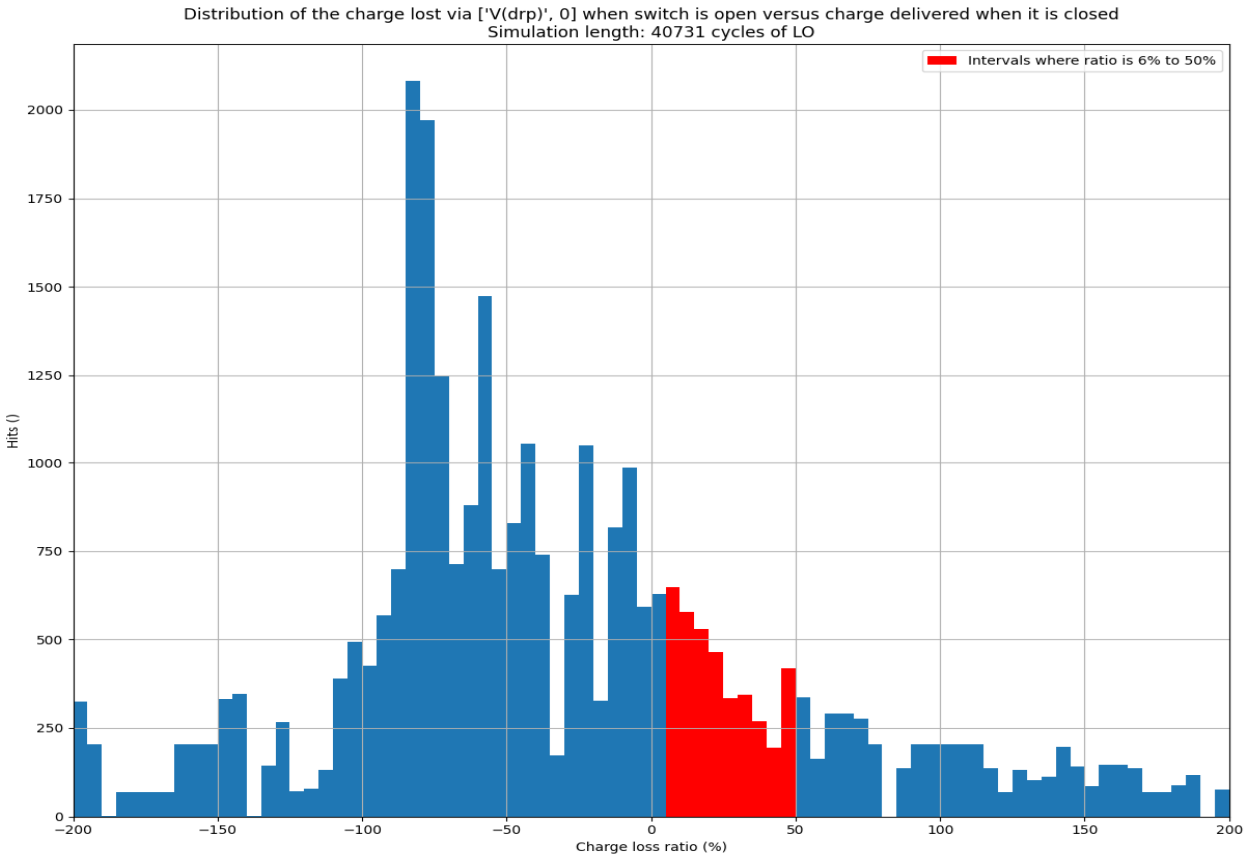
DEMAW-SIM-FIG. 5.10. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.10).

74. DEMAW-SIM-FIG. 6.10 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.10.



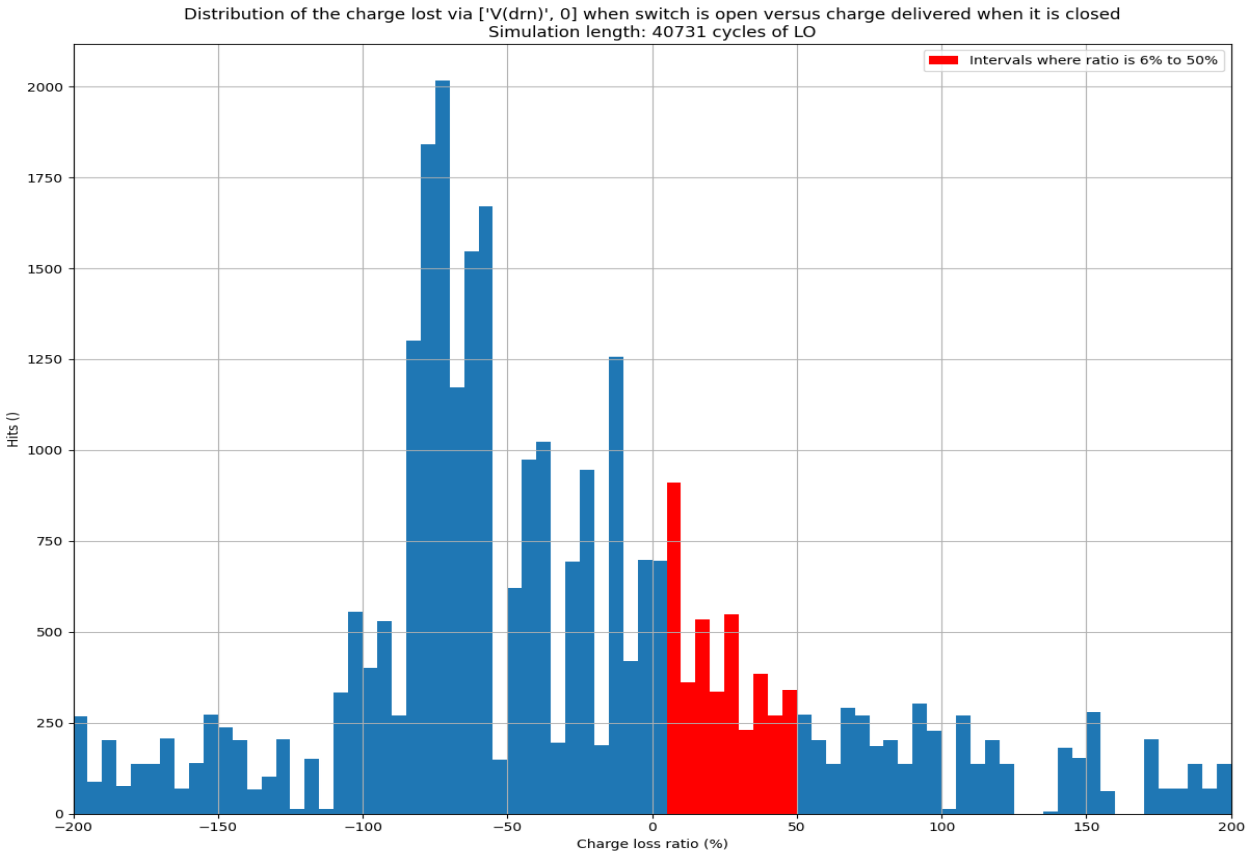
DEMAW-SIM-FIG. 6.10. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.10).

75. DEMAW-SIM-FIG. 7.10A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.10.



DEMAW-SIM-FIG. 7.10A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.10).

76. DEMAW-SIM-FIG. 7.10B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.10.

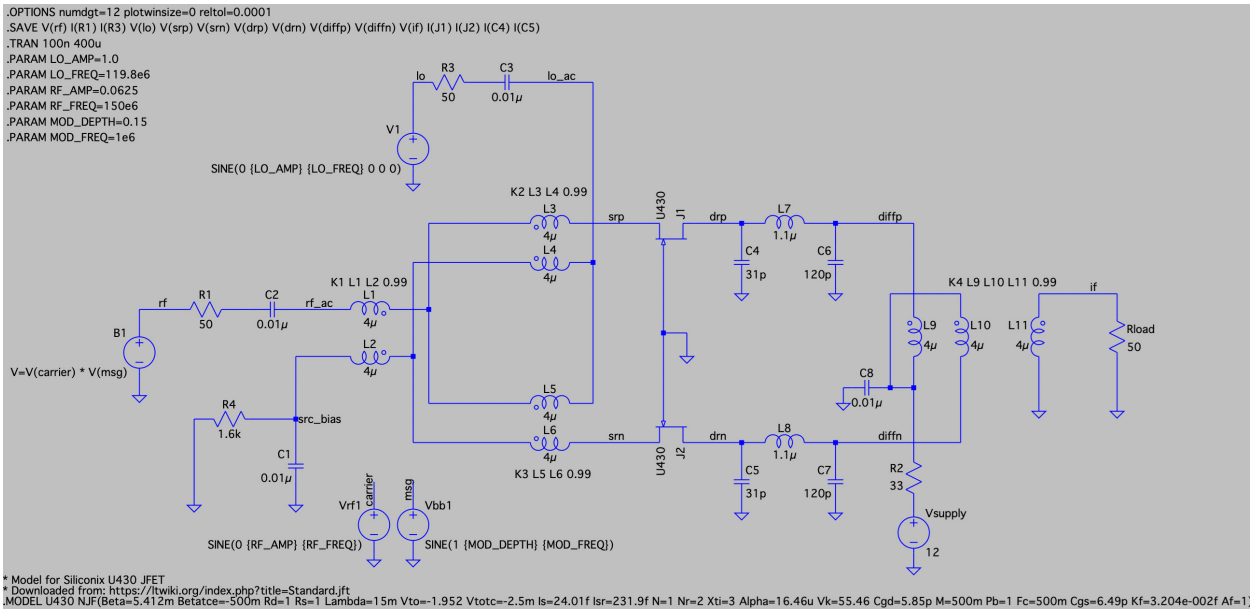


DEMAW-SIM-FIG. 7.10B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.10).

E. Simulation Results For an Input Signal Reduced by 24 dB

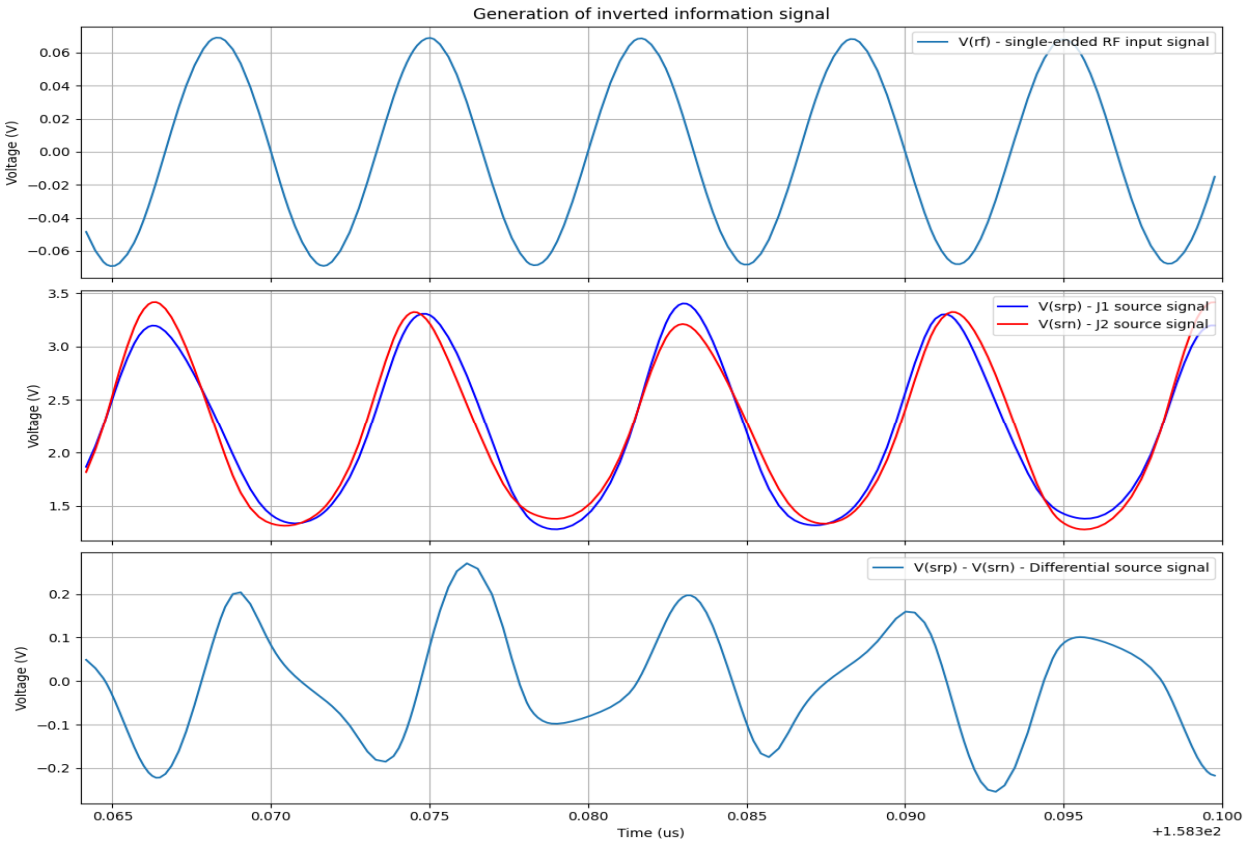
77. DEMAW-SIM-FIG. 1.11 is a schematic illustration of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 24 dB. I have created additional figures DEMAW-SIM-FIGS. 4.11, 5.11, 6.11, 7.11A and 7.11B based on simulation output from DEMAW-SIM-FIG. 1.11. DEMAW-SIM-FIGS. 4.11, 5.11, 6.11, 7.11A and 7.11B show the same simulation output from DEMAW-SIM-FIG. 1.11 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.11, 4.11, 5.11, 6.11, 7.11A and 7.11B.



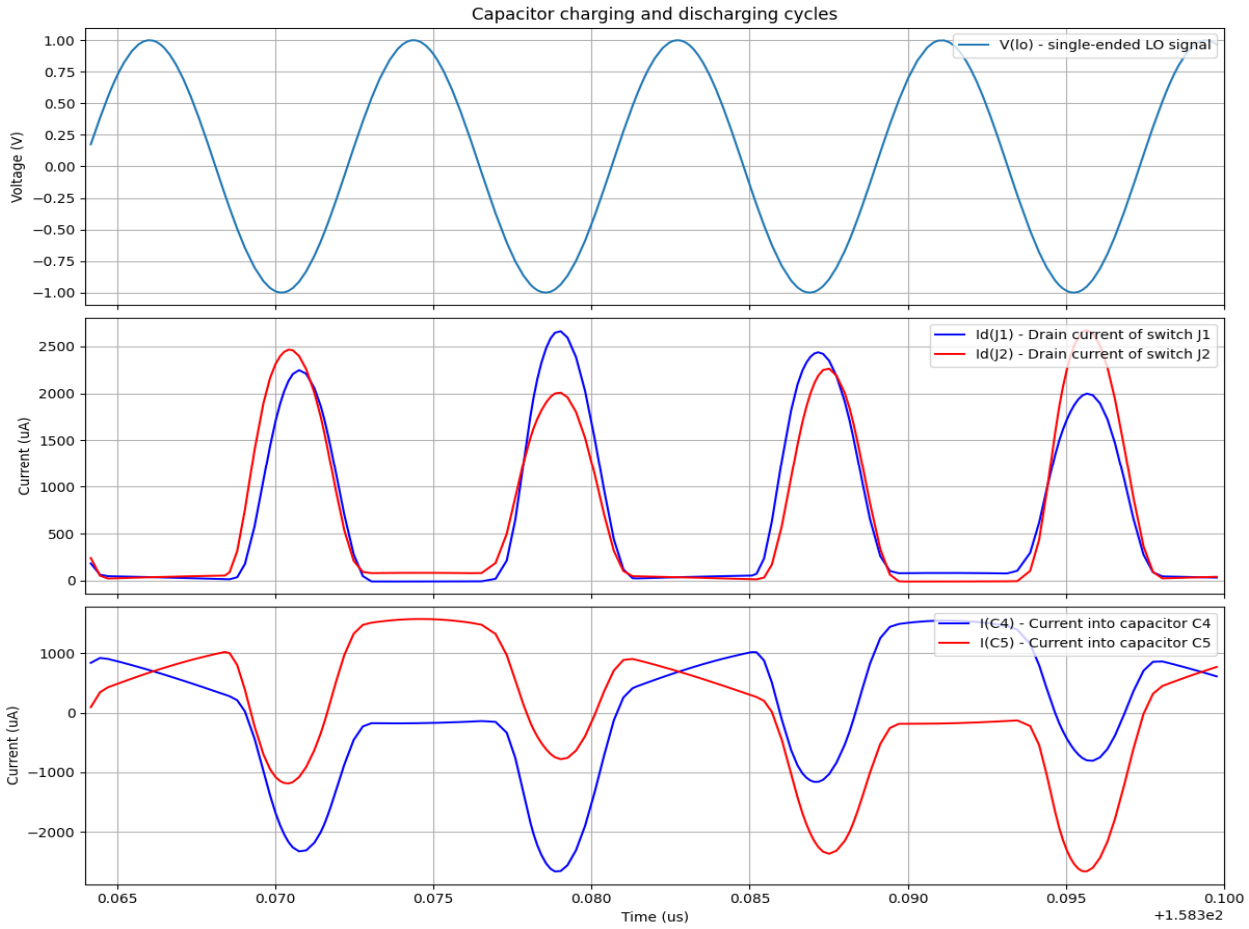
DEMAW-SIM-FIG. 1.11. DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 24 dB.

78. DEMAW-SIM-FIG. 4.11 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.11.



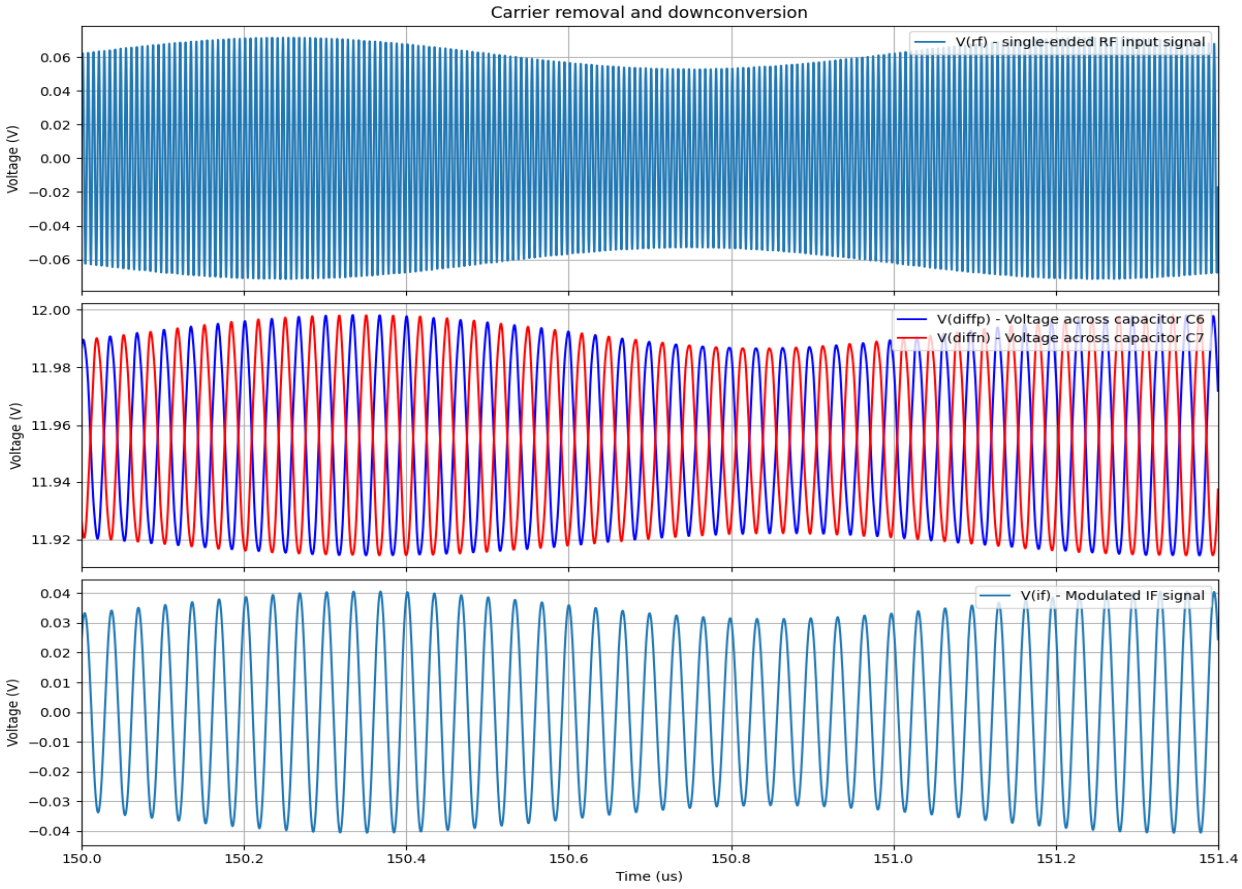
DEMAW-SIM-FIG. 4.11. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.11).

79. DEMAW-SIM-FIG. 5.11 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.11.



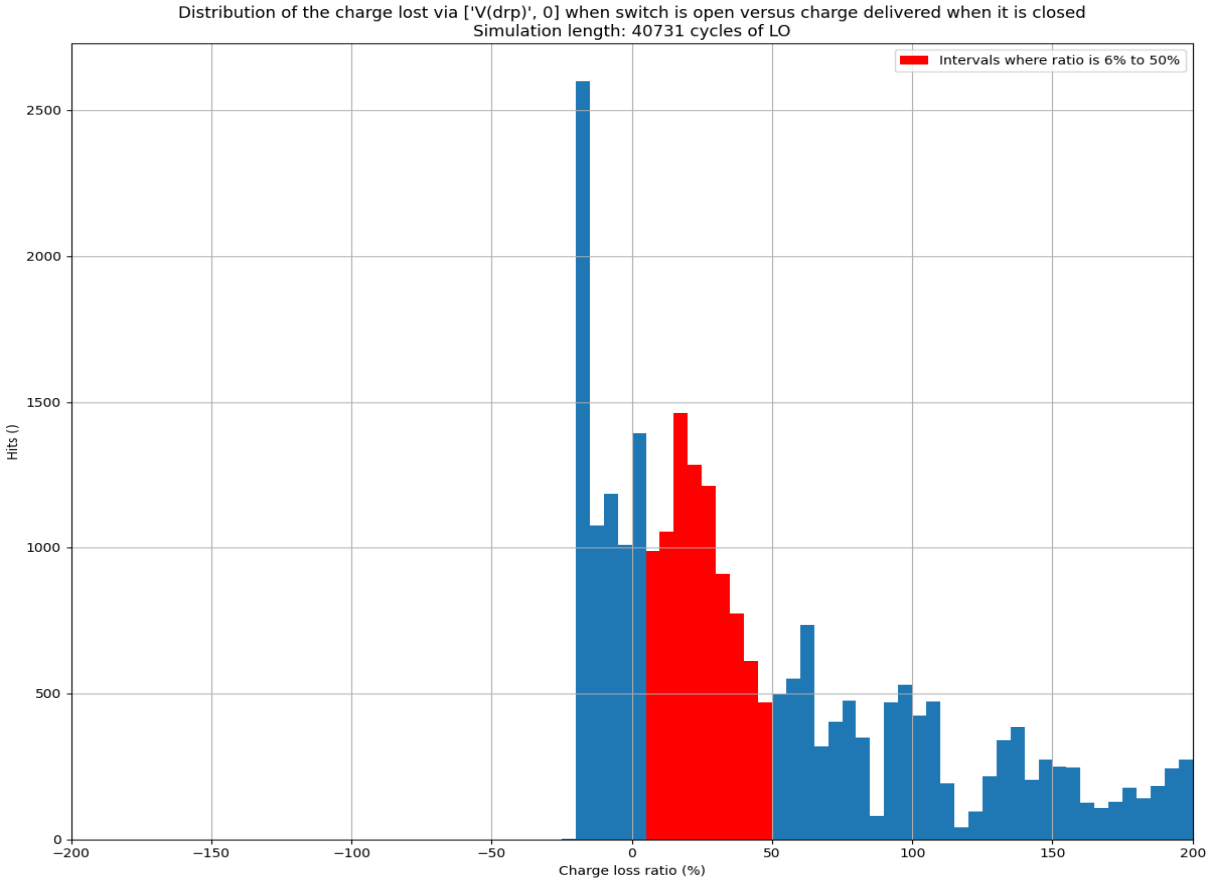
DEMAW-SIM-FIG. 5.11. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.11).

80. DEMAW-SIM-FIG. 6.11 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.11.



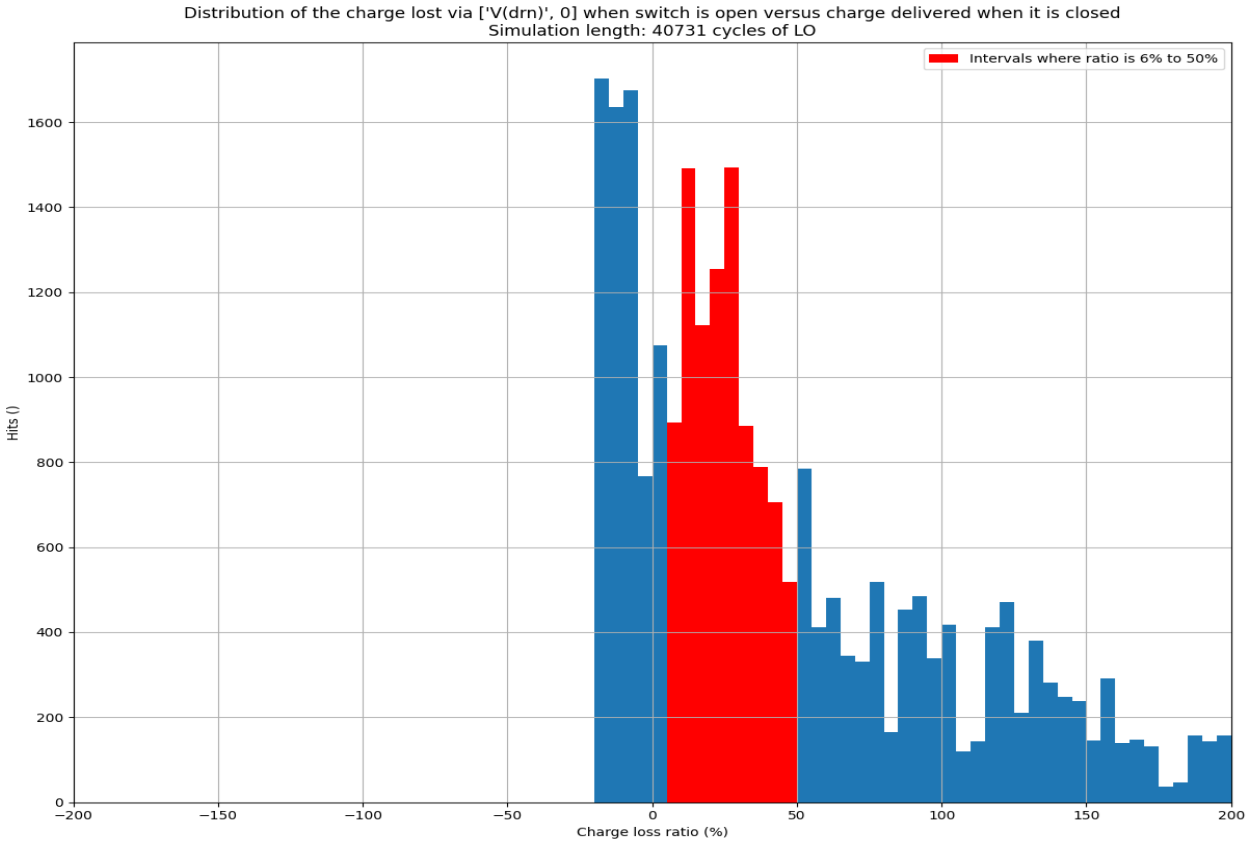
DEMAW-SIM-FIG. 6.11. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.11).

81. DEMAW-SIM-FIG. 7.11A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.11.



DEMAW-SIM-FIG. 7.11A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.11).

82. DEMAW-SIM-FIG. 7.11B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.11.



DEMAW-SIM-FIG. 7.11B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.11).

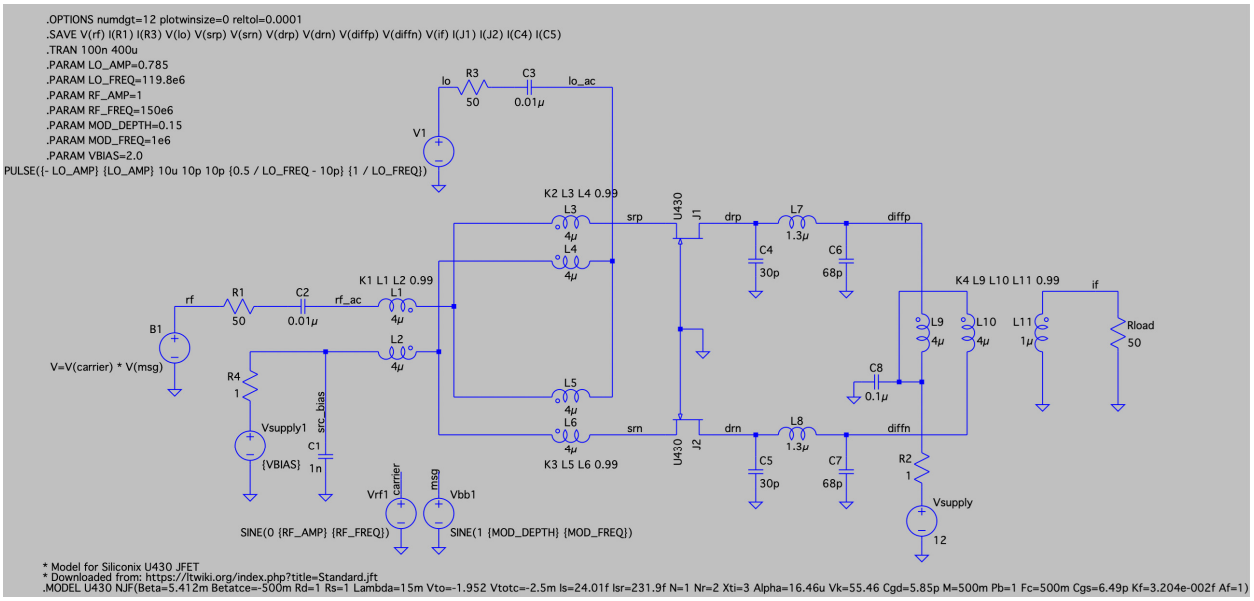
V. DeMaw Circuit Modified to Match Oxner With a Squared-Up LO

83. The DeMaw textbook references Siliconix Application Note AN72-1 written by E. Oxner that presents a circuit, denoted as the "Oxner circuit" herein. DeMaw states that the Oxner circuit is "similar" to that shown in FIG. 6.7 of DeMaw. The AN72-1 application note provides more detailed information about the Oxner circuit than DeMaw provides about the circuit shown in DeMaw FIG. 6.7. To further demonstrate that I have not chosen component values and circuit configurations to "get the results [that TI] needed" as alleged in the POPR, the simulation results

presented in this section correspond to the circuit with the component values and configuration described in the AN72-1 application note. Again, five sets of simulation results are presented which differ only in the power of the RF input to the mixer.

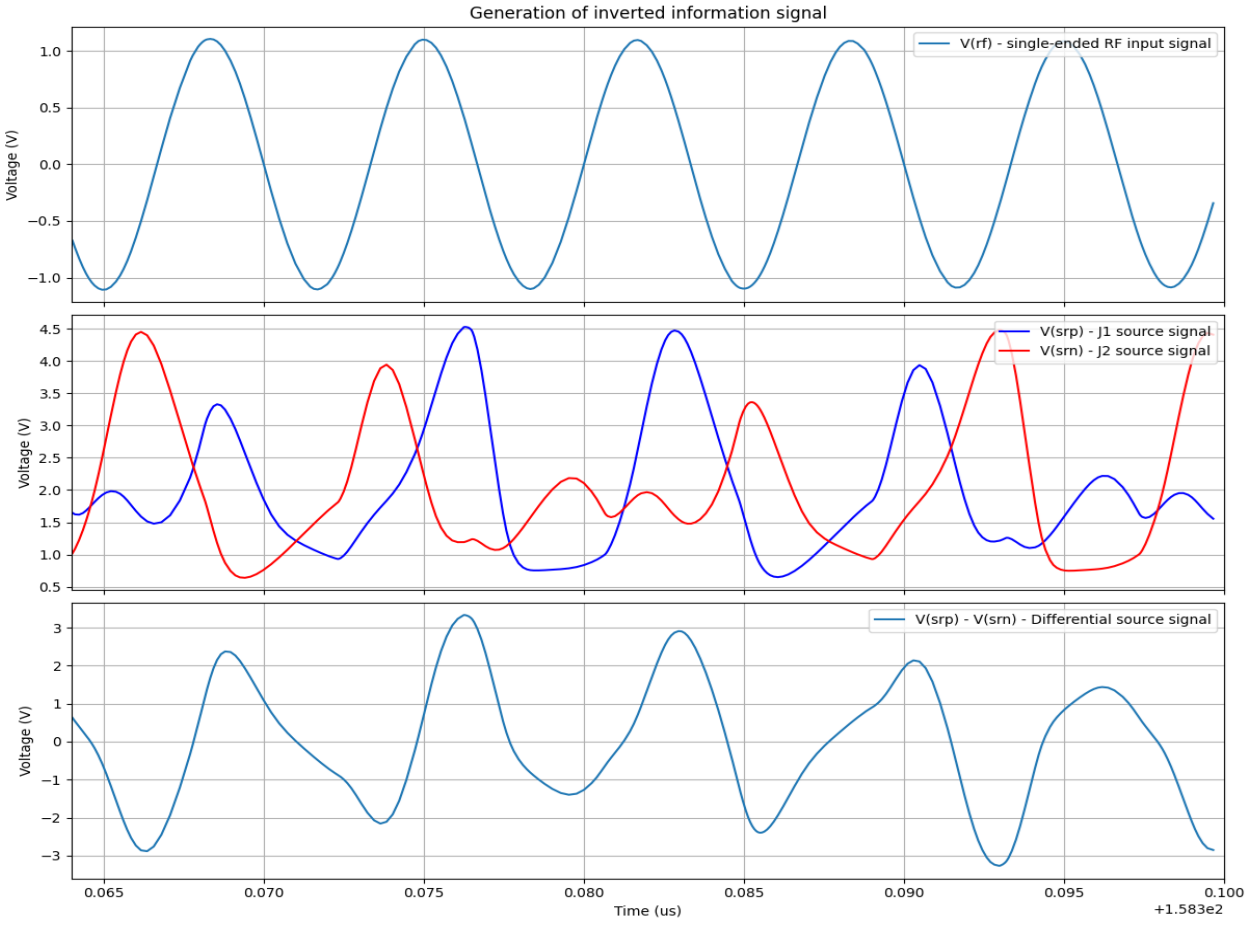
A. Simulation Results For a Large Input Signal

84. DEMAW-SIM-FIG. 1.12 is a schematic illustration of the simulated DeMaw FIG. 6.7 circuit modified Oxner with a squared-up LO and a large input signal. I have created additional figures DEMAW-SIM-FIGS. 4.12, 5.12, 6.12, 7.12A and 7.12B based on simulation output from DEMAW-SIM-FIG. 1.12. DEMAW-SIM-FIGS. 4.12, 5.12, 6.12, 7.12A and 7.12B show the same simulation output from DEMAW-SIM-FIG. 1.12 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.12, 4.12, 5.12, 6.12, 7.12A and 7.12B.



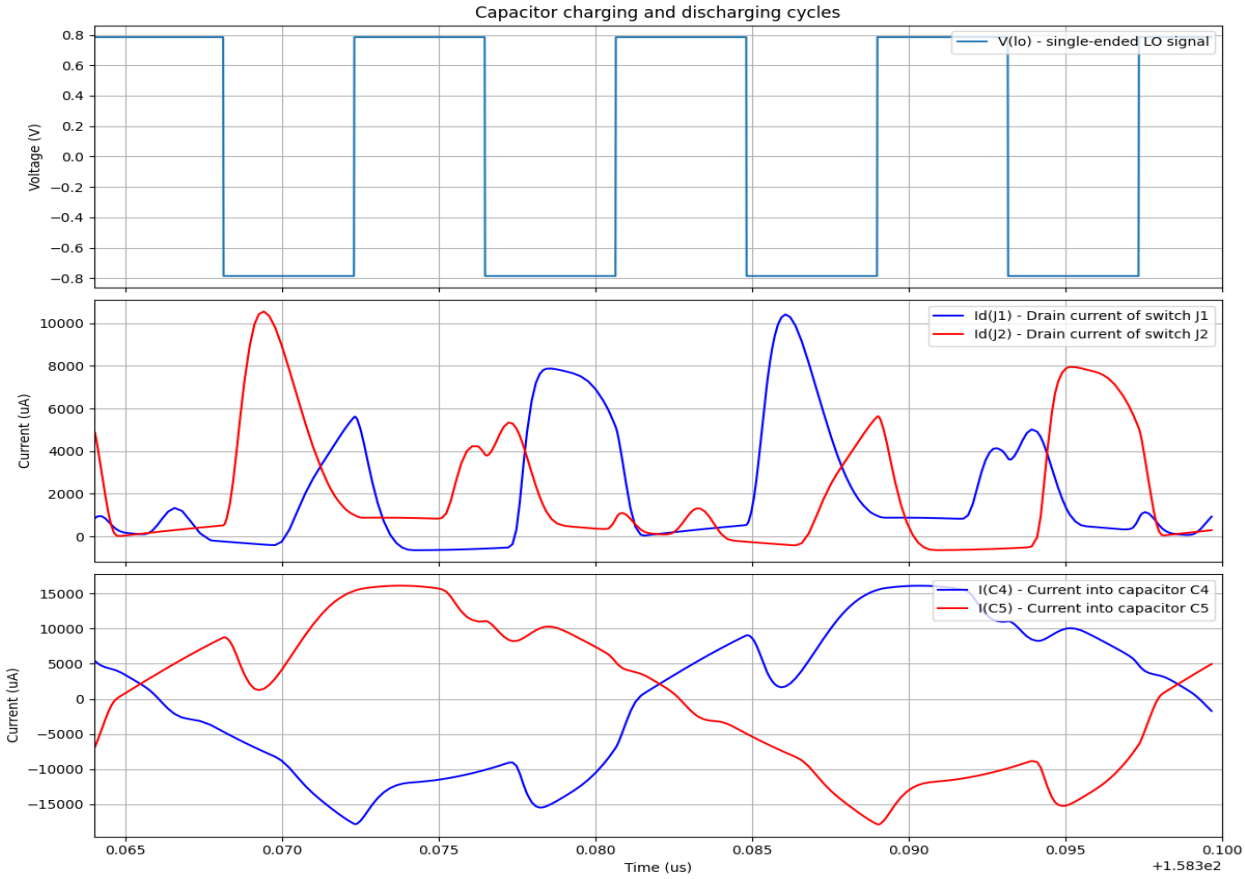
DEMAW-SIM-FIG. 1.12. DeMaw circuit modified to match Oxner with a squared-up LO and a large input signal.

85. DEMAW-SIM-FIG. 4.12 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.12.



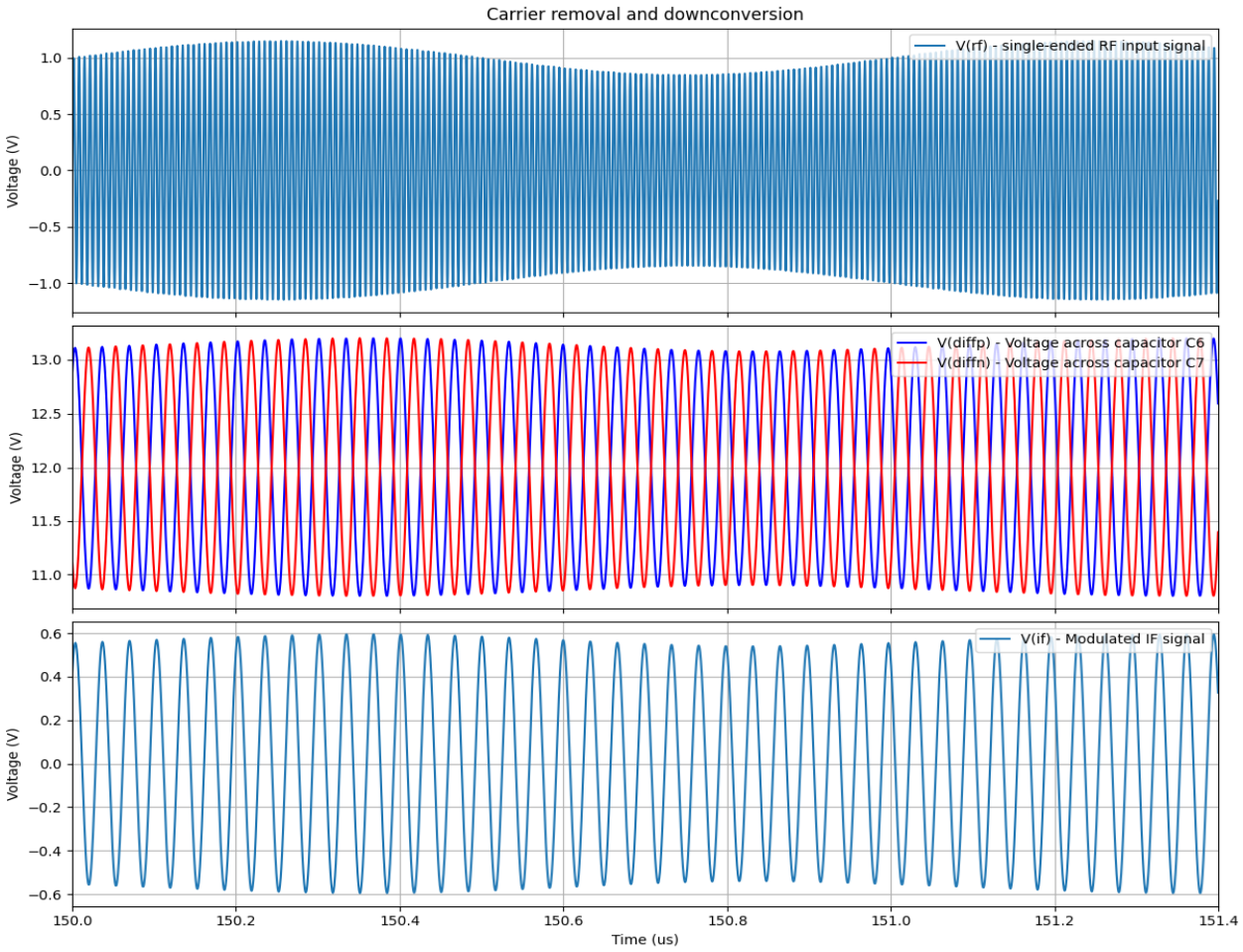
DEMAW-SIM-FIG. 4.12. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.12).

86. DEMAW-SIM-FIG. 5.12 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.12.



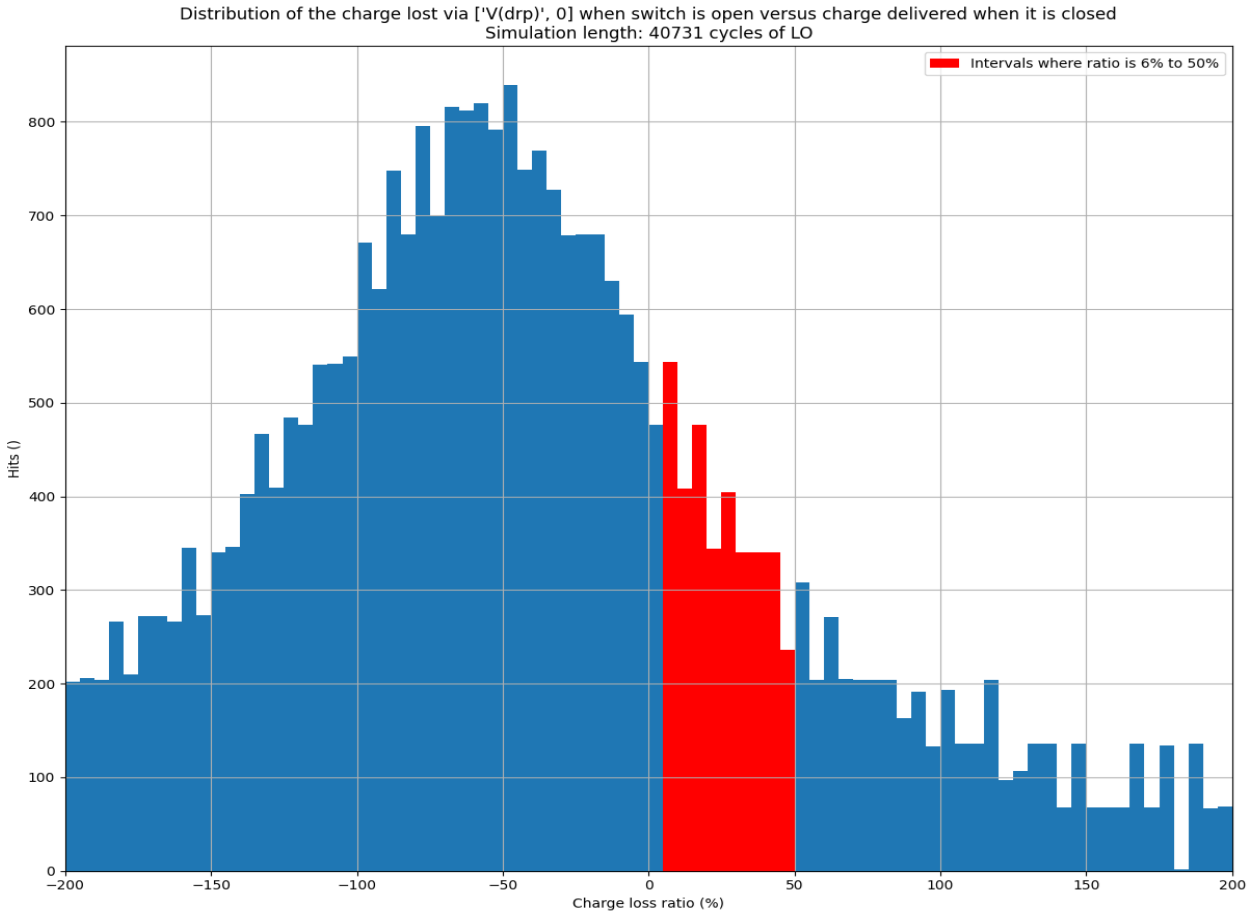
DEMAW-SIM-FIG. 5.12. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.12).

87. DEMAW-SIM-FIG. 6.12 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.12.



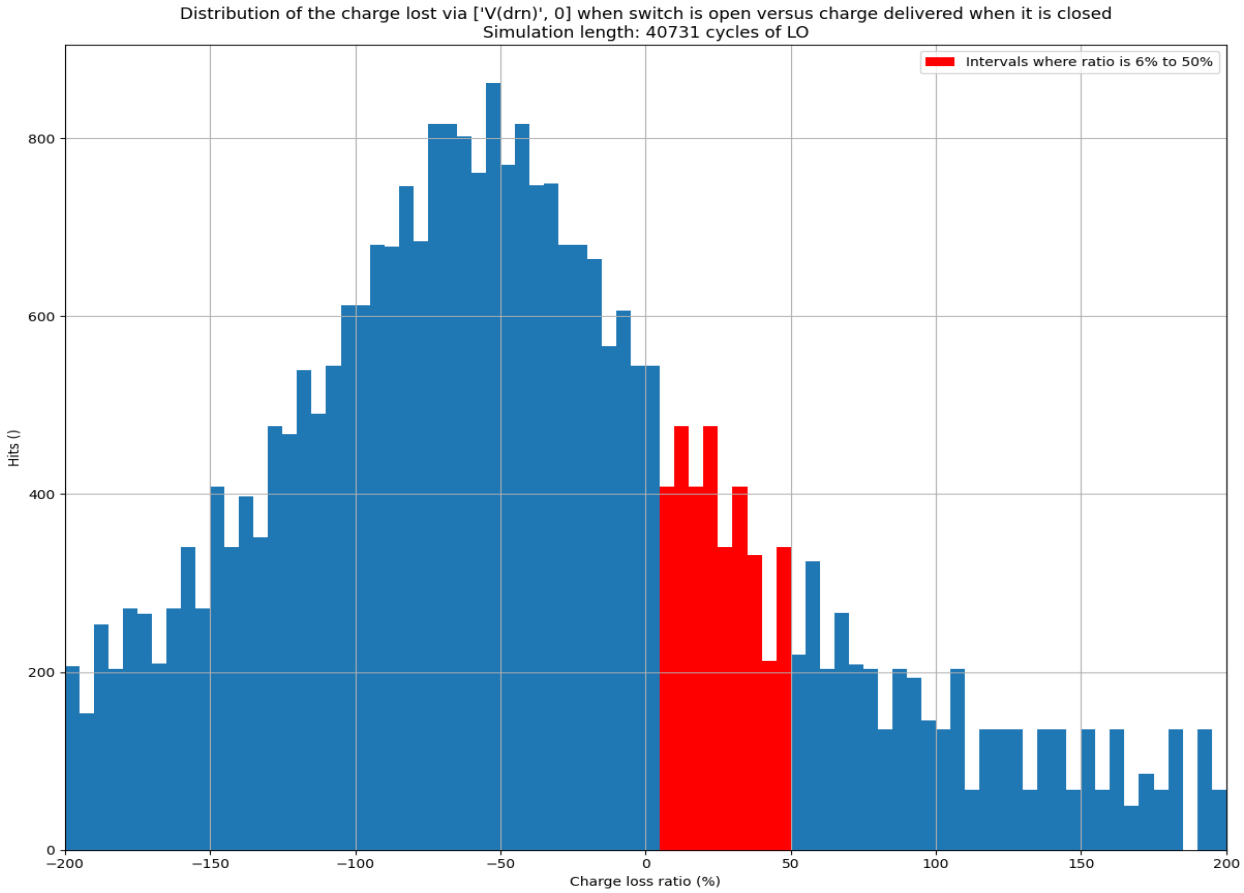
DEMAW-SIM-FIG. 6.12. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.12).

88. DEMAW-SIM-FIG. 7.12A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.12.



DEMAW-SIM-FIG. 7.12A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.12).

89. DEMAW-SIM-FIG. 7.12B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.12.

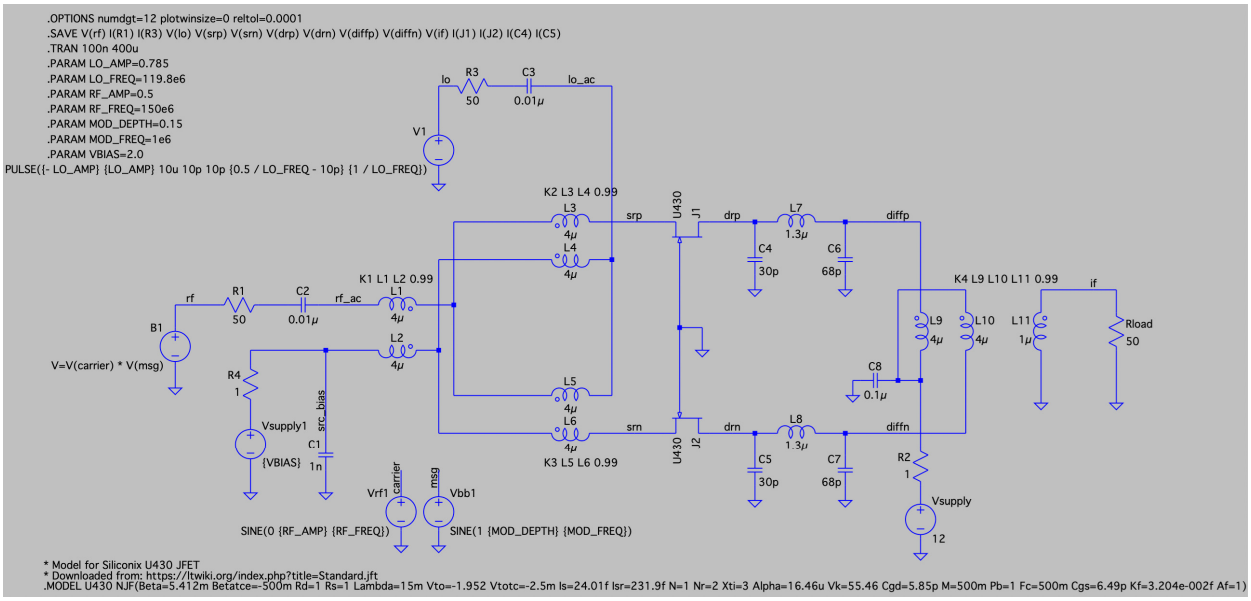


DEMAW-SIM-FIG. 7.12B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.12).

B. Simulation Results For an Input Signal Reduced by 6 dB

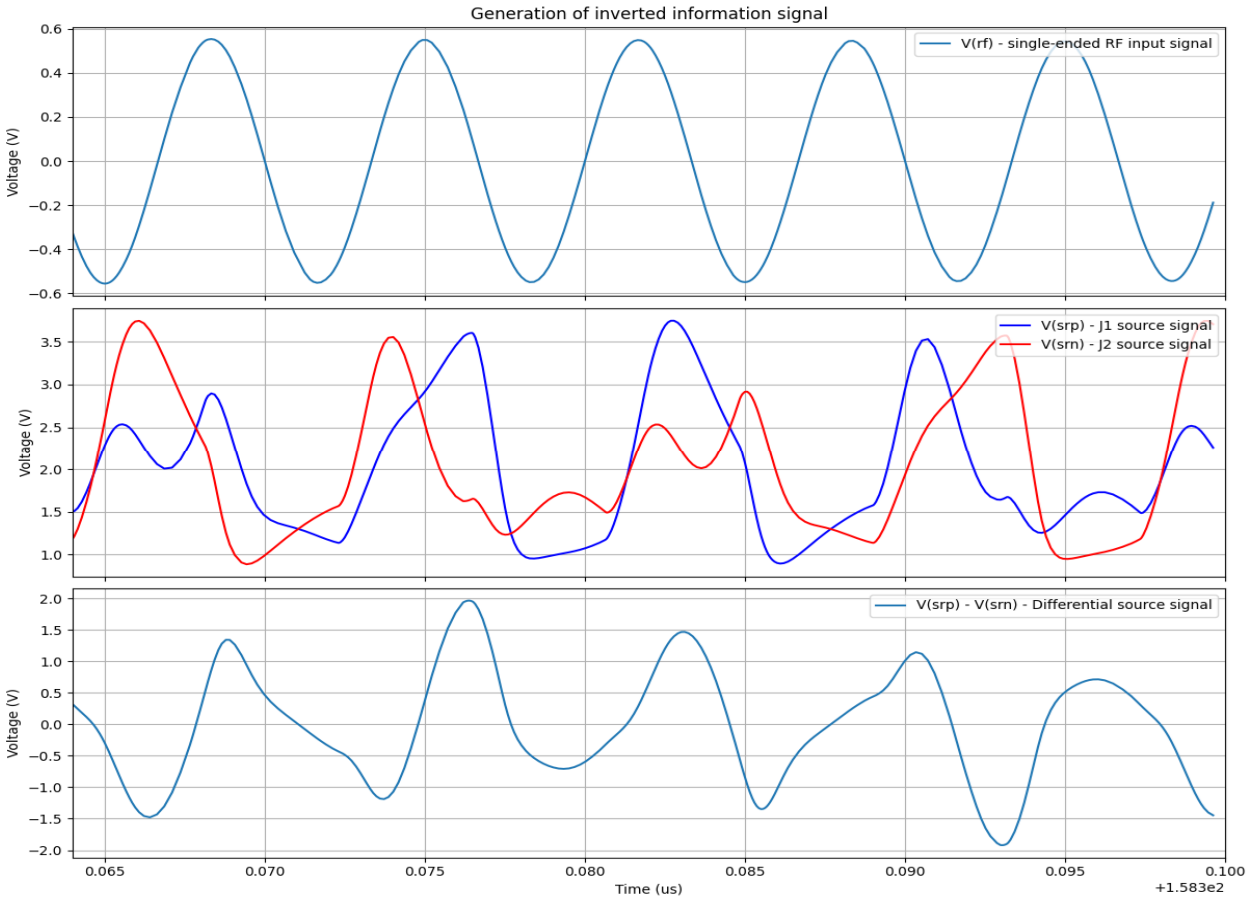
90. DEMAW-SIM-FIG. 1.13. DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 6 dB. I have created additional figures DEMAW-SIM-FIGS. 4.13, 5.13, 6.13, 7.13A and 7.13B based on simulation output from DEMAW-SIM-FIG. 1.13. DEMAW-SIM-FIGS. 4.13, 5.13, 6.13, 7.13A and 7.13B show the same simulation output from DEMAW-SIM-FIG. 1.13 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-

SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.13, 4.13, 5.13, 6.13, 7.13A and 7.13B.



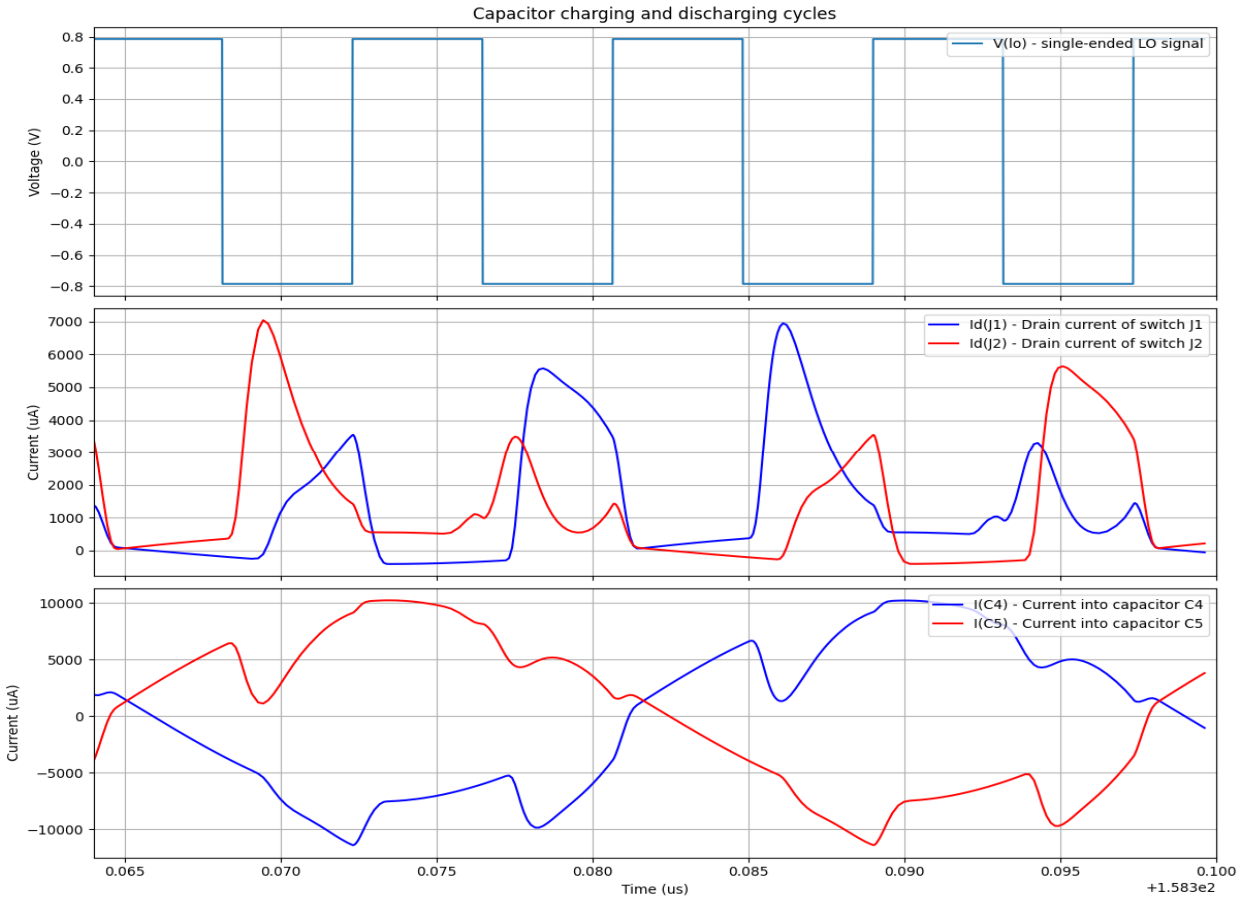
DEMAW-SIM-FIG. 1.13. DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 6 dB.

91. DEMAW-SIM-FIG. 4.13 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.13.



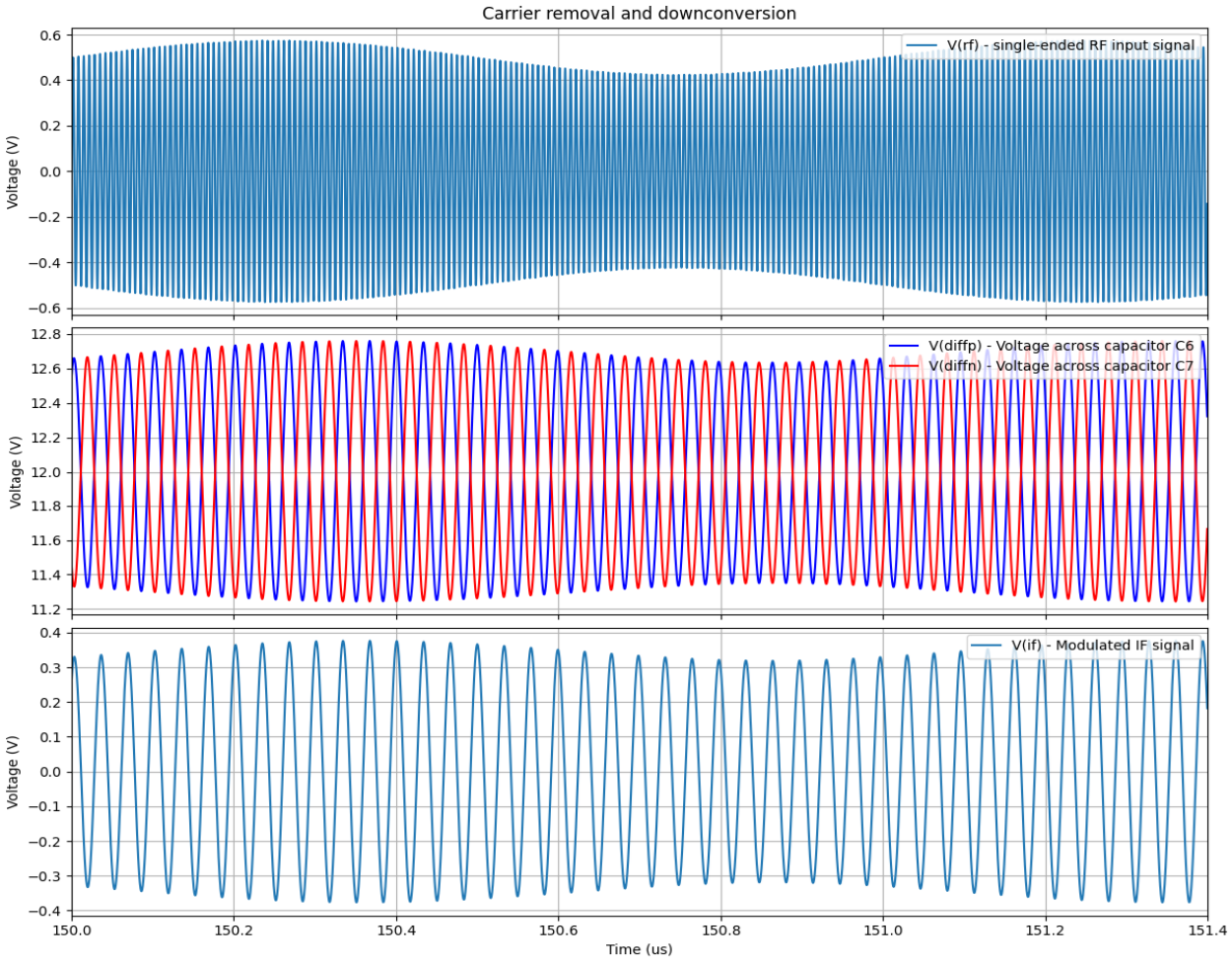
DEMAW-SIM-FIG. 4.13. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.13).

92. DEMAW-SIM-FIG. 5.13 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.13.



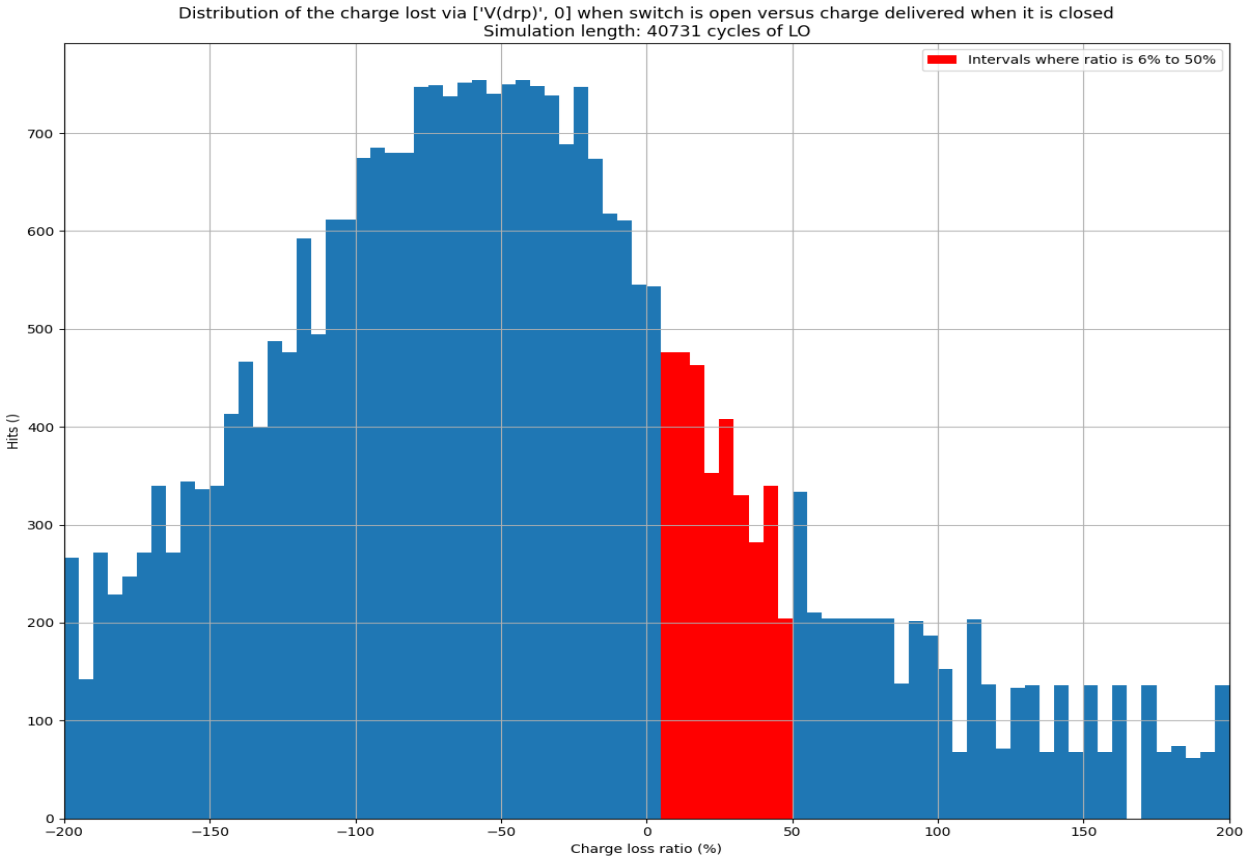
DEMAW-SIM-FIG. 5.13. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.13).

93. DEMAW-SIM-FIG. 6.13 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.13.



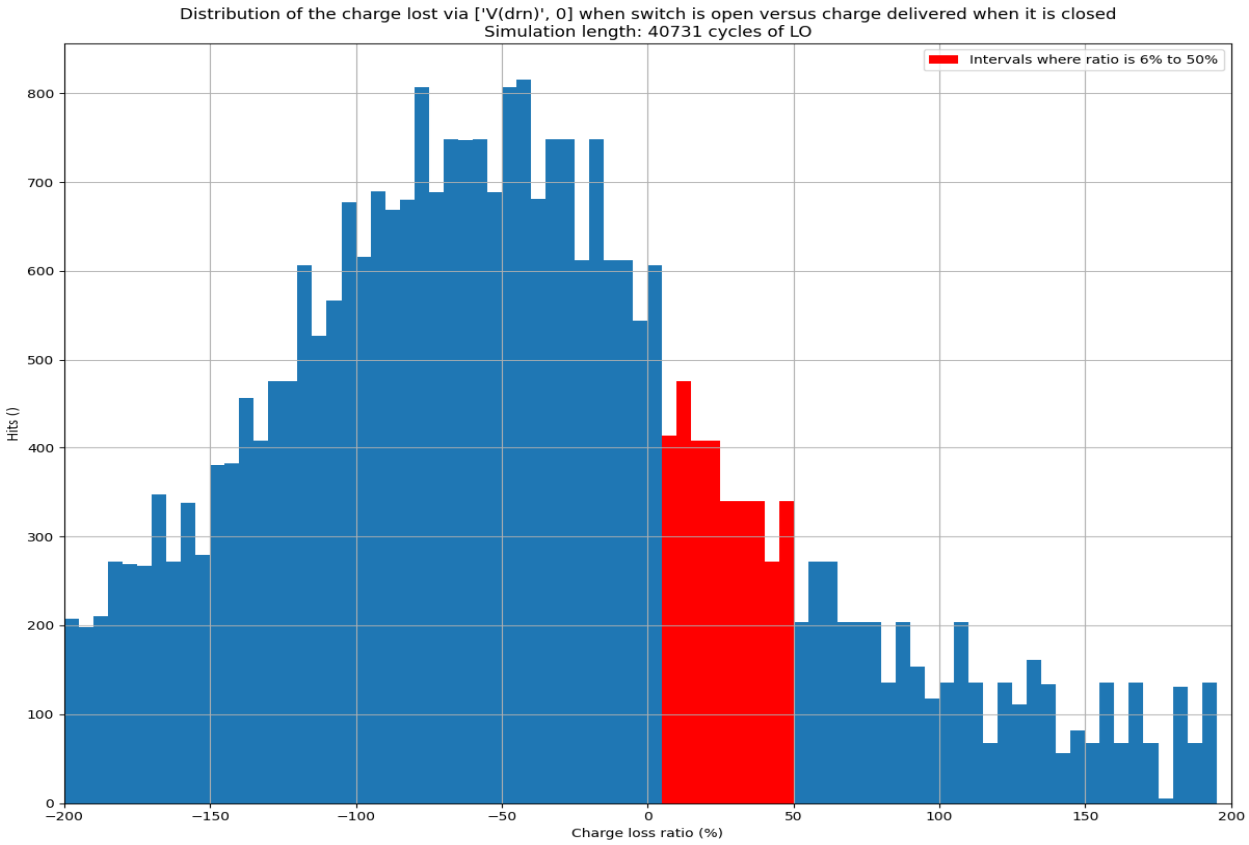
DEMAW-SIM-FIG. 6.13. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.13).

94. DEMAW-SIM-FIG. 7.13A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.13.



DEMAW-SIM-FIG. 7.13A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.13).

95. DEMAW-SIM-FIG. 7.13B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.13.

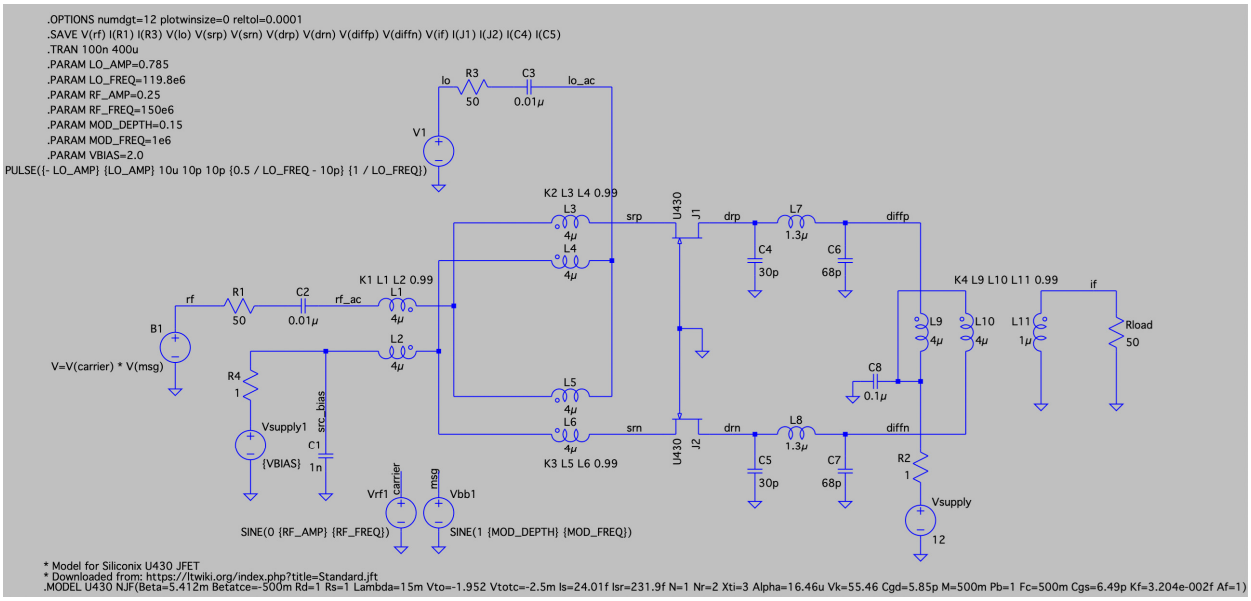


DEMAW-SIM-FIG. 7.13B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.13).

C. Simulation Results For an Input Signal Reduced by 12 dB

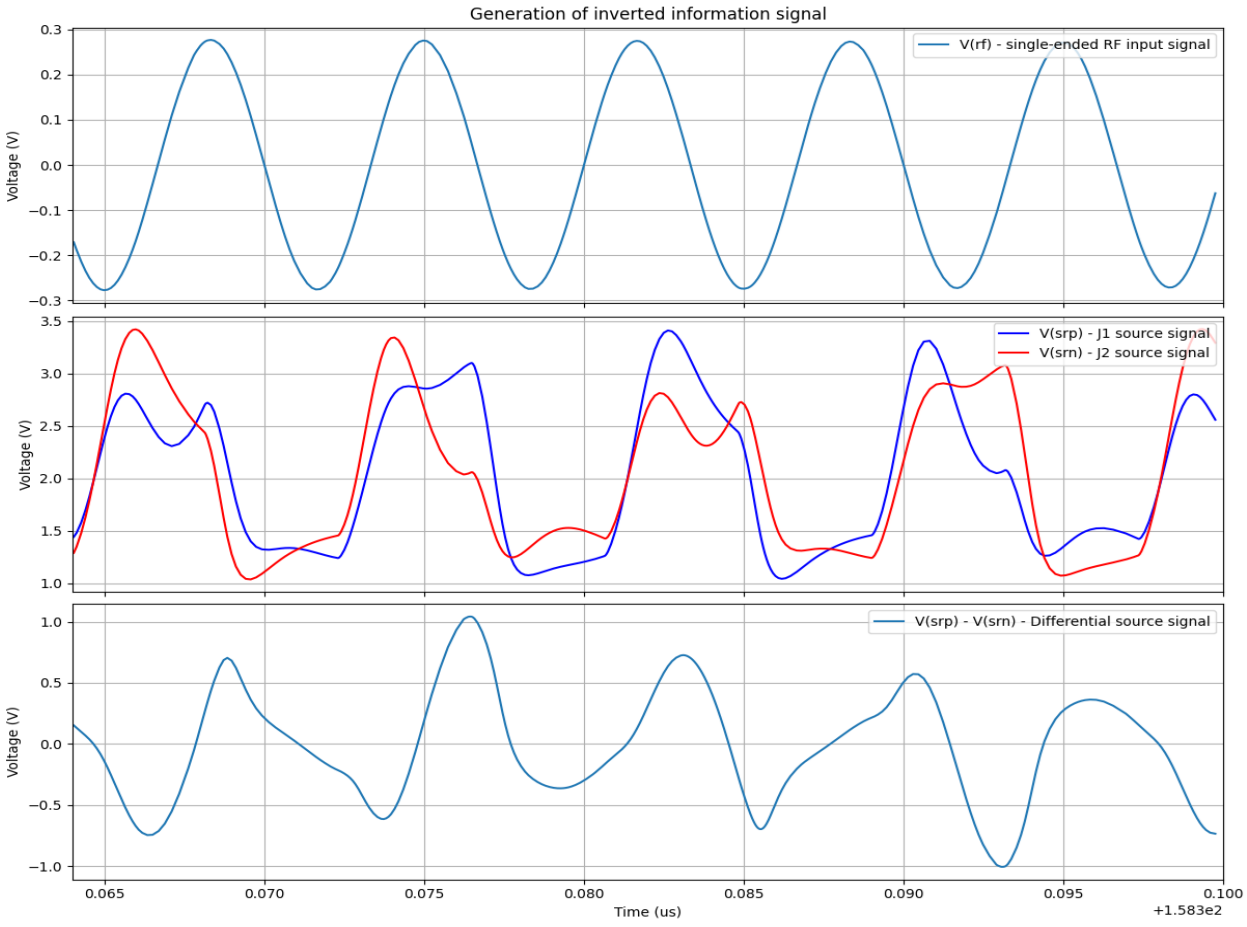
96. DEMAW-SIM-FIG. 1.14 is a schematic diagram of the simulated DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 12 dB. I have created additional figures DEMAW-SIM-FIGS. 4.14, 5.14, 6.14, 7.14A and 7.14B based on simulation output from DEMAW-SIM-FIG. 1.14. DEMAW-SIM-FIGS. 4.14, 5.14, 6.14, 7.14A and 7.14B show the same simulation output from DEMAW-SIM-FIG. 1.14 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding

the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.14, 4.14, 5.14, 6.14, 7.14A and 7.14B.



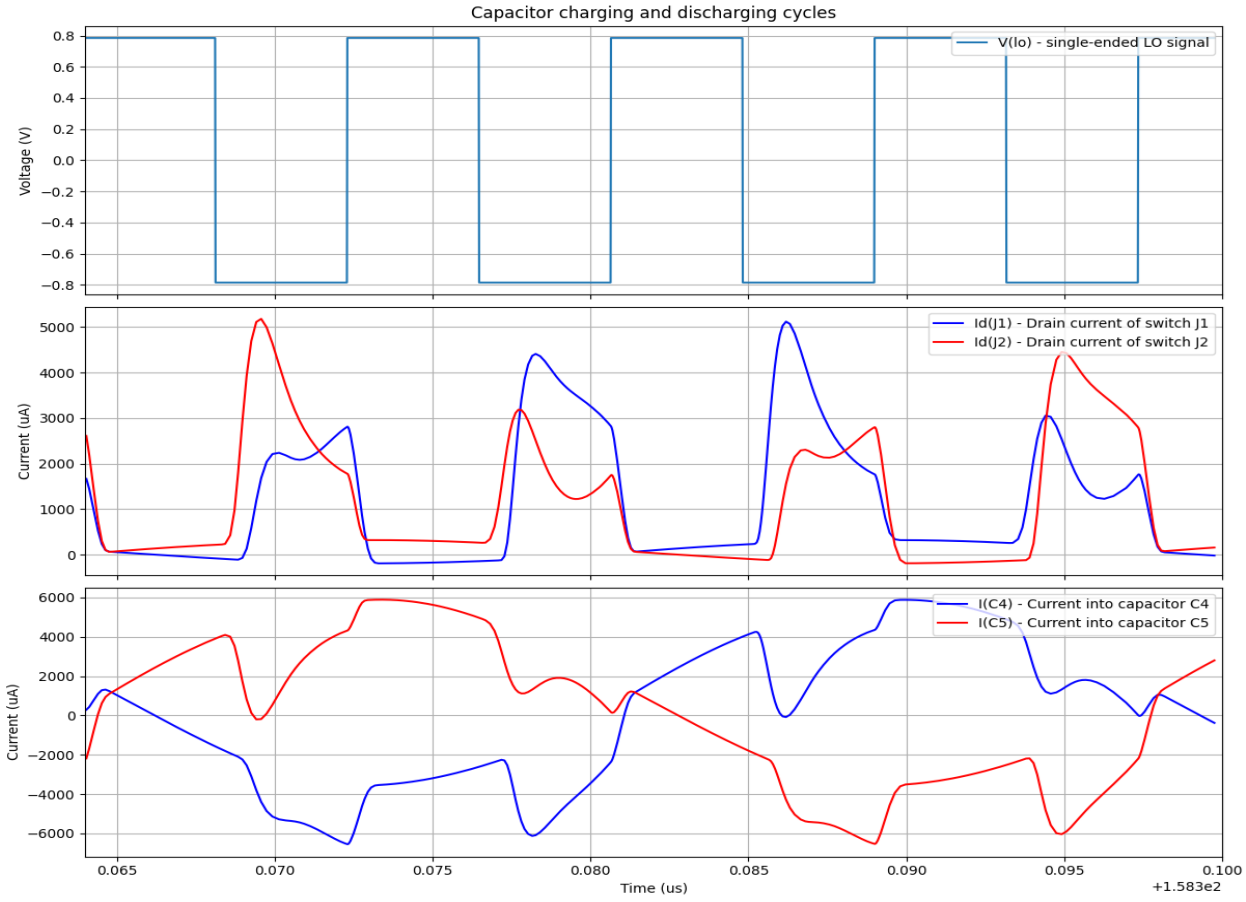
DEMAW-SIM-FIG. 1.14. DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 12 dB.

97. DEMAW-SIM-FIG. 4.14 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.14.



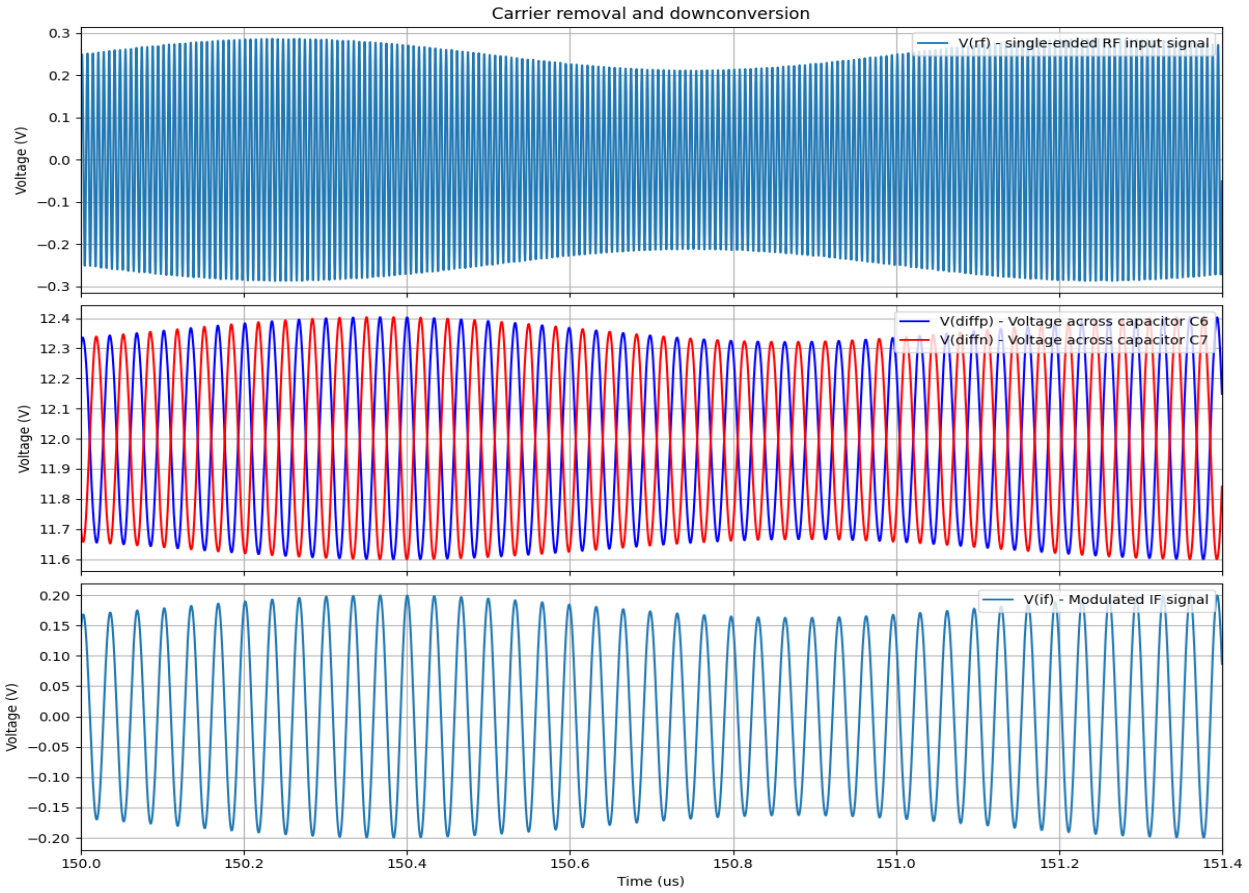
DEMAW-SIM-FIG. 4.14. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.14).

98. DEMAW-SIM-FIG. 5.14 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.14.



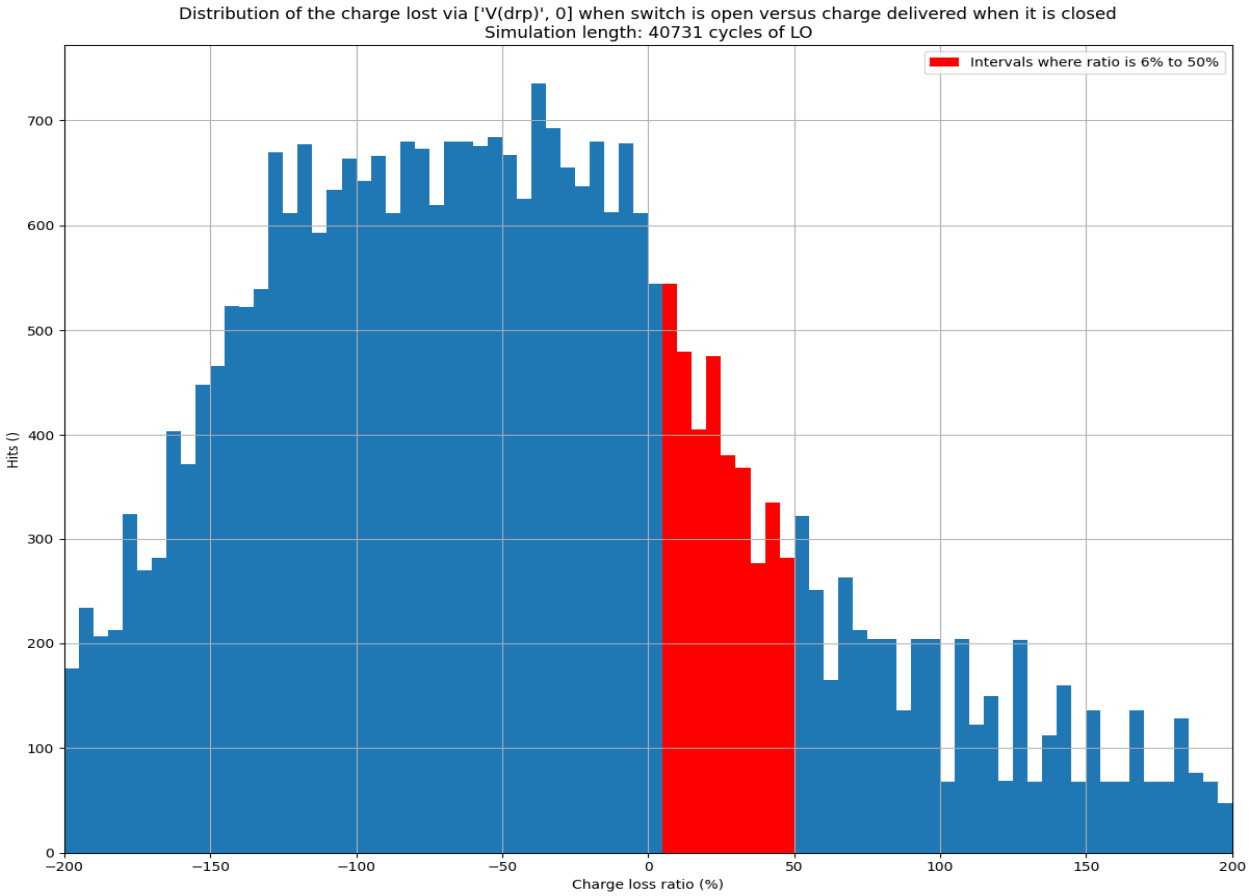
DEMAW-SIM-FIG. 5.14. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.14).

99. DEMAW-SIM-FIG. 6.14 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.14.



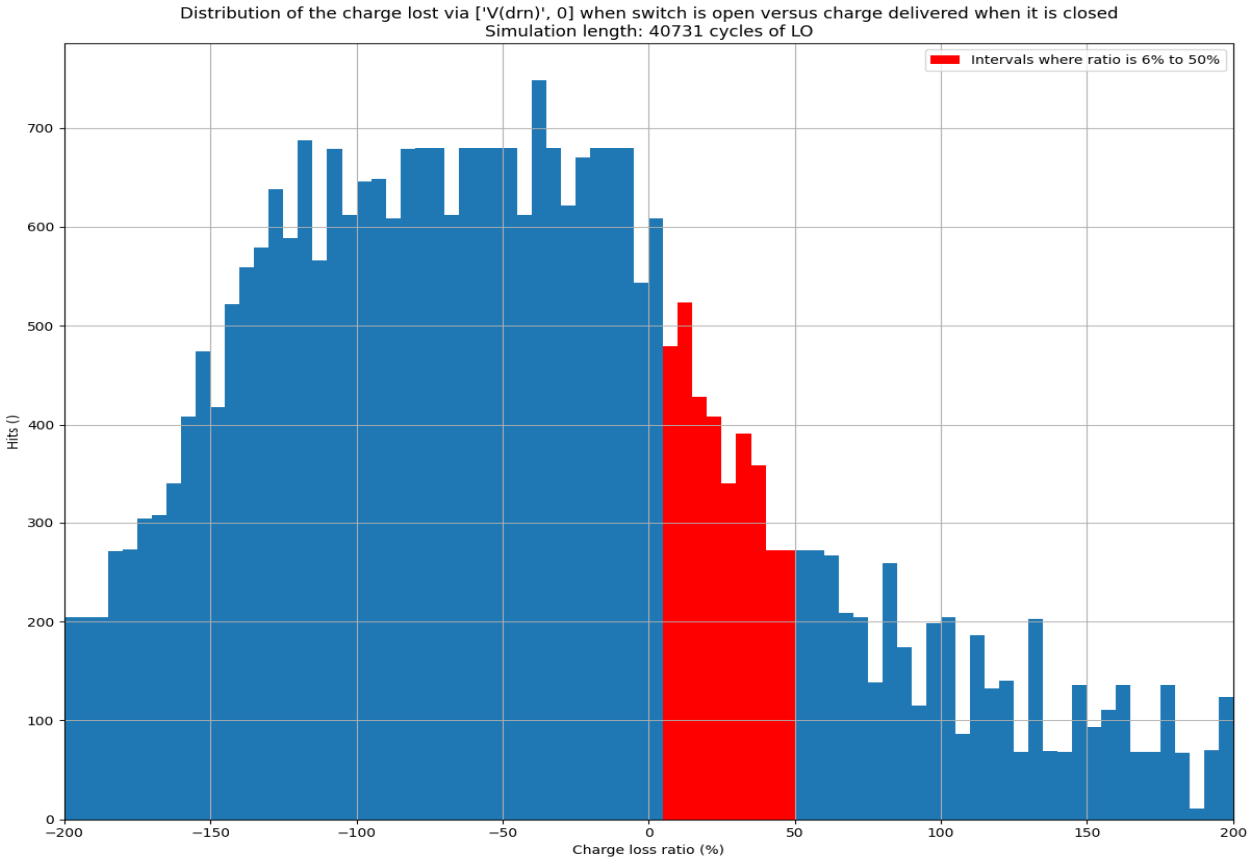
DEMAW-SIM-FIG. 6.14. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.14).

100. DEMAW-SIM-FIG. 7.14A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.14.



DEMAW-SIM-FIG. 7.14A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.14).

101. DEMAW-SIM-FIG. 7.14B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.14.

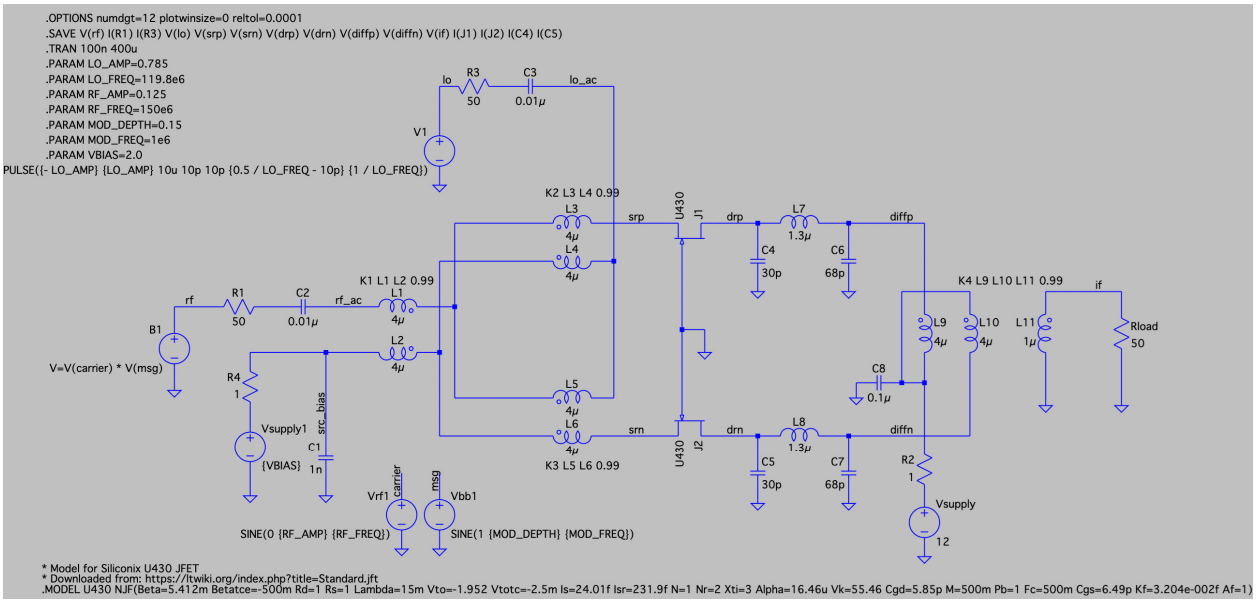


DEMAW-SIM-FIG. 7.14B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.14).

D. Simulation Results For an Input Signal Reduced by 18 dB

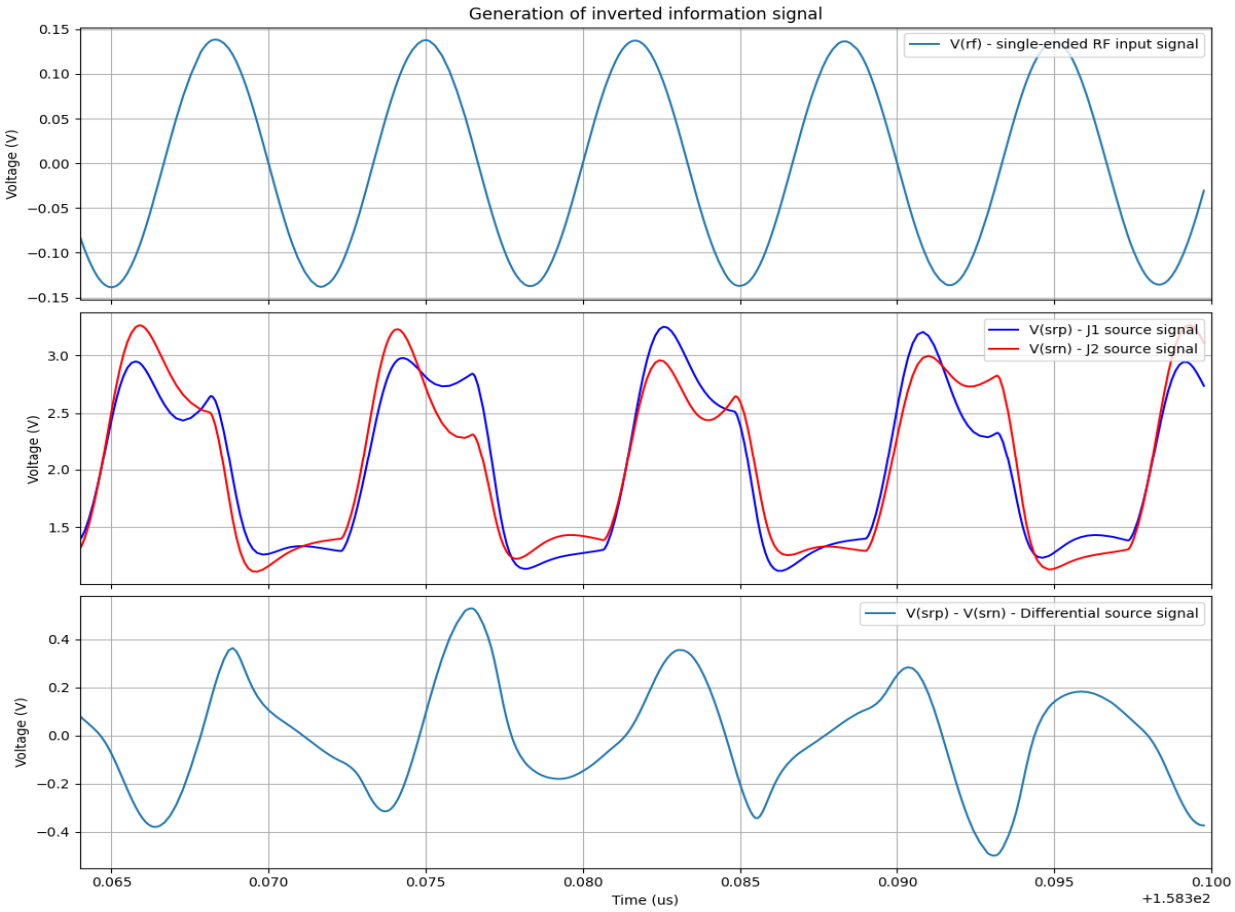
102. DEMAW-SIM-FIG. 1.15 is a schematic diagram of the simulated DeMaw FIG. 6.7 circuit modified to match Oxner with a squared-up LO and input signal reduced by 18 dB. I have created additional figures DEMAW-SIM-FIGS. 4.15, 5.15, 6.15, 7.15A and 7.15B based on simulation output from DEMAW-SIM-FIG. 1.15. DEMAW-SIM-FIGS. 4.15, 5.15, 6.15, 7.15A and 7.15B show the same simulation output from DEMAW-SIM-FIG. 1.15 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.15, 4.15, 5.15, 6.15, 7.15A and 7.15B.



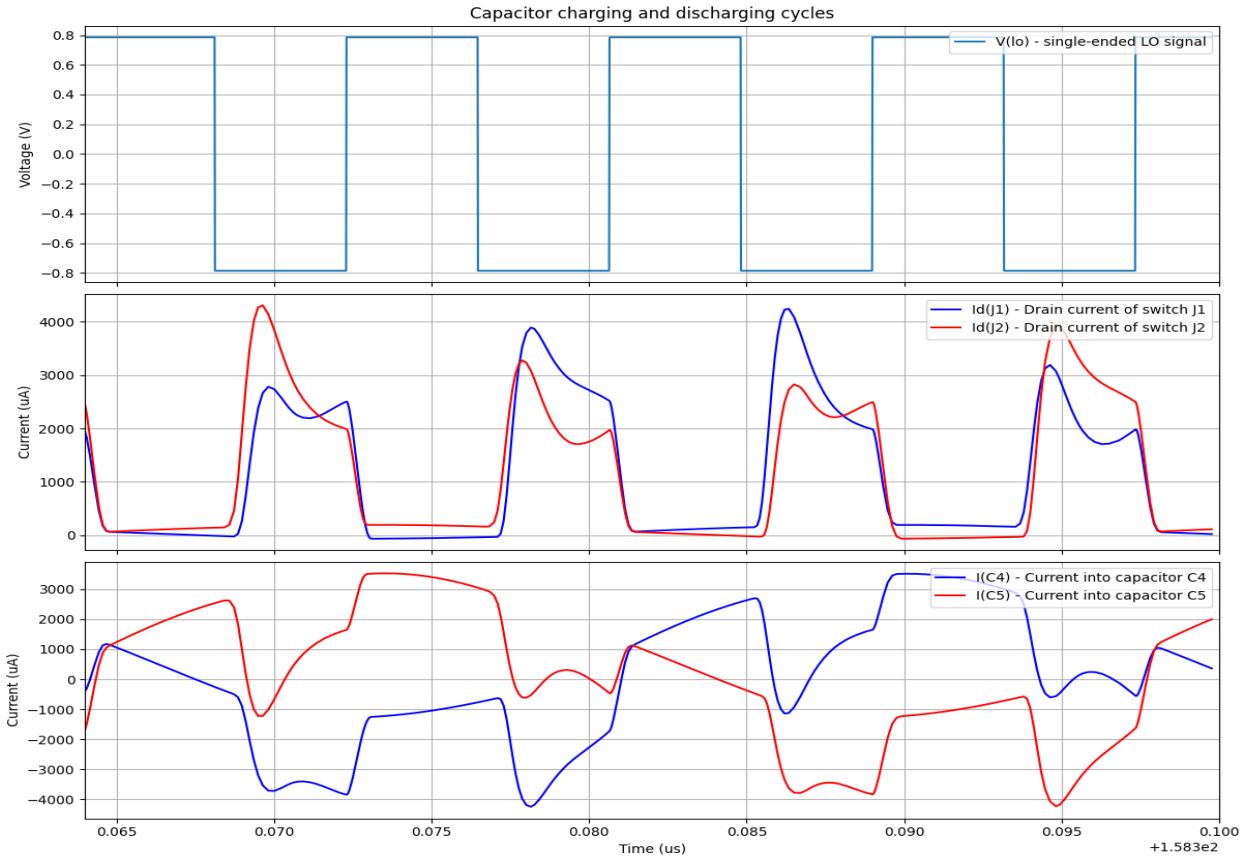
DEMAW-SIM-FIG. 1.15. DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 18 dB.

103. DEMAW-SIM-FIG. 4.15 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.15.



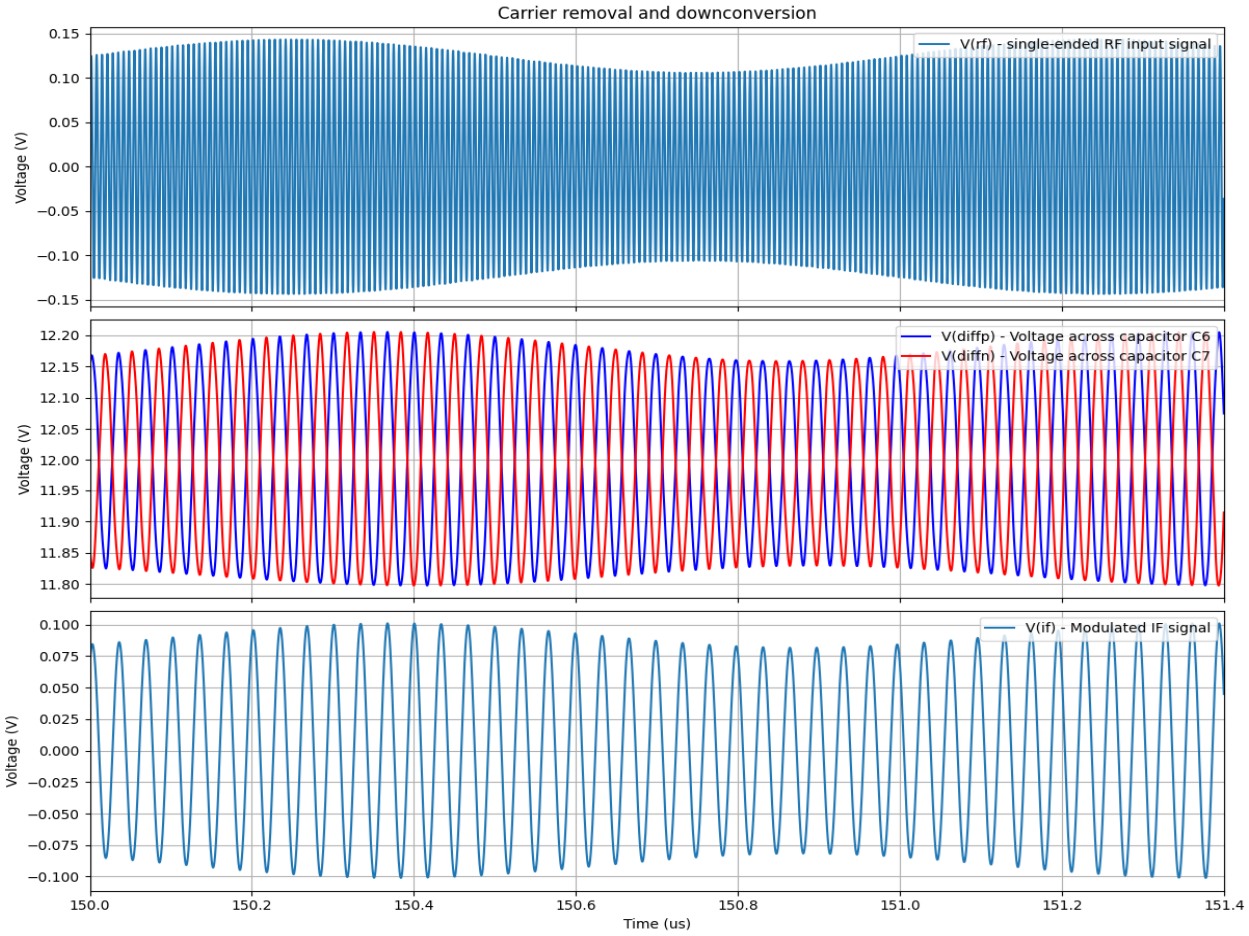
DEMAW-SIM-FIG. 4.15. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.15).

104. DEMAW-SIM-FIG. 5.15 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.15.



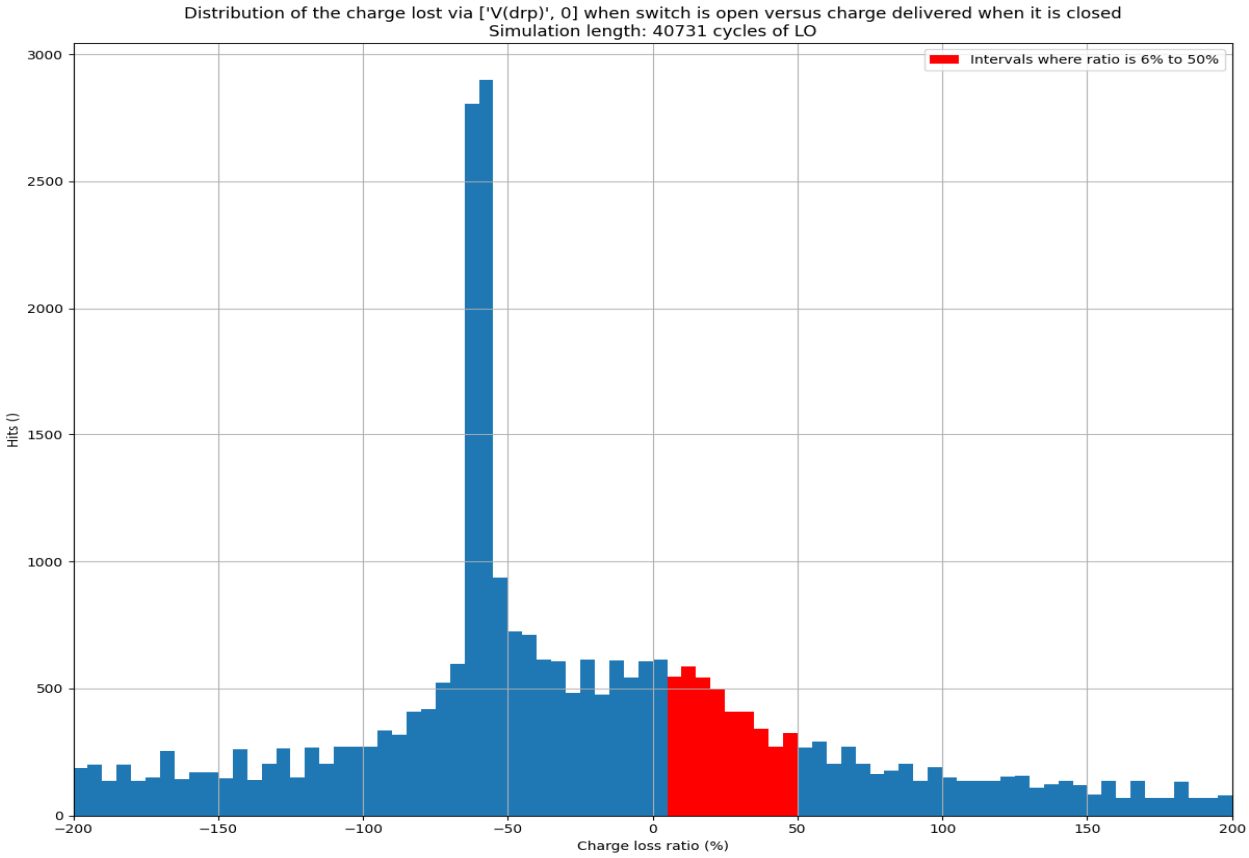
DEMAW-SIM-FIG. 5.15. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.15).

105. DEMAW-SIM-FIG. 6.15 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.15.



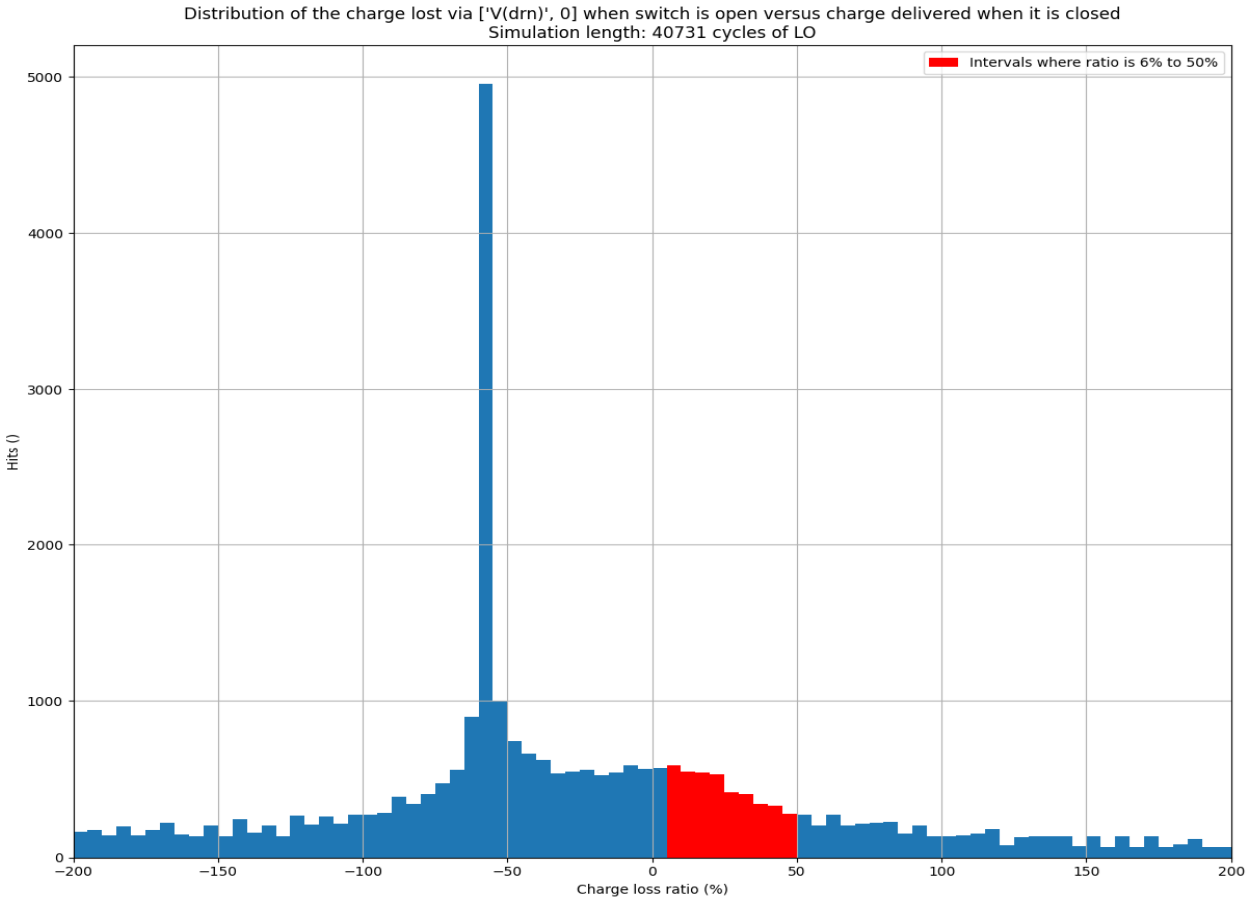
DEMAW-SIM-FIG. 6.15. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.15).

106. DEMAW-SIM-FIG. 7.15A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.15.



DEMAW-SIM-FIG. 7.15A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.15).

107. DEMAW-SIM-FIG. 7.15B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.15.

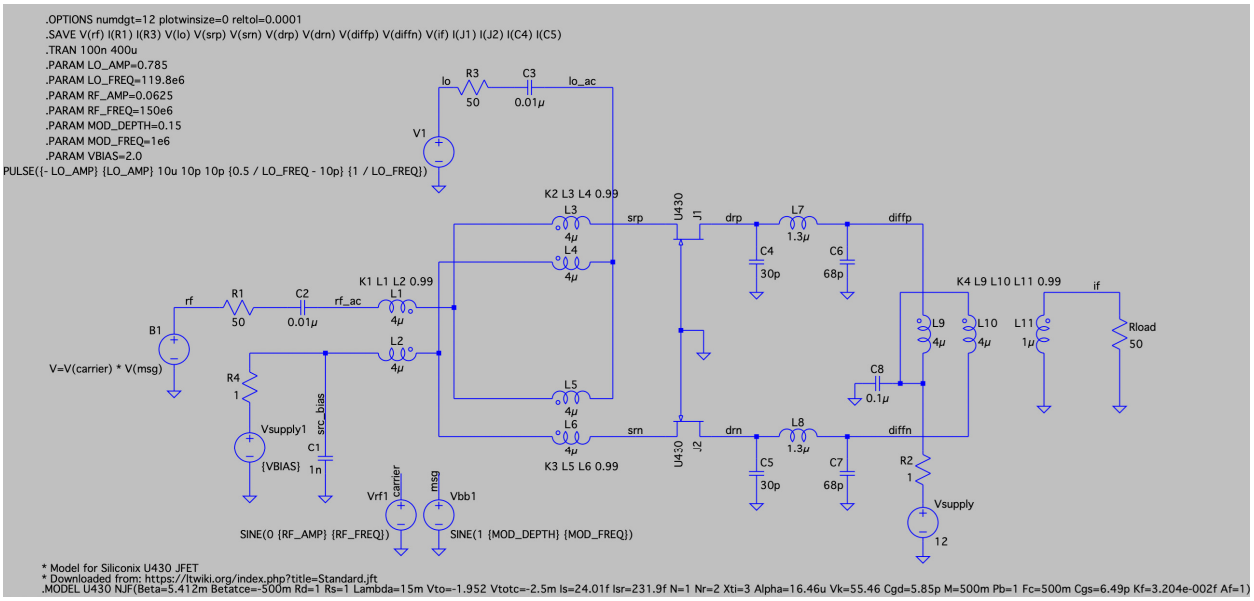


DEMAW-SIM-FIG. 7.15B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.15).

E. Simulation Results For an Input Signal Reduced by 24 dB

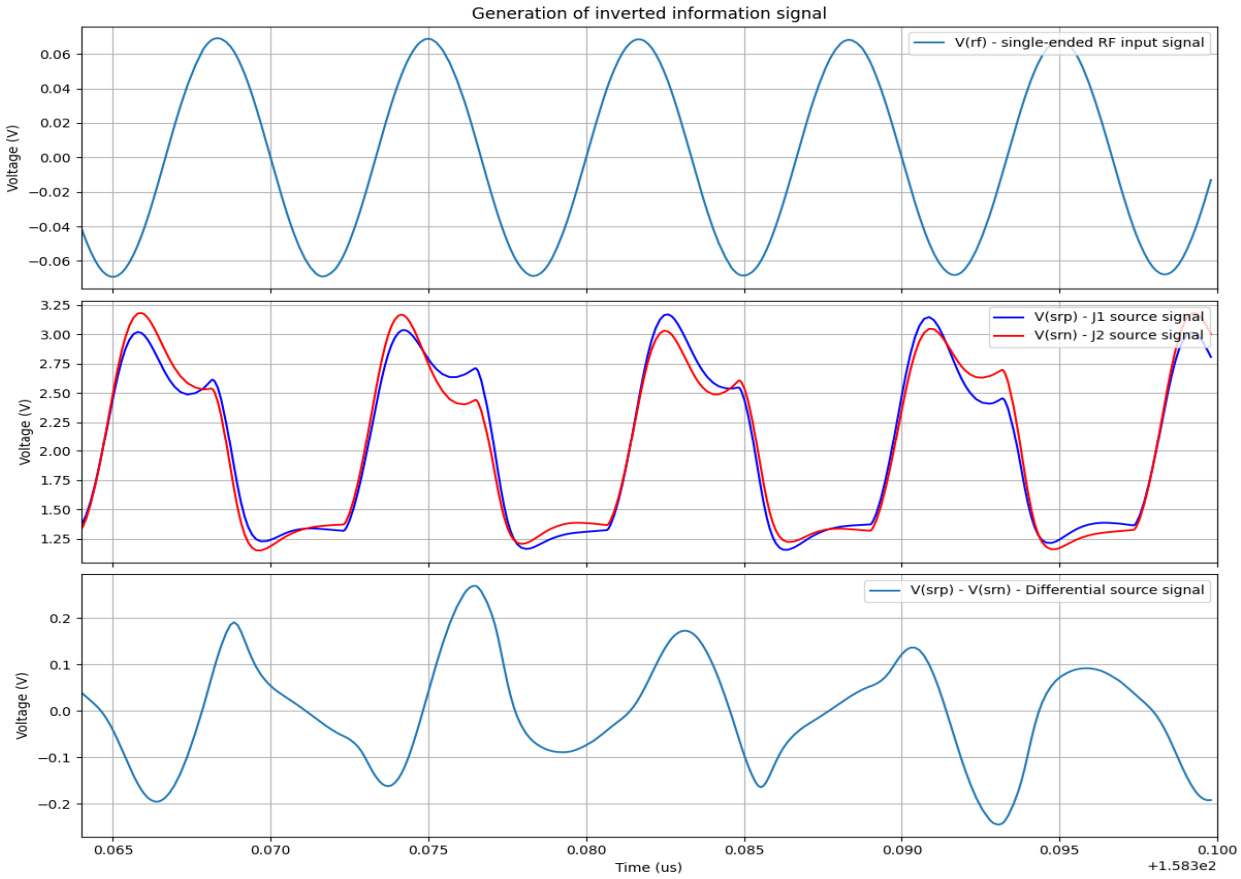
108. DEMAW-SIM-FIG. 1.16 is a schematic diagram of the simulated DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 24 dB. I have created additional figures DEMAW-SIM-FIGS. 4.16, 5.16, 6.16, 7.16A and 7.16B based on simulation output from DEMAW-SIM-FIG. 1.16. DEMAW-SIM-FIGS. 4.16, 5.16, 6.16, 7.16A and 7.16B show the same simulation output from DEMAW-SIM-FIG. 1.16 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show

from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.16, 4.16, 5.16, 6.16, 7.16A and 7.16B.



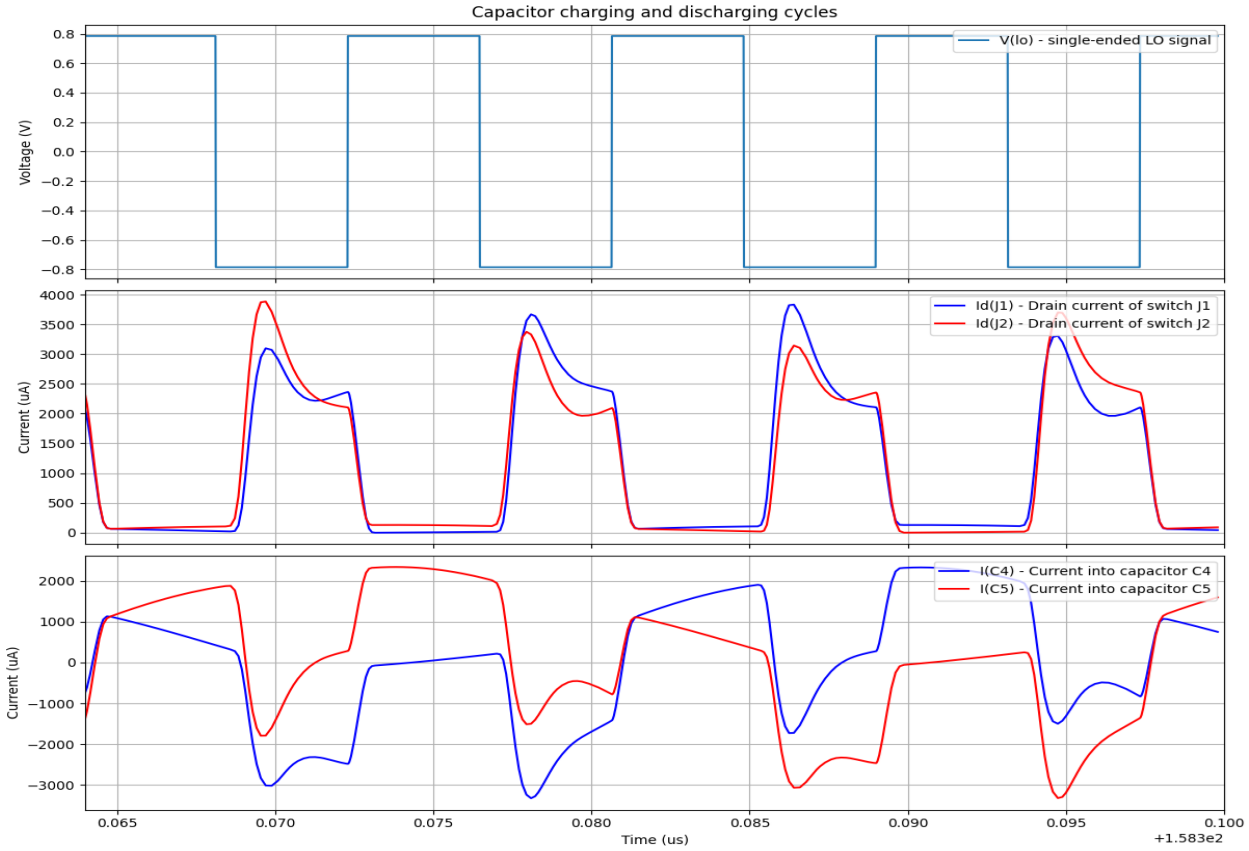
DEMAW-SIM-FIG. 1.16. DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 24 dB.

109. DEMAW-SIM-FIG. 4.16 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.16.



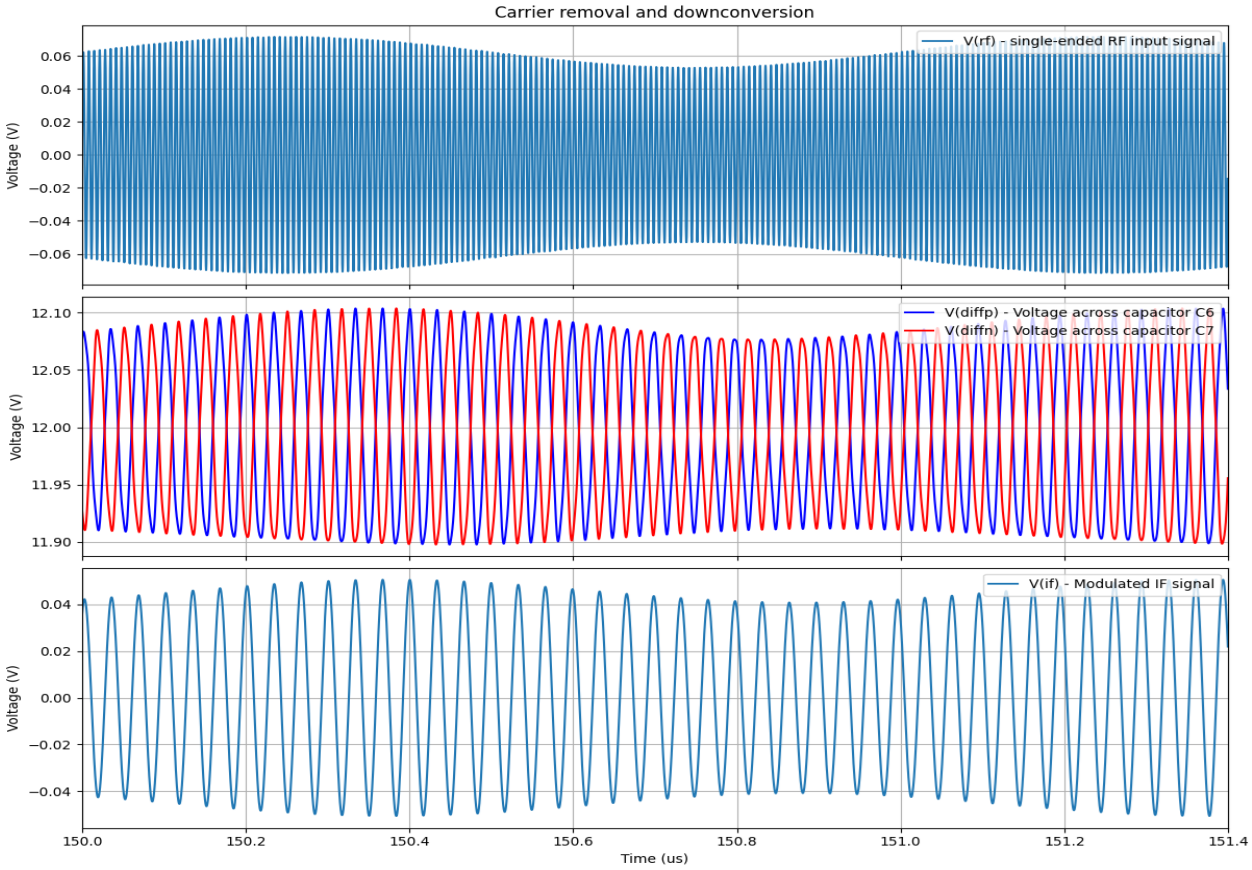
DEMAW-SIM-FIG. 4.16. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.16).

110. DEMAW-SIM-FIG. 5.16 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.16.



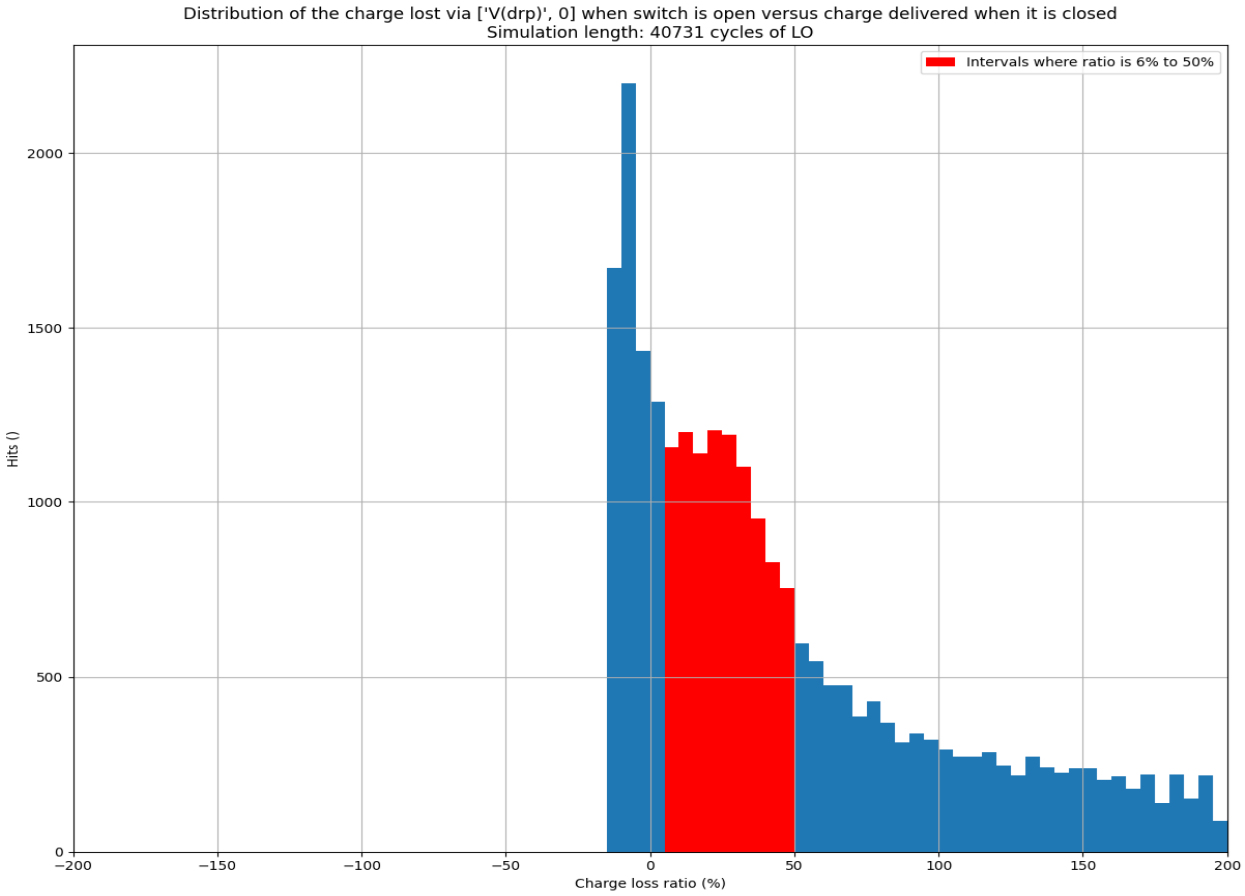
DEMAW-SIM-FIG. 5.16. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.16).

111. DEMAW-SIM-FIG. 6.16 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.16.



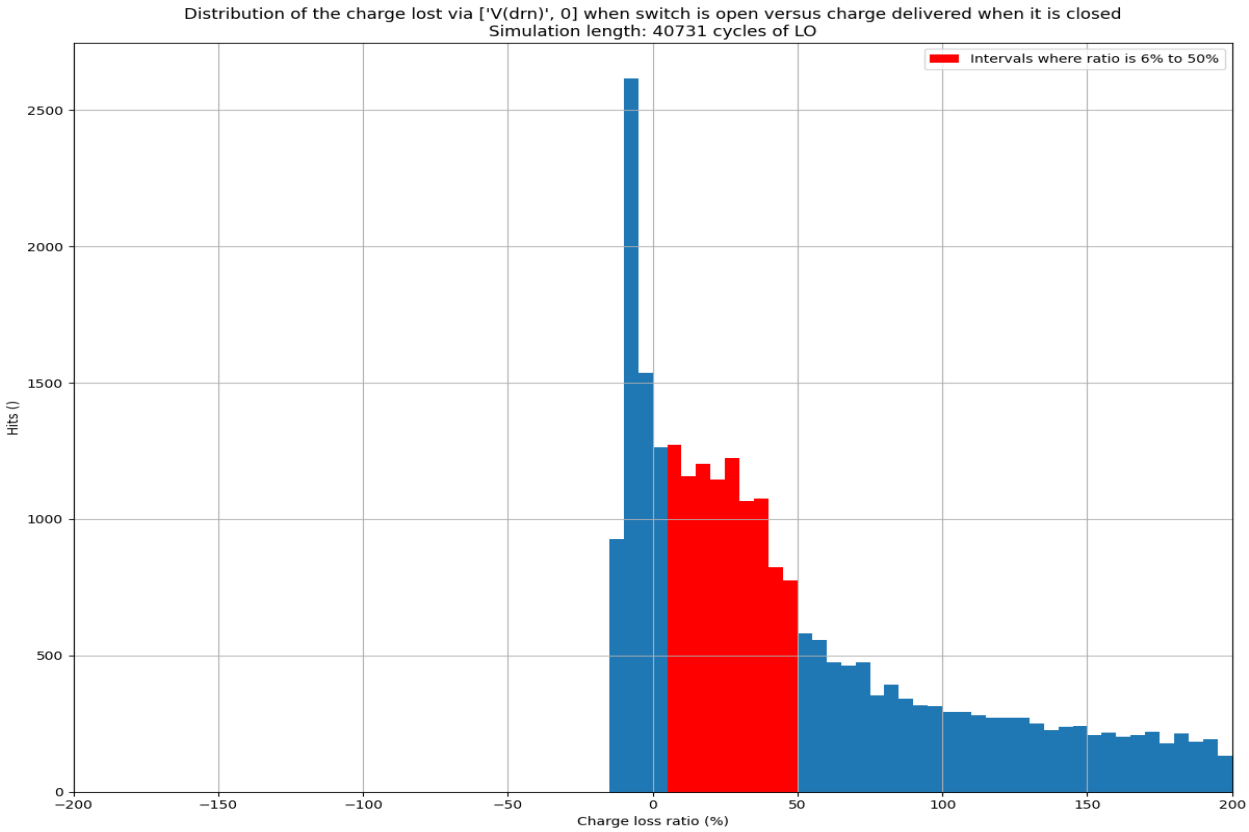
DEMAW-SIM-FIG. 6.16. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.16).

112. DEMAW-SIM-FIG. 7.16A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.16.



DEMAW-SIM-FIG. 7.16A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.16).

113. DEMAW-SIM-FIG. 7.16B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.16.



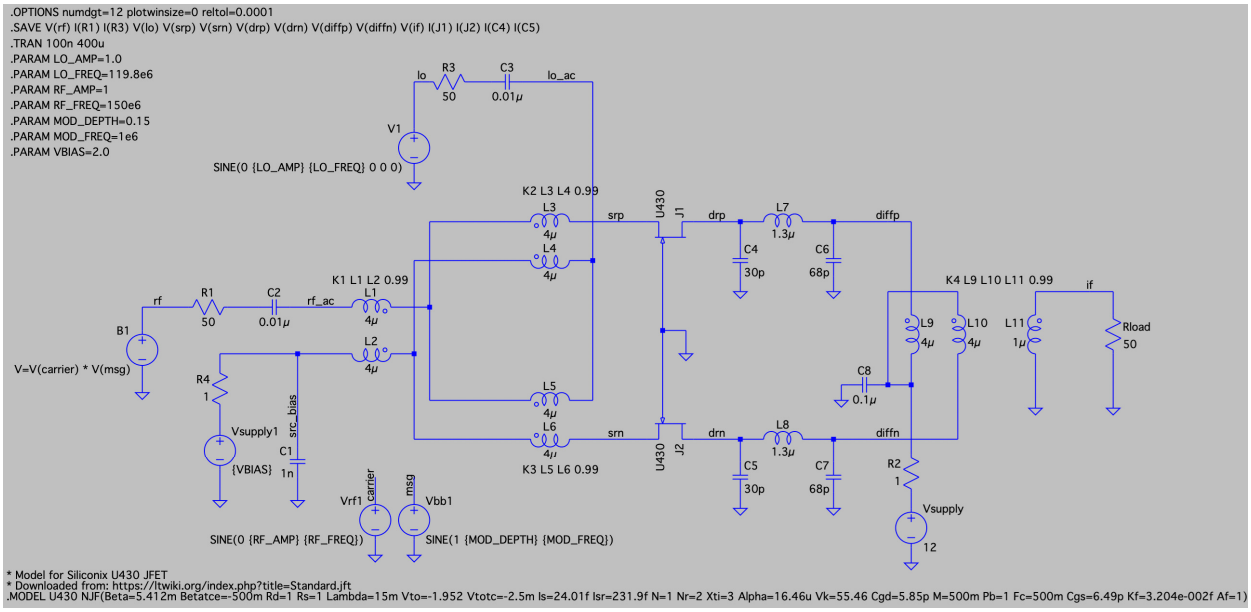
DEMAW-SIM-FIG. 7.16B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.16).

VI. DeMaw Circuit Modified to Match Oxner With a Sinusoidal LO

114. As I testified in my deposition, using sinusoidal LO signals in place of squared-up LO signals would not result in circuit behavior that would lead to different conclusions than those presented in my original Declaration, despite the POPR's false claims to the contrary. The simulation results presented in this section support my testimony. They correspond to the same circuit and input conditions as those for the simulation results presented in Section V except with a sinusoidal LO in place of a squared-up LO.

A. Simulation Results For a Large Input Signal

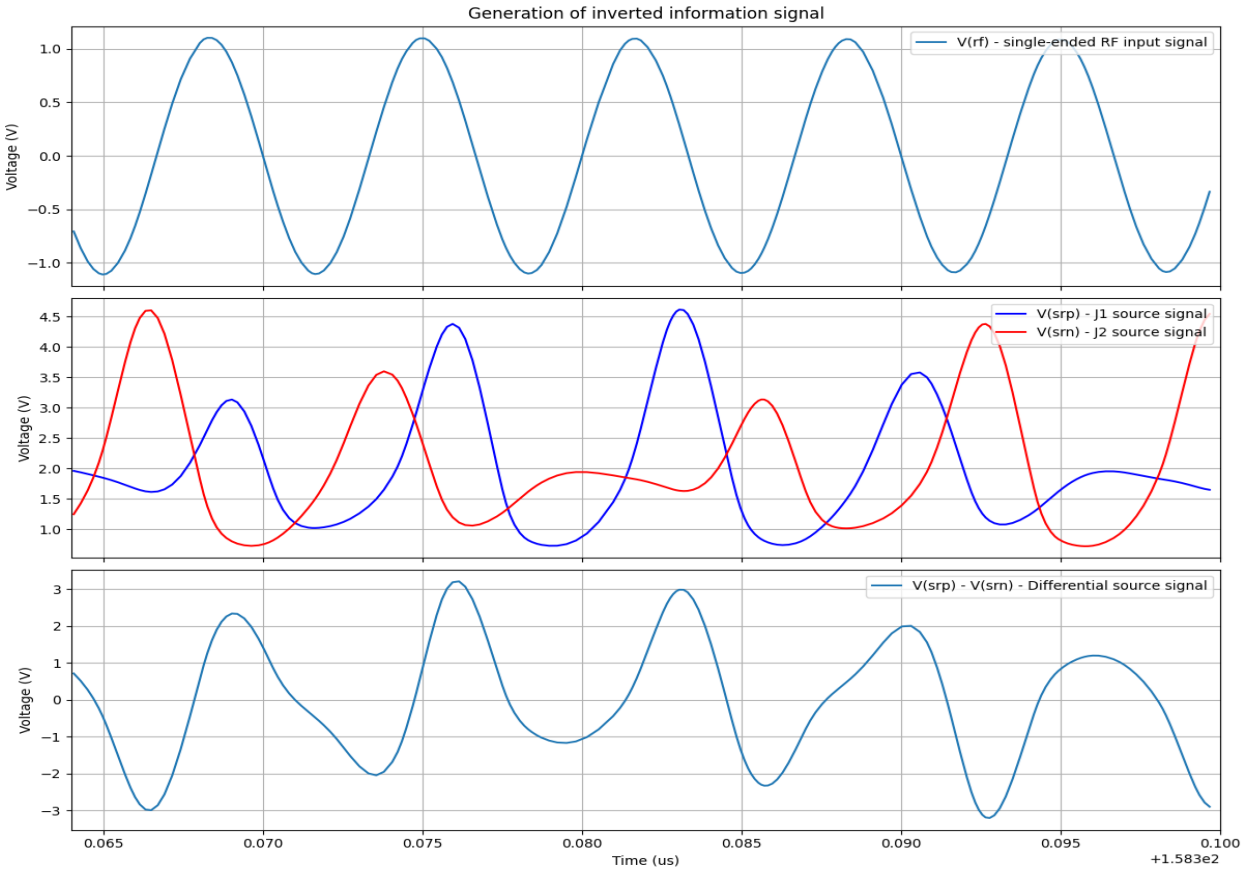
115. DEMAW-SIM-FIG. 1.17 is a schematic diagram of the DeMaw circuit modified to match Oxner with a sinusoidal LO and a large input signal. I have created additional figures DEMAW-SIM-FIGS. 4.17, 5.17, 6.17, 7.17A and 7.17B based on simulation output from DEMAW-SIM-FIG. 1.17. DEMAW-SIM-FIGS. 4.17, 5.17, 6.17, 7.17A and 7.17B show the same simulation output from DEMAW-SIM-FIG. 1.17 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.17, 4.17, 5.17, 6.17, 7.17A and 7.17B.



DEMAW-SIM-FIG. 1.17. DeMaw circuit modified to match Oxner with a sinusoidal LO and a large input signal.

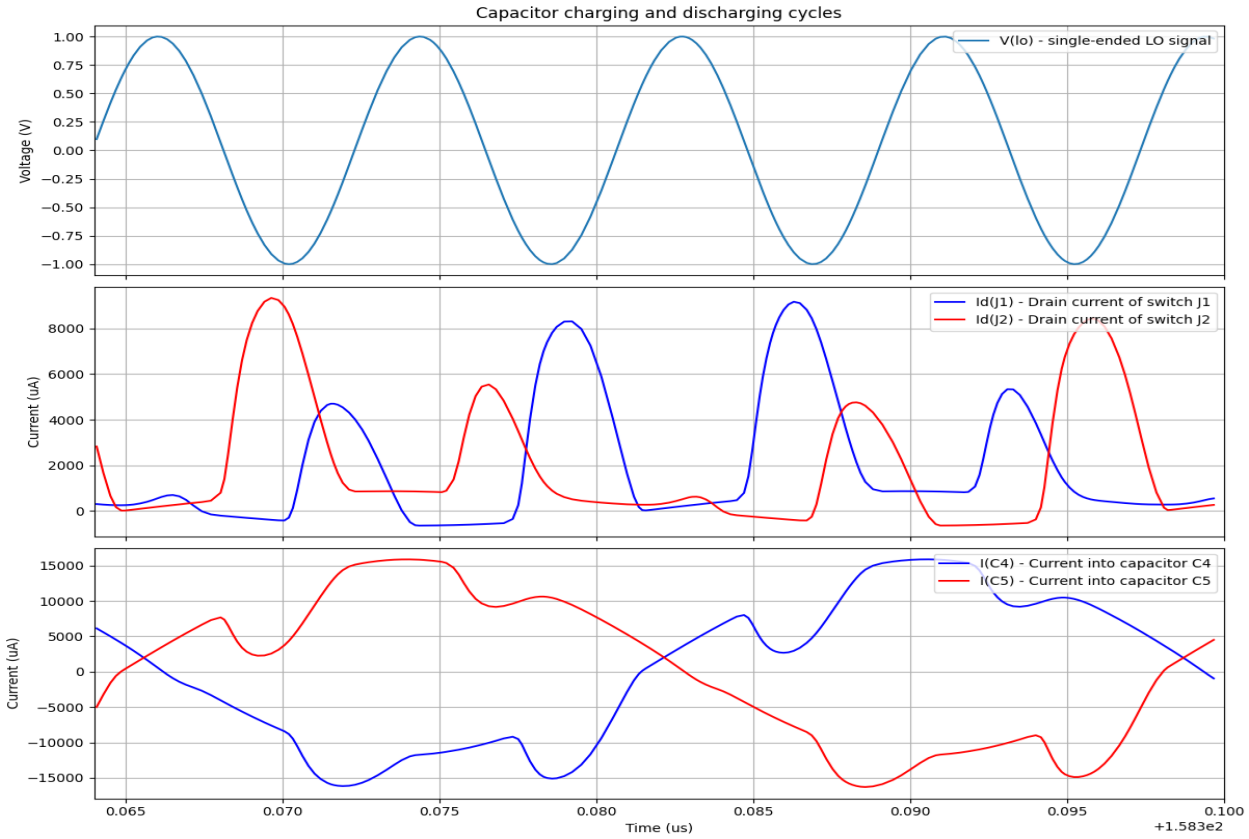
116. DEMAW-SIM-FIG. 4.17 is a graphical representation of the generation

of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.17.



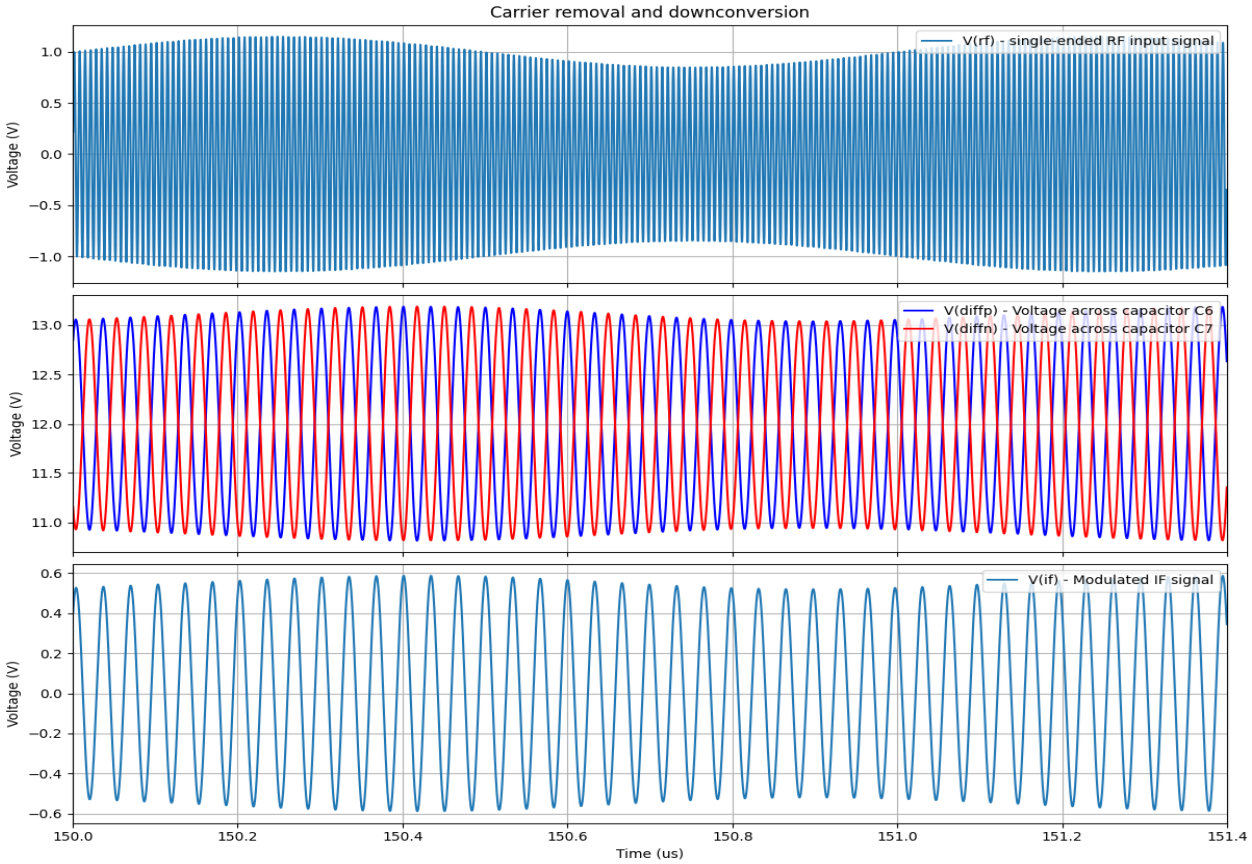
DEMAW-SIM-FIG. 4.17. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.17).

117. DEMAW-SIM-FIG. 5.17 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.17.



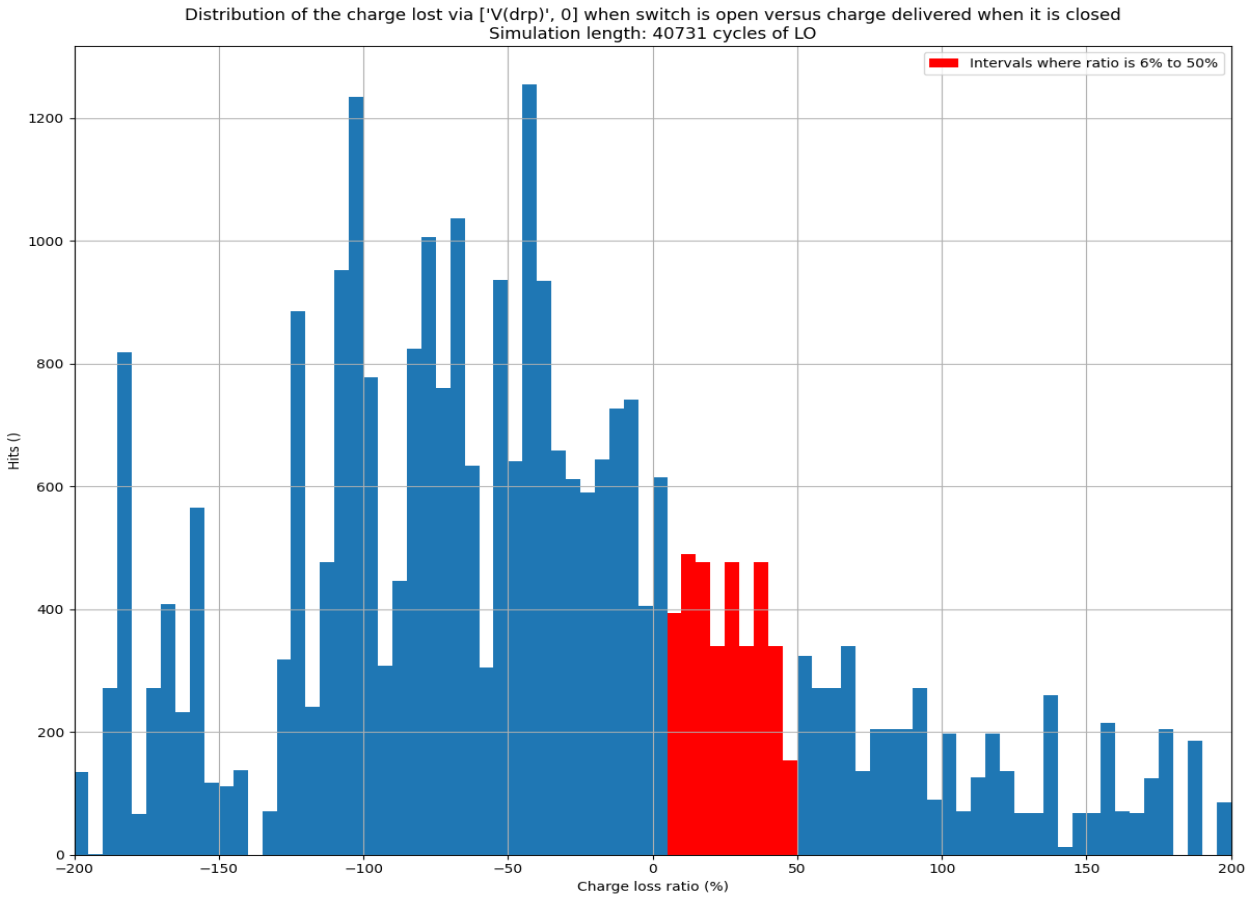
DEMAW-SIM-FIG. 5.17. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.17).

118. DEMAW-SIM-FIG. 6.17 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.17.



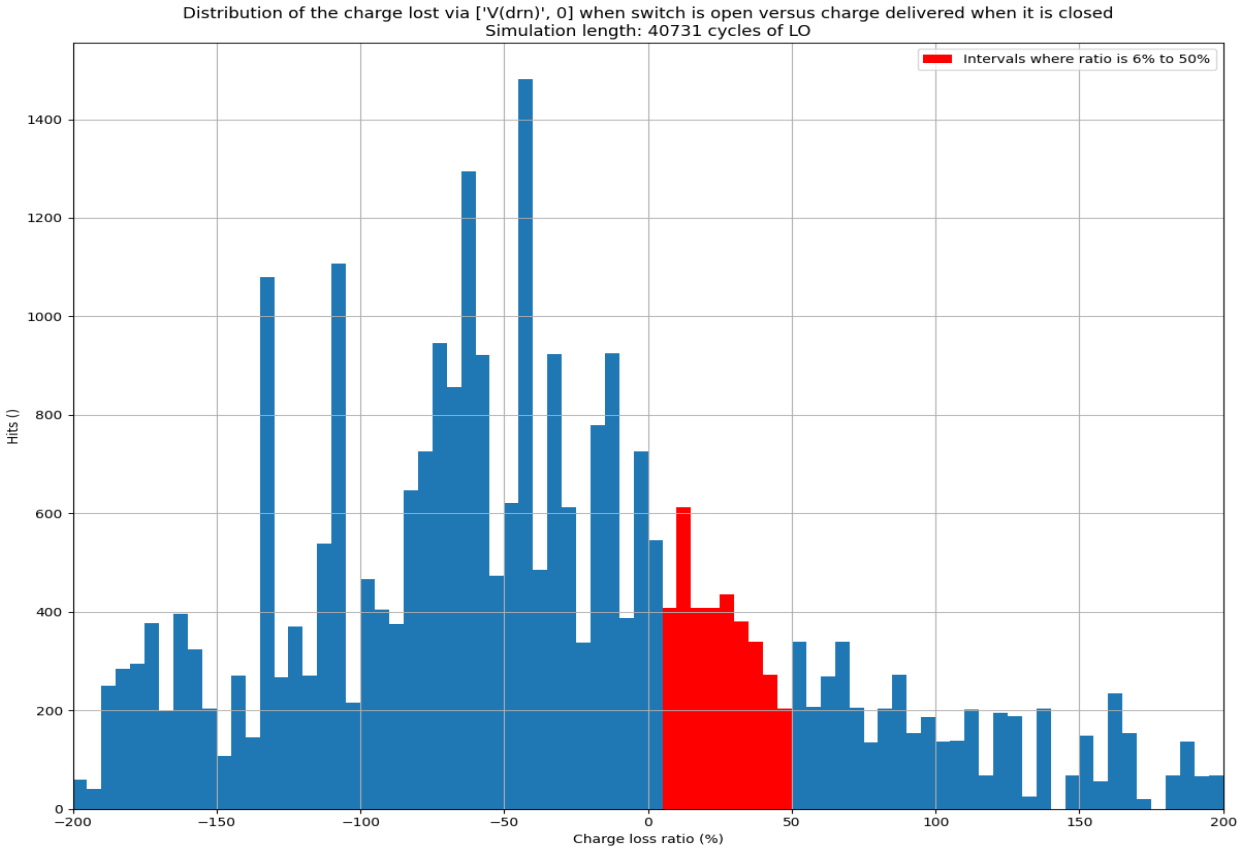
DEMAW-SIM-FIG. 6.17. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.17).

119. DEMAW-SIM-FIG. 7.17A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.17.



DEMAW-SIM-FIG. 7.17A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.17).

120. DEMAW-SIM-FIG. 7.17B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.17.

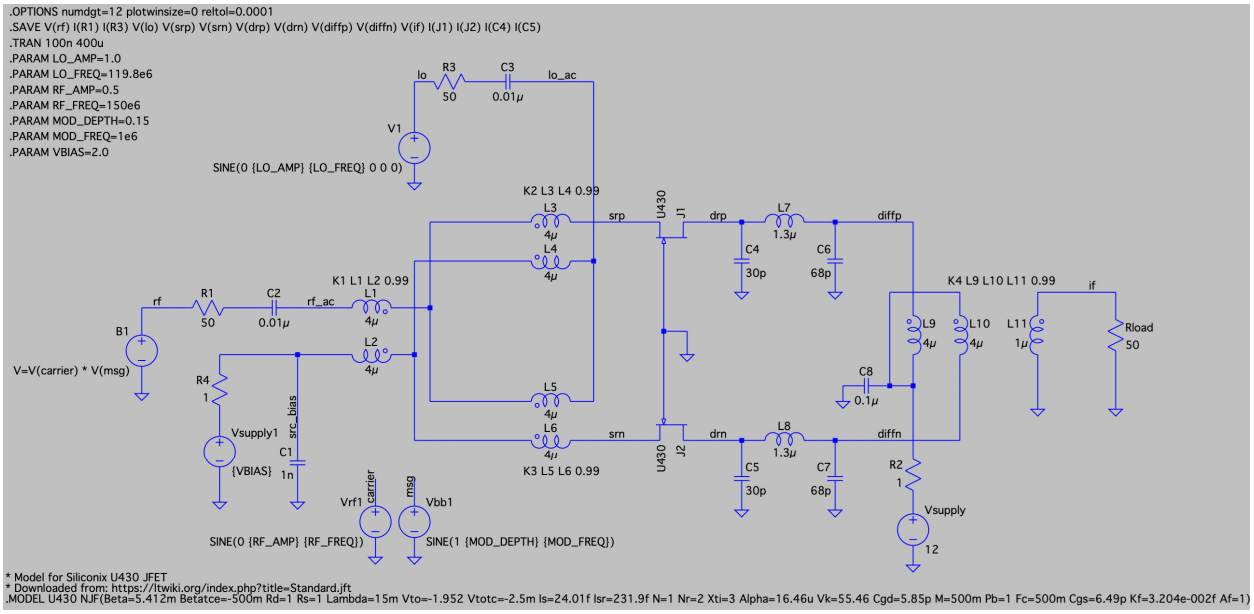


DEMAW-SIM-FIG. 7.17B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.17).

B. Simulation Results For an Input Signal Reduced by 6 dB

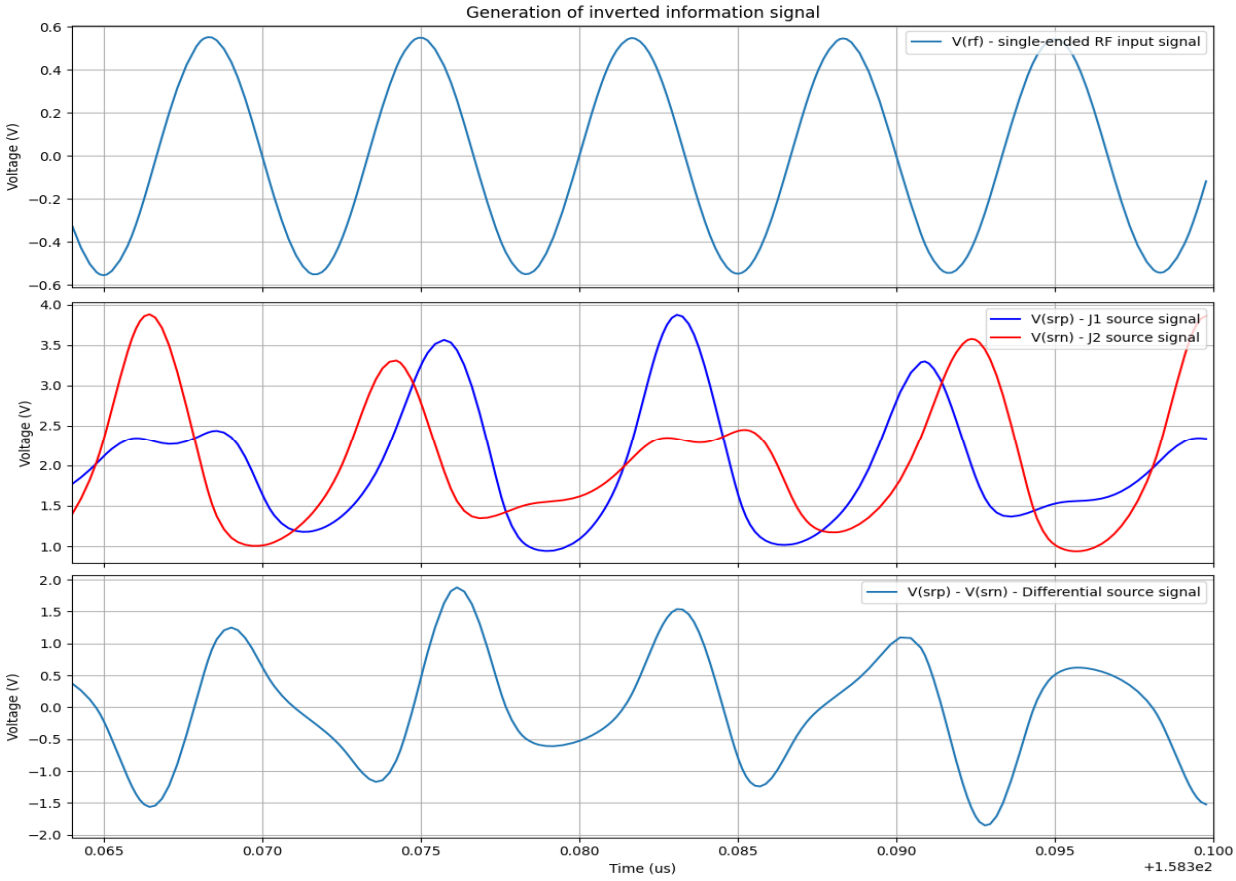
121. DEMAW-SIM-FIG. 1.18 is a schematic diagram of the simulated DeMaw FIG. 6.7 circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 6 dB. I have created additional figures DEMAW-SIM-FIGS. 4.18, 5.18, 6.18, 7.18A and 7.18B based on simulation output from DEMAW-SIM-FIG. 1.18. DEMAW-SIM-FIGS. 4.18, 5.18, 6.18, 7.18A and 7.18B show the same simulation output from DEMAW-SIM-FIG. 1.18 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.18, 4.18, 5.18, 6.18, 7.18A and 7.18B.



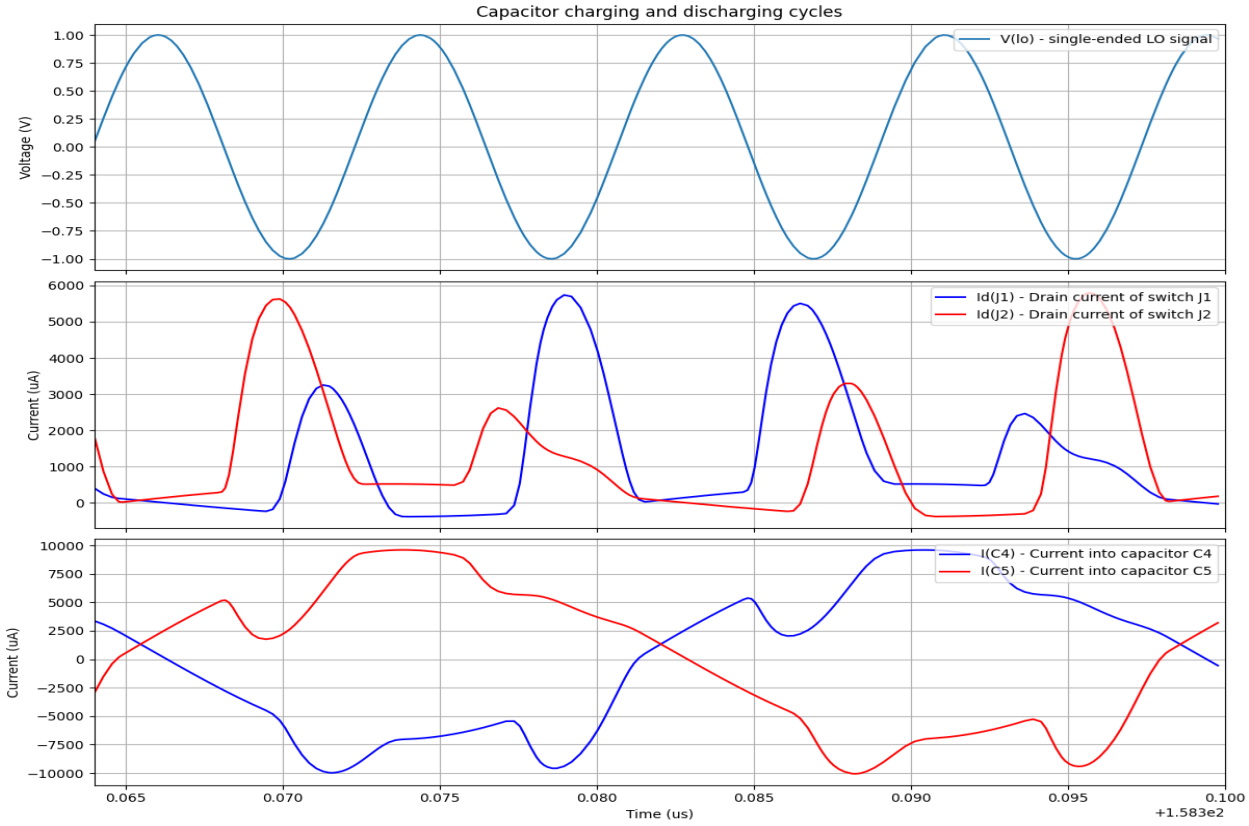
DEMAW-SIM-FIG. 1.18. DeMaw circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 6 dB.

122. DEMAW-SIM-FIG. 4.18 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.18.



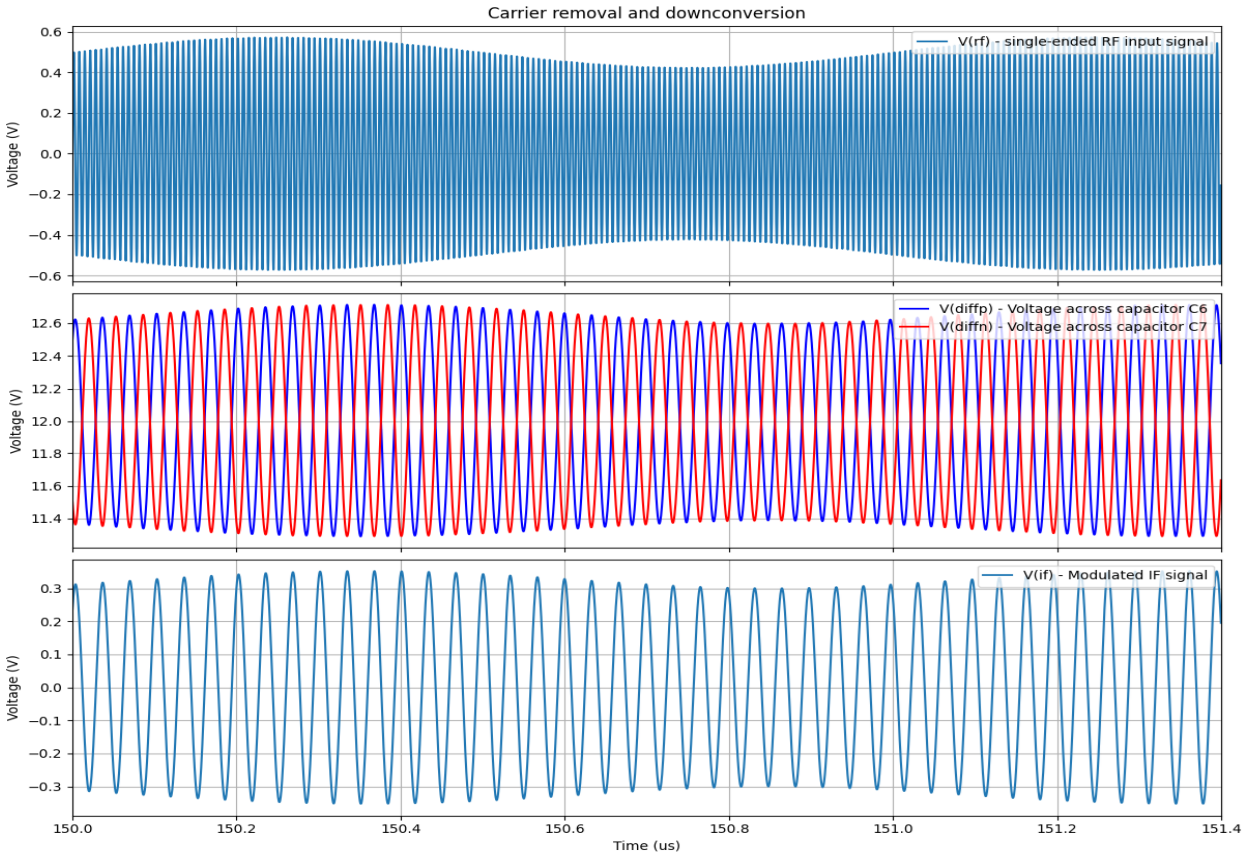
DEMAW-SIM-FIG. 4.18. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.18).

123. DEMAW-SIM-FIG. 5.18 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.18.



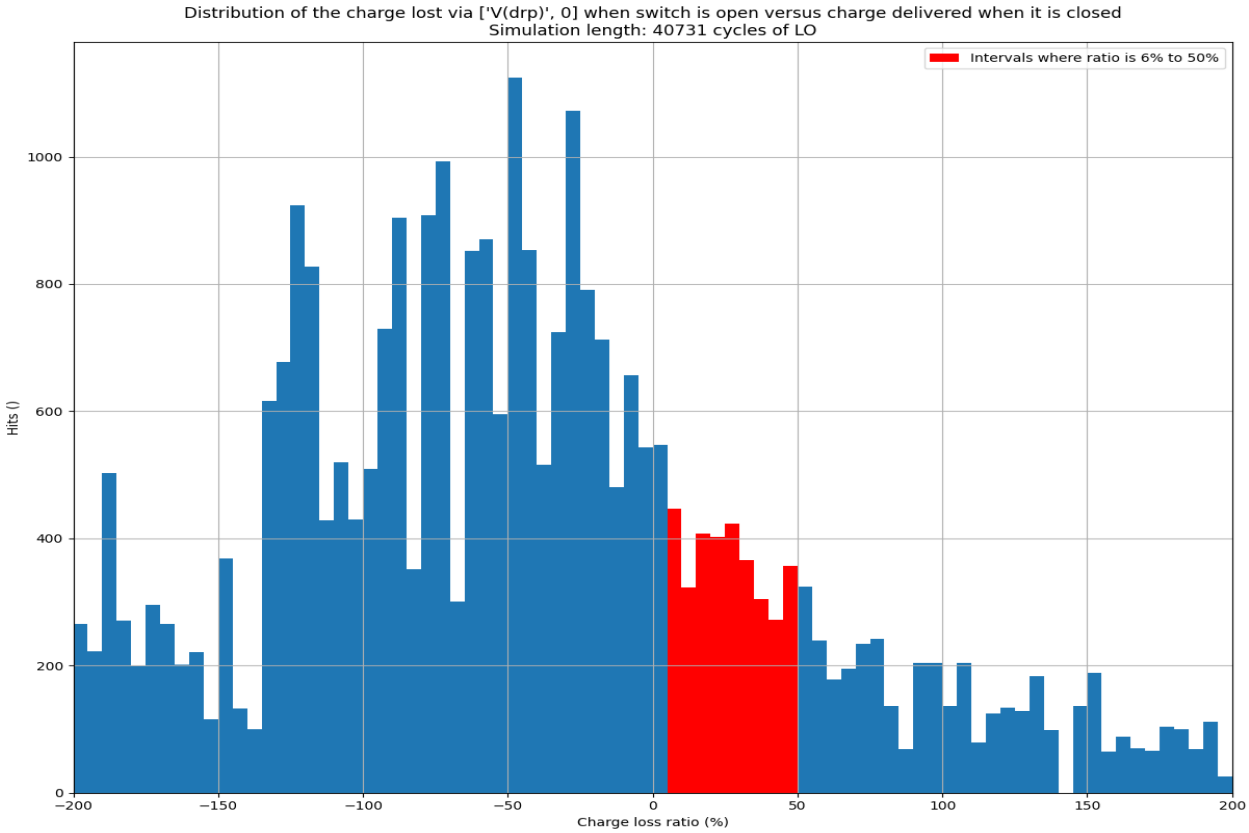
DEMAW-SIM-FIG. 5.18. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.18).

124. DEMAW-SIM-FIG. 6.18 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.18.



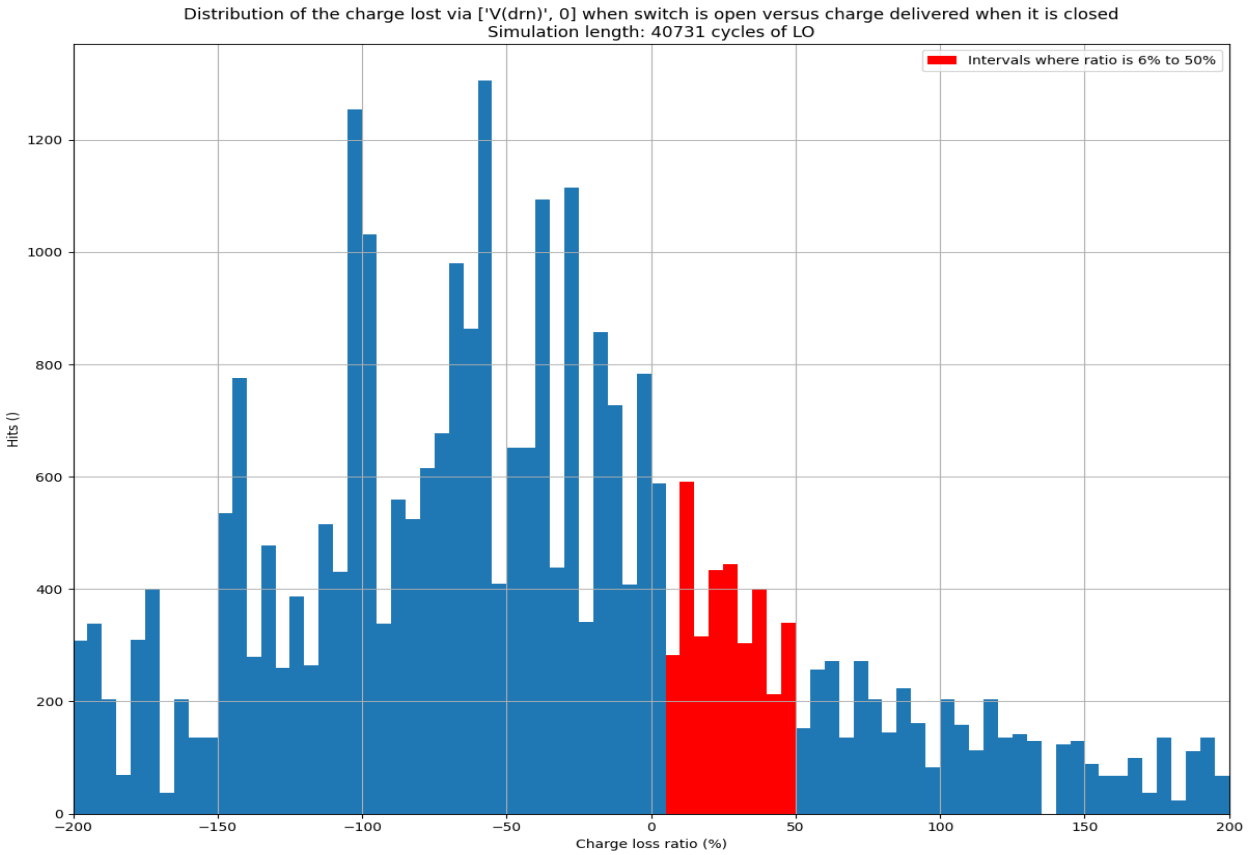
DEMAW-SIM-FIG. 6.18. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.18).

125. DEMAW-SIM-FIG. 7.18A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.18.



DEMAW-SIM-FIG. 7.18A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.18).

126. DEMAW-SIM-FIG. 7.18B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.18.

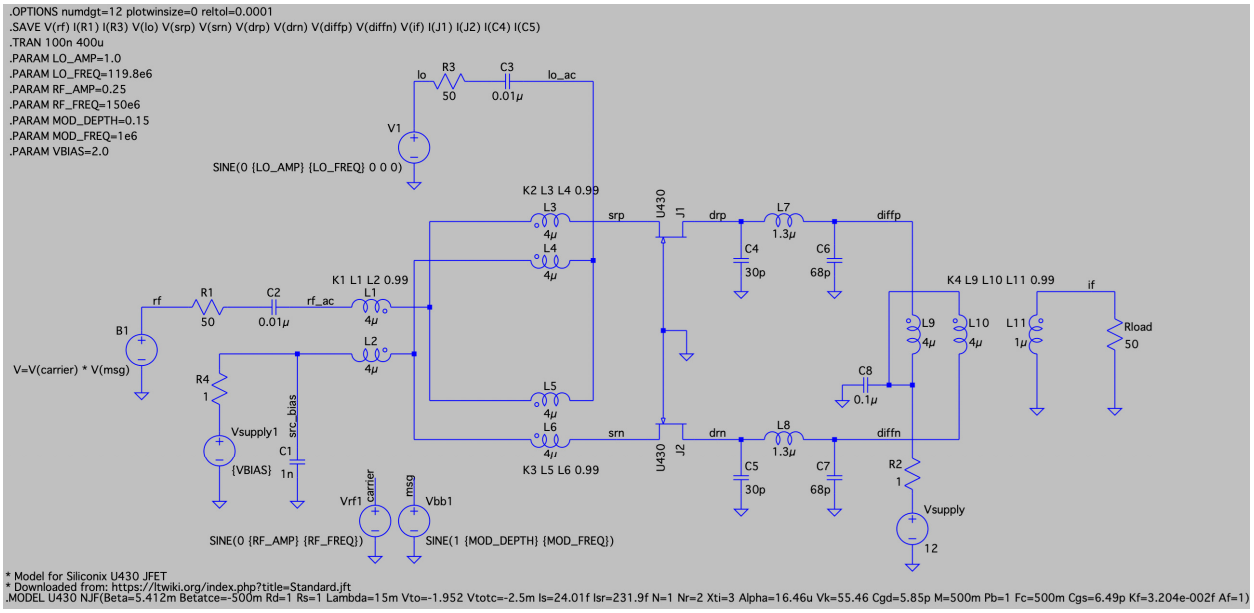


DEMAW-SIM-FIG. 7.18B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.18).

C. Simulation Results For an Input Signal Reduced by 12 dB

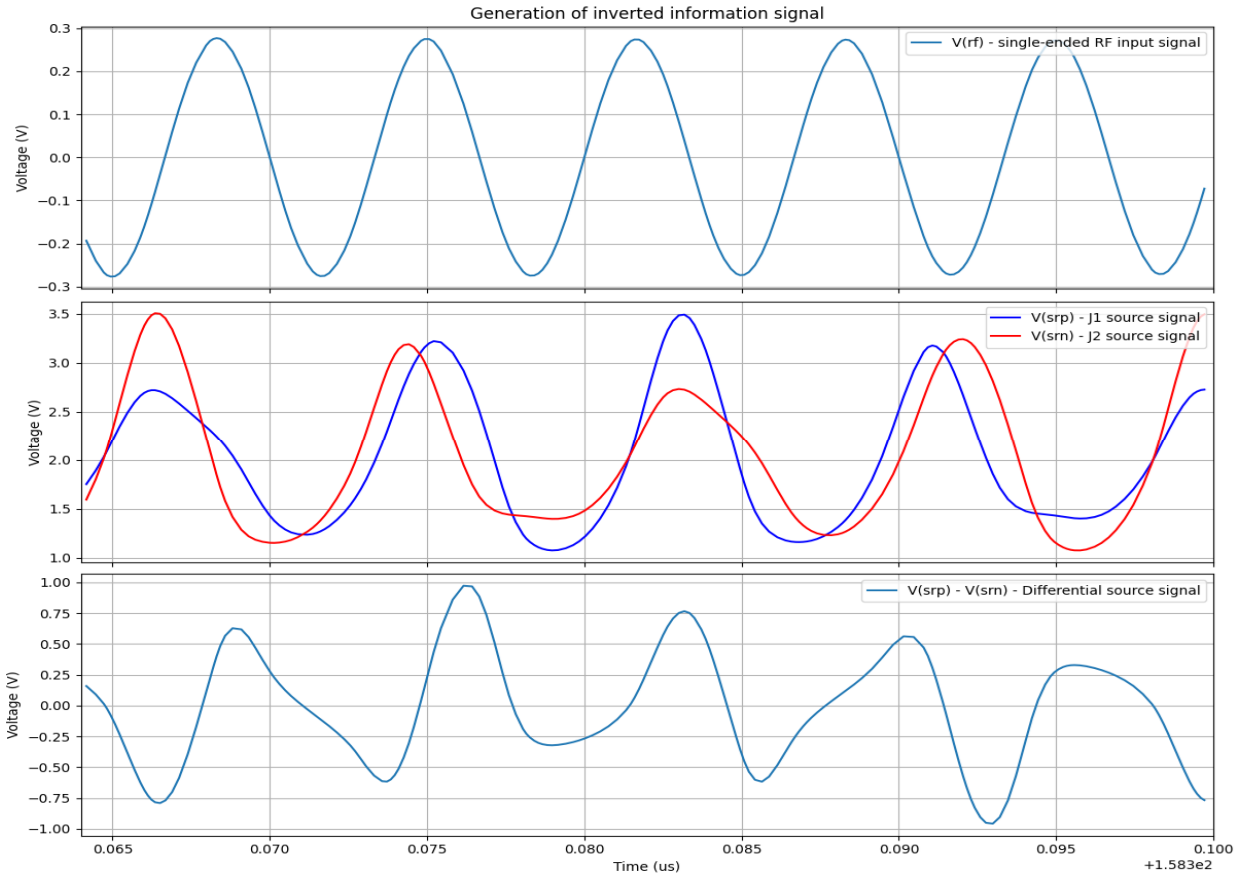
127. DEMAW-SIM-FIG. 1.19 is a schematic diagram of the simulated DeMaw FIG. 6.7 circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 12 dB. I have created additional figures DEMAW-SIM-FIGS. 4.19, 5.19, 6.19, 7.19A and 7.19B based on simulation output from DEMAW-SIM-FIG. 1.19. DEMAW-SIM-FIGS. 4.19, 5.19, 6.19, 7.19A and 7.19B show the same simulation output from DEMAW-SIM-FIG. 1.19 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.19, 4.19, 5.19, 6.19, 7.19A and 7.19B.



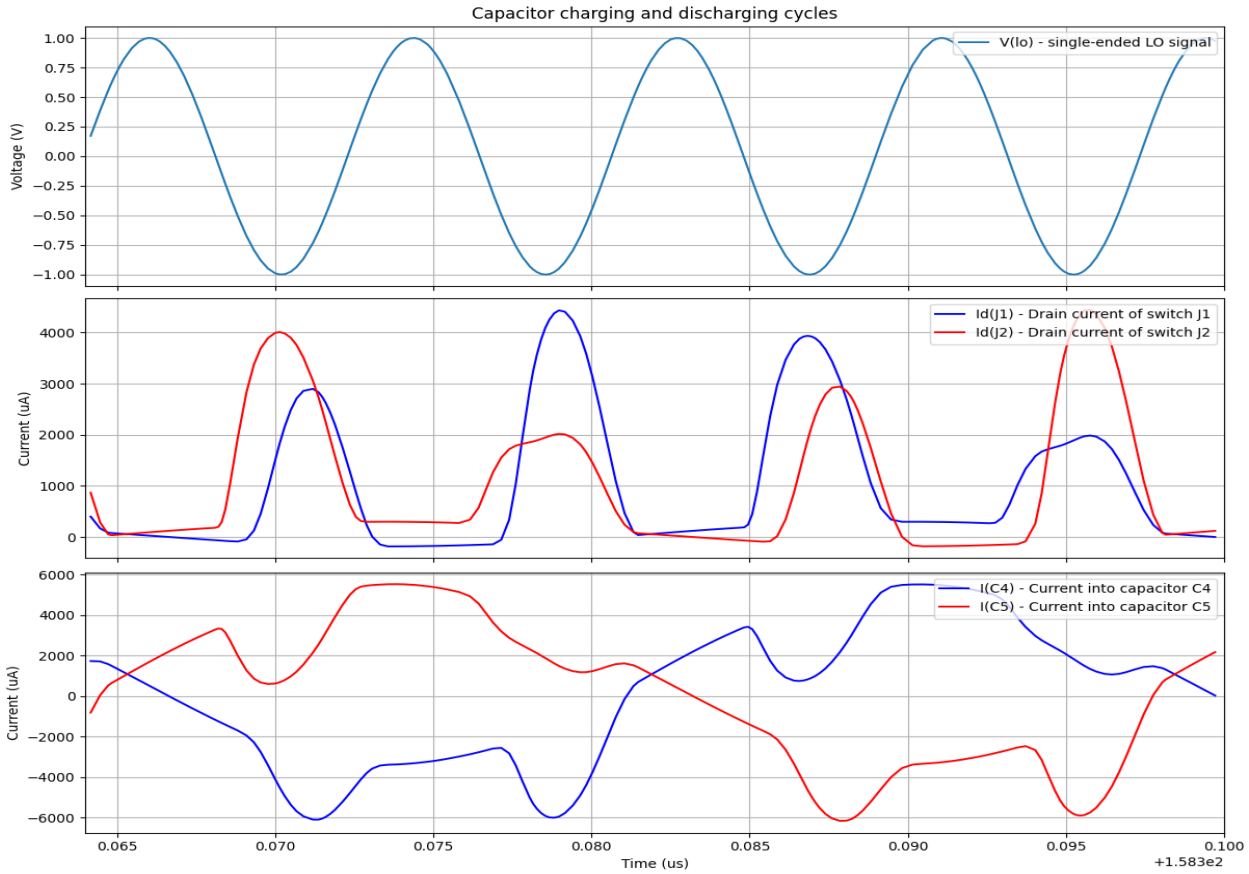
DEMAW-SIM-FIG. 1.19. DeMaw circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 12 dB.

128. DEMAW-SIM-FIG. 4.19 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.19.



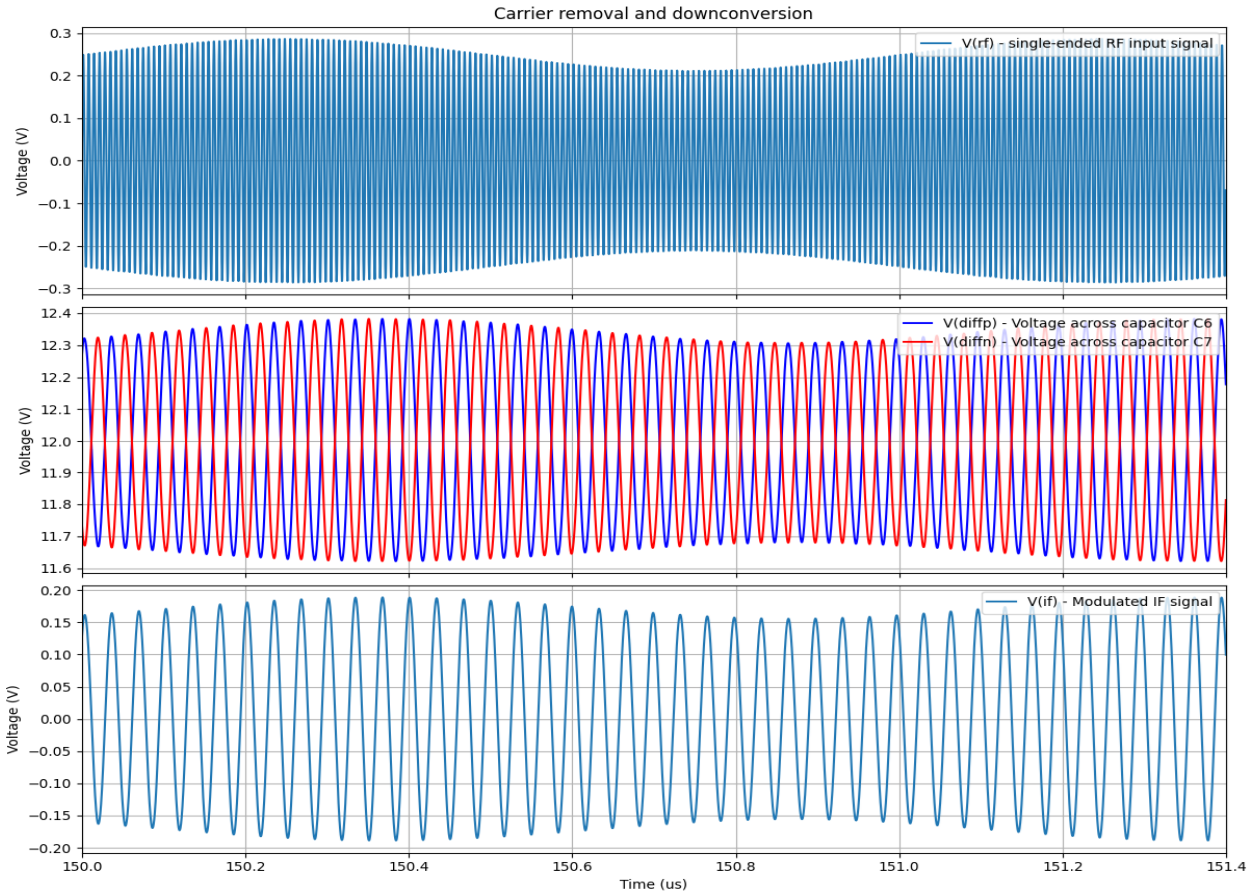
DEMAW-SIM-FIG. 4.19. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.19).

129. DEMAW-SIM-FIG. 5.19 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.19.



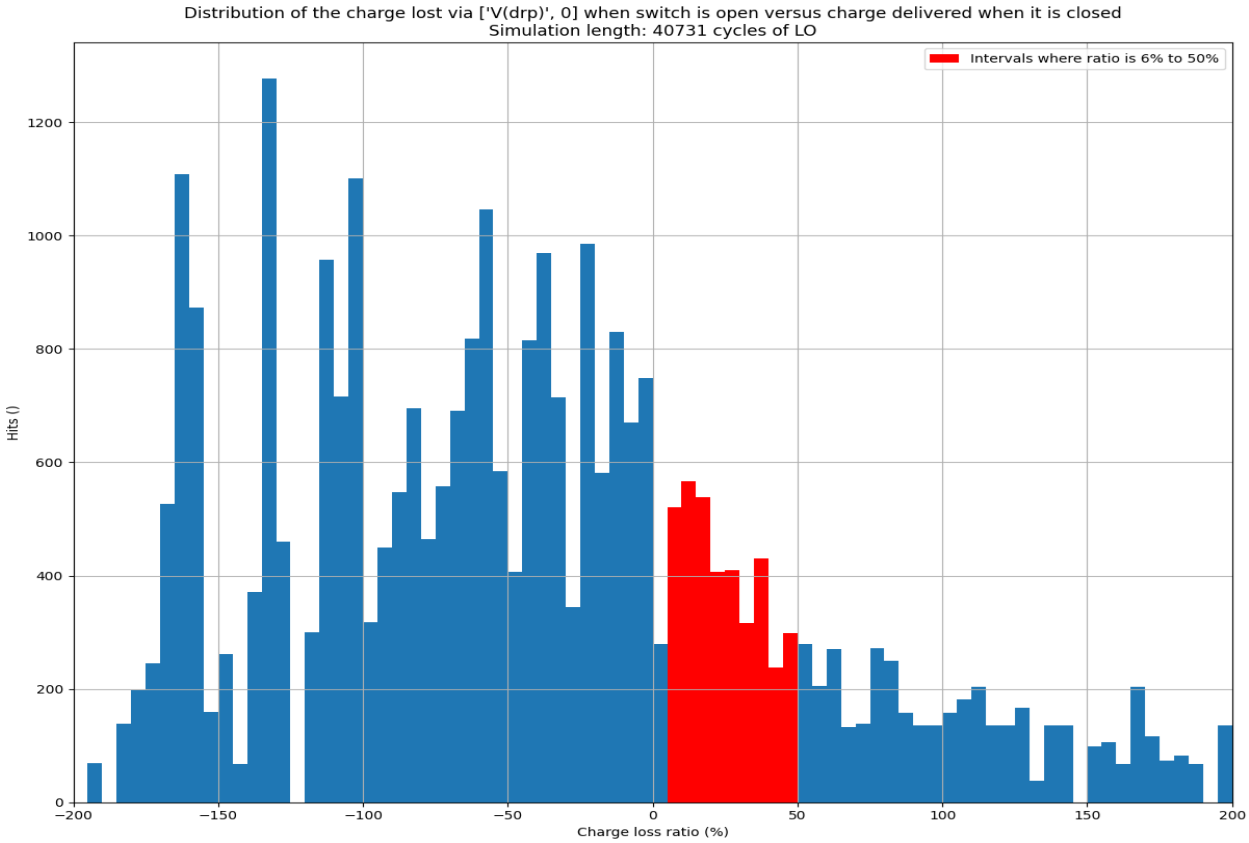
DEMAW-SIM-FIG. 5.19. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.19).

130. DEMAW-SIM-FIG. 6.19 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.19.



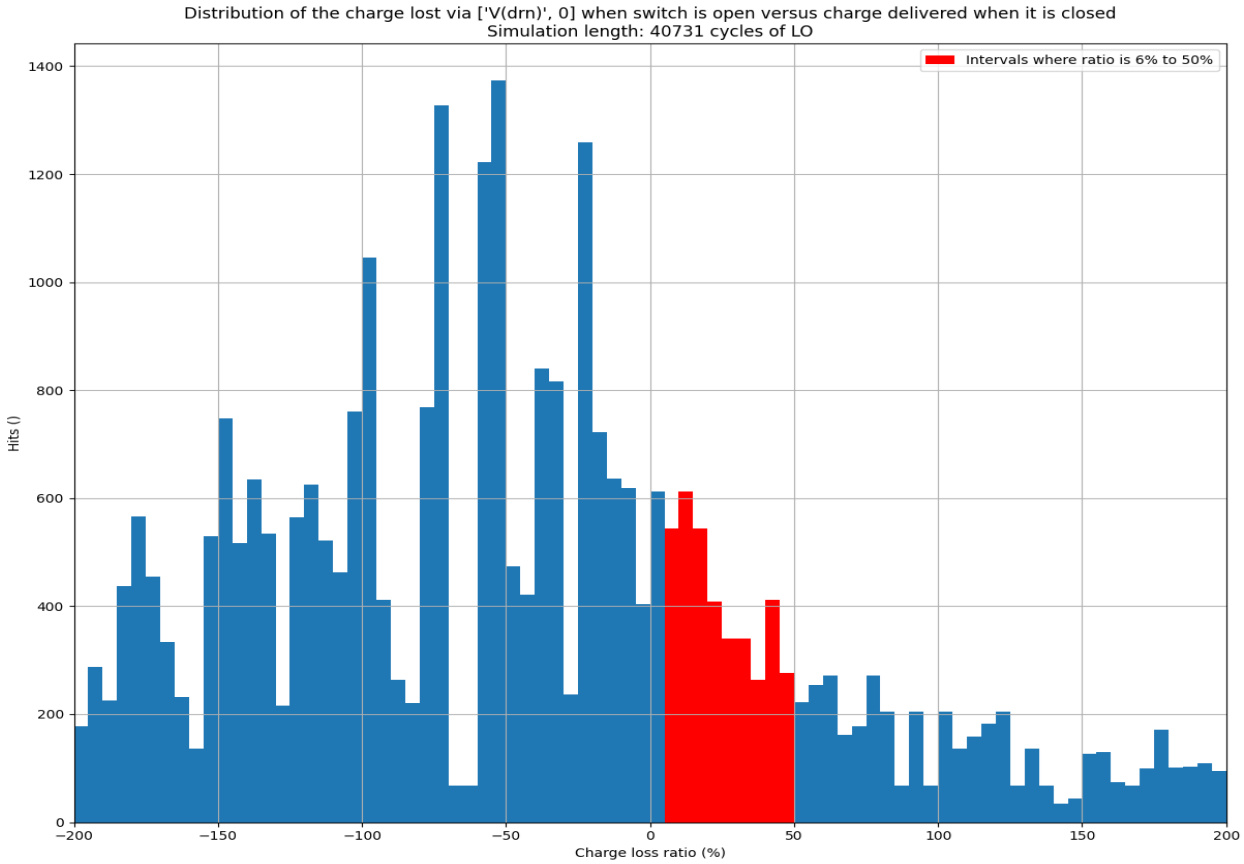
DEMAW-SIM-FIG. 6.19. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.19).

131. DEMAW-SIM-FIG. 7.19A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.19.



DEMAW-SIM-FIG. 7.19A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.19).

132. DEMAW-SIM-FIG. 7.19B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.19.

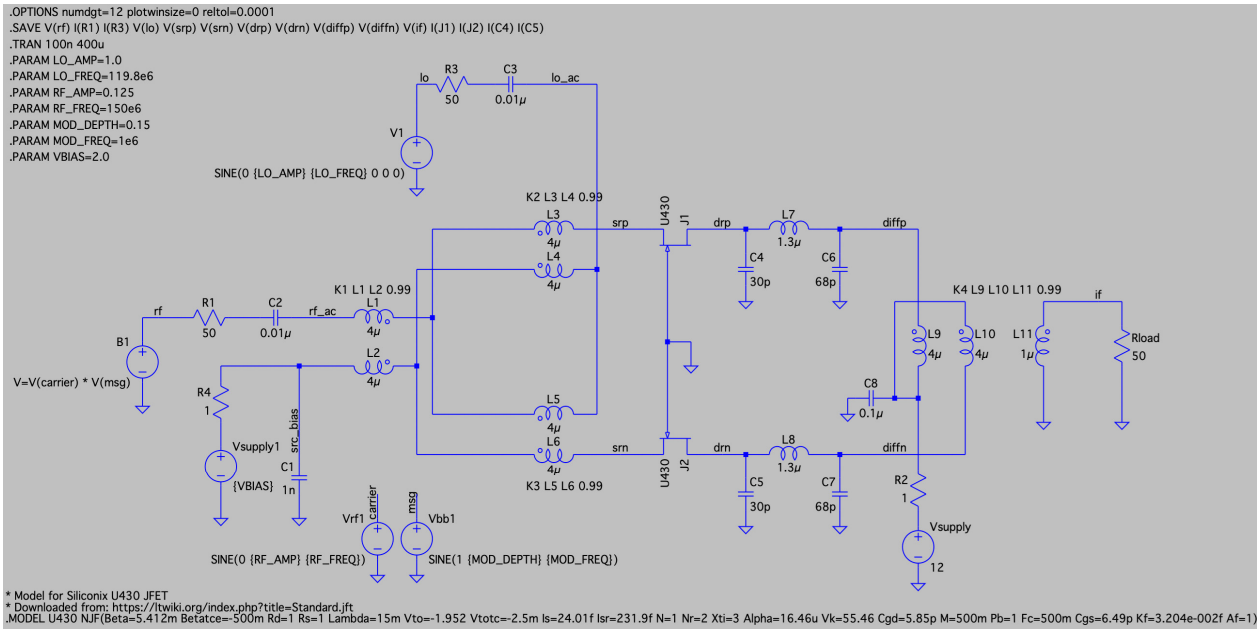


DEMAW-SIM-FIG. 7.19B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.19).

D. Simulation Results For an Input Signal Reduced by 18 dB

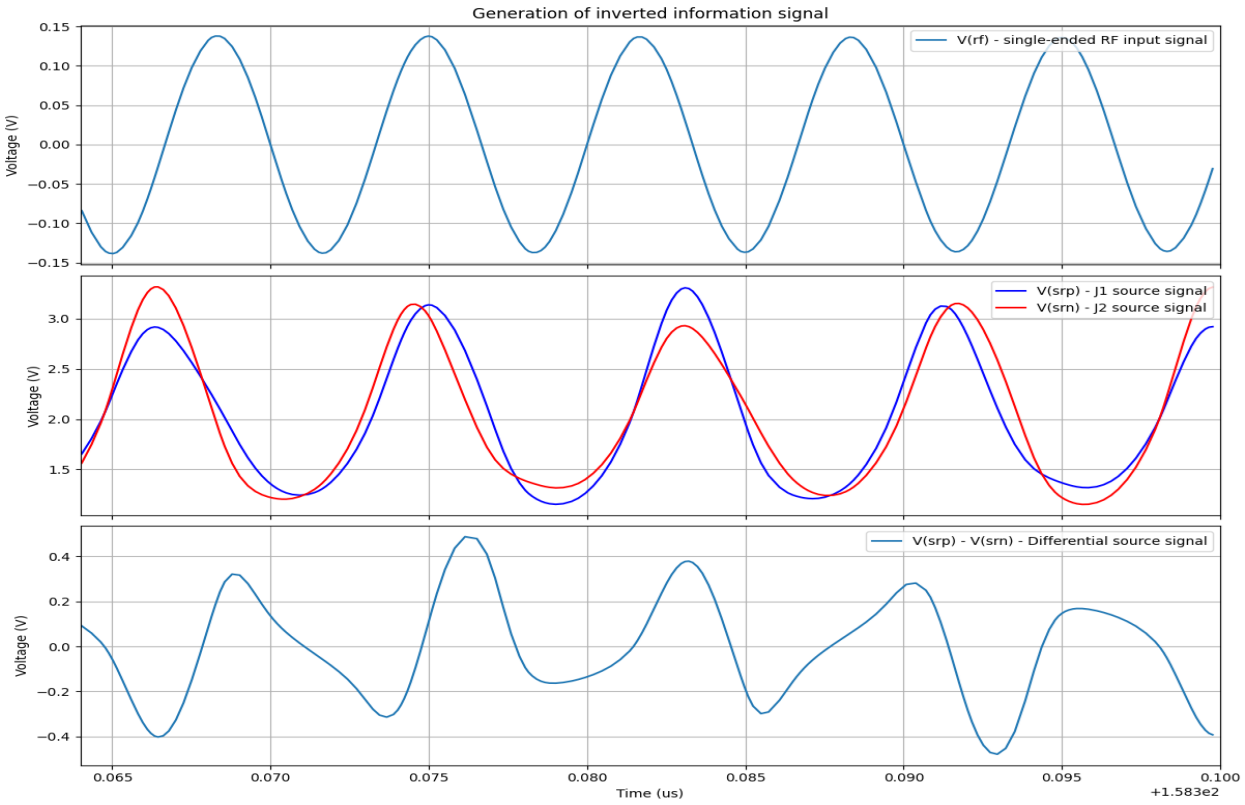
133. DEMAW-SIM-FIG. 1.20 is a schematic diagram of the simulated DeMaw FIG. 6.7 circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 18 dB. I have created additional figures DEMAW-SIM-FIGS. 4.20, 5.20, 6.20, 7.20A and 7.20B based on simulation output from DEMAW-SIM-FIG. 1.20. DEMAW-SIM-FIGS. 4.20, 5.20, 6.20, 7.20A and 7.20B show the same simulation output from DEMAW-SIM-FIG. 1.20 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.20, 4.20, 5.20, 6.20, 7.20A and 7.20B.



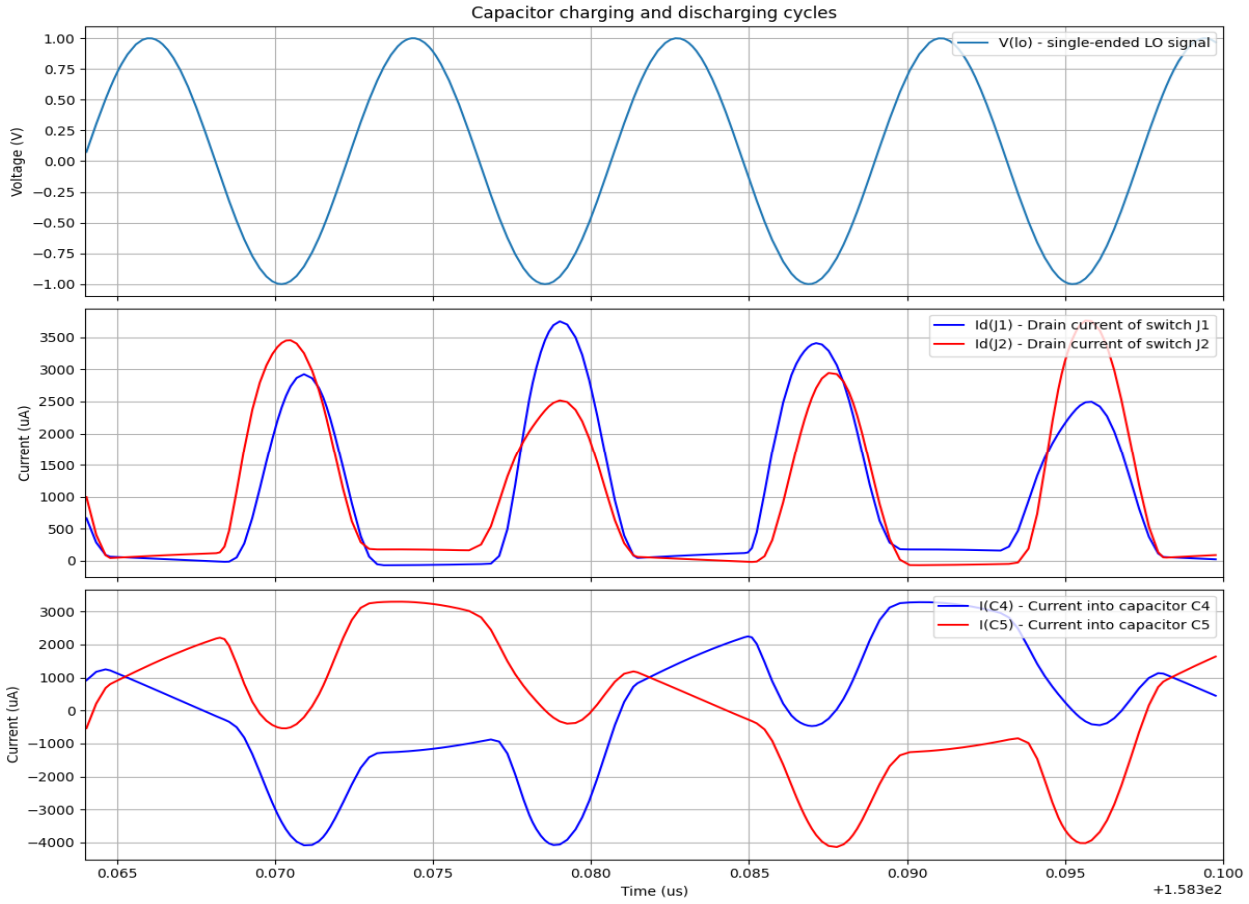
DEMAW-SIM-FIG. 1.20. DeMaw circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 18 dB.

134. DEMAW-SIM-FIG. 4.20 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.20.



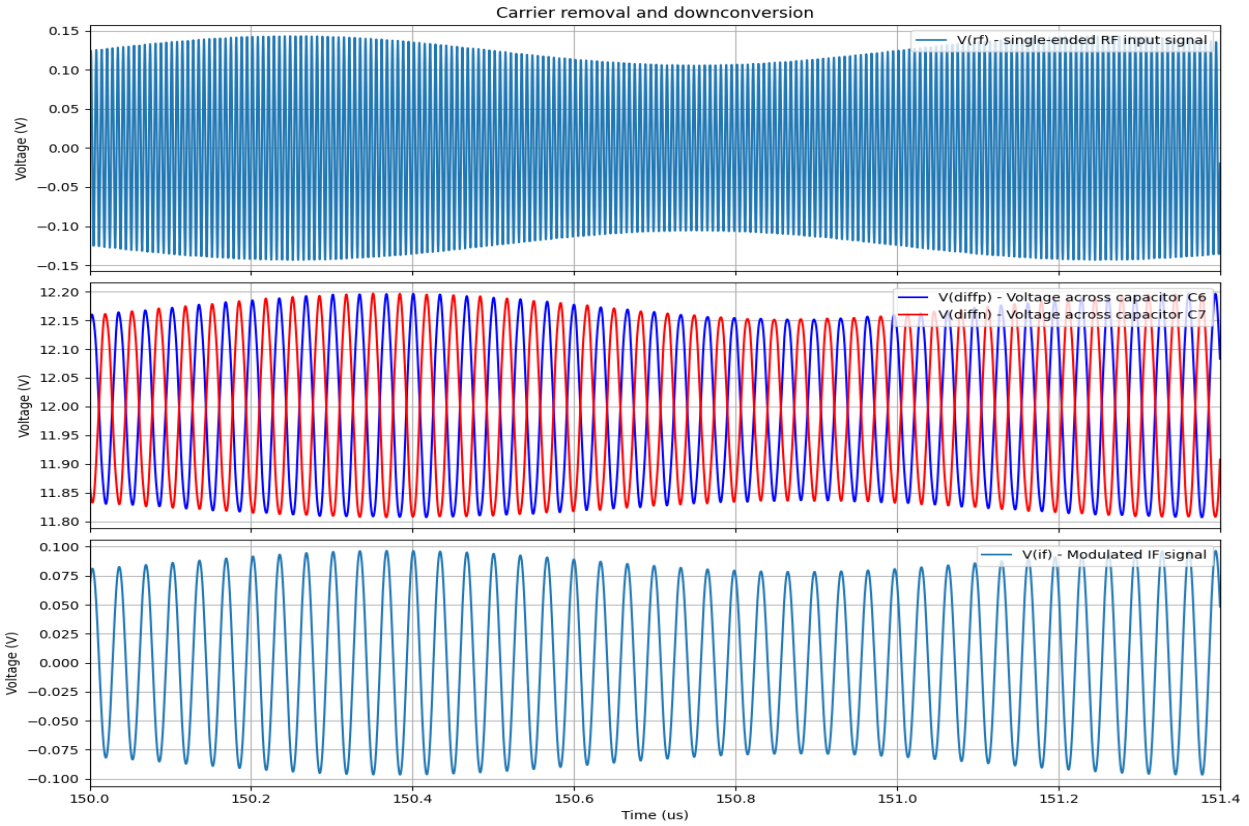
DEMAW-SIM-FIG. 4.20. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.20).

135. DEMAW-SIM-FIG. 5.20 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.20.



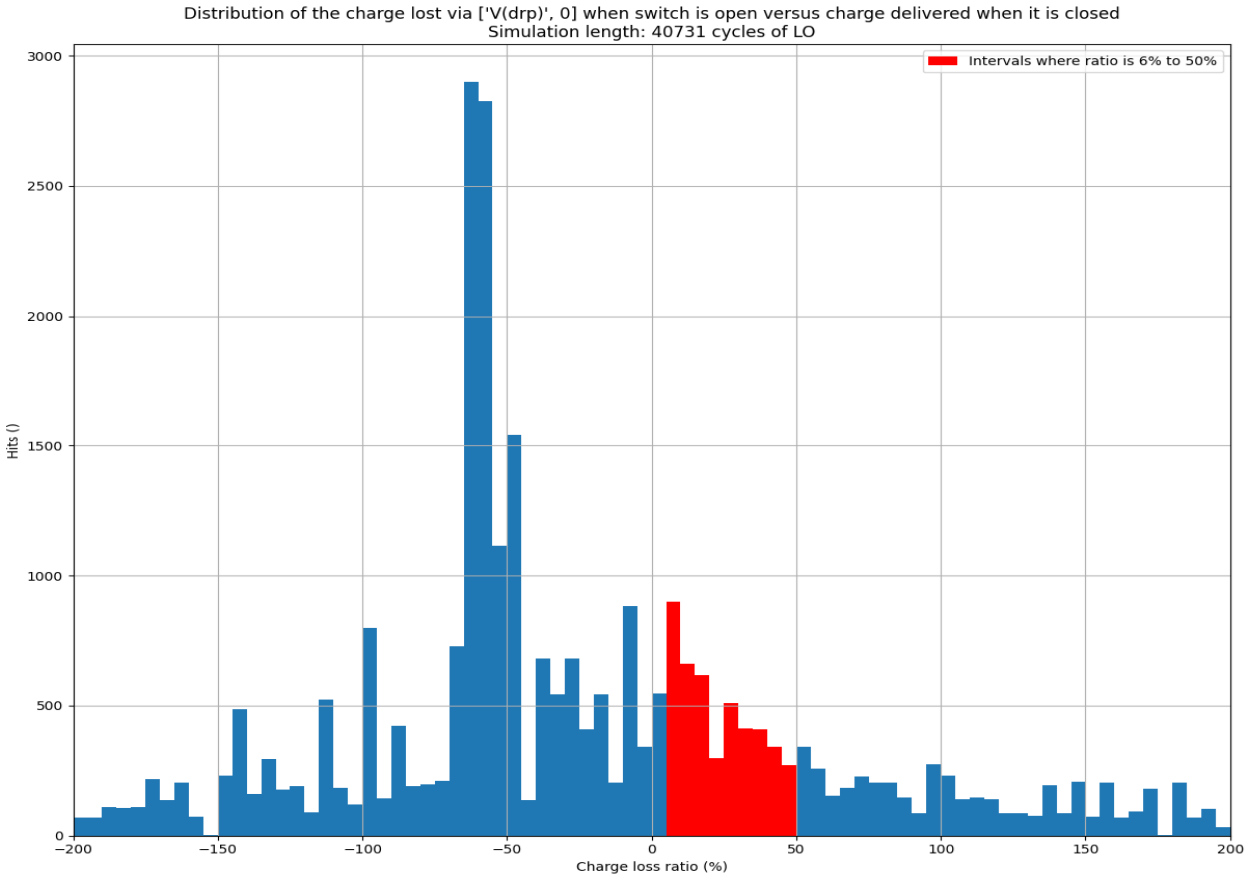
DEMAW-SIM-FIG. 5.20. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.20).

136. DEMAW-SIM-FIG. 6.20 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.20.



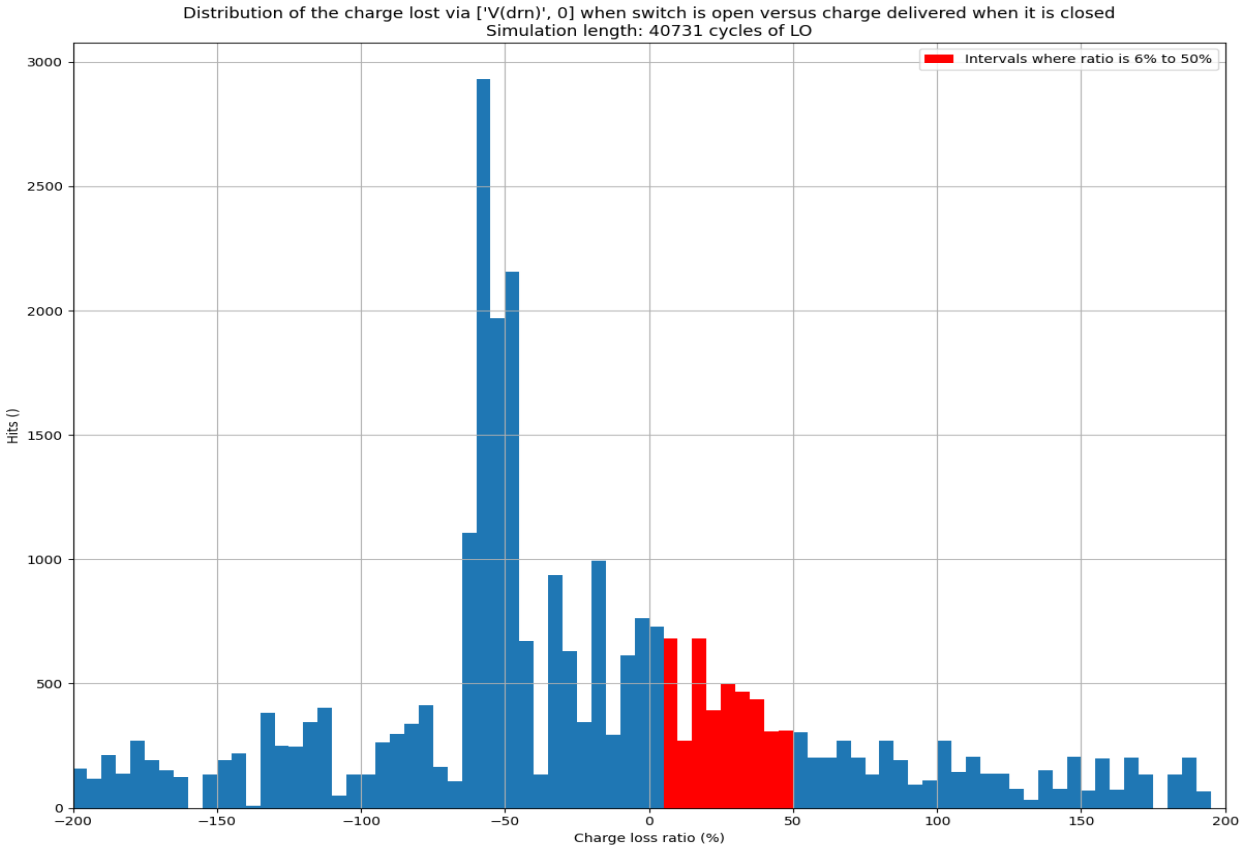
DEMAW-SIM-FIG. 6.20. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.20).

137. DEMAW-SIM-FIG. 7.20A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.20.



DEMAW-SIM-FIG. 7.20A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.20).

138. DEMAW-SIM-FIG. 7.20B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.20.

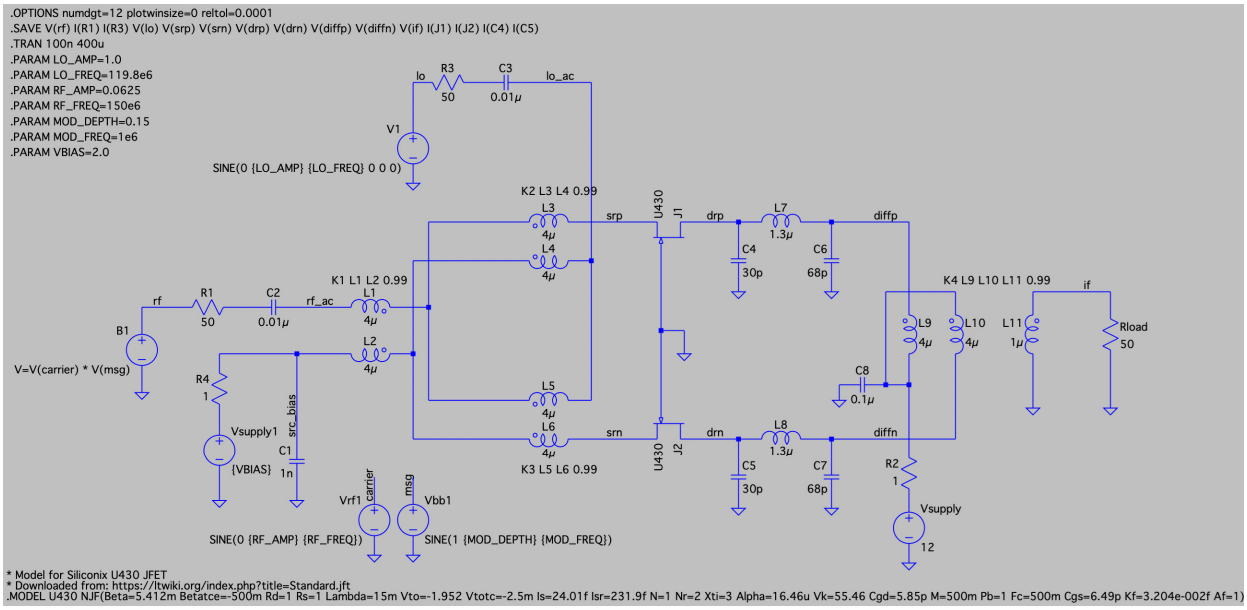


DEMAW-SIM-FIG. 7.20B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.20).

E. Simulation Results For an Input Signal Reduced by 24 dB

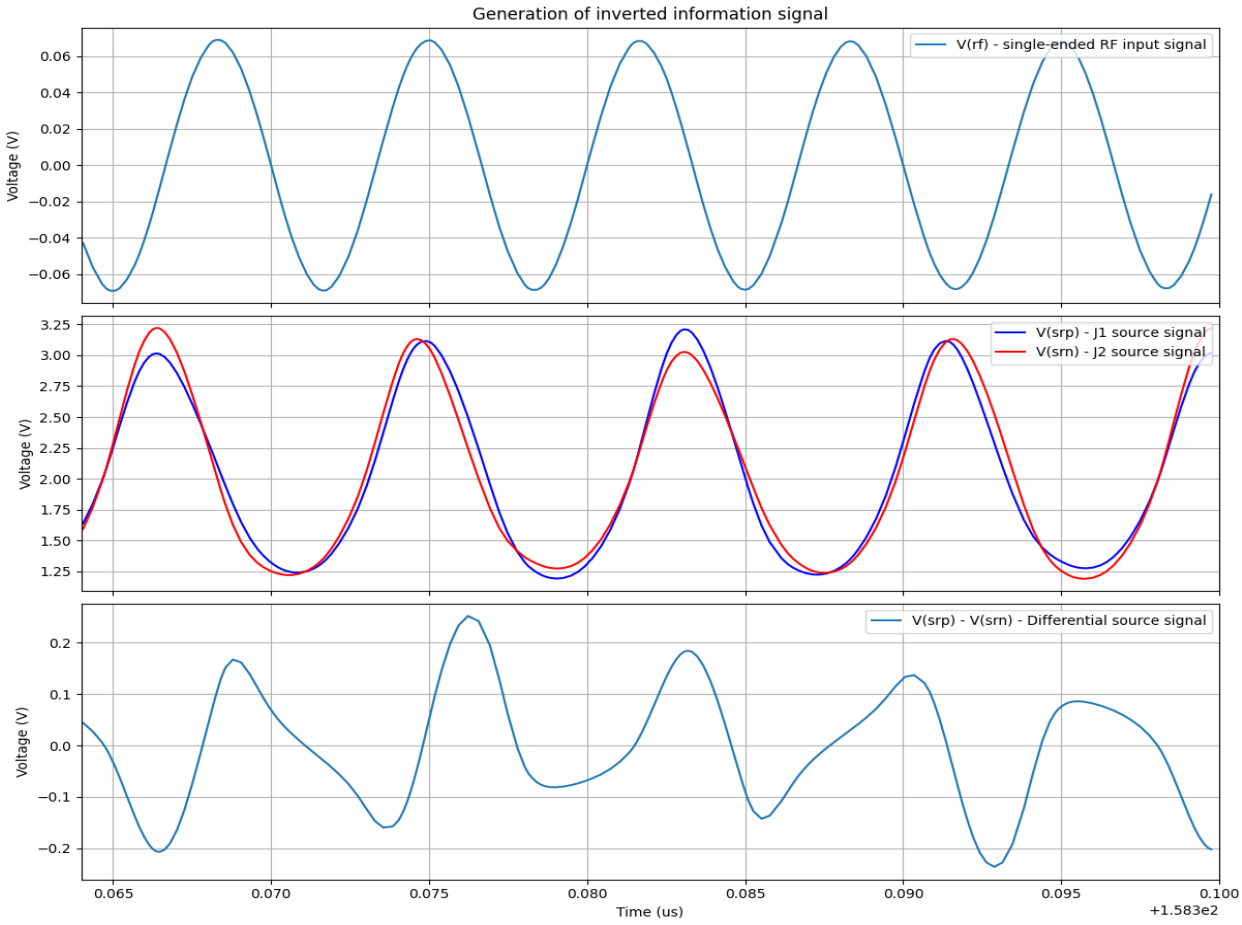
139. DEMAW-SIM-FIG. 1.21 is a schematic diagram of the simulated DeMaw FIG. 6.7circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 24 dB. I have created additional figures DEMAW-SIM-FIGS. 4.21, 5.21, 6.21, 7.21A and 7.21B based on simulation output from DEMAW-SIM-FIG. 1.21. DEMAW-SIM-FIGS. 4.21, 5.21, 6.21, 7.21A and 7.21B show the same simulation output from DEMAW-SIM-FIG. 1.21 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.21, 4.21, 5.21, 6.21, 7.21A and 7.21B.



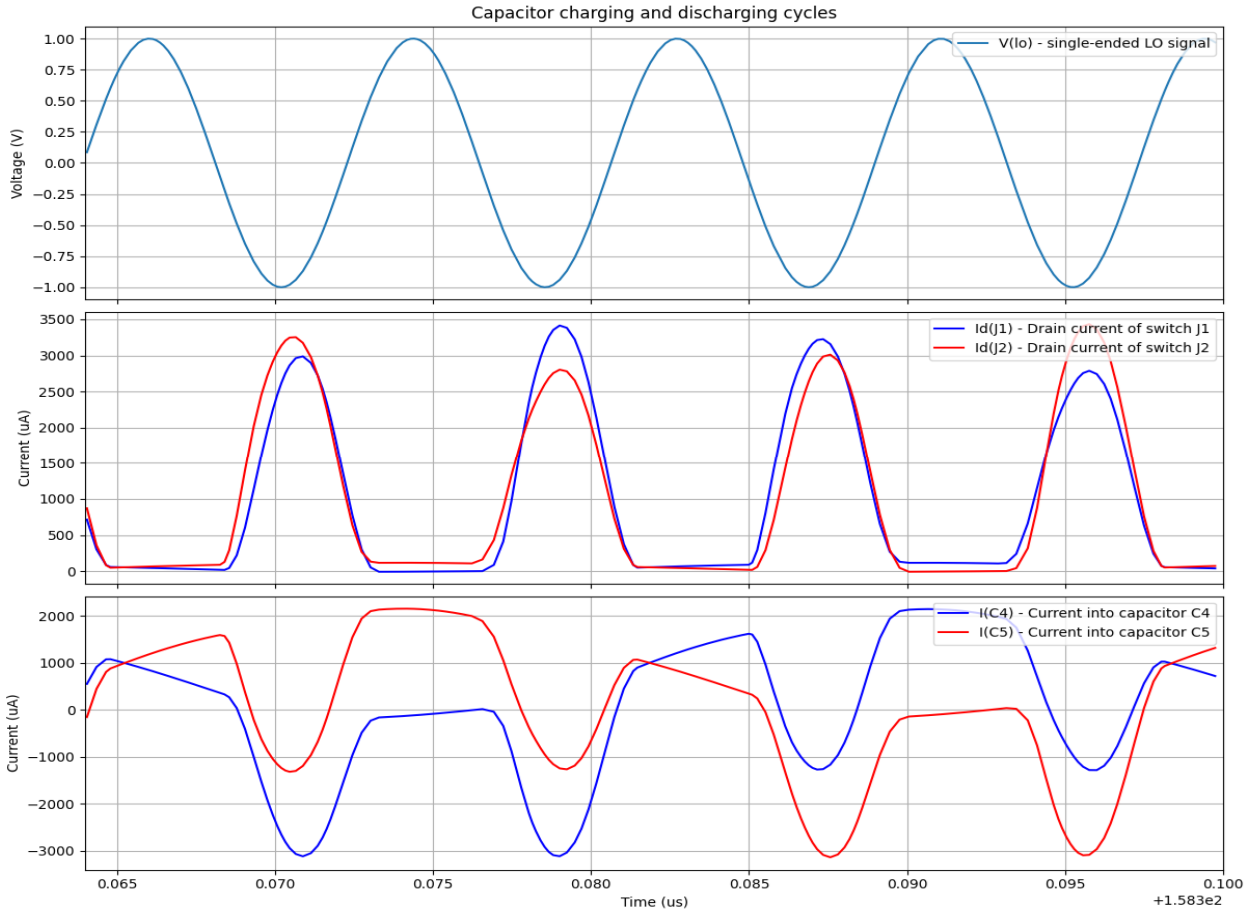
DEMAW-SIM-FIG. 1.21. DeMaw circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 24 dB.

140. DEMAW-SIM-FIG. 4.21 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.21.



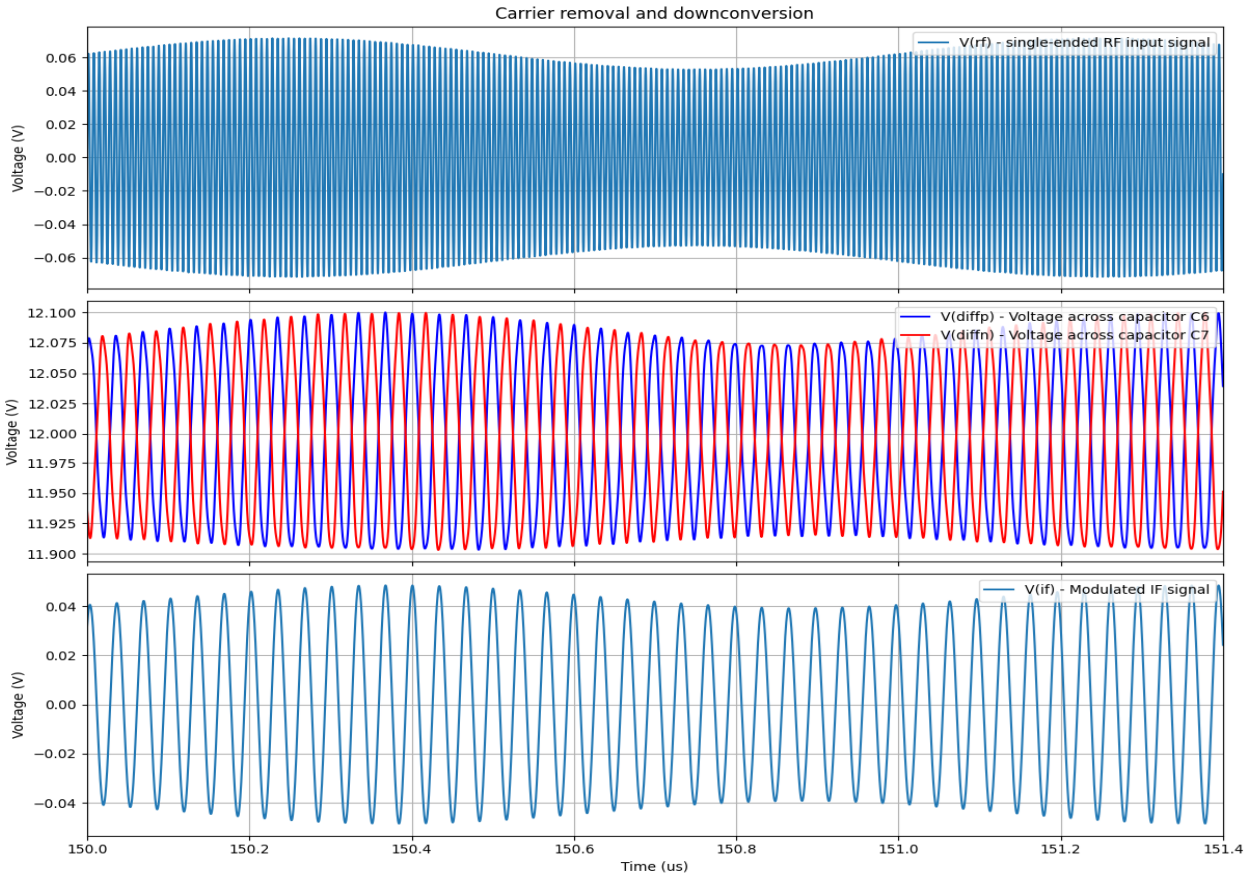
DEMAW-SIM-FIG. 4.21. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.21).

141. DEMAW-SIM-FIG. 5.21 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.21.



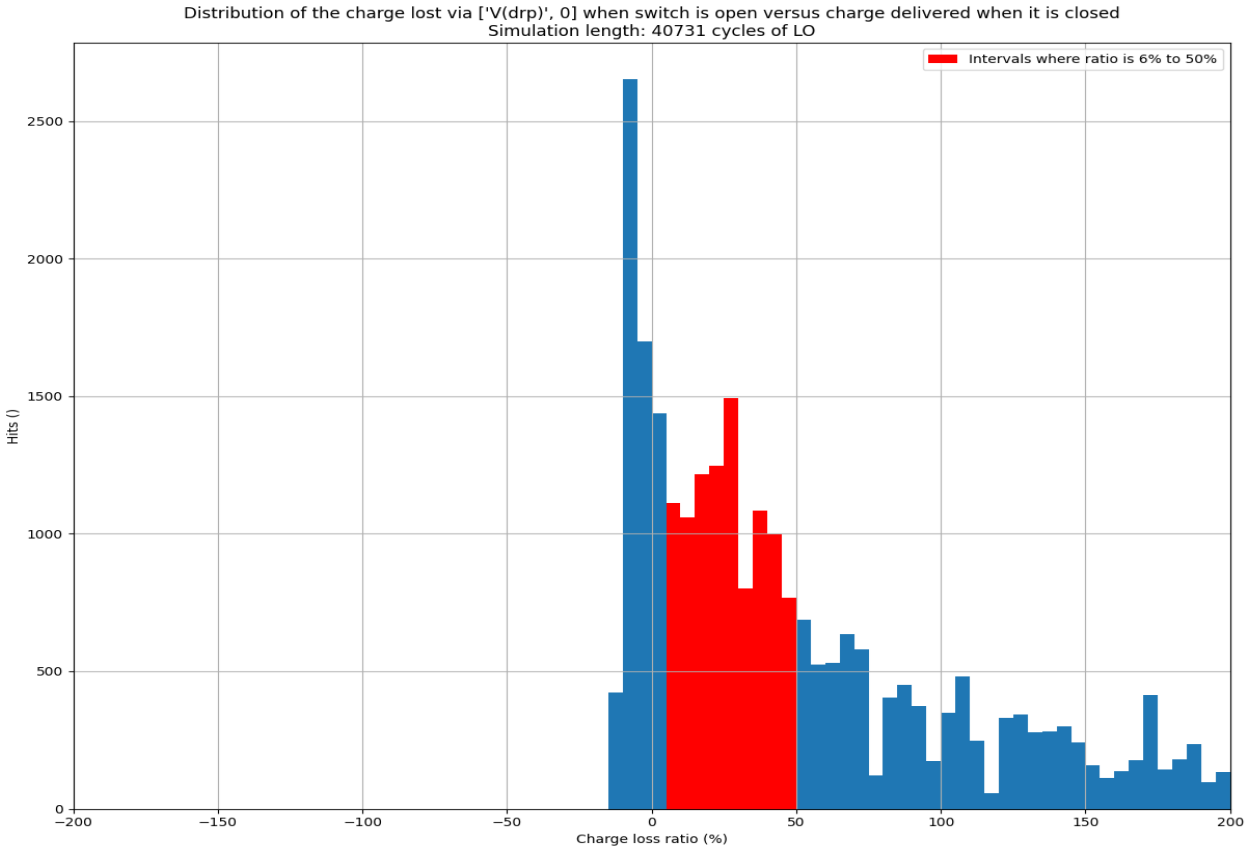
DEMAW-SIM-FIG. 5.21. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.21).

142. DEMAW-SIM-FIG. 6.21 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.21.



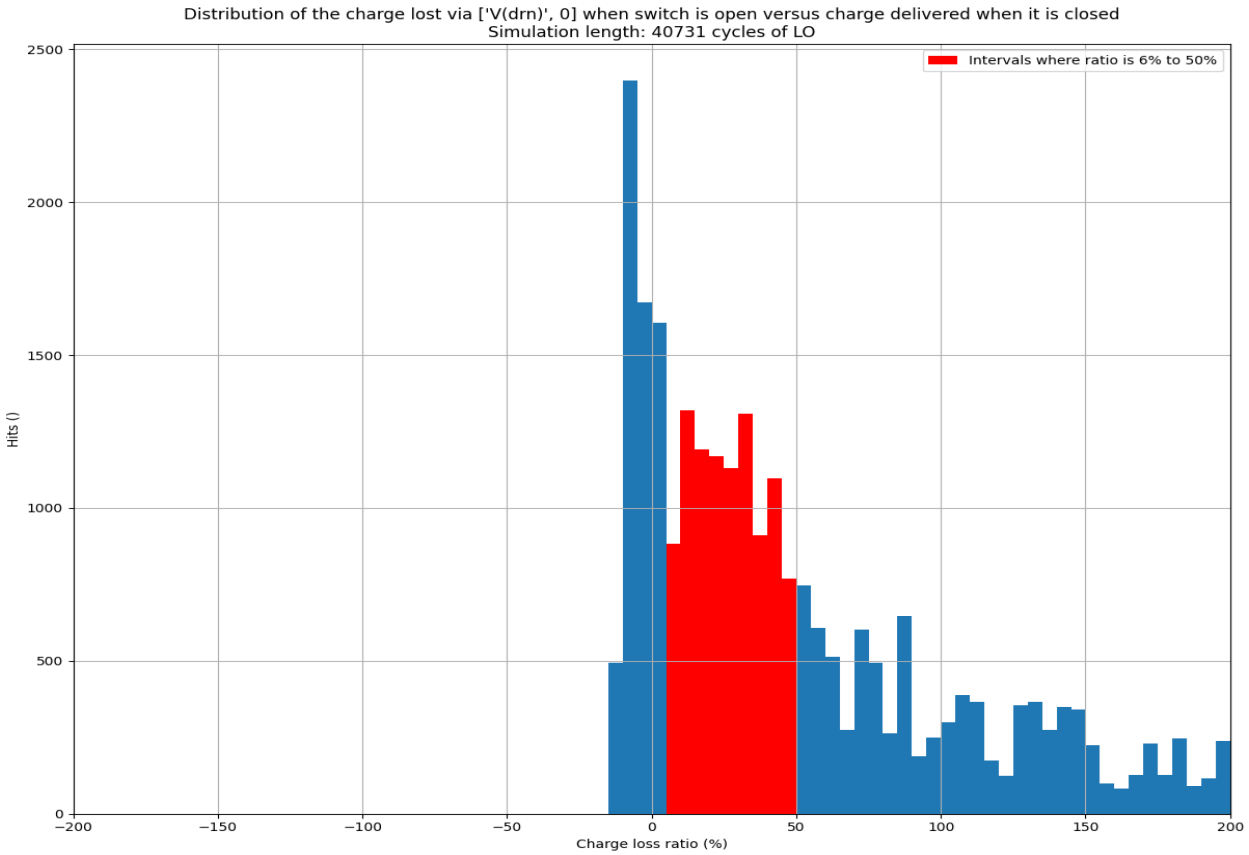
DEMAW-SIM-FIG. 6.21. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.21).

143. DEMAW-SIM-FIG. 7.21A is a histogram showing the charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.21.



DEMAW-SIM-FIG. 7.21A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.21).

144. DEMAW-SIM-FIG. 7.21B is a histogram showing the charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.21.



DEMAW-SIM-FIG. 7.21B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.21).

VII. Macnally Circuit Modified to Match That Presented in Macnally Patent

145. To further demonstrate that I have not chosen component values and circuit configurations to "get the results [that TI] needed" as alleged in the POPR, the simulation results presented in this section correspond to the mixer circuit presented in the Macnally patent with component values and an input signal that matches the information presented in the Macnally patent as closely as possible. These changes include:

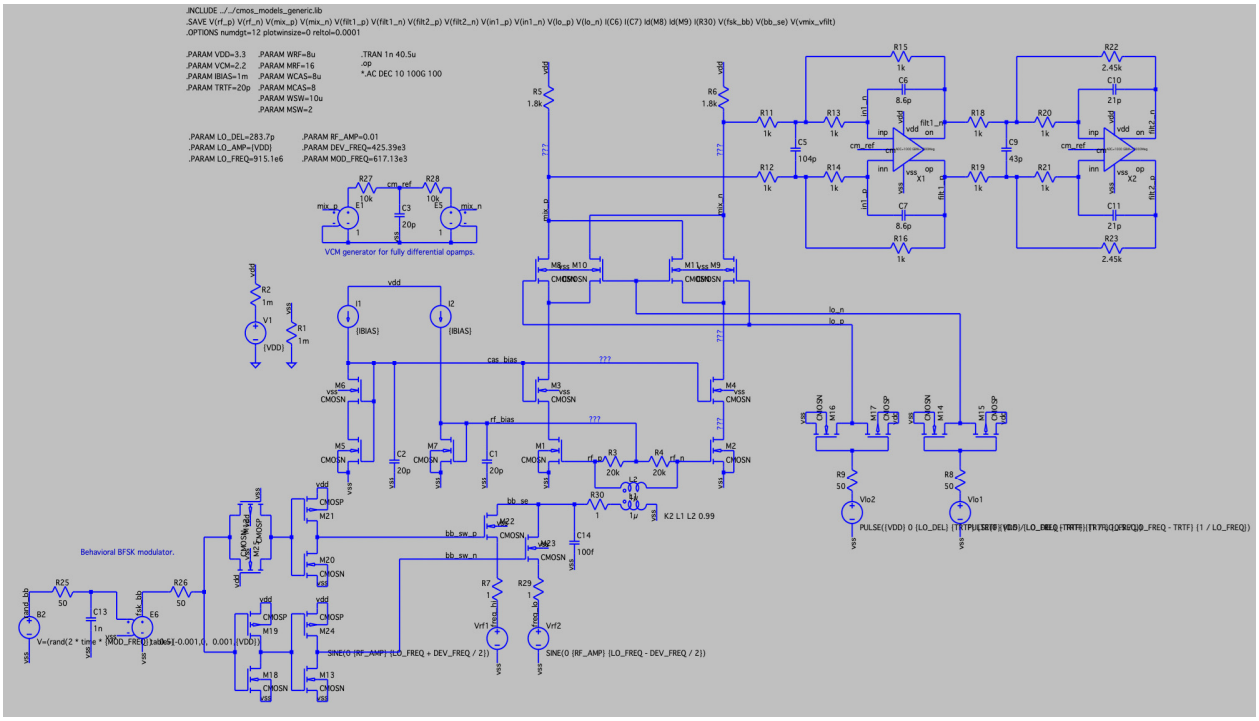
- Actual resistors are used to implement R3 and R4 in FIG. 3 of Macnally

(in contrast, the corresponding circuit described in my original Declaration used a combination of current sources and resistors to implement the effect of R3 and R4, which is common practice in circuit design).

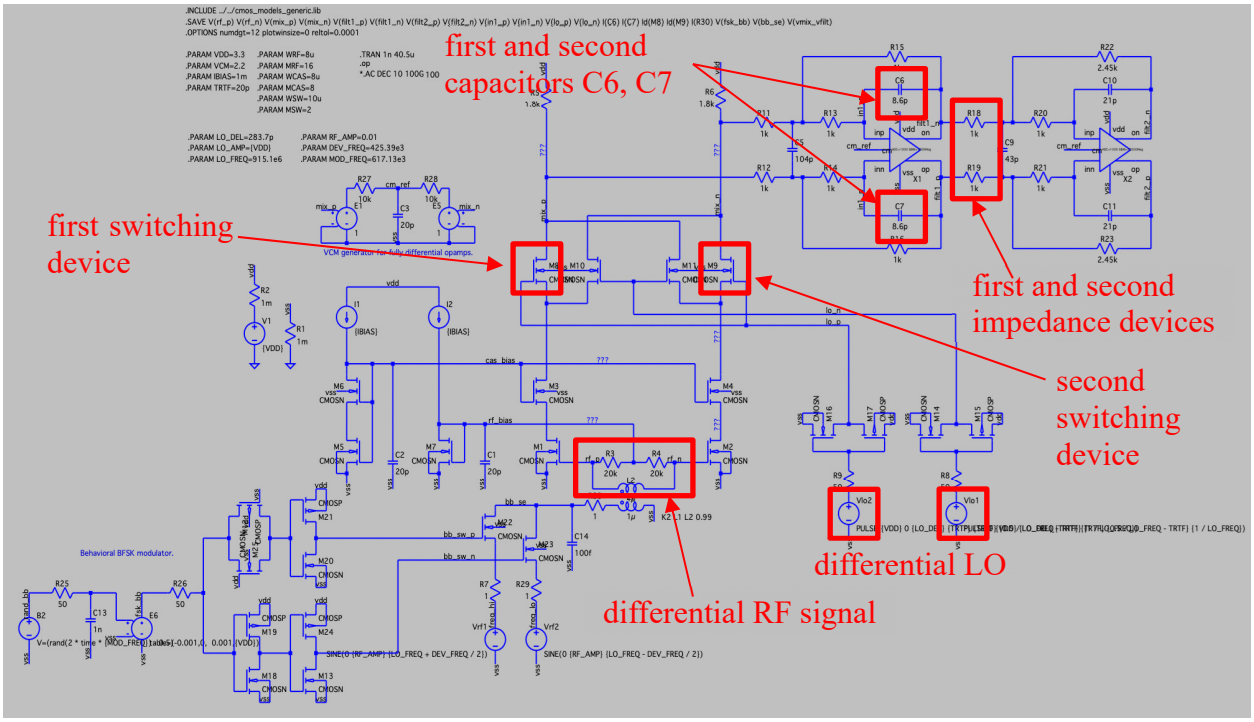
- The mixer gain was increased to that described in Macnally by changing the size and bias voltages of the M1 and M2 transistors shown in FIG. 3 of Macnally (to achieve the 8.5 mS of transconductance mentioned in Macnally), and adjusting the cross-over points of the pseudo-differential LO signals to prevent the mixer core transistors, i.e., M5, M6, M7, and M8 in FIG. 3 of Macnally, from cross-conducting.
- The RF input signal was changed to have BFSK modulation and a center frequency of 915 MHz to more closely match the application mentioned in Macnally.

146. MACNALLY-SIM-FIG. 1.1 depicts the simulation with the changes noted above. None of the changes cause differences in the simulated results that change the conclusions presented in my original Declaration regarding the alleged invention disclosed in the ’342 patent. I have created additional figures MACNALLY-SIM-FIGS. 2.1, 3.1, 4.1A and 4.1B based on simulation output from MACNALLY-SIM-FIG. 1.1. MACNALLY-SIM-FIGS. 2.1, 3.1, 4.1A and 4.1B show the same simulation output from MACNALLY-SIM-FIG. 1.1 as

MACNALLY-SIM-FIGS. 2, 3, 4, 5 and 6 show from MACNALLY-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on MACNALLY-SIM-FIGS 1-5 are likewise supported by MACNALLY-SIM-FIGS. 1.1, 2.1, 3.1, 4.1A and 4.1B.

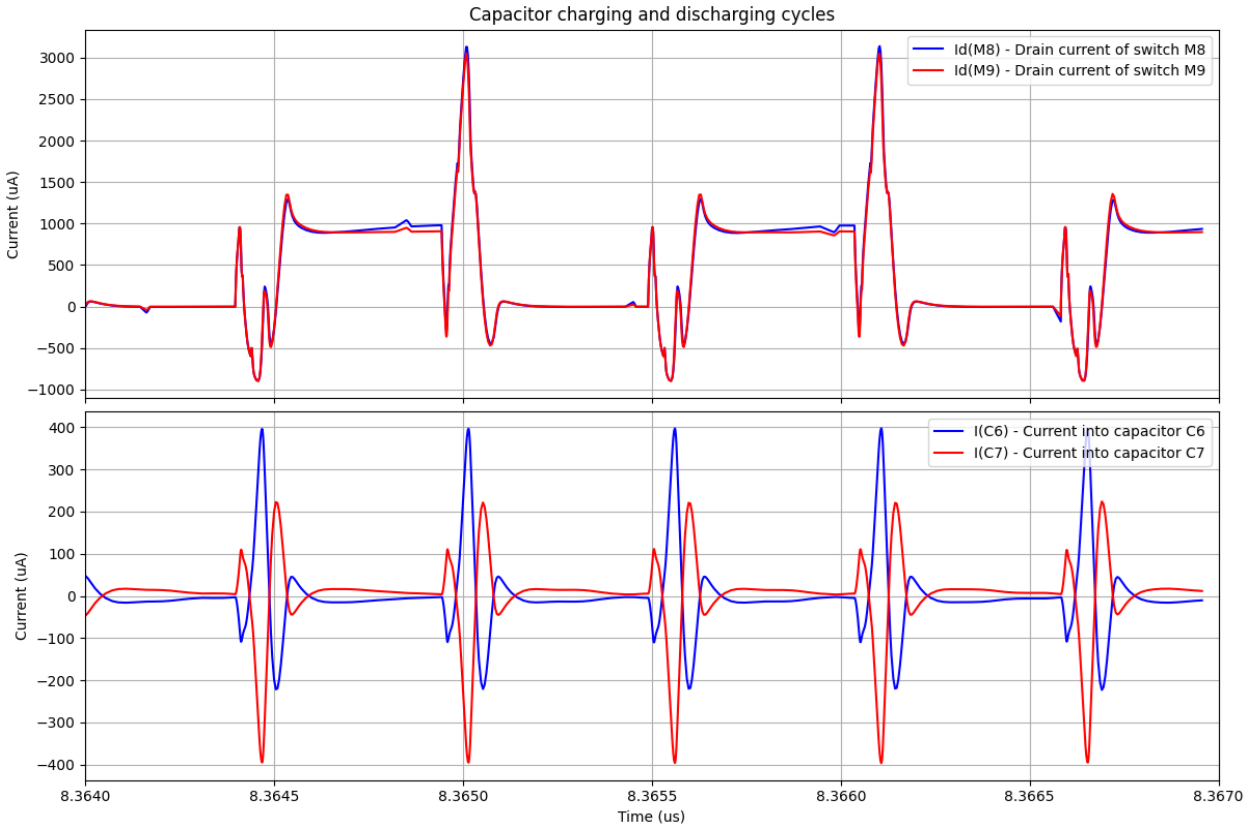


MACNALLY-SIM-FIG. 1.1 (clean). Macnally circuit simulation.



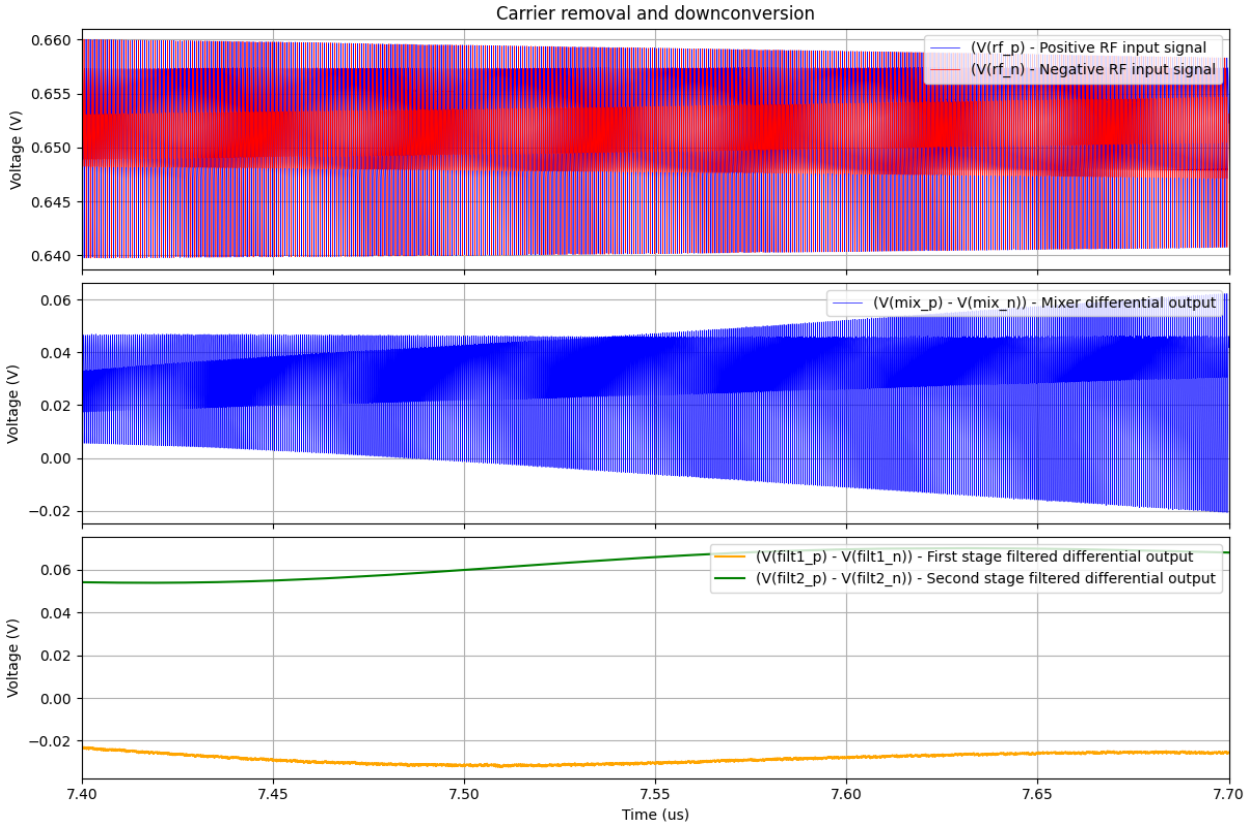
MACNALLY-SIM-FIG. 1.1 (annotated). Macnally circuit simulation.

147. MACNALLY-SIM-FIG. 2.1 is a graphical representation illustrating the charging and discharging cycles for capacitors C6 and C7 in the circuit of MACNALLY-SIM-FIG. 1.1.



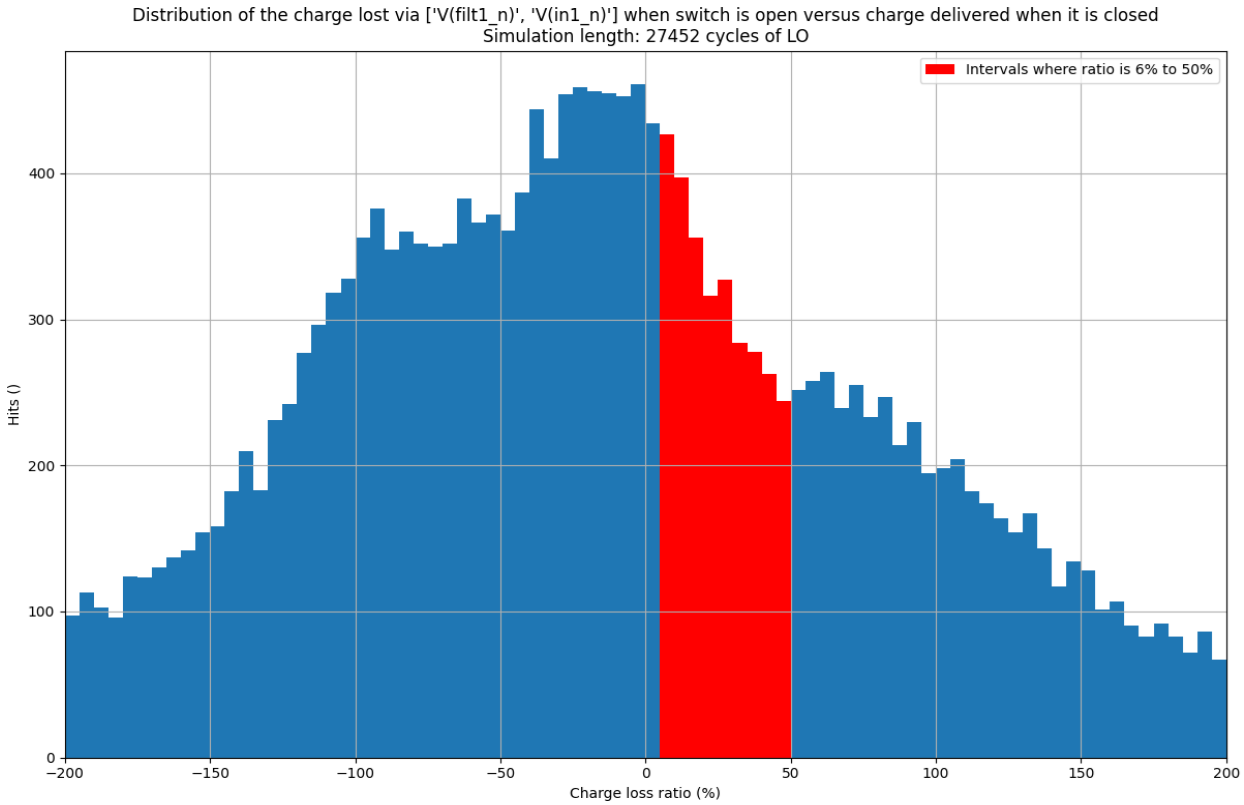
MACNALLY-SIM-FIG. 2.1. Capacitor charging and discharging cycles (circuit of MACNALLY-SIM-FIG. 1.1).

148. MACNALLY-SIM-FIG. 3.1 is a graphical representation of carrier removal and down-conversion for the circuit of MACNALLY-SIM-FIG. 1.1. MACNALLY-SIM-FIGS. 3 and 5 in the original Declaration include graphs from MACNALLY-SIM-FIG. 6. MACNALLY-SIM-FIG. 3.1 includes the same three types of graphs in MACNALLY-SIM-FIG. 6, but based on simulation output from MACNALLY-SIM-1.1.



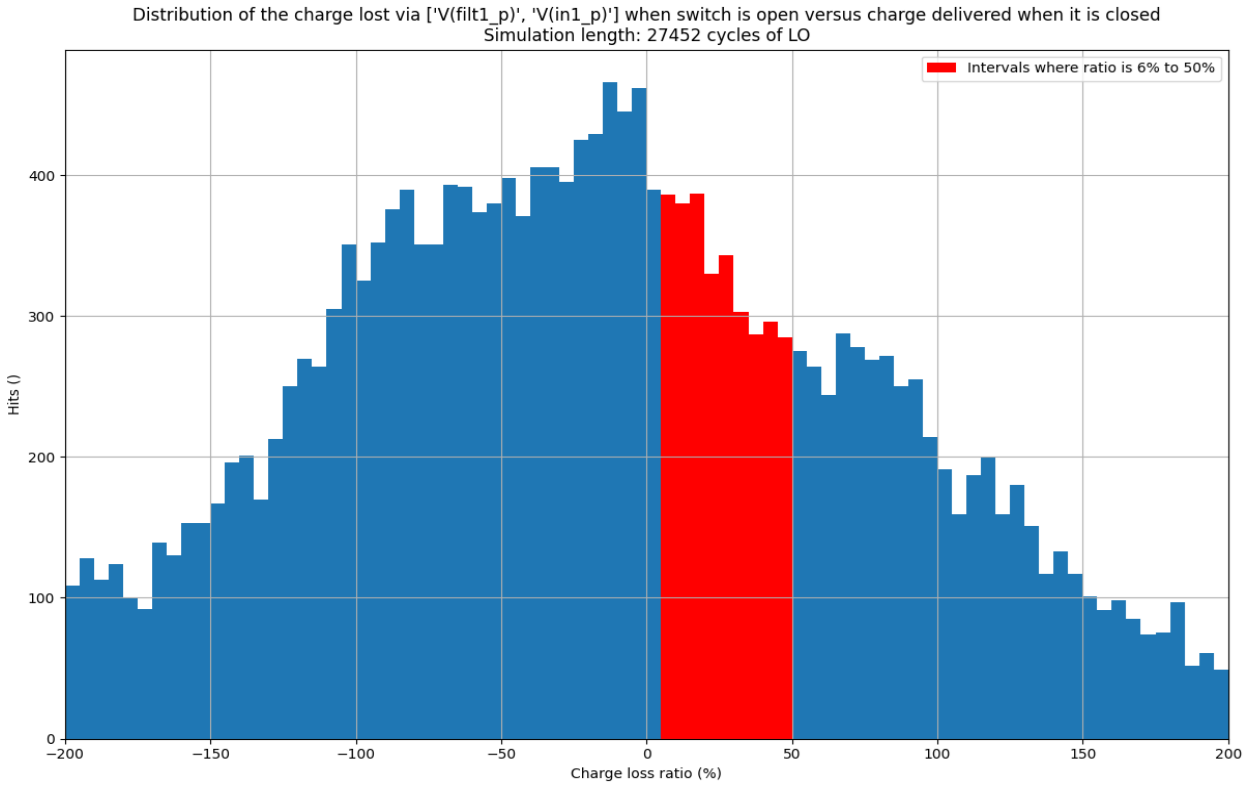
MACNALLY-SIM-FIG. 3.1. Carrier removal and down-conversion (circuit of MACNALLY-SIM-FIG. 1.1).

149. I my original Declaration, I provided one histogram of the charge loss ratio percentages that was representative of capacitors C6 and C7 (MACNALLY-SIM-FIG. 4). I have generated two histograms here; one for each capacitor MACNALLY-SIM-FIG. 4A and 4B. Everything I wrote in my original Declaration about MACNALLY-SIM-FIG. 4 is true of MACNALLY-SIM-FIG. 4A and 4B. MACNALLY-SIM-FIG. 4.1A is a histogram showing the charge loss ratio percentages for capacitor C6 for the circuit of MACNALLY-SIM-FIG. 1.1.



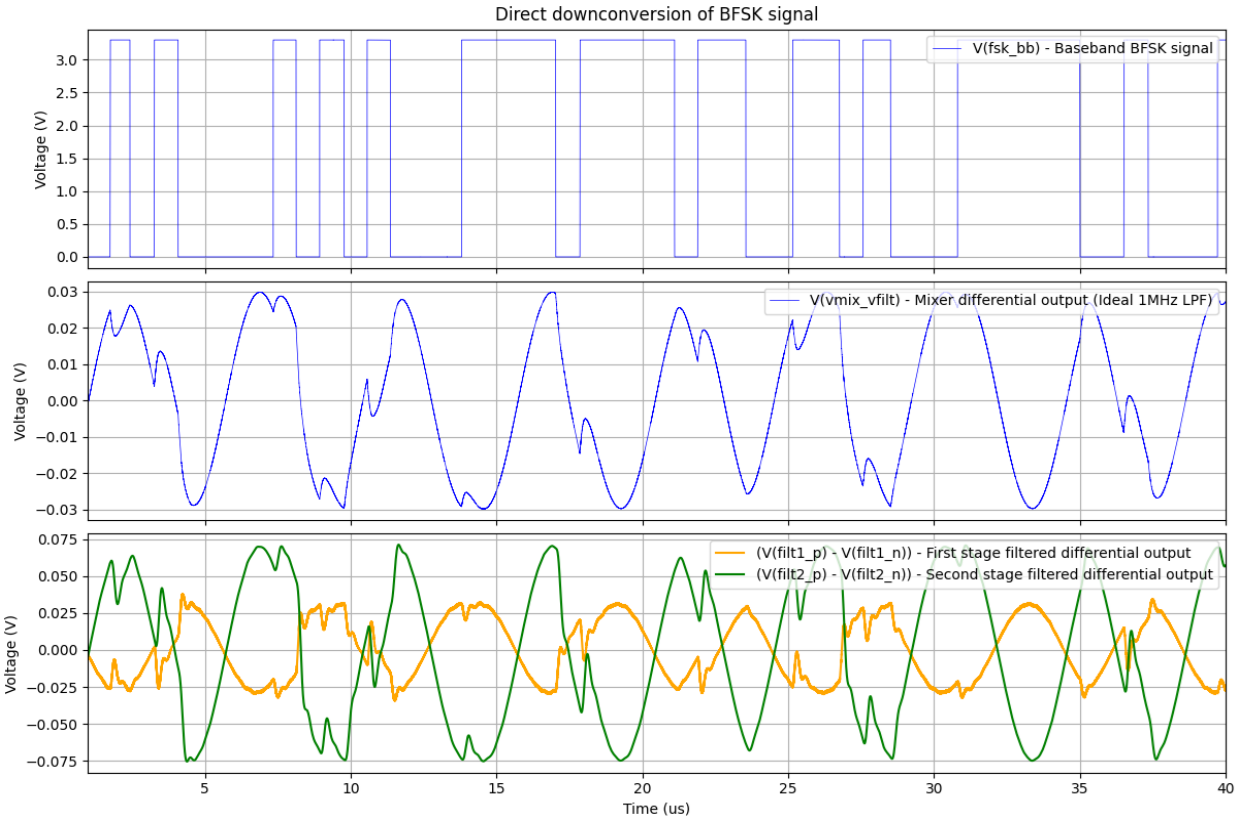
MACNALLY-SIM-FIG. 4.1A. Charge loss ratio percentages histogram for capacitor C6 (circuit of MACNALLY-SIM-FIG. 1.1).

150. MACNALLY-SIM-FIG. 4.1B is a histogram of the charge loss ratio percentages for capacitor C7 for the circuit of MACNALLY-SIM-FIG. 1.1.



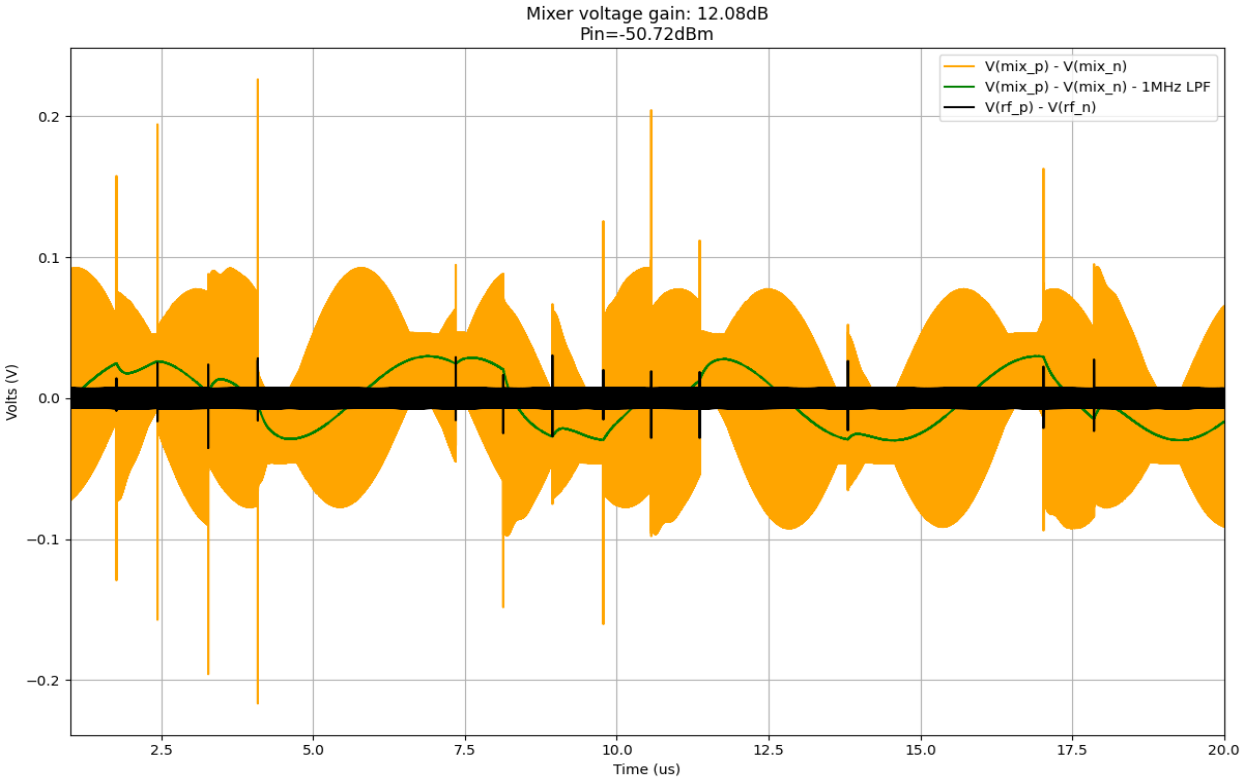
MACNALLY-SIM-FIG. 4.1B. Charge loss ratio percentages histogram for capacitor C7 (circuit of MACNALLY-SIM-FIG. 1.1).

151. MACNALLY-SIM-7.1 is a graphical representation of the generation of inverted information signal for the circuit of MACNALLY-SIM-FIG. 1.1.



MACNALLY-SIM-FIG. 7.1. Generation of inverted information signal (circuit of MACNALLY-SIM-FIG. 1.1).

152. MACNALLY-SIM-FIG. 8 is a graphical illustration of waveforms that demonstrate mixer gain of the circuit of MACNALLY-SIM-FIG. 1.1.



MACNALLY-SIM-FIG. 8. Waveforms which demonstrate mixer gain (circuit of MACNALLY-SIM-FIG. 1.1)

VIII. Changes to Simulator Settings and Post-Processing

A. Changes to Simulator Settings and Post-Processing Relative to Original Declaration

153. For each of the simulations provided above, the accuracy of the simulation results has been increased from those provided in the original Declaration by changing the default LTspice accuracy settings and by changes to the post-processing Python script. The changes to the default LTspice accuracy settings are as follows:

- The reltol parameter was tightened from the default value of 1e-3 to 1e-4.

- The numdgt parameter was increased from the default value of 6 significant digits to 12 significant digits. This does not affect the simulator's internal precision, but it increases the number of significant digits used when exporting waveform data to text files.
- The plotwinsize parameter was set to zero. By default, LTspice applies a post-processing step to the simulated waveforms before exporting data to a file. The goal of this post-processing is to reduce data file size by selectively discarding data points according to LTspice's algorithm, at the expense of waveform accuracy. By setting this parameter to 0, we have disabled the post-processing, ensuring maximum accuracy.

154. The accuracy of the simulation results was further increased by changing how charge integration is calculated during Python script postprocessing. In the original Python script, capacitor charge delivered over a time interval was computed by numerically integrating the capacitor current waveforms. Any numerical integration of the data is subject to the accumulation of rounding errors. Thus, rather than numerically integrating the capacitor current over a time interval, the modified Python script uses the difference between the capacitor voltage at the end and the start of the time interval, which are related by the integral of the capacitor equation, I=CdV/dt. This is more precise, especially for Macnally, which has much sharper current waveforms. The changes in the modified Python script had little

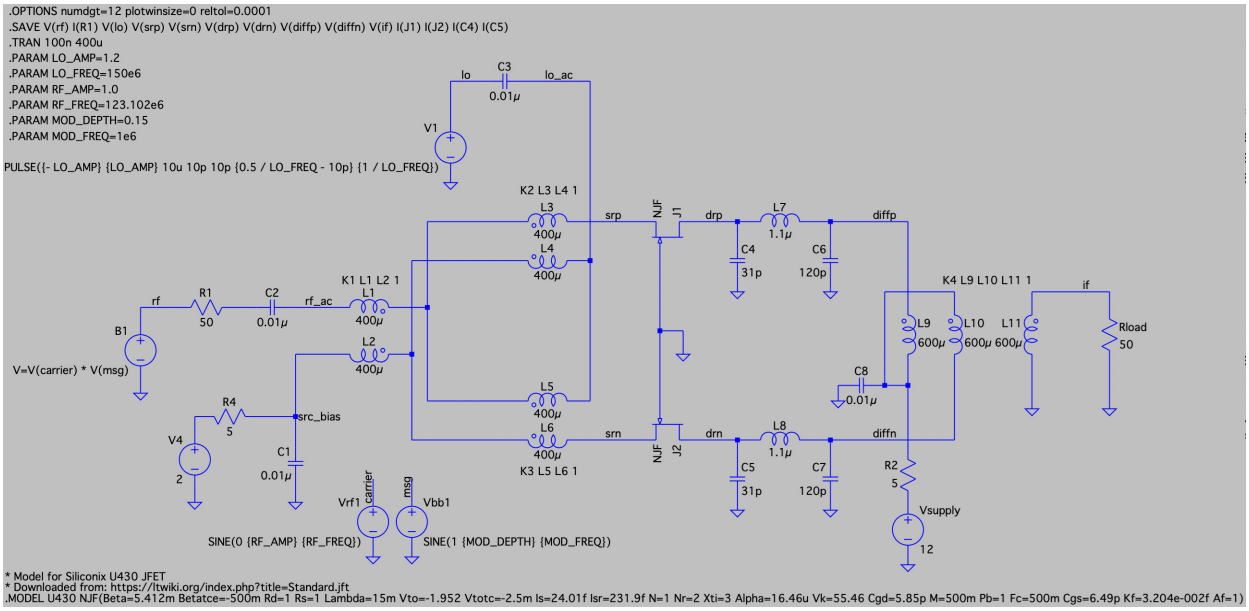
effect on the DeMaw simulations, and in neither case did it lead to different conclusions than were presented in the original Declaration.

155. A bug was found in the original Python script used to post-process the simulation results from the Macnally circuit (there was no corresponding bug for the DeMaw circuit simulations) in the original Declaration. Specifically, for only the MacNally histograms, the computed charge removed from the capacitors while the switch is off was accidentally sign-flipped. As a result, the percentage range plotted [0, 200] corresponds to the range [0, -200]. This bug has been corrected.

156. None of the differences described above change the conclusions presented in my original Declaration. To demonstrate this point, the remainder of this section presents simulation results from my original Declaration juxtaposed with the same results except using the LTspice parameter and Python script changes described above.

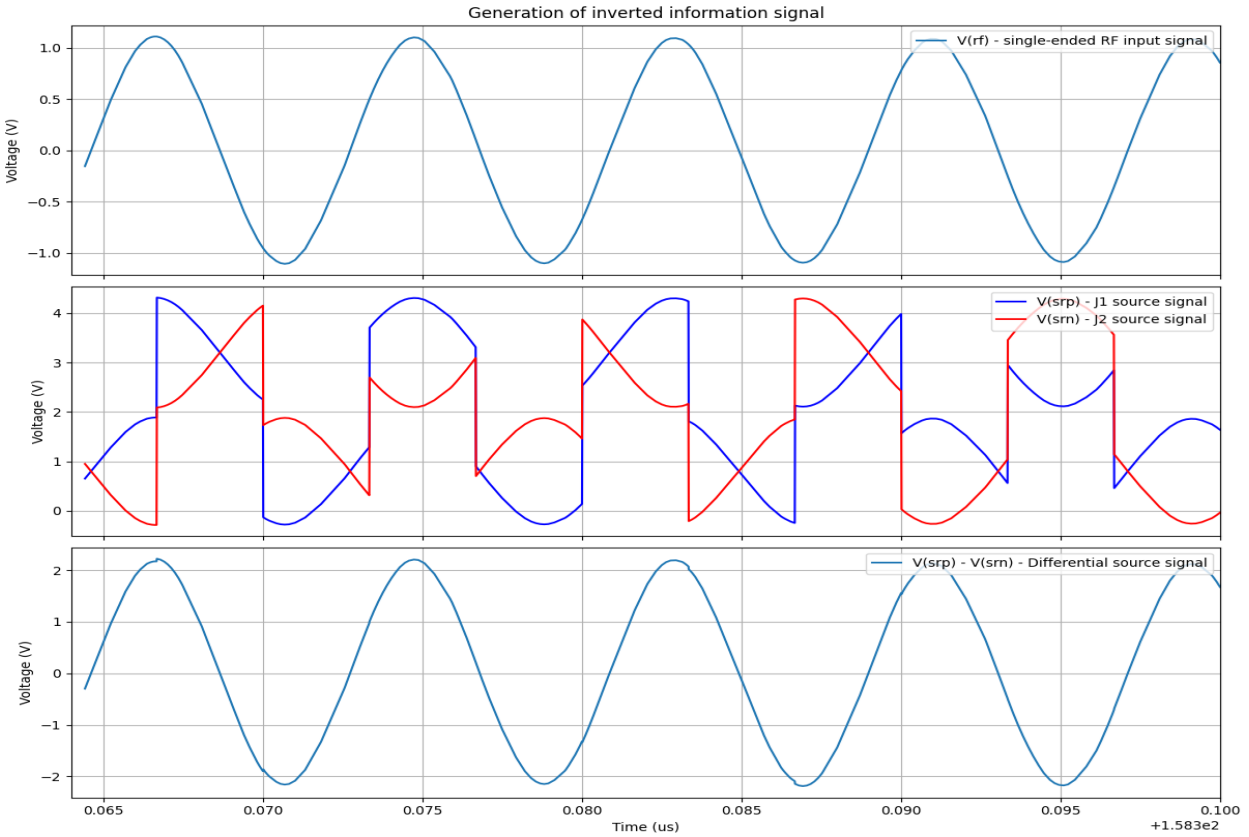
B. Original DeMaw Simulation With/Without Revised Simulator Settings and Post-Processing

157. DEMAW-SIM-FIG. 1 (different settings) is a schematic diagram of the simulated DeMaw circuit from the original Declaration with revised simulator accuracy settings. DEMAW-SIM-FIG. 1 (different settings) maintains the default, generic LTspice JFET models.



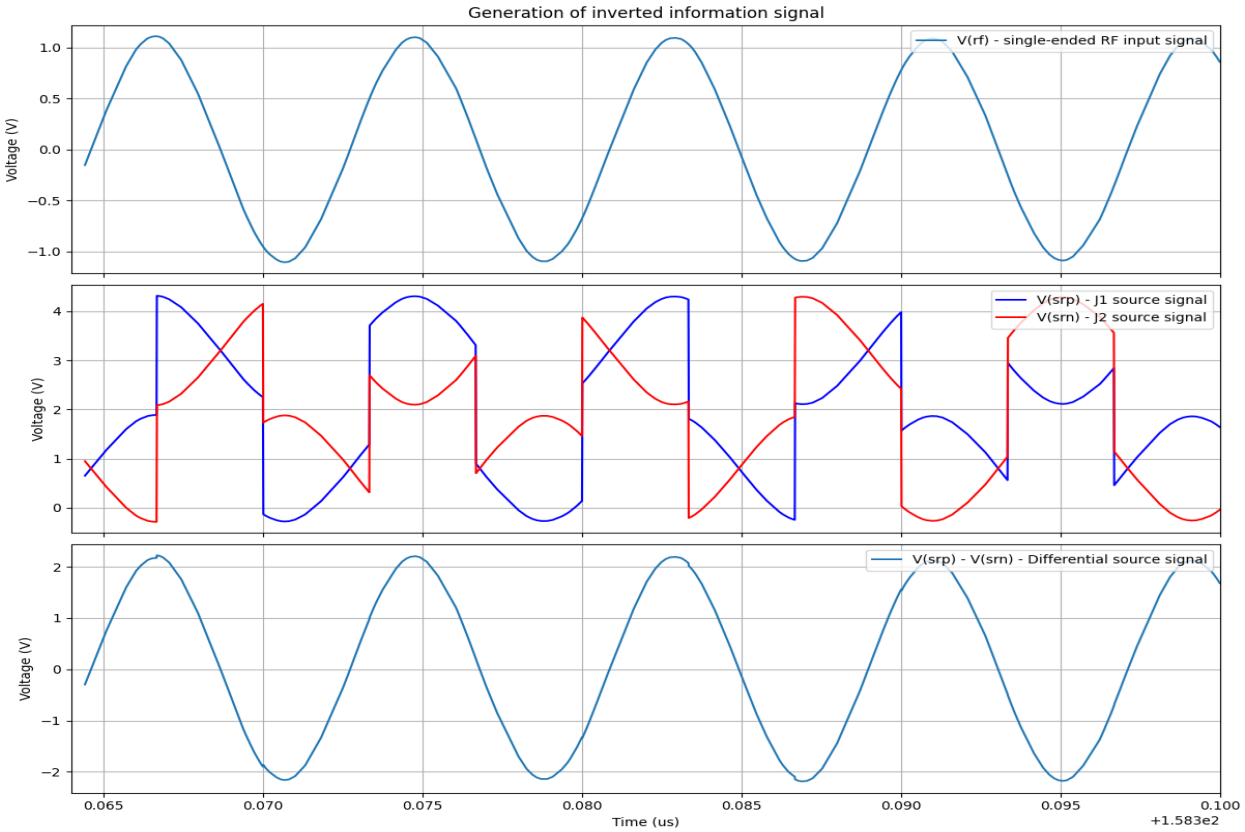
DEMAW-SIM-FIG. 1 (different sim settings) is a schematic diagram of the simulated DeMaw circuit from the original Declaration with revised simulator accuracy settings.

158. DEMAW-SIM-FIG. 4 is a graphical representation of the generation of inverted information signal for the DeMaw circuit from the original Declaration, further including the V(rf) and V(srp)-V(sm) graphs generated for DEMAW-SIM-FIG. 1.



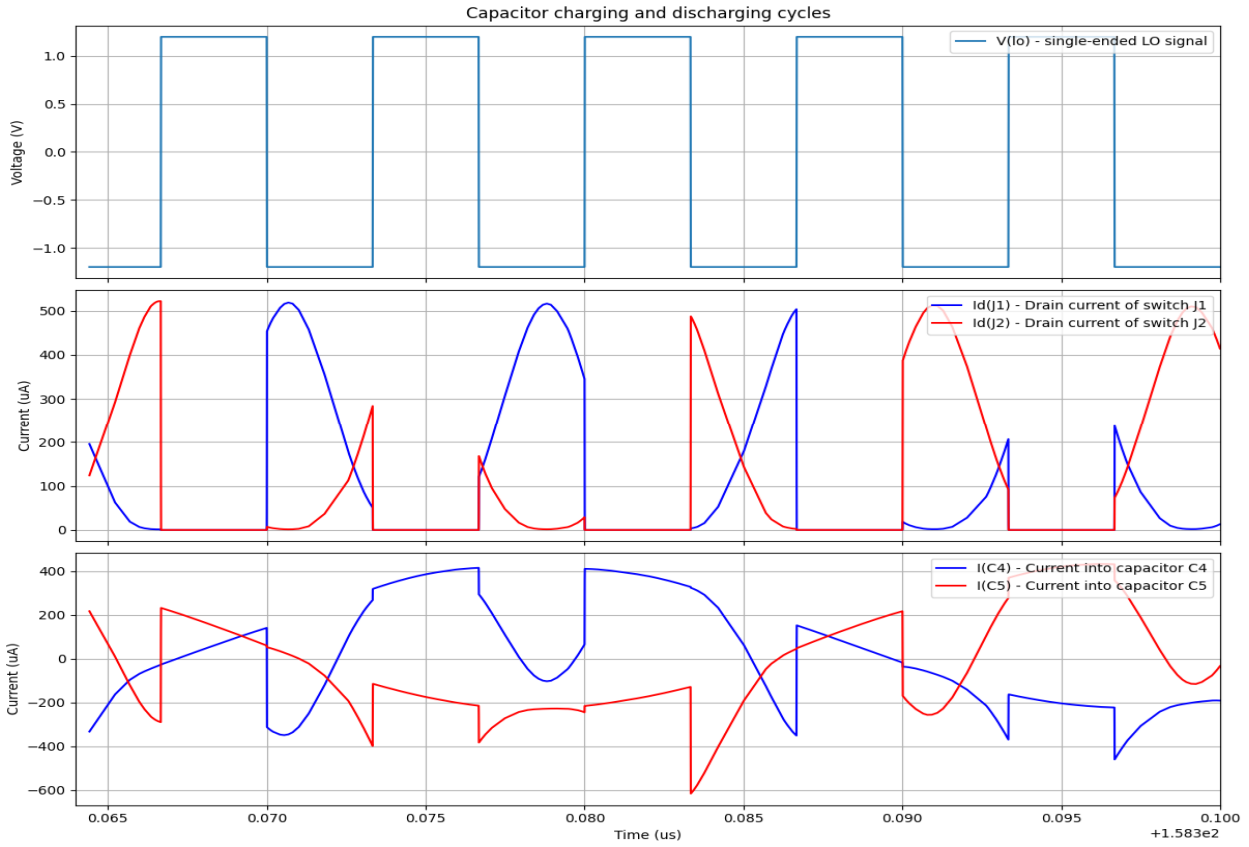
DEMAW-SIM-FIG. 4. Generation of inverted information signal (DeMaw circuit from the original Declaration).

159. DEMAW-SIM-FIG. 4 (different sim settings) is a graphical representation showing the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1 (different sim settings).



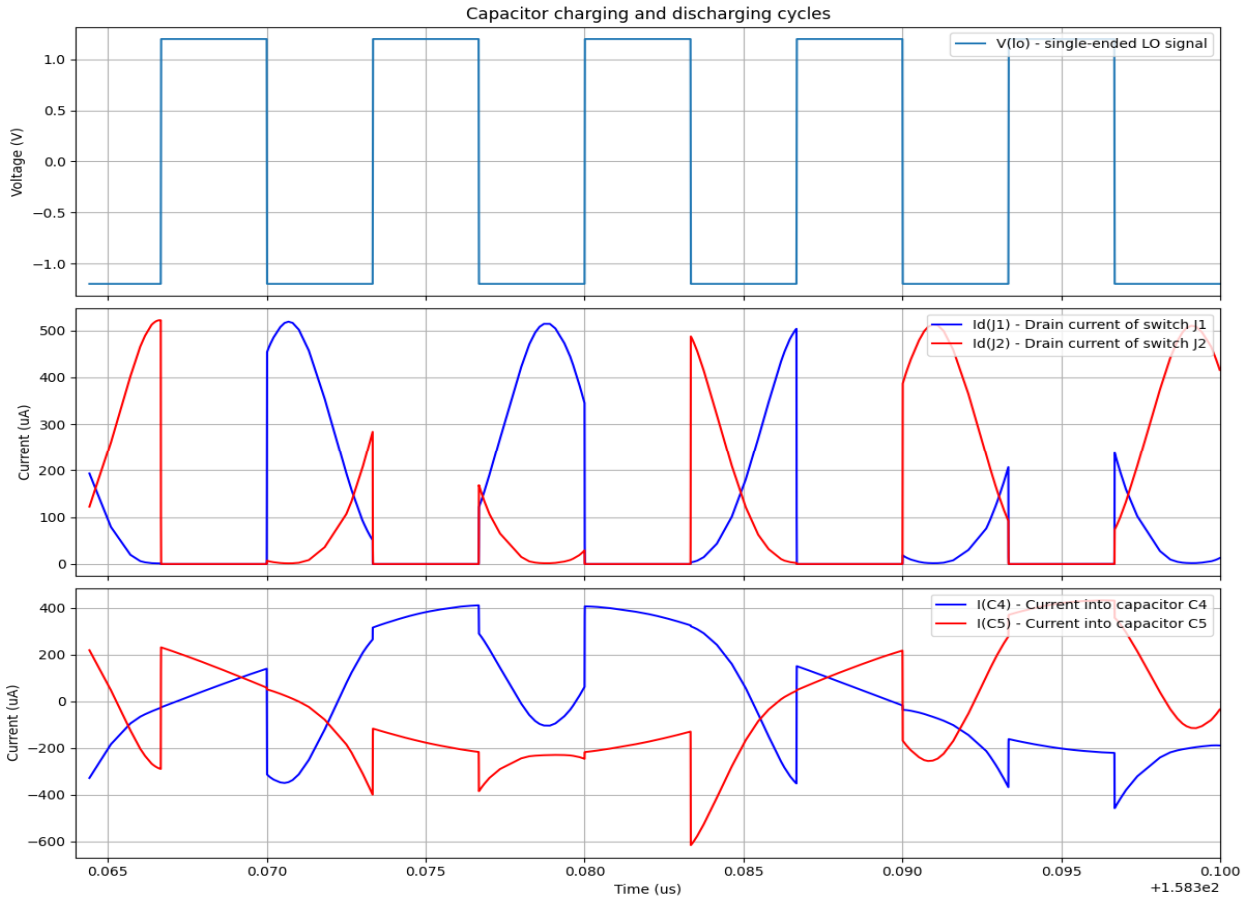
DEMAW-SIM-FIG. 4 (different sim settings). Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1(different sim settings)).

160. DEMAW-SIM-FIG. 5 is a graphical representation illustrating the charging and discharging cycles for capacitors C4 and C5 in the DeMaw circuit from the original Declaration.



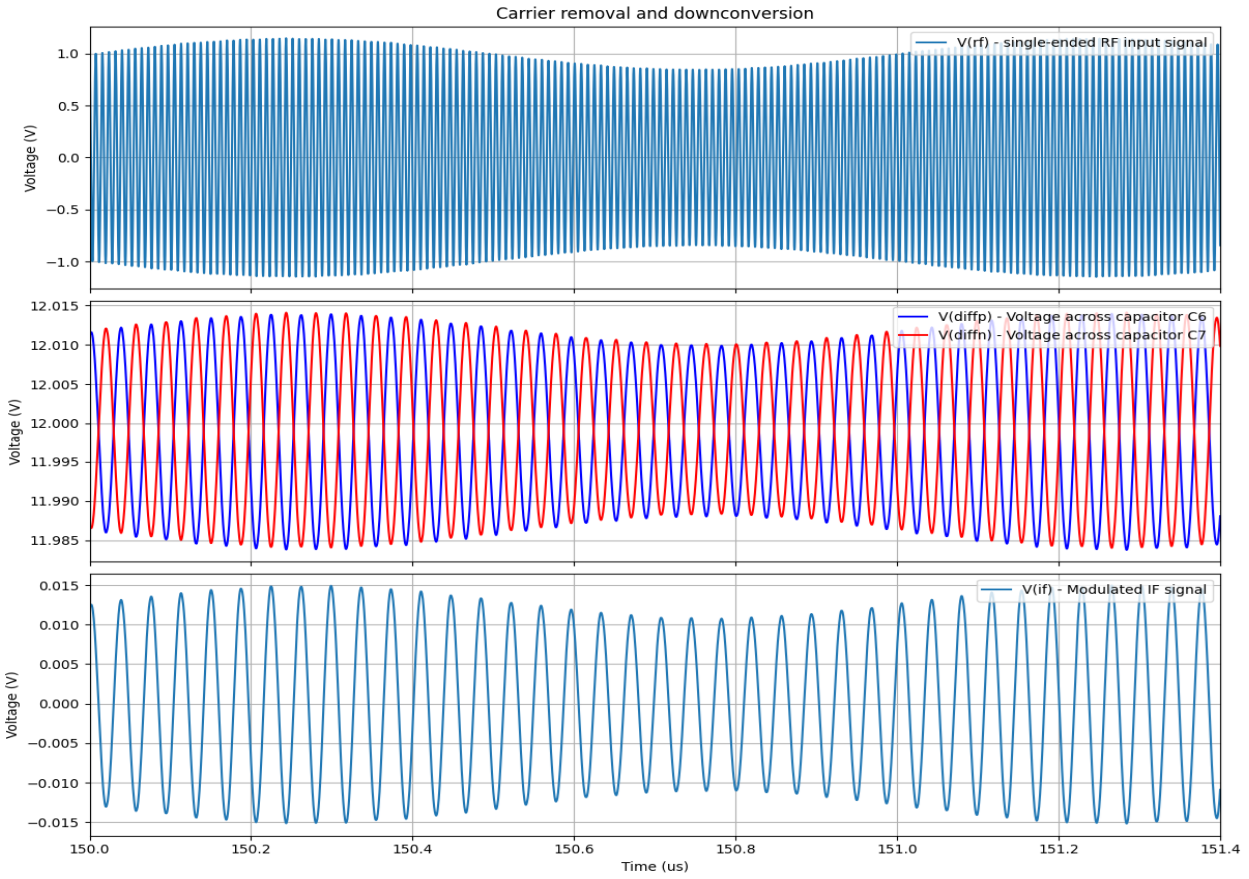
DEMAW-SIM-FIG. 5. Capacitor charging and discharging cycles (DeMaw circuit from the original Declaration).

161. DEMAW-SIM-FIG. 5 (different sim settings) is a graphical representation illustrating the charging and discharging cycles for capacitors C4 and C5 in the circuit of DEMAW-SIM-FIG. 1 (different sim settings).



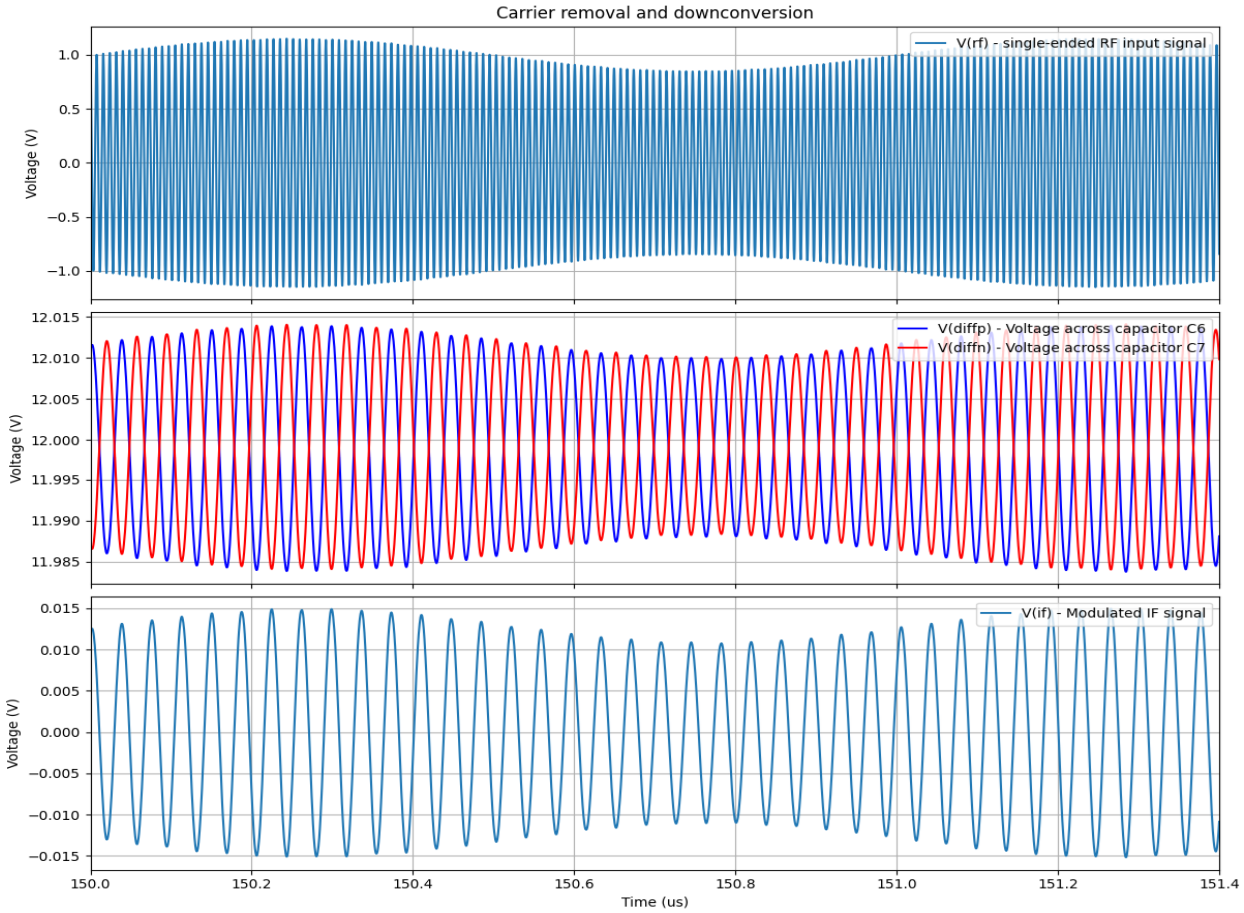
DEMAW-SIM-FIG. 5 (different sim settings). Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1 (different sim settings)).

162. DEMAW-SIM-FIG. 6 is a graphical representation of carrier removal and down-conversion for the DeMaw circuit from the original Declaration.



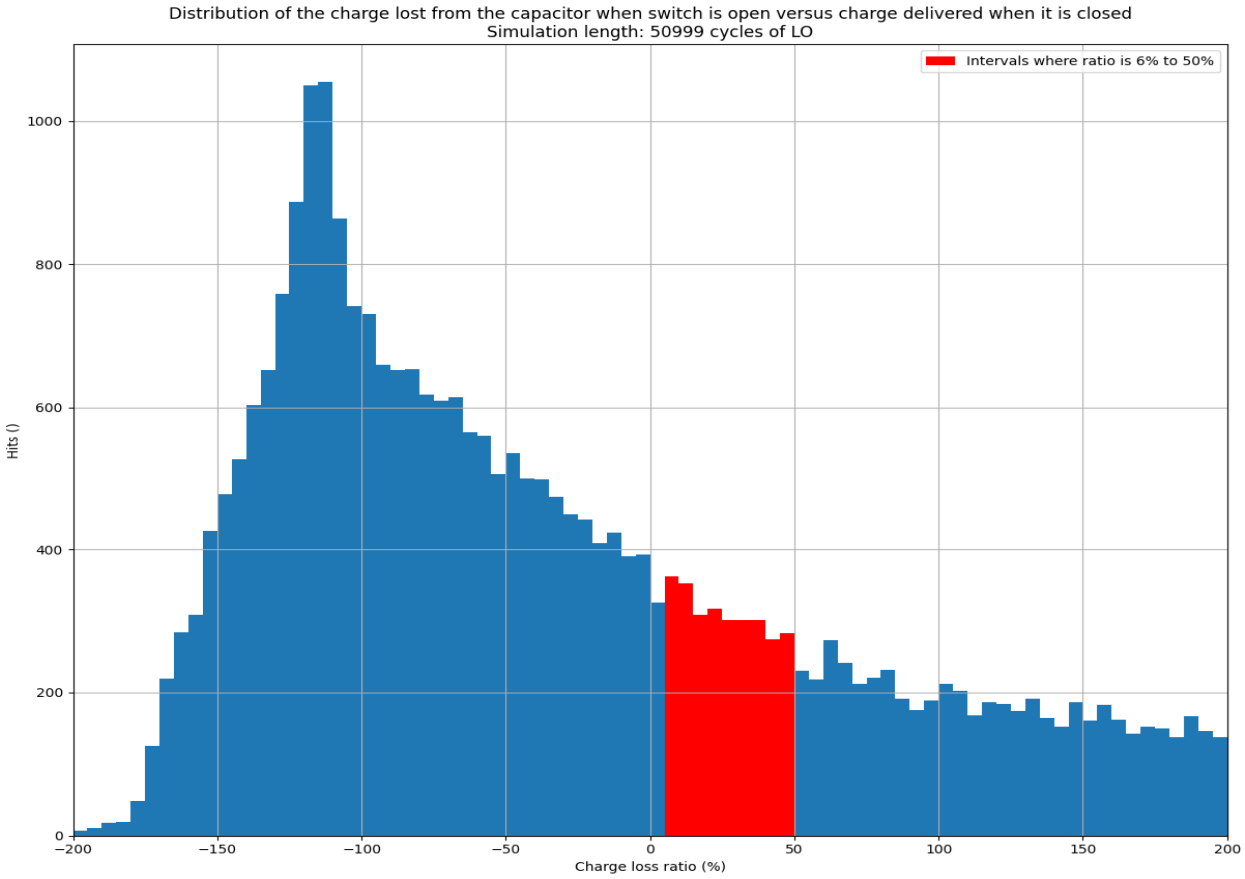
DEMAW-SIM-FIG. 6. Carrier removal and down-conversion (DeMaw circuit from the original Declaration).

163. DEMAW-SIM-FIG. 6 (different sim settings) is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1 (different sim settings).



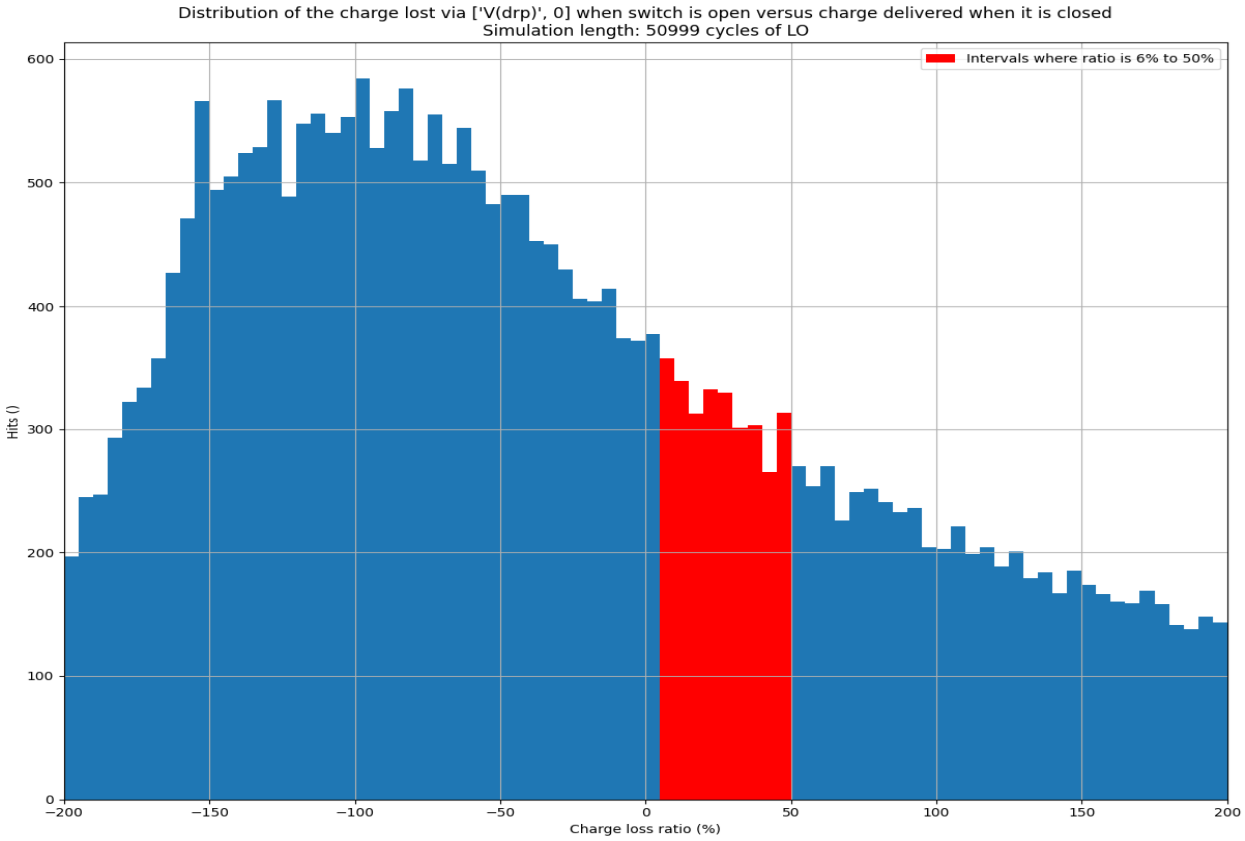
DEMAW-SIM-FIG. 6 (different sim settings). Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1 (different sim settings)).

164. DEMAW-SIM-FIG. 7 is a histogram of the charge loss ratio percentages for capacitor C4 for the DeMaw circuit from the original Declaration.



DEMAW-SIM-FIG. 7. Charge loss ratio percentages histogram for capacitor C4 (DeMaw circuit from the original Declaration).

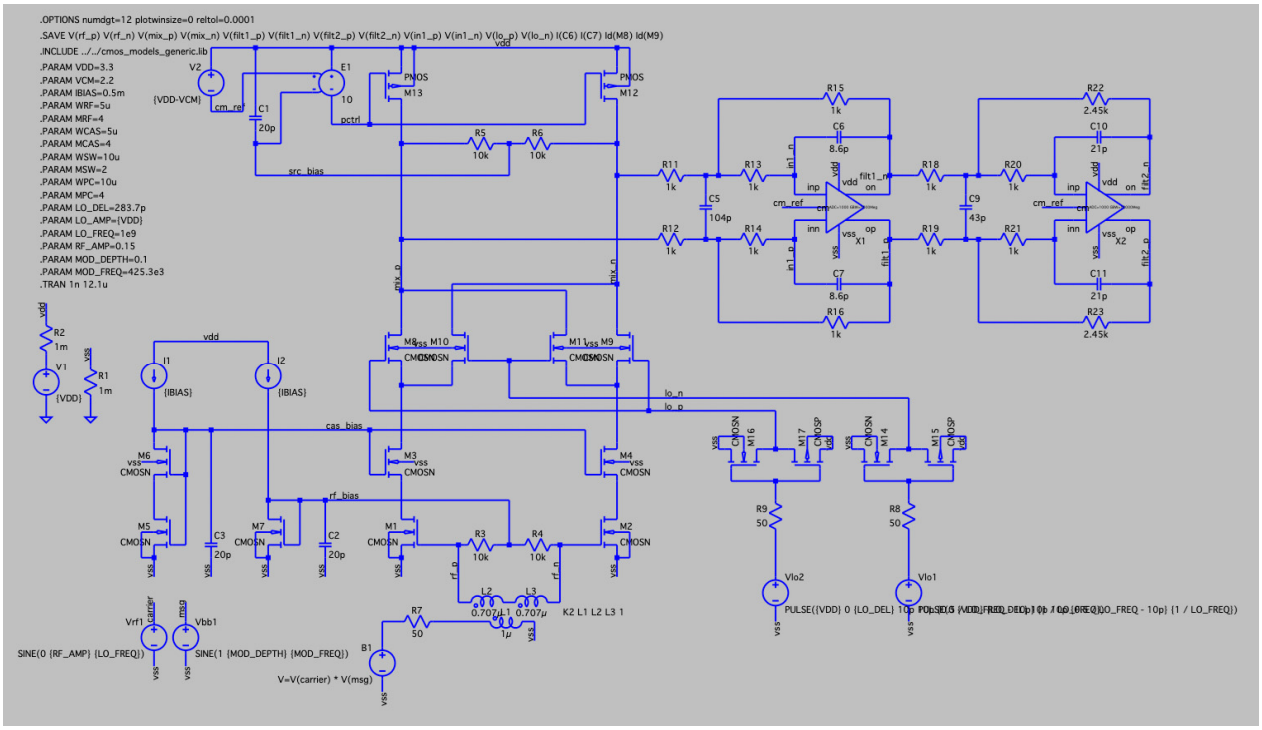
165. DEMAW-SIM-FIG. 7 (different sim settings) is a histogram of the charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1 (different sim settings).



DEMAW-SIM-FIG. 7. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1 (different sim settings)).

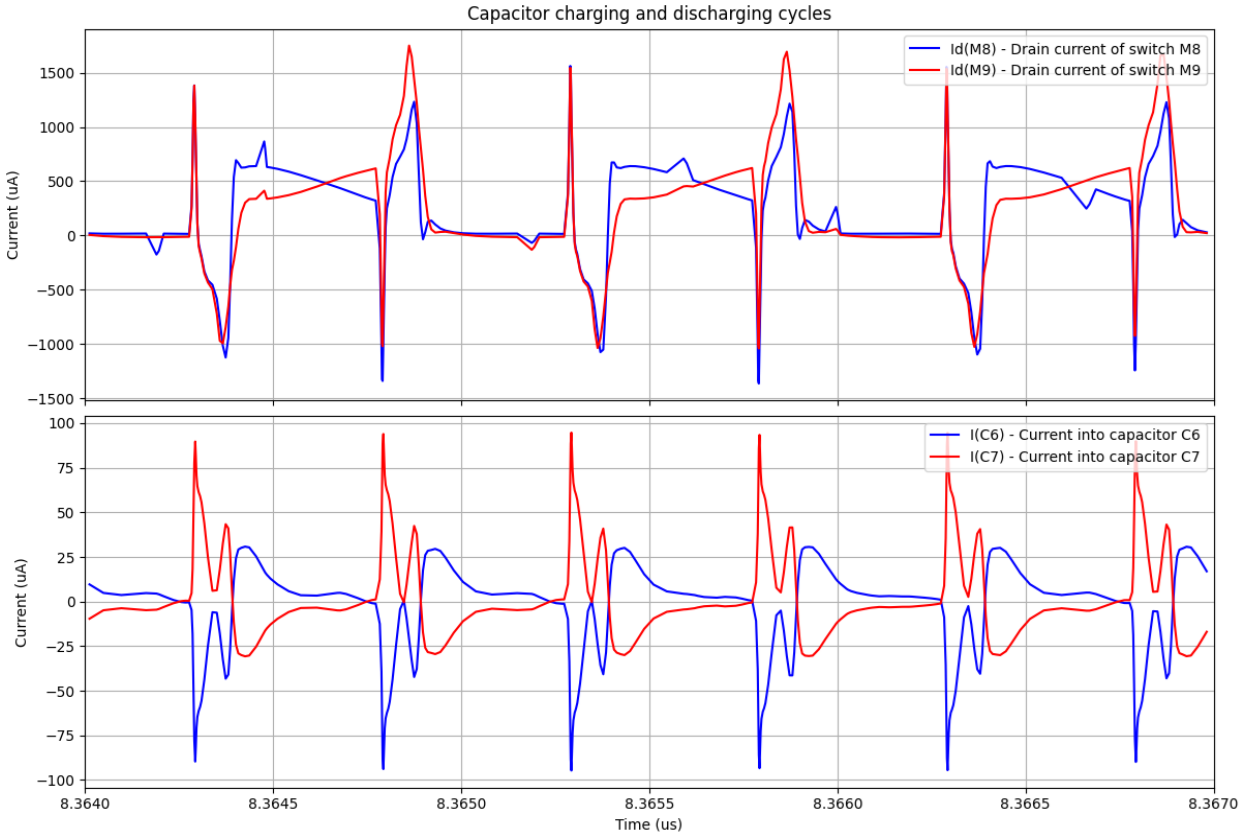
C. Original Macnally Simulation With/Without Revised Simulator Settings and Post-Processing

166. MACNALLY-SIM-FIG. 1 (different sim settings) is a schematic diagram of the simulated Macnally circuit from the original Declaration with revised simulator accuracy settings.



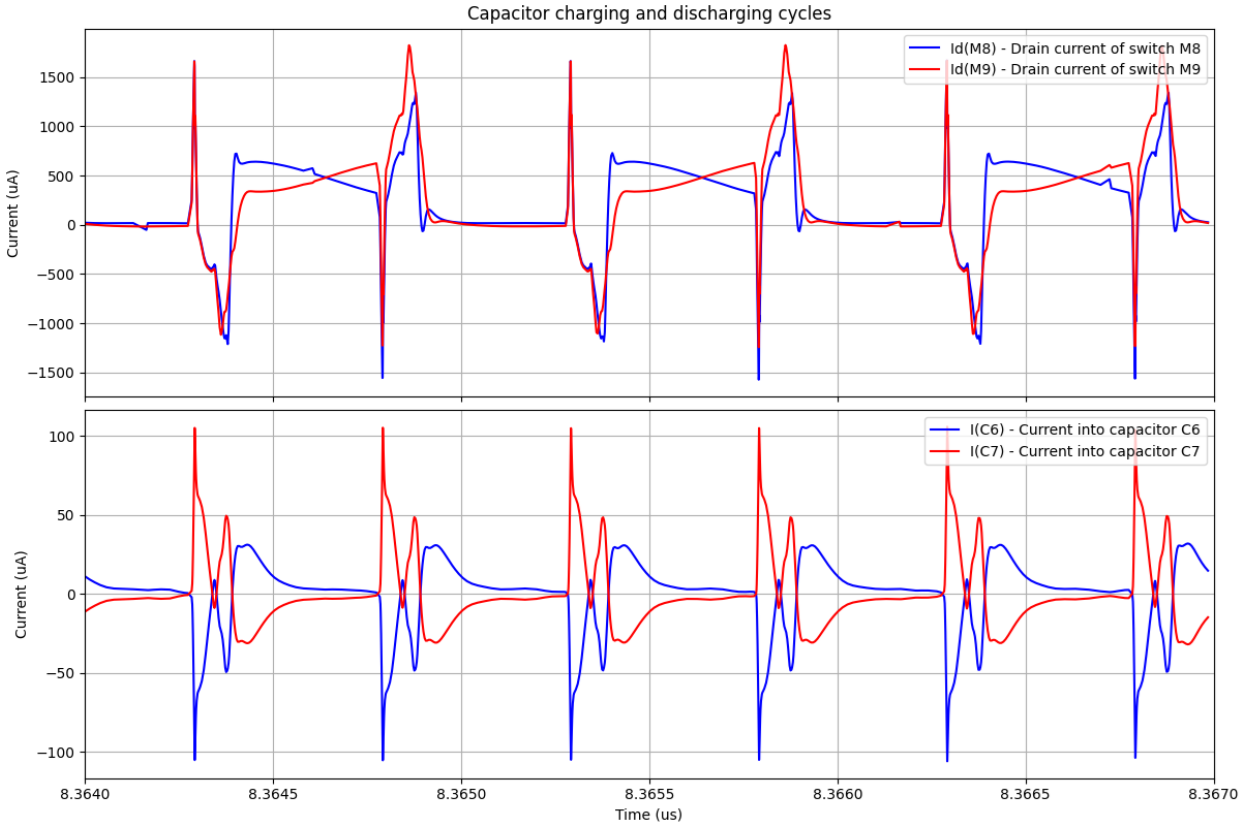
MACNALLY-SIM-FIG. 1 (different sim settings). Macnally circuit from the original Declaration with revised simulator accuracy settings

167. MACNALLY-SIM-FIG. 2 is a graphical representation illustrating charging and discharging cycles for capacitors C6 and C7 for the Macnally circuit from the original Declaration.



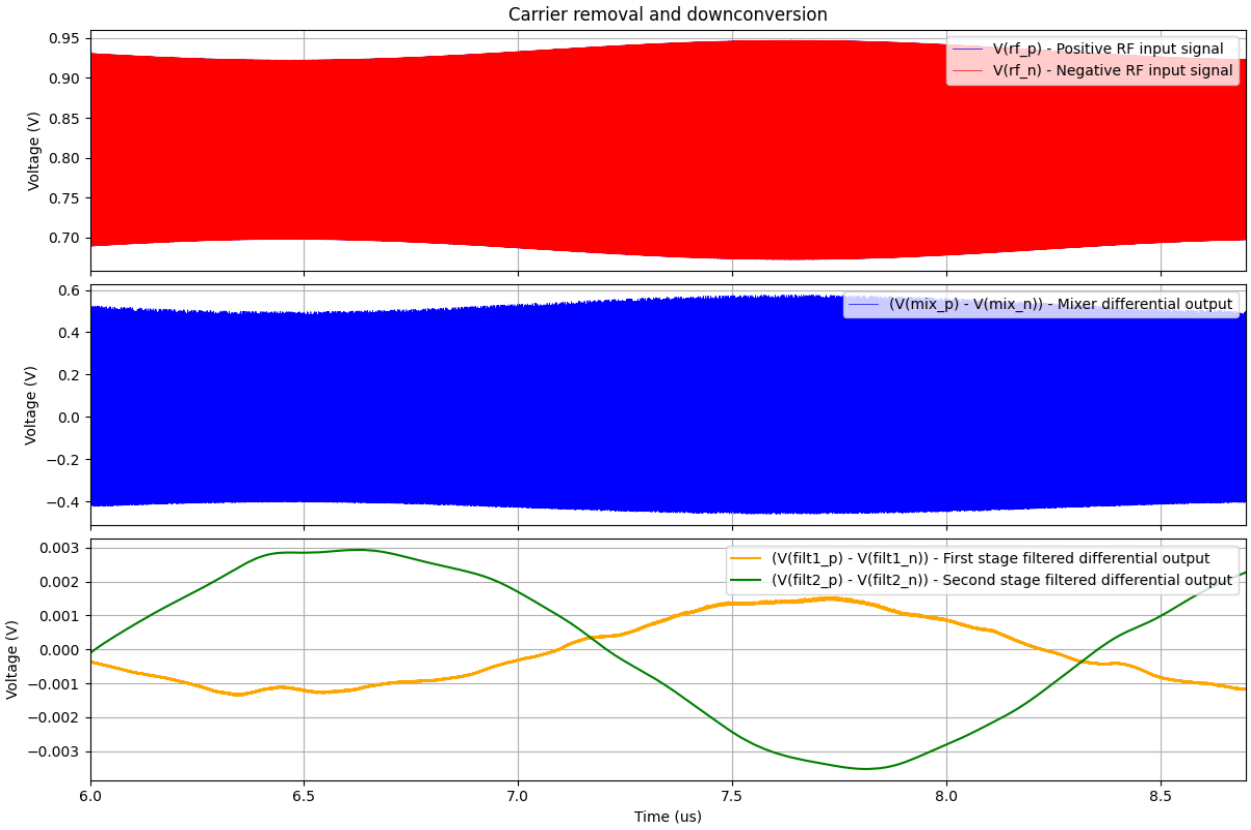
MACNALLY-SIM-FIG. 2. Capacitor charging and discharging cycles (Macnally circuit from the original Declaration).

168. MACNALLY-SIM-FIG. 2 (different sim settings) is a graphical representation illustrating charging and discharging cycles for capacitors C6 and C7 of the circuit of MACNALLY-SIM-FIG. 1 (different sim settings).



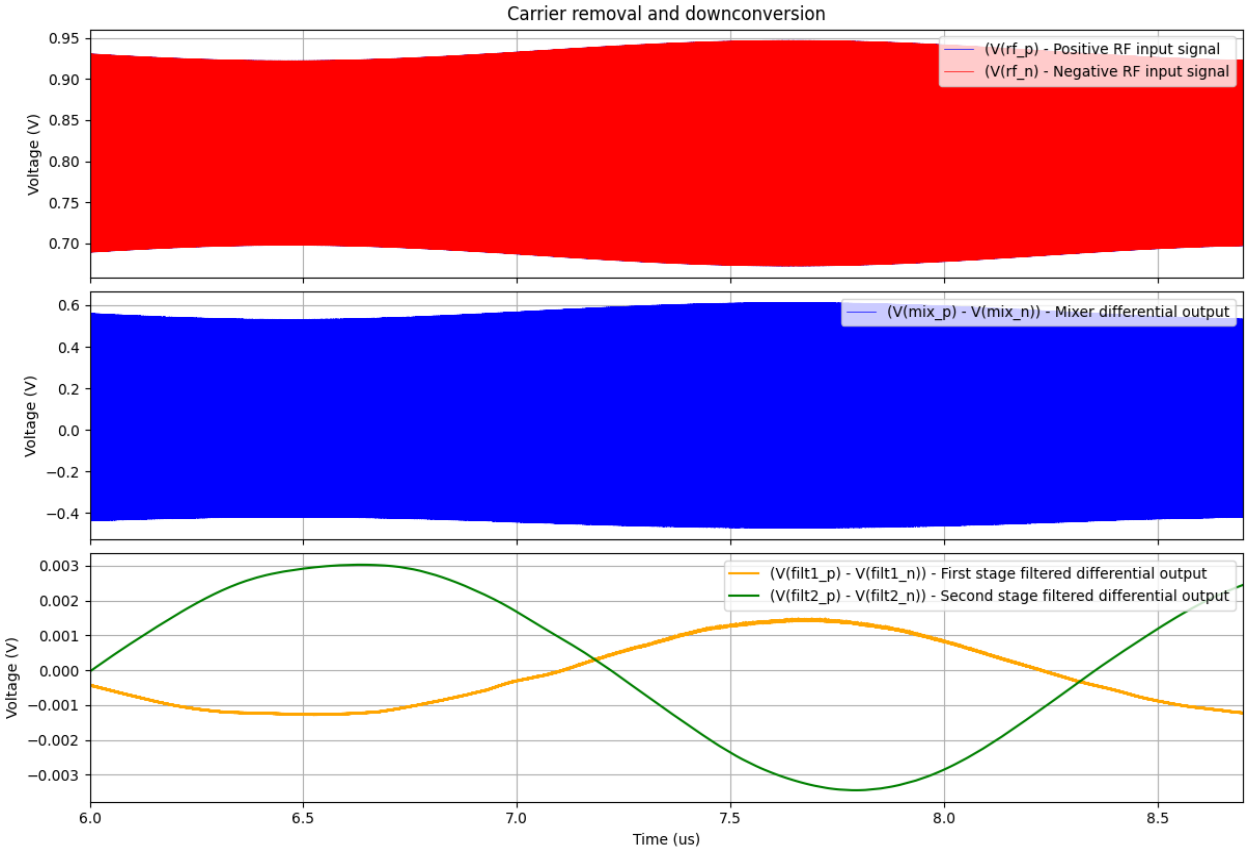
MACNALLY-SIM-FIG. 2 (different sim settings). Capacitor charging and discharging cycles (circuit of MACNALLY-SIM-FIG. 1 (different sim settings)).

169. MACNALLY-SIM-FIG. 6 is a graphical representation of carrier removal and down-conversion from the Macnally circuit from the original Declaration.



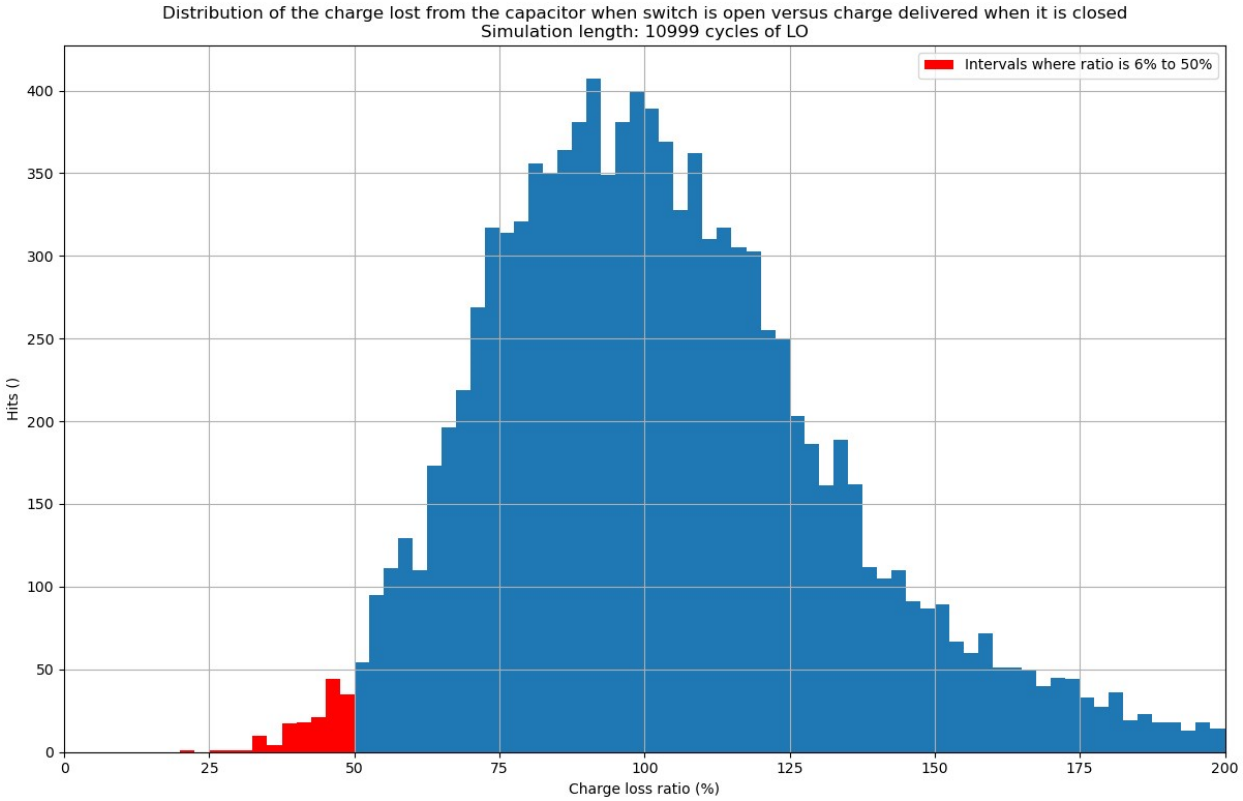
MACNALLY-SIM-FIG. 6. Carrier removal and down-conversion (Macnally circuit from the original Declaration).

170. MACNALLY-SIM-FIG. 6 (different sim settings) is a graphical representation of the carrier removal and down-conversion for the circuit of MACNALLY-SIM-FIG. 1 (different sim settings).



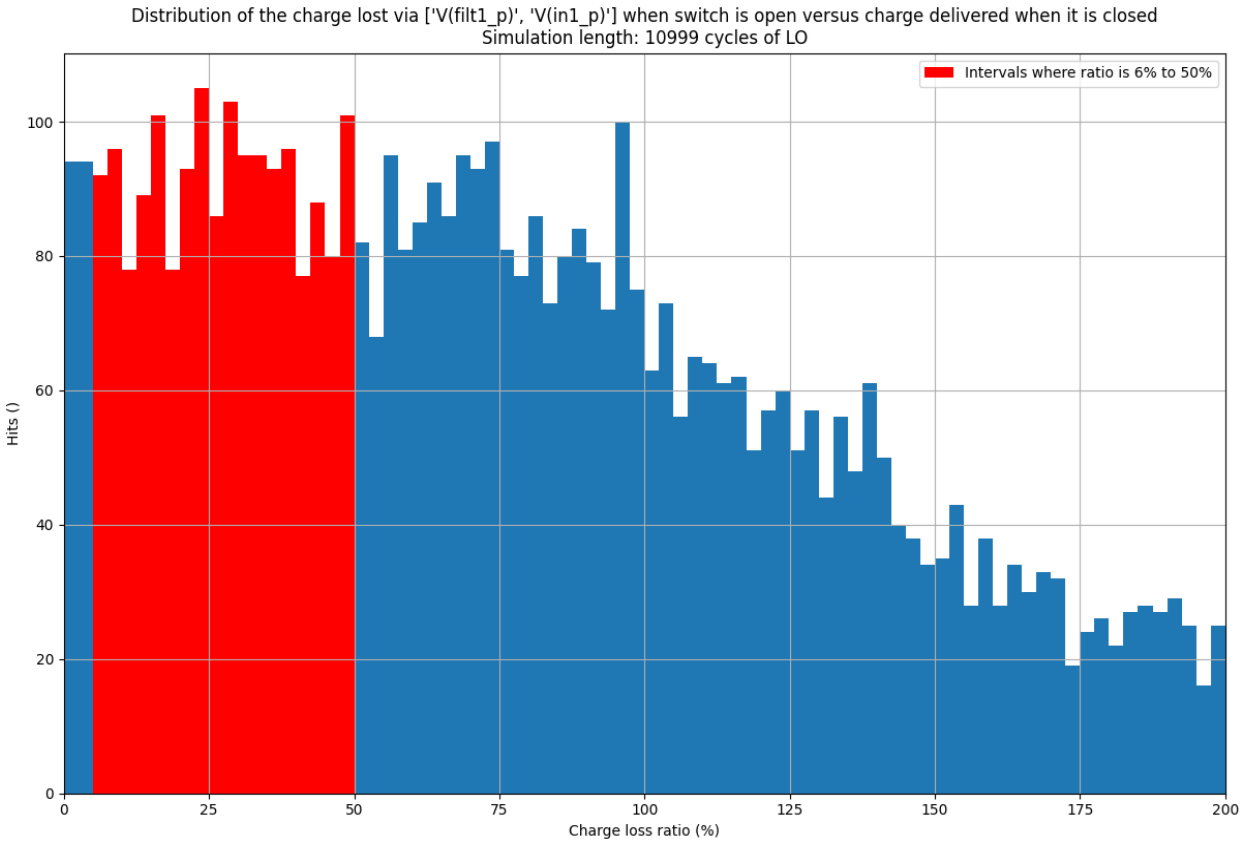
MACNALLY-SIM-FIG. 6 (different sim settings). Carrier removal and down-conversion (circuit of MACNALLY-SIM-FIG. 1 (different sim settings)).

171. MACNALLY-SIM-FIG. 4 is a histogram of charge loss ratio percentages for capacitor C6 from the Macnally circuit from the original Declaration generated using the improved Python script.



MACNALLY-SIM-FIG. 4. Charge loss ratio percentages histogram for capacitor C6 (Macnally circuit from the original Declaration).

172. MACNALLY-SIM-FIG. 4 (different sim settings) is a histogram of the charge loss ratio percentages for capacitor C6 from the circuit of MACNALLY-SIM-FIG. 1 (different sim settings).



MACNALLY-SIM-FIG. 4 (different sim settings). Charge loss ratio percentages histogram for capacitor C6 (circuit of MACNALLY-SIM-FIG. 1 (different sim settings)).

IX. Additional Remarks

173. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

174. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code.

Dated: March 17, 2024 By: /Dr. Ian Galton /

Dr. Ian Galton

ParkerVision Exhibit 2039
TI v. ParkerVision - IPR2024-00934

EXHIBIT 2

ParkerVision Exhibit 2039
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```
# ******************************************************************************
#
# Author: Colin Weltin-Wu (colinww@gmail.com)
# Date Created: Tue May 14 16:04:46 2024
# Project: parkervision
#
# Description
# -----------
# Common library of functions.
#
# Version History
# ---------------
# 14-May-24: Initial version.
#
# ******************************************************************************

import os
import numpy as np
import matplotlib.pyplot as plt
from datetime import datetime

# Uncomment this if you install PyLTSpice and you want to read raw directly
from PyLTSpice import RawRead

#%%#############################################################################
########
```


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```
27  # Constants
28  ##########################################################################
29  #######
30
31  SUFFIX = 'txt'
32  TNOW = datetime.now().strftime("%y_%m_%d_%H_%M_%S")
33
34  #%%#######################################################################
35  ########
36  # Helper functions
37  ##########################################################################
38  #######
39
40  def _load_ascii(fname):
41      try:
42          raw_data = np.loadtxt(fname, skiprows=1)
43      except:
44          return '', {}
45      # Get variable names
46      var_names = []
47      with open(fname, 'r') as fh:
48          var_names = fh.readline().split()
49      if not var_names:
50          print(f"Unable to open file or read first line: {fname}")
51          assert False
52      # Ensure same number of variable names as columns in data matrix
53      if (len(var_names) != raw_data.shape[1]):
```


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```
54          print(f"Data size {raw_data.shape[1]} != Variable names: {var_names}")
55          assert False
56      # Get the string name of the file
57      file_root = os.path.splitext(fname)[0]
58      # Create a lookup for the data
59      ddict = {}
60      for ii in range(len(var_names)):
61          ddict[var_names[ii]] = raw_data[:, ii]
62      return file_root, ddict
63
64  def _load_raw(fname):
65      try:
66          rawfile = RawRead(fname)
67      except:
68          return '', {}
69      var_names = rawfile.get_trace_names()
70      # Create a lookup for the data
71      ddict = {}
72      for vn in var_names:
73          if ('time' == vn):
74              ddict[vn] = rawfile.get_axis()
75          else:
76              ddict[vn] = rawfile.get_trace(vn).data
77      # Get the string name of the file
78      file_root = os.path.splitext(fname)[0]
79      return file_root, ddict
```


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```
80
81  def load_data(fname):
82      # Get file suffix, and determine what to do from there
83      _, sfx = os.path.splitext(fname)
84      if ('' == sfx):
85          sfx = '.' + SUFFIX
86      if '.raw' == sfx:
87          return _load_raw(fname + sfx)
88      elif '.txt' == sfx:
89          return _load_ascii(fname + sfx)
90      else:
91          print(f"ERROR: Don't know how to read {fname + sfx}")
92
93  def trim(tvec, xmin, xmax):
94      # Get independent axis and find index bounds
95      idxs = np.sum(xmin > tvec)
96      idxe = np.sum(xmax > tvec) - 1
97      tvec = tvec[idxs:idxe]
98      return (idxs, idxe), tvec
99
100
101 #%%#########################################################################
102 ########
103 # Useful functions
104 #########################################################################
105 #######
106
```


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```
107 def pwr_delivered(tvec, vin=None, iin=None, rload=50):
108     """Compute precise power delivered.
109
110     Parameters
111     ----------
112     tvec : float array
113         Time points.
114     vin : float array, optional
115         Voltage points across load. The default is None.
116     iin : float array, optional
117         Current delivered to load. The default is None.
118     rload : float, optional
119         Ideal load resistance. The default is 50.
120
121     Returns
122     -------
123     pdbm : float
124         Time-averaged power delivered to load (dBm).
125
126     Note
127     ----
128     We expect one or both of vin, iin to be provided. If both are provided, the
129     power is computed as the V*I product. If only one is provided, it is
130     assumed this is the node voltage/branch current across an ideal resistivd
131     load rload.
132
```


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```
133     """
134     # Check valid input
135     if iin is None and vin is None:
136         assert False, "Provided V, I, or both"
137     elif iin is None:
138         inst_pwr = vin * vin / rload
139     elif vin is None:
140         inst_pwr = iin * iin * rload
141     else:
142         inst_pwr = vin * iin
143     # Trapezoidal integral
144     pwr_avg = np.sum((inst_pwr[1:] + inst_pwr[:-1]) / 2 *
145                      (tvec[1:] - tvec[:-1]) /
146                      (tvec[-1] - tvec[0]))
147     return 10 * np.log10(1e3 * np.abs(pwr_avg))
148
149 def slice_wave(vlo, sig, vthresh=0, act_lo=True):
150     """Slice a signal waveform into consecutive pairs of segments.
151
152     Parameters
153     ----------
154     vlo : TYPE
155         DESCRIPTION.
156     sig : TYPE
157         DESCRIPTION.
158     vthresh : TYPE, optional
```


ParkerVision Exhibit 2039
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```
159         DESCRIPTION. The default is 0.
160     act_lo : TYPE, optional
161         DESCRIPTION. The default is True.
162
163     Returns
164     -------
165     None.
166
167     """
168     # Generate a sequential array of edge transitions. Get the starting state
169     # of the LO, to be used later
170     edge_idxs = np.zeros(len(vlo), dtype=int)
171     init_state = (vlo[0] > vthresh)
172     curr_state = init_state
173     idx = 0
174     for ii in range(len(vlo)):
175         if curr_state:
176             # LO is high, look for falling edge
177             if (vlo[ii] <= vthresh):
178                 edge_idxs[idx] = ii
179                 curr_state = 0
180                 idx += 1
181         else:
182             # LO is low, look for rising edge
183             if (vlo[ii] > vthresh):
184                 edge_idxs[idx] = ii
```


ParkerVision Exhibit 2039
TI v. ParkerVision - IPR2024-00934

```
185             curr_state = 1
186             idx += 1
187     # If act_lo=True, these are (falling, rising) index stamps of the LO.
188     # If act_lo=False, these are (rising, falling) indicies
189     if not (act_lo ^ init_state):
190         # Either active low AND initial state is high, OR, active high and
191         # initial state is low. Either way, first index is useful
192         idx_new = (idx // 2) * 2
193         if (idx_new < idx):
194             idx_new += 2
195         edge_idxs = edge_idxs[:idx_new]
196     else:
197         # We are active low and initial state is low, or active high and init
198         # state is high. Either way, we need to trim off the first index
199         idx_new = (((idx - 1) // 2) * 2) + 1
200         if (idx_new < idx):
201             idx_new += 2
202         edge_idxs = edge_idxs[1:idx_new]
203     # Return the array reshaped into (N, 2)
204     return edge_idxs.reshape((-1, 2))
205
206 #%%#########################################################################
207 ########
208 # DeMaw plots
209 #########################################################################
210 #######
211
```


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```
212 def demaw_inverted_information(fd, fn, dat, tstart=158.364e-6, tend=158.4e-6):
213     """Plots The  RF signal, and the source switching signals which clearly
214     shows the modulated differential RF signal.
215 
216     Parameters
217     ----------
218     fd : string
219         Output file destination.
220     fn : string
221         Root filename.
222     dat : dict
223         Simulation data.
224     tstart : float, optional
225         Plot start time. The default is 158.364e-6.
226     tend : float, optional
227         Plot end time. The default is 158.4e-6.
228 
229     Returns
230     -------
231     None.
232 
233     """
234     # Trim RF input signal
235     (idxs, idxe), tvec = trim(dat['time'], tstart, tend)
236     rfvec = dat['V(rf)'][idxs:idxe]
237     # Source voltages
```


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```
238     srp = dat['V(srp)'][idxs:idxe]
239     srn = dat['V(srn)'][idxs:idxe]
240     # Differential source voltage
241     src_diff = srp - srn
242     # Plot
243     fh, axs = plt.subplots(3, 1, sharex=True, figsize=(12, 10),
244                            constrained_layout=True)
245     axs[0].plot(1e6 * tvec, rfvec, lw=1.5,
246                 label='V(rf) - single-ended RF input signal')
247     axs[1].plot(1e6 * tvec, srp, lw=1.5, c='b',
248                 label='V(srp) - J1 source signal')
249     axs[1].plot(1e6 * tvec, srn, lw=1.5, c='r',
250                 label='V(srn) - J2 source signal')
251     axs[2].plot(1e6 * tvec, src_diff, lw=1.5,
252                 label='V(srp) - V(srn) - Differential source signal')
253     # Pretty-up plot
254     for ax in axs:
255       ax.grid(True)
256       ax.set_ylabel('Voltage (V)')
257       ax.legend(loc='upper right')
258     axs[-1].set_xlabel('Time (us)')
259     axs[-1].set_xlim([1e6 * tstart, 1e6 * tend])
260     axs[0].set_title('Generation of inverted information signal')
261     fh.savefig(fd + '/' + f'{fn}_inverted_information_{TNOW}.png')
262
263 def demaw_capacitor_charging(fd, fn, dat, tstart=158.364e-6, tend=158.4e-6):
```


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```
264     """Plots the switch and capacitor current waveforms against the LO.
265
266     Parameters
267     ----------
268     fd : string
269       Output file destination.
270     fn : string
271       Root filename.
272     dat : dict
273       Simulation data.
274     tstart : float, optional
275       Plot start time. The default is 158.364e-6.
276     tend : float, optional
277       Plot end time. The default is 158.4e-6.
278
279     Returns
280     -------
281     None.
282
283     """
284     # Trim time
285     (idxs, idxe), tvec = trim(dat['time'], tstart, tend)
286     # Empty plot pane
287     fh, axs = plt.subplots(3, 1, sharex=True, figsize=(12, 8),
288                            constrained_layout=True)
289     # LO signal
```


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```
290     dvec = dat['V(lo)']
291     axs[0].plot(1e6 * tvec, dvec[idxs:idxe], lw=1.5,
292             label='V(lo) - single-ended LO signal')
293     axs[0].set_ylabel('Voltage (V)')
294     # Switch drain current
295     dvec = dat['Id(J1)']
296     axs[1].plot(1e6 * tvec, 1e6 * dvec[idxs:idxe], lw=1.5, c='b',
297             label='Id(J1) - Drain current of switch J1')
298     dvec = dat['Id(J2)']
299     axs[1].plot(1e6 * tvec, 1e6 * dvec[idxs:idxe], lw=1.5, c='r',
300             label='Id(J2) - Drain current of switch J2')
301     axs[1].set_ylabel('Current (uA)')
302     # Capacitor voltages
303     dvec = dat['I(C4)']
304     axs[2].plot(1e6 * tvec, 1e6 * dvec[idxs:idxe], lw=1.5, c='b',
305             label='I(C4) - Current into capacitor C4')
306     dvec = dat['I(C5)']
307     axs[2].plot(1e6 * tvec, 1e6 * dvec[idxs:idxe], lw=1.5, c='r',
308             label='I(C5) - Current into capacitor C5')
309     axs[2].set_ylabel('Current (uA)')
310     # Pretty-up plot
311     for ax in axs:
312       ax.grid(True)
313       ax.legend(loc='upper right')
314     axs[-1].set_xlabel('Time (us)')
315     axs[-1].set_xlim([1e6 * tstart, 1e6 * tend])
```


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```
316     axs[0].set_title('Capacitor charging and discharging cycles')
317     fh.savefig(fd + '/' + f'{fn}_capacitor_charging_discharging_{TNOW}.png')
318
319 def demaw_downconverted_information(fd, fn, dat, tstart=150e-6, tend=151.4e-6):
320     """Plot shows the mixer downconverting RF to IF.
321
322     Parameters
323     ----------
324     fd : string
325         Output file destination.
326     fn : string
327         Root filename.
328     dat : dict
329         Simulation data.
330     tstart : float, optional
331         Plot start time. The default is 150e-6.
332     tend : float, optional
333         Plot end time. The default is 151.4e-6.
334
335     Returns
336     -------
337     None.
338
339     """
340     # Trim time
341     (idxs, idxe), tvec = trim(dat['time'], tstart, tend)
```


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```
342     # Empty plot pane
343     fh, axs = plt.subplots(3, 1, sharex=True, figsize=(12, 8),
344                            constrained_layout=True)
345     # RF input signals
346     dvec = dat['V(rf)']
347     axs[0].plot(1e6 * tvec, dvec[idxs:idxe], lw=1.5,
348             label='V(rf) - single-ended RF input signal')
349     axs[0].set_ylabel('Voltage (V)')
350     # Differential output signal
351     dvec = dat['V(diffp)']
352     axs[1].plot(1e6 * tvec, dvec[idxs:idxe], lw=1.5, c='b',
353             label='V(diffp) - Voltage across capacitor C6')
354     dvec = dat['V(diffn)']
355     axs[1].plot(1e6 * tvec, dvec[idxs:idxe], lw=1.5, c='r',
356             label='V(diffn) - Voltage across capacitor C7')
357     axs[1].set_ylabel('Voltage (V)')
358     # Single-ended output signal
359     dvec = dat['V(if)']
360     axs[2].plot(1e6 * tvec, dvec[idxs:idxe], lw=1.5,
361             label='V(if) - Modulated IF signal')
362     axs[2].set_ylabel('Voltage (V)')
363     # Pretty-up plot
364     for ax in axs:
365       ax.grid(True)
366       ax.legend(loc='upper right')
367     axs[-1].set_xlabel('Time (us)')
```


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```
368     axs[-1].set_xlim([1e6 * tstart, 1e6 * tend])
369     axs[0].set_title('Carrier removal and downconversion')
370     fh.savefig(fd + '/' + f'{fn}_carrier_removal_downconversion_{TNOW}.png')
371
372 def demaw_voltage_conv_gain(fd, fn, dat, tstart=320e-6, tend=330e-6):
373     """Plot shows the conversion gain and voltage gain.
374
375     Parameters
376     ----------
377     fd : string
378         Output file destination.
379     fn : string
380         Root filename.
381     dat : dict
382         Simulation data.
383     tstart : float, optional
384         Plot start time. The default is 320e-6.
385     tend : float, optional
386         Plot end time. The default is 330e-6.
387
388     Returns
389     -------
390     None.
391
392     """
393     # Trim time
```


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```
394     (idxs, idxe), tvec = trim(dat['time'], tstart, tend)
395     # Input signal
396     vin = dat['V(rf)'][idxs:idxe]
397     iin = dat['I(R1)'][idxs:idxe]
398     # Compute power from the voltage source
399     psrc_dbm = pwr_delivered(tvec, vin, iin)
400     # Compute power dissipated in the series resistor
401     pres_dbm = pwr_delivered(tvec, iin=iin, rload=50)
402     pin_dbm = 10 * np.log10(10**(psrc_dbm / 10) - 10**(pres_dbm / 10))
403     # Compute power out
404     vout = dat['V(if)'][idxs:idxe]
405     pout_dbm = pwr_delivered(tvec, vin=vout, rload=50)
406     # Conversion gain
407     conv_gain = pout_dbm - pin_dbm
408     # Plot Vrf vs Vdiff
409     vdiff = (dat['V(drp)'][idxs:idxe] - dat['V(drn)'][idxs:idxe])
410     #  av_gain = 20 * np.log10(np.std(vdiff) / np.std(vin))
411     fh, ax = plt.subplots(1, 1, sharex=True, figsize=(12, 10),
412                           constrained_layout=True)
413     ax.plot(1e6 * tvec, vin, lw=1.5, label='V(rf)', c='k')
414     ax.plot(1e6 * tvec, vdiff, lw=1.5, label='V(drp) - V(drn)', c='orange')
415     ax.set_xlim([1e6 * tstart, 1e6 * tstart + 1])
416     ax.grid(True)
417     ax.legend()
418     ax.set_xlabel('Time (us)')
419     ax.set_ylabel('Volts (V)')
```


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```
420     ax.set_title(f'Mixer conversion gain: {conv_gain:.2f}dB\n' +
421                  f'Pin={pin_dbm:.2f}dBm, Pout={pout_dbm:.2f}dBm')
422     fh.savefig(fd + '/' + f'{fn}_conv_gain_{TNOW}.png')
423
424
425 #%%#########################################################################
426 ########
427 # MacNally plots
428 ##########################################################################
429 #######
430
431 def macnally_capacitor_charging(fd, fn, dat, tstart=8.364e-6, tend=8.367e-6):
432     """Plots the switch and capacitor current waveforms against the LO.
433
434     Parameters
435     ----------
436     fd : string
437         Output file destination.
438     fn : string
439         Root filename.
440     dat : dict
441         Simulation data.
442     tstart : float, optional
443         Plot start time. The default is 8.364e-6.
444     tend : float, optional
445         Plot end time. The default is 8.367e-6.
446
```


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```
447     Returns
448     -------
449     None.
450
451     """
452     # Trim time
453     (idxs, idxe), tvec = trim(dat['time'], tstart, tend)
454     # Empty plot pane
455     fh, axs = plt.subplots(2, 1, sharex=True, figsize=(12, 8),
456                            constrained_layout=True)
457     # Switch drain current
458     dvec = dat['Id(M8)']
459     axs[0].plot(1e6 * tvec, 1e6 * dvec[idxs:idxe], lw=1.5, c='b',
460             label='Id(M8) - Drain current of switch M8')
461     dvec = dat['Id(M9)']
462     axs[0].plot(1e6 * tvec, 1e6 * dvec[idxs:idxe], lw=1.5, c='r',
463             label='Id(M9) - Drain current of switch M9')
464     axs[0].set_ylabel('Current (uA)')
465     # Capacitor voltages
466     dvec = dat['I(C6)']
467     axs[1].plot(1e6 * tvec, 1e6 * dvec[idxs:idxe], lw=1.5, c='b',
468             label='I(C6) - Current into capacitor C6')
469     dvec = dat['I(C7)']
470     axs[1].plot(1e6 * tvec, 1e6 * dvec[idxs:idxe], lw=1.5, c='r',
471             label='I(C7) - Current into capacitor C7')
472     axs[1].set_ylabel('Current (uA)')
```


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```
473     # Pretty-up plot
474     for ax in axs:
475         ax.grid(True)
476         ax.legend(loc='upper right')
477     axs[-1].set_xlabel('Time (us)')
478     axs[-1].set_xlim([1e6 * tstart, 1e6 * tend])
479     axs[0].set_title('Capacitor charging and discharging cycles')
480     fh.savefig(fd + '/' + f'{fn}_capacitor_charging_discharging_{TNOW}.png')
481
482 def macnally_downconverted_information(fd, fn, dat, tstart=7.4e-6,
483                                        tend=7.7e-6):
484     """Plot shows the mixer downconverting to baseband.
485
486     Parameters
487     ----------
488     fd : string
489         Output file destination.
490     fn : string
491         Root filename.
492     dat : dict
493         Simulation data.
494     tstart : float, optional
495         Plot start time. The default is 6e-6.
496     tend : float, optional
497         Plot end time. The default is 8.7e-6.
498
```


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```
499     Returns
500     -------
501     None.
502
503     """
504     # Trim time
505     (idxs, idxe), tvec = trim(dat['time'], tstart, tend)
506     # Empty plot pane
507     fh, axs = plt.subplots(3, 1, sharex=True, figsize=(12, 8),
508                            constrained_layout=True)
509     # RF input signals
510     dvec = dat['V(rf_p)']
511     axs[0].plot(1e6 * tvec, dvec[idxs:idxe], lw=0.5, c='b',
512             label='(V(rf_p) - Positive RF input signal')
513     axs[0].set_ylabel('Voltage (V)')
514     dvec = dat['V(rf_n)']
515     axs[0].plot(1e6 * tvec, dvec[idxs:idxe], lw=0.5, c='r',
516             label='(V(rf_n) - Negative RF input signal')
517     axs[0].set_ylabel('Voltage (V)')
518     # Differential mixer signal
519     dvec = dat['V(mix_p)'] - dat['V(mix_n)']
520     axs[1].plot(1e6 * tvec, dvec[idxs:idxe], lw=0.5, c='b',
521             label='(V(mix_p) - V(mix_n)) - Mixer differential output')
522     axs[1].set_ylabel('Voltage (V)')
523     # Filtered differential signal
524     dvec = dat['V(filt1_p)'] - dat['V(filt1_n)']
```


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```
525     dvec -= np.mean(dvec)
526     axs[2].plot(1e6 * tvec, dvec[idxs:idxe], lw=1.5, c='orange',
527             label='(V(filt1_p) - V(filt1_n)) - First stage filtered differential output')
528     axs[2].set_ylabel('Voltage (V)')
529     # Second filtered differential signal
530     dvec = dat['V(filt2_p)'] - dat['V(filt2_n)']
531     dvec -= np.mean(dvec)
532     axs[2].plot(1e6 * tvec, dvec[idxs:idxe], lw=1.5, c='g',
533             label='(V(filt2_p) - V(filt2_n)) - Second stage filtered differential output')
534     axs[2].set_ylabel('Voltage (V)')
535     # Pretty-up plot
536     for ax in axs:
537       ax.grid(True)
538       ax.legend(loc='upper right')
539     axs[-1].set_xlabel('Time (us)')
540     axs[-1].set_xlim([1e6 * tstart, 1e6 * tend])
541     axs[0].set_title('Carrier removal and downconversion')
542     fh.savefig(fd + '/' + f'{fn}_carrier_removal_downconversion_amplification_{TNOW}.png')
543
544 def macnally_bfsk(fd, fn, dat, tstart=1e-6, tend=40e-6):
545     """Plot shows the BFSK downconversion.
546
547     Parameters
548     ----------
549     fd : string
550       Output file destination.
```


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```
551     fn : string
552         Root filename.
553     dat : dict
554         Simulation data.
555     tstart : float, optional
556         Plot start time. The default is 6e-6.
557     tend : float, optional
558         Plot end time. The default is 8.7e-6.
559
560     Returns
561     -------
562     None.
563
564     """
565     # Trim time
566     (idxs, idxe), tvec = trim(dat['time'], tstart, tend)
567     # Empty plot pane
568     fh, axs = plt.subplots(3, 1, sharex=True, figsize=(12, 8),
569                            constrained_layout=True)
570     # RF input signals
571     dvec = dat['V(fsk_bb)']
572     axs[0].plot(1e6 * tvec, dvec[idxs:idxe], lw=0.5, c='b',
573                 label='V(fsk_bb) - Baseband BFSK signal')
574     axs[0].set_ylabel('Voltage (V)')
575     # Differential mixer signal
576     dvec = dat['V(vmix_vfilt)']
```


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```
577     axs[1].plot(1e6 * tvec, dvec[idxs:idxe], lw=0.5, c='b',
578             label='V(vmix_vfilt) - Mixer differential output (Ideal 1MHz LPF)')
579     axs[1].set_ylabel('Voltage (V)')
580     # Filtered differential signal
581     dvec = dat['V(filt1_p)'] - dat['V(filt1_n)']
582     dvec -= np.mean(dvec)
583     axs[2].plot(1e6 * tvec, dvec[idxs:idxe], lw=1.5, c='orange',
584             label='(V(filt1_p) - V(filt1_n)) - First stage filtered differential output')
585     axs[2].set_ylabel('Voltage (V)')
586     # Second filtered differential signal
587     dvec = dat['V(filt2_p)'] - dat['V(filt2_n)']
588     dvec -= np.mean(dvec)
589     axs[2].plot(1e6 * tvec, dvec[idxs:idxe], lw=1.5, c='g',
590             label='(V(filt2_p) - V(filt2_n)) - Second stage filtered differential output')
591     axs[2].set_ylabel('Voltage (V)')
592     # Pretty-up plot
593     for ax in axs:
594       ax.grid(True)
595       ax.legend(loc='upper right')
596     axs[-1].set_xlabel('Time (us)')
597     axs[-1].set_xlim([1e6 * tstart, 1e6 * tend])
598     axs[0].set_title('Direct downconversion of BFSK signal')
599     fh.savefig(fd + '/' + f'{fn}_bfsk_modulation_{TNOW}.png')
600
601 def macnally_voltage_gain(fd, fn, dat, tstart=1e-6, tend=20e-6):
602     """Plot shows the mixer voltage gain (since output not matched to 50).
```


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```
603
604     Parameters
605     ----------
606     fd : string
607         Output file destination.
608     fn : string
609         Root filename.
610     dat : dict
611         Simulation data.
612     tstart : float, optional
613         Plot start time. The default is 320e-6.
614     tend : float, optional
615         Plot end time. The default is 330e-6.
616
617     Returns
618     -------
619     None.
620
621     """
622     # Trim time
623     (idxs, idxe), tvec = trim(dat['time'], tstart, tend)
624     # Input signal
625     vin = dat['V(bb_se)'][idxs:idxe]
626     iin = dat['I(R30)'][idxs:idxe]
627     # Compute power from the voltage source
628     psrc_dbm = pwr_delivered(tvec, vin, iin)
```


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```
629     # Compute power dissipated in the series resistor
630     pres_dbm = pwr_delivered(tvec, iin=iin, rload=1)
631     pin_dbm = 10 * np.log10(10**(psrc_dbm / 10) - 10**(pres_dbm / 10))
632     # Filtered Vdiff
633     vmix_vfilt = dat['V(vmix_vfilt)'][idxs:idxe]
634     # Plot Vrf vs Vdiff
635     vdiff = (dat['V(mix_p)'][idxs:idxe] - dat['V(mix_n)'][idxs:idxe])
636     av_gain = 20 * np.log10(np.std(vmix_vfilt) / np.std(vin))
637     fh, ax = plt.subplots(1, 1, sharex=True, figsize=(12, 10),
638                           constrained_layout=True)
639     ax.plot(1e6 * tvec, vdiff, lw=1.5, label='V(mix_p) - V(mix_n)', c='orange')
640     ax.plot(1e6 * tvec, vmix_vfilt, lw=1.5, label='V(mix_p) - V(mix_n) - 1MHz LPF',
641             c='green')
642     ax.plot(1e6 * tvec, vin, lw=1.5, label='V(rf_p) - V(rf_n)', c='k')
643     ax.set_xlim([1e6 * tstart, 1e6 * tend])
644     ax.grid(True)
645     ax.legend()
646     ax.set_xlabel('Time (us)')
647     ax.set_ylabel('Volts (V)')
648     ax.set_title(f'Mixer voltage gain: {av_gain:.2f}dB\n' +
649                  f'Pin={pin_dbm:.2f}dBm')
650     fh.savefig(fd + '/' + f'{fn}_voltage_gain_{TNOW}.png')
651
652 #%%#########################################################################
653 ########
654 # Histograms
```


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```
655 ##########################################################################
656 #######
657
658 def cap_histogram(fd, fn, dat, lo, cap, tstart=60e-6, tend=400e-6, npts=None,
659                   pct_range=[-200, 200], act_lo=True):
660     """Plot shows the histogram of charge in and out of the capacitor.
661
662     Parameters
663     ----------
664     fd : string
665         Output file destination.
666     fn : string
667         Root filename.
668     dat : dict
669         Simulation data.
670     lo : string
671         LO waveform name.
672     cap : string
673         Capacitor to be plotted.
674     tstart : float, optional
675         Plot start time. The default is 320e-6.
676     tend : float, optional
677         Plot end time. The default is 330e-6.
678     npts : int
679         Number of points to plot, if not provided, plot all.
680     pct_range : pair float
```


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```
681         Histogram plotting range.
682     Returns
683     -------
684     None.
685
686     """
687     # Trim time
688     (idxs, idxe), tvec = trim(dat['time'], tstart, tend)
689     # Trim LO signal
690     if isinstance(lo, (list, tuple)):
691         # Differential signals given
692         vlo = dat[lo[0]][idxs:idxe] - dat[lo[1]][idxs:idxe]
693     else:
694         # Single-ended signal
695         vlo = dat[lo][idxs:idxe]
696     # Check if second item is a number, in which case the voltage is
697     # provided single-ended
698     if isinstance(cap[1], (int, float)):
699         cap_sig = dat[cap[0]][idxs:idxe] - cap[1]
700     else:
701         cap_sig = dat[cap[0]][idxs:idxe] - dat[cap[1]][idxs:idxe]
702     # Use LO signal to divide up intervals
703     crosses = slice_wave(vlo, cap_sig, act_lo=act_lo)
704     # Get the number of events, subtract one since we need the final crossing
705     nevent = crosses.shape[0]
706     nevent -= 1
```


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```
707     # Determine if we should limit the number of points
708     if npts is not None and (npts < nevent):
709         nevent = npts
710     # Compute the total charge delivered to the cap when the switch is on, and
711     # the charge lost from the cap when the switch is off
712     qin = np.zeros(nevent)
713     qout = np.zeros(nevent)
714     for ii in range(nevent):
715         idx0 = crosses[ii, 0]
716         idx1 = crosses[ii, 1]
717         idx2 = crosses[ii + 1, 0]
718         # Use capacitor voltage, already integrated by spice
719         qin[ii] = cap_sig[idx1] - cap_sig[idx0]
720         qout[ii] = -(cap_sig[idx2] - cap_sig[idx1])
721         # Remove NaN values. This is safe since if qin[ii] is extremely small,
722         # the charge transfer ratio is huge anyway, doesn't matter for this
723         # computation. Just want to suppress divide by 0 warnings
724         if (0 == qin[ii]):
725             qin[ii] = np.nextafter(0, 1)
726     # Plot histogram
727     qloss = 100 * qout / qin
728     hist_vals, hist_bins = np.histogram(qloss, range=pct_range, bins=80)
729     fh, ax = plt.subplots(1, 1, figsize=(12, 10), constrained_layout=True)
730     ax.bar(hist_bins[:-1], hist_vals, width=np.diff(hist_bins), align='edge',
731            label='__no_legend')
732     # Plot subset of data in the 6-50% range
```


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```
733     idxs = np.sum(5 > hist_bins)
734     idxe = np.sum(50 > hist_bins)
735     ax.bar(hist_bins[idxs:idxe], hist_vals[idxs:idxe],
736         width=np.diff(hist_bins[idxs:idxe + 1]),
737         align='edge', color='red',
738         label='Intervals where ratio is 6% to 50%')
739     ax.legend()
740     ax.set_xlabel('Charge loss ratio (%)')
741     ax.set_ylabel('Hits ()')
742     ax.grid(True)
743     ax.set_xlim(pct_range)
744     ttl = (f'Distribution of the charge lost via {cap} when switch is open ' +
745         'versus charge delivered when it is closed')
746     ttl += '\nSimulation length: {} cycles of LO'.format(nevent)
747     ax.set_title(ttl)
748     capstr = '_'.join([str(x) for x in cap])
749     fh.savefig(fd + '/' + f'{fn}_cap_charge_histogram_{capstr}_{TNOW}.png')
750
751
752
753 #######
754 # DEBUG
755 #######
756 if False:
757     from PyLTSpice import RawRead
758     # Just check that RawRead works in OSX
759     rawread = RawRead('macnally_mixer.raw')
```


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```
760     rawread.get_trace_names()
761
762     dat = rawdat
763     tstart = 60e-6
764     tend = 400e-6
765     lo = 'V(lo)'
766     cap = 'I(C4)'
767     pct_range = [-200, 200]
768
769     # Trim time
770     (idxs, idxe), tvec = com.trim(dat['time'], tstart, tend)
771     # Trim LO signal
772     vlo = dat[lo][idxs:idxe]
773     # Trim capacitor current
774     icap = dat[cap][idxs:idxe]
775     crosses = com.slice_wave(vlo, icap, act_lo=True)
776
777
778 if False:
779     fn, dat = _load_raw('macnally_mixer.raw')
780     tstart = 1e-6
781     tend = 12e-6
782     lo = ['V(lo_p)', 'V(lo_n)']
783     cap = 'I(C7)'
784     (idxs, idxe), tvec = trim(dat['time'], tstart, tend)
785     vlo = dat[lo[0]][idxs:idxe] - dat[lo[1]][idxs:idxe]
```

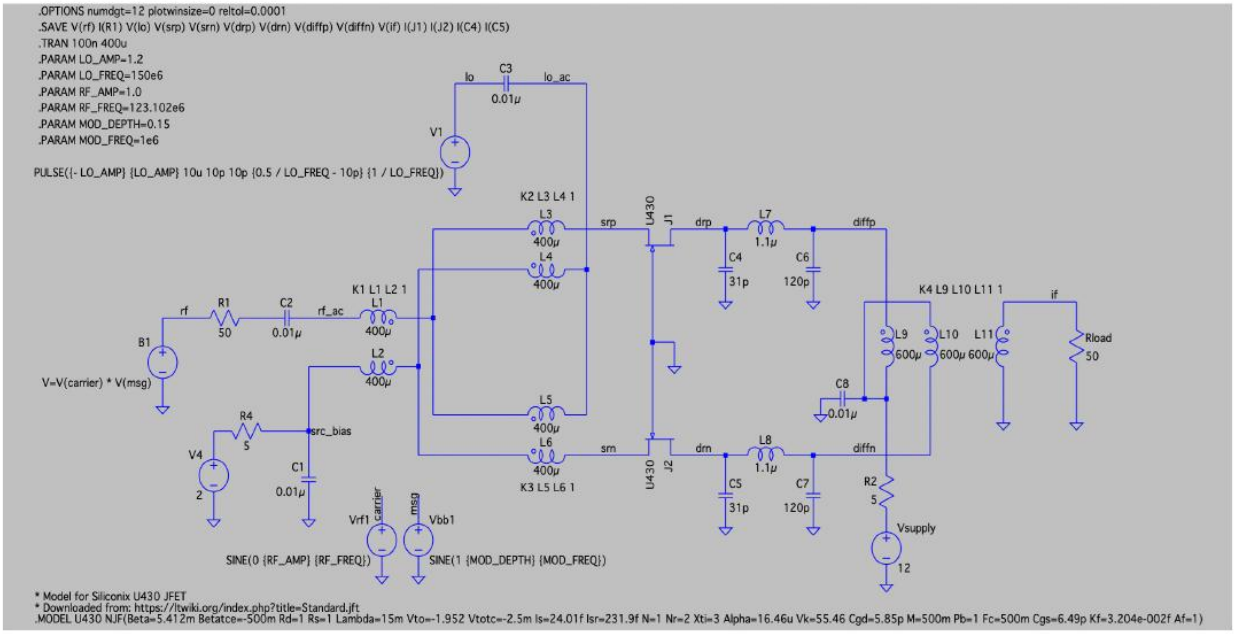

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```
786         icap = dat[cap][idxs:idxe]
787         crosses = slice_wave(vlo, icap, act_lo=False)
788         nevent = crosses.shape[0]
789         nevent -= 1
790
791
792
```

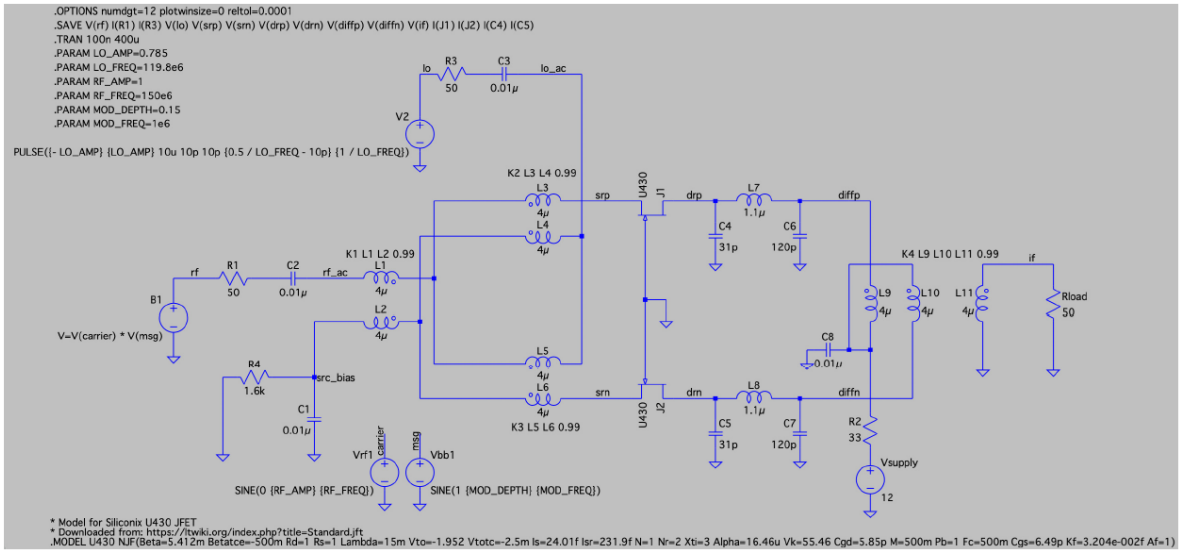

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EXHIBIT 3

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DEMAW-SIM-FIG. 1 (revised, clean). DeMaw circuit as described in the original Declaration but with U430 JFET models (highlighting two capacitors).



DEMAW-SIM-FIG. 1.2. DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and a large input signal.