

IPR2024-00934
U.S. Patent No. 7,496,342
Patent Owner's Response

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Texas Instruments Incorporated
Petitioner,

v.

PARKERVISION, INC.
Patent Owner.

U.S. Patent No. 7,496,342

Issue Date: February 24, 2009

Title: DOWN-CONVERTING ELECTROMAGNETIC SIGNALS, INCLUDING
CONTROLLED DISCHARGE OF CAPACITORS

Inter Partes Review No. IPR2024-00934

**PATENT OWNER'S RESPONSE TO PETITION FOR *INTER PARTES*
REVIEW OF UNITED STATES PATENT NO. 7,496,342**

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PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2007-2020	RESERVED
2021	Declaration of Dr. David Ricketts
2022-2024	RESERVED
2025	Excerpts from Howe, R. et al., Microelectronics: An Integrated Approach
2026-2030	RESERVED
2031	Excerpt of Graf, R., Modern Dictionary of Electronics, Seventh Edition
2032	Rofougaran, A., et al., A 1 GHz CMOS RF Front-End IC for a Direct Conversion Wireless Receiver
2033	U.S. Patent No. 6,061,551
2034	Deposition Transcript of Ian Galton, dated March 12, 2025
2035	Sedra, Microelectronic Circuits (4 th ed. 1998)
2036	Deposition Transcript of Ian Galton, dated February 28, 2025
2037	CMOS Analog Circuit Design
2038	Sze, Physics of Semiconductor Devices (2 nd ed. 1981)
2039	Deposition Transcript of Ian Galton, dated April 14, 2025
2040	Email dated 2/28/2025 from Petitioner to Patent Owner
2041	Email dated 3/4/2025 from Patent Owner to PTAB

I. INTRODUCTION

The claims of U.S. Patent No. 7,496,342 (“’342 patent”) are directed to a method for down-converting a radio signal.

Petitioner alleges that claims 19-21 are invalid in view of DeMaw and Macnally.

The claims require that capacitors discharge specific percentages of “the total charge stored therein *during a period of time that the first switching devices is open.*” With regard to DeMaw, Petitioner relies on its expert’s circuit simulations and calculations to show these percentages. However, the expert uses the wrong formula when calculating discharge percentages. In particular, the expert failed to calculate the discharge as a percentage of “total” charge stored on a capacitor. When the correct formula is used, the percentage discharge falls outside of the claimed percentage ranges. Moreover, Petitioner failed to calculate the percentage discharged when the switching device is “open” (OFF) as required by the claims. This is because the alleged switching devices in DeMaw are never open (OFF).

The claims also require “electrically coupling” an information signal to a capacitor. Macnally, however, does not disclose “electrically coupling” under the PTAB’s prior construction of this term. Further, Macnally does not disclose switching devices, because the alleged switching devices in Macnally do not open a circuit.

Accordingly, Petitioner has failed to demonstrate that the challenged claims are invalid.

II. LEVEL OF ORDINARY SKILL IN THE ART

A POSITA would have (a) a BS degree in electrical or computer engineering (or a related academic field), and at least two (2) additional years of work experience in the design and development of radio frequency circuits and/or systems, or (b) at least five (5) years of work experience and training in the design and development of radio frequency circuits and/or systems.

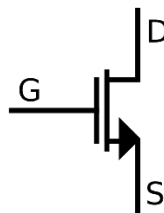
III. TECHNOLOGY BACKGROUND

A. Circuit Components

1. Transistor¹

A transistor is a semiconductor device used to switch, detect, or amplify electronic signals and electrical power.

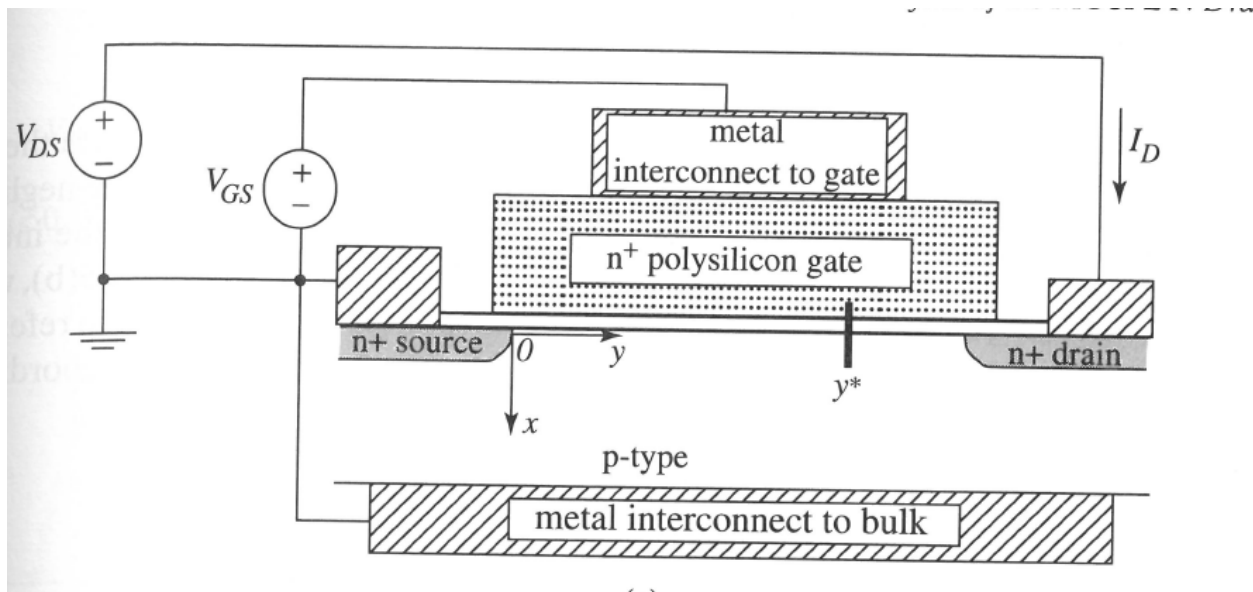
The symbol for one type of FET is shown below.



¹ Ex.-2021, ¶¶49-56.

2. NMOS transistors²

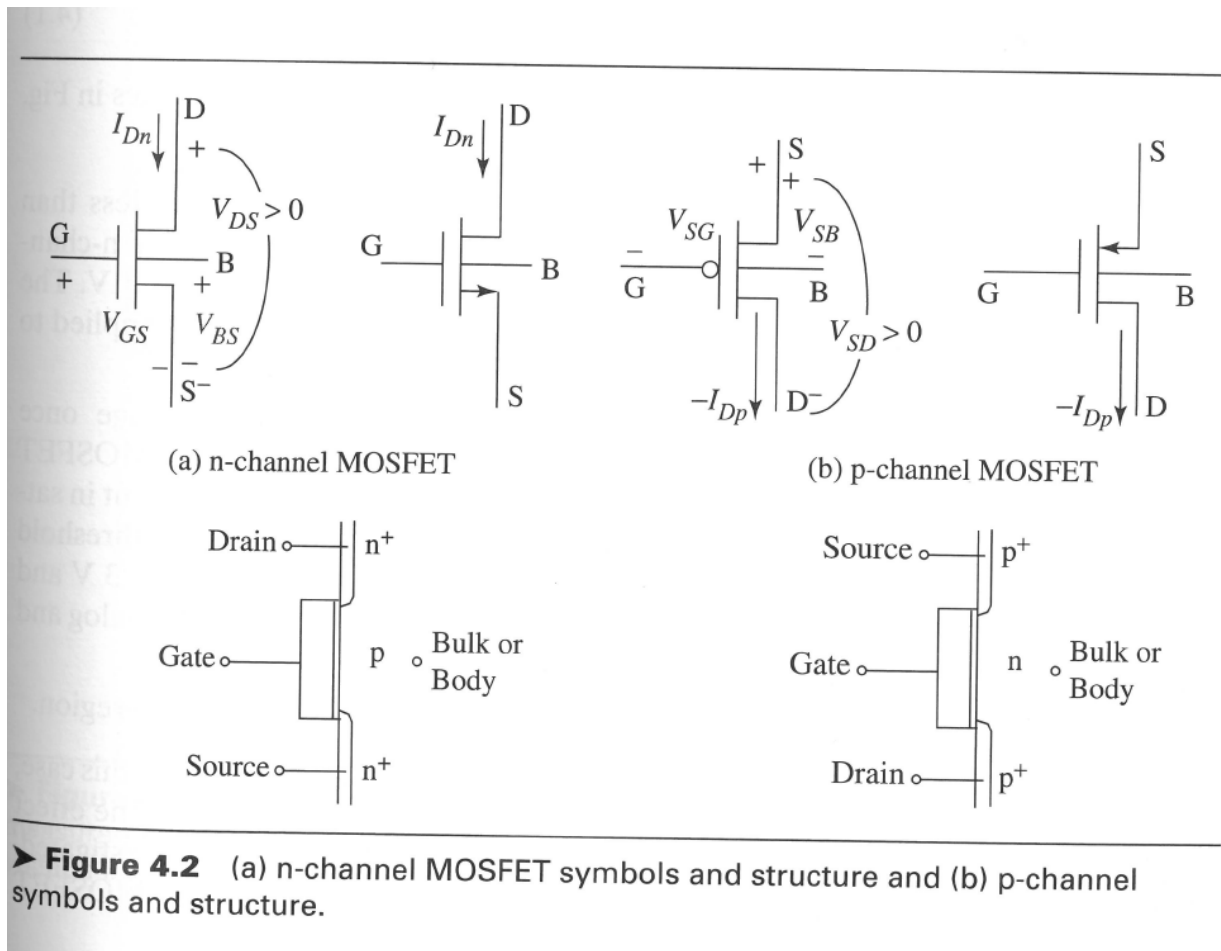
An NMOS (N-channel Metal-Oxide-Semiconductor) Field-Effect Transistor (FET) consists of three terminals: gate (G), drain (D), and source (S). The electron flow (current) from the drain (D) to the source (S) is controlled by the voltage at the gate (G).



Ex.-2025, p. 199.

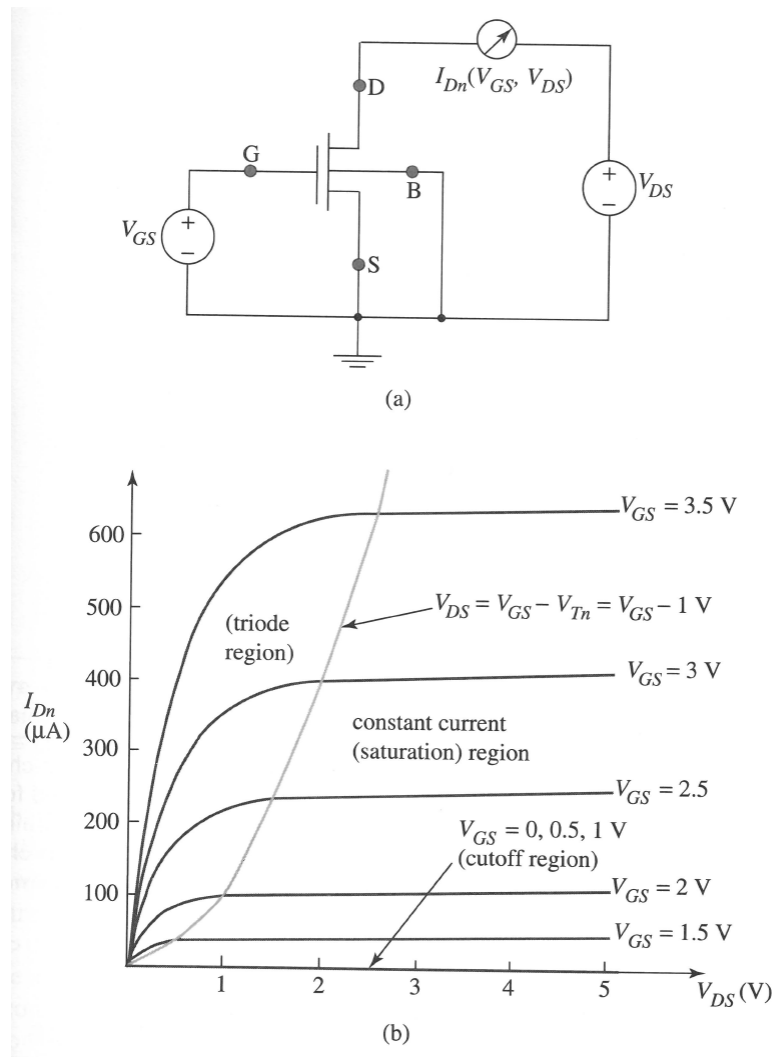
The symbol for n-channel and p-channel MOSFETs are shown below.

² Ex.-2021, ¶¶57-64.



Ex.-2025, 195.

NMOS MOSFETs have two primary regions of operation: (1) triode region and (2) saturation region, (shown below).



Ex.-2025, 197.

In saturation, the current flows only from the drain to the source (unidirectional).

3. Resistor³

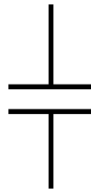
A resistor is a circuit element that introduces resistance into a circuit.

³ Ex.-2021, ¶¶65-67.



4. Capacitor⁴

A capacitor is one type of circuit element used to accumulate energy.



5. Electrical Load⁵

An electrical load is an electrical element or portion of a circuit that absorbs power and converts it into a desired form. A resistor is a type of load.

There are high impedance loads and low impedance loads. A high impedance load inhibits current from moving in a circuit. A low impedance load provides little constraint to current moving in a circuit and absorbs electrical energy.

6. Local Oscillator⁶

A local oscillator is used to create an LO signal. Ex.-2031, p. 5.

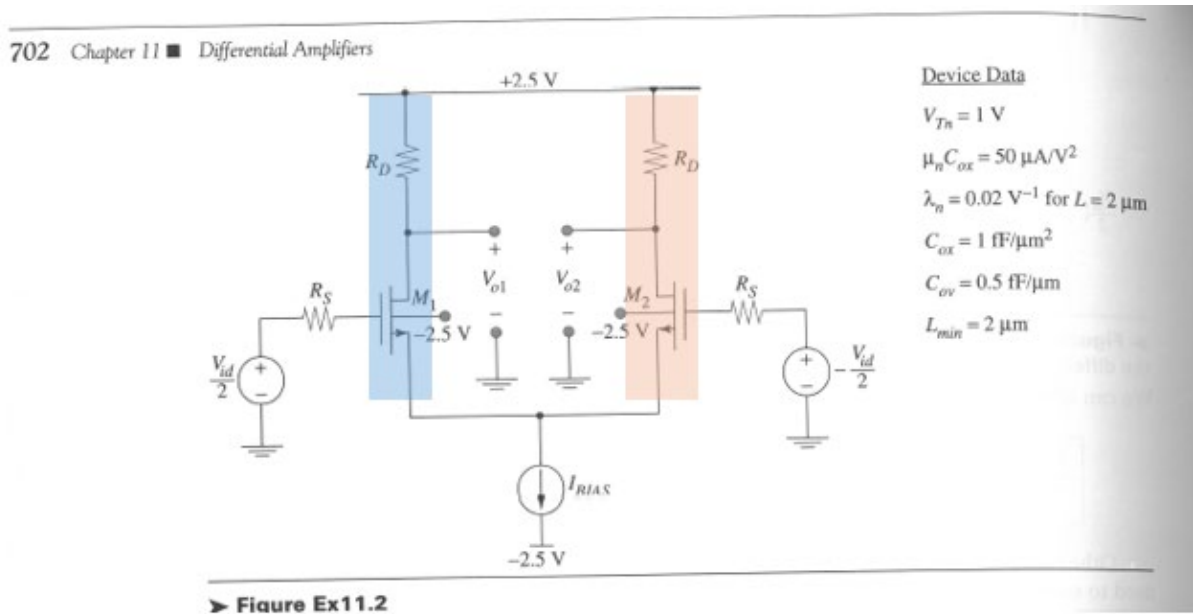
⁴ Ex.-2021, ¶¶68-74.

⁵ Ex.-2021, ¶¶75-77.

⁶ Ex.-2021, ¶¶78-82.

7. Differential Amplifiers⁷

A differential amplifier circuit amplifies a differential input signal using a “differential pair,” which consists of a pair of transistors (see below).



Ex.-2025, at p. 702.

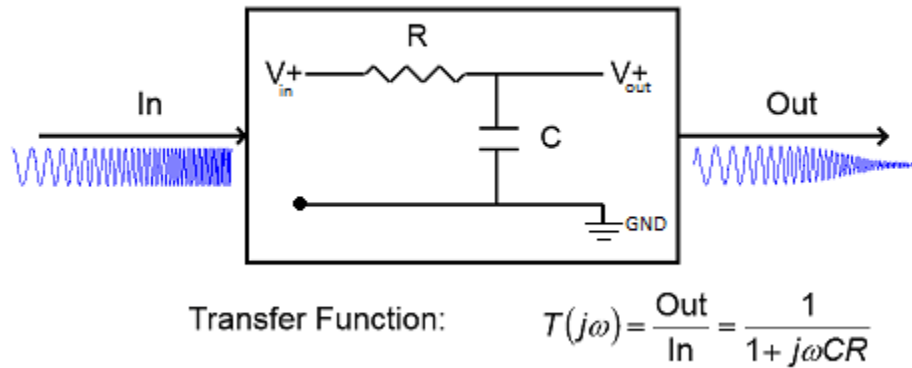
The differential input voltage (V_{id}) steers the current I_{BIAS} between the two branches (blue and red).

8. Low-pass Filter⁸

A low pass filter is a circuit that attenuates high-frequency signals while allowing low-frequency signals to pass through.

⁷ Ex.-2021, ¶¶83-90.

⁸ Ex.-2021, ¶¶91-92.



In the simple RC filter above, filtering is achieved due to the frequency-dependent impedance of the capacitor, C.

9. Transformers

A transformer is a passive electrical device that transfers electrical energy between two or more circuits through electromagnetic induction. Transformers are commonly used to increase (step-up) or decrease (step-down) voltage levels in a circuit while maintaining power balance. Ex.-2021, ¶93.

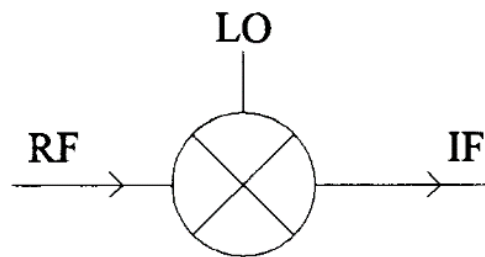
IV. DOWN-CONVERSION SYSTEMS

There are two types of down-conversion technology: (1) non-sampling/heterodyning; and (2) sampling-based down-conversion. Ex.-2021, ¶94.

A. Heterodyning (Non-Sampling)

Heterodyne receivers use non-sampling mixers that operate by continuously multiplying two sinusoidal signals—an incoming RF signal with a local oscillator (LO) signal. Ex.-2021, ¶¶95-97.

The typical symbol for a mixer is shown below. Ex.-2021,¶98.



A mixer converts a signal received at one frequency to another frequency. A local oscillator sends a signal to the mixer to effect down-conversion. Ex.-2021,¶¶99-107.

B. Sampling

Sampling-based down-conversion uses switches to capture discrete samples of the RF signal at specific time intervals. Ex.-2021,¶108.

Sampling-based down-conversion systems can be categorized into: (1) voltage sampling systems, and (2) energy transfer (energy sampling) systems. Ex.-2021,¶109.

1. Energy Sampling

Energy transfer (energy sampling) was/is a fundamentally different and competing method to voltage sampling. Energy samplers do not attempt to replicate or sample the voltage of an RF signal. Ex.-2021,¶¶115-116.

In ParkerVision's energy transfer system, non-negligible amounts of energy from an input signal (a radio frequency (RF) signal) pass through the switch and the

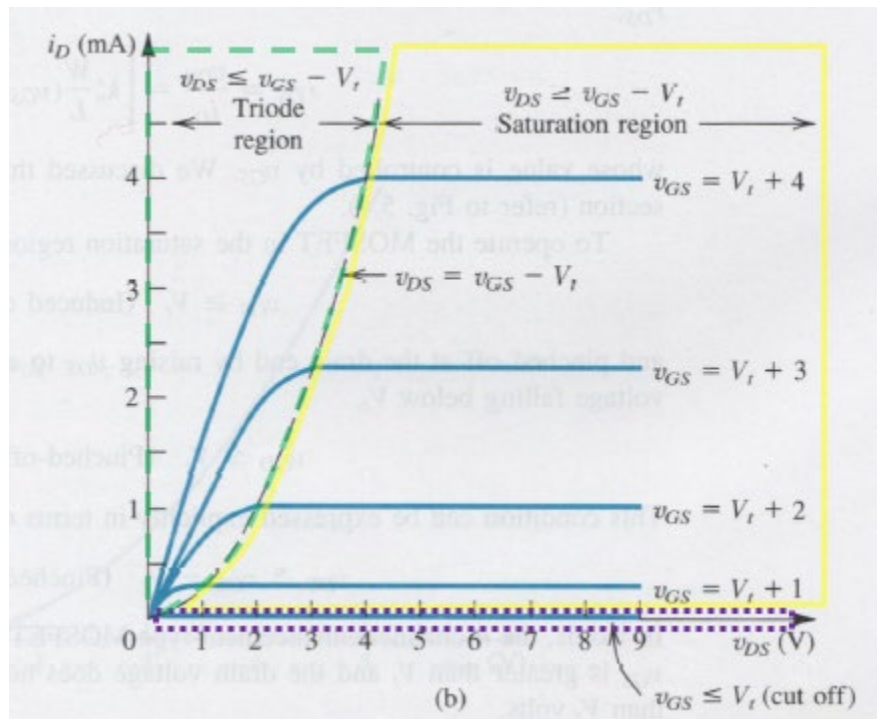
energy transferred itself to a load forms the down-converted (baseband) signal. In an energy transfer system, energy is integrated in a storage module (e.g., capacitor) and a low impedance load is used. This configuration allows energy to continuously flow to the low impedance load and forms the baseband signal. Energy flows from the switch when the switch is closed (ON) and from the storage module when the switch is opened (OFF). Ex.-2021, ¶117.

If the capacitor did not continue to drive the low impedance load, the energy transfer system would not work properly, and information would be lost. Ex.-2021, ¶¶118-120.

Energy sampling is an accurate way to form a baseband signal. What ParkerVision realized, and others did not, was that accurately capturing the voltage of the RF signal is not critical; it was actually undesirable. ParkerVision realized that using most or all of the available energy from the RF signal was the best way to form the baseband signal. Moreover, the baseband signal carries significant power because non-negligible energy is discharged from the capacitor for driving a low impedance load. Ex.-2021, ¶¶121-122.

V. OPERATION OF FETS

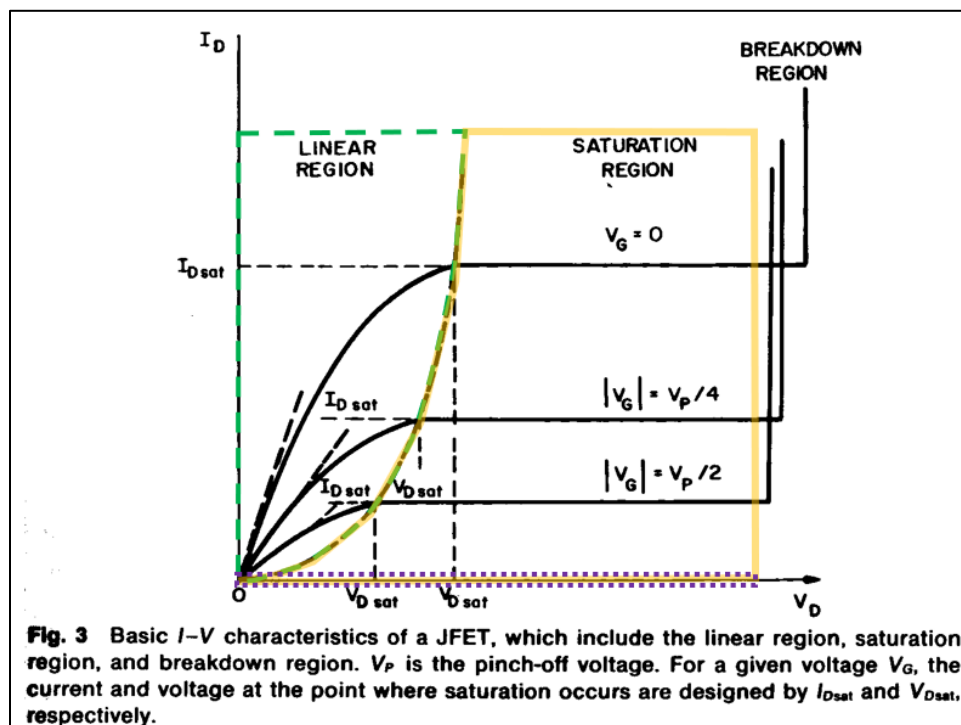
The function a FET performs depends on how it is configured within a circuit. Ex.-2021, ¶¶123-128.



Ex.-2035, 367.

One type of FET is a MOSFET having distinct regions of operation: (i) cutoff region (purple); (ii) triode region (green); and (iii) saturation region (yellow). Ex.-2021, ¶¶129-133.

Another type of FET is the junction field-effect transistor (JFET). Ex.-2021, ¶134.



Ex.-2038, 315.

A JFET exhibits similar behavior to a MOSFET, with three operational regions: (i) pinch-off region (dotted purple box); (ii) linear region (dashed green box); and (iii) saturation region (yellow box). Ex.-2021, ¶¶135-139.

VI. THE '342 PATENT

A. Overview

The '342 patent relates to a system/method to down-convert an electromagnetic signal (RF signal). Ex.-2021, ¶140.

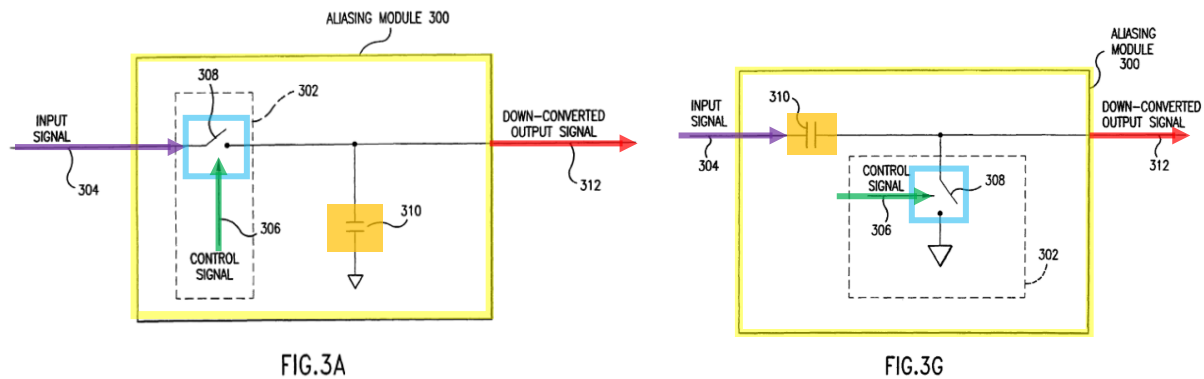
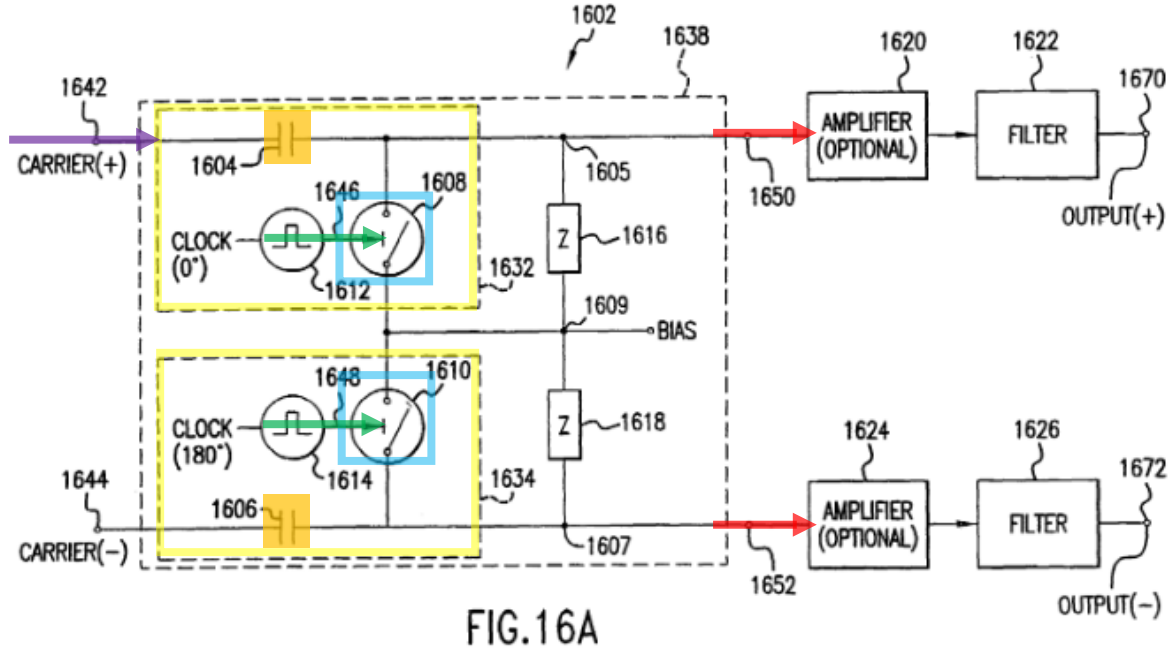


Figure 3A (above left) shows an aliasing module 300 for down-conversion. Ex.-1001, 7:31-33. Aliasing module 300 (yellow) includes (1) a universal frequency translation (UFT) module 302 (implemented as a switch 308 (blue) with a control signal 306 (green) for controlling the switch) and (2) a capacitor 310 (orange) for storing and discharging energy. *Id.*, 7:33-36. The switch receives an input signal 304 (purple arrow), samples the signal as discussed below, and outputs a down-converted output signal 312 (red arrow). The switch 302 is in series with input signal 304 and capacitor 310 is shunted to e.g., ground. *Id.*, 7:37-41. Ex.-2021, ¶141.

Figure 3G (above right) shows another configuration of the aliasing module 300. In this embodiment, capacitor 310 is in series with input signal 304 and the switch 308 is shunted to ground. *Id.*, 7:41-45. Ex.-2021, ¶142.

The configurations of Figures 3A/3G will operate in the same way. Ex.-2021, ¶143.

The '342 patent discloses receivers into which the aliasing module of Figures 3A/3G can be incorporated – e.g., receiver 7000, Figures 16A. Ex.-2021, ¶144.



Figures 16A illustrates a receiver 1602 that down-converts a modulated carrier signal. *Id.*, 18:6-9. Receiver 1602 receives a modulated carrier signal 1642 at its carrier (+) port. *Id.*, 19:56-57. The modulated carrier signal 1642 is inverted to generate signal 1644, which is input to carrier port (-) of receiver 1602. *Id.*, 19:62-63. The resulting output signal is a differential down-converted signal, formed by the sum of signals 1670 and 1672. *Id.*, 19:9-21. Ex.-2021, ¶145.

Receiver 1602 includes a universal frequency down-conversion (UFD) module 1638, a first optional amplifier 1620, a first low-pass filter 1622, a second optional amplifier 1624, and a second low-pass filter 1626. *Id.*, 18:9-12. The UFD module 1638 includes two aliasing modules 1632, 1634 (yellow)—each configured as shown in Figure 3G—and two impedances 1616, 1618 (resistors). *Id.*, 18:13-22.

Within each aliasing module, a capacitor 1604, 1606 (orange) and a switching device 1608, 1610 (blue) operate under the control of an aperture generator 1612, 1614, respectively. *Id.*, 18:34-37, 51-54. Ex.-2021, ¶146.

Input signal 1642, 1644 is provided to the input of aliasing module 1632, 1634, respectively. *Id.*, 18:39-41, 55-56. A switch in the aliasing module 1632, 1634 is turned ON (closes) and OFF (opens) based on a control signal 1646, 1648 (green), respectively. *Id.*; *see also id.*, 19:59-61, 66-67. As the switch opens and closes, a down-converted signal 1650 (red) is formed. *Id.*, 20:1-11. The down-converted signal 1650, 1652 may then pass through an amplifier 1620, 1624, respectively, and filter 1622, 1626, respectively. *Id.*, 20:12-17. Ex.-2021, ¶147.

The differential output signal of UFD module 1638 is formed by signals 1650 and 1652, which are 180 degrees out of phase. *Id.*, 20:11-13. The total output of receiver 1602 is the sum of these signals. *Id.* Ex.-2021, ¶148.

Figures 15/16H/160/17/18A/19/20A/20E/20F/21 illustrate other receiver embodiments using the aliasing modules of Figures 3A/3G. Ex.-2021, ¶149.

B. Down-conversion systems

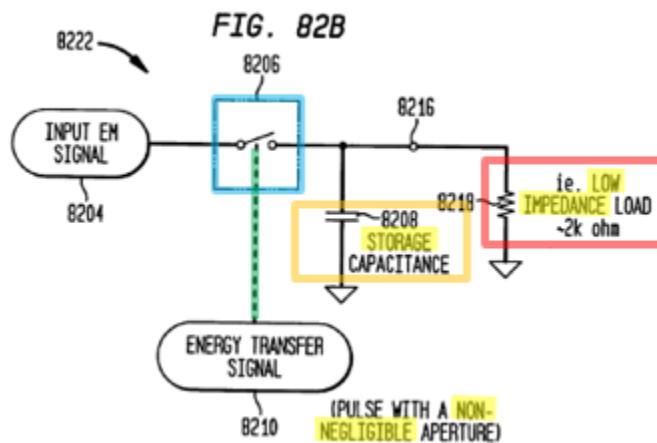
The disclosure regarding down-conversion in U.S. Patent No. 6,061,551 (“’551 patent”) (Ex.-2033) is incorporated by reference into the ’342 patent.

The '551 patent and, thus, the '342 patent, discloses two systems for down-conversion: (1) energy transfer (energy sampling) and (2) sample and hold (voltage sampling). Ex.-2021, ¶151.

Claims 19-21 of the '342 patent are directed to energy transfer. See Section VII.C. Ex.-2021, ¶¶152-153.

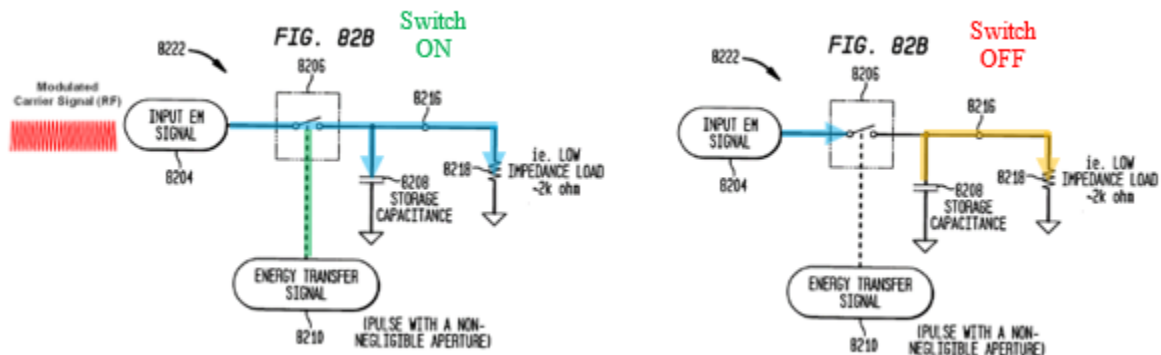
1. Energy Transfer (energy sampling)

Figure 82B of the '528 patent (below) illustrates an energy transfer (energy sampling) system, which would be incorporated into a transceiver chip of a wireless device. Ex.-2021, ¶154.

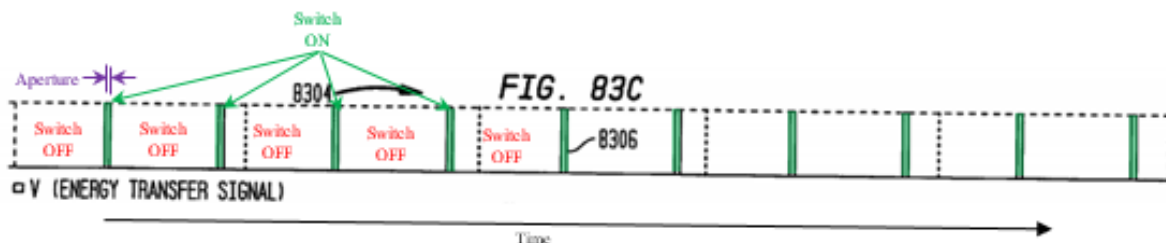


The system includes a switch 8206 (blue), an energy transfer signal 8210 (green) for controlling the switch, a “storage” capacitor 8208 (orange) for storing and discharging energy, and a low impedance load (red). Notably, there are several key features (yellow highlights) that distinguish an energy transfer system from sample and hold. In particular, an energy transfer system uses (1) a control signal

having a pulse with a non-negligible aperture/duration, and (2) a “storage” capacitor for storing and discharging non-negligible amounts of energy for driving a low impedance load. Indeed, low impedance is what enables a storage capacitor to discharge its energy when the switch is OFF (open). If the impedance were high, the “storage” capacitor could not discharge sufficient energy for the system to perform energy transfer (energy sampling) and form a down-converted signal from energy transferred to the low impedance load. Ex.-2021, ¶155.

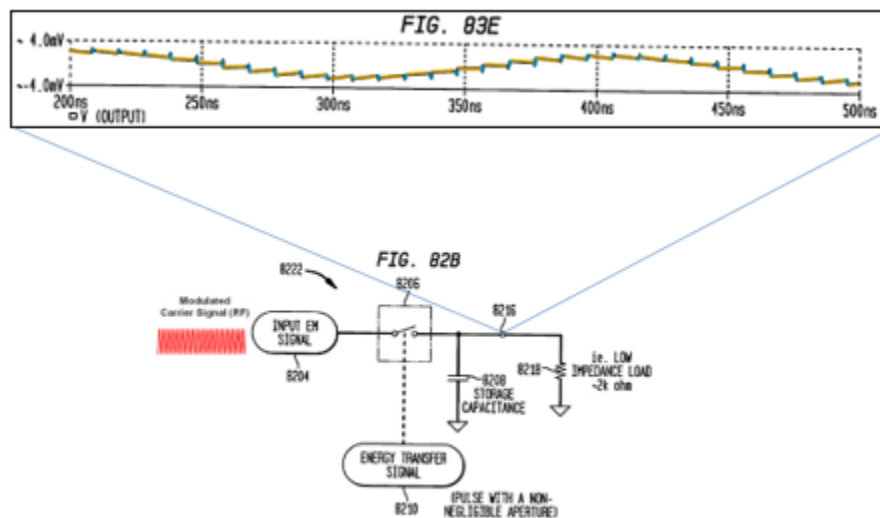


The annotations in Figure 82B above illustrate how an energy transfer system down-converts a high frequency input EM signal 8204 (e.g., modulated carrier signal (red)) to a baseband signal. In particular, down-conversion occurs by repetitively opening and closing the switch 8206. Ex.-2021, ¶156.

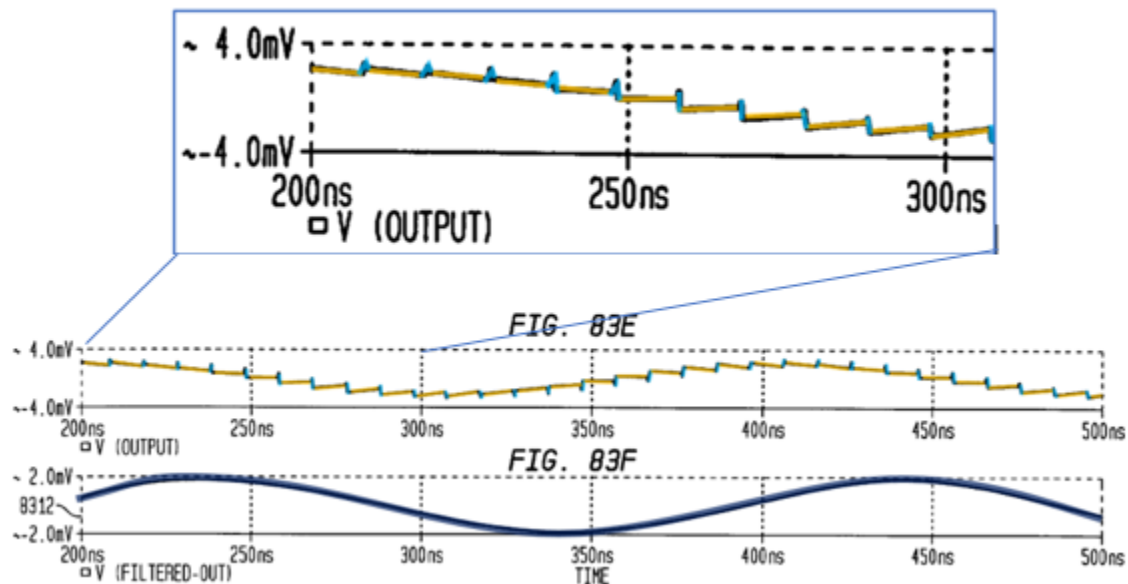


As shown in Figure 83C above, the switch is turned ON (closed) by sending a pulse 8306 (green) to the switch. The switch is kept ON (kept closed) for the duration of the pulse (i.e., a non-negligible aperture (purple) of the pulse). As shown by the repetitive pulses 8306, this opening and closing of the switch repeats continuously over time. Ex.-2021, ¶157.

As shown in Figure 82B above (left), when the switch is ON (during the aperture), a portion of the input EM signal 8204 (blue) passes to the “storage” capacitor 8208 and the low impedance load 8218. When the pulse 8306 (green) stops, the switch is turned OFF (opened), and the input EM signal is prevented from passing through the switch. Since the load is low impedance, when the switch is OFF (opened), as shown in Figure 82B above (right), energy (orange) stored in the “storage” capacitor 8208 is discharged to the low impedance load 8218. For this reason, the “storage” capacitor is said to “drive the load.” Ex.-1001, 73:65-74:2. Ex.-2021, ¶158.

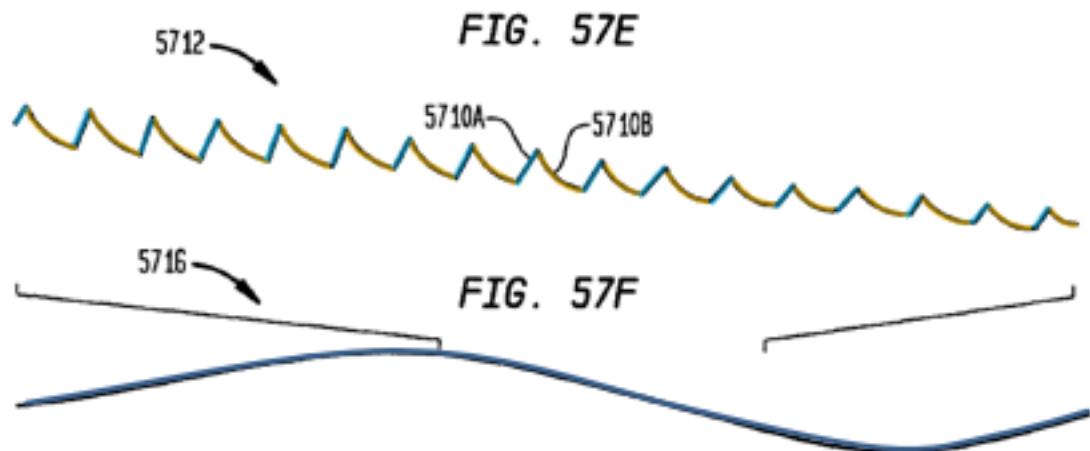


The repetitive opening and closing of the switch results in the waveform (blue/orange) shown above in Figure 83E at terminal 8216. The waveform is made up of energy (blue) from the EM signal and discharged energy (orange) from the “storage” capacitor. Indeed, the discharged energy (orange) from the “storage” capacitor is essential. Without the discharged energy, the waveform of Figure 83E would be incomplete (the orange portions would be missing), thereby producing a degraded and/or unusable signal that could not be properly processed by a receiving wireless device. Ex.-2021, ¶159.



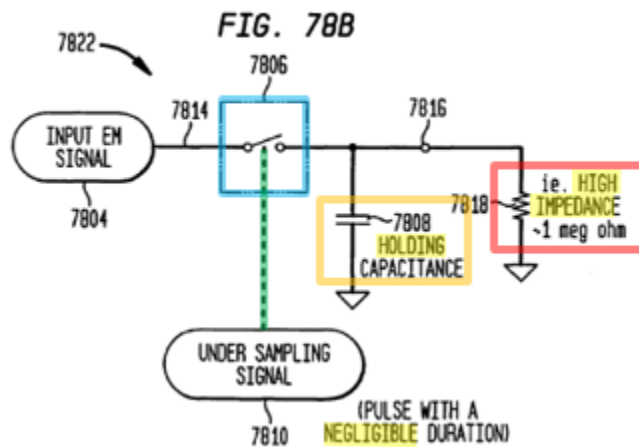
As shown above, the waveform of Figure 83E is filtered to create a smooth waveform (dark blue) as shown in Figure 83F. Ex.-2021, ¶160.

The figures below illustrate a close-up view of another embodiment of a down-converted signal in an energy transfer system. Ex.-2021, ¶¶161-162.

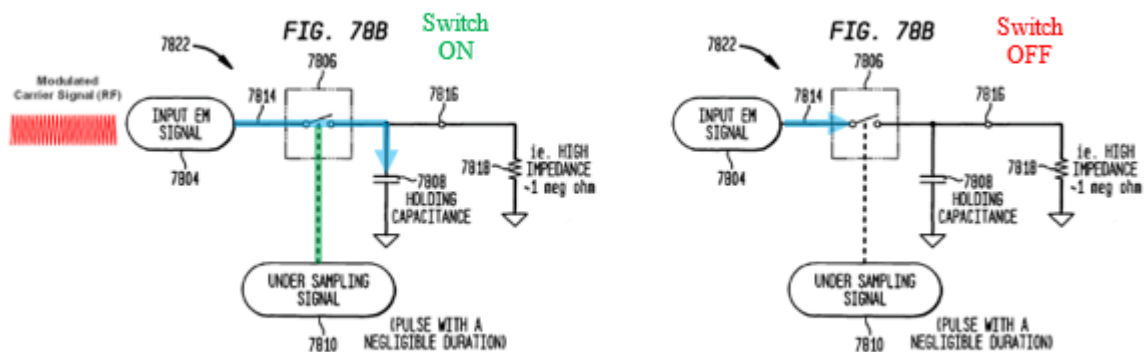


2. Sample-and-hold (voltage sampling)

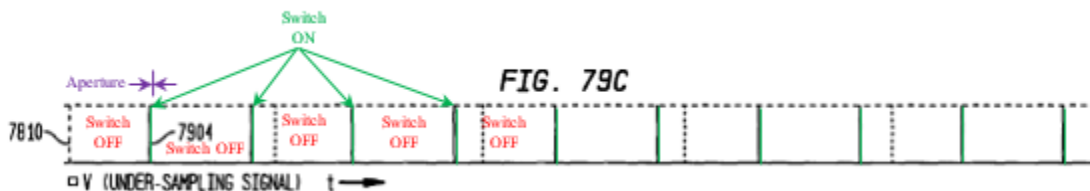
Figure 78B of the '528 patent illustrates a sample and hold (voltage sampling) system. Ex.-2021,¶163.



The system includes a switch 7806 (blue), a control signal 7810 (green) for controlling the switch, a “holding” capacitor 7808 (orange) for holding a voltage across the capacitor, and a high impedance load (red). A high impedance load is specifically included to prevent the holding capacitor from discharging energy. Ex.-2021,¶164.



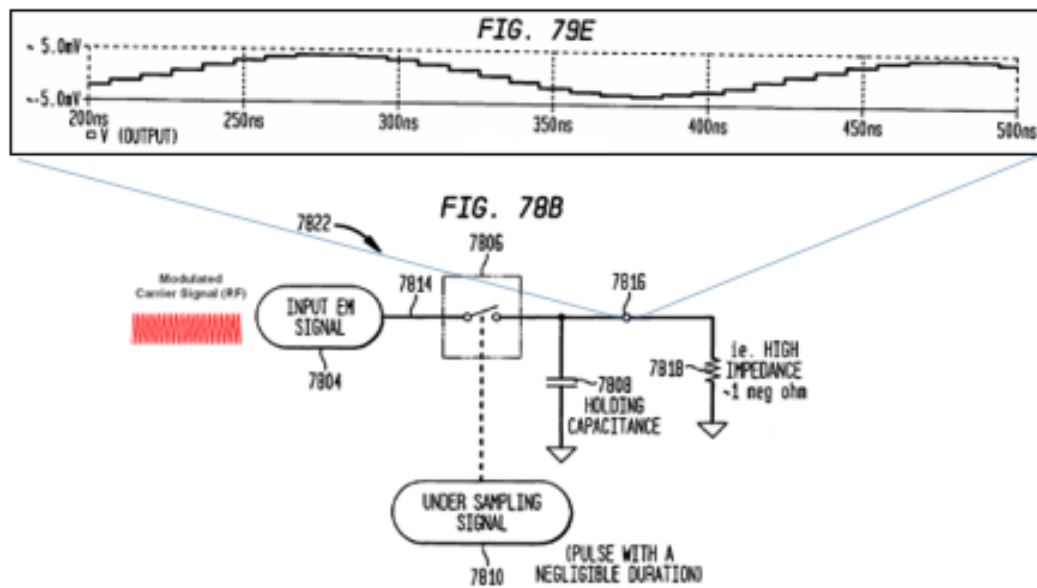
The annotations in Figure 78B illustrate how a sample and hold system down-converts a high frequency input EM signal 7804 (e.g., modulated carrier signal (red)) to a baseband signal. Ex.-2021,¶165.



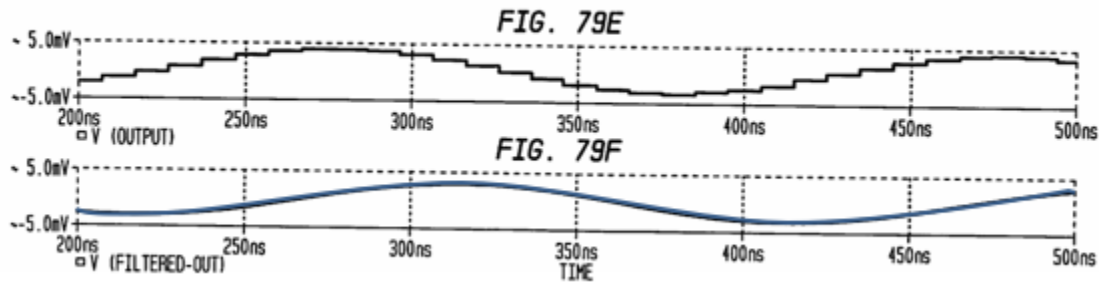
As shown in Figure 79C, the switch is turned ON (closed) by sending a pulse 7904 (green vertical line) of an extremely short/negligible duration to the switch. Thus, the aperture (purple) of a pulse is referred to as a negligible aperture because the pulse width “tend[s] toward zero time.” Ex.-1001, 70:2-4. As shown by the repetitive pulses 7904, this opening and closing of the switch repeats continuously over time. Ex.-2021,¶166.

As shown in Figure 78B above, when the switch is ON (closed) (during the aperture), the EM signal 8204 (blue) is sent to the “holding” capacitor 7808. When the pulse 7904 (green) stops, the switch is turned OFF (opened). But unlike energy transfer (energy sampling), since sample and hold uses a high impedance load, when the switch is OFF (opened), there is high resistance to the flow of current. Ex.-2021,¶167.

Because there is no significant energy discharge between pulses, the terminal 7816 maintains a constant voltage value until the next pulse. Ex.-1001, 70:43-48. The voltage value serves as the “sample” of a discrete voltage value that the system uses to recover the baseband signal. Ex.-2021, ¶168.



As shown in Figure 79E, sample and hold produces a voltage wave with a stair step pattern. The vertical part of the step represents the “sample” of the voltage value which occurs at the time of pulse 7904. The horizontal portion of the step represents the “holding” of that voltage value until the next pulse when the next sample of voltage is taken. Id., 70:48-52. Ex.-2021, ¶¶169-170.



C. Claims 19-21 are directed to an energy transfer system

Claims 19-21 of the '342 patent specifically recite various elements that are specific to an energy transfer system.

Claim 18 recites “*performing a plurality of charging and discharging cycles of the first and second capacitors to generate first and second down-converted information signals across first and second impedance devices.*” Further, claims 19-21 recite significant percentage discharge from the capacitors – 6% or more of the total charge stored – when a switching device is open (OFF).

The '342 patent only discloses two types of systems – an energy transfer system and a voltage sampling system. Energy transfer systems discharge significant amounts of charge/energy when a switching device is open. See Sections V.B.2, VII.B.1. Voltage sampling systems do not discharge stored charged when a switching device is open. In a voltage sampling system, current is held on the capacitor when the switching device is open. See Sections V.B.1, VII.B.2; Ex.-1001, 37:60-38:15. Ex.-2021, ¶173.

Because there are only two disclosed systems and voltage sampling does not discharge when a switching device is open, the only system that can be covered by claims 19-21 of the '342 patent is an energy transfer system. Ex.-2021,¶174.

Notably, the Federal Circuit recently held that ParkerVision's energy transfer/sampling technology is different from voltage sampling: "ParkerVision's down-converting system uses a technique called 'energy sampling,' which differs from the technique of 'voltage sampling,' which was used in conventional down-converting systems." *ParkerVision Inc. v. Qualcomm Inc.*, 116 F.4th 1345, 1349 (Fed. Cir. 2024).

VII. CLAIM CONSTRUCTION

A. Switching Device

The PTAB previously construed "switch" to mean "an electronic device for opening and closing a circuit." *Intel Corp. v. ParkerVision, Inc.*, IPR2021-00346, Paper 33, at 25-26 (PTAB July 20, 2022), *aff'd*, *ParkerVision, Inc. v. Vidal*, No. 2022-2173, slip op. at 2 (Fed. Cir. 2024). The same definition should apply to "switching device."

B. Electrically Coupling

Claim 19-21 recite "electrically coupling" an information signal to capacitors. The PTAB previously construed the term "electrically coupling" to mean "indirectly

or directly connecting such that an electric signal can flow between.” *Farmwald v. ParkerVision, Inc.*, IPR2014-01107, Paper 7, p. 10 (Jan. 8, 2015).

Connecting the information (electric) signal to the capacitors allows the signal to flow to the capacitors. Not only can coupling be a direct connection but the specification makes it clear that the signal can also be *indirectly* connected to a capacitor through a switching device. See Ex.-1001, Figure 16H (and corresponding description), 49:56-64.

C. Controlling a Charging and Discharging Cycle

The term “controlling a charging and discharging cycle” should be given its plain and ordinary meaning. Ex.-2021, ¶182.

Petitioner, however, seeks to incorporate a specific timing of charging and discharging by improperly inserting the word “then” into the claim language: “controlling a cycle of charging and *then* discharging.”⁹ Pet., 5.

Petitioner asserts that “the alleged invention is always either charging or discharging, and never simultaneously both charging and discharging.” *Id.* Not so.

Petitioner ignores the claimed embodiment where two switches and two capacitors are being used. In this embodiment, the first and second capacitors can

⁹ Unless otherwise noted, all emphasis has been added.

operate simultaneously but on opposite schedules – i.e., the first capacitor can be charging while the second capacitor is discharging and vice versa. Ex.-2021, ¶185.

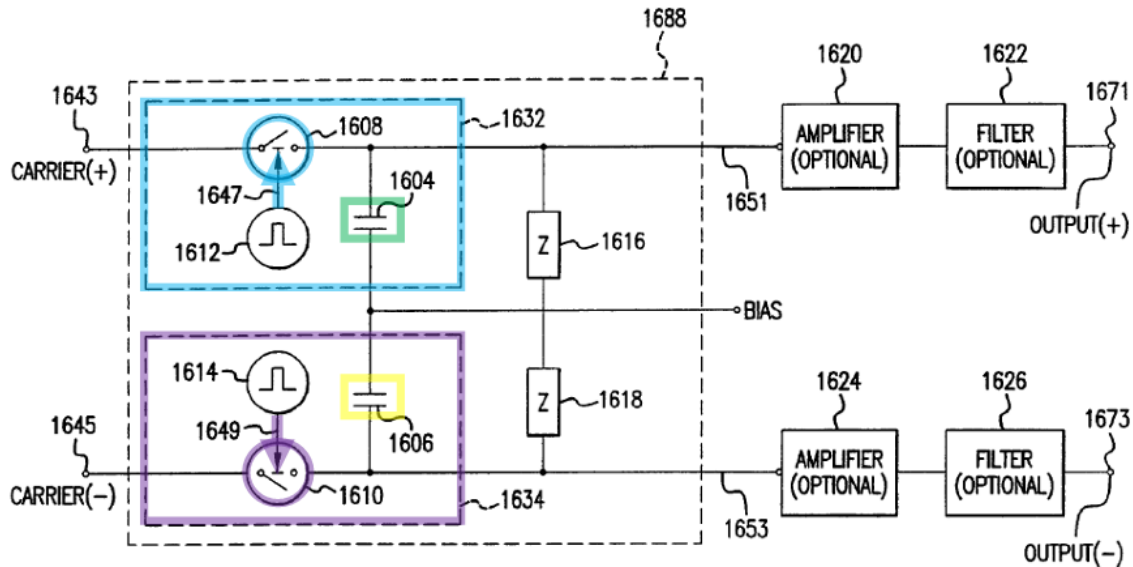


FIG. 16H

For example, Figure 16H (above) illustrates a receiver having a first aliasing module 1632 (blue box) and a second aliasing module 1634 (purple box). Ex.-1001, 18:13-15; 20:33-39; 21:27-31. Ex.-2021, ¶186.

The first aliasing module 1632 (blue box) includes a first switching device 1608 (blue circle) and a first capacitor 1604 (green box). The second aliasing module 1634 (purple box) includes a second switching device 1610 (purple circle) and a second capacitor 1606 (yellow box). *Id.*, 18:34-36. Ex.-2021, ¶187.

The switching device 1608, 1610 is turned ON (closed) and OFF (open) based on a control signal 1647, 1649, respectively. The closing and opening of the

switching device 1608, 1610 controls the charging and discharging of their corresponding capacitors 1604, 1606, respectively. *Id.*, 49:64-50:25. Ex.-2021, ¶188.

Petitioner's construction requires that the charging/discharging cycles of both first and second capacitors are synchronized. That is not how the technology works. Ex.-2021, ¶189.

The specification explicitly states that the apertures of the control signals for the first and second switching devices “do not overlap” and are “180 degrees out of phase.” *See, id.*, FIG. 16I, 18:59-61; 19:48-53; 20:40-43. This means that the first and second switching devices do not turn ON and OFF at the same time. Instead, while one capacitor is charging (due to the first switch being ON (closed)), the other is discharging (due to the second switch being OFF (open)), and vice versa. Ex.-2021, ¶190.

VIII. THE ALLEGED PRIOR ART

A. DeMaw

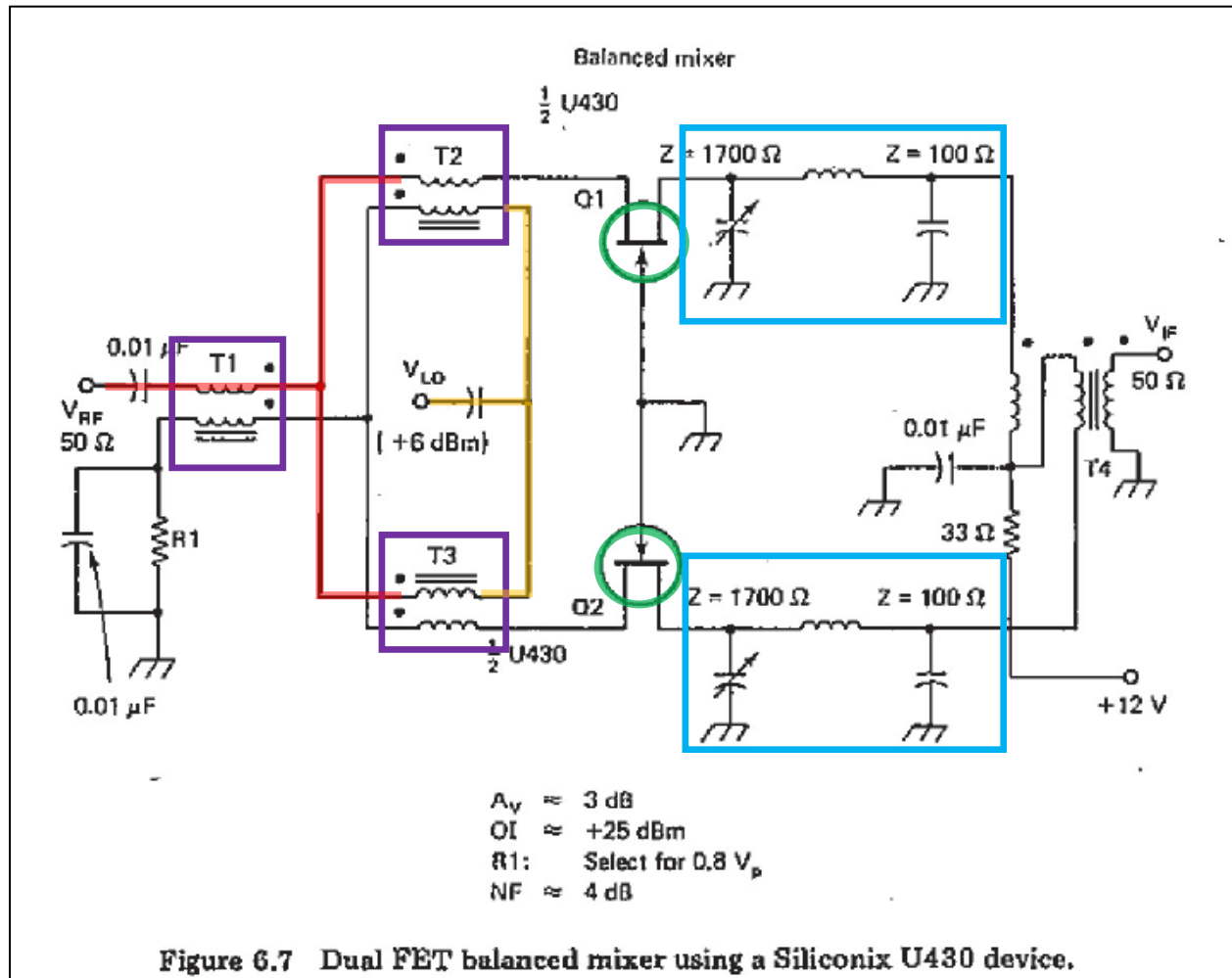


Figure 6.7 in DeMaw illustrates a dual FET balanced mixer using a Siliconix U430 device. *Id.*, 196. Figure 6.7 includes an RF input (V_{RF} (red path)), an LO input (V_{LO} (orange path)), transformers (T1, T2, and T3 (purple boxes)), transistors (Q1 and Q2 (green circles)), and low-pass matching networks (blue boxes). Ex.-2021, ¶¶191-196.

The RF signal (V_{RF}) passes through transformer T1, which splits the signal into two paths that feed into the left side of transformers T2 and T3. The LO signal (V_{LO}) splits at a node and is applied to the opposite (right) side of transformer T2 and T3. The outputs of transformers T2 and T3 combine the RF and LO signals, facilitating the mixing operation. Ex.-2021, ¶¶197-199.

As discussed above in Section IV.A.1 and VI, a JFET is a three-terminal device that controls the flow of current between its drain and source based on the voltage applied to its gate. Ex.-2021, ¶200.

A POSITA understands that a JFET operates in different modes depending on the gate-source voltage (V_{GS}). When $V_{GS} = 0V$, the JFET is in its fully conducting “ON” state, allowing current to flow freely. As V_{GS} becomes more negative, the conducting channel narrows, restricting current flow. If V_{GS} reaches a critical threshold called the pinchoff voltage (V_P or $V_{GS(OFF)}$), the JFET effectively turns off, blocking current flow. Ex.-2021, ¶¶201.

DeMaw specifically teaches that resistor R1 is selected so that V_{GS} remains at 80% of the pinchoff voltage. Ex.1016, 196. (“R1 is selected to give a V_{GS} of 0.8 the pinchoff voltage....”). A POSITA would understand that this design choice ensures that transistors Q1 and Q2 remain in a conductive state, and do not turn off. Ex.-2021, ¶202.

B. U.S. Patent No. 7,065,327

Macnally discloses a direct conversion transceiver. Ex.-1021, Abstract.

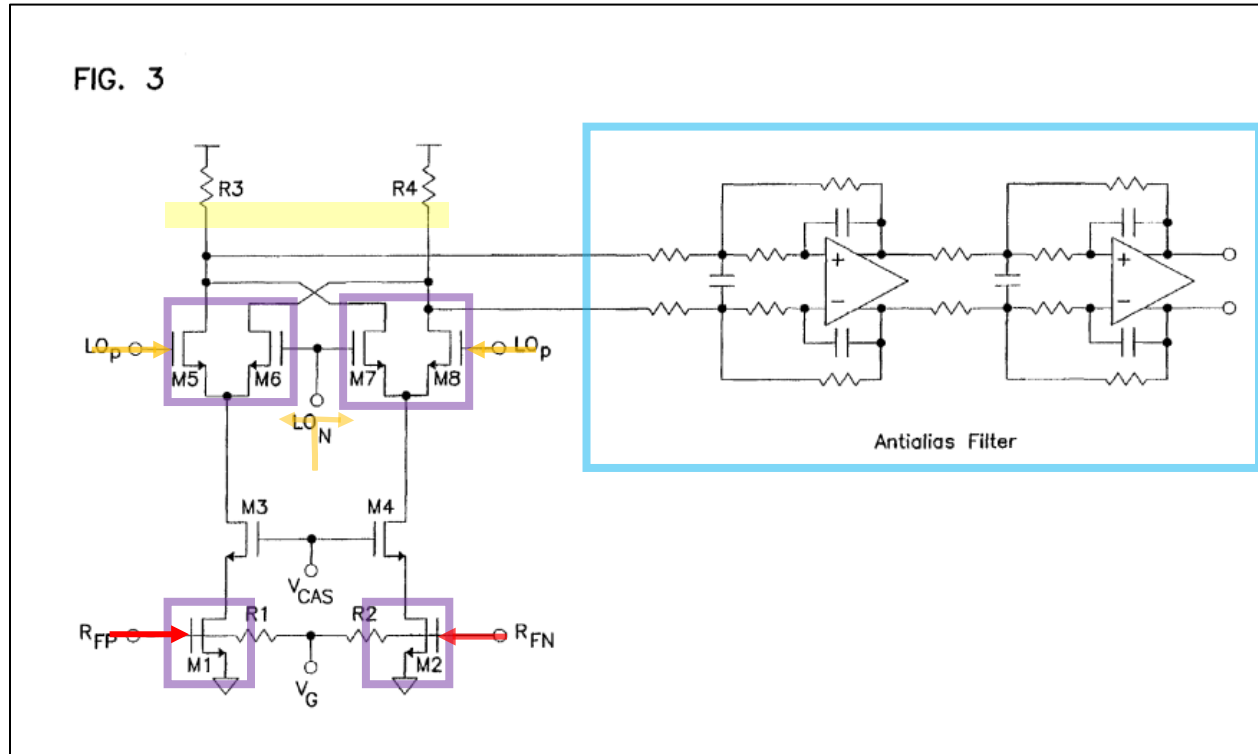
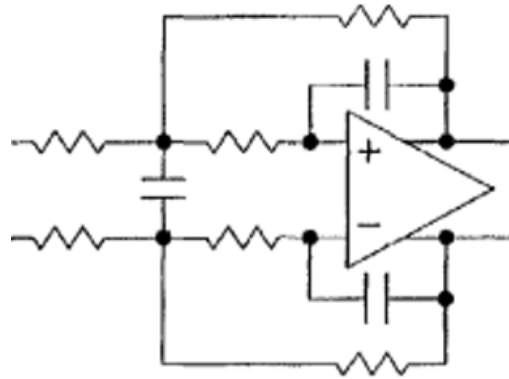


Figure 3 illustrates a circuit diagram of a Gilbert cell double-balanced mixer and antialias filter (blue box). Ex.-1021, 7:7-16; Ex.-2034, 57:17-58:5. Ex.-2021, ¶¶205, 207.

The circuit includes a differential RF input signal (red paths), differential LO signal (orange paths), and transistors (purple boxes). Id.



The antialias filter is made up of two biquad two-pole filters (one filter is shown above). Ex.-1021, 7:17-29; Ex.-2034, 56:14-57:5, 288:9-14. Ex.-2021, ¶206.

As shown in Figure 3, signals R_{FP} and R_{FN} are applied to the gates of transistors M1 and M2, respectively. Ex.-2021, ¶208.

Transistors M5, M6 and M7, M8 in Figure 3 are driven by a differential LO signal (labeled LO_p and LO_n). Local oscillators are typically sinusoidal waveforms or near-sinusoidal waveforms. Ex.-2021, ¶209.

The LO signals LO_p and LO_n are applied to the gates of transistors M5, M8, and transistors M6, M7, respectively. “The LO input transistors [M5, M6, M7, M8] operate as switches that steer a process and temperature independent current.” *Id.*, 7:12-14. Ex.-2021, ¶210.

Because Macnally's mixer circuit provides gain (conversion gain of 14.3dB, Ex.-1021, 7:8), a POSITA would understand that the mixer is an active non-sampling mixer, using the NMOS FETs as voltage-controlled current sources. *See*

Section V. This enables the circuit to amplify the signal while performing frequency conversion. Ex.-2021, ¶211.

Because Macnally's active mixer has high gain, Macnally is not transferring the RF input signal or its energy to the output of the mixer. Rather, Macnally creates a new output signal based on the input signal and its modulation information and adds gain to create a copy of that information signal at the output of the mixer. Macnally is using energy from a power supply (shown in yellow above) to accomplish this. In other words, unlike an energy sampling (transfer) system, the output signal energy in Macnally comes from a power supply, not from sampled energy of the RF input signal itself. Ex.-2021, ¶212.

Transistors M1-M8 are NMOS field-effect transistors (FETs) because they use the symbol for NMOS FETs. The RF input signal is applied to the gates of M1 and M2. The drain terminals of M1 and M2 are connected to the power source (yellow box) through resistors R3 and R4. Ex.-2021, ¶213.

FIG. 3

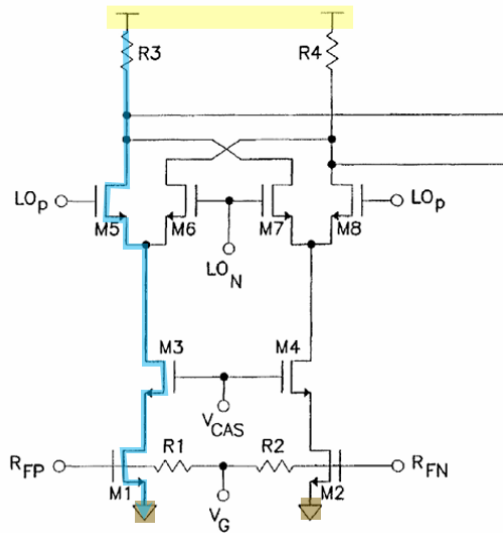
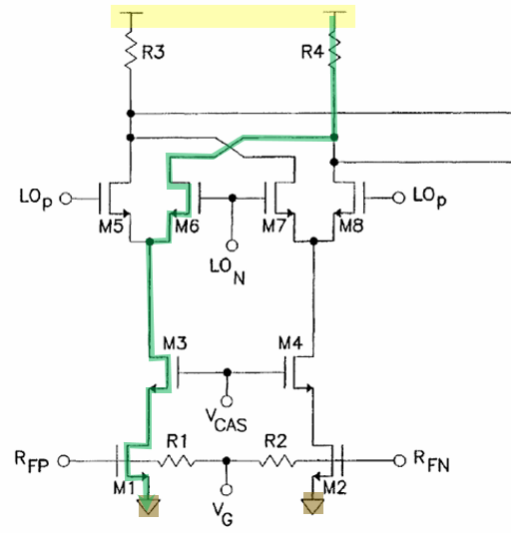


FIG. 3



A POSITA understand that transistors M5, M6 form a well-known circuit topology known as a differential pair. Transistors M7, M8 also form a differential pair. Ex.-2021, ¶214.

A POSITA would also understand that transistors M5, M6 and M7, M8 pass a DC current that flows from the power source (yellow) to ground (brown triangles). As shown above by the blue arrow, current flows downward through resistor R3 and transistors M5, M3, M1 (in the direction of the arrows of the transistors). As shown above by the green arrow, current flows downward through resistor R4 and transistors M6, M3, M1 (in the direction of the arrows of the transistors). Similarly, current flows downward through R3, M7, M4, M2 and R4, M8, M4, M2. Ex.-2021, ¶215.

There is always current flowing downward from the power source to ground. In other words, current is always flowing through M1 and M2 to ground. In particular, a POSITA understands that Macnally uses a 50% duty cycle LO. This means that 50% of the time current flows from R3 to M5 to M1 and simultaneously from R3 to M7 to M2. The other 50% of the time, current flows from R4 to M6 to M1 and simultaneously from R4 to M8 to M2. Ex.-2021, ¶216.

A POSITA understands from fundamental circuit theory that the current flowing from the power source to ground must be direct current (DC). DC is the non-time varying (non-RF) current that provides the bias and operating points for M5, M6 and M7, M8. Ex.-2021, ¶217.

The transistor pair M5, M6 operates by steering current from the power source through either R3 and M5 or R4 and M6, depending on the local oscillator (LO) signal applied to their gates. As the LO signal varies, it modulates the gate voltages of M5, M6 which, in turn, affects the flow of current through them. When the gate voltage of M5 is substantially greater than that of M6, current flows from the power source, through R3 and M5, and down through M1 to ground. Conversely, when the gate voltage of M6 is substantially greater than that of M5, current flows from the power source, through R4 and M6, and down through M1 to ground. Therefore, M5 and M6 serve as a current-steering mechanism that routes current from the power source through either R3 or R4 before reaching M1. Ex.-2021, ¶218.

The switching pair M7, M8 works the same way as M5, M6 to steer current except that the current passes through M2 to ground. Ex.-2021, ¶219.

The RF input signal (R_{FP} and R_{FN}) modulates the gate voltage of M1 and M2, respectively, which, in turn, affects/modulates the flow of current from the power source to ground. Ex.-2021, ¶220.

A POSITA understands that in order for Macnally to achieve high gain, M5, M6 and M7, M8 must remain in saturation. A POSITA understands that for an NMOS transistor to remain in saturation, the drain-to-source voltage must be positive, meaning current can only flow from the drain to the source. *See* Section III.A.2. Therefore, a POSITA would understand that, in the NMOS transistors used in Macnally, current flows from the drain to the source, not in the opposite direction. Current cannot flow upward from the drains of M1 and M2 toward M5-M8. Ex.-2021, ¶221.

Further, because the RF input signal is applied to the gates of M1 and M2, a POSITA understands that the gate terminal controls the flow of current through the channel but does not conduct current itself. No current flows from the gate into the drain; rather, the RF signal modulates the drain-to-source current, which continues to flow in the downward direction only. Thus, current cannot—and does not—flow upward through the NMOS transistors, nor from the gate into the drain. Ex.-2021, ¶222.

A POSITA further understands that in Macnally, current flows from the power source downward towards M1 and M2—from a higher potential to a lower potential. Ex.-2021, ¶223.

While M1 and M2 can modulate the amount of current flowing downward from the power source, they do not reverse the current flow direction. No current flows upward through M1 or M2 toward the power source. Because the RF input signal is at the gate of a FET, neither the RF input signal nor its current/energy propagates upward towards M5, M6, M7, M8 or R3, R4. Ex.-2021, ¶224.

To circumvent this fact, Dr. Galton appears to assert that a signal flows upward in the circuit. Ex.-1003, ¶¶134, 137, 146, 148. Not so. While current flowing downward from the power source to ground is affected by the RF input signal, the current remains unidirectional—always flowing downward to ground. There is never a scenario in which current from the RF input signal flows from M1, M2 toward the power source or the capacitors in the antialias filter. Ex.-2021, ¶225.

IX. SIMULATIONS

A. Overview

Dr. Galton's declaration (Ex.-1003) provided simulations that purported to model the mixer circuits disclosed in DeMaw and Macnally.¹⁰

¹⁰ The simulations in Ex-1003 are referred to herein as DeMaw-1 and Macnally-1.

On August 29, 2024, ParkerVision filed its Patent Owner's Preliminary Response (POPR), which identified material mistakes in Dr. Galton's simulation setup and analysis.

Then, during his February 28, 2025 deposition, Dr. Galton acknowledged that he had mistakenly used the wrong transistor model in his DeMaw simulations. Ex.-2036. He also indicated that he ran other simulations with various modifications in response to criticisms in the POPR. *Id.* He offered to share these newly created simulations. *Id.*

ParkerVision initially declined to accept these simulations because they were untimely, had not been previously disclosed, and fell outside the evidentiary record.

After the deposition, Petitioner offered to provide new simulations using the correct transistor model. Ex.-2040. Because ParkerVision believed these new simulations would be included with Petitioner's Reply Brief and ParkerVision's expert (Dr. Ricketts) may not get the opportunity to address these new simulations in ParkerVision's sur-reply, ParkerVision contacted the Board for guidance on how to proceed. Ex.-2041.

The parties had a conference call with the Board. The Board indicated that it could not rule on the admissibility of the new simulations until the Petitioner filed

them. Given the uncertainty as to whether the new simulations would be permitted, ParkerVision requested that Petitioner produce any new simulations so that Dr. Ricketts could consider and respond to them.

On March 17, 2025, Petitioner served additional materials from Dr. Galton, including a Second Declaration (Ex.-2039, Ex.-1) and the native Python code used for simulations (*Id.*, Ex.-2). The Second Declaration included dozens of new simulations purportedly prepared in response to criticisms in the POPR. The Second Declaration also presented new simulated circuits for DeMaw with changes to the circuit topology/component values, as well as additional simulations of the Macnally circuit.¹¹

Having provided flawed simulations in his original Declaration and recognizing that he is not allowed to provide new theories, Dr. Galton now asserts that his new simulations merely show the same simulation output and support his original declaration. As shown below, this is demonstrably false. The new simulations and their outputs are materially different from Dr. Galton's original simulations.

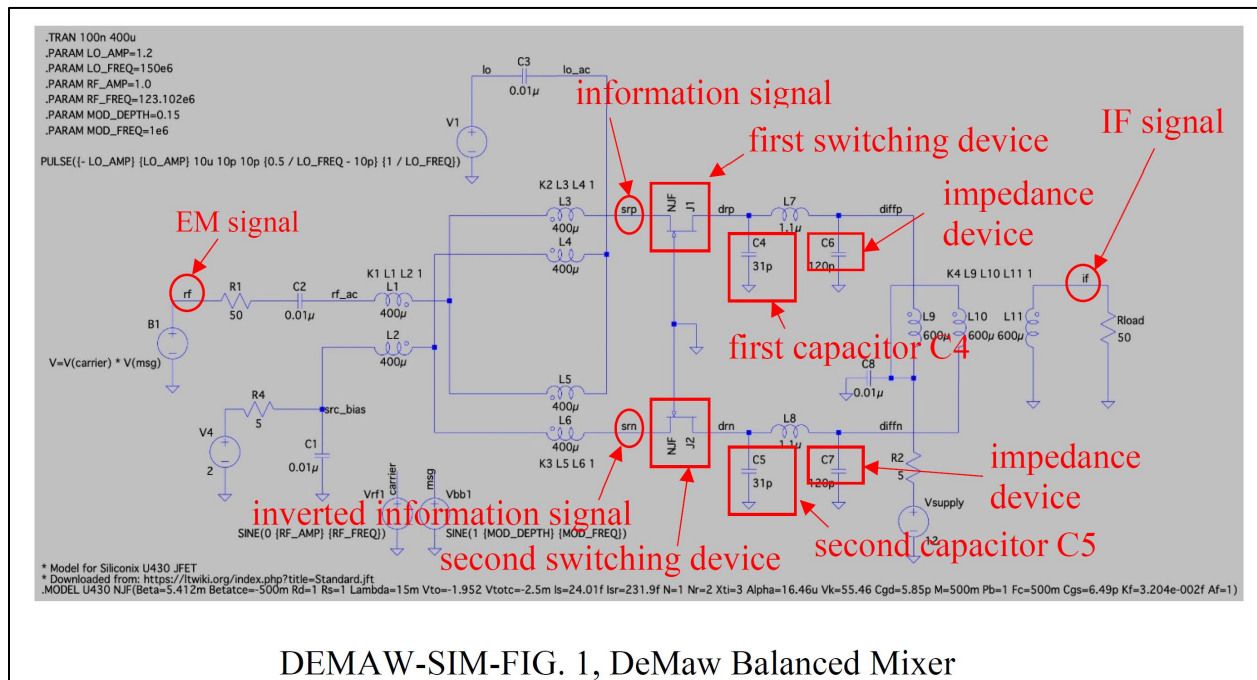
¹¹ The simulations in Second Declaration are referred to herein as DeMaw-2 and Macnally-2.

Because Dr. Galton could have performed all of his new simulations in his original Declaration (Ex.-1003), these new simulations should be struck if submitted with Petitioner's Reply Brief.

B. DeMaw-1

1. Dr. Galton's Original Simulations

Dr. Galton simulated DeMaw's circuit using LTSpice¹² with the setup shown in DEMAW-SIM-FIG. 1 (below). Ex.-1003, ¶¶72. Ex.-2021, ¶¶227.



Because Dr. Galton did not provide the necessary back-up materials with his Declaration, Dr. Ricketts had to replicate this circuit. In doing so, Dr. Ricketts was able to determine that Dr. Galton's setup deviated significantly from DeMaw's

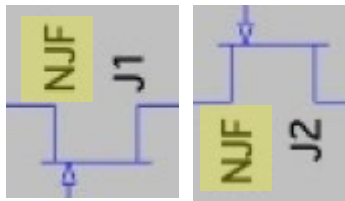
¹² LTSpice is circuit simulator software.

circuit. These deviations render Dr. Galton's simulations inaccurate and unreliable.

Ex.-2021, ¶¶228-229.

a. JFET Model

Though Dr. Galton purported to simulate DeMaw's dual JFET mixer in his original declaration, he does not do so. Ex. 2034, 44:6–20; 24:21–25:2. Instead, of using the Siliconix U430 model specifically disclosed in DeMew, as shown below, Dr. Galton used a default, generic N-channel JFET provided by LTspice (labeled "NJF"). Ex.-2021, ¶¶230-231.



If Dr. Galton has used/loaded the correct transistor model (Siliconix U430), the schematic would have shown "U430" (or the corresponding filename). Ex.-2021, ¶232.

As discussed in Section IX.B, using the incorrect JFET model materially affected the operation of the transistors. Ex.-2021, ¶¶233-235.

b. Local Oscillator Signal

Dr. Galton modeled the LO signal in his simulation as "a *square wave* of 150 MHz and amplitude of 1.2V peak." Ex.-1003, ¶74. Specifically, the LTspice

configuration uses the following command, which would generate a square wave.

Ex.-2021, ¶¶236-237.

```
PULSE({-LO_AMP} {LO_AMP} 10u 10p 10p {0.5/LO_FREQ-10p} {1/LO_FREQ})
```

Dr. Galton alleges that “ V_{LO} can be considered a periodic waveform with fundamental frequency f_{LO} (DeMaw 3.A.1) (or a squared-up version of a sinusoid thereof, as described in Section VII).”¹³ Ex.-1003, ¶69. To justify the use of a square wave, Dr. Galton cites to his own 2019 paper. Ex. 1003, ¶37. Dr. Galton’s 2019 paper, however, does not show the state-of-the-art knowledge at the time of the ’342 patent. Ex.-2021, ¶¶238-239.

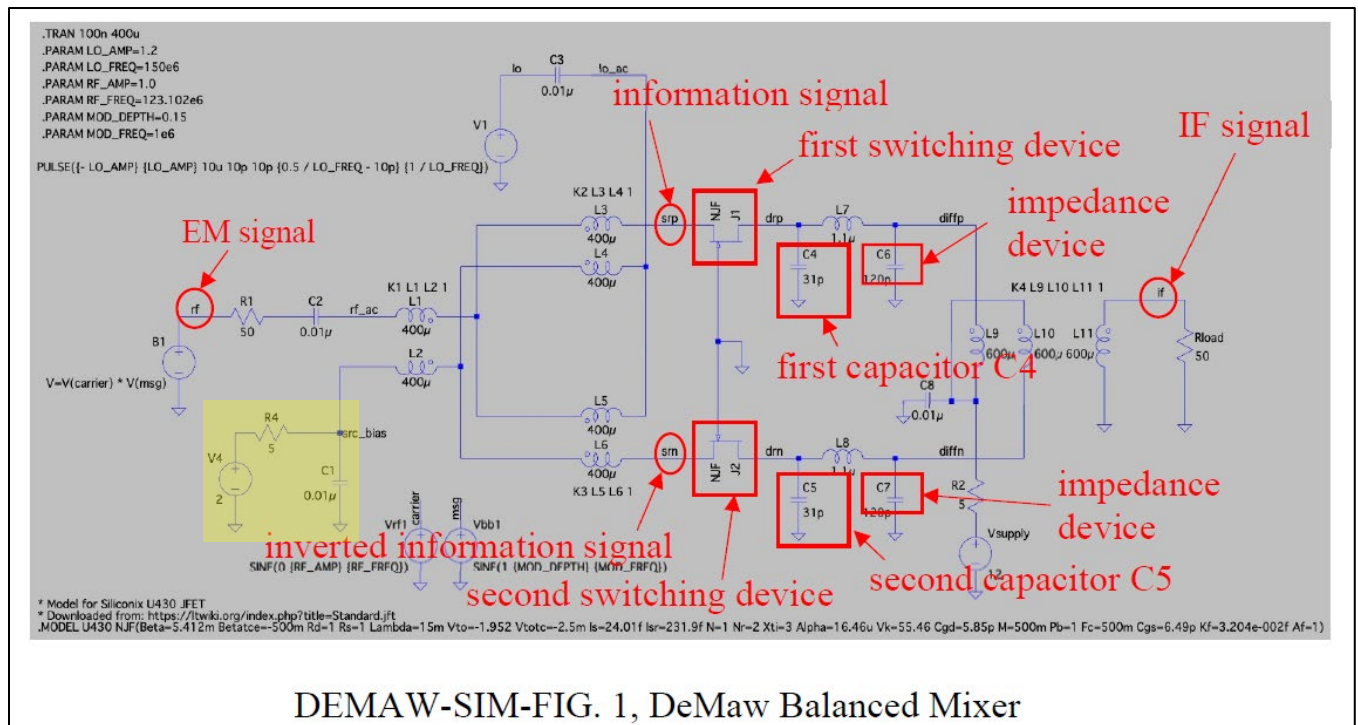
Indeed, DeMaw itself provides no basis for using a square wave. To the contrary, a POSITA understands that DeMaw teaches a sinusoidal signal. In particular, Table 6.1 in DeMaw specifically states that “ $LO = f_o$, signal frequency = f_s .” A POSITA understands this refers to a sinusoidal signal, because a sinusoidal signal has a “single frequency” component. A square wave, however, is not a single frequency but, rather, a composite of multiple harmonics/frequencies. Ex.-2021, ¶¶240-241.

¹³ I note that “DeMaw 3.A.1” refers to the Petition at III.A.1, not to any portion of DeMaw itself.

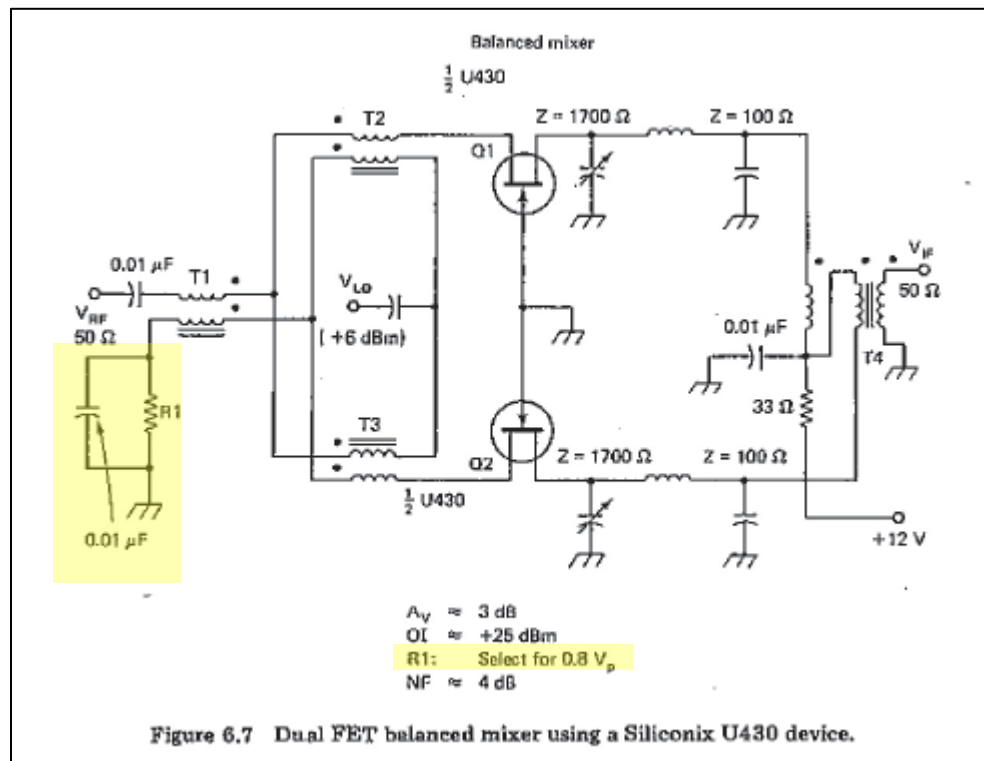
By substituting a square wave for a sinusoidal LO, Dr. Galton introduced high-frequency components that do not exist in DeMaw. These harmonics force artificial switching behavior and distort the mixer's operation. Ex.-2021, ¶242.

c. Biasing

Dr. Galton biased the JFETs in his simulation using a 2V DC supply in series with a 5Ω resistor (highlighted in yellow below). Ex.-2021, ¶243.



This bias configuration results in a gate-source voltage (V_{GS}) at or near the JFET's pinch-off voltage. DeMaw, however, teaches that V_{GS} is 0.8 the pinchoff voltage. Ex.-1016, 196. The yellow highlight below shows DeMaw's actual bias configuration including using 0.8Vp. Ex.-2021, ¶¶244-246.



Dr. Galton change to the bias configuration has a material effect because it biases the JFETs closer to cutoff, exaggerating ON/OFF transitions and further deviating from DeMaw's intended circuit operation. Ex.-2021, ¶247.

d. Operating Frequencies

Dr. Galton's simulation uses an RF signal at 123.102 MHz and an LO at 150 MHz. Ex.-1003, ¶¶ 74, 96. These values, however, are well outside the 3–30 MHz range specified by DeMaw's transformer design. Ex.-1016, 197. Ex.-2021, ¶¶248-250.

The frequencies Dr. Galton used exceed DeMaw's range *by a factor of five*—further distorting DeMaw's intended operation. A POSITA understands that

transformers are frequency-dependent components. Operating them outside their design range produces inaccurate behavior. Ex.-2021, ¶251.

Dr. Galton also uses an LO amplitude of 1.2V peak (2.4V peak-to-peak). But DeMaw teaches that the LO amplitude should be 80% of $V_{GS(off)}$. For a pinchoff voltage of 2V, this corresponds to 0.8V peak, not 1.2V. Dr. Galton's value is 50% too high. By using much higher frequency and amplitude values, Dr. Galton further distorts the behavior of the simulated circuit—creating switching behavior that is not representative of how DeMaw's mixer operates. Ex.-2021, ¶¶252-253.

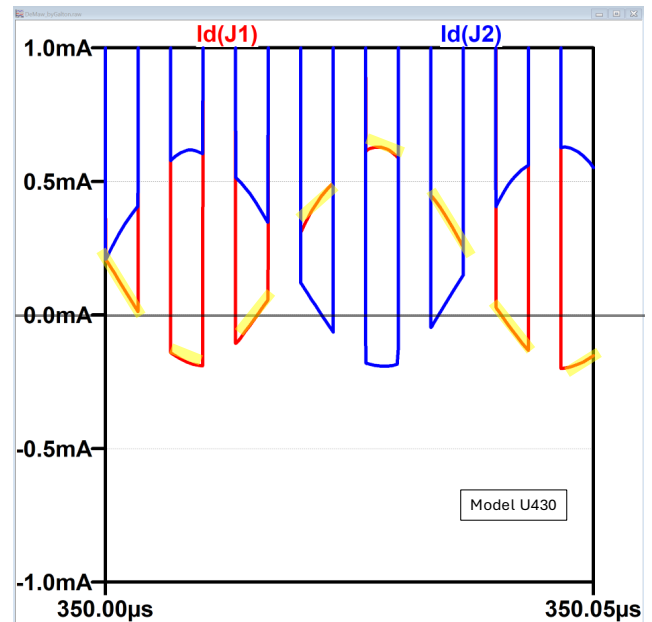
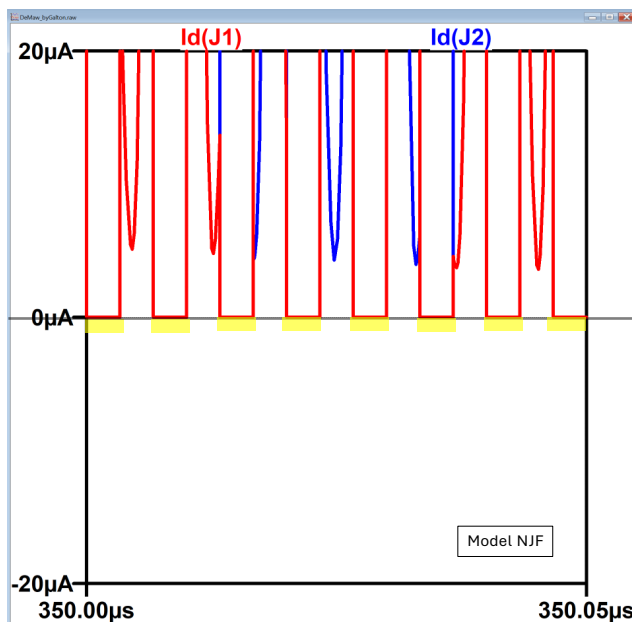
At bottom, Dr. Galton specifically chose values and waveforms that deviated from DeMaw in order to show a transistor being open (OFF) when capacitors discharge. But, Dr. Ricketts explains, this is not how DeMaw actually operates. *See* Sections VIII.A, IX.B. A POSITA recognizes that Dr. Galton's deviations are not minor modeling differences but, rather, materially affect the circuit's behavior—force the transistors into artificial ON/OFF transitions that do not actually occur. Ex.-2021, ¶¶254-255.

In view of the foregoing, Dr. Galton's conclusions are not grounded in the actual operation of DeMaw and should be given no weight.

2. Using the correct transistor model dramatically changes simulation results.

Dr. Ricketts setup the DeMaw circuit just like Dr. Galton except Dr. Ricketts used the correct JFET model disclosed in DeMaw (Siliconix U430). Dr. Ricketts did not change another of the other incorrect parameters (See Section IX.B.1.b-d). By doing so, Dr. Ricketts shows that using the correct JFET model alone had a significant impact on DeMaw's operation. Ex.-2021, ¶¶257-260.

Using the Siliconix U430 fundamentally altered the shape of the drain current waveform. As shown below, the red waveform represents the drain current of switch J1 and the blue waveform represents the drain current of switch J2. Ex.-2021, ¶261.



As shown above left, in Dr. Galton's NJF-based simulation (which Dr. Galton admitted used the wrong JFET model), the drain current periodically drops and

remains at zero (0 μA) (yellow highlights)—suggesting that the transistors are open (OFF) during those times. In contrast, as shown above right, when using the correct U430 model, the drain current never remains at zero.^{14,15} Instead, as shown by the yellow highlights, the current fluctuates continuously throughout the entire cycle, indicating that the transistors conduct current at all times (i.e., the transistors are always closed (ON) and never open (OFF)). This is consistent with the expected operation of a non-sampling mixer, as in DeMaw, where conduction is continuous and bidirectional. Ex.-2021, ¶¶262-264.

This distinction is critical. In his declaration, Dr. Galton explicitly states that “the switches are off when their drain currents are zero and on when their drain currents are non-zero.” Ex.-1003, ¶103. By his own definition, the presence or absence of drain current serves as a proxy for the state of the transistor—i.e., whether the JFET is ON or OFF. Ex.-2021, ¶¶265-267.

¹⁴ It should be noted that when zoomed in the scale of the plots change from microamps (μA) to milliamps (mA). 1 milliamp is 1000 microamps.

¹⁵ A POSITA understands that merely crossing zero (0 mA/0 μA) is not the same as to being at zero. Drain current is only zero when it remains flat along the 0 mA/0 μA axis over some interval—which is not observed in the U430 simulation.

The corrected U430-based simulation directly contradicts Dr. Galton's that the JFETs in DeMaw act as switches—turning ON and OFF. The correct simulation using the U430 model shows no OFF (open) state. Instead, the transistors operate to continuously conduct current, consistent with the non-sampling mixing behavior disclosed in DeMaw.

C. DeMaw-2

Section II of Dr. Galton's Second Declaration specifically addresses the use of the incorrect JFET model. Dr. Galton merely substitutes the correct Siliconix U430 models in place of the incorrect generic JFETs that he used, while keeping all other incorrect parameters the same. Ex.-2021, ¶¶268-270.

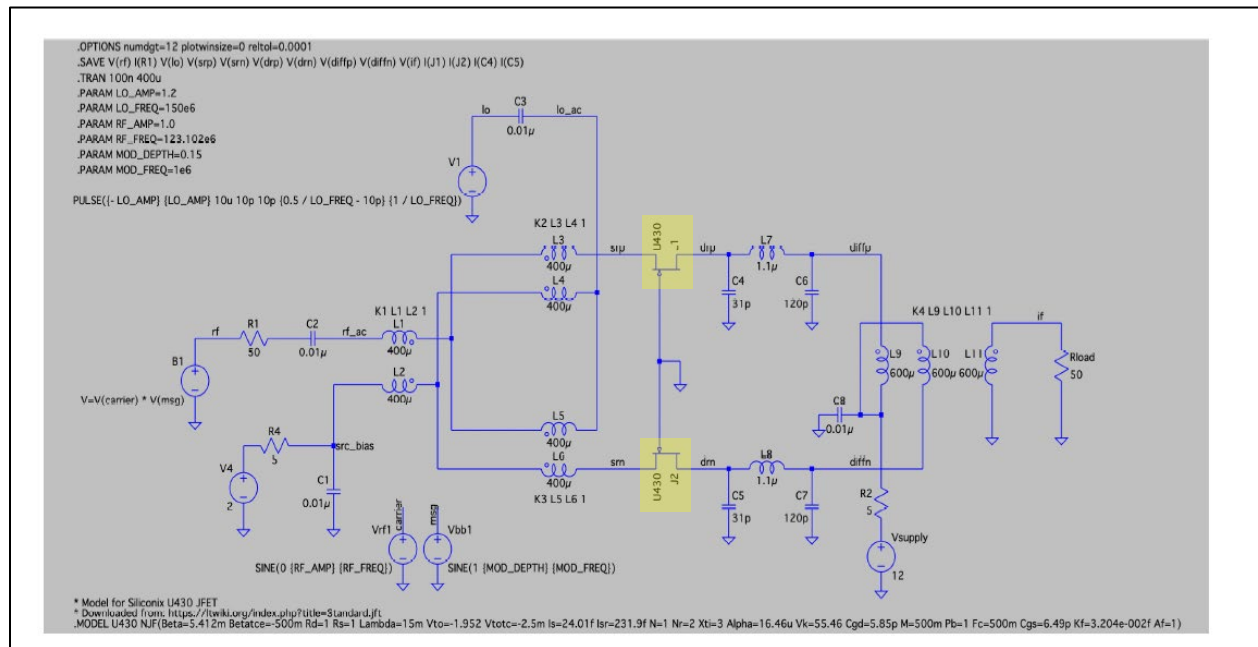
Sections III through VI of Dr. Galton's Second Declaration introduce additional modifications to his setup of DeMaw's circuit. Ex.-2021, ¶¶271.

1. DeMaw-2, Section II

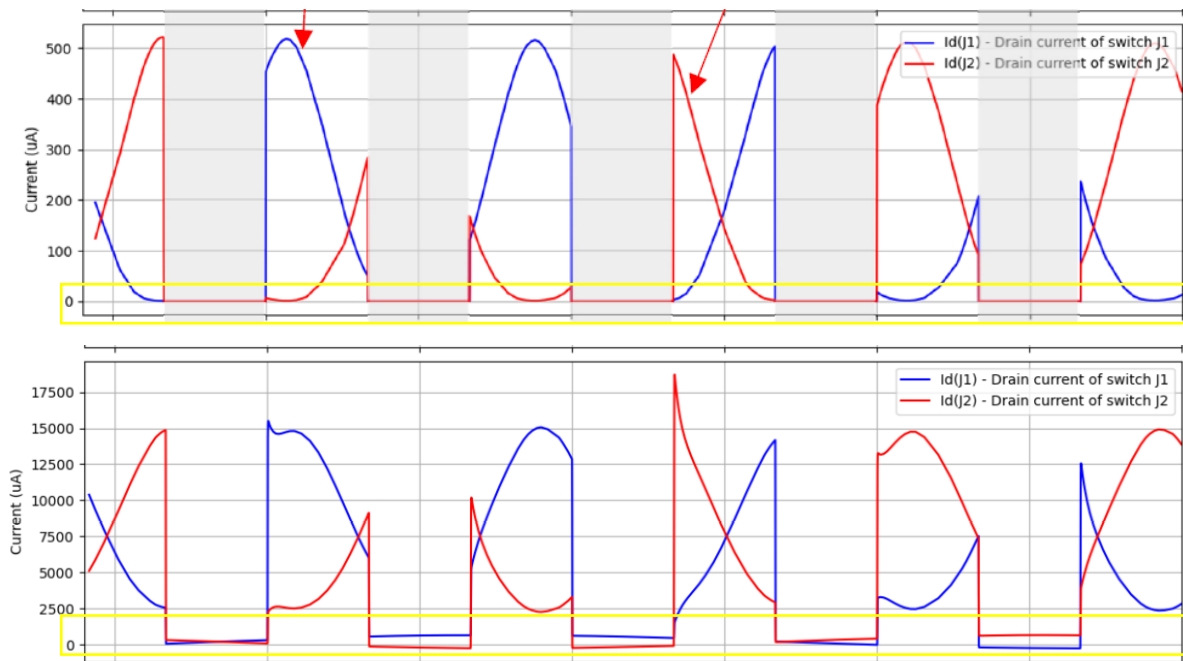
Section II addresses the transistor model error identified in Dr. Galton's original simulations—namely, his failure to use the Siliconix U430 JFET models as required by DeMaw. Ex.-2021, ¶272.

In Section II.A, Dr. Galton re-runs the exact same DeMaw simulation setup presented in his original Declaration except he uses the correct Siliconix U430 model in place of the generic “NJF” transistor. Ex.-2039, Ex.-1 ¶3. Ex.-2021, ¶273.

As shown below by yellow highlights, Dr. Galton's new simulation uses the U430 model. Ex.-2021, ¶274.



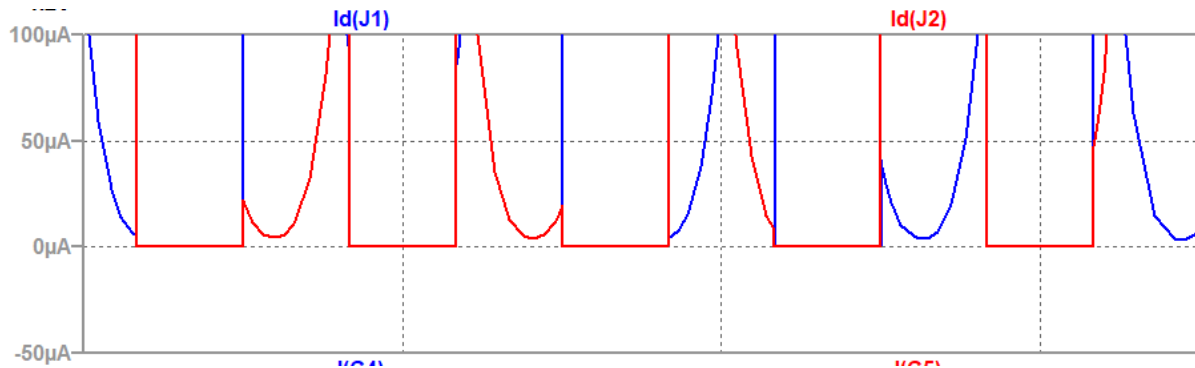
Consistent with the behavior Dr. Ricketts observed, Dr. Galton acknowledges that using the U430 model increases the mixer gain significantly. Ex.-2039, Ex.-1 ¶4. Ex.-2021, ¶¶275-276.



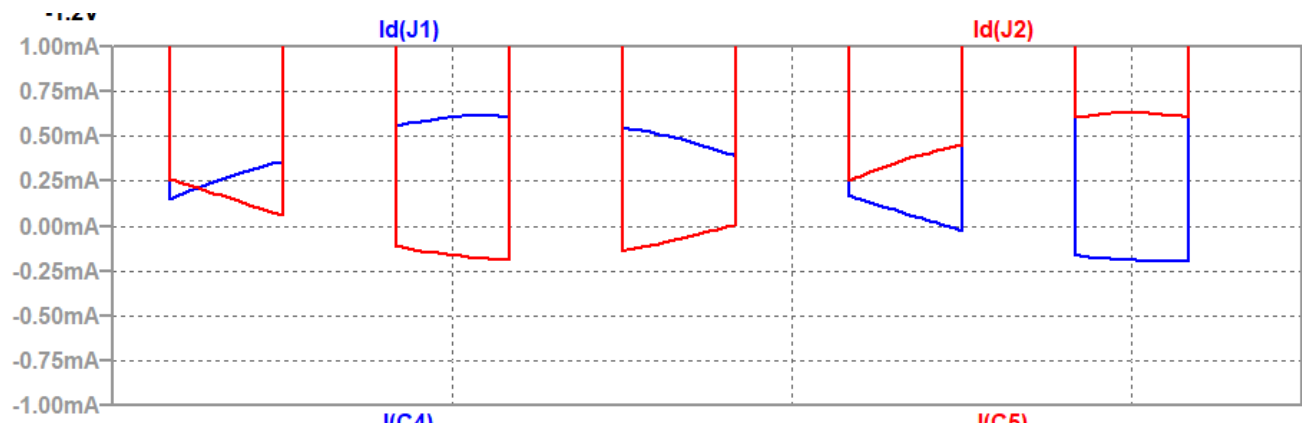
As shown above, Dr. Galton provides the drain current waveforms for his original simulation using the incorrect JFET model (top graph – DEMAW-SIM-FIG. 5) and his new simulation using the correct U430 model (bottom graph – DEMAW-SIM-FIG. 5 (revised)). Ex.-2021, ¶¶277-280.

A closer look at the simulation results — around the 0 μA axis (yellow boxes above)—reveals a material difference in the simulations, particularly with regard to how the transistors conduct current. Ex.-2021, ¶281.

To clearly show the difference, Dr. Ricketts re-ran both simulations (the incorrect JFET model and the correct U430 model) and zoomed in on the relevant regions of the drain current waveforms for transistors J1 and J2. Ex.-2021, ¶282.



As shown above, when zooming in on the drain current plot for the incorrect JFET model, one can see the current drops to and flattens at 0 μA during certain intervals—suggesting that the transistors are open (OFF) during those times. Ex.-2021, ¶¶283-284.



In contrast, when zooming in on drain current plot for the *correct* Siliconix U430 JFET model, one can see that the current *never* flattens/remains at 0 mA/0 μA . Instead, the current continues to fluctuate, thus, demonstrating continuous conduction through both transistors. Ex.-2021, ¶¶285-286.

In view of the foregoing, when the correct U430 model is used, the transistors do not open (turn OFF). Instead, the transistors remain in a state of continuous

bidirectional conduction (current flows continuously in one of two directions). This is consistent with the expected behavior of a non-sampling mixer such as disclosed in DeMaw. Ex.-2021, ¶¶287, 289.

The artificial ON/OFF behavior observed in Dr. Galton's original simulations was simply a byproduct of him using the incorrect transistor model. Id.

Dr. Galton asserts that "Everything I wrote in my original Declaration about DEMAW-SIM-FIG. 5 is true of this revised version." Ex.-2039, Ex.-1 ¶¶8, 12. As demonstrated above, he is wrong. The behavior shown in the correct simulations is materially different from his original simulation. Ex.-2021, ¶288.

Because Dr. Galton is presenting a new circuit simulation and a new/materially different theory (which is untimely and procedurally improper) in an attempt to rehabilitate/cure deficiencies in his original flawed analysis, Dr. Galton's Section II simulations should be disregarded. Indeed, the PTAB has repeatedly held that a Petitioner may not offer new theories, evidence, or simulations for the first time in reply. *See, e.g., Apple Inc. v. Maxell, Ltd.*, IPR2021-00225, Paper 34 at 37 (PTAB July 15, 2022) (excluding reply expert simulations as improper new evidence).

Further, because Dr. Galton's Section II simulations continue to use the wrong parameters, all of the deficiencies discussed in Section IX.B.1.b-d above still remain. Ex.-2021, ¶¶290-296.

Dr. Galton's deviation, individually and collectively, from the circuit actually disclosed in DeMaw renders Dr. Galton's simulations inaccurate/unreliable. Ex.-2021, ¶297. Thus, Dr. Galton's conclusions— particularly regarding ON/OFF switching behavior and percentage discharge—are unsupported and should be afforded no weight.

2. DeMaw-2, Section III

Section III attempts to address the criticism raised in the POPR. Ex.-2039, Ex.-1 ¶18. Section III introduces significant modifications to Dr. Galton's original simulation and Section II simulations. A POSITA would recognize that these changes are not mere adjustments but constitute a new and materially different simulation. Ex.-2021, ¶¶298-311.

A summary of all modifications introduced in Section III compared to Dr. Galton's simulation setup in his original declaration (Ex.-1003) is shown below. Ex.-2021, ¶312.

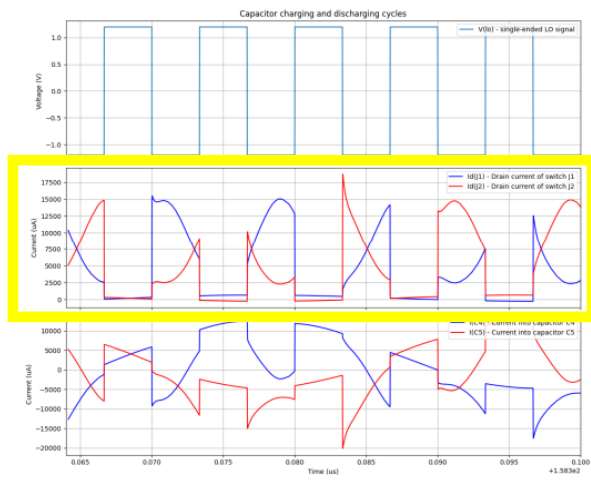
Parameter	Original Declaration	Second Declaration
JFET Model	default, generic LTspice JFET model	Siliconix U430 JFET
Bias Network	V4 = 2 V Resistor R4 = 5Ω	No V4 Resistor R4 = 1.6kΩ
LO input	No source impedance	Resistor R3 = 50Ω added
VDD supply resistor	Resistor R2 = 5Ω	Resistor R2 = 33Ω
Inductors L1, L2, L3, L4, L5 and L6	400 μH	4 μH

Inductors L9, L10, and L11	600 μ H	4 μ H
RF Frequency	123.102 MHz	150 MHz
LO Frequency ¹⁶	150 MHz	119.8 MHz
LO Amplitude	1.2V	0.785

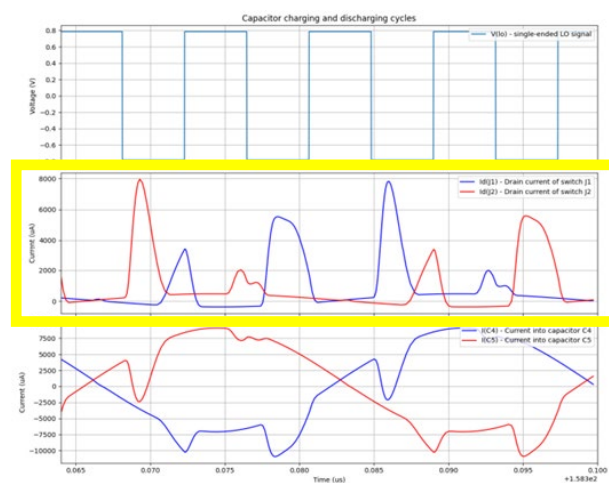
Dr. Galton alleges that each of the results provided in Section III.A-III.E¹⁷ “show the same simulation output” as his original simulations and therefore support the “original Declaration regarding the claims.” Ex.-2039, Ex.-1 ¶20. Not so. Ex.-2021, ¶¶301-311.

¹⁶ The Section III (as well as Section IV-VI) simulations still retain critical flaws. Specifically, The RF and LO frequencies (150 MHz and 119.8 MHz, respectively) remain well outside the 3–30 MHz range disclosed in DeMaw for its transformer-based mixer. A POSITA would understand that transformer characteristics degrade significantly outside this range—making the simulation results physically unrealistic and unreliable. Ex.-2021, ¶321.

¹⁷ Sections III.B–III.E repeat the same simulation of Section III.A with RF input power reduced by 6 dB, 12 dB, 18 dB, and 24 dB, respectively. The only change across those subsections is the RF amplitude. Ex.-2021, ¶313.



DEMAW-SIM-FIG. 5 (revised). Graphical representation of the charging and



DEMAW-SIM-FIG. 5.2. Capacitors C4 and C5 charging and discharging cycles

As shown in the yellow box (above left) and discussed in Section IX.C.1 above, the Section II simulation plots differ considerably/materially from Dr. Galton's original simulation using the incorrect JFET model. And, as shown in the yellow box (above right), the Section III simulation plots differs considerable from Dr. Galton's Section II simulation and original simulation. The Section III plots (which attempts to use the actual parameters disclosed in DeMaw) provides an even clearer picture demonstrating that the current *never* flattens/remains at 0 mA/0 μ A i.e., current continuously flow through both transistors and the transistors do not open (turn OFF). Ex.-2021, ¶¶315-318, Appendix B (showing zoomed-in waveforms of the Section III simulations).

Dr. Galton asserts that "DEMAW-SIM-FIGS. 4.2, 5.2, 6.2, 7.2A and 7.2B show the same simulation output as DEMAW-SIM-FIGS. 4, 5, 6, and 7... and therefore support my original Declaration regarding the claims." Ex.-2039, Ex.1

¶20; *see also id.* at ¶26. As shown above, Dr. Galton is incorrect. The switching behavior, impedance response, and waveform profiles are materially different. Dr. Galton's new simulations do not support, and in fact undermine, the claims made in his original Declaration. Ex.-2021, ¶¶319-320.

Dr. Galton's Section III simulations illustrates the extent of his changes—and the fact that these simulations represent an entirely new configuration, not a correction of his original setup. A POSITA would not consider Dr. Galton's new circuit configuration in Section III to be the same circuit as in his original Declaration. The modified biasing, signal frequencies, impedances, and inductor values all reflect a circuit that materially differs from what Dr. Galton originally simulated.

Dr. Galton's Section III simulations are the first time that Dr. Galton attempts to simulate the actual circuit of DeMaw Figure 6.7. But, in doing so, Dr. Galton abandons his original simulations/theory and introduces an entirely new simulations/circuits representing an entirely new theory never presented with the Petition. Such a shift in positions is procedurally improper and legally impermissible in IPR proceedings.

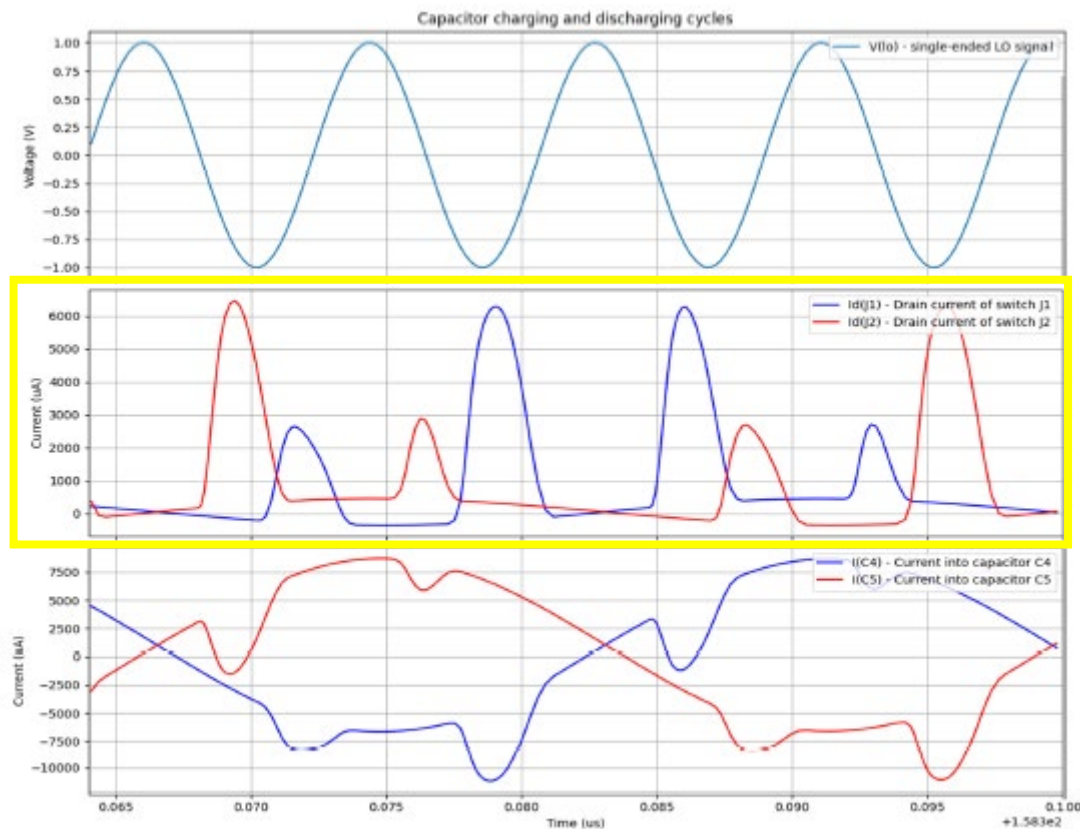
Because Dr. Galton is presenting a new circuit simulation and a new/materially different theory (which is untimely and procedurally improper) in an

attempt to rehabilitate/cure deficiencies in his original flawed analysis, Dr. Galton's Section III simulations should be disregarded.

3. DeMaw-2, Section IV

Section IV.A-IV.E makes all the same modification discussed in Section III and, in addition, uses a sinusoidal LO instead of a square wave.¹⁸ Ex.-2039, Ex.1 ¶65. Ex.-2021, ¶¶323-326.

¹⁸ Sections IV.B–IV.E repeat the same simulation of Section IV.A with RF input power reduced by 6 dB, 12 dB, 18 dB, and 24 dB, respectively. The only change across those subsections is the RF amplitude. Ex.-2021, ¶324.



DEMAW-SIM-FIG. 5.7. Capacitor charging and discharging cycles (circuit of

And, as shown in the yellow box, the Section IV simulation plot differs considerably from Dr. Galton's Section II simulation and original simulation. Similar to the Section III plot, the Section IV plots provide an even clearer picture demonstrating that the current *never* flattens/remains at 0 mA/0 μ A i.e., current continuously flow through both transistors and the transistors do not open (turn OFF). Ex.-2021, ¶¶327-329, Appendix B (showing zoomed-in waveforms of the Section IV simulations).

Dr. Galton asserts that "DEMAW-SIM-FIGS. 4.7, 5.7, 6.7, 7.7A and 7.7B show the same simulation output ... as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show

from DEMAW-SIM-FIG. 1. The conclusion in my original Declaration regarding the claims...are likewise supported.” Ex.-2039, Ex.1 ¶51; *see also id.* at ¶¶57, 63, 71, 77. As shown above, Dr. Galton is incorrect. The switching behavior, impedance response, and waveform profiles are materially different. Dr. Galton’s new simulations do not support, and in fact undermine, the claims made in his original Declaration. Ex.-2021, ¶¶330-332.

Because Dr. Galton is presenting a new circuit simulation and a new/materially different theory (which is untimely and procedurally improper) in an attempt to rehabilitate/cure deficiencies in his original flawed analysis, Dr. Galton’s Section IV simulations should be disregarded. Ex.-2021, ¶333.

4. DeMaw-2, Section V

Section V.A-V.E introduces a new circuit simulation that is based on a completely new references¹⁹ – Siliconix Application Note AN72-1 authored by E. Oxner. Ex.-2039, Ex.1 ¶83. Notably, in his original Declaration, Dr. Galton expressly stated: “DeMaw is a different circuit than Oxner.” Ex.-1003, ¶62. Despite

¹⁹ Sections V.B–V.E repeat the same simulation of Section V.A with RF input power reduced by 6 dB, 12 dB, 18 dB, and 24 dB, respectively. The only change across those subsections is the RF amplitude. Ex.-2021, ¶338.

this, Dr. Galton now presents new simulation results that are explicitly based on Oxner's component values and configuration. Ex.-2021, ¶¶334-335.

The new theory is procedurally improper. Dr. Galton was clearly aware of the Oxner reference at the time of his original Declaration (as evidenced by his direct discussion of it) yet chose not to rely on it when setup up his DeMaw simulations. He cannot now introduce a circuit derived from Oxner post hoc in an attempt to bolster his earlier, deficient analysis.

A POSITA would understand that the Oxner's and DeMaw's circuits have materially different configurations and operating conditions—and therefore cannot be used interchangeably.

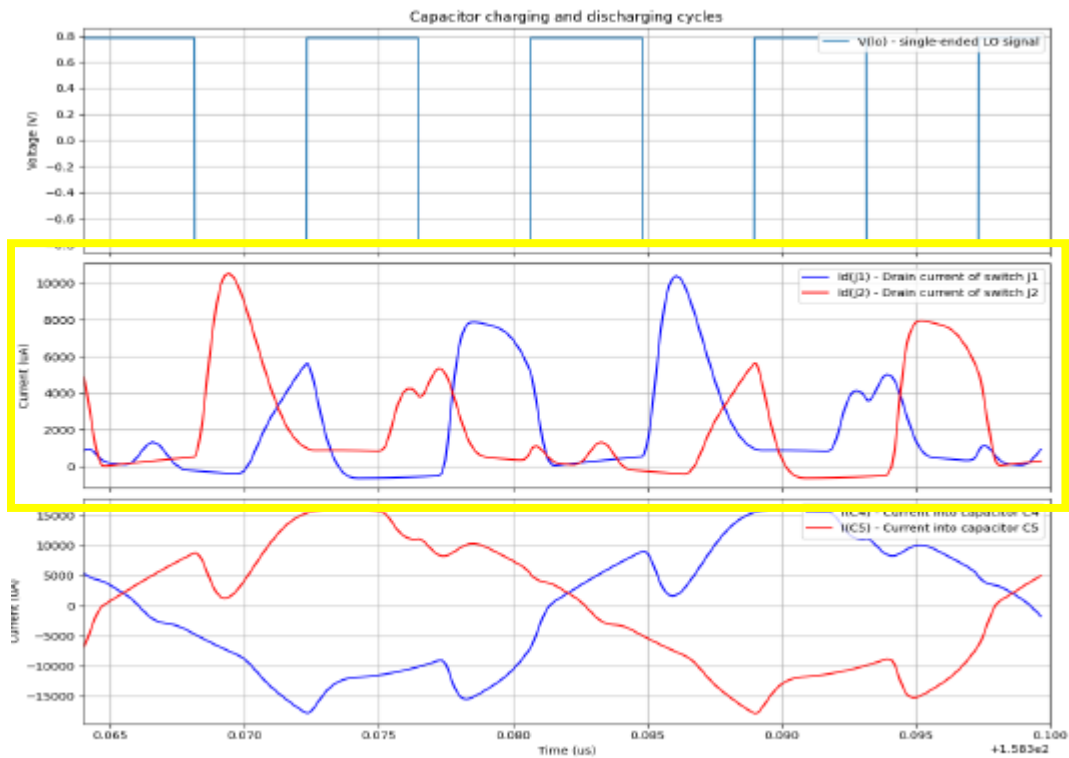
A summary of all modifications introduced in Section V (many of which are the same changes made in Section III and IV) compared to Dr. Galton's simulation setup in his original declaration (Ex.-1003) is shown below. Ex.-2021, ¶¶336-337.

Parameter	Original Declaration	Second Declaration
JFET Model	default, generic LTspice JFET model	Siliconix U430 JFET
LO input	No source impedance	Resistor R3 = 50Ω added
VDD supply resistor	Resistor R2 = 5Ω	Resistor R2 = 1Ω
Inductors L1, L2, L3, L4, L5 and L6	400 μH	4 μH
Inductors L9, L10	600 μH	4 μH
RF Frequency	123.102 MHz	150 MHz
LO Frequency	150 MHz	119.8 MHz

LO Amplitude	1.2 V	0.785
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In addition, Section V introduces other modifications not presented in Sections III or IV.

Parameter	Original Declaration	Second Declaration
Bias Network	Resistor R4 = 5Ω	Resistor R4 = 1Ω
VDD supply resistor	Resistor R2 = 5Ω	Resistor R2 = 1Ω
Inductors L11	$600\ \mu\text{H}$	$1\ \mu\text{H}$
Capacitors C4, C5	31p	30p
Capacitors C6, C7	120p	68p



DEMAW-SIM-FIG. 5.12. Capacitor charging and discharging cycles (circuit of

And, as shown in the yellow box, the Section V simulation plots differ considerable from Dr. Galton's Section II simulation and original simulation. Similar to the Section III and IV plot, the Section V plots provide an even clearer picture demonstrating that the current *never* flattens/remains at 0 mA/0 μ A i.e., current continuously flow through both transistors and the transistors do not open (turn OFF). Ex.-2021, ¶¶340-342, Appendix B (showing zoomed-in waveforms of the Section V simulations).

Dr. Galton asserts that "DEMAWSIM-FIGS. 4.12, 5.12, 6.12, 7.12A and 7.12B show the same simulation output from DEMAW-SIM-FIG. 1.12 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusion in my original Declaration regarding the claims...are likewise supported." Ex.-2039, Ex.-1 ¶84; *see also id.* at ¶¶90, 96, 102, 108. As shown above, Dr. Galton is incorrect. The switching behavior, impedance response, and waveform profiles are materially different. Dr. Galton's new simulations do not support, and in fact undermine, the claims made in his original Declaration. Ex.-2021, ¶¶343-345.

Section V represents yet another attempt to introduce a new simulation theory—in this case, based on an entirely different reference (Oxner) than the one actually at issue (DeMaw). Indeed, Dr. Galton's sudden reliance on Oxner is particularly problematic, because he expressly distinguished Oxner from DeMaw in his opening Declaration, and made no attempt to synthesize or rely on Oxner's

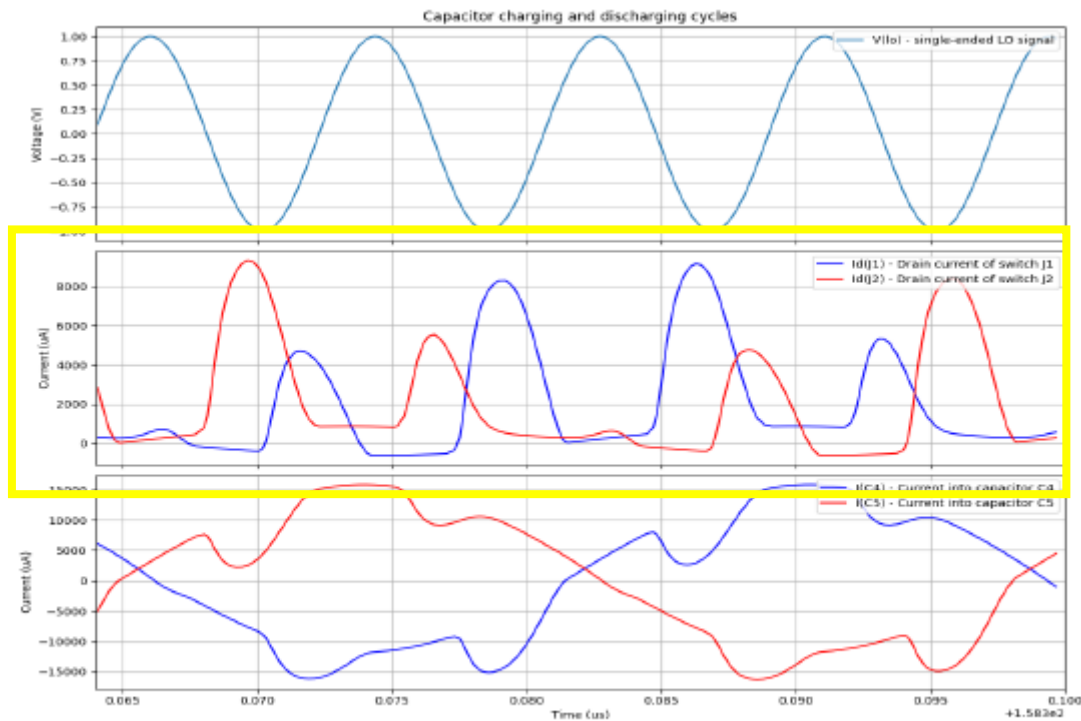
component values until this late stage. A POSITA would recognize that such material differences preclude treating Oxner-based simulations as substitutes for those based on DeMaw.

Because Dr. Galton is presenting a new circuit simulation and a new/materially different theory (which is untimely and procedurally improper) in an attempt to rehabilitate/cure deficiencies in his original flawed analysis, Dr. Galton's Section V simulations should be disregarded.

5. DeMaw-2, Section VI

Section VI.A-E makes all the same modification discussed in Section V using Oxner and, in addition, uses a sinusoidal LO instead of a square wave.²⁰ Ex.-2039, Ex.-1 ¶114. Ex.-2021, ¶¶346-347.

²⁰ Sections VI.B–VI.E repeat the same simulation of Section VI.A with RF input power reduced by 6 dB, 12 dB, 18 dB, and 24 dB, respectively. The only change across those subsections is the RF amplitude. Ex.-2021, ¶348.



DEMAW-SIM-FIG. 5.17. Capacitor charging and discharging cycles (circuit of

And, as shown in the yellow box, the Section VI simulation plots differ considerable from Dr. Galton's Section II simulation and original simulation. Similar to the Sections III, IV, and V plots, the Section VI plots provide an even clearer picture demonstrating that the current *never* flattens/remains at 0 mA/0 μ A i.e., current continuously flow through both transistors and the transistors do not open (turn OFF). Ex.-2021, ¶¶350-352, Appendix B (showing zoomed-in waveforms of the Section VI simulations).

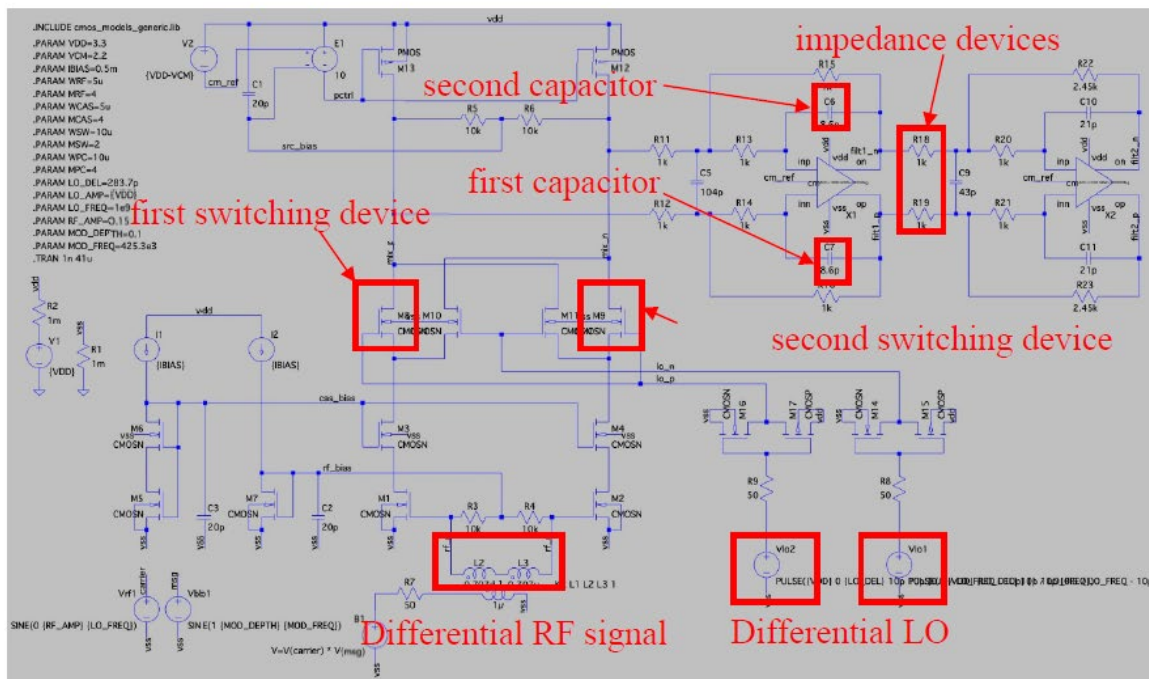
Dr. Galton asserts that "DEMAW-SIM-FIGS. 4.17, 5.17, 6.17, 7.17A and 7.17B show the same simulation output from DEMAW-SIM-FIG. 1.17 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my

original Declaration regarding the claims...are likewise supported.” Ex.-2039, Ex.1 ¶115; *see also id.* at ¶¶121, 127, 133, 139. As shown above, Dr. Galton is incorrect. The switching behavior, impedance response, and waveform profiles are materially different. Dr. Galton's new simulations do not support, and in fact undermine, the claims made in his original Declaration. Ex.-2021, ¶¶353-355.

Because Dr. Galton is presenting a new circuit simulation and a new/materially different theory (which is untimely and procedurally improper) in an attempt to rehabilitate/cure deficiencies in his original flawed analysis, Dr. Galton's Section VI simulations should be disregarded.

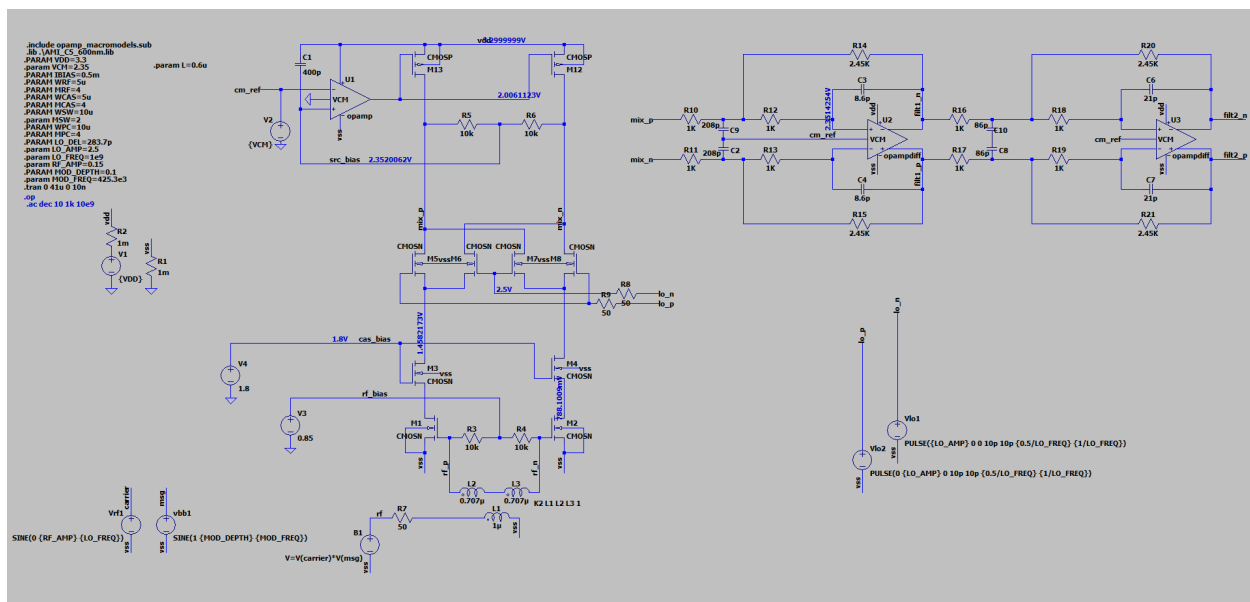
D. Macnally-1

Dr. Galton simulated Macnally's circuit using LTSpice with the setup shown in MACNALLY-SIM-FIG. 1 (below). Ex.-1003, ¶93. Ex.-2021, ¶¶356-357.



MACNALLY-SIM-FIG. 1 (annotated)

Because Dr. Galton did not provide the necessary back-up materials with his Declaration, Dr. Ricketts had to replicate this circuit (shown below). Ex.-2021, ¶358.



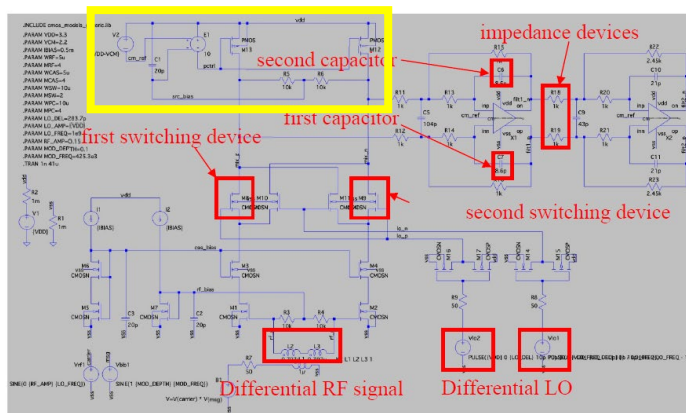
Dr. Ricketts identified several deviations between Dr. Galton's simulation and

the actual teachings of Macnally. Indeed, Dr. Galton concedes that “[t]he circuit was built using the limited descriptive text available in the patent.” Ex.-1003, ¶92. Ex.-2021, ¶¶359-364.

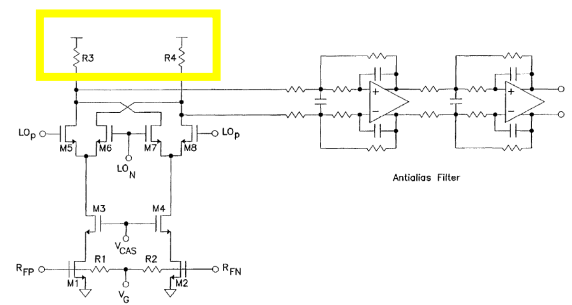
For example, while Macnally does not specify an LO drive circuit, Dr. Galton's simulation uses a “full-swing LO clock signal” (Ex.-1003, ¶149) that is neither taught nor suggested by the patent. Ex.-2021, ¶365.

Further, while Macnally describes BFSK modulation, Dr. Galton instead simulates down-conversion of a “1.0 GHz sinusoidal carrier amplitude-modulated (AM) 10% by a 425.3 kHz sinusoidal message signal.” Ex.-1003 ¶94. Dr. Galton admits that his simulation “deviates from the original patent's intended modulation of BFSK.” Ex.-1003, ¶94. Ex.-2021, ¶366.

Dr. Galton also inserted a biasing network using transistors M12 and M13—circuit elements that do not appear anywhere in Macnally. Ex.-2021, ¶367.



MACNALLY-SIM-FIG. 1 (annotated)



As shown above, the left image highlights the biasing network using transistor

M12, M13 (shown in the yellow box) in MACNALLY-SIM-FIG.1 of Dr. Galton's original Declaration. In contrast, the corresponding region of Macnally's Figure 3 (right) simply shows resistors R3 and R4. Ex.-2021, ¶368.

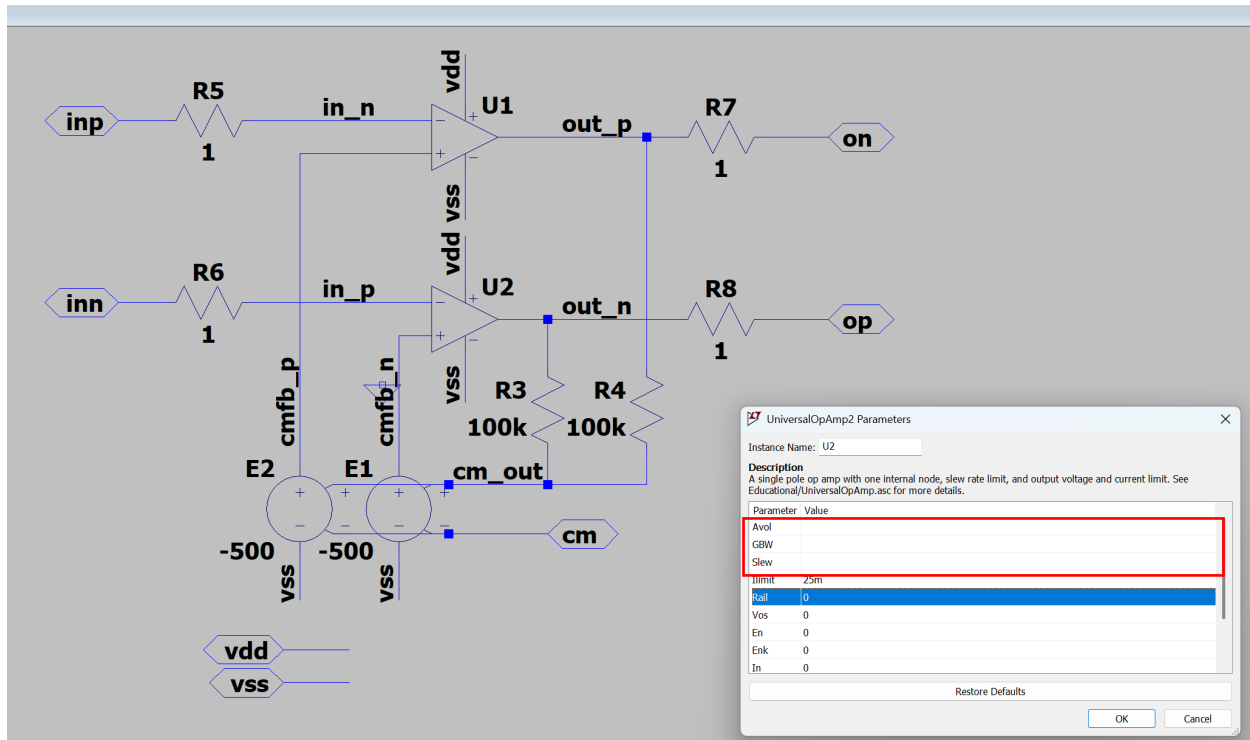
In Section VII of Dr. Galton's Second Declaration (Ex.-2039, Ex. 1) (discussed below), Dr. Galton provides the LTspice simulation files. Upon reviewing the native files, Dr. Ricketts identified several deficiencies with Dr. Galton's original simulation setup (Ex.-2021, ¶¶369-376):

Load Devices: In his original simulation, the active load transistors M12 and M13 were modeled using LTspice default devices, which have no defined electrical parameters (e.g., V_{th} , K_n , λ). These transistors are not part of the Macnally disclosure and were later removed and replaced with resistors in Dr. Galton's revised simulation.

Transistor Gate Length: Though Dr. Galton states that his Macnally simulations used a 0.6 μm CMOS process (Ex.-1003, ¶92), transistors M8–M11 in his simulated circuit (corresponding to transistors M5-M8 in Macnally Figure 3) were modeled with a gate length of 300nm—half the stated value. All other transistors used the 600nm gate length. A POSITA would understand that such inconsistency materially affects parasitic capacitance, gain, and switching behavior.

Operational Amplifier Model: In his original Declaration, Dr. Galton states that an operational amplifier “macromodel was used that emulates an op-amp with

60 dB of DC gain.” Ex.-1003, ¶92. However, Dr. Ricketts found that the operational amplifier component (universalopamp2) lacks any specified parameter values. As shown in the red box below, no values were provided for performance characteristics such as open-loop gain (A_{vol}), gain-bandwidth product (GBW), or slew rate.



Without these values, one cannot verify whether the op-amp model used by Dr. Galton actually achieves the 60 dB of gain he claimed. A POSITA would recognize that omitting such parameters renders the op-amp behavior undefined and the simulation results unreliable.

Missing Parasitic Capacitances: The original simulation omits device parasitic capacitances entirely. A POSITA would not consider a simulation omitting these parasitics to be reliable for evaluating high-frequency analog performance.

Dr. Galton's omissions and inconsistencies materially affect the simulated behavior of the Macnally circuit. A POSITA would not regard Dr. Galton's original simulation as a faithful representation of Macnally's actual teachings. Instead, it reflects an incomplete and speculative construction—one that is insufficient to support the conclusions presented in Dr. Galton's original Declaration.

E. Macnally-2

In his Second Declaration, Dr. Galton submits new simulations. Section VII purportedly address criticism raised in the POPR. Ex.-2039, Ex.-1 ¶145. Ex.-2021, ¶377.

Notably, Dr. Galton's second Declaration was his first attempts to simulate a circuit that actually "matches" the Macnally schematic in Figure 3. *Id.* Rather than defending the validity of his original modeling choices, Dr. Galton now concedes—implicitly—that his initial configuration was flawed.

Dr. Galton's new simulations more than a minor revision. A POSITA would recognize that these changes are not mere adjustments but constitute a new and materially different simulation from what was presented in Dr. Galton's original Declaration. Ex.-2021, ¶379.

Dr. Galton identifies several changes that he made to the setup used in his original Declaration (Ex.-2021, ¶¶380-387):

Use of Actual Resistors: Dr. Galton states that he replaced the current

source/resistor combinations used in his original simulation with actual resistors to implement R3 and R4 from Macnally Figure 3. Ex.-2039, Ex.1 ¶145. While Dr. Galton characterizes this as “common practice,” he could have implemented actual resistors in the original simulation. Moreover, Macnally does not disclose values for resistors R3 and R4, and Dr. Galton provides no citation or justification for the values he now selects.

Mixer Gain Adjustment: Dr. Galton modified the sizes and bias voltages of transistors M1/M2 allegedly “to achieve the 8.5 mS of transconductance mentioned in Macnally,” and adjusted the LO signal crossover points allegedly “to prevent the mixer core transistors... from cross-conducting.” *Id.* These modifications are unsupported. Macnally does not disclose any 8.5 mS transconductance value—or any transconductance value at all. In addition, the term “cross-conducting” never appears in Macnally. A POSITA would understand Dr. Galton’s assertions as speculative design choices, not faithful implementations of Macnally’s circuit.

BFSK Signal Change: Dr. Galton modified the RF input signal to incorporate BFSK modulation centered at 915 MHz. The modulation format disclosed in Macnally was known at the time of Dr. Galton’s original Declaration. Dr. Galton could have used BFSK in his original simulations but chose not to.

In addition, Dr. Galton made several other material changes in his second Declaration that he fails to mention:

Transistor Dimensions Updated: In the revised simulation, transistors M8–M11 (corresponding to transistors M5–M8 in Figure 3 of Macnally) use a gate length of 600 nm. However, his original simulation used 300 nm gate lengths for these same devices. This inconsistency materially impacts switching behavior, parasitics, and gain.

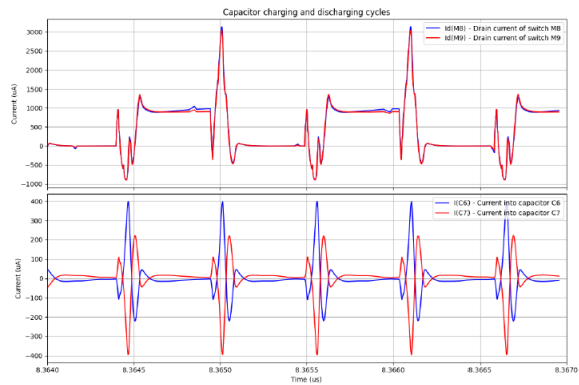
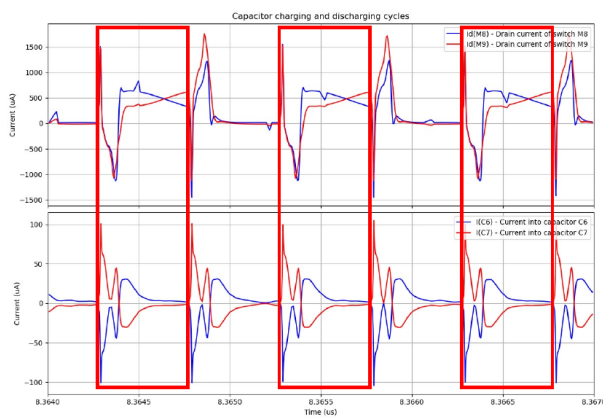
Op-Amp Topology Changed: The original simulation used differential macro-model operational amplifiers, which Dr. Galton claimed “accelerate simulation time but do not affect the presented results.” Ex.-1003, ¶92. In the revised simulation, however, these have been replaced with single-ended op-amps—a architectural change that is not acknowledged or justified. Ex.-2021, ¶386.

Transistor Redesign Throughout: All transistors in the circuit—except for those in the LO inverter—have been redesigned with new dimensions. Ex.-2021, ¶387. A POSITA would view this as a complete redesign. Notably, Dr. Galton only mentions modifications to transistors M1 and M2, but this redesign extends circuit-wide. Dr. Galton claims these changes were used to achieve a particular transconductance allegedly “described” in Macnally. However, no such transconductance value is disclosed in the Macnally.

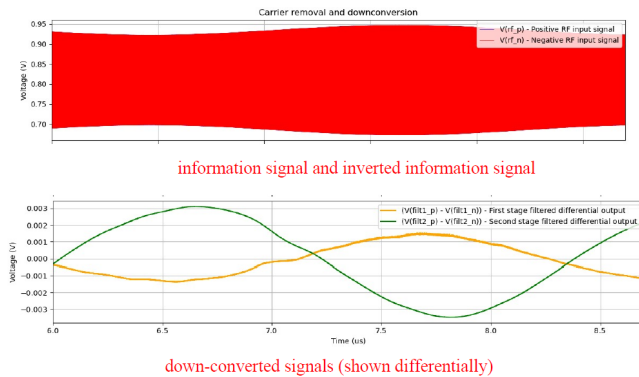
The modifications above reflect a fundamentally different simulation than the one presented in Dr. Galton's original Declaration. The revised circuit uses new component values, altered geometries, changed op-amp topologies, and a different

modulation format. These are not minor refinements—they are substantial departures that collectively represent a new theory of how Macnally allegedly operates. Ex.-2021, ¶¶388.

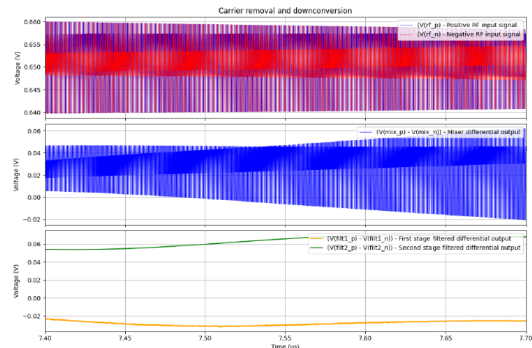
Notably, even the waveforms used in Section VII differ materially from Dr. Galton's original declaration.



MACNALLY-SIM-FIG. 2.1. Capacitor charging and discharging cycles (circuit of MACNALLY-SIM-FIG. 1.1).

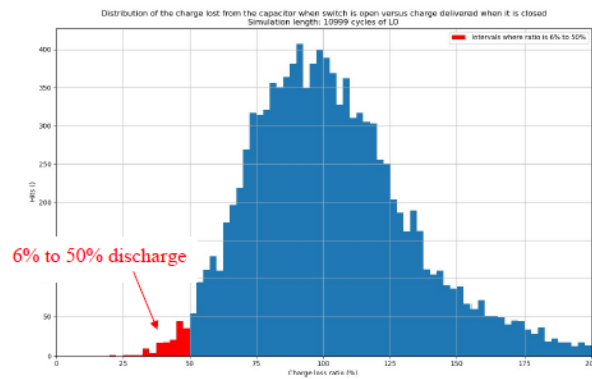


MACNALLY-SIM-FIG. 3 (annotated)

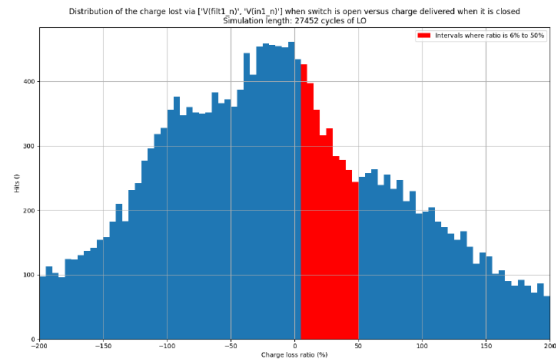


MACNALLY-SIM-FIG. 3.1. Carrier removal and downconversion (circuit of MACNALLY-SIM-FIG. 1.1).

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Patent Owner's Response



MACNALLY-SIM-FIG. 4 (annotated)



MACNALLY-SIM-FIG. 4.1A. Charge loss ratio percentages histogram for capacitor C6 (circuit of MACNALLY-SIM-FIG. 1.1).

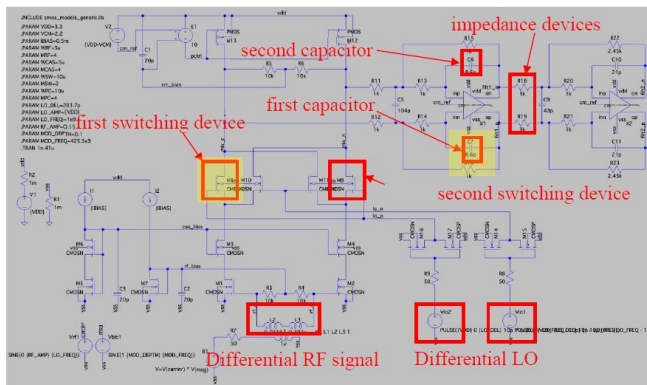
Above is a side-by-side comparison of the corresponding waveforms from Dr. Galton's original Declaration (left side above – DEMA W-SIM-FIGs. 2, 3, 4) to Dr. Galton's Second Declaration (right side above - MACNALLY-SIM-FIG. 2.1, 3.1, and 4.1). Ex.-2021, ¶389.

The waveforms differ noticeably in both shape and magnitude. As shown above, the histograms (Figure 4 and Fig. 4.1A) are also significantly different. Yet Dr. Galton concludes: “MACNALLY-SIM-FIGS. 2.1, 3.1, 4.1A and 4.1B show the same simulation output from MACNALLY-SIM-FIG. 1.1 as MACNALLY-SIM-FIGS. 2, 3, 4, 5 and 6 show from MACNALLY-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims... are likewise supported.” Ex.-2039, Ex.1 ¶146 (emphasis added). Ex.-2021, ¶390.

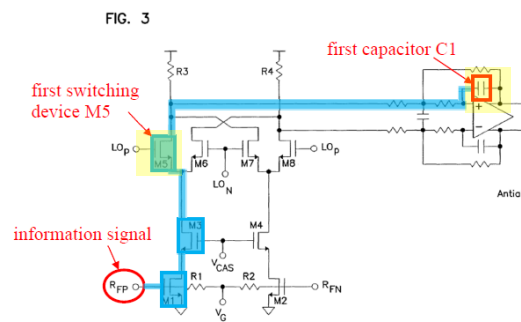
The changes to circuit topology, loading conditions, transistor dimensions, and signal behavior reflect a materially different simulation. Because Dr. Galton is presenting a new circuit simulation and a new/materially different theory (which is

untimely and procedurally improper) in an attempt to rehabilitate/cure deficiencies in his original flawed analysis, Dr. Galton's Section VII Macnally simulations should be disregarded. Ex.-2021, ¶¶391.

Nevertheless, Dr. Galton provides no waveforms for charge and discharge of capacitors—only Python-processed calculations. However, Dr. Ricketts ran Dr. Galton's Section VII simulations using the native files Dr. Galton provided. Ex.-2021, ¶¶392-393.



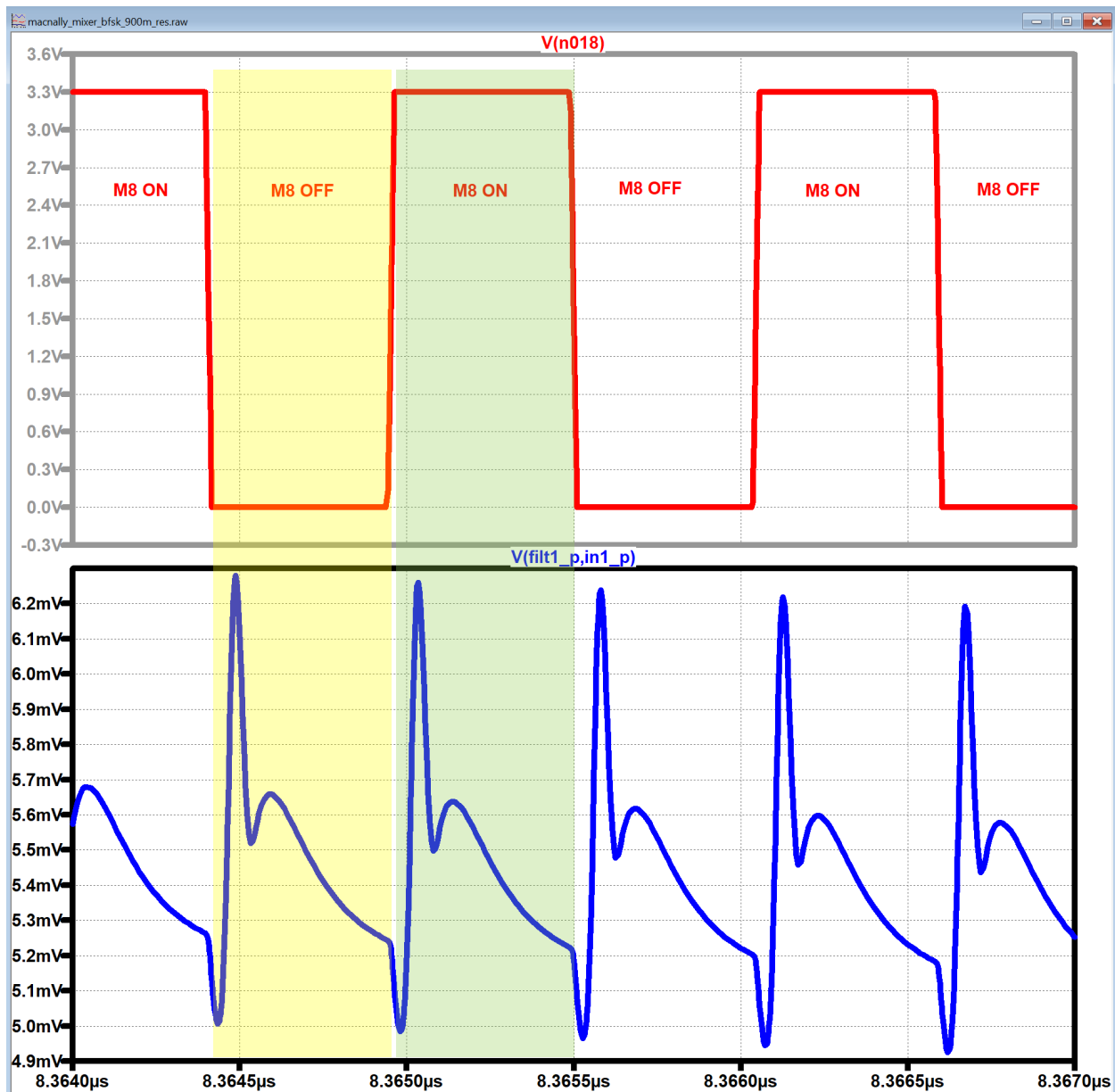
MACNALLY-SIM-FIG. 1 (annotated)



Macnally, FIG. 3 (partial, annotated)

As shown above, in Dr. Galton's simulations, transistor M8 and capacitor C7 (highlighted in yellow) correspond to what Dr. Galton identifies as transistor M5 and capacitor C1 in MacNally's Figure 3 (above right). Transistor M8 turns on when the LO_p signal is high. Ex.-2021, ¶¶394.

As shown in the plot below, which shows both the LO_p signal and capacitor voltage (V_c), the charge on the capacitor remains materially the same whether M8 is ON or OFF (id.):

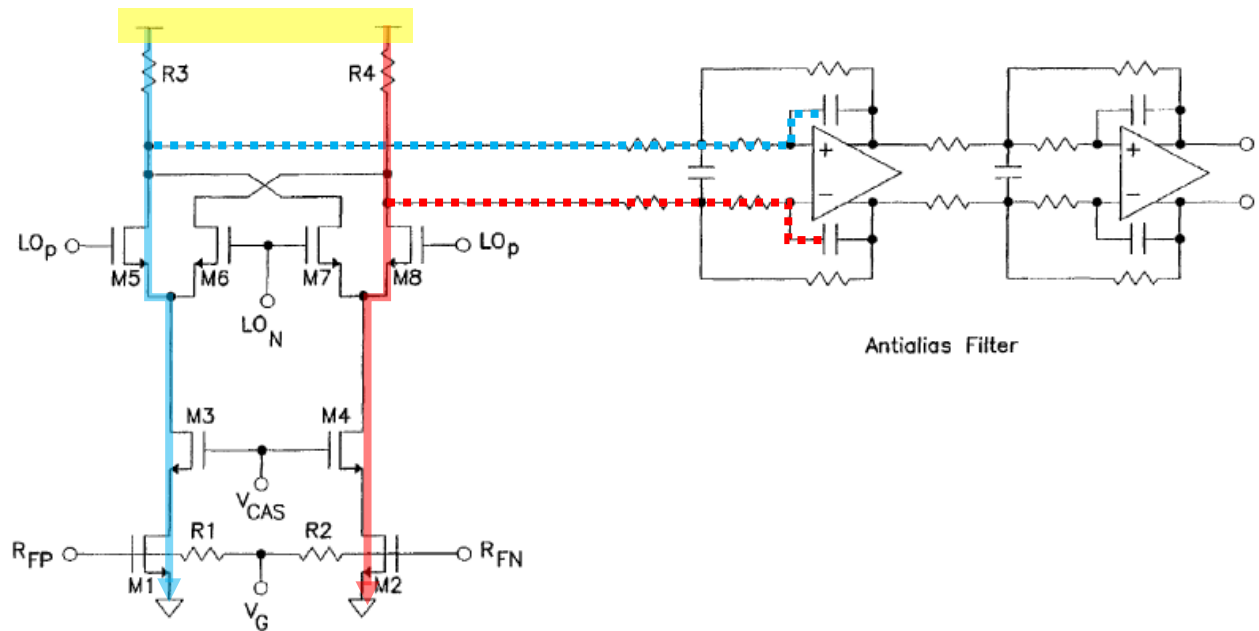


In particular, as shown above, when the transistor M8 is ON (green) or OFF (yellow), the total charge on the capacitor remains materially the same. This is because in Macnally's design, current continuously flows to capacitors C1 and C2—and through M1 and M2—regardless of LO state. Ex.-2021, ¶395.

A POSITA would understand that the LO_P and LO_N signals are differential

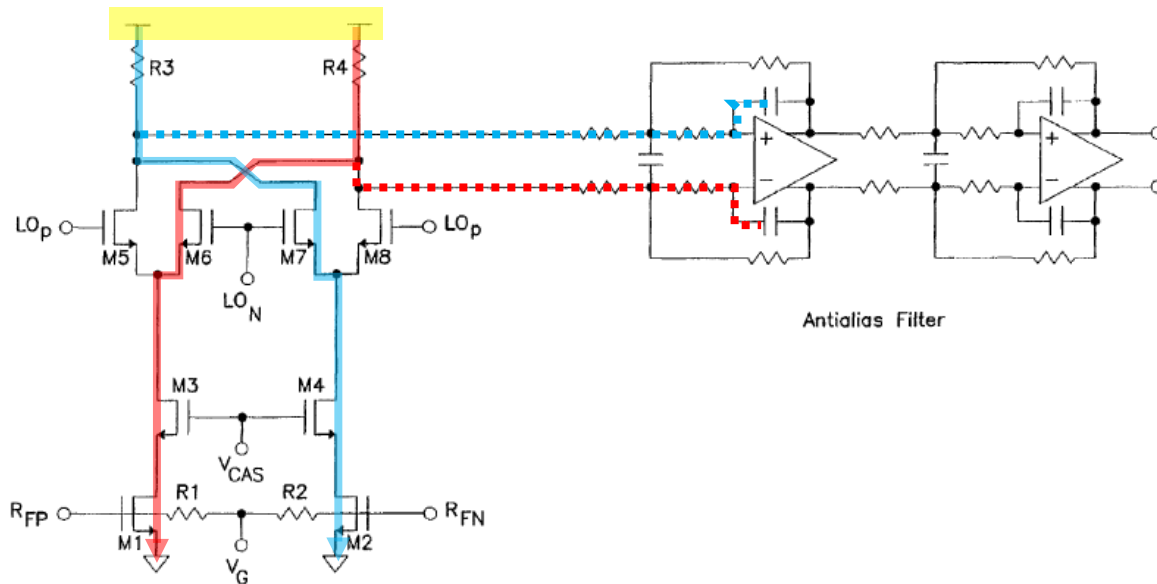
signals, meaning that when LO_P is high, LO_N is low, and vice versa. Ex.-2021, ¶396.

FIG. 3



When the LO_p signal is high, transistors M5 and M8 conduct. Current from the power supply (yellow box) flows through resistor R3, some of it is directed to capacitor C1 (shown by the dashed blue line), while the remainder flows through M5 and M1 (solid blue). Similarly, current from the power supply flows through resistor R4, with some of it directed to capacitor C2 (shown by the dashed red line), while the remainder flows through M8 and M2 (solid red). Ex.-2021, ¶397.

FIG. 3



Likewise, when the LO_p signal is low, LO_n is high, and transistors M6 and M7 conduct. Current from the power supply flows through resistor R3, some of it directed to capacitor C1 (shown by the dashed blue line), while the remainder flows through M7 and M2 (solid blue). Current from the power supply also flows through resistor R4, with some directed to capacitor C2 (shown by the dashed red line), while the remainder flows through M6 and M1 (solid red). Ex.-2021, ¶¶398.

X. VALIDITY OF THE '342 PATENT

A. GROUND 1A: DeMaw

1. DeMaw does not disclose, teach, or suggest the claimed discharge percentages.

Claims 19-21 require that (1) the first capacitor discharges specific percentages of “the total charge stored therein during a period of time that the first switching devices is open,” and (2) the second capacitor discharges specific percentages of “the total charge stored therein during a period of time that the second switching devices is open.” Claim 19 recites a discharge range of 6-50%, claim 20 recites a discharge range of 10–25%, and claim 21 recites 15–30%.

DeMaw does not discuss any percentage discharged from the capacitors. Thus, Petitioner relies entirely on simulations performed by Dr. Galton. Ex.-2021, ¶400.

The claims require calculating how much of the “total charge stored” in a capacitor is discharged during the time a switch is open. Dr. Galton, however, ignores the claim language and computes the wrong percentage. Instead of calculating the percentage the capacitor discharges of the “total” charge stored, Dr. Galton performs a cycle-by-cycle analysis—comparing the charge discharged during an alleged switch-open interval with the charge added during the immediately preceding switch-closed interval of the same cycle. Ex.-2021, ¶¶401-402.

Dr. Galton confirmed this methodology in deposition. Dr. Galton's Python

script defines discharge percentage as $q_{loss} = 100 * q_{out}/q_{in}$. Ex.-2039, Ex.-2, line 727. Dr. Galton admitted that “ q_{in} ” represents the charge delivered to the capacitor during one switch-on (closed) interval, and that “ q_{out} ” represents the charge discharged during one switch-off (open) interval. Ex.-2039, 34:9-12; *see also* id., 34:14-22, 37:4-13. Ex.-2021, ¶¶403-404.

As a POSITA would understand, the capacitors in DeMaw (C4 and C5 in Dr. Galton's simulation) do not fully discharge between LO cycles. Instead, they incrementally accumulate charge over many cycles. The residual baseline voltage—set by a 12V power supply—remains largely unchanged, and new charge is added on top of what was previously stored. Accordingly, the “total charge stored” at any given discharge event is the cumulative charge on the capacitor—not just what was added in the immediately prior cycle. Ex.-2021, ¶406.

Thus, to calculate the percentage of “total charge stored” that has been discharged, one must consider *all* of the charge that is on a capacitor when a discharge occurs – not just the most recent increment. Ex.-2021, ¶407.

The proper formula for calculating discharge under the claims is (Ex.-2021, ¶408):

$$\% \text{ discharge} = \frac{\text{Charge discharged during the period switch is open}}{\text{Total charge stored at the beginning of the discharge period}}$$

Because charges on a capacitor are proportional to the voltage across it, i.e.,

$Q=CV$, and capacitance (C) is constant, we can directly use voltages to calculate the discharge ratio: $\frac{Q_2-Q_1}{Q_1} = \frac{CV_2-CV_1}{CV_1} = \frac{V_2-V_1}{V_1}$. A negative result indicates a discharge; a positive value indicates a charge. Because LO controls the switching, one computes this ratio for every LO pulse across an IF cycle and report the maximum observed discharge. Ex.-2021, ¶¶409-411.

Rather than using the correct formula above, Dr. Galton uses a different, incorrect formula: (Ex.-2021, ¶412).

$$\% \text{ discharge} = \frac{\text{Charge discharged during the period switch is open}}{\text{Charge stored in the same cycle}}$$

In doing so, Dr. Galton ignores the accumulated charge already present on the capacitor before the current cycle began and thus significantly overstates the calculated percentage. Ex.-2021, ¶413.

Dr. Galton fails to account for the baseline 12V charge on the capacitors—even though he acknowledges that a 12V supply charges them. Ex.-2036, 19:4–15. By failing to account for this charge, Dr. Galton understates the denominator and thereby overstates the calculated discharge percentage. This is a fundamental analytical error. Ex.-2021, ¶¶414-415.

Using Dr. Galton's revised simulations (DEMAW-SIM-FIG. 1 (revised)), Dr. Ricketts computed the percentage discharge across capacitors C4 and C5 during the

time their corresponding switches are allegedly open as defined by Dr. Galton—i.e., when LO is high. Ex.-2021, ¶416.

While there is no actual switch-open period in DeMaw, Dr. Ricketts analysis adopts Dr. Galton's own assumptions for illustrative purposes. Ex.-2021, ¶417.

Figure 1 (below) shows voltage across C4 and C5 over one full cycle of the modulated IF signal, which contains multiple LO pulses (Modulation frequency 1MHz, IF frequency 26.9MHz, LO frequency 150MHz). Ex.-2021, ¶418.

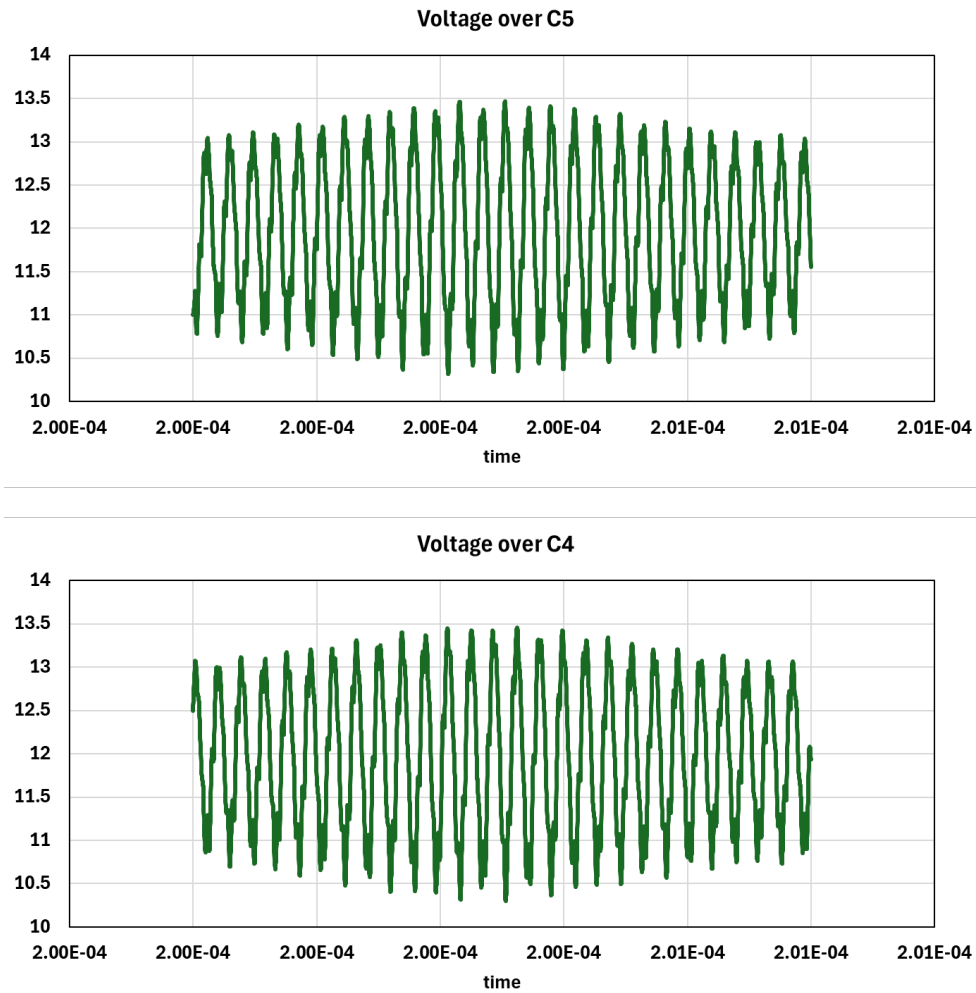
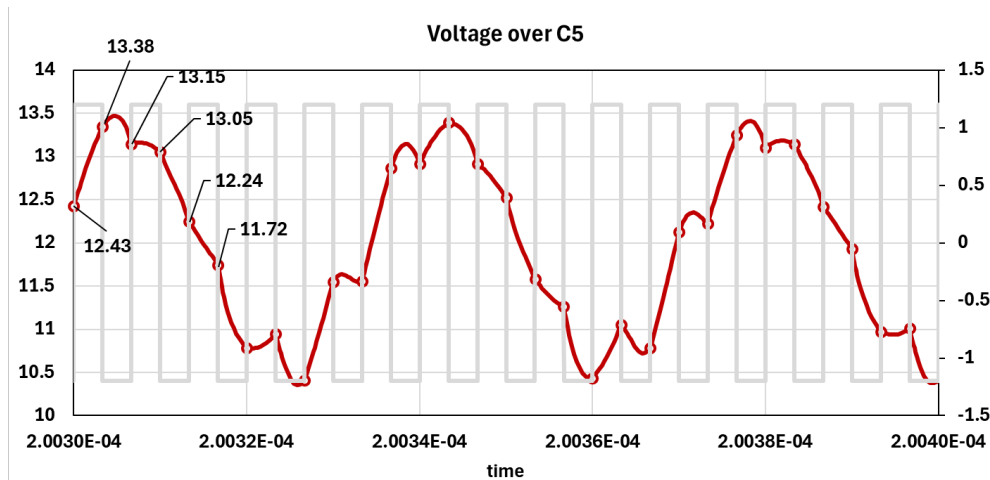


FIGURE 1

Figure 2 shows a zoomed in span of voltage across C5 together with the LO pulses. Ex.-2021, ¶419.

**FIGURE 2**

The switch is allegedly open when LO is “high” or positive. Dr. Ricketts uses the proper discharge equation (equation (1) above) to calculate the discharge ratio for all the times LO is high. Ex.-2021, ¶420.

As an example for the few points shown in Figure 2 above, Dr. Ricketts have the numbers shown below. Ex.-2021, ¶421.

V(t0)	V(t1)	%
12.427	13.348	7.42 (charging)
13.146	13.052	-0.71
12.248	11.748	-4.08

For each LO pulse, Dr. Ricketts measured the voltage at the rising and falling edges of LO. Using Equation (1), he computed the discharge ratio. Ex.-2021, ¶422.

A positive value (e.g., +7.42%) indicates the capacitor charged rather than discharged.

Because the transistors in DeMaw are never off, there is no period of time when the switch is open, nor a period of time when the transistors are not

contributing to the charge of the capacitors. As such, the claimed “period of time that the [] switching device is open” does not exist in DeMaw’s circuit. Nevertheless, Dr. Ricketts calculated the maximum percentage discharge across the capacitors for all of Dr. Galton’s revised simulations using the correct equation (1) and Dr. Galton’s assumption that LO-high corresponds to a switch-open interval, as shown in Appendix B. The maximum discharge is shown for each simulation using the correct discharge equation. Ex.-2021, ¶¶424-425, Appendix B.

Using the data from Dr. Galton’s own simulation results and plugging the data into the correct formula demonstrates that nearly all of the percentage discharged falls outside the ranges set forth in claims 19-21. Nevertheless, to the extent any percentages fall within the claimed ranges, these do not reflect when the switch is open, as required by the claim. Ex.-2021, ¶426.

2. DeMaw does not disclose, teach, or suggest the claimed discharged percentages during “a period of time that the [] switching device is open.”

Claims 19-21 of the ’342 patent require specific discharge percentages “during a period of time that the first switching device is open.”

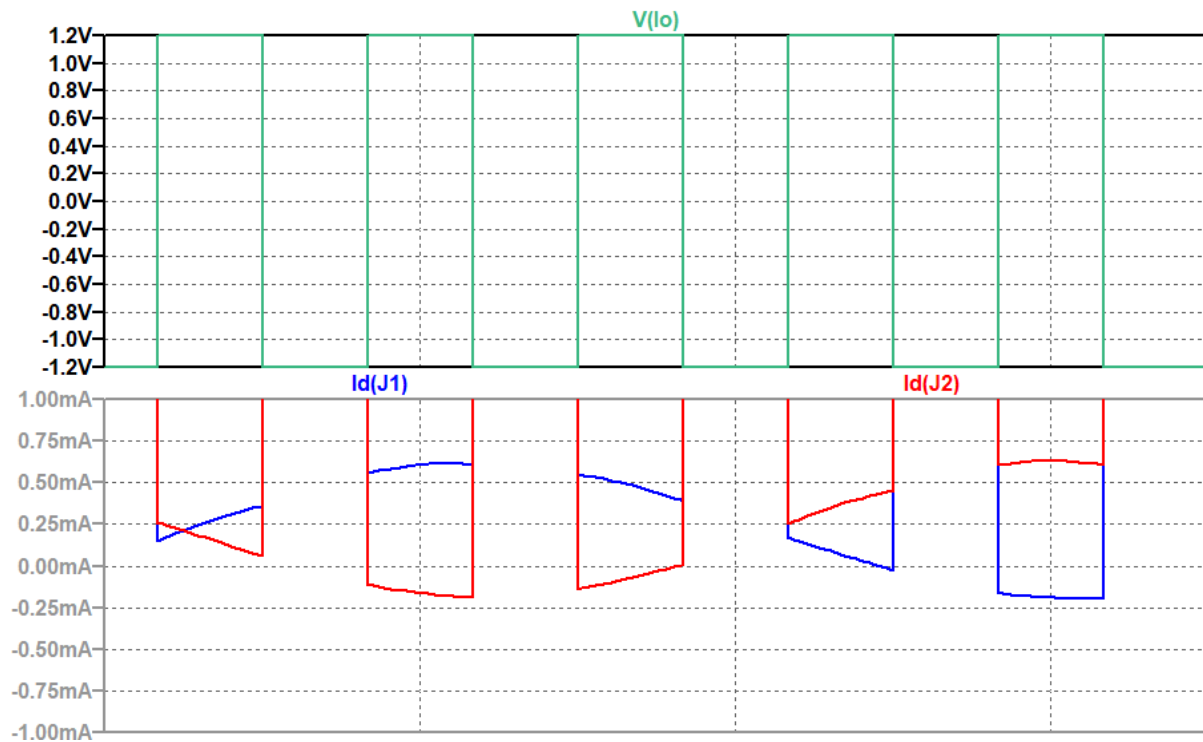
As discussed in Sections IX.B and IX.C above, DeMaw’s transistors are never open (OFF). The transistors are always closed (ON). Thus, DeMaw’s capacitors cannot discharge during a period of time when the switch is open. Ex.-2021, ¶428.

As Dr. Galton acknowledges, the “open” or “off” state of a switching device is not an arbitrary signal timing event—it must be tied to the actual state of the switch, i.e., whether the transistor is conducting current. Ex.-2021,¶429.

In fact, in his original Declaration, Dr. Galton expressly defined the alleged switching behavior as follows: “The switches are off when their drain currents are zero and on when their drain currents are non-zero.” Ex.-1003, ¶103. Ex.-2021,¶430.

A JFET in a switching configuration is considered “on” when it conducts drain current and “off” when drain current is zero (0). Thus, by Dr. Galton's own definition, the switch-open period begins when the drain current drops to zero and ends when current resumes. Ex.-2021,¶431.

Yet, when computing the discharge percentage, Dr. Galton abandons this definition. Instead of calculated the discharge percentage during the time when a switch is open (OFF) – when the switch is at 0 mA/0 μ A (when drain current is zero), Dr. Galton uses the duration of the LO signal being “high” as a proxy for when the switch is open. *See, e.g.*, Ex.-2039, Ex. 1, ¶90. But as shown below, this substitution is factually and technically incorrect. Ex.-2021,¶432.

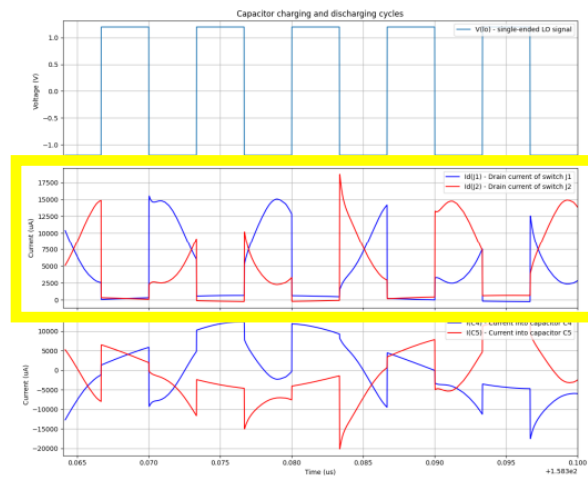


As shown above (using the correct JFET model) and discussed in Section IV.C.1, Dr. Ricketts plotted the drain current waveforms of J1 (blue) and J2 (red) alongside the LO waveform (green). Similar to Dr. Galton's plots (shown Section IV.C.1), Dr. Ricketts plots reveal that the drain current continues to flow—often in both directions—even while LO (green) is high at 1.2V. Ex.-2021, ¶¶433-435.

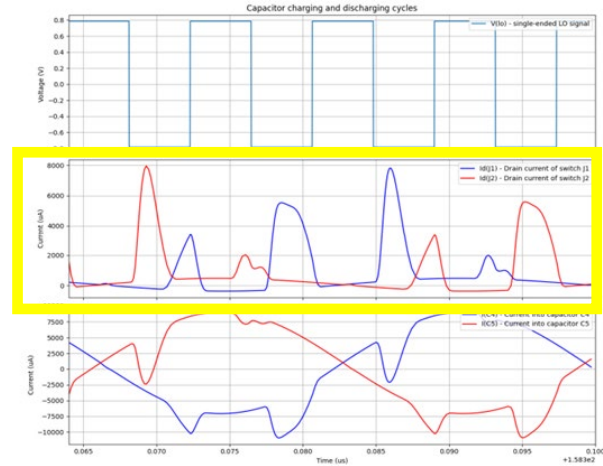
The current through J1 and J2 does not drop to zero at the LO high transitions. In fact, the current never flattens/remains 0 mA, even during LO “high” periods.

Thus, the switch is never open (OFF) as defined by Dr. Galton (i.e., zero drain current), and the assumption that LO being “high” corresponds to the switch being “open” is incorrect.

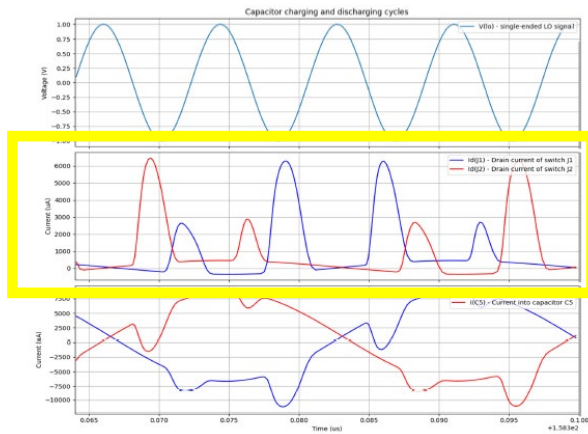
IPR2024-00934 (U.S. Patent No. 7,496,342)
Patent Owner's Response



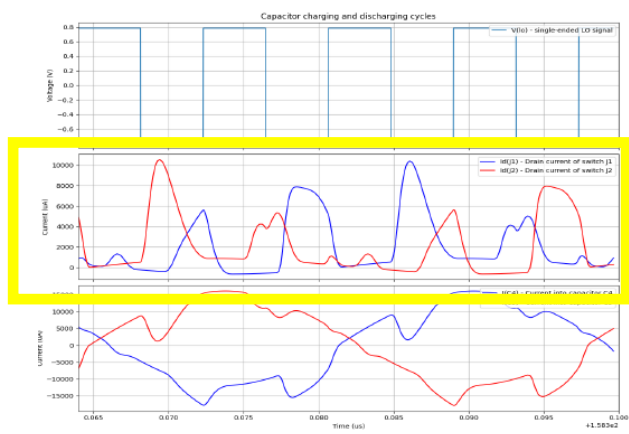
DEMAW-SIM-FIG. 5 (revised). Graphical representation of the charging and



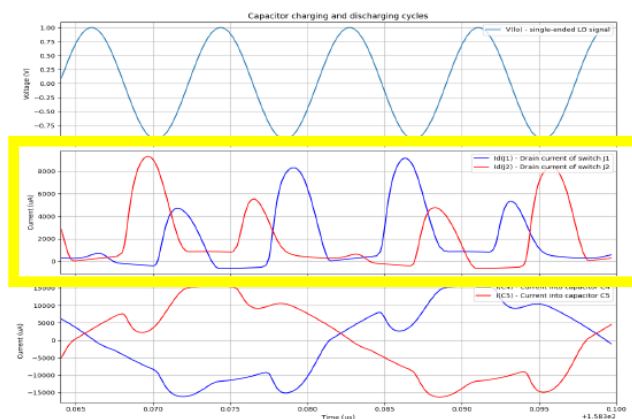
DEMAW-SIM-FIG. 5.2. Capacitors C4 and C5 charging and discharging cycles



DEMAW-SIM-FIG. 5.7. Capacitor charging and discharging cycles (circuit of



DEMAW-SIM-FIG. 5.12. Capacitor charging and discharging cycles (circuit of



DEMAW-SIM-FIG. 5.17. Capacitor charging and discharging cycles (circuit of

Indeed, as discussed in Section IX.C, all of Dr. Galton's new simulations show that the switch does not open. The plots reveal that the drain current continues to flow—often in both directions—even while the LO is high.

Accordingly, Dr. Galton has not shown the claim discharged percentages are present in DeMaw when the switches are open (OFF).

3. Dr. Galton's discharge period is overstated.

By defining the “switch open period” as the entire LO high interval, Dr. Galton's analysis includes time segments during which the transistor is clearly conducting current – when the switch is closed (ON). This inflates the time interval over which voltage is measured and distorts the computed discharge percentage. For example, if LO is high from time t_0 to t_1 , but the drain current remains non-zero for all or part of that window, then the switch is not actually “open” during the full period. By including that full interval in his calculation, Dr. Galton overstates the duration of discharge, which biases the percentage downward or causes incorrect interpretation of charging versus discharging behavior. Ex.-2021, ¶436.

A POSITA would know that if the transistor is still conducting, then charge is not being discharged from the capacitor through a high-impedance open switch. Rather, it is still part of an active conduction path, which may involve both charging and discharging effects due to reactive feedback. Ex.-2021, ¶437.

A POSITA would recognize that the claimed “period of time that the first switching device is open” must correspond to actual switch behavior—not just control signal levels. Ex.-2021,¶438.

Accordingly, Dr. Galton's discharge calculations are based on the wrong time interval, rendering his percentage discharge values inaccurate and unsupported by the evidence. Ex.-2021,¶439.

These inconsistencies further undermine the reliability of Dr. Galton's analysis and confirm that DeMaw does not disclose the required claim limitation. Ex.-2021,¶440.

B. Ground 2: Macnally

Macnally fails to disclose, teach, or suggest each and every limitation of claims 18-21. Specifically, Macnally does not disclose (1) “electrically coupling the information signal to a first capacitor and the inverted information signal to a second capacitor,” (2) first and second “switching device,” or (3) capacitors discharging certain percentages of “total charge stored” “during a period of time that the [first/second] *switching device is open*.” Ex.-2021,¶441.

The reason that Macnally does not disclose these claim elements is because, unlike the claimed invention, Macnally is a heterodyne system, which uses non-sampling mixers. In Macnally, the transistors remain active – there is a continuous current flow. There are no periods of time when the transistors are “open” (OFF) as

required by claims 19-21. Thus, Macnally does not disclose, teach, or suggest the claimed features. Ex.-2021,¶442.

Notably, Petitioner does not (and cannot) point to any express disclosure in Macnally that describes the charging/discharging cycles of capacitors, let alone the discharge percentage ranges as claimed in claims 19-21. Macnally contains no such teachings. Petitioner is, thus, forced to rely on Dr. Galton's circuit simulations. Ex.-2021,¶443.

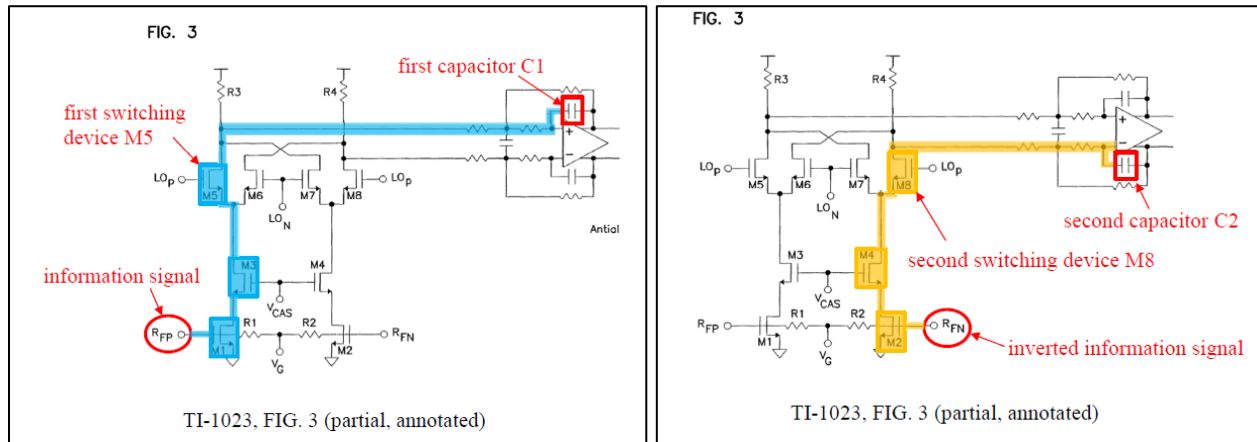
But Dr. Galton's simulations are flawed as discussed in Sections IX.D, E. Dr. Galton's simulations are purely speculative and insufficient to establish that the claimed capacitor discharge behavior is present in Macnally. Ex.-2021,¶444.

1. Macnally does not disclose, teach, or suggest the “electrically coupling.”

Claim 18 recites: “electrically coupling the information signal to a first capacitor and the inverted information signal to a second capacitor.” The PTAB already construed “electrically coupling” to be “indirectly or directly connecting such that an electrical signal can flow between.” See Section VII.B. Petitioner does not dispute this construction nor does Petitioner seek an alternative construction. Pet., 6.

In view of the PTAB's prior construction of “electrically coupled,” the claim language requires that the information signal (an electrical signal) *itself* must be able

to flow to the first capacitor, and the inverted information signal (another electrical signal) *itself* must be able to flow to the second capacitor. Petitioner ignores this requirement and simply focuses on the information signals being indirectly or directly connected to capacitors. Ex.-2021, ¶446.



In particular, Petitioner asserts that, in Macnally, (1) the R_{FP} input (blue above) is the information signal that is “electrically coupled” to capacitor C1 through first switching device M5, and (1) the R_{FN} input (orange above) in the inverted information signal that is “electrically coupled” to capacitor C2 through second switching device M8. Pet., 60-63. Ex.-2021, ¶447.

M1 and M2 are CMOS FETs. Dr. Galton agrees. Ex.-2036, 68:16-22. As shown above, Macnally's R_{FP} and R_{FN} inputs are applied to the *gates* of FETs M1 and M2, respectively, to *control* the flow of current between the drain (D) and source (S). Ex.-2021, ¶448.

As discussed above in Section VIII.B, in saturation, current only flows from the drain to the source. Ex.-2021, ¶449.

Unlike the drain and source of a CMOS FET, the gate does not provide a path for current to flow upward or through the drain. Instead, the gate acts as a control terminal that modulates the flow of current between the source and the drain. Ex.-2021, ¶450.

Because the R_{FP} and R_{FN} inputs are not themselves able to flow to capacitors C1 and C2 but instead merely *control* operation of M1 and M2, R_{FP} and R_{FN} inputs are not *electrically coupled* to the capacitors as construed by the PTAB. Ex.-2021, ¶451.

No signal or current flows upward or comes from M1, M2, R_{FP} , or R_{FN} . No current or signal flows from M1 or M2 to capacitors C1 or C1. As discussed in Section VIII.B above, the only current flowing in Figure 3 of Macnally comes from a power source and current only flows downward from the power source to ground. Ex.-2021, ¶452.

[illegible]

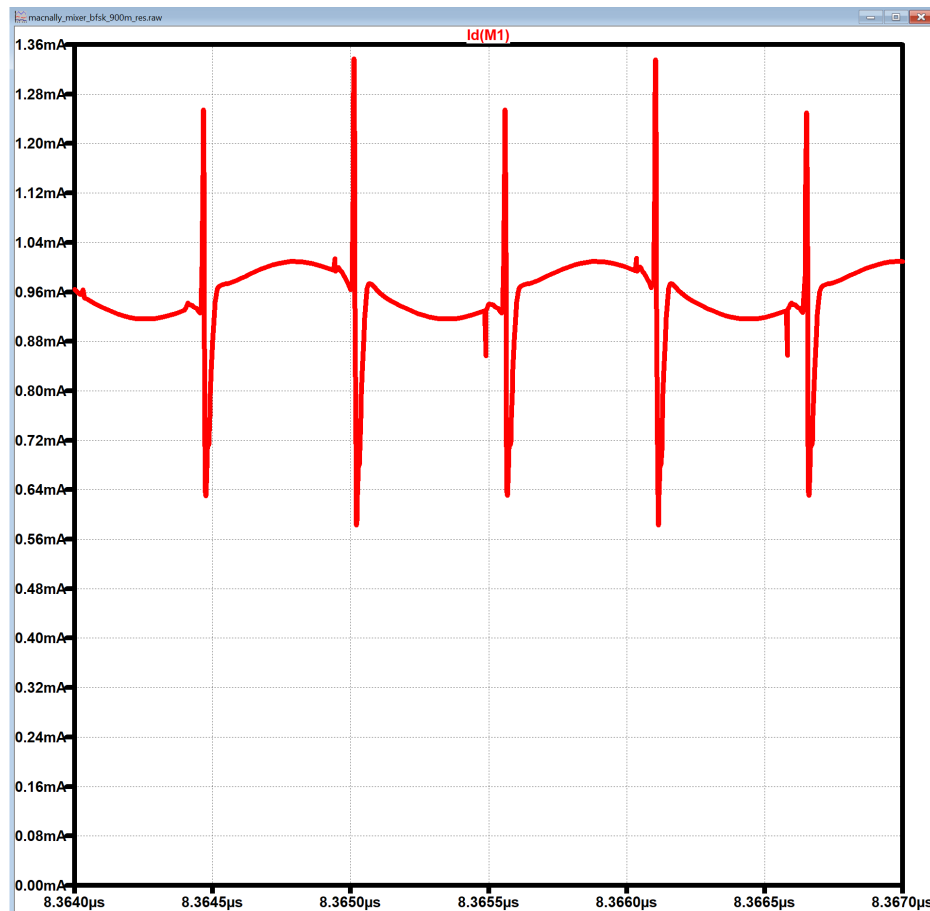
A POSITA understands that the LO_P and LO_N signals are differential signals, meaning that when LO_P is high, LO_N is low, and vice versa. Ex.-2021, ¶454.

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current flows through M5 and M1 to ground and M8 and M2 to ground.²¹ Ex.-2021,¶455.

Transistors M1 and M2 (and the RF input signals) only control how much of the current from the power supply is directed downward through M5, M6, M7, and M8. Ex.-2021,¶456.

²¹ On the other hand, when LO_N is high and LO_P is low, transistors M6 and M7 conduct. Current from the power supply flows through resistor R3 and R4. Some of the current is directed to capacitor C1 and C2), while the remainder of the current flows through M6 and M1 to ground and M7 and M2 to ground. Ex.-2021,n.10.



This behavior is confirmed in the simulations Dr. Ricketts ran using Dr. Galton's native LTspice files. Dr. Ricketts measured the current flowing from the drain to the source, i.e., the current flowing downward. As shown in the plot above, current through M1—the transistor controlled by the RFP signal—is strictly unidirectional (the current never becomes negative, which would be required for current to flow upward through M1), and thus only flows downward. This demonstrates that the information signal applied to the gate of M1 is not—and cannot be—electrically coupled to any capacitor in the circuit, as required by the claims. Furthermore, this plot demonstrates that there is no energy flowing upward

from the gate, as this is the plot of drain current, which would be the sum of any and all currents in the CMOS FET that flow through the drain node – the current is always downward. Ex.-2021,¶457.

While transistors M1 and M2 affect the distribution of current flow from the power source, they do not themselves actually supply the current to the capacitors. See Section VIII.B. Thus, neither current nor a signal flows from the R_{FP} and R_{FN} input signal to the capacitors. Accordingly, the R_{FP} and R_{FN} signals are not *electrically coupled* to capacitors C1 and C2 as that term has been construed. Ex.-2021,¶458.

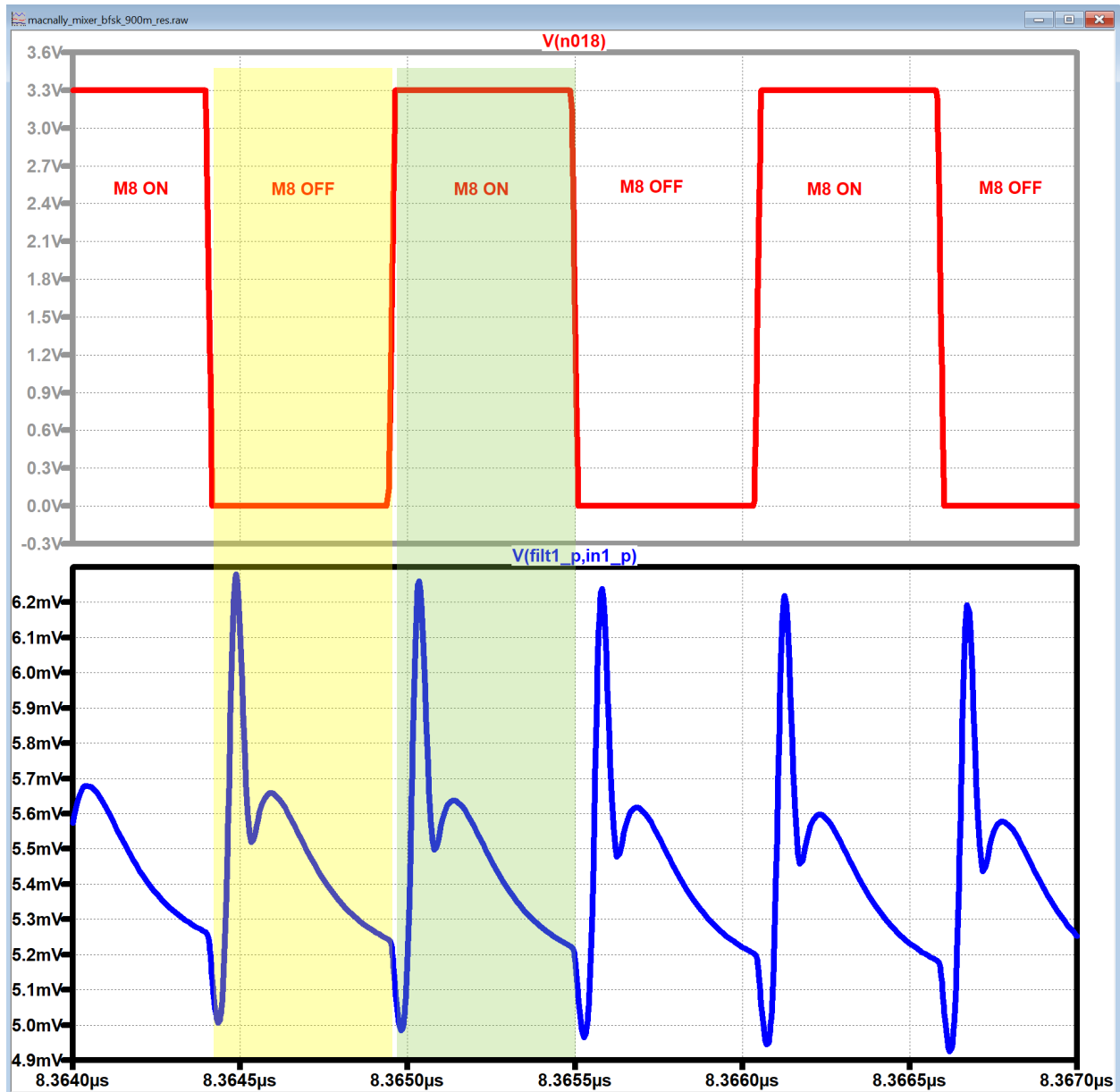
2. Macnally does not disclose a first and second “switching device.”

Claim 18 recites “a first and second switching device.” The Federal Circuit previously held that a “switch” is “an electronic component for opening and closing a circuit.” See Section VII.A. “Switching device” would have the same meaning.

Petitioner identifies transistors M5 and M8 in Figure 3 of Macnally as the claimed switching devices. However, transistors M5 and M8 do not “open” a circuit and, therefore, are not switching devices. Ex.-2021,¶460.

In Macnally's circuit, there is a continuous flow of current to capacitors C1 and C2, and also a continuous flow of current through transistors M1 and M2 regardless of the LO signal state. Ex.-2021,¶461.

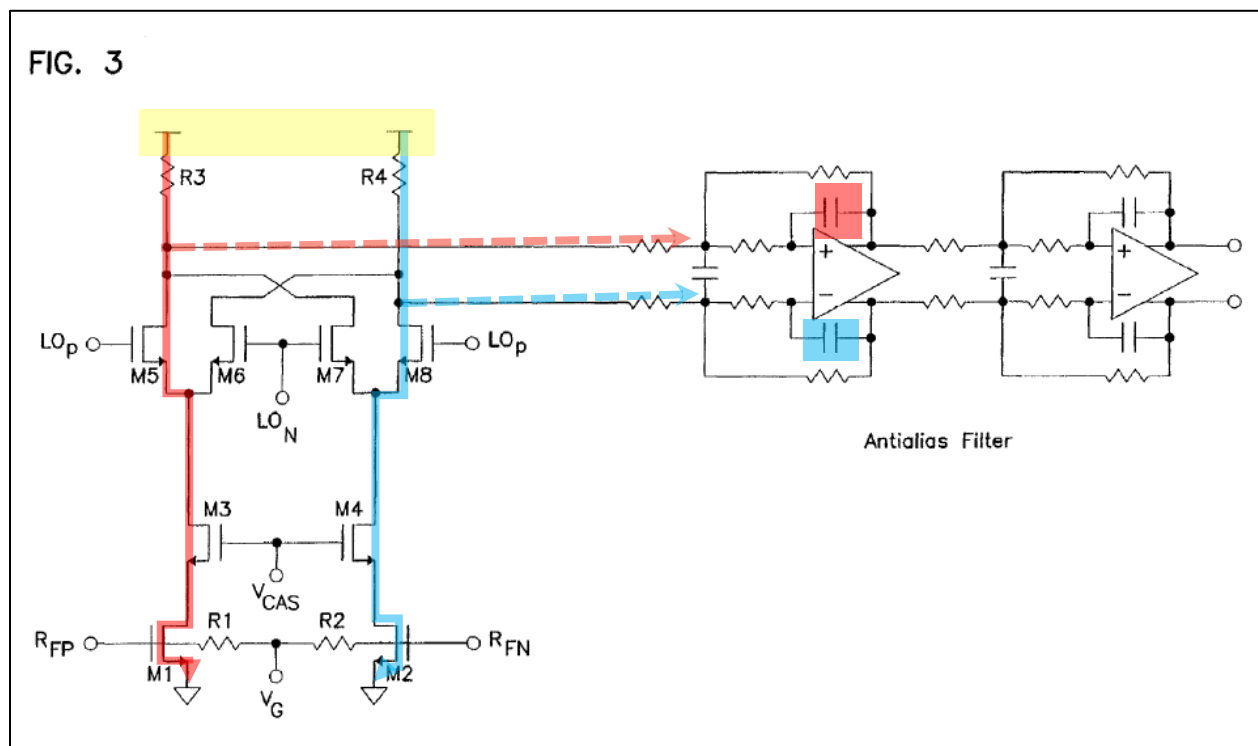
As demonstrated by the simulation results discussed in Section IX.E, the plot below shows both the LO signal and the capacitor voltage (V_c). The charge on the capacitor remains materially the same whether the corresponding transistor is ON (conducting) or OFF (not conducting) (Ex.-2021, ¶462):



As shown above, when M8 is ON (green) or OFF (yellow), the capacitor voltage remains materially unchanged across both phases. This is consistent with a continuous conduction – not switching. Ex.-2021,¶463.

If transistor M5 or M8 operated as switches in a sampling system, turning them OFF would isolate the capacitor from the signal path, allowing the capacitor to discharge through a load. But that is not what Macnally shows. Instead, energy continues to flow into the capacitors, even when M5 and M8 are OFF. Ex.-2021,¶464.

Thus, because the current supply is always flowing through the circuit from the power supply down to M1 and M2, transistors M5 and M8 are not “opening” a circuit. Even if M5 and M8 are not conducting (i.e., they are open/OFF), Macnally's circuit never experiences any interruption in the flow of current. This is due to the way that Macnally is configured to operate. Ex.-2021,¶465.



As shown above, when the LO_P signal is high, transistors M5 and M8 conduct. Current from the power supply (yellow) flows through resistor R3. Some of the current (dashed red line) flows to capacitor C1 (red box) while the remainder of the current (solid red line) flows down through M5 and M1. At the same time, current from the power supply flows through resistor R4. Some of the current (dashed blue line) flows to capacitor C2 (blue box) while the remainder of the current (slide blue line) flows through M8 and M2. Ex.-2021, ¶466.

[illegible]

Petitioner fails to account for the fact that when transistors M5 and M8 are not conducting current, M6 and M7 continue to conduct and vice versa. Consequently, the current supply remains uninterrupted in Macnally's circuit, and M5 and M8 do

not “opening a circuit.” Thus, transistors M5 and M8 are not “switching devices.”

Ex.-2021,¶468.

3. Dr. Galton's discharge calculations are incorrect.

During his deposition, Dr. Galton testified that he used the same Python script to generate the discharge percentage histograms for both the DeMaw and Macnally simulations. Ex.-2039, 37:16-38:2. Accordingly, the same flaws identified in Section X.A above regarding the discharge calculations in DeMaw apply equally to Dr. Galton's discharge calculations for Macnally. Dr. Galton has not shown that Macnally's capacitors discharge within the claimed percentage range when the switching device is open. Ex.-2021,¶469.

Dated: April 21, 2025

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that this Patent Owner's Response complies with the type-volume limitation of 37 C.F.R. § 42.24(b) because it contains 13,875 words, as determined by the word-processing program used to prepare the brief, excluding the parts of the brief exempted by 37 C.F.R. § 42.24(a)(1).

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that the foregoing PATENT OWNER'S RESPONSE and Exhibits were served electronically via email on April 21, 2025, on the following counsel of record for Petitioners:

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