

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Title:	DOWN-CONVERTING ELECTROMAGNETIC SIGNALS, INCLUDING CONTROLLED DISCHARGE OF CAPACITORS	

SECOND DECLARATION OF IAN GALTON, PH.D.

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I, Dr. Ian Galton, declare:

I. Overview

1. This document provides an overview of additional simulations performed beyond those described in my original Declaration (TI-1003) in support of the '342 patent IPR petition. All additional circuits and configurations that have been simulated to support my analysis of the prior art for the '342 patent beyond those presented in my original Declaration are described in the document, and none of the results change the conclusions presented in my original Declaration regarding the alleged invention disclosed in the '342 patent.

2. All of the files necessary to duplicate the results presented below along with additional text files that provide relevant instructions and information are being provided with this Second Declaration.

II. DeMaw Circuit With Siliconix U430 JFET Models

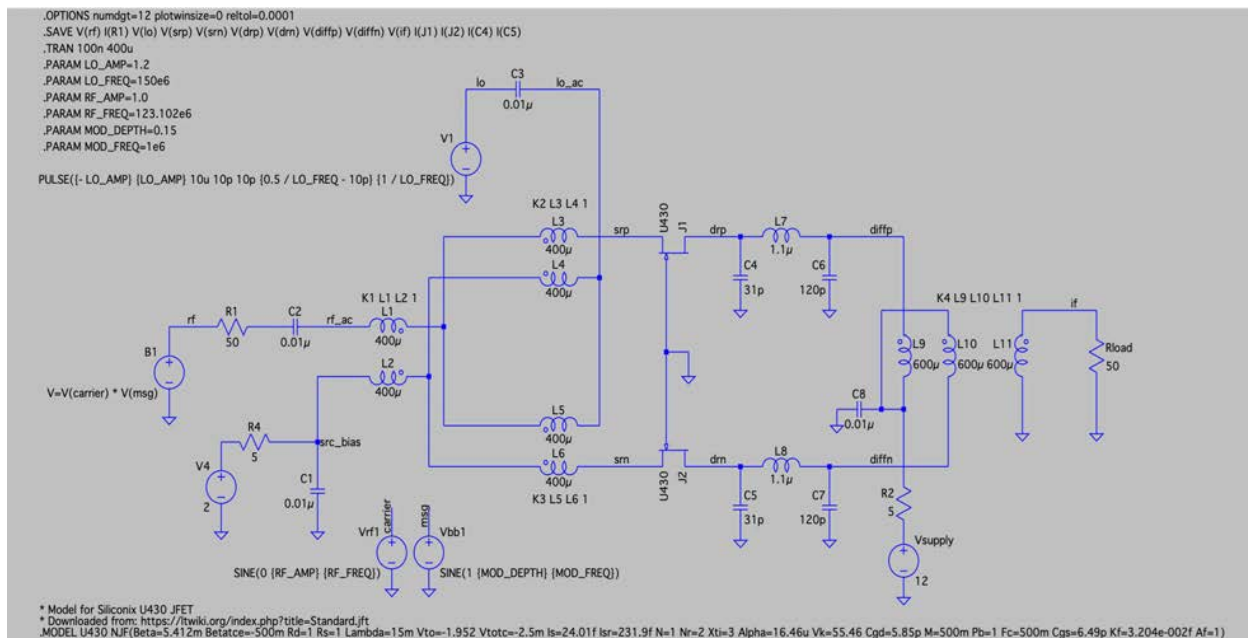
3. My original Declaration mentioned that the DeMaw circuit had been simulated with Siliconix U430 JFET models. However, the circuit was inadvertently simulated with default, generic LTspice JFET models. The first set of simulation results shown in **Part A** of this section correspond to the same version of the DeMaw circuit, the same input, and the same local oscillator (LO) signals that were described in my original Declaration, except with the Siliconix U430 JFET models.

4. Using the Siliconix U430 JFET models in place of the generic LTspice

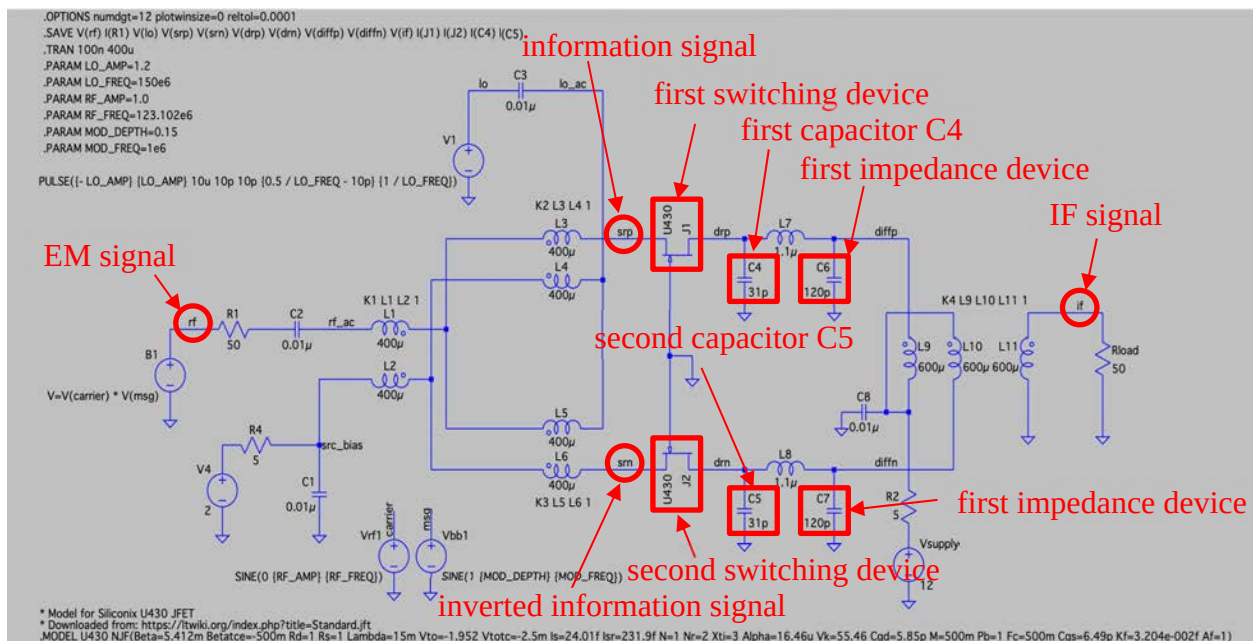
JFET models resulted in a significant increase in mixer gain. To ensure that the increase in mixer gain did not cause the mixer to operate above its compression point (i.e., outside of its linear region), the second set of simulation results shown in **Part B** of this section correspond to exactly the circuit configuration and LO signal as in the simulation results shown in **Part A** except with a 6 dB lower-power input signal. As can be seen from the results presented below, using the 6 dB lower-power input signal reduced the mixer's output signal power by 6 dB, thereby indicating that the mixer was not operating above its compression point when simulated to generate the Part A results.

A. Simulation of DeMaw Circuit Using Siliconix U430 JFET Models

5. DEMAW-SIM-FIG. 1 (revised, clean), below, is a graphical representation of the LTspice simulation of the DeMaw Figure 6.7 circuit using the Siliconix U430 JFET models. DEMAW-SIM-FIG. 1 (revised, annotated) is an annotated version that identifies the elements of claim 18 and corresponds to DEMAW-SIM-FIG. 1 in my original Declaration. Everything I wrote in my original Declaration about DEMAW-SIM-FIG. 1 is true of DEMAW-SIM-FIG. 1 (revised).



DEMAW-SIM-FIG. 1 (revised, clean). DeMaw circuit as described in the original Declaration but with U430 JFET models (highlighting two capacitors).

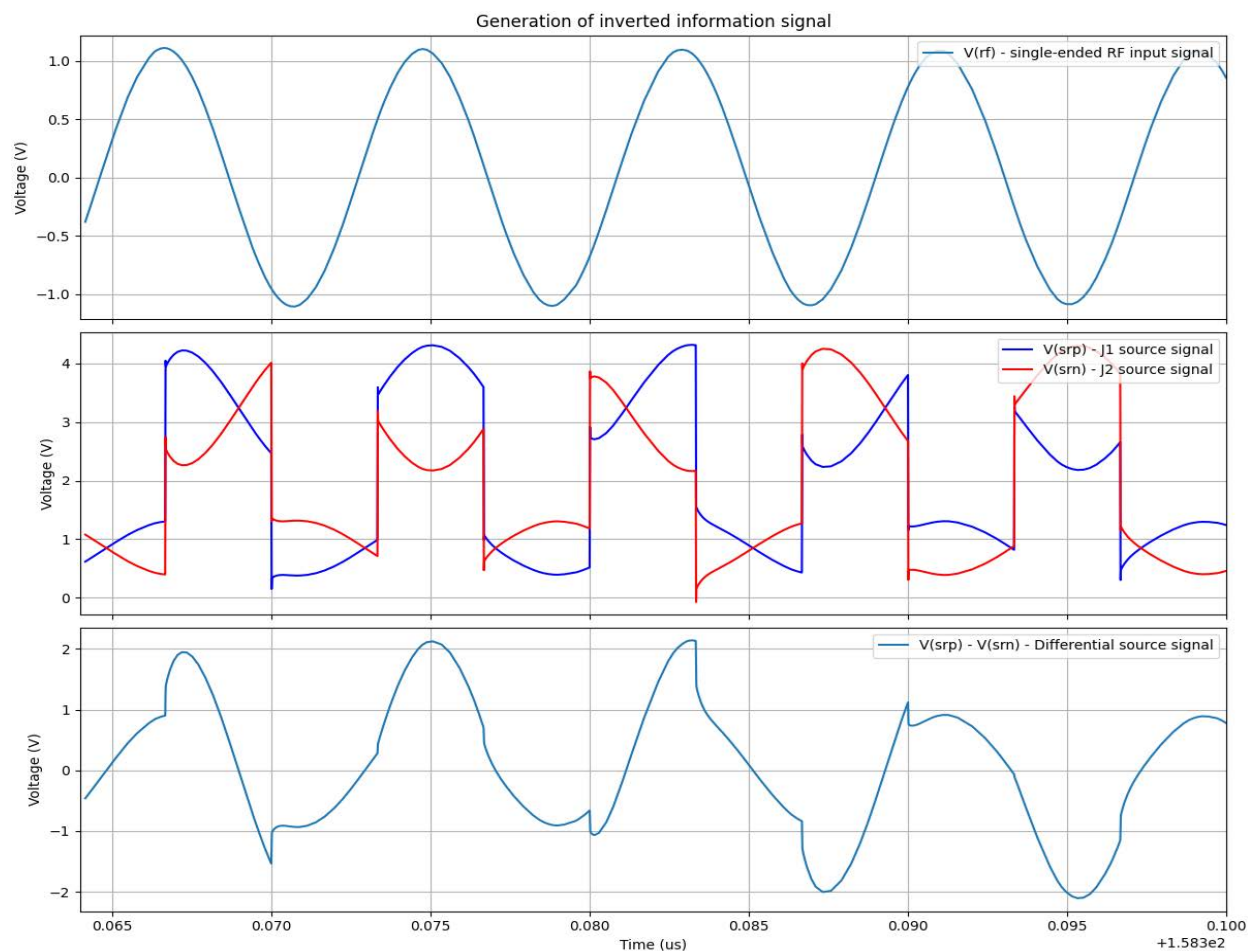


DEMAW-SIM-FIG. 1 (revised, annotated).

6. As I mentioned already, the circuit simulation above is structurally the

same as the simulation I provided in my previous declaration. Therefore, I only provide one annotation to the updated DeMaw circuit simulation graphic showing the structural elements (including the U430 JFETs), even though I also provide further simulations using different input values and circuit component values.

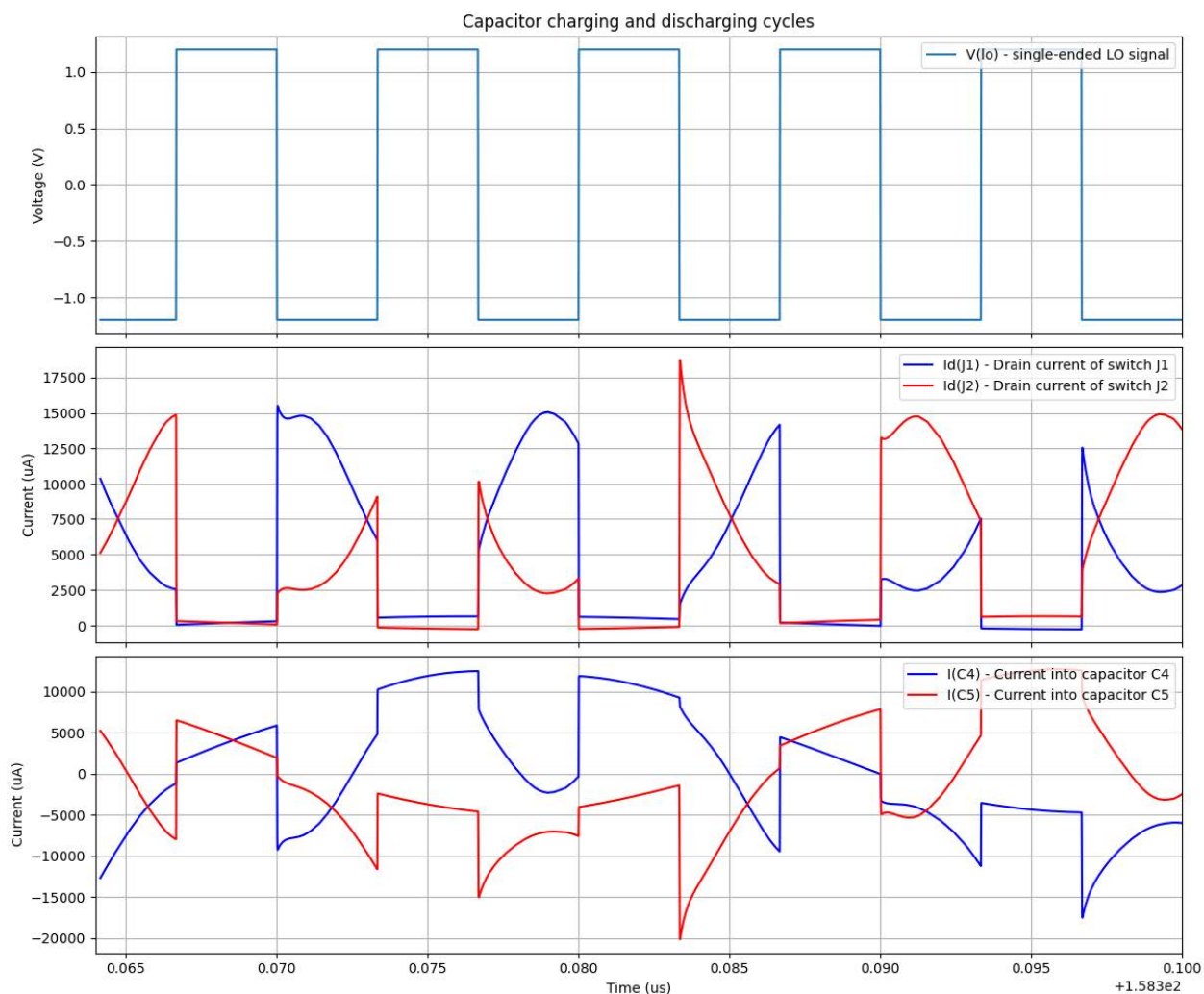
7. DEMAW-SIM-FIG. 4 (revised) is a graphical representation of the generation of the inverted information signal of the DeMaw circuit simulation of DEMAW-SIM-FIG. 1 (revised). The revised version additionally shows $V(\text{rf})$, the single ended RF input signal, and $V(\text{srp})$ - $V(\text{sm})$, the differential source signal. The information signal and inverted information signal correspond to claims 18.1-18.2. Everything I wrote in my original Declaration about DEMAW-SIM-FIG. 4 is true of this revised version.



DEMAW-SIM-FIG. 4. Graphical representation of the generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1 (revised)).

8. DEMAW-SIM-FIG. 5 (revised) is a graphical representation of the charging and discharging cycles of both of the capacitors C4 and C5 highlighted in the DeMaw circuit of DEMAW-SIM-FIG. 1 (revised). DEMAW-SIM-FIG. 5 (revised) is applicable to elements 18.3-18.6, as well as claims 19-21. Everything I wrote in my original Declaration about DEMAW-SIM-FIG. 5 is true of this revised version. I noticed a typographical error in paragraphs 102-104 of the original Declaration where it mistakenly refers to “DEMAW-SIM-FIG. 4” when it should

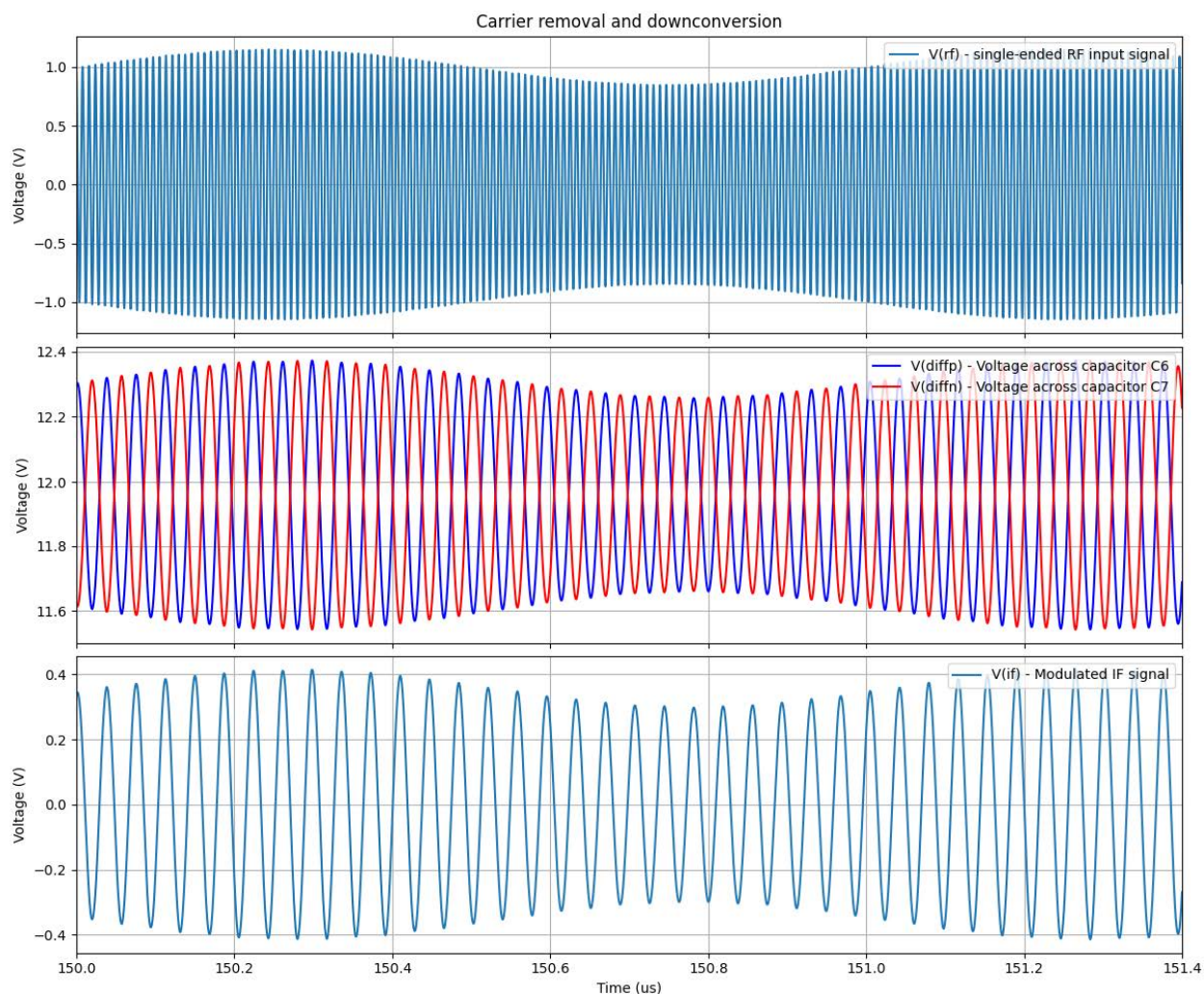
have referred to DEMA-SIM-FIG. 5, because paragraphs 102-104 describe and reproduce the content of DEMA-SIM-FIG. 5, not DEMA-SIM-FIG 4. Additionally, in paragraph 108, an annotated version of DEMA-SIM-FIG. 5 is mislabeled as “DEMA-SIM-FIG 4 (annotated).”



DEMA-SIM-FIG. 5 (revised). Graphical representation of the charging and discharging cycles of both of the capacitors highlighted in the DeMaw circuit of DEMA-SIM-FIG. 1 (revised).

9. DEMA-SIM-FIG. 6 (revised) is a graphical representation showing

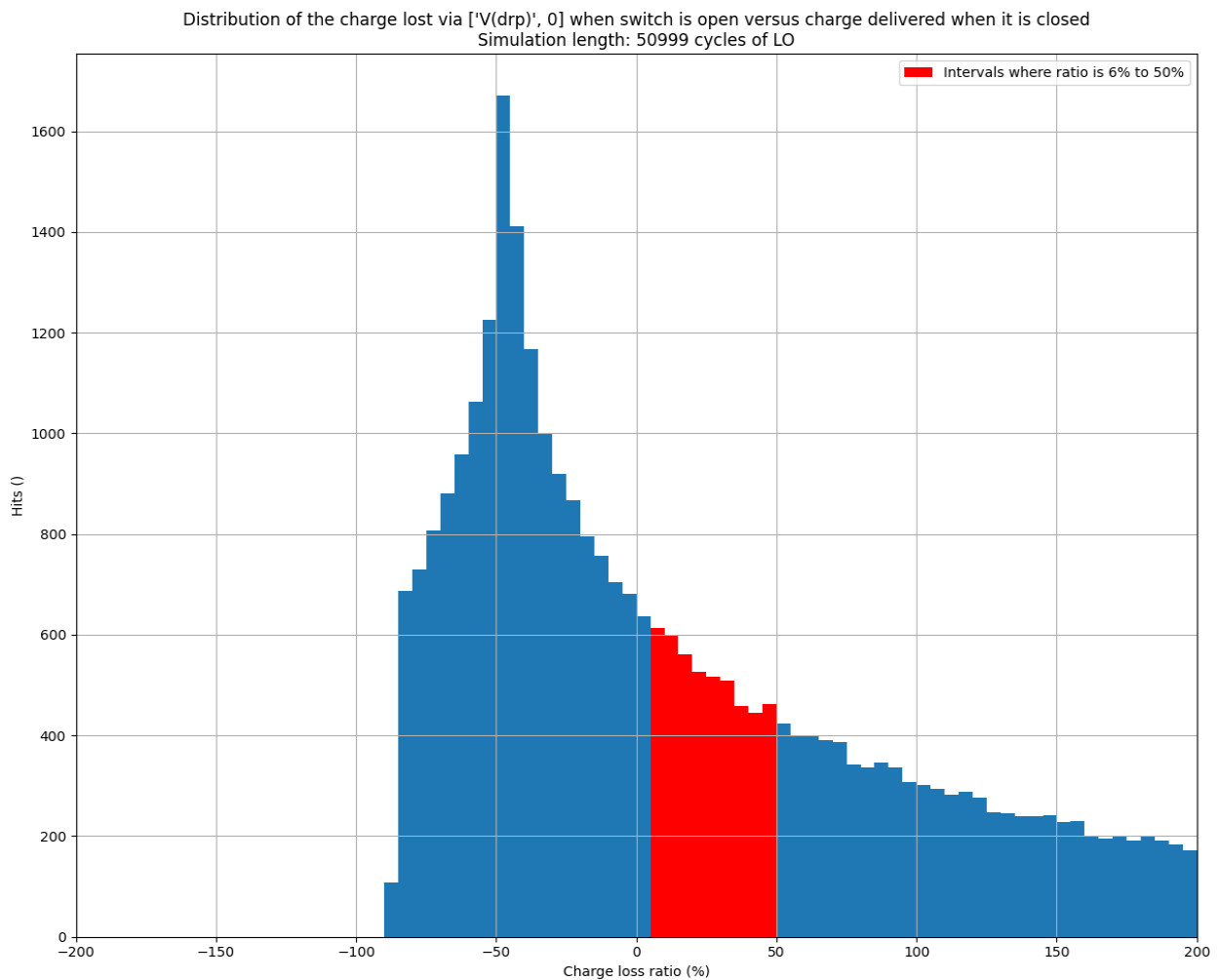
the carrier removal and down-conversion. DEMAW-SIM-FIG. 6 (revised) is applicable to claims 18.5 and 23 (both of which I understand are statutorily disclaimed. Everything I wrote in my original Declaration about DEMAW-SIM-FIG. 6 is true of this revised version. I noticed a typographical error in paragraph 110 of the original Declaration where it mistakenly reproduces a portion of DEMAW-SIM-FIG. 6 labeled as “DEMAW-SIM-FIG. 5.” The correction to the mistake is clear, however, because the graph mislabeled as DEMAW-SIM-FIG. 5 is clearly a portion of DEMAW-SIM-FIG. 6.



DEMAW-SIM-FIG. 6 (revised). Graphical representation of the carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1 (revised)).

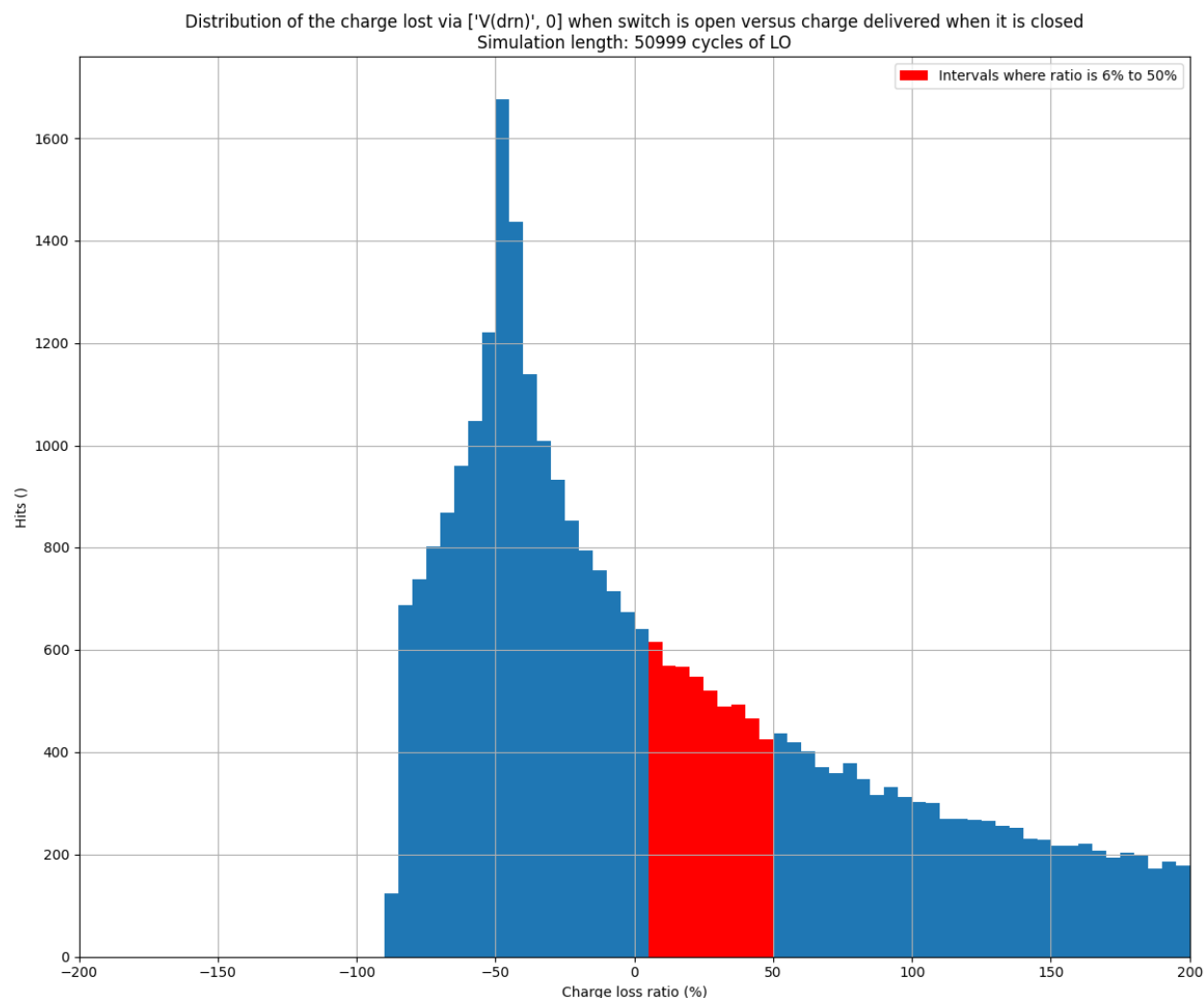
10. In my original Declaration, I provided one histogram of the charge loss ratio percentages that was representative of capacitors C4 and C5 (DEMAW-SIM-FIG. 7). I have generated two histograms here; one for each capacitor DEMAW-SIM-FIG. 7A and 7B. Everything I wrote in my original Declaration about DEMAW-SIM-FIG. 7 is true of DEMAW-SIM-FIG. 7A and 7B (revised). DEMAW-SIM-FIG. 7A (revised) is a histogram showing the charge loss ratio percentages for

the first capacitor C4 of the circuit of DEMAW-SIM-FIG. 1 (revised).



DEMAW-SIM-FIG. 7A (revised). Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1 (revised)).

11. DEMAW-SIM-FIG. 7B (revised) is a histogram of the charge loss ratio percentages for the second capacitor C5 of the circuit of the circuit of DEMAW-SIM-FIG. 1 (revised).

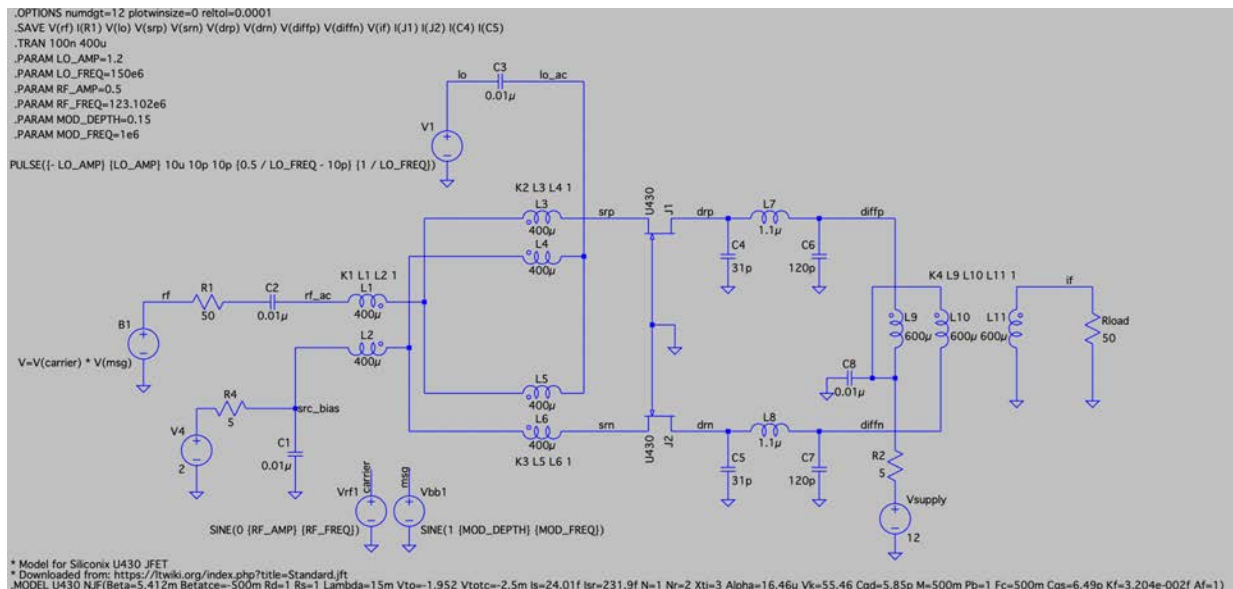


DEMAW-SIM-FIG. 7B (revised). Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1 (revised)).

B. DeMaw Circuit Simulation of DEMAW-SIM-FIG. 1 (revised) Using Smaller Input Signal

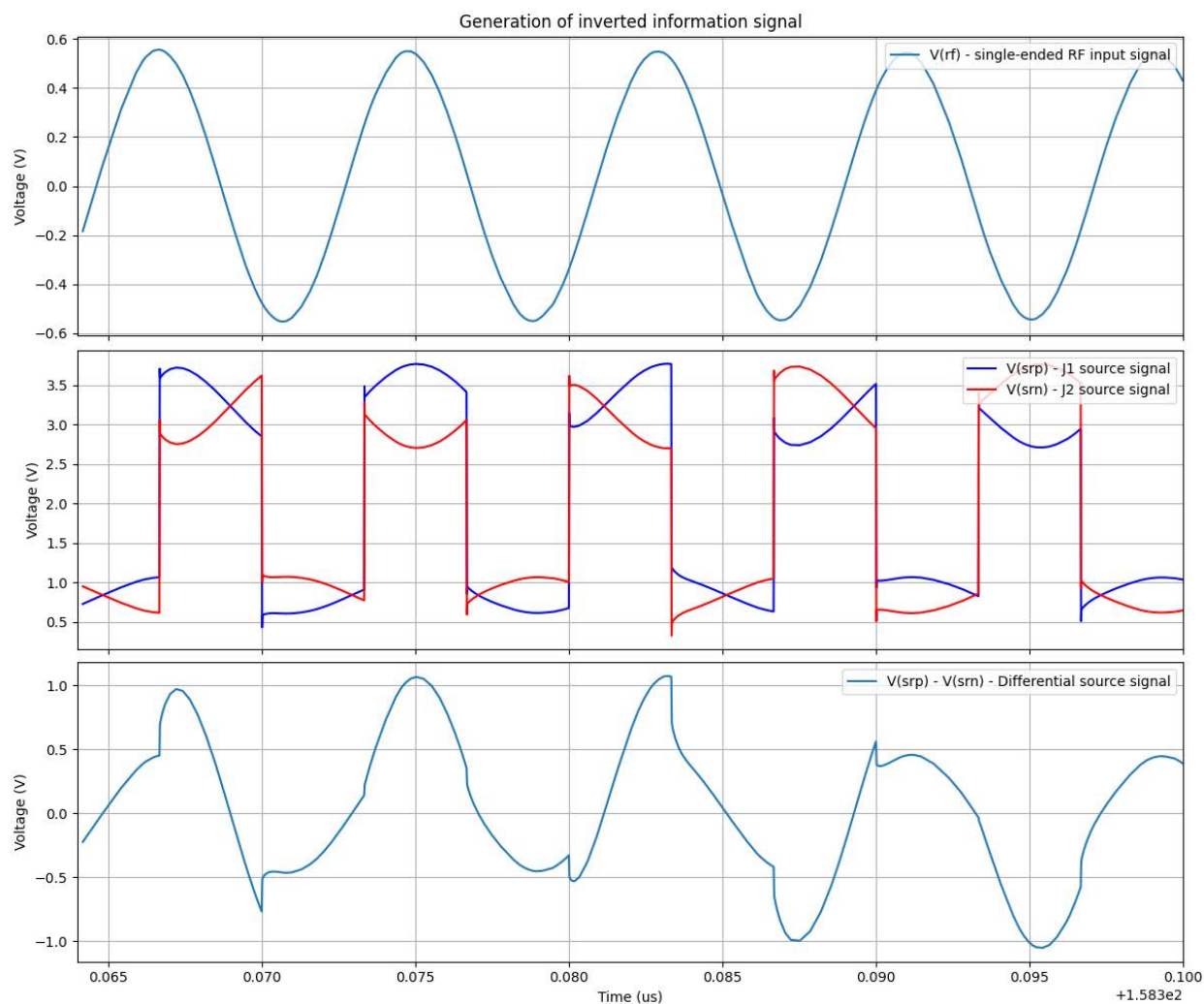
12. DEMAW-SIM-FIG. 1.1 is a graphical representation of the LTspice simulation of the DeMaw Figure 6.7 circuit using the Siliconix U430 JFET models (as shown in DEMAW-SIM-FIG. 1 (revised)), but with a smaller input signal amplitude. I have created additional figures DEMAW-SIM-FIGS. 4.1, 5.1, 6.1, 7.1A

and 7.1B based on simulation output from DEMA-W-SIM-FIG. 1.1. DEMA-W-SIM-FIGS. 4.1, 5.1, 6.1, 7.1A and 7.1B respectively show the same simulation output from DEMA-W-SIM-FIG. 1.1 as DEMA-W-SIM-FIGS. 4, 5, 6, and 7 show from DEMA-W-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMA-W-SIM-FIGS. 1, 4, 5, 6, and 7 are likewise supported by DEMA-W-SIM-FIGS. 1.1, 4.1, 5.1, 6.1, 7.1A and 7.1B.



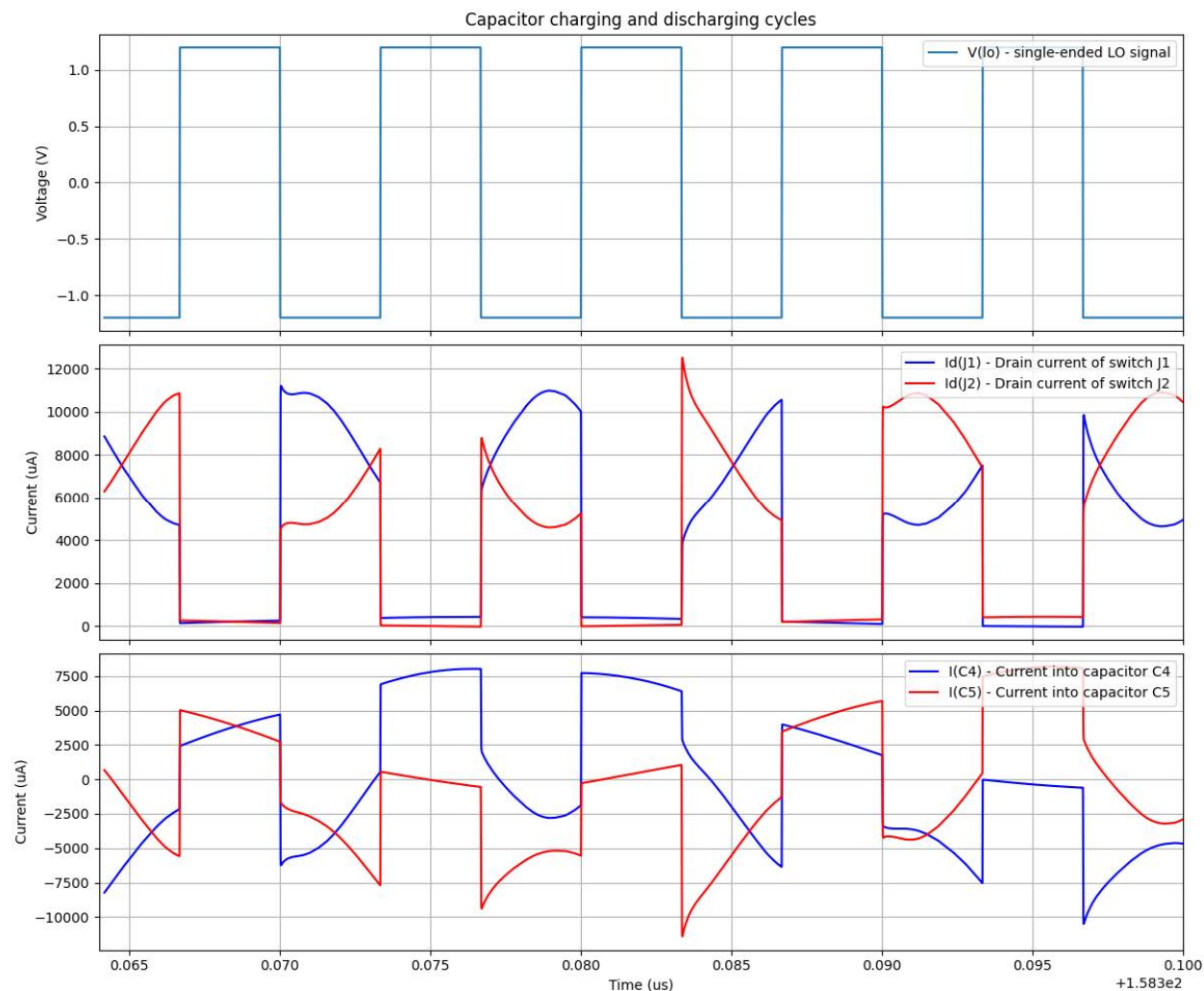
DEMAW-SIM-FIG. 1.1. DeMaw circuit as described in the original Declaration except with U430 JFET Models and reduced input signal amplitude.

13. DEMA-W-SIM-FIG. 4.1 is a graphical representation of the generation of the inverted information signal of the DeMaw circuit simulation of DEMA-W-SIM-FIG. 1.1.



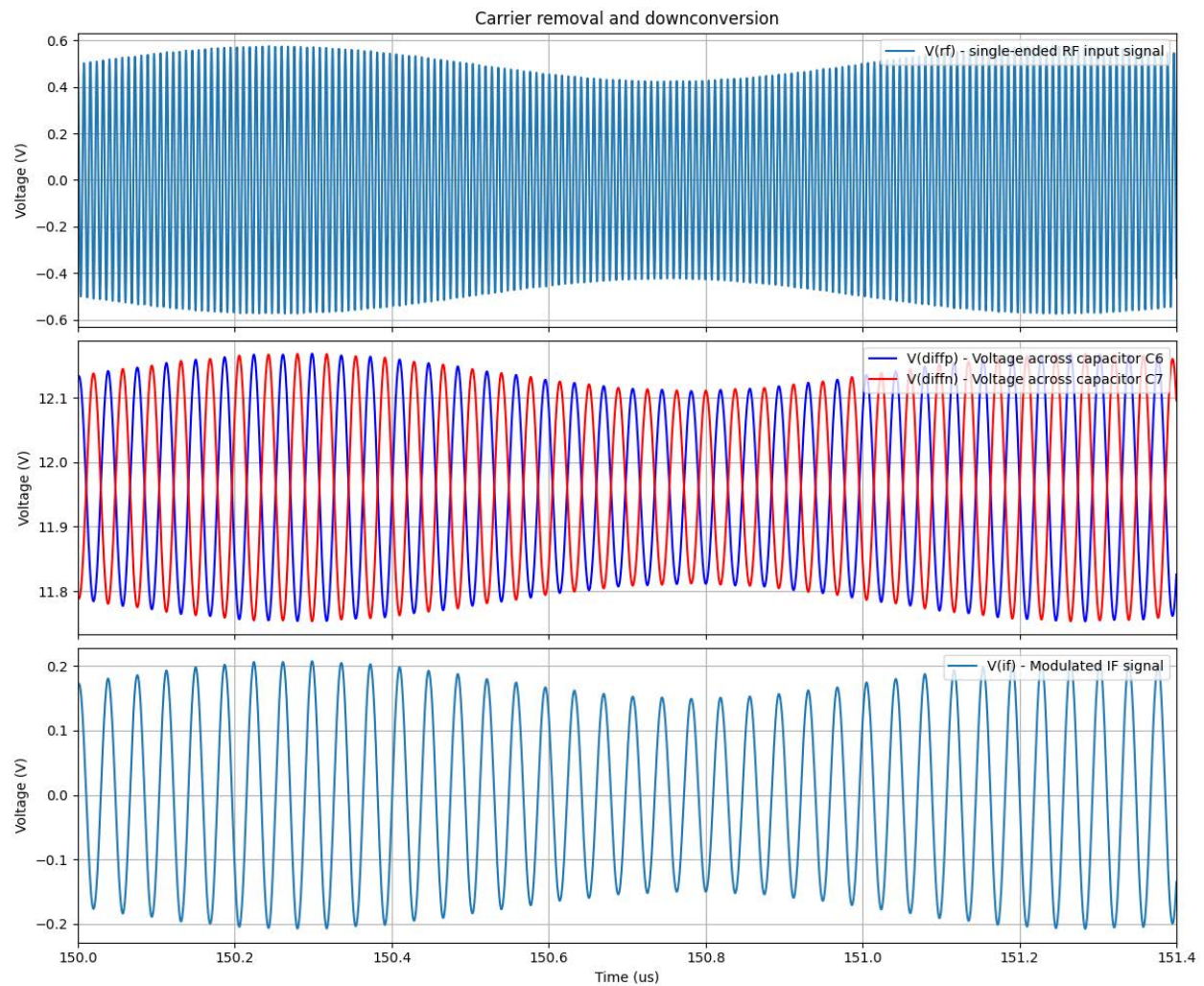
DEMAW-SIM-FIG. 4.1. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.1).

14. DEMAW-SIM-FIG. 5.1 is a graphical representation of the charging and discharging cycles of both of the capacitors C4 and C5 highlighted in the DeMaw circuit of DEMAW-SIM-FIG. 1.1. My conclusions regarding claim elements 18.3-18.6, as well as claims 19-21, based on DEMAW-SIM-FIG. 5 (revised) are likewise supported by DEMAW-SIM-FIG. 5.1.



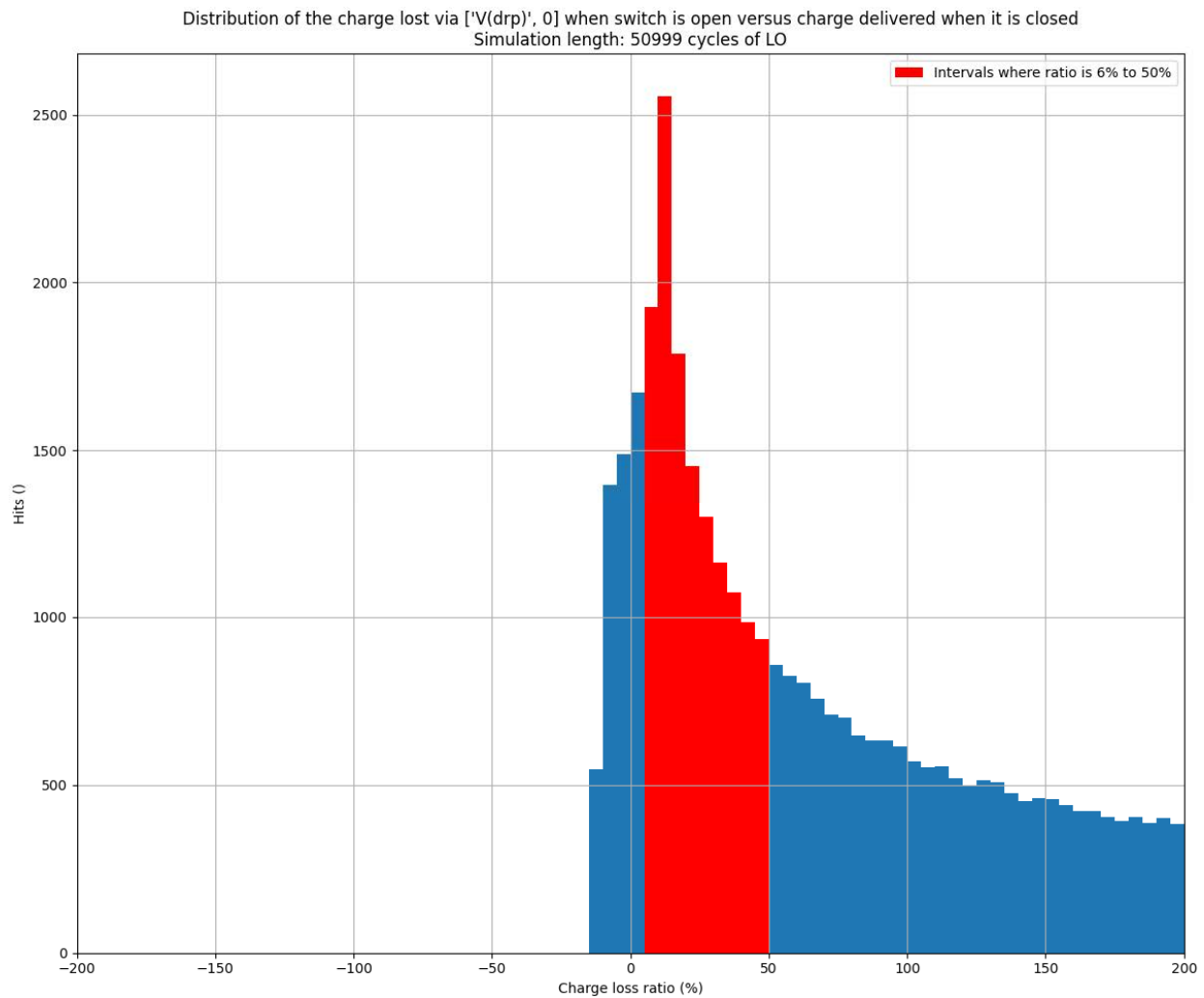
DEMAW-SIM-FIG. 5.1. Graphical representation of the charging and discharging cycles of capacitors C4 and C5 in the DeMaw circuit of DEMAW-SIM-FIG. 1.1.

15. DEMAW-SIM-FIG. 6.1 is a graphical representation showing the carrier removal and down-conversion. My conclusions regarding claim element 18.5 and claim 23 based on DEMAW-SIM-FIG. 6 are likewise supported by DEMAW-SIM-FIG. 6.1.



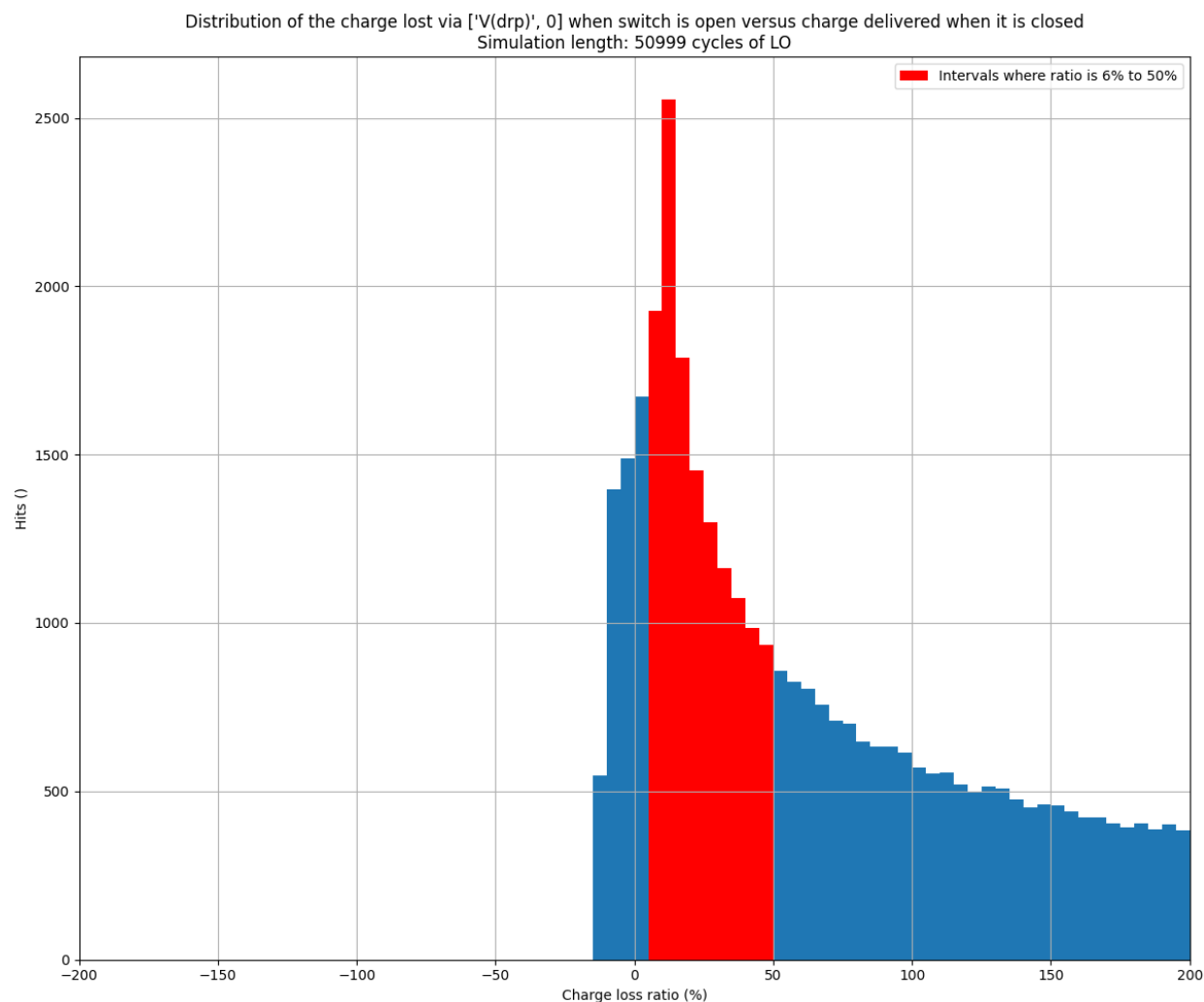
DEMAW-SIM-FIG. 6.1. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.1).

16. DEMAW-SIM-FIG. 7.1A is a histogram showing the charge loss ratio percentages for the first capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.1.



DEMAW-SIM-FIG. 7.1A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.1).

17. DEMAW-SIM-FIG. 7.1B is a histogram of the charge loss ratio percentages for the second capacitor C5 of the circuit of the circuit of DEMAW-SIM-FIG. 1.1.



DEMAW-SIM-FIG. 7.1B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.1).

III. DeMaw Circuit Modified to Match DeMaw FIG. 6.7 With a Squared-Up LO

18. As explained in my original Declaration, the simulated DeMaw circuit had some minor differences relative to the circuit shown in FIG. 6.7 of DeMaw. Although my original Declaration explained why these differences are not significant to the conclusions presented in the original Declaration, the Patent

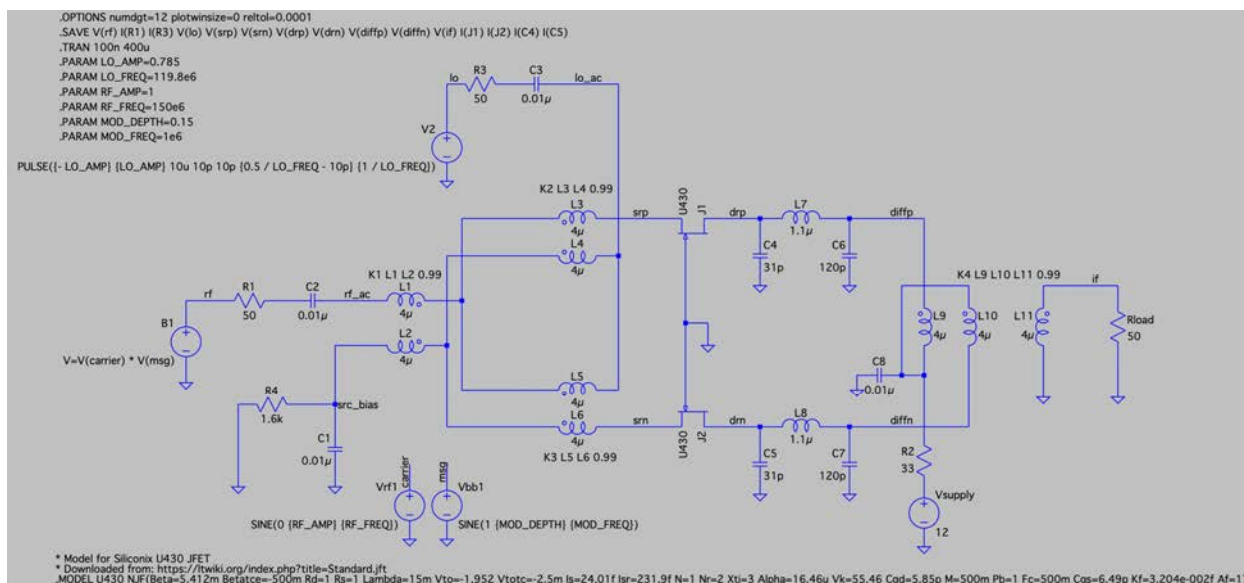
Owner's Preliminary Response (POPR) accused me of having made the circuit different than that shown in FIG. 6.7 of DeMaw to "get the results [that TI] needed." To address this criticism, the set of simulation results presented in this section correspond as closely as possible to the circuit shown in FIG. 6.7 given the information provided in the figure and associated text of DeMaw. Five sets of simulation results are presented which differ only in the power of the RF input to the mixer.

19. The POPR falsely claims that DeMaw "specifically teaches a sinusoidal LO." As I explained in my deposition, it is common practice to use LO signals that approximate square waves (also known as "squared-up" LO signals), so the simulations below use a squared-up LO.

A. Simulation Results For a Large Input Signal

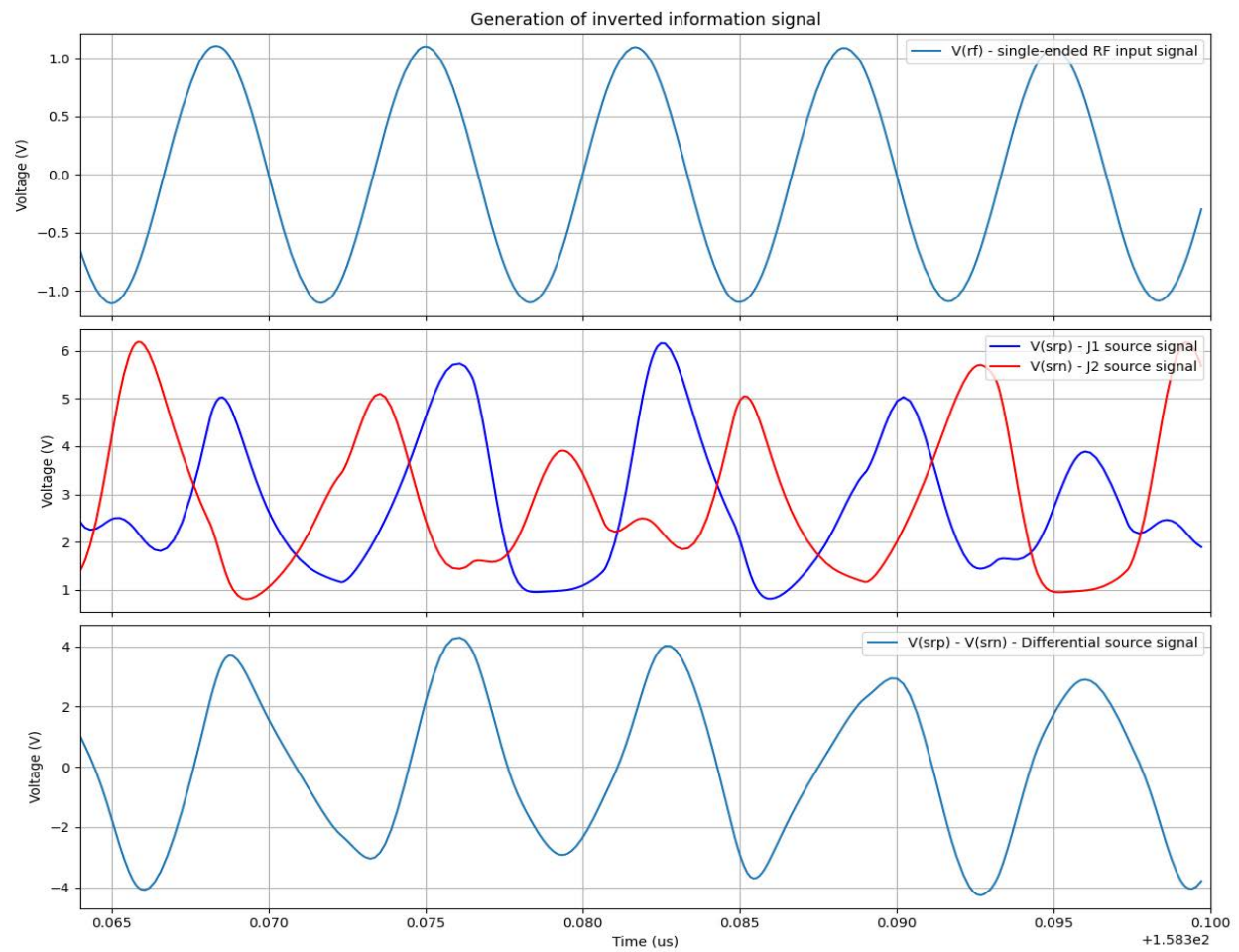
20. DEMA-SIM-FIG. 1.2 is a schematic representation of the simulated DeMaw Figure 6.7 circuit using a large input signal and a squared-up LO. I have created additional figures DEMA-SIM-FIGS. 4.2, 5.2, 6.2, 7.2A and 7.2B based on simulation output from DEMA-SIM-FIG. 1.2. DEMA-SIM-FIGS. 4.2, 5.2, 6.2, 7.2A and 7.2B show the same simulation output from DEMA-SIM-FIG. 1.2 as DEMA-SIM-FIGS. 4, 5, 6, and 7 show from DEMA-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMA-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMA-SIM-FIGS. 1.2, 4.2,

5.2, 6.2, 7.2A and 7.2B.



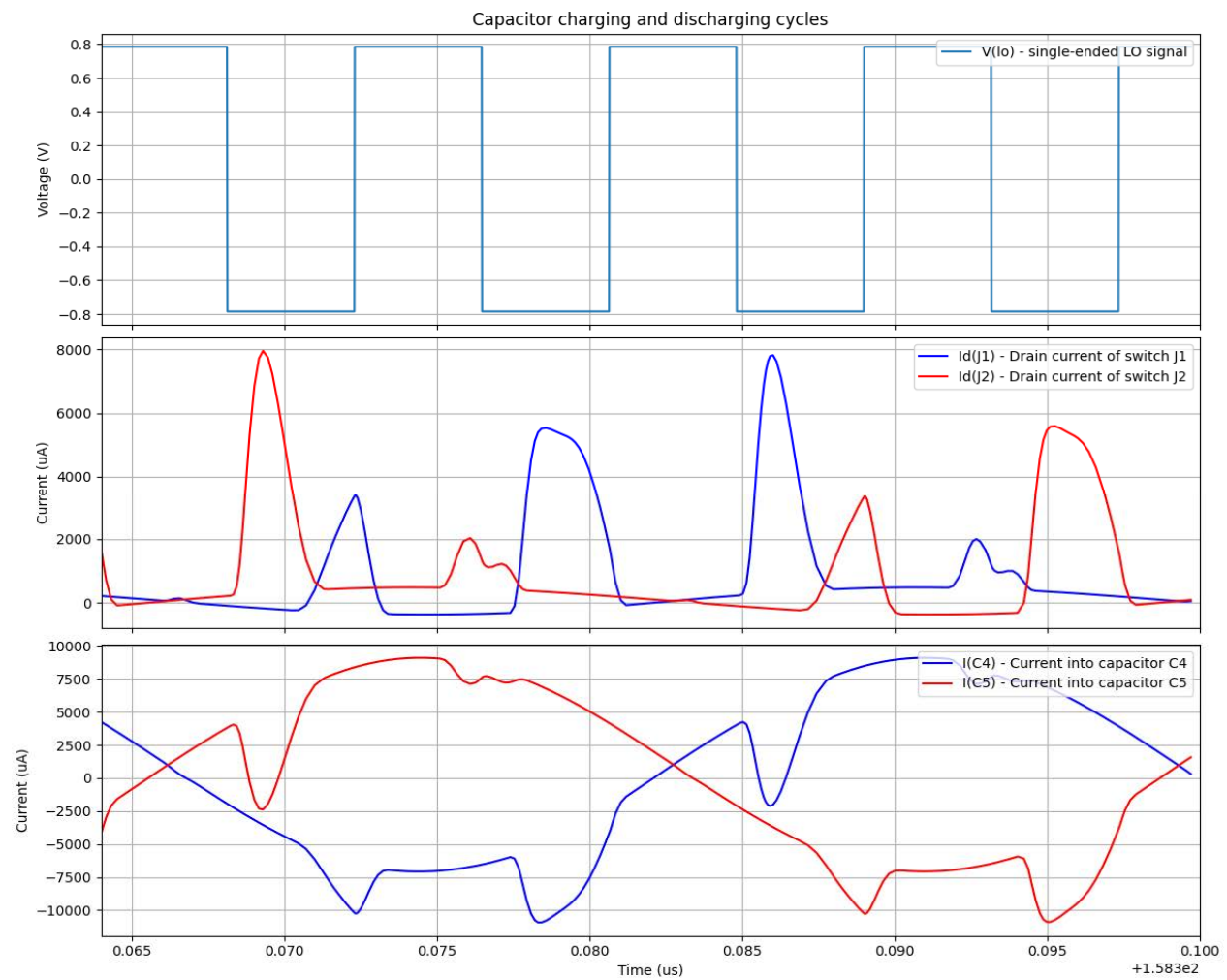
DEMAW-SIM-FIG. 1.2. DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and a large input signal.

21. DEMAW-SIM-FIG. 4.2 is a graphical representation of the generation of the inverted information signal of the DeMaw circuit simulation of DEMAW-SIM-FIG. 1.2.



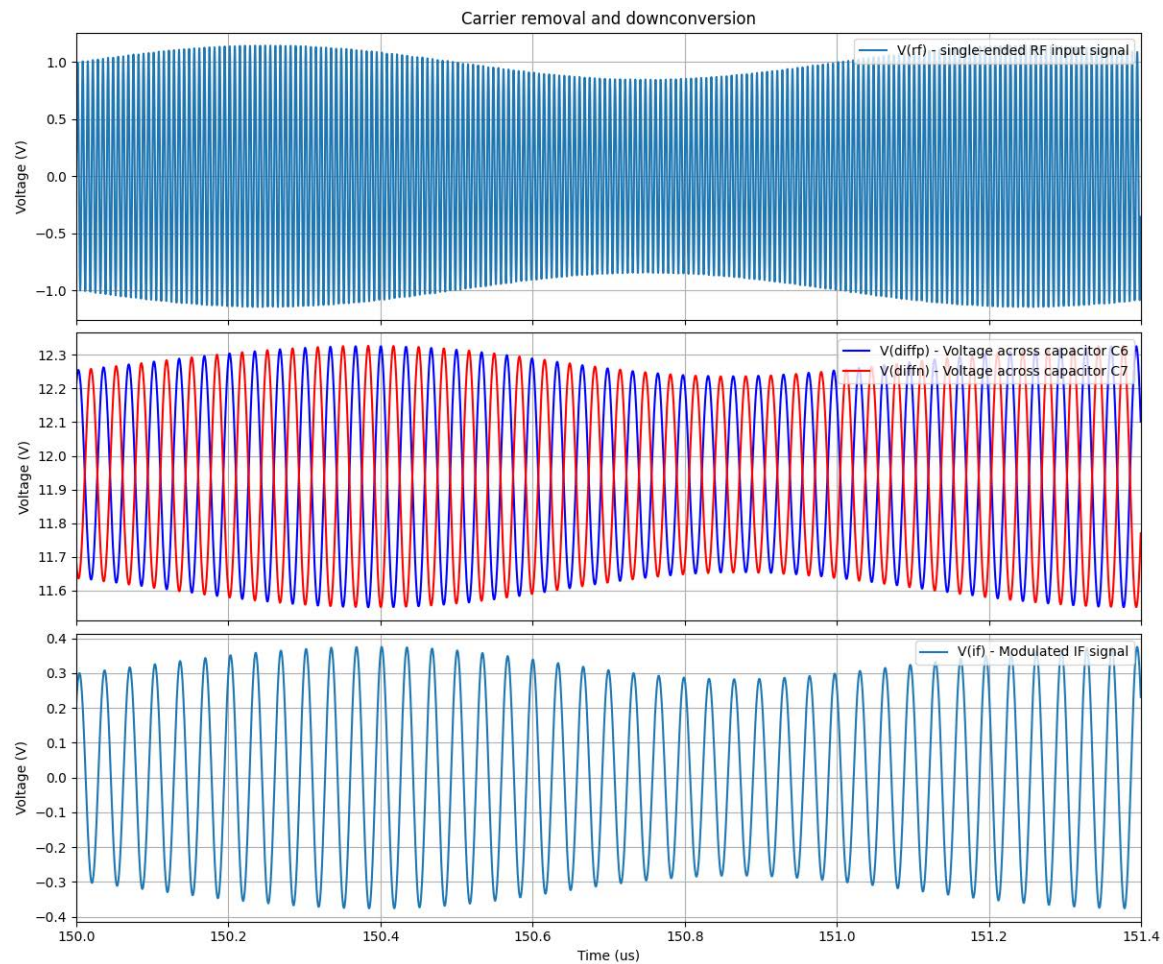
DEMAW-SIM-FIG. 4.2. Generation of information signal and inverted information signal (circuit of DEMAW-SIM-FIG. 12).

22. DEMAW-SIM-FIG. 5.2 is a graphical representation of the capacitor charging and discharging cycles of capacitors C4 and C5 of the circuit of DEMAW-SIM-FIG. 1.2.



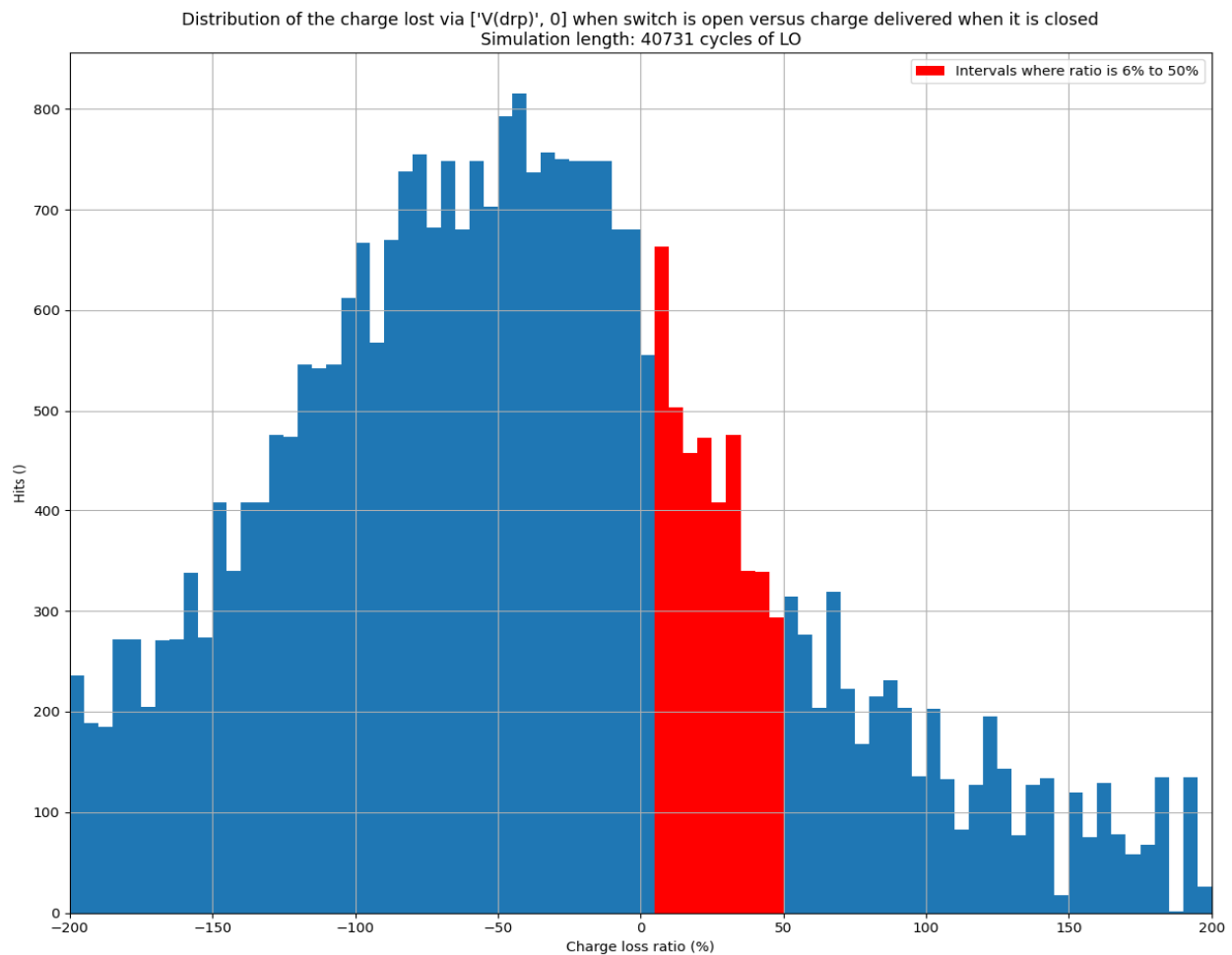
DEMAW-SIM-FIG. 5.2. Capacitors C4 and C5 charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.2).

23. DEMAW-SIM-FIG. 6.2 is a graphical representation of the carrier removal and down-conversion of the circuit of DEMAW-SIM-FIG. 1.2.



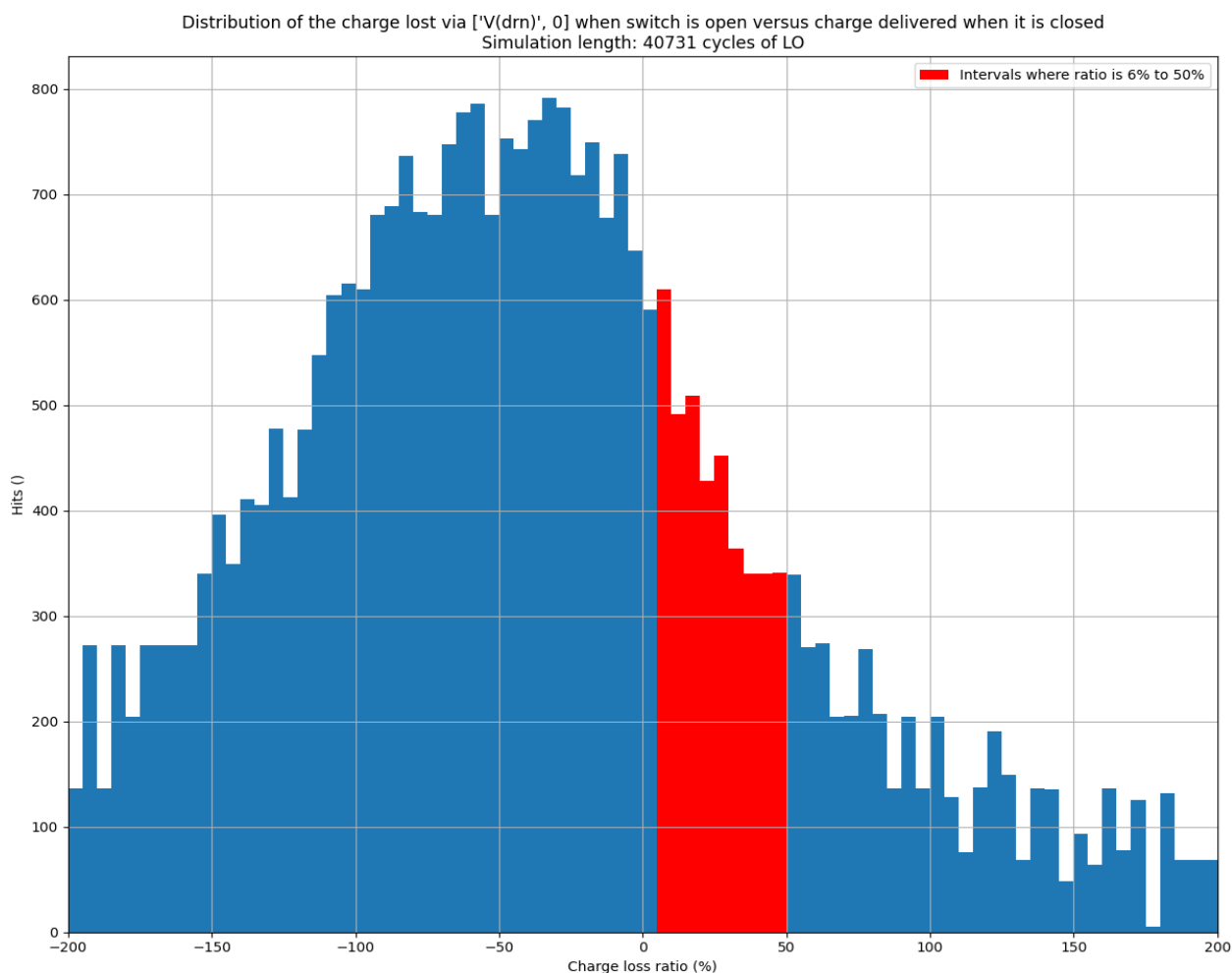
DEMAW-SIM-FIG. 6.2. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.2).

24. DEMAW-SIM-FIG. 7.2A is a histogram showing the charge loss ratio percentages for capacitor C4 in the circuit of DEMAW-SIM-FIG. 1.2.



DEMAW-SIM-FIG. 7.2A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.2).

25. DEMAW-SIM-FIG. 7.2B is a histogram of the charge loss ratio percentages for capacitor C5 of the circuit of DEMAW-SIM-FIG. 1.2.

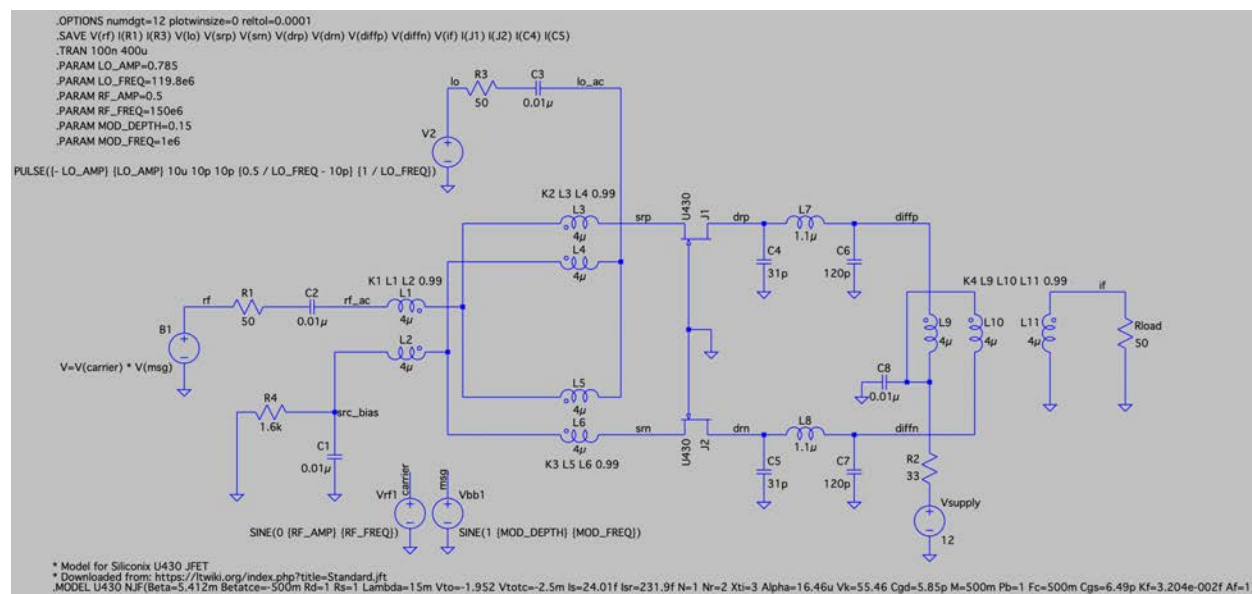


DEMAW-SIM-FIG. 7.2B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.2).

B. Simulation Results For an Input Signal Reduced by 6 dB

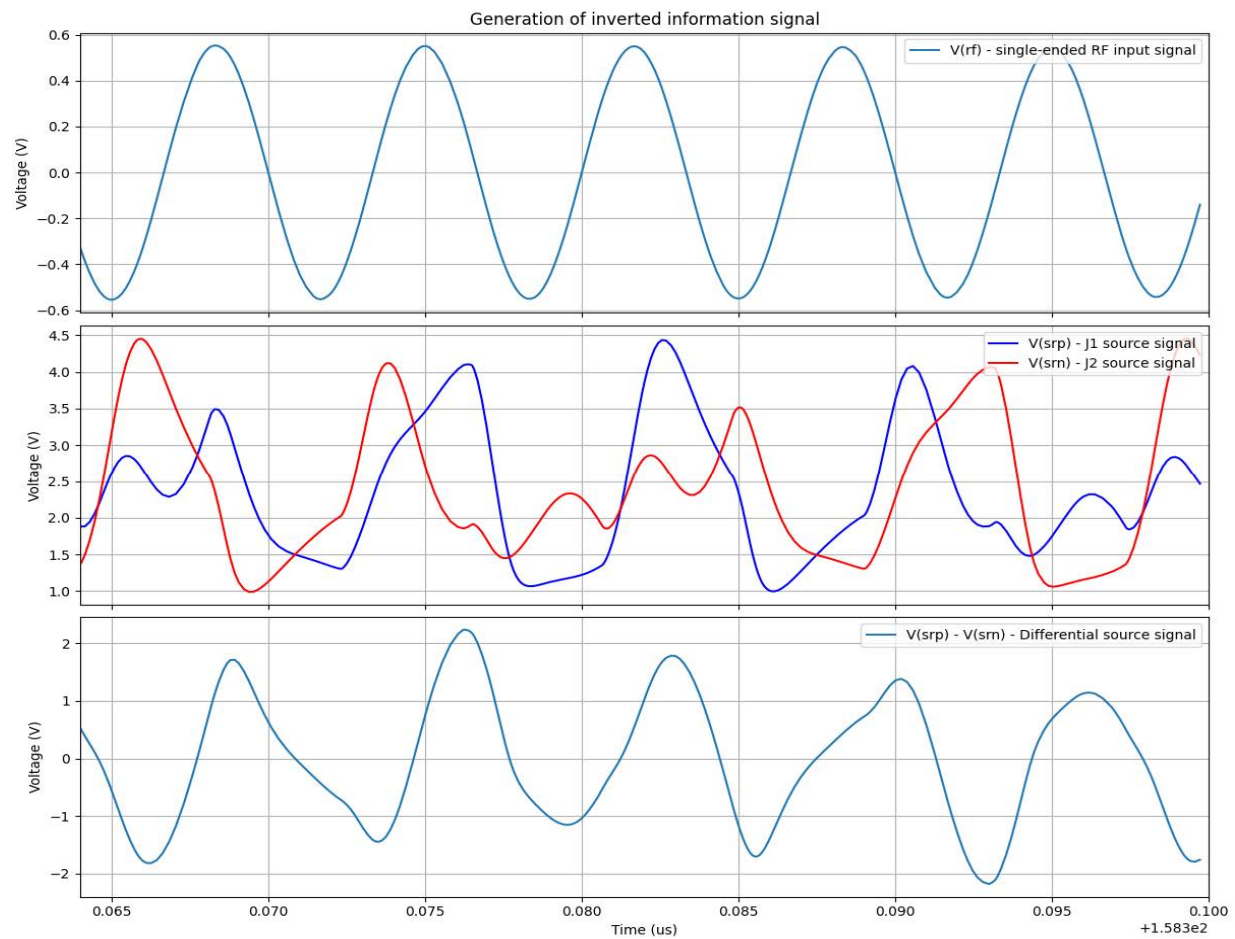
26. DEMAW-SIM-FIG. 1.3 is a schematic representation of the DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 6 dB. I have created additional figures DEMAW-SIM-FIGS. 4.3, 5.3, 6.3, 7.3A and 7.3B based on simulation output from DEMAW-SIM-FIG. 1.3. DEMAW-SIM-FIGS. 4.3, 5.3, 6.3, 7.3A and 7.3B show the same simulation output

from DEMA-SIM-FIG. 1.3 as DEMA-SIM-FIGS. 4, 5, 6, and 7 show from DEMA-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMA-SIM-FIGS. 1, 4, 5, 6, and 7 are likewise supported by DEMA-SIM-FIGS. 1.3, 4.3, 5.3, 6.3, 7.3A and 7.3B.



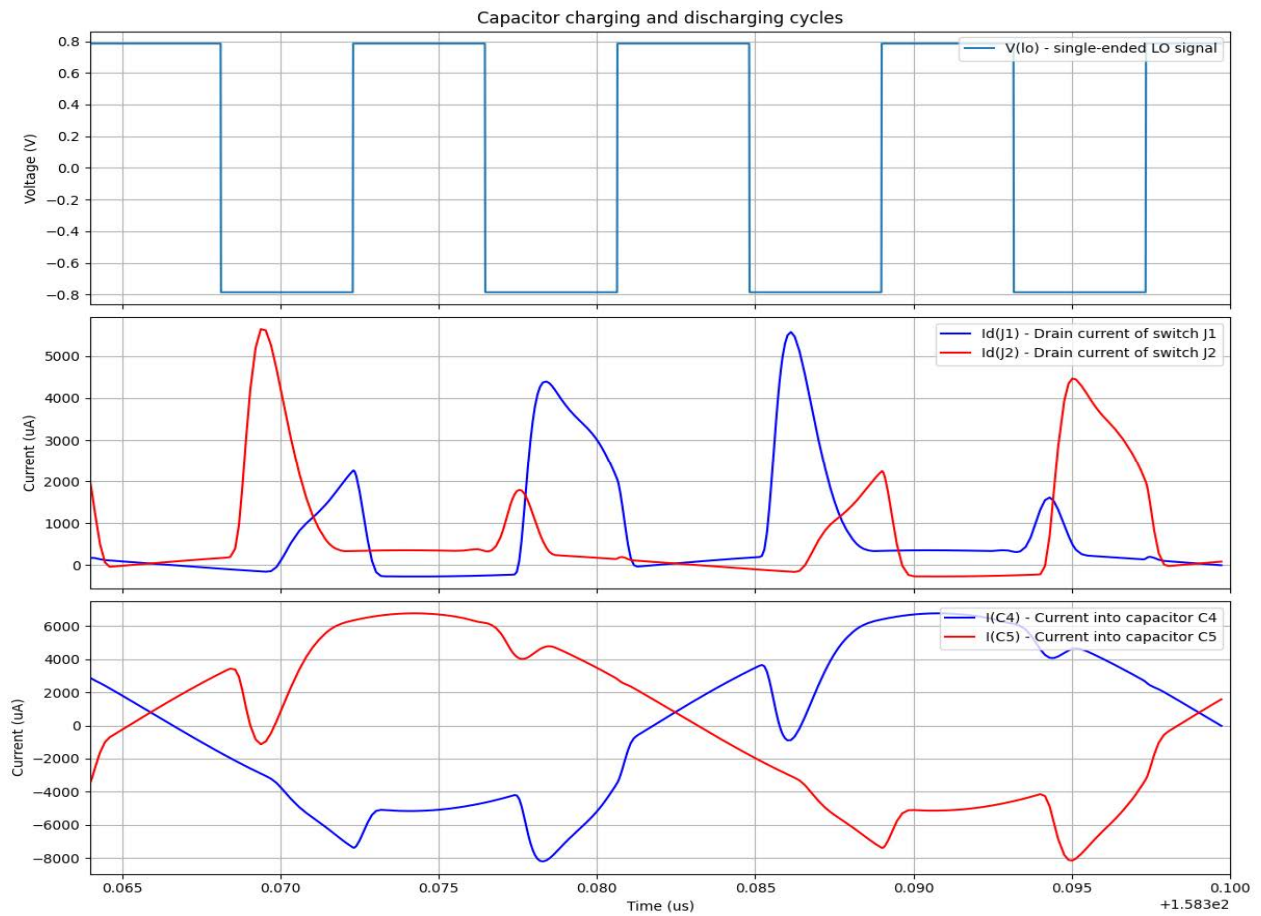
DEMA-SIM-FIG. 1.3. DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 6 dB.

27. DEMA-SIM-FIG. 4.3 is a graphical representation of the generation of the information signal and the inverted information signal in the circuit of DEMA-SIM-FIG. 1.3.



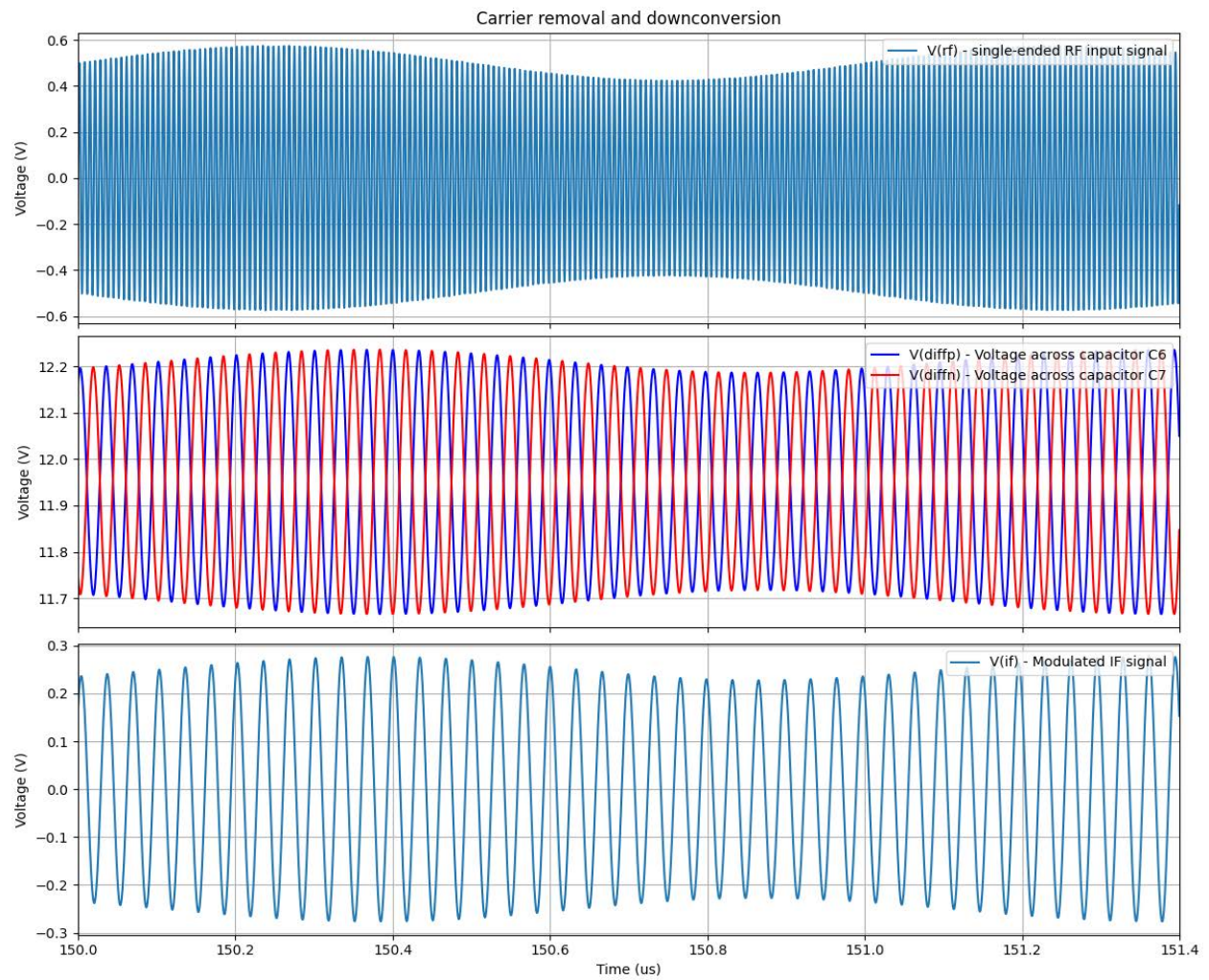
DEMAW-SIM-FIG. 4.3. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.3).

28. DEMAW-SIM-FIG. 5.3 is a graphical representation showing the charging and discharging cycles of the capacitors C4 and C5 in circuit of DEMAW-SIM-FIG. 1.3.



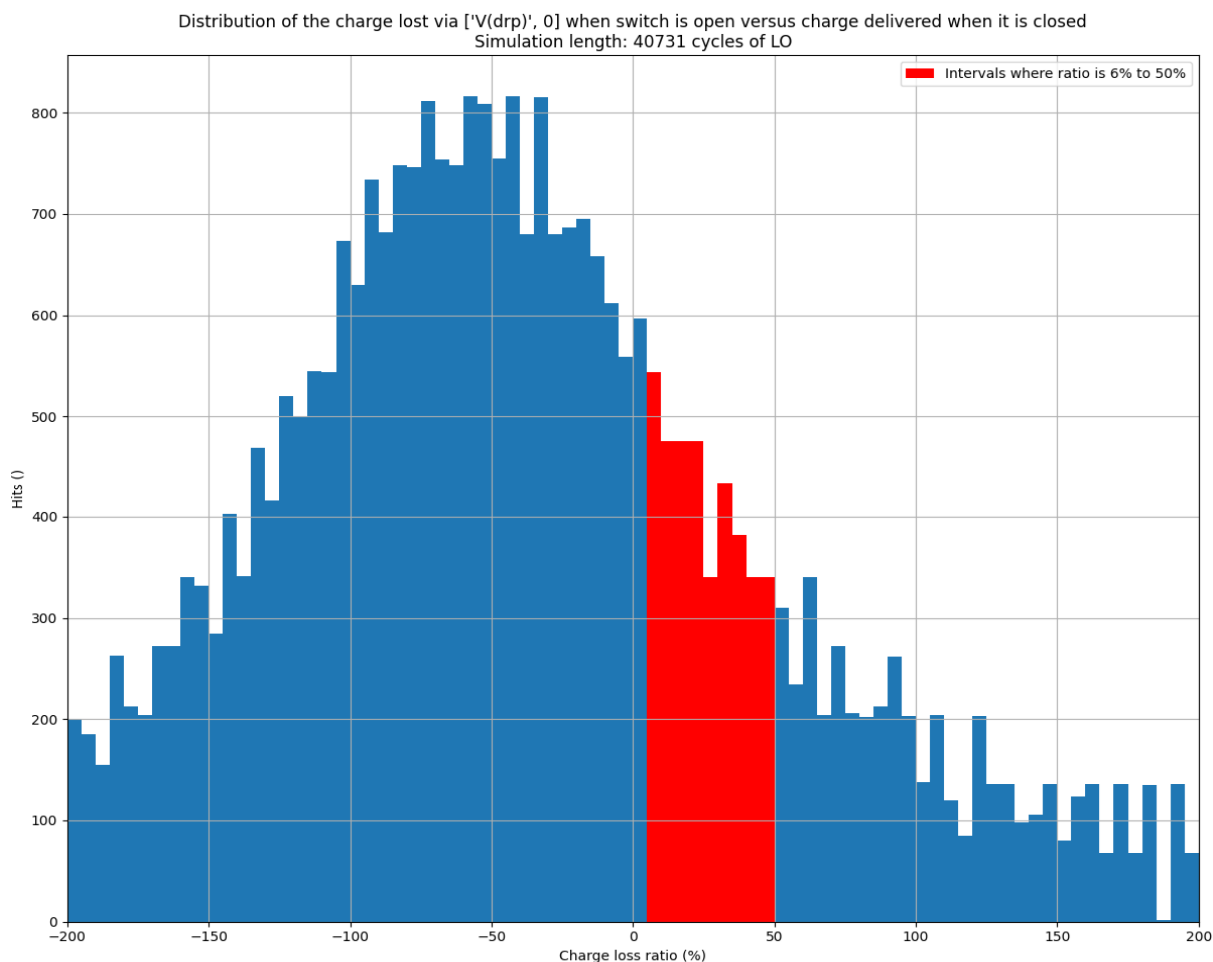
DEMAW-SIM-FIG. 5.3. Charging and discharging cycles of capacitors C4 and C5 (circuit of DEMAW-SIM-FIG. 1.3).

29. DEMAW-SIM-FIG. 6.3 is a graphical representation of the carrier removal and down-conversion of the circuit of DEMAW-SIM-FIG. 1.3.



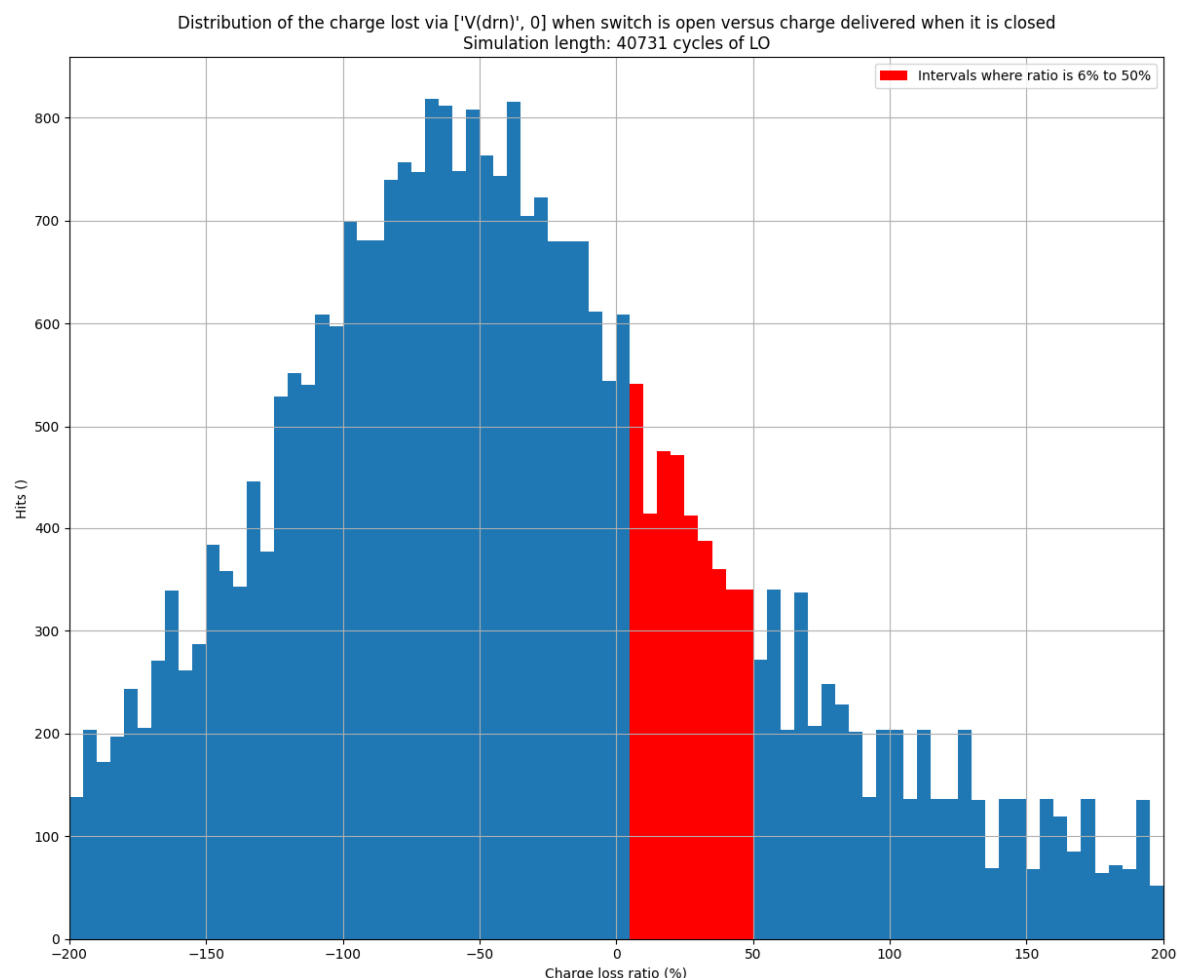
DEMAW-SIM-FIG. 6.3. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.3).

30. DEMAW-SIM-FIG. 7.3A is a histogram of the charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.3.



DEMAW-SIM-FIG. 7.3A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.3).

31. DEMAW-SIM-FIG. 7.3B is a histogram showing the charge loss ratio percentages for capacitor C5 of the circuit of DEMAW-SIM-FIG. 1.3.

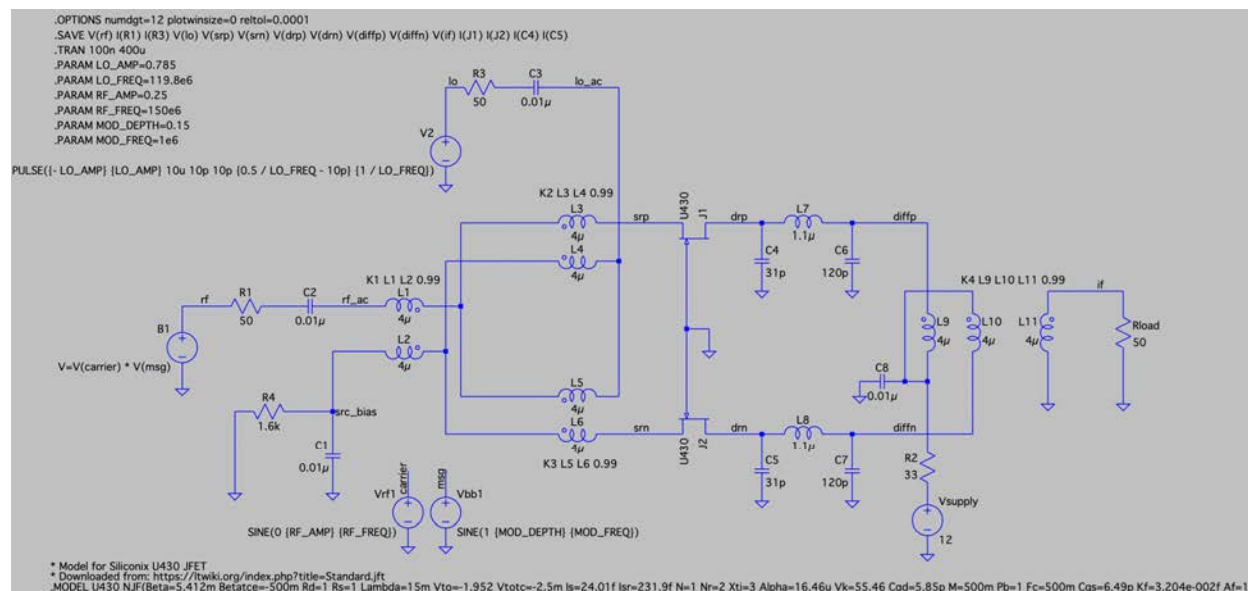


DEMAW-SIM-FIG. 7.3B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.3).

C. Simulation Results For an Input Signal Reduced by 12 dB

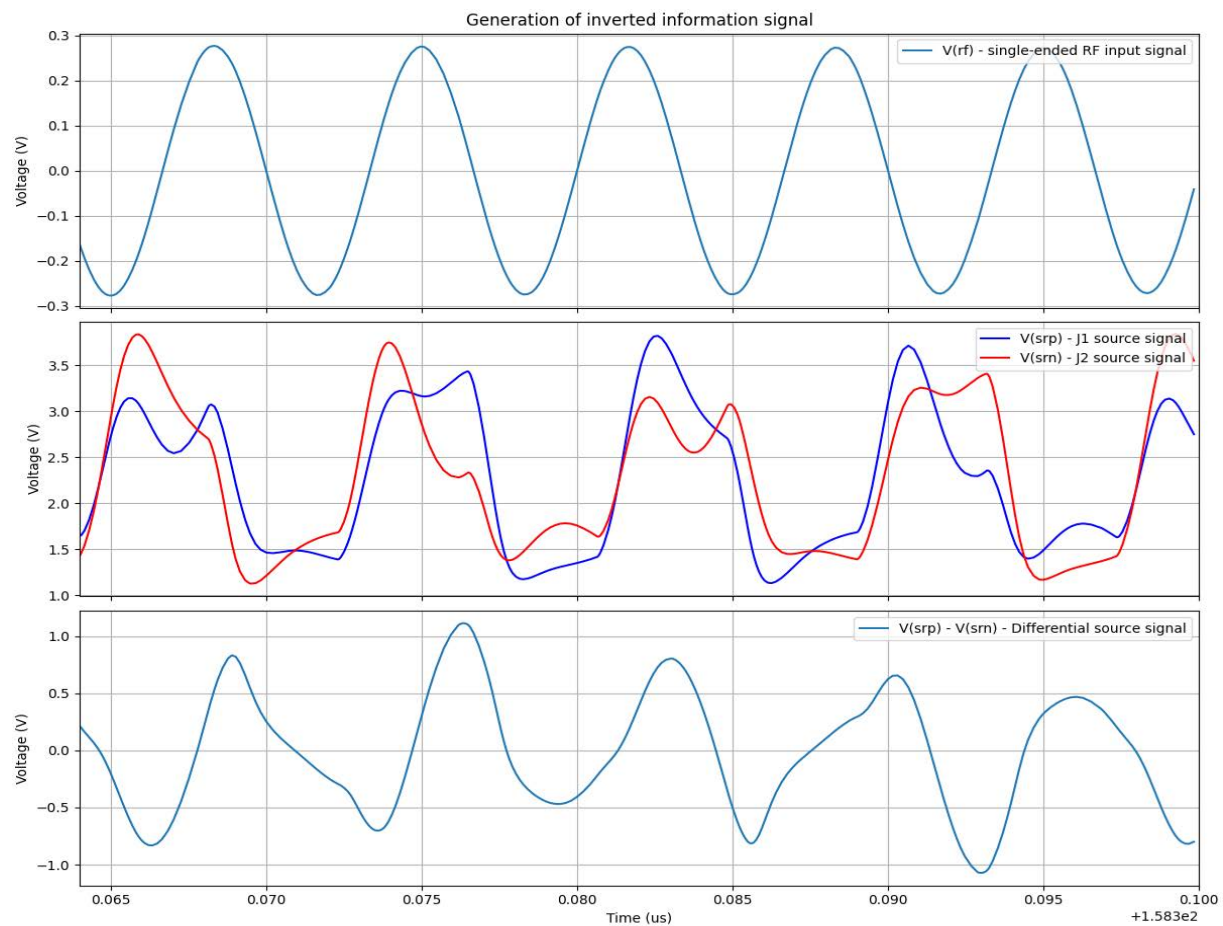
32. DEMAW-SIM-FIG. 1.4 is a schematic representation of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 12 dB. I have created additional figures DEMAW-SIM-FIGS. 4.4, 5.4, 6.4, 7.4A and 7.4B based on simulation output from DEMAW-SIM-FIG. 1.4. DEMAW-SIM-FIGS. 4.4, 5.4, 6.4, 7.4A and 7.4B show the same simulation output from DEMAW-SIM-FIG. 1.4 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from

DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIGS. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.4, 4.4, 5.4, 6.4, 7.4A and 7.4B.



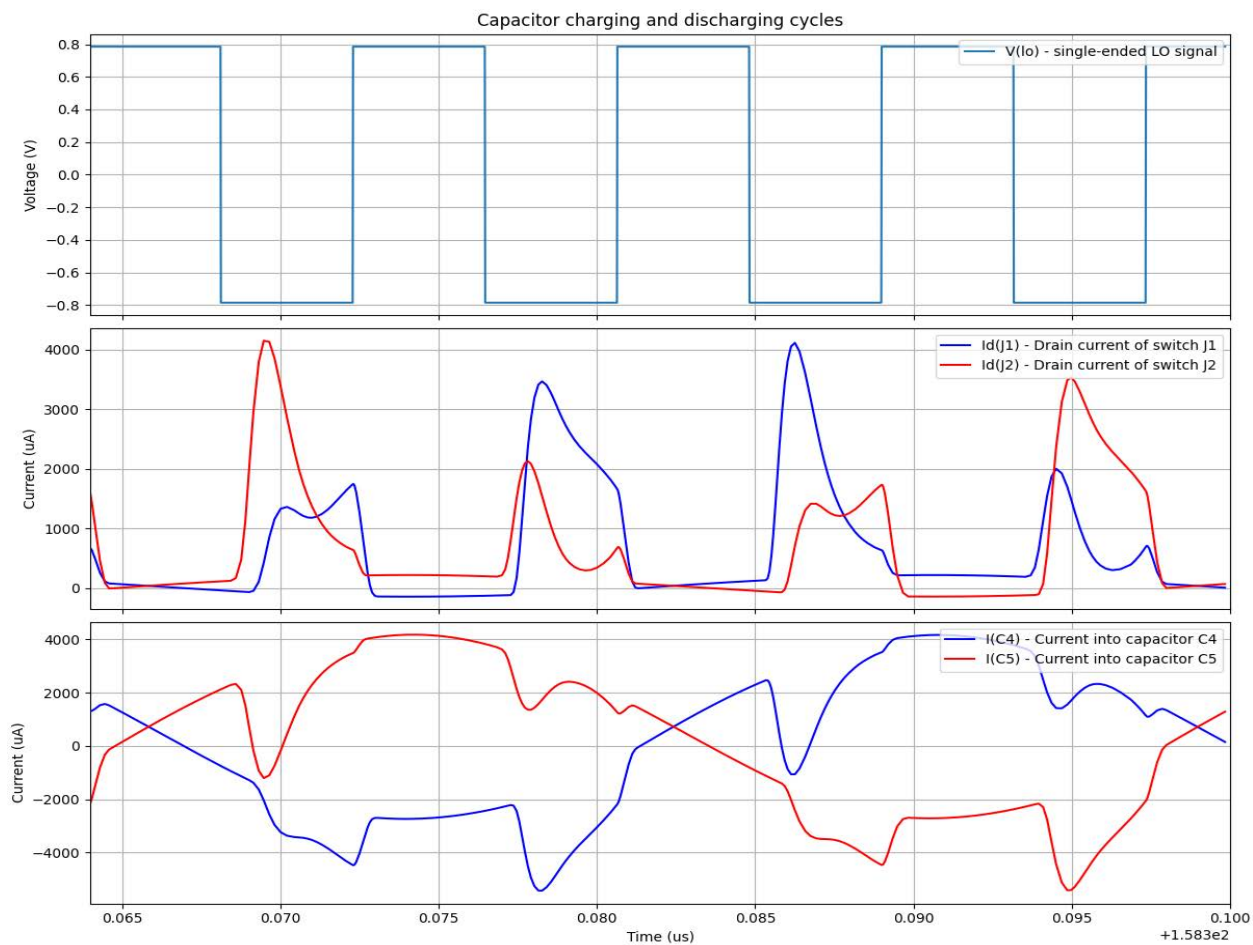
DEMAW-SIM-FIG. 1.4. Simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 12 dB.

33. DEMAW-SIM-FIG. 4.4 is a graphical representation of the generation of inverted information signal of the circuit of DEMAW-SIM-FIG. 1.4.



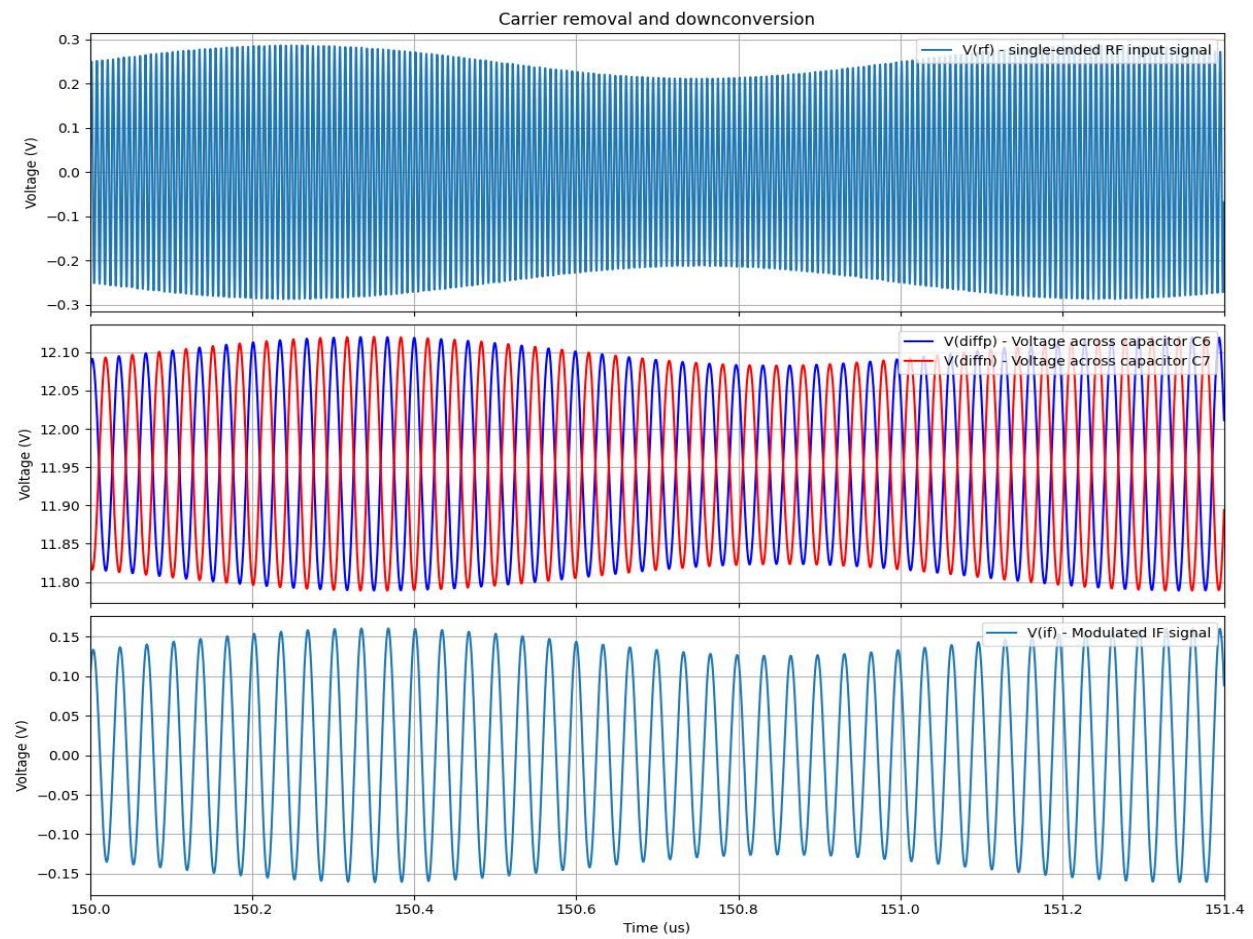
DEMAW-SIM-FIG. 4.4. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.4).

34. DEMAW-SIM-FIG. 5.4 is a graphical representation of the charging and discharging cycles of capacitors C4 and C5 of the circuit of DEMAW-SIM-FIG. 1.4.



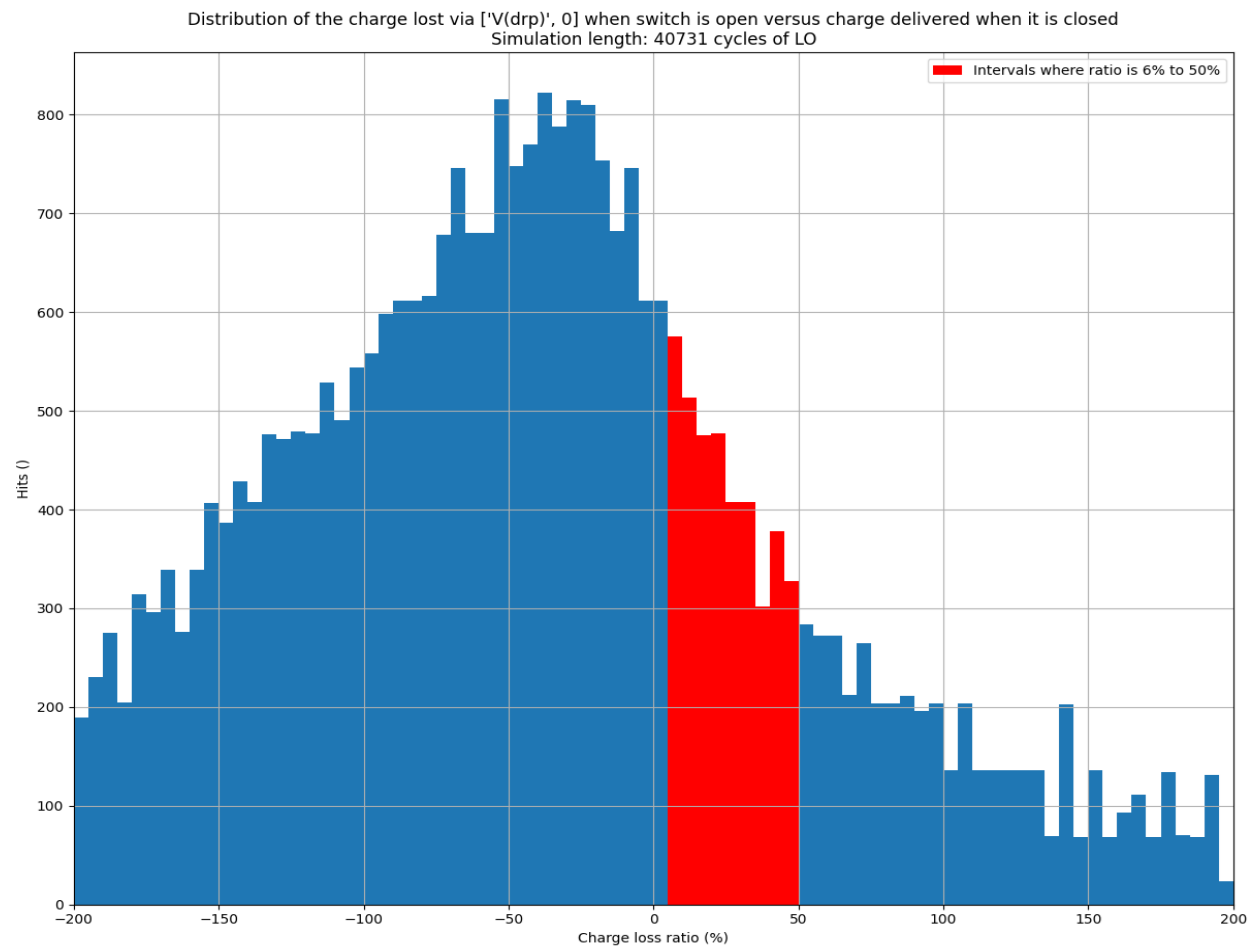
DEMAW-SIM-FIG. 5.4. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.4).

35. DEMAW-SIM-FIG. 6.4 is a graphical representation showing the carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.4.



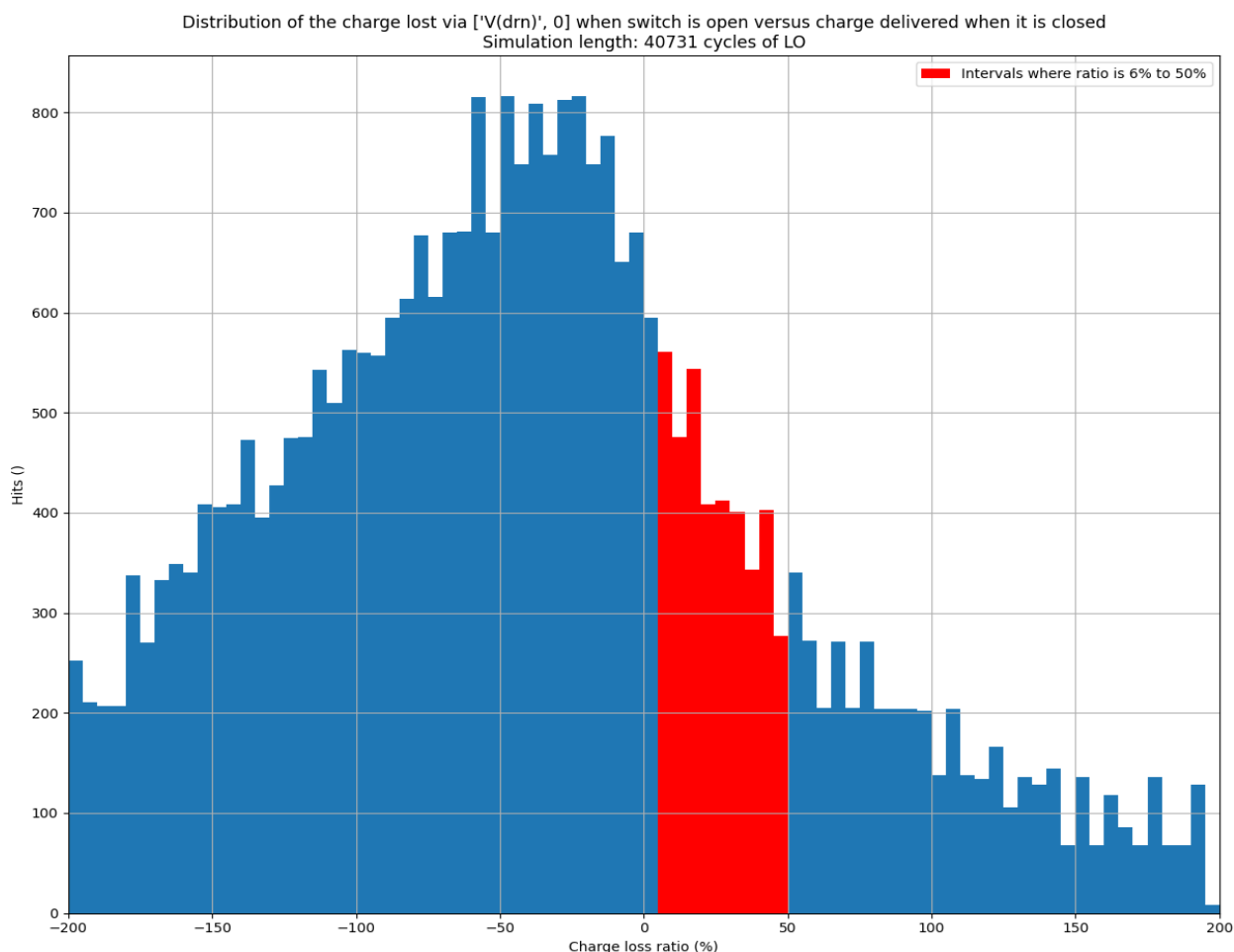
DEMAW-SIM-FIG. 6.4. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.4).

36. DEMAW-SIM-FIG. 7.4A is a histogram of the charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.4.



DEMAW-SIM-FIG. 7.4A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.4).

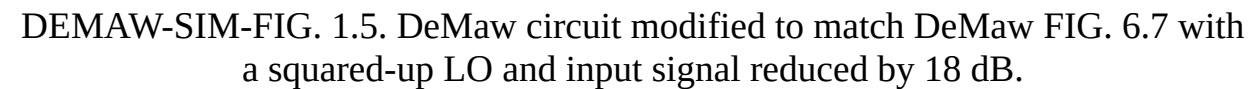
37. DEMAW-SIM-FIG. 7.4B is a histogram of the charge loss ratio percentages for capacitor C5 of the circuit of DEMAW-SIM-FIG. 1.4.



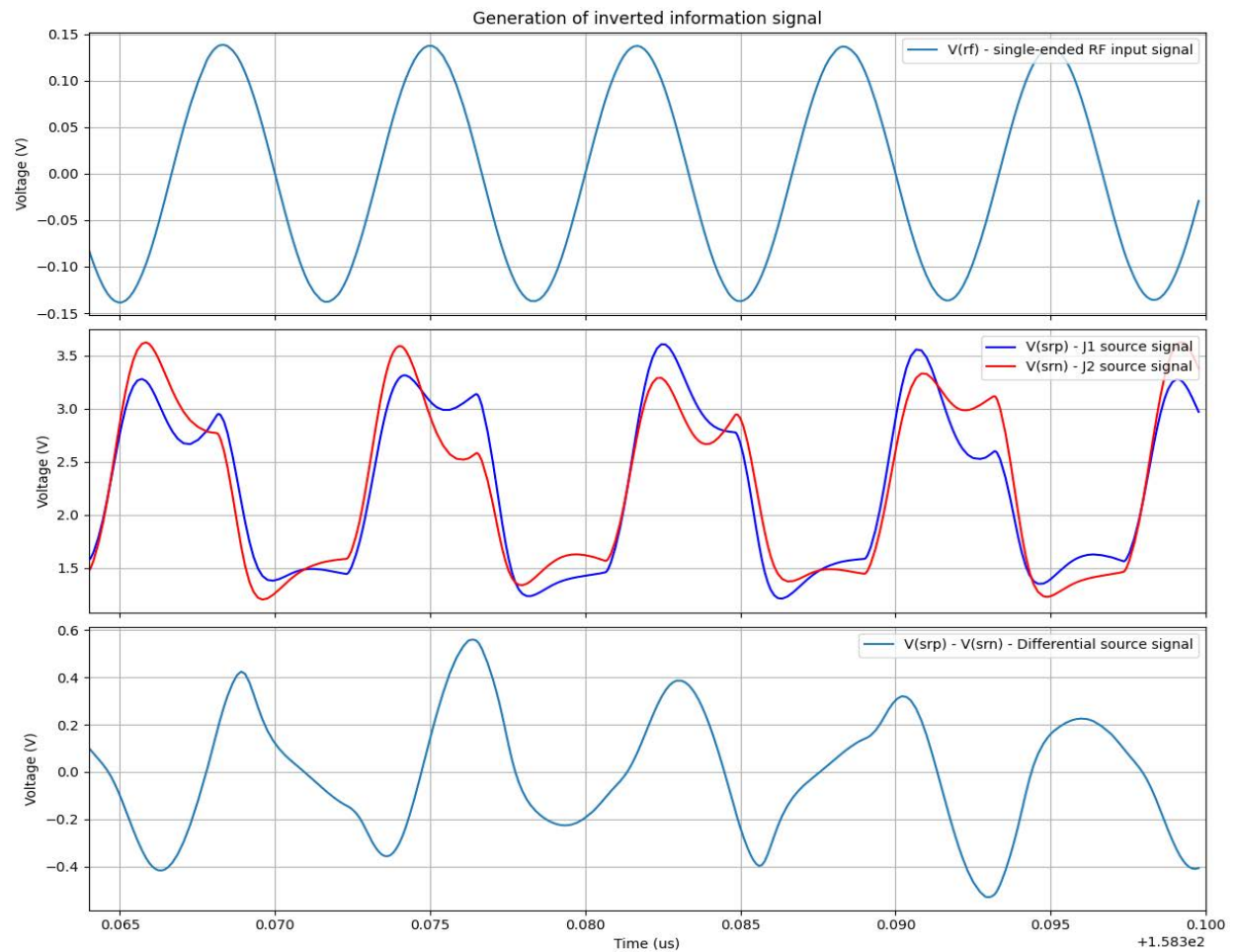
DEMAW-SIM-FIG. 7.4B. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.4).

D. Simulation Results For an Input Signal Reduced by 18 dB

38. DEMAW-SIM-FIG. 1.5 is a schematic diagram of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 18 dB. I have created additional figures DEMAW-SIM-FIGS. 4.5, 5.5, 6.5, 7.5A and 7.5B based on simulation output from DEMAW-SIM-FIG. 1.5. DEMAW-SIM-FIGS. 4.5, 5.5, 6.5, 7.5A and 7.5B show the same simulation output from DEMAW-SIM-FIG. 1.5 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from

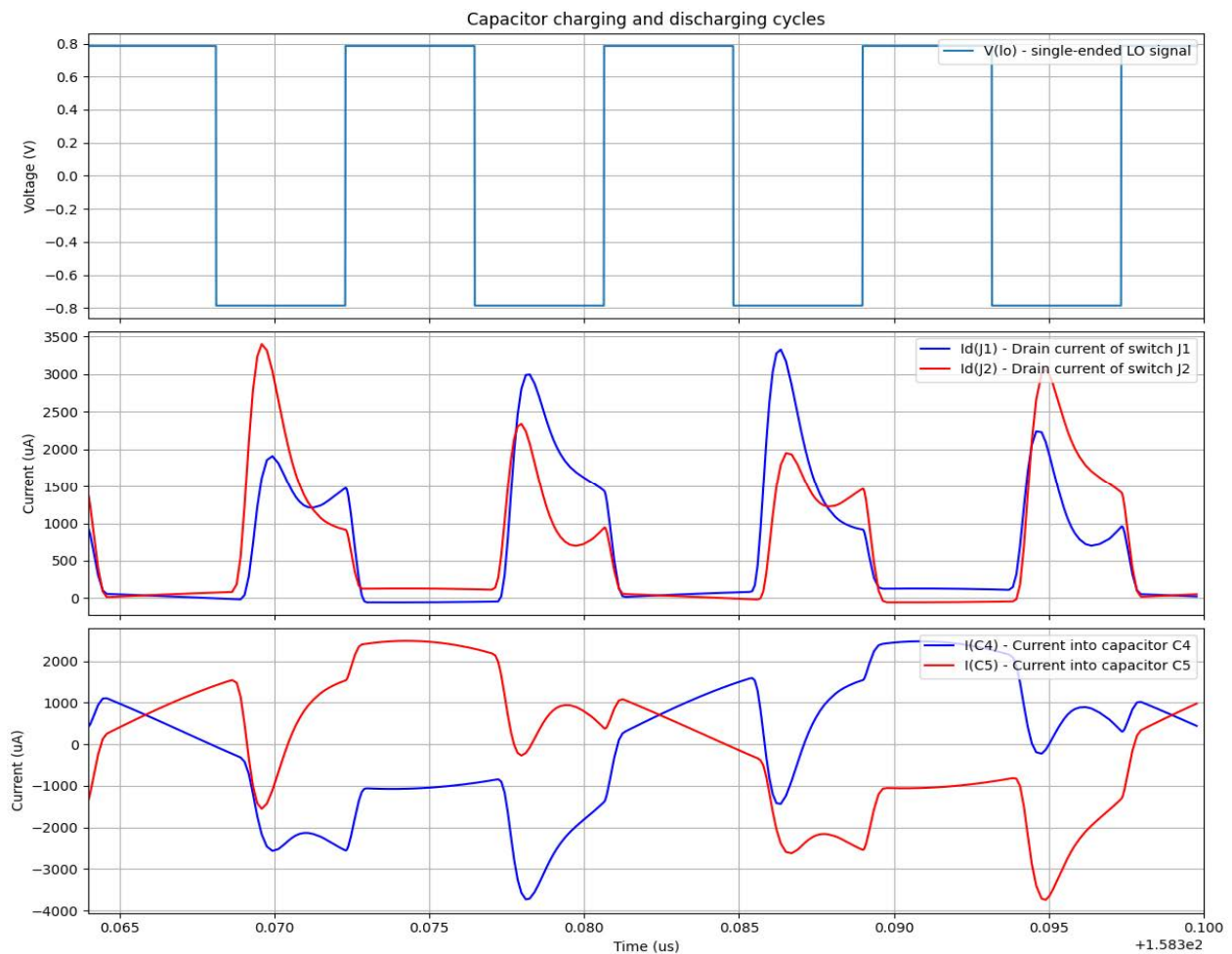


39



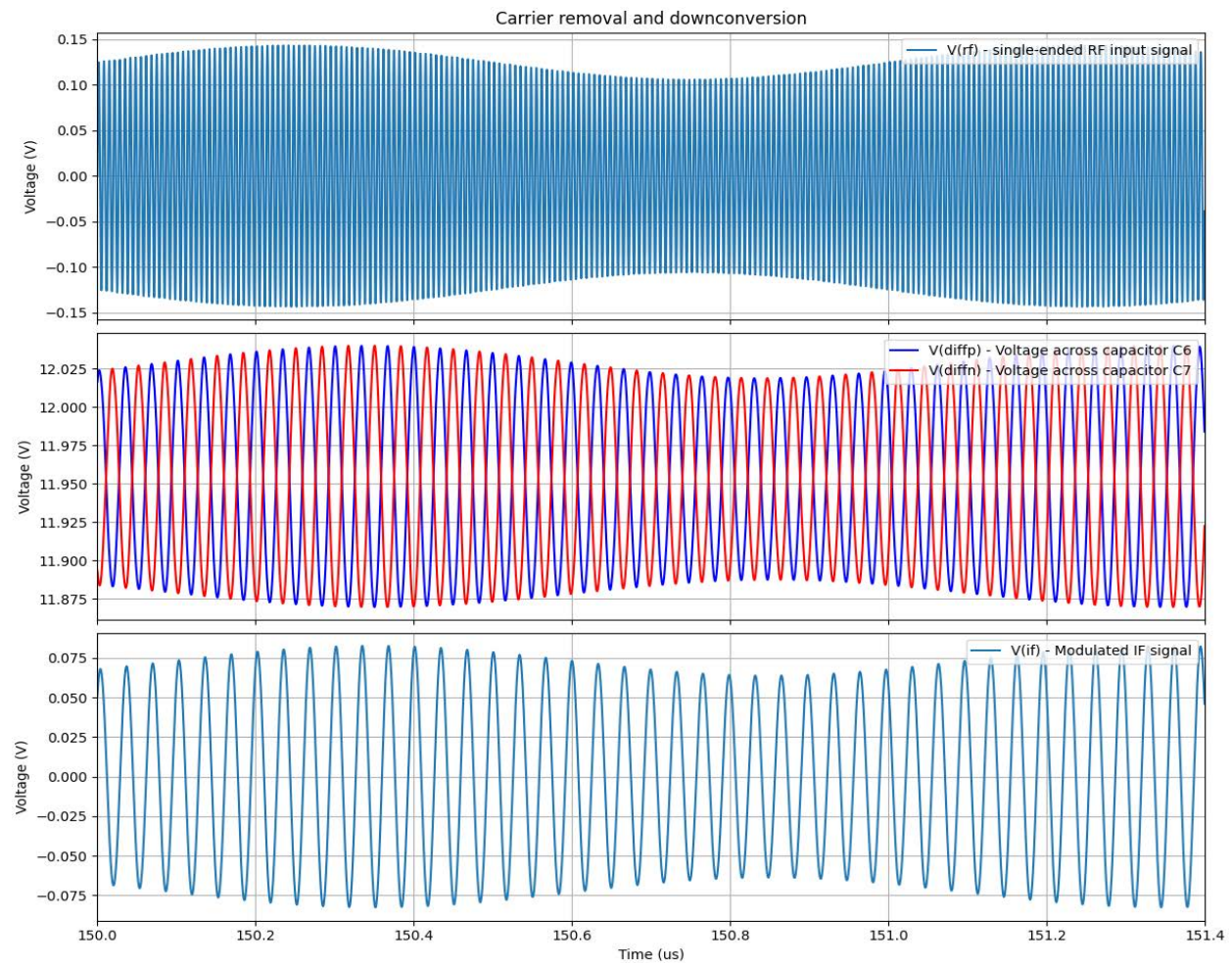
DEMAW-SIM-FIG. 4.5. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.5).

40. DEMAW-SIM-FIG. 5.5 is a graphical representation illustrating the charging and discharging cycles of the capacitors C4 and C5 of the circuit of DEMAW-SIM-FIG. 1.5.



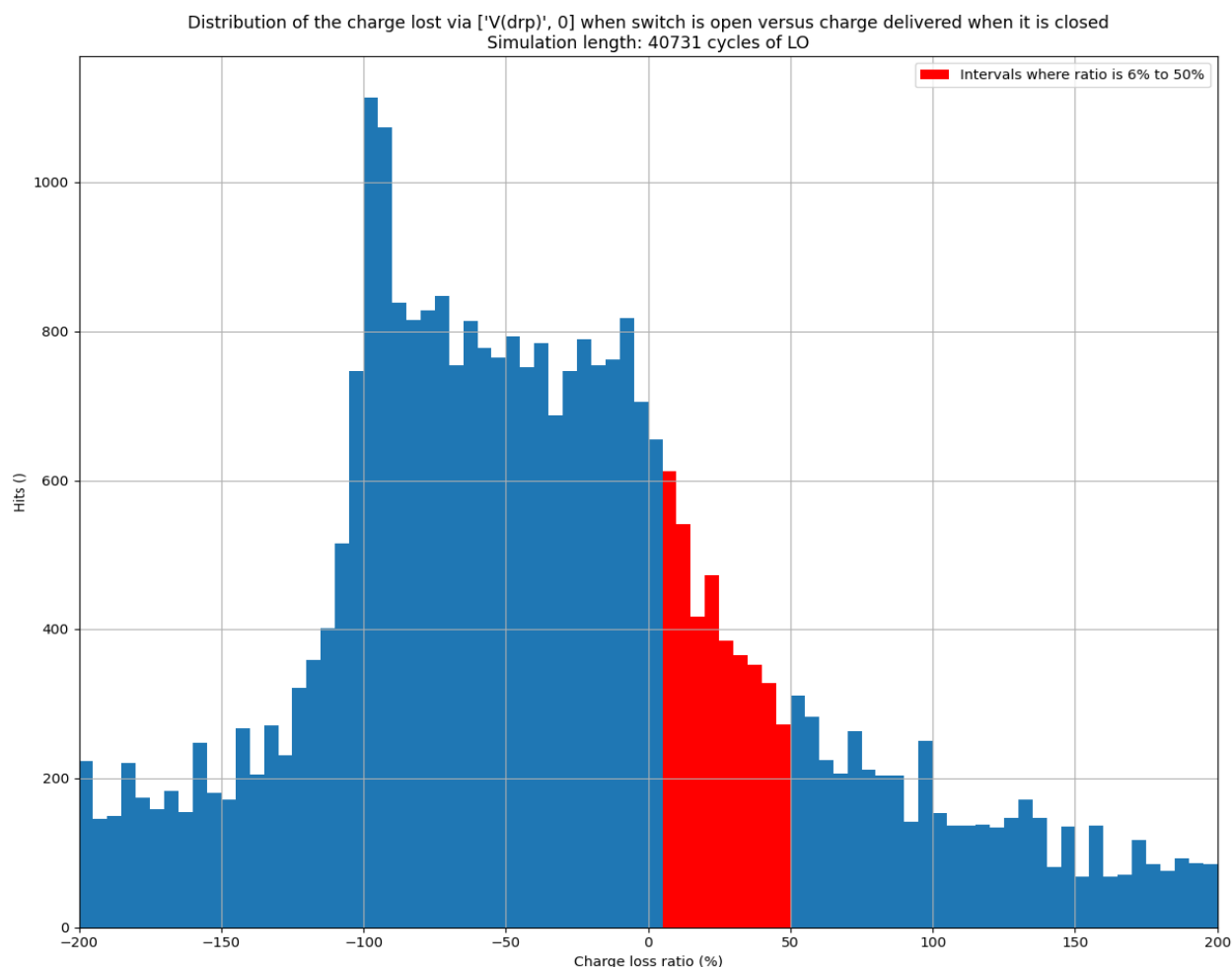
DEMAW-SIM-FIG. 5.5. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.5).

41. DEMAW-SIM-FIG. 6.5 is a schematic representation illustrating the carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.5.



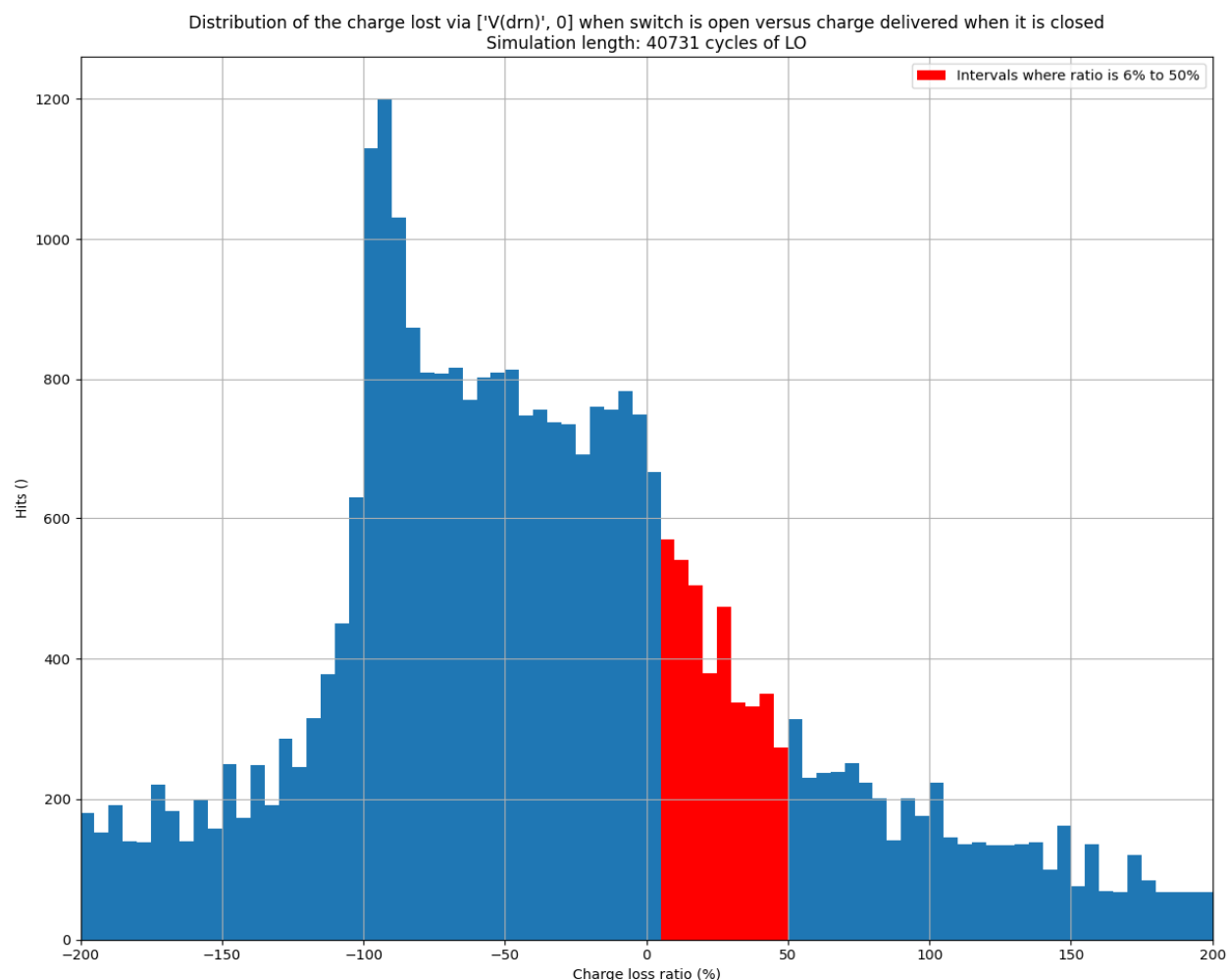
DEMAW-SIM-FIG. 6.5. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.5).

42. DEMAW-SIM-FIG. 7.5A is a histogram illustrating the charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.5.



DEMAW-SIM-FIG. 7.5A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.5).

43. DEMAW-SIM-FIG. 7.5B is a histogram showing the charge loss ratio percentages for capacitor C5 of the circuit of DEMAW-SIM-FIG. 1.5.

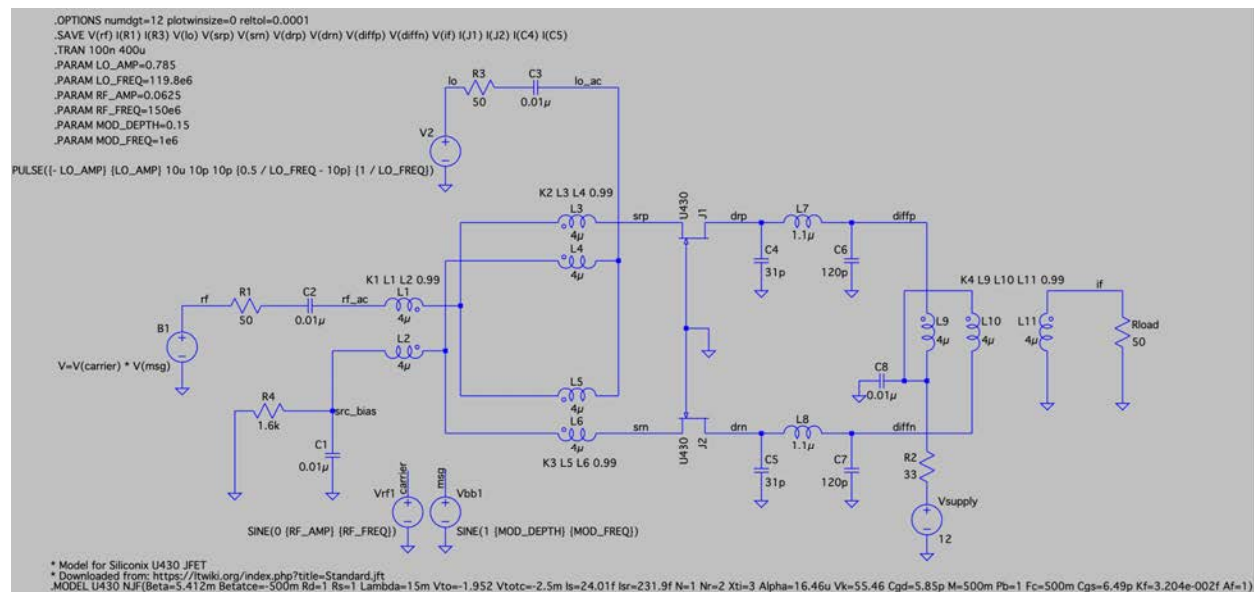


DEMAW-SIM-FIG. 7.5B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.5).

E. Simulation Results For an Input Signal Reduced by 24 dB

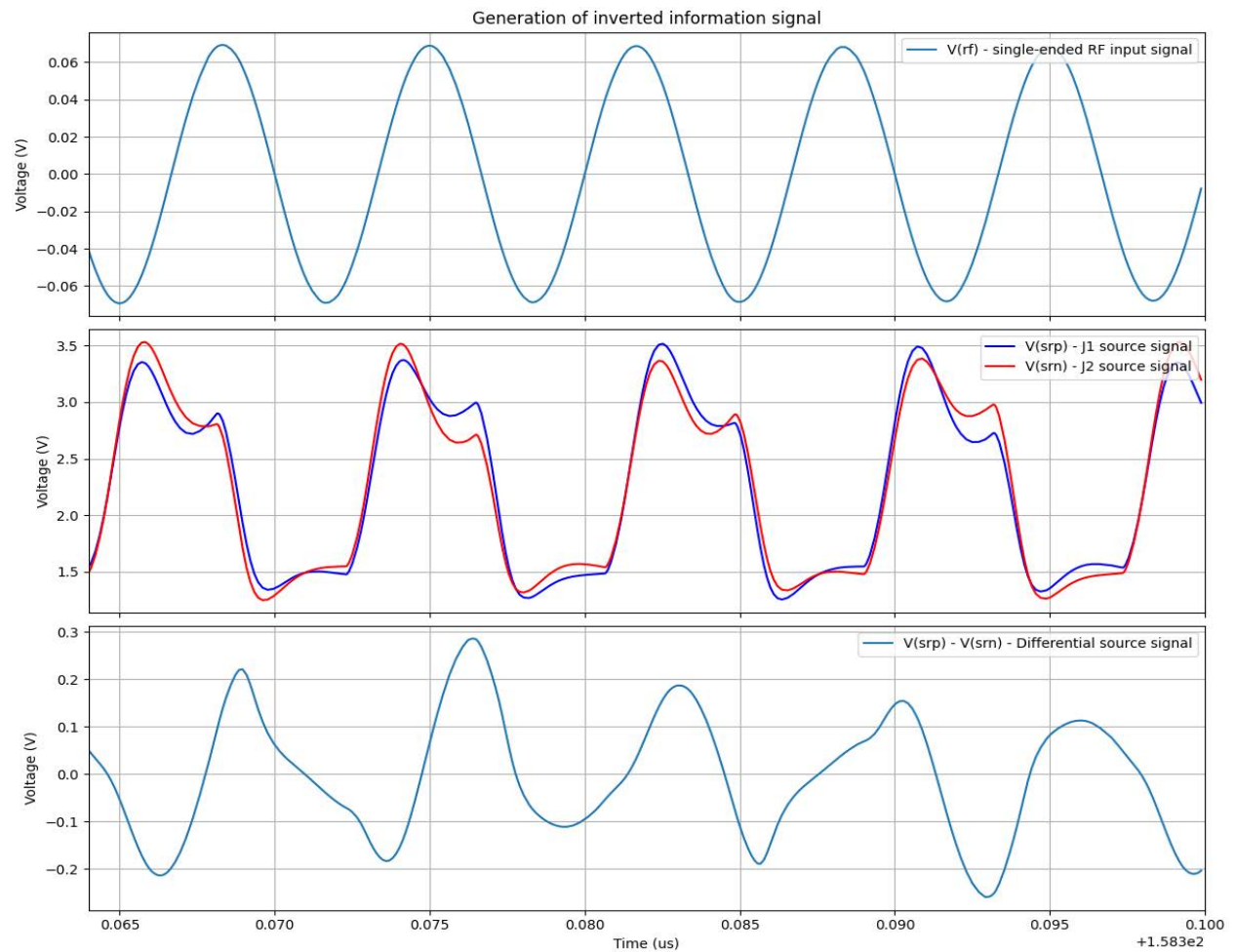
44. DEMAW-SIM-FIG. 1.6 is a schematic representation of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 24 dB. I have created additional figures DEMAW-SIM-FIGS. 4.6, 5.6, 6.6, 7.6A and 7.6B based on simulation output from DEMAW-SIM-FIG. 1.6. DEMAW-SIM-FIGS. 4.6, 5.6, 6.6, 7.6A and 7.6B show the same simulation output

from DEMA-SIM-FIG. 1.6 as DEMA-SIM-FIGS. 4, 5, 6, and 7 show from DEMA-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMA-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMA-SIM-FIGS. 1.6, 4.6, 5.6, 6.6, 7.6A and 7.6B.



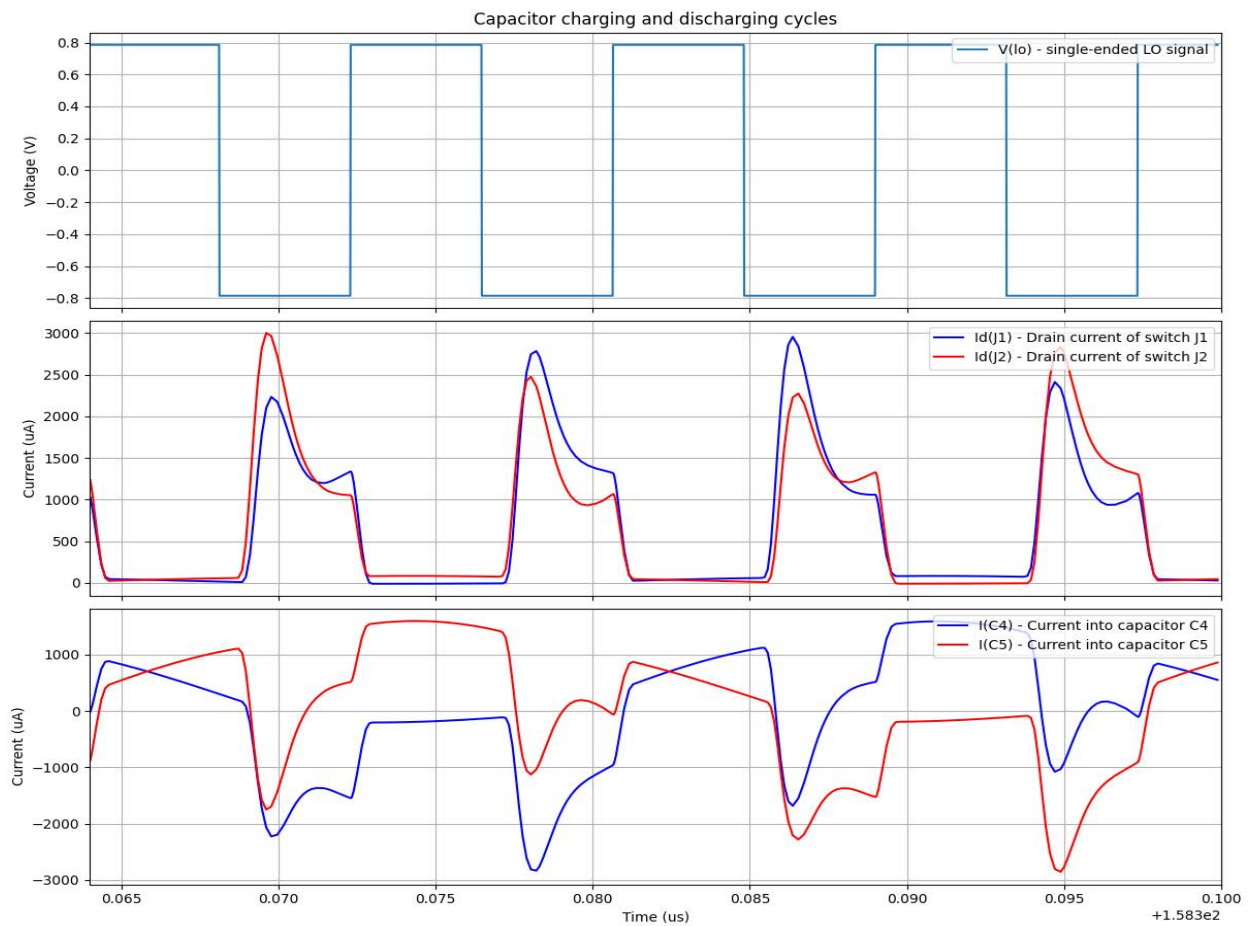
DEMA-SIM-FIG. 1.6 is a schematic representation of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a squared-up LO and input signal reduced by 24 dB.

45. DEMA-SIM-FIG. 4.6 is a graphical representation of the generation of inverted information signal in the circuit of DEMA-SIM-FIG. 1.6.



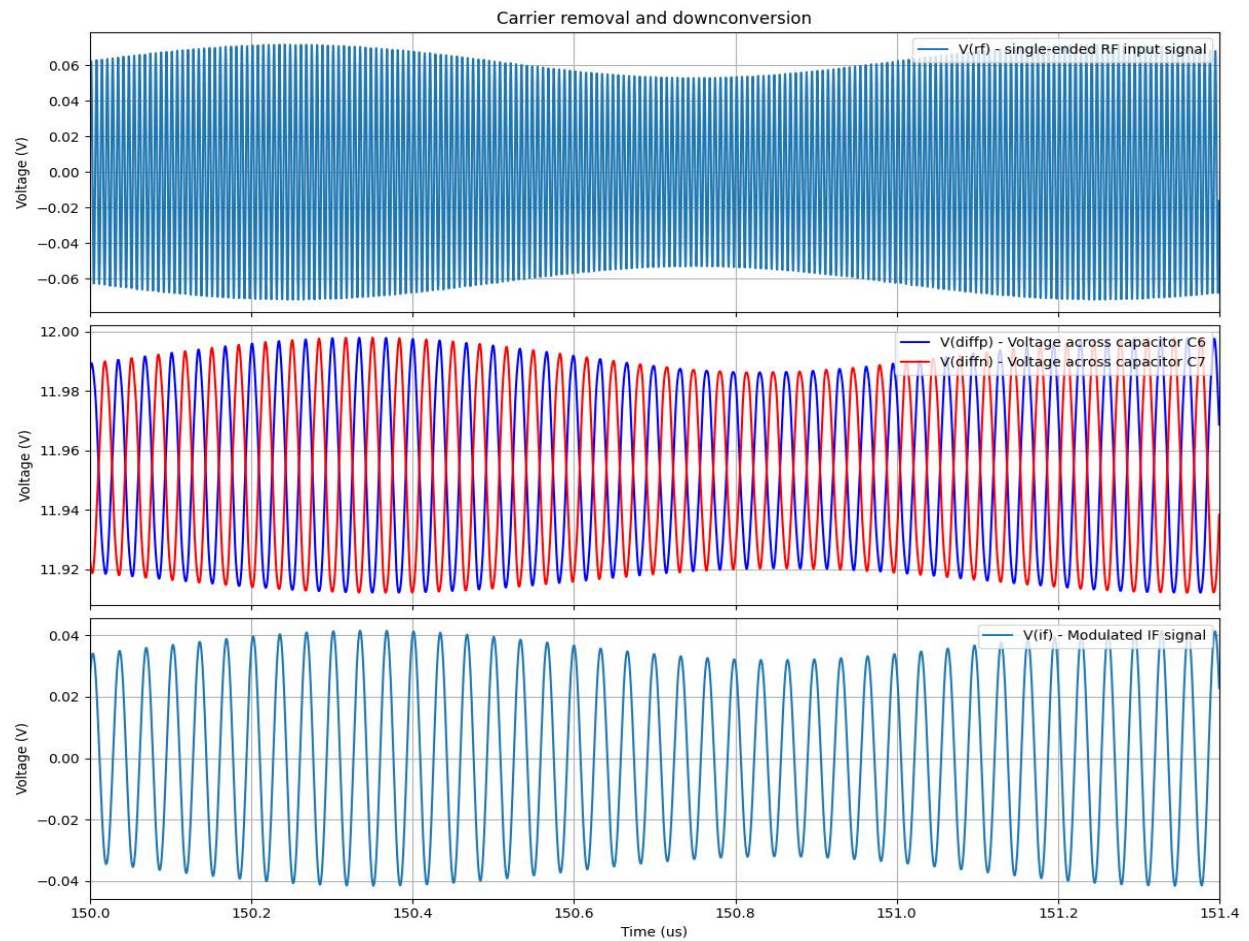
DEMAW-SIM-FIG. 4.6. Graphical representation of the generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.6).

46. DEMAW-SIM-FIG. 5.6 is a graphical representation of the charging and discharging cycles for capacitors C4 and C5 in circuit of DEMAW-SIM-FIG. 1.6.



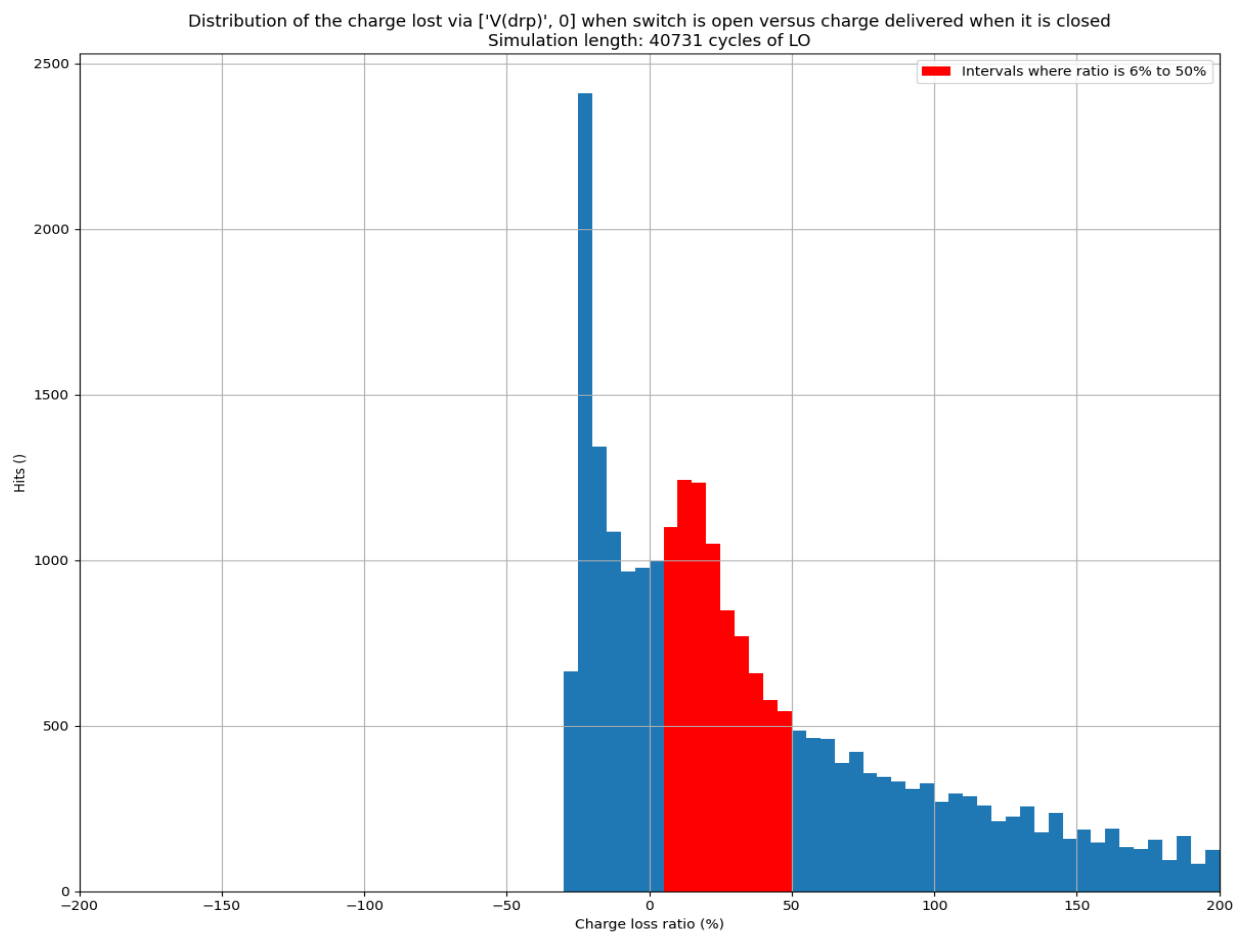
DEMAW-SIM-FIG. 5.6. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.6).

47. DEMAW-SIM-FIG.6.6 is a graphical representation of carrier removal and down-conversion for circuit of DEMAW-SIM-FIG. 1.6.



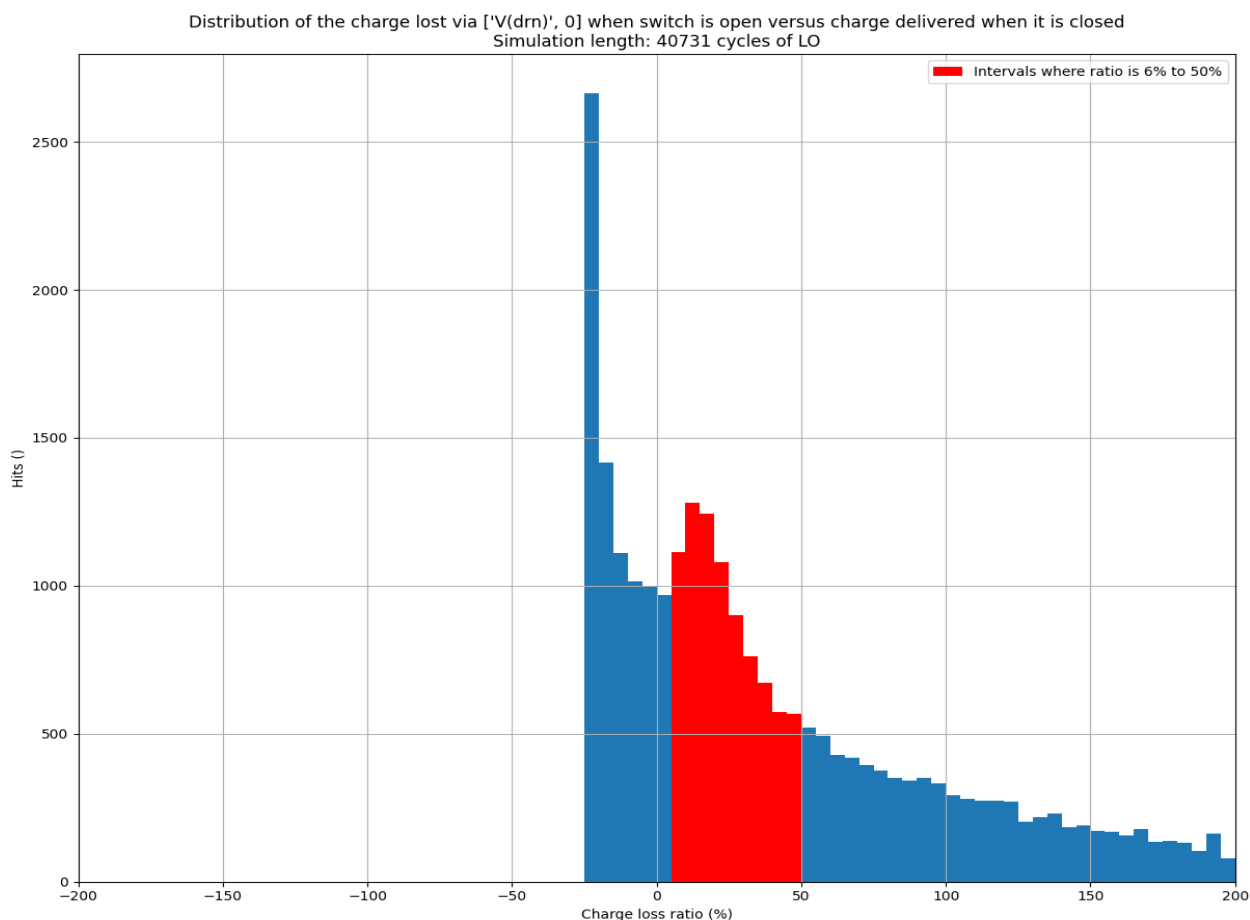
DEMAW-SIM-FIG. 6.6. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.6).

48. DEMAW-SIM-FIG. 7.6A is a histogram showing charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.6.



DEMAW-SIM-FIG. 7.6A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.6).

49. DEMAW-SIM-FIG. 7.6B is a histogram of the charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.6.



DEMAW-SIM-FIG. 7.6B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.6).

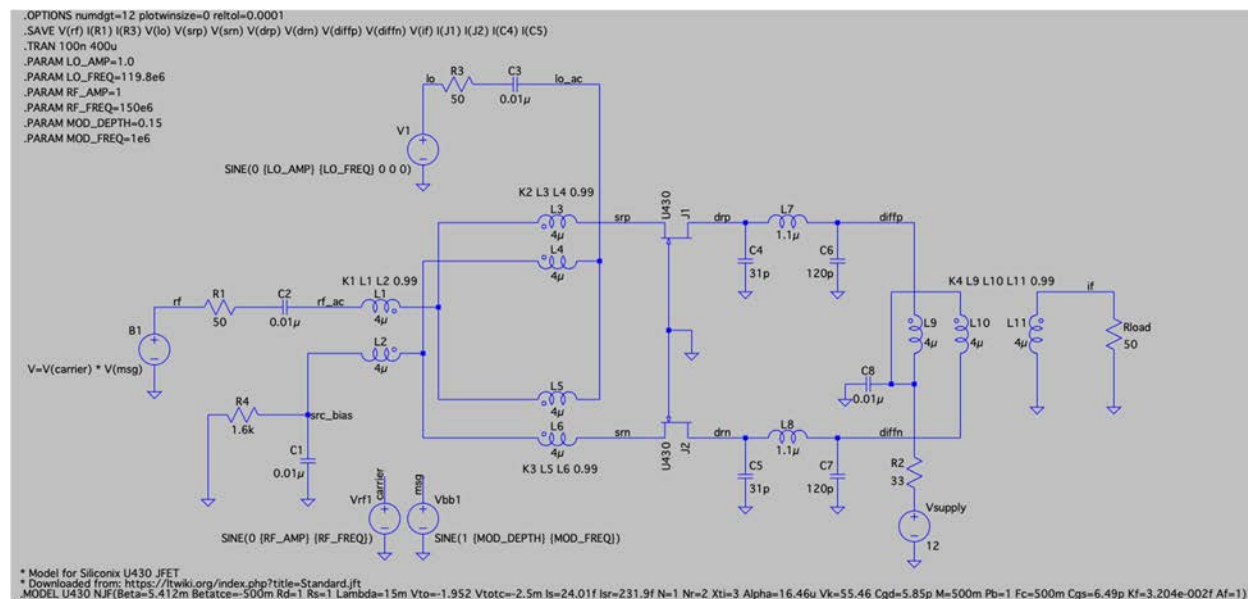
IV. DeMaw Circuit Modified to Match DeMaw FIG. 6.7 With a Sinusoidal LO

50. As I testified in my deposition, using sinusoidal LO signals in place of squared-up LO signals would not result in circuit behavior that would lead to different conclusions than those presented in my original Declaration, despite the POPR's false claims to the contrary. The simulation results presented in this section support my testimony. They correspond to the same circuit and input conditions as those for the simulation results presented in Section **Error! Reference source not**

found. except with a sinusoidal LO in place of a squared-up LO.

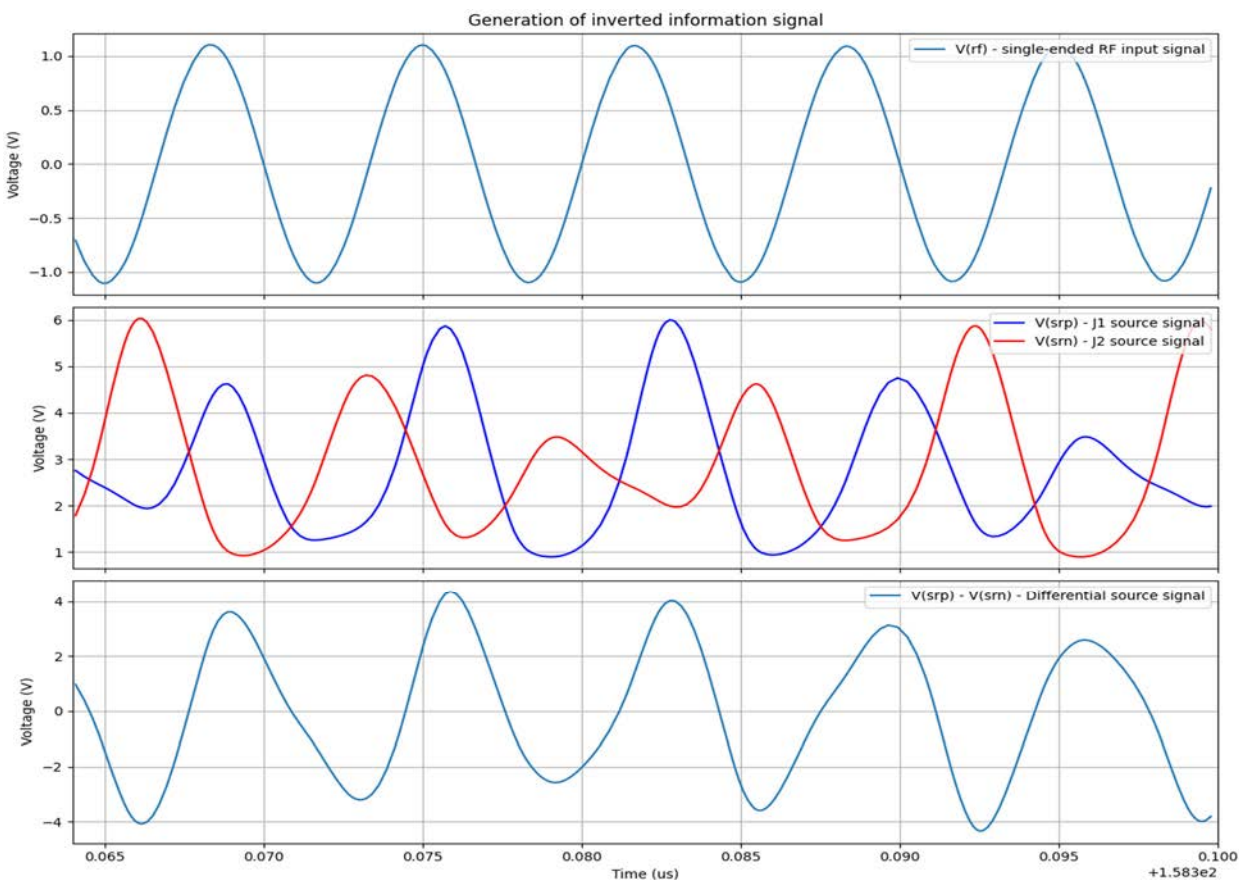
A. Simulation Results For a Large Input Signal

51. DEMAW-SIM-FIG. 1.7 is a schematic illustration of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and a large input signal. I have created additional figures DEMAW-SIM-FIGS. 4.7, 5.7, 6.7, 7.7A and 7.7B based on simulation output from DEMAW-SIM-FIG. 1.7. DEMAW-SIM-FIGS. 4.7, 5.7, 6.7, 7.7A and 7.7B show the same simulation output from DEMAW-SIM-FIG. 1.7 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.7, 4.7, 5.7, 6.7, 7.7A and 7.7B.



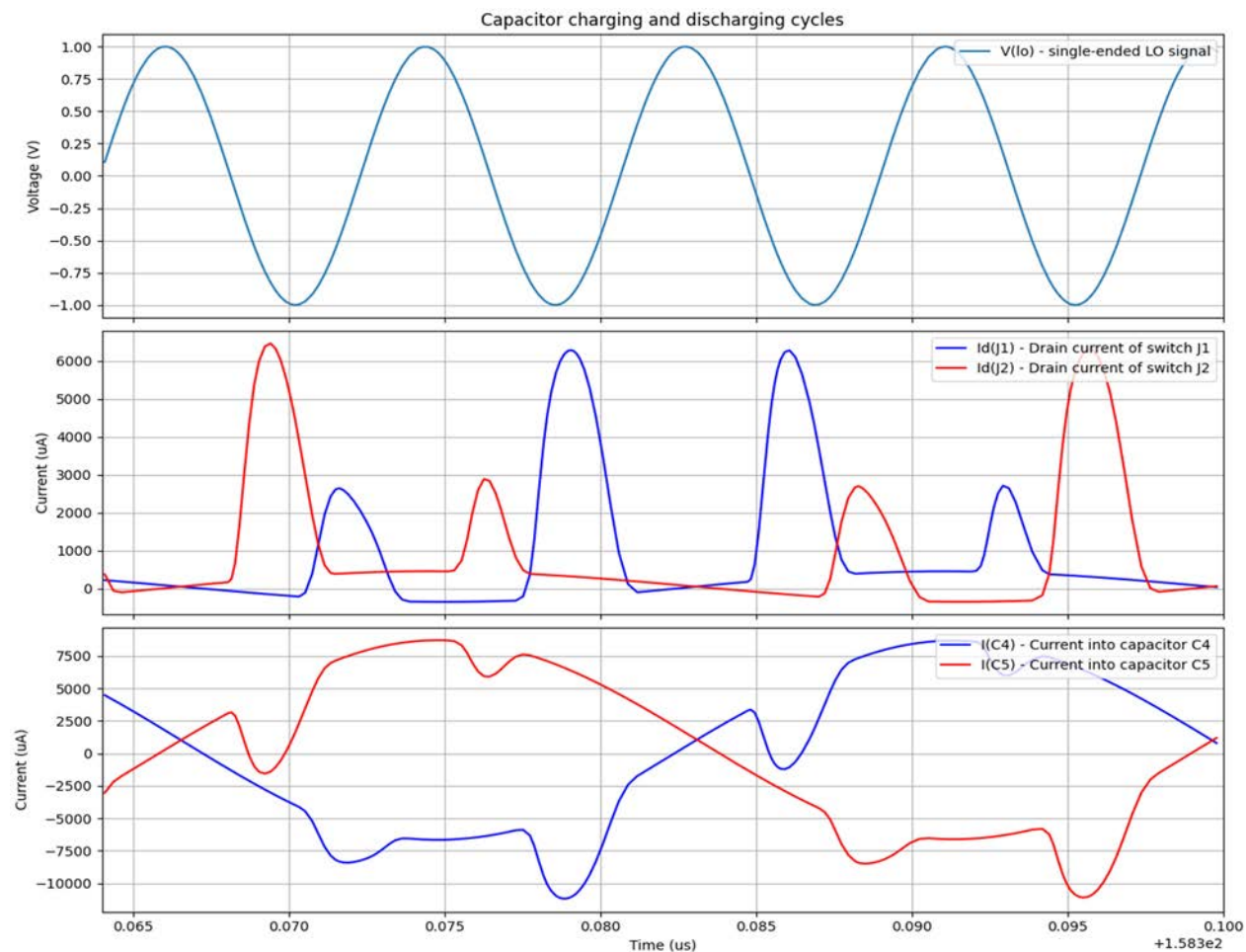
DEMAW-SIM-FIG. 1.7. DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and a large input signal.

52. DEMAW-SIM-FIG. 4.7 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.7.



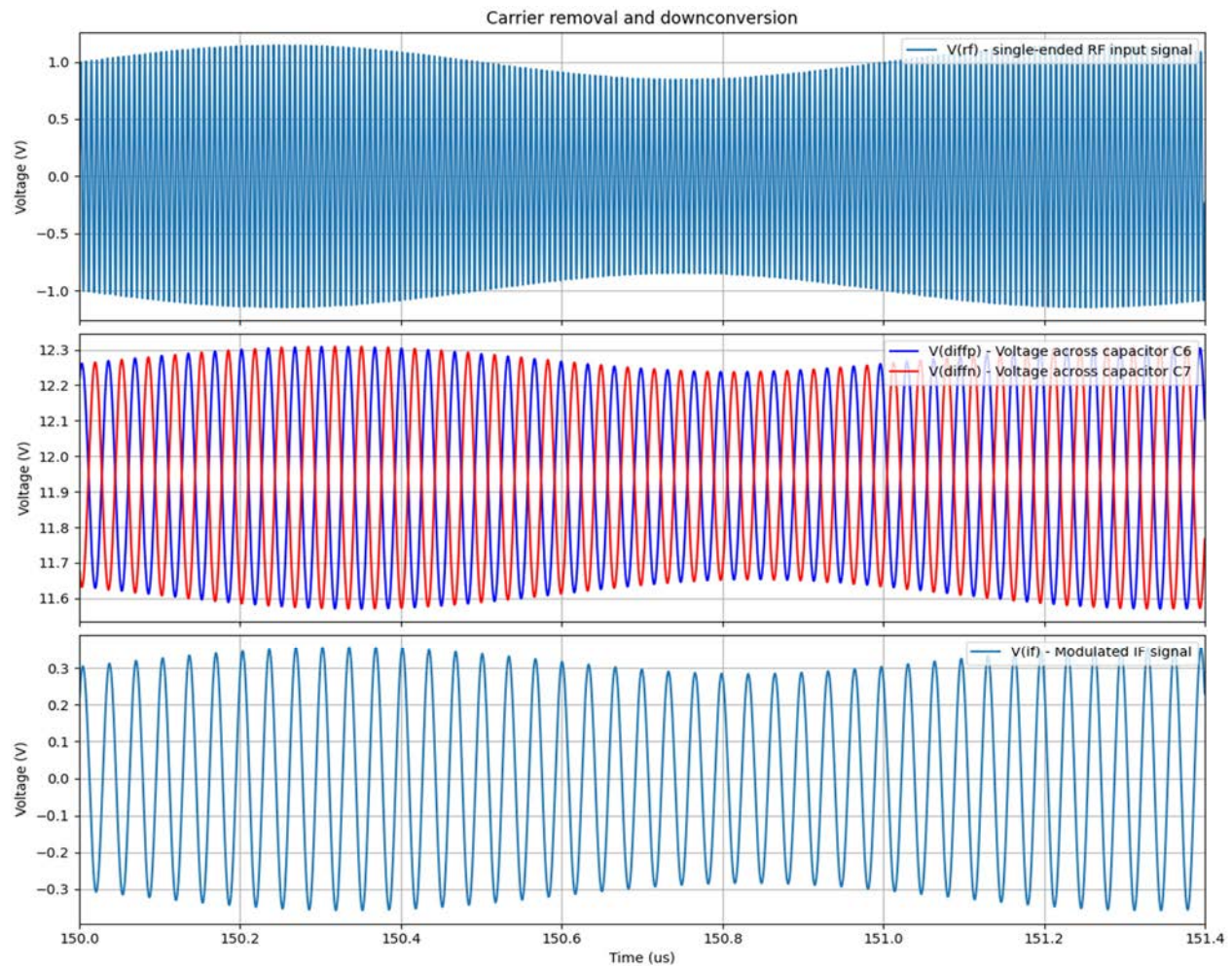
DEMAW-SIM-FIG. 4.7. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.7).

53. DEMAW-SIM-FIG. 5.7 is a graphical representation of the charging and discharging cycles of capacitors C4 and C5 for circuit of DEMAW-SIM-FIG. 1.7.



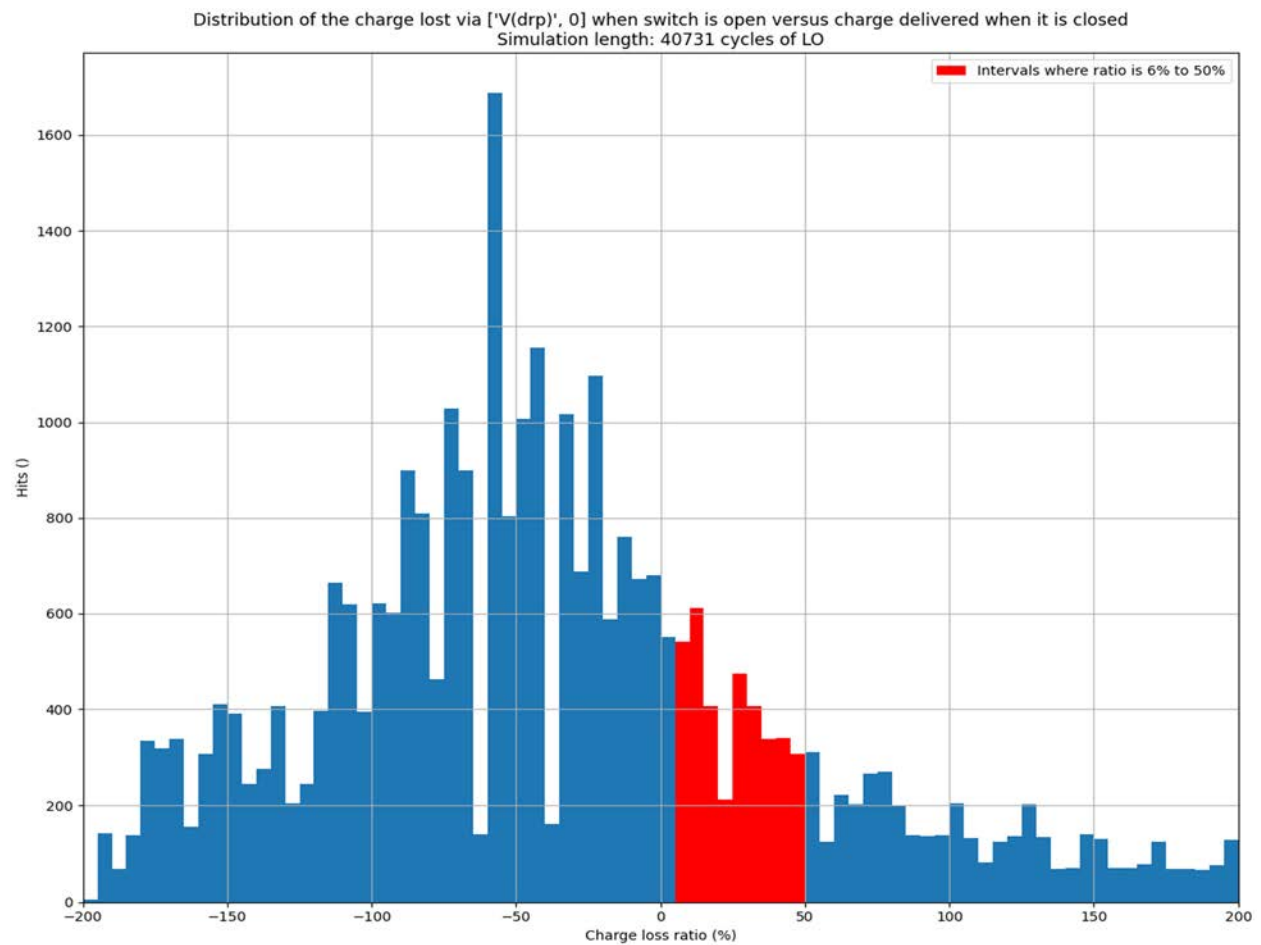
DEMAW-SIM-FIG. 5.7. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.7).

54. DEMAW-SIM-FIG. 6.7 is a graphical representation showing carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.7.



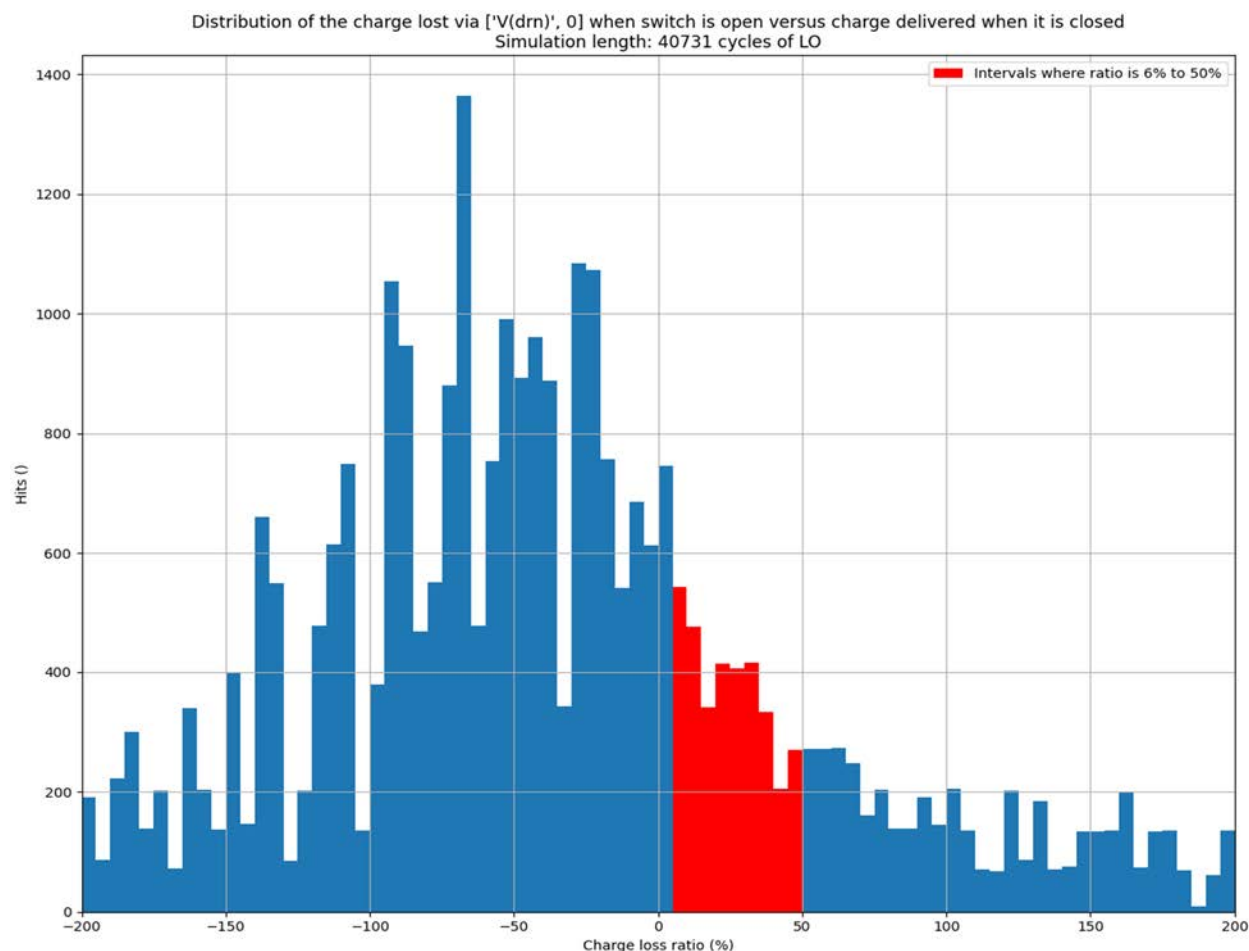
DEMAW-SIM-FIG. 6.7. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.7).

55. DEMAW-SIM-FIG. 7.7A is a histogram of the charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.7.



DEMAW-SIM-FIG. 7.7A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.7).

56. DEMAW-SIM-FIG. 7.7B is a histogram of the charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.7.

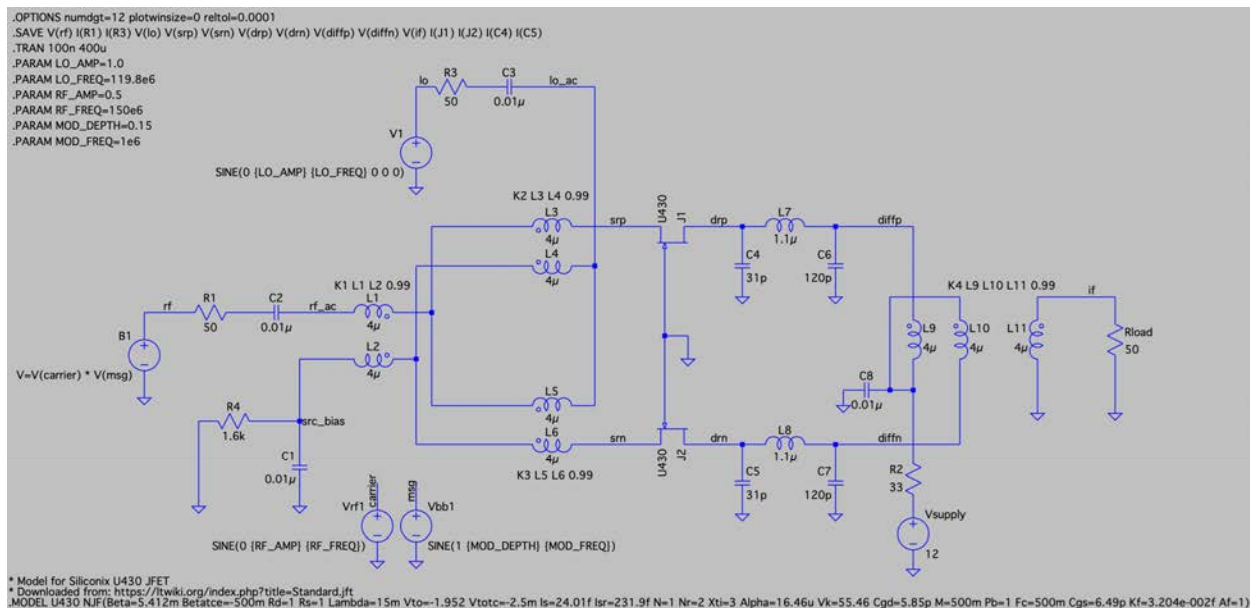


DEMAW-SIM-FIG. 7.7B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.7).

B. Simulation Results For an Input Signal Reduced by 6 dB

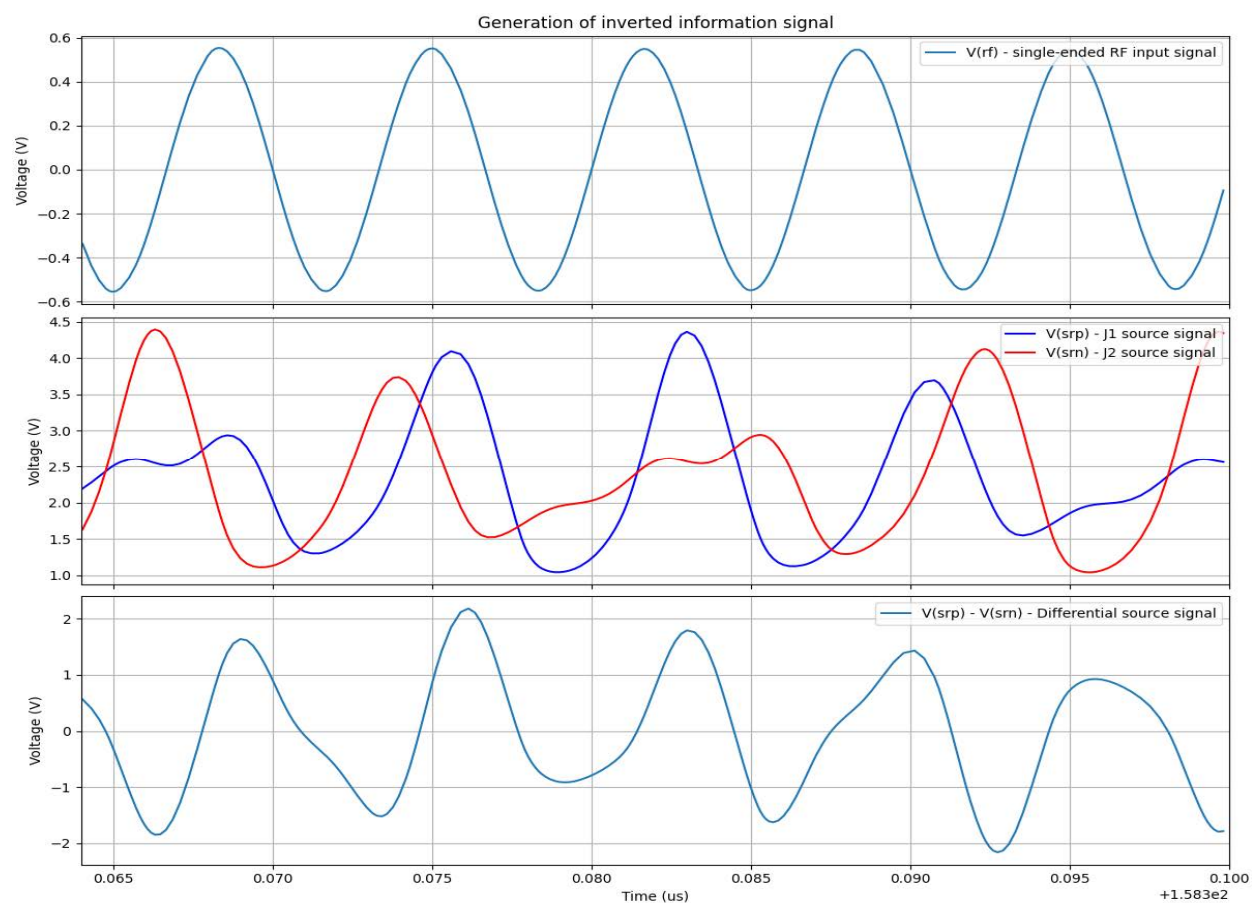
57. DEMAW-SIM-FIG. 1.8 is a schematic illustration of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 6 dB. I have created additional figures DEMAW-SIM-FIGS. 4.8, 5.8, 6.8, 7.8A and 7.8B based on simulation output from DEMAW-SIM-FIG. 1.8. DEMAW-SIM-FIGS. 4.8, 5.8, 6.8, 7.8A and 7.8B show the same simulation output from DEMAW-SIM-FIG. 1.8 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from

DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.8, 4.8, 5.8, 6.8, 7.8A and 7.8B.



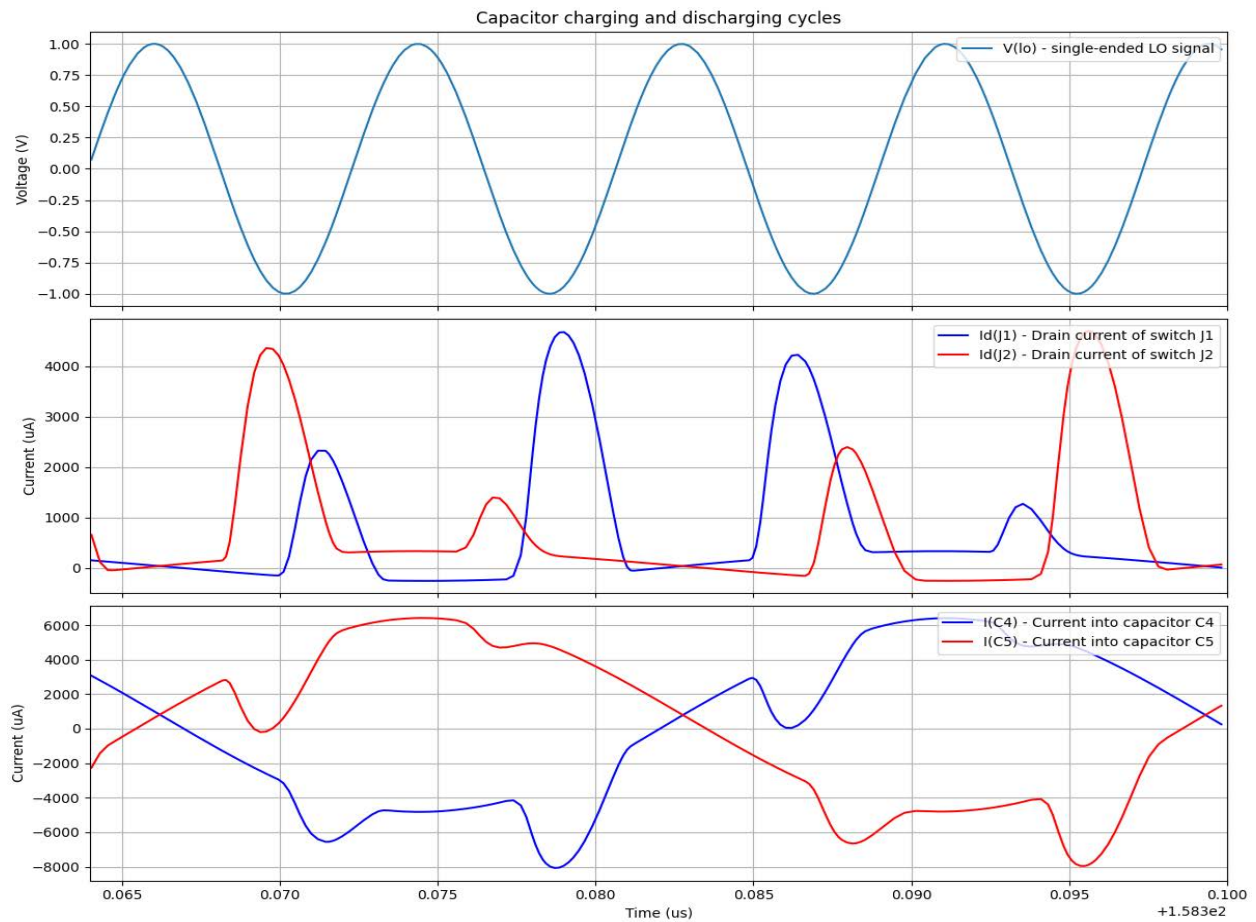
DEMAW-SIM-FIG. 1.8. DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 6 dB.

58. DEMAW-SIM-FIG. 4.8 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.8.



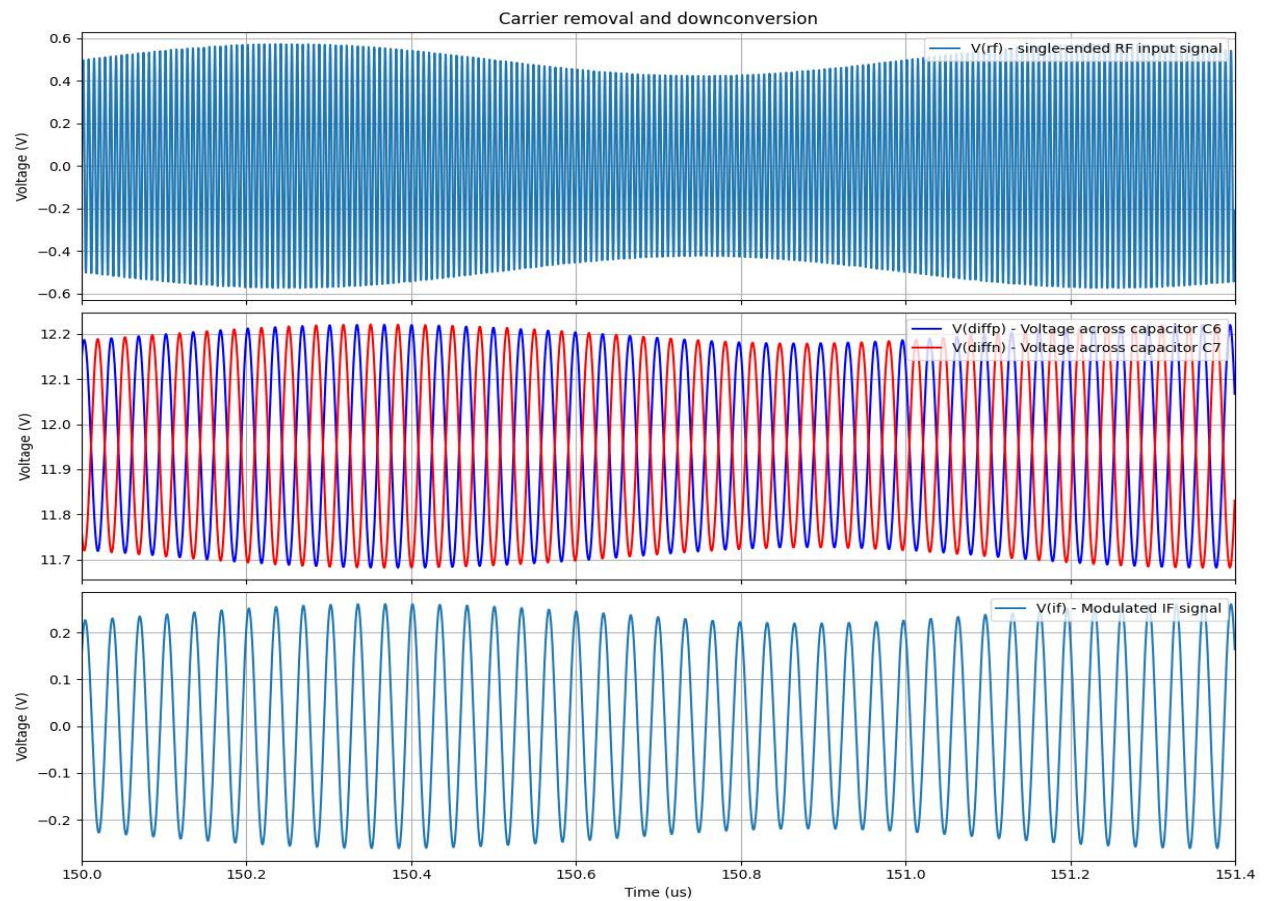
DEMAW-SIM-FIG. 4.8. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.8).

59. DEMAW-SIM-FIG. 5.8 is a graphical representation of the charging and discharging cycles for capacitors C4 and C5 of the circuit of DEMAW-SIM-FIG. 1.8.



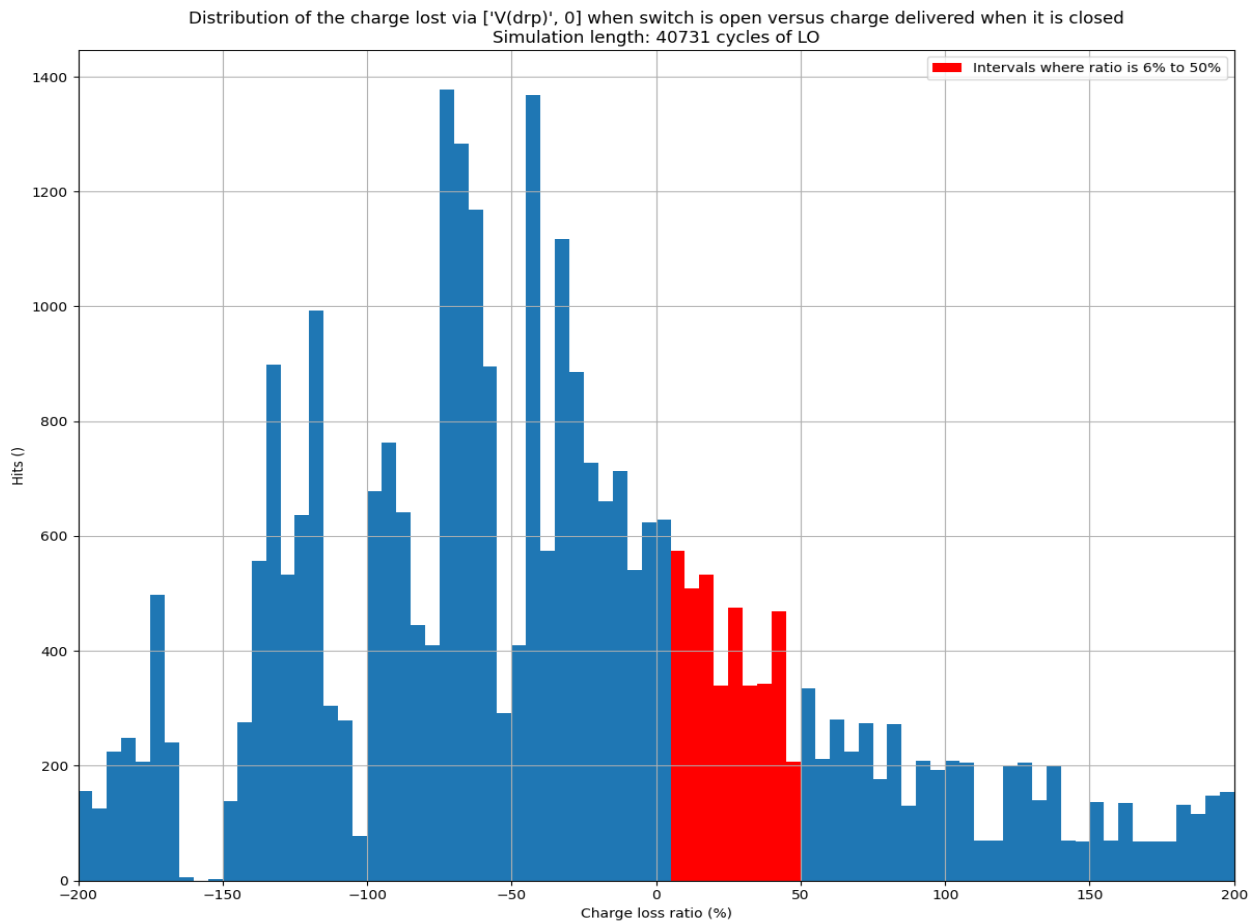
DEMAW-SIM-FIG. 5.8. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.8).

60. DEMAW-SIM-FIG. 6.8 is a graphical representation of the carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.8.



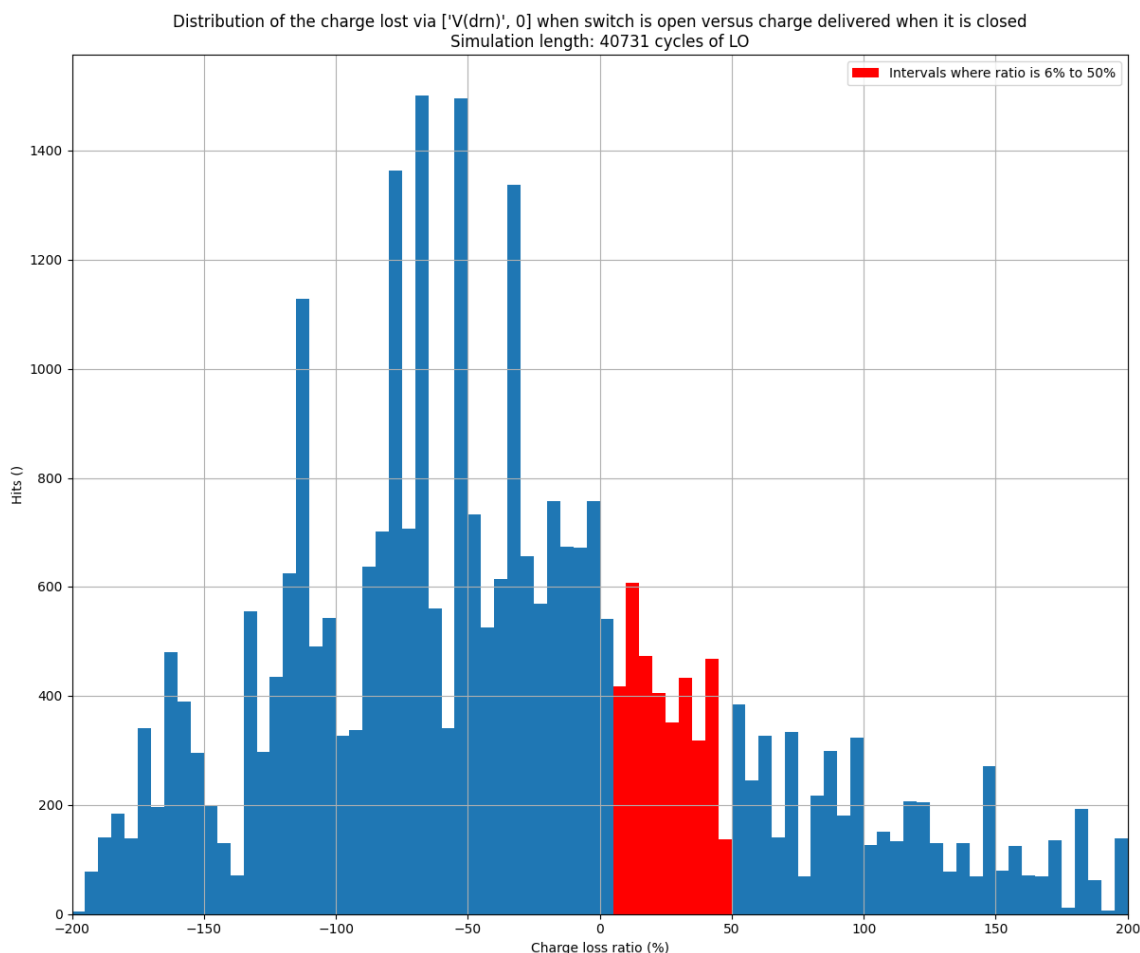
DEMAW-SIM-FIG. 6.8. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.8).

61. DEMAW-SIM-FIG. 7.8A is a histogram of the charge loss ratio percentages for capacitor C4 of the circuit of DEMAW-SIM-FIG. 1.8.



DEMAW-SIM-FIG. 7.8A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.8).

62. DEMAW-SIM-FIG. 7.8B is a histogram of the charge loss ratio percentages for capacitor C5 of the circuit of DEMAW-SIM-FIG. 1.8.

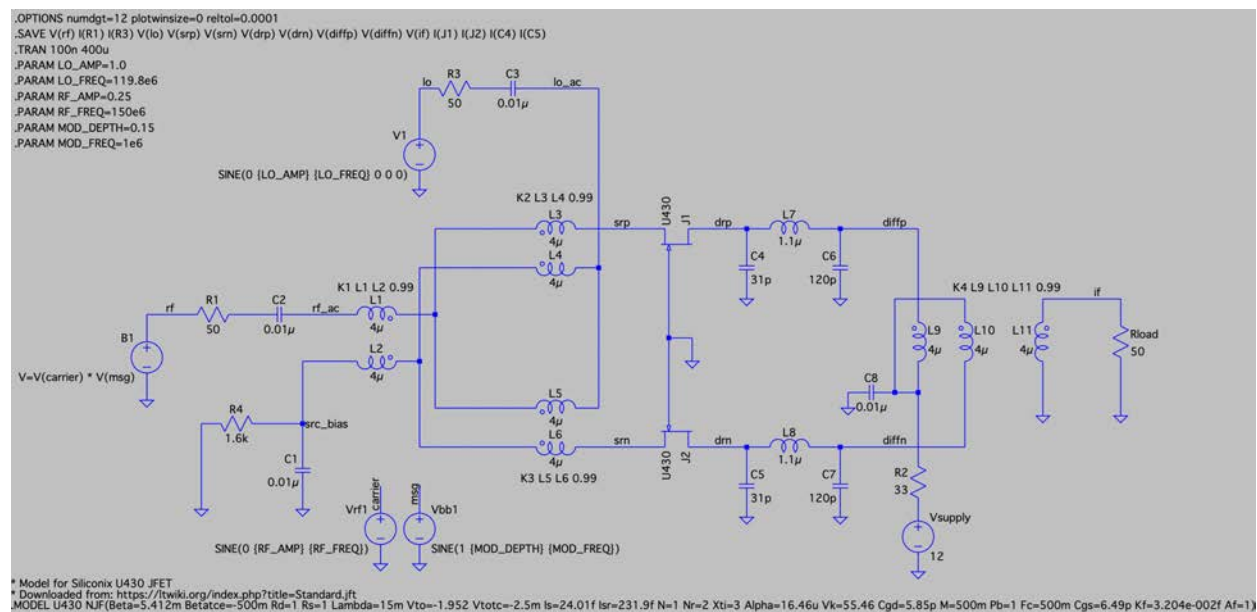


DEMAW-SIM-FIG. 7.8B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.8).

C. Simulation Results For an Input Signal Reduced by 12 dB

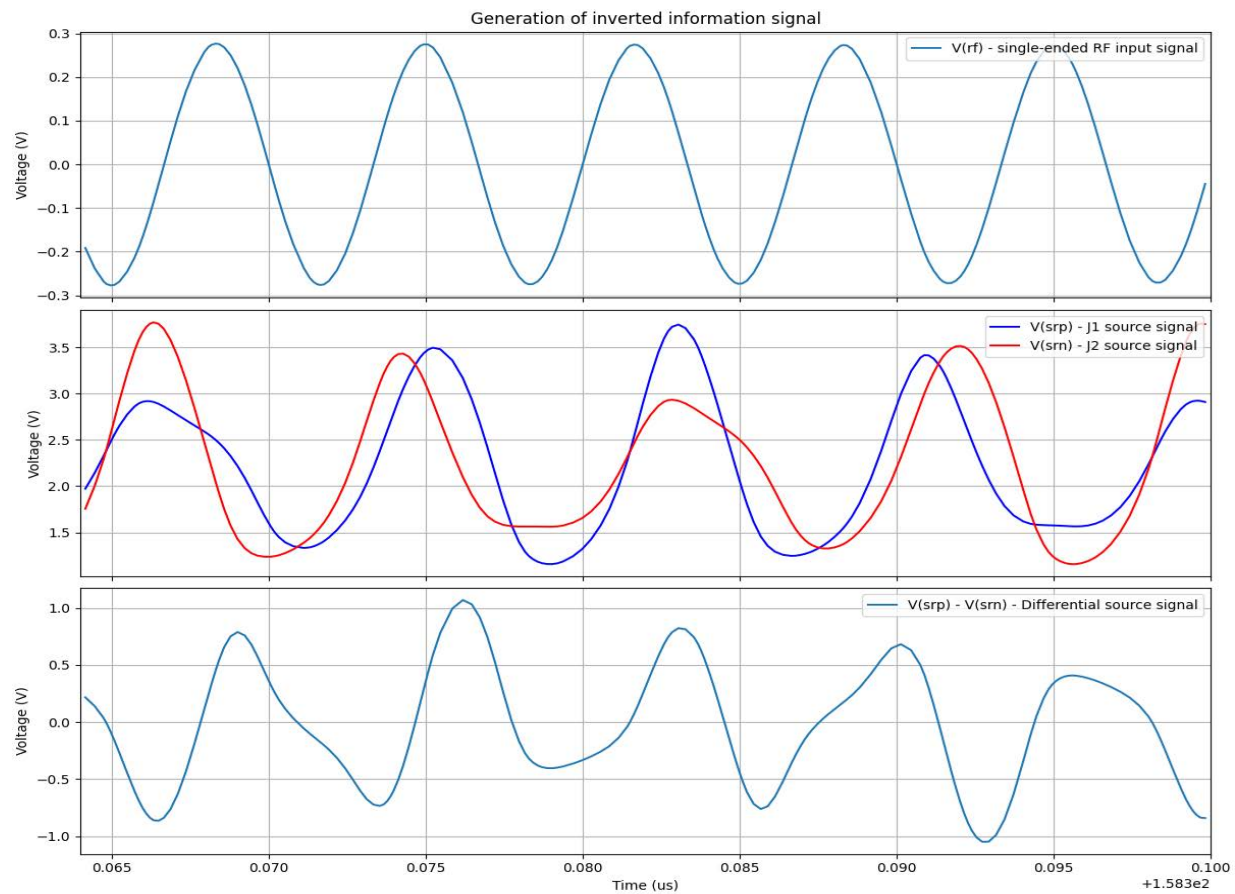
63. DEMAW-SIM-FIG. 1.9 is a schematic representation of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 12 dB. I have created additional figures DEMAW-SIM-FIGS. 4.9, 5.9, 6.9, 7.9 and 7.9B based on simulation output from DEMAW-SIM-FIG. 1.9. DEMAW-SIM-FIGS. 4.9, 5.9, 6.9, 7.9A and 7.9B show the same simulation output from DEMAW-SIM-FIG. 1.9 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from

DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.9, 4.9, 5.9, 6.9, 7.9A and 7.9B.



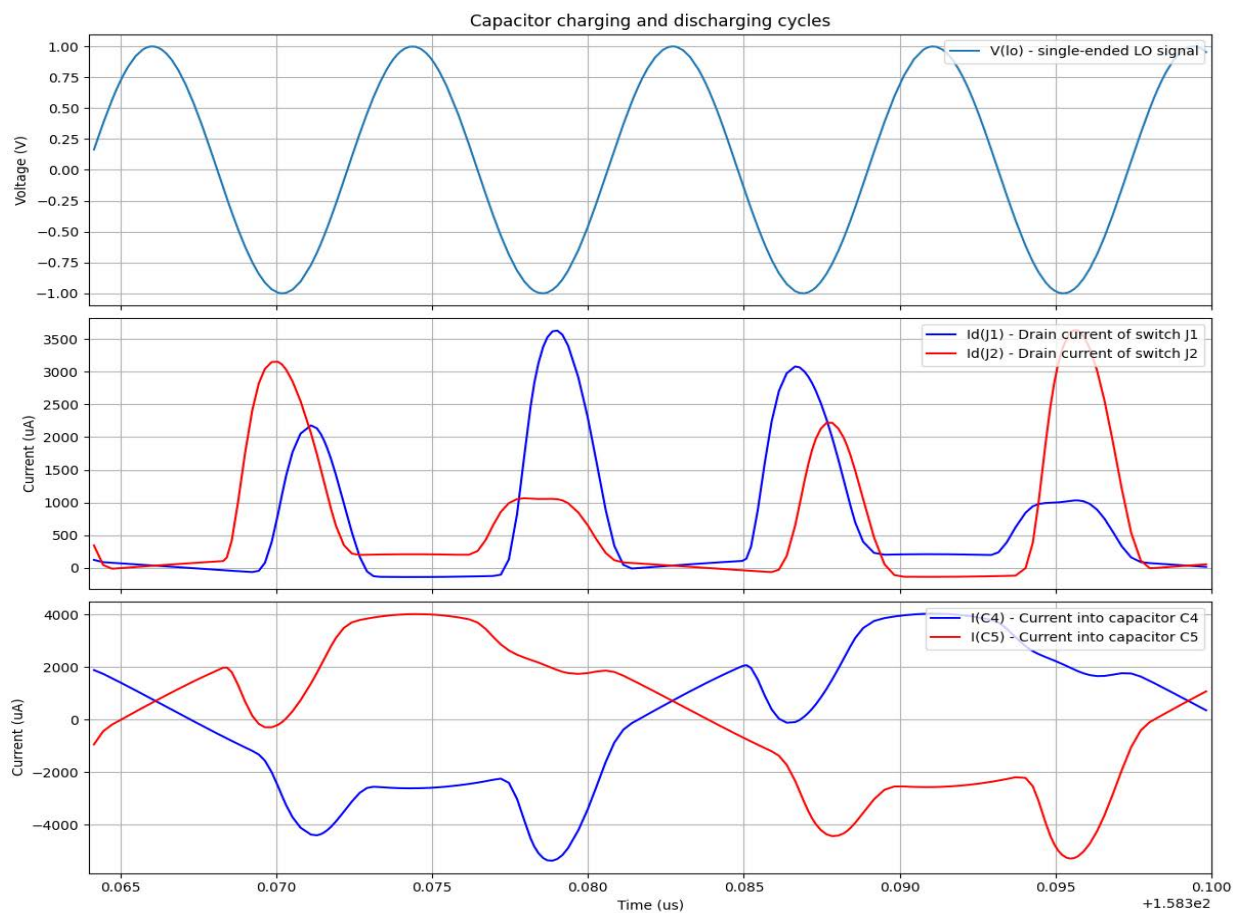
DEMAW-SIM-FIG. 1.9. DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 12 dB.

64. DEMAW-SIM-FIG. 4.9 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.9.



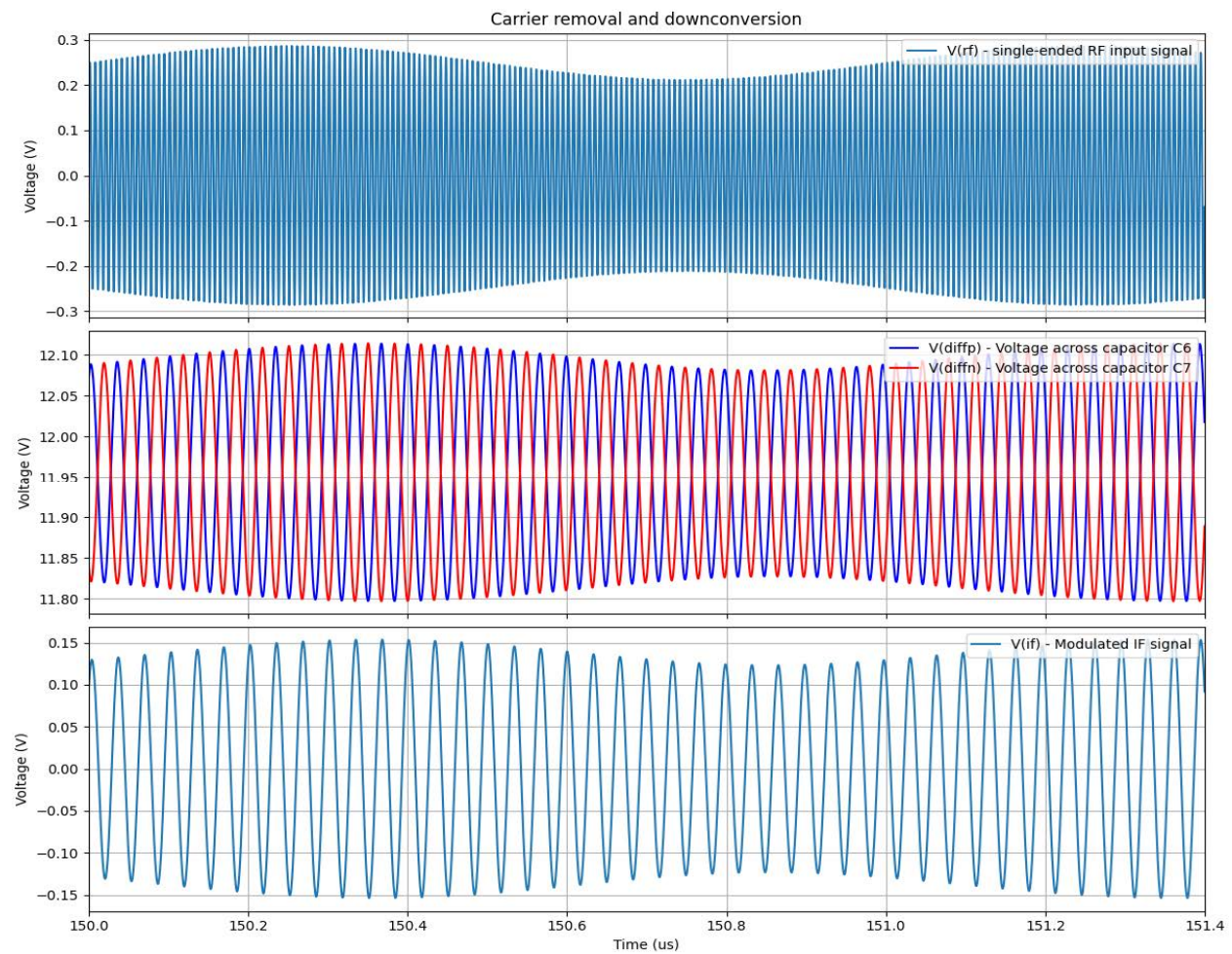
DEMAW-SIM-FIG. 4.9. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.9).

65. DEMAW-SIM-FIG. 5.9 is a graphical representation of the charging and discharging cycles for capacitors C4 and C5 of the circuit of DEMAW-SIM-FIG. 1.9.



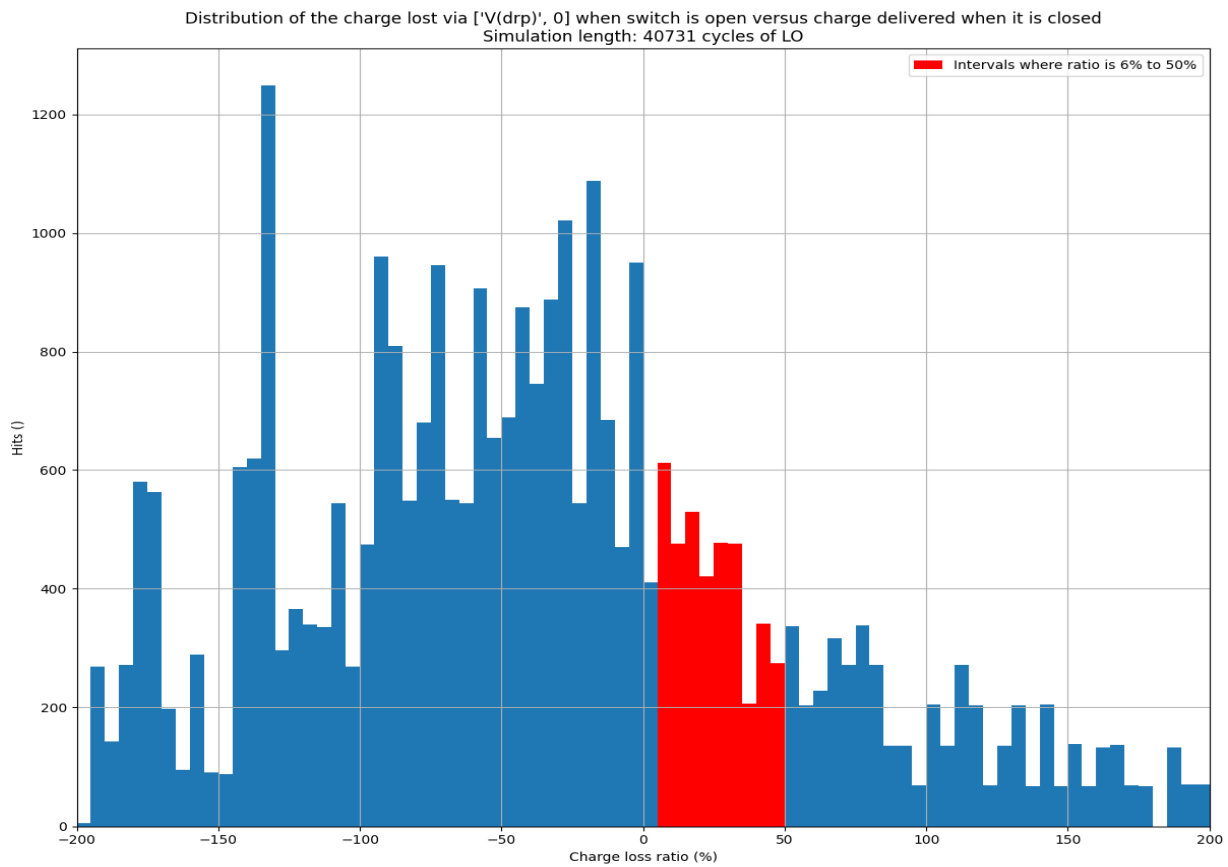
DEMAW-SIM-FIG. 5.9. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.9).

66. DEMAW-SIM-FIG. 6.9 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.9.



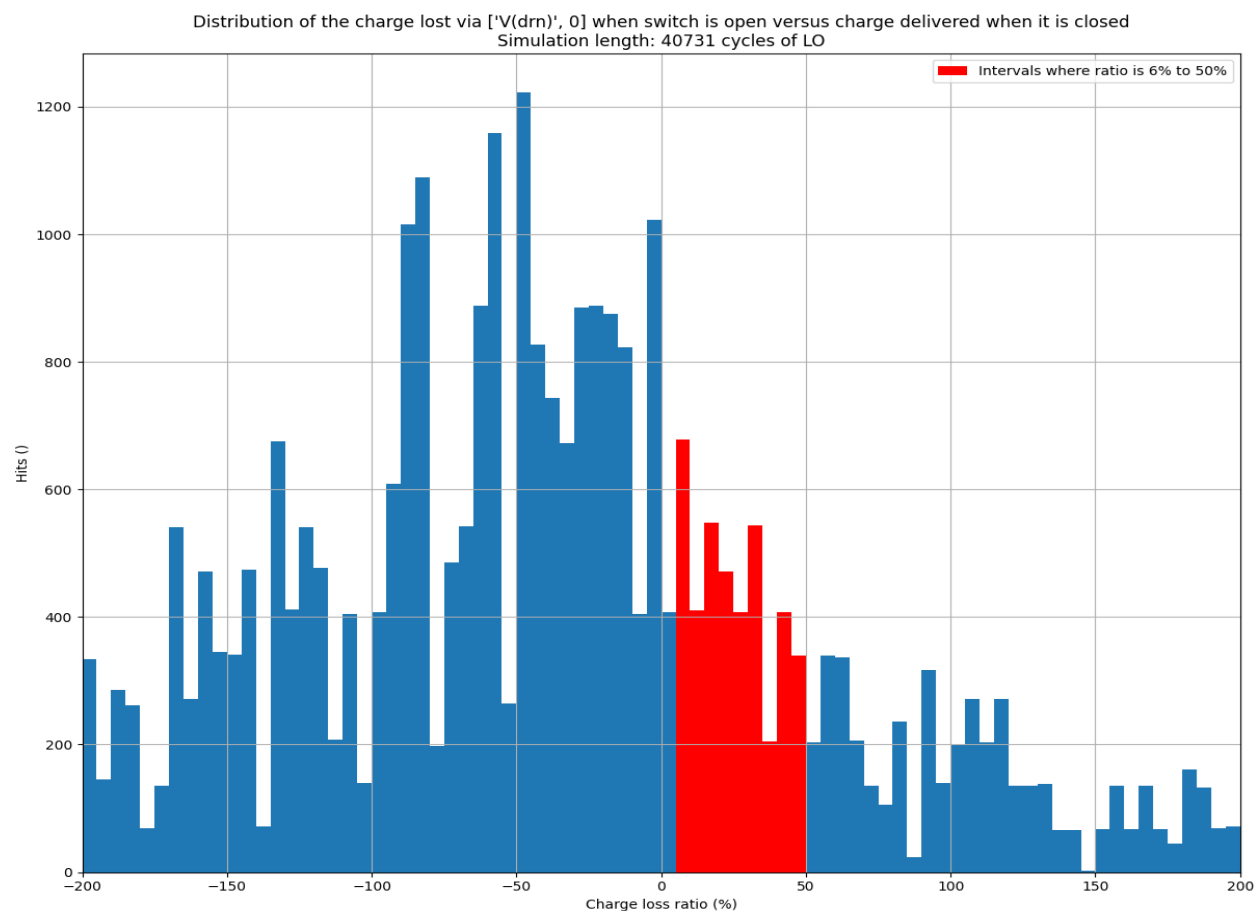
67. DEMAW-SIM-FIG. 6.9. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.9).

68. DEMAW-SIM-FIG. 7.9A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.9.



DEMAW-SIM-FIG. 7.9A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.9).

69. DEMAW-SIM-FIG. 7.9B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.9.

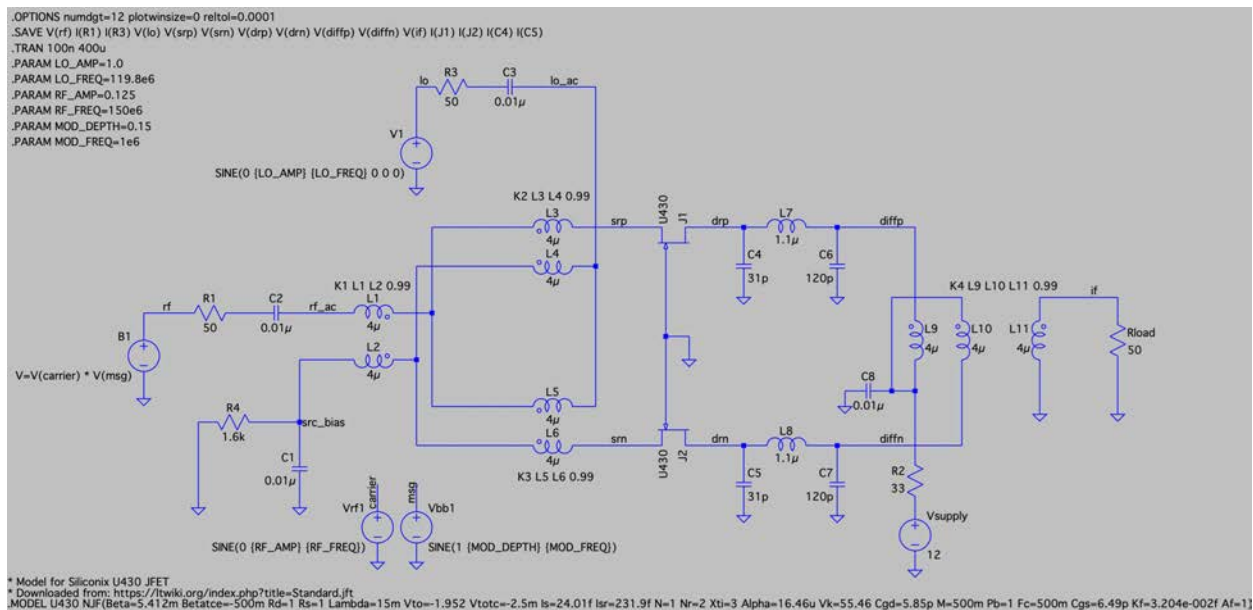


70. DEMAW-SIM-FIG. 7.9B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.9).

D. Simulation Results For an Input Signal Reduced by 18 dB

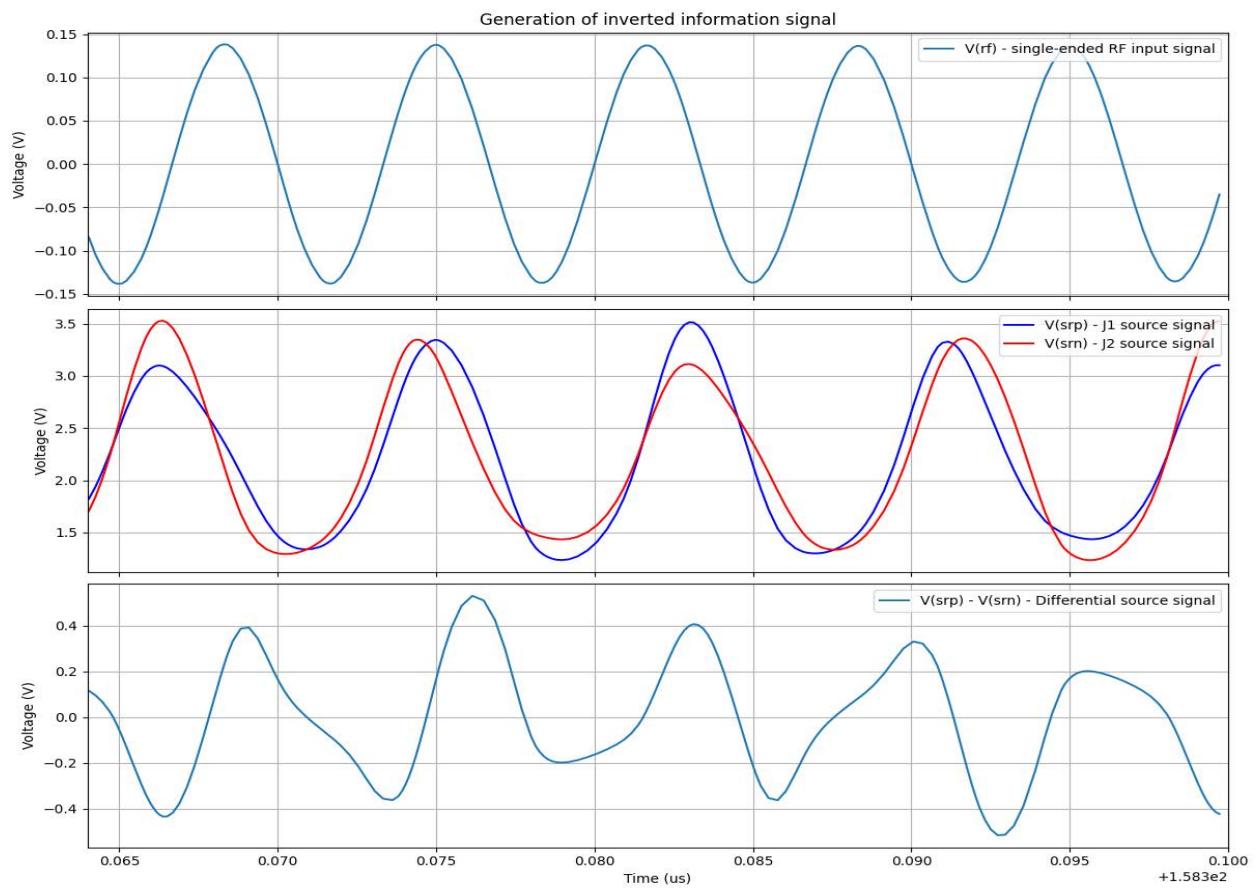
71. DEMAW-SIM-FIG. 1.10 is a schematic illustration of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 18 dB. I have created additional figures DEMAW-SIM-FIGS. 4.10, 5.10, 6.10, 7.10A and 7.10B based on simulation output from DEMAW-SIM-FIG. 1.10. DEMAW-SIM-FIGS. 4.10, 5.10, 6.10, 7.10A and 7.10B show the same simulation output from DEMAW-SIM-FIG. 1.10 as DEMAW-SIM-FIGS. 4, 5, 6,

and 7 show from DEMA-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMA-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMA-SIM-FIGS. 1.10, 4.10, 5.10, 6.10, 7.10A and 7.10B.



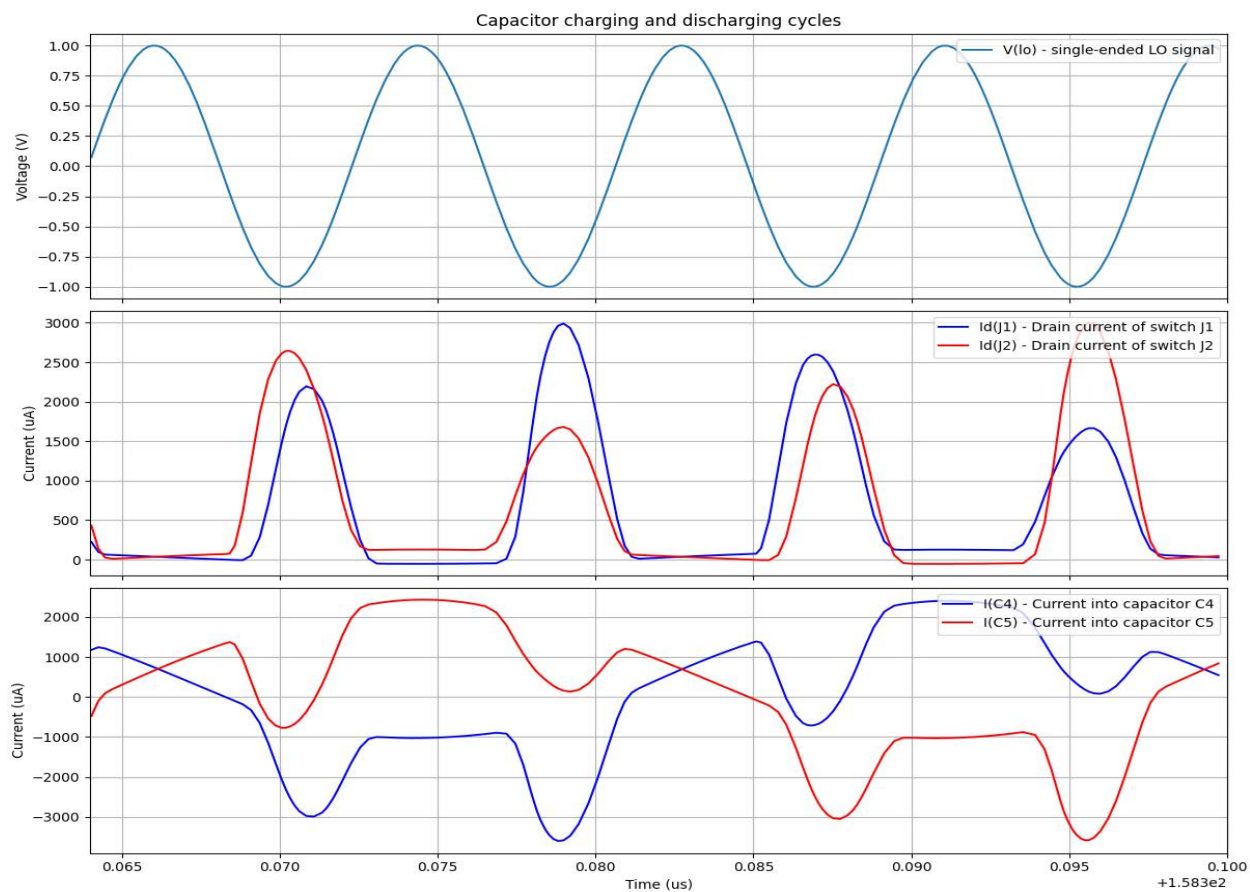
DEMA-SIM-FIG. 1.10. DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 18 dB.

72. DEMA-SIM-FIG. 4.10 is a graphical representation of the generation of inverted information signal for the circuit of DEMA-SIM-FIG. 1.10).



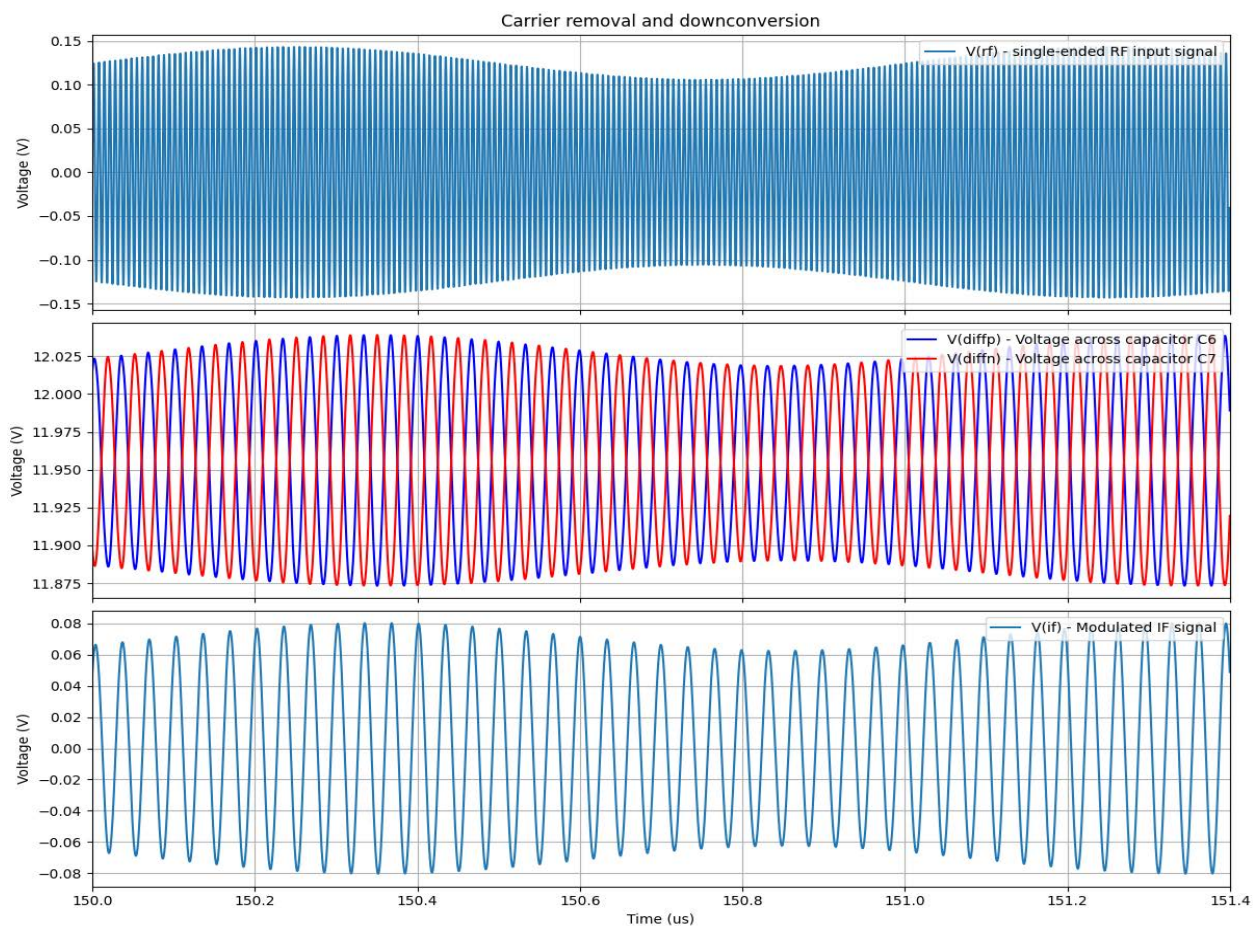
DEMAW-SIM-FIG. 4.10. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.10).

73. DEMAW-SIM-FIG. 5.10 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.10.



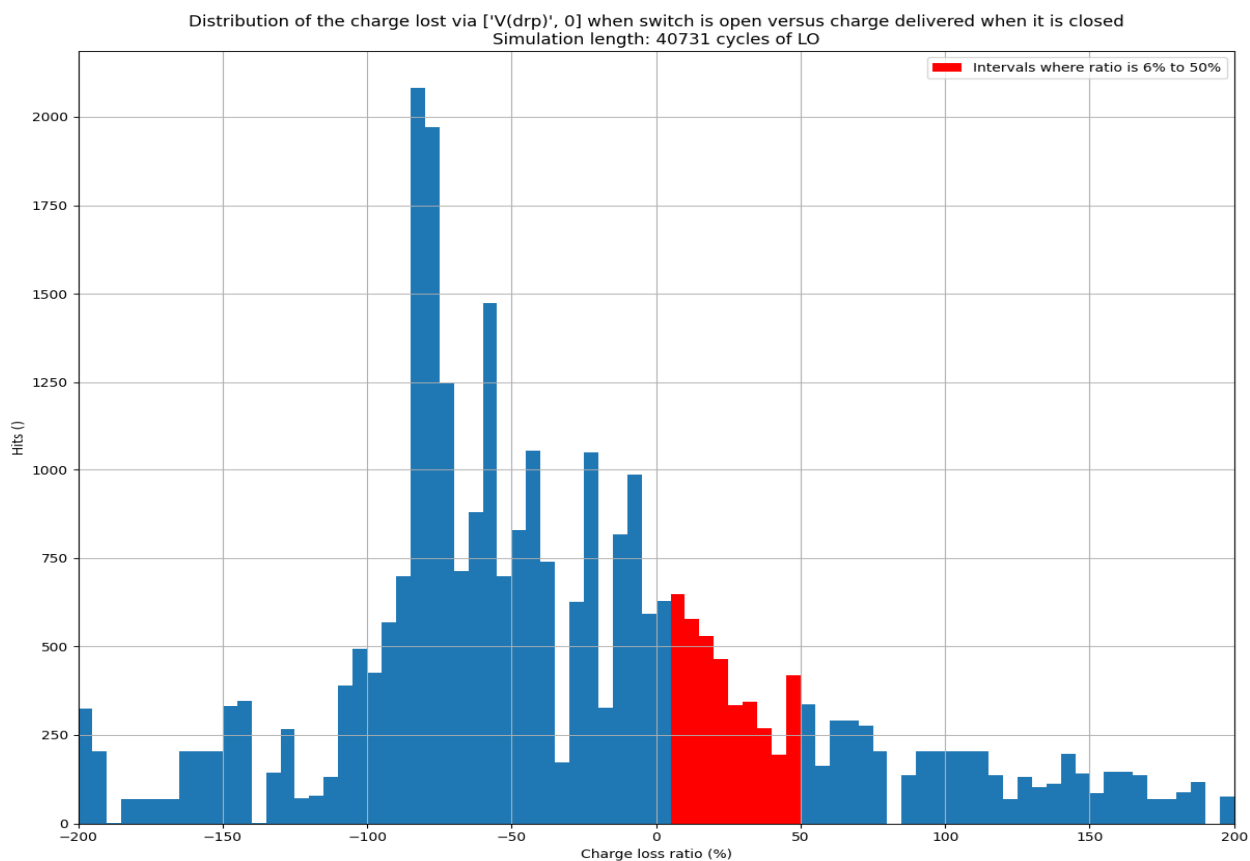
DEMAW-SIM-FIG. 5.10. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.10).

74. DEMAW-SIM-FIG. 6.10 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.10.



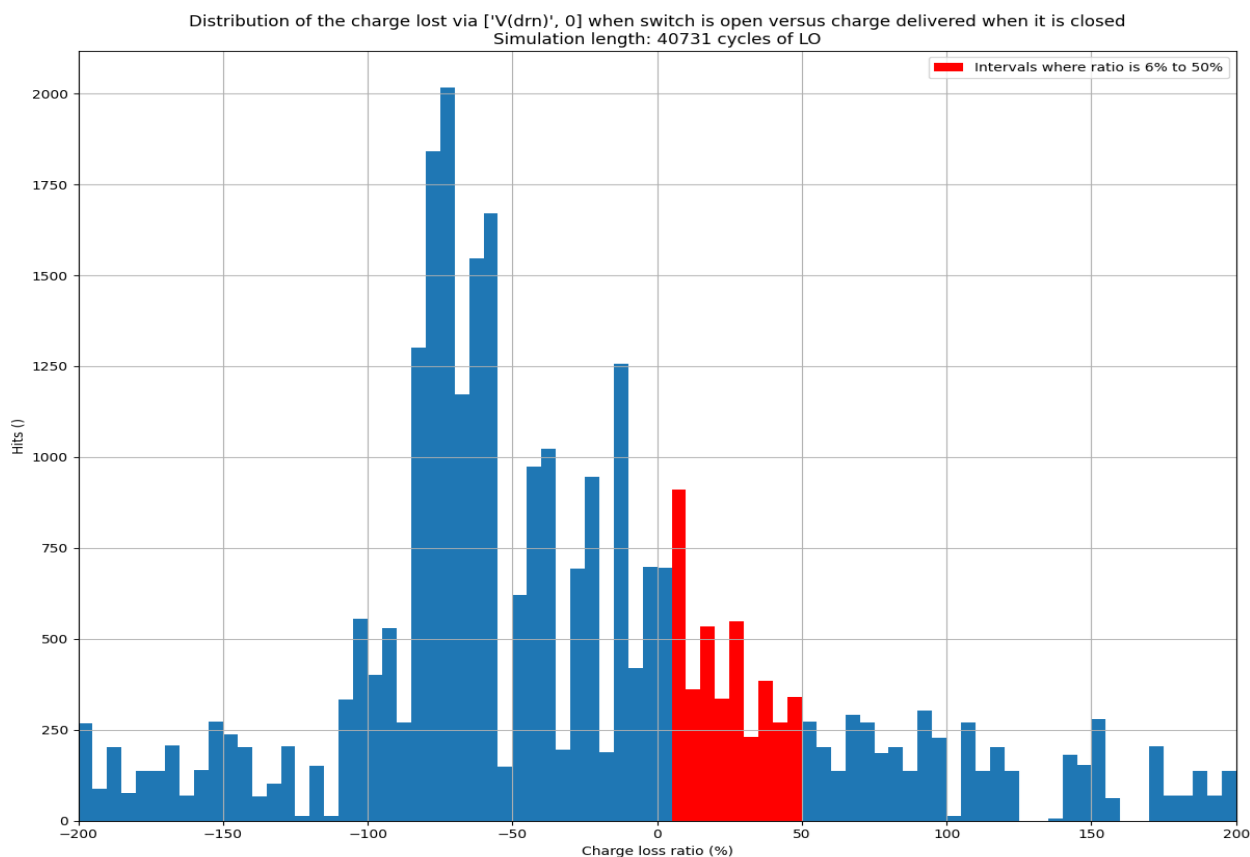
DEMAW-SIM-FIG. 6.10. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.10).

75. DEMAW-SIM-FIG. 7.10A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.10.



DEMAW-SIM-FIG. 7.10A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.10).

76. DEMAW-SIM-FIG. 7.10B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.10.

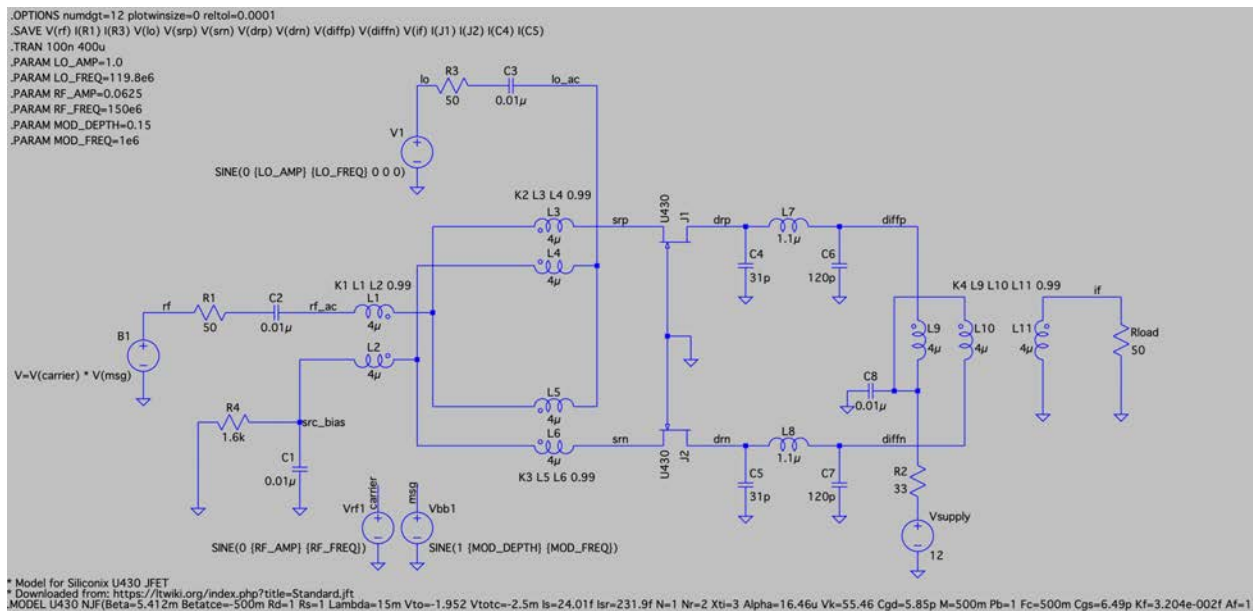


DEMAW-SIM-FIG. 7.10B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.10).

E. Simulation Results For an Input Signal Reduced by 24 dB

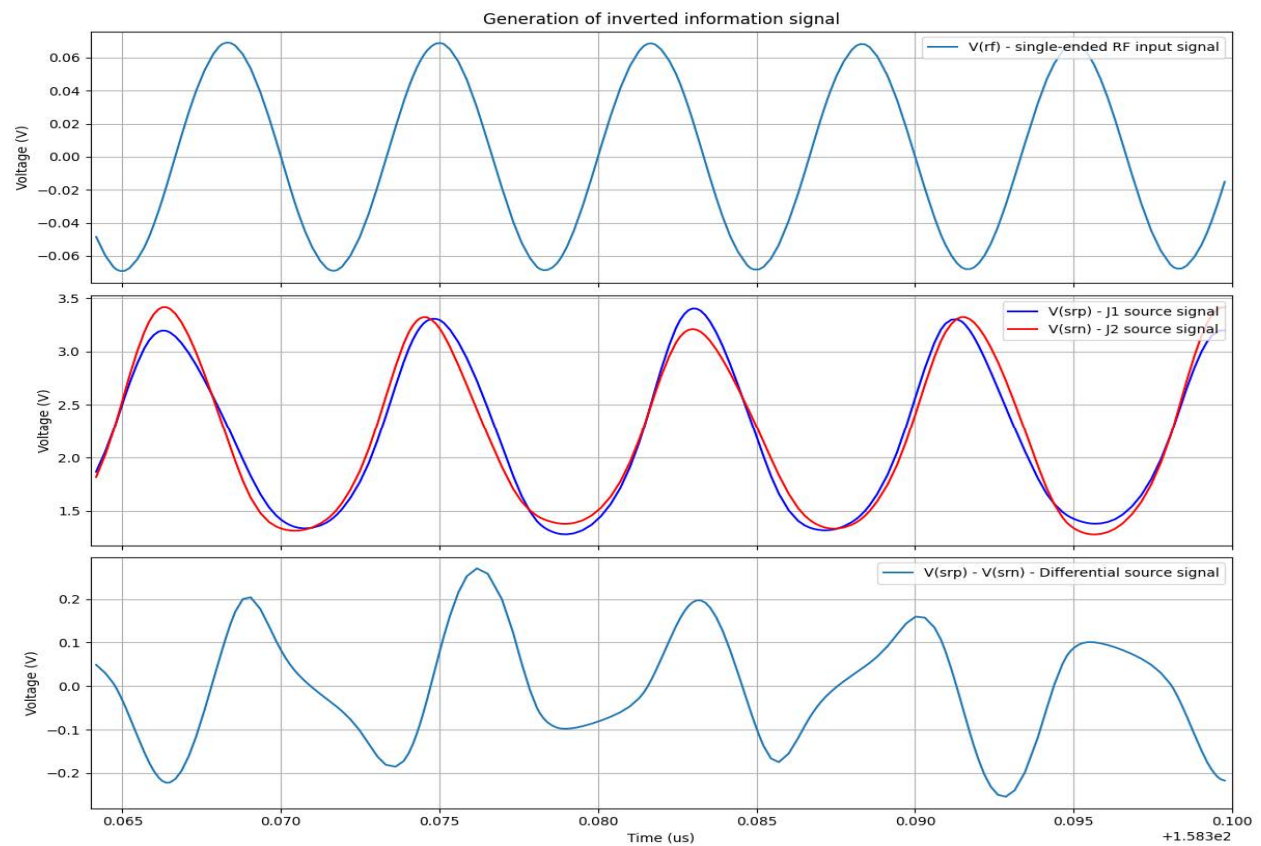
77. DEMAW-SIM-FIG. 1.11 is a schematic illustration of the simulated DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 24 dB. I have created additional figures DEMAW-SIM-FIGS. 4.11, 5.11, 6.11, 7.11A and 7.11B based on simulation output from DEMAW-SIM-FIG. 1.11. DEMAW-SIM-FIGS. 4.11, 5.11, 6.11, 7.11A and 7.11B show the same simulation output from DEMAW-SIM-FIG. 1.11 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMA-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMA-SIM-FIGS. 1.11, 4.11, 5.11, 6.11, 7.11A and 7.11B.



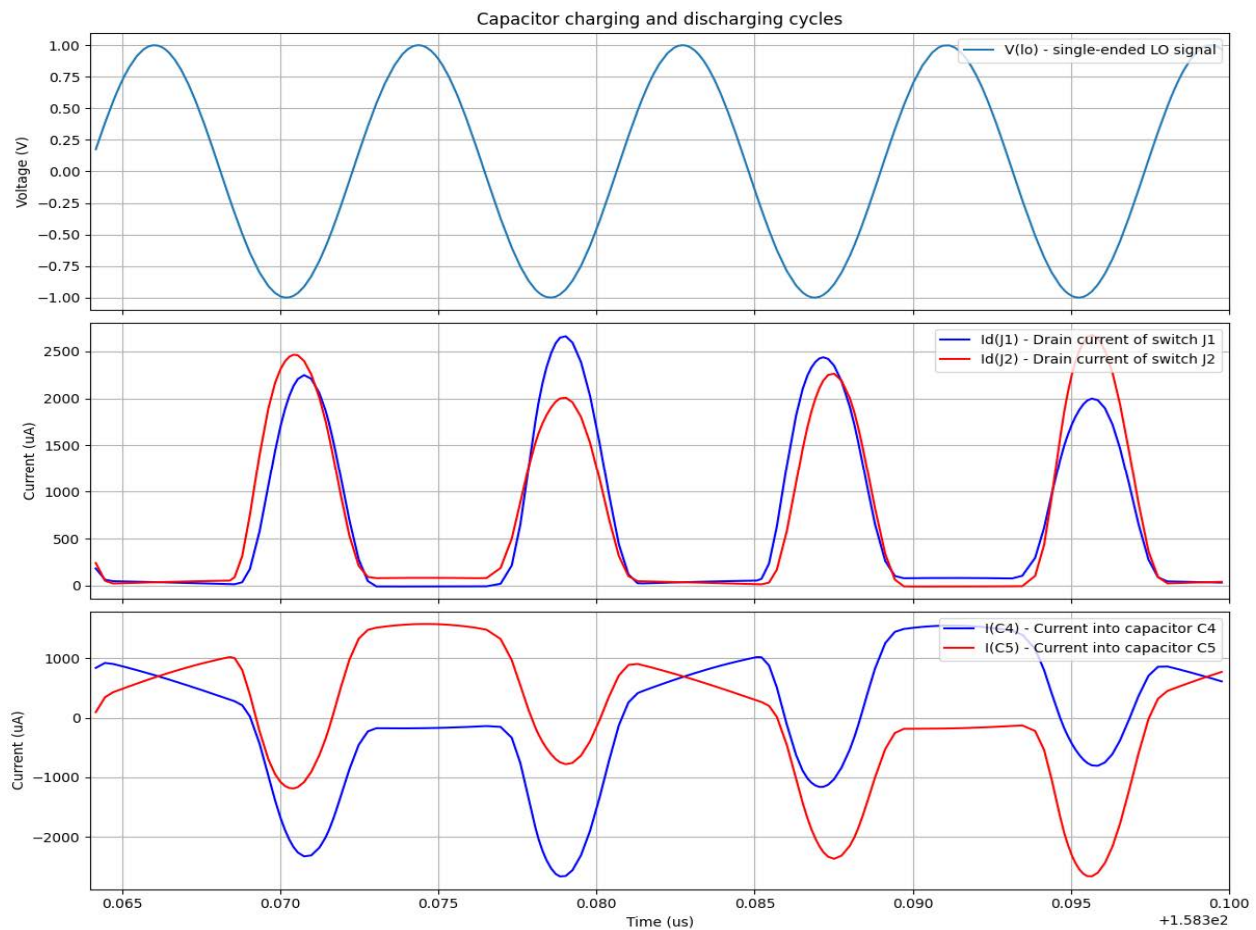
DEMA-SIM-FIG. 1.11. DeMaw circuit modified to match DeMaw FIG. 6.7 with a sinusoidal LO and input signal reduced by 24 dB.

78. DEMA-SIM-FIG. 4.11 is a graphical representation of the generation of inverted information signal for the circuit of DEMA-SIM-FIG. 1.11.



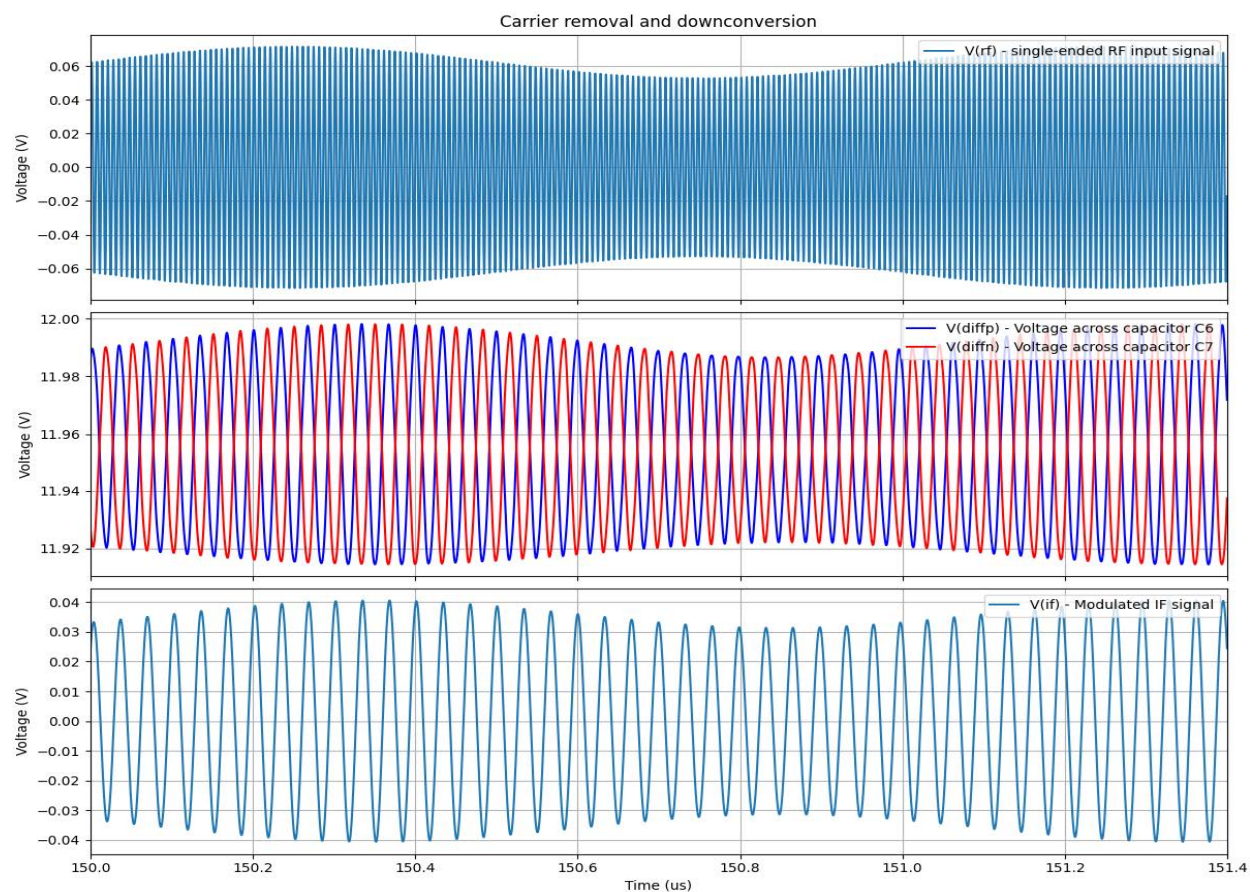
DEMAW-SIM-FIG. 4.11. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.11).

79. DEMAW-SIM-FIG. 5.11 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.11.



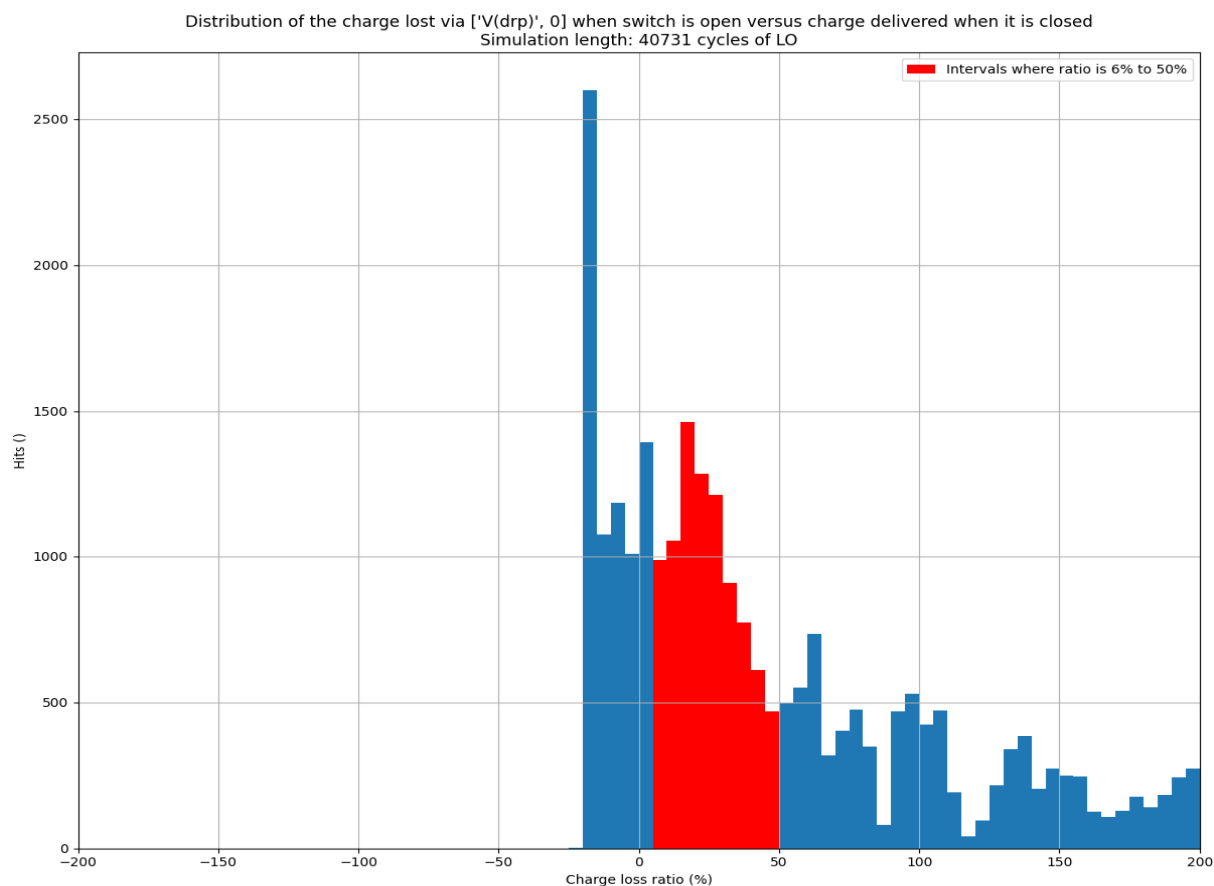
DEMAW-SIM-FIG. 5.11. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.11).

80. DEMAW-SIM-FIG. 6.11 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.11.



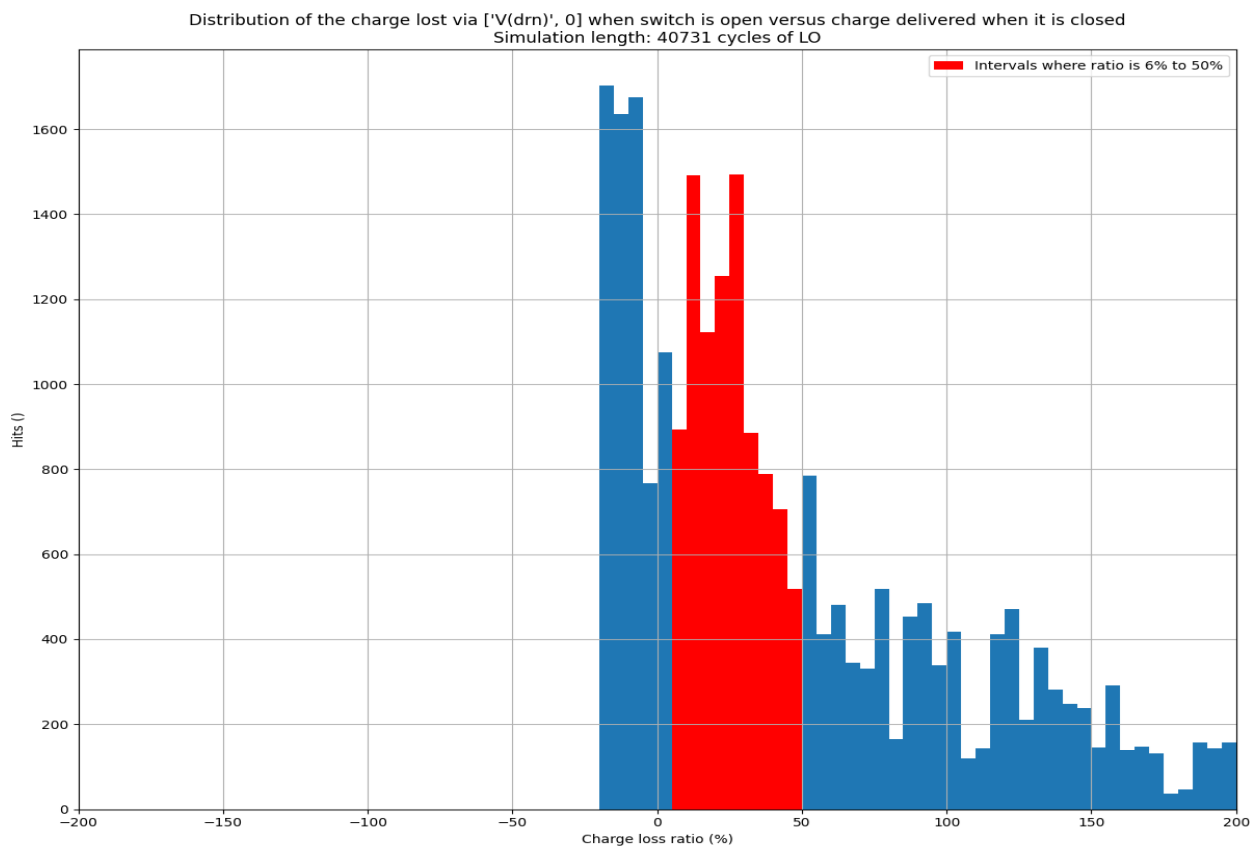
DEMAW-SIM-FIG. 6.11. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.11).

81. DEMAW-SIM-FIG. 7.11A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.11.



DEMAW-SIM-FIG. 7.11A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.11).

82. DEMAW-SIM-FIG. 7.11B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.11.



DEMAW-SIM-FIG. 7.11B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.11).

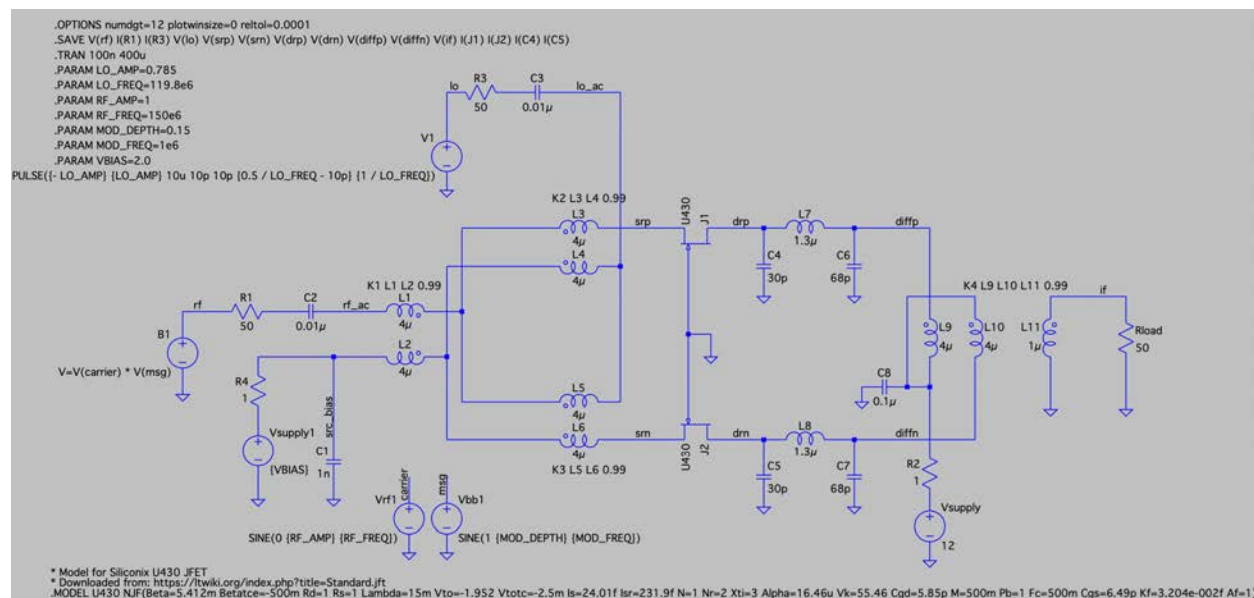
V. DeMaw Circuit Modified to Match Oxner With a Squared-Up LO

83. The DeMaw textbook references Siliconix Application Note AN72-1 written by E. Oxner that presents a circuit, denoted as the “Oxner circuit” herein. DeMaw states that the Oxner circuit is “similar” to that shown in FIG. 6.7 of DeMaw. The AN72-1 application note provides more detailed information about the Oxner circuit than DeMaw provides about the circuit shown in DeMaw FIG. 6.7. To further demonstrate that I have not chosen component values and circuit configurations to “get the results [that TI] needed” as alleged in the POPR, the simulation results

presented in this section correspond to the circuit with the component values and configuration described in the AN72-1 application note. Again, five sets of simulation results are presented which differ only in the power of the RF input to the mixer.

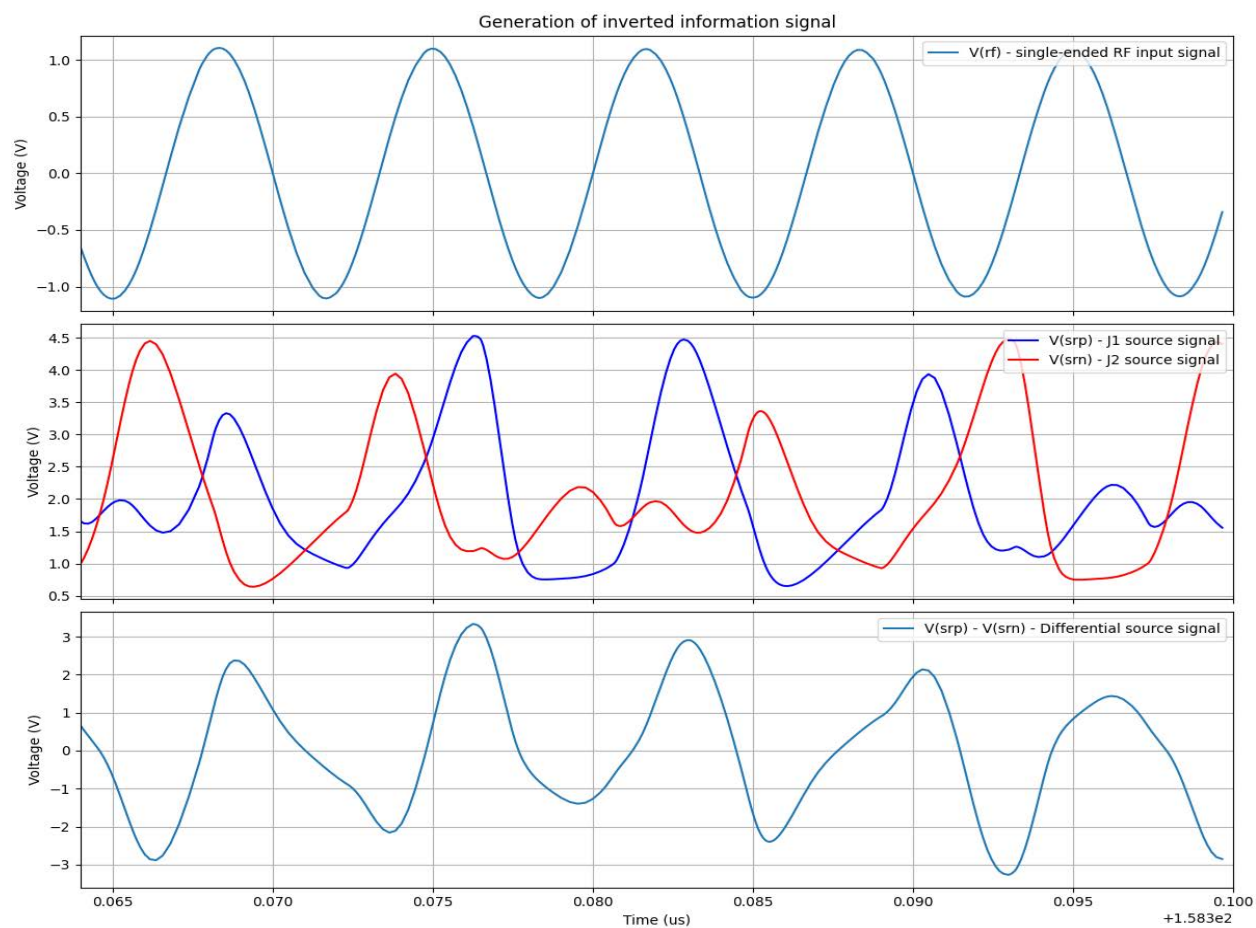
A. Simulation Results For a Large Input Signal

84. DEMAW-SIM-FIG. 1.12 is a schematic illustration of the simulated DeMaw FIG. 6.7 circuit modified Oxner with a squared-up LO and a large input signal. I have created additional figures DEMAW-SIM-FIGS. 4.12, 5.12, 6.12, 7.12A and 7.12B based on simulation output from DEMAW-SIM-FIG. 1.12. DEMAW-SIM-FIGS. 4.12, 5.12, 6.12, 7.12A and 7.12B show the same simulation output from DEMAW-SIM-FIG. 1.12 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.12, 4.12, 5.12, 6.12, 7.12A and 7.12B.



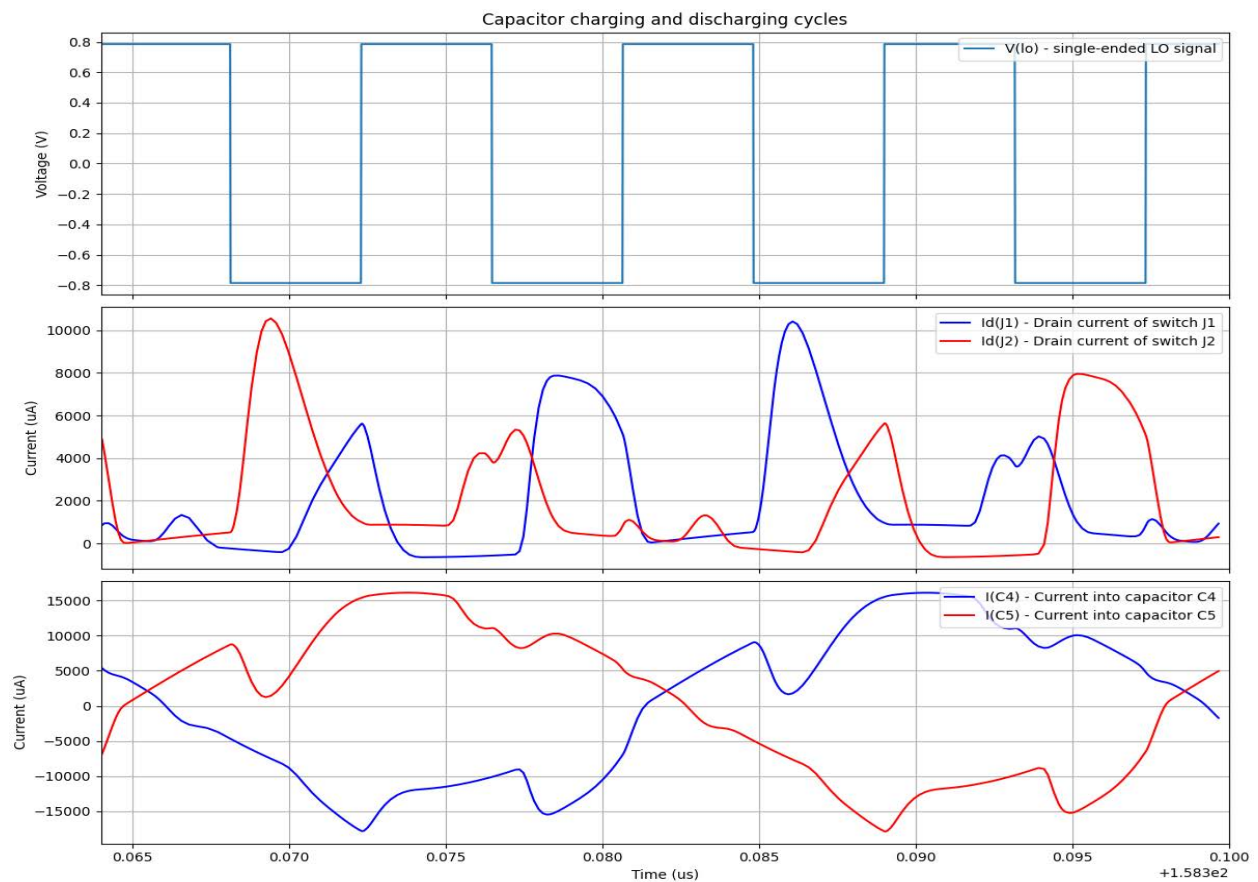
DEMAW-SIM-FIG. 1.12. DeMaw circuit modified to match Oxner with a squared-up LO and a large input signal.

85. DEMAW-SIM-FIG. 4.12 is a graphical representation of the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.12.



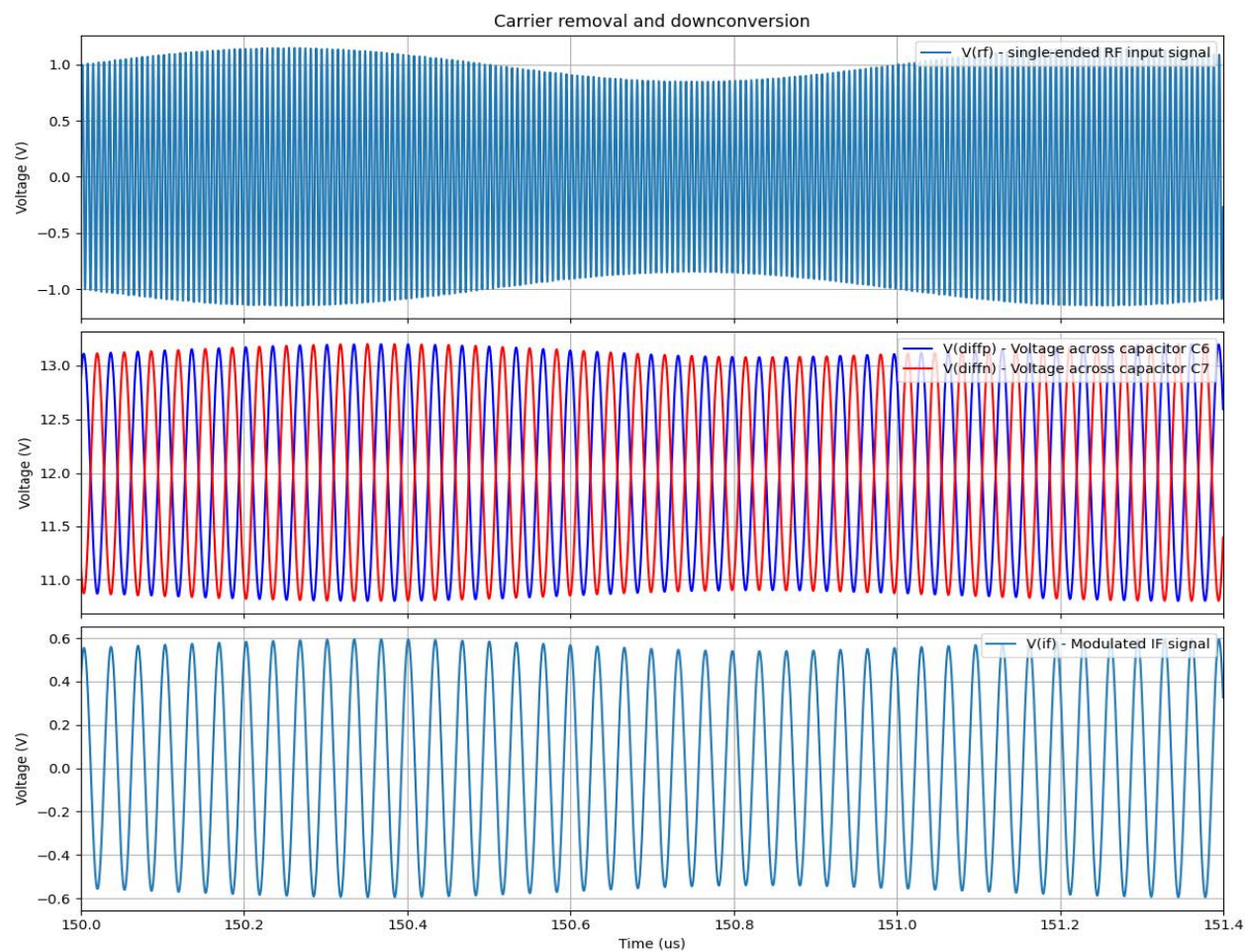
DEMAW-SIM-FIG. 4.12. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.12).

86. DEMAW-SIM-FIG. 5.12 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.12.



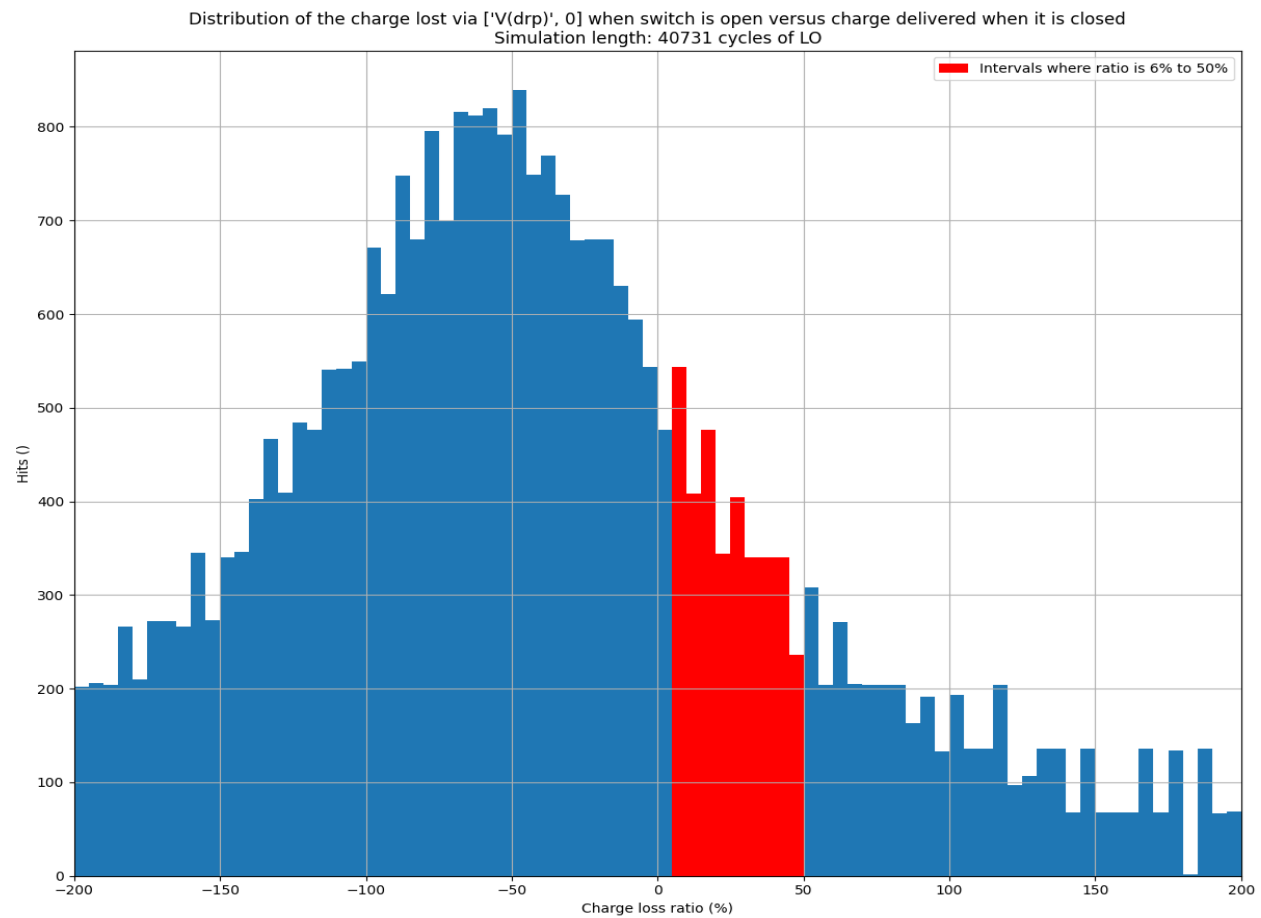
DEMAW-SIM-FIG. 5.12. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.12).

87. DEMAW-SIM-FIG. 6.12 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.12.



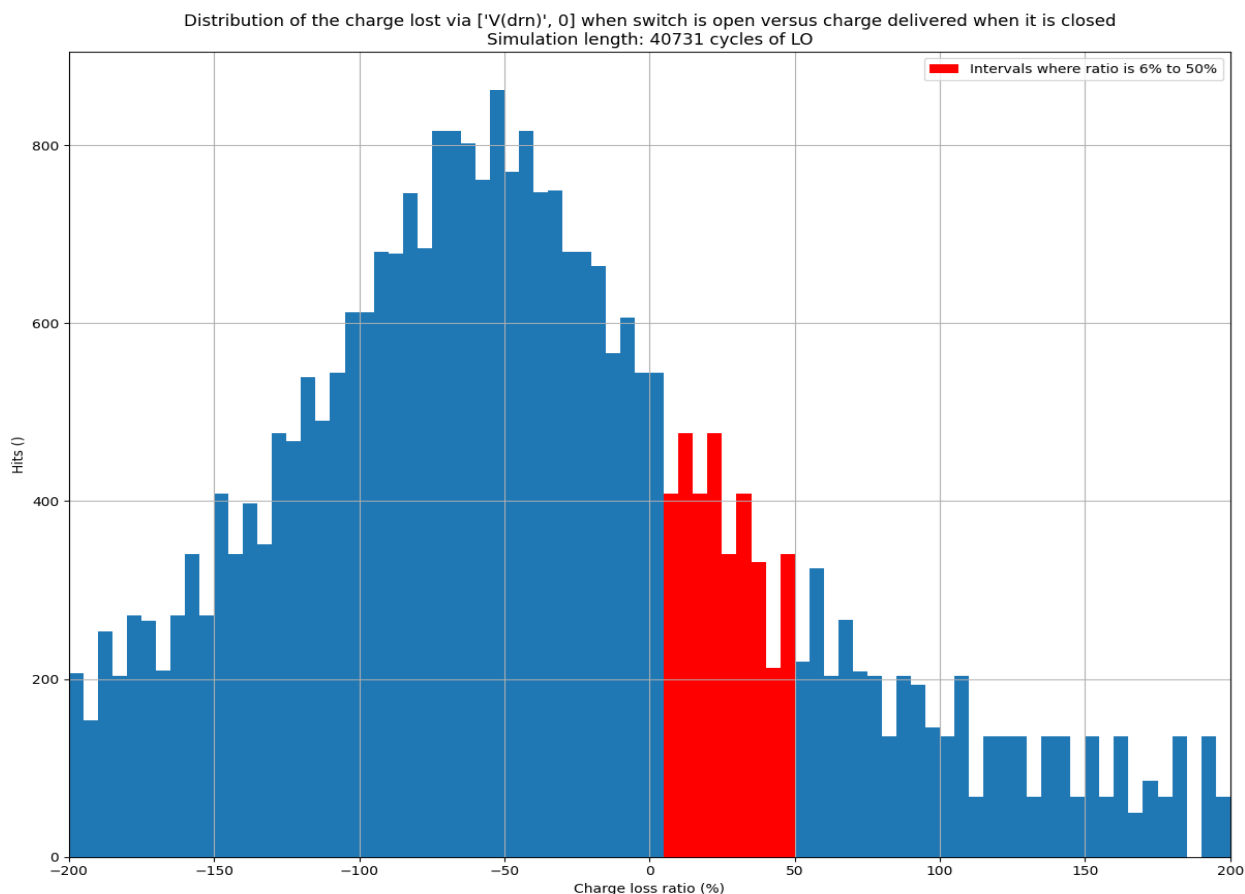
DEMAW-SIM-FIG. 6.12. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.12).

88. DEMAW-SIM-FIG. 7.12A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.12.



DEMAW-SIM-FIG. 7.12A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.12).

89. DEMAW-SIM-FIG. 7.12B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.12.

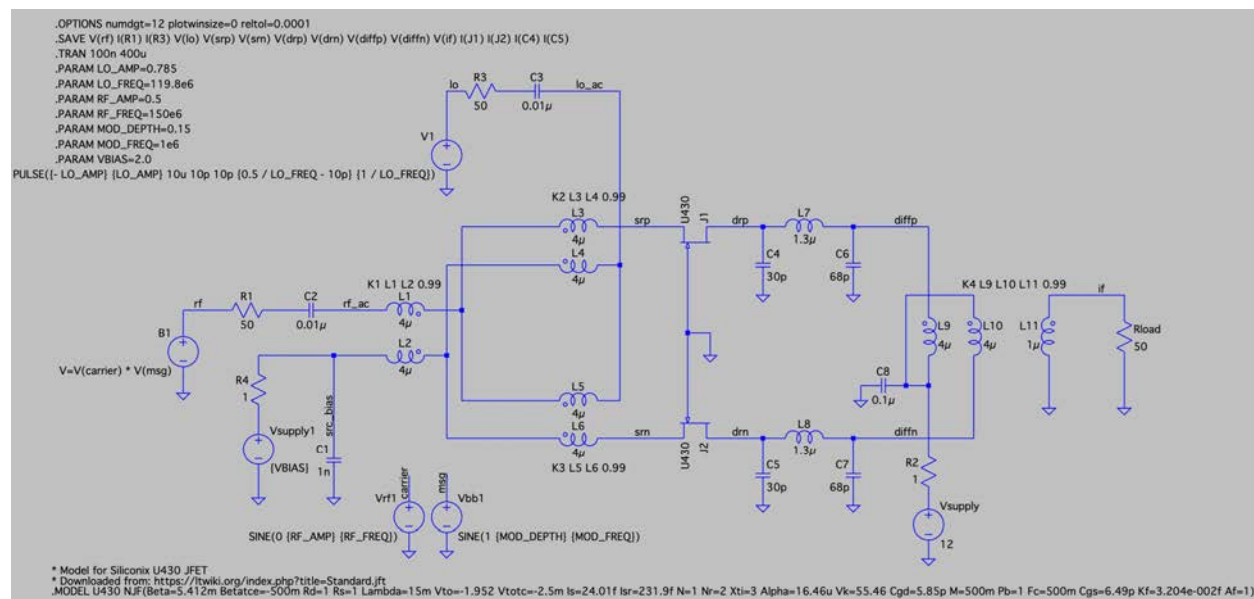


DEMAW-SIM-FIG. 7.12B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.12).

B. Simulation Results For an Input Signal Reduced by 6 dB

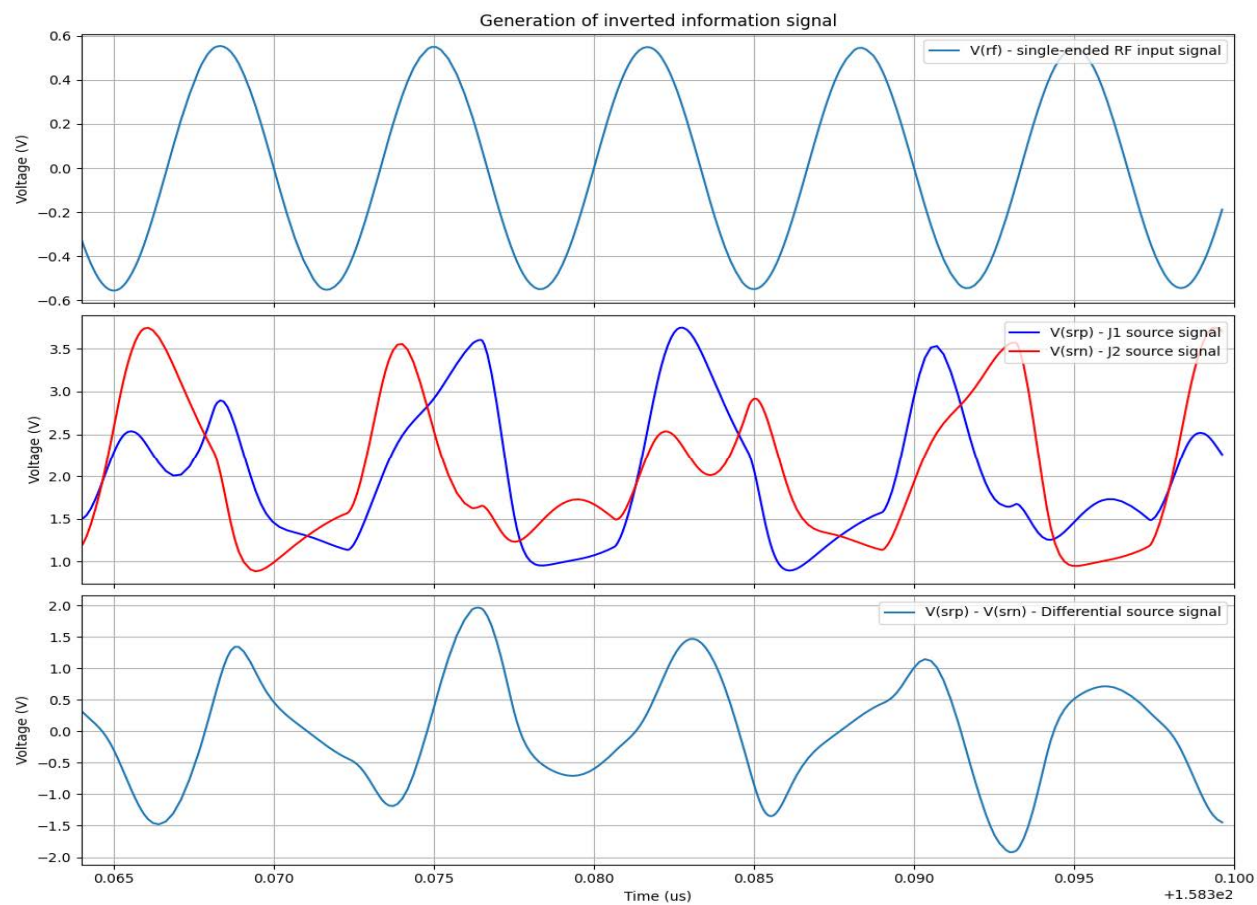
90. DEMAW-SIM-FIG. 1.13. DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 6 dB. I have created additional figures DEMAW-SIM-FIGS. 4.13, 5.13, 6.13, 7.13A and 7.13B based on simulation output from DEMAW-SIM-FIG. 1.13. DEMAW-SIM-FIGS. 4.13, 5.13, 6.13, 7.13A and 7.13B show the same simulation output from DEMAW-SIM-FIG. 1.13 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-

SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMA-SIM-FIGS. 1.13, 4.13, 5.13, 6.13, 7.13A and 7.13B.



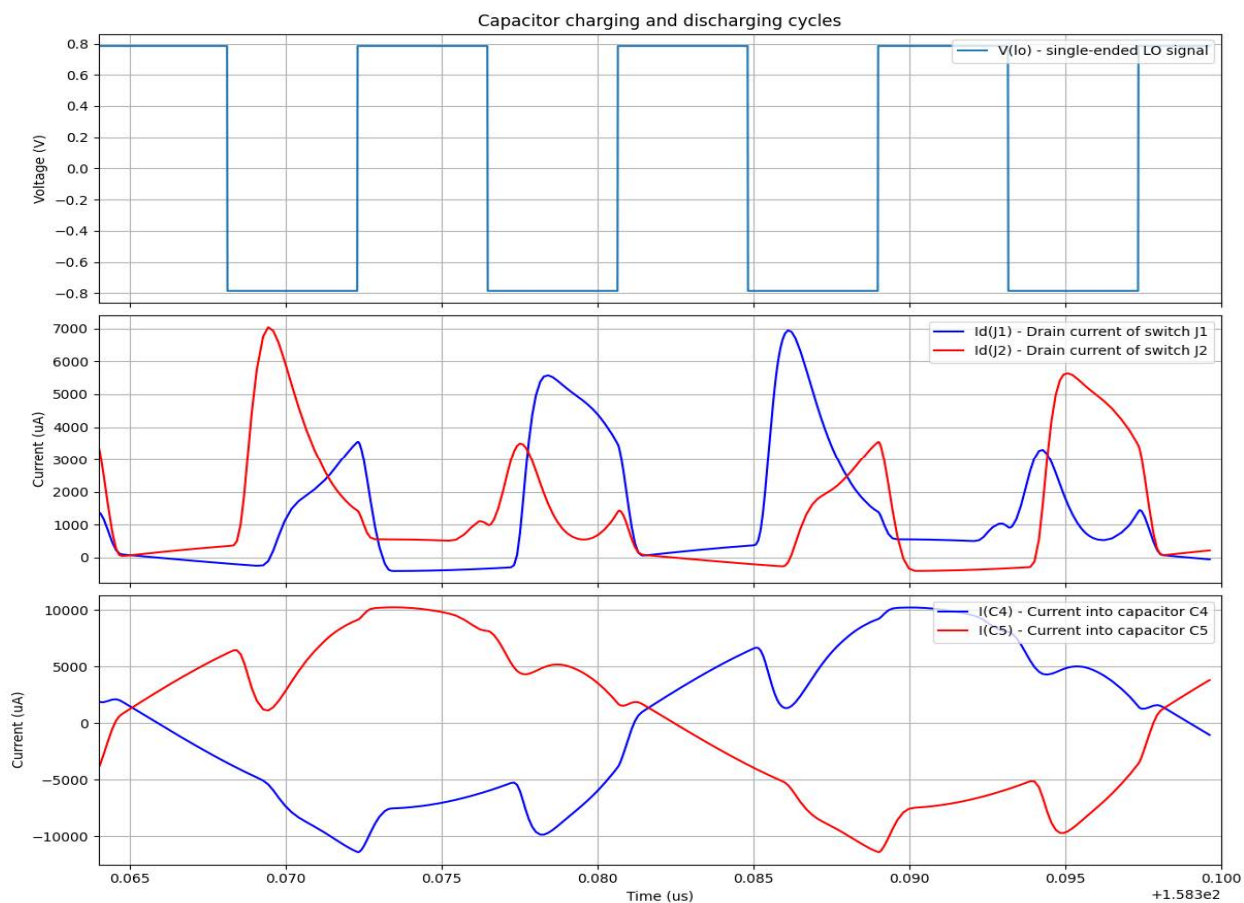
DEMAW-SIM-FIG. 1.13. DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 6 dB.

91. DEMA-SIM-FIG. 4.13 is a graphical representation of the generation of inverted information signal for the circuit of DEMA-SIM-FIG. 1.13.



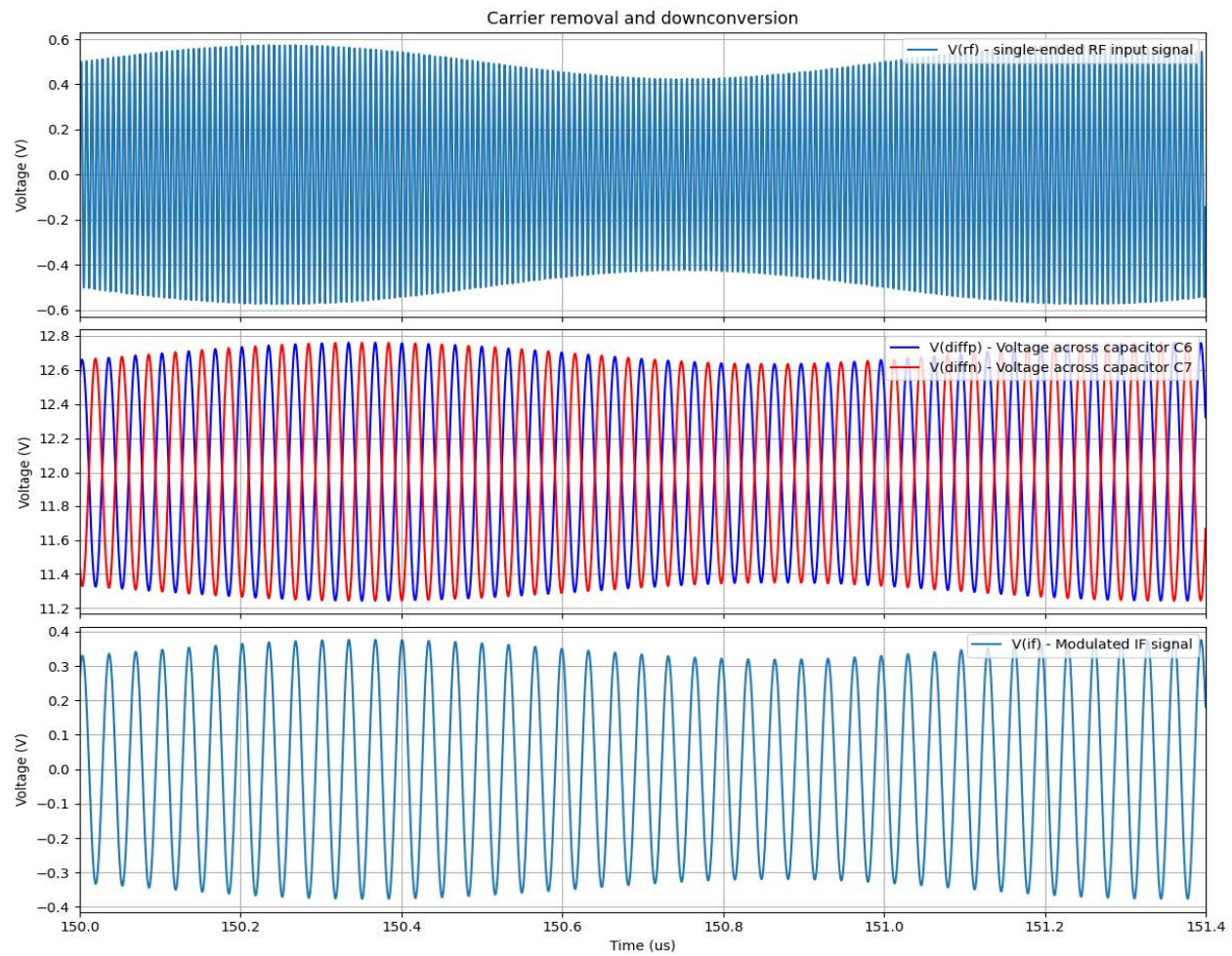
DEMAW-SIM-FIG. 4.13. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.13).

92. DEMAW-SIM-FIG. 5.13 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.13.



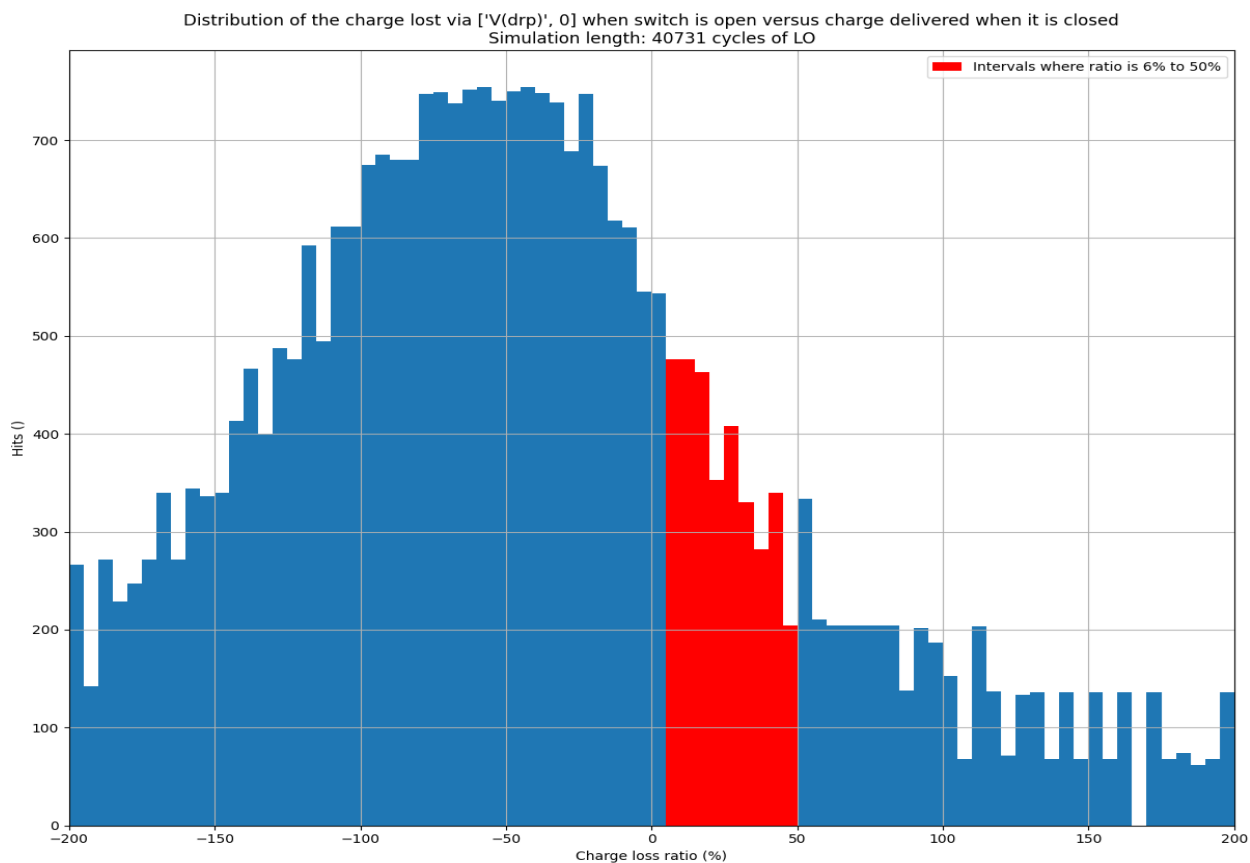
DEMAW-SIM-FIG. 5.13. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.13).

93. DEMAW-SIM-FIG. 6.13 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.13.



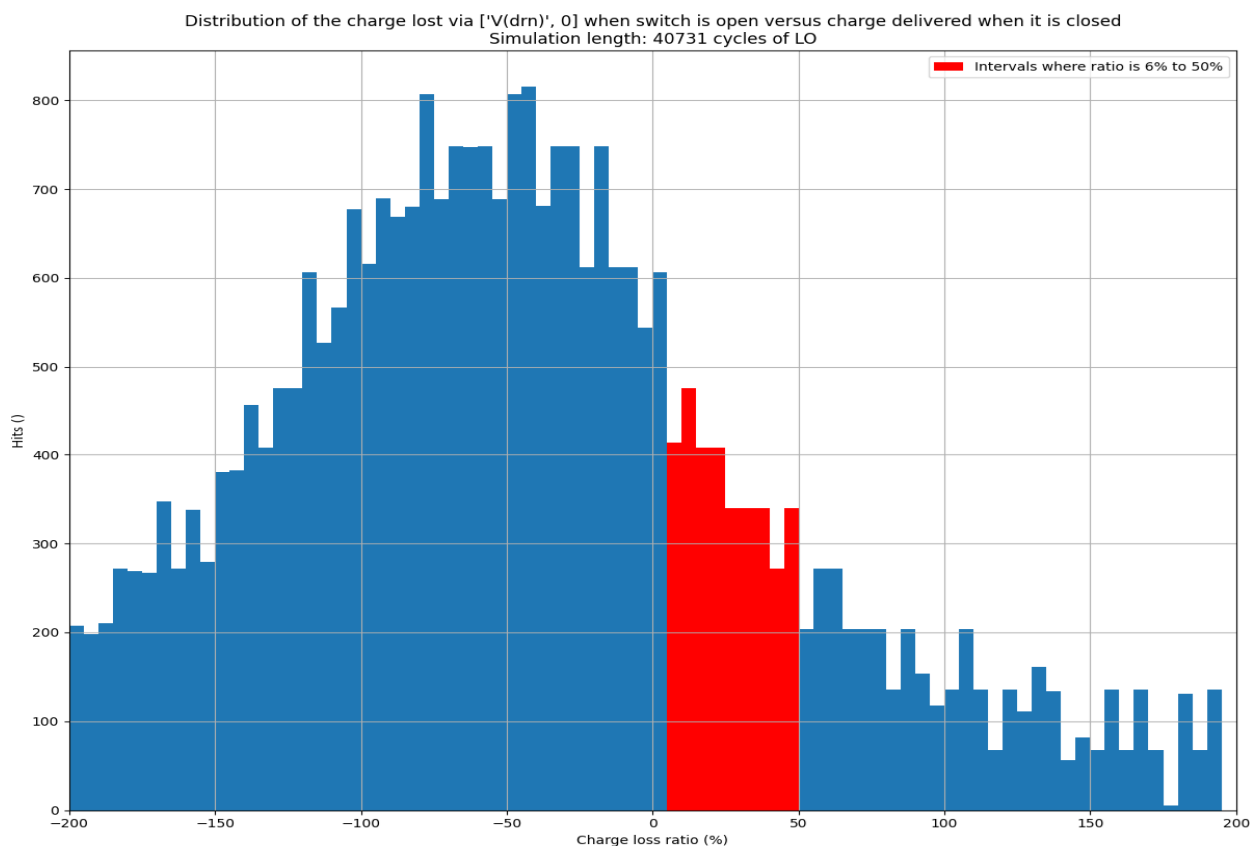
DEMAW-SIM-FIG. 6.13. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.13).

94. DEMAW-SIM-FIG. 7.13A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.13.



DEMAW-SIM-FIG. 7.13A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.13).

95. DEMAW-SIM-FIG. 7.13B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.13.

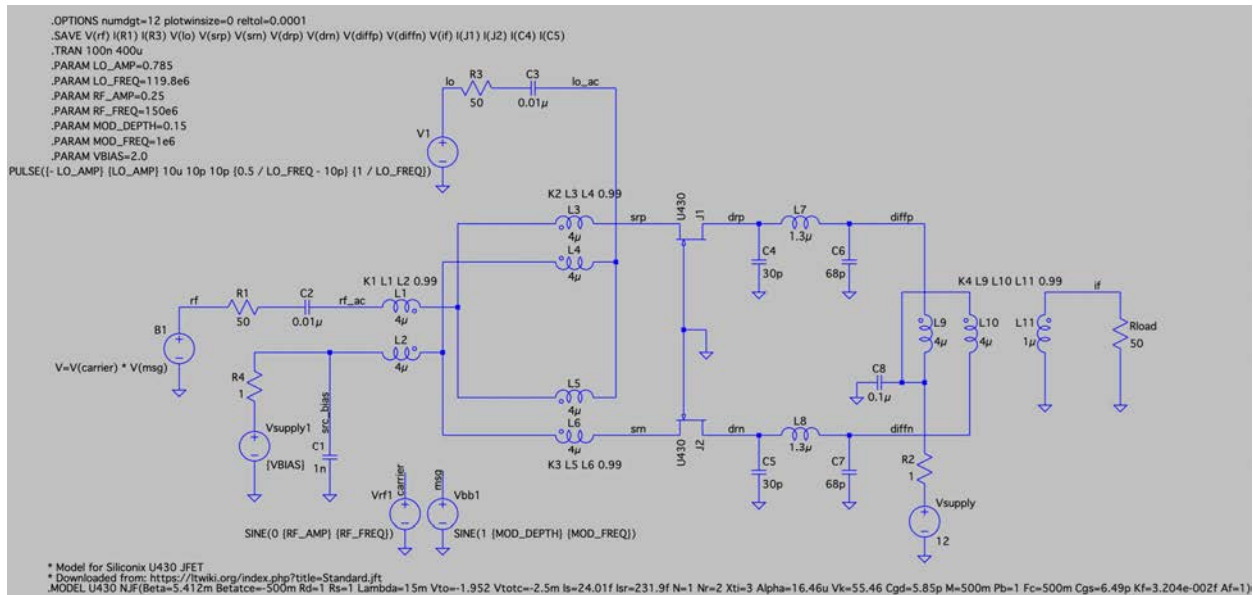


DEMAW-SIM-FIG. 7.13B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.13).

C. Simulation Results For an Input Signal Reduced by 12 dB

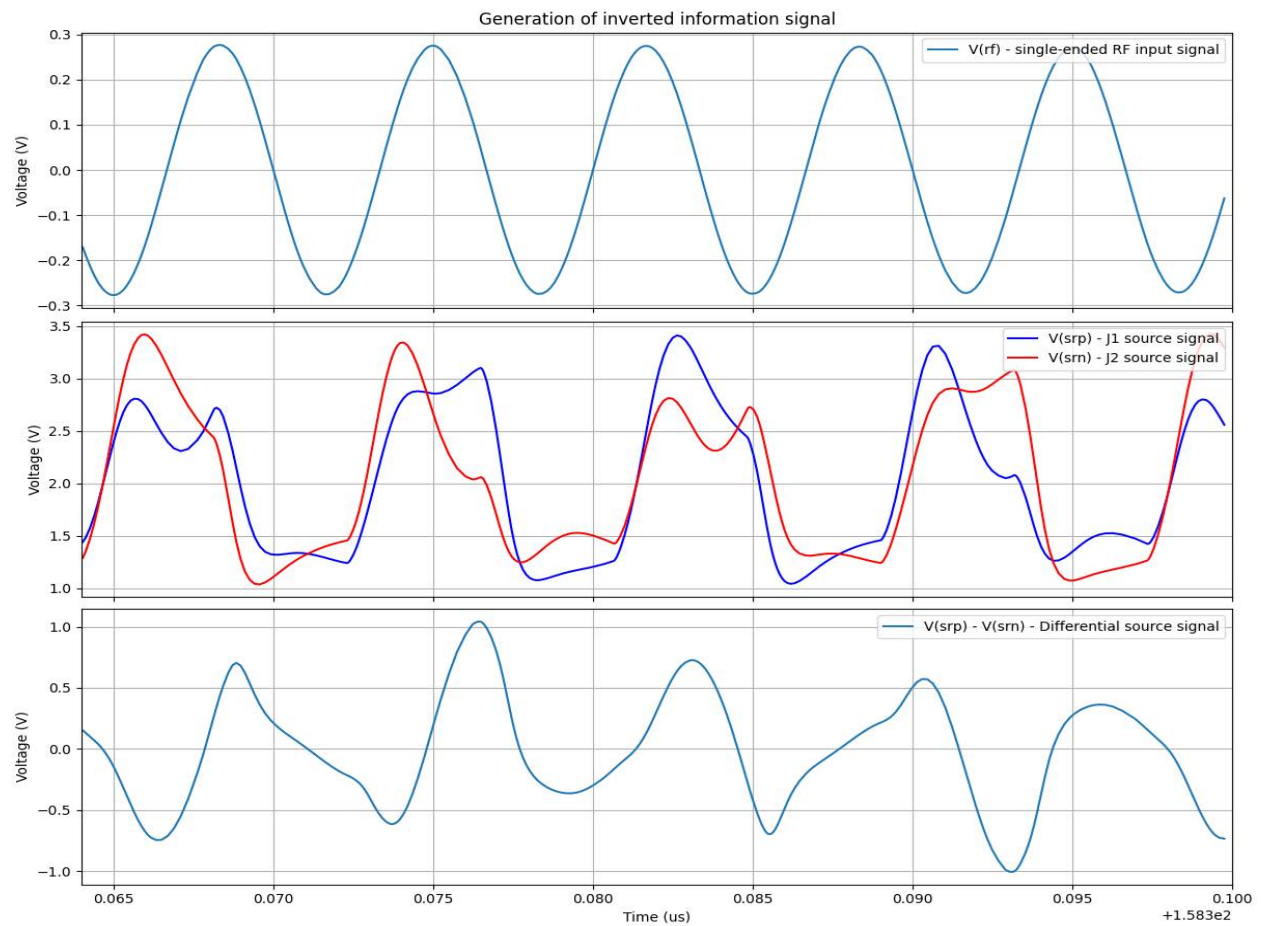
96. DEMAW-SIM-FIG. 1.14 is a schematic diagram of the simulated DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 12 dB. I have created additional figures DEMAW-SIM-FIGS. 4.14, 5.14, 6.14, 7.14A and 7.14B based on simulation output from DEMAW-SIM-FIG. 1.14. DEMAW-SIM-FIGS. 4.14, 5.14, 6.14, 7.14A and 7.14B show the same simulation output from DEMAW-SIM-FIG. 1.14 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding

the claims based on DEMA-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMA-SIM-FIGS. 1.14, 4.14, 5.14, 6.14, 7.14A and 7.14B.



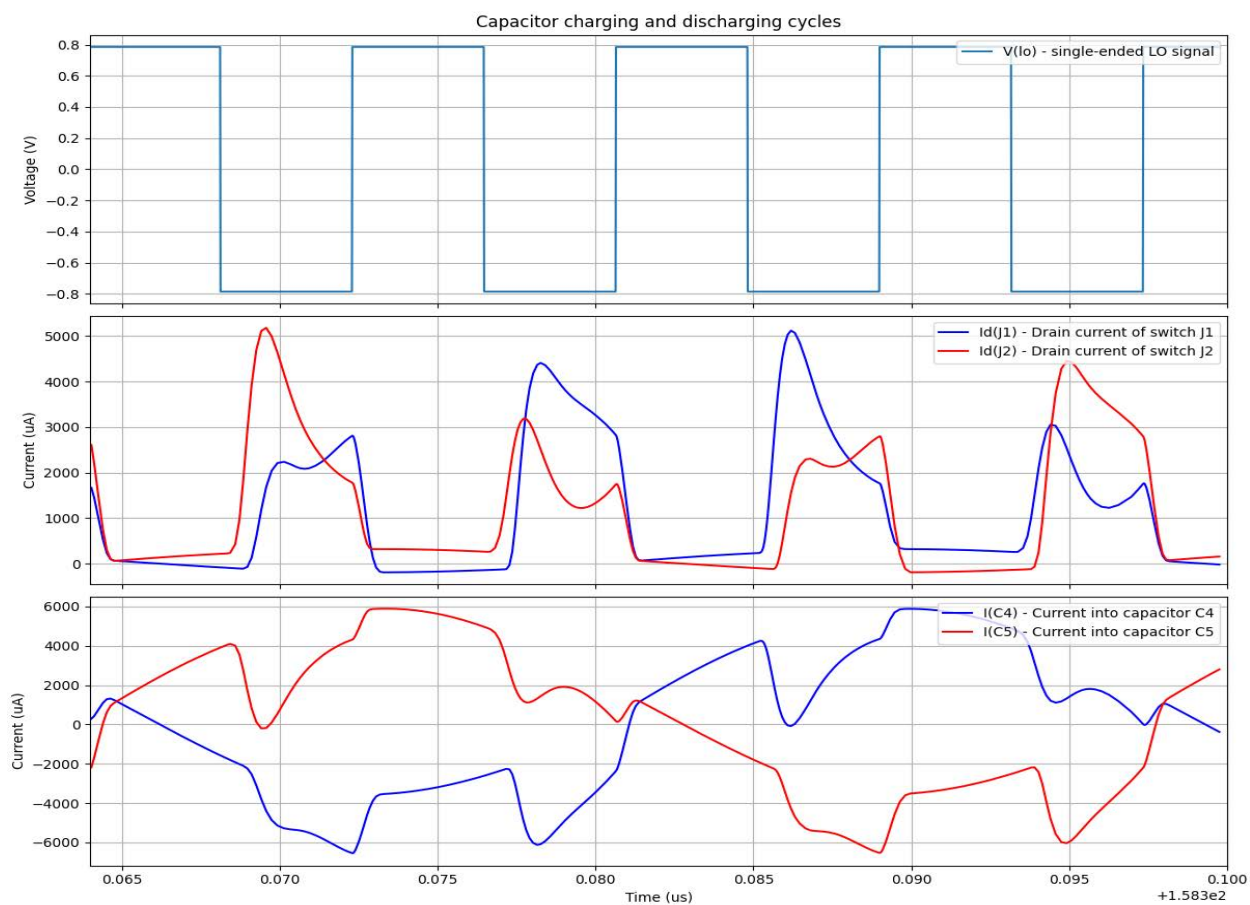
DEMAW-SIM-FIG. 1.14. DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 12 dB.

97. DEMA-SIM-FIG. 4.14 is a graphical representation of the generation of inverted information signal for the circuit of DEMA-SIM-FIG. 1.14.



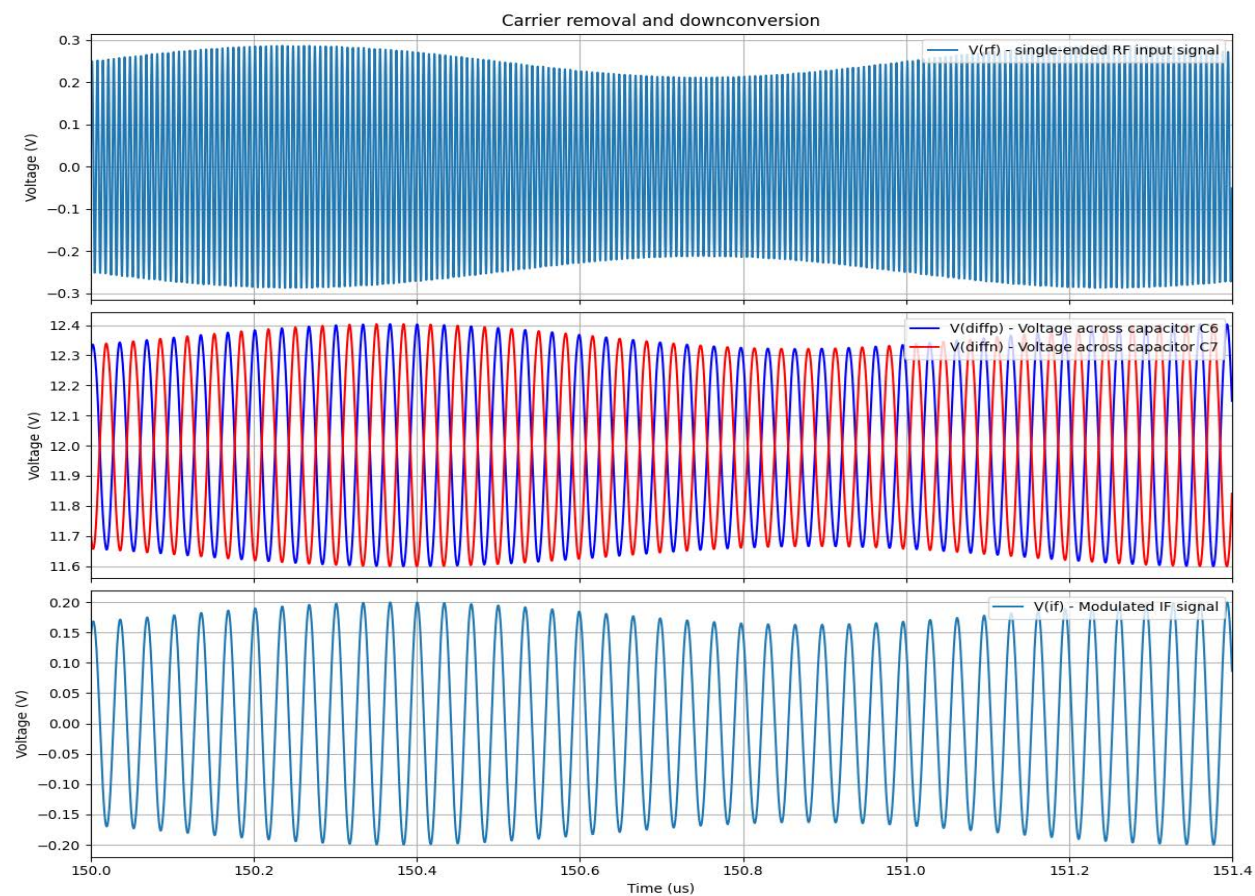
DEMAW-SIM-FIG. 4.14. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.14).

98. DEMAW-SIM-FIG. 5.14 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.14.



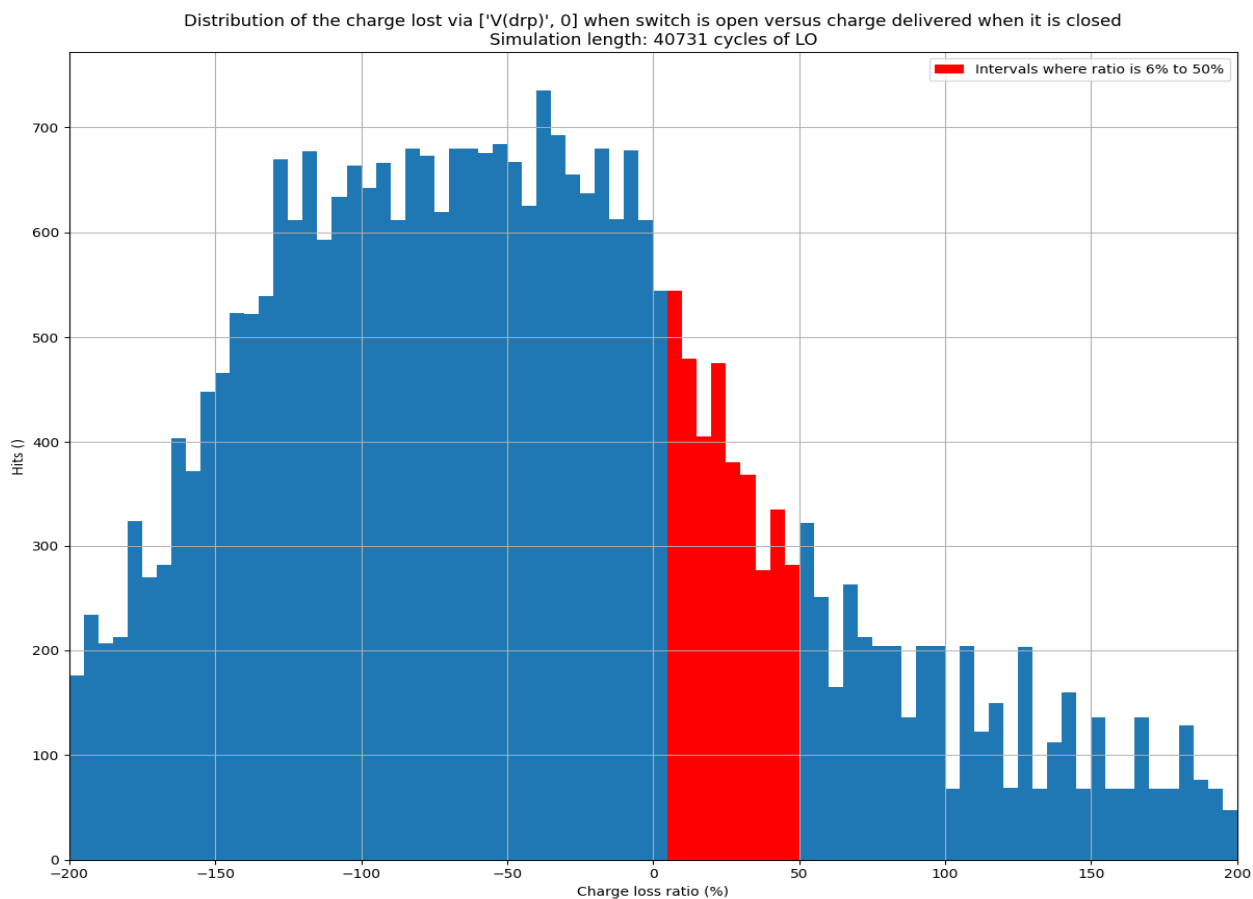
DEMAW-SIM-FIG. 5.14. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.14).

99. DEMAW-SIM-FIG. 6.14 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.14.



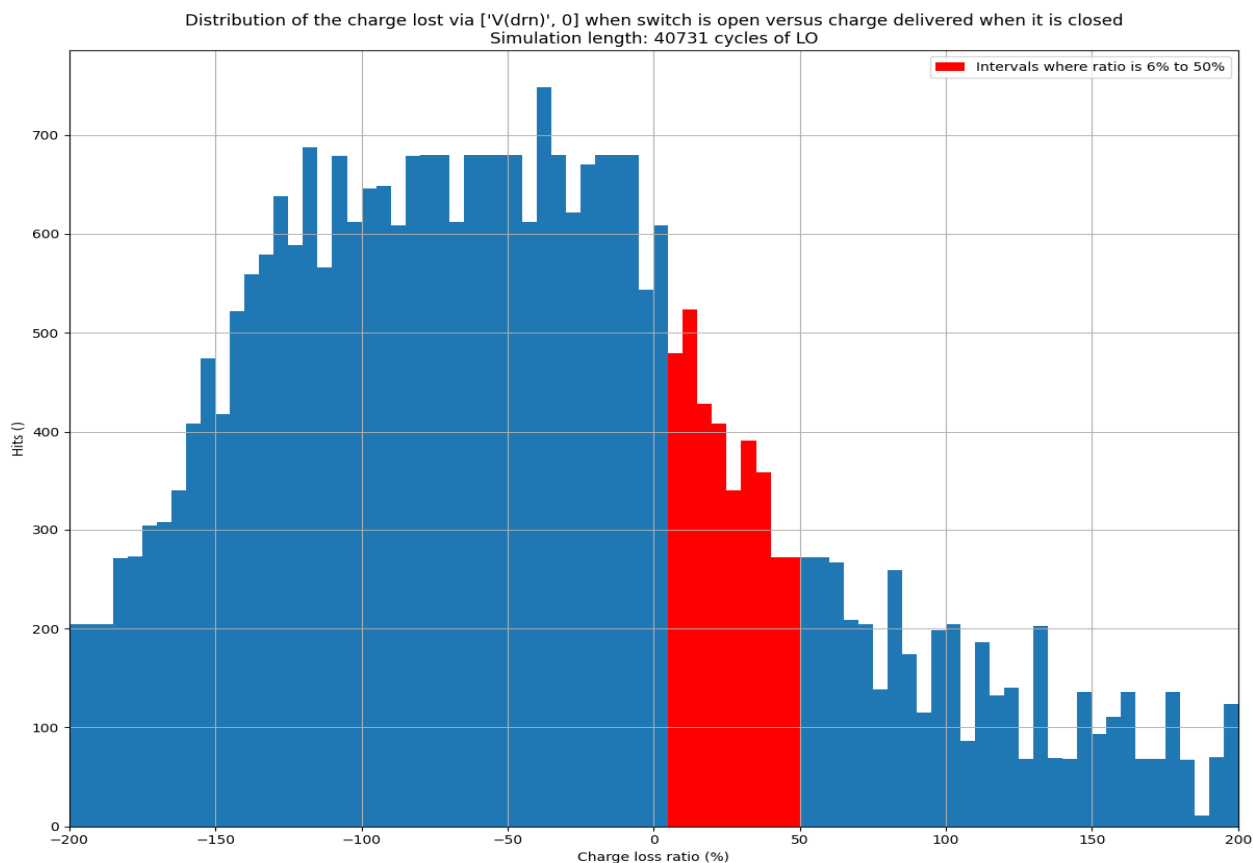
DEMAW-SIM-FIG. 6.14. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.14).

100. DEMAW-SIM-FIG. 7.14A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.14.



DEMAW-SIM-FIG. 7.14A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.14).

101. DEMAW-SIM-FIG. 7.14B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.14.

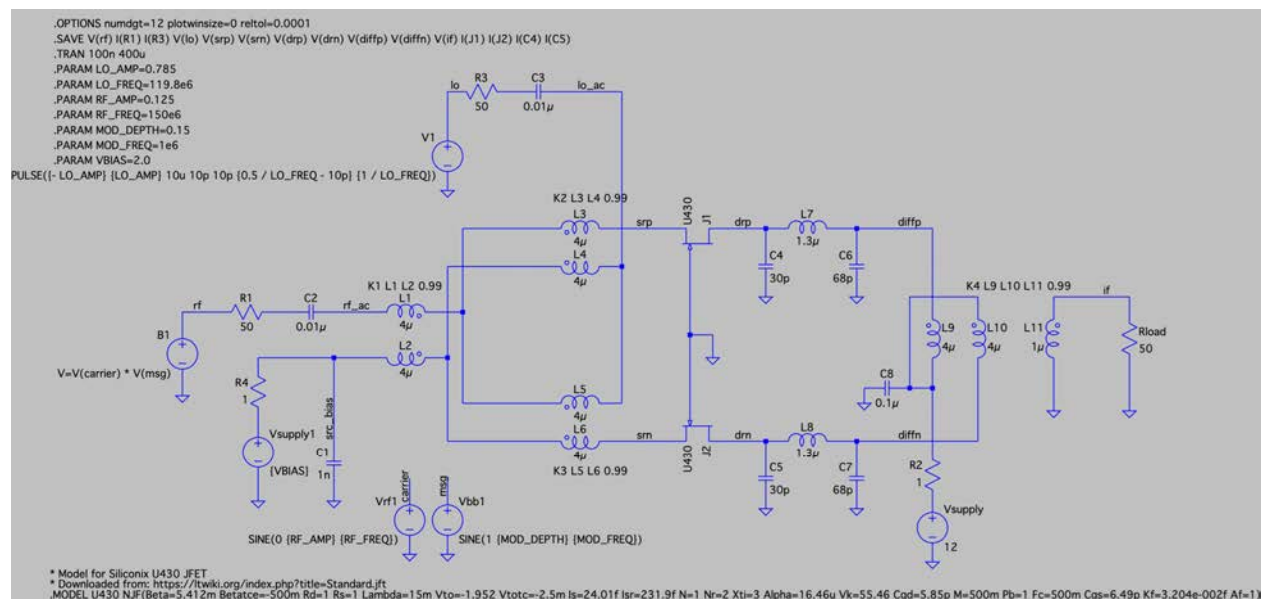


DEMAW-SIM-FIG. 7.14B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.14).

D. Simulation Results For an Input Signal Reduced by 18 dB

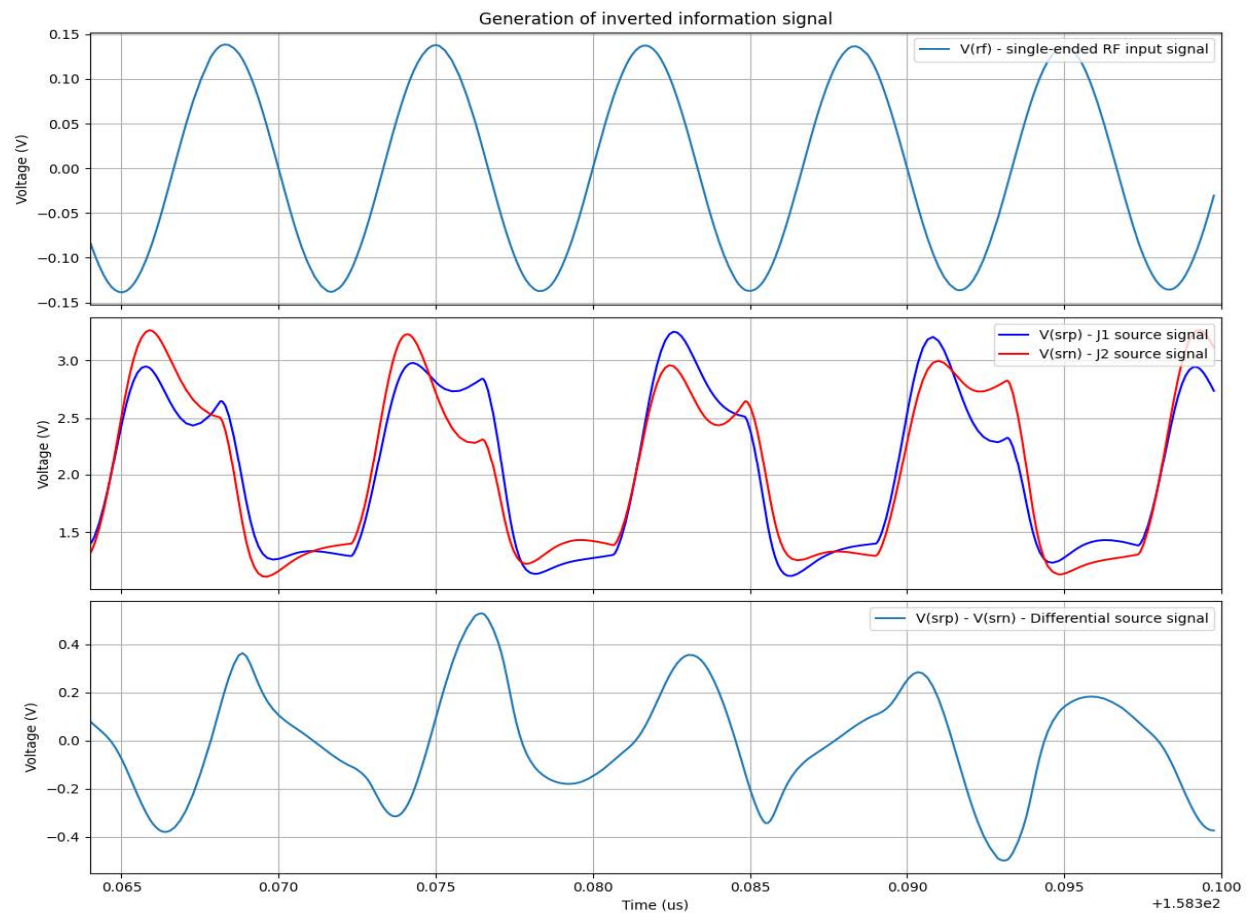
102. DEMAW-SIM-FIG. 1.15 is a schematic diagram of the simulated DeMaw FIG. 6.7 circuit modified to match Oxner with a squared-up LO and input signal reduced by 18 dB. I have created additional figures DEMAW-SIM-FIGS. 4.15, 5.15, 6.15, 7.15A and 7.15B based on simulation output from DEMAW-SIM-FIG. 1.15. DEMAW-SIM-FIGS. 4.15, 5.15, 6.15, 7.15A and 7.15B show the same simulation output from DEMAW-SIM-FIG. 1.15 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMAU-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAU-SIM-FIGS. 1.15, 4.15, 5.15, 6.15, 7.15A and 7.15B.



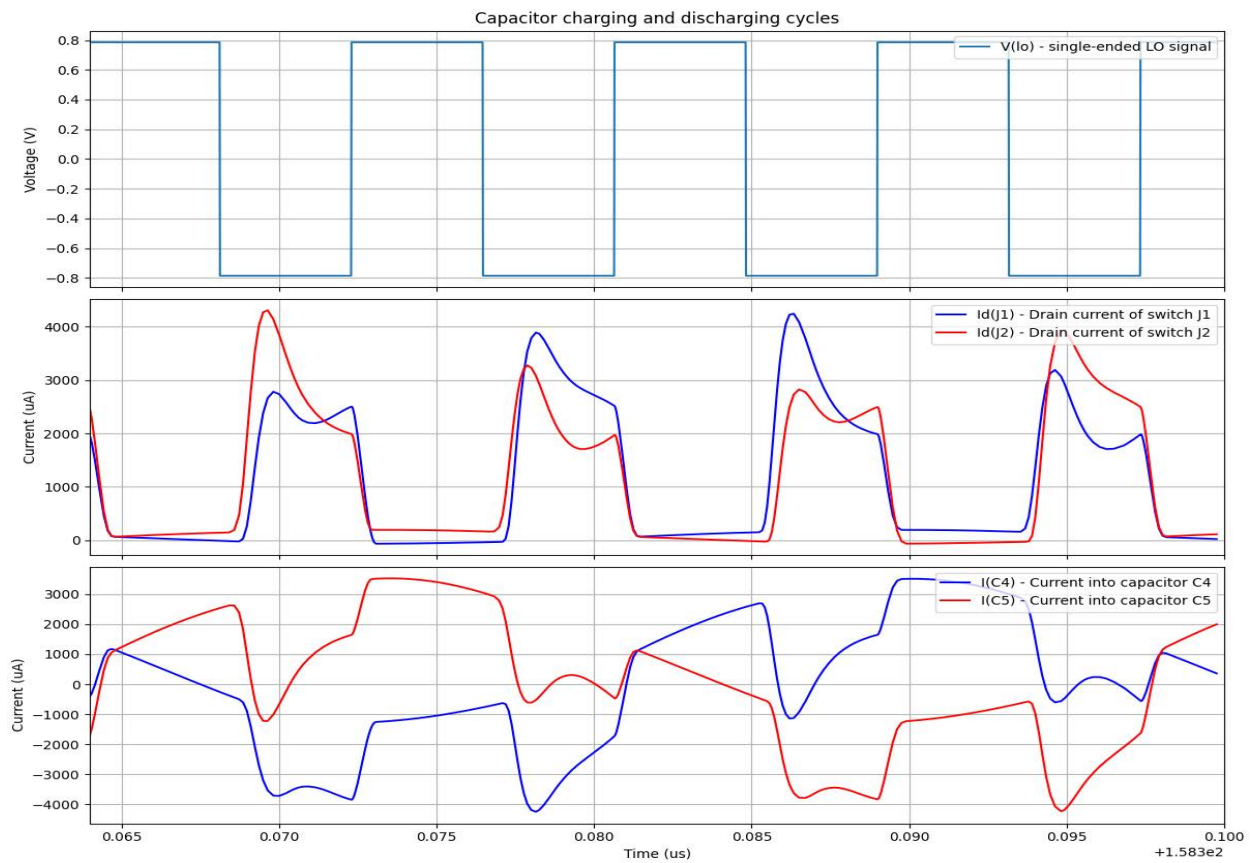
DEMAU-SIM-FIG. 1.15. DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 18 dB.

103. DEMAU-SIM-FIG. 4.15 is a graphical representation of the generation of inverted information signal for the circuit of DEMAU-SIM-FIG. 1.15.



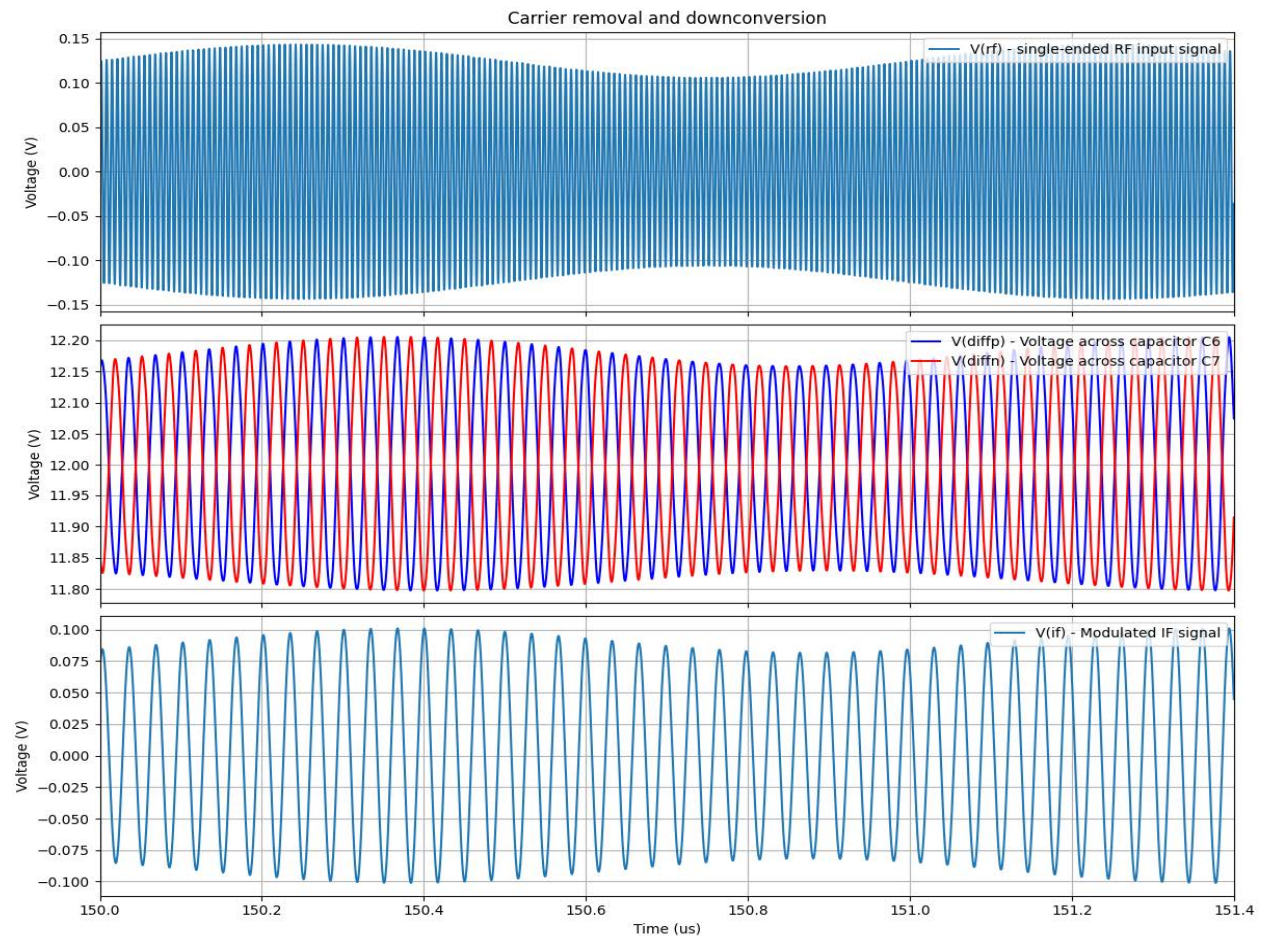
DEMAW-SIM-FIG. 4.15. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.15).

104. DEMAW-SIM-FIG. 5.15 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.15.



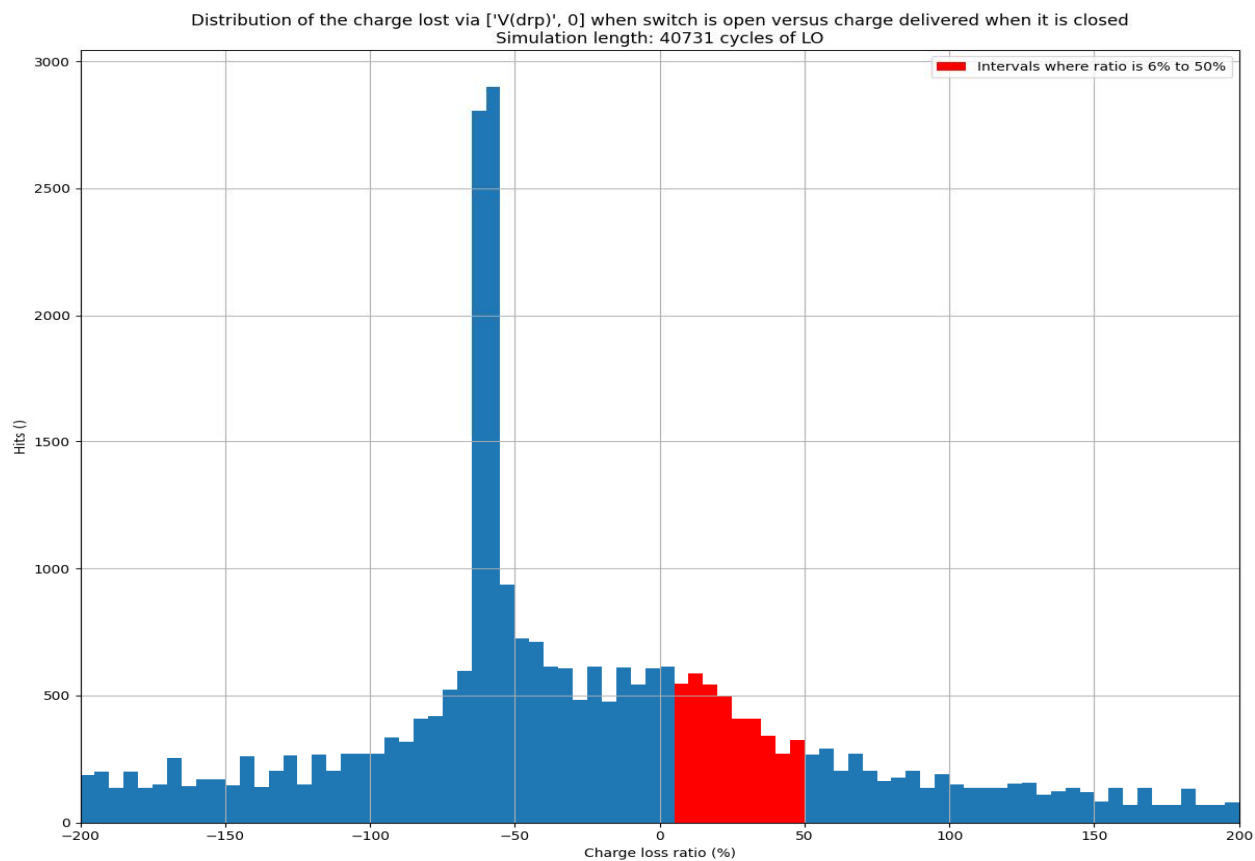
DEMAW-SIM-FIG. 5.15. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.15).

105. DEMAW-SIM-FIG. 6.15 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.15.



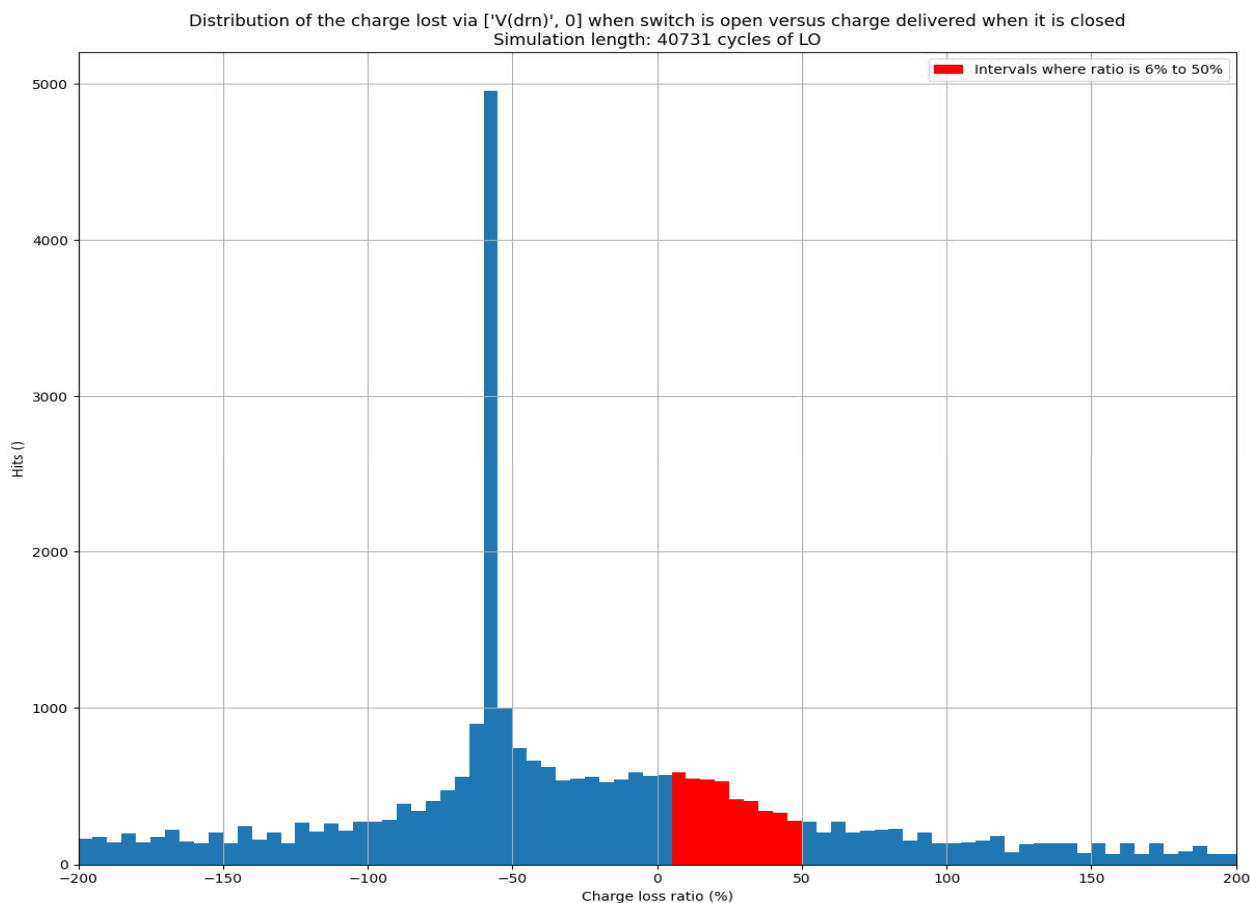
DEMAW-SIM-FIG. 6.15. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.15).

106. DEMAW-SIM-FIG. 7.15A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.15.



DEMAW-SIM-FIG. 7.15A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.15).

107. DEMAW-SIM-FIG. 7.15B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.15.

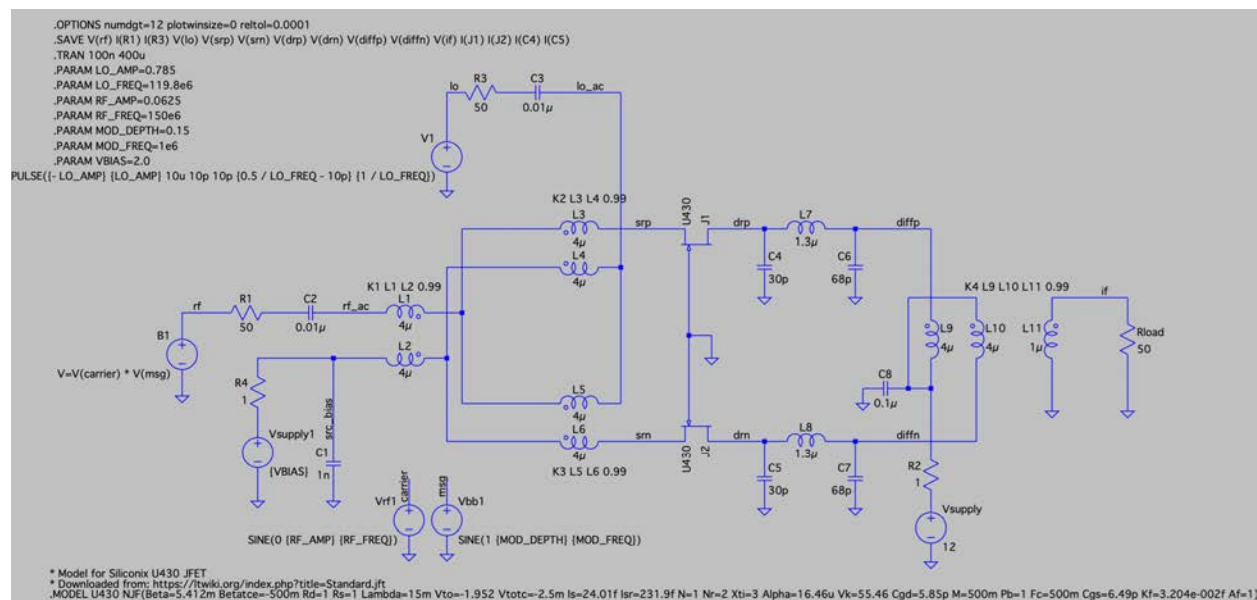


DEMAW-SIM-FIG. 7.15B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.15).

E. Simulation Results For an Input Signal Reduced by 24 dB

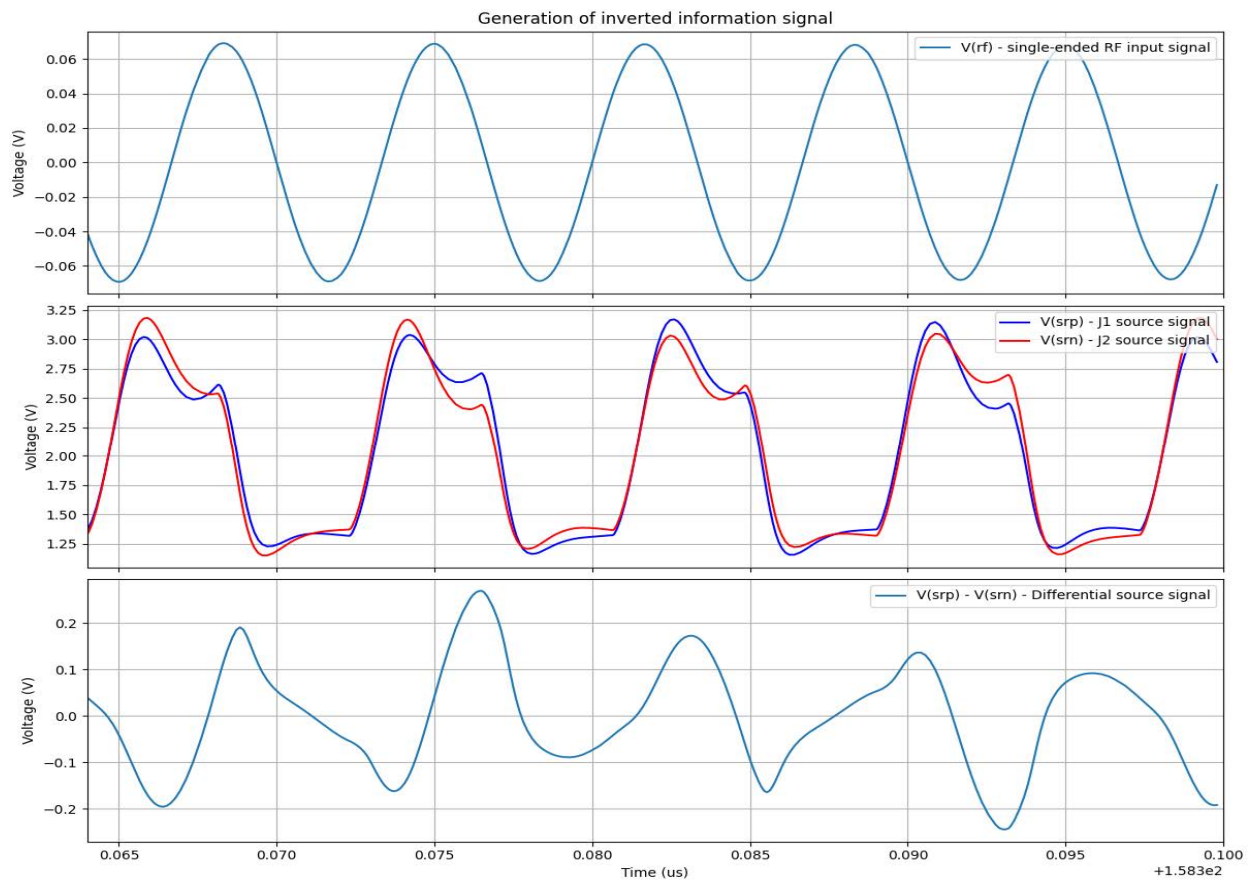
108. DEMAW-SIM-FIG. 1.16 is a schematic diagram of the simulated DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 24 dB. I have created additional figures DEMAW-SIM-FIGS. 4.16, 5.16, 6.16, 7.16A and 7.16B based on simulation output from DEMAW-SIM-FIG. 1.16. DEMAW-SIM-FIGS. 4.16, 5.16, 6.16, 7.16A and 7.16B show the same simulation output from DEMAW-SIM-FIG. 1.16 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show

from DEMA-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMA-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMA-SIM-FIGS. 1.16, 4.16, 5.16, 6.16, 7.16A and 7.16B.



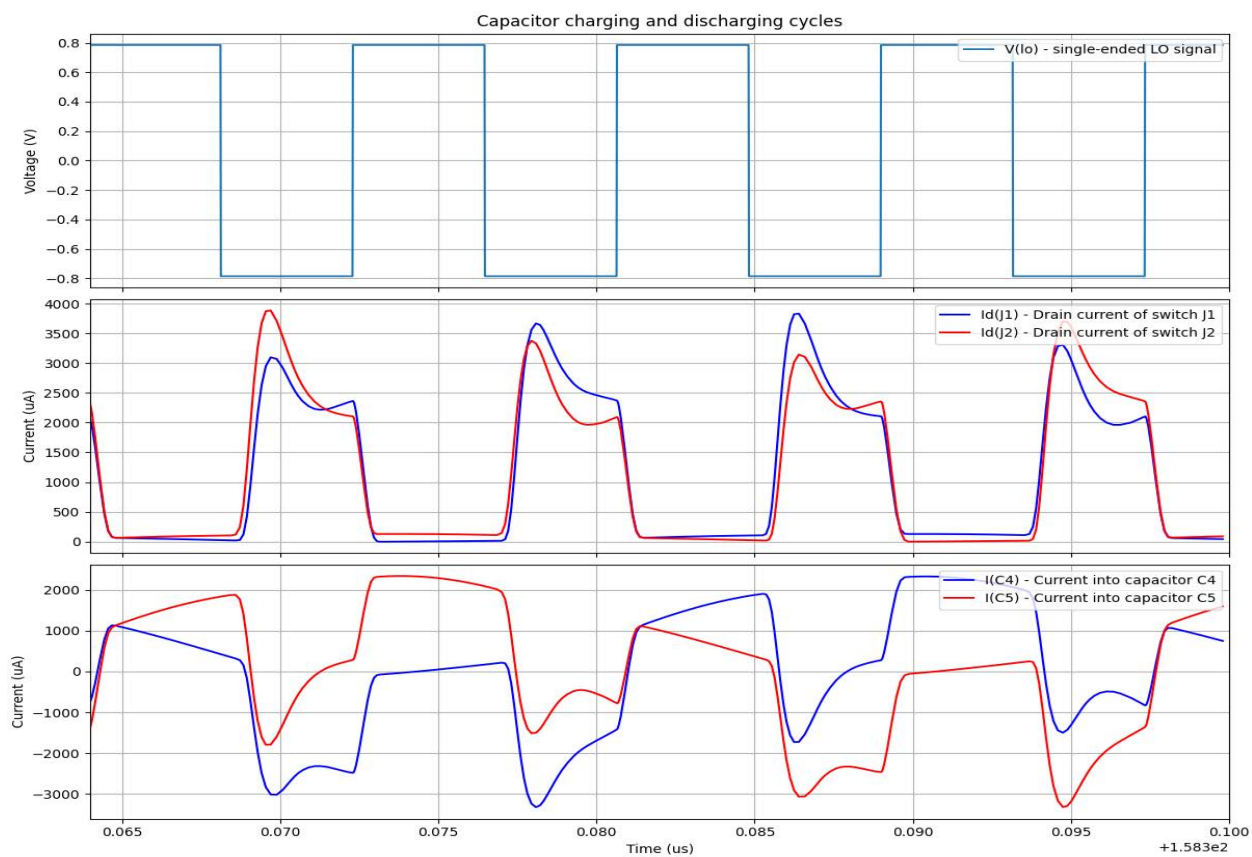
DEMA-SIM-FIG. 1.16. DeMaw circuit modified to match Oxner with a squared-up LO and input signal reduced by 24 dB.

109. DEMA-SIM-FIG. 4.16 is a graphical representation of the generation of inverted information signal for the circuit of DEMA-SIM-FIG. 1.16.



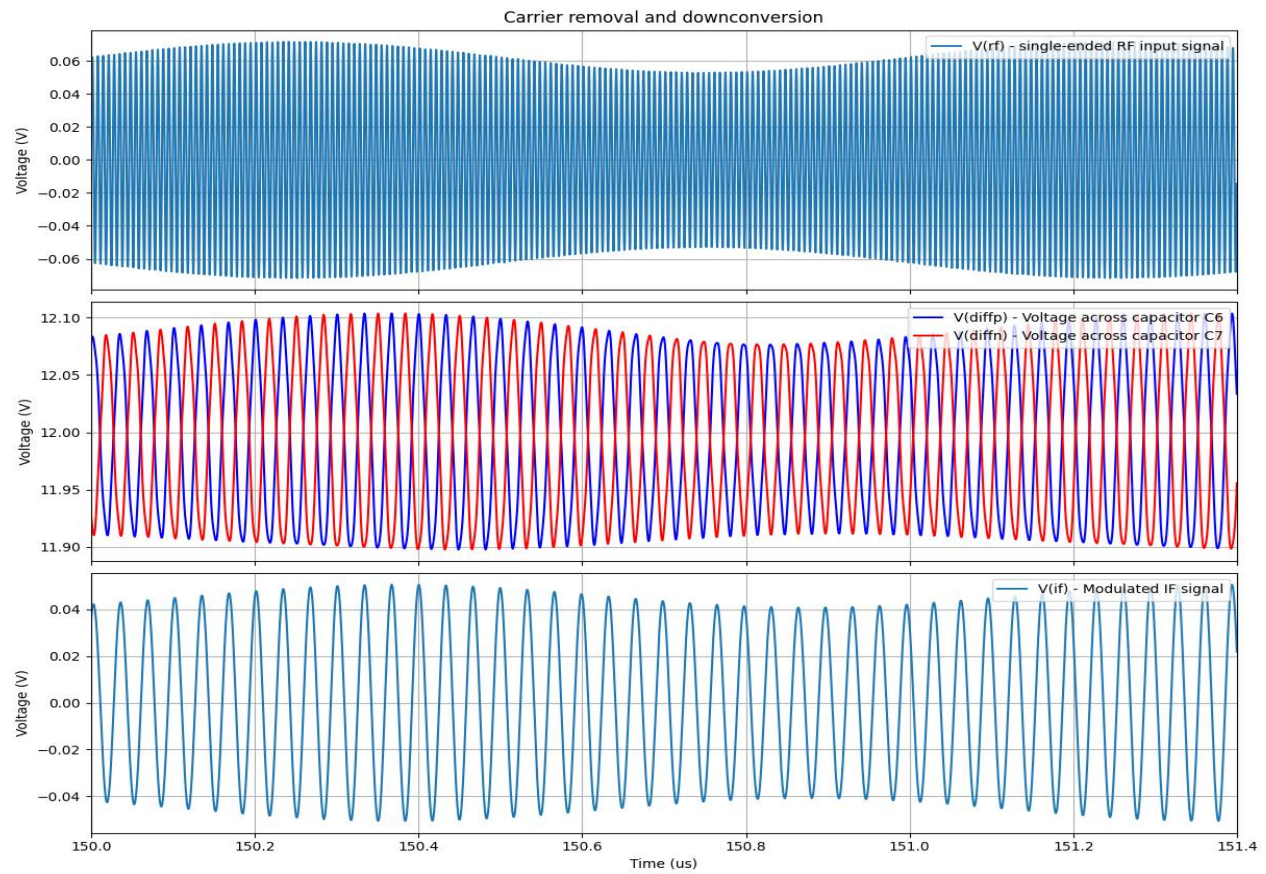
DEMAW-SIM-FIG. 4.16. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.16).

110. DEMAW-SIM-FIG. 5.16 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.16.



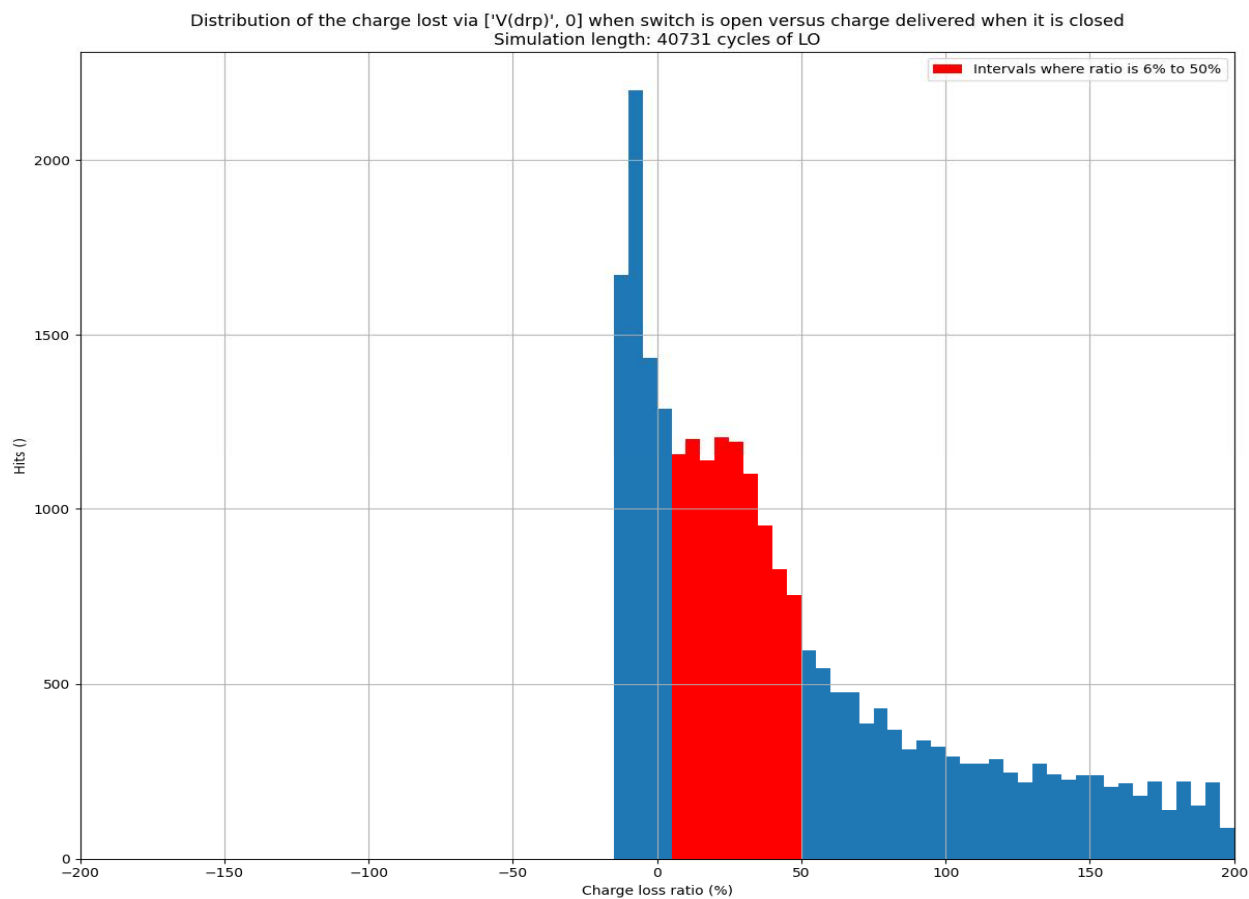
DEMAW-SIM-FIG. 5.16. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.16).

111. DEMAW-SIM-FIG. 6.16 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.16.



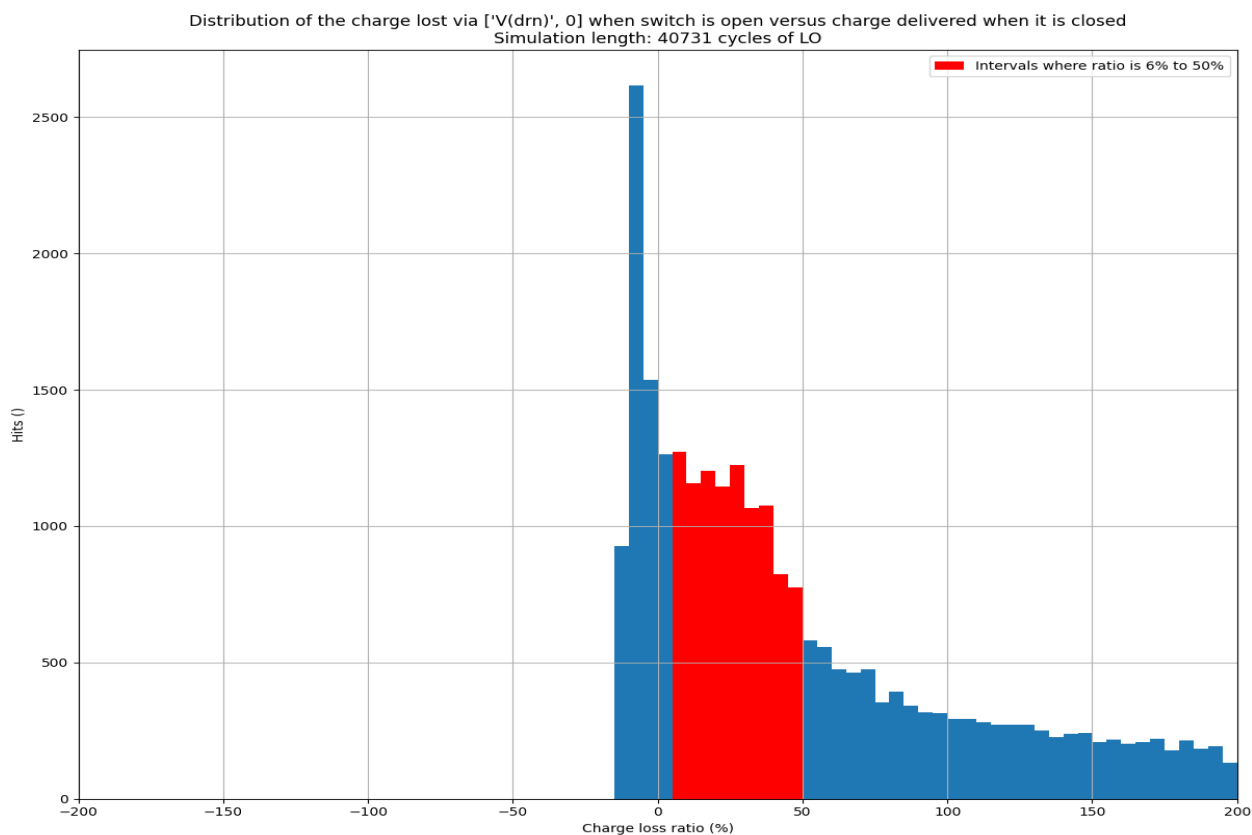
DEMAW-SIM-FIG. 6.16. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.16).

112. DEMAW-SIM-FIG. 7.16A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.16.



DEMAW-SIM-FIG. 7.16A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.16).

113. DEMAW-SIM-FIG. 7.16B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.16.



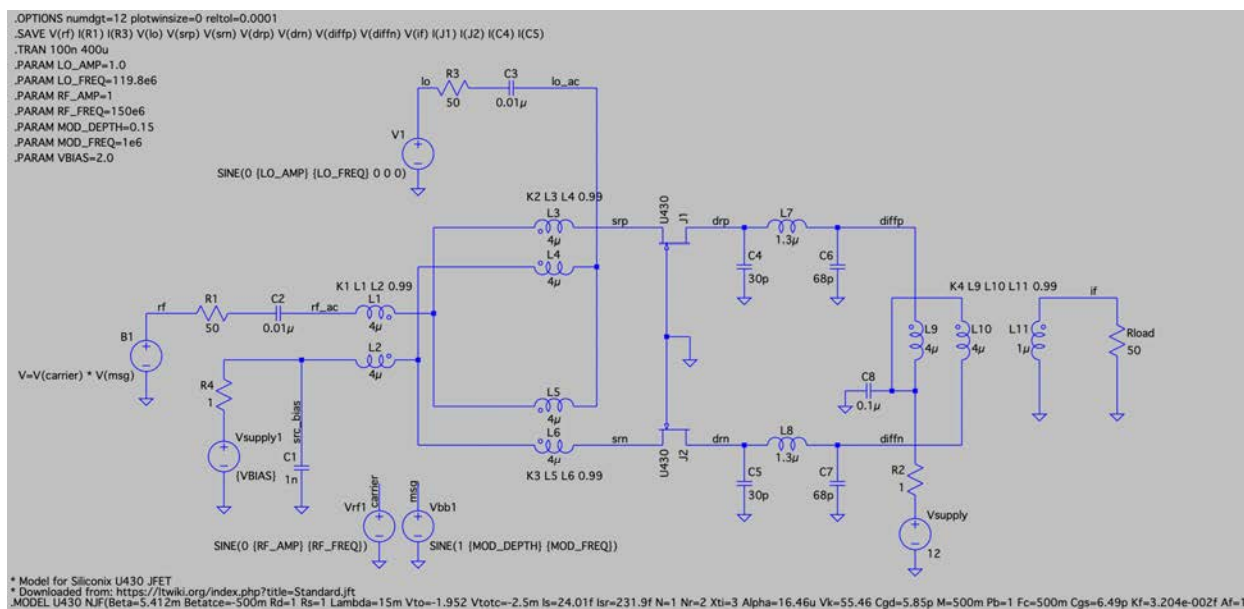
DEMAW-SIM-FIG. 7.16B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.16).

VI. DeMaw Circuit Modified to Match Oxner With a Sinusoidal LO

114. As I testified in my deposition, using sinusoidal LO signals in place of squared-up LO signals would not result in circuit behavior that would lead to different conclusions than those presented in my original Declaration, despite the POPR's false claims to the contrary. The simulation results presented in this section support my testimony. They correspond to the same circuit and input conditions as those for the simulation results presented in Section V except with a sinusoidal LO in place of a squared-up LO.

A. Simulation Results For a Large Input Signal

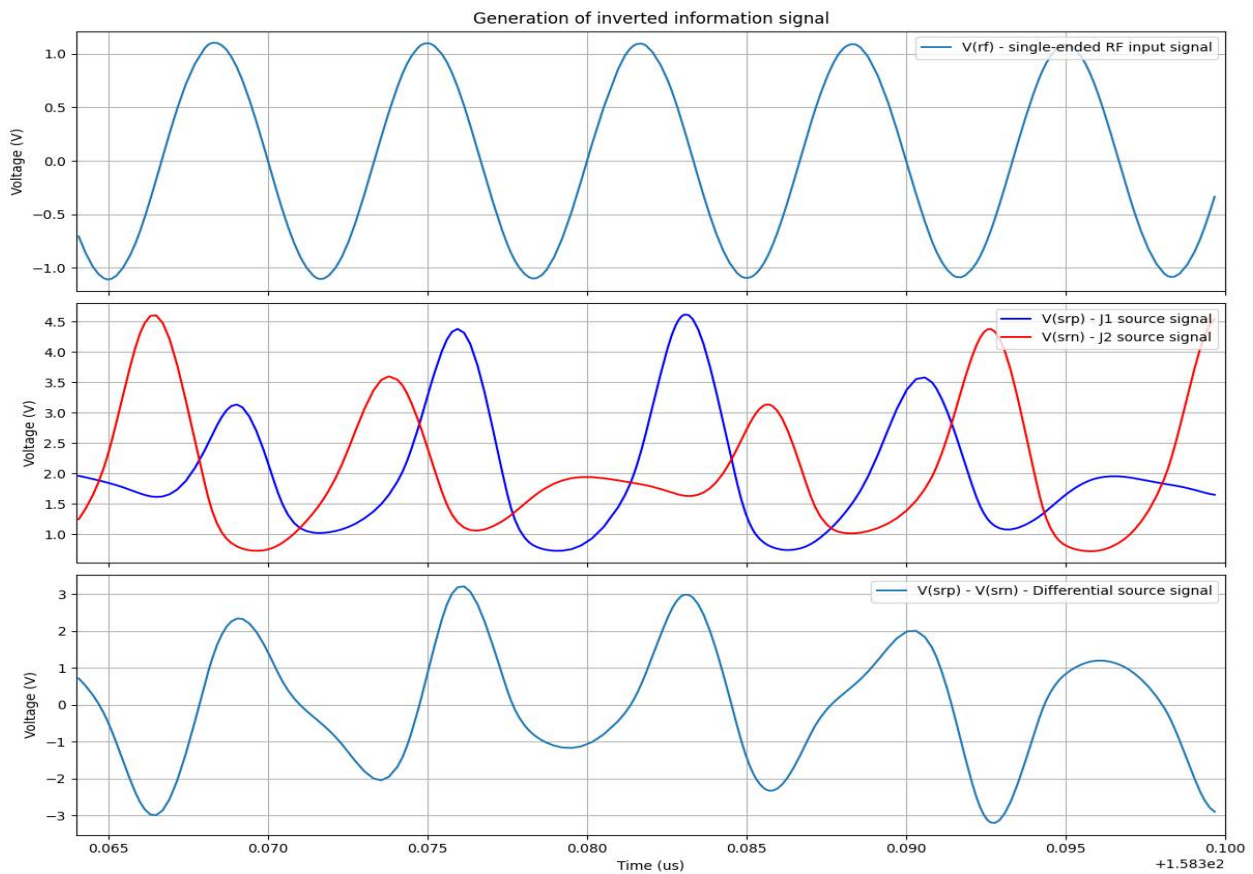
115. DEMAW-SIM-FIG. 1.17 is a schematic diagram of the DeMaw circuit modified to match Oxner with a sinusoidal LO and a large input signal. I have created additional figures DEMAW-SIM-FIGS. 4.17, 5.17, 6.17, 7.17A and 7.17B based on simulation output from DEMAW-SIM-FIG. 1.17. DEMAW-SIM-FIGS. 4.17, 5.17, 6.17, 7.17A and 7.17B show the same simulation output from DEMAW-SIM-FIG. 1.17 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on DEMAW-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMAW-SIM-FIGS. 1.17, 4.17, 5.17, 6.17, 7.17A and 7.17B.



DEMAW-SIM-FIG. 1.17. DeMaw circuit modified to match Oxner with a sinusoidal LO and a large input signal.

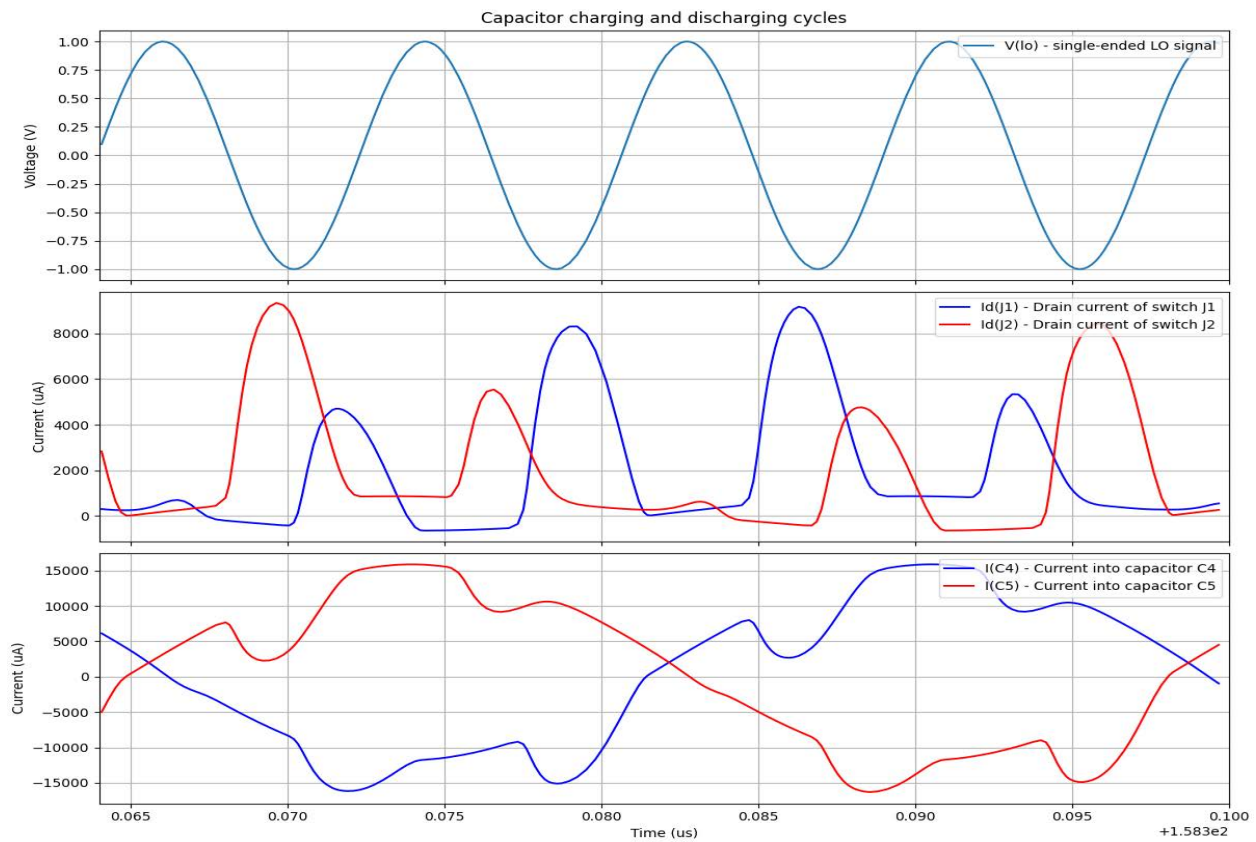
116. DEMAW-SIM-FIG. 4.17 is a graphical representation of the generation

of inverted information signal for the circuit of DEMAW-SIM-FIG. 1.17.



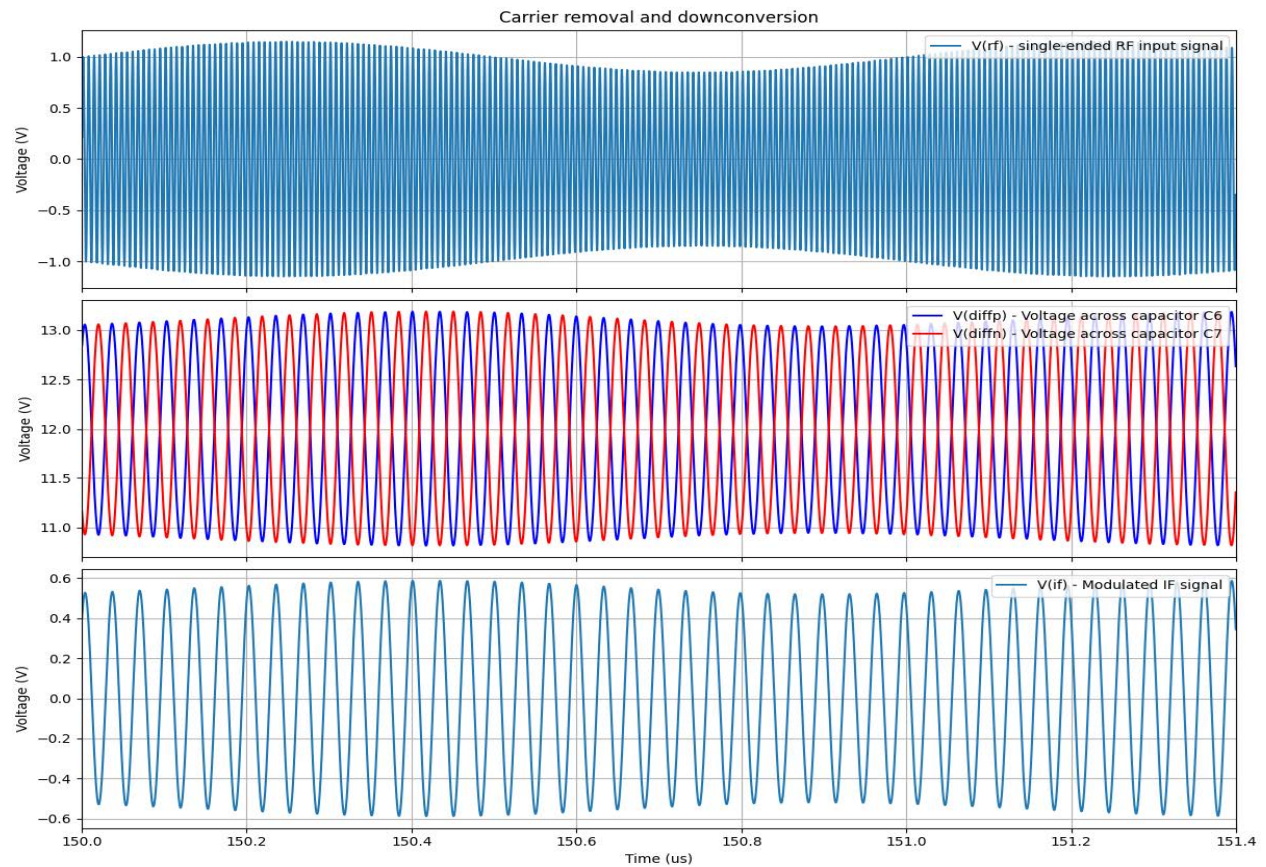
DEMAW-SIM-FIG. 4.17. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.17).

117. DEMAW-SIM-FIG. 5.17 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.17.



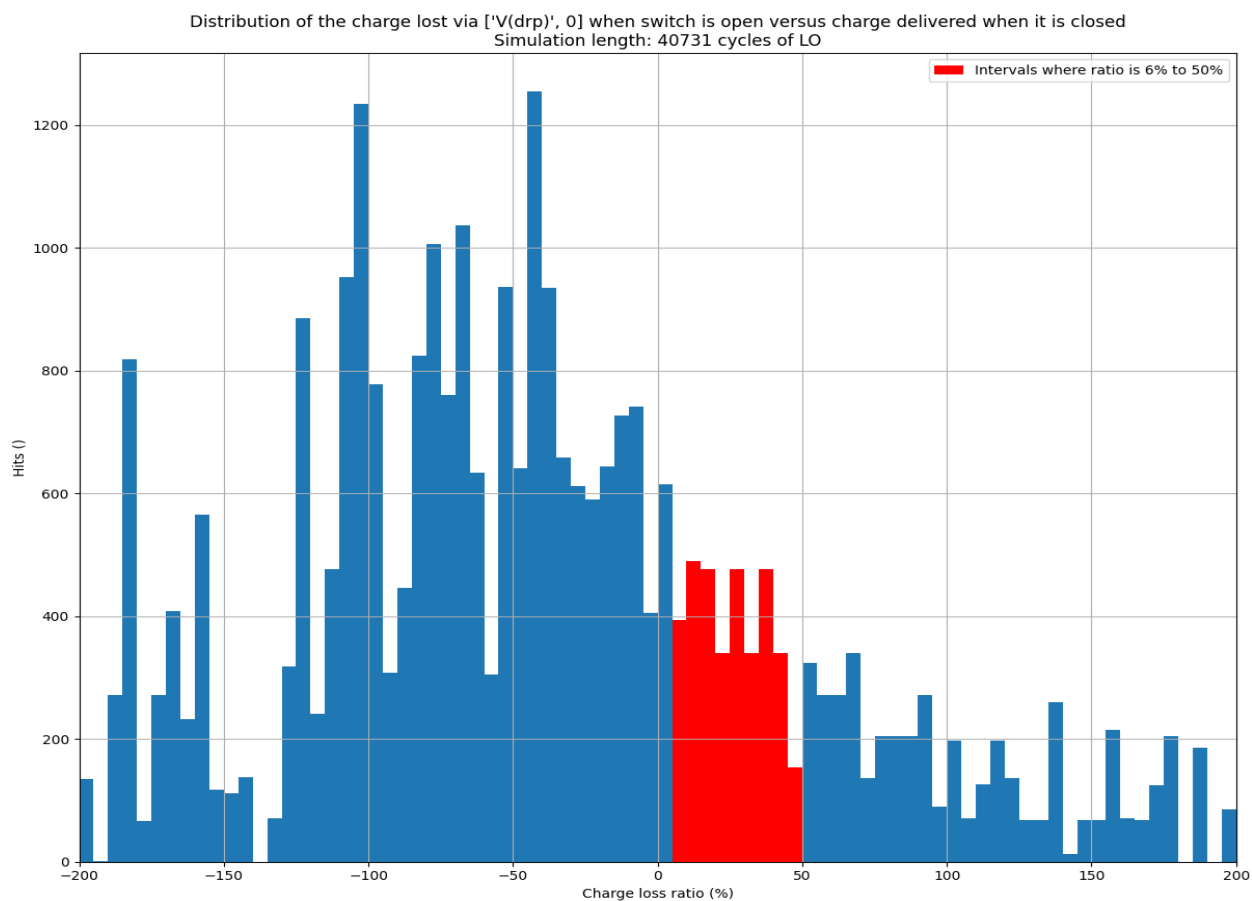
DEMAW-SIM-FIG. 5.17. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.17).

118. DEMAW-SIM-FIG. 6.17 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.17.



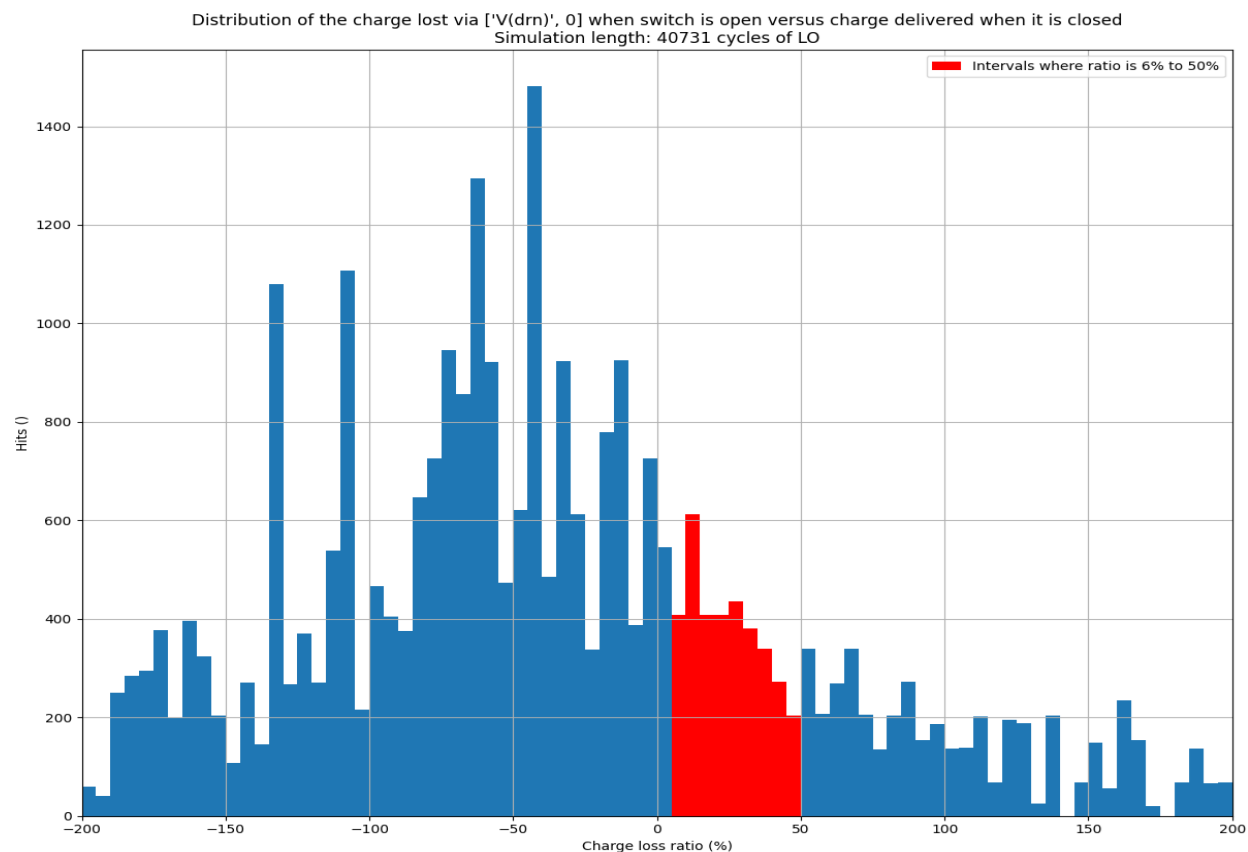
DEMAW-SIM-FIG. 6.17. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.17).

119. DEMAW-SIM-FIG. 7.17A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.17.



DEMAW-SIM-FIG. 7.17A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.17).

120. DEMAW-SIM-FIG. 7.17B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.17.

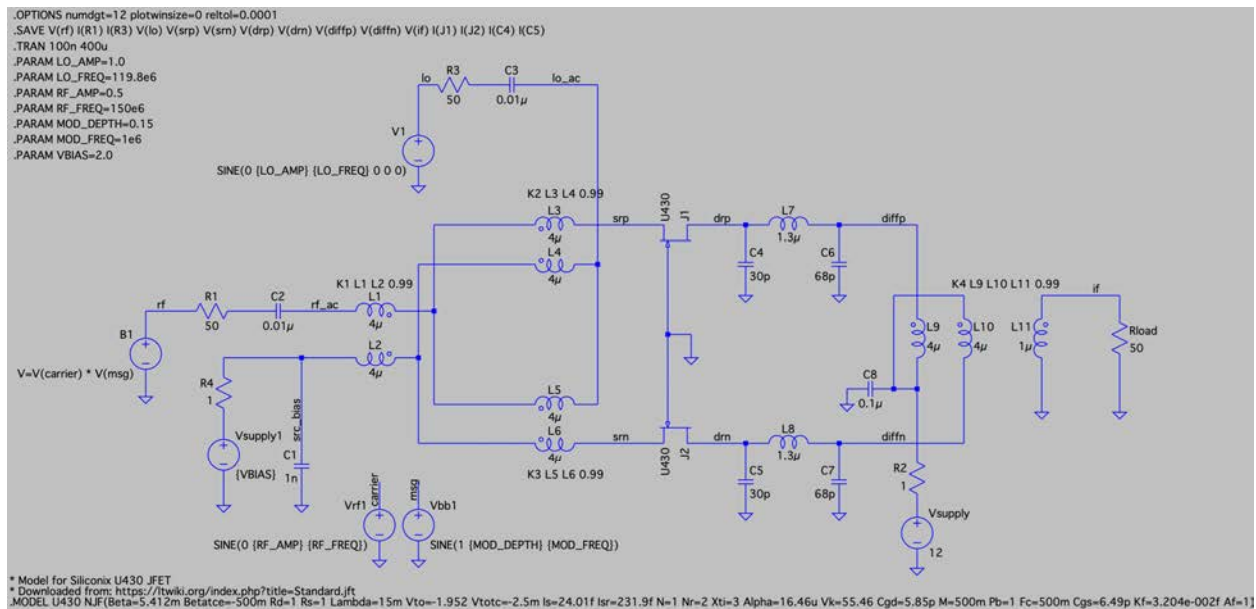


DEMAW-SIM-FIG. 7.17B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.17).

B. Simulation Results For an Input Signal Reduced by 6 dB

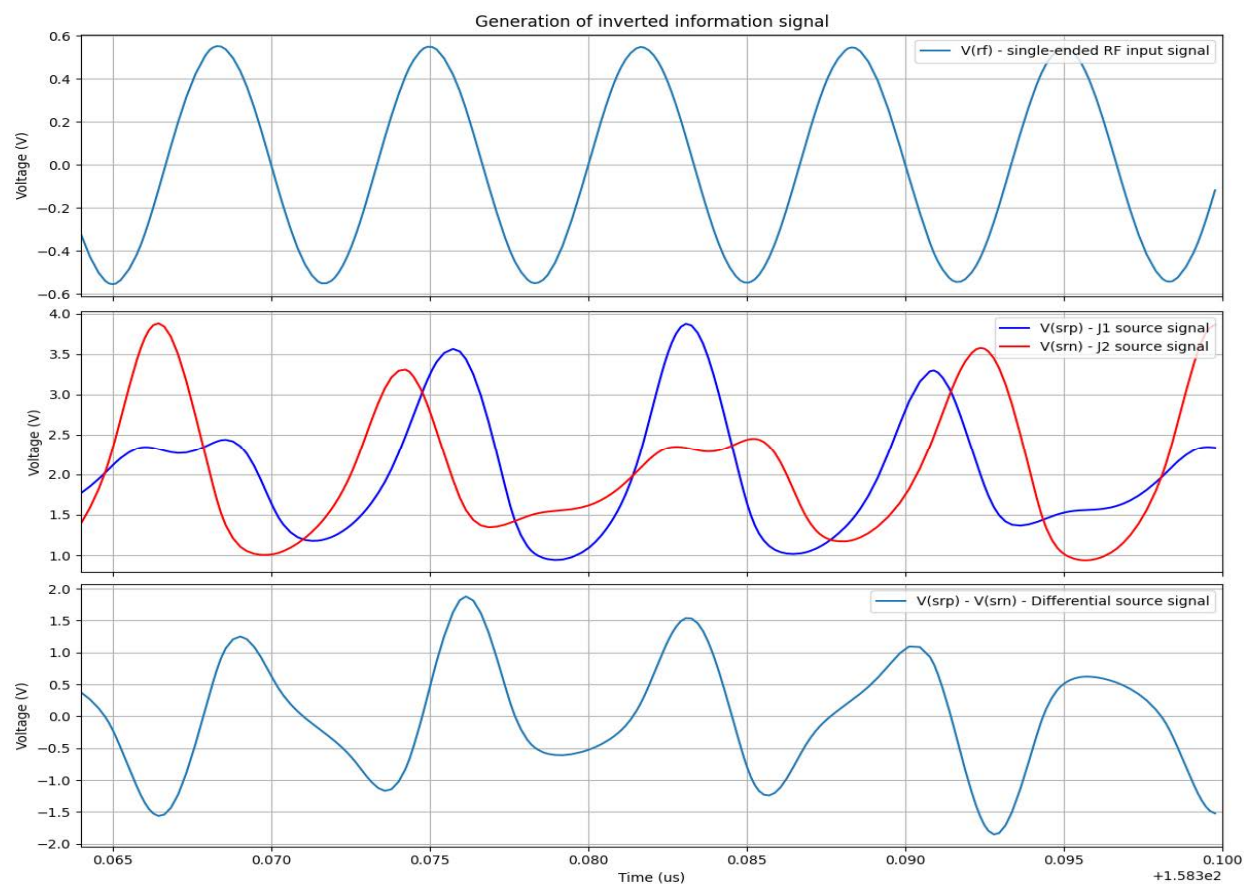
121. DEMAW-SIM-FIG. 1.18 is a schematic diagram of the simulated DeMaw FIG. 6.7 circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 6 dB. I have created additional figures DEMAW-SIM-FIGS. 4.18, 5.18, 6.18, 7.18A and 7.18B based on simulation output from DEMAW-SIM-FIG. 1.18. DEMAW-SIM-FIGS. 4.18, 5.18, 6.18, 7.18A and 7.18B show the same simulation output from DEMAW-SIM-FIG. 1.18 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMA-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMA-SIM-FIGS. 1.18, 4.18, 5.18, 6.18, 7.18A and 7.18B.



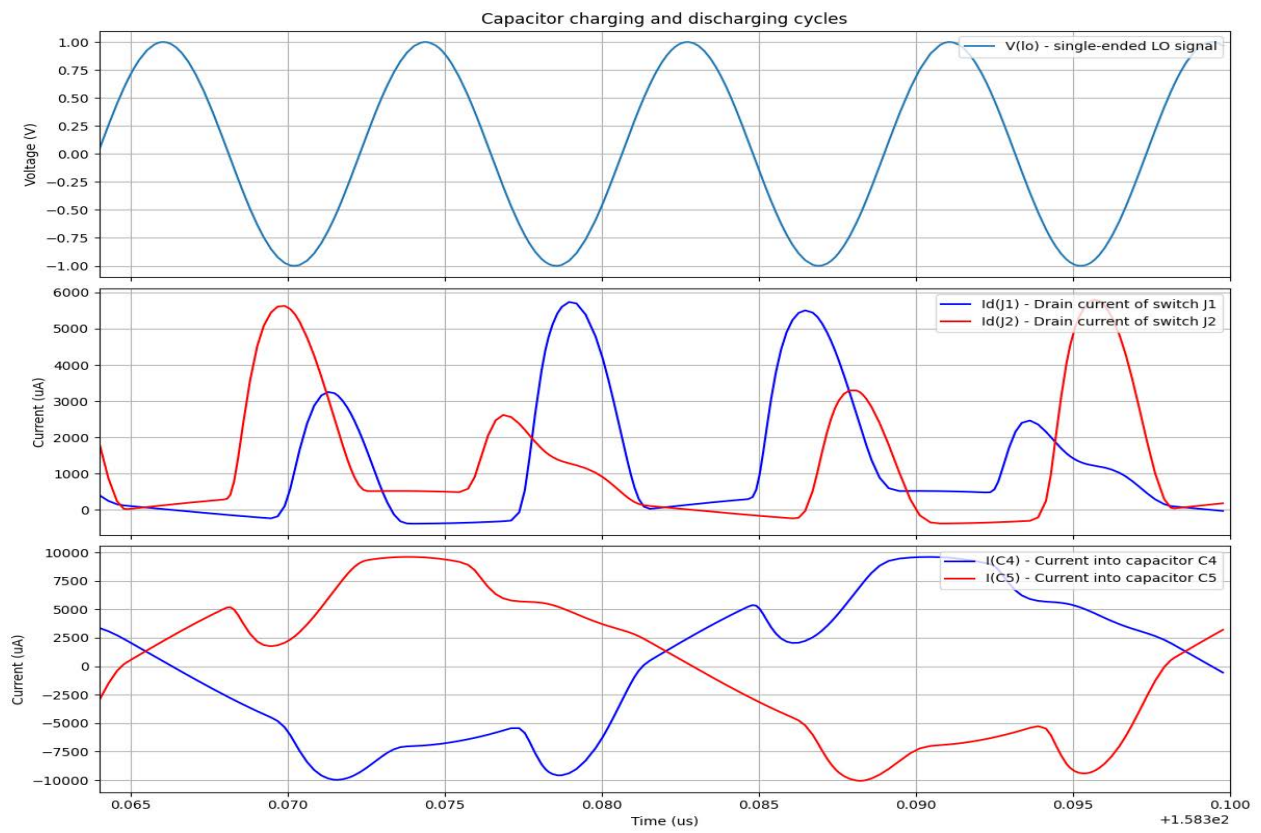
DEMA-SIM-FIG. 1.18. DeMaw circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 6 dB.

122. DEMA-SIM-FIG. 4.18 is a graphical representation of the generation of inverted information signal for the circuit of DEMA-SIM-FIG. 1.18.



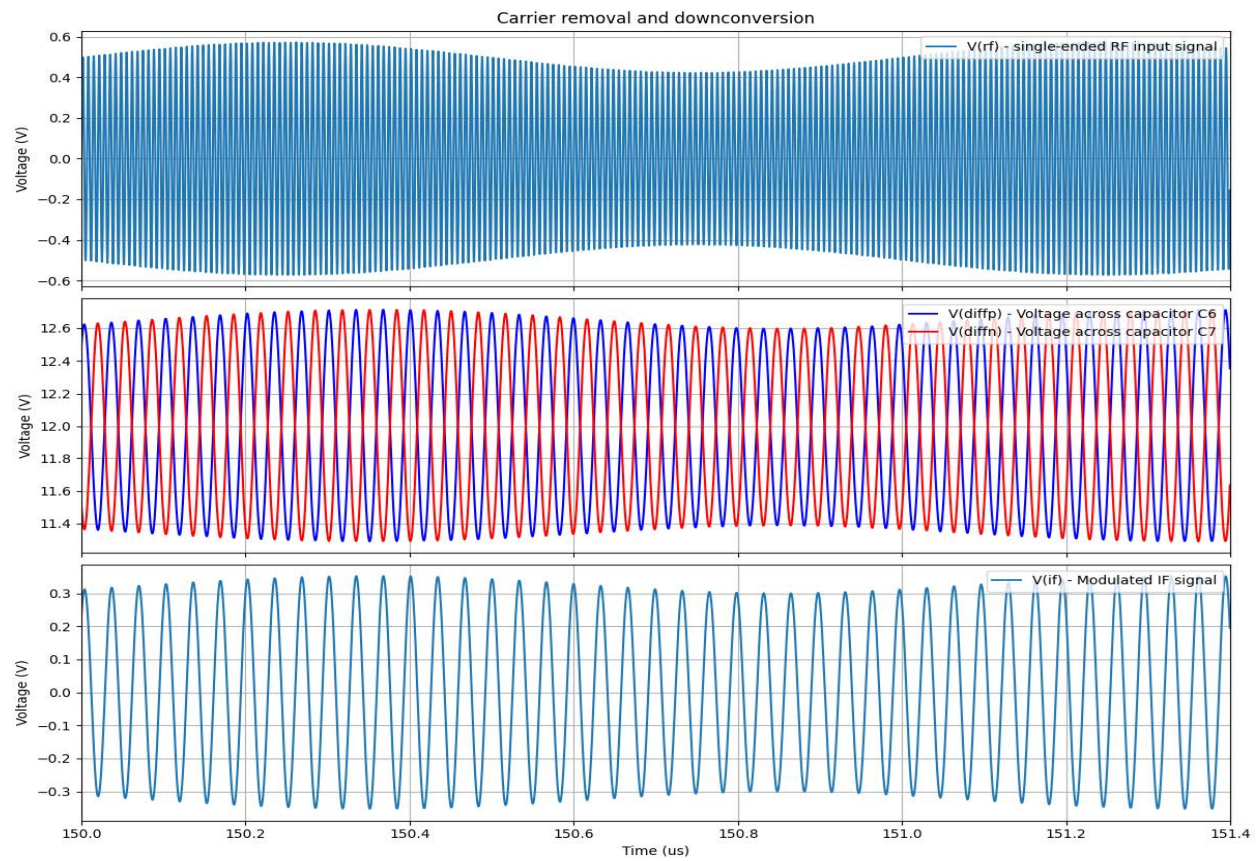
DEMAW-SIM-FIG. 4.18. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.18).

123. DEMAW-SIM-FIG. 5.18 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.18.



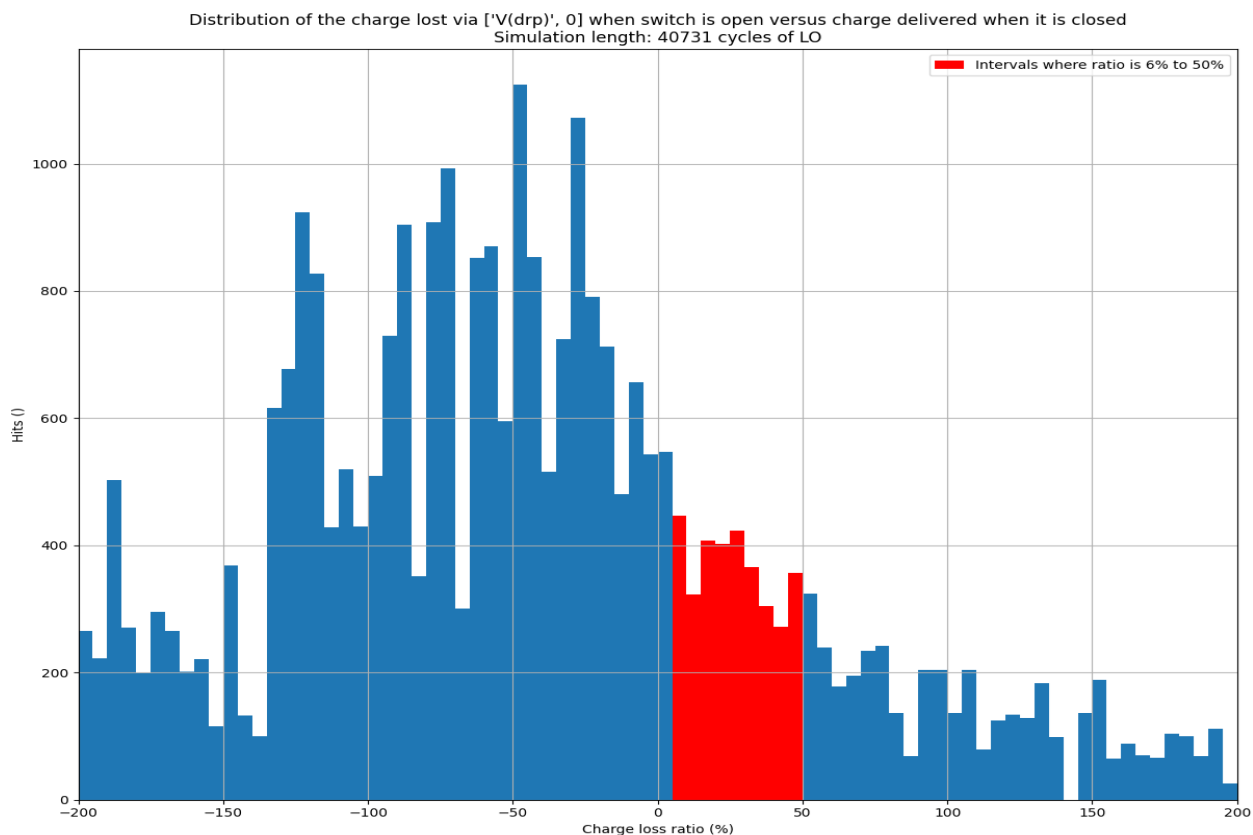
DEMAW-SIM-FIG. 5.18. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.18).

124. DEMAW-SIM-FIG. 6.18 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.18.



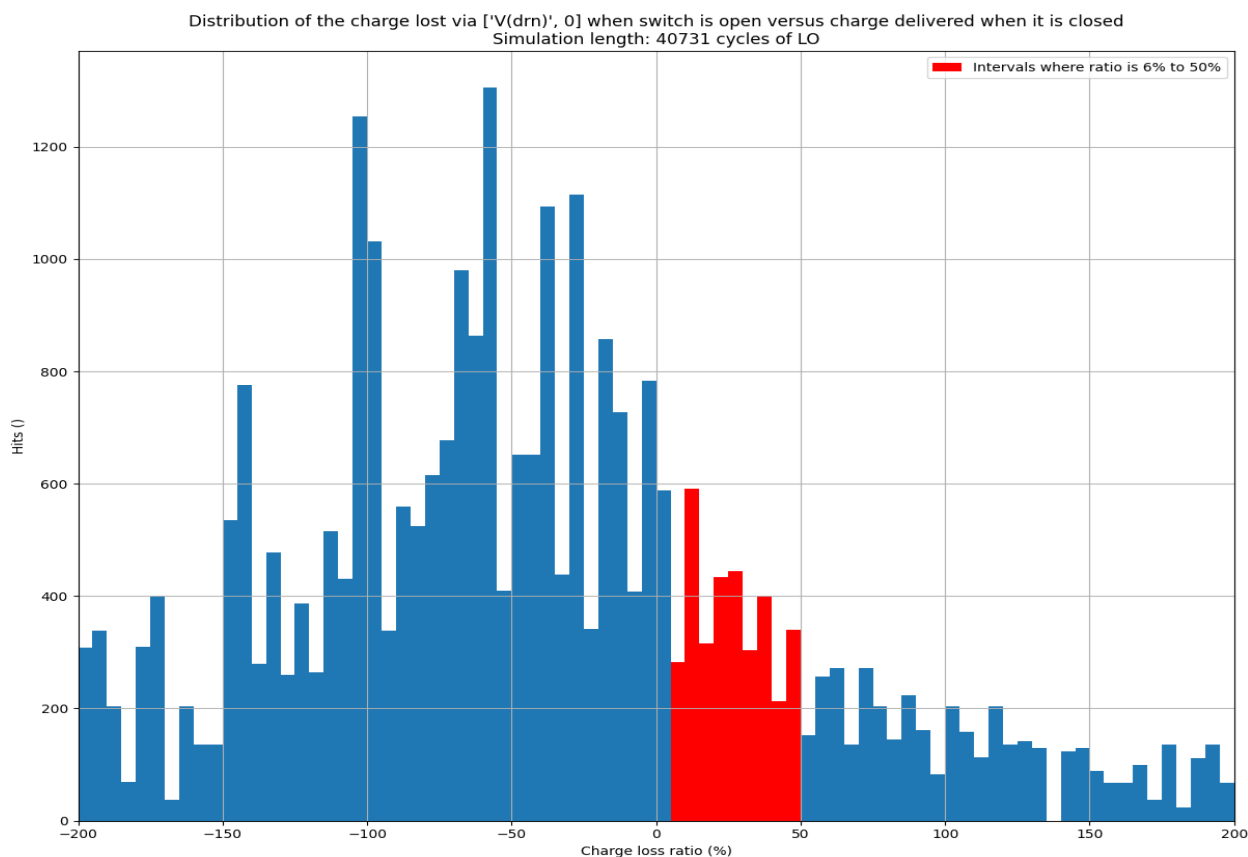
DEMAW-SIM-FIG. 6.18. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.18).

125. DEMAW-SIM-FIG. 7.18A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.18.



DEMAW-SIM-FIG. 7.18A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.18).

126. DEMAW-SIM-FIG. 7.18B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.18.

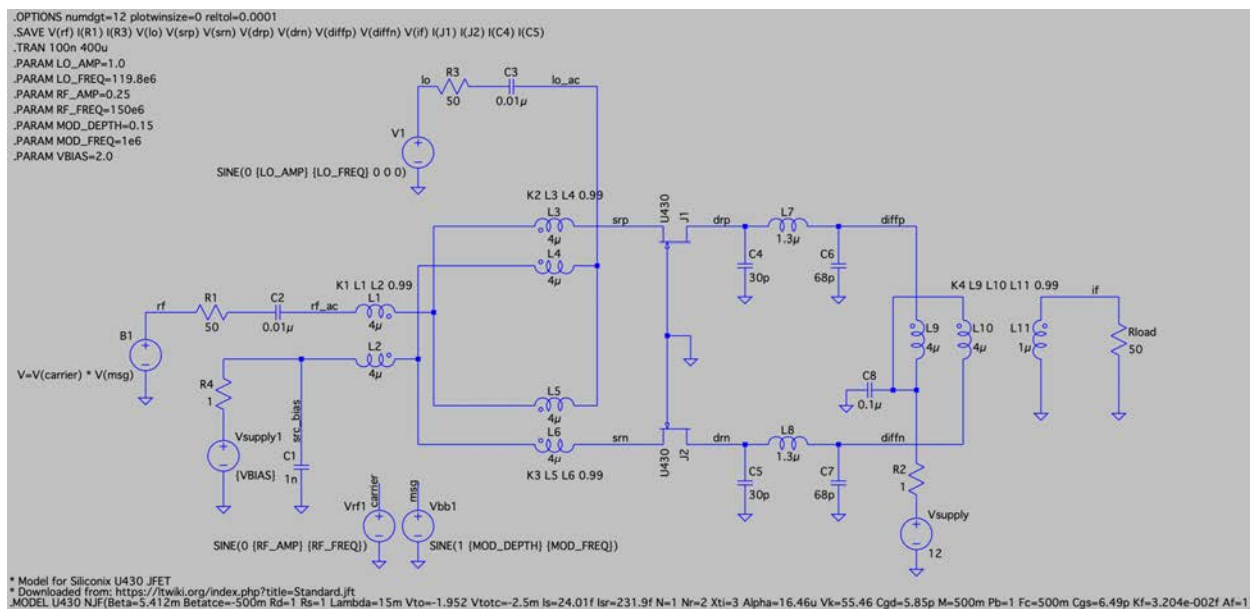


DEMAW-SIM-FIG. 7.18B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.18).

C. Simulation Results For an Input Signal Reduced by 12 dB

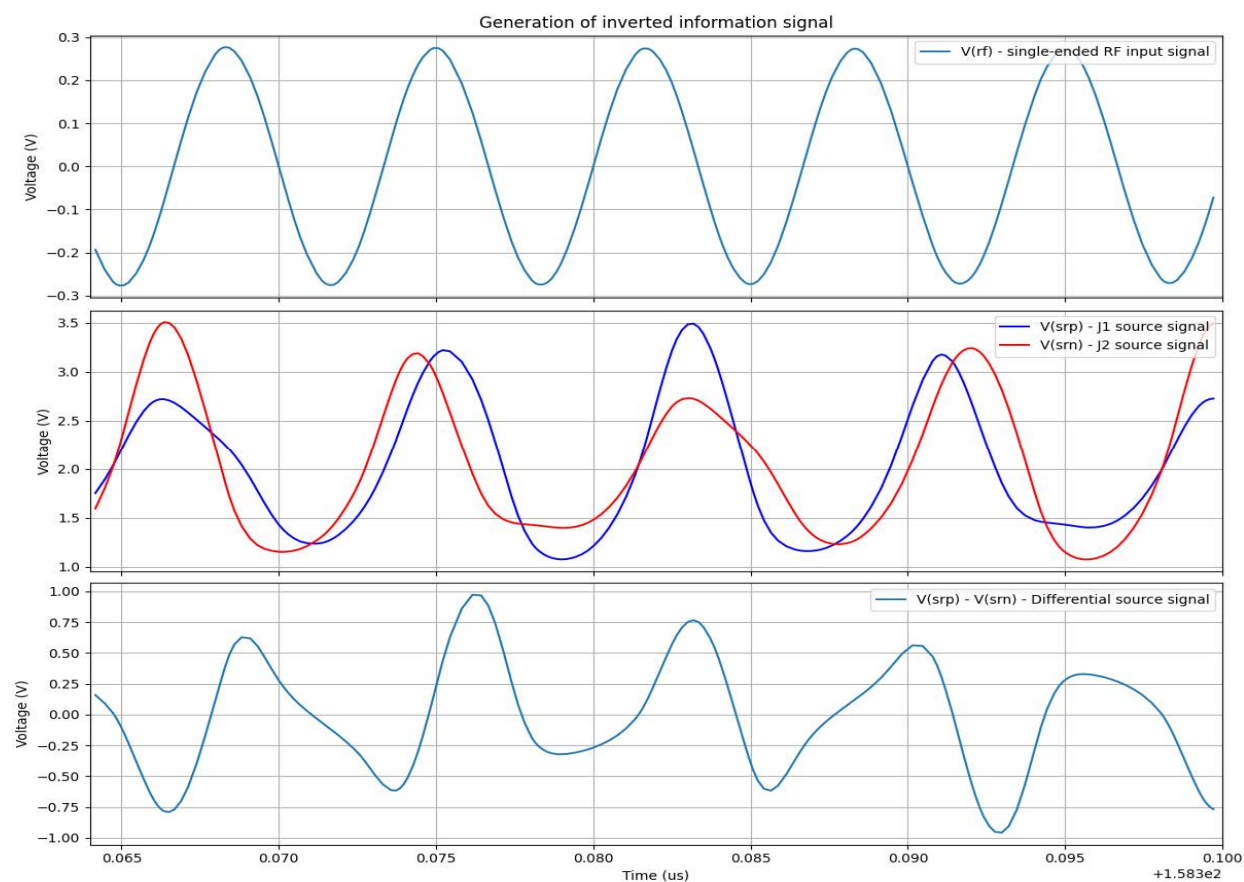
127. DEMAW-SIM-FIG. 1.19 is a schematic diagram of the simulated DeMaw FIG. 6.7 circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 12 dB. I have created additional figures DEMAW-SIM-FIGS. 4.19, 5.19, 6.19, 7.19A and 7.19B based on simulation output from DEMAW-SIM-FIG. 1.19. DEMAW-SIM-FIGS. 4.19, 5.19, 6.19, 7.19A and 7.19B show the same simulation output from DEMAW-SIM-FIG. 1.19 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMA-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMA-SIM-FIGS. 1.19, 4.19, 5.19, 6.19, 7.19A and 7.19B.



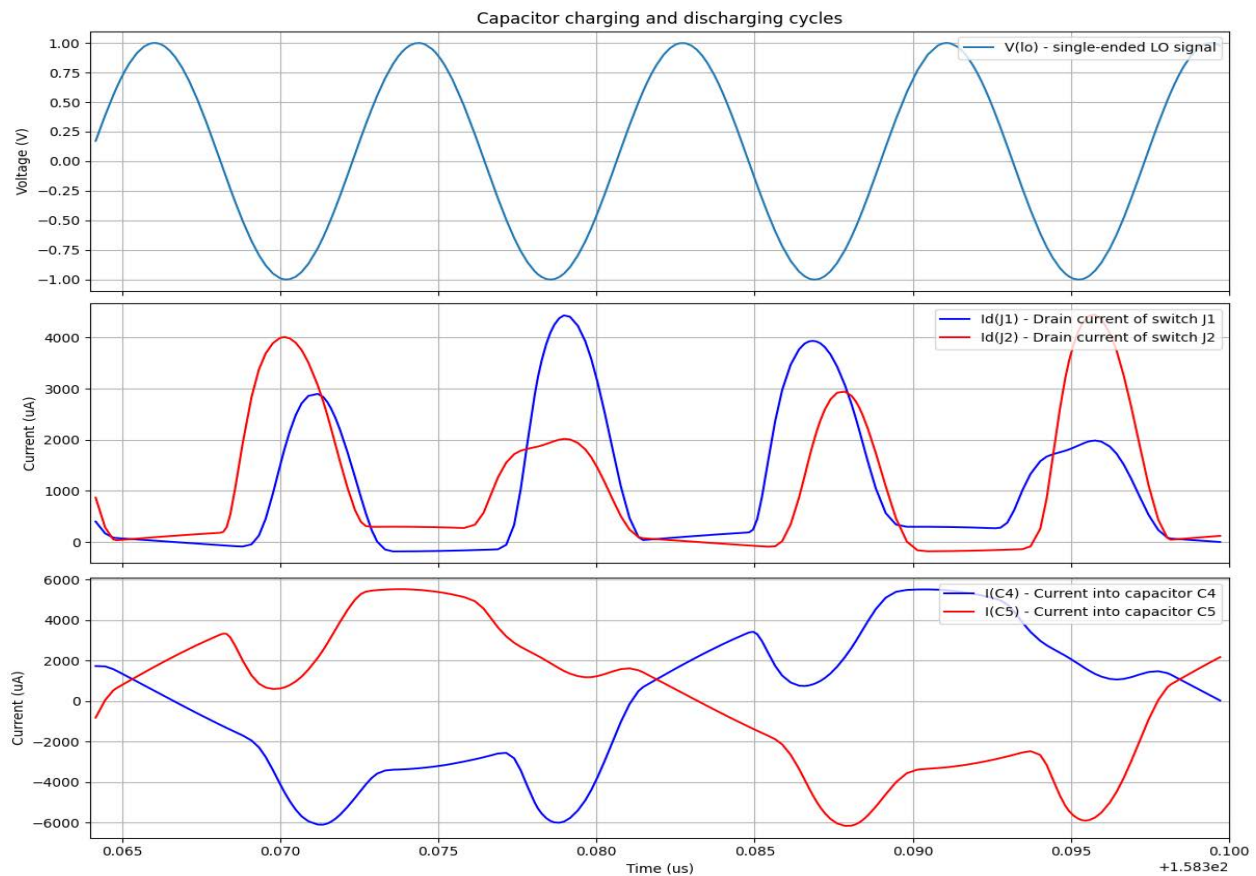
DEMA-SIM-FIG. 1.19. DeMaw circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 12 dB.

128. DEMA-SIM-FIG. 4.19 is a graphical representation of the generation of inverted information signal for the circuit of DEMA-SIM-FIG. 1.19.



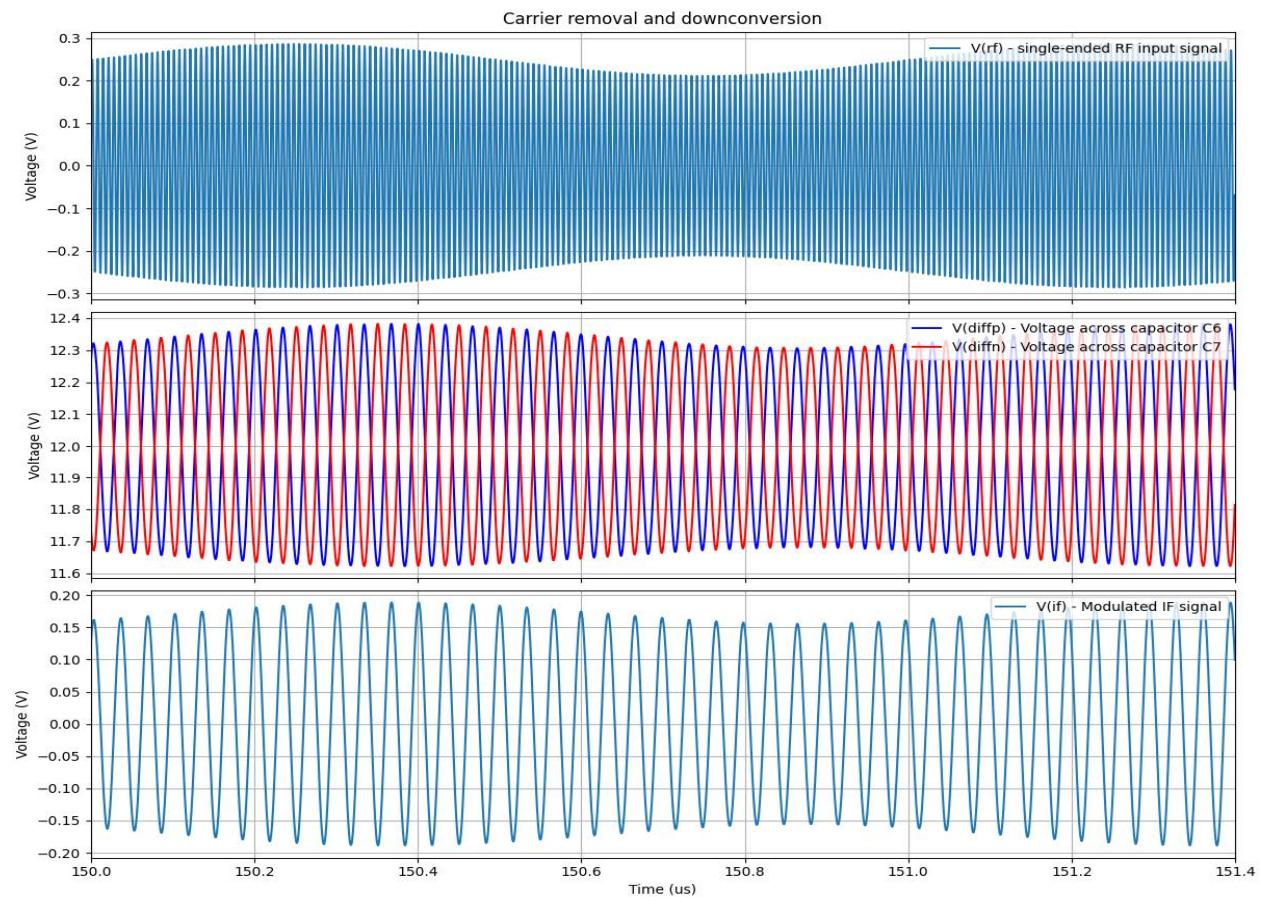
DEMAW-SIM-FIG. 4.19. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.19).

129. DEMAW-SIM-FIG. 5.19 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.19.



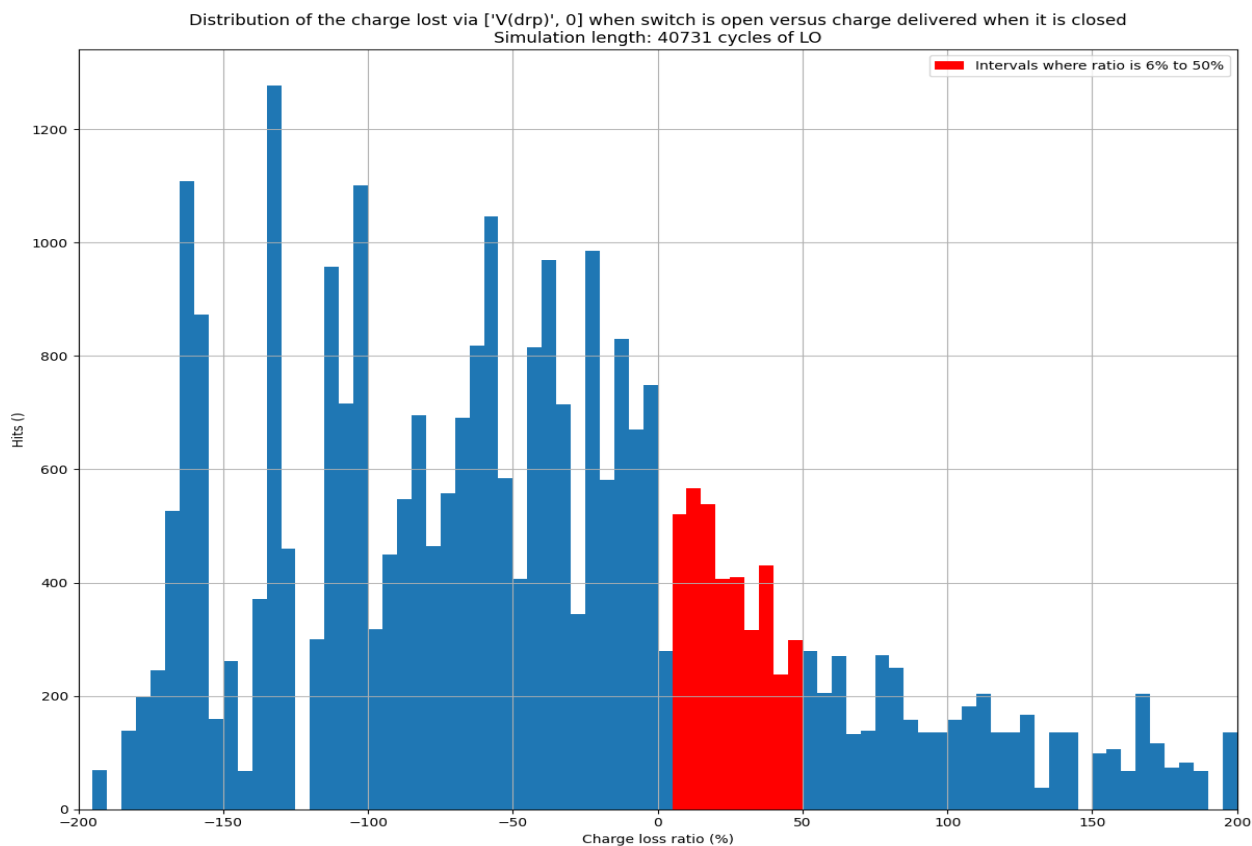
DEMAW-SIM-FIG. 5.19. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.19).

130. DEMAW-SIM-FIG. 6.19 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.19.



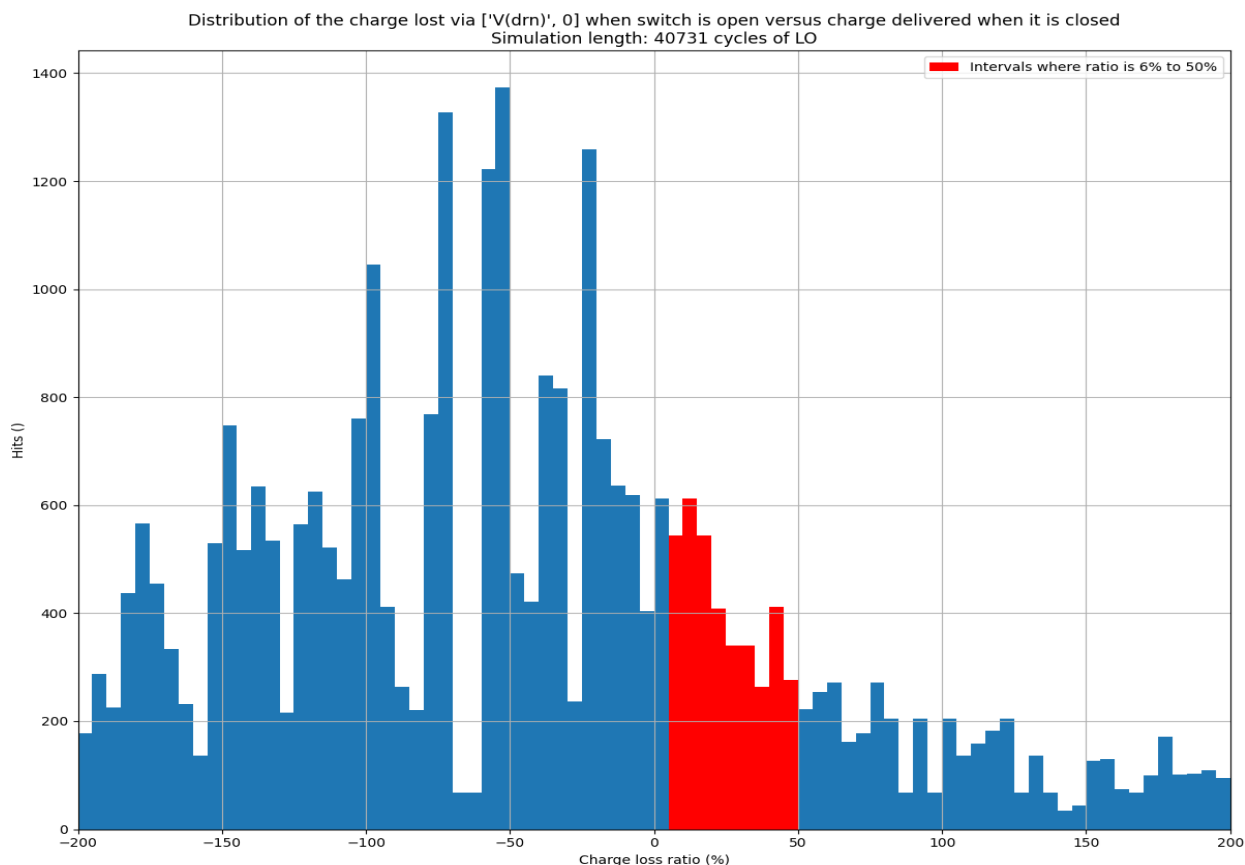
DEMAW-SIM-FIG. 6.19. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.19).

131. DEMAW-SIM-FIG. 7.19A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.19.



DEMAW-SIM-FIG. 7.19A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.19).

132. DEMAW-SIM-FIG. 7.19B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.19.

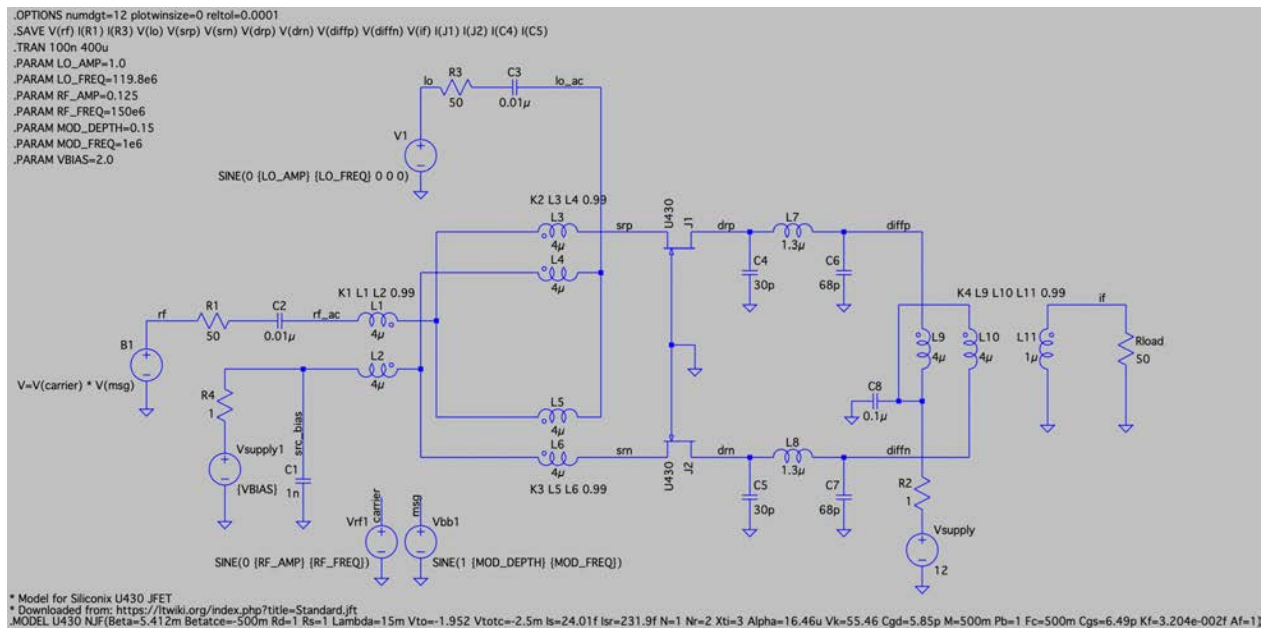


DEMAW-SIM-FIG. 7.19B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.19).

D. Simulation Results For an Input Signal Reduced by 18 dB

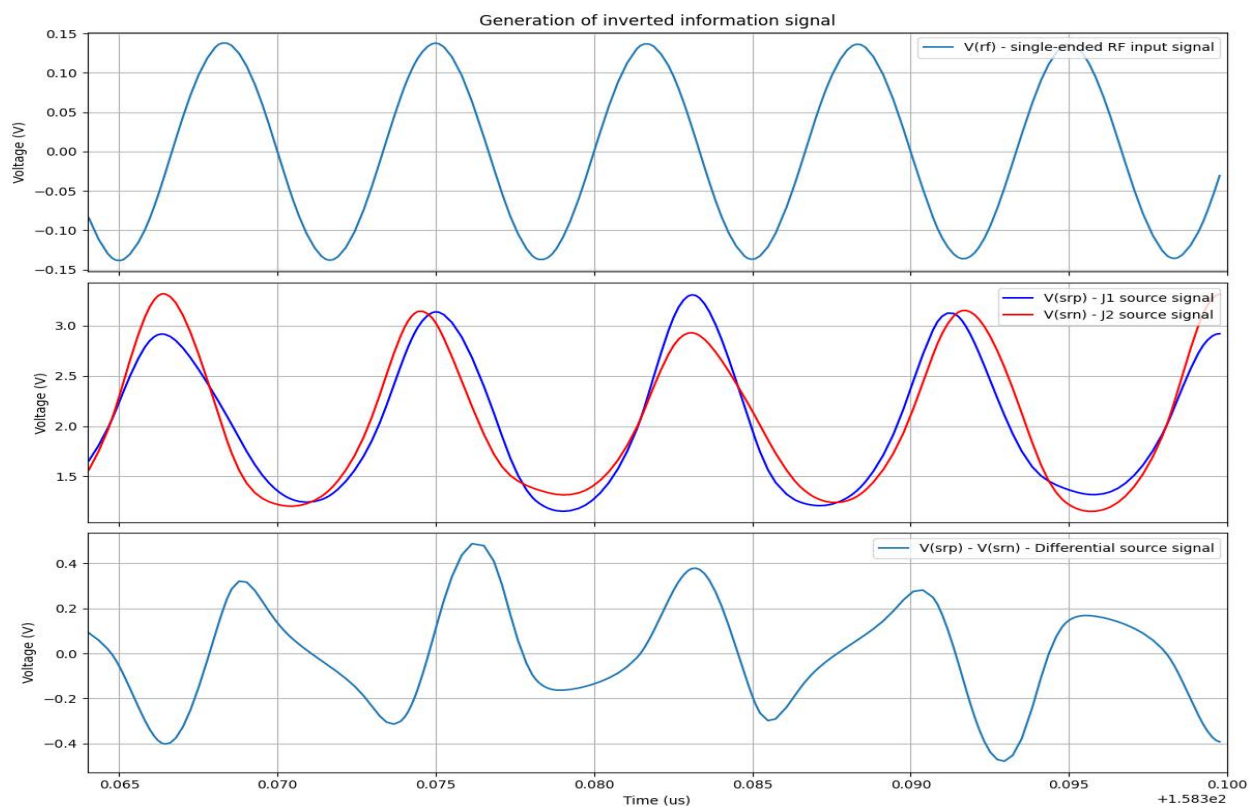
133. DEMAW-SIM-FIG. 1.20 is a schematic diagram of the simulated DeMaw FIG. 6.7 circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 18 dB. I have created additional figures DEMAW-SIM-FIGS. 4.20, 5.20, 6.20, 7.20A and 7.20B based on simulation output from DEMAW-SIM-FIG. 1.20. DEMAW-SIM-FIGS. 4.20, 5.20, 6.20, 7.20A and 7.20B show the same simulation output from DEMAW-SIM-FIG. 1.20 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMA-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMA-SIM-FIGS. 1.20, 4.20, 5.20, 6.20, 7.20A and 7.20B.



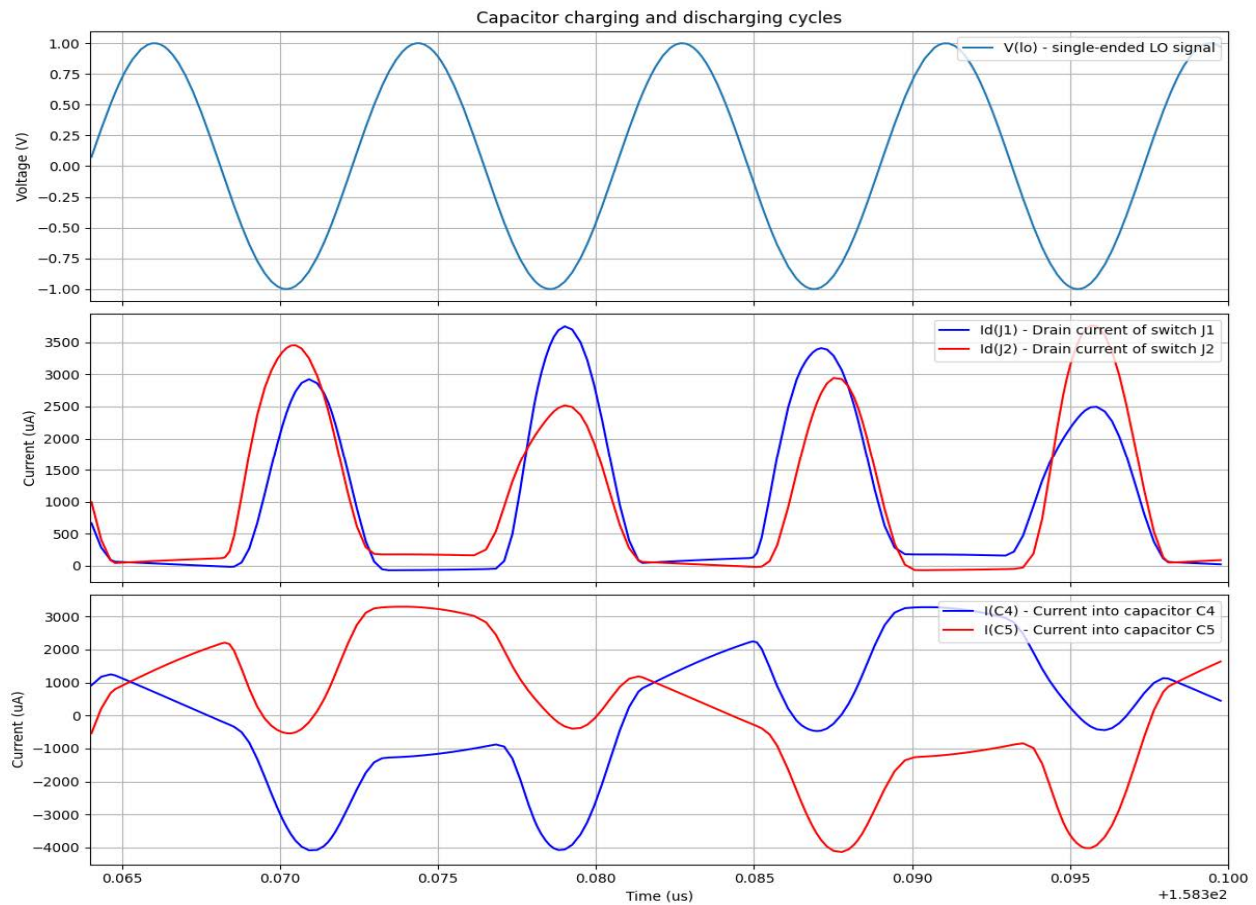
DEMA-SIM-FIG. 1.20. DeMaw circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 18 dB.

134. DEMA-SIM-FIG. 4.20 is a graphical representation of the generation of inverted information signal for the circuit of DEMA-SIM-FIG. 1.20.



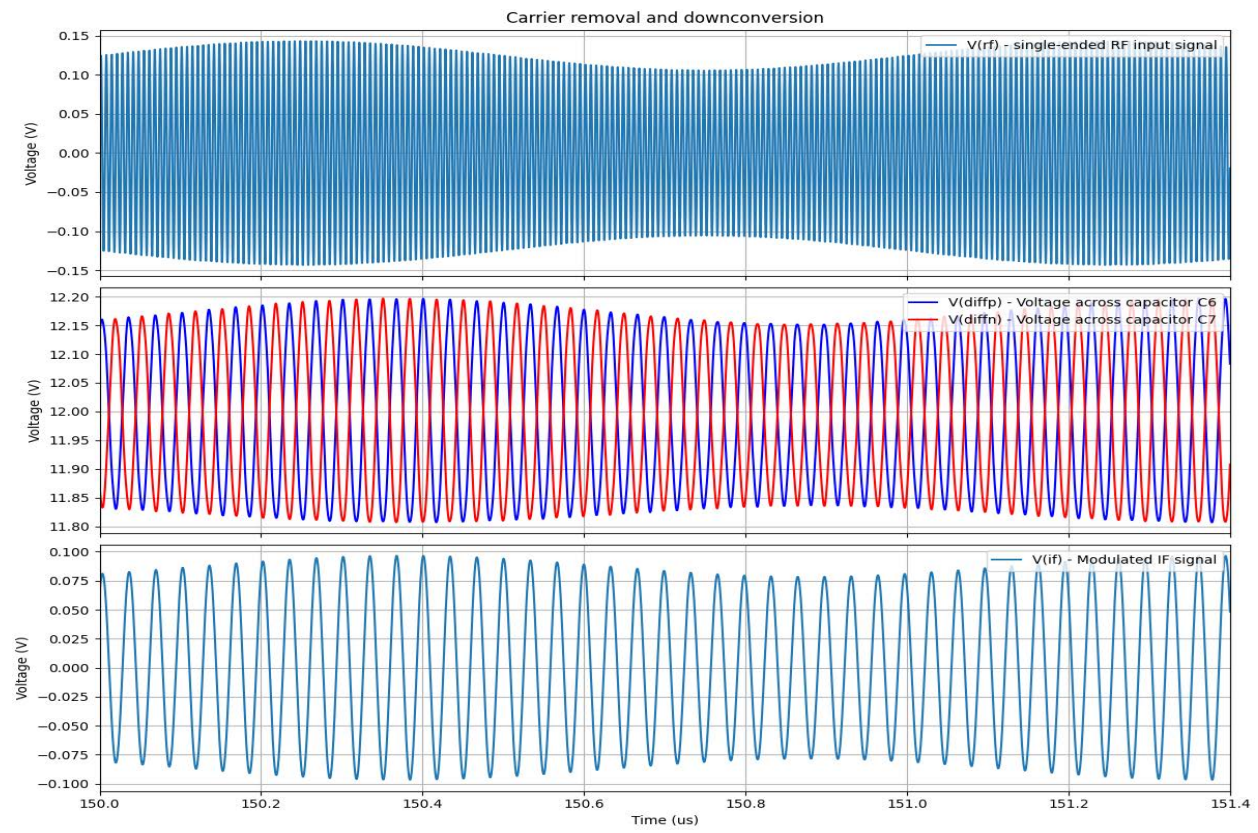
DEMAW-SIM-FIG. 4.20. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.20).

135. DEMAW-SIM-FIG. 5.20 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.20.



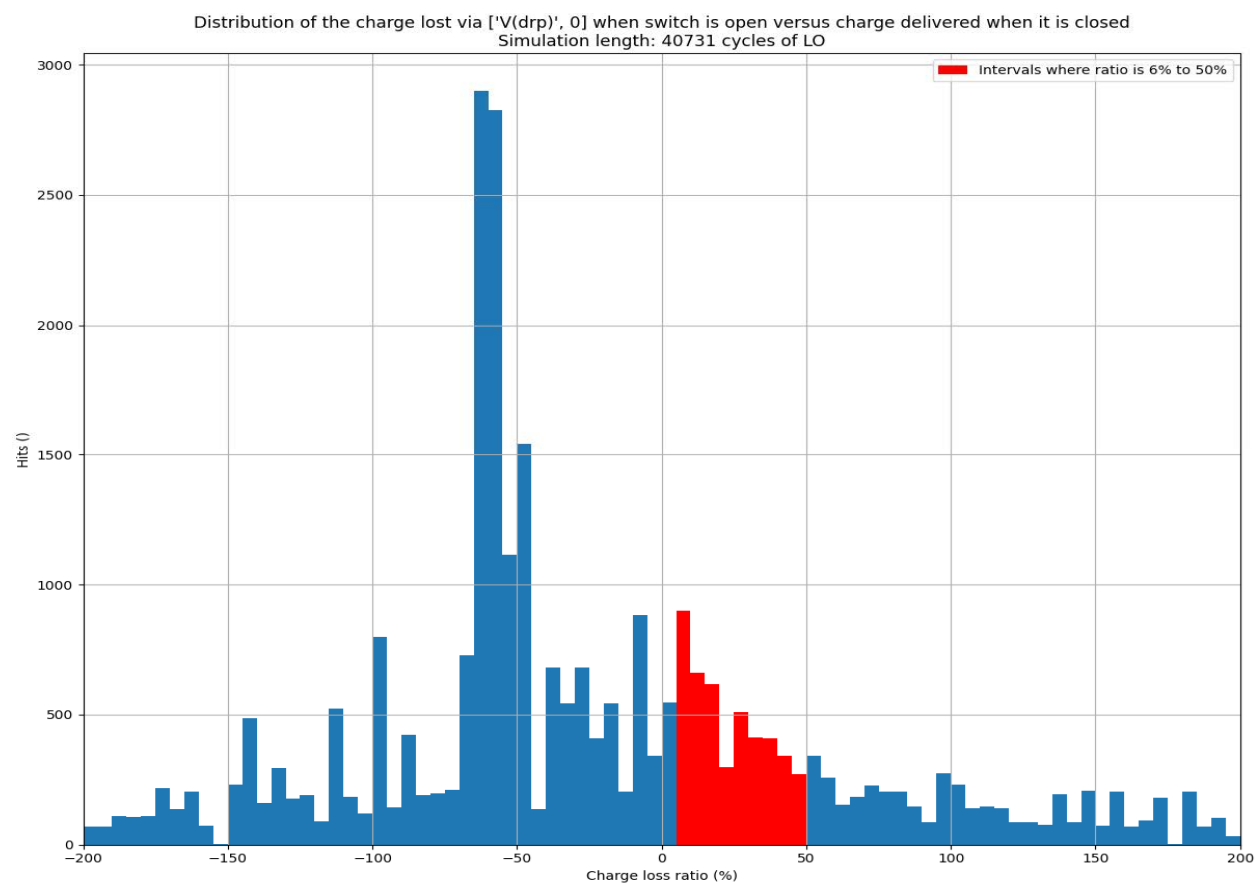
DEMAW-SIM-FIG. 5.20. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.20).

136. DEMAW-SIM-FIG. 6.20 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.20.



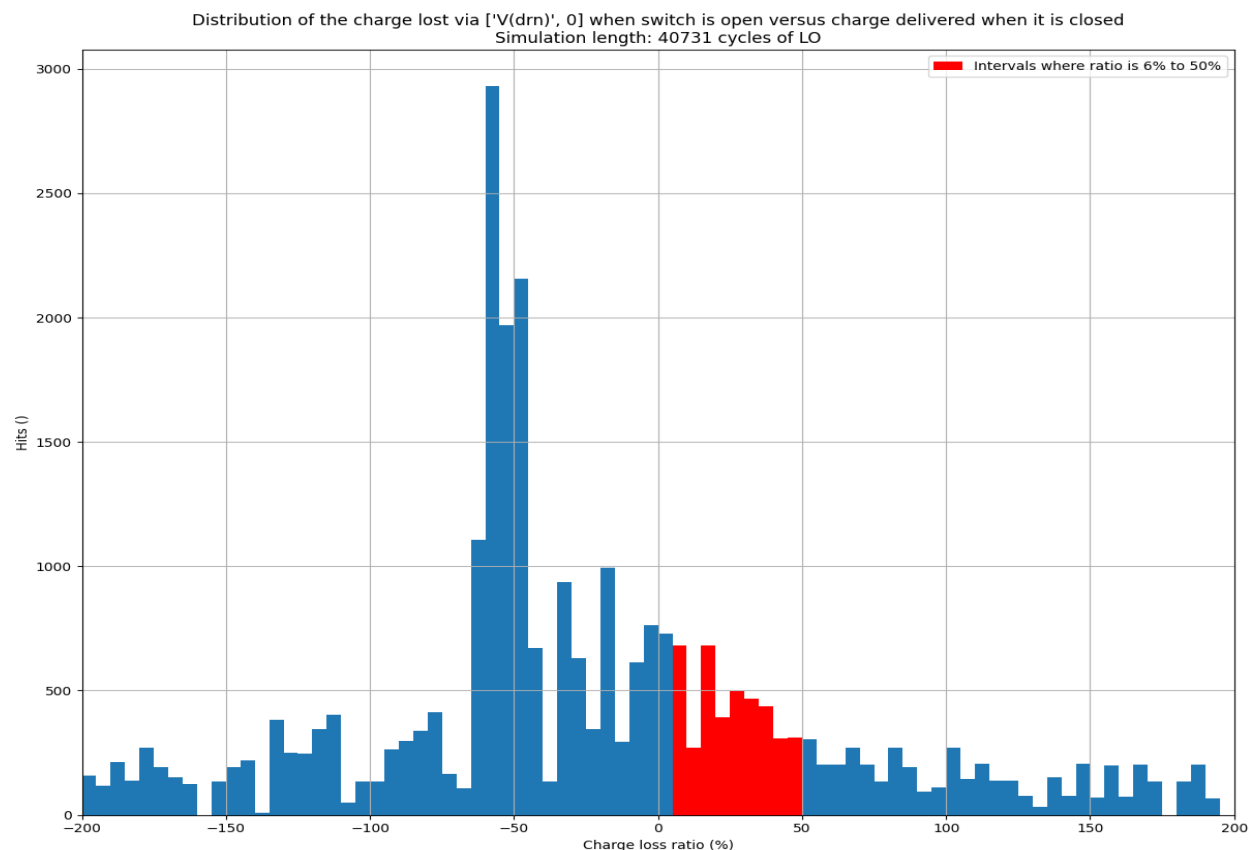
DEMAW-SIM-FIG. 6.20. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.20).

137. DEMAW-SIM-FIG. 7.20A is a histogram showing charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.20.



DEMAW-SIM-FIG. 7.20A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.20).

138. DEMAW-SIM-FIG. 7.20B is a histogram showing charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.20.

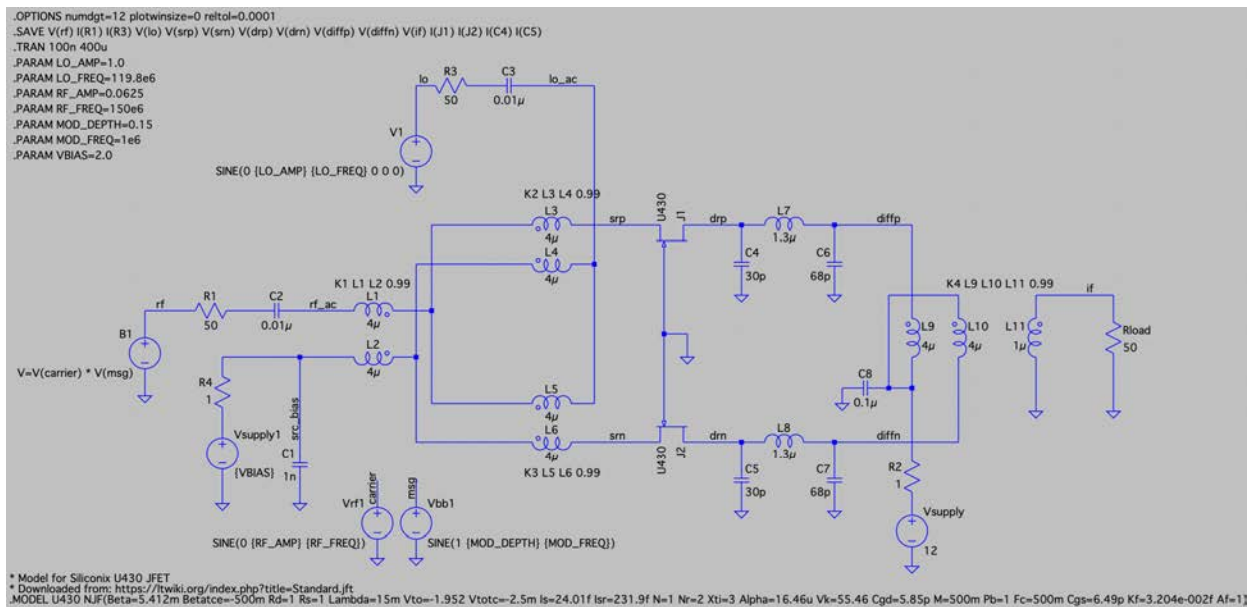


DEMAW-SIM-FIG. 7.20B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.20).

E. Simulation Results For an Input Signal Reduced by 24 dB

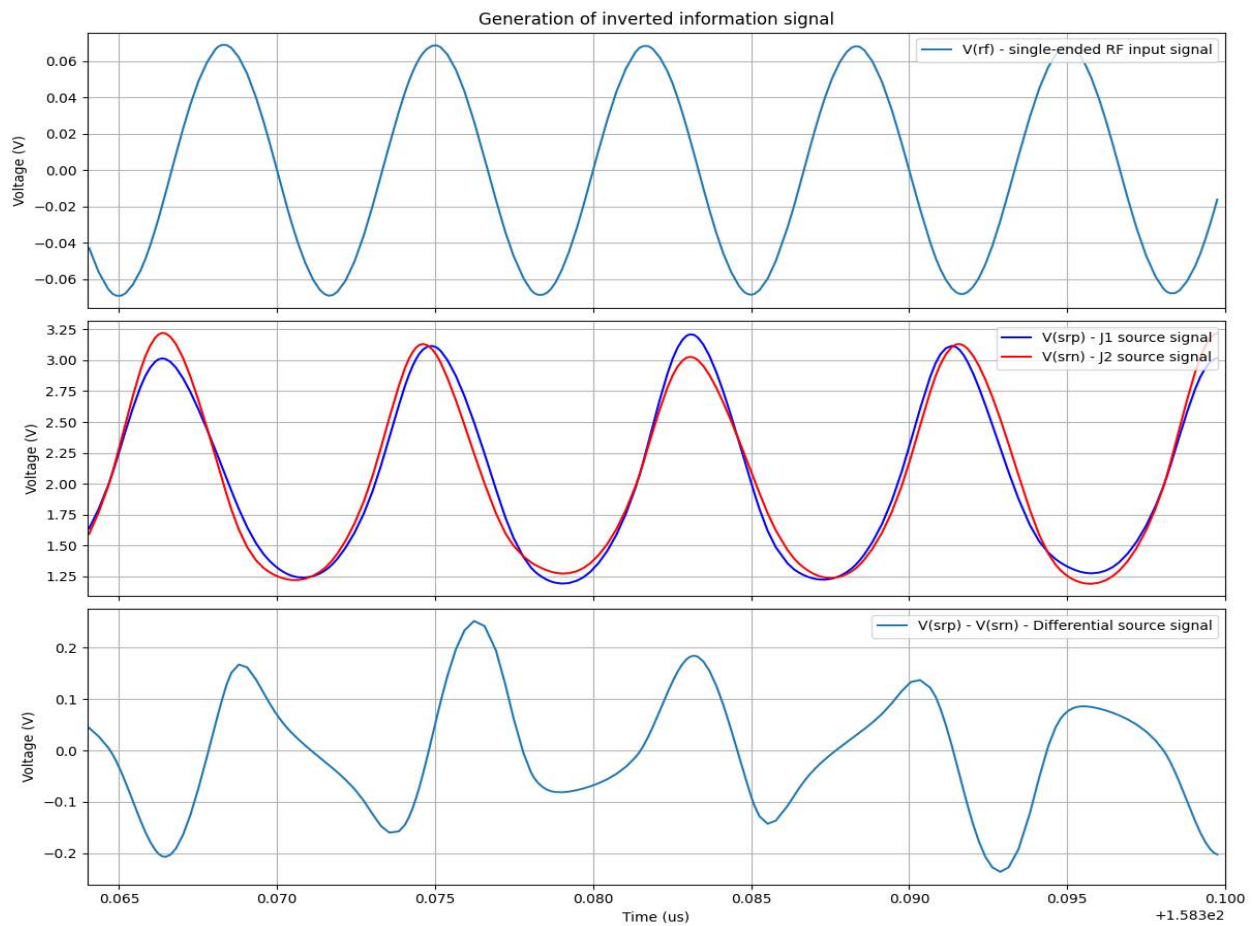
139. DEMAW-SIM-FIG. 1.21 is a schematic diagram of the simulated DeMaw FIG. 6.7 circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 24 dB. I have created additional figures DEMAW-SIM-FIGS. 4.21, 5.21, 6.21, 7.21A and 7.21B based on simulation output from DEMAW-SIM-FIG. 1.21. DEMAW-SIM-FIGS. 4.21, 5.21, 6.21, 7.21A and 7.21B show the same simulation output from DEMAW-SIM-FIG. 1.21 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration

regarding the claims based on DEMA-W-SIM-FIG. 1, 4, 5, 6, and 7 are likewise supported by DEMA-W-SIM-FIGS. 1.21, 4.21, 5.21, 6.21, 7.21A and 7.21B.



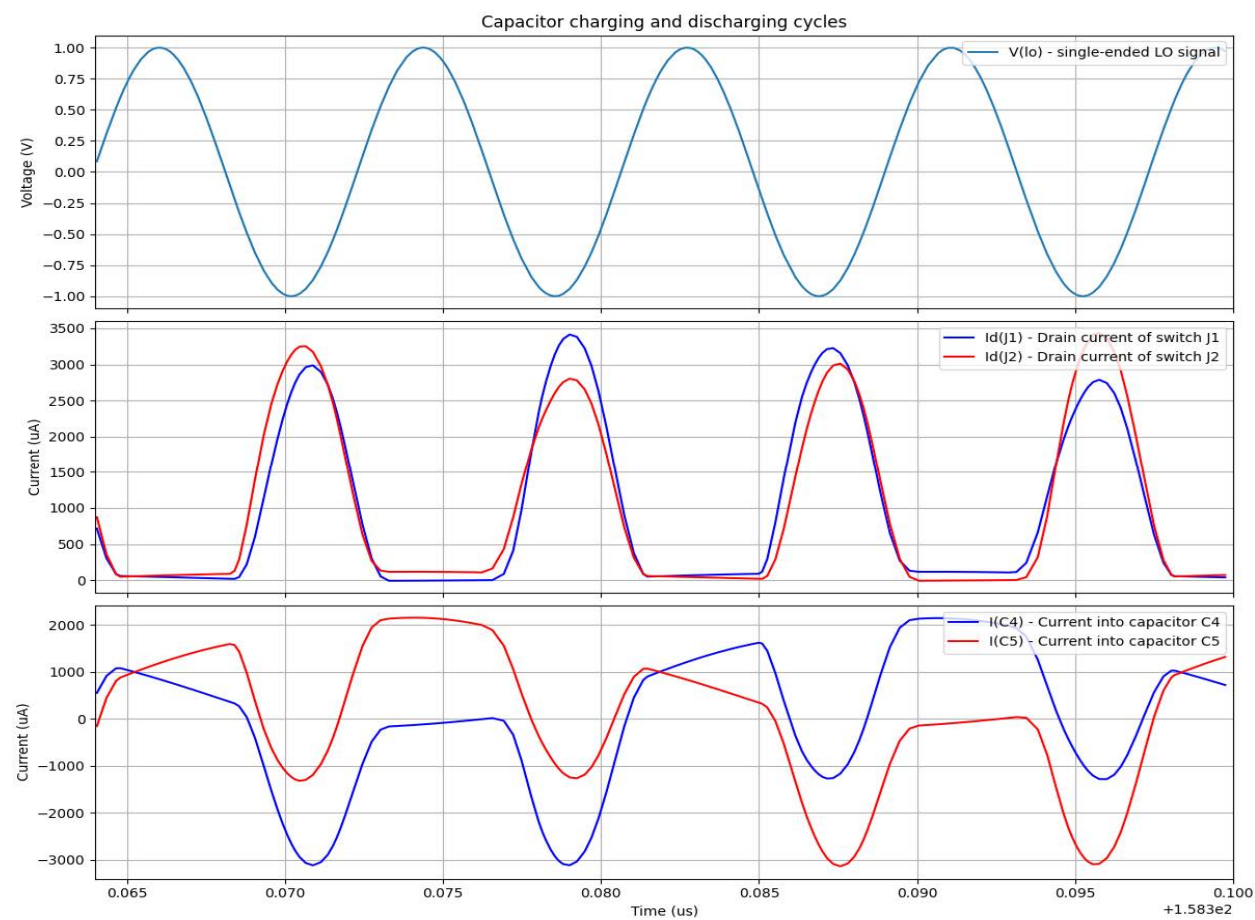
DEMA-W-SIM-FIG. 1.21. DeMaw circuit modified to match Oxner with a sinusoidal LO and input signal reduced by 24 dB.

140. DEMA-W-SIM-FIG. 4.21 is a graphical representation of the generation of inverted information signal for the circuit of DEMA-W-SIM-FIG. 1.21.



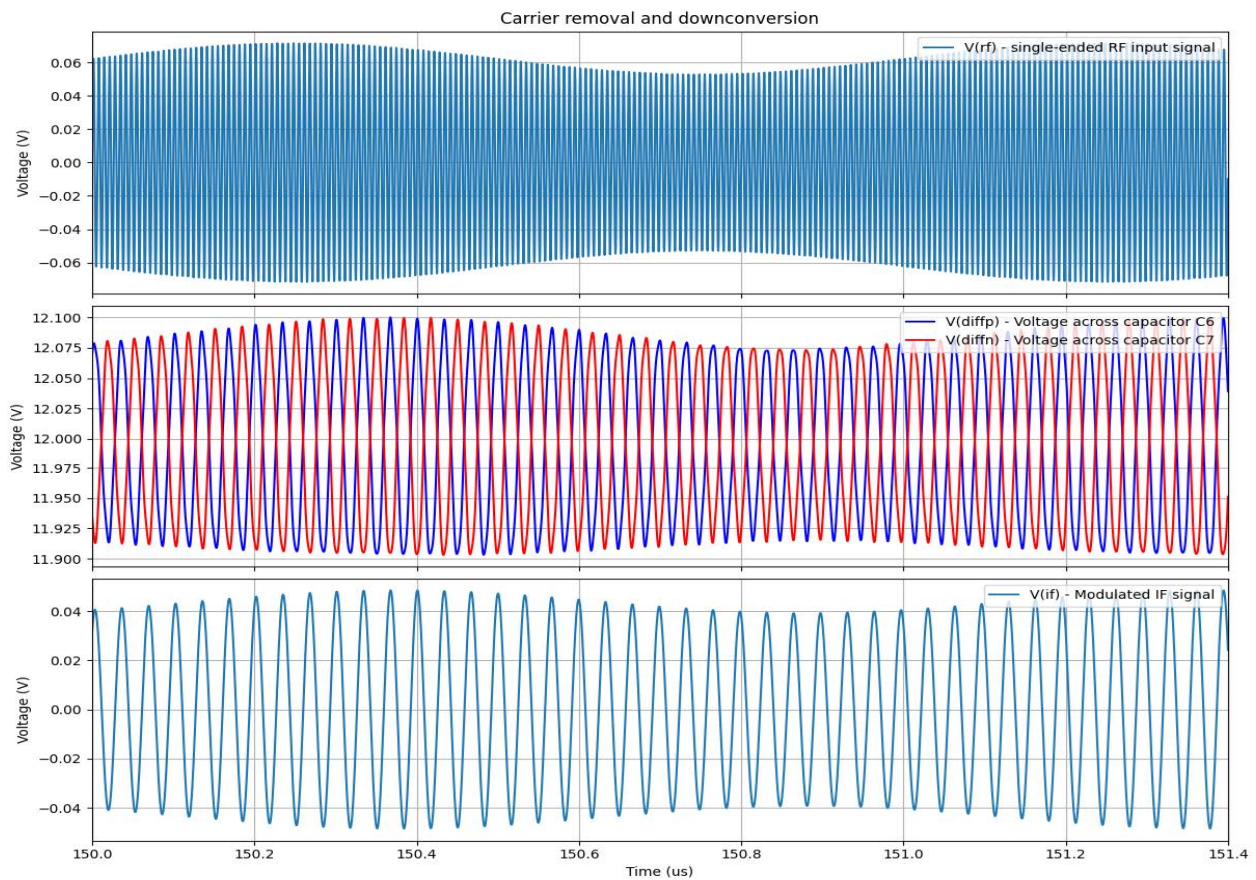
DEMAW-SIM-FIG. 4.21. Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1.21).

141. DEMAW-SIM-FIG. 5.21 is a graphical representation showing the charging and discharging cycles for capacitors C4 and C5 for the circuit of DEMAW-SIM-FIG. 1.21.



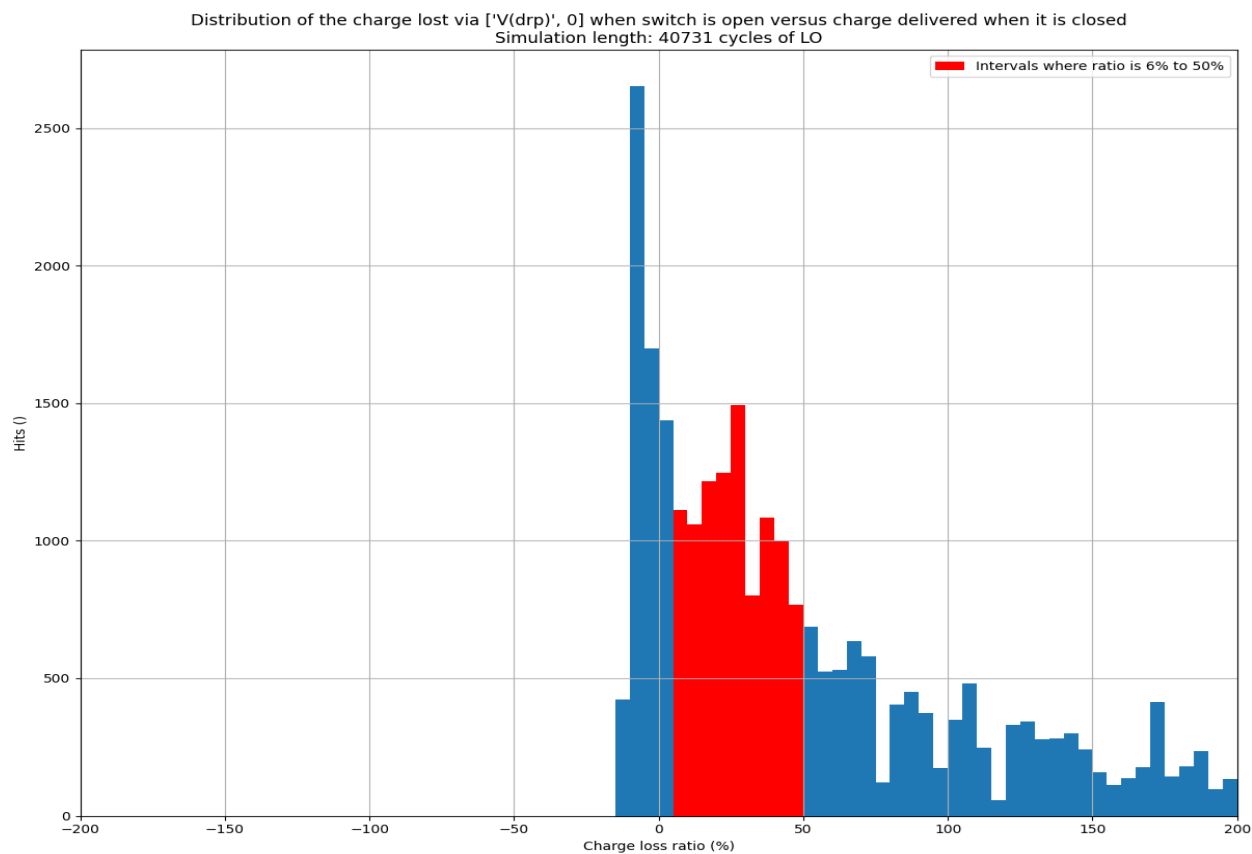
DEMAW-SIM-FIG. 5.21. Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1.21).

142. DEMAW-SIM-FIG. 6.21 is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1.21.



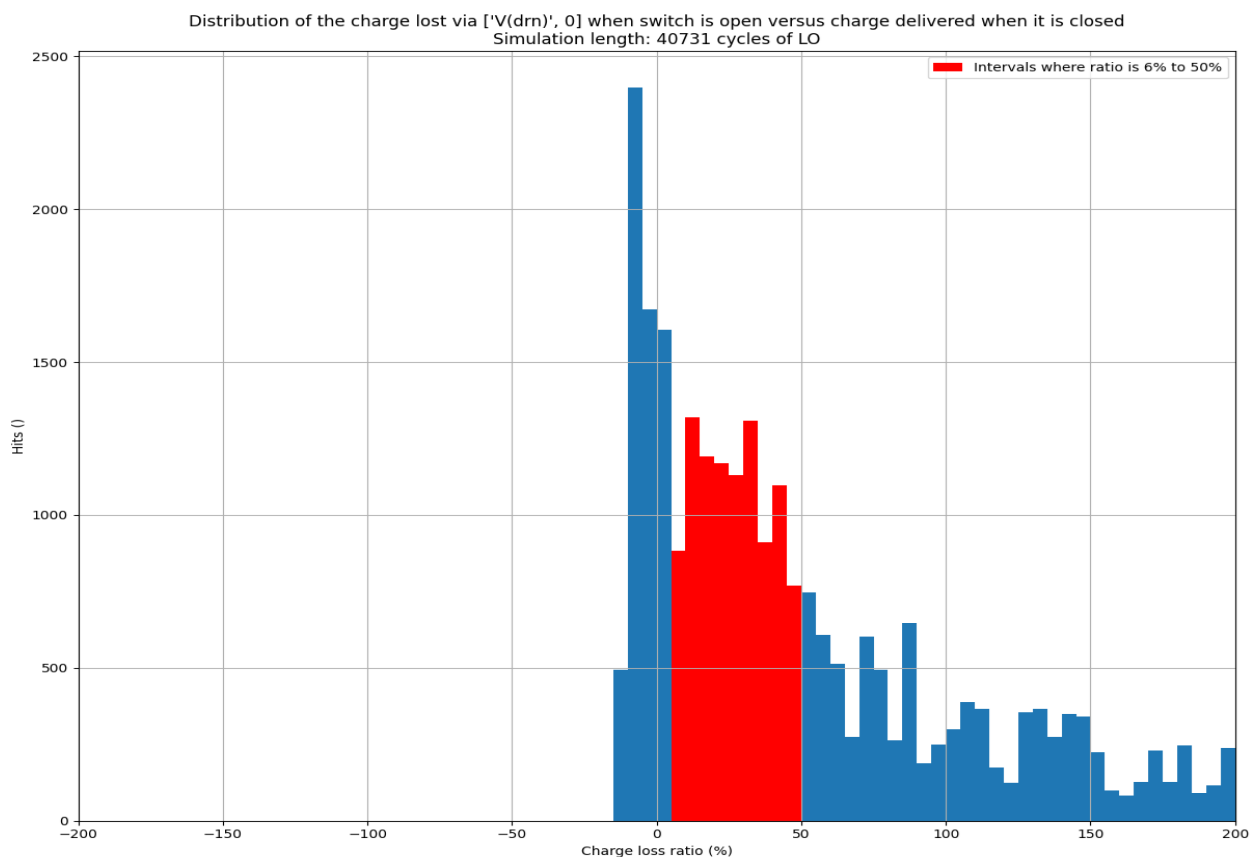
DEMAW-SIM-FIG. 6.21. Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1.21).

143. DEMAW-SIM-FIG. 7.21A is a histogram showing the charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1.21.



DEMAW-SIM-FIG. 7.21A. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.21).

144. DEMAW-SIM-FIG. 7.21B is a histogram showing the charge loss ratio percentages for capacitor C5 for the circuit of DEMAW-SIM-FIG. 1.21.



DEMAW-SIM-FIG. 7.21B. Charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.21).

VII. Macnally Circuit Modified to Match That Presented in Macnally Patent

145. To further demonstrate that I have not chosen component values and circuit configurations to “get the results [that TI] needed” as alleged in the POPR, the simulation results presented in this section correspond to the mixer circuit presented in the Macnally patent with component values and an input signal that matches the information presented in the Macnally patent as closely as possible. These changes include:

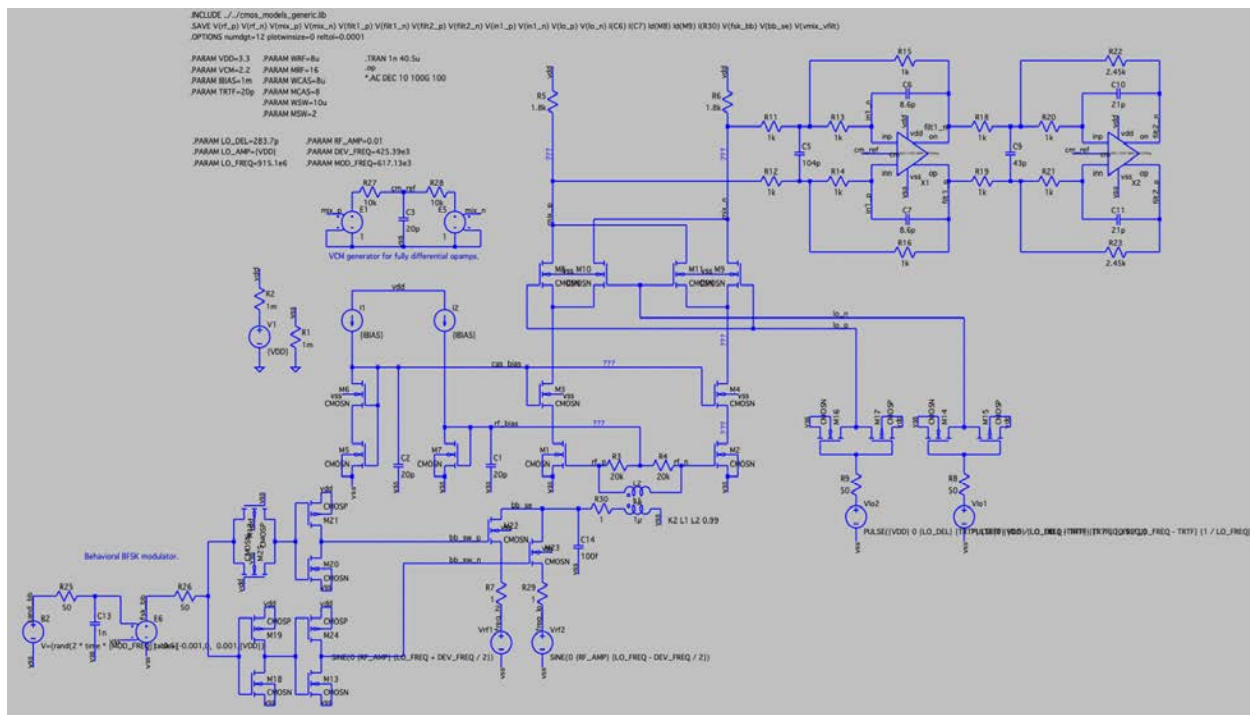
- Actual resistors are used to implement R3 and R4 in FIG. 3 of Macnally

(in contrast, the corresponding circuit described in my original Declaration used a combination of current sources and resistors to implement the effect of R3 and R4, which is common practice in circuit design).

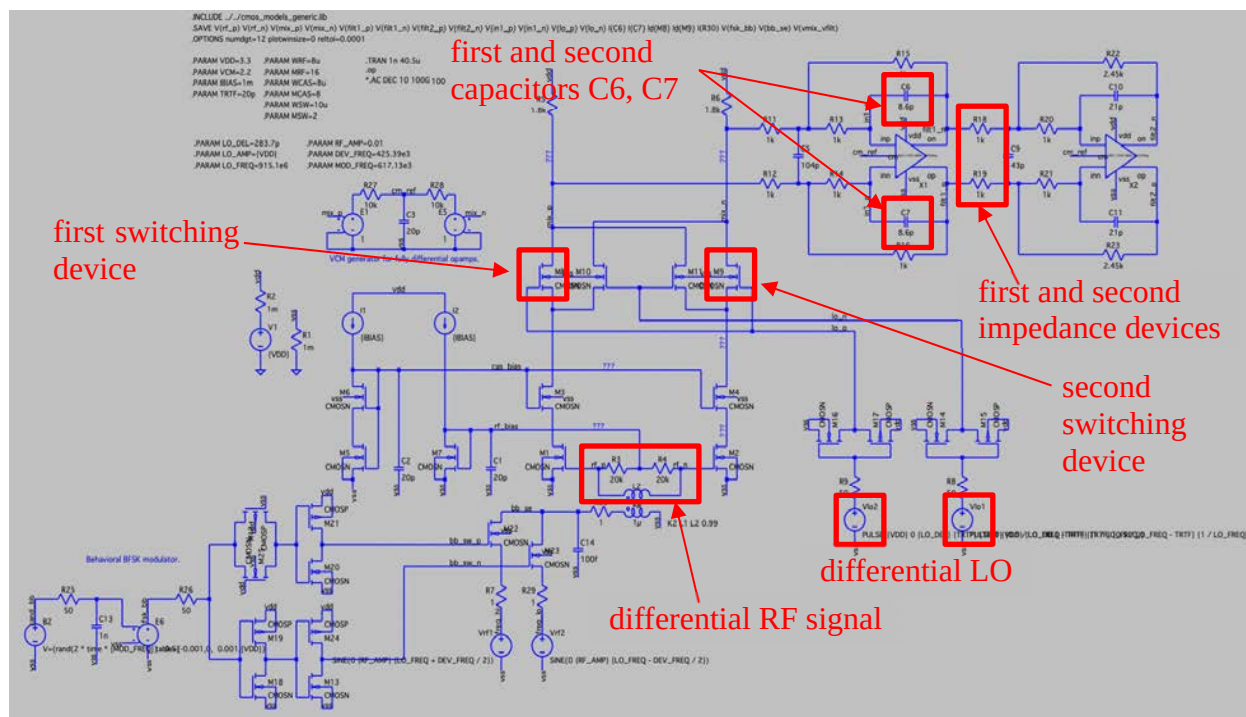
- The mixer gain was increased to that described in Macnally by changing the size and bias voltages of the M1 and M2 transistors shown in FIG. 3 of Macnally (to achieve the 8.5 mS of transconductance mentioned in Macnally), and adjusting the cross-over points of the pseudo-differential LO signals to prevent the mixer core transistors, i.e., M5, M6, M7, and M8 in FIG. 3 of Macnally, from cross-conducting.
- The RF input signal was changed to have BFSK modulation and a center frequency of 915 MHz to more closely match the application mentioned in Macnally.

146. MACNALLY-SIM-FIG. 1.1 depicts the simulation with the changes noted above. None of the changes cause differences in the simulated results that change the conclusions presented in my original Declaration regarding the alleged invention disclosed in the '342 patent. I have created additional figures MACNALLY-SIM-FIGS. 2.1, 3.1, 4.1A and 4.1B based on simulation output from MACNALLY-SIM-FIG. 1.1. MACNALLY-SIM-FIGS. 2.1, 3.1, 4.1A and 4.1B show the same simulation output from MACNALLY-SIM-FIG. 1.1 as

MACNALLY-SIM-FIGS. 2, 3, 4, 5 and 6 show from MACNALLY-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims based on MACNALLY-SIM-FIGS 1-5 are likewise supported by MACNALLY-SIM-FIGS. 1.1, 2.1, 3.1, 4.1A and 4.1B.

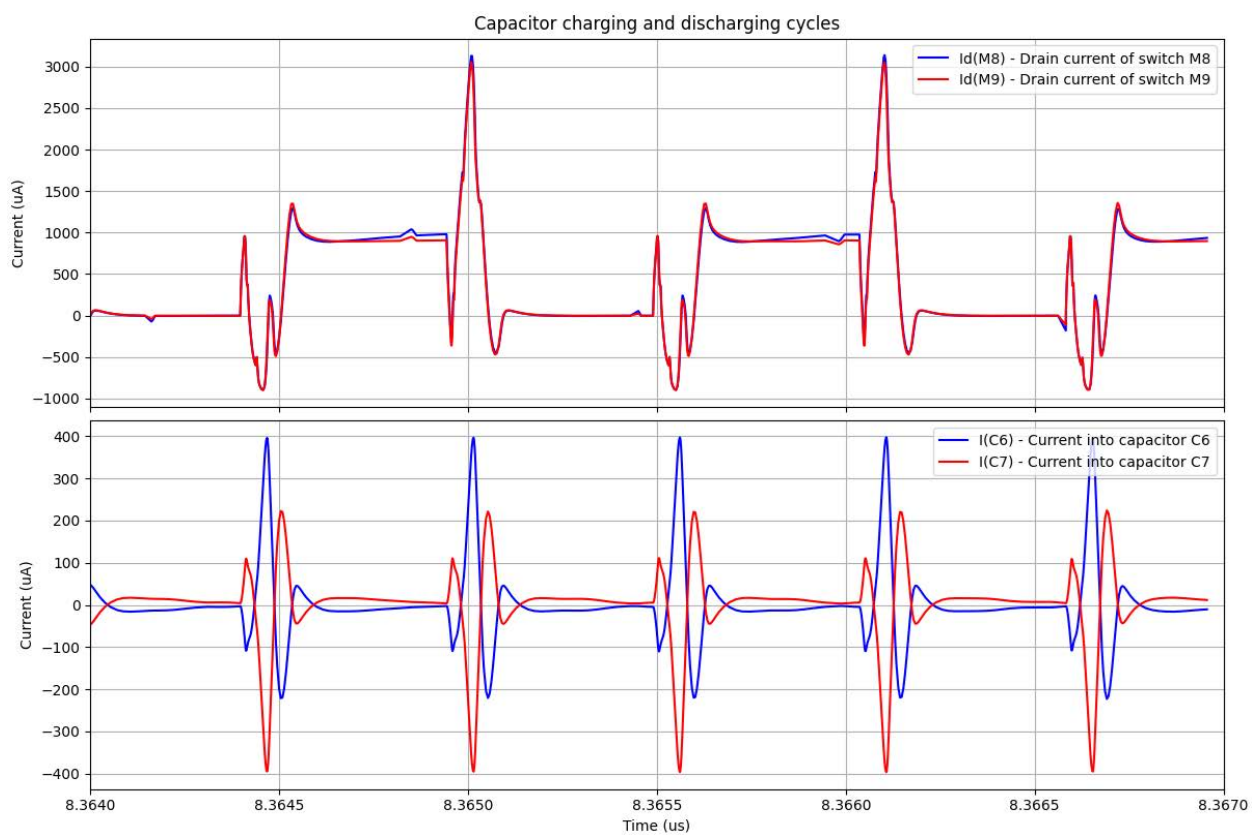


MACNALLY-SIM-FIG. 1.1 (clean). Macnally circuit simulation.



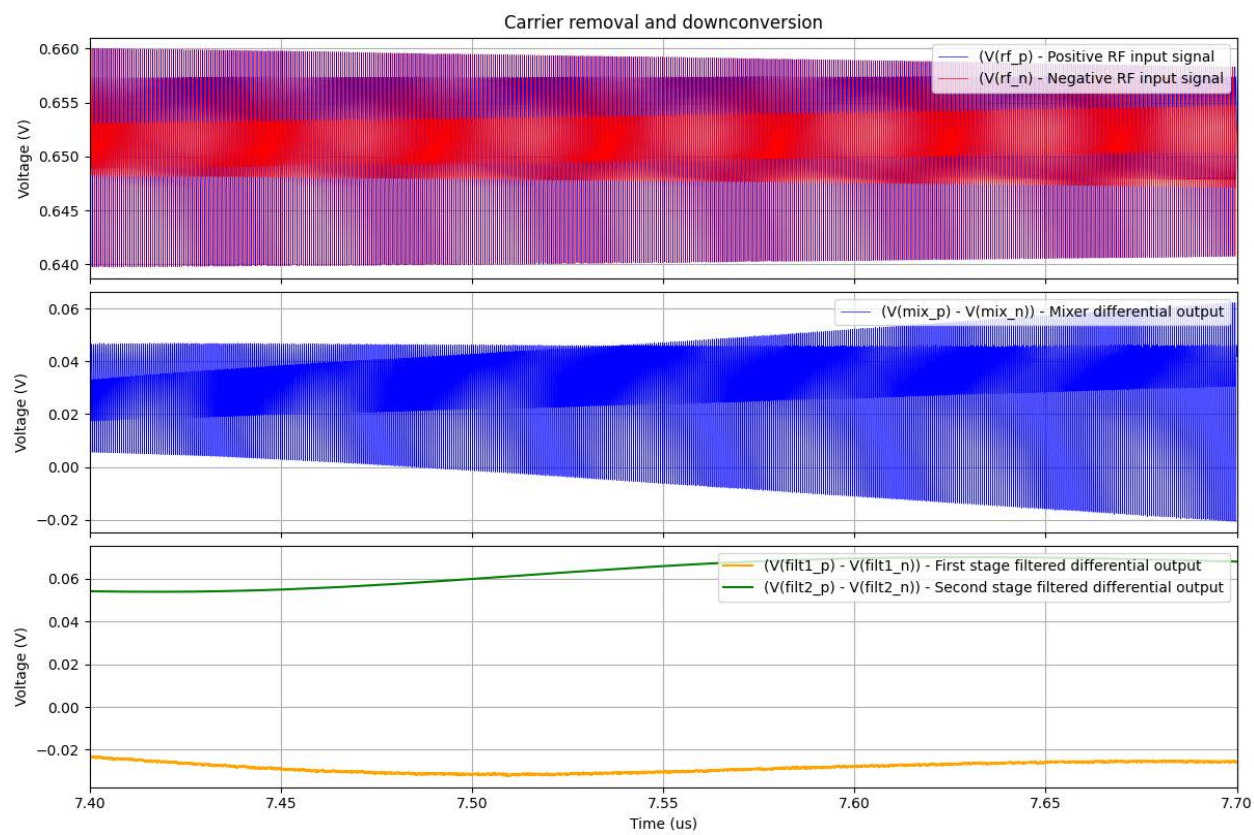
MACNALLY-SIM-FIG. 1.1 (annotated). Macnally circuit simulation.

147. MACNALLY-SIM-FIG. 2.1 is a graphical representation illustrating the charging and discharging cycles for capacitors C6 and C7 in the circuit of MACNALLY-SIM-FIG. 1.1.



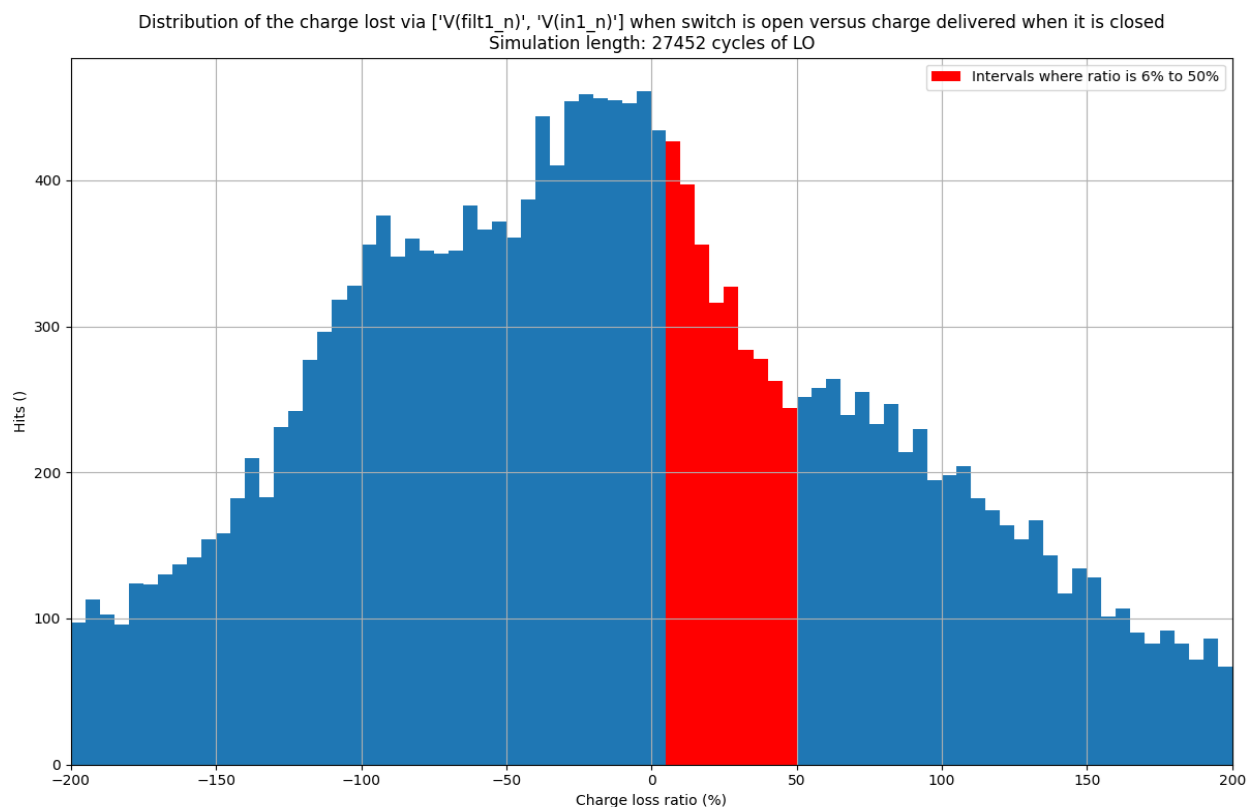
MACNALLY-SIM-FIG. 2.1. Capacitor charging and discharging cycles (circuit of MACNALLY-SIM-FIG. 1.1).

148. MACNALLY-SIM-FIG. 3.1 is a graphical representation of carrier removal and down-conversion for the circuit of MACNALLY-SIM-FIG. 1.1. MACNALLY-SIM-FIGS. 3 and 5 in the original Declaration include graphs from MACNALLY-SIM-FIG. 6. MACNALLY-SIM-FIG. 3.1 includes the same three types of graphs in MACNALLY-SIM-FIG. 6, but based on simulation output from MACNALLY-SIM-1.1.



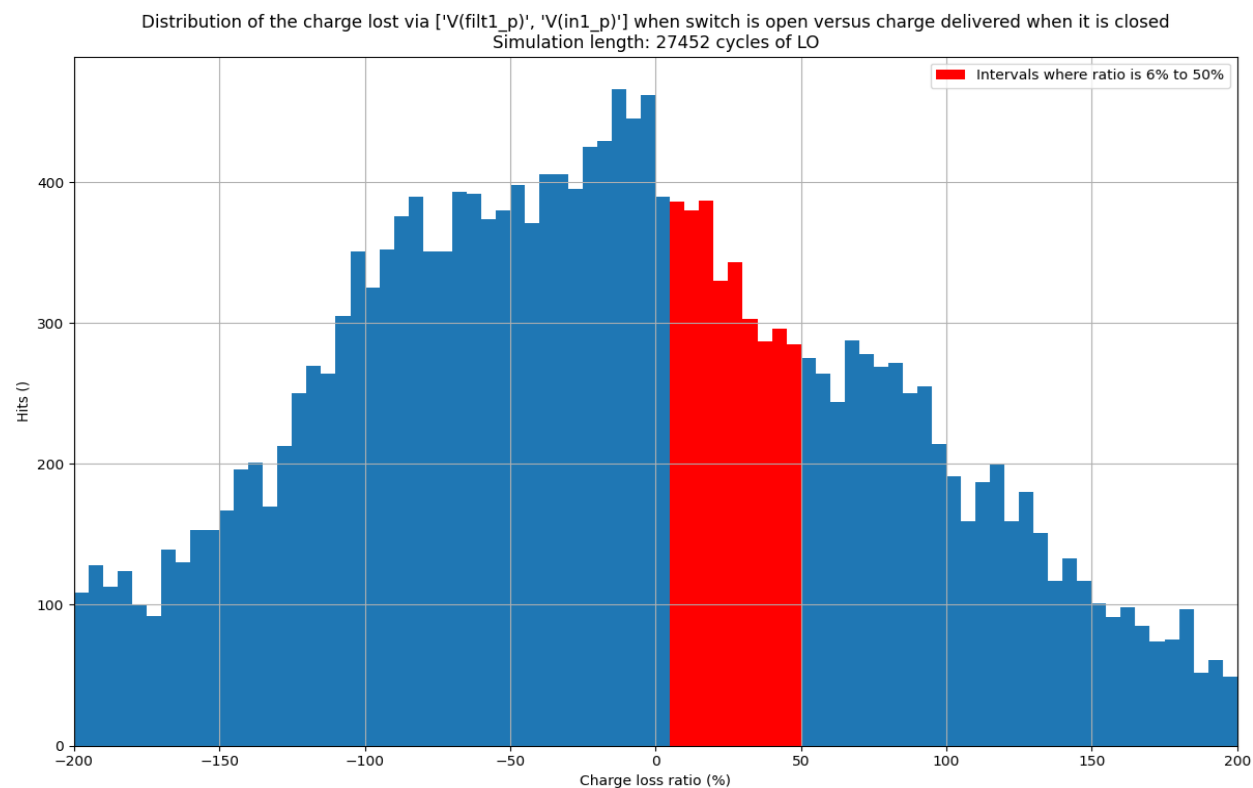
MACNALLY-SIM-FIG. 3.1. Carrier removal and down-conversion (circuit of MACNALLY-SIM-FIG. 1.1).

149. I my original Declaration, I provided one histogram of the charge loss ratio percentages that was representative of capacitors C6 and C7 (MACNALLY-SIM-FIG. 4). I have generated two histograms here; one for each capacitor MACNALLY-SIM-FIG. 4A and 4B. Everything I wrote in my original Declaration about MACNALLY-SIM-FIG. 4 is true of MACNALLY-SIM-FIG. 4A and 4B. MACNALLY-SIM-FIG. 4.1A is a histogram showing the charge loss ratio percentages for capacitor C6 for the circuit of MACNALLY-SIM-FIG. 1.1.



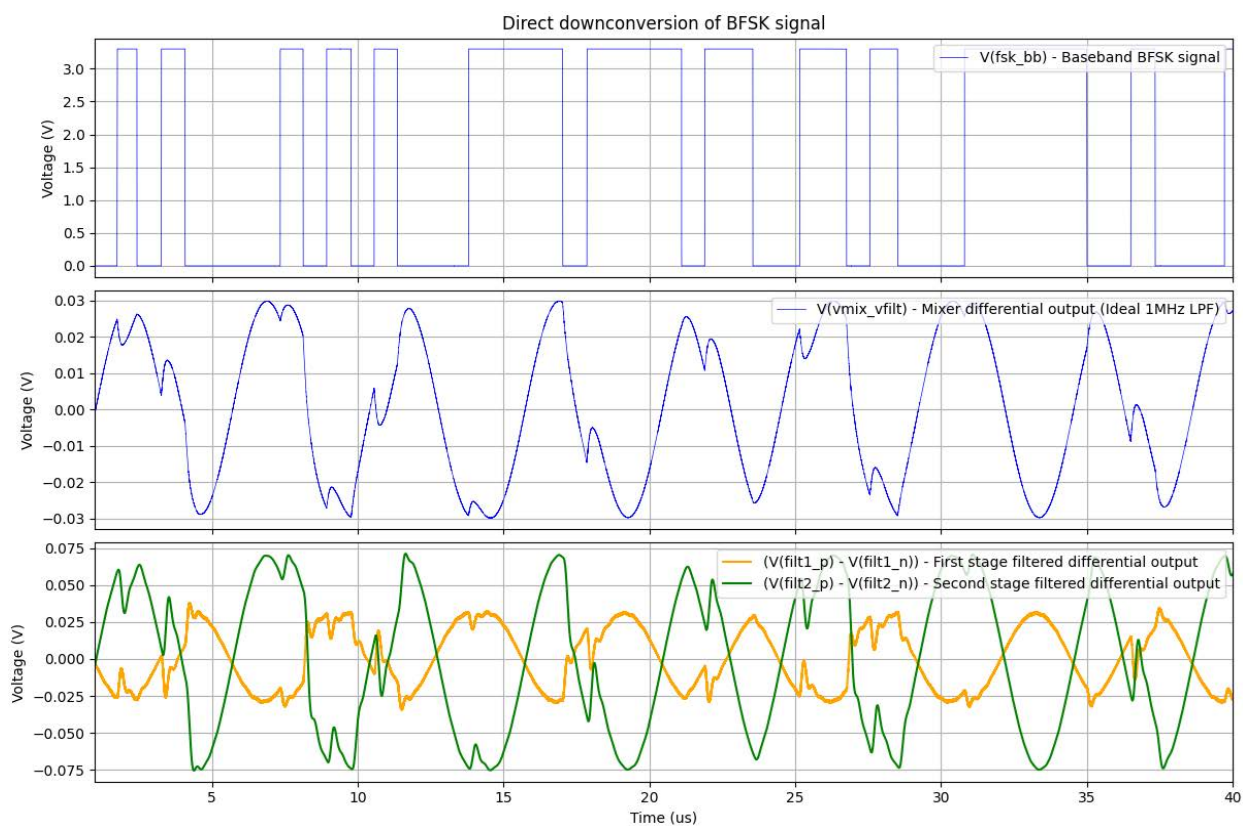
MACNALLY-SIM-FIG. 4.1A. Charge loss ratio percentages histogram for capacitor C6 (circuit of MACNALLY-SIM-FIG. 1.1).

150. MACNALLY-SIM-FIG. 4.1B is a histogram of the charge loss ratio percentages for capacitor C7 for the circuit of MACNALLY-SIM-FIG. 1.1.



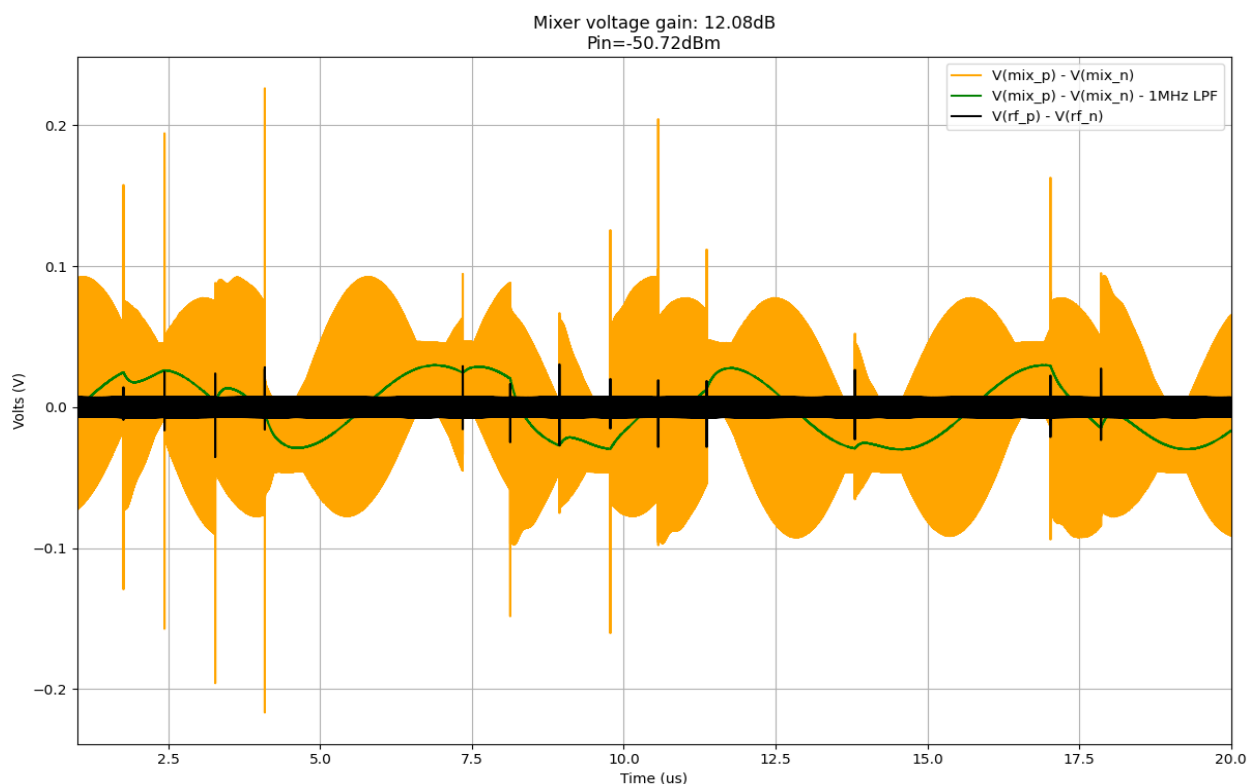
MACNALLY-SIM-FIG. 4.1B. Charge loss ratio percentages histogram for capacitor C7 (circuit of MACNALLY-SIM-FIG. 1.1).

151. MACNALLY-SIM-7.1 is a graphical representation of the generation of inverted information signal for the circuit of MACNALLY-SIM-FIG. 1.1.



MACNALLY-SIM-FIG. 7.1. Generation of inverted information signal (circuit of MACNALLY-SIM-FIG. 1.1).

152. MACNALLY-SIM-FIG. 8 is a graphical illustration of waveforms that demonstrate mixer gain of the circuit of MACNALLY-SIM-FIG. 1.1.



MACNALLY-SIM-FIG. 8. Waveforms which demonstrate mixer gain (circuit of MACNALLY-SIM-FIG. 1.1)

VIII. Changes to Simulator Settings and Post-Processing

A. Changes to Simulator Settings and Post-Processing Relative to Original Declaration

153. For each of the simulations provided above, the accuracy of the simulation results has been increased from those provided in the original Declaration by changing the default LTspice accuracy settings and by changes to the post-processing Python script. The changes to the default LTspice accuracy settings are as follows:

- The reltol parameter was tightened from the default value of 1e-3 to 1e-4.

- The numdgt parameter was increased from the default value of 6 significant digits to 12 significant digits. This does not affect the simulator's internal precision, but it increases the number of significant digits used when exporting waveform data to text files.
- The plotwinsize parameter was set to zero. By default, LTspice applies a post-processing step to the simulated waveforms before exporting data to a file. The goal of this post-processing is to reduce data file size by selectively discarding data points according to LTspice's algorithm, at the expense of waveform accuracy. By setting this parameter to 0, we have disabled the post-processing, ensuring maximum accuracy.

154. The accuracy of the simulation results was further increased by changing how charge integration is calculated during Python script postprocessing. In the original Python script, capacitor charge delivered over a time interval was computed by numerically integrating the capacitor current waveforms. Any numerical integration of the data is subject to the accumulation of rounding errors. Thus, rather than numerically integrating the capacitor current over a time interval, the modified Python script uses the difference between the capacitor voltage at the end and the start of the time interval, which are related by the integral of the capacitor equation, $I=CdV/dt$. This is more precise, especially for Macnally, which has much sharper current waveforms. The changes in the modified Python script had little

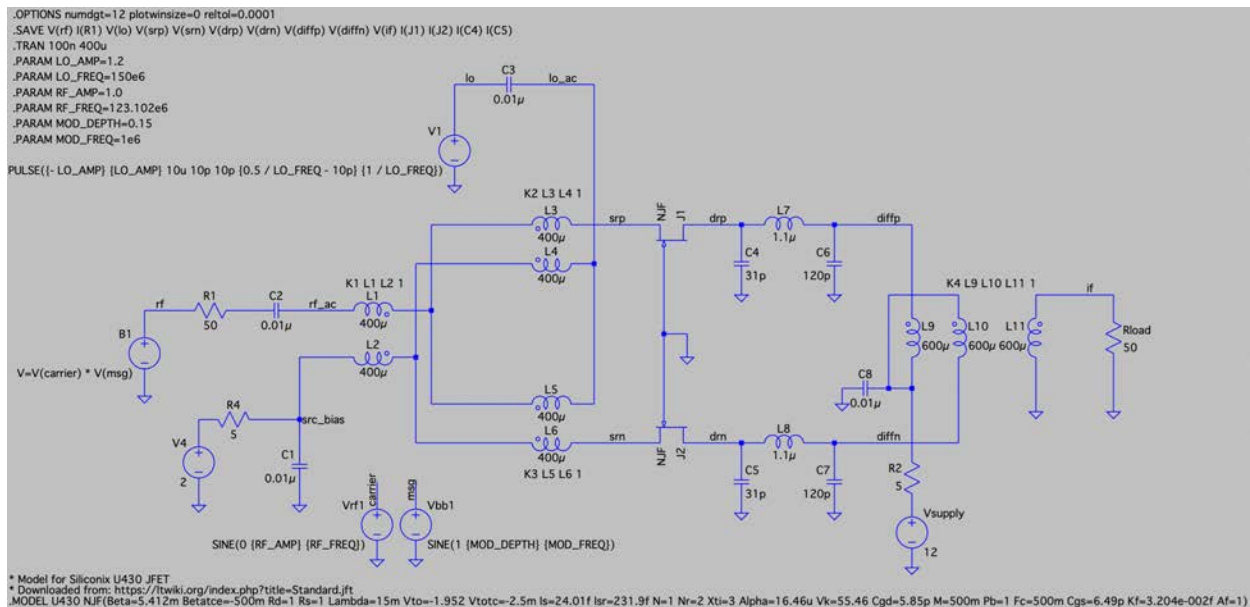
effect on the DeMaw simulations, and in neither case did it lead to different conclusions than were presented in the original Declaration.

155. A bug was found in the original Python script used to post-process the simulation results from the Macnally circuit (there was no corresponding bug for the DeMaw circuit simulations) in the original Declaration. Specifically, for only the MacNally histograms, the computed charge removed from the capacitors while the switch is off was accidentally sign-flipped. As a result, the percentage range plotted $[0, 200]$ corresponds to the range $[0, -200]$. This bug has been corrected.

156. None of the differences described above change the conclusions presented in my original Declaration. To demonstrate this point, the remainder of this section presents simulation results from my original Declaration juxtaposed with the same results except using the LTspice parameter and Python script changes described above.

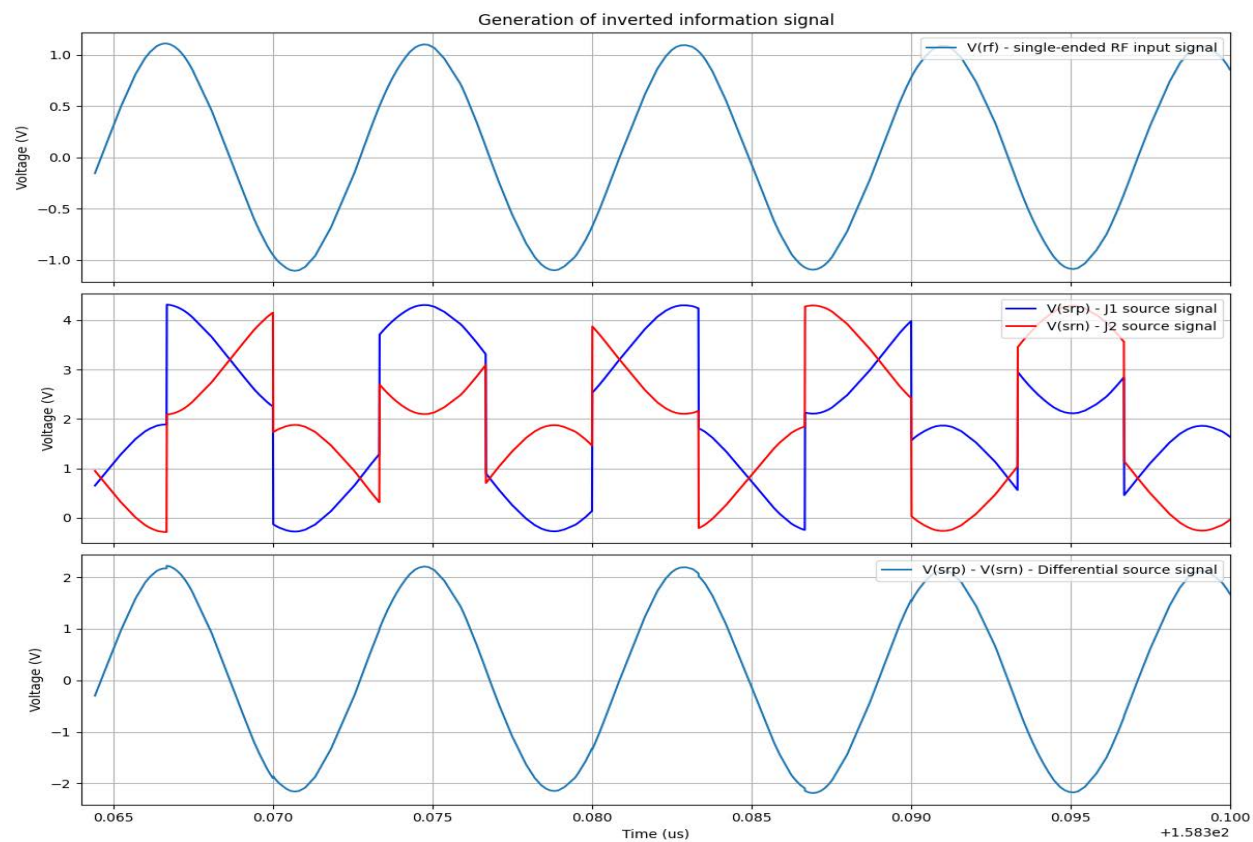
B. Original DeMaw Simulation With/Without Revised Simulator Settings and Post-Processing

157. DEMAW-SIM-FIG. 1 (different settings) is a schematic diagram of the simulated DeMaw circuit from the original Declaration with revised simulator accuracy settings. DEMAW-SIM-FIG. 1 (different settings) maintains the default, generic LTspice JFET models.



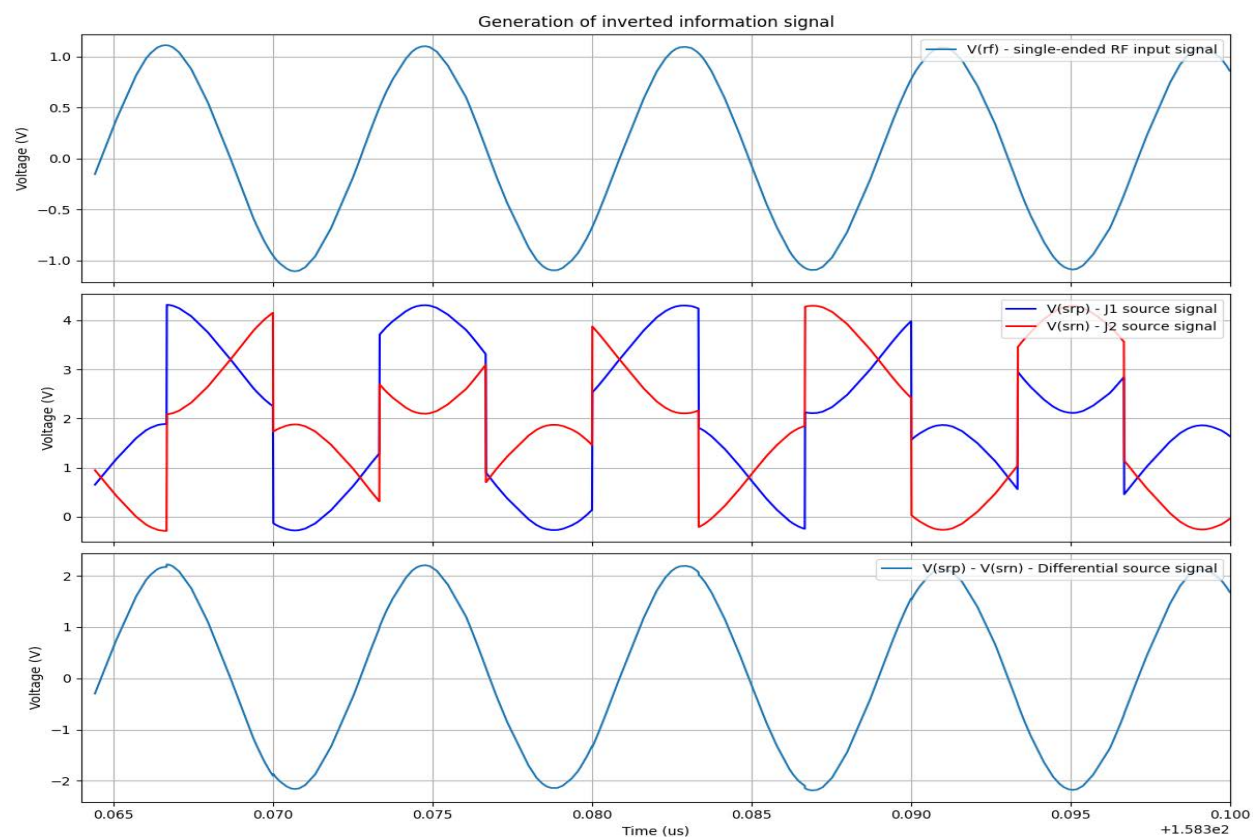
DEMAW-SIM-FIG. 1 (different sim settings) is a schematic diagram of the simulated DeMaw circuit from the original Declaration with revised simulator accuracy settings.

158. DEMAW-SIM-FIG. 4 is a graphical representation of the generation of inverted information signal for the DeMaw circuit from the original Declaration, further including the V(rf) and V(srp)-V(sm) graphs generated for DEMAW-SIM-FIG. 1.



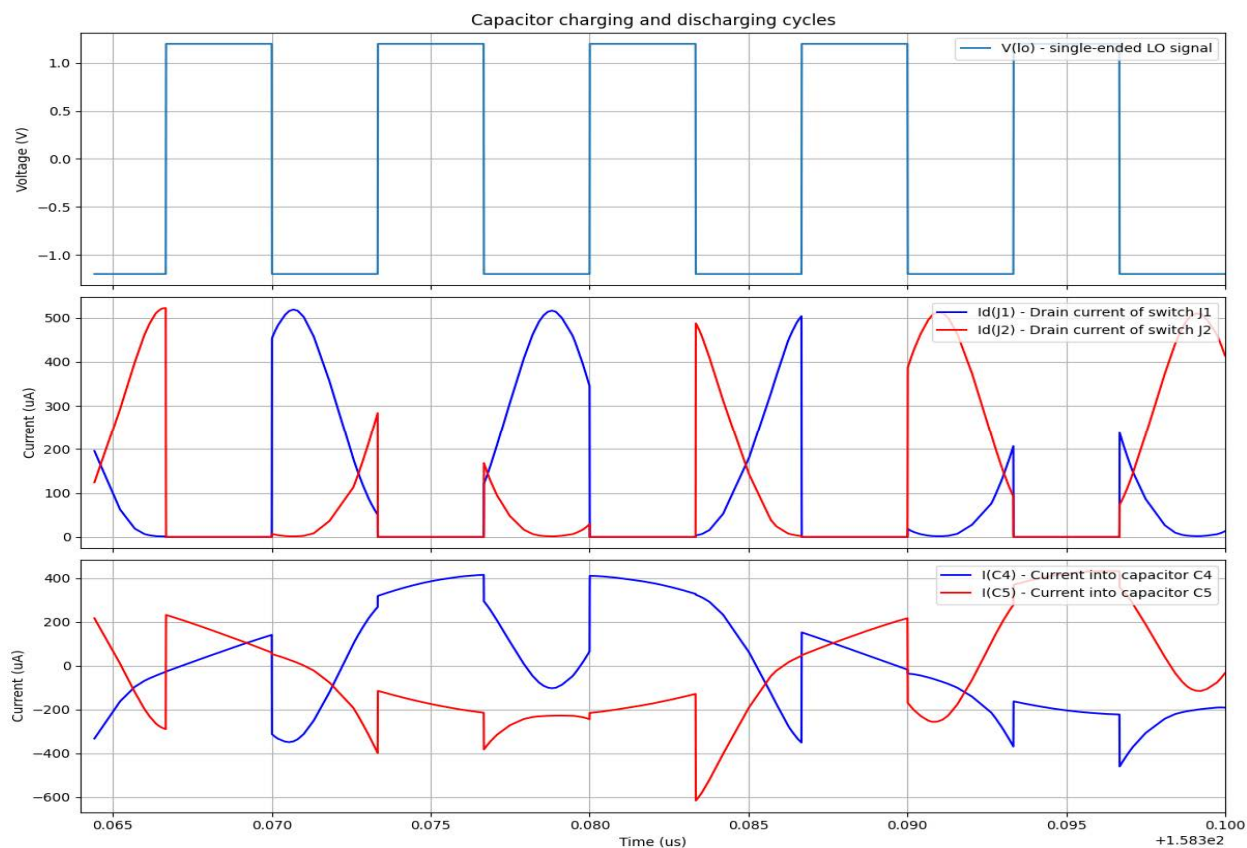
DEMAW-SIM-FIG. 4. Generation of inverted information signal (DeMaw circuit from the original Declaration).

159. DEMAW-SIM-FIG. 4 (different sim settings) is a graphical representation showing the generation of inverted information signal for the circuit of DEMAW-SIM-FIG. 1 (different sim settings).



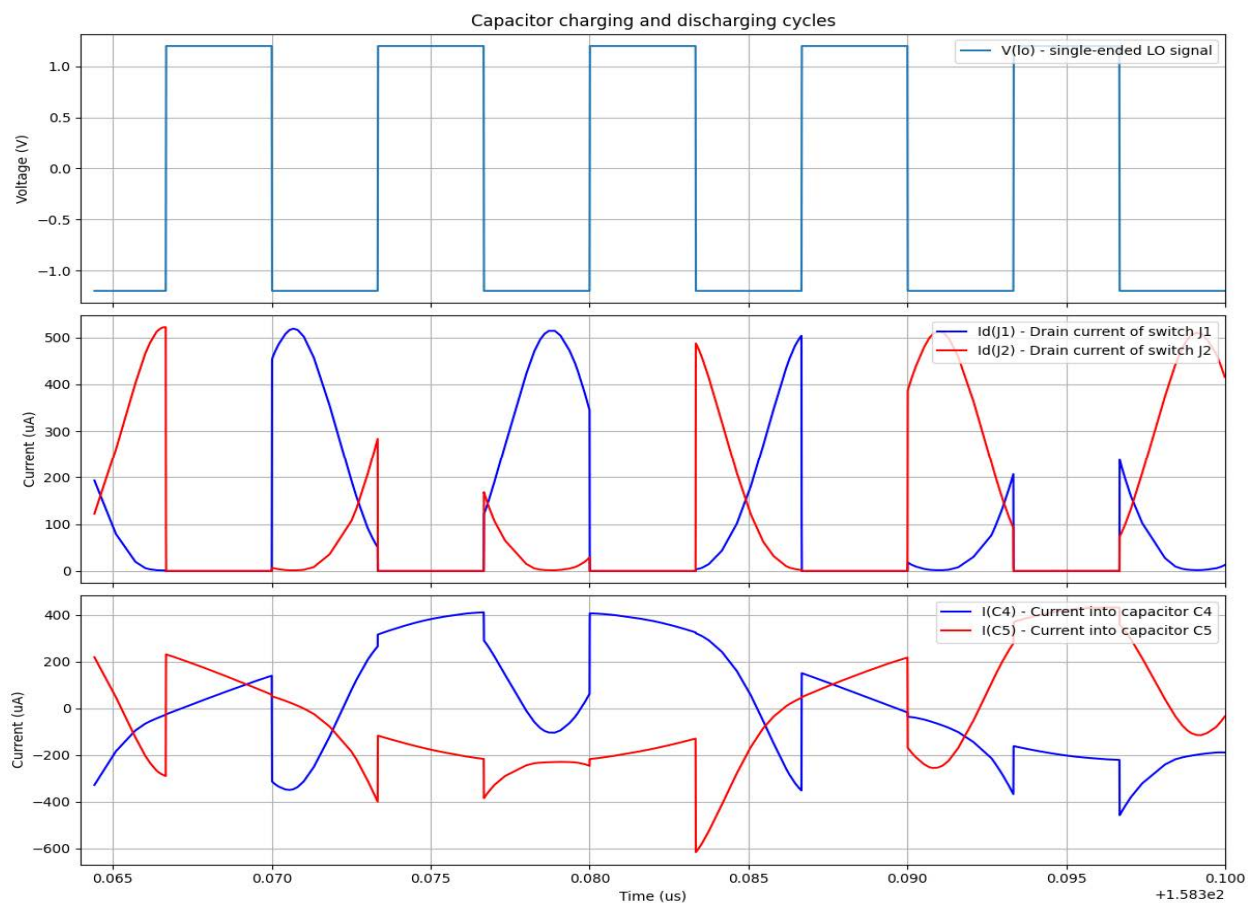
DEMAW-SIM-FIG. 4 (different sim settings). Generation of inverted information signal (circuit of DEMAW-SIM-FIG. 1(different sim settings)).

160. DEMAW-SIM-FIG. 5 is a graphical representation illustrating the charging and discharging cycles for capacitors C4 and C5 in the DeMaw circuit from the original Declaration.



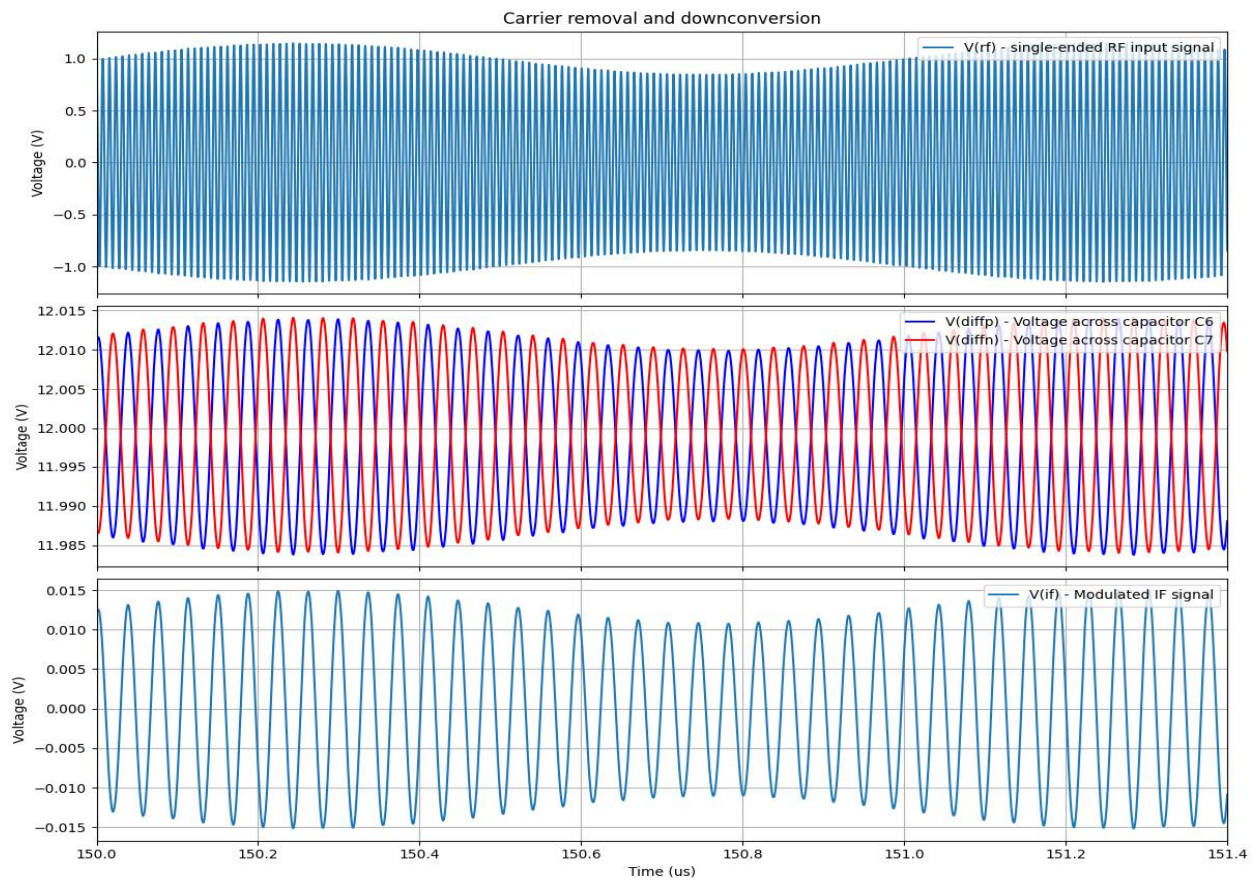
DEMAW-SIM-FIG. 5. Capacitor charging and discharging cycles (DeMaw circuit from the original Declaration).

161. DEMAW-SIM-FIG. 5 (different sim settings) is a graphical representation illustrating the charging and discharging cycles for capacitors C4 and C5 in the circuit of DEMAW-SIM-FIG. 1 (different sim settings).



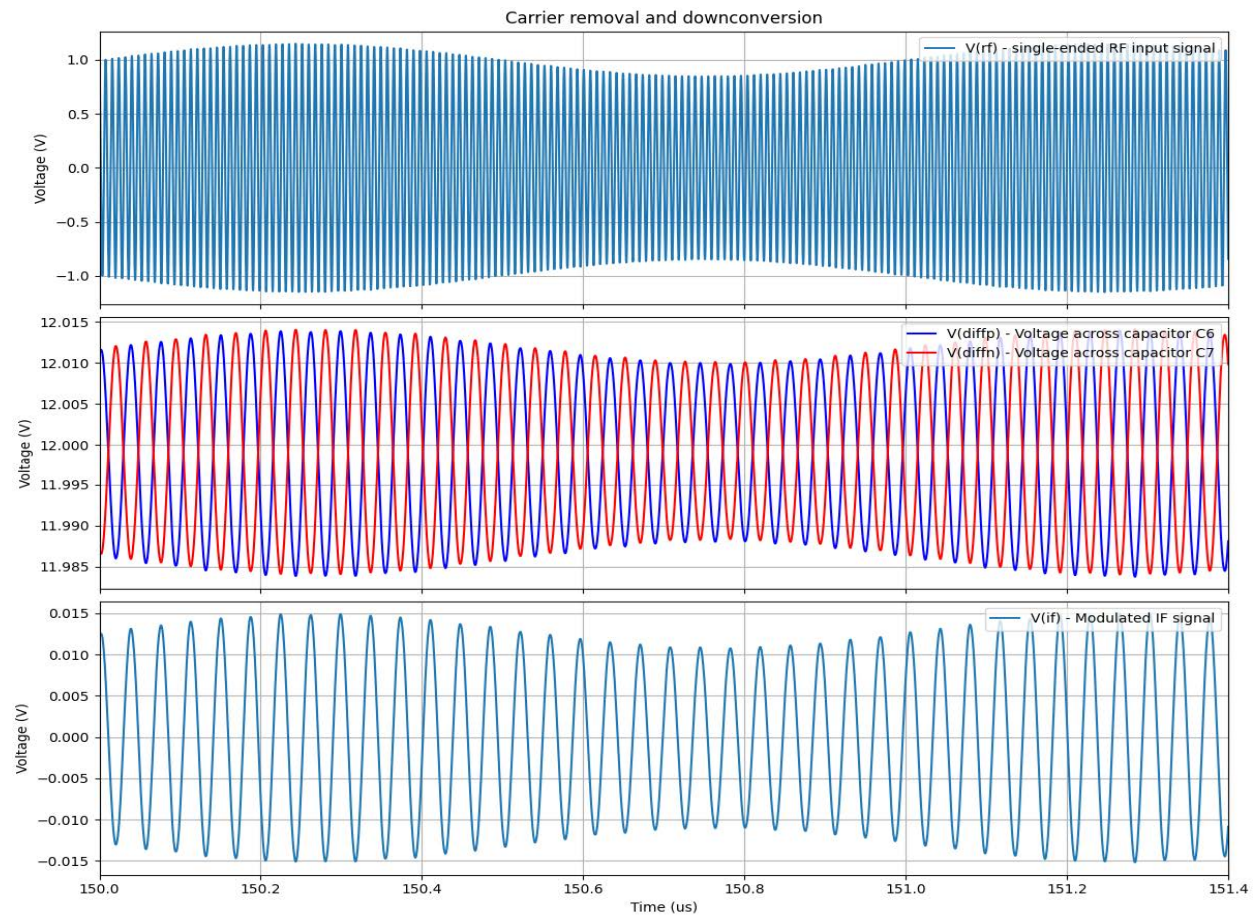
DEMAW-SIM-FIG. 5 (different sim settings). Capacitor charging and discharging cycles (circuit of DEMAW-SIM-FIG. 1 (different sim settings)).

162. DEMAW-SIM-FIG. 6 is a graphical representation of carrier removal and down-conversion for the DeMaw circuit from the original Declaration.



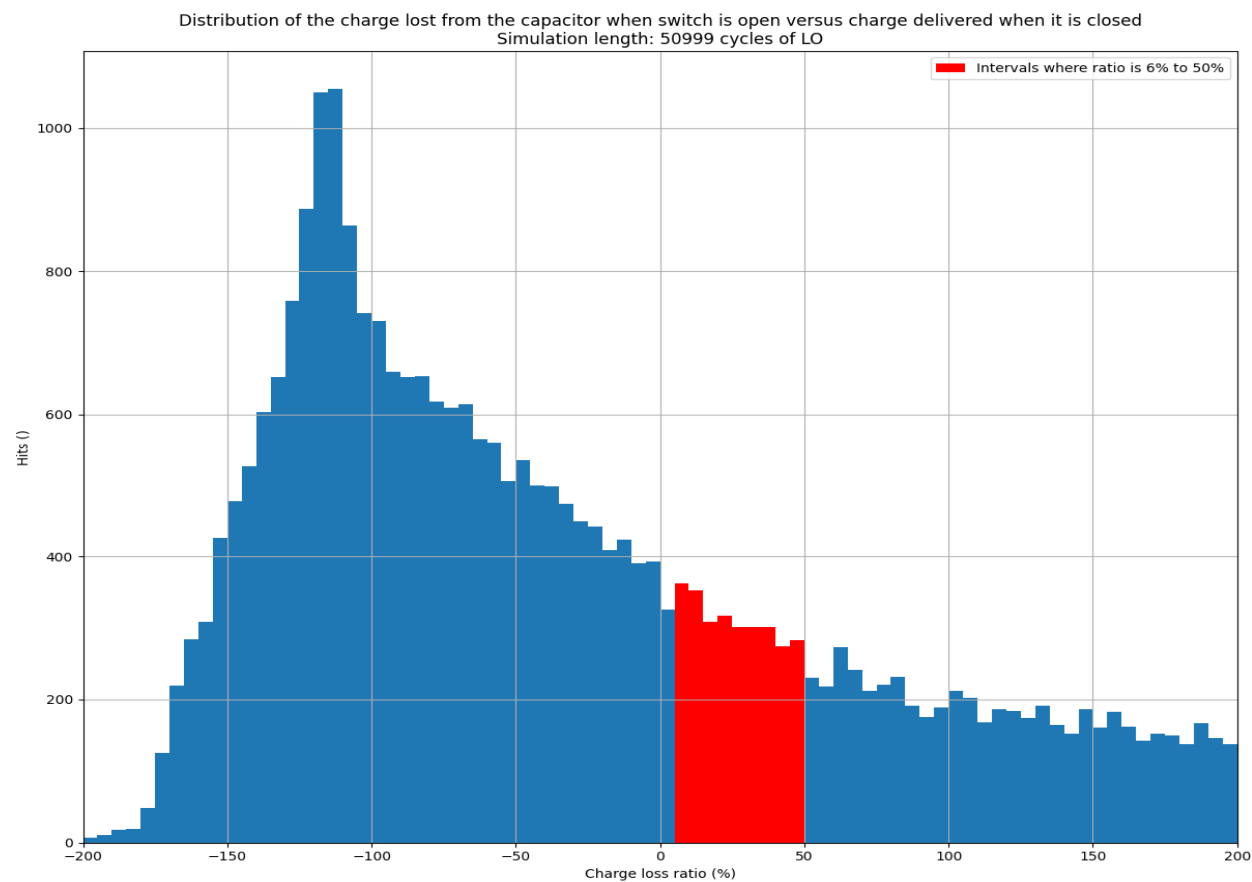
DEMAW-SIM-FIG. 6. Carrier removal and down-conversion (DeMaw circuit from the original Declaration).

163. DEMAW-SIM-FIG. 6 (different sim settings) is a graphical representation of carrier removal and down-conversion for the circuit of DEMAW-SIM-FIG. 1 (different sim settings).



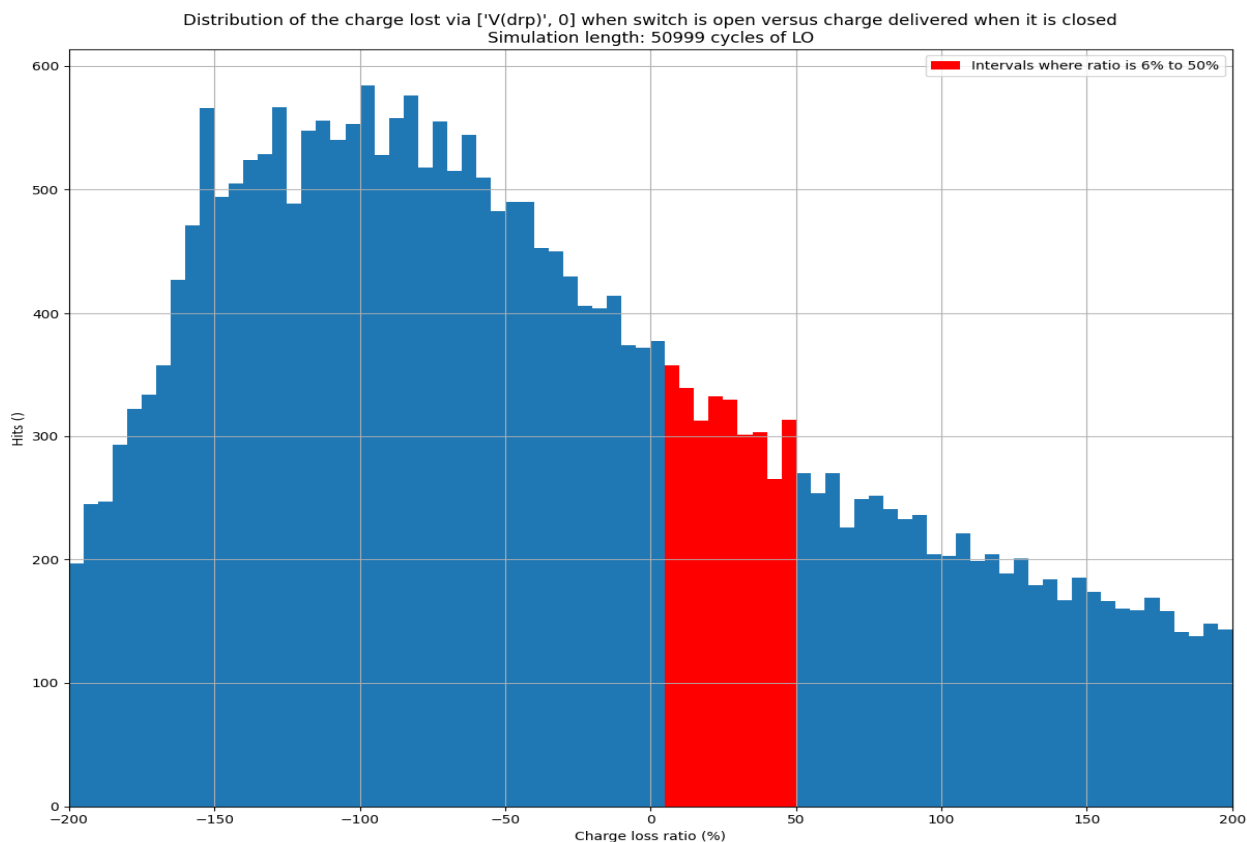
DEMAW-SIM-FIG. 6 (different sim settings). Carrier removal and down-conversion (circuit of DEMAW-SIM-FIG. 1 (different sim settings)).

164. DEMAW-SIM-FIG. 7 is a histogram of the charge loss ratio percentages for capacitor C4 for the DeMaw circuit from the original Declaration.



DEMAW-SIM-FIG. 7. Charge loss ratio percentages histogram for capacitor C4 (DeMaw circuit from the original Declaration).

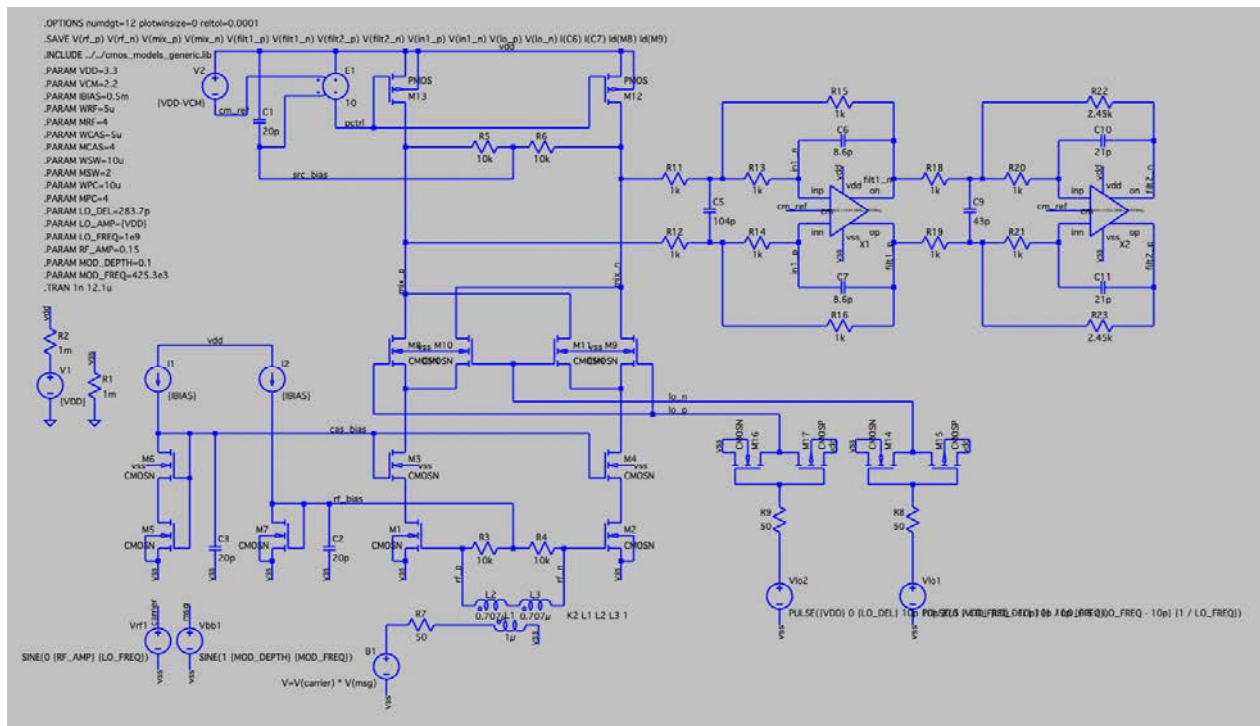
165. DEMAW-SIM-FIG. 7 (different sim settings) is a histogram of the charge loss ratio percentages for capacitor C4 for the circuit of DEMAW-SIM-FIG. 1 (different sim settings).

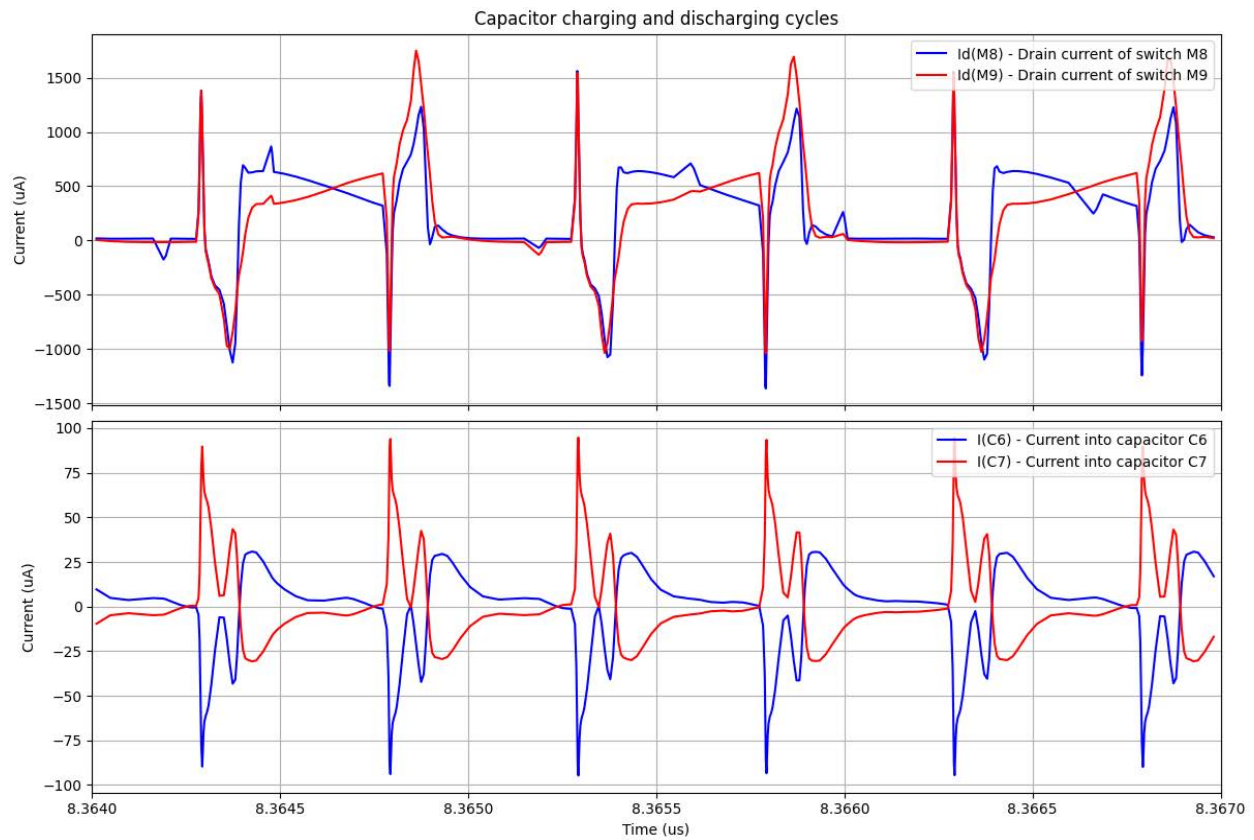


DEMAW-SIM-FIG. 7. Charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1 (different sim settings)).

C. Original Macnally Simulation With/Without Revised Simulator Settings and Post-Processing

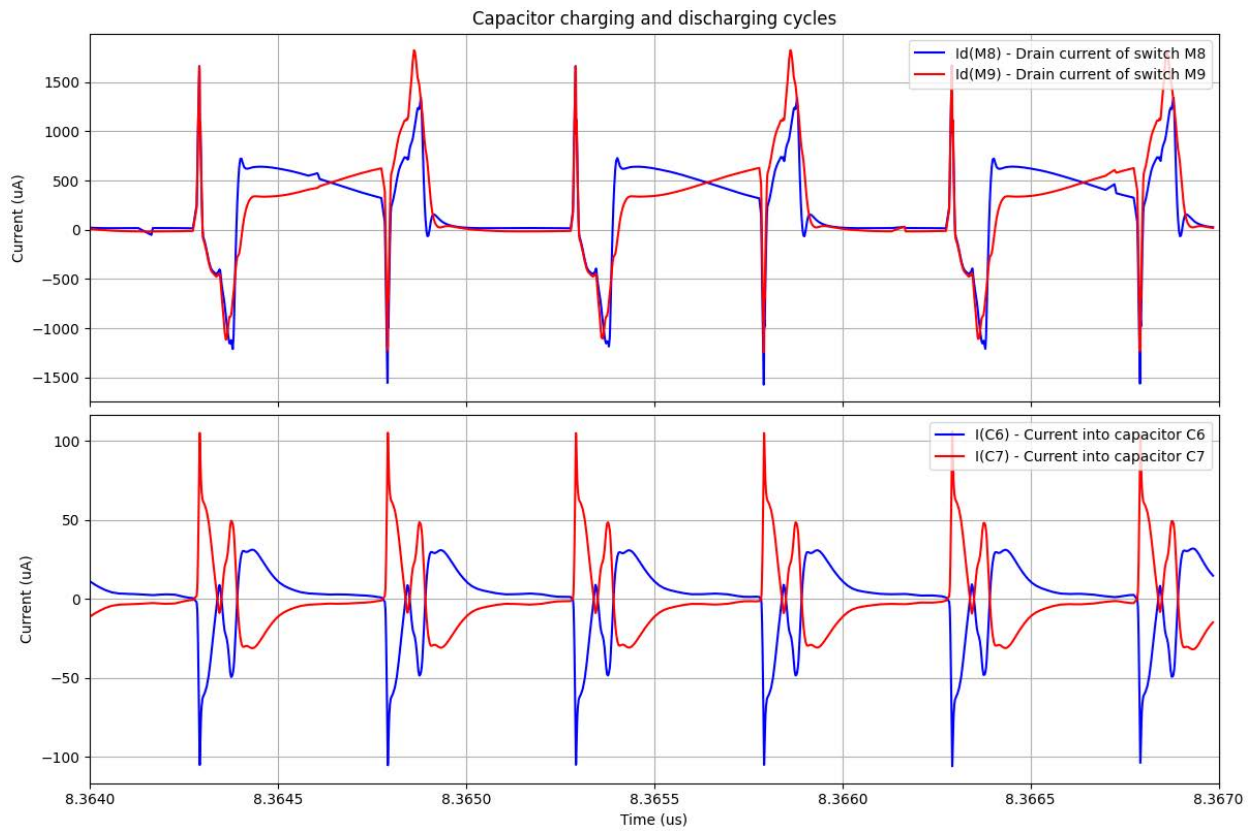
166. MACNALLY-SIM-FIG. 1 (different sim settings) is a schematic diagram of the simulated Macnally circuit from the original Declaration with revised simulator accuracy settings.





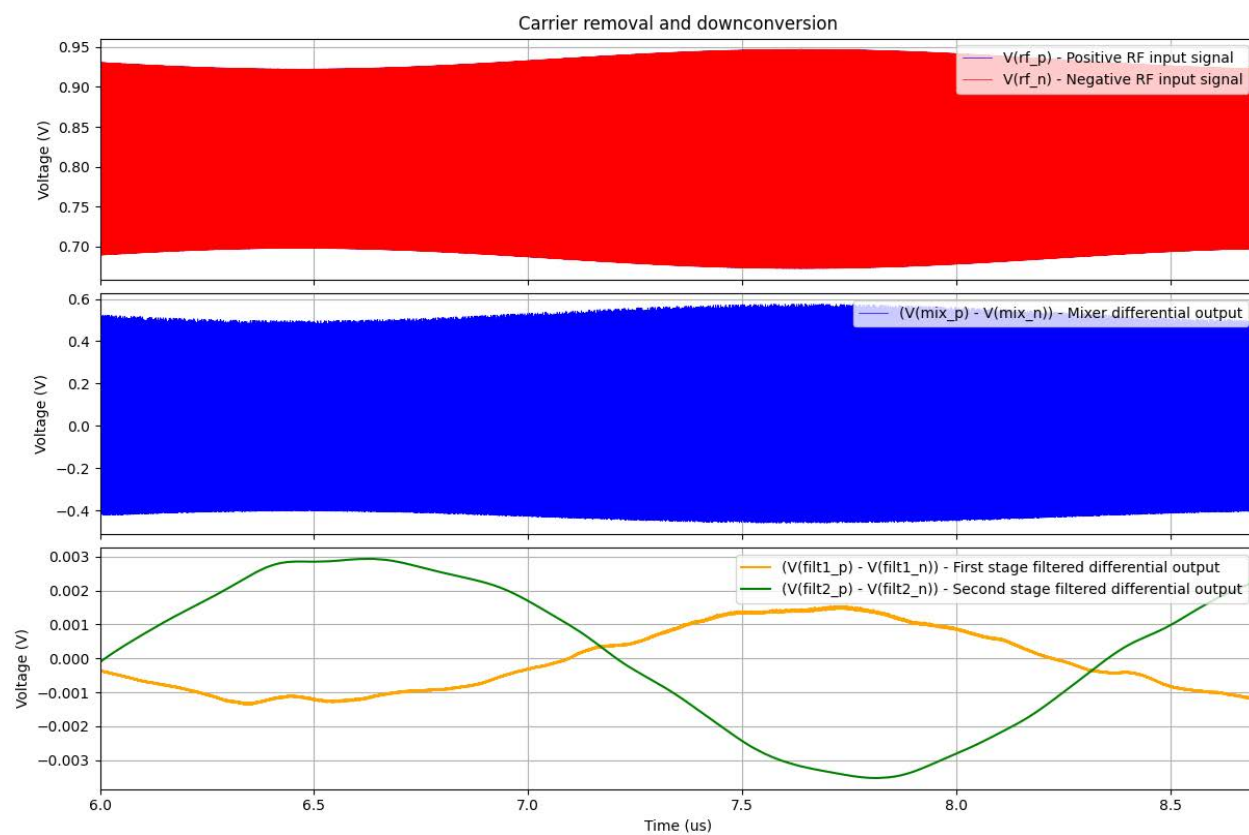
MACNALLY-SIM-FIG. 2. Capacitor charging and discharging cycles (Macnally circuit from the original Declaration).

168. MACNALLY-SIM-FIG. 2 (different sim settings) is a graphical representation illustrating charging and discharging cycles for capacitors C6 and C7 of the circuit of MACNALLY-SIM-FIG. 1 (different sim settings).



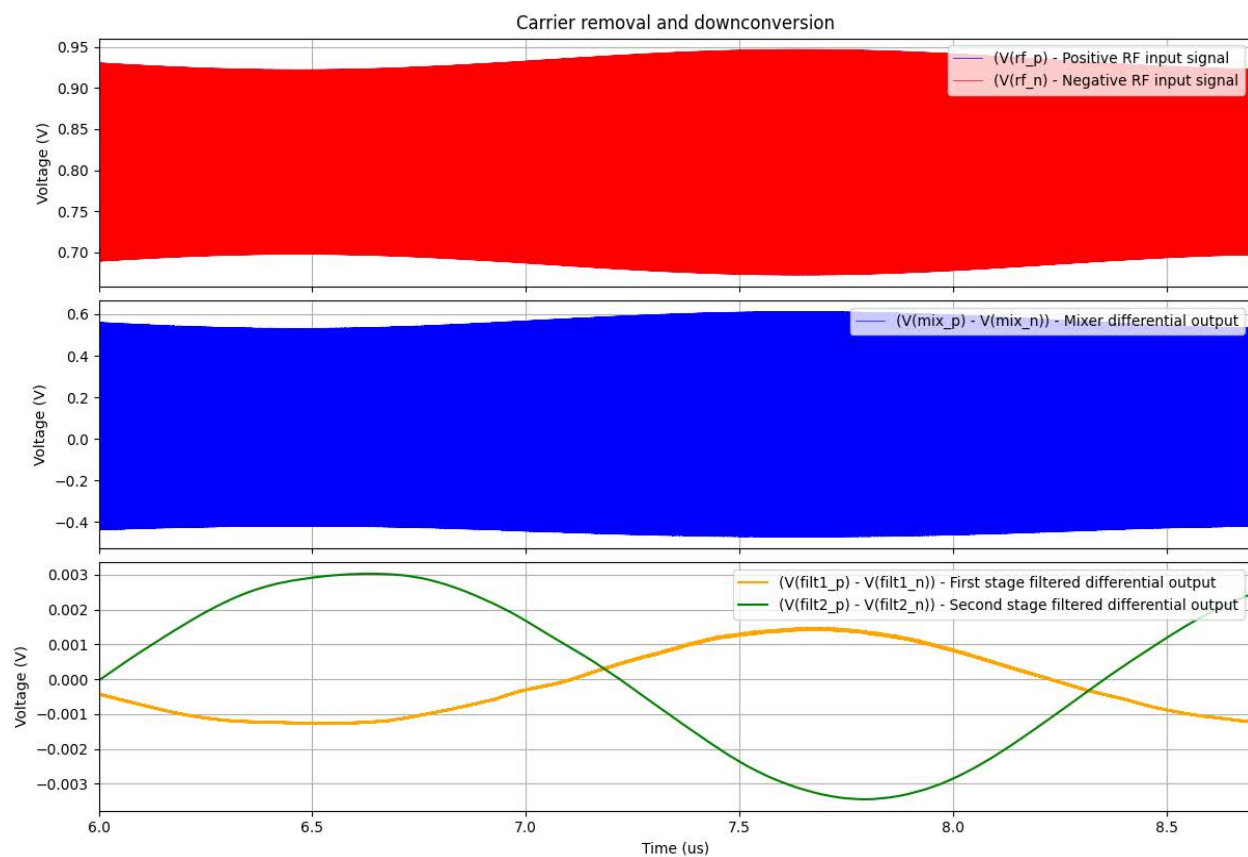
MACNALLY-SIM-FIG. 2 (different sim settings). Capacitor charging and discharging cycles (circuit of MACNALLY-SIM-FIG. 1 (different sim settings)).

169. MACNALLY-SIM-FIG. 6 is a graphical representation of carrier removal and down-conversion from the Macnally circuit from the original Declaration.



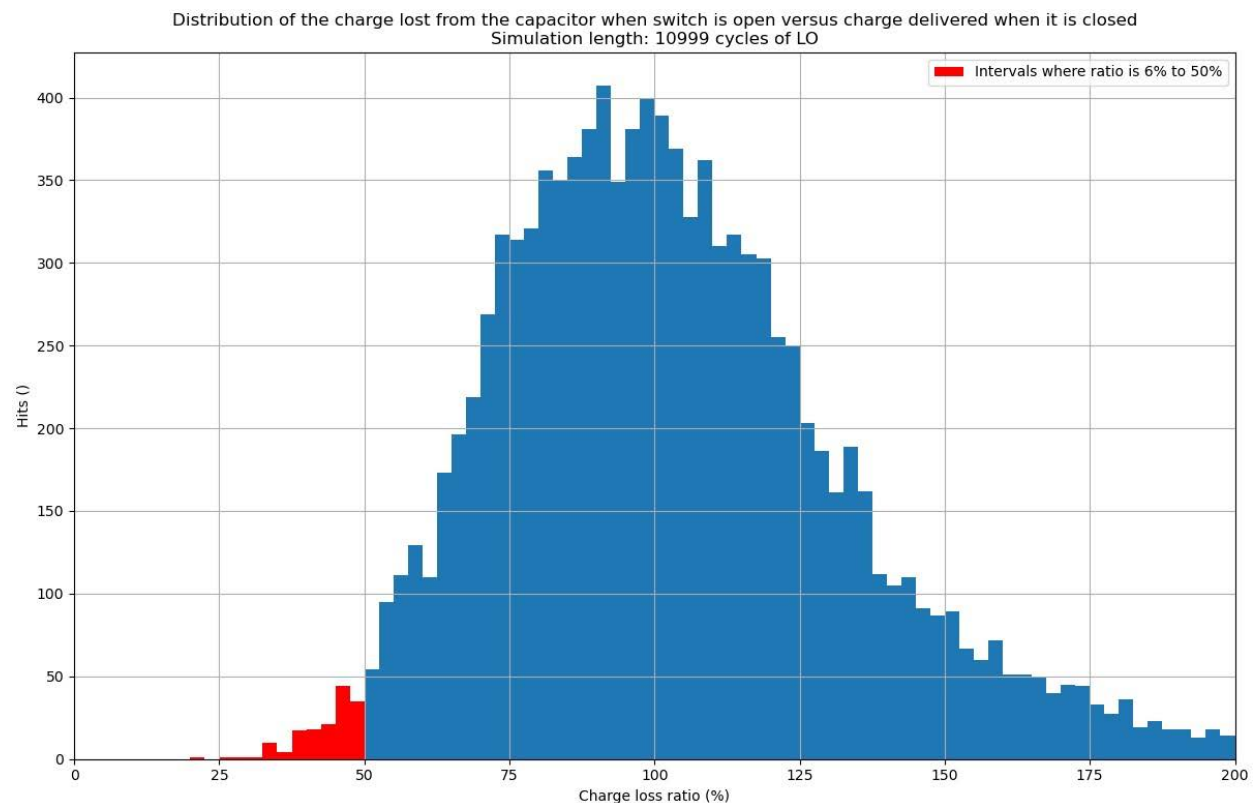
MACNALLY-SIM-FIG. 6. Carrier removal and down-conversion (Macnally circuit from the original Declaration).

170. MACNALLY-SIM-FIG. 6 (different sim settings) is a graphical representation of the carrier removal and down-conversion for the circuit of MACNALLY-SIM-FIG. 1 (different sim settings).



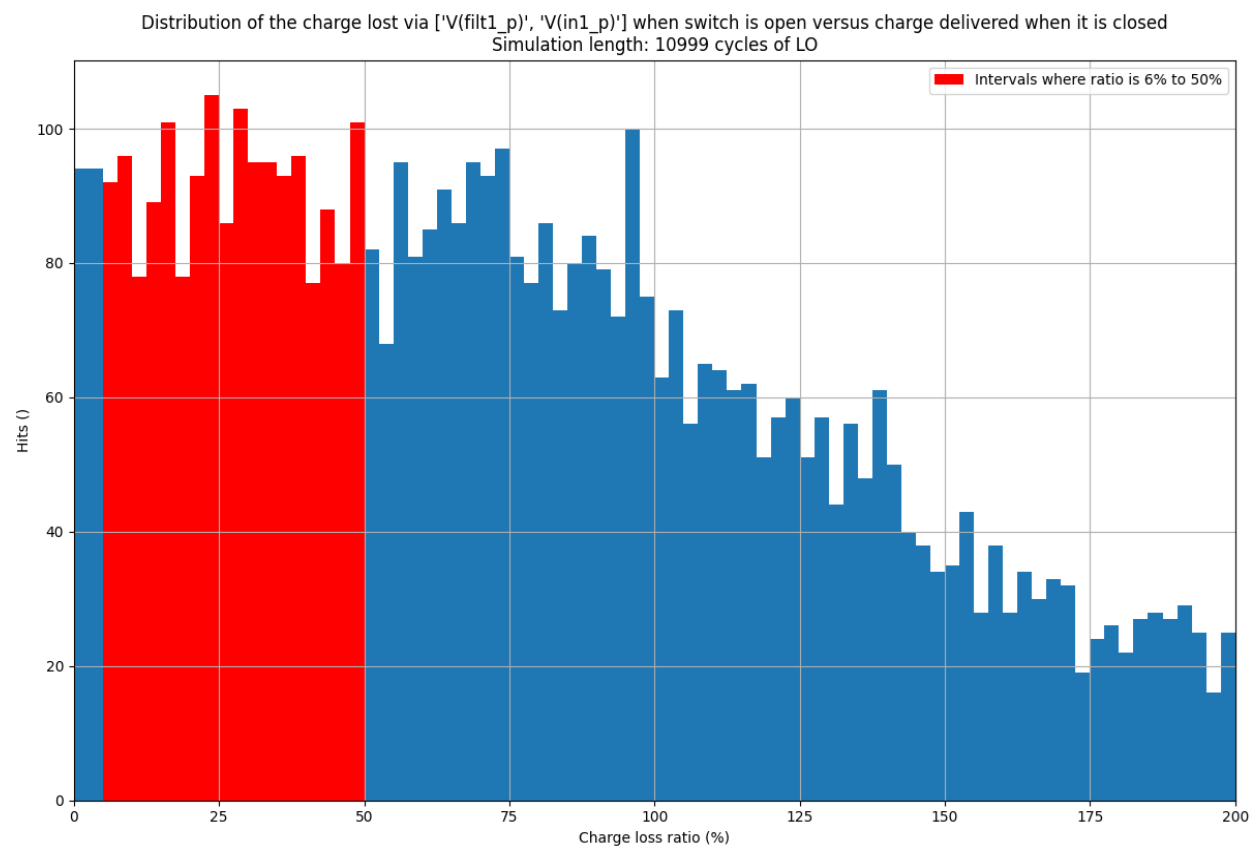
MACNALLY-SIM-FIG. 6 (different sim settings). Carrier removal and down-conversion (circuit of MACNALLY-SIM-FIG. 1 (different sim settings)).

171. MACNALLY-SIM-FIG. 4 is a histogram of charge loss ratio percentages for capacitor C6 from the Macnally circuit from the original Declaration generated using the improved Python script.



MACNALLY-SIM-FIG. 4. Charge loss ratio percentages histogram for capacitor C6 (Macnally circuit from the original Declaration).

172. MACNALLY-SIM-FIG. 4 (different sim settings) is a histogram of the charge loss ratio percentages for capacitor C6 from the circuit of MACNALLY-SIM-FIG. 1 (different sim settings).



MACNALLY-SIM-FIG. 4 (different sim settings). Charge loss ratio percentages histogram for capacitor C6 (circuit of MACNALLY-SIM-FIG. 1 (different sim settings)).

IX. Additional Remarks

173. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

174. I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both under Section 1001 of Title 18 of the United States Code.

Dated: March 17, 2024

By: /Dr. Ian Galton /

Dr. Ian Galton