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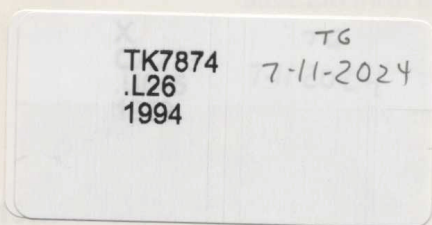
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Example 2-13

What is the cutoff frequency for a 1 k Ω resistor, realized in p -base diffusion with $R_R = 130 \Omega/\square$ and $C_R = 0.2 \text{ pF}/\square$. Calculate the frequency at which the parasitic capacitance causes a phase shift of 10° with respect to low frequencies.

Solution. For 1 k Ω , 8 squares are needed. As a result, $f_{RC} = 15 \text{ GHz}/(L/W)^2$ or $15 \text{ GHz}/64 = 230 \text{ MHz}$. A phase shift of 10° is reached at the frequency f_{10} where $t_g(10^\circ) = f_{10}/f_{RC}$ or at about 40 MHz.

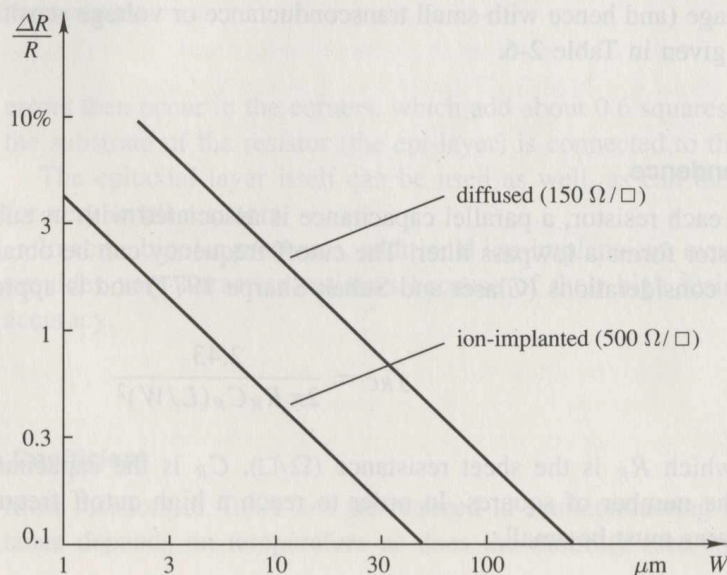
2-9-6 Absolute and Relative Accuracy

To realize a resistor with absolute accuracy is difficult, but layout tricks can be applied to reduce the uncertainties. For example, the contact and corner areas can be covered with $p+$ islands. Nevertheless, good design must never be based on absolute values. Relative values such as resistor ratios must be used. The relative errors obtained are about one-tenth of the absolute accuracies given in Table 2-6. Obviously, the larger the dimensions, the better the relative accuracy that can be achieved.

This is illustrated in Fig. 2-31 for both diffused (base diffusion: $150 \Omega/\square$) resistors. The relative accuracy improves more or less proportionally to the resistor width. Moreover, the relative error is approximately a factor of three smaller for ion-implanted devices than for diffused ones. In order to reach a relative error of 0.1 percent, ion-implanted resistances must be taken with about $40 \mu\text{m}$ width.

Many other layout tricks (see Sec. 6-7) can be applied to improve matching.

FIGURE 2-31 Matching of resistors with width W .



2-9-7 Resistors in a CMOS Process

In a conventional n -well CMOS process, several resistances are available. They are the source/drain resistance, the polysilicon gate and the n -well region. However, none of these are intended to be used as a resistor. The control on the accuracy of the resistivity is very poor (see Table 2-6). An analog CMOS process quite often includes an additional polysilicon resistor with excellent properties. Its temperature and voltage coefficient are then low as well.

2-9-8 Thin Film Resistors

On top of a chip, a thin-film resistor can be easily deposited. Actually, the aluminium metallization layer is such a resistor, albeit with very low resistivity. A higher resistivity is obtained with NiCr or Ta, which yield values from 100 to 4 k $\Omega/\square$. The control on its resistivity is excellent and so are its temperature and voltage coefficient. This is why they are used for very high precision circuits and for circuits at very high frequencies.

2-9-9 Capacitors

In a bipolar process, junction capacitance is available at each junction. The most useful is the collector-base junction capacitance (see Table 2-7), shown in Fig. 2-32. It is not very accurate, however, and it is very voltage dependent (see Table 1-5). This applies to all other junction capacitances as well.

Note that the capacitance on the bottom side is always connected by a parasitic capacitance C_p to the substrate. This capacitance is always a fixed fraction of the useful capacitance and cannot be avoided.

Much more accuracy can be obtained with a MOS capacitance in a CMOS process (see Fig. 2-33). Not only is its value larger, but its accuracy is much higher, especially for the poly-to-poly capacitance. Also, the temperature and voltage coefficients are quasi-nihil. Its parasitic capacitance from the bottom plate to ground is decreased to

TABLE 2-7 CAPACITORS

Process	Type	C nF/cm ²	absolute accuracy percent	temperature coefficient percent/°C	voltage coefficient percent V	breakdown voltage V
Bipolar	C_{CB}	16	10	0.02	2	50
	C_{EB}	50	10	0.02	1	7
	C_{CS}	8	20	0.01	0.5	60
CMOS	$C_{ox}(50 \text{ nm})$	70	5	0.002	0.005	40
	$C_{m,poly}$	12	10	0.002	0.005	40
	$C_{poly,poly}$	56	2	0.002	0.005	40
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20
	$C_{m,substrate}$	5.2	10	0.01	0.05	20
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20

Many of the parasitic C 's, namely, C_{GS} , C_{GD} , C_{jD} , and C_{jS} , are associated with the MOST model described in Chap. 1. The expressions for each, in the three MOST operating regions, are summarized in Table 8-1. Source and drain-to-bulk capacitances C_{jS} and C_{jD} are voltage dependent and consequently enhance nonlinear distortion. The relations for voltage dependent C_{jSB} and C_{jDB} can be found in Table 1-5. All the MOST parasitics scale in direct proportion with the geometric dimensions of the MOST (i.e., W , L_{eff} , L_D , A_S , A_D defined in Chap. 1). Hence, their values are only within the control of the designer insofar as the need to keep the MOSTs as small as a prudent electrical design permits. Recall that the amount of C_{ox} , the gate-to-channel capacitance, in C_{GS} and C_{GD} , varies with the operating region and $C_{\text{ox}T} = C_{\text{ox}} W L_{\text{eff}} \gg C_{GS0}$, C_{GD0} .

Parasitic C_R represents the accumulated capacitance formed by the metal interconnect level, i.e., metal-to-substrate over field oxide. It is determined by $C_{\text{ox}m}$, defined in Table 1-7, and the dimensions of the route $L_R \times W_R$. C_R 's are very much within the control of the designer, and they can be minimized (at least the critical ones) in a well planned layout. Parasitic C_B is formed by the Poly 1 bottom plate associated with C_A , and the field oxide and substrate. C_B scales directly with the dimensions of the poly 1 bottom plate $L_B \times W_B$, that underlies the entire C_A structure (recall Fig. 7-4d). It also depends on $C_{\text{ox}p}$, the capacitance associated with poly 1-to-substrate over field oxide. Hence, the value of C_B is not usually within designer control and will always be a fixed percentage of C_A . The relations for parasitics C_R and C_B are also listed in Table 8-1.

Example 8-1

With $C_{\text{ox}p} = 6.5 \text{ nF/cm}^2$, calculate the bottom-plate parasitic capacitances C_{B1} and C_{B2} for the double-poly capacitors C_1 and C_2 in Fig. 8-5 (see color plate 1).

Solution. From the dimensions, the areas for the bottom plates of C_1 and C_2 are, respectively, $A_1 = 778 \text{ } \mu\text{m}^2 = 778 \times 10^{-8} \text{ cm}^2$ and $A_2 = 7264 \text{ } \mu\text{m}^2 = 7264 \times 10^{-8} \text{ cm}^2$. Thus, $C_{B1} = C_{\text{ox}p} A_1 = 0.05 \text{ pF}$ and $C_{B2} = C_{\text{ox}p} A_2 = 0.47 \text{ pF}$.

TABLE 8-1 PARASITIC CAPACITANCES (WHERE $C_{\text{ox}T} = C_{\text{ox}} W L_{\text{eff}}$ AS PER TABLE 1-5)

		Region	
Cutoff		Triode	Saturation
C_{GS}	$C_{GS0} = C_{\text{ox}} W L_D$	$C_{GS0} + \frac{1}{2} C_{\text{ox}T}$	$C_{\text{ox}} W L_D + \frac{2}{3} C_{\text{ox}T}$
C_{GD}	$C_{GD0} = C_{\text{ox}} W L_D$	$C_{GD0} + \frac{1}{2} C_{\text{ox}T}$	C_{GD0}
C_{jS}	$\approx C_{jSB} A_S$	$\approx C_{jSB} A_S + \frac{1}{2} C_{BC}$	$\approx C_{jSB} A_S + \frac{2}{3} C_{BC}$
C_{jD}	$\approx C_{jDB} A_D$	$\approx C_{jDB} A_D + \frac{1}{2} C_{BC}$	$\approx C_{jDB} A_D$
C_R		$C_{\text{ox}m} W_R L_R$	
C_B		$C_{\text{ox}p} W_B L_B$	