

TP 13.5 A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones

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A high level of integration is critical in lowering the cost of electronics for communication systems such as cellular phones, cordless phones, and wireless LANs. A number of recent papers report increasing levels of transceiver integration. RF, baseband analog, and mixed-signal circuits have been integrated [1]. RF, baseband analog, and voltage-controlled oscillator (VCO) circuits have been realized on a single die [2].

This fully-integrated transceiver incorporates RF circuits, synthesizer, baseband filters, demodulator, and digital signal processing (Figure 13.5.1). The few off-chip components include an ISM band filter, a balun, an RF matching network, an RC loop filter for the PLL, a crystal resonator, and a resistor for biasing. A transmit/receive (T/R) switch is avoided by sharing a single RF port between transmitter and receiver. An offset cancellation method attenuates offsets in the baseband without sacrificing bandwidth in the direct conversion receiver. Careful circuit design, timing, and layout considerations provide isolation between the sensitive RF signals and the digital switching noise. The IC is in 0.6 μ m CMOS and provides a complete interface between antenna and voiceband codec.

Architectural and circuit techniques make this level of integration possible without sacrificing performance. Time-division duplex (TDD) ensures isolation between transmitter and receiver. Direct conversion eliminates expensive, off-chip radio frequency (RF) image-reject filters and diplexer, and replaces off-chip intermediate frequency (IF) channel select filters with on-chip low pass filters. Active on-chip offset reduction by feedback and feedforward loops is combined with digitally-controlled automatic gain control (AGC) that settles within the 160ms preamble of the receive burst. A fully-differential analog signal path minimizes supply and substrate noise coupling. The burst-mode controller (BMC) uses CMOS logic for low power dissipation and high circuit density. To reduce coupling, CMOS logic gate transitions occur in a 5ns period after sampling instants of switched capacitor circuits. The synthesizer dividers use source-coupled logic to reduce coupling. Automatic calibration allows integration of a 1.8GHz LC VCO with a wide tuning range. The receiver has 104dB maximum gain and -104dBm sensitivity.

The low noise amplifier (LNA) and power amplifier (PA) designs make possible sharing a common RF port, eliminating the external TR switch. The LNA input transistors are not stressed by this arrangement because the fabrication technology is 5V-capable, the supply is 3.3V, and the LNA power-down mode allows the source/drain terminals to float to V_{DD} . The LNA, shown in Figure 13.5.2, is implemented as a cascade of two stages. The first stage employs a capacitively cross-coupled input pair, M1 and M2, that provides both gain and impedance matching in parallel with a differential pair, M3 and M4, for additional gain. The second stage of the LNA is also a differential pair. All gain stages are loaded by on-chip spiral inductors. The combined LNA gain can be set to 12dB or 28dB.

The PA is implemented as a three-stage, class AB amplifier. The first stage is a resistively-loaded differential pair, the second stage is a common-source stage loaded with on-chip spiral inductors, and

the output stage consists of large open-drain devices whose drains are connected to the LNA input. The bias currents of the final stage are provided by off-chip RF chokes. The output power, measured at the balun, can be varied from +2dBm to +20dBm.

The mixer uses a double-balanced structure without a tail current source to increase headroom. Biasing for the RF input transistors is by a replica circuit that suppresses transconductance variations with process and temperature. The LO input transistors operate as switches that steer a process and temperature independent current. The output of the mixer is fed to a four-pole Butterworth antialias filter with 2.4MHz cut-off frequency.

Switched-capacitor I and Q baseband filters sample the output of the antialias filter at 24MHz, attenuate adjacent channels, and provide AGC. Each baseband signal path comprises a fourth-order low-pass Chebyshev filter, implemented with two biquad sections, followed by a group-delay equalizer (GDE). The biquads and the GDE have programmable gain of one or four. The filter is followed by a switched-capacitor variable-gain amplifier (VGA) that is programmable with a gain of one, two, or four. This arrangement provides a baseband gain of 0dB to 48dB in 6dB steps.

In a direct conversion receiver, LO leakage can lead to large offsets at the inputs to the baseband filters. Offsets in the switched-capacitor filter sections can accumulate and render the output signal undetectable. To overcome this, feedback integrators cancel offsets in the first biquad and in the GDE (Figure 13.5.1). To prevent baseline wander from causing errors, the integrators are placed in hold mode when data is transferred.

Switched-capacitor peak detectors sample maximum and minimum values of the filtered I and Q signals. The AGC controller uses the peak detector outputs to estimate signal levels and adjusts baseband gain. Offset information, derived from the peak detectors, is filtered and subtracted from the baseband filter output. Offset-cancelled I and Q signals are fed to a BFSK demodulator.

The BFSK demodulator is implemented with switched-capacitor circuits clocked at 6MHz. It generates a digital output based on the direction of rotation of the I/Q constellation. The digital output of the demodulator is processed by an on-chip BMC, comprising over 8000 CMOS standard-cell gates, that performs clock recovery and direct sequence spreading and despreading. The receiver bit error rate (BER), shown in Figure 13.5.3, illustrates receiver sensitivity. Selectivity and blocking are given in Table 13.5.1.

A single frequency synthesizer creates LO and PA input signals for receive and transmit, respectively. The circuit generates channels from 900MHz to 930MHz in 750kHz increments. During receive, a divide-by-two circuit creates I and Q LO signals from the output of a VCO operating at twice the desired frequency in a high-bandwidth PLL. During transmit, the PLL bandwidth is reduced, allowing filtered transmit data to directly modulate the VCO while maintaining a constant center frequency. The transmit spectrum for +20dBm output power is shown in Figure 13.5.4. The VCO, shown in Figure 13.5.5, is a cross-coupled differential pair loaded by spiral inductors and by capacitors. The load capacitors include ac-coupled channel varactors, modulation varactors, and a bank of capacitors for automatic coarse frequency adjustment.

Measured performance is summarized in Table 13.5.1. Figure 13.5.6 is a die photo.

Acknowledgements:

The authors are indebted to P. Gray, P. Heedley, J. Parker, and D. Ray for technical assistance. The authors thank D. Ballinger, J. Orton, and T. Toullelan for work on the BMC and S. Luna for help in IC fabrication.

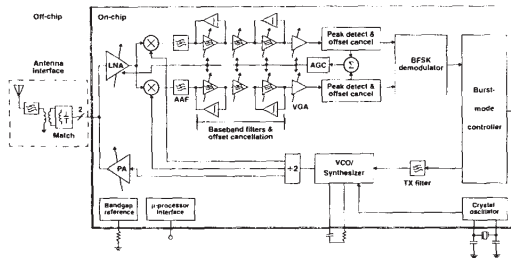


Figure 13.5.1: Transceiver architecture.

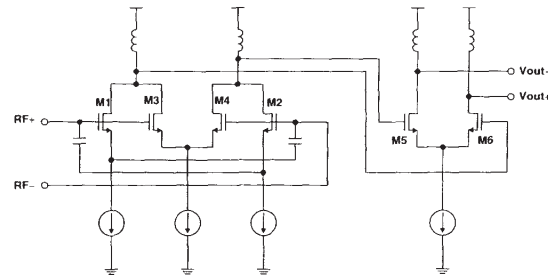


Figure 13.5.2: Low-noise amplifier circuit.

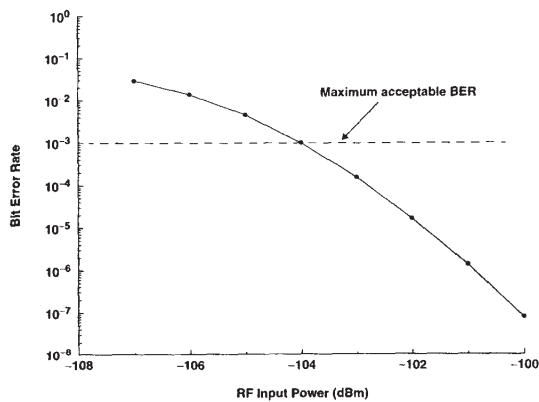


Figure 13.5.3: Measured BER vs. RSL.

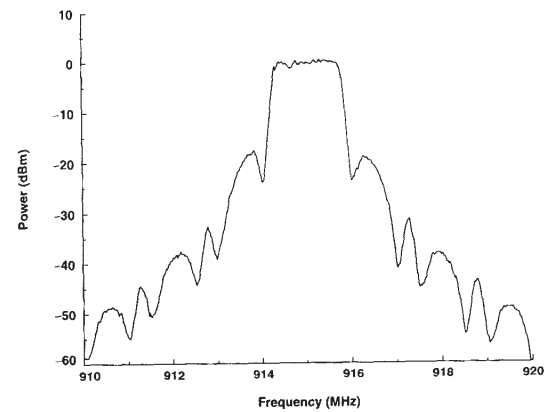


Figure 13.5.4: Measured transmit spectrum.

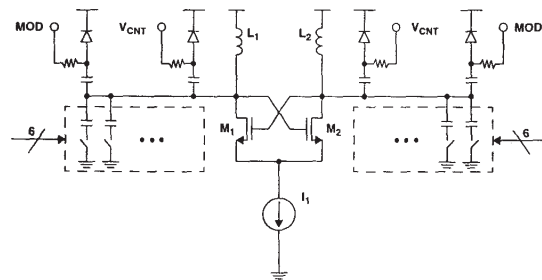


Figure 13.5.5: VCO circuit diagram

Figure 13.5.6: See page 464.

Receiver

Sensitivity	-104dBm
Dynamic range	110dB
Noise figure (DSB)	4.5dB
IIP2 (high gain)	+22dBm
IIP3 (high gain)	-21dBm
Selectivity	3, 23, 57dB

(co-channel 1.5MHz, 3MHz)

Blocking (4.5MHz)	67dB
Dissipation (3.3V)	525mW

Transmitter

Output power (into 50Ω)	2, 8, 14dBm
Bandwidth	1.5MHz
Modulation accuracy	±1%
Dissipation (3.3V, 2dBm)	254mW

General

Technology	0.6μm 2p3m CMOS
Die area	5.4x6.7mm ²

Table 13.5.1: Performance summary.

References:

- [1] A. Rofougaran, et al., "A Single-Chip 900MHz Spread-Spectrum Wireless Transceiver in 1-mm CMOS - Part I: Architecture and Transmitter Design," IEEE J. of Solid-State Circuits, vol. 33, No. 4, pp. 515-534, Apr. 1998.
- [2] M. Steyaert, et al., "A Single-Chip CMOS Transceiver for DCS-1800 Wireless Communications," ISSCC Digest of Technical Papers, pp. 48-49, Feb. 1998.

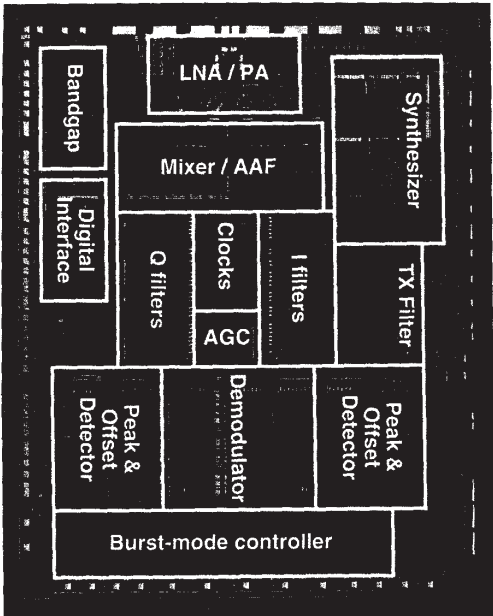


Figure 13.5.6: Die micrograph.

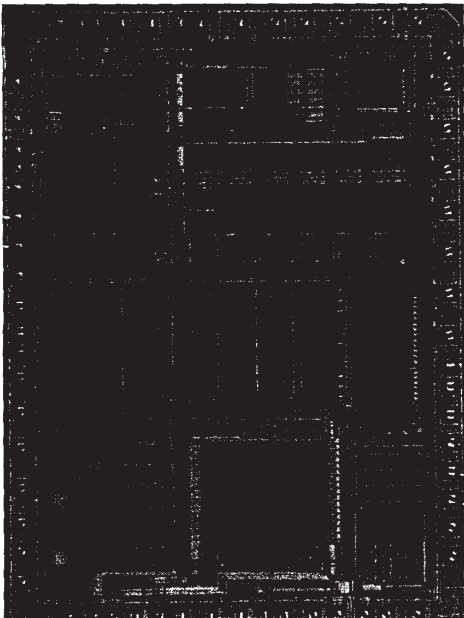


Figure 14.1.7: ADISL die micrograph.

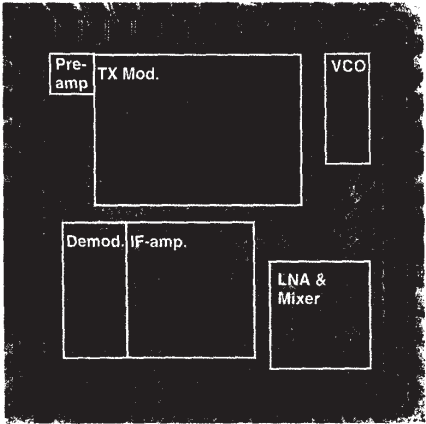


Figure 13.7.7: Die micrograph.

Complete RX (including duplexer and filters)	NF iIP3 iCP Overall gain Blocking	8.1dB(SSB) -4dBm -16dBm +101dB +6dBm at 915MHz (w. c.)
LNA	Gain NF	+15.3dB, -3.7dB 1.9dB
Mixer	Conv. gm NF	8.5mS 15.6dB(SSB)
IF-Amp	Gain NF	-20.9 .. +58dB (2dB steps) 3.8dB
Demodulator	Image suppr. Gain	>43dB($\Delta\phi<1^\circ$) 16dB
Baseband Filters	Type Cut-off freq. Gain	Bessel 4th Ord. active RC 150kHz 15.7dB
Modulator	Output power LO suppr. Image suppr. RMS phase err.	-17dBm >50dB >31dB 1.6°
Pre-amp	Output power Gain oCP	+3dBm 21dB +5.4dBm

Table 13.7.1: Measured transceiver characteristics.

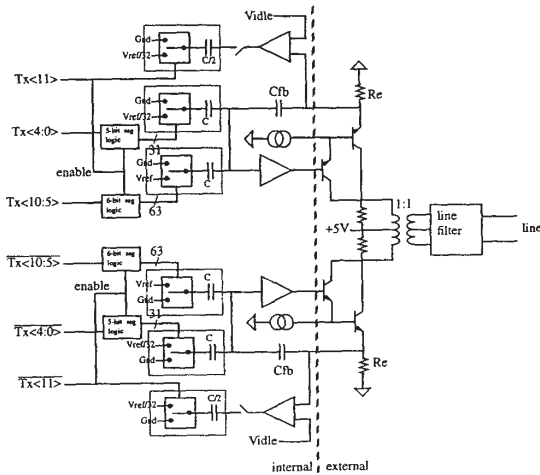


Figure 14.5.2: Transmitter.