DECLARATION OF JUNE ANN MUNFORD

1. My name is June Ann Munford. I am over the age of 18, have personal knowledge of the facts set forth herein, and am competent to testify to the same.

2. I earned a Master of Library and Information Science (MLIS) from the University of Wisconsin-Milwaukee in 2009. I have over ten years of experience in the library/information science field. Beginning in 2004, I have served in various positions in the public library sector including Assistant Librarian, Youth Services Librarian and Library Director. I have attached my Curriculum Vitae as Appendix CV.

3. During my career in the library profession, I have been responsible for materials acquisition for multiple libraries. In that position, I have cataloged, purchased and processed incoming library works. That includes purchasing materials directly from vendors, recording publishing data from the material in question, creating detailed material records for library catalogs and physically preparing that material for circulation. In addition to my experience in acquisitions, I was also responsible for analyzing large collections of library materials, tailoring library records for optimal catalog

search performance and creating lending agreements between libraries during my time as a Library Director.

4. I am fully familiar with the catalog record creation process in the library sector. In preparing a material for public availability, a library catalog record describing that material would be created. These records are typically written in Machine Readable Catalog (herein referred to as “MARC”) code and contain information such as a physical description of the material, metadata from the material’s publisher, and date of library acquisition. In particular, the 008 field of the MARC record is reserved for denoting the date of creation of the library record itself. As this typically occurs during the process of preparing materials for public access, it is my experience that an item’s MARC record indicates the date of an item’s public availability.

5. Typically, in creating a MARC record, a librarian would gather various bits of metadata such as book title, publisher and subject headings among others and assign each value to a relevant numerical field. For example, a book’s physical description is tracked in field 300 while title/attribution is tracked in field 245. The 008 field of the MARC record is reserved for denoting the creation of the library record itself. As this is the only date reflecting the inclusion of said materials within the library’s collection, it is my experience

that an item's 008 field accurately indicates the date of an item's public availability.

6. I am familiar with the Internet Archive, a digital library accessible to the general public. Among other services that the Internet Archive makes available to the general public is the Wayback Machine, an online archive of the web. The Internet Archive's Wayback Machine service archives webpages as of a certain capture date to track changes in the web over time. The Internet Archive has been in operation as a nonprofit library since 1996 and has hosted the Wayback Machine service since its inception in 2001. During my time as a librarian, I frequently used the Internet Archive's Wayback Machine for research and instruction purposes. This includes teaching instructional classes on using the Wayback Machine to library patrons and using the Wayback Machine to research reference inquiries that require hard-to-find online resources. I consider the Internet Archive's recordskeeping to be as rigorous and detailed as other formal library recordskeeping practices such as MARC records, OCLC records and Dublin Core.

7. I have reviewed Exhibit TI-1043, "A 900-MHz CMOS Direct Conversion Receiver" by Behzad Razavi as published in 1997 Symposium on VLSI Circuits.

8. Attached hereto as Appendix RAZAVI01 is a true and correct copy of the MARC record for 1997 Symposium on VLSI Circuits as held by the Penn State University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix RAZAVI01 accurately describes the title, publisher and ISBN number of 1997 Symposium on VLSI Circuits.

9. Attached hereto as Appendix RAZAVI02 is a true and correct copy of "A 900-MHz CMOS Direct Conversion Receiver" as published in 1997 Symposium on VLSI Circuits as held by the Penn State University Library. These scans were secured from the library's collection. In comparing Exhibit TI-1043 to Appendix RAZAVI02, it is my determination that Exhibit TI-1043 is a true and correct copy of "A 900-MHz CMOS Direct Conversion Receiver" by Behzad Razavi as published in 1997 Symposium on VLSI Circuits.

10. The 008 field of the MARC record in Appendix RAZAVI01 indicates the date of record creation. The 008 field of Appendix RAZAVI01 indicates the Penn State University Library first acquired 1997 Symposium on VLSI Circuits as of December 8, 1999. Considering this information, it is my determination that 1997 Symposium on VLSI Circuits and therefore "A 900-MHz CMOS Direct Conversion Receiver" was made available to the public shortly after December 8, 1999.

11. I have reviewed Exhibit TI-1044, a document entitled "Application Note: FETs in Balanced Mixers".

12. Attached hereto as Appendix SILICONIX01 is a screen capture of a webpage entitled Siliconix FET Design Catalog 1979 as hosted on the Internet Archive website. I secured these screen captures myself from https://archive.org/details/siliconix-fet-design-catalog-1979pdf/page/n1/mode/2up.

13. Appendix SILICONIX01 is a PDF copy of the Siliconix FET Design Catalog 1979 containing various documents associated with Siliconix products. Pages 120 - 125 of Appendix SILICONIX01 contain a true and correct copy of "Application Note: FETs in Balanced Mixers", indicating

this document was included within the Siliconix FET Design Catalog 1979 upon publication. In comparing Appendix SILICONIX01 to Exhibit TI-1044, it is my determination that Exhibit TI-1044 is a true and correct copy of "Application Note: FETs in Balanced Mixers".

14. Attached hereto as Appendix SILICONIX02 is a true and correct copy of the MARC record for FET Design Catalog 1979 as held by the Syracuse University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix SILICONIX02 accurately describes the title, author and publisher of FET Design Catalog 1979.

15. The 008 field of the MARC record in Appendix SILICONIX02 indicates the date of record creation. The 008 field of Appendix SILICONIX02 indicates the Syracuse University Library first acquired FET Design Catalog 1979 as of March 3, 1983. Considering this information, it is my determination that FET Design Catalog 1979 and therefore "Application Note: FETs in Balanced Mixers" was made available to the public shortly after its initial acquisition as of March 3, 1983.

16. I have reviewed Exhibit TI-1045, "The MICROMIXER: a Highly Linear Variant of the Gilbert Mixer Using a Bisymmetric Class-AB Input Stage" by B. Gilbert, et al as published in IEEE Journal of Solid-State Circuits September 1997.

17. Attached hereto as Appendix GILBERT01 is a true and correct copy of the MARC record for IEEE Journal of Solid-State Circuits as held by the Penn State University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix GILBERT01 accurately describes the title, publisher and ISSN number of IEEE Journal of Solid-State Circuits. The Availability field present on page 4 of this record indicates the library's collection includes the September 1997 issue of IEEE Journal of Solid-State Circuits containing "The MICROMIXER: a Highly Linear Variant of the Gilbert Mixer Using a Bisymmetric Class-AB Input Stage".

18. Attached hereto as Appendix GILBERT02 is a true and correct copy of "The MICROMIXER: a Highly Linear Variant of the Gilbert Mixer Using a Bisymmetric Class-AB Input Stage" as published in IEEE Journal of Solid-State Circuits as held by the Penn State University Library. These scans were secured from the library's collection. In comparing Exhibit TI-1045 to

Appendix GILBERT02, it is my determination that Exhibit TI-1045 is a true and correct copy of "The MICROMIXER: a Highly Linear Variant of the Gilbert Mixer Using a Bisymmetric Class-AB Input Stage" by B. Gilbert, et al as published in IEEE Journal of Solid-State Circuits.

19. The 008 field of the MARC record in Appendix GILBERT01 indicates the date of record creation. The 008 field of Appendix GILBERT01 indicates the Penn State University Library first acquired IEEE Journal of Solid-State Circuits as of May 14, 1982 and held the journal in perpetuity until the publication of "The MICROMIXER: a Highly Linear Variant of the Gilbert Mixer Using a Bisymmetric Class-AB Input Stage". Considering this information, it is my determination that IEEE Journal of Solid-State Circuits September 1997 and therefore "The MICROMIXER: a Highly Linear Variant of the Gilbert Mixer Using a Bisymmetric Class-AB Input Stage" was made available to the public shortly after its initial publication in September 1997.

20. I have reviewed Exhibit TI-1047, Basic Electric Circuit Analysis by David E. Johnson.

21. Attached hereto as Appendix JOHNSON01 is a true and correct copy of the MARC record for Basic Electric Circuit Analysis as held by the Penn State University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix JOHNSON01 accurately describes the title, author, publisher, and ISBN number of Basic Electric Circuit Analysis.

22. Attached hereto as Appendix JOHNSON02 is a true and correct copy of Basic Electric Circuit Analysis as held by the Penn State University Library. These scans were secured from the library's collection. In comparing Exhibit TI-1047 to Appendix JOHNSON02, it is my determination that Exhibit TI-1047 is a true and correct copy of Basic Electric Circuit Analysis by David E. Johnson.

23. The 008 field of the MARC record in Appendix JOHNSON01 indicates the date of record creation. The 008 field of Appendix JOHNSON01 indicates the Penn State University Library first acquired Basic Electric Circuit Analysis as of July 7, 1982. Considering this information, it is my determination that Basic Electric Circuit Analysis was made available to the public shortly after its initial acquisition as of July 7, 1982.

24. I have reviewed Exhibit TI-1048, Microelectronic Circuits by Adel S. Sedra.

25. Attached hereto as Appendix SEDRA01 is a true and correct copy of the MARC record for Microelectronic Circuits as held by the Penn State University Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix SEDRA01 accurately describes the title, author, publisher, and ISBN number of Microelectronic Circuits.

26. Attached hereto as Appendix SEDRA02 is a true and correct copy of Microelectronic Circuits as held by the Penn State University Library. These scans were secured from the library's collection. In comparing Exhibit TI-1048 to Appendix SEDRA02, it is my determination that Exhibit TI-1048 is a true and correct copy of Microelectronic Circuits by Adel S. Sedra.

27. The 008 field of the MARC record in Appendix SEDRA01 indicates the date of record creation. The 008 field of Appendix SEDRA01 indicates the Penn State University Library first acquired Microelectronic Circuits as of August 19, 1997. Considering this information, it is my determination that Microelectronic Circuits was made available to the public shortly after its initial acquisition as of August 19, 1997.

28. I have reviewed Exhibit TI-1049, Design of Analog Integrated Circuits and Systems by Kenneth R. Laker.

29. Attached hereto as Appendix LAKER01 is a true and correct copy of the MARC record for Design of Analog Integrated Circuits and Systems as held by the Linda Hall Library. I secured this record myself from the library's public catalog. The MARC record contained within Appendix LAKER01 accurately describes the title, author, publisher, and ISBN number of Design of Analog Integrated Circuits and Systems.

30. Attached hereto as Appendix LAKER02 is a true and correct copy of Design of Analog Integrated Circuits and Systems as held by the Linda Hall Library. These scans were secured from the library's collection. In comparing Exhibit TI-1049 to Appendix LAKER02, it is my determination that Exhibit TI-1049 is a true and correct copy of Design of Analog Integrated Circuits and Systems by Kenneth R. Laker.

31. The 008 field of the MARC record in Appendix LAKER01 indicates the date of record creation. The 008 field of Appendix LAKER01 indicates the Linda Hall Library first acquired Design of Analog Integrated Circuits and Systems as of December 15, 1993. Considering this information, it is my

determination that Design of Analog Integrated Circuits and Systems was made available to the public shortly after its initial acquisition as of December 15, 1993.

32. I have reviewed Exhibit TI-1050, “A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones” by R. Cho, et al as published in Proceedings of the 1999 IEEE International Solid-State Circuits Conference.

33. Attached hereto as Appendix CHO01 is a true and correct copy of the MARC record for Proceedings of the 1999 IEEE International Solid-State Circuits Conference as held by the Penn State University Library. I secured this record myself from the library’s public catalog. The MARC record contained within Appendix CHO01 accurately describes the title, publisher and ISBN number of Proceedings of the 1999 IEEE International Solid-State Circuits Conference.

34. Attached hereto as Appendix CHO02 is a true and correct copy of “A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones” as published in Proceedings of the 1999 IEEE International Solid-State Circuits Conference as held by the Penn State

University Library. These scans were secured from the library's collection. In comparing Exhibit TI-1050 to Appendix CHO02, it is my determination that Exhibit TI-1050 is a true and correct copy of "A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones" by R. Cho, et al as published in Proceedings of the 1999 IEEE International Solid-State Circuits Conference.

35. The 008 field of the MARC record in Appendix CHO01 indicates the date of record creation. The 008 field of Appendix CHO01 indicates the Penn State University Library first acquired Proceedings of the 1999 IEEE International Solid-State Circuits Conference as of September 11, 1998. Considering this information, it is my determination that Proceedings of the 1999 IEEE International Solid-State Circuits Conference and therefore "A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones" was made available to the public shortly after September 11, 1998.

36. I have been retained on behalf of the Petitioner to provide assistance in the above-illustrated matter in establishing the authenticity and public availability of the documents discussed in this declaration. I am being compensated for my services in this matter at the rate of $200.00 per hour

plus reasonable expenses. My statements are objective, and my compensation does not depend on the outcome of this matter.

37. I declare under penalty of perjury that the foregoing is true and correct. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: 6/27/2025

June Ann Munford

APPENDIX CV

June A. Munford
Curriculum Vitae

Education

University of Wisconsin-Milwaukee - MS, Library & Information Science, 2009
Milwaukee, WI

- Coursework included cataloging, metadata, data analysis, library systems, management strategies and collection development.
- Specialized in library advocacy, cataloging and public administration.

Grand Valley State University - BA, English Language & Literature, 2008
Allendale, MI

- Coursework included linguistics, documentation and literary analysis.
- Minor in political science with a focus in local-level economics and government.

Professional Experience

Researcher / Expert Witness, October 2017 – present
Freelance ● Pittsburgh, Pennsylvania & Grand Rapids, Michigan

- Material authentication and public accessibility determination. Declarations of authenticity and/or public accessibility provided upon research completion. Experienced with appeals and deposition process.

- Research provided on topics of public library operations, material publication history, digital database services and legacy web resources.

- Past clients include Alston & Bird, Arnold & Porter, Baker Botts, Fish & Richardson, Erise IP, Irell & Manella, O'Melveny & Myers, Perkins-Coie, Pillsbury Winthrop Shaw Pittman and Slayden Grubert Beard.

Library Director, February 2013 - March 2015
Dowagiac District Library ● Dowagiac, Michigan

- Executive administrator of the Dowagiac District Library. Located in Southwest Michigan, this library has a service area of 13,000, an annual operating budget of over $400,000 and total assets of approximately $1,300,000.

● Developed careful budgeting guidelines to produce a 15% surplus during the 2013-2014 & 2014-2015 fiscal years while being audited.

● Using this budget surplus, oversaw significant library investments including the purchase of property for a future building site, demolition of existing buildings and building renovation projects on the current facility.

● Led the organization and digitization of the library's archival records.

● Served as the public representative for the library, developing business relationships with local school, museum and tribal government entities.

● Developed an objective-based analysis system for measuring library services - including a full collection analysis of the library's 50,000+ circulating items and their records.

November 2010 - January 2013
Librarian & Branch Manager, Anchorage Public Library ● Anchorage, Alaska

● Headed the 2013 Anchorage Reads community reading campaign including event planning, staging public performances and creating marketing materials for mass distribution.

● Co-led the social media department of the library's marketing team, drafting social media guidelines, creating original content and instituting long-term planning via content calendars.

● Developed business relationships with The Boys & Girls Club, Anchorage School District and the US Army to establish summer reading programs for children.

June 2004 - September 2005, September 2006 - October 2013
Library Assistant, Hart Area Public Library
Hart, MI

● Responsible for verifying imported MARC records and original MARC cataloging for the local-level collection as well as the Michigan Electronic Library.

● Handled OCLC Worldcat interlibrary loan requests & fulfillment via ongoing communication with lending libraries.

Professional Involvement

Alaska Library Association - Anchorage Chapter

● Treasurer, 2012

Library Of Michigan
- ● Level VII Certification, 2008
- ● Level II Certification, 2013

Michigan Library Association Annual Conference 2014
- ● New Directors Conference Panel Member

Southwest Michigan Library Cooperative
- ● Represented the Dowagiac District Library, 2013-2015

Professional Development

Library Of Michigan Beginning Workshop, May 2008
Petoskey, MI
- ● Received training in cataloging, local history, collection management, children's literacy and reference service.

Public Library Association Intensive Library Management Training, October 2011
Nashville, TN
- ● Attended a five-day workshop focused on strategic planning, staff management, statistical analysis, collections and cataloging theory.

Alaska Library Association Annual Conference 2012 - Fairbanks, February 2012
Fairbanks, AK
- ● Attended seminars on EBSCO advanced search methods, budgeting, cataloging, database usage and marketing.

Depositions

2019 ● Fish & Richardson

Apple v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282 and 39521-00421IP2)

2019 ● Erise IP

Implicit, LLC v. Netscout Systems, Inc (Case No. 2:18-cv-53-JRG)

2019 ● Perkins-Coie

Adobe Inc. v. RAH Color Technologies LLC (Case No. IPR2019-00627, IPR2019-00628, IPR2019-00629 and IPR2019-00646)

2020 ● O'Melveny & Myers

Maxell, Ltd. v. Apple Inc. (Case No. 5:19-cv-00036-RWS)

2021 ● Pillsbury Winthrop Shaw Pittman LLP

Intel v. SRC (Case No. IPR2020-1449)

2022 ● Perkins-Coie

Realtek v. Future Link (Case No. IPR2021-01182)

2023 ● Fish & Richardson

Neuroderm Ltd. v. Abbvie, Inc (Case No. PGR2022-00040)

2023 ● Fish & Richardson

Nearmap US Inc. v. Pictometry International Corp. (Case No. IPR2022-00735)

2023 ● Fish & Richardson

Samsung Electronics v. MemoryWeb LLC (Case No. 39843-0136PS1)

2023 ● Pillsbury Winthrop Shaw Whitman LLP

Gravel Rating Systems v. Costco Wholesale Corp. (Case No. 4:21-cv-149-ALM)

2024 ● Willkie-Farr

Netflix, Inc. v. VideoLabs. Inc. (Case No. IPR2023-00628)

2024 ● Quinn Emanuel Urquhart & Sullivan

Purdue University v. Wolfspeed (Case No. 1:21-CV-840)

2024 ● Fish & Richardson

Dish Network v. Entropic Communications (Case No. IPR2024-00393)

2025 ● Perkins Coie

Amazon.com, Inc. v. Nokia Technologies Oy (Case No. IPR2024-00572)

2025 ● Fish & Richardson

Dish Network v. Entropic Communications (Case No. IPR2024-00373)

Limited Case and Clientele History

Alston & Bird

- Ericsson

  v. Collision Communications (Case No. IPR2022-01233)

- Nokia

  v. Neptune Subsea, Xtera (Case No. 1:17-cv-01876)

- Universal Electronics Inc

  v. Roku Inc (Case No. IPR2022-00818)

Alavi & Anaipakos PLLC

- Stingray Group Inc. and Stingray Music USA, Inc.

  v. Edwin A. Hernandez-Mondragon and Egla Corp. (Case No. 1:24-cv-21226-RAR)

Arnold & Porter

- Ivantis

  v. Glaukos (Case No. 8:18-cv-00620)

- Samsung

  v. Jawbone (Case No. 2:21-cv-00186)

Benesch Friedlander Coplan & Aronoff

- Voyis

  v. Cathx (Case No. 5:21-cv-00077-RWS)

Buchanan, Ingersoll & Rooney PC

- Google LLC, AT&T Service Inc., T Mobile USA Inc., Cellco Partnership, Ericsson Inc. & Nokia of America Corp.

  v. KT Corp & Pegasus Wireless Innovation LLC (Case No. IPR2025-00293)

Deschert LLP

- Smaxtec Animal Care

  v. ST Reproductive Technologies, LLC (Case No. IPR2024-00885)

Duane Morris

- Kangxi Communication Technologies

  v. Skyworks Solutions Inc. (Case No. IPR2025-00373)

- Microsoft

  v. Edge Networking Systems LLC (Case No. 1:24-cv-00215)

Erise I.P.

- Apple

  v. Ericsson Inc. (Case No. IPR2022-00715)

  v. Future Link Systems (Case No. IPRs 6317804, 6622108, 6807505, and 7917680)

  v. INVT (Case No. 20-1881)

  v. Navblazer LLC (Case No. IPR2020-01253)

  v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

v. Quest Nettech Corp (Case No. 2:19-cv-00118-JRG)

v. Telefonaktiebolaget LM Ericsson (Case No. IPR2022-00275)

v. Theta IP, LLC (Case No. IPR2024-00818)

v. THL Holding Company LLC (Case No. 1:23-cv-00548)

- Fanduel

  v. CGT (Case No. 19-1393)

- Garmin

  v. Phillips North America LLC (Case No. 2:19-cv-6301-AB-KS)

- Netscout

  v. Longhorn HD LLC (Case No. 2:20-cv-00349)

  v. Implicit, LLC (Case No. 2:18-cv-53-JRG)

- Sony Interactive Entertainment LLC

  v. Bot M8 LLC (Case No. IPR2020-01288)

  v. Infernal Technology LLC (Case No. 2:19-CV-00248-JRG)

- Tesla

  v. Charge Fusion Technologies LLC (Case No. IPR2025-00032)

- Unified Patents

  v. GE Video Compression (Case No. 2:19-cv-248)

Fish & Richardson

- Apple

  v. AliveCor (Case No. 3:21-cv-03958)

  v. LBS Innovations (Case No. 2:19-cv-00119-JRG-RSP)

  v. Koss Corporation (Case No. IPR2021-00305)

v. Masimo (Case No. IPR 50095-0012IP1, 50095-0012IP2, 50095-0013IP1, 50095-0013IP2, 50095-0006IP1, 50095-0135IP1)

v. Neonode (Case No. 21-cv-08872-EMC)

v. Qualcomm (Case No. IPR2018-001281, 39521-00421IP, IPR2018-01282, 39521-00421IP2)

v. Resonant Sys. (Case No. 7:23-cv-00077-ADA)

- AsusTek Computer Inc.
  v. Videolabs, Inc. (Case No. 22-CV-00720-ADA)

- Dell
  v. Neo Wireless (Case No. IPR2022-00616)

- Dish Network

  v. Entropic Communications, LLC (Case No. 2:2023-CV-01043)

  v. Entropic Communications LLC (Case No. IPR2024-00393)

  v. Realtime Adaptive Streaming (Case No. 1:17-CV-02097-RBJ)

  v. TQ Delta LLC (Case No. 18-1798)

- Evapco Dry Cooling

  v. SPG Dry Cooling (Case No. IPR2021-00688)

- Genetec

  v. Sensormatic Electronics (Case No. 1:20-CV-00760)

- Huawei

  v. Bell Northern Research LLC (Case No. IPR2019-01174)

- Kianxis

  v. Blue Yonder (Case No. 3:20-cv-03636)

- LG Electronics

  v. Bell Northern Research LLC (Case No. 3:18-cv-2864-CAB-BLM)

- MediaTek

  v. MOSAID (Case No. IPR2024-00718)

- Metaswitch

  v. Sonus Networks (Case No. IPR2018-01719)

- Microsoft

  v. Throughputer Inc (Case No. IPR2022-00757)

- Mom Enterprises

  v. Ddrops Company (Case No. 1:22-cv-00332)

- MLC Intellectual Property

  v. MicronTech (Case No. 3:14-cv-03657-SI)

- Nearmap Inc

  v. EagleView Technologies (Case No. IPR2022-01009)

- Neuroderm Ltd.

  v. Abbvie, Inc (Case No. PGR2022-00040)

- Posco Co Ltd.

  v. Pascal Drillet et al. (Case No. IPR2025-00370)

- Realtek Semiconductor

  v. Future Link (Case No. IPR2021-01182)

- Quectel
  - v. Koninklijke Philips (Case No. 1:20-cv-01710)

- Samsung
  - v. Aire Technology (Case No. IPR2022-00877)
  - v. Bell Northern Research (Case No. 2:19-cv-00286-JRG)
  - v. Communication Technologies Inc (Case No. IPR2022-01221)
  - v. Jawbone Innovations (Case No. IPR2022-00865)
  - v. MemoryWeb LLC (Case No. IPR2022-00885)
  - v. Dodots Licensing Solutions (Case No. IPR2023-00701)
  - v. Telefonaktiebolaget LM Ericsson (Case No. IPR2021-00615)

- Texas Instruments
  - v. Vantage Micro LLC (Case No. IPR2020-01261)

- Xilinx
  - v. Sentient Sensors LCC (Case No. 1:22-cv-00173)

Goodwin Proctor

- Intel
  - v. Proxense, LLC (Case No. 6:24-cv-00283)

- Samsung Electronics
  - v. Mobile Data Technologies (Case No. 2:24-cv-00435)

- Taiwan Semiconductor Manufacturing Company Ltd.
  - v. Advanced Integrated Circuit Process LLC (Case No. 2:24-cv-00623)

Groombridge Wu

- Nearmap

  v. Eagle View Technologies Inc. and Pictometry International Corp. (Case No. 2:21-cv-00283-TS-DAO)

Irell & Manella

- Curium

Latham & Watkins LLP

- Apple

  v. Advanced Coding Research LLC

Leydig, Voit & Mayer, Ltd.

- Public Availability Consultancy

O'Melveny & Myers

- Apple

  v. Maxell (Case No. 5:19-cv-00036-RWS)

- Disney Media & Entertainment Distribution LLC

  v. Digital Media Technology Holdings, LLC (Case No. 2:22-cv-01642)

- Micron Technology Inc.

  v. Besang Inc (Case No. IPR2023-00900)

- Samsung

  v. Daedalus Prime LLC (1335 Investigation)

Perkins-Coie

- Amazon
  - v. Nokia (Case No. IPR2024-00847 and IPR2024-00848)
  - v. Nokia Technologies Oy (Case No. IPR2024-00572)
- Heru Industries
  - v. The UAB Research Foundation (Case No. IPR2022-01148)
- Intel Corporation
  - v. BeSang Inc. (Case No. IPR2023-00991)
  - v. BitMICRO (Case No. 5:23-cv-00625)
  - v. Telefonaktiebolaget L M Ericsson (Case No. IPR2024-00610)
- Realtek Semiconductor
  - v. Future Link (Case No. IPR2021-01182)
- r-pac
  - v. Adasa, Inc. (Case No. 1:2024cv06102)
- Twitter Inc
  - v. VOIP-Pal.com (Case No. 3:20-cv-02397-JD)
- TCL Industries
  - v. Koninklijke Philips NV (Case No. IPR2021-00495, IPR2021-00496 and IPR2021-00497)
- VusionGroup
  - v. Hanshow (Case No. IPR2024-00857)

Pillsbury Winthrop Shaw Pittman

- Intel

  v. FG SRC LLC (Case No. 6:20-cv-00315)

- Gravel Rating Systems

  v. Costco (Case No. 4:21-cv-149)
  v. Lowe's Home Centers (Case No. 4:21-cv-150)
  v. T-Mobile USA (Case No. 4:21-cv-152)
  v. Kohl's Inc. (Case No. 4:21-cv-258)
  v. Under Armor (Case No. 4:21-cv-356)

Quinn Emanuel

- Exact Sciences Corporation

  v. Geneoscopy, Inc. (Case No. IPR2024-00459 and IPR2024-1330)

- ServiceNow, Inc.

  v. InQuisient, Inc. (Case No. 22-900-CJB)

- Wolfspeed

  v. The Trustees of Purdue University (Case No. 1:2021-cv-00840)

Sheppard, Mullin, Richter & Hampton LLP

- Advanced Micro Devices, Inc and Pensando Systems, Inc.

  v. Concurrent Ventures LLC and Xtreamedge, Inc. (Case No. IPR2025-00478)

- Cadence Design Systems Inc.

  v. Semiconductor Design Technologies (Case No. 3:23-cv-01001)

Shook, Hardy & Bacon LLP

- HP Inc.

  v. Universal Connectivity Technologies (Case No. 1:23-cv-01177)

Stern, Kessler, Goldstein & Fox

- Preliminary Research

Wilmer, Cutler, Pickering, Hale and Dorr

- Apple

  v. Shunock (Case No. 1:23-cv-08598)

- Quest Diagnostics Inc., Haystack Oncology Inc. and Haystack Oncology GmbH

  v. Natera, Inc. (Case No. 1:23-cv-08598)

- Roche Diabetes, Inc.

  v. Trividia Health, Inc. (Case No. 1:24-cv-00668)

Willkie, Farr & Gallagher LLP

- Lenovo, Dell, HP

  v. Universal Connectivity Technologies Inc. (Case No. 2:2023cv00449)

- Neurent

  v. The Foundry, LLC (Case No. IPR2024-00669)

- Netflix, Inc.

  v. VideoLabs, Inc. (Case No. IPR2023-00628)

APPENDIX RAZAVI01

MARC View

LEADER 01387nam a22003492 4500				
001 22612503				
003 SIRSI				
005 20180314130447.0				
006 m d				
007 cr n				
008 991208nuuuuuuuuunjua s||||||| 2|eng|d				
010			a| 98143583	
020			a| 9784930813763	
020			a| 493081376X (Trade Cloth) 9| Active Record	
024	3		a| 9784930813763	
037			b| 00402864	
040			a| BIP US d| WaSeSS	
050		0	a| TK7874.75.S98 1997	
082	0	0	a| 621.39/5 2| 21	
110	2		a| Symposium on VLSI Circuits e| Contribution by 4| oth	
245	1	0	a| 1997 Symposium on VLSI Circuits h| [electronic resource]: b| Digest of Technical Papers, June 12-14, 1997, Kyoto	
260			a| New Providence : b| BPR Publishers	
300			b| ill	
506			a| License restrictions may limit access.	
655		0	a| Electronic books.	
710	1		a| Kyoto, Japan.	
710	1		a| Oyo Butsuri Gakkai.	
710	1		a| IEEE, Solid-State Circuits Council Staff.	
710	1		a| Denshi Jeoheo Tseushin Gakkai Staff.	
856	4	0	u| http://SK8ES4MC2L.search.serialssolutions.com/?sid=sersol&SS_jc=TC0000455163&title=1997%20Symposium%20on%20VLSI%20Circuits%3A%20Digest%20of%20Technical%20Papers%2C%20June%2012-14%2C%201997%2C%20Kyoto	
955			a| Books In Print, (c) 2011 R.R. Bowker LLC	
949			a| Electronic resource w| ASIS c| 1 i| 22612503-1001 l| ONLINE m| ONLINE r| Y s| Y t| ONLINE u| 3/20/2018 o| .STAFF. 360 MARC	

ASK A LIBRARIAN

PennState

Copyright @2019 The Pennsylvania State University. All rights reserved. Except where otherwise noted, this work is subject to a Creative Commons Attribution 4.0 license. Details and exceptions.

Legal Statements | PSU Hotlines

PENN STATE UNIVERSITY LIBRARIES

Libraries Home (814) 865-6368
Libraries Intranet (Staff Only)
Accessibility Help
Website Feedback
Policies and Guidelines
Staff Directory

CONNECT WITH PENN STATE UNIVERSITY LIBRARIES

Facebook
Twitter
Instagram

1997 Symposium on VLSI Circuits [electronic resource]: Digest of Technical Papers, June 12-14, 1997, Kyoto

Corporate Author	Symposium on VLSI Circuits
Published	New Providence : BPR Publishers
Physical Description	ill
Additional Creators	Kyoto, Japan, Oyo Butsuri Gakkai, IEEE, Solid-State Circuits Council Staff, and Denshi Jouhou Tseushin Gakkai Staff

ASK A LIBRARIAN

Access Online

serialssolutions.com

Restrictions on Access

License restrictions may limit access.

Genre(s)

Electronic books

ISBN

9784930813763

493081376X (Trade Cloth)

View MARC record | catkey: 22612503

PennState

Copyright @2019 The Pennsylvania State University. All rights reserved. Except where otherwise noted, this work is subject to a Creative Commons Attribution 4.0 license. Details and exceptions.

Legal Statements | PSU Hotlines

PENN STATE UNIVERSITY LIBRARIES

Libraries Home (814) 865-6368

Libraries Intranet (Staff Only)

Accessibility Help

Website Feedback

Policies and Guidelines

Staff Directory

CONNECT WITH PENN STATE UNIVERSITY LIBRARIES

Facebook

Twitter

Instagram

APPENDIX RAZAVI02

15–2

A 900-MHz CMOS Direct Conversion Receiver

Behzad Razavi
Formerly with: Hewlett-Packard Laboratories, Palo Alto, CA
Presently with: University of California, Los Angeles

This paper describes the design of a single-chip 900-MHz CMOS direct conversion receiver (DCR) fabricated in a digital 0.6-μm technology and operating from a 3-V supply.

Shown in Fig. 1 is the DCR architecture, consisting of a low-noise amplifier (LNA), quadrature mixers, simple low-pass filters (LPFs), a local oscillator (LO), a divide-by-two circuit, and baseband amplifiers, A_1. An important goal in the design has been to achieve a relatively high gain (approximately 35 dB) in the RF section so as to minimize the effect of the $1/f$ noise contributed by the baseband amplifiers. For this reason, passive mixers have been avoided even though they provide potentially higher linearity than do their active counterparts. Another goal has been to include the LO on the chip so as to obtain a realistic estimate of the leakage to the front end. The design incorporates on-chip inductors extensively to improve the performance.

Fig. 2 shows the implementation of the LNA and the quadrature mixers. The LNA is configured as a cascode stage, M_1 and M_2, with a 10-nH inductive load [1]. Providing high isolation between the output and the input, the cascode transistor not only improves the stability of the circuit but suppresses the LO leakage to the antenna as well. Utilizing large devices [$(W/L)_1 = 2000\ \mu$m$/0.6\ \mu$m)] and a relatively high bias current (≈ 5 mA), the LNA achieves a noise figure of less than 2 dB and a voltage gain of approximately 20 dB. The inductive load provides a high gain while consuming negligible voltage headroom.

The use of an inductive load in the LNA prohibits the use of feedback to define the bias current and the output dc voltage of the circuit. While M_3 and I_b determine the bias current, the output voltage remains close to V_{DD}, a serious problem with respect to the bias point of the *following* stage—the mixer. This issue is resolved as explained below.

The mixer employs a single-balanced topology consisting of an input transistor M_4 and a switching pair M_5-M_6. In order to improve the linearity of the voltage-to-current conversion performed by the input stage, capacitor C_1 degenerates transistor M_4 at 900 MHz [2]. The current source defines the bias condition of M_4 with little dependence on its gate voltage. The problem of noise differentiation [2] is overcome by allowing L_2 and the bottom-plate parasitic capacitance of C_2 (C_p) to resonate in the vicinity of 900 MHz and shunt the noise current at higher harmonics of this frequency. Capacitor C_2 provides ac coupling, relaxing the limited voltage headrooom issues in the switching stage and also suppressing low-frequency beat signals that are generated if two input interferers experience *even-order* distortion in M_1, M_2, and M_4.

Even without the voltage headroom loss that would otherwise accompany M_4 in a simple mixer, the switching stage in Fig. 2 entails a number of trade-offs. To achieve a high conversion gain, M_5 and M_6 must remain in saturation and, more importantly, the voltage drop across R_1 and R_2 must be maximized. On the other hand, to minimize the noise current of M_7, the allowable drain-source voltage of this device must be as large as possible. In this design, the noise current of M_7 is suppressed in the band of interest (and higher harmonics thereof) through the use of the degenerating inductor L_3. This technique makes it possible to choose $V_{DS7} \approx 0.5$ V with negligible noise penalty, thereby allowing a large voltage drop across R_1 and R_2.

The output nodes of the mixer are loaded with on-chip capacitors to suppress high-frequency components, but channel-selection filtering is not included here.

Fig. 3 illustrates the LO and the divide-by-two circuit. Using a cross-coupled pair M_1-M_2 and 10-nH inductors L_1 and L_2, the oscillator operates at 1.8 GHz while directly driving the divider. The latter is configured as a master-slave flipflop driven differentially through M_3-M_4 and M_5-M_6. Proper sizing of the devices in each latch provides division speeds in excess of 2 GHz even with the relatively heavy capacitive loading imposed by the switching pairs in the quadrature mixers. Resistors R_5 and R_6 shift the high level of I_{LO} and Q_{LO} down to avoid driving the mixer switching pairs into the triode region.

The downconverted signal can be further processed by one of the three permutations depicted in Fig. 4 [3]. In Fig. 4(a), a low-pass filter suppresses out-of-channel interferers, allowing A_1 to be a nonlinear, high-gain amplifier and the analog-to-digital converter (ADC) to have a moderate dynamic range. (roughly 4 to 8 bits depending on the gain control in the RF domain and the type of modulation). However, the low-pass filter design entails severe noise-linearity-power tradeoffs. The second permutation, shown in Figure 4(b), relaxes the LPF noise requirements while demanding a higher performance in the amplifier. The difficulty here is that the signals are still quite small and the interferers quite large. Thus, A_1 must exhibit both low noise and high linearity. The present design is intended for permutations in Figs. 4(b) and (c).

Shown in Fig. 5 is the implementation of the baseband amplifier, consisting of a degenerated differential pair M_1-M_2 and load devices R_1-R_2 and M_3-M_4. Since high linearity requires a large $I_S R_S$, the maximum voltage gain with a 3-V supply is quite limited. To resolve this issue, the PMOS current sources have been added so as to provide about 75% of the drain current of M_1 and M_2, thereby allowing a large value for R_1 and R_2 and hence a high gain in the stage.

The linearity of the baseband amplifier is limited by both the nonlinear characteristics of M_1-M_2 and the nonlinear *output impedance* of M_3-M_4, even though all the transistors are in saturation. For this reason, the length of M_3-M_4 has been increased to 4 μm. To reduce the $1/f$ noise, wide transistors have been used: $W_{1,2} = 2000\ \mu$m, $W_{3,4} = 1600\ \mu$m.

The complete receiver has been fabricated in a 0.6-μm digital CMOS technology. The inductors are implemented as a stack of two spiral structures made of the second and third metal layers

Authorized licensed use limited to: Penn State University. Downloaded on June 25,2025 at 18:37:35 UTC from IEEE Xplore. Restrictions apply.

with no additional wafer processing steps. Table 1 summarizes the preliminary measured performance of the overall receiver and Fig. 6 shows the LO divided output spectrum.

REFERENCES

[1] D. K. Shaeffer and T. H. Lee, "A 1.5 V 1.5 GHz CMOS Low Noise Amplifier," *VLSI Symp. Dig. Tech. Papers*, pp. 32-33, June 1996.

[2] B. Razavi, "A 1.5-V 900-MHz Downconversion Mixer," *ISSCC Dig. Tech. Papers*, pp. 48-49 , Feb. 1996.

[3] B. Razavi, "Design Considerations for Direct-Conversion Receivers," to be published in *IEEE Trans. Circuits and Systems II*, May 1997.

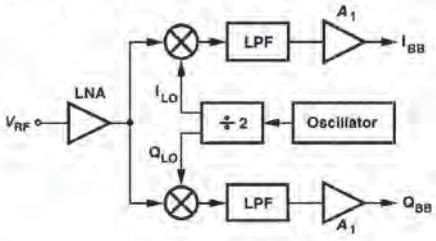


Fig. 1. Receiver architecture.

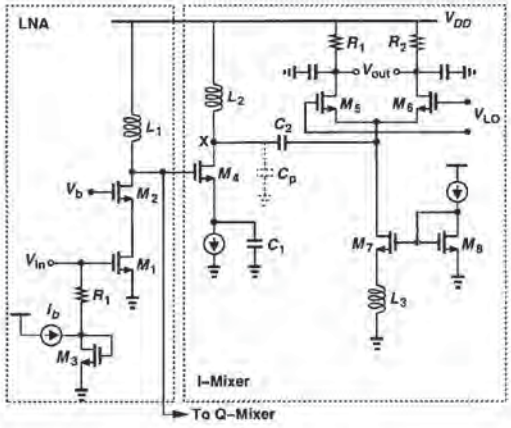


Fig. 2. LNA/mixer implementation.

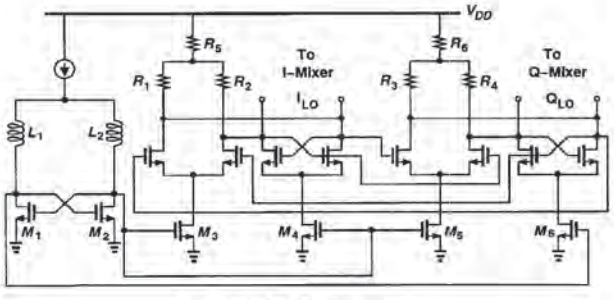


Fig. 3. LO/divider circuit.

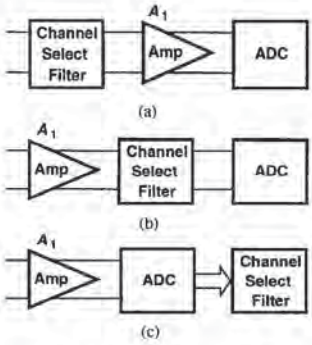


Fig. 4. Baseband processing.

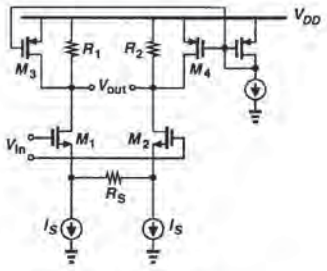


Fig. 5. Baseband amplifier.

Noise Figure	4 dB
IIP_3	−20 dBm
IIP_2	+10 dBm
LO Leakage	−65 dBm
LO Phase Noise	−90 dBc/Hz @100 kHz offset
Voltage Gain	55 dB
Power Dissipation	90 mW
Supply Voltage	3 V
Technology	0.6-μm CMOS

Table 1. Measured performance.

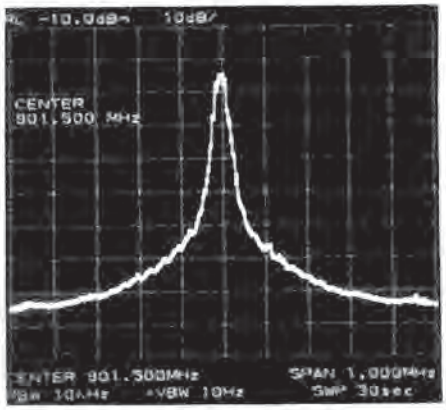
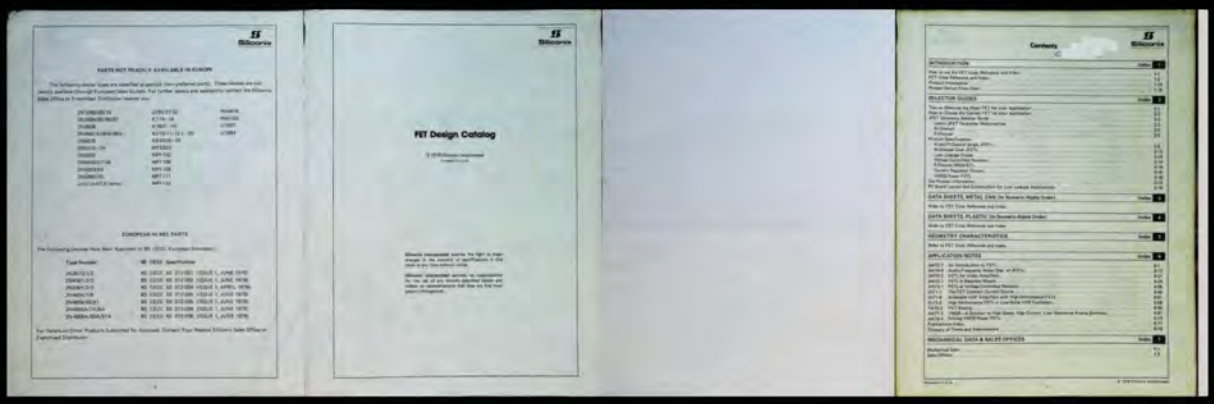


Fig. 6. LO divided output spectrum. (Horiz., 100 kHz/div.;Vert. 10 dB/div.; Resolution bandwidth, 10 kHz.)

Authorized licensed use limited to: Penn State University. Downloaded on June 25,2025 at 18:37:35 UTC from IEEE Xplore. Restrictions apply.

APPENDIX SILICONIX01

INTERNET ARCHIVE WEB TEXTS VIDEO AUDIO SOFTWARE IMAGES SIGN UP | LOG IN UPLOAD Search
ABOUT BLOG PROJECTS HELP DONATE CONTACT JOBS VOLUNTEER PEOPLE



Siliconix FET Design Catalog 1979pdf

by RFguru

Favorite Share Flag

Publication date	2023-06-21
Topics	databook, Field Effect Transistor, Siliconix, FET
Collection	catalogs_inbox; catalogs; additional_collections
Language	English
Item Size	123.4M

Contains all the FETs manufactured by Siliconix up to 1979, with application notes.

Addeddate	2023-06-22 03:21:13
Identifier	siliconix-fet-design-catalog-1979pdf
Identifier-ark	ark:/13960/s2g813rrn70
Ocr	tesseract 5.3.0-3-g9920
Ocr_detected_lang	en
Ocr_detected_lang_conf	1.0000
Ocr_detected_script	Latin
Ocr_detected_script_conf	0.4579
Ocr_module_version	0.0.21
Ocr_parameters	-l eng
Pdf_module_version	0.0.22
Ppi	150

SHOW MORE

Reviews

Add Review

There are no reviews yet. Be the first one to write a review.

234 Views

DOWNLOAD OPTIONS

CHOCR	1 file
DAISY For users with print-disabilities	Temporarily Unavailable
EPUB	Temporarily Unavailable
FULL TEXT	1 file
HOCR	1 file
ITEM TILE	1 file
OCR PAGE INDEX	1 file
OCR SEARCH TEXT	1 file
PAGE NUMBERS JSON	1 file
PDF	1 file
PDF WITH TEXT	1 file
SINGLE PAGE PROCESSED JP2 ZIP	1 file
TORRENT	1 file

SHOW ALL 16 Files 6 Original

IN COLLECTIONS

Catalogs Inbox and Contributions
Catalogs Collection
Additional Collections

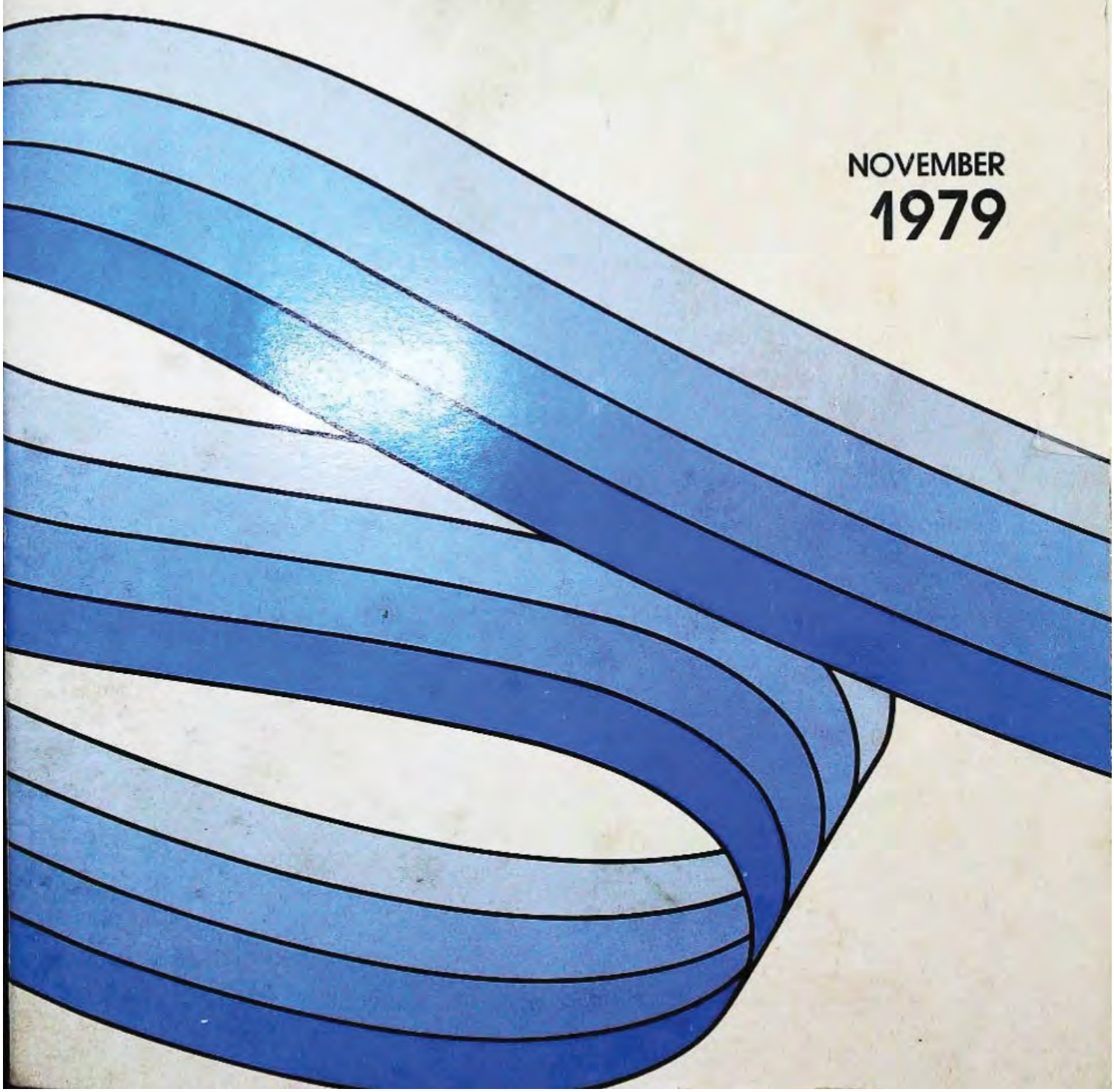
Uploaded by

RFguru
on June 22, 2023

Siliconix

FET Design Catalog

NOVEMBER 1979



Siliconix

PARTS NOT READILY AVAILABLE IN EUROPE

The following device types are classified as *specials* (non-preferred parts). These devices are not readily available through European Sales Outlets. For further details and availability contact the Siliconix Sales Office or Franchised Distributor nearest you.

2N3368/69/70	J230/31/32	PN4416
2N3684/85/86/87	K114–18	PN5163
2N3909	K1837–18	U1837
2N4867A/68A/69A	K210/11/12 (–18)	U1994
2N5078	KK4416–18	
2N5515–24	MFE823	
2N5555	MPF102	
2N5556/57/58	MPF108	
2N5653/54	MPF109	
2N5669/70	MPF111	
JAN/JANTX Series	MPF112	

EUROPEAN HI-REL PARTS

The Following Devices Have Been Approved to BS CECC European Standards:

Type Number	BS CECC Specification
2N3970/1/2	BS CECC 50 012-001 (ISSUE 1, JUNE 1978)
2N4091/2/3	BS CECC 50 012-002 (ISSUE 1, JUNE 1978)
2N4391/2/3	BS CECC 50 012-004 (ISSUE 1, APRIL 1978)
2N4856/7/8	BS CECC 50 012-005 (ISSUE 1, JUNE 1978)
2N4859/60/61	BS CECC 50 012-005 (ISSUE 1, JUNE 1978)
2N4856A/7A/8A	BS CECC 50 012-006 (ISSUE 1, JUNE 1978)
2N4859A/60A/61A	BS CECC 50 012-006 (ISSUE 1, JUNE 1978)

For Details on Other Products Submitted for Approval, Contact Your Nearest Siliconix Sales Office or Franchised Distributor.

Siliconix

FET Design Catalog

© 1979 Siliconix incorporated
Printed in U.S.A.

Siliconix incorporated reserves the right to make changes in the circuitry or specifications in this book at any time without notice.

Siliconix incorporated assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

Contents

Siliconix

INTRODUCTION Index 1

How to use the FET Cross Reference and Index . . . 1-1
FET Cross Reference and Index . . . 1-2
Product Information . . . 1-14
Process Option Flow Chart . . . 1-15

SELECTOR GUIDES Index 2

Tips on Selecting the Right FET for your Application . . . 2-1
How to Choose the Correct FET for your Application . . . 2-2
JFET Geometry Selector Guide . . . 2-3
- Useful JFET Parameter Relationships . . . 2-3
- N-Channel . . . 2-4
- P-Channel . . . 2-5

Product Specifications
- N and P-Channel Single JFETs . . . 2-6
- N-Channel Dual JFETs . . . 2-12
- Low Leakage Diodes . . . 2-14
- Voltage Controlled Resistors . . . 2-14
- P-Channel MOSFETs . . . 2-14
- Current Regulator Diodes . . . 2-15
- VMOS Power FETs . . . 2-16

Die Process Information . . . 2-17
PC Board Layout and Construction for Low Leakage Applications . . . 2-18

DATA SHEETS, METAL CAN (In Numeric-Alpha Order) Index 3

Refer to FET Cross Reference and Index

DATA SHEETS, PLASTIC (In Numeric-Alpha Order) Index 4

Refer to FET Cross Reference and Index

GEOMETRY CHARACTERISTICS Index 5

Refer to FET Cross Reference and Index

APPLICATION NOTES Index 6

AN73-7 An Introduction to FETs . . . 6-1
AN74-4 Audio-Frequency Noise Char. of JFETs . . . 6-13
AN70-2 FETs for Video Amplifiers . . . 6-21
AN72-1 FETs in Balanced Mixers . . . 6-29
AN73-1 FETs as Voltage-Controlled Resistors . . . 6-39
DI71-1 The FET Constant Current Source . . . 6-49
DI71-9 Wideband UHF Amplifiers with High-Performance FETs . . . 6-51
DI73-2 High-Performance FETs in Low-Noise VHF Oscillators . . . 6-55
TA70-2 FET Biasing . . . 6-59
AN77-2 VMOS—A Solution to High Speed, High Current, Low Resistance Analog Switches . . . 6-67
AN79-4 Driving VMOS Power FETs . . . 6-73
Publications Index . . . 6-77
Glossary of Terms and Abbreviations . . . 6-79

MECHANICAL DATA & SALES OFFICES Index 7

Mechanical Data . . . 7-1
Sales Offices . . . 7-3

Printed in U.S.A.

© 1979 Siliconix incorporated

how to use the
FET Cross Reference *and* Index

The following examples illustrate how the FET Cross Reference and Index should be used:

Case (1) Recommended replacement offered by Siliconix is identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N3458	N JFET	2N3458

Case (2) Recommended replacement offered by Siliconix is not identical to Industry Part Number.

Industry Part Number	Type and Classification	Recommended Replacement
2N3457	N JFET	2N4338

The recommended replacement may be exact, tighter or looser on electrical characteristics, and may be a different package or pin-out. Data sheets for both parts should, if possible, be reviewed for a complete comparison. **Refer to appropriate page number listed under Data Sheet or Geometry column.**

Type and classification abbreviations are described as follows:

CR (Current Limiter)
D (Dual)
DPAD (Dual Pico Ampere Diode)
ENH (Enhancement-Mode Normally-Off)
G (Gate)
JPAD (Plastic Pico Ampere Diode)
N (N-Channel)
P (P-Channel)
PAD (Pico Ampere Diode)
VMOS (Vertical MOSFET)

© 1979 Siliconix incorporated

FET Cross Reference *and* Index

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
1N5283	CL N JFET	CR022	3-45	5-12
1N5284	CL N JFET	CR024	3-45	5-12
1N5285	CL N JFET	CR027	3-45	5-12
1N5286	CL N JFET	CR030	3-45	5-12
1N5287	CL N JFET	CR033	3-45	5-12
1N5288	CL N JFET	CR039	3-45	5-12
1N5289	CL N JFET	CR043	3-45	5-12
1N5290	CL N JFET	CR047	3-45	5-12
1N5291	CL N JFET	CR056	3-45	5-12
1N5292	CL N JFET	CR062	3-45	5-12
1N5293	CL N JFET	CR068	3-45	5-13
1N5294	CL N JFET	CR075	3-45	5-13
1N5295	CL N JFET	CR082	3-45	5-13
1N5296	CL N JFET	CR091	3-45	5-13
1N5297	CL N JFET	CR100	3-45	5-13
1N5298	CL N JFET	CR110	3-45	5-13
1N5299	CL N JFET	CR120	3-45	5-13
1N5300	CL N JFET	CR130	3-45	5-13
1N5301	CL N JFET	CR140	3-45	5-13
1N5302	CL N JFET	CR150	3-45	5-13
1N5303	CL N JFET	CR160	3-45	5-14
1N5304	CL N JFET	CR180	3-45	5-14
1N5305	CL N JFET	CR200	3-45	5-14
1N5306	CL N JFET	CR220	3-45	5-14
1N5307	CL N JFET	CR240	3-45	5-14
1N5308	CL N JFET	CR270	3-45	5-14
1N5309	CL N JFET	CR300	3-45	5-14
1N5310	CL N JFET	CR330	3-45	5-14
1N5311	CL N JFET	CR360	3-45	5-14
1N5312	CL N JFET	CR390	3-45	5-14
1N5313	CL N JFET	CR430	3-45	5-14
1N5314	CL N JFET	CR470	3-45	5-14
2N2386	P JFET	2N608		
2N2386A	P JFET	2N609		
2N2497	P JFET	2N3329		
2N2498	P JFET	2N3330		
2N2499	P JFET	2N3331		
2N2500	P JFET	2N3332		
2N506	P JFET	2N2608		
2N2606JAN	P JFET	2N2608JAN		
2N2607	P JFET	2N2608		
2N2607JAN	P JFET	2N2608JAN		
2N2608	P JFET	2N2608	3-1	5-36
2N2608JAN	P JFET	2N2608JAN		
2N2609	P JFET	2N2609	3-1	5-37
2N2609JAN	P JFET	2N2609JAN		
2N2841	P JFET	2N2843		
2N2842	P JFET	2N2843		
2N2843	P JFET	2N2843	3-2	5-36
2N2844	P JFET	2N2844	3-2	5-37
2N3066	N JFET	2N4340		
2N3067	N JFET	2N4338		
2N3068	N JFET	2N4338		
2N3069	N JFET	2N4341		
2N3070	N JFET	2N4339		
2N3071	N JFET	2N4338		
2N3084	N JFET	2N3459		
2N3085	N JFET	2N3459		
2N3086	N JFET	2N3459		
2N3087	N JFET	2N3459		
2N3088	N JFET	2N3460		
2N3088A	N JFET	2N3460		
2N3089	N JFET	2N3460		
2N3089A	N JFET	2N3460		
2N3113	P JFET	2N2843		
2N3277	P JFET	2N2608		
2N3278	P JFET	2N2608		
2N3328	P JFET	2N3438		
2N3329	P JFET	2N3329	3-3	5-36
2N3330	P JFET	2N3330	3-3	5-36
2N3331	P JFET	2N3331	3-3	5-36
2N3332	P JFET	2N3332	3-3	5-36
2N3365	N JFET	2N4340		
2N3366	N JFET	2N4338		
2N3367	N JFET	2N4338		
2N3368	N JFET	2N3368	3-4	5-19
2N3369	N JFET	2N3369	3-4	5-19
2N3370	N JFET	2N3370	3-4	5-19
2N3376	P JFET	2N3329		
2N3378	P JFET	2N3330		
2N3380	P JFET	2N3331		
2N3382	P JFET	2N3382	3-5	5-38
2N3384	P JFET	2N3384	3-5	5-38
2N3386	P JFET	2N3386	3-5	5-38
2N3436	N JFET	2N3436	3-6	5-19
2N3437	N JFET	2N3437	3-6	5-19
2N3438	N JFET	2N3438	3-6	5-19
2N3452	N JFET	2N4340		
2N3453	N JFET	2N4338		
2N3454	N JFET	2N4338		
2N3455	N JFET	2N4340		
2N3456	N JFET	2N4338		
2N3457	N JFET	2N4338		
2N3458	N JFET	2N3458	3-7	5-19
2N3459	N JFET	2N3459	3-7	5-19
2N3460	N JFET	2N3460	3-7	5-19
2N3574	P JFET	2N2843		
2N3575	P JFET	2N2843		
2N3578	P JFET	2N2608		
2N3608	P MOS ENH	3N163		
2N3684	N JFET	2N3684	3-8	5-6
2N3685	N JFET	2N3685	3-8	5-6
2N3686	N JFET	2N3686	3-8	5-6
2N3687	N JFET	2N3687	3-8	5-6
2N3819	N JFET	2N3819	4-1	5-25
2N3820	P JFET	J270		
2N3821	N JFET	2N3821	3-9	5-25
2N3822	N JFET	2N3822	3-9	5-25
2N3823	N JFET	2N3823	3-10	5-25
2N3824	N JFET	2N3824	3-11	5-25

© 1979 Siliconix Incorporated

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N3909	P JFET	2N3909	3-12	5-36
2N3909A	P JFET	2N3909		
2N3921	D N JFET	2N3921	3-13	5-17
2N3922	D N JFET	2N3922	3-13	5-17
2N3954	D N JFET	2N3954	3-14	5-6
2N3954A	D N JFET	2N3954A	3-14	5-6
2N3955	D N JFET	2N3955	3-14	5-6
2N3955A	D N JFET	2N3955A	3-14	5-6
2N3956	D N JFET	2N3956	3-15	5-6
2N3957	D N JFET	2N3957	3-15	5-6
2N3958	D N JFET	2N3958	3-15	5-6
2N3966	N JFET	2N3966	3-16	5-8
2N3967	N JFET	2N4221		
2N3967A	N JFET	2N4221		
2N3968	N JFET	2N3685		
2N3968A	N JFET	2N3685		
2N3969	N JFET	2N3686		
2N3969A	N JFET	2N3686		
2N3970	N JFET	2N3970	3-17	5-3
2N3971	N JFET	2N3971	3-17	5-3
2N3972	N JFET	2N3972	3-17	5-3
2N3993	P JFET	2N3386		
2N3993A	P JFET	2N3386		
2N3994	P JFET	2N3382		
2N3994A	P JFET	2N3382		
2N4084	D N JFET	2N4084	3-13	5-17
2N4085	D N JFET	2N4085	3-13	5-17
2N4091	N JFET	2N4091	3-19	5-3
2N4091A	N JFET	2N4091		
2N4092	N JFET	2N4092	3-19	5-3
2N4092A	N JFET	2N4092		
2N4093	N JFET	2N4093	3-19	5-3
2N4093A	N JFET	2N4093		
2N4117	N JFET	2N4117	3-20	5-29
2N4117A	N JFET	2N4117A	3-20	5-29
2N4118	N JFET	2N4118	3-20	5-29
2N4118A	N JFET	2N4118A	3-20	5-29
2N4119	N JFET	2N4119	3-20	5-29
2N4119A	N JFET	2N4119A	3-20	5-29
2N4120	P MOS ENH	3N163		
2N4139	N JFET	2N3822		
2N4220	N JFET	2N4220	3-22	5-25
2N4220A	N JFET	2N4220A	3-22	5-25
2N4221	N JFET	2N4221	3-22	5-25
2N4221A	N JFET	2N4221A	3-22	5-25
2N4222	N JFET	2N4222	3-22	5-25
2N4222A	N JFET	2N4222A	3-22	5-25
2N4223	N JFET	2N4223	3-23	5-25
2N4224	N JFET	2N4224	3-23	5-25
2N4267	P MOS ENH	3N163		
2N4302	N JFET	PN4302-18		
2N4303	N JFET	PN4303-18		
2N4304	N JFET	PN4304-18		
2N4338	N JFET	2N4338	3-24	5-19
2N4339	N JFET	2N4339	3-24	5-19
2N4340	N JFET	2N4340	3-24	5-19
2N4341	N JFET	2N4341	3-24	5-19
2N4352	P MOS ENH	3N163		
2N4381	F JFET	2N2609		
2N4382	P JFET	2N5115		
2N4391	N JFET	2N4391	3-26	5-3
2N4392	N JFET	2N4392	3-26	5-3
2N4393	N JFET	2N4393	3-26	5-3
2N4416	N JFET	2N4416	3-27	5-8
2N4416A	N JFET	2N4416A	3-27	5-8
2N445	N JFET	2N5432		
2N446	N JFET	2N5433		
2N448	N JFET	2N5432		
2N448	N JFET	2N5433		
2N4856	N JFET	2N4856	3-28	5-3
2N4856A	N JFET	2N4856A	3-29	5-3
2N4856JAN	N JFET	2N4856JAN		5-3
2N4856JANTX	N JFET	2N4856JANTX		5-3
2N4856JANTXV	N JFET	2N4856JANTXV		5-3
2N4857	N JFET	2N4857	3-28	5-3
2N4857A	N JFET	2N4857A	3-29	5-3
2N4857JAN	N JFET	2N4857JAN		5-3
2N4857JANTX	N JFET	2N4857JANTX		5-3
2N4857JANTXV	N JFET	2N4857JANTXV		5-3
2N4858	N JFET	2N4858	3-28	5-3
2N4858A	N JFET	2N4858A	3-29	5-3
2N4858JAN	N JFET	2N4858JAN		5-3
2N4858JANTX	N JFET	2N4858JANTX		5-3
2N4858JANTXV	N JFET	2N4858JANTXV		5-3
2N4859	N JFET	2N4859	3-28	5-3
2N4859A	N JFET	2N4859A	3-29	5-3
2N4859JAN	N JFET	2N4859JAN		5-3
2N4859JANTX	N JFET	2N4859JANTX		5-3
2N4859JANTXV	N JFET	2N4859JANTXV		5-3
2N4860	N JFET	2N4860	3-28	5-3
2N4860A	N JFET	2N4860A	3-29	5-3
2N4860JAN	N JFET	2N4860JAN		5-3
2N4860JANTX	N JFET	2N4860JANTX		5-3
2N4860JANTXV	N JFET	2N4860JANTXV		5-3
2N4861	N JFET	2N4861	3-28	5-3
2N4861A	N JFET	2N4861A	3-29	5-3
2N4861JAN	N JFET	2N4861JAN		5-3
2N4861JANTX	N JFET	2N4861JANTX		5-3
2N4861JANTXV	N JFET	2N4861JANTXV		5-3
2N4867	N JFET	2N4867	3-30	5-27
2N4867A	N JFET	2N4867A	3-30	5-27
2N4868	N JFET	2N4868	3-30	5-27
2N4868A	N JFET	2N4868A	3-30	5-27
2N4869	N JFET	2N4869	3-30	5-27
2N4869A	N JFET	2N4869A	3-30	5-27
2N4977	N JFET	2N5432		
2N4978	N JFET	2N5433		
2N4979	N JFET	2N5434		
2N5018	P JFET	2N5018	3-31	5-39
2N5019	P JFET	2N5019	3-31	5-39

© 1979 Siliconix Incorporated

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N5020	P JFET	2N2843		
2N5021	P JFET	2N2608		
2N5033	P JFET	2N2608		
2N5045	D N JFET	2N5045	3-32	5-17
2N5046	D N JFET	2N5046	3-32	5-17
2N5047	D N JFET	2N5047	3-32	5-17
2N5103	N JFET	2N4416		
2N5104	N JFET	2N4416		
2N5105	N JFET	2N4416		
2N5114	P JFET	2N5114	3-33	5-39
2N5115	P JFET	2N5115	3-33	5-39
2N5116	P JFET	2N5116	3-33	5-39
2N5158	N JFET	2N5434		
2N5159	N JFET	2N5433		
2N5196	D N JFET	2N5196	3-34	5-15
2N5197	D N JFET	2N5197	3-34	5-15
2N5198	D N JFET	2N5198	3-34	5-15
2N5199	D N JFET	2N5199	3-34	5-15
2N5245	N JFET	KK4418		
2N5246	N JFET	J305-18		
2N5247	N JFE	J304-18		
2N5248	N JFET	2N5486		
2N5257	N JFET	2N5457		
2N5258	N JFET	2N5458		
2N5259	N JFET	2N5459		
2N5265	P JFET	2N2608		
2N5266	P JFET	2N2608		
2N5267	P JFET	2N2608		
2N5268	P JFET	2N2608		
2N5269	P JFET	2N3331		
2N5270	P JFET	2N3331		
2N5358	N JFET	2N3686		
2N5359	N JFET	2N3686		
2N5360	N JFET	2N3685		
2N5361	N JFET	2N3684		
2N5362	N JFET	2N3684		
2N5363	N JFET	2N4222A		
2N5364	N JFET	2N4224		
2N5391	N JFET	2N4857A		
2N5392	N JFET	2N4858A		
2N5393	N JFET	2N4869A		
2N5394	N JFET	2N4869A		
2N5395	N JFET	2N4869A		
2N5396	N JFET	2N4869A		
2N5397	N JFET	U310		
2N5398	N JFET	U312		
2N5432	N JFET	2N5432	3-35	5-10
2N5433	N JFET	2N5433	3-35	5-10
2N5434	N JFET	2N5434	3-35	5-10
2N5452	D N JFET	2N5452	3-36	5-6
2N5453	D N JFET	2N5453	3-36	5-6
2N5454	D N JFET	2N5454	3-36	5-6
2N5457	N JFET	2N5457	4-2	5-25
2N5458	N JFET	2N5458	4-2	5-25
2N5459	N JFET	2N5459	4-2	5-25

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N5484	N JFET	2N5484	4-3	5-8
2N5485	N JFET	2N5485	4-3	5-8
2N5486	N JFET	2N5486	4-3	5-8
2N5515	D N JFET	2N5515	3-37	5-27
2N5516	D N JFET	2N5516	3-37	5-27
2N5517	D N JFET	2N5517	3-37	5-27
2N5518	D N JFET	2N5518	3-37	5-27
2N5519	D N JFET	2N5519	3-37	5-27
2N5520	D N JFET	2N5520	3-37	5-27
2N5521	D N JFET	2N5521	3-37	5-27
2N5522	D N JFET	2N5522	3-37	5-27
2N5523	D N JFET	2N5523	3-37	5-27
2N5524	D N JFET	2N5524	3-37	5-27
2N5545	D N JFET	2N5545	3-38	5-15
2N5546	D N JFET	2N5546	3-38	5-15
2N5547	D N JFET	2N5547	3-38	5-15
2N5549	N JFET	2N4392		
2N5555	N JFET	2N5555	4-4	5-8
2N5556	N JFET	2N5556	3-39	5-25
2N5557	N JFET	2N5557	3-39	5-25
2N5558	N JFET	2N5558	3-39	5-25
2N5561	D N JFET	U401		
2N5562	D N JFET	U402		
2N5563	D N JFET	U404		
2N5564	D N JFET	2N5564	3-40	5-3
2N5565	D N JFET	2N5565	3-40	5-3
2N5566	D N JFET	2N5566	3-40	5-3
2N5592	N JFET	2N3822		
2N5593	N JFET	2N3822		
2N5594	N JFET	2N3822		
2N5638	N JFET	2N5638	4-5	5-3
2N5639	N JFET	2N5639	4-5	5-3
2N5640	N JFET	2N5640	4-5	5-3
2N5647	N JFET	2N4117A		
2N5648	N JFET	2N4117A		
2N5649	N JFET	2N4117A		
2N5653	N JFET	2N5653	4-6	5-3
2N5654	N JFET	2N5654	4-6	5-3
2N5668	N JFET	2N5668	4-7	5-8
2N5669	N JFET	2N5669	4-7	5-8
2N5670	N JFET	2N5670	4-7	5-8
2N5797	P JFET	2N2608		
2N5798	P JFET	2N2608		
2N5799	P JFET	2N2608		
2N5800	P JFET	2N2608		
2N5801	N JFET	2N4393		
2N5802	N JFET	2N4393		
2N5803	N JFET	2N4392		
2N5902	D N JFET	2N5902	3-41	5-29
2N5903	D N JFET	2N5903	3-41	5-29
2N5904	D N JFET	2N5904	3-41	5-29
2N5905	D N JFET	2N5905	3-41	5-29
2N5906	D N JFET	2N5906	3-41	5-29
2N5907	D N JFET	2N5907	3-41	5-29
2N5908	D N JFET	2N5908	3-41	5-29

© 1979 Siliconix Incorporated

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2N5909	D N JFET	2N5909	3-41	5-29
2N5911	D N JFET	2N5911	3-43	5-34
2N5912	D N JFET	2N5912	3-43	5-34
2N5949	N JFET	K1837-18		
2N5950	N JFET	K1837-18		
2N5951	N JFET	K1837-18		
2N5952	N JFET	K305-18		
2N5953	N JFET	K305-18		
2N6451	N JFET	2N4393		
2N6452	N JFET	2N4393		
2N6453	N JFET	2N4393		
2N6454	N JFET	2N4393		
2N6483	D N JFET	U401		
2N6484	D N JFET	U402		
2N6585	D N JFET	U404		
2N6568	N JFET	U290		
2N6656	V MOS N ENH	2N6656		
2N6657	V MOS N ENH	2N6657		
2N6658	V MOS N ENH	2N6658		
2N6659	V MOS N ENH	2N6659		
2N6660	V MOS N ENH	2N6660		
2N6661	V MOS N ENH	2N6661		
3N145	P MOS ENH	3N163		
3N146	P MOS ENH	3N163		
3N155	P MOS ENH	3N163		
3N155A	P MOS ENH	3N163		
3N156	P MOS ENH	3N163		
3N156A	P MOS ENH	3N163		
3N157	P MOS ENH	3N163		
3N157A	P MOS ENH	3N163		
3N158	P MOS ENH	3N163		
3N158A	P MOS ENH	3N163		
3N163	P MOS ENH	3N163	3-44	5-1
3N164	P MOS ENH	3N164	3-44	5-1
3N174	P MOS ENH	3N163		
14T	N JFET	2N4224		
142T	N JFET	PN4392		
158T	N JFET	2N4302		
159T	N JFET	KK4416-18		
100S	N JFET	2N4304		
100U	N JFET	2N3684		
102M	N JFET	2N5486		
102S	N JFET	2N4302		
103M	N JFET	2N5457		
103S	N JFET	2N5459		
104M	N JFET	2N5458		
105M	N JFET	2N5459		
105U	N JFET	2N4222		
106M	N JFET	2N5485		
107M	N JFET	2N5486		
110U	N JFET	2N3685		
115U	N JFET	2N4340		
120U	N JFET	2N3686		
125U	N JFET	2N4339		
130U	N JFET	2N3687		

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
135U	N JFET	2N4339		
155U	N JFET	2N4416		
182S	N JFET	2N4391		
183S	N JFET	2N3823		
197S	N JFET	2N4338		
198S	N JFET	2N4340		
199S	N JFET	2N4341		
200S	N JFET	2N4392		
200U	N JFET	2N3824		
201S	N JFET	2N4391		
202S	N JFET	2N4392		
203S	N JFET	2N3821		
204S	N JFET	2N3821		
210U	N JFET	2N4416		
231S	D N JFET	2N3954		
232S	D N JFET	2N3955		
233S	D N JFET	2N3956		
234S	D N JFET	2N3957		
235S	D N JFET	2N3958		
241U	N JFET	2N4869		
250U	N JFET	2N4091		
251U	N JFET	2N4392		
703U	N JFET	2N4220		
704U	N JFET	2N4220		
705U	N JFET	2N4224		
707U	N JFET	2N4860		
714U	N JFET	2N3822		
734U	N JFET	2N4416		
734EU	N JFET	KK4416-18		
751U	N JFET	2N4340		
752U	N JFET	2N4340		
753U	N JFET	2N4341		
754U	N JFET	2N4340		
755U	N JFET	2N4341		
756U	N JFET	2N4340		
1277A	N JFET	2N3822		
1278A	N JFET	2N3821		
1279A	N JFET	2N3821		
1280A	N JFET	2N4224		
1281A	N JFET	2N3822		
1282A	N JFET	2N4341		
1283A	N JFET	2N4340		
1284A	N JFET	2N4222		
1285A	N JFET	2N3821		
1286A	N JFET	2N4220		
1325A	N JFET	2N4222		
1714A	N JFET	2N4340		
2000M	N JFET	2N3823		
2001M	N JFET	2N3823		
2078A	D N JFET	2N3955		
2079A	D N JFET	2N3955		
2080A	D N JFET	2N5546		
2081A	D N JFET	2N5546		
2093M	N JFET	2N3687		
2094M	N JFET	2N3686		

© 1979 Siliconix Incorporated

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
2095M	N JFET	2N3686		
2098A	D NJFET	2N5545		
2099A	D N JFET	2N5546		
2130U	D N JFET	2N5452		
2132U	D N JFET	2N3955		
2134U	D N JFET	2N3956		
2136U	D N JFET	2N3957		
2138U	D N JFET	2N3958		
2139U	D N JFET	2N3958		
2147U	D N JFET	2N3958		
2148U	D N JFET	2N3958		
2149U	D N JFET	2N3958		
A5T3821	N JFET	K305-18		
A5T3822	N JFET	K305-18		
A5T3823	N JFET	KK4416-18		
A5T3824	N JFET	J302-18		
A192	N JFET	2N4416		
AD830	D N JFET	U421		
AD831	D N JFET	U421		
AD832	D N JFET	U422		
AD833	D N JFET	U426		
AD833A	D N JFET	U423		
AD835	D N JFET	2N3921		
AD836	D N JFET	2N3921		
AD837	D N JFET	2N3922		
AD838	D N JFET	2N4085		
AD839	D N JFET	2N4085		
AD840	D N JFET	2N5196		
AD841	D N JFET	2N5197		
AD842	D N JFET	2N5199		
AD3954	D N JFET	2N3954		
AD3954A	D N JFET	2N3954A		
AD3955	D N JFET	2N3955		
AD3956	D N JFET	2N3956		
AD3957	D N JFET	2N3957		
AD3958	D N JFET	2N3958		
BC264	N JFET	2N4304		
BC264A	N JFET	2N4302		
BC264B	N JFET	2N4304		
BC264C	N JFET	2N4304		
BC264D	N JFET	KK4416-18		
BFR45	N JFET	2N4416		
BFS21	D N JFET	2N5199		
BFS21A	D N JFET	2N5199		
BFS67	N JFET	2N3821		
BFS67P	N JFET	2N4303		
BFS68	N JFET	2N3823		
BFS68P	N JFET	KK4416-18		
BFS70	N JFET	2N3821		
BFS71	N JFET	2N3822		
BFS72	N JFET	2N3823		
BFS73	N JFET	2N3821		
BFS74	N JFET	2N4856		
BFS75	N JFET	2N4857		
BFS76	N JFET	2N4858		
BFS77	N JFET	2N4859		
BFS78	N JFET	2N4860		
BFS79	N JFET	2N4861		
BFS80	N JFET	2N4416A		
BFW10	N JFET	2N3823		
BFW11	N JFET	2N3822		
BFW54	N JFET	2N3822		
BFW55	N JFET	2N3822		
BFW56	N JFET	2N4869		
BFW61	N JFET	2N4224		
BSV22	N JFET	2N4416		
BSV78	N JFET	2N4856A		
BSV80	N JFET	2N4858A		
C413N	N JFET	2N5434		
C673	N JFET	2N4341		
C674	N JFET	2N4341		
C680	N JFET	2N4338		
C680A	N JFET	2N4338		
C681	N JFET	2N4338		
C681A	N JFET	2N4338		
C682	N JFET	2N4339		
C682A	N JFET	2N4339		
C683	N JFET	2N4339		
C683A	N JFET	2N4339		
C684	N JFET	2N4220		
C684A	N JFET	2N4220		
C685	N JFET	2N4220		
C685A	N JFET	2N4220		
C6690	N JFET	2N3458		
C6691	N JFET	2N3458		
C6892	N JFET	2N3459		
CM600	N JFET	2N4092		
CM601	N JFET	2N4091		
CM602	N JFET	2N4091		
CM603	N JFET	2N4091		
CM640	N JFET	2N4093		
CM641	N JFET	2N4093		
CM642	N JFET	2N4093		
CM643	N JFET	2N4092		
CM644	N JFET	2N4092		
CM645	N JFET	2N4092		
CM646	N JFET	2N4092		
CM647	N JFET	2N4091		
CM650	N JFET	2N5432		
CM651	N JFET	2N5433		
CM652	N JFET	2N5432		
CM653	N JFET	2N5433		
CM697	N JFET	2N5434		
CM800	N JFET	2N5434		
CMX740	N JFET	U290		
CP640	N JFET	U296		
CP643	N JFET	2N5434		
CP650	N JFET	U322		
CP651	N JFET	U320		
CP652	N JFET	U322		
CP653	N JFET	U320		

© 1979 Siliconix Incorporated

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
CR022 Thru CR470 Referenced Under 1N Series				
DPAD1	D PAD N JFET	DPAD1	3-48	
DPAD2	D PAD N JFET	DPAD2	3-48	
DPAD5	D PAD N JFET	DPAD5	3-48	
DPAD10	D PAD N JFET	DPAD10	3-48	
DPAD20	D PAD N JFET	DPAD20	3-48	
DPAD50	D PAD N JFET	DPAD50	3-48	
DPAD100	D PAD N JFET	DPAD100	3-48	
DU4339	D N JFET	U235		
DU4340	D N JFET	U235		
E100	N JFET	J203-18		
E101	N JFET	J201-18		
E102	N JFET	J202-18		
E103	N JFET	J105-18		
E105	N JFET	J105-18		
E106	N JFET	J106-18		
E107	N JFET	J107-18		
E108	N JFET	J108-18		
E109	N JFET	J109-18		
E110	N JFET	J110-18		
E111	N JFET	J111-18		
E112	N JFET	J112-18		
E113	N JFET	J113-18		
E114	N JFET	K114-18		
E174	P JFET	J174-18		
E175	P JFET	J175-18		
E176	P JFET	J176-18		
E177	P JFET	J177-18		
E201	N JFET	J201-18		
E202	N JFET	J202-18		
E203	N JFET	J203-18		
E204	N JFET	J204-18		
E210	N JFET	K210-18		
E211	N JFET	K211-18		
E212	N JFET	K212-18		
E230	N JFET	J230-18		
E231	N JFET	J231-18		
E232	N JFET	J232-18		
E270	P JFET	J270-18		
E271	P JFET	J271-18		
E300	N JFET	K300-18		
E304	N JFET	K304-18		
E305	N JFET	K305-18		
E308	N JFET	K308-18		
E309	N JFET	K309-18		
E310	N JFET	K310-18		
E400	D N JFET	U410		
E401	D N JFET	U411		
E402	D N JFET	U410		
E410	D N JFET	U410		
E411	D N JFET	U411		
E412	D N JFET	U412		
E413	D N JFET	U410		
E414	D N JFET	U411		
E415	D N JFET	U412		
E420	D N JFET	U440		
E421	D N JFET	U441		
E430	D N JFET	U430		
E431	D N JFET	U431		
E500	CL N JFET	J500		
E501	CL N JFET	J501		
E502	CL N JFET	J502		
E503	CL N JFET	J503		
E504	CL N JFET	J504		
E505	CL N JFET	J505		
E506	CL N JFET	J506		
E507	CL N JFET	J507		
EPAD50	DD N JFET	JPAD50		
EPAD100	DD N JFET	JPAD100		
EPAD200	DD N JFET	JPAD200		
EPAD500	DD N JFET	JPAD500		
FE100	N JFET	2N3821		
FE100A	N JFET	2N3821		
FE102	N JFET	2N4119		
FE102A	N JFET	2N4119		
FE104	N JFET	2N4118		
FE104A	N JFET	2N4118		
FE200	N JFET	2N3821		
FE202	N JFET	2N3821		
FE204	N JFET	2N3821		
FE300	N JFET	2N3822		
FE302	N JFET	2N3821		
FE304	N JFET	2N3821		
FE0654A	N JFET	2N5486		
FE0654B	N JFET	2N5485		
FE3819	N JFET	2N3819		
FE5457	N JFET	2N5457		
FE5458	N JFET	2N5458		
FE5459	N JFET	2N5459		
FE5484	N JFET	2N5484		
FE5485	N JFET	2N5485		
FE5486	N JFET	2N5486		
FM3954	D N JFET	2N3954		
FM3954A	D N JFET	2N3954A		
FM3955	D N JFET	2N3955		
FM3955A	D N JFET	2N3955A		
FM3956	D N JFET	2N3956		
FM3957	D N JFET	2N3957		
FM3958	D N JFET	2N3958		
FT0654A	N JFET	2N5486		
FT0654B	N JFET	2N5486		
FT0654C	N JFET	2N4221		
FT0654D	N JFET	2N4221		
FT704	P MOS ENH	3N163		
GET5457	N JFET	2N5457		
GET5458	N JFET	2N5458		
GET5459	N JFET	2N5459		
HDIG1030	P MOS ENH	3N163		
ID100	D PAD N JFET	DPAD1		

© 1979 Siliconix Incorporated

Siliconix

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
ID101	D PAD N JFET	DPAD10		
IMF3954	D N JFET	2N3954		
IMF3954A	D N JFET	2N3954A		
IMF3955	D N JFET	2N3955		
IMF3955A	D N JFET	2N3955A		
IMF3956	D N JFET	2N3956		
IMF3957	D N JFET	2N3957		
IMF3958	D N JFET	2N3958		
IMF6485	D N JFET	U405		
IT100	P JFET	2N5116		
IT101	P JFET	2N5114		
IT108	N JFET	2N5486		
IT109	N JFET	U310		
IT1700	P MOS ENH	3N163		
IT1702	P MOSENH	3N163		
ITE500	CL N JFET	J500		
ITE501	CL N JFET	J501		
ITE502	CL N JFET	J502		
ITE503	CL N JFET	J503		
ITE504	CL N JFET	J504		
ITE505	CL N JFET	J505		
ITE506	CL N JFET	J506		
ITE507	CL N JFET	J507		
ITE3066	N JFET	J202-18		
ITE3067	N JFET	J201-18		
ITE3068	N JFET	J201-18		
ITE4117	N JFET	2N4117		
ITE4118	N JFET	2N4118		
ITE4119	N JFET	2N4119		
ITE4338	N JFET	J201-18		
ITE4339	N JFET	J201-18		
ITE4340	N JFET	J202-18		
ITE4341	N JFET	J203-18		
ITE4391	N JFET	PN4391-18		
ITE4392	N JFET	PN4392-18		
ITE4393	N JFET	PN4393-18		
ITE4416	N JFET	KK4416-18		
ITE4867	N JFET	J230-18		
ITE4868	N JFET	J231-18		
ITE4869	N JFET	J232-18		
J105	N JFET	J105	4-8	5-31
J105-18	N JFET	J105-18	4-8	5-31
J106	N JFET	J106	4-8	5-31
J106-18	N JFET	J106-18	4-8	5-31
J107	N JFET	J107	4-8	5-31
J107-18	N JFET	J107-18	4-8	5-31
J108	N JFET	J108	4-9	5-10
J108-18	N JFET	J108-18	4-9	5-10
J109	N JFET	J109	4-9	5-10
J109-18	N JFET	J109-18	4-9	5-10
J110	N JFET	J110	4-9	5-10
J110-18	N JFET	J110-18	4-9	5-10
J111	N JFET	J111	4-10	5-3
J111-18	N JFET	J111-18	4-10	5-3
J112	N JFET	J112	4-10	5-3
J112-18	N JFET	J112-18	4-10	5-3
J113	N JFET	J113	4-10	5-3
J113-18	N JFET	J113-18	4-10	5-3
J114	N JFET	J114	4-11	5-34
J174	P JFET	J174	4-12	5-39
J174-18	P JFET	J174-18	4-12	5-39
J175	P JFET	J175	4-12	5-39
J175-18	P JFET	J175-18	4-12	5-39
J176	P JFET	J176	4-12	5-39
J176-18	P JFET	J176-18	4-12	5-39
J177	P JFET	J177	4-12	5-39
J177-18	P JFET	J177-18	4-12	5-39
J201	N JFET		4-13	5-19
J201-18	N JFET		4-13	5-19
J202	N JFET		4-13	5-19
J202-18	N JFET		4-13	5-19
J203	N JFET		4-13	5-19
J203-18	N JFET		4-13	5-19
J204	N JFET	J204	4-14	5-19
J204-18	N JFET	J204-18	4-14	5-19
J210	N JFET	J210	4-15	5-34
J211	N JFET	J211	4-15	5-34
J212	N JFET	J212	4-15	5-34
J230	N JFET	J230	4-16	5-27
J230-18	N JFET	J230-18	4-16	5-27
J231	N JFET	J231	4-16	5-27
J231-18	N JFET	J231-18	4-16	5-27
J232	N JFET	J232	4-16	5-27
J232-18	N JFET	J232-18	4-16	5-27
J270	P JFET	J270	4-17	5-39
J270-18	P JFET	J270-18	4-17	5-39
J271	P JFET	J271	4-17	5-39
J271-18	P JFET	J271-18	4-17	5-39
J300	N JFET	J300	4-18	5-34
J304	N JFET	J304	4-19	5-8
J305	N JFET	J305	4-19	5-8
J308	N JFET	J308	4-20	5-32
J309	N JFET	J309	4-20	5-32
J310	N JFET	J310	4-20	5-32
J401	D N JFET	U401		
J402	D N JFET	U402		
J403	D N JFET	U403		
J404	D N JFET	U404		
J405	D N JFET	U405		
J406	D N JFET	U406		
J410	D N JFET	U410		
J411	D N JFET	U411		
J412	D N JFET	U412		
J500	CL N JFET	J500	4-21	5-5
J501	CL N JFET	J501	4-21	5-5
J502	CL N JFET	J502	4-21	5-5
J503	CL N JFET	J503	4-21	5-5
J504	CL N JFET	J504	4-21	5-5
J505	CL N JFET	J505	4-21	5-5
J506	CL N JFET	J506	4-22	5-5

© 1979 Siliconix incorporated

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
J507	CL N JFET	J507	4-22	5-5
J508	CL N JFET	J508	4-22	5-5
J509	N JFET	J509	4-22	5-5
J510	N JFET	J510	4-22	5-5
J511	CL N JFET	J511	4-22	5-5
JPAD50	PAD N JFET	JPAD50	4-23	
JPAD100	PAD N JFET	JPAD100	4-23	
JPAD200	PAD NJFET	JPAD200	4-23	
JPAD500	PAD N JFET	JPAD500	4-23	
J1401	D N JFET	U401		
J1402	D N JFET	U402		
J1403	D N JFET	U403		
J1404	D N JFET	U404		
J1405	D N JFET	U405		
J1406	D N JFET	U406		
K114-18	N JFET	K114-18	4-24	5-34
K1837-18	N JFET	K1837-18	4-25	5-8
K210-18	N JFET	K210-18	4-26	5-34
K211-18	N JFET	K210-18	4-26	5-34
K212-18	N JFET	K210-18	4-26	5-34
K300-18	N JFET	K300-18	4-27	5-34
K304-18	N JFET	K304-18	4-28	5-8
K305-18	N JFET	K304-18	4-28	5-8
K308-18	N JFET	K308-18	4-29	5-32
K309-18	N JFET	K309-18	4-29	5-32
K310-18	N JFET	K310-8	4-29	5-32
KE3684	N JFET	2N3684		
KE3685	N JFET	2N3685		
KE3686	N JFET	2N3686		
KE3687	N JFET	2N3687		
KE3823	N JFET	J304-18		
KE3970	N JFET	PN4391-18		
KE3971	N JFET	PN4392-18		
KE3972	N JFET	PN4393-18		
KE4091	N JFET	PN4391-18		
KE4092	N JFET	PN4392-18		
KE4093	N JFET	PN4393-18		
KE4220	N JFET	2N5457		
KE4221	N JFET	2N5457		
KE4222	N JFET	2N5459		
KE4223	N JFET	J304-18		
KE4224	N JFET	J304-18		
KE4391	N JFET	PN4391-18		
KE4392	N JFET	PN4392-18		
KE4393	N JFET	PN4393-18		
KE4416	N JFET	KK4416-18		
KE4856	N JFET	PN4391-18		
KE4857	N JFET	PN4392-18		
KE4858	N JFET	PN4393-18		
KE4859	N JFET	PN4391-18		
KE4860	N JFET	PN4392-18		
KE4861	N JFET	PN4393-18		
KE5103	N JFET	K305-18		
KE5104	N JFET	K304-18		
KE5105	N JFET	K304-18		
KK4416-18	N JFET	KK4416-18	4-30	5-8
LDF603	N JFET	2N4221A		
LDF604	N JFET	2N4221A		
LDF605	N JFET	2N4221A		
M163	P MOS ENH	3N163		
M164	P MOS ENH	3N164		
MEM520	P MOS ENH	3N164		
MEM520C	P MOS ENH	3N164		
MEM561	P MOS ENH	3N163		
MEM561C	P MOS ENH	3N163		
MEM806	P MOS ENH	3N163		
MEM806A	P MOS ENH	3N163		
MFE823	P MOS ENH	MFE823	3-47	5-1
MFE2000	N JFET	2N4416		
MFE2001	N JFET	2N4416		
MFE2004	N JFET	2N4093		
MFE2005	N JFET	2N4092		
MFE2006	N JFET	2N4091		
MFE2007	N JFET	2N4860		
MFE2008	N JFET	2N4859		
MFE2009	N JFET	2N4859		
MFE2010	N JFET	2N5434		
MFE2011	N JFET	2N5433		
MFE2012	N JFET	2N5432		
MFE2093	N JFET	2N3687		
MFE2094	N JFET	2N3686		
MFE2095	N JFET	2N3685		
MFE4007	P JFET	2N2608		
MFE4008	P JFET	2N2608		
MFE4009	P JFET	2N3329		
MFE4010	P JFET	2N3330		
MFE4011	P JFET	2N3330		
MFE4012	P JFET	2N3331		
MK10	N JFET	2N4416		
MMF1	D N JFET	2N3921		
MMF2	D N JFET	2N3921		
MMF3	D N JFET	2N3921		
MMF4	D N JFET	2N3921		
MMF5	D N JFET	2N3921		
MMF6	D N JFET	2N3921		
MMT3823	N JFET	2N3823		
MPF102	N JFET	MPF102	4-31	5-8
MPF103	N JFET	2N5457		
MPF104	N JFET	2N5458		
MPF105	N JFET	2N5459		
MPF106	N JFET	2N5485		
MPF107	N JFET	2N5486		
MPF108	N JFET	MPF108	4-32	5-8
MPF109	N JFET	MPF109	4-33	5-25
MPF111	N JFET	MPF111	4-34	5-25
MPF112	N JFET	MPF112	4-35	5-8
MPF256	N JFET	J309		
MPF820	N JFET	U310		
MPF970	P JFET	J174		
MPF971	P JFET	J176		

© 1979 Siliconix incorporated

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
MPF4391	N JFET	PN4391-18		
MPF4392	N JFET	PN4392-18		
MPF4393	N JFET	PN4393-18		
NF500	N JFET	2N4416		
NF501	N JFET	2N4416		
NF506	N JFET	2N4416		
NF510	N JFET	2N4393		
NF511	N JFET	2N4393		
NF520	N JFET	2N3684		
NF521	N JFET	2N3686		
NF522	N JFET	2N3684		
NF523	N JFET	2N3686		
NF530	N JFET	2N4341		
NF531	N JFET	2N4339		
NF532	N JFET	2N4341		
NF533	N JFET	2N4339		
NF580	N JFET	2N5432		
NF581	N JFET	2N5432		
NF582	N JFET	2N5433		
NF583	N JFET	2N5434		
NF584	N JFET	2N5433		
NF585	N JFET	2N4859		
NF4302	N JFET	2N4302		
NF4303	N JFET	2N4303		
NF4304	N JFET	2N4304		
NF4445	N JFET	2N5432		
NF4446	N JFET	2N5433		
NF4447	N JFET	2N5432		
NF4448	N JFET	2N5433		
NF5163	N JFET	2N5163		
NF5457	N JFET	2N5457		
NF5458	N JFET	2N5458		
NF5459	N JFET	2N5459		
NF5484	N JFET	2N5484		
NF5485	N JFET	2N5485		
NF5486	N JFET	2N5486		
NF5555	N JFET	2N5555		
NF5638	N JFET	2N5638		
NF5639	N JFET	2N5639		
NF5640	N JFET	2N5640		
NF5653	N JFET	2N5653		
NF5654	N JFET	2N5654		
PAD1	PAD N JFET	PAD1	3-49	
PAD2	PAD N JFET	PAD2	3-49	
PAD5	PAD N JFET	PAD5	3-49	
PAD10	PAD N JFET	PAD10	3-49	
PAD20	PAD N JFET	PAD20	3-49	
PAD50	PAD N JFET	PAD50	3-49	
PAD100	PAD N JFET	PAD100	3-49	
P1086	P JFET	P1086	4-36	5-39
P1086-18	P JFET	P1086-18	4-36	5-39
P1087	P JFET	P1087	4-36	5-39
P1087-18	P JFET	P1087-18	4-36	5-39
PN4091	N JFET	PN4091	4-37	5-3
PN4092	N JFET	PN4092	4-37	5-3
PN4093	N JFET	PN4093	4-37	5-3
PN4302	N JFET	PN4302	4-38	5-19
PN4302-18	N JFET	PN4302-18	4-38	5-19
PN4303	N JFET	PN4303	4-38	5-19
PN4303-18	N JFET	PN4303-18	4-38	5-19
PN4304	N JFET	PN4304	4-38	5-19
PN4304-18	N JFET	PN4304-18	4-38	5-19
PN4391	N JFET	PN4391	4-39	5-3
PN4391-18	N JFET	PN4391-18	4-39	5-3
PN4392	N JFET	PN4392	4-39	5-3
PN4392-18	N JFET	PN4392-18	4-39	5-3
PN4393	N JFET	PN4393	4-39	5-3
PN4393-18	N JFET	PN4393-18	4-39	5-3
PN4416	N JFET	PN4416	4-40	5-8
PN5163	N JFET	PN5163	4-41	
PF510	P JFET	2N5018		
PF511	P JFET	2N5014		
SU2078	D N JFET	U425		
SU2079	D N JFET	U425		
SU2098	D N JFET	2N5197		
SU2098A	D N JFET	2N5197		
SU2098B	D N JFET	2N5196		
SU2099	D N JFET	2N5197		
SU2099A	D N JFET	2N5197		
SU2365	D N JFET	U401		
SU2365A	D N JFET	U401		
SU2366	D N JFET	U402		
SU2366A	D N JFET	U402		
SU2367	D N JFET	U403		
SU2367A	D N JFET	U403		
SU2368	D N JFET	U404		
SU2368A	D N JFET	U404		
SU2369	D N JFET	U405		
SU2369A	D N JFET	U405		
SU2410	D N JFET	U424		
SU2411	D N JFET	U425		
SU2412	D N JFET	U426		
TD5902	D N JFET	2N5902		
TD5902	D N JFET	2N5902		
TD5902A	D N JFET	2N5902		
TD5903	D N JFET	2N5903		
TD5903A	D N JFET	2N5903		
TD5904	D N JFET	2N5904		
TD5904A	D N JFET	2N5904		
TD5905	D N JFET	2N5905		
TD5905A	D N JFET	2N5905		
TD5906	D N JFET	2N5906		
TD5906A	D N JFET	2N5906		
TD5907	D N JFET	2N5907		
TD5907A	D N JFET	2N5907		
TD5908	D N JFET	2N5908		
TD5908A	D N JFET	2N5908		
TD5909	D N JFET	2N5909		
TD5909A	D N JFET	2N5909		
TD5911	D N JFET	2N5911		

© 1979 Siliconix incorporated

Siliconix

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
TD5911A	D N JFET	2N5911		
TD5912	D N JFET	2N5912		
TD5912A	D N JFET	2N5912		
TIS14	N JFET	2N4340		
TIS25	D N JFET	U401		
TIS26	D N JFET	U402		
TIS27	D N JFET	U404		
TIS41	N JFET	2N4859		
TIS58	N JFET	J305-18		
TIS59	D N JFET	U1837		
TIS73	N JFET	PN4391-18		
TIS74	N JFET	PN4392-18		
TIS75	N JFET	PN4393-18		
TIS88	N JFET	2N5486		
TIXS41	N JFET	2N4859		
TIXS42	N JFET	PN4393-18		
TN4117	N JFET	2N4117		
TN4117A	N JFET	2N4117A		
TN4118	N JFET	2N4118		
TN4118A	N JFET	2N4118A		
TN4119	N JFET	2N4119		
TN4119A	N JFET	2N4119A		
TN4338	N JFET	2N4338		
TN4339	N JFET	2N4339		
TN4340	N JFET	2N4340		
TN4341	N JFET	2N4341		
TP5114	P JFET	2N5114		
TP5115	P JFET	2N5115		
TP5116	P JFET	2N5116		
U110	P JFET	2N2608		
U112	P JFET	2N2608		
U133	P JFET	2N2608		
U146	P JFET	2N2608		
U147	P JFET	2N2608		
U148	P JFET	2N2608		
U149	P JFET	2N2609		
U168	P JFET	2N2609		
U182	N JFET	2N4857		
U183	N JFET	2N3824		
U197	N JFET	2N4339		
U198	N JFET	2N4340		
U199	N JFET	2N4341		
U200	N JFET	U200	3-50	5-3
U201	N JFET	U201	3-50	5-3
U202	N JFET	U202	3-50	5-3
U221	N JFET	2N4391		
U222	N JFET	2N4391		
U231	D N JFET	U231	3-51	5-15
U232	D N JFET	U232	3-51	5-15
U233	D N JFET	U233	3-51	5-15
U234	D N JFET	U234	3-51	5-15
U235	D N JFET	U235	3-51	5-15
U240	N JFET	2N5432		
U241	N JFET	2N5433		
U242	N JFET	2N5432		
U243	N JFET	2N5433		
U248	D N JFET	2N5902		
U248A	D N JFET	2N5906		
U249	D N JFET	2N5903		
U249A	D N JFET	2N5907		
U250	D N JFET	2N5904		
U250A	D N JFET	2N5908		
U251	D N JFET	2N5905		
U251A	D N JFET	2N5909		
U254	N JFET	2N4859		
U255	N JFET	2N4860		
U256	N JFET	2N4861		
U257	D N JFET	U257	3-52	5-34
U273	N JFET	2N4118A		
U273A	N JFET	2N4118A		
U274	N JFET	2N4119A		
U274A	N JFET	2N4119A		
U275	N JFET	2N4119A		
U275A	N JFET	2N4119A		
U280	D N JFET	U231		
U281	D N JFET	U231		
U282	D N JFET	U232		
U283	D N JFET	U232		
U284	D N JFET	U233		
U285	D N JFET	U234		
U290	N JFET	U290	3-53	5-31
U291	N JFET	U291	3-53	5-31
U295	N JFET	U295		
U296	N JFET	U296		
U300	P JFET	2N5114		
U301	P JFET	2N5115		
U304	P JFET	U304	3-54	5-39
U305	P JFET	U305	3-54	5-39
U306	P JFET	U306	3-54	5-39
U308	N JFET	U308	3-55	5-32
U309	N JFET	U309	3-55	5-32
U310	N JFET	U310	3-55	5-32
U311	N JFET	U311	3-57	5-32
U312	N JFET	U312	3-58	5-34
U320	N JFET	U320	3-59	5-10
U321	N JFET	U321	3-59	5-10
U322	N JFET	U322	3-59	5-10
U401	D N JFET	U401	3-61	5-17
U402	D N JFET	U402	3-61	5-17
U403	D N JFET	U403	3-61	5-17
U404	D N JFET	U404	3-61	5-17
U405	D N JFET	U405	3-61	5-17
U406	D N JFET	U406	3-61	5-17
U410	D N JFET	U410	3-63	5-21
U411	D N JFET	U411	3-63	5-21
U412	D N JFET	U412	3-63	5-21
U421	D N JFET	U421	3-64	5-23
U422	D N JFET	U422	3-64	5-23
U423	D N JFET	U423	3-64	5-23
U424	D N JFET	U424	3-64	5-23

© 1979 Siliconix incorporated

Siliconix

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
U425	D N JFET	U425	3-64	5-23
U426	D N JFET	U426	3-64	5-23
U430	D N JFET	U430	3-66	5-32
U431	D N JFET	U431	3-66	5-32
U440	D N JFET	U440	3-67	5-34
U441	D N JFET	U441	3-67	5-34
U508	N JFET	CR030		
U1177	N JFET	2N4220A		
U1178	N JFET	2N3821		
U1179	N JFET	2N3821		
U1180	N JFET	2N4221A		
U1181	N JFET	2N4220A		
U1182	N JFET	2N3821		
U1277	N JFET	2N3684		
U1278	N JFET	2N3685		
U1279	N JFET	2N3686		
U1280	N JFET	2N3684		
U1281	N JFET	2N3822		
U1282	N JFET	2N4341		
U1283	N JFET	2N4340		
U1284	N JFET	2N4341		
U1285	N JFET	2N4220		
U1286	N JFET	2N4341		
U1287	N JFET	2N4092		
U1321	N JFET	2N3966		
U1322	N JFET	2N4221A		
U1323	N JFET	2N4221A		
U1324	N JFET	2N4220A		
U1325	N JFET	2N4222		
U1420	N JFET	2N3821		
U1421	N JFET	2N3822		
U1422	N JFET	2N3822		
U1714	N JFET	2N4340		
U1837	N JFET	U1837	4-42	5-8
U1837E	N JFET	U1837		
U1897	N JFET	U1897	4-43	5-3
U1897-18	N JFET	U1897-18	4-43	5-3
U1897E	N JFET	U1897-18		
U1898	N JFET	U1898	4-43	5-3
U1898-18	N JFET	U1898-18	4-43	5-3
U1898E	N JFET	U1898-18		
U1899	N JFET	U1899	4-43	5-3
U1899-18	N JFET	U1899-18	4-43	5-3
U1899E	N JFT	U1899-18		
U1994	N JFET	U1994	4-44	5-8
U1994E	N JFET	U1994		
U2047E	N JFET	KK4416-18		
U3000	N JFET	2N4341		
U3001	N JFET	2N4339		
U3002	N JFET	2N4338		
U3010	N JFET	2N4341		
U3011	N JFET	2N4340		
U3012	N JFET	2N4338		
UC20	N JFET	2N3687		
UC40	P JFET	2N2608		
UC41	P JFET	2N2608		
UC100	N JFET	2N3684		
UC110	N JFET	2N3685		
UC115	N JFET	2N4340		
UC120	N JFET	2N3686		
UC130	N JFET	2N3687		
UC155	N JFET	2N4416		
UC200	N JFET	2N3824		
UC201	N JFET	2N3824		
UC210	N JFET	2N4416		
UC220	N JFET	2N3822		
UC240	N JFET	2N4869		
UC241	N JFET	2N4869		
UC250	N JFET	2N4091		
UC251	N JFET	2N4392		
UC300	P JFET	2N2608		
UC310	P JFET	2N2843		
UC320	P JFET	2N2843		
UC330	P JFET	2N2843		
UC340	P JFET	2N2843		
UC400	P JFET	2N3331		
UC401	P JFET	2N5116		
UC410	P JFET	2N3330		
UC420	P JFET	2N3329		
UC450	P JFET	2N5114		
UC451	P JFET	2N5116		
UC588	N JFET	2N4417		
UC703	N JFET	2N4220		
UC704	N JFET	2N4220		
UC705	N JFET	2N4224		
UC707	N JFET	2N4860		
UC714	N JFET	2N3822		
UC714E	N JFET	J203-18		
UC734	N JFET	2N4416		
UC734E	N JFET	KK4416-18		
UC751	N JFET	2N4340		
UC752	N JFET	2N4340		
UC753	N JFET	2N4341		
UC754	N JFET	2N4340		
UC755	N JFET	2N4341		
UC756	N JFET	2N4340		
UC805	P JFET	2N3331		
UC807	N JFET	2N4860		
UC814	P JFET	2N3331		
UC851	P JFET	2N2608		
UC853	P JFET	2N2608		
UC854	P JFET	2N2608		
UC855	P JFET	2N2609		
UC1700	P MOS ENH	3N163		
UC1764	P MOS ENH	3N163		
UC2130	D N JFET	2N5452		
UC2132	D N JFET	2N3955		
UC2134	D N JFET	2N3956		
UC2136	D N JFET	2N3957		
UC2138	D N JFET	2N3958		

© 1979 Siliconix Incorporated

Siliconix

FET Cross Reference *and* Index (cont'd.)

Siliconix

Industry Part Number	Type and Classification	Recommended Replacement	Data Sheet Page	Geometry Page
UC2139	D N JFET	2N3958		
UC2147	D N JFET	2N3958		
UC2148	D N JFET	2N3958		
UC2149	D N JFET	2N3958		
VCR2N	N JFET	VCR2N	3-68	5-3
VCR3P	P JFET	VCR3P	3-68	5-38
VCR4N	N JFET	VCR4N	3-68	5-19
VCR5P	P JFET	VCR5P	3-68	5-36
VCR6P	P JFET	2N5116		
VCR7N	N JFET	VCR7N	3-68	5-29
VMP1	VMOS N ENH	2N6657		
VMP2	VMOS N ENH	2N6660		
VMP4	VMOS N ENH	VMP4		
VMP11	VMOS N ENH	2N6656		
VMP12	VMOS N ENH	2N6658		
VMP21	VMOS N ENH	2N6659		
VMP22	VMOS N ENH	2N6661		
VN30AA	VMOS N ENH	VN30AA		
VN30AB	VMOS N ENH	VN30AB		
VN33AJ	VMOS N ENH	VN33AJ		
VN33AK	VMOS N ENH	VN33AK		
VN35AA	VMOS N ENH	VN35AA		
VN35AB	VMOS N ENH	VN35AB		
VN35AJ	VMOS N ENH	VN35AJ		
VN35AK	VMOS N ENH	VN35AK		
VN40AF	VMOS N ENH	VN40AF		
VN46AF	VMOS N ENH	VN46AF		
VN64GA	VMOS N ENH	VN64GA		
VN66AF	VMOS N ENH	VN64GF		
VN66AJ	VMOS N ENH	VN66AJ		
VN66AK	VMOS N ENH	VN66AK		
VN67AA	VMOS N ENH	VN67AA		
VN67AB	VMOS N ENH	VN67AB		
VN67AF	VMOS N ENH	VN67AF		
VN67AJ	VMOS N ENH	VN67AJ		
VN67AK	VMOS N ENH	VN67AK		
VN88AF	VMOS N ENH	VN88AF		
VN89AA	VMOS N ENH	VN89AA		
VN89AB	VMOS N ENH	VN89AB		
VN89AF	VMOS N ENH	VN89AF		
VN90AA	VMOS N ENH	VN90AA		
VN90AB	VMOS N ENH	VN90AB		
VN98AJ	VMOS N ENH	VN98AJ		
VN98AK	VMOS N ENH	VN98AK		
VN99AJ	VMOS N ENH	VN99AJ		
VN99AK	VMOS N ENH	VN99AK		
WK5457	N JFET	2N5457		
WK5458	N JFET	2N5458		
WK5459	N JFET	2N5459		

Siliconix

© 1979 Siliconix Incorporated

product information

Siliconix

Siliconix products are divided into three basic categories:

Standard Products, Modified Standard Products, Custom Products

- **Standard Products** — All the part numbers described in this catalog are standard products. A summary list of the prefixes used is shown below in the Device Identification Table. Ordering any of the standard products is easily done by referring to the data sheet part number. For example, a 2N4391 is simply ordered by that number: "2N4391." It will also appear in that form on the price lists, published separately.
- **Examples of Modified Standard Products are:**

Electrical Specials — Devices with either tightened, relaxed and/or special electrical specifications selected from a standard product.

Mechanical Specials — Devices with standard or modified electrical specifications mounted in non-standard packages or modified (lead formed) standard packages. Modifications and/or additions to standard marking are also considered mechanical specials.

High Reliability Specials — Siliconix has a number of standard High-Reliability screening options that can be ordered as standard products. These options include MIL-750B. High-Rel process option details will be found in the introductory section of this data book. In addition, Siliconix offers certain JEDEC-registered FETs with JAN, JANTX, or JANTXV processing. Refer to any current Siliconix OEM price list for details on specific part numbers. If existing screening processes do not meet individual customer requirements, Siliconix can provide special additional inspections and controls to meet the stringent demands.

In all of the above cases (with the exception of JAN, JANTX, or JANTXV parts), a special part number is assigned which defines the part either by reference to customer's print(s) or by associated special requirements. Each special product is proprietary to the customer, and is *not* made available to other customers.

- **Custom Products** — Are designed to meet customer requirements not realizable by selection from standard parts; usually, these products require special engineering development. The proprietary relationship described above also applies to custom products.

Inquiries for *SPECIAL DEVICES* may be directed to the nearest field sales office or to:

FET Marketing Department, Siliconix incorporated, 2201 Laurelwood Road, Santa Clara, California 95054, Telephone: (408) 988-8000.

FETs/Part Number Prefixes and Suffixes

Prefix	XXX	XXXX
CR	Si Standard N-Channel Current Regulator	
DPAD	Si Standard Dual JFET Diode	
FN	Special N-Channel JFET	Special N-Channel JFET
J	Si Standard TO-92 Cased FET	Special TO-92 Cased FET
JPAD	Si Standard TO-92 Cased JFET Diode	
K	Si Standard TO-92 Cased FET	
KK	Si Standard TO-92 Cased FET	
M	Si Standard MOSFET	
MEM	Si Standard MOSFET	
MU	Special MOSFET	
PAD	Si Standard JFET Diode	
PF	Special P-Channel JFET	
PN		Si Standard TO-92 Cased FET
SU	Special P-Channel JFET	
U	Si Standard FET	Si Standard FET
VCR	Si Standard N- and P-Channel Voltage Controlled Resistors	
VMP	VMOS Power FET N-Channel	
VN		VMOS Power FET N-Channel
2N		JEDEC-Registered Device
3N	JEDEC-Registered Device	

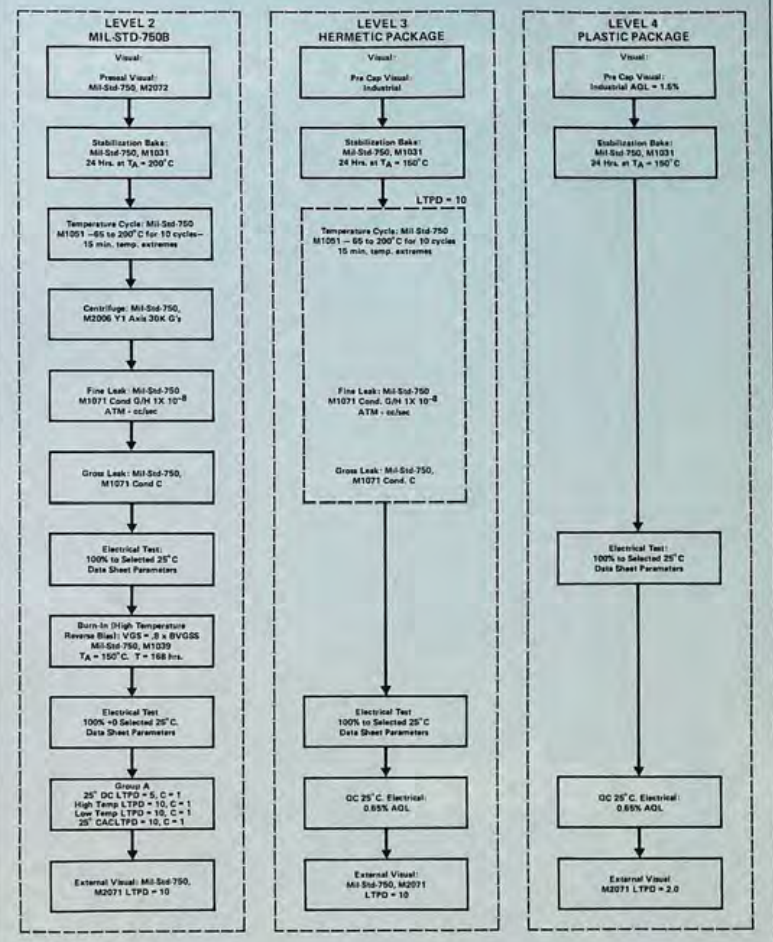
Suffix	
-18	Std TO-92 Package with Center Lead Formed Toward Flat in TO-18 Pin Circle

The above prefix list does not include some second source products supplied by Siliconix. Refer to FET Cross Reference and Index or current price list for availability of these devices.

© 1979 Siliconix Incorporated

process option flow chart

Siliconix



© 1979 Siliconix Incorporated

selector guides

index 2

tips on selecting the right FET for your application

Siliconix

The "Product Specification," a short form version of technical data, will provide you direct reference to Siliconix part numbers and a condensed version of technical specifications

IF YOU ARE NOT FAMILIAR WITH THE FET PARAMETERS YOU NEED:

1. Turn to page 2-2 "How to Choose the Correct FET for Your Application." Using this guide, determine the important FET parameters.
2. Next, turn to page 2-4 "JFET Geometry Selector Guide." Using this guide, choose the appropriate geometry.
3. Once you have chosen a geometry, turn to the "Geometry Characteristics" section 5 of the catalog. Here you make the choice of a suitable part number.
4. Now that you have the part number, you will find complete electrical specifications of these products In the "Data Sheets" sections 3 and 4 of the catalog.

IF YOU ARE FAMILIAR WITH THE PARAMETERS YOU NEED:

1. Turn to the "Product Specifications" pages 2-6 through 2-16 to determine the proper part number(s).
2. Double-check your choices against the data sheets, and select the part most suited for your application.

© 1979 Siliconix incorporated

how to choose the correct FET for your application

Siliconix

Application	Detail Application	Important FET Parameters Required	Major Tradeoffs	Unimportant FET Parameters
AMPLIFIER	Audio	Low noise ($\overline{E_n}$), g_{fs}/g_{os}	Voltage amplification factor μ = g_{fs}/g_{os} = $\Delta V_{DS}/\Delta V_{GS}$ @ I_D = const	$R_{DS(on)}$, $V_{DS(on)}$, $I_{D(off)}$, Switching Times
	Buffer	Low I_G, high g_{fs}		
	Differential	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G		
	High Input Impedance	Very low I_G (eg., MOSFET)		
	High Frequency	High g_{fs}/C_{iss} ratio, NF, RF parameters		
	FET Input Op Amp	Good matching V_{GS}, g_{fs}, I_{DSS}, I_G		
	Low Distortion	High $V_{GS(off)}$ compared to signal amplitude		
	Low Supply Voltage	Low $V_{GS(off)}$		
	Low Noise	Low $\overline{e_n}$, $\overline{i_n}$, low 1/f noise, low NF		Noise, $\overline{e_n}$, NF while using high level signals
	Preamplifier	Operate near I_{DZO}, high g_{fs}/I_D ratio		
	Video	High g_{fs}/C_{iss} ratio, NF		
CONSTANT CURRENT SOURCE	Current Limiting	Low g_{os}, low $V_{GS(off)}$, high BV_{GSS}	g_{fs}, $R_{DS(on)}$, $I_{D(off)}$, $V_{DS(on)}$ switching times, RF parameters capacitance	RF parameters while operating below RF frequencies
	Reference Current Source			
	Biasing			
MIXERS	VHF	RF parameters, NF, high g_{fs}/C_{iss} ratio, low C_{rss}	$R_{DS(on)}$, $V_{DS(on)}$, $I_{D(off)}$	Capacitance & switching times while operating in audio and lower frequencies
	UHF			
	Double Balanced	Matching characteristics		
OSCILLATORS	Class A	Good g_{fs} at operating frequency		
	Class C	Low C_{iss} for VHF operation		
SWITCHES	Analog Gates	Fast switching time	$R_{DS(on)}$ vs Capacitance	g_{fs}, g_{os}
	Choppers	$r_{DS}/I_{D(off)}$ switching efficiency		
	Commutators	Low C_{rss}		
	Digital	Fast switching time		
	Integrator Reset	Very low $R_{DS(on)}$, High I_{DSS}		
	Sample and Hold	Low C_{rss}		
VOLTAGE CONTROLLED RESISTORS	Gain Control	High $V_{GS(off)}$ for wide dynamic range and low distortion		g_{fs}, BV_{GSS}, I_{DSS}
	Amplitude Stability			
	Attenuators			

© 1979 Siliconix Incorporated

JFET geometry selector guide

Siliconix

Once you have chosen the major FET parameters, you will find selecting the optimum JFET geometry is easy. If you are familiar with Field Effect Transistors, start your selection using the characteristic graphs on page 2-4. You will find the $V_{GS(off)}$ vs I_{DSS} graph the most meaningful, since it shows — in order of ascending active area — the complete line of Siliconix junction FETs.

To give you an idea how this guide works, let's find the most suitable geometry for a 70 ohm ON-resistance analog switch which will be required to operate as close as 5 volts from the negative power supply. The power supply restraint requires a maximum $V_{GS(off)}$ of 5 volts. Examining the $R_{DS(on)}$ vs $V_{GS(off)}$ figure, you will find the NC, NIP, and NVA geometries meet the R_{on} and $V_{GS(off)}$ requirements. In order to minimize your cost, choose the geometry having the least chip area, that is the NC. You will find characteristic data and part numbers in the Geometry Characteristics section of the catalog. Below are the most important parameter inter-relationships expressed in analytical form.

USEFUL JFET PARAMETER RELATIONSHIPS (APPROX.)

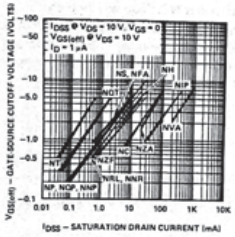
g_{fso}	=	$K \frac{I_{DSS}}{V_{GS(off)}}$	Forward transconductance as a function of I_{DSS} and $V_{GS(off)}$ at zero gate-source voltage (K = 1.5 to 2.5; typically = 2 for N-channel junction FET)
g_{fs}	=	$g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)$	Variation of g_{fs} with gate bias
g_{fs}	=	$g_{fso}\sqrt{I_D/I_{DSS}}$	Variation of g_{fs} with drain current
$V_{GS(off)}$	=	$\frac{2\ I_{DSS}}{g_{fso}}$	Gate-Source cutoff voltage in terms of I_{DSS} and g_{fso}
V_{DS}	≈	$V_{GS(off)}\left(\frac{I_D}{I_{DSS}}\right)^{\frac{1}{2}}$	Drain voltage at which drain current saturates
r_{DS}	≃	$\frac{1}{g_{fs}}$	Reciprocal relationship between drain-source resistance and forward transconductance. Accurate when $V_{DS} < V_{GS(off)}$ i.e., in the triode region
r_{DS}	≃	$\frac{[V_{GS(off)}]^2}{K I_{DSS}\ [V_{GS(off)} - V_{GS}]}$	K = 1.5 to 2.5 Variation of drain resistance in the triode region
I_D	=	$I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$	Variation of drain current with gate-source voltage. The square law transfer characteristic.

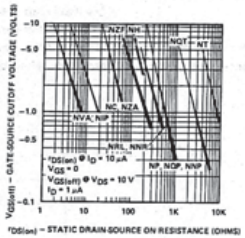
© 1979 Siliconix Incorporated

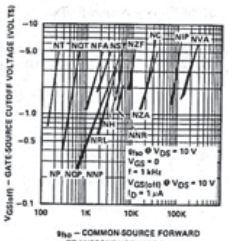
JFET geometry selector guide (cont'd)

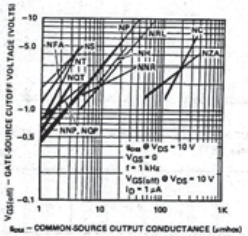
Siliconix

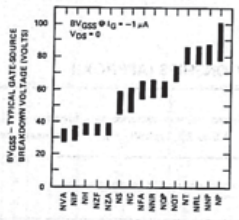
n-channel JFETs

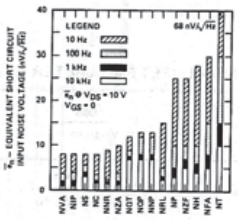


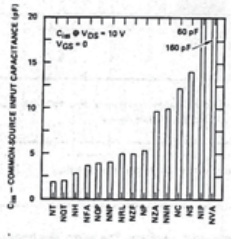


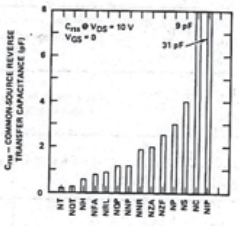










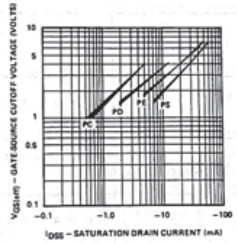


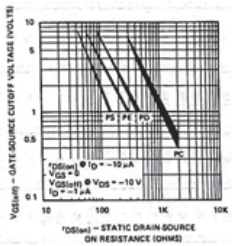
© 1979 Siliconix Incorporated

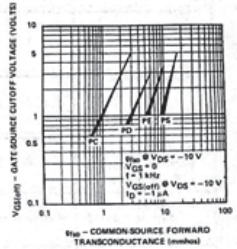
JFET geometry selector guide (cont'd)

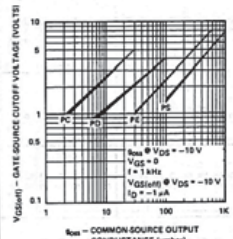
Siliconix

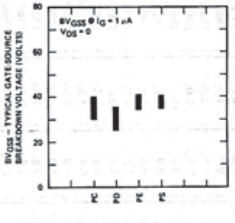
p-channel JFET

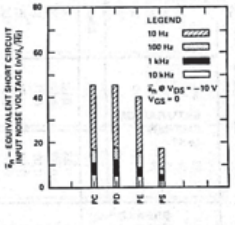


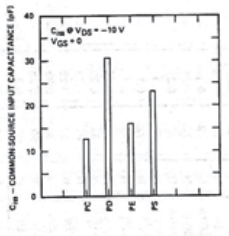


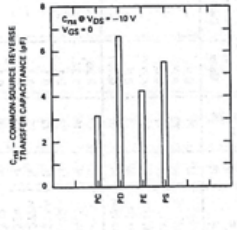












© 1979 Siliconix Incorporated

Product Specifications

N & P-Channel Single JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (umhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		DEVICE	LOW LEAKAGE	RF AMP	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.	GEOMETRY (Section 5)			GEOMETRY (Section 5)
2N411	N	TO-72	0.01	—	1.8	40	0.03	0.09	70	210	3	—	—	—	NT	NT	NP	NP
2N411A	N	TO-72	0.001	—	1.8	40	0.03	0.09	70	210	3	—	—	—	NT	NT	NP	NP
2N4118	N	TO-72	0.01	—	3.0	40	0.08	0.24	80	250	3	—	—	—	NT	NT	NP	NP
2N4118A	N	TO-72	0.001	—	3.0	40	0.08	0.24	80	250	3	—	—	—	NT	NT	NP	NP
2N4119	N	TO-72	0.01	—	6.0	40	0.2	0.6	100	330	3	—	—	—	NT	NT	NP	NP
2N4119A	N	TO-72	0.001	—	6.0	40	0.2	0.6	100	330	3	—	—	—	NT	NT	NP	NP
2N3459	N	TO-18	0.25	—	3.4	60	0.8	4.0	1500	6000	18	4	1M	—	NP	NP	NP	NP
2N4220	N	TO-72	0.1	—	4.0	30	0.5	3.0	1000	4000	6	2.5	1M	—	NRL	NRL	NP	NP
2N4221A	N	TO-72	0.1	—	6.0	30	2.0	6.0	2000	5000	6	2.5	1M	—	NRL	NRL	NP	NP
2N4222A	N	TO-72	0.1	—	8.0	30	5.0	15	2500	6000	6	2.5	1M	—	NRL	NRL	NP	NP
2N4338	N	TO-18	0.1	—	1.0	60	0.2	0.6	600	1800	7	1.0	1M	—	NRL	NRL	NP	NP
2N4339	N	TO-18	0.1	—	1.8	60	0.5	1.5	800	2400	7	1.0	1M	—	NRL	NRL	NP	NP
2N4340	N	TO-18	0.1	—	3.0	60	1.2	3.6	1300	3000	7	1.0	1M	—	NRL	NRL	NP	NP
2N4341	N	TO-18	0.1	—	6.0	60	3.0	9.0	2000	4000	7	1.0	1M	—	NRL	NRL	NP	NP
2N867	N	TO-72	0.25	—	2.0	40	0.4	1.2	700	2000	25	20	—	—	NS	NS	NS	NS
2N867A	N	TO-72	0.25	—	2.0	40	0.4	1.2	700	2000	25	20	—	—	NS	NS	NS	NS
2N4858	N	TO-72	0.25	—	3.0	40	1.0	3.0	1000	3000	25	10	—	—	NS	NS	NS	NS
2N4858A	N	TO-72	0.25	—	3.0	40	1.0	3.0	1000	3000	25	10	—	—	NS	NS	NS	NS
2N4859	N	TO-72	0.25	—	5.0	40	2.5	7.5	1300	4000	25	10	—	—	NS	NS	NS	NS
2N4859A	N	TO-72	0.25	—	5.0	40	2.5	7.5	1300	4000	25	10	—	—	NS	NS	NS	NS
2N5556	N	TO-72	0.1	—	4.0	30	0.5	2.5	1500	6500	6	35	—	—	NRL	NRL	NS	NS
2N5557	N	TO-72	0.1	—	5.0	30	2.0	5.0	1500	6500	6	35	—	—	NRL	NRL	NS	NS
2N5558	N	TO-72	0.1	—	6.0	30	4.0	10	1500	6500	6	35	—	—	NRL	NRL	NS	NS
J230-18	N	TO-92	0.25	—	3.0	40	0.7	3.0	1000	2500	30	—	—	—	NS	NS	NS	NS
J230	N	TO-92	0.25	—	3.0	40	0.7	3.0	1000	2500	30	—	—	—	NS	NS	NS	NS
J231	N	TO-92	0.25	—	5.0	40	2.0	6.0	1500	3000	30	—	—	—	NS	NS	NS	NS
J231-18	N	TO-92	0.25	—	5.0	40	2.0	6.0	1500	3000	30	—	—	—	NS	NS	NS	NS
J232	N	TO-92	0.25	—	6.0	40	5.0	10	2500	4000	30	—	—	—	NS	NS	NS	NS
J232-18	N	TO-92	0.25	—	6.0	40	5.0	10	2500	4000	30	—	—	—	NS	NS	NS	NS
J270-18	P	TO-92	0.2	—	2.0	30	5.0	15	6000	15000	—	—	—	—	PS	PS	PS	PS
2N3819	N	TO-92	0.5	—	8.0	30	2.0	20	2000	6500	8.0	—	1K	—	NRL	NRL	NRL	NRL
2N3823	N	TO-72	0.5	—	8.0	30	4.0	20	3500	6500	6	2.5	1K	—	NRL	NRL	NRL	NRL
2N4223	N	TO-72	0.25	—	8.0	30	3.0	18	3000	7000	6	5.0	1K	—	NRL	NRL	NRL	NRL
2N4224	N	TO-72	0.5	—	8.0	30	2.0	20	2000	7500	6	—	—	—	NRL	NRL	NRL	NRL
2N4416	N	TO-72	0.1	—	6.0	30	5.0	15	4500	7500	4	2.0	1K	—	NH	NH	NP	NP
2N4416A	N	TO-72	0.1	—	6.0	35	5.0	15	4500	7500	4	2.0	1K	—	NH	NH	NP	NP
2N5078	N	TO-72	0.25	—	8.0	30	4.0	25	4500	10000	6	3.0	1K	—	—	—	—	—

© 1979 Siliconix Incorporated

Product Specifications (cont'd)

N & P-Channel Single JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (umhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		DEVICE	RF AMPLIFIERS	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl Ω, Max.	GEOMETRY (Section 5)		GEOMETRY (Section 5)
2N5484	N	TO-92	1.0	—	3.0	25	1.0	5.0	3000	6000	5	3.0	1K	—	NH		NH
2N5485	N	TO-92	1.0	—	4.0	25	4.0	10	3500	7000	5	2.0	1K	—	NH		NH
2N5486	N	TO-92	1.0	—	4.0	25	8.0	20	4000	8000	5	2.0	1K	—	NH		NH
2N5668	N	TO-92	1.0	—	4.0	25	1.0	5.0	1500	6500	7	2.5	1K	—	NH		NH
2N5669	N	TO-92	2.0	—	6.0	25	4.0	10	2000	6500	7	2.5	1K	—	NH		NH
2N5670	N	TO-92	2.0	—	8.0	25	8.0	20	3000	7500	7.0	2.5	1K	—	NH		NH
J210	N	TO-92	0.1	—	3.0	25	2.0	15	4000	12000	—	—	—	—	NZF		NZF
J211	N	TO-92	0.1	—	4.5	25	7.0	20	7000	12000	—	—	—	—	NZF		NZF
J212	N	TO-92	0.1	—	6.0	25	15	40	7000	12000	—	—	—	—	NZF		NZF
J270	P	TO-92	0.2	—	2.0	30	2.0	15	6000	15000	—	—	—	—	PS		PS
J271	P	TO-92	0.2	—	4.5	30	6.0	50	8000	18000	—	—	—	—	PS		PS
J300	N	TO-92	0.5	—	6.0	25	6.0	30	4500	9000	5.5	—	—	—	NZF		NZF
J304	N	TO-92	0.1	—	6.0	30	5.0	15	4500	7500	—	—	—	—	NH		NH
J305	N	TO-92	0.1	—	3.0	30	1.0	8.0	3000	—	—	—	—	—	NH		NH
J308	N	TO-92	1.0	—	6.5	25	12	60	8000	20000	7.5	—	—	—	NZA		NZA
J309	N	TO-92	1.0	—	4.0	25	12	30	10000	20000	7.5	—	—	—	NZA		NZA
J310	N	TO-92	1.0	—	6.5	25	24	60	8000	18000	7.5	—	—	—	NZA		NZA
K210-18	N	TO-92	0.1	—	3.0	25	2.0	15	4000	12000	—	—	—	—	NZF		NZF
K211-18	N	TO-92	0.1	—	4.5	25	7.0	20	7000	12000	—	—	—	—	NZF		NZF
K212-18	N	TO-92	0.1	—	6.0	25	15	40	7000	12000	—	—	—	—	NZF		NZF
K300-18	N	TO-92	0.5	—	6.0	25	6.0	30	4500	9000	5.5	—	—	—	NZF		NZF
K304-18	N	TO-92	0.1	—	6.0	30	5.0	15	4500	7500	—	—	—	—	NH		NH
K305-18	N	TO-92	0.1	—	3.0	30	1.0	8.0	3000	—	—	—	—	—	NH		NH
K308-18	N	TO-92	1.0	—	6.5	25	12	60	8000	20000	7.5	—	—	—	NZA		NZA
K309-18	N	TO-92	1.0	—	4.0	25	12	30	10000	20000	7.5	—	—	—	NZA		NZA
K310-18	N	TO-92	1.0	—	6.5	25	24	60	8000	18000	7.5	—	—	—	NZA		NZA
K1837-18	N	TO-92	0.25	—	8.0	30	4.0	25	4500	10000	6.0	3.0	1K	—	NH		NH
KK416-18	N	TO-92	1.0	—	6.0	30	5.0	15	4500	7500	4.0	2.0	1K	—	NH		NH
PN4416	N	TO-92	1.0	—	6.0	30	5.0	15	4500	7500	4.0	2.0	1K	—	NH		NH
MPF102	N	TO-92	2.0	—	7.5	25	2.0	20	2000	7500	7.0	—	—	—	NH		NH
MPF108	N	TO-92	1.0	—	8.0	25	1.5	24	2000	7500	6.5	2.5	1M	—	NH		NH
MPF112	N	TO-92	100	—	10	25	1.0	25	1000	7500	—	—	—	—	NH		NH
U308	N	TO-52	0.15	—	6.0	25	12	60	10000	20000	7.5	—	—	—	NZA		NZA
U309	N	TO-52	0.15	—	4.0	25	12	30	10000	20000	7.5	—	—	—	NZA		NZA
U310	N	TO-52	0.15	—	6.0	25	24	60	10000	18000	7.5	—	—	—	NZA		NZA
U311	N	TO-72	0.15	—	6.0	25	20	60	10000	20000	7.5	—	—	—	NZA		NZA
U312	N	TO-52	0.1	—	6.0	25	10	30	6000	10000	5.0	—	—	—	NZF		NZF
U320	N	TO-92	3.0	—	10	25	100	500	7500	20000	30	—	—	—	NHP		NHP
U321	N	TO-92	3.0	—	4.0	25	80	250	7500	20000	30	—	—	—	NHP		NHP

© 1979 Siliconix Incorporated

N & P-Channel Single JFETs

Product Specifications (cont'd)

Siliconix

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	LEAKAGE (nA, MAX.) Chnl	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (umhos) Min.	TRANS-CONDUCTANCE gfs (umhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE Gate r1	RESISTANCE Chnl r2, Max.	GEOMETRY (Section 5)	RF AMP	DEVICE
U322	N	39	3.0	—	—	25	200	700	—	7500	30	—	—	NRP	NP	NP	
U1837	N	92	0.25	—	8.0	30	4.0	25	4500	10000	6.0	—	—	1K	NH	NH	
U1837-18	N	92	0.25	—	8.0	30	4.0	25	4500	10000	6.0	—	—	1K	NH	NH	
U1994	N	92	0.1	—	8.0	50	5.0	—	4500	7500	4.0	3.0	—	—	NH	NH	
2N3824	N	72	0.1	1.0	8.0	30	—	—	—	—	6.0	—	—	250	NRL	—	
2N3966	N	72	0.1	1.0	8.0	50	2.0	—	—	—	6.0	—	—	220	NH	—	
2N3970	N	18	0.25	0.25	10	40	50	150	—	—	25	—	—	30	NC	—	
2N3971	N	18	0.25	0.25	5.0	40	25	75	—	—	25	—	—	60	NC	—	
2N3972	N	18	0.25	0.25	3.0	40	5.0	30	—	—	25	—	—	100	NC	—	
2N4091	N	18	0.2	0.2	10	40	50	150	—	—	16	—	—	30	NC	—	
2N4092	N	18	0.2	0.2	7.0	40	25	75	—	—	16	—	—	50	NC	—	
2N4093	N	18	0.2	0.2	5.0	40	8.0	30	—	—	16	—	—	80	NC	—	
2N4391	N	18	0.1	0.1	10	40	50	150	—	—	14	—	—	30	NC	—	
2N4392	N	18	0.1	0.1	5.0	40	25	75	—	—	14	—	—	60	NC	—	
2N4393	N	18	0.1	0.1	3.0	40	5.0	30	—	—	14	—	—	100	NC	—	
2N4856	N	18	0.25	0.25	10	40	50	150	—	—	18	—	—	25	NC	—	
2N4857	N	18	0.25	0.25	6.0	40	20	100	—	—	10	—	—	40	NC	—	
2N4857A	N	18	0.25	0.25	6.0	40	20	100	—	—	10	—	—	40	NC	—	
2N4858	N	18	0.25	0.25	4.0	40	8.0	80	—	—	10	—	—	60	NC	—	
2N4858A	N	18	0.25	0.25	4.0	40	8.0	80	—	—	10	—	—	25	NC	—	
2N4859	N	18	0.25	0.25	10	30	50	150	—	—	10	—	—	40	NC	—	
2N4859A	N	18	0.25	0.25	10	30	50	150	—	—	10	—	—	60	NC	—	
2N4860	N	18	0.25	0.25	6.0	30	20	100	—	—	10	—	—	25	NC	—	
2N4860A	N	18	0.25	0.25	6.0	30	20	100	—	—	10	—	—	40	NC	—	
2N4861	N	18	0.25	0.25	4.0	30	8.0	80	—	—	18	—	—	40	NC	—	
2N4861A	N	18	0.25	0.25	4.0	30	8.0	80	—	—	10	—	—	60	NC	—	
2N5018	P	18	2.0	10.0	5.0	30	10	—	—	—	45	—	—	75	NP	—	
2N5019	P	18	2.0	10.0	5.0	30	10	—	—	—	45	—	—	150	NP	—	
2N5114	P	18	0.5	0.5	10	30	90	—	—	—	25	—	—	75	PS	—	
2N5115	P	18	0.5	0.5	6.0	30	60	—	—	—	25	—	—	75	PS	—	
2N5116	P	18	0.5	0.5	4.0	30	25	—	—	—	25	—	—	100	PS	—	
2N5432	N	52	0.2	0.2	10	25	150	—	—	—	30	—	—	150	PS	—	
2N5433	N	52	0.2	0.2	9.0	25	100	—	—	—	30	—	—	5.0	NP	—	
2N5434	N	52	0.2	0.2	4.0	25	30	—	—	—	30	—	—	7.0	NP	—	
2N5555	N	52	0.2	10.0	10	25	15	—	—	—	30	—	—	10	NP	—	
2N5638	N	92	1.0	1.0	12	30	50	—	—	—	10	—	—	150	NH	—	
2N5639	N	92	1.0	1.0	8.0	30	25	—	—	—	10	—	—	60	NC	—	

© 1979 Siliconix Incorporated

N & P-Channel Single JFETs

Product Specifications (cont'd)

Siliconix

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	LEAKAGE (nA, MAX.) Chnl	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (umhos) Min.	TRANS-CONDUCTANCE gfs (umhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE Gate r1	RESISTANCE Chnl r2, Max.	GEOMETRY (Section 5)	DEVICE
ZN5640	N	92	1.0	1.0	6.0	30	5.0	—	—	—	10	—	—	100	NC	
ZN5653	N	92	1.0	1.0	12	30	40	500	—	—	10	—	—	50	NC	
ZN5654	N	92	1.0	1.0	8.0	30	15	500	—	—	10	—	—	30	NC	
J105	N	92	3.0	3.0	10.0	25	—	500	—	—	10	—	—	3.0	NVA	
J105-18	N	92	3.0	3.0	10.0	25	—	500	—	—	10	—	—	3.0	NVA	
J106	N	92	3.0	3.0	6.0	25	—	200	—	—	10	—	—	6.0	NVA	
J106-18	N	92	3.0	3.0	6.0	25	—	200	—	—	10	—	—	6.0	NVA	
J107	N	92	3.0	3.0	4.5	25	—	100	—	—	10	—	—	8.0	NVA	
J107-18	N	92	3.0	3.0	4.5	25	—	100	—	—	10	—	—	8.0	NVA	
J108	N	92	3.0	3.0	10	25	—	80	—	—	10	—	—	8.0	NIP	
J108-18	N	92	3.0	3.0	10	25	—	80	—	—	10	—	—	8.0	NIP	
J109	N	92	3.0	3.0	6.0	25	—	40	—	—	10	—	—	12	NIP	
J109-18	N	92	3.0	3.0	6.0	25	—	40	—	—	10	—	—	12	NIP	
J110	N	92	3.0	3.0	4.0	25	—	40	—	—	10	—	—	18	NIP	
J110-18	N	92	3.0	3.0	4.0	25	—	40	—	—	10	—	—	18	NIP	
J111	N	92	1.0	1.0	10	35	—	20	—	—	10	—	—	30	NC	
J111-18	N	92	1.0	1.0	10	35	—	20	—	—	10	—	—	30	NC	
J112	N	92	1.0	1.0	5.0	35	—	20	—	—	10	—	—	50	NC	
J112-18	N	92	1.0	1.0	5.0	35	—	20	—	—	10	—	—	50	NC	
J113	N	92	1.0	1.0	3.0	35	—	5.0	—	—	10	—	—	100	NC	
J113-18	N	92	1.0	1.0	3.0	35	—	5.0	—	—	10	—	—	100	NC	
J114	N	92	1.0	1.0	10	25	—	20	—	—	10	—	—	15	NIP	
J174	P	92	1.0	1.0	10	30	—	100	—	—	20	—	—	15	NIP	
J174-18	P	92	1.0	1.0	6.0	30	—	60	—	—	20	—	—	85	PS	
J175	P	92	1.0	1.0	6.0	30	—	60	—	—	20	—	—	125	PS	
J175-18	P	92	1.0	1.0	4.0	30	—	25	—	—	20	—	—	250	PS	
J176	P	92	1.0	1.0	4.0	30	—	25	—	—	20	—	—	250	PS	
J176-18	P	92	1.0	1.0	2.25	30	—	15	—	—	20	—	—	300	PS	
J177	P	92	1.0	1.0	2.25	30	—	15	—	—	20	—	—	300	PS	
J177-18	P	92	1.0	1.0	2.25	30	—	15	—	—	20	—	—	300	NZP	
K114-18	N	92	1.0	1.0	10	25	—	150	—	—	14	—	—	30	NC	
PN4391	N	92	1.0	1.0	10	40	—	150	—	—	14	—	—	30	NC	
PN4391-18	N	92	1.0	1.0	10	40	—	150	—	—	14	—	—	30	NC	
PN4392	N	92	1.0	1.0	5.0	40	—	75	—	—	14	—	—	60	NC	
PN4392-18	N	92	1.0	1.0	5.0	40	—	75	—	—	14	—	—	60	NC	
PN4393	N	92	1.0	1.0	3.0	40	5.0	30	—	—	14	—	—	100	NC	
PN4393-18	N	92	1.0	1.0	3.0	40	5.0	30	—	—	14	—	—	100	NC	
P1086	P	92	2.0	10.0	10	30	10	—	—	—	45	—	—	75	PS	
P1086-18	P	92	2.0	10.0	10	30	10	—	—	—	45	—	—	75	PS	

© 1979 Siliconix Incorporated

Product Specifications (cont'd)

Siliconix

N & P-Channel Single JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (µmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 5)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl rD, Max.		
P1087	P	92	2.0	10.0	5.0	30	5.0								PS	GENERAL PURPOSE
P1087-18	P	92	2.0	10.0	5.0	30	5.0	75							150	
U200	N	18	1.0	1.0	3.0	30	3.0	25							PS	SWITCHES & CHOPPERS
U201	N	18	1.0	1.0	5.0	30	15	75							150	
U202	N	18	1.0	1.0	10	30	30	150							75	
U290	N	52	1.0	1.0	10	30	200								NC	
U291	N	52	1.0	1.0	4.5	30	500								2.5	
U304	P	18	0.5	0.5	3.0	60	15	60			60				NVA	
U305	P	18	0.5	0.5	6.0	30	30				27				7.0	
U306	P	18	0.5	0.5	4.0	30	5.0	25			27				NVA	
U897	N	92	0.4	0.2	10	40	30				16				85	
U897-18	N	92	0.4	0.2	10	40	30				16				PS	
U898	N	92	0.4	0.2	7.0	40	15				16				110	
U898-18	N	92	0.4	0.2	7.0	40	15				16				PS	
U899	N	92	0.4	0.2	5.0	40	8.0				16				175	
U899-18	N	92	0.4	0.2	5.0	40	8.0				16				PS	
ZN2608	P	18	10			30	0.9	4.5	1000		17	3	1M	1M	PC	
ZN2609	P	18	30			40	2.0	10.0	2500		17	3	1M	1M	PD	
ZN2843	P	18	10			30	0.2	1.0	540		17	3	1M	1M	PC	
ZN2844	P	18	30			30	0.44	2.2	1400		30	3	1M	1M	PD	
ZN3329	P	72	10			50	1.0	3.0	1000		20	3	1M	1M	PC	
ZN3330	P	72	10			60	2.0	6.0	1500		20	3	1M	1M	PD	
ZN3331	P	72	10			80	5.0	15	2000		20	4	1M	1M	PC	
ZN3332	P	72	10			60	2.0	6.0	1000		20	1	1M	1M	PC	
ZN3368	N	18	5.0			40	2.0	12	2000		20	4	1M	1M	PC	
ZN3369	N	18	5.0			40	0.5	2.5	600		20	4	1M	1M	PC	
ZN3370	N	18	5.0			40	0.1	0.6	300		20	4	1M	1M	PC	
ZN3382	P	72	15			30	3.0	30	4500	12500	20				PE	
ZN3384	P	72	15			30	15.0	50	7500	15000					PE	
ZN3386	P	72	15			30	15.0	50	7500	15000					PE	
ZN3436	N	18	0.5			50	3.0	15	2500	10000	18	4	1M	1M	PC	
ZN3437	N	18	0.5			50	0.8	4.0	1500	6000	18	4	1M	1M	NP	
ZN3438	N	18	0.5			50	0.2	1.0	800	4500	18	2	1M	1M	NP	
ZN3458	N	18	0.25			50	3.0	15	2500	10000	18	6	1M	1M	NP	
ZN3684	N	72	0.1			50	2.5	7.5	2000	3000	4	0.5	10M	10M	NFA	
ZN3685	N	72	0.1			50	1.0	3.0	1500	2500	4	0.5	10M	10M	NFA	
ZN3686	N	72	0.1			50	0.4	1.2	1000	2000	4	0.5	10M	10M	NFA	
ZN3687	N	72	0.1			50	0.1	0.5	500	1500	4	0.5	10M	10M	NFA	

© 1979 Siliconix Incorporated

Product Specifications (cont'd)

Siliconix

N & P-Channel Single JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.)		THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MAX.)	SATURATION CURRENT (mA)		TRANS-CONDUCTANCE gfs (µmhos)		INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	RESISTANCE		GEOMETRY (Section 5)	DEVICE
			Gate	Chnl			Min.	Max.	Min.	Max.			Gate Ω	Chnl rD, Max.		
2N3821	N	72	0.1		0.5	50	2.0	10	2.5	4500	6	200			NRL	GENERAL PURPOSE
2N3822	N	72	0.1		2.0	50	0.3	15	1000	6500	6	200			NRL	
2N3909	P	72	10		8.0	20	0.3	15	1000	5000	32				PC	
2N4220	N	72	0.1		4.0	30	0.5	3.0	1000	4000	6				NRL	
2N4221	N	72	0.1		6.0	30	2.0	6.0	2000	5000	6				NRL	
2N4222	N	72	0.1		8.0	30	5.0	15	2500	6000	6				NRL	
2N5457	N	92	1.0		6.0	25	1.0	5.0	1000	5000	7	3.0			NRL	
2N5458	N	92	1.0		7.0	25	2.0	9.0	1500	5500	7	3.0			NRL	
2N5459	N	92	1.0		8.0	25	4.0	16	2000	6000	7	3.0			NRL	
J201	N	92	0.1		1.5	40	0.2	1.0	500		5.0				100M	
J201-18	N	92	0.1		1.5	40	0.2	1.00	500		5.0				NP	
J202	N	92	0.1		4.0	40	0.9	4.5	1000		5.0				NP	
J202-18	N	92	0.1		4.0	40	0.9	4.5	1000		5.0				NP	
J203	N	92	0.1		10	40	4.0	20	1500		5.0				NP	
J203-18	N	92	0.1		10	40	4.0	20	1500		5.0				NP	
J204	N	92	0.1		2.0	25					5.0				NP	
J204-18	N	92	0.1		2.0	25					5.0				NP	
J271-18	P	92	0.2		4.5	30	6.0	50	8000	18000					PS	
P4302	N	92	1.0		4.0	30	0.5	5.0	1000		6	2.0			NP	
P4302-18	N	92	1.0		4.0	30	0.5	5.0	1000		6	2.0			NP	
P4303	N	92	1.0		6.0	30	4.0	10	2000		6	2.0			NP	
P4303-18	N	92	1.0		6.0	30	4.0	10	2000		6	2.0			NP	
P4304	N	92	1.0		10.0	30	0.5	15	1000		6	3.0	1M	1M	NP	
P4304-18	N	92	1.0		10.0	30	0.5	15	1000		6	3.0	1M	1M	NP	
PN5163	N	92	0.1		8.0	25	1.0	40.0	2000	9000	20	50.0	1M	1M	NRL	
MPF109	N	92	1.0		8.0	25	0.5	24	800	6000	7.0	2.5	1M	1M	NRL	
MPF111	N	92	100			20	0.5	20	500		5.0				NRL	

© 1979 Siliconix Incorporated

Product Specifications (cont'd)

Siliconix

N-Channel Dual JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MIN.)	SATURATION CURRENT (mA) Max.	SATURATION CURRENT (mA) Min.	TRANS-CONDUCTANCE gfs (umhos) Max.	TRANS-CONDUCTANCE gfs (umhos) Min.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	THRESHOLD Static Match (mV, Max.)	THRESHOLD Temp Tracking µV/°C	OUTPUT CONDUCTANCE gos (µmhos, MAX.)	GEOMETRY (Section 5)	DEVICE
2N5196	N	71	0.025	4.0	50	0.7	7.0	1000	7.0	6.0	20	5.0	5.0	50	NNP or NP-D	LOW LEAKAGE
2N5197	N	71	0.025	4.0	50	0.7	7.0	1000	7.0	6.0	20	5.0	10	50	NNP or NP-D	
2N5198	N	71	0.025	4.0	50	0.7	7.0	1000	7.0	6.0	20	5.0	20	50	NNP or NP-D	
2N5199	N	71	0.025	4.0	50	0.7	7.0	1000	7.0	6.0	20	5.0	40	50	NNP or NP-D	
2N5545	N	71	0.1	4.5	50	0.5	8.0	1500	8.0	6.0	200	5.0	10	25	NNP or NP-D	
2N5546	N	71	0.1	4.5	50	0.5	8.0	1500	8.0	6.0	200	10	20	25	NNP or NP-D	
2N5547	N	71	0.1	4.5	50	0.5	8.0	1500	8.0	6.0	200	15	40	25	NNP or NP-D	
2N5902	N	78	0.005	4.5	40	0.03	0.5	70	0.5	3.0	0.2	5.0	10	1.0	NT	
2N5903	N	78	0.005	4.5	40	0.03	0.5	70	0.5	3.0	0.2	5.0	20	1.0	NT	
2N5904	N	78	0.005	4.5	40	0.03	0.5	70	0.5	3.0	0.2	15	40	1.0	NT	
2N5905	N	78	0.002	4.5	40	0.03	0.5	70	0.5	3.0	0.1	5.0	10	1.0	NT	
2N5906	N	78	0.002	4.5	40	0.03	0.5	70	0.5	3.0	0.1	5.0	20	1.0	NT	
2N5907	N	78	0.002	4.5	40	0.03	0.5	70	0.5	3.0	0.1	10	40	1.0	NT	
2N5908	N	78	0.002	4.5	40	0.03	0.5	70	0.5	3.0	0.1	15	80	1.0	NT	
2N5909	N	78	0.002	4.5	40	0.03	0.5	70	0.5	3.0	0.1	15	80	1.0	NT	
U401	N	71	0.025	2.5	50	0.5	10	2000		8.0	20	5.0	10	2.0	NNR	
U402	N	71	0.025	2.5	50	0.5	10	2000		8.0	20	10	25	2.0	NNR	
U403	N	71	0.025	2.5	50	0.5	10	2000		8.0	20	15	40	2.0	NNR	
U404	N	71	0.025	2.5	50	0.5	10	2000		8.0	20	20	80	2.0	NNR	
U405	N	71	0.025	2.5	50	0.5	10	2000		8.0	20	25	80	2.0	NNR	
U406	N	71	0.025	2.5	50	0.5	10	2000		8.0	20	30	80	2.0	NNR	
2N5515	N	71	0.25	4.0	40	0.5	7.5	1000		25	30	5.0	5.0	1.0	NS	LOW NOISE
2N5516	N	71	0.25	4.0	40	0.5	7.5	1000		25	30	5.0	10	1.0	NS	
2N5517	N	71	0.25	4.0	40	0.5	7.5	1000		25	30	10	20	1.0	NS	
2N5518	N	71	0.25	4.0	40	0.5	7.5	1000		25	30	15	40	1.0	NS	
2N5519	N	71	0.25	4.0	40	0.5	7.5	1000		25	30	15	80	1.0	NS	
2N5520	N	71	0.25	4.0	40	0.5	7.5	1000		25	15	5.0	5.0	1.0	NS	
2N5521	N	71	0.25	4.0	40	0.5	7.5	1000		25	15	5.0	10	1.0	NS	
2N5522	N	71	0.25	4.0	40	0.5	7.5	1000		25	15	10	20	1.0	NS	
2N5523	N	71	0.25	4.0	40	0.5	7.5	1000		25	15	15	40	1.0	NS	
2N5524	N	71	0.25	4.0	40	0.5	7.5	1000		25	15	25	80	1.0	NS	
U402	N	71	0.025	2.5	50	0.5	10	2000		8.0	20	5.0	10	2.0	NNR	
U403	N	71	0.025	2.5	50	0.5	10	2000		8.0	20	10	25	2.0	NNR	

© 1979 Siliconix incorporated

Product Specifications (cont'd)

Siliconix

N-Channel Dual JFETs

PART NUMBER	N or P	PACKAGE (TO-)	LEAKAGE (nA, MAX.) Gate	THRESHOLD VOLTAGE (V, MAX.)	BREAKDOWN VOLTAGE (V, MIN.)	SATURATION CURRENT (mA) Min.	SATURATION CURRENT (mA) Max.	TRANS-CONDUCTANCE gfs (umhos) Min.	TRANS-CONDUCTANCE gfs (umhos) Max.	INPUT CAPACITANCE (pF, MAX.)	NOISE VOLTAGE (nV/√Hz, MAX.) or (NF, dB, MAX.)	THRESHOLD Static Match (mV, Max.)	THRESHOLD Temp Tracking µV/°C	OUTPUT CONDUCTANCE gos (µmhos, MAX.)	GEOMETRY (Section 5)	DEVICE
2N3921	N	71	1.0	3.0	50	1.0	10	1500			18	2.0	5.0	10	35	NNR or NRL-D	GENERAL PURPOSE
2N3922	N	71	1.0	3.0	50	1.0	10	1500			18	2.0	5.0	25	35	NNR or NRL-D	
2N394	N	71	0.1	4.5	50	0.5	5.0	1000			4.0	0.5	5.0	10	35	NFA	
2N394A	N	71	0.1	4.5	50	0.5	5.0	1000			4.0	0.5	5.0	20	35	NFA	
2N395	N	71	0.1	4.5	50	0.5	5.0	1000			4.0	0.5	10	25	35	NFA	
2N395A	N	71	0.1	4.5	50	0.5	5.0	1000			4.0	0.5	15	35	35	NFA	
2N396	N	71	0.1	4.5	50	0.5	5.0	1000			4.0	0.5	15	50	35	NFA	
2N3957	N	71	0.1	4.5	50	0.5	5.0	1000			4.0	0.5	20	75	35	NFA	
2N3958	N	71	0.1	4.5	50	0.5	5.0	1000			4.0	0.5	25	100	35	NFA	
2N4084	N	71	1.0	3.0	50	1.0	10	1500			18	2	15	10	35	NNR or NRL-D	
2N4085	N	71	1.0	3.0	50	1.0	10	1500			18	2	15	25	35	NNR or NRL-D	
2N5045	N	71	0.25	4.5	50	0.5	8.0	1500			8.0	200	5.0	67	25	NNR or NRL-D	
2N5046	N	71	0.25	4.5	50	0.5	8.0	1500			8.0	200	10	133	25	NNR or NRL-D	
2N5047	N	71	0.25	4.5	50	0.5	8.0	1500			8.0	200	15	200	25	NNR or NRL-D	
2N5452	N	71	0.1	4.5	50	0.5	5.0	1000			4.0	20	5.0	5.0	1.0	NFA	
2N5453	N	71	0.1	4.5	50	0.5	5.0	1000			4.0	20	10	10	1.0	NFA	
2N5454	N	71	0.1	4.5	50	0.5	5.0	1000			4.0	20	15	25	1.0	NFA	
U231	N	71	0.1	4.5	50	0.5	5.0	1000			6.0	80	5.0	10	35	NNP or NP-D	
U232	N	71	0.1	4.5	50	0.5	5.0	1000			6.0	80	10	25	35	NNP or NP-D	
U233	N	71	0.1	4.5	50	0.5	5.0	1000			6.0	80	15	50	35	NNP or NP-D	
U234	N	71	0.1	4.5	50	0.5	5.0	1000			6.0	80	20	75	35	NNP or NP-D	
U235	N	71	0.1	4.5	50	0.5	5.0	1000			6.0	80	25	100	35	NNP or NP-D	
U410	N	71	0.2	3.5	40	0.5	6.0	1000			6.0	13	10	10	20	NOP	
U411	N	71	0.2	3.5	40	0.5	6.0	1000			6.0	13	20	25	20	NOP	
U412	N	71	0.2	3.5	40	0.5	6.0	1000			6.0	13	40	80	20	NOP	
2N404	N	71	0.025	2.5	50	0.5	10	2000			8.0	20	5.0	25	2.0	NNR	LOW NOISE
U405	N	71	0.025	2.5	50	0.5	10	2000			8.0	20	40	80	2.0	NNR	
U406	N	71	0.025	2.5	50	0.5	10	2000			8.0	20	80	200	2.0	NNR	
2N5564	N	71	0.1	3.0	40	5.0	30	7500			12	5.0	10	45	45	NC	RF AMPLIFIER
2N5565	N	71	0.1	3.0	40	5.0	30	7500			12	10	25	50	45	NC	
2N5911	N	78	0.1	5.0	25	7.0	40	5000			3.0	20	10	20	100	NZF	
2N5912	N	78	0.1	5.0	25	7.0	40	5000			3.0	20	15	40	100	NZF	
U257	N	78	0.1	5.0	25	5.0	40	5000			3.0	30	100	150	150	NZF	
U430	N	99	0.15	4.0	25	12	30	10000			7.5	12	-	-	150	NZA	
U431	N	99	0.15	6.0	25	24	60	10000			7.5	10	-	-	150	NZA	
U440	N	71	0.50	6.0	25	6.0	30	4500			-	-	10	-	200	NZF	
U441	N	71	0.50	6.0	25	6.0	30	4500			-	-	20	-	200	NZF	
2N3921	N	71	1.0	3.0	50	1.0	10	1500			-	-	5.0	10	35	NNR or NRL-D	LOW NOISE
2N3922	N	71	1.0	3.0	50	1.0	10	1500			-	-	5.0	25	35	NNR or NRL-D	
2N394	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	5.0	10	35	NFA	
2N394A	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	5.0	20	35	NFA	
2N395	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	5.0	25	35	NFA	
2N395A	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	5.0	35	35	NFA	
2N396	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	5.0	50	35	NFA	
2N3957	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	5.0	75	35	NFA	
2N3958	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	5.0	100	35	NFA	
2N4084	N	71	1.0	3.0	50	1.0	10	1500			-	-	5.0	10	35	NNR or NRL-D	
2N4085	N	71	1.0	3.0	50	1.0	10	1500			-	-	5.0	25	35	NNR or NRL-D	
2N5045	N	71	0.25	4.5	50	0.5	8.0	1500			-	-	5.0	67	25	NNR or NRL-D	
2N5046	N	71	0.25	4.5	50	0.5	8.0	1500			-	-	10	133	25	NNR or NRL-D	
2N5047	N	71	0.25	4.5	50	0.5	8.0	1500			-	-	15	200	25	NNR or NRL-D	
2N5452	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	5.0	5.0	1.0	NFA	
2N5453	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	10	10	1.0	NFA	
2N5454	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	15	25	1.0	NFA	
U231	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	5.0	10	35	NNP or NP-D	
U232	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	10	25	35	NNP or NP-D	
U233	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	15	50	35	NNP or NP-D	
U234	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	20	75	35	NNP or NP-D	
U235	N	71	0.1	4.5	50	0.5	5.0	1000			-	-	25	100	35	NNP or NP-D	
U410	N	71	0.2	3.5	40	0.5	6.0	1000			-	-	10	10	20	NOP	
U411	N	71	0.2	3.5	40	0.5	6.0	1000			-	-	20	25	20	NOP	
U412	N	71	0.2	3.5	40	0.5	6.0	1000			-	-	40	80	20	NOP	

© 1979 Siliconix incorporated

Low Leakage Diodes

Part Number	Package (TO-)	Diode	Reverse Current (pA, Max.)	Breakdown Voltage (Volts)		Forward Voltage Drop (pF, Max.)	Capacitance
				Min.	Max.		
DPAD1	72	Dual	1	45	120	1.5	0.8
DPAD2	72	Dual	2	45	120	1.5	0.8
DPAD5	72	Dual	5	45	120	1.5	0.8
DPAD10	72	Dual	10	35	–	1.5	2.0
DPAD20	72	Dual	20	35	–	1.5	2.0
DPAD50	72	Dual	50	35	–	1.5	2.0
DPAD100	72	Dual	100	35	–	1.5	2.0
JPAD50	TO-92/TO-106	Single	20	35	–	1.5	2.0
JPAD100	TO-92/TO-106	Single	50	35	–	1.5	2.0
JPAD200	TO-92/TO-106	Single	100	35	–	1.5	2.0
JPAD500	TO-92/TO-106	Single	500	35	–	1.5	2.0
PAD1	18	Single	1	45	120	1.5	0.8
PAD2	18	Single	2	45	120	1.5	0.8
PAD5	18	Single	5	45	120	1.5	0.8
PAD10	18	Single	10	35	–	1.5	2.0
PAD20	18	Single	20	35	–	1.5	2.0
PAD50	18	Single	50	35	–	1.5	2.0
PAD100	18	Single	100	35	–	1.5	2.0

Voltage Controlled Resistors

Part Number	N or P	Package (TO-)	Breakdown Voltage (Volts, Min.)	Threshold Voltage (Volts)		Resistance (Channel Ω)		Geometry
				Min.	Max.	Min.	Max.	
VCR2N	N	18	15	3.5	7.0	20	60	NC
VCR3P	P	72	15	3.5	7.0	70	200	PE
VCR4N	N	18	15	3.5	7.0	200	600	NP
VCR5P	P	72	15	3.5	7.0	300	900	PC
VCR7N	N	72	15	2.5	5.0	4000	8000	NT

P-Channel MOSFETS

Part Number	Package (TO-)	Operating Mode	Threshold Voltage (Volts, Max.)	Resistance Channel (Ω, Max.)	Leakage Channel On (mA)		Leakage Channel Off (nA, Max.)	Breakdown Voltage (Volts, Max.)	Input Capacitance (pF, Max.)	Reverse Capacitance (pF, Max.)	Geometry
					Min.	Max.					
3N163	72	ENH	5.0	250	5.0	30	–	40	2.5	0.7	MRA
3N164	72	ENH	5.0	300	3.0	30	–	30	2.5	0.7	MRA
MFE823	18	ENH	6.0	–	3.0	–	20	25	6.0	1.5	MRA

© 1979 Siliconix incorporated

Current Regulator Diodes

Part Number	Package (TO-)	Forward Current (mA)	Forward Current Tolerance (%)	Limiting Voltage (Volts, Max.)	Peak Operating Voltage (Volts, Max.)	Dynamic Impedance (MΩ, Max.)	Forward Capacitance (pF, typ)	Geometry
CR022	18	0.22	10	1.00	100	13	–	NKL
CR024	18	0.24	10	1.00	100	10	–	NKL
CR027	18	0.27	10	1.00	100	9.0	–	NKL
CR030	18	0.30	10	1.00	100	8.0	–	NKL
CR033	18	0.33	10	1.00	100	6.6	–	NKL
CR039	18	0.39	10	1.05	100	4.1	–	NKL
CR043	18	0.43	10	1.05	100	3.3	–	NKL
CR047	18	0.47	10	1.10	100	2.7	–	NKL
CR056	18	0.56	10	1.20	100	1.9	–	NKL
CR062	18	0.62	10	1.30	100	1.55	–	NKL
CR068	18	0.68	10	1.15	100	1.35	–	NKM
CR075	18	0.75	10	1.20	100	1.15	–	NKM
CR082	18	0.82	10	1.25	100	1.00	–	NKM
CR091	18	0.91	10	1.29	100	0.88	–	NKM
CR100	18	1.00	10	1.35	100	0.80	–	NKM
CR110	18	1.10	10	1.40	100	0.70	–	NKM
CR120	18	1.20	10	1.45	100	0.64	–	NKM
CR130	18	1.30	10	1.50	100	0.58	–	NKM
CR140	18	1.40	10	1.55	100	0.54	–	NKM
CR150	18	1.50	10	1.60	100	0.51	–	NKM
CR160	18	1.60	10	1.65	100	0.475	–	NKO
CR180	18	1.80	10	1.75	100	0.42	–	NKO
CR200	18	2.00	10	1.85	100	0.395	–	NKO
CR220	18	2.20	10	1.95	100	0.37	–	NKO
CR240	18	2.40	10	2.00	100	0.345	–	NKO
CR270	18	2.70	10	2.15	100	0.32	–	NKO
CR300	18	3.00	10	2.25	100	0.30	–	NKO
CR330	18	3.30	10	2.35	100	0.28	–	NKO
CR360	18	3.60	10	2.50	100	0.265	–	NKO
CR390	18	3.90	10	2.60	100	0.255	–	NKO
CR430	18	4.30	10	2.75	100	0.245	–	NKO
CR470	18	4.70	10	2.90	100	0.235	–	NKO
J500	92	0.24	20	1.20	50	5.0	2	NCL
J501	92	0.33	20	1.30	50	3.0	2	NCL
J502	92	0.43	20	1.50	50	2.0	2	NCL
J503	92	0.56	20	1.70	50	1.4	2	NCL
J504	92	0.75	20	1.90	50	1.0	2	NCL
J505	92	1.00	20	2.10	50	0.6	2	NCL
J506	92	1.40	20	2.50	50	0.4	2	NCL
J507	92	1.80	20	2.80	50	0.25	2	NCL
J508	92	2.40	20	3.10	50	0.25	2	NCL
J509	92	3.00	20	3.50	50	0.20	2	NCL
J510	92	3.60	20	3.90	50	0.20	2	NCL
J511	92	4.70	20	4.20	50	0.15	2	NCL

© 1979 Siliconix incorporated

Product Specifications

Siliconix

VMOS Power FETs

$R_{DS(on)}$	BREAKDOWN VOLTAGE										PACKAGE
	35 V		40 V		60 V		80 V		90 V		
	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	
0.4						VN64GA					
1.8	2N6656	VN33AJ									
2.5	VN35AA	VN35AJ									
3.0					2N6657	VN66AJ					
3.5					VN67AA	VN67AJ					
4.0									2N6658	VN98AJ	
4.5							VN89AA			VN99AJ	
5.0	VN30AA								VN90AA		TO-3
1.8	2N6659	VN33AK									
2.5	VN35AB	VN35AK									
3.0					2N6660	VN66AK					
3.5					VN67AB	VN67AK					
4.0									2N6661	VN98AK	
4.5							VN89AB			VN99AK	
5.0	VN30AB								VN90AB		TO-39
3.0			VN46AF		VN66AF						
3.5					VN67AF						
4.0							VN88AF				
4.5							VN89AF				
5.0			VN40AF								TO-202AA
5.0					VN10KM						TO-237
3.0						VMP4					380-SOE

Detailed Technical Specifications for the VMOS Power FETs listed above *are not* included in this data book.

Please contact your nearest Siliconix Sales Office for a VMOS Design Catalog.

© 1979 Siliconix Incorporated

Die Process Information

Siliconix

Siliconix is a large volume supplier of die to the hybrid industry. Both military and industrial grades are available. Screening includes 100% DC electrical probe and 100% visual inspection of each die.

Physical Data

- Physical layout and dimensions are presented in the die topography section.
- Each die is passivated with approximately 8,000 angstroms of non-crystalline glass.
- All die are gold backed. Gold backing is approximately 1,500 angstroms thick.
- Die metallization is deposited aluminum approximately 12,000 angstroms thick.

Die Screening Criteria

Electrical Probe – Die are 100% probed in wafer form at 25°C to DC criteria.

Visual Criteria – Die are supplied with 100% visual sort to the criteria of MIL-Std-750 method 2072.

Packaging

Die are supplied in dust proof, anti-static waffle packs. (see illustration)

Assembly

- Chips supplied in waffle packs normally do not require cleaning. Wafers should be cleaned after sawing or scribing, and fracturing.
- Chips should be handled with a vacuum pick-up with protected tip or with tweezers gripping the chip on its sides.
- When handling MOSFET chips, particularly non-gate protected types, steps must be taken to prevent damage by static discharge. In some extreme cases, handling precautions may be necessary for junction FET chips.
- Chips can be die attached either eutectically or by conductive epoxy when lower temperatures are necessary. Gold silicon eutectic occurs at temperatures between 385°C and 425°C.
- Bonding of wires from chip pads to posts can be achieved by thermocompression gold wire or ultrasonic aluminum wire bonded.

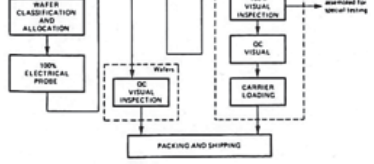
Options

- **SEM** – Scanning electron microscope examination and control in accordance with MIL-Std-883 Method 2018 can be ordered on chips and wafers.
- **Wafer qualification to unprobed parameters** – sample testing of purchased chips to demonstrate capability to perform at data sheet temperature extremes by use of LTPD techniques can be provided.
- **Hot probe** – Siliconix has a chip processor/distributor with hot probe capability available.

Chip Packaging

Chips are packaged as individual die in the flat waffle carrier illustrated in Figure 1. The carrier has a cavity size adequate to allow ease of loading/unloading and also prevents die from rotating within the cavity.

Chip and Wafer Processing



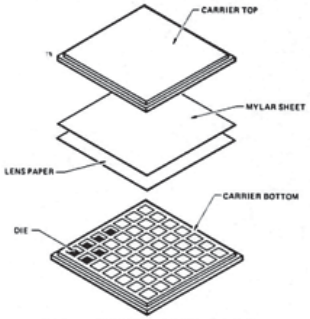


Figure 1

© 1979 Siliconix Incorporated

pc board layout and construction for low leakage applications

Siliconix

In order to realize the full capability of these devices in circuits that are sensitive to very low currents, considerable care should be exercised in PC board layout and construction techniques. If proper care is not taken, board leakage currents can easily become much larger than the leakage currents of the devices themselves, especially under conditions of high temperature and humidity. Excessive leakage currents can be produced by poor quality boards, socket leakage, poor board layout, imperfectly cleaned boards, or improperly applied or cured protective coatings.

It is important to start with quality PC boards which have high resistivity and low susceptance to moisture. Boards of teflon or polycarbonate composition exhibit these attributes and are preferred. Glass-epoxy boards are less desirable because they will absorb moisture, and if used must be protected with a conformal coating.

The use of sockets should be avoided wherever possible since the pin-to-pin isolation is often not great enough to prevent small leakage currents from occurring. These currents can significantly degrade device performance in low leakage applications. If sockets cannot be avoided use the highest quality available, preferably teflon.

In laying out PC boards, care should be taken to keep pins and runs which are sensitive to very low currents away from pins and runs which will be at significantly higher or lower voltages. The most common leakage current problems occur between pins sensitive to low current levels and nearby pins at or near one of the supply voltages. Thus, if the isolation between critical pins and nearby high or low voltage pins is increased, leakage is minimized.

In order to reduce leakage currents, it is very important that all PC boards and experimental breadboards be thoroughly cleaned with a solvent after construction. A recommended procedure is to wash each board in an ultrasonic cleaning bath of alcohol, trichloroethylene, or some other commercial solvent, and to blow dry with compressed air. The purpose of this is to remove all skin oils (the greatest cause of leakage in improperly cleaned boards), solder fluxes, and other films and residues left over from the construction process which can cause gross leakage problems and erratic device behavior, especially at temperatures above 85°C.

For best results, the thoroughly cleaned boards should be protected against dirt, conductive films, and humidity by the application of a conformal coating. Urethane and Dow Corning's R-4-3117 Silicone are easy to use and offer sufficient protection under most operating conditions. Epoxy results in a more durable coating but care must be taken to insure that it is cured properly; an improperly cured layer of epoxy will make the high temperature leakage problem worse. Union Carbide's Parylene also results in a relatively durable coating.

The ultimate leakage protection method consists of printed circuit metalization guard rings driven from a low impedance buffer amplifier whose output is at the same potential as the pin being protected. This completely eliminates board surface leakage at critical pins by removing any difference in potential, but it is difficult to implement due to the extra buffer amplifier required and the tight PC board metalization spacings encountered.

© 1979 Siliconix incorporated

data sheets metal

index 3

p-channel JFETs *designed for . . .*

Siliconix

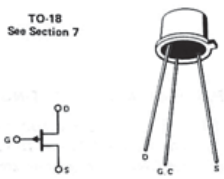
Performance Curves PC PD
See Section 5

■ General Purpose Amplifiers

BENEFITS

- JAN Approved Version Available

TO-18
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain and Gate-Source Voltage (Note 3).....30 V
Gate Current, Forward Biased (Note 1)..... 50 mA
Total Device Dissipation (Derate 2 mW/°C) ..... 300 mW
Storage Temperature Range .....–65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N2608 Min	2N2608 Max	2N2609 Min	2N2609 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		10		30	nA	V_{GS} = 30 V, V_{DS} = 0 V	
2	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		10		30	µA	V_{GS} = 5 V, V_{DS} = 0, T_A = 150°C	
3	STATIC	BV_{GSS}	Gate Source Breakdown Voltage	30		30		V	I_G = 1 µA, V_{DS} = 0 V	
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	1	4	1	4	V	V_{DS} = -5 V, I_D = 1 µA	
5	STATIC	I_{DSS}	Saturation Drain Current	-0.90	-4.50	-2	-10	mA	V_{DS} = -5 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000		2500		µmho	V_{DS} = -5 V, V_{GS} = 0 V	f = 1 kHz
7	DYNAMIC	C_{iss}	Common-Source Input Capacitance		17		30	pF	V_{DS} = -5 V, V_{GS} = 1 V	f = 140 kHz
8	DYNAMIC	NF	Noise Figure		3		3	dB	V_{DS} = -5 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz

*JEDEC Registered Data

PC PD

NOTES:
1. Not JEDEC Registered
2. I_{GSS} is JEDEC Registered at V_{GS} = 5 V
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged

© 1979 Siliconix Incorporated

p-channel JFETs *designed for . . .*

Siliconix

Performance Curves PC PD
See Section 5

- **Small-Signal Amplifiers**

BENEFITS
- Low Supply Voltage Operation
  $V_{GS(off)}$ Typically 1.2 V

TO-18
See Section 7





***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain and Gate-Source Voltage (Note 3) . . . . . 30 V
Gate Current, Forward Biased (Note 1) . . . . . 50 mA
Total Device Dissipation (Derate 2mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N2843 Min	2N2843 Max	2N2844 Min	2N2844 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		10		30	nA	V_{GS} = 30 V, V_{DS} = 0	
2			(Note 2)		10		30	µA	V_{GS} = 5 V, V_{DS} = 0, T_A = 150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	I_G = 1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		1.7		1.7	V	V_{DS} = -5 V, I_D = -1 µA	
5		I_{DSS}	Saturation Drain Current	-200	-1000	-440	-2200	µA	V_{DS} = -5 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	540		1400		µmho	V_{DS} = -5 V, V_{GS} = 0	f = 1 kHz
7		C_{iss}	Common-Source Capacitance		17		30	pF	V_{DS} = -5 V, V_{GS} = 1 V	f = 140 kHz
8		NF	Noise Figure		3		3	dB	V_{DS} = -5 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz
				PC		PD				

*JEDEC Registered Data

NOTES:
1. Not JEDEC Registered
2. I_{GSS} is JEDEC Registered at V_{GS} = 5 V.
3. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

© 1979 Siliconix Incorporated

p-channel JFETs *designed for . . .*

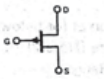
Siliconix

Performance Curves PC
See Section 5

- **Small-Signal Amplifiers**
- **Analog Multipliers**
- **Modulators**

BENEFITS
- Ease of Amplifier Design
  I_{DSS} & G_{fs} Closely Specified

TO-72
See Section 7





***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain and Gate-Source Voltage (Note 1) . . . . . 20 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or below)
25°C Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 230°C

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N3329 Min	2N3329 Max	2N3330 Min	2N3330 Max	2N3331 Min	2N3331 Max	2N3332 Min	2N3332 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		0.01		0.01		0.01		0.01	µA	V_{GS} = 10 V, V_{DS} = 0	
2					10		10		10		10		V_{GS} = 10 V, V_{DS} = 0, T_A = 150°C	
3		BV_{GSS}	Gate-Source Breakdown Voltage	20		20		20		20		V	I_G = 10 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		5		6		8		6		V_{DS} = -15 V, I_D = -10 µA	
5		I_{DSS}	Saturation Drain Current	-1	-3	-2	-6	-5	-15	-1	-6	mA	V_{DS} = -10 V, V_{GS} = 0	
6		$r_{DS(on)}$	Drain-Source ON Resistance		1000		800		600			Ω	I_D = -100 µA, V_{GS} = 0	
7	DYNAMIC	g_{is}	Common-Source Input Conductance		0.2		0.2		0.2		0.2	µmho	V_{DS} = -10 V, 2N3329: I_D = -1 mA, 2N3330: I_D = -2 mA, 2N3331: I_D = -5 mA, 2N3332: I_D = -1 mA	f = 1 kHz
8		g_{rs}	Common-Source Reverse Transfer Conductance		0.1		0.1		0.1		0.1			
9		g_{os}	Common-Source Output Conductance		20		40		100		20			
10		g_{fs}	Common-Source Forward Transconductance	1000	2000	1500	3000	2000	4000	1000	2200			
11				900		1350		1800		900				f = 10MHz
12		C_{iss}	Common-Source Input Capacitance		20		20		20		20	pF	V_{DS} = -10 V, V_{GS} = 1 V	f = 1 MHz
13		NF	Noise Figure		3		3		4		1	dB	V_{DS} = -5 V, I_D = -1 mA, R_{gen} = 1 MΩ	f = 1 kHz
14		NF	Noise Figure								5		V_{DS} = -5 V, I_D = -1 mA, R_{gen} = 10 MΩ	f = 10 Hz

*JEDEC registered data PC

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2.0 mW/°C

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NP
See Section 5

- **Small-Signal Low Power Applications**

TO-18
See Section 7





***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) . . . . –40 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . –65 to +175°C
Maximum Operating Temperature . . . . . 150°C

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N3368 Min	2N3368 Max	2N3369 Min	2N3369 Max	2N3370 Min	2N3370 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-5		-5	nA	V_{GS} = -30 V, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current		-1.5		-1.5		-1.5	µA	V_{GS} = -30 V, V_{DS} = 0	100°C
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 µA, V_{DS} = 0	
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage		-11.5		-6.5		-3.2	V	V_{DS} = 20 V, I_D = 1 µA	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current		5 (-12.0)		5 (-7.0)		5 (-3.5)	nA (V)	V_{DS} = 20 V, V_{GS} = ( )	
6	STATIC	I_{DSS}	Saturation Drain Current	2.0	12.0	0.5	2.5	0.1	0.6	mA	V_{DS} = 30 V (Note 3), V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	4000	600	2500	300	2500	µmho	V_{DS} = 30 V (Note 3), V_{GS} = 0	f = 1 kHz
8	DYNAMIC	g_{oss}	Common-Source Output Conductance		80		30		15	µmho	V_{DS} = 30 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{oss}	Common-Source Output Capacitance		3		3		3	pF	V_{DS} = 30 V, V_{GS} = 0	f = 1 MHz
10	DYNAMIC	C_{iss}	Common-Source Input Capacitance		20		20		20	pF	V_{DS} = 8 V, V_{GS} = 0	f = 1 MHz

NP

*JEDEC registered data.

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 150°C free-air temperature at rate of 2.1 mW/°C.
3. To minimize heating on high I_{DSS} units, this parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

© 1979 Siliconix Incorporated

p-channel JFETs *designed for . . .*

Siliconix

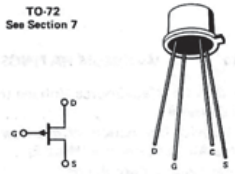
Performance Curves PE
See Section 5

- **Analog Switches**
- **Choppers**
- **Commutators**
- **Amplifiers**

BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 150\ \Omega$ (2N3386)

TO-72
See Section 7



***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain Voltage (Note 1) . . . . . 30 V
Gate-Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . 50 mA
Storage Temperature Range . . . . . -65 to +200°C
Total Dissipation at 25°C T_A (Note 2) . . . . . 300 mW

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N3382 Min	2N3382 Max	2N3384 Min	2N3384 Max	2N3386 Min	2N3386 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		15		15		15	nA	V_{GS} = 30 V, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current		15		15		15	µA	V_{GS} = 5 V, V_{DS} = 0	T_A = 150°C
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 µA, V_{DS} = 0	
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage (Note 3)	1.0	5.0	4.0	5.0	4.0	9.5	V	V_{DS} = -5 V, I_D = -1 µA	
5	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	-3.0	-30.0	-15.0	-30.0	-15.0	-50.0	mA	V_{DS} = -10 V, V_{GS} = 0	
6	STATIC	$I_{D(off)}$	Drain Cutoff Current		-2 (6)		-2 (6)		-2.5 (10)	nA (V)	V_{DS} = -5 V, V_{GS} = ( )	
7	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance		300		180		150	Ω	V_{GS} = 0, V_{DS} = 0	f = 1 kHz
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	4500	12,500	7500	12,500	7500	15,000	µmho	V_{DS} = -10 V, V_{GS} = 0	f = 1 kHz
9	DYNAMIC	C_{gs} + C_{dgs}	Source-Gate Capacitance Plus Drain-Gate Capacitance		6.0		6.0		6.0	pF	V_{DS} = 0, V_{GS} = 10 V	f = 140 kHz
10	DYNAMIC	C_{iss}	Common-Source Input Capacitance	16 Typ						pF	V_{DS} = -5 V, V_{GS} = 1 V	f = 140 kHz

PE

*JEDEC registered data.

NOTE:
1. Due to symmetrical geometry, units may be operated with source and drain leads interchanged.
2. Derate linearly to +175°C at 2 mW/°C
3. Pulsewidth = 2 ms, duty cycle ≤ 3%.

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

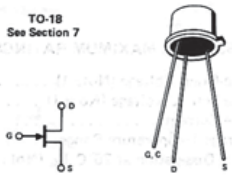
Performance Curves NP
See Section 5

- **Small-Signal Amplifiers**
- **Switches**

BENEFITS

- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

TO-18
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... –50 V
Gate Current ..... 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) ..... 300 mW
Storage Temperature Range ..... –65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3436 Min	2N3436 Max	2N3437 Min	2N3437 Max	2N3438 Min	2N3438 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–0.5		–0.5		–0.5	nA	V_{GS} = –30 V, V_{DS} = 0	
2					–1.0		–1.0		–1.0	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–50		–50		–50		V	I_G = –1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		1.0 (–10.0)		1.0 (–5.0)		1.0 (–2.5)	nA (V)	V_{DS} = 20 V, V_{GS} = ( )	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–9.8		–4.8		–2.3	V	V_{DS} = 20 V, I_D = 1 μA	
6		I_{DSS}	Saturation Drain Current	3.0	15.0	0.8	4.0	0.2	1.0	mA	V_{DS} = 20 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2500	10,000	1500	6000	800	4500	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8		g_{oss}	Common-Source Output Conductance		35		20		5		V_{DS} = 30 V, V_{GS} = 0	f = 1 MHz
9		C_{oss}	Common-Source Output Capacitance		6		6		6	pF		
10		C_{iss}	Common-Source Input Capacitance		18 (10)		18 (6)		18 (4)	pF (V)	V_{GS} = 0 V, V_{DS} = ( )	
11		NF	Noise Figure		2		2		2	dB	V_{DS} = 10 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 6 Hz	f = 1 kHz

*JEDEC Registered Data.

NP

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 200°C free-air temperature at rate of 1.7 mW/°C.

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

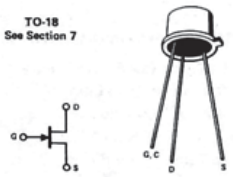
Performance Curves NP
See Section 5

- **Small-Signal Low Noise Amplifiers**

BENEFITS

- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

TO-18
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... –50 V
Gate Current ..... 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) ..... 300 mW
Storage Temperature Range ..... –65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3458 Min	2N3458 Max	2N3459 Min	2N3459 Max	2N3460 Min	2N3460 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–0.25		–0.25		–0.25	nA	V_{GS} = –30 V, V_{DS} = 0	
2					–0.5		–0.5		–0.5	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–50		–50		–50		V	I_G = –1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		1 (–8)		1 (–4)		1 (–2)	nA (V)	V_{DS} = 20 V, V_{GS} = ( )	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–7.8		–3.4		–1.8	V	V_{DS} = 20 V, I_D = 1 μA	
6		I_{DSS}	Drain Current at Zero Gate Voltage	3.0	15.0	0.8	4.0	0.2	1.0	mA	V_{DS} = 20 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2500	10,000	1500	6000	800	4500	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8		g_{oss}	Common-Source Output Conductance		35		20		5		V_{DS} = 30 V, V_{GS} = 0	f = 1 MHz
9		C_{oss}	Common-Source Output Capacitance		5		5		5	pF		
10		C_{iss}	Common-Source Input Capacitance		18 (10)		18 (6)		18 (4)	pF (V)	V_{GS} = 0 V, V_{DS} = ( ),	f = 1 MHz
11		NF	Noise Figure		6		4		4	dB	V_{DS} = 10 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 6 Hz	f = 20 Hz

* JEDEC registered data.

NP

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 200°C free-air temperature at rate of 1.7 mW/°C.

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

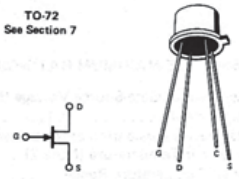
Performance Curves NFA
See Section 5

- **Low Noise Amplifiers**
- **Choppers**
- **Switches**

BENEFITS

- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

TO-72
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 2)	−50 V
Gate Current or Drain Current	50 mA
Total Device Dissipation (Derate 2 mW/°C to 175°C)	350 mW
Storage Temperature Range	−65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3684 Min	2N3684 Max	2N3685 Min	2N3685 Max	2N3686 Min	2N3686 Max	2N3687 Min	2N3687 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−0.1		−0.1		−0.1		−0.1	nA	V_{GS} = −30 V, V_{DS} = 0	
2					−0.5		−0.5		−0.5		−0.5	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		−50		V	I_G = −1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−2	−5	−1	−3.5	−0.6	−2	−0.3	−1.2		V_{DS} = 20 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current	2.5	7.5	1	3	0.4	1.2	0.1	0.5	mA	V_{DS} = 20 V, V_{GS} = 0	
6		$r_{DS(on)}$	Drain-Source ON Resistance (Note 1)		600		800		1200		2400	ohm	V_{DS} = 0 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	3000	1500	2500	1000	2000	500	1500	µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		50		25		10		5			
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2	pF		
10		C_{iss}	Common-Source Input Capacitance		4		4		4		4			
11		$\bar{e}_n$	Equivalent Short Circuit Input Spot Noise Voltage		0.15		0.15		0.15		0.15	$\frac{\mu V}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	f = 20 Hz
12		NF	Noise Figure		0.5		0.5		0.5		0.5	dB	V_{DS} = 10 V, V_{GS} = 0, R_{gen} = 10 meg, BW = 6 Hz	f = 100 Hz

*JEDEC registered data

NFA

NOTES:
1. Not JEDEC registered data
2. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NRL
See Section 5

- **Small-Signal Amplifiers**
- **Oscillators**

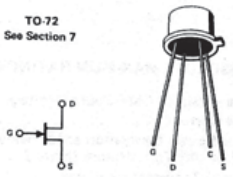
BENEFITS

- Operates from High Supply Voltages
  $BV_{GSS} > 50$ V

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1)	−50 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature (Note 2)	300 mW
Storage Temperature Range	−65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-72
See Section 7



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N3821 Min	2N3821 Max	2N3822 Min	2N3822 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−0.1		−0.1	nA	V_{GS} = −30 V, V_{DS} = 0	
2					−0.1		−0.1	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		V	I_G = −1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4		−6		V_{DS} = 15 V, I_D = 0.5 nA	
5		V_{GS}	Gate-Source Voltage	−0.5	−2				V_{DS} = 15 V, I_D = 50 µA	
						−1	−4		V_{DS} = 15 V, I_D = 200 µA	
6		I_{DSS}	Saturation Drain Current (Note 3)	0.5	2.5	2	10	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1500	4500	3000	6500	µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	1500		3000				f = 100 MHz
9		g_{os}	Common-Source Output Conductance (Note 3)		10		20			f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		6		6	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3			
12		NF	Noise Figure		5		5	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 5 Hz	f = 10 Hz
13		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		200		200	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0, BW = 5 Hz	

*JEDEC Registered Data.

NRL

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

© 1979 Siliconix Incorporated

n-channel JFET
designed for . . .

Siliconix

Performance Curves NRL
See Section 5

- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

BENEFITS

- Low Noise
  NF < 2.5 dB @ 100 MHz

TO-72
See Section 7





*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -30 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature (1/16" From Case for 10 Sec) . . . 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.5	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-0.5	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-8		V_{DS} = 15 V, I_D = 0.5 nA	
5		V_{GS}	Gate-Source Voltage	-1.0	-7.5		V_{DS} = 15 V, I_D = 400 µA	
6		I_{DSS}	Saturation Drain Current	4	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 3)	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	3,500	6,500	µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz (Note 3)
8		$\|y_{fs}\|$	Common-Source Forward Transadmittance	3,200				f = 200 MHz
9		g_{os}	Common-Source Output Conductance		35			f = 1 kHz (Note 3)
10		g_{iss}	Common-Source Input Conductance		800			f = 200 MHz
11		g_{oss}	Common-Source Output Conductance		200			
12		C_{iss}	Common-Source Input Capacitance		6	pF		f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		NF	Noise Figure		2.5	dB	V_{DS} = 15 V, V_{GS} = 0 R_G = 1 kΩ	f = 100 MHz

NRL

*JEDEC Registered Data

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

© 1979 Siliconix Incorporated

n-channel JFET
designed for . . .

Siliconix

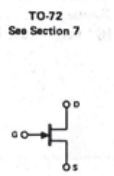
Performance Curves NRL
See Section 5

- **High Speed Commutators**
- **Choppers**

BENEFITS

- Low Insertion Loss
  $r_{ds(on)}$ < 250 Ω
- High Off-Isolation
  $I_{D(off)}$ < 0.1 nA

TO-72
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . -50 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.1	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 µA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		0.1	nA	V_{DS} = 15 V, V_{GS} = -8 V	
					0.1	µA		150°C
5	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance		250	Ω	V_{GS} = 0 V, I_D = 0	f = 1 kHz
6		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
7		C_{rss}	Common-Source Reverse Transfer Capacitance		3		V_{GS} = -8 V, V_{DS} = 0	

*JEDEC registered data.

NRL

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.

© 1979 Siliconix Incorporated

p-channel JFET
designed for . . .

Siliconix

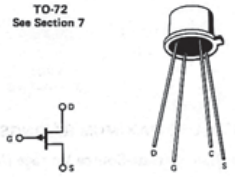
Performance Curves PC
See Section 5

- **General Purpose Amplifiers**

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) ..... 20 V
Drain-Source Voltage ..... -20 V
Gate Current ..... 10 mA
Total Device Dissipation at (or below)
25°C Free-Air Temperature (Note 2) ..... 300 mW
Storage Temperature Range ..... -65 to +200°C
Lead Temperature 1/16" From Case For 10 Sec .... 300°C

TO-72
See Section 7



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N3909 Min	2N3909 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		10	nA	V_{GS} = 10 V, V_{DS} = 0	
2					1	µA		T = 100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	20		V	I_G = 10 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		8.0		V_{DS} = -10 V, I_D = -10 µA	
5		V_{GS}	Gate-Source Voltage	0.3	7.9		V_{DS} = -10 V, I_D = -30 µA	
6		I_{DSS}	Saturation Drain Current	-0.3	-15	mA	V_{DS} = -10 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000	5,000	µmho		f = 1 kHz
8		g_{os}	Common-Source Output Conductance		100			
9		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	900				f = 10 MHz
10		C_{iss}	Common-Source Input Capacitance		32	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		16			

PC

*JEDEC registered data

Notes
1 Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2 Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.

Siliconix

© 1979 Siliconix Incorporated

monolithic dual n-channel JFETs
designed for . . .

Siliconix

Performance Curves NNR
See Section 5

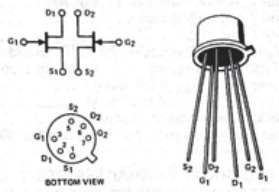
- **Differential Amplifiers**

BENEFITS
- Minimum System Error and Calibration
  5 mV Offset Maximum (2N3921)
- Simplifies Amplifier Design
  Low Output Conductance

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage ..... -50 V
Gate Current ..... 50 mA
Total Device Dissipation
(Derate 1.7 mW/°C to 200°C) ..... 300 mW
Storage Temperature Range ..... -65 to +200°C

TO-71
See Section 7



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-1	µA		100°C
3		BV_{DGO}	Drain-Gate Breakdown Voltage	50			I_D = 1 µA, I_S = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-3	V	V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-2.7		V_{DS} = 10 V, I_D = 100 µA	
6		I_G	Gate Operating Current		-250	pA	V_{DG} = 10 V, I_D = 700 µA	
7					-25	nA		100°C
8		I_{DSS}	Saturation Drain Current (Note 1)	1	10	mA	V_{DS} = 10 V, V_{GS} = 0	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	7500	µmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		35			
11		C_{iss}	Common-Source Input Capacitance		18	pF		
12		C_{rss}	Common-Source Reverse Transfer Capacitance		6			
13		g_{fs}	Common-Source Forward Transconductance	1500		µmho	V_{DG} = 10 V, I_D = 700 µA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		20			
15		NF	Spot Noise Figure		2	dB	V_{DS} = 10 V, V_{GS} 0	f = 1 kHz, R_G = 1 meg

		Characteristic		2N3921 Min	2N3921 Max	2N3922 Min	2N3922 Max	2N4084 Min	2N4084 Max	2N4085 Min	2N4085 Max	Unit	Test Conditions	
16	MATCH	$\lvert V_{GS1}-V_{GS2} \rvert$	Differential Gate-Source Voltage		5		5		15		15	mV	V_{DG} = 10 V, I_D = 700 µA	
17		$\frac{\Delta\lvert V_{GS1}-V_{GS2} \rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		10		25		10		25	µV/°C		T_A = 0°C T_B = 100°C
18		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 3)	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	–		f = 1 kHz

*JEDEC registered data.

NOTES:
1. Pulse test duration = 2 ms.
2. Measured at end points, T_A and T_B.
3. Assumes smaller value in numerator.

NNR
NRL-D

© 1979 Siliconix Incorporated

matched dual n-channel JFETs *designed for . . .*

- **Low and Medium Frequency Differential Amplifiers**
- **High Input Impedance Amplifiers**

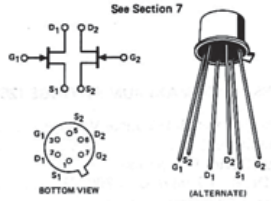
Siliconix

Performance Curves NFA See Section 5

BENEFITS

- High Accuracy & Stability
  Offset Less Than 5 mV (2N3954, 54A)
  Drift Less Than 5 μV/°C (2N3954A)
- Wide Dynamic Range
  I_G Specified @ V_{DS} = 20 V
- Low Capacitance
  $C_{iss} < 4$ pF

TO-71
See Section 7



***ABSOLUTE MAXIMUM RATINGS (25°C)**

Any Case-To-Lead Voltage	±100 V
Gate-Drain or Gate-Source Voltage	-50 V
Gate-To-Gate Voltage	±100 V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	-65 to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N3954 Min	2N3954 Max	2N3954A Min	2N3954A Max	2N3955 Min	2N3955 Max	2N3955A Min	2N3955A Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-500		-500		-500		-500	nA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	V_{DS} = 0, I_G = -1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		2.0		V_{DS} = 0, I_G = 1 mA	
6		V_{GS}	Gate-Source Voltage		-4.2		-4.2		-4.2		-4.2		V_{DS} = 20 V	I_D = 50 μA
7				-0.5	-4.0	-0.5	-4.0	-0.5	-4.0	-0.5	-4.0			I_D = 200 μA
8		I_G	Gate Operating Current		-50		-50		-50		-50	pA	V_{DS} = 20 V, I_D = 200 μA	
9					-250		-250		-250		-250	nA		T_A = 125°C
10		I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
11	DYNAMIC	$\|y_{fs}\|$	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
12				1000		1000		1000		1000				f = 200 MHz
13		g_{os}	Common-Source Output Conductance		35		35		35		35			f = 1 kHz
14		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0		4.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2			
16		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
17		NF	Common Source Spot Noise Figure		0.5		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz
18	MATCHING	$\|I_{G1}-I_{G2}\|$	Differential Gate Current		10		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA,	T = 125°C
19		I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 1)	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	–	V_{DS} = 20 V V_{GS} = 0	
20		$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage		5.0		5.0		10.0		5.0	mV	V_{DS} = 20 V, I_D = 200 μA	
21		$\Delta\|V_{GS1}-V_{GS2}\|$	Gate-Source Differential Voltage Change with Temperature		0.8		0.4		2.0		1.2			T = 25°C to -55°C
22					1.0		0.5		2.5		1.5			T = 25°C to 125°C
23		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	–		f = 1 kHz

*JEDEC registered data

NOTE:
1. Assumes smaller value in numerator.

NFA

© 1979 Siliconix Incorporated

matched dual n-channel JFETs *designed for . . .*

- **Low and Medium Frequency Differential Amplifiers**
- **High Input Impedance Amplifiers**

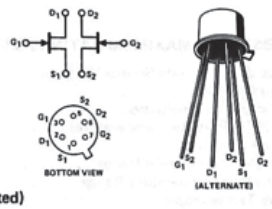
Siliconix

Performance Curves NFA See Section 5

BENEFITS

- Wide Dynamic Range
  I_G Specified @ V_{DS} = 20 V
- Low Capacitance
  $C_{iss} < 4$ pF

TO-71
See Section 7



***ABSOLUTE MAXIMUM RATINGS (25°C)**

Any Lead-To-Case Voltage	±100 V
Gate-Drain or Gate-Source Voltage	-50 V
Gate-To-Gate Voltage	±100 V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	-65 to +250°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N3956 Min	2N3956 Max	2N3957 Min	2N3957 Max	2N3958 Min	2N3958 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-500		-500		-500	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0 V, I_G = -1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0	-4.5	-1.0	-4.5	-1.0	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		V_{DS} = 0 V, I_G = 1 mA	
6		V_{GS}	Gate-Source Voltage		-4.2		-4.2		-4.2		V_{DS} = 20 V, I_D = 50 μA	
7				-0.5	-4.0	-0.5	-4.0	-0.5	-4.0		V_{DS} = 20 V, I_D = 200 μA	
8		I_G	Gate Operating Current		-50		-50		-50	pA	V_{DS} = 20 V, I_D = 200 μA	
9					-250		-250		-250	nA		T_A = 125°C
10		I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
11	DYNAMIC	$\|y_{fs}\|$	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
12				1000		1000		1000				f = 200 MHz
13		g_{os}	Common-Source Output Conductance		35		35		35			f = 1 kHz
14		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
16		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
17		NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0 V, R_G = 10 MΩ	f = 100 Hz
18	MATCHING	$\|I_{G1}-I_{G2}\|$	Differential Gate Reverse Current		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA	T = 125°C
19		I_{DSS1}/I_{DSS2}	Saturation Drain Current Ratio (Note 1)	0.95	1.0	0.90	1.0	0.85	1.0	–	V_{DS} = 20 V, V_{GS} = 0	
20		$\|V_{GS1}-V_{GS2}\|$	Differential Gate-Source Voltage		15		20		25	mV	V_{DS} = 20 V, I_D = 200 μA	
21		$\Delta\|V_{GS1}-V_{GS2}\|$	Gate-Source Voltage Differential Change With Temperature		4.0		6.0		8.0			T = 25°C to -55°C
22					5.0		7.5		10.0			T = 25°C to 125°C
23		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.95	1.0	0.90	1.0	0.85	1.0	–		f = 1 kHz

*JEDEC registered data

NOTE:
1. Assumes smaller value in numerator.

NFA

© 1979 Siliconix Incorporated

n-channel JFET
designed for . . .

- **Analog Switches**
- **Choppers**
- **Commutators**

Siliconix

Performance Curves NH
See Section 5

BENEFITS

- Low Insertion Loss, No Offset Voltage
  $R_{DS(on)} < 220\ \Omega$
- Short Switching Aperture Times
  $C_{rss} < 1.5$ pF
  $t_{(on)} + t_{(off)} < 50$ ns Typical

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . −30 V
Gate Current . . . . . 10 mA
Total Device Dissipation
(25°C Free-Air Temperature) . . . . . 300 mW
Power Derating . . . . . 1.7 mW/°C
Storage Temperature Range . . . . . −55 to +200°C
Operating Temperature Range . . . . . −55 to +175°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-72
See Section 7



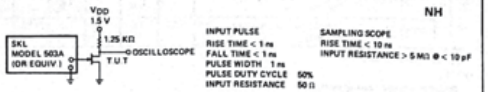
***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1		I_{GSS}	Gate Reverse Current			-0.1	nA	$V_{GS} = -20$ V, $V_{DS} = 0$	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4		-6.0	V	$V_{DS} = 10$ V, $I_D = 10$ nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30				$I_G = -1\ \mu$A, $V_{DS} = 0$	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 1)	2.0			mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
5		$I_{D(off)}$	Drain Cutoff Current			1.0	nA	$V_{DS} = 10$ V, $V_{GS} = -7$ V	
6						2.0	μA		$T_A = 150°C$
7		$r_{DS(on)}$	Static Drain-Source ON Resistance			220	Ω	$V_{DS} = \leq 0.1$ V, $V_{GS} = 0$	
8		$V_{DS(on)}$	Drain-Source ON Voltage			0.25	V	$I_D = 1$ mA, $V_{GS} = 0$	
9		I_{DGO}	Drain Reverse Current			0.1	nA	$V_{DG} = 20$ V, $I_S = 0$	
10						0.2	μA		$T_A = 150°C$
11	DYN	$r_{ds(on)}$	Drain-Source ON Resistance			220	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
12		C_{iss}	Common-Source Input Capacitance		3.1	6.0	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	1.5		$V_{DS} = 0$, $V_{GS} = -7$ V	
14	SWITCH	$t_{d(on)}$	Turn ON Delay Time		3.0	20	ns	$V_{DD} = 1.5$ V $I_{D(on)} = 1.0$ mA $V_{GS(on)} = 0$ $V_{GS(off)} = -6$ V $R_L = 1.25$k Ω	See Circuit Below
15		t_r	Rise Time		10.0	100			
16		t_{off}	Turn OFF Time		30.0	100			
17		$t_{d(off)}$	Turn OFF Delay Time (Note 2)		10.0				
18		t_f	Fall Time (Note 2)		20.0				

*JEDEC registered parameters unless otherwise noted (apply to min/max only).

NOTES:
1. Pulse test duration ≤ 2 ms.
2. Non-JEDEC registered parameters:
$t_{d(off)} + t_f = t_{off}$.

NH



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 ms
PULSE DUTY CYCLE 50%
INPUT RESISTANCE 50 Ω

SAMPLING SCOPE
RISE TIME < 10 ns
INPUT RESISTANCE > 5 MΩ @ < 10 pF

© 1979 Siliconix incorporated

n-channel JFETs
designed for . . .

- **Analog Switches**
- **Choppers**
- **Amplifiers**

Siliconix

Performance Curves NC
See Section 5

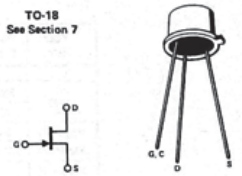
BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (2N3970)
- Good Off-Isolation
  $I_{D(off)} < 250$ pA

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Note 1) . . . . . 1.8 W
Storage Temperature Range . . . . . −65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 7



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N3970 Min	2N3970 Max	2N3971 Min	2N3971 Max	2N3972 Min	2N3972 Max	Unit	Test Conditions	
1		BV_{GSS}	Gate Reverse Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu$A, $V_{DS} = 0$	
2		I_{DGO}	Drain Reverse Current		250		250		250	pA	$V_{DG} = 20$ V, $I_S = 0$	
3					500		500		500	nA		150°C
4		$I_{D(off)}$	Drain Cutoff Current		250		250		250	pA	$V_{DS} = 20$ V, $V_{GS} = -12$ V	
5	STATIC				500		500		500	nA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3	V	$V_{DS} = 20$ V, $I_D = 1$ nA	
7		I_{DSS}	Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%)	50	150	25	75	5	30	mA	$V_{DS} = 20$ V, $V_{GS} = 0$	
8		$V_{DS(on)}$	Drain-Source ON Voltage						2	V	$V_{GS} = 0$	$I_D = 5$ mA
9							1.5					$I_D = 10$ mA
10					1							$I_D = 20$ mA
11		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 1$ mA	
12		$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13	DYN	C_{iss}	Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = 20$ V, $V_{GS} = 0$	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		6		6		6		$V_{DS} = 0$, $V_{GS} = -12$ V	
15	SW	$t_{d(on)}$	Turn-On Delay Time		10		15		40	ns	$V_{DD} = 10$ V, $V_{GS(on)} = 0$	
16		t_r	Rise Time		10		15		40		$I_{D(on)}$ R_L $V_{GS(off)}$	
17		t_{off}	Turn-Off Time		30		60		100		2N3970 20 mA 450 Ω -10 V 2N3971 10 mA 850 Ω -5 V 2N3972 5 mA 1.6KΩ -3 V	

*JEDEC registered data.

NOTE:
1. Derate linearly at the rate of 10 mW/°C.

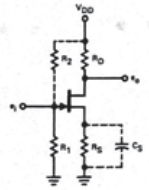
NC



© 1979 Siliconix incorporated

Siliconix

APPLICATIONS



Amplifier Design Chart
(C_S for 3 dB Point at 50 Hz)

V_{DD} (V)	R_S (Ω)	R_1 (MΩ)	R_2 (MΩ)	C_S (μF)	I_{DD} (mA)	R_D (Ω)	e_o Max (V)	A_V
2N3970								
30	560	1	∞	100	11	1K	3	9
	2.7K	3.3	10	100	6	1K	2.5	8
V_{DD} = 15 V_{SS} = -15	3K	1	Source Follower		7	0	8.5	0.96
	7.5K	1			6	0	8.5	0.96
V_{DD} = 15 V_{SS} = -15	7.5K	1	Source Follower		6	0	15	0.97
2N3971								
20	2K	4.7	11	100	5	1K	1.5	8-11
	330	1	∞	100	8	820	1.5	9
	330	1	∞	0	8	820	3	1.9
30	2K	4.7	11	100	6	2.7K	5	18-24
	330	1	∞	100	8	1.5K	2.5	15
	330	1	∞	0	8	1.5K	5.5	3.3
V_{DD} = 15 V_{SS} = -15	4.7K	1	Source Follower		5	0	11	0.97
2N3972								
10	220	1	∞	0	5	1.2K	1.5	3.5
20	220	1	∞	0	5	2.2K	3.5	7
30	1K	1	12	100	4	3.9K	5	38
	1K	1	12	100	4	5.6K	3.5	40-55
V_{DD} = 15 V_{SS} = -15	4.7K	1	Source Follower		2.5	0	13	0.98
	7.5K	1			1.5	0	13	0.98

© 1979 Siliconix Incorporated

n-channel JFETs
designed for . . .

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NC
See Section 5

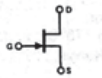
BENEFITS

- Low Insertion Loss
  High Accuracy in Test Systems
  $R_{ON} < 30\ \Omega$ (2N4091)
- High Off-Isolation
  $I_{D(off)} < 200$ pA
- High Speed
  $t_{rise} < 10$ ns (2N4091)
- Short Sample and Hold Aperture Time
  $C_{rss} < 5$ pF

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage . . . . . -40 V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . -55 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 7



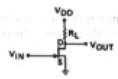


***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N4091 Min	2N4091 Max	2N4092 Min	2N4092 Max	2N4093 Min	2N4093 Max	Unit	Test Conditions		
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0		
2		I_{DGO}	Drain Reverse Current		200		200		200	pA	V_{GS} = -20 V, I_S = 0		
3					400		400		400	nA			150°C
4		$I_{D(off)}$	Drain Cutoff Current						200	pA	V_{DS} = 20 V	V_{GS} = - 6 V	
5									400	nA			150°C
6							200			pA		V_{GS} = - 8 V	
7							400			nA			150°C
8					200					pA		V_{GS} = -12 V	
9					400					nA			150°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5	-10	-2	-7	-1	-5	V	V_{DS} = 20 V, I_D = 1 nA		
11		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8		mA	V_{DS} = 20 V, V_{GS} = 0		
12		$V_{DS(on)}$	Drain-Source ON Voltage						0.2	V	V_{GS} = 0	I_D = 2.5 mA	
13							0.2					I_D = 4 mA	
14					0.2							I_D = 6.6 mA	
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	V_{GS} = 0, I_D = 1 mA		
16	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		50		80	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
17		C_{iss}	Common-Source Input Capacitance		16		16		16	pF	V_{DS} = 20 V, V_{GS} = 0		f = 1 MHz
18		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5		V_{DS} = 0, V_{GS} = -20 V		
19	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		20	ns	V_{DD} = 3 V, $V_{GS(on)}$ = 0		
20		t_r	Rise Time		10		20		40			$I_{D(on)}$	$V_{GS(off)}$	R_L
21		t_{off}	Turn-OFF Time		40		60		80		2N4091	6.6 mA	-12 V	425 Ω
											2N4092	4	-8	700
											2N4093	2.5	-6	1120

*JEDEC registered data.

NOTE:
1. Pulsewidth = 300 μs, duty cycle ≤ 3%.



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 μs
PULSE DUTY CYCLE < 10%
PULSE GENERATOR IMPEDANCE 50Ω

NC
SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.7 pF

© 1979 Siliconix Incorporated

n-channel JFETs designed for . . .

Siliconix

Performance Curves NT
See Section 5

- **Ultra-High Input Impedance Amplifiers**
  - **Electrometers**
  - **pH Meters**
  - **Smoke Detectors**

BENEFITS

- Low Power
  $I_{DSS} < 90\ \mu A$ (2N4117)
- Minimum Circuit Loading
  $I_{GSS} < 1$ pA (2N4117A Series)

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) ..... -40 V
Gate-Current ..... 50 mA
Total Device Dissipation
(Derate 2 mW/°C to 175°C) ..... 300 mW
Storage Temperature Range ..... -65 to +175°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 255°C

TO-72
See Section 7





***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N4117 2N4117A Min	2N4117 2N4117A Max	2N4118 2N4118A Min	2N4118 2N4118A Max	2N4119 2N4119A Min	2N4119 2N4119A Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current 2N4117 Series Only		-10		-10		-10	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-25		-25		-25	nA		150°C
3		I_{GSS}	Gate Reverse Current 2N4117A Series Only		-1		-1		-1	pA	V_{GS} = -20 V, V_{DS} = 0	
4					-2.5		-2.5		-2.5	nA		150°C
5		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 μA, V_{DS} = 0	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-1.8	-1	-3	-2	-6		V_{DS} = 10 V, I_D = 1 nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	0.03	0.09	0.08	0.24	0.20	0.60	mA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	70	210	80	250	100	330	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		3		5		10			
10		C_{iss}	Common-Source Input Capacitance		3		3		3	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5			

NT

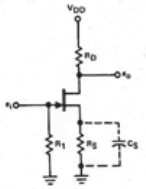
*JEDEC registered data.

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. This parameter is measured during a 2 ms interval 100 ms after power is applied. (Not a JEDEC condition.)

© 1979 Siliconix Incorporated

APPLICATIONS

Siliconix



Amplifier Design Chart

V_{DD} (V)	R_S (kΩ)	C_S	I_{DD} (μA)	R_D (kΩ)	e_o Max (pK V)	A_V
2N4117						
10	10		45	120	1	5.7
20	10		45	270	1.5	12
				360	1	15
30	10		45	420	4	17
				620	1	22
V_{DD} = +15 V_{SS} = -15	510	Source Follower	35	0	8	0.97
2N4118						
10	8.2		120	36	0.6	2.2
				50	0.2	3.5
20	8.2		120	120	1	7.5
30	8.2		120	180	2	10
V_{DD} = +15 V_{SS} = -15	510	Source Follower	35	0	8	0.97
2N4119						
20	56	5 μF* at 5 V	70	150	1	10
30	56		70	240	3	17
				330	1	17-23
20	6.8		300	27	1	1.8
30	6.8		300	68	2	4.5
V_{DD} = +15 V_{SS} = -15	510	Source Follower	40	0	10	0.97

*AC Amplifier

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NRL
See Section 5

- **Small-Signal Amplifiers**
- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

BENEFITS
- High Gain
- Low Receiver Noise Figure

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) ..... -30 V
Gate Current ..... 10 mA
Drain Current ..... 15 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) ..... 300 mW
Storage Temperature Range..... -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds)..... 300°C

TO-72
See Section 7





***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N4220, 2N4220A		2N4221, 2N4221A		2N4222, 2N4222A		Units	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2					-0.1		-0.1		-0.1	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -10 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		-8	V	V_{DS} = 15 V, I_D = 0.1 nA	
5		V_{GS}	Gate-Source Voltage	-0.5	-2.5	-1	-5	-2	-6	V	V_{DS} = 15 V, I_D = ( )	
				(50)	(50)	(200)	(200)	(500)	(500)	(µA)		
6		I_{DSS}	Saturation Drain Current (Note 3)	0.5	3	2	6	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1000	4000	2000	5000	2500	6000	µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	750		750		750				f = 100 MHz
9		g_{os}	Common-Source Output Conductance (Note 3)		10		20		40			f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		6		6		6	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2			
12		NF	Noise Figure, Only 2N4220A, 2N4221A, 2N4222A		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0 R_{gen} = 1 meg	f = 100 Hz

*JEDEC registered data. NRL

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

© 1979 Siliconix incorporated

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NRL
See Section 5

- **VHF Amplifiers**
- **Mixers**

BENEFITS
- Low Noise
  NF = 3 dB Typical @ 200 MHz
- Easy Tuning
  $C_{rss} < 2$ pF

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) ..... -30 V
Gate Current ..... 10 mA
Drain Current ..... 20 mA
Total Device Dissipation at (or below) 25°C
Free-Air Temperature (Note 2) ..... 300 mW
Storage Temperature Range..... -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds)..... 300°C

TO-72
See Section 7





***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N4223		2N4224		Unit	Test Conditions	
				Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.5	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-0.25		-0.5	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		V	I_G = -10 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.1	-8	-0.1	-8	V	V_{DS} = 15 V, I_D = ( )	
				(0.25)	(0.25)	(0.5)	(0.5)	(nA)		
5		V_{GS}	Gate-Source Voltage	-1.0	-7.0	-1.0	-7.5	V		
				(0.3)	(0.3)	(0.2)	(0.2)	(mA)		
6		I_{DSS}	Saturation Drain Current (Note 3)	3	18	2	20	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYN	g_{fs}	Common-Source Forward Transconductance (Note 3)	3000	7000	2000	7500	µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		C_{iss}	Common-Source Input Capacitance (Output Shorted)		6		6	pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		2		2			
10	HIGH FREQ	$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	2700		1700		µmho	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
11		g_{iss}	Common-Source Input Conductance (Output Shorted)		800		800			
12		g_{oss}	Common-Source Output Conductance (Input Shorted)		200		200			
13		G_{ps}	Small Signal Power Gain	10				dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 K	
14		NF	Noise Figure		5					

*JEDEC registered data. NRL

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

© 1979 Siliconix incorporated

n-channel JFETs *designed for . . .*

Siliconix

- **Small-Signal Amplifiers**
- **Choppers**
- **Voltage-Controlled Resistors**

Performance Curves NP
See Section 5

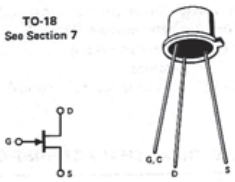
BENEFITS

- Low Noise
  NF < 1 dB at 1 kHz
- Operation from Low Power Supply Voltages
  $V_{GS(off)}$ < 1 V (2N4338)
- Simple Biasing Design with Tightly Specified Parameter Tolerances
  3:1 I_{DSS}, V_P, g_{fs} Ranges
- High Off-Isolation as a Switch
  $I_{D(off)}$ < 50 pA

*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... -50 V
Gate Current ..... 50 mA
Total Device Dissipation (Note 2) ..... 300 mW
Storage Temperature Range ..... -65 to +200°C
Maximum Operating Temperature ..... 175°C
Lead Temperature
(1/16" from case for 10 seconds) .....300°C

TO-18
See Section 7



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

		Characteristic		2N4338 Min	2N4338 Max	2N4339 Min	2N4339 Max	2N4340 Min	2N4340 Max	2N4341 Min	2N4341 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.1		-0.1		-0.1		-0.1	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-1	-0.6	-1.8	-1	-3	-2	-6		V_{DS} = 15 V, I_D = 0.1 µA	
5		$I_{D(off)}$	Drain Cutoff Current		0.05 (-5)		0.05 (-5)		0.05 (-5)		0.07 (-10)	nA (V)	V_{DS} = 15 V, V_{GS} = ( )	
6		I_{DSS}	Saturation Drain Current (Note 3)	0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	600	1800	800	2400	1300	3000	2000	4000	µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		5		15		30		60			
9		$r_{ds(on)}$	Drain-Source ON Resistance		2500		1700		1500		800	ohm	V_{DS} = 0, V_{GS} = 0	
10		C_{iss}	Common-Source Input Capacitance		7		7		7		7	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3		3			
12		NF	Noise Figure		1		1		1		1	dB	V_{DS} = 15 V, V_{GS} = 0 R_{gen} = 1 meg, BW = 200 Hz	f = 1 kHz

*JEDEC registered data

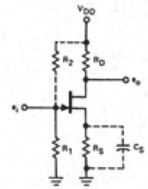
NP

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Derate linearly to 175°C free-air temperature at rate of 2 mW/°C.
3. These parameters are measured during a 2 msec interval 125 msec (I_{DSS}) and 625 msec (g_{fs}) after d-c power is applied. (Not a JEDEC condition.)

© 1979 Siliconix Incorporated

APPLICATIONS

Siliconix



Amplifier Design Chart

V_{DD} (V)	R_S (Ω)	R_1 (Ω)	R_2 (Ω)	C_S (µF)	I_{DD} (mA)	R_D (KΩ)	e_o Max (pk V)	A_V
2N4338								
15	1500	1M	∞	0	0.25	36	2.5	9-12
				30		36	1.5	16-24
						47	2.0	20-30
	5100	1M	∞	0	0.12	82	3.0	10-10.5
				25		82	1.5	24-37
	36K	1M	2M	30	0.15	27	1.0	13-18.5
30	1500	1M	∞	0	0.25	82	4.0	21.5-27
				30		82	2.5	32-49
						100	3.0	43-64
	5100	1M	∞	0	0.12	150	4.5	14.5-16
				25		150	2.5	38-54
						200	1.5	49-50
	36K	1M	5M	30	0.15	82	5.0	37-52
45	1500	1M	∞	0	0.25	120	6.5	27-33
				30		120	4.0	45-68
	5100	1M	∞	0	0.12	270	10	28-31
				25		270	5.0	76-105
	36K	1M	8.2M	0	0.15	120	14	2.8
				30		120	7.0	54-76
V_{DD} = +15 V_{SS} = -15	100K	1M	∞	0	0.15	0	9.0	0.98
2N4339								
15	1800	1M	∞	0	0.42	20	3.0	7-7.5
				40		20	2.0	17-22
						27	2.0	23-27
	9100	1M	6.8M	35	0.32	18	2.0	17-19
						30	2.5	26-28
	27K	1M	3M	25	0.2	22	1.0	16-18
						43	2.0	28-30
30	1800	1M	∞	0	0.42	47	6.5	15-17
				40		47	4.0	38-47
						51	4.5	40-50
	9100	1M	13M	0	0.32	43	8.0	4.5
				35		43	5.0	40-43
						68	4.5	53-60
	27K	1M	7.5M	25	0.2	68	4.0	49-52
						100	7.0	66-70
45	1800	1M	∞	0	0.42	75	7.5	23-25
				40		75	5.0	58-70
						100	7.0	73-77
	9100	1M	22M	0	0.32	68	7.0	7.0
				25		68	6.5	59-64
						120	7.0	80-85
	27K	1M	12M	0	0.2	100	12	3.3
				25		100	5.0	65-68
						180	8.0	100-115
V_{DD} = +15 V_{SS} = -15	75K	1M	∞	0	0.22	0	10	0.98

V_{DD} (V)	R_S (Ω)	R_1 (Ω)	R_2 (Ω)	C_S (µF)	I_{DD} (mA)	R_D (KΩ)	e_o Max (pk V)	A_V
2N4340								
15	680	1M	∞	0	1.5	5.1	3.0	3.5-4
				65		5.1	1.5	7-8.5
						6.8	2.0	9-10.5
	1200	1M	∞	0	1.1	7.5	2.5	3.5-4
				60		7.5	2.0	9-11
						10	2.0	11-13
	3900	1M	∞	0	0.4	18	4.0	3.5-4
				40		18	1.5	15-18
						22	1.0	19-22
30	680	1M	∞	0	1.5	12	6.0	9.5-10
				65		12	3.0	17-22
						18	1.0	24-26
	1200	1M	∞	0	1.1	18	6.0	9-9.5
				60		18	4.0	21-26
						24	2.0	29
	3900	1M	∞	0	0.4	39	7.0	7.5-8
				40		39	7.0	30-36
						62	0.5	34-45
	20K	1M	6.8M	35	0.35	30	3.0	25-27
						56	6.5	40
45	680	1M	∞	0	1.5	20	10.5	14-15.5
				65		20	8.0	27-32
						27	4.0	35
	1200	1M	∞	0	1.1	27	12.5	16-18
				60		27	5.0	30-37
						39	2.0	39-42
	3900	1M	∞	0	0.4	68	12	12-13
				40		68	7.0	52-61
						91	3.0	56-63
	20K	2M	3M	55	1.0	10	5.0	15
						20	4.0	27-28
V_{DD} = +15 V_{SS} = -15	22K	1M	∞	0	0.75	0	12	0.96
2N4341								
15	1000	1M	∞	70	2.7	2	1.0	3-3.5
						2.7	2.0	4-4.5
	1200	1.2M	7.5M	80	3.5	1.2	2.0	2.5
						2.2	3.0	3-4.5
	2000	1M	∞	65	1.8	3	2.0	4-4.5
						4.7	1.5	6-6.5
30	1000	1M	∞	0	2.7	6.2	7.0	4.0
				70		6.2	3.5	10
						9.1	1.5	11-13
	1200	1.1M	15M	80	3.5	3.9	4.0	7.5-8
	2000	1M	∞	0	1.8	9.1	6.0	3.0
				65		9.1	4.0	12
						15	1.0	13-19
	15K	1M	3.3M	60	0.7	18	3.0	16-21
45	1000	1M	∞	0	2.7	10	8.5	6.3
				70		10	6.0	16
	1200	1M	22M	80	3.5	6.8	7.0	13
	2000	1M	∞	0	1.8	15	8.5	5.5
				65		15	5.0	20-21
	15K	1M	5.6M	60	0.7	30	9.0	28-35
V_{DD} = +15 V_{SS} = -15	10K	1M	∞	0	1.9	0	13.5	0.94

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Siliconix

Performance Curves NC
See Section 5

BENEFITS

- Low Insertion Loss, High Accuracy in Test Systems $r_{ON} < 30\ \Omega$ (2N4391)
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- High Off-Isolation $I_{D(off)} < 100$ pA
- High Speed $t_{ON} < 20$ ns

TO-18
See Section 7



***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage . . . . . –40 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

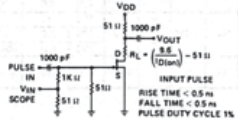
		Characteristic	2N4391 Min	2N4391 Max	2N4392 Min	2N4392 Max	2N4393 Min	2N4393 Max	Unit	Test Conditions	
1	STATIC	I_{GSS} Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -20 V, V_{DS} = 0	
2				-200		-200		-200	nA		150°C
3		BV_{GSS} Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 µA, V_{DS} = 0	
4		$I_{D(off)}$ Drain Cutoff Current						100	pA	V_{DS} = 20 V	V_{GS} = -5 V
5								200	nA		150°C
6						100			pA		V_{GS} = -7 V
7						200			nA		150°C
8				100					pA		V_{GS} = -12 V
9				200					nA		150°C
10		$V_{GS(f)}$ Gate-Source Forward Voltage		1		1		1	V	I_G = 1 mA, V_{DS} = 0	
11		$V_{GS(off)}$ Gate-Source Cutoff Voltage	-4	-10	-2	-5	-0.5	-3		V_{DS} = 20 V, I_D = 1 nA	
12		I_{DSS} Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0	
13		$V_{DS(on)}$ Drain Source ON Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA
14						0.4					I_D = 6 mA
15				0.4							I_D = 12 mA
16		$r_{DS(on)}$ Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA	
17		$r_{ds(on)}$ Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
18	DYN	C_{iss} Common-Source Input Capacitance		14		14		14	pF	V_{DS} = 20 V, V_{GS} = 0	
19		C_{rss} Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0	V_{GS} = -6 V
20						3.5					V_{GS} = -7 V
21				3.5							V_{GS} = -12 V
22	SW	$t_{d(on)}$ Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0	
23		t_r Rise Time		5		5		5			
24		$t_{d(off)}$ Turn-OFF Delay Time		20		35		50			
25		t_f Fall Time		15		20		30			

	$I_{D(on)}$	$V_{GS(off)}$	R_L
2N4391	12 mA	-12 V	800 Ω
2N4392	6	-7	1.6K Ω
2N4393	3	-5	3.2K Ω

NC

*JEDEC registered data.

NOTE:
1. Pulse test required, pulse width = 300 µs, duty cycle ≤ 3%.



© 1979 Siliconix incorporated

n-channel JFETs *designed for . . .*

- **VHF Amplifiers**
- **Mixers**

Siliconix

Performance Curves NH
See Section 5

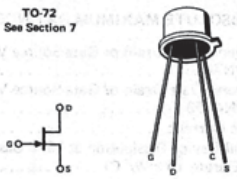
BENEFITS

- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Band
  High g_{fs}/C_{iss} Ratio

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage, 2N4416 . . . . . -30 V
Gate-Drain or Gate-Source Voltage, 2N4416A . . . . . -35 V
Gate Current . . . . . 10 mA
Total Device Dissipation (Derate 1.7 mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-72
See Section 7



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic	Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS} Gate Reverse Current		-0.1	nA	V_{GS} = -20 V, V_{DS} = 0 V	
2				-0.1	µA		150°C
3		BV_{GSS} Gate-Source Breakdown Voltage	-30		V	I_G = -1 µA, V_{DS} = 0 V	2N4416
			-35				2N4416A
4		$V_{GS(off)}$ Gate-Source Cutoff Voltage		-6	V	V_{DS} = 15 V, I_D = 1 nA	2N4416
			-2.5	-6			2N4416A
5		I_{DSS} Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs} Common-Source Forward Transconductance	4500	7500	µmho		f = 1 kHz
7		g_{os} Common-Source Output Conductance		50	µmho		
8		C_{rss} Common-Source Reverse Transfer Capacitance		0.8	pF		
9		C_{iss} Common-Source Input Capacitance		4	pF		f = 1 MHz
10		C_{oss} Common-Source Output Capacitance		2			

		Characteristic	100 MHz Min	100 MHz Max	400 MHz Min	400 MHz Max	Unit	Test Conditions
11	HIGH FREQUENCY	g_{iss} Common-Source Input Conductance		100		1000	µmho	V_{DS} = 15 V, V_{GS} = 0 V
12		b_{iss} Common-Source Input Susceptance		2500		10,000	µmho	
13		g_{oss} Common-Source Output Conductance		75		100	µmho	
14		b_{oss} Common-Source Output Susceptance		1000		4000	µmho	
15		g_{fs} Common-Source Forward Transconductance			4000		µmho	
16		G_{ps} Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
17		NF Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1K Ω

*JEDEC Registered data

NH

NOTES:
1. Pulse test duration = 300 µs.

© 1979 Siliconix incorporated

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NC
See Section 5

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

BENEFITS

- Low Insertion Loss and High Accuracy in Test Systems
  $r_{DS(on)} < 25\ \Omega$ (2N4856, 59)
- High Off-Isolation
  $I_{D(off)} < 250$ pA
- High Speed
  $t_{ON} < 9$ ns
- Fully Qualified
  JAN, JANTX and JANTXV Available

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage, 2N4856-58 ..... -40 V
Reverse Gate-Drain or Gate-Source Voltage, 2N4859-61 ..... -30 V
Gate Current ..... 50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C) ..... 1.8 W
Storage Temperature Range ..... -65 to +200°C
Lead Temperature (1/16" from case for 10 seconds) ..... 300°C

TO-18
See Section 7



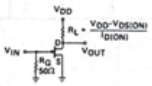
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4856 2N4859 Min	2N4856 2N4859 Max	2N4857 2N4860 Min	2N4857 2N4860 Max	2N4858 2N4861 Min	2N4858 2N4861 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	2N4856-58	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2			2N4859-61	-30		-30		-30				
3		I_{GSS} Gate Reverse Current	2N4856-58		-250		-250		-250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4					-500		-500		-500	nA		150°C
5			2N4859-61		-250		-250		-250	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
6					-500		-500		-500	nA		150°C
7		$I_{D(off)}$ Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
8					500		500		500	nA		150°C
9		$V_{GS(off)}$ Gate-Source Cutoff Voltage		-4	-10	-2	-6	-0.8	-4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
10		I_{DSS} Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		$V_{DS(on)}$ Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\ )$	
12	DYN	$r_{ds(on)}$ Drain-Source ON Resistance			25		40		60	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss} Common-Source Input Capacitance			18		18		18	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
14		C_{rss} Common-Source Reverse Transfer Capacitance			8		8		8			
15	SWITCHING	$t_{d(on)}$ Turn-ON Delay Time			6 (20) [-10]		6 (10) [-6]		10 (5) [-4]	ns (mA) [V]	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $I_{D(on)} = (\ )$, $V_{GS(off)} = [\ ]$	$R_L =$ 464 Ω, 2N4856, 59; 953 Ω, 2N4857, 60; 1910 Ω, 2N4858, 61
16		t_r Rise Time			3 (20) [-10]		4 (10) [-6]		10 (5) [-4]	ns (mA) [V]		
17		t_{off} Turn-OFF Time			25 (20) [-10]		50 (10) [-6]		100 (5) [-4]	ns (mA) [V]		

*JEDEC registered data.

NOTE:
1. Pulse test required, pulsewidth = 100 µs, duty cycle ≤ 10%.

NC



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pF

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NC
See Section 5

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

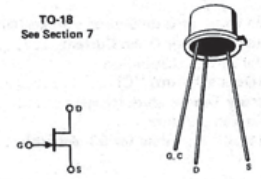
BENEFITS

- Low Insertion Loss and High Accuracy in Test Systems
  $r_{DS(on)} < 25\ \Omega$ (2N4856A, 59A)
- High Off-Isolation
  $I_{D(off)} < 250$ pA
- Short Sample and Hold Aperture Time
  $C_{rss} < 4$ pF
- High Speed
  $t_{ON} < 8$ ns

*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage, 2N4856A-58A. ..... -40 V
Reverse Gate-Drain or Gate-Source Voltage, 2N4859A-61A. ..... -30 V
Gate Current ..... 50 mA
Total Device Dissipation at 25°C Case Temperature (Derate 10 mW/°C) ..... 1.8 W
Storage Temperature Range ..... -65 to +200°C
Lead Temperature (1/16" from case for 10 seconds) ..... 300°C

TO-18
See Section 7



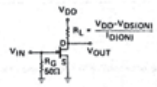
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N4856A 2N4859A Min	2N4856A 2N4859A Max	2N4857A 2N4860A Min	2N4857A 2N4860A Max	2N4858A 2N4861A Min	2N4858A 2N4861A Max	Unit	Test Conditions	
1	STATIC	BV_{GSS} Gate-Source Breakdown Voltage	2N4856A-58A	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
2			2N4859A-61A	-30		-30		-30				
3		I_{GSS} Gate Reverse Current	2N4856A-58A		-250		-250		-250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
4					-500		-500		-500	nA		150°C
5			2N4859A-61A		-250		-250		-250	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
6					-500		-500		-500	nA		150°C
7		$I_{D(off)}$ Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
8					500		500		500	nA		150°C
9		$V_{GS(off)}$ Gate-Source Cutoff Voltage		-4	-10	-2	-6	-0.8	-4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
10		I_{DSS} Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
11		$V_{DS(on)}$ Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\ )$	
12	DYN	$r_{ds(on)}$ Drain-Source ON Resistance			25		40		60	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
13		C_{iss} Common-Source Input Capacitance			10		10		10	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
14		C_{rss} Common-Source Reverse Transfer Capacitance			4		3.5		3.5			
15	SWITCHING	$t_{d(on)}$ Turn-ON Delay Time			5 (20) [-10]		6 (10) [-6]		8 (5) [-4]	ns (mA) [V]	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $I_{D(on)} = (\ )$, $V_{GS(off)} = [\ ]$	$R_L =$ 464 Ω, 2N4856A, 59A; 953 Ω, 2N4857A, 60A; 1910 Ω, 2N4858A, 61A
16		t_r Rise Time			3 (20) [-10]		4 (10) [-6]		8 (5) [-4]	ns (mA) [V]		
17		t_{off} Turn-OFF Time			20 (20) [-10]		40 (10) [-6]		80 (5) [-4]	ns (mA) [V]		

NC

*JEDEC registered data.

NOTE:
1. Pulse test required, pulsewidth = 100 µs, duty cycle ≤ 10%.



INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pF

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NS See Section 5

- **Audio and Sub-Audio Amplifiers**

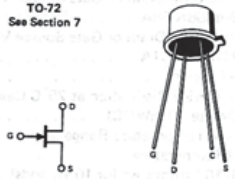
BENEFITS

- Ultra Low Noise
  $\overline{e_n}$ = 8 nV/√Hz Typical at 10 Hz
  $\overline{e_n}$ = 2 nV/√Hz Typical at 1 kHz

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . −40 V
Gate Current or Drain Current . . . . . 50 mA
Total Device Dissipation
(Derate 1.7 mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . . −65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-72
See Section 7



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N4867 2N4867A Min	2N4867 2N4867A Max	2N4868 2N4868A Min	2N4868 2N4868A Max	2N4869 2N4869A Min	2N4869 2N4869A Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0	
2					-0.25		-0.25		-0.25	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-2	-1	-3	-1.8	-5		V_{DS} = 20 V, I_D = 1 µA	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.4	1.2	1	3	2.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	700	2000	1000	3000	1300	4000	µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		1.5		4		10			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		25		25		25			
10		$\overline{e_n}$	Short Circuit Equivalent Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	2N4867 Series, f = 10 Hz
11					10		10		10			2N4867A Series, f = 10 Hz
12					10		10		10			2N4867 Series, f = 1 kHz
13					5		5		5			2N4867A Series, f = 1 kHz
14		NF	Spot Noise Figure		1		1		1	dB	V_{DS} = 10 V, V_{GS} = 0, R_{gen} = 20 K, 2N4867 Series; 5 K, 2N4867A Series	f = 1 kHz

*JEDEC registered data. NS

NOTES:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.
2. Pulse test duration = 2 ms.

© 1979 Siliconix Incorporated

p-channel JFETs *designed for . . .*

Siliconix

Performance Curves PS See Section 5

- **Analog Switches**
- **Commutators**
- **Choppers**

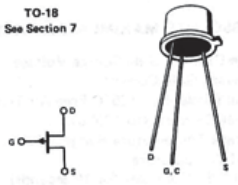
BENEFITS

- Low Insertion Loss
  $R_{DS(on)}$ < 75 Ω (2N5018)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage
(Note 1) . . . . . 30 V
Gate Current . . . . . 50 mA
Total Device Dissipation, Free-Air
(Derate 3 mW/°C) . . . . . 500 mW
Storage Temperature Range . . . . . −65 to +200°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 7

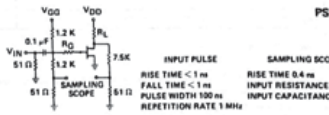


***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N5018 Min	2N5018 Max	2N5019 Min	2N5019 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	I_G = 1 µA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current		2		2	nA	V_{GS} = 15 V, V_{DS} = 0	
3		$I_{D(off)}$	Drain Cutoff Current		−10		−10		V_{DS} = −15 V, V_{GS} = 12 V (2N5018)	
4					−10		−10	µA	V_{GS} = 7 V (2N5019)	150°C
5		I_{DGO}	Drain Reverse Current		−2		−2	nA	V_{DG} = −15 V, I_S = 0	
6					−3		−3	µA		150°C
7		$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	V_{DS} = −15 V, I_D = −1 µA	
8		I_{DSS}	Saturation Drain Current	−10		−5		mA	V_{DS} = −20 V, V_{GS} = 0	
9		$V_{DS(on)}$	Drain-Source ON Voltage		−0.5		−0.5	V	V_{GS} = 0, I_D = −6 mA (2N5018), I_D = −3 mA (2N5019)	
10		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	I_D = −1 mA, V_{GS} = 0	
11		$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	I_D = 0, V_{GS} = 0	f = 1 kHz
12	DYN	C_{iss}	Common-Source Input Capacitance		45		45	pF	V_{DS} = −15 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		V_{DS} = 0, V_{GS} = 12 V (2N5018), V_{GS} = 7 V (2N5019)	
14	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	V_{DD} = −6 V, $V_{GS(on)}$ = 0	
15		t_r	Rise Time		20		75		$V_{GS(off)}$ / $I_{D(on)}$ / R_L: 2N5018: 12 V / −6 mA / 910 Ω; 2N5019: 7 V / −3 mA / 1.8K Ω	
16		$t_{d(off)}$	Turn-OFF Delay Time		15		25			
17		t_f	Fall Time		50		100			

*JEDEC registered data. PS

NOTE:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.



© 1979 Siliconix Incorporated

monolithic dual n-channel JFETs *designed for . . .*

Siliconix

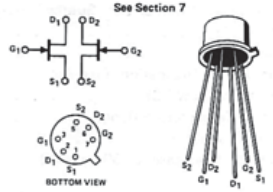
Performance Curves NNR
See Section 5

- **High Gain Differential Amplifiers**

BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5045)
- Low Drift
  5 mV Drift Maximum (2N5045)

TO-71
See Section 7



***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage	-50 V
Forward Gate Current	30 mA
Total Dissipation (25°C Free Air Temp.)	400 mW
Power Derating (to 175°C)	2.67 mW/°C
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic (Note 1)		2N5045 Min	2N5045 Max	2N5046 Min	2N5046 Max	2N5047 Min	2N5047 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	µA	V_{GS} = -50 V, V_{DS} = 0 V	
2					-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0 V	
3					-250		-250		-250			T = 150°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5	-0.5	-4.5	-0.5	-4.5	V	V_{DS} = 15 V, I_D = 0.5 nA	
5		I_{DSS}	Drain Saturation Current	0.5	8.0	0.5	8.0	0.5	8.0	mA		
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1.5	6.0	1.5	6.0	1.5	6.0	mmho	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
7		$\lvert y_{fs}\rvert$	Common-Source Forward Admittance	1.5		1.5		1.5				f = 100 MHz
8		g_{os}	Common-Source Output Conductance		25		25		25	µmho		f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0	pF		f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
11		NF	Spot Noise Figure		5.0		5.0			dB		f = 10 Hz, R_G = 1 MΩ
12		e_n	Equivalent Short-Circuit Input Noise Voltage		200		200			$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz
13	MATCHING	$\lvert I_{GSS1}-I_{GSS2}\rvert$	Differential Gate Current		10		10		10	nA	V_{GS} = -15 V, V_{DS} = 0 V	T_A = 100°C
14		I_{DSS1}/I_{DSS2}	Drain Current Ratio (Note 2)	0.95	1.0	0.9	1.0	0.8	1.0	—	V_{GS} = 0 V, V_{DS} = 15 V	
15		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DS} = 15 V	I_D = 50 µA
16					5		10		15			I_D = 200 µA
17		$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Voltage Differential Drift (Note 3)		5		10		15		V_{DS} = 15 V, I_D = 200 µA, T_A = 25°C	T_B = -25°C
18					5		10		15			T_B = 100°C
19		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 2)	0.95	1.0	0.9	1.0	0.8	1.0	—	V_{DS} = 15 V, I_D = 200 µA	f = 1 kHz
20		$\lvert g_{os1}-g_{os2}\rvert$	Diff. Output Conductance		1.0		2.0		3.0	µmho		

*JEDEC registered data.

NNR
NRL-D

NOTES:
1. Individual FET characteristics. The terminals of the FET not under test are open-circuited for these measurements..
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

© 1979 Siliconix Incorporated

p-channel JFETs *designed for . . .*

Siliconix

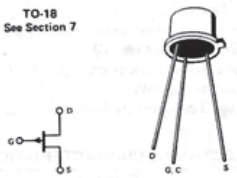
Performance Curves PS
See Section 5

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

BENEFITS

- Simplifies Series-Shunt Switching when Combined with 2N4393, its N-Channel Complement
- Low Insertion Loss in Switching Systems $R_{ON} < 75\ \Omega$ (2N5114)
- Short Sample and Hold Aperture Time $C_{rss} < 7$ pF
- High Off-Isolation $I_{D(off)} < 500$ pA

TO-18
See Section 7



***ABSOLUTE MAXIMUM RATINGS (25°C)**

Reverse Gate-Drain or Gate-Source Voltage (Note 1)	30 V
Gate Current	50 mA
Total Device Dissipation, Free-Air (Derate 3 mW/°C)	500 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

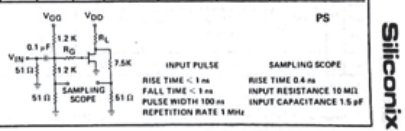
***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N5114 Min	2N5114 Max	2N5115 Min	2N5115 Max	2N5116 Min	2N5116 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 µA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current		500		500		500	pA	V_{GS} = 20 V, V_{DS} = 0	
3					1.0		1.0		1.0	µA		150°C
4		$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	V_{DS} = -15 V, V_{GS} = 12 V (2N5114) V_{GS} = 7 V (2N5115), V_{GS} = 5 V (2N5116)	
5					-1.0		-1.0		-1.0	µA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4	V	V_{DS} = -15 V, I_D = -1 nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	V_{GS} = 0, V_{DS} = -18 V (2N5114) V_{DS} = -15 V (2N5115, 2N5116)	
8		$V_{GS(f)}$	Forward Gate-Source Voltage		-1		-1		-1	V	I_G = -1 mA, V_{DS} = 0	
9		$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6		V_{GS} = 0, I_D = -15 mA (2N5114) I_D = -7 mA (2N5115), I_D = -3 mA (2N5116)	
10		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		100		150	Ω	V_{GS} = 0, I_D = -1 mA	
11		$r_{ds(on)}$	Drain-Source ON Resistance		75		100		150	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
12	DYN	C_{iss}	Common-Source Input Capacitance		25		25		25	pF	V_{DS} = -15, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7		V_{DS} = 0, V_{GS} = 12 V (2N5114) V_{GS} = 7 V (2N5115), V_{GS} = 5 V (2N5116)	
14	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		6		10		12	ns	V_{DD}	2N5114: -10 V; 2N5115: -6 V; 2N5116: -6 V
15		t_r	Rise Time		10		20		30		$V_{GS(off)}$	12 V; 7 V; 5 V
16		$t_{d(off)}$	Turn-OFF Delay Time		6		8		10		R_L	580 Ω; 743 Ω; 1800 Ω
17		t_f	Fall Time		15		30		50		$V_{GS(on)}$	0; 0; 0
											$I_{D(on)}$	-15 mA; -7 mA; -3 mA

*JEDEC registered data.

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse Test PW 300 µs, duty cycle < 3%.

PS



© 1979 Siliconix Incorporated

monolithic dual n-channel JFETs *designed for . . .*

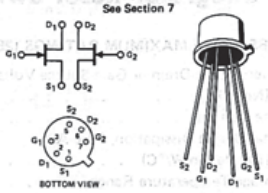
- **Differential Amplifiers**
- **FET Input Op Amps**

Siliconix

Performance Curves NNP
See Section 5

BENEFITS
- Minimum System Error and Calibration
  5 mV Maximum Offset (2N5196, 97)
- Low Drift
  5 μV/°C Maximum (2N5196)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	−50 V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 85°C	
(Derate 2.56 mW/°C)	250 mW
Total Device Dissipation, T_A = 85°C	
(Derate 4.3 mW/°C)	500 mW
Storage Temperature Range	−65 to +200°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-25	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-50	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-3.8			
6		I_G	Gate Operating Current		-15	pA	V_{DG} = 20 V, I_D = 200 μA	
					-15	nA		125°C
7		I_{DSS}	Saturation Drain Current	0.7	7	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	700	1600		V_{DG} = 20 V, I_D = 200 μA	
10		g_{os}	Common-Source Output Conductance		50		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance		4		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			f = 1 kHz
14		NF	Spot Noise Figure		0.5	dB		f = 100 Hz, R_G = 10 MΩ
15		$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 1 kHz

		Characteristic		2N5196 Min	2N5196 Max	2N5197 Min	2N5197 Max	2N5198 Min	2N5198 Max	2N5199 Min	2N5199 Max	Unit	Test Conditions	
16	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5		5	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	–	V_{DS} = 20 V, V_{GS} = 0 V	
18		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	–		f = 1 kHz
19		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
20		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		5		10		20		40	μV/°C	V_{DG} = 20 V, I_D = 200 μA	T_A = 25°C, T_B = 125°C
21					5		10		20		40			T_A = -55°C, T_B = 25°C
22		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		1		1		1		1	μmho		f = 1 kHz

*JEDEC registered data.

NNP
NP-D

NOTES:
1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

© 1979 Siliconix incorporated

n-channel JFETs *designed for . . .*

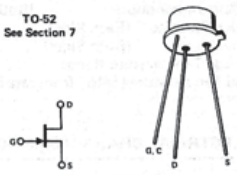
- **Low ON Resistance Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Capacitors**
- **Low Noise Audio Amplifiers**

Siliconix

Performance Curves NIP
See Section 5

BENEFITS
- Low Insertion Loss
  $R_{DS(on)}$ < 5 Ω (2N5432)
- Small Error in Measurement Systems
  $V_{DS(on)}$ < 50 mV (2N5432)
- High Off-Isolation
  $I_{D(off)}$ < 200 pA
- High Speed
  $t_{d(on)}$ < 4 ns
- Low Noise Audio-Frequency Amplification
  e_n < 2 nV/√Hz at 1 kHz Typical

TO-52
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage	−25 V
Gate Current	100 mA
Drain Current	400 mA
Total Device Dissipation at 25°C	
Free-Air Temperature (Note 1)	300 mW
Storage Temperature Range	−65 to +150°C
Lead Temperature	
(1/16" from case for 10 seconds)	300°C

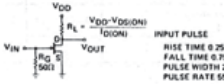
*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5432 Min	2N5432 Max	2N5433 Min	2N5433 Max	2N5434 Min	2N5434 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-200		-200		-200	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-200		-200		-200	nA		150°C
3		BV_{GSS}	Gate Source Breakdown Voltage	-25		-25		-25		V	I_G = -1 μA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	V_{DS} = 5 V, V_{GS} = -10 V	
5					200		200		200	nA		150°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-3	-9	-1	-4	V	V_{DS} = 5 V, I_D = 3 nA	
7		I_{DSS}	Saturation Drain Current (Note 2)	150		100		30		mA	V_{DS} = 15 V, V_{GS} = 0	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	V_{GS} = 0, I_D = 10 mA	
9		$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV		
10		$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
11	DYN	C_{iss}	Common-Source Input Capacitance		30		30		30	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		15		15		15			
13	SW	$t_{d(on)}$	Turn-ON Delay Time		4		4		4	ns	V_{DD} = 1.5 V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = -12 V, $I_{D(on)}$ = 10 mA, R_L = 145 Ω (2N5432), 143 Ω (2N5433), 140 Ω (2N5434)	
14		t_r	Rise Time		1		1		1			
15		$t_{d(off)}$	Turn-OFF Delay Time		6		6		6			
16		t_f	Fall Time		30		30		30			

*JEDEC registered data.

NIP

NOTES:
1. Derate linearly at the rate of 2.3 mW/°C.
2. Pulse test required pulsewidth 300 μs, duty cycle < 3%.



© 1979 Siliconix incorporated

matched dual n-channel JFETs *designed for . . .*

Siliconix

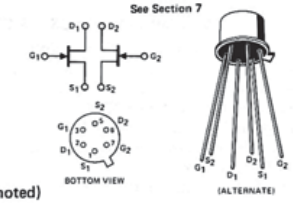
■ Low and Medium Frequency Differential Amplifiers

Performance Curves NFA See Section 5

BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5452)
- Simplifies Amplifier Design
  Output Conductance Less that 1 μmho

TO-71
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Any Lead–To–Case Voltage . . . . . ±100 V
Gate-Drain or Gate-Source Voltage . . . . . –50 V
Gate-To-Gate Voltage . . . . . ±100 V
Gate Current . . . . . 50 mA
Total Device Dissipation 85°C (Each Side) . . . . . 250 mW
Case Temperature (Both Sides) . . . . . 500 mW
Power Derating (Each Side) . . . . . 2.86 mW/°C
(Both Sides) . . . . . 4.3 mW/°C
Storage Temperature Range . . . . . –65 to +250°C
Lead Temperature (1/16" from case for 10 seconds) . . . 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5452 Min	2N5452 Max	2N5453 Min	2N5453 Max	2N5454 Min	2N5454 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0 V	
2					-200		-200		-200	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0 V, I_G = -1 μA	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-4.5	-1	-4.5	-1	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2		V_{DS} = 20 V, I_D = 50 μA	
6		$V_{GS(f)}$	Gate-Source Forward Voltage		2		2		2		V_{DS} = 0 V, I_G = 1 mA	
7		I_{DSS}	Drain Saturation Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0 V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
9				1000		1000		1000				f = 100 MHz
10		g_{os}	Common-Source Output Conductance		3.0		3.0		3.0		V_{DS} = 20 V, I_D = 200 μA	f = 1 kHz
11					1.0		1.0		1.0			
12		C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2			
14		C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0 V	
15		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
16		NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0 V, R_G = 10 MΩ	f = 100 Hz
17	MATCHING	I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio (Note 1)	0.95	1.0	0.95	1.0	0.95	1.0	–	V_{DS} = 20 V, V_{GS} = 0 V	
18		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		10.0		15.0	mV	V_{DS} = 20 V, I_D = 200 μA	
19		$\lvert\Delta V_{GS1}-V_{GS2}\rvert$	Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0			T = 25°C to -55°C
20					0.5		1.0		2.5			T = 25°C to +125°C
21		g_{fs1}/g_{fs2}	Transconductance Ratio (Note 1)	0.97	1.0	0.97	1.0	0.95	1.0	–		f = 1 kHz
22		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.25		0.25		0.25	μmhos		

*JEDEC registered data

NOTE:
1. Assumes smaller value in numerator.

NFA

© 1979 Siliconix incorporated

matched dual n-channel JFETs *designed for . . .*

Siliconix

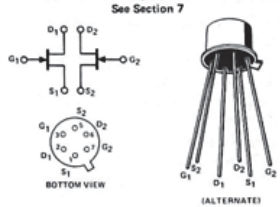
■ Differential Amplifiers

Performance Curves NS See Section 5

BENEFITS

- Ultra-Low Noise
  $\overline{e}_n$ = 8 nV/√Hz at 10 Hz (Typical)
  $\overline{e}_n$ = 2 nV/√Hz at 1 kHz (Typical)
- Minimum System Error and Calibration
  5 mV Offset Maximum
  CMRR > 100 dB

TO-71
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -40 V
Gate Current . . . . . 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 2.0 mW/°C) . . . . . 250 mW
Total Device Dissipation, T_A = 85°C
(Derate 3.0 mW/°C) . . . . . 375 mW
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 30 seconds) . . . . . .300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-250	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-250	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate Source Voltage	-0.2	-3.8			
6		I_G	Gate Operating Current		-100	pA	V_{DG} = 20 V, I_D = 200 μA	
					-100	nA		125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
9		g_{fs}	Common Source Forward Transconductance (Note 1)	500	1000		V_{DG} = 20 V, I_D = 200 μA	
10		g_{os}	Common-Source Output Conductance		10		V_{DS} = 20 V, V_{GS} = 0	
11		g_{os}	Common Source Output Conductance		1		V_{DG} = 20 V, I_D = 200 μA	
12		C_{iss}	Common Source Input Capacitance		25	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common Source Reverse Transfer Capacitance		5			
14		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		30 (2N5515-19)	$\frac{nV}{\sqrt{Hz}}$	V_{DG} = 20 V, I_D = 200 μA	f = 10 Hz
					15 (2N5520-24)			
					10 (2N5515-24)			f = 1 kHz

		Characteristic		2N5515,20 Min	2N5515,20 Max	2N5516,21 Min	2N5516,21 Max	2N5517,22 Min	2N5517,22 Max	2N5518,23 Min	2N5518,23 Max	2N5519,24 Min	2N5519,24 Max	Unit	Test Conditions	
15	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
16		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1	–	V_{DS} = 20 V, V_{GS} = 0	
17		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate Source Voltage		5		5		10		15		15	mV		
18		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate Source Voltage Differential Drift (Note 3)		5		10		20		40		80	μV/°C	V_{DG} = 20 V, I_D = 200 μA	T_A = 25°C, T_B = 125°C
					5		10		20		40		80			T_A = -55°C, T_B = 25°C
19		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.1		0.1		0.1		0.1		0.1	μmho		f = 1 kHz
20		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1	–		
21		CMRR	Common Mode Rejection Ratio (Note 4)	100		100		90						dB	V_{DD} = 10 to 20 V, I_D = 200 μA	

*JEDEC registered data.

NOTES:
1. Pulse test required, pulsewidth = 300 μs, duty cycle < 3%.
2. Assumes smaller value in numerator
3. Measured at end points, T_A and T_B
4. CMRR = $20\log_{10}\left(\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right)$, ΔV_{DD} = 10 V.

NS

© 1979 Siliconix incorporated

monolithic dual n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NNP See Section 5

■ General Purpose Differential Amplifiers

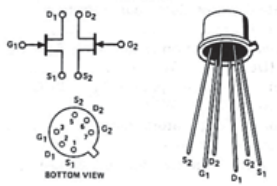
BENEFITS

- High Input Impedance
  $I_G < 50$ pA
- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5545)

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . –50 V
Gate Current . . . . . 30 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 1.67 mW/°C) . . . . . 250 mW
Total Device Dissipation, T_A = 25°C
(Derate 2.67 mW/°C) . . . . . 400 mW
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 30 seconds) . . . . . 300°C

TO-71
See Section 7



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-150	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		V_{DS} = 15 V, I_D = 0.5 nA	
5		I_G	Gate Operating Current		-50	pA	V_{DG} = 15 V, I_D = 200 μA	
6		I_{DSS}	Saturation Drain Current	0.5	8	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1500	6000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		25			
9		C_{iss}	Common-Source Input Capacitance		6	pF		f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
11		NF	Spot Noise Figure		3.5	dB	V_{DG} = 15 V, I_D = 200 μA, 2N5545	f = 10 Hz, R_G = 1 MΩ
					5		2N5546	
12		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		180	$\frac{nV}{\sqrt{Hz}}$	2N5545	f = 10 Hz
					200		2N5546	

		Characteristic		2N5545 Min	2N5545 Max	2N5546 Min	2N5546 Max	2N5547 Min	2N5547 Max	Unit	Test Conditions	
13	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5	nA	V_{DG} = 15 V, I_D = 200 μA	T_A = 125°C
14		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.90	1	0.90	1	–	V_{DS} = 15 V, V_{GS} = 0	
15		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DG} = 15 V	I_D = 50 μA
					5		10		15			I_D = 200 μA
16		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)		10		20		40	μV/°C	V_{DG} = 15 V, I_D = 200 μA	T_A = 25°C, T_B = 125°C
					10		20		40			T_A = -55°C, T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.95	1	0.90	1	–		f = 1 kHz
18		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		1		2		3	μmho		

*JEDEC registered data.
NOTES:
1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

NNP
NP-D

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

Performance Curves NRL See Section 5

■ General Purpose Amplifiers

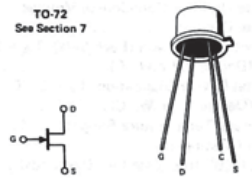
BENEFITS

- Low Noise
- Low Output Conductance

***ABSOLUTE MAXIMUM RATINGS (at 25°C)**

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . -30 V
Gate Current . . . . . 10 mA
Total Device Dissipation
(25°C Free Air Temperature) . . . . . 300 mW
Power Derating (to +175°C) . . . . . 2.0 mW/°C
Storage Temperature Range . . . . . –65 to +200°C
Operating Temperature Range . . . . . –65 to +175°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 240°C

TO-72
See Section 7



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

		Characteristic		2N5556 Min	2N5556 Max	2N5557 Min	2N5557 Max	2N5558 Min	2N5558 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0 V	
2					-100		-100		-100			T = 150°C
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.2	-4.0	-0.8	5.0	-1.5	-6.0	V	V_{DS} = 15 V, I_D = 1 nA	
4		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30			I_G = -10 μA, V_{DS} = 0 V	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.5	2.5	2.0	5.0	4.0	10.0	mA	V_{DG} = 15 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1500	6500	1500	6500	1500	6500	μmho	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		20		20		20			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		6		6		6			
10		$\overline{e}_n$	Common-Source Equivalent Short Circuit Input Noise Voltage		35		35		35	$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz
11					20		20		20			f = 100 Hz
12		NF	Noise Figure		1		1		1	dB	V_{DS} = 15 V, V_{GS} = 0 V, BW = 1.0 Hz	f = 10 Hz
13					1		1		1			f = 100 Hz

*JEDEC registered data
NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Pulse test duration ≤ 2 ms.

NRL

© 1979 Siliconix Incorporated

matched dual n-channel JFETs *designed for . . .*

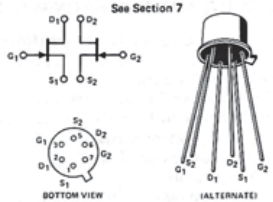
Siliconix

- **Wideband Differential Amplifiers**
- **Commutators**

Performance Curves NC
See Section 5

BENEFITS
- High Gain
  7500 μmho Minimum g_{fs}
- Specified Matching Characteristics

TO-71
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	50 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 2.2 mW/°C)	325 mW
Total Device Dissipation, T_A = 25°C (Derate 3.3 mW/°C)	650 mW
Storage Temperature Range	-65 to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-200	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3		V_{DS} = 15 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Voltage		1.0		V_{DS} = 0 V, I_G = 2 mA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	30	mA	V_{DS} = 15 V, V_{GS} = 0	
7		$r_{DS(on)}$	Static Drain Source ON Resistance		100	Ω	I_D = 1 mA, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	7500	12,500	μmho	V_{DG} = 15 V, I_D = 2 mA	f = 1 kHz
				7000				f = 100 MHz
9		g_{os}	Common-Source Output Conductance		45			f = 1 kHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF		f = 1 MHz
11		C_{iss}	Common-Source Input Capacitance		12			
12		NF	Spot Noise Figure		1.0	dB		f = 10 Hz, R_g = 1M
13		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz

		Characteristics		2N5564 Min	2N5564 Max	2N5565 Min	2N5565 Max	2N5566 Min	2N5566 Max	Unit	Test Conditions	
14	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	0.95	1	–	V_{DS} = 15 V, V_{GS} = 0	
15		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		20	mV	V_{DS} = 15 V, I_D = 2 mA	
16		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		10		25		50	μV/°C		T_A = 25°C, T_B = 125°C
					10		25		50			T_A = -55°C, T_B = 25°C
17		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	0.95	1	0.90	1	0.90	1	–		f = 1 kHz

*JEDEC registered data.

NC

NOTES:
1. Pulse test required, pulse width 300 μs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at ends points, T_A and T_B.

© 1979 Siliconix Incorporated

matched dual n-channel JFETs *designed for . . .*

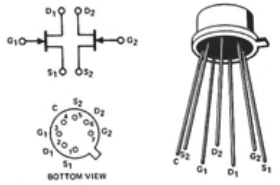
Siliconix

- **Differential Amplifiers**
- **High Input Impedance Amplifiers**

Performance Curves NT
See Section 5

BENEFITS
- Matching Characteristics Specified
- High Input Impedance
  I_G = 1 pA Max (2N5906–9)

TO-78
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-40 V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3 mW/°C)	367 mW
Total Device Dissipation, T_A = 25°C (Derate 4 mW/°C)	500 mW
Storage Temperature Range	-65 to +150°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5902-5 Min	2N5902-5 Max	2N5906-9 Min	2N5906-9 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-2	pA	V_{GS} = -20 V, V_{DS} = 0	
2					-10		-5	nA		125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.6	-4.5	-0.6	-4.5		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate Source Voltage		-4		-4			
6		I_G	Gate Operating Current		-3		-1	pA	V_{DG} = 10 V, I_D = 30 μA	
7					-3		-1	nA		125°C
8	DYNAMIC	I_{DSS}	Saturation Drain Current	30	500	30	500	μA	V_{DS} = 10 V, V_{GS} = 0	
9		g_{fs}	Common-Source Forward Transconductance	70	250	70	250	μmho		f = 1 kHz
10		g_{os}	Common-Source Output Conductance		5		5			
11		C_{iss}	Common-Source Input Capacitance		3		3	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5			
13		g_{fs}	Common-Source Forward Transconductance	50	150	50	150	μmho	V_{DG} = 10 V, I_D = 30 μA	
14		g_{os}	Common-Source Output Conductance		1		1			f = 1 kHz
15		$\overline{e}_n$	Equivalent Short Circuit Input Noise Voltage		0.2		0.1	$\frac{\mu V}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	
16		NF	Spot Noise Figure		3		1	dB		f = 100 Hz, R_G = 10 M

		Characteristic		2N5902, 6 Min	2N5902, 6 Max	2N5903, 7 Min	2N5903, 7 Max	2N5904, 8 Min	2N5904, 8 Max	2N5905, 9 Min	2N5905, 9 Max	Unit	Test Conditions	
17	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		2.0		2.0		2.0		2.0	nA	V_{DG} = 10 V, I_D = 30 μA, T_A = 125°C	2N5902-5
18					0.2		0.2		0.2		0.2			2N5906-9
19		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	–	V_{DS} = 10 V, V_{GS} = 0	
20		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	–	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
21		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
22		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)		5		10		20		40	μV/°C		T_A = 25°C, T_B = 125°C
23					5		10		20		40			T_A = -55°C, T_B = 25°C
24		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.2		0.2		0.2		0.2	μmho		f = 1 kHz

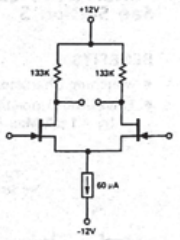
*JEDEC registered data.

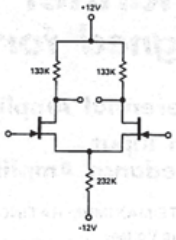
NT

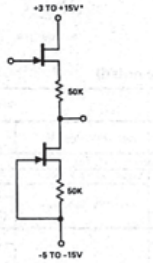
NOTES:
1. Assumes smaller value in numerator.
2. Measured at end points, T_A and T_B.

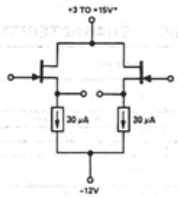
© 1979 Siliconix Incorporated

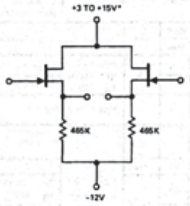
APPLICATIONS

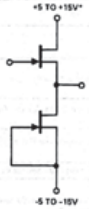












*Use lower voltages for minimum I_G

© 1979 Siliconix Incorporated

matched dual n-channel JFETs *designed for . . .*

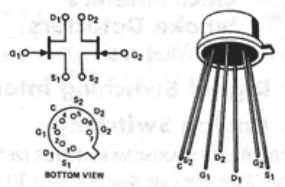
■ Wideband Differential Amplifiers

Performance Curves NZF See Section 5

BENEFITS

- High Gain through 100 MHz $g_{fs} > 5000$ µmho
- Matching Characteristics Specified

TO-78 See Section 7



***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-to-Gate Voltage	±80 V
Gate-Drain or Gate-Source Voltage	-25 V
Gate Current	50 mA
Device Dissipation (Each Side), (Derate 3 mW/°C)	367 mW
Total Device Dissipation, (Derate 4 mW/°C)	500 mW
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

***ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)**

			Characteristic	Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-250	nA		T_A = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.3	-4			
6		I_G	Gate Operating Current		-100	pA	V_{DG} = 10 V, I_D = 5 mA	
					-100	nA		T_A = 125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0 V	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	5000	10,000	µmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
9		g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
10		g_{os}	Common-Source Output Conductance		100			f = 1 kHz
11		g_{os}	Common-Source Output Conductance		150			f = 100 MHz
12		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
15		NF	Spot Noise Figure		1	dB		f = 10 kHz R_G = 100K

			Characteristic	2N5911 Min	2N5911 Max	2N5912 Min	2N5912 Max	Unit	Test Conditions	
16	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5 mA	T_A = 125°C
17		$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.95	1	0.95	1	–	V_{DS} = 10 V, V_{GS} = 0	
18		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		10		15	mV	V_{DG} = 10 V, I_D = 5 mA	
19		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)		20		40	µV/°C		T_A = 25°C T_B = 125°C
20					20		40			T_A = -55°C T_B = 25°C
21		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0.95	1	0.95	1	–		f = 1 kHz

*JEDEC registered data. NZF

NOTES:
1. Pulsewidth ≤ 300 µs, duty cycle ≤ 3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

© 1979 Siliconix Incorporated

enhancement-type p-channel MOSFETs

Siliconix

designed for . . .

- **Ultra-High Input Impedance Amplifiers**
  - **Electrometers**
  - **Smoke Detectors**
  - **pH Meters**
- **Digital Switching Interfaces**
- **Analog Switching**

Performance Curves MRA See Section 5

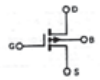
BENEFITS

- Rugged MOS Gate Minimizes Handling Problems
  ±150 V Transient Capability
- Low Gate-Leakage
  Typically 0.02 pA
- High Off-Isolation as a Switch
  I_{DSS} < 200 pA

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Drain-Source or Gate-Source Voltage 3N163 . . . . . −40 V
Drain-Source or Gate-Source Voltage 3N164 . . . . . −30 V
Transient Gate-Source Voltage (Note 1) . . . . . ±150 V
Drain Current . . . . . −50 mA
Storage Temperature . . . . . −65 to +200°C
Operating Junction Temperature . . . . . −55 to +150°C
Total Device Dissipation
(Derate 3.0 mW/°C to 150°C) . . . . . 375 mW
Lead Temperature 1/16" From Case For 10 Seconds . .265°C

TO-72
See Section 7





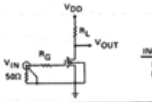
***ELECTRICAL CHARACTERISTICS (25°C and V_{BS} = 0 unless otherwise noted)**

		Characteristic		3N163 Min	3N163 Max	3N164 Min	3N164 Max	Unit	Test Conditions	
1		I_{GSS}	Gate-Body Leakage Current		-10			pA	V_{GS} = -40 V, V_{DS} = 0	T_A = 125°C
2					-25					
3							-10		V_{GS} = -30 V, V_{DS} = 0	T_A = 125°C
4							-25			
5	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30		V	I_D = -10 µA, V_{GS} = 0	
6		BV_{SDS}	Source-Drain Breakdown Voltage	-40		-30			I_S = -10 µA, V_{GD} = V_{BD} = 0	
7		V_{GS}	Gate Source Voltage	-3	-6.5	-2.5	-6.5		V_{DS} = -15 V, I_D = -0.5 mA	
8		$V_{GS(th)}$	Gate-Source Threshold Voltage	-2	-5	-2	-5		V_{DS} = V_{GS}, I_D = -10 µA	
9		I_{DSS}	Drain Cutoff Current		-200		-400	pA	V_{DS} = -15 V, V_{GS} = 0	
10		I_{SDS}	Source Cutoff Current		-400		-800		V_{SD} = -20 V, V_{GD} = 0, V_{DB} = 0	
11		$I_{D(on)}$	ON Drain Current	-5	-30	-3	-30	mA	V_{DS} = -15 V, V_{GS} = -10 V	
12		$r_{DS(on)}$	Drain-Source ON Resistance		250		300	Ω	V_{GS} = -20 V, I_D = -100 µA	
13	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2,000	4,000	1,000	4,000	µmho	V_{DS} = -15 V, I_D = -10 mA	f = 1 kHz
14		g_{os}	Common-Source Output Conductance		250		250			
15		C_{iss}	Common-Source Input Capacitance		2.5		2.5	pF	V_{DS} = -15 V, I_D = -10 mA	f = 1 MHz
16		C_{rss}	Common-Source Reverse Transfer Capacitance		0.7		0.7			
17		C_{oss}	Common-Source Output Capacitance		3		3			
18	SW	$t_{d(on)}$	Turn-ON Delay Time		12		12	ns	V_{DD} = -15 V, $I_{D(on)}$ = -10 mA, R_G = R_L = 1.5 kΩ	
19		t_r	Rise Time		24		24			
20		t_{off}	Turn-OFF Time		50		50			

*JEDEC registered data

MRA

NOTE:
1. Transient gate-source voltage JEDEC registered as ±125 V.



INPUT PULSE
RISE TIME < 2 ns
PULSE WIDTH > 200 ns

SAMPLING SCOPE
t_r < 0.2 ns
C_{IN} < 2 pF
R_{IN} > 10 MΩ

© 1979 Siliconix Incorporated

current regulator diodes

Siliconix

designed for . . .

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Low Voltage References**

Performance Curves NKL NKM NKO See Section 5

BENEFITS

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes
  Temperature Coefficient Better Than 1500 ppm/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources
  No Power Supplies Required

ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage . . . . . 100 V
Forward Current . . . . . 20 mA
Reverse Current . . . . . 50 mA
Thermal Resistance θ_{JC} . . . . . 100°C/W
Power Dissipation at T_C = 25°C . . . . . 1.25 W
Operating Junction Temperature . . . . . −55 to +150°C
Storage Temperature . . . . . −55 to +200°C

TO-18
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

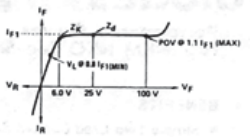
Symbol	I_{P1}			Z_d		Z_k		V_L		POV	r_{T1}			GEOM
Parameter	Regulator Current			Dynamic Impedance		Knee Impedance		Limiting Voltage		Peak Operating Voltage	Temperature Coefficient			
Test Conditions	V_P = 25 V (Note 1)			V_P = 25 V (Note 2)		V_P = 6 V		I_P = 0.8 $I_{P1(Min)}$ (Note 3)		I_P = 1.1 $I_{P1(Max)}$ (Note 4)	V_P = 25 V −55°C < T_A < 25°C	V_P = 25 V 0°C < T_A < 50°C	V_P = 25 V 25°C < T_A < 125°C	
Units	(mA)			MΩ		MΩ		Volts		Min Volts	Typ ppm/°C	Typ ppm/°C	Typ ppm/°C	
	Nom	Min	Max	Min	Typ	Min	Typ	Max	Typ					
CR022	0.22	0.198	0.242	13.0	16.0	2.75	3.5	1.0	0.40	100	+1350	+1050	+750	
CR024	0.24	0.216	0.264	10.0	14.0	2.25	3.0	1.0	0.45	100	+1200	+900	+600	
CR027	0.27	0.243	0.297	9.0	13.0	1.95	2.8	1.0	0.50	100	+1000	+700	+400	
CR030	0.30	0.270	0.330	8.0	12.0	1.60	2.5	1.0	0.55	100	+800	+500	+200	
CR033	0.33	0.297	0.363	6.6	11.0	1.25	2.2	1.0	0.60	100	+600	+300	-50	NKL
CR039	0.39	0.351	0.429	4.10	9.5	1.00	1.90	1.05	0.70	100	+300	+50	-200	
CR043	0.43	0.387	0.473	3.20	8.6	0.87	1.65	1.05	0.78	100	+150	-150	-450	
CR047	0.47	0.423	0.517	2.70	8.0	0.75	1.50	1.10	0.85	100	-50	-300	-600	
CR056	0.56	0.504	0.616	1.90	6.5	0.56	1.25	1.20	0.98	100	-300	-600	-900	
CR062	0.62	0.558	0.682	1.55	6.2	0.47	1.15	1.30	1.10	100	-500	-800	-1100	
CR068	0.68	0.612	0.748	1.35	8.5	0.400	1.70	1.15	0.70	100	+850	+400	-50	
CR075	0.75	0.675	0.825	1.15	7.2	0.335	1.50	1.20	0.75	100	+650	+200	-250	
CR082	0.82	0.738	0.902	1.00	6.0	0.290	1.30	1.25	0.80	100	+450	+50	-450	
CR091	0.91	0.819	1.001	0.88	5.2	0.240	1.10	1.29	0.85	100	+300	-150	-600	
CR100	1.00	0.900	1.100	0.80	4.4	0.205	0.95	1.35	0.95	100	+150	-300	-750	NKM
CR110	1.10	0.990	1.210	0.70	3.8	0.180	0.80	1.40	1.05	100	+50	-450	-900	
CR120	1.20	1.08	1.32	0.64	3.3	0.155	0.71	1.45	1.15	100	-150	-600	-1050	
CR130	1.30	1.17	1.43	0.58	3.2	0.135	0.60	1.50	1.25	100	-300	-750	-1200	
CR140	1.40	1.26	1.54	0.54	3.5	0.115	0.52	1.55	1.30	100	-400	-850	-1300	
CR150	1.50	1.35	1.65	0.51	2.2	0.105	0.46	1.60	1.35	100	-500	-950	-1400	
CR160	1.60	1.44	1.76	0.475	1.00	0.092	0.35	1.65	0.50	100	+650	+350	+50	
CR180	1.80	1.62	1.98	0.420	0.95	0.074	0.30	1.75	0.55	100	+500	+200	-100	
CR200	2.00	1.80	2.20	0.395	0.88	0.061	0.25	1.85	0.60	100	+350	+50	-250	
CR220	2.20	1.98	2.42	0.370	0.80	0.052	0.22	1.95	0.65	100	+200	-100	-350	
CR240	2.40	2.16	2.64	0.345	0.75	0.044	0.20	2.00	0.70	100	+50	-200	-450	NKO
CR270	2.70	2.43	2.97	0.320	0.68	0.035	0.18	2.15	0.75	100	-100	-300	-550	
CR300	3.00	2.70	3.30	0.300	0.60	0.029	0.14	2.25	0.85	100	-250	-450	-700	
CR330	3.30	2.97	3.63	0.280	0.56	0.024	0.13	2.35	0.90	100	-400	-600	-800	
CR360	3.60	3.24	3.96	0.265	0.52	0.020	0.11	2.50	0.95	100	-550	-750	-900	
CR390	3.90	3.51	4.29	0.255	0.48	0.017	0.10	2.60	1.00	100	-700	-850	-1000	
CR430	4.30	3.87	4.73	0.245	0.45	0.014	0.09	2.75	1.10	100	-850	-950	-1100	
CR470	4.70	4.23	5.17	0.235	0.40	0.012	0.08	2.90	1.40	100	-1000	-1100	-1200	

NOTES
1. Pulse test — steady state currents may vary.
2. Pulse test — steady state impedances may vary.
3. Min V_P required to insure $I_P > 0.8\ I_{P1(Min)}$.
4. Max V_P where $I_P < 1.1\ I_{P1(Max)}$ is guaranteed.

NKL, NKM, NKO

© 1979 Siliconix Incorporated

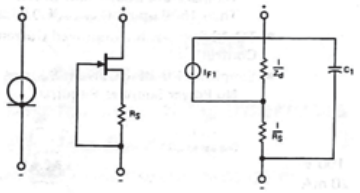
Current-Limiter Diode V-I Characteristic



SYMBOLS AND DEFINITIONS

A	Anode (Drain)
C	Cathode (Source and Gate Shorted)
I_F	Forward Current (Anode Positive)
I_{F1}	Current at a specified Test Voltage, V_F
POV	Peak Operating Voltage
θ_I	Current Temperature Coefficient
θ_{JC}	Thermal Resistance Junction to Case
θ_{JA}	Thermal Resistance Junction to Ambient
Z_K	Knee AC Impedance at specified V_F. Z_K should be as high as possible and is specified as a minimum.
Z_d	Dynamic Impedance at specified V_F. Z_d is specified as a minimum.

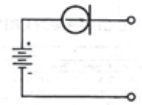
EQUIVALENT CIRCUIT



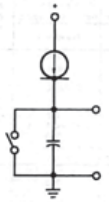
APPLICATIONS

The current-limiter diode is the electrical dual of the Zener diode.

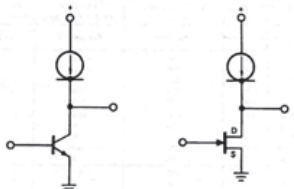
Constant-Current Supply or Current-Limiting Element



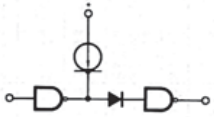
Constant-Current Timing Circuits



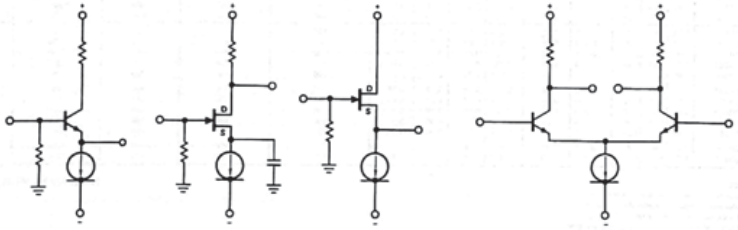
Collector or Drain Hi-Z Load Resistors



Logic Circuit Pull-Up Current Source



Emitter or Source Biasing



© 1979 Siliconix incorporated

enhancement-type p-channel MOSFET *designed for . . .*

Siliconix

Performance Curves MRA See Section 5

- **High-Input Impedance Amplifiers**
  - **Smoke Detectors**
  - **Electrometers**
  - **pH Meters**

BENEFITS

- High Input Impedance
  I_{GSS} = 30 Femto Amp Typical
- High Gain
  g_{fs} = 1000 μmho Minimum

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage	25 V
Gate-Source Voltage	±10 V
Drain Current	30 mA
Total Device Dissipation at (Or Below) T_A = 25°C	
(Derate 3 mW/°C to +150°C)	375 mW
Operating Junction Temperature	−55 to +150°C
Storage Temperature	−65 to +200°C
Lead Temperature	
(1/16" from case for 10 seconds)	265°C

TO-18
See Section 7





ELECTRICAL CHARACTERISTICS (25°C)

			Characteristic	Min	Max	Unit	Test Conditions
1	STATIC	I_{GSS}	Gate-Source Leakage Current		−1.0	pA	V_{GS} = −10 V, V_{DS} = 0
2		BV_{DSS}	Drain-Source Breakdown Voltage	−25		V	I_D = −10 μA, V_{GS} = 0
3		V_{GS}	Gate-Source Voltage	−2.0	−6.0	V	V_{DS} = −10 V, I_D = −10 μA
4		I_{DSS}	Drain Cutoff Current		−20	nA	V_{DS} = −10 V, V_{GS} = 0
5		$I_{D(on)}$	ON Drain Current	−3.0		mA	V_{DS} = −10 V, V_{GS} = −10 V
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1000		μmhos	V_{DS} = −10 V, I_D = −2 mA, f = 1 kHz
7		C_{iss}	Common-Source Input Capacitance		6.0	pF	V_{DS} = −10 V, V_{GS} = −10 V, f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		

MRA

© 1979 Siliconix incorporated

dual pico ampere diodes
designed for . . .

- **Clipping Circuits**
- **Diode Switching**
- **High Impedance Protection Circuits**

BENEFITS
- Very High Off-Isolation 1 pA Max (DPAD1)
- High Isolation Between Diodes 20 Femto Amp Typical (DPAD1)
- Matched Capacitances
- Compact Packaging

TO-71 (Pins 2 and 6 Removed) See Section 7

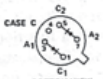


TO-78 (DPAD1 Only) See Section 7





BOTTOM VIEW (ALTERNATE)



BOTTOM VIEW

ABSOLUTE MAXIMUM RATINGS (25°C)

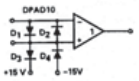
Forward Gate Current, Each Side . . . . . 50 mA
Total Device Dissipation @ T_A = 25°C
Derate 4.0 mW/°C to 125°C . . . . . 400 mW
Storage Temperature Range . . . . . −55 to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

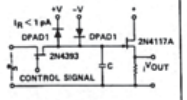
		CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITION	
1	STATIC	I_R	Reverse Current			−1	pA	V_R = −20 V	DPAD1
2						−2			DPAD2
3						−5			DPAD5
4						−10			DPAD10
5						−20			DPAD20
6						−50			DPAD50
7						−100			DPAD100
8		B_{VR}	Reverse Breakdown Voltage	−45		−120	V	I_R = −1 µA	DPAD1, 2, 5
9				−35					DPAD10, 20, 50, 100
10		V_F	Forward Voltage Drop		0.8	1.5		I_F = 1 mA	DPAD1, 2, 5, 10, 20, 50, 100
11	DYN	C_R	Capacitance			0.8	pF	V_R = −5 V, f = 1 MHz	DPAD1, 2, 5
12						2.0			DPAD10, 20, 50, 100
13	MAT	$\lvert C_{R1}-C_{R2}\rvert$	Differential Capacitance		0.1	0.2	pF	$V_{R1} = V_{R2}$ = −5 V, f = 1 MHz	DPAD1, 2, 5, 10, 20, 50, 100

APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by DPADS D_1 and D_2 Common mode input voltage limited by DPADS D_3 and D_4 to ±15 V.



Typical sample and hold circuit with clipping. DPAD diodes reduce offset voltages fed capacitively from the FET switch gate.



© 1979 Siliconix Incorporated

low-leakage pico-amp diodes
designed for . . .

- **Clipping Circuits**
- **Diode Switching**
- **High Impedance Protection Circuits**

BENEFITS
- Very High Off-Isolation 1 pA Max (PAD1)

TO-18 See Section 7





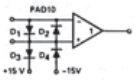
CASE LEAD FOR PAD1, 2, 5 ONLY

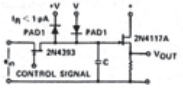
ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Current . . . . . 50 mA
Total Device Dissipation . . . . . 300 mW
Storage Temperature Range . . . . . −55°C to +125°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_R	Reverse Current			−1	pA	V_R = −20 V	PAD1
2						−2			2
3						−5			5
4						−10			PAD10
5						−20			20
6						−50			50
7						−100			PAD100
8		BV_R	Breakdown Voltage (Reverse)	−45		−120	V	I_R = −1 µA	PAD1, 2, 5
9				−35					PAD10, 20, 50, 100
10		V_F	Forward Voltage Drop		0.8	1.5		I_F = 5 mA	PAD1, 2, 5, 10, 20, 50, 100
11	DYN	C_R	Capacitance			0.8	pF	V_R = −5 V, f = 1 MHz	PAD1, 2, 5
12						2			PAD10, 20, 50, 100





APPLICATION

Operational Amplifier Protection. Input Differential Voltage limited to 0.8 V (typ) by PADS D_1 and D_2 Common mode input voltage limited by PADS D_3 and D_4 to ±15 V.

Typical sample and hold circuit with clipping. PAD diodes reduce offset voltages fed capacitively from the FET switch gate.

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

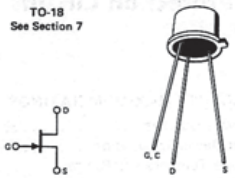
- **Analog Switches**
- **Commutators**
- **Choppers**

Performance Curves NC See Section 5

BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 50\ \Omega$ (U202)
- Good Off-Isolation
  $I_{D(off)} < 1$ nA

TO-18
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -30 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Case Temperature
(Derate 10 mW/°C) . . . . . 1.8 W
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U200 Min	U200 Max	U201 Min	U201 Max	U202 Min	U202 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-1		-1		-1	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-3	-1.5	-5	-3.5	-10		V_{DS} = 20 V, I_D = 10 nA	
5		$I_{D(off)}$	Drain Cutoff Current		1		1		1	nA	V_{DS} = 10 V, V_{GS} = -12 V	
					1		1		1	µA		150°C
6		I_{DSS}	Saturation Drain Current (Note 1)	3	25	15	75	30	150	mA	V_{DS} = 20 V, V_{GS} = 0	
7		$r_{ds(on)}$	Drain-Source ON Resistance		150		75		50	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
8	DYN	C_{iss}	Common-Source Input Capacitance (Note 1)		30		30		30	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		8		8		8		V_{DS} = 0, V_{GS} = -12 V	

NOTE:
1. Pulse test required, pulsewidth = 300 µsec, duty cycle ≤ 3%.

NC

© 1979 Siliconix incorporated

monolithic dual n-channel JFETs *designed for . . .*

Siliconix

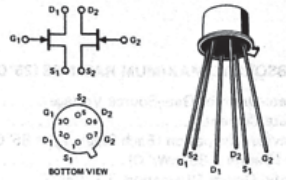
- **Differential Amplifiers**

Performance Curves NNP See Section 5

BENEFITS

- Good Matching Characteristics

TO-71
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -50 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C
(Derate 1.7 mW/°C to 200°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
2					-500	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5		V_{DS} = 20 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	-0.3	-4.0			
6		I_G	Gate Operating Current		-50	pA	V_{DG} = 20 V, I_D = 200 µA	
					-250	nA		125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	3000	µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
9				1000				f = 100 MHz
10		g_{fs}	Common-Source Forward Transconductance (Note 1)	600	1600		V_{DG} = 20 V, I_D = 200 µA	f = 1 kHz
11		g_{os}	Common-Source Output Conductance		35		V_{DS} = 20 V, V_{GS} = 0	
12		g_{os}	Common-Source Output Conductance		10		V_{DG} = 20 V, I_D = 200 µA	
13		C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
15		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		80	$\frac{nV}{\sqrt{Hz}}$		f = 100 Hz

		Characteristic		U231 Max	U232 Max	U233 Max	U234 Max	U235 Max	Unit	Test Conditions	
15	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	10	10	10	10	10	nA	V_{DG} = 20 V, I_D = 200 µA	125°C
16		$\frac{(I_{DSS1}-I_{DSS2})}{I_{DSS1}}$	Saturation Drain Current Match (Note 1)	5	5	5	10	15	%	V_{DS} = 20 V, V_{GS} = 0	
17		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	5	10	15	20	25	mV		
18		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)	10	25	50	75	100	µV/°C	V_{DG} = 20 V, I_D = 200 µA	T_A = 25°C, T_B = 125°C
19				10	25	50	75	100			T_A = -55°C, T_B = 25°C
20		$\frac{(g_{fs1}-g_{fs2})}{g_{fs1}}$	Transconductance Match (Note 1)	3	5	5	10	15	%		f = 1 kHz
21		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance	5	5	5	5	5	µmho		

NOTES:
1. Pulse test required, pulsewidth = 300 µs, duty cycle ≤ 3%.
2. Measured at end points, T_A and T_B.

NNP
NP-D

© 1979 Siliconix incorporated

matched dual n-channel JFET *designed for . . .*

Siliconix

- **Wideband Differential Amplifiers**

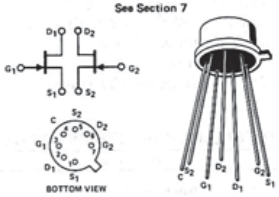
Performance Curves NZF See Section 5

BENEFITS
- High Gain through 100 MHz g_{fs} = 5000 μmho Minimum
- Matching Characteristics Specified

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 50 mA
Device Dissipation (Each Side), T_A = 85°C
(Derate 3.85 mW/°C) . . . . . 250 mW
Total Device Dissipation, T_A = 85°C
(Derate 7.7 mW/°C) . . . . . 500 mW
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

TO-78
See Section 7



ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-250	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-5		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	5	40	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
7		g_{fs}	Common-Source Forward Transconductance	5000	10,000		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
8		g_{os}	Common-Source Output Conductance		150		V_{DS} = 10 V, I_D = 5 mA	f = 1 kHz
9		g_{os}	Common-Source Output Conductance		150		V_{DG} = 10 V, I_D = 5 mA	f = 100 MHz
10		C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
12		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		30	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
13	MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	0.85	1		V_{DS} = 10 V, V_{GS} = 0	
14		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		100	mV	V_{DG} = 10 V, I_D = 5 mA	
15		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 2)	0.85	1			f = 1 kHz
16		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		20	μmho		

NZF

NOTES:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 30%.
2. Assumes smaller value in numerator.

© 1979 Siliconix incorporated

n-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**

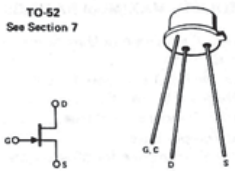
Performance Curves NVA See Section 5

BENEFITS
- Ultra-Low Insertion Loss $R_{DS(on)} < 2.5\ \Omega$ (U290)
- High Off-Isolation $I_{D(off)} < 1$ nA

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . -30 V
Gate Current . . . . . 100 mA
Drain Current . . . . . 1.5 A
Total Device Dissipation at 25°C
Free-Air Temperature (Note 1) . . . . . 500 mW
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-52
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U290 Min	U290 Max	U291 Min	U291 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1	nA	V_{GS} = -15 V, V_{DS} = 0	
2					-1		-1	μA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4	-10	-1.5	-4.5		V_{DS} = 15 V, I_D = 3 nA	
5		$I_{D(off)}$	Drain Cutoff Current		1		1	nA	V_{DS} = 5 V, V_{GS} = -10 V	
6					1		1	μA		150°C
7		$V_{DS(on)}$	Drain-Source ON Voltage		25		70	mV	V_{GS} = 0, I_D = 10 mA	
8		I_{DSS}	Saturation Drain Current (Note 2)	500		200		mA	V_{DS} = 10 V, V_{GS} = 0	
9		$r_{DS(on)}$	Static Drain-Source ON Resistance	1.0	2.5	2	7	Ω	V_{GS} = 0 V, I_D = 10 mA	
10	DYNAMIC	$r_{ds(on)}$	Drain-Source ON Resistance	1.0	2.5	2	7	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
11		C_{SGO}	Source-Gate OFF Capacitance		30		30	pF	V_{SG} = 15 V, I_D = 0	f = 1 MHz
12		C_{DGO}	Drain-Gate OFF Capacitance		30		30		V_{DG} = 15 V, I_S = 0	
13		$C_{SG}+C_{DG}$	Source Gate Plus Drain Gate On Capacitance		160		160		V_{DS} = 0, V_{GS} = 0	
14	SWITCHING	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	V_{DD} = 1.5 V, $I_{D(on)}$ = 30 mA, R_L = 50 Ω, $V_{GS(on)}$ = 0 V, $V_{GS(off)}$ = -12 V (U290) $V_{GS(off)}$ = - 7 V (U291)	
15		t_r	Rise Time		20		20			
16		$t_{d(off)}$	Turn-OFF Delay Time		15		15			
17		t_f	Fall Time		20		20			

NVA

NOTES:
1. Derate linearly at the rate of 4.0 mW/°C.
2. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.

© 1979 Siliconix incorporated

p-channel JFETs
designed for . . .

- **Analog Switches**
- **Commutators**
- **Choppers**

Siliconix

Performance Curves PS
See Section 5

BENEFITS

- Low Insertion Loss
  $R_{DS(on)} < 85\ \Omega$ (U304)
- High Off-Isolation
  $I_{D(off)} < 500$ pA

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) . . 30 V
Gate Current . . . . . 50 mA
Total Device Dissipation, Free-Air
(Derate 2.8 mW/°C) . . . . . 350 mW
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 60 seconds) . . . . . 300°C

TO-18
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U304 Min	U304 Max	U305 Min	U305 Max	U306 Min	U306 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		500		500		500	pA	V_{GS} = 20 V, V_{DS} = 0	
2					1.0		1.0		1.0	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4		V_{DS} = -15 V, I_D = -1 µA	
5		$V_{DS(on)}$	Drain-Source ON Voltage		-1.3		-0.8		-0.6		V_{GS} = 0, I_D = -15 mA (U304), I_D = -7 mA (U305), I_D = -3 mA (U306)	
6		I_{DSS}	Saturation Drain Current (Note 2)	-30	-90	-15	-60	-5	-25	mA	V_{DS} = -15 V, V_{GS} = 0	
7		$I_{D(off)}$	Drain Cutoff Current		-500		-500		-500	pA	V_{DS} = -15 V, V_{GS} = 12 V (U304), V_{GS} = 7 V (U305), V_{GS} = 5 V (U306)	
8					-1.0		-1.0		-1.0	µA		150°C
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0 V, I_D = -1 mA	
10		$r_{ds(on)}$	Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0 V, I_D = 0	f = 1 kHz
11	DYN	C_{iss}	Common-Source Input Capacitance		27		27		27	pF	V_{DS} = -15 V, V_{GS} = 0	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7		V_{DS} = 0, V_{GS} = 12 V (U304) V_{GS} = 7 V (U305), V_{GS} = 5 V (U306)	
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		20		25		25	ns		
14		t_r	Rise Time		15		25		35			
15		$t_{d(off)}$	Turn-OFF Delay Time		10		15		20			
16		t_f	Fall Time		25		40		60			

	U304	U305	U306
V_{DD}	-10 V	-6 V	-6 V
$V_{GS(off)}$	12 V	7 V	5 V
R_L	580 Ω	743 Ω	1800 Ω
$V_{GS(on)}$	0	0	0
$I_{D(on)}$	-15 mA	-7 mA	-3 mA

PS

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse test pulsewidth = 300 µs, duty cycle < 3%.

© 1979 Siliconix Incorporated

n-channel JFETs
designed for . . .

- **VHF Amplifiers**
- **Front End High Sensitivity Amplifiers**
- **Oscillators**
- **Mixers**

Siliconix

Performance Curves NZA
See Section 5

BENEFITS

- Industry Standard
- High Power Gain
  16 dB at 105 MHz, Common-Gate
  11 dB at 450 MHz, Common-Gate
- Low Noise
  2.7 dB Noise Figure at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- 75 Ω Input Match Common Gate

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 20 mA
Total Power Dissipation at T_A = 25°C . . . . . 500 mW
Power Derating to 150°C . . . . . 4.0 mW/°C
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-52
See Section 7





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U308 Min	U308 Typ	U308 Max	U309 Min	U309 Typ	U309 Max	U310 Min	U310 Typ	U310 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current			-150			-150			-150	pA	V_{GS} = -15 V, V_{GS} = 0	
2						-150			-150			-150	nA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-6.0	-1.0		-4.0	-2.5		-6.0		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	I_G = 10 mA, V_{DS} = 0	
7	DYNAMIC	g_{fg}	Common-Gate Forward Transconductance (Note 1)	10		20	10		20	10		18	mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{og}	Common-Gate Output Conductance			200			200			200	µmho		
9		C_{gd}	Drain-Gate Capacitance			2.5			2.5			2.5	pF	V_{GS} = -10 V, V_{DS} = 10 V	f = 1 MHz
10		C_{gs}	Gate-Source Capacitance			5.0			5.0			5.0			
11		$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
12	HI FREQ	g_{fg}	Common-Gate Forward Transconductance		15			15			15		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
13					14			14			14				f = 450 MHz
14		g_{og}	Common-Gate Output Conductance		0.18			0.18			0.18				f = 105 MHz
15					0.32			0.32			0.32				f = 450 MHz
16		G_{pg}	Common-Gate Power Gain (Note 2)	14	16		14	16		14	16		dB		f = 105 MHz
17				10	11		10	11		10	11				f = 450 MHz
18		NF	Noise Figure		1.5	2.0		1.5	2.0		1.5	2.0			f = 105 MHz
19					2.7	3.5		2.7	3.5		2.7	3.5			f = 450 MHz

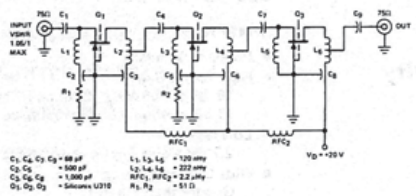
NZA

NOTES:
1. Pulse test duration = 2 ms.
2. Gain (G_{pg}) measured at optimum input noise match.

© 1979 Siliconix Incorporated

APPLICATIONS

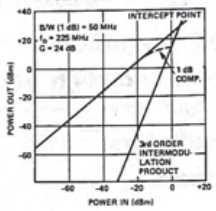
200–250 MHz Wideband Amplifer (1 dB Ripple)
3-Stage Amplifier Circuit



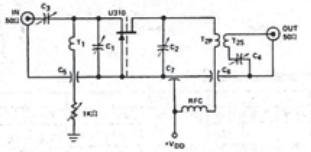
C_1, C_4, C_7, C_9 = 68 pF
C_2, C_5 = 500 pF
C_3, C_6, C_8 = 1,000 pF
Q_1, Q_2, Q_3 = Siliconix U310

L_1, L_3, L_5 = 120 nHy
L_2, L_4, L_6 = 222 nHy
RFC1, RFC2 = 2.2 μHy
R_1, R_2 = 51 Ω

2 Tone Intercept & Compression
Point Measurement



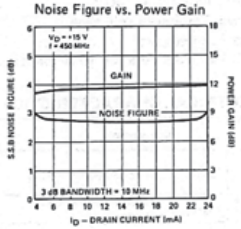
450 MHz Common Gate Amplifier



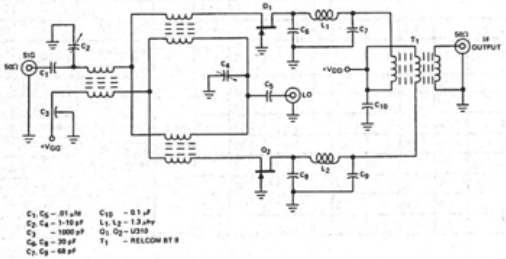
C_1, C_2 – 0.8–10 pF JFD model MVM 010H
C_3, C_4 – 8–35 pF Emc series 539-002D
C_5, C_6 – 5000 pF Erie (2443-000)
C_7 – 1000 pF ALLEN BRADLEY type FASC

RFC – 33 μH MILLER type (9230-30)
T_1 – one turn, #16 copper wire, ¼" I.D. (Air Core)
T_{2P} – one turn, #16 copper wire, ¼" I.D. (Air Core)
T_{2S} – one turn, #16 copper wire, ¼" I.D. (Air Core)

Noise Figure vs. Power Gain

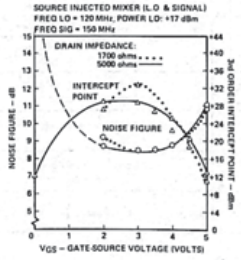


Prototype Active Balanced Mixer*



C_1, C_5 – .01 μF
C_2, C_4 – 1-10 pF
C_3 – 1000 pF
C_6, C_8 – 39 pF
C_7, C_9 – 68 pF
C_{10} – 0.1 μF
L_1, L_2 – 1.3 μHy
Q_1, Q_2 – U310
T_1 – RELCOM BT-9

Comparison of Mixer IM
Characteristics



*Reference Siliconix Application Note AN71-2.

© 1979 Siliconix incorporated

n-channel JFET
designed for . . .

- **VHF Amplifiers**
- **Oscillators**
- **Mixers**

Siliconix

Performance Curves NZA
See Section 5

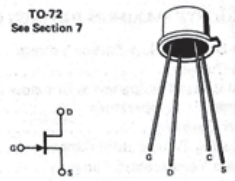
BENEFITS

- High Power Gain
  16 dB Typ @ 105 MHz, Common-Gate
  11 dB Typ @ 450 MHz, Common-Gate
- Low Noise Figure
  1.5 dB Typ @ 105 MHz
  2.7 dB Typ @ 450 MHz
- Wide Dynamic Range—Greater than 100 dB

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 10 mA
Total Device Dissipation (Derate 1.7 mW/°C) . . . . . 300 mW
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-72
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-150	pA	V_{GS} = -15 V, V_{DS} = 0	
2					-150	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-6		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	20	60	mA	V_{DS} = 10 V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage		1	V	I_G = 1 mA, V_{DS} = 0	
7	DYN	g_{fg}	Common-Gate Forward Transconductance (Note 1)	10,000	20,000	μmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{og}	Common-Gate Output Conductance		200			
9		C_{gd}	Gate-Drain Capacitance		2.5	pF	V_{DG} = 10 V, I_D = 5 mA	f = 1 MHz
10		C_{gs}	Gate-Source Capacitance		5.0			

NZA

NOTE:
1. Pulse test duration = 2 ms.

© 1979 Siliconix incorporated

n-channel JFET
designed for . . .

- **VHF/UHF Common-Gate Amplifiers**
- **Mixers**

Siliconix

Performance Curves NZF
See Section 5

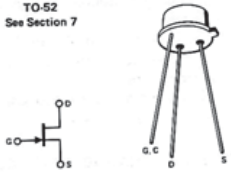
BENEFITS

- High Power Gain
  10 dB Typical at 450 MHz, Common Gate
- Low Noise
  NF = 3.5 dB Typical at 450 MHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 10 mA
Total Power Dissipation at or below 25°C
Free-Air Temperature . . . . . 500 mW
Power Derating . . . . . 4.0 mW/°C
Operating Temperature Range . . . . . -65 to +150°C
Storage Temperature Range . . . . . -65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

TO-52
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2					-0.1	µA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-6	V	V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	10	30	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYN	g_{fg}	Common-Gate Forward Transconductance (Note 1)	6000	10,000	µmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
7		g_{og}	Common-Gate Output Conductance		200	µmho		
8		C_{gd}	Gate-Drain Capacitance		1.2	pF	V_{DG} = 10 V, I_D = 10 mA	f = 1 MHz
9		C_{gs}	Gate-Source Capacitance		3.8	pF		

NZF

NOTE:
1. Pulse test duration = 2 ms.

© 1979 Siliconix incorporated

n-channel JFETs
designed for . . .

- **VHF Buffer Amplifiers**
- **IF Amplifiers**

Siliconix

Performance Curves NIP
See Section 5

BENEFITS

- High Gain
  g_{fs} = 120,000 µmho Typical
- Wide Dynamic Range
- Low Intermodulation Distortion

TO-39
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 100 mA
Total Device Dissipation (25°C Case Temperature) . . . . . .3 W
Power Derating (to 150°C) . . . . . 24 mW/°C
Storage Temperature Range . . . . . -55 to +150°C
Operating Temperature Range. . . . . -55 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

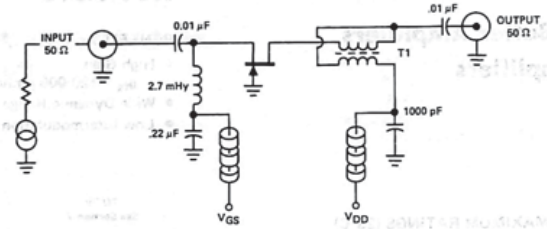
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U320 Min	U320 Typ	U320 Max	U321 Min	U321 Typ	U321 Max	U322 Min	U322 Typ	U322 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{GS} = -15 V, V_{DS} = 0 V	
2						-0.5			-0.5			-0.5	µA		T = 100°C
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-2		-10	-1		-4	-3		-10	V	V_{DS} = 5 V, I_D = 1 mA	
4		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				I_G = -1 µA, V_{DS} = 0 V	
5		I_{DSS}	Saturation Drain Current (Note 2)	100		500	80		250	200		700	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1			1			1	V	I_G = 1 mA, V_{DS} = 0 V	
7		$r_{DS(on)}$	Drain-Source ON Resistance			10			11			8	Ω	V_{GS} = 0 V, I_D = 10 mA	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	75	120	200	75	120	200	75	130	200	mmhos	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance			30			30			30	pF	V_{GS} = -10 V, V_{DS} = 0 V	f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance			15			15			15			
11		C_{gs}	Gate-Source Capacitance		12			12			12			V_{GS} = -10 V, I_D = 0	
12		C_{gd}	Gate-Drain Capacitance		12			12			12			V_{GD} = -10 V, I_S = 0	
13		$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		2			2			2		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 5 V, I_D = 10 mA	f = 1 kHz
14	HIGH FREQ	g_{fg}	Common Gate Forward Transconductance		55			55			55		mmho	V_{DG} = 20 V, I_D = 25 mA	f = 50 MHz
15		g_{ig}	Common-Gate Input Conductance		56			56			56				
16		g_{og}	Common-Gate Output Conductance		0.5			0.5			0.5				
17		G_{PS}	Power Gain (Note 3)		9			9			9		dB		
18		F_t	Gain-Bandwidth (Note 4)		400			400			400		MHz	V_{DS} = 15 V, V_{GS} = 0 V	
19		NF	Noise Figure (Note 3)		2.5			2.5			2.5		dB	V_{DG} = 20 V, I_D = 25 mA	f = 30 MHz

NIP

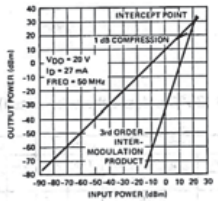
NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.
3. Noise figure (SSB) and power gain measured in circuit shown in Figure 1.
4. Computed as g_{fs}/C_{rss}.

© 1979 Siliconix Incorporated



T1–6 TURNS #22 AWG TWISTED PAIR WIRE ON 0.375 INCH DIAMETER INDIANA GENERAL F625-9Q2 TOROID CORE.

50 MHz Power Gain and Noise Figure Test Circuit for U320, U321 and U322
Figure 1



Gain – Intermodulation Characteristics
Figure 2

© 1979 Siliconix Incorporated

monolithic dual n-channel JFETs *designed for . . .*

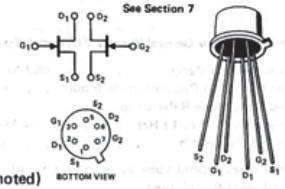
- **Low Noise FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Performance Curves NNR See Section 5

BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (U401)
  95 dB Minimum CMRR (U401-04)
- Low Drift with Temperature
  10 μV/°C Maximum (U401, 02)
- Operates from Low Power Supply Voltages
  $V_{GS(off)} < 2.5$ V
- Simplifies Amplifier Design
  Output Conductance < 2 μmho
- Low Noise
  $\overline{e_n}$ = 6 nV/√Hz at 10 Hz Typical

TO-71
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage	50 V
Forward Gate Current	10 mA
Device Dissipation (each side) @ T_A = 85°C derate 2.6 mW/°C	300 mW
Total Device Dissipation @ T_A = 85°C (derate 5 mW/°C)	500 mW
Storage Temperature Range	−65 to 200°C

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

		Characteristic	U401 Min	U401 Max	U402 Min	U402 Max	U403 Min	U403 Max	U404 Min	U404 Max	U405 Min	U405 Max	U406 Min	U406 Max	Unit	Test Conditions	
1		BV_{GSS} Gate-Source Breakdown Voltage	−50		−50		−50		−50		−50		−50		V	V_{DS} = 0, I_G = −1 μA	
2		I_{GSS} Gate Reverse Current (Note 1)		−25		−25		−25		−25		−25		−25	pA	V_{DS} = 0, V_{GS} = −30 V	
3	S	$V_{GS(off)}$ Gate-Source Cutoff Voltage	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	−.5	−2.5	V	V_{DS} = 15 V, I_D = 1 nA	
4	A	$V_{GS(on)}$ Gate-Source Voltage (on)		−2.3		−2.3		−2.3		−2.3		−2.3		−2.3		V_{DG} = 15 V, I_D = 200 μA	
5	C	I_{DSS} Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10 V, V_{GS} = 0	
6		I_G Gate Current (Note 1)		−15		−15		−15		−15		−15		−15	pA	V_{DG} = 15 V,	
7				−10		−10		−10		−10		−10		−10	nA	I_D = 200 μA	T_A = 125°C
8		BV_{G1-G2} Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0, I_G = ±1 μA	
9		g_{fs} Common-Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
10		g_{os} Common-Source Output Conductance		20		20		20		20		20		20			
11	D Y N A M I C	g_{fs} Common-Source Forward Transconductance	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600		V_{DG} = 15 V, I_D = 200 μA	f = 1 kHz
12		g_{os} Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0			
13		C_{iss} Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF		f = 1 MHz
14		C_{rss} Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0			
15		$\overline{e}_N$ Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0	f = 10 Hz
16	M A T C H I N G	CMRR Common-Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	V_{DG} = 10 to 20 V, I_D = 200 μA	
17		$\lvert V_{GS1} - V_{GS2} \rvert$ Differential Gate-Source Voltage		5		10		10		15		20		40	mV	V_{DG} = 10 V, I_D = 200 μA	
18		$\frac{\Delta\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$ Gate-Source Voltage Differential Drift (Note 4)		10		10		25		25		40		80	μV/°C	V_{DG} = 10 V, I_D = 200 μA	T_A = −55°C, T_B = +25°C T_C = +125°C

NOTES
1. Approximately doubles for every 10°C increase in T_A. 2. Pulse test duration = 300 μs, duty cycle ≤ 3%. 3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1} - V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.
4. Measured at end points, T_A, T_B and T_C.

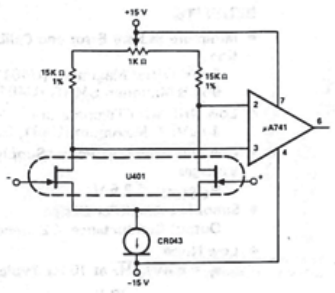
NNR
NRL-D

© 1979 Siliconix Incorporated

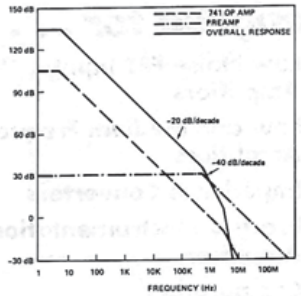
APPLICATIONS

Siliconix

General Purpose FET Input Op Amp



Open Loop Gain and Frequency Response of Op Amp



Typical Specs for General Purpose FET Input Op Amp*

Common Mode Range . . . . . +6.7 to −8.8 Volts
Worst Case Drift Referred to the Input . . ≈ 12 μV/°C
Broad Band Noise Referred to
the Input (0.1 to 1 kHz) . . . . . ≈ 188 nV/Rms
Gain and Bandwidth . . . . . (see graph)

*These specs depend upon the specifications of the Operational amplifier IC used.

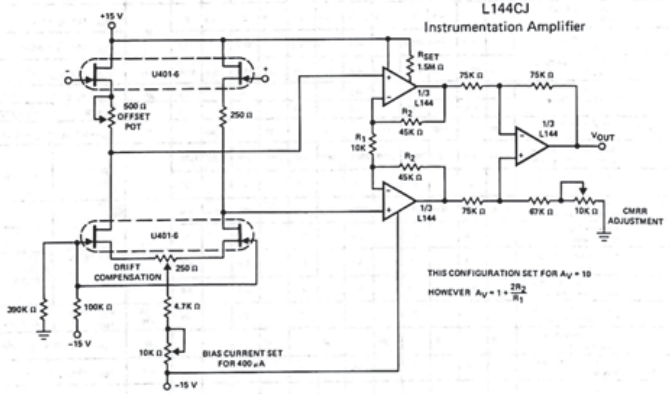
For futher design information, write for:

DESIGNING FET-INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included. (16 pages).

FET Input Instrumentation Amplifier

L144CJ
Instrumentation Amplifier



© 1979 Siliconix incorporated

monolithic dual n-channel JFETs *designed for . . .*

Siliconix

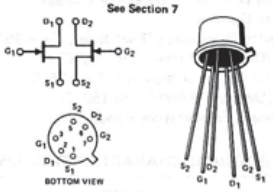
- **FET Input Amplifiers**
- **Low and Medium Frequency Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

Performance Curves NQP See Section 5

BENEFITS

- Low Cost
- Minimum System Error and Calibration
  10 mV Offset Maximum (U410)
  70 dB Minimum CMRR (U410)
- Low Drift with Temperature
  10 μV/°C Maximum (U410)
- Simplifies Amplifier Design
  Low Output Conductance

TO-71
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage . . . . . ±40 V
Gate-Drain or Gate-Source Voltage . . . . . −40 V
Gate Current . . . . . 50 mA
Total Package Dissipation (25°C Free-Air) . . . . . 375 mW
Power Derating . . . . . 3.0 mW/°C
Storage Temperature Range . . . . . −65 to +150°C
Lead Temperature (1/16" from case for 10 seconds) . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U410 Min	U410 Typ	U410 Max	U411 Min	U411 Typ	U411 Max	U412 Min	U412 Typ	U412 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-200			-200			-200	pA	V_{DS} = 0, V_{GS} = -30 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-3.5	-1.0		-3.5	-1.0		-3.5	V	V_{DS} = 20 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			V	V_{DS} = 0 V, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	0.5		5.0	0.5		5.0	0.5		5.0	mA	V_{DS} = 20 V, V_{GS} = 0 V	
5	STATIC	I_G	Gate Current (Note 1)			-200			-200			-200	pA	V_{DG} = 20 V, I_D = 200 μA	
6	STATIC	V_{GS}	Gate-Source Voltage	-0.2		-3.0	-0.2		-3.0	-0.2		-3.0	V		
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1,000		4,000	1,000		4,000	1,000		4,000	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	600		1,200	600		1,200	600		1,200	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
9	DYNAMIC	g_{os}	Common-Source Output Conductance			20			20			20	μmho	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 kHz
10	DYNAMIC	g_{os}	Common-Source Output Conductance			5			5			5	μmho	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4.5			4.5			4.5		pF	V_{DS} = 20 V, V_{GS} = 0 V	f = 1 MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			1.2			1.2		pF		f = 1 MHz
13	DYNAMIC	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage			50			50			50	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, I_D = 200 μA	f = 100 Hz
14	MATCHING	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			20			40	mV	V_{DG} = 20 V, I_D = 200 μA	
15	MATCHING	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Drift (Note 3)			10			25			80	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = 25°C to T_B = 85°C	
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 4)		80			80			70		dB	V_{DD} = 10 V to V_{DD} = 20 V I_D = 200 μA	

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 μsec, duty cycle ≤ 3%.
3. Measured at end points, T_A and T_B.
4. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$, ΔV_{DD} = 10 V.

NQP

© 1979 Siliconix incorporated

Siliconix

monolithic dual n-channel JFETs *designed for . . .*

Siliconix

- **Very High Input Impedance Differential Amplifiers**
  - **Electrometers**
- **Impedance Converters**

Performance Curves NQT See Section 5

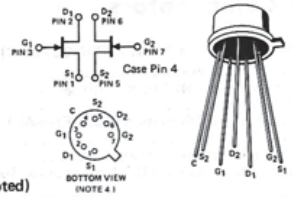
BENEFITS

- High Input Impedance
  I_G = 0.1 pA Maximum (U421-3)
- High Gain g_{fs} = 140 μmho Minimum @ I_D = 30 μA (U421-3)
- Low Power Supply Operation
  $V_{GS(off)}$ = 2 V Maximum (U421-3)
- Minimum System Error and Calibration
  10 mV Maximum Offset
  90 dB Minimum CMRR (U421, U424)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage	±40 V
Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3.2 mW/°C to 150°C)	400 mW
Total Device Dissipation, T_A = 25°C (Derate 6.0 mW/°C to 150°C)	750 mW
Storage Temperature Range	−65 to +150°C

TO-78
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U421-3 Min	U421-3 Typ	U421-3 Max	U424-6 Min	U424-6 Typ	U424-6 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40	−60		−40	−60		V	I_G = −1 μA, V_{DS} = 0	
2		BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40				I_G = −1 μA, I_D = 0, I_S = 0	
3		I_{GSS}	Gate Reverse Current (Note 1)			0.2			1.0	pA	T = +25°C	V_{GS} = −20 V, V_{DS} = 0
						0.5			1.0	nA	T = +125°C	
4		I_G	Gate Operating Current (Note 1)			0.1			0.5	pA	T = +25°C	V_{DG} = 10 V, I_D = 30 μA
						−100			−500		T = +125°C	
5		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.4		−2.0	−0.4		−3.0	V	V_{DS} = 10 V, I_D = 1 nA	
6		V_{GS}	Gate-Source Voltage			−1.8			−2.9		V_{DG} = 10 V, I_D = 30 μA	
7		I_{DSS}	Saturation Drain Current	60		1000	60		1800	μA	V_{DS} = 10 V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	300		800	300		1000	μ℧	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
9		g_{os}	Common-Source Output Conductance			3.0			5.0			
10		C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF		f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5			
12		g_{fs}	Common-Source Forward Transconductance	140		250	135		300	μ℧	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
13		g_{os}	Common-Source Output Conductance			0.5			1.0			
14		$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		20	50		20	70	$nV/\sqrt{Hz}$		f = 10 Hz
					10			10	50			f = 1 kHz
15		NF	Noise Figure			1.0			1.0	dB	f = 10 Hz	R_G = 10M Ω

		Characteristic		U421, 4 Min	U421, 4 Typ	U421, 4 Max	U422, 5 Min	U422, 5 Typ	U422, 5 Max	U423,6 Min	U423,6 Typ	U423,6 Max	Unit	Test Conditions
16	MATCH	$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage			10			15			25	mV	V_{DG} = 10 V, I_D = 30 μA
17		$\frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Differential Gate-Source Voltage Change With Temperature (Note 2)			10			25			40	μV/°C	V_{DG} = 10 V, I_D = 30 μA, T_A = −55°C, T_B = 25°C, T_C = 125°C
18		CMRR	Common Mode Rejection Ratio (Note 3)	90	95		80	90		80	90		dB	I_D = 30 μA, V_{DG} = 10 to 20 V

NOTES
1. Approximately doubles for every 10°C increase in T_A.
2. Measured at end points T_A, T_B and T_C.
3. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta V_{GS1} - V_{GS2}}\right]$ ΔV_{DD} = 10 V
4. Case lead not connected

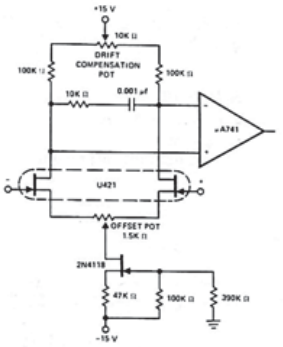
NQT

© 1979 Siliconix incorporated

APPLICATIONS

Siliconix

Very Low Leakage FET Input Op Amps



I_G = 0.1 pA at V_{cm} = 0
Offset = Can be nulled to 0 volts
Drift = Can be nulled to 2 μV/°C
Slew Rate = 0.5 V/μs

NOTE: Pin 4 (case) is isolated from the substrate and should be left floating.

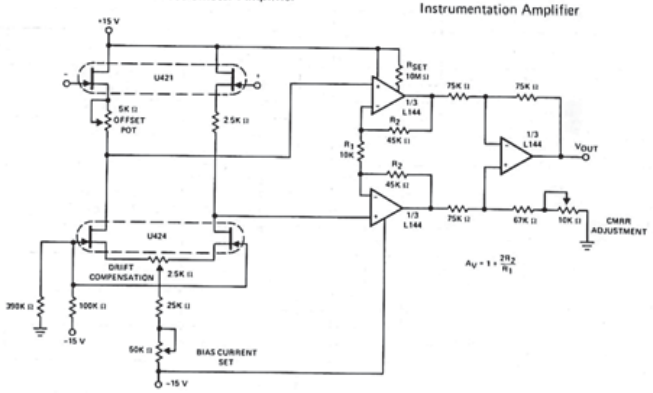
For more information see:

DESIGNING FET INPUT OPERATIONAL AMPLIFIERS (AN74-3)

Describes the advantages of FET input operational amplifiers over their bipolar transistor counterparts. Includes data on noise, leakage current, offset and drift, CMRR and slew rate. Detailed design information and several practical circuits are included.

Electrometer Amplifier

L144CJ
Instrumentation Amplifier



Voltage Gain = 10
Input Current = 0.1 pA
Compensated Drift = 3 μV/°C
Nulled Offset = 0 mV
CMRR = 80 dB typical
Power Consumption = Approx. 30 Volt x 120 μA = 3.6 mW

© 1979 Siliconix incorporated

matched dual n-channel JFETs *designed for . . .*

Siliconix

- **Balanced Mixers**
- **Differential Amplifiers**

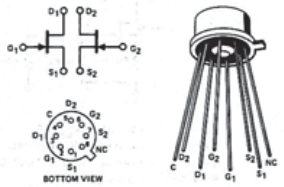
Performance Curves NZA
See Section 5

BENEFITS
- Low Noise Figure
- Low IMD
  30 dBm Intercept Point

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25 V
Gate Current . . . . . 10 mA
Total Continuous Power Dissipation
(or Below) 25°C Free Air Temperature
Derate 4 mW/°C to 150°C. . . . . 500 mW
Continuous Device Dissipation (Each Side) at
(or Below) 25°C Free Air Temperature
Derate 2.4 mW/°C to 150°C . . . . . 300 mW
Storage Temperature Range . . . . . –65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-99
See Section 7



ELECTRICAL CHARACTERISTICS (25° unless otherwise noted)

			Characteristic	U430 Min	U430 Typ	U430 Max	U431 Min	U431 Typ	U431 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current			–150			–150	pA	V_{GS} = –15 V, V_{DS} = 0 V	
2						–150			–150	nA		T = 150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			V	I_G = –1 µA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1.0		–4.0	–2.0		–6.0		V_{DS} = 10 V, I_D = 1 nA	
5		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0		V_{DS} = 0 V, I_G = 10 mA	
6		I_{DSS}	Saturation Drain Current (Note 4)	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0 V	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	10		20	10		20	mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			200			200	µmho		
9		C_{gs}	Gate-Source Capacitance			5.0			5.0	pF	V_{GS} = –10 V, V_{DS} = 0 V	f = 1 MHz
10		C_{gd}	Drain Gate Capacitance			2.5			2.5			
11		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
12	HI FREQ	g_{fs}	Common-Source Forward Transconductance		12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 100 MHz
13		g_{os}	Common-Source Output Conductance		0.15			0.15				
14		g_{ig}	Power-Match Source Admittance		12			12				
15		G_c	Conversion Gain (See Note 1)		3.0			3.0		dB	V_{DS} = 20 V, V_{GS} = 1/2 $V_{GS(off)}$	
16		IMD	Intercept Point (See Notes 1 and 2)		+30			+30		dBm		
17	MATCH	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 3)	0.9		1.0	0.9		1.0		V_{DS} = 10 V	V_G = 0 V
18		$\frac{V_{GS(off)1}}{V_{GS(off)2}}$	Gate-Source Cutoff Voltage Ratio (Note 3)	0.9		1.0	0.9		1.0			I_D = 1 nA
19		$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 3)	0.9		1.0	0.9		1.0			I_D = 10 mA

NZA

NOTES:
1. VHF single-balanced mixer drain load impedance 2k Ω.
2. 2-tone 3rd-order IMD.
3. Assumes smaller value in numerator.
4. Pulse test pulsewidth = 300 µs, duty cycle ≤ 3%.

© 1979 Siliconix Incorporated

matched dual n-channel JFETs *designed for . . .*

Siliconix

- **VHF/UHF Amplifiers**

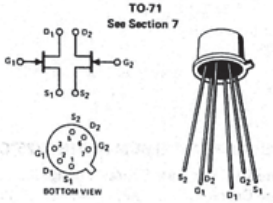
Performance Curves NZF
See Section 5

BENEFITS
- High Gain
  g_{fs} = 4500 µmho Minimum
- Dual Version of J300 with Matched Gate-to-Source Voltage

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-To-Gate Voltage . . . . . ±50 V
Gate-Drain or Gate-Source Voltage . . . . . –25 V
Gate Current . . . . . 50 mA
Total Package Dissipation
(25°C Free-Air Temperature) . . . . . 350 mW
Power Derating . . . . . 2.8 mW/°C
Storage Temperature Range . . . . . –65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

TO-71
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	U440 Min	U440 Typ	U440 Max	U441 Min	U441 Typ	U441 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			–500			–500	pA	V_{DS} = 0, V_{GS} = –15 V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1		–6	–1		–6	V	V_{DS} = 10 V, I_D = 1 nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25				V_{DS} = 0, I_G = –1 µA	
4		I_{DSS}	Saturation Drain Current (Note 2)	6		30	6		30	mA	V_{DS} = 10 V, V_{GS} = 0	
5		I_G	Gate Current (Note 1)			–500			–500	pA	V_{DG} = 10 V, I_D = 5 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500		9,000	4,500		9,000	µmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			200			200			
8		C_{iss}	Common-Source Input Capacitance		3.5			3.5		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8			0.8				
10	MAT	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			20	mV	V_{DG} = 10 V, I_D = 5 mA	

NZF

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 µsec, duty cycle ≤ 3%.

© 1979 Siliconix Incorporated

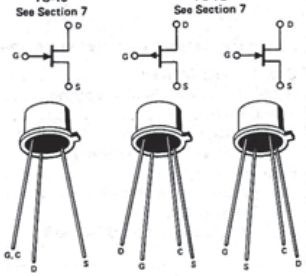
voltage-controlled resistor FETs *designed for . . .*

Siliconix

Performance Curves NC NP NT PC PE See Section 5

- **Small Signal Attenuators**
- **Filters**
- **Amplifier Gain Control**
- **Oscillator Amplitude Control**

TO-18 See Section 7 — TO-72 See Section 7



ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage . . . . . 15 V
Gate Current . . . . . 10 mA
Total Device Dissipation at T_A = 25°C
(Derate at 2.0 mW/°C to 175°C) . . . . . 300 mW
Storage Temperature Range . . . . . −55 to +175°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

N-Channel VCR FETs

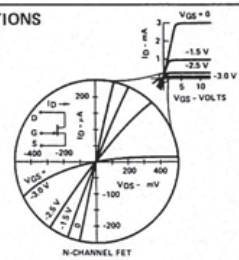
		Characteristic		VCR2N Min	VCR2N Max	VCR4N Min	VCR4N Max	VCR7N Min	VCR7N Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-5		-0.2		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-15		-15		-15		V	I_G = -1 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3.5	-7	-3.5	-7	-2.5	-5	V	I_D = 1 μA, V_{DS} = 10 V	
4	STATIC	$r_{ds(on)}$	Drain Source ON Resistance	20	60	200	600	4,000	8,000	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		7.5		3		1.5	pF	V_{GD} = -10 V, I_S = 0	f = 1 MHz
6	DY	C_{sgo}	Source-Gate Capacitance		7.5		3		1.5	pF	V_{GS} = -10 V, I_D = 0	f = 1 MHz
				NC		NP		NT				

P-Channel VCR FETs

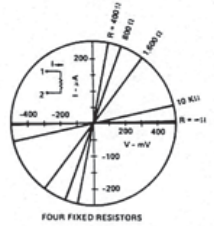
		Characteristic		VCR3P Min	VCR3P Max	VCR5P Min	VCR5P Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		20		10	nA	V_{GS} = 15 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	15		15		V	I_G = 1 μA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	3.5	7	3.5	7	V	I_D = -1 μA, V_{DS} = -10 V	
4	STATIC	$r_{ds(on)}$	Drain-Source ON Resistance	70	200	300	900	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DY	C_{dgo}	Drain-Gate Capacitance		6		3	pF	V_{GD} = 10 V, I_S = 0	f = 1 MHz
6	DY	C_{sgo}	Source-Gate Capacitance		6		3	pF	V_{GS} = 10 V, I_D = 0	f = 1 MHz
				PE		PC				

© 1979 Siliconix incorporated

APPLICATIONS



N-Channel JFET Output Characteristic Enlarged Around V_{DS} = 0
Figure 1



V-I Characteristic of Four Fixed Resistors
Figure 2

The VCR FET has an a-c drain-source resistance, evaluated around V_{DS} = 0, that is controlled by d-c bias voltage V_{GS} applied to the high-impedance gate terminal. Minimum r_{ds} occurs when V_{GS} = 0 and, as V_{GS} approaches the pinch-off voltage, r_{ds} rapidly increases. Comparing Fig. 1 and 2, for $V_{DS} < \pm 0.1$ volt and V_{GS} = constant, the VCR FET has a bilateral characteristic with no offset voltage, just like a fixed resistor. However, when $V_{DS} > \pm 0.1$ volts, the VCR FET characteristic has noticeable curvature.

This series of junction FETs is intended for applications where the drain-source voltage is a low-level a-c signal with no d-c component. Thus the FET operating point will swing symmetrically around V_{DS} = 0. In the first quadrant, signal distortion depends on what extent the FET output characteristic deviates from a straight line or linear relation. Besides the linearity problem in the third quadrant, when V_{GS} is near zero and $v_{ds} > 0.5$ volt rms, the gate-channel junction will become forward biased and cause additional curvature in the characteristic. Also, whenever the gate becomes forward biased due to any combination of V_{GS} and v_{ds}, it ceases to be a high-impedance control terminal for the VCR.

Fig. 3 presents a normalized plot of r_{DS} versus normalized V_{GS} where $V_{GS(off)}$ is defined as that value of V_{GS} at I_D/I_{DSS} = 0.001. The dynamic range of r_{DS} is shown as greater than 100:1. For best control of r_{DS} the normalized V_{GS} should lie between 0 and 0.8 $V_{GS(off)}$ because as V_{GS} approaches $V_{GS(off)}$, r_{DS} increases very rapidly so that r_{ds} control becomes very critical and unit-to-unit matching is almost impossible. In Fig. 4, $r_{ds(on)}$ (drain-source resistance at V_{DS} = V_{GS} = 0) varies as an inverse function of $V_{GS(off)}$. In Fig. 5 r_{ds} has a typical 0.7%/°C temperature coefficient for P-channels which decreases as V_{GS} approaches the zero t.c. point. N-channel devices have a typical 0.3%/°C t.c. specific bias voltage to set operation at the zero t.c. point varies, as does $V_{GS(off)}$, from device to device.*

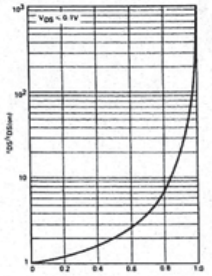


Fig. 3

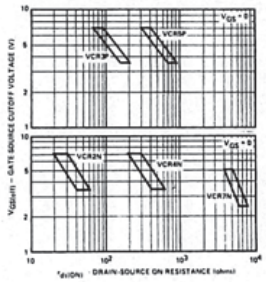


Fig. 4

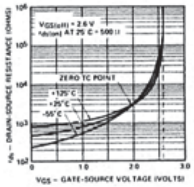


Fig. 5

For further information on using FETs as voltage-variable resistors, consult Siliconix Application Note AN73-1.

* L. Evans; "Biasing FETs for Zero DC Drift"; Electro Technology, August 1964.

© 1979 Siliconix incorporated

data sheets plastic

index 4

n-channel JFET
designed for . . .

- **General Purpose Amplifiers**
- **Analog Switching**

Siliconix

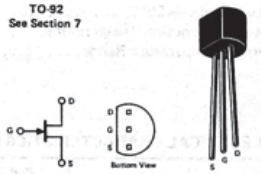
Performance Curves NRL
See Section 5

BENEFITS
- Low Cost
- Specified at 100 MHz
- Automatic Insertion Package

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Drain-Source Voltage . . . . . 25 V
Reverse Gate-Source Voltage. . . . . –25 V
Gate Current. . . . . 10 mA
Continuous Device Dissipation
at (or Below) 25°C Free Air Temperature
(Note 1) . . . . . 200 mW
Storage Temperature Range . . . . . –55°C to +150°C
Lead Temperature
(1/16" from Case for 10 seconds) . . . . . 260°C

TO-92
See Section 7



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –1 μA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current		–2	nA	V_{GS} = –15 V, V_{DS} = 0	
3					–2	μA		T_A = 100°C
4		I_{DSS}	Saturation Drain Current	2	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 2)	
5		V_{GS}	Gate-Source Voltage	–0.5	–7.5	V	V_{DS} = 15 V, I_D = 200 μA	
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–8	V	V_{DS} = 15 V, I_D = 2 nA	
7	DYNAMIC	$\lvert y_{fs} \rvert$	Common-Source Forward Transfer Admittance	2000	6500	μmho	V_{DS} = 15 V, V_{GS} = 0 (Note 2)	f = 1 kHz
8		$\lvert y_{os} \rvert$	Common Source Output Admittance		50	μmho		
9		C_{iss}	Common Source Input Capacitance		8	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
10		C_{rss}	Common Source Reverse Transfer Capacitance		4	pF		
11		$\lvert y_{fs} \rvert$	Common Source Forward Transfer Admittance	1600		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz

*JEDEC registered data

NRL

NOTES:

1. Derate linearly to 125°C (free air temperature at a rate of 2 mW/°C).
2. Pulse tested pulse width = 100 ms, duty cycle ≤ 10%.

© 1979 Siliconix Incorporated

n-channel JFETs
designed for . . .

- **General Purpose Amplifiers**
- **Switches**

Siliconix

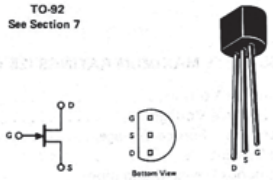
Performance Curves NRL
See Section 5

BENEFITS
- Low Cost
- Automated Insertion Package

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Source Voltage	25 V
Drain-Gate Voltage	25 V
Source-Gate Voltage	25 V
Total Device Dissipation at 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature	135°C
Storage Temperature Range	-65 to +150°C

TO-92
See Section 7



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5457 Min	2N5457 Typ	2N5457 Max	2N5458 Min	2N5458 Typ	2N5458 Max	2N5459 Min	2N5459 Typ	2N5459 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-.01	-1.0		-.01	-1.0		-.01	-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
2						-200			-200			-200			T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25	-60		-25	-60		-25	-60		V	I_G = -10 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5		-6.0	-1.0		-7.0	-2.0		-8.0		V_{DS} = 15 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current	1.0		5.0	2.0		9.0	4.0		16	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	$\|y_{fs}\|$	Common-Source Forward Transconductance	1,000		5,000	1,500		5,500	2,000		6,000	µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		y_{os}	Common-Source Output Conductance		10	50		15	50		20	50			
8		C_{iss}	Common-Source Input Capacitance		4.5	7.0		4.5	7.0		4.5	7.0	pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	3.0		1.0	3.0		1.0	3.0			
10		NF	Noise Figure		.04	3.0		.04	3.0		.04	3.0	dB	V_{DS} = 15 V, V_{GS} = 0 R_G = 1 MΩ, NBW = 1 Hz	f = 1 kHz

*JEDEC registered data

NOTE:
1. Pulse test pulsewidth = 2 ms.

NRL

© 1979 Siliconix incorporated

n-channel JFETs
designed for . . .

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**
- **Analog Switches**

Siliconix

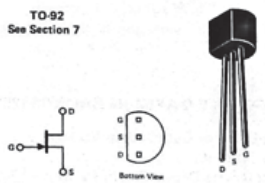
Performance Curves NH
See Section 5

BENEFITS
- Low Cost
- Completely Specified for 400 MHz Operation
- Low Error Analog Switch
  Very Little Charge Coupling
  C_{rss} < 1.0 pF

*ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage	25 V
Source Gate Voltage	25 V
Drain Current	30 mA
Forward Gate Current	10 mA
Total Device Dissipation @ 25°C	360 mW
Derate above 25°C	3.27 mW/°C
Operating Junction Temperature Range	-65 to +135°C
Storage Temperature Range	-65 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	240°C

TO-92
See Section 7



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N5484 Min	2N5484 Max	2N5485 Min	2N5485 Max	2N5486 Min	2N5486 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	V_{GS} = -20 V, V_{DS} = 0	
2					-200		-200		-200			T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25		-25		-25		V	I_G = -1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3	-3.0	-0.5	-4.0	-2.0	-6.0		V_{DS} = 15 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current	1.0	5.0	4.0	10	8.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	$\|y_{fs}\|$	Common-Source Forward Transconductance	3,000	6,000	3,500	7,000	4,000	8,000	µmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		y_{os}	Common-Source Output Conductance		50		60		75			
8		$Re(y_{fs})$	Common-Source Forward Transconductance	2,500								f = 100 MHz
9						3,000		3,500				f = 400 MHz
10		$Re(y_{os})$	Common-Source Output Conductance		75							f = 100 MHz
11							100		100			f = 400 MHz
12		$Re(y_{is})$	Common-Source Input Conductance		100							f = 100 MHz
13							1,000		1,000			f = 400 MHz
14		C_{iss}	Common-Source Input Capacitance		5.0		5.0		5.0	pF		f = 1 MHz
15		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0		1.0		1.0			
16		C_{oss}	Common-Source Output Capacitance		2.0		2.0		2.0			
17		NF	Noise Figure		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1 MΩ	f = 1 kHz
18					3.0						V_{DS} = 15 V, I_D = 1 mA, R_G = 1 kΩ	
19							2.0		2.0		V_{DS} = 15 V, I_D = 4 mA, R_G = 1 kΩ	f = 100 MHz
20							4.0		4.0			f = 400 MHz
21		G_{ps}	Common-Source Power Gain	16	25						V_{DS} = 15 V, I_D = 1 mA	f = 100 MHz
22						18	30	18	30		V_{DS} = 15 V, I_D = 4 mA	
23						10	20	10	20			f = 400 MHz

* JEDEC registered data

NOTE:
1 Pulse Test PW 300 µs, duty cycle ≤ 3%

NH

© 1979 Siliconix incorporated

n-channel JFET
designed for . . .

Siliconix

Performance Curves NH
See Section 5

- **Analog Switches**
- **Choppers**
- **Commutators**

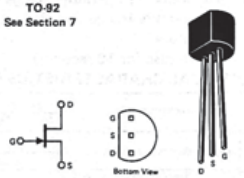
BENEFITS

- Low Cost
- Automatic Insertion Package
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
- Low Charge Coupling from Driver to Load
  C_{rss} = 0.8 pF Typically

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Gate-Drain or Gate-Source Voltage . . . . . –25 V
Gate Current . . . . . 10 mA
Total Device Dissipation at (or Below) T_A = 25°C . . 360 mW
(Derate 3.28 mW/°C to 135°C)
Operating Temperature Range. . . . . –55 to +135°C
Storage Temperature Range . . . . . –65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .240°C

TO-92
See Section 7



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

			Characteristic	Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–1.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–0.2	µA		T_A = 100°C
3		I_{DGO}	Drain Leakage Current		1.0	nA	V_{DG} = 15 V, I_S = 0	
4					0.2	µA		T_A = 100°C
5		$I_{D(off)}$	Drain Cutoff Current		10	nA	V_{DS} = 12 V, V_{GS} = –10 V	
6					2.0	µA		T_A = 100°C
7		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –10 µA, V_{DS} = 0	
8		$V_{GS(f)}$	Gate-Source Forward Voltage		1.0		I_G = 1 mA, V_{DS} = 0	
9		$V_{DS(on)}$	Drain-Source ON Voltage		1.5		I_D = 7 mA, V_{GS} = 0	
10		$r_{DS(on)}$	Static Drain-Source ON Resistance		150	Ω	I_D = 0.1 mA, V_{GS} = 0	
11		I_{DSS}	Saturation Drain Current	15		mA	V_{DS} = 15 V, V_{GS} = 0	
12	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		150	Ω	I_D = 0, V_{GS} = 0	f = 1 kHz
13		C_{iss}	Common-Source Input Capacitance		5.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		V_{DS} = 0, V_{GS} = –10 V	
15	SWITCH	$t_{d(on)}$	Turn ON Delay Time		5	ns	V_{DD} = 10 V, $I_{D(on)}$ = 7 mA, R_L = 1.21K Ω $V_{GS(on)}$ = 0, $V_{GS(off)}$ = –10 V	
16		t_r	Rise Time		5			
17		$t_{d(off)}$	Turn OFF Delay Time		15			
18		t_f	Fall Time		10			

*JEDEC registered data

NH

© 1979 Siliconix Incorporated

n-channel JFETs
designed for . . .

Siliconix

Performance Curves NC
See Section 5

- **Analog Switches**
- **Commutators**
- **Choppers**

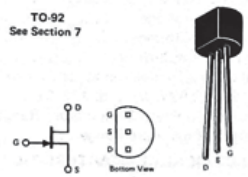
BENEFITS

- Low Cost
- Industry Standard Package
- Automatic Insertion Package
- Fast Switching
  t_{rise} < 5 ns (2N5638)
- Low Insertion Loss
  $R_{DS(on)}$ < 30 Ω (2N5638)
- Short Sample and Hold Aperture Time
  C_{rss} < 4 pF

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Drain-Source Breakdown Voltage . . . . . 30 V
Drain-Gate Breakdown Voltage . . . . . 30 V
Source-Gate Breakdown Voltage . . . . . 30 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation at T_{LEAD} = 25°C . . . . . 625 mW
Derate above 25°C . . . . . 5.68 mW/°C
Operating Junction Temperature Range . . . . . –65 to +135°C
Storage Temperature Range . . . . . –65 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . .300°C

TO-92
See Section 7

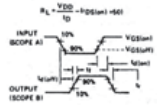


***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

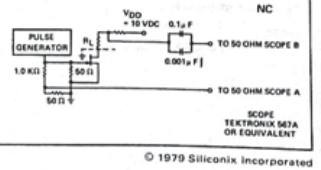
			Characteristic	2N5638 Min	2N5638 Max	2N5639 Min	2N5639 Max	2N5640 Min	2N5640 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -10 µA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current		-1.0		-1.0		-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
3					-1.0		-1.0		-1.0	µA		T_A = +100°C
4		$I_{D(off)}$	Drain Cutoff Current		1.0		1.0		1.0	nA	V_{DS} = 15 V, V_{GS} = -12 V (2N5638)	
5					1.0		1.0		1.0	µA	V_{GS} = -8 V (2N5639), V_{GS} = -6 V (2N5640)	T_A = +100°C
6		I_{DSS}	Saturation Drain Current	50		25		5.0		mA	V_{DS} = 20 V, V_{GS} = 0 (Note 1)	
7		$V_{DS(on)}$	Drain-Source ON Voltage		0.5		0.5		0.5	V	V_{GS} = 0, I_D = 12 mA (2N5638), I_D = 6 mA (2N5639), I_D = 3 mA (2N5640)	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	I_D = 1 mA, V_{GS} = 0	
9	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		V_{GS} = 0, I_D = 0	f = 1 kHz
10		C_{iss}	Common-Source Input Capacitance		10		10		10	pF	V_{GS} = -12 V, V_{DS} = 0	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
12	SWITCH	$t_{d(on)}$	Turn-On Delay Time		4.0		6.0		8.0	nsec	V_{DD} = 10 V $I_{D(on)}$ = 12 mA (2N5638) R_L = 800 Ω (2N5638)	
13		t_r	Rise Time		5.0		8.0		10		$V_{GS(on)}$ = 0 $I_{D(on)}$ = 6 mA (2N5639) R_L = 1.6k Ω (2N5639)	
14		$t_{d(off)}$	Turn-OFF Delay Time		5.0		10		15		$V_{GS(off)}$ = -10 V $I_{D(on)}$ = 3 mA (2N5640) R_L = 3.2k Ω (2N5640)	
15		t_f	Fall Time		10		20		30			

* JEDEC registered data

NOTE:
1 Pulse test PW ≤ 300 µsec, duty cycle ≤ 3.0%



NC



© 1979 Siliconix Incorporated

n-channel JFETs
designed for . . .

Siliconix

Performance Curves NC
See Section 5

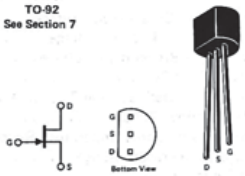
- **Analog Switches**
- **Commutators**
- **Choppers**

BENEFITS
- Low Cost
- Automatic Insertion Package
- High Speed
  $t_{ON} + t_{OFF}$ = 24 ns Max (2N5653)
- Low Insertion Loss
  $R_{DS(on)}$ = 50 Ω Max (2N5653)

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Drain-Source Voltage . . . . . 30 V
Drain-Gate Voltage . . . . . 30 V
Source-Gate Voltage . . . . . 30 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation at (or Below) T_A = 25°C
(Derate 2.82 mW/°C to 135°C) . . . . . 360 mW
Operating Junction Temperature Range . . . . . −65 to +135°C
Storage Temperature Range . . . . . −65 to +150°C

TO-92
See Section 7

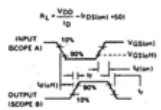


***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

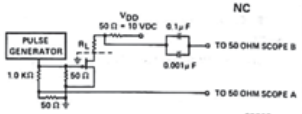
			Characteristic	2N5653 Min	2N5653 Max	2N5654 Min	2N5654 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−30		−30		V	I_G = −10 μA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current		−1.0		−1.0	nA	V_{GS} = −15 V, V_{DS} = 0	
3					−1.0		−1.0	μA		T_A = +100°C
4		$I_{D(off)}$	Drain Cutoff Current		1.0		1.0	nA	V_{DS} = 15 V, V_{GS} = −12 V (2N5653)	
5					1.0		1.0	μA	V_{GS} = −8 V (2N5654)	T_A = +100°C
6		I_{DSS}	Saturation Drain Current	40		15		mA	V_{DS} = 20 V, V_{GS} = 0 (Note 1)	
7		$V_{DS(on)}$	Drain-Source ON Voltage		0.75		0.75	V	V_{GS} = 0, I_D = 10 mA (2N5653), I_D = 5 mA (2N5654)	
8		$r_{DS(on)}$	Static Drain-Source ON Resistance		50		100	Ω	I_D = 1 mA, V_{GS} = 0	
9		$r_{ds(on)}$	Drain-Source ON Resistance		50		100		V_{GS} = 0, I_D = 0	f = 1 kHz
10	DYN	C_{iss}	Common-Source Input Capacitance		10		10	pF	V_{GS} = −12 V, V_{DS} = 0	f = 1 MHz
11		C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5			
12	SW	$t_{d(on)}$	Turn-ON Delay Time		4.0		6.0	nsec	V_{DD} = 10 V, $I_{D(on)}$ = 10 mA (2N5653)	
13		t_r	Rise Time		5.0		8.0		$V_{GS(on)}$ = 0, $I_{D(on)}$ = 5 mA (2N5654)	
14		$t_{d(off)}$	Turn-OFF Delay Time		5.0		10		$V_{GS(off)}$ = −12 V, R_L = 925 Ω (2N5653)	
15		t_f	Fall Time		10		20		R_L = 1.85K Ω (2N5654)	

*JEDEC registered data

NOTE:
1. Pulse test PW < 300 μs, duty cycle < 3%.



NC



© 1979 Siliconix Incorporated

n-channel JFETs
designed for . . .

Siliconix

Performance Curves NH
See Section 5

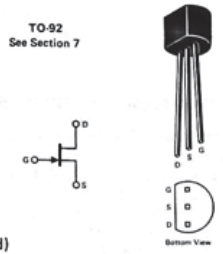
- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

BENEFITS
- Low Cost
- Automatic Insertion Package
- Specified for 100 MHz Operation

***ABSOLUTE MAXIMUM RATINGS (25°C)**

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage . . . . . 25 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . −55 to 135°C
Storage Temperature Range . . . . . −55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 7



***ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)**

			Characteristic	2N5668 Min	2N5668 Max	2N5669 Min	2N5669 Max	2N5670 Min	2N5670 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−2.0		−2.0		−2.0	nA	V_{GS} = −15 V, V_{DS} = 0	
2					−2.0		−2.0		−2.0	μA		T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−25		−25		−25		V	I_G = −10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.2	4.0	1.0	6.0	2.0	8.0		V_{DS} = 15 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current	1.0	5.0	4.0	10	8.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1500	6500	2000	6500	3000	7500	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		20		50		75			
8		$Re_{(y_{fs})}$	Common-Source Forward Transconductance	1000		1600		2500				f = 100 MHz
9		$Re_{(y_{os})}$	Common-Source Output Conductance		50		100		150			
10		$Re_{(y_{is})}$	Common-Source Input Conductance		800		800		800			
11		C_{iss}	Common-Source Input Capacitance		7.0		7.0		7.0	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0			
13		C_{oss}	Common-Source Output Capacitance		4.0		4.0		4.0			
14		NF	Noise Figure		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1K Ω	f = 100 MHz
15		G_{ps}	Common-Source Power Gain	16		16		16			V_{DS} = 15 V, V_{GS} = 0	

*JEDEC registered data

NOTE:
1. Pulse test PW = 300 μs, duty cycle < 3%.

NH

© 1979 Siliconix Incorporated

Siliconix

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**

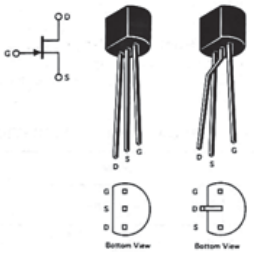
Siliconix

Performance Curves NVA
See Section 5

BENEFITS

- Very Low Insertion Loss
  $R_{DS(on)} < 3\ \Omega$ (J105)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver

TO-92
See Section 7



(-18)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J105 Min	J105 Typ	J105 Max	J106 Min	J106 Typ	J106 Max	J107 Min	J107 Typ	J107 Max	Unit	Test Conditions
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{DS} = 0 V, V_{GS} = -15 V
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-4.5		-10	-2		-6	-0.5		-4.5	V	V_{DS} = 5 V, I_D = 1 µA
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				V_{DS} = 0 V, I_G = -1 µA
4		I_{DSS}	Drain Saturation Current (Note 2)	500			200			100			mA	V_{DS} = 15 V, V_{GS} = 0 V
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	V_{DS} = 5 V, V_{GS} = -10 V
6		$r_{DS(on)}$	Drain Source ON Resistance			3			6			8	Ω	$V_{DS} \leq 0.1$ V, V_{GS} = 0 V
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			35			35			35	pF	V_{DS} = 0 V, V_{GS} = -10 V; f = 1 MHz
8		$C_{sg(off)}$	Source Gate OFF Capacitance			35			35			35		
9		$C_{dg(on)}$ + $C_{sg(on)}$	Drain Gate plus Source Gate ON Capacitance			160			160			160		V_{DS} = V_{GS} = 0 V; f = 1 MHz
10		$t_{d(on)}$	Turn On Delay Time		15			15			15		ns	Switching Time Test Conditions
11		t_r	Rise Time		20			20			20			
12		$t_{d(off)}$	Turn Off Delay Time		15			15			15			
13		t_f	Fall Time		20			20			20			

Switching Time Test Conditions	J105	J106	J107
V_{DD}	1.5 V	1.5 V	1.5 V
$V_{GS(off)}$	-12 V	-7 V	-5 V
R_L	50 Ω	50 Ω	50 Ω

NVA

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 µs, duty cycle ≤ 3%.

© 1979 Siliconix incorporated

n-channel JFETs *designed for . . .*

- **Analog Switches**
- **Choppers**
- **Commutators**
- **Low Noise Audio Amplifiers**

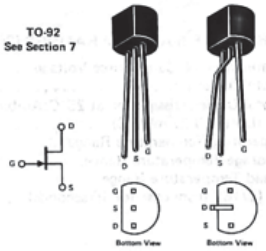
Siliconix

Performance Curves NIP
See Section 5

BENEFITS

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $R_{DS(on)} < 8\ \Omega$ (J108)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{D(on)} + t_r$ = 5 ns Typical
- Low Noise
  $\overline{e_n}$ = 6 nV/√Hz at 10 Hz, Typ (J110)

TO-92
See Section 7



(-18)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J108 Min	J108 Typ	J108 Max	J109 Min	J109 Typ	J109 Max	J110 Min	J110 Typ	J110 Max	Unit	Test Conditions
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-3			-3			-3	nA	V_{DS} = 0 V, V_{GS} = -15 V
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3		-10	-2		-6	-0.5		-4	V	V_{DS} = 5 V, I_D = 1 µA
3		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25				V_{DS} = 0 V, I_G = -1 µA
4		I_{DSS}	Drain Saturation Current (Note 2)	80			40			10			mA	V_{DS} = 15 V, V_{GS} = 0 V
5		$I_{D(off)}$	Drain Cutoff Current (Note 1)			3			3			3	nA	V_{DS} = 5 V, V_{GS} = -10 V
6		$r_{DS(on)}$	Drain-Source ON Resistance			8			12			18	Ω	$V_{DS} \leq 0.1$ V, V_{GS} = 0 V
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance			15			15			15	pF	V_{DS} = 0 V, V_{GS} = -10 V; f = 1 MHz
8		$C_{sg(off)}$	Source-Gate OFF Capacitance			15			15			15		
9		$C_{dg(on)}$ + $C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			85			85			85		V_{DS} = V_{GS} = 0; f = 1 MHz
10		$t_{d(on)}$	Turn ON Delay Time		4			4			4		ns	Switching Time Test Conditions
11		t_r	Rise Time		1			1			1			
12		$t_{d(off)}$	Turn OFF Delay Time		6			6			6			
13		t_f	Fall Time		30			30			30			

Switching Time Test Conditions	J108	J109	J110
V_{DD}	1.5 V	1.5 V	1.5 V
$V_{GS(off)}$	-12 V	-7 V	-5 V
R_L	150 Ω	150 Ω	150 Ω

NIP

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 µs; duty cycle ≤ 3%.

© 1979 Siliconix incorporated

n-channel FETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NC
See Section 5

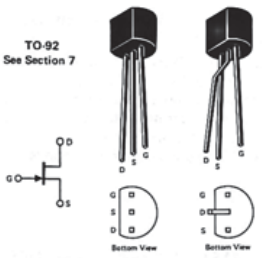
BENEFITS

- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  $R_{DS(on)} < 30\ \Omega$ (J111)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Fast Switching
  $t_{D(on)} + t_r = 13$ ns Typical
- Short Sample and Hold Aperture Time
  $C_{gd(off)} < 5$ pF
  $C_{gs(off)} < 5$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –35V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 7



(-18)

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J111 Min	J111 Typ	J111 Max	J112 Min	J112 Typ	J112 Max	J113 Min	J113 Typ	J113 Max	UNIT	Test Conditions
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-1			-1			-1	nA	$V_{DS} = 0$ V, $V_{GS} = -15$ V
2	STATIC	$V_{GS(off)}$	Gate Source Cutoff Voltage	3		-10	-1		-5	-0.5		-3	V	$V_{DS} = 5$ V, $I_D = 1$ µA
3	STATIC	BV_{GSS}	Gate Source Breakdown Voltage	35			35			-35			V	$V_{DS} = 0$ V, $I_G = -1$ µA
4	STATIC	I_{DSS}	Drain Saturation Current (Note 2)	20			5			2			mA	$V_{DS} = 15$ V, $V_{GS} = 0$ V
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			-1			-1			-1	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V
6	STATIC	$r_{DS(on)}$	Drain Source ON Resistance			30			50			100	Ω	$V_{DS} = 0.1$ V, $V_{GS} = 0$ V
7	DYNAMIC	$C_{dg(off)}$	Drain Gate OFF Capacitance			5			5			5	pF	$V_{DS} = 0$ V, $V_{GS} = -10$ V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source Gate OFF Capacitance			5			5			5	pF	$V_{DS} = 0$ V, $V_{GS} = -10$ V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance			28			28			28	pF	$V_{DS} = V_{GS} = 0$; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		7			7			7		ns	Switching Time Test Conditions
11	DYNAMIC	t_r	Rise Time		6			6			6		ns	
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		20			20			20		ns	
13	DYNAMIC	t_f	Fall Time		15			15			15		ns	

Switching Time Test Conditions	J111	J112	J113
V_{DD}	10 V	10 V	10 V
$V_{GS(off)}$	-12 V	-7 V	-5 V
R_L	800 Ω	1,600 Ω	3,200 Ω

NC

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300 µs; duty cycle ≤ 3%.

© 1979 Siliconix incorporated

n-channel JFET *designed for . . .*

Siliconix

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves NZF
See Section 5

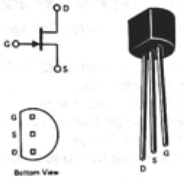
BENEFITS

- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Very Fast Switching
  $t_{D(on)} + t_r = 6$ ns Typical
- Short Sample and Hold Aperture Time
  $C_{gd(off)} < 2$ pF
  $C_{gs(off)} < 2$ pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J114 Min	J114 Typ	J114 Max	Unit	Test Conditions
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-1	nA	$V_{DS} = 0$, $V_{GS} = -15$ V
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3		-10	V	$V_{DS} = 5$ V, $I_D = 1$ µA
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25			V	$V_{DS} = 0$, $I_G = -1$ µA
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	15			mA	$V_{DS} = 15$ V, $V_{GS} = 0$
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			1	nA	$V_{DS} = 5$ V, $V_{GS} = -10$ V
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance			150	Ω	$V_{DS} \leq 0.1$ V, $V_{GS} = 0$
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance			2	pF	$V_{DS} = 0$, $V_{GS} = -10$ V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source-Gate OFF Capacitance			2	pF	$V_{DS} = 0$, $V_{GS} = -10$ V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			8	pF	$V_{DS} = V_{GS} = 0$; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		3		ns	Switching Time Test Conditions
11	DYNAMIC	t_r	Rise Time		3		ns	
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		12		ns	
13	DYNAMIC	t_f	Fall Time		8		ns	

Switching Time Test Conditions
$V_{DD} = 10$ V, $V_{GS(off)} = -12$ V
$R_L = 1$ KΩ, $V_{GS(on)} = 0$

NZF

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 µs; duty cycle ≤ 3%

© 1979 Siliconix incorporated

p-channel JFETs *designed for . . .*

Siliconix

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves PS
See Section 5

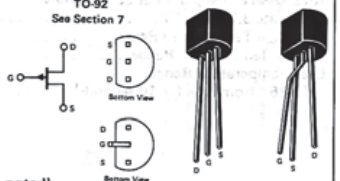
BENEFITS

- Low Cost
- Simplifies Series-Shunt Switching when when Combined with J113, its N-Chan-Channel Complement
- Low Insertion Loss
  $R_{DS(on)} < 85\ \Omega$ (J174)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
  $C_{sg(off)} < 5.5$ pF
  $C_{dg(off)} < 5.5$ pF
- Fast Switching
  $t_{d(on)} + t_r = 7$ ns Typical

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristics		J174 Min	J174 Typ	J174 Max	J175 Min	J175 Typ	J175 Max	J176 Min	J176 Typ	J176 Max	J177 Min	J177 Typ	J177 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			1			1			1			1	nA	V_{DS} = 0, V_{GS} = 20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	V_{DS} = -15 V, I_D = -10 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30			30			30			30			V	V_{DS} = 0, I_G = 1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	-20		-100	-7		-60	-2		-25	-1.5		-20	mA	V_{DS} = -15 V, V_{GS} = 0	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 2)			-1			-1			-1			-1	nA	V_{DS} = -15 V, V_{GS} = 10 V	
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance			85			125			250			300	Ω	V_{GS} = 0, V_{DS} = -0.1 V	
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10 V	f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10 V	f = 1 MHz
9	DYNAMIC	$C_{dg(on)}$ + $C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance		32			32			32			32		pF	V_{DS} = V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions	
11	DYNAMIC	t_r	Rise Time		5			10			20			25		ns		
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		5			10			15			20		ns		
13	DYNAMIC	t_f	Fall Time		10			20			20			25		ns		

Switching Time Test Conditions	J174	J175	J176	J177
V_{DD}	-10 V	-6 V	-6 V	-6 V
$V_{GS(off)}$	12 V	8 V	6 V	3 V
R_L	560 Ω	1.2 KΩ	5.6 KΩ	10 KΩ
$V_{GS(on)}$	0 V	0 V	0 V	0 V

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A
3. Pulse test duration = 300 μs, duty cycle ≤ 3%.

PS

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

- **General Purpose Amplifiers**

Performance Curves NP
See Section 5

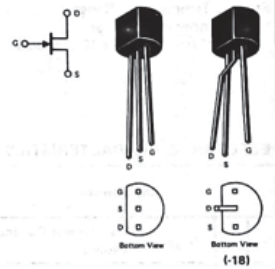
BENEFITS

- High Input Impedance
  I_G = 35 pA Typical
- Good for Low Power Supply Operation
  $V_{GS(off)} < 1.5$ V (J201)

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . –40 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J201 Min	J201 Typ	J201 Max	J202 Min	J202 Typ	J202 Max	J203 Min	J203 Typ	J203 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			-100			-100			-100	pA	V_{DS} = 0, V_{GS} = -20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.3		-1.5	-0.8		-4.0	-2.0		-10.0	V	V_{DS} = 20 V, I_D = 10 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	0.2		1.0	0.9		4.5	4.0		20	mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		-35			-35			-35		pA	V_{DG} = 20 V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	500			1,000			1,500			μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance		1			3.5			10		μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4			4			4		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$\overline{e_n}$	Equivalent Short-Circuit Input Noise Voltage		5			5			5		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

NP

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

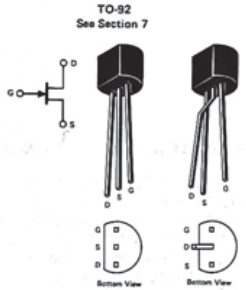
■ General Purpose Switching

Performance Curves NP
See Section 5

BENEFITS

- Very Low Leakage

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . –25V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J204 Min	J204 Typ	J204 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			–100	pA	V_{DS} = 0, V_{GS} = –20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5		–2.0	V	V_{DS} = 20 V, I_D = 10 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25			V	V_{DS} = 0, I_G = –1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)		1.2		mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		–35		pA	V_{DG} = 20 V, I_D = 200 μA	
6	DYNAMIC	g_{fs}	Common Source Forward Transconductance (Note 3)		1500		μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance		2.5		μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz

NP

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

© 1979 Siliconix incorporated

n-channel JFETs *designed for . . .*

Siliconix

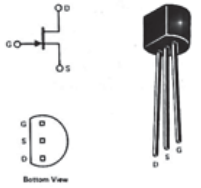
■ General Purpose Amplifiers

Performance Curves NZF
See Section 5

BENEFITS

- High Gain
  G_{FS} = 7000 μmho Minimum
  (J211, J212)
- High Input Impedance
  I_{GSS} = 100 pA Maximum
  C_{iss} = 5 pF Typical

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25 V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J210 Min	J210 Typ	J210 Max	J211 Min	J211 Typ	J211 Max	J212 Min	J212 Typ	J212 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			–100			–100			–100	pA	V_{DS} = 0, V_{GS} = –15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1		–3	–2.5		–4.5	–4		–6	V	V_{DS} = 15 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25			V	V_{DS} = 0, I_G = –1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	2		15	7		20	15		40	mA	V_{DS} = 15 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 1)		–10			–10			–10		pA	V_{DG} = 10 V, I_D = 1 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,000		12,000	7,000		12,000	7,000		12,000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance			150			200			200	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4			4			4		pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1		pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz

NZF

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

© 1979 Siliconix incorporated

n-channel JFETs designed for . . .

Siliconix

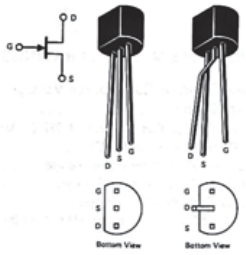
■ Audio and Sub-Audio Amplifiers

Performance Curves NS See Section 5

BENEFITS

- Ultra Low Noise
  $\overline{e_n}$ = 8 nV/√Hz Typical at 10 Hz
  $\overline{e_n}$ = 2 nV/√Hz Typical at 1 kHz

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) . . . . . –40V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J230 Min	J230 Typ	J230 Max	J231 Min	J231 Typ	J231 Max	J232 Min	J232 Typ	J232 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			-250			-250			-250	pA	V_{DS} = 0, V_{GS} = -30 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-3	-2		-5	-4		-6	V	V_{DS} = 20 V, I_D = 1 µA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-40			-40			-40			V	V_{DS} = 0, I_G = -1 µA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	0.7		3	2		6	5		10	mA	V_{DS} = 20 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		-10			-10			-10		pA	V_{DG} = 10 V, I_D = 0.5 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1,000		2,500	1,500		3,000	2,500		4,000	µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance			2			4			6	µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		12			12			12		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		2			2			2		pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
10	DYNAMIC	$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		8	30		8	30		8	30	nV/√Hz	V_{DS} = 10 V, V_{GS} = 0	f = 10 Hz
11	DYNAMIC	$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		2			2			2		nV/√Hz	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz

NS

NOTES:
1. Geometry is symmetrical. Unit may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

© 1979 Siliconix incorporated

p-channel JFETs designed for . . .

Siliconix

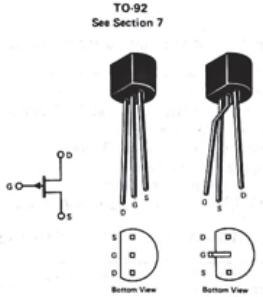
■ General Purpose Amplifiers

Performance Curves PS See Section 5

BENEFITS

- Low Cost
- Automatic Insertion Package
- High Gain Amplifiers
  g_{fs} = 14,000 µmho Typical (J271)
- Low Noise
  $\overline{e_n}$ = 6 nV/√Hz at 1 kHz Typical

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate Source Voltage (Note 1) . . . . . 30 V
Gate Current . . . . . –50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J270 Min	J270 Typ	J270 Max	J271 Min	J271 Typ	J271 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			200			200	pA	V_{DS} = 0, V_{GS} = 20 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.5		2.0	1.5		4.5	V	V_{DS} = -15 V, I_D = -1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30			30			V	V_{DS} = 0, I_G = 1 µA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	-2		-15	-6		-50	mA	V_{DS} = -15 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 2)		15			60		pA	V_{DG} = -15 V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	6,000		15,000	8,000		18,000	µmho	V_{DS} = -15 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance			200			500	µmho	V_{DS} = -15 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		32			32		pF	V_{DS} = -15 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		4			4		pF	V_{DS} = -15 V, V_{GS} = 0	f = 1 MHz
10	DYNAMIC	e_n	Equivalent Short-Circuit Input Noise Voltage		6			6		nV/√Hz	V_{DS} = -10 V, I_D = $I_{DSS(min)}$	f = 1 kHz

PS

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

© 1979 Siliconix Incorporated

n-channel JFETs designed for . . .

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

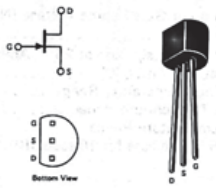
Siliconix

Performance Curves NZF See Section 5

BENEFITS

- **High Power Gain**
  20–23 dB Typical at 100 MHz, Common-Source
  17.5–20.5 dB Typical at 100 MHz, Common-Gate
- **Low Noise Figure**
  1.3 dB Typical at 100 MHz
- **High Dynamic Range**
  Greater than 100 dB

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25 V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–0.5	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–0.1	μA		T_A = 125°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage (Note 1)	–1.5	–7.0		V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1, 2)	4	45	mA	V_{DS} = 10 V, V_{GS} = 0	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	4500	9000	μmho	V_{DS} = 10 V, I_D = 5 mA, f = 1 kHz	
7		g_{os}	Common-Source Output Conductance		200			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.7	pF	V_{DG} = 10 V, I_D = 5 mA, f = 1 MHz	
9		C_{iss}	Common-Source Input Capacitance		5.5			

NOTES:
1. I_{DSS} and $V_{GS(off)}$ are selected into 5 ranges and labeled according to above table.
2. Pulse test PW < 300 μs, duty cycle < 3%.

NZF

© 1979 Siliconix incorporated

n-channel JFETs designed for . . .

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

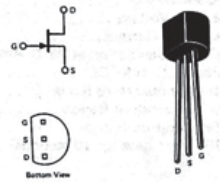
Siliconix

Performance Curves NH See Section 5

BENEFITS

- **Characterized for Operation at 100 and 400 MHz**
- **Low Noise**
  NF = 1.7 dB Typical at 100 MHz

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –30 V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J304 Min	J304 Typ	J304 Max	J305 Min	J305 Typ	J305 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			–100			–100	pA	V_{DS} = 0, V_{GS} = –20 V	
2		$V_{GS(off)}$	Gate Source Cutoff Voltage	–2		–6	–0.5		–3	V	V_{DS} = 15 V, I_D = 1 nA	
3		BV_{GSS}	Gate Source Breakdown Voltage	–30			–30				V_{DS} = 0, I_G = –1 μA	
4		I_{DSS}	Saturation Drain Current (Note 2)	5		15	1		8	mA	V_{DS} = 15 V, V_{GS} = 0	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,500		7,500	3,000			μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
6		g_{os}	Common-Source Output Transconductance			50			50			
7		C_{iss}	Common-Source Input Capacitance		3.5			3.5		pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.85			0.85				
9		C_{oss}	Common-Source Output Capacitance		1.0			1.0				
10	HIGH FREQUENCY	g_{fs}	Common-Source Forward Transconductance					3,000		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
11					4,200							f = 400 MHz
12		g_{oss}	Common-Source Output Conductance		60			60				f = 100 MHz
13					80							f = 400 MHz
14		b_{oss}	Common-Source Output Susceptance		800			800				f = 100 MHz
15					3,600							f = 400 MHz
16		g_{iss}	Common-Source Input Conductance		80			80				f = 100 MHz
17					800							f = 400 MHz
18		b_{iss}	Common-Source Input Susceptance		2,000			2,000				f = 100 MHz
19					7,500							f = 400 MHz
20		G_{ps}	Common-Source Power Gain		20					dB	V_{DS} = 15 V, I_D = 5 mA	f = 100 MHz
21					11							f = 400 MHz
22		NF	Noise Figure (Single Sideband)		1.7						V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ	f = 100 MHz
23					3.8							f = 400 MHz

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NH

© 1979 Siliconix incorporated

n-channel JFETs
designed for . . .

- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Siliconix

Performance Curves NZA
See Section 5

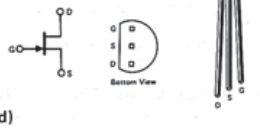
BENEFITS

- Industry Standard Part
  In Low Cost Plastic Package
- High Power Gain
  11 dB Typical at 450 MHz
  Common-Gate
- Low Noise
  2.7 dB Typical at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- Easily Matches to 75 Ω Input

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	J308 Min	J308 Typ	J308 Max	J309 Min	J309 Typ	J309 Max	J310 Min	J310 Typ	J310 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25			–25			–25			V	I_G = –1 μA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current			–1.0			–1.0			–1.0	nA	V_{GS} = –15 V, V_{DS} = 0	
3						–1.0			–1.0			–1.0	μA		T = +125°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1.0		–6.5	–1.0		–4.0	–2.0		–6.5	V	V_{DS} = 10 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	V_{DS} = 0, I_G = 1 mA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	8,000		20,000	10,000		20,000	8,000		18,000	μmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			200			200			200			
9		g_{fg}	Common-Gate Forward Transconductance		13,000			13,000			12,000				
10		g_{og}	Common-Gate Output Conductance		150			100			150				
11		C_{gd}	Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5	pF	V_{DS} = 0, V_{GS} = –10 V	f = 1 MHz
12		C_{gs}	Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0			
13		$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
14	HI FREQ	$Re(y_{fs})$	Common-Source Forward Transconductance		12			12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
15		$Re(y_{ig})$	Common-Gate Input Conductance		14			14			14				
16		$Re(y_{is})$	Common-Source Input Conductance		0.4			0.4			0.4				
17		$Re(y_{os})$	Common-Source Output Conductance		0.15			0.15			0.15				
18		G_{pg}	Common-Gate Power Gain at Noise Match		16			16			16		dB		
19		NF	Noise Figure		1.5			1.5			1.5				f = 450 MHz
20		G_{pg}	Common-Gate Power Gain at Noise Match		11			11			11				
21		NF	Noise Figure		2.7			2.7			2.7				

NOTE:
1 Pulse test PW 300 μs, duty cycle < 3%

NZA

© 1979 Siliconix incorporated

n-channel JFETs
current regulator diodes
designed for . . .

- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

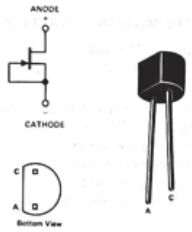
Siliconix

Performance Curves NCL
See Section 5

BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources
  No Power Supplies Required
- Good Operating Current Tolerance
  ±20%

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage . . . . . 50 V
Forward Current . . . . . 20 mA
Reverse Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

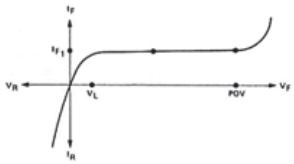
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic		J500	J501	J502	J503	J504	J505	Unit	Test Conditions
1	STATIC	I_{FI}	Forward Current (Note 1)	Min	0.192	0.264	0.344	0.448	0.600	0.800	mA	V_F = 25 V
2				Nominal	0.240	0.330	0.430	0.560	0.750	1.000		
3				Max	0.288	0.396	0.516	0.672	0.900	1.200		
4		POV	Peak Operating Voltage (Notes 1 and 2)	Min	50	50	50	50	50	50	V	I_F = 1.1 I_{FI} (Max)
5		V_L	Limiting Voltage (Note 3)	Max	1.2	1.3	1.5	1.7	1.9	2.1		I_F = 0.9 I_{FI} (Min)
6				Typ	0.8	0.9	1.1	1.2	1.4	1.5		
7	DYN	Z_{FI}	Small-Signal Dynamic Impedance (Note 1)	Min	5.0	3.0	2.0	1.4	1.0	0.6	MΩ	V_F = 25 V, f = 1 kHz
8				Typ	8.0	6.0	4.4	3.4	2.5	1.9		
9		C_F	Anode-Cathode Capacitance	Typ	2	2	2	2	2	2	pF	V_F = 25 V, f = 1 MHz

NCL

NOTES:
1. Pulse test duration = 2 ms.
2. Maximum V_F where $I_F < 1.1\ I_{FI(Max)}$ is guaranteed.
3. Minimum V_F required to insure $I_F > 0.9\ I_{FI(Min)}$.

Current-Limiter Diode
V-I Characteristic



© 1979 Siliconix Incorporated

n-channel JFETs current regulator diodes

designed for . . .

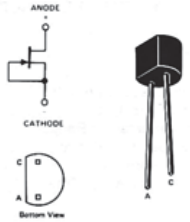
- **Current Regulation**
- **Current Limiting**
- **Biasing**
- **Linear Ramp and Staircase Generator**

Performance Curves NCL See Section 5

BENEFITS

- Low Cost
- Simple Two Lead Current Source
- Simplifies Floating Current Sources No Power Supplies Required
- Good Operating Current Tolerance ±20%

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Peak Operating Voltage . . . . . 50 V
Forward Current . . . . . 20 mA
Reverse Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient (Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range (1/16" from case for 10 seconds) . . . . . 300°C

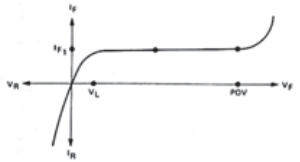
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic			J506	J507	J508	J509	J510	J511	Unit	Test Conditions
1	STATIC	I_{FI} Forward Current (Note 1)		Min	1.120	1.440	1.9	2.4	2.9	3.8	mA	V_F = 25 V
2				Nominal	1.400	1.800	2.4	3.0	3.6	4.7		
3				Max	1.680	2.160	2.9	3.6	4.3	5.6		
4		POV Peak Operating Voltage (Notes 1 and 2)		Min	50	50	50	50	50	50	V	I_F = 1.1 I_{FI} (Max)
5		V_L Limiting Voltage (Note 3)		Max	2.5	2.8	3.1	3.5	3.9	4.2		I_F = 0.9 I_{FI} (Min)
6				Typ	1.8	2.0	2.2	2.5	2.8	3.0		
7	DYN	Z_{FI} Small-Signal Dynamic Impedance (Note 1)		Min	0.4	0.25	0.25	0.20	0.20	0.15	MΩ	V_F = 25 V, f = 1 kHz
8				Typ	1.4	1.0	0.70	0.60	0.50	0.30		
9		C_F Anode-Cathode Capacitance		Typ	2	2	2	2	2	2	pF	V_F = 25 V, f = 1 MHz

NCL

NOTES:
1. Pulse test duration = 2 ms.
2. Maximum V_F where $I_F < 1.1\ I_{FI(Max)}$ is guaranteed.
3. Minimum V_F required to insure $I_F > 0.9\ I_{FI(Min)}$

Current-Limiter Diode
V-I Characteristic



© 1979 Siliconix incorporated

low-leakage pico-amp diodes

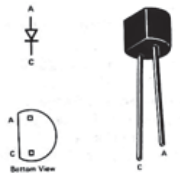
designed for . . .

- **High Impedance Diode Switching**
- **High Dynamic Range Log Amps**
- **High Isolation Protection Circuits**

BENEFITS

- Low Cost

TO-92
See Section 7





(TO-106)

Also Available As EPAD50, 100, 200, 500 (TO-106)

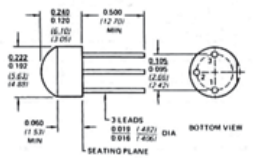
ABSOLUTE MAXIMUM RATINGS (25°C)

Forward Current . . . . . 10 mA
Total Device Dissipation . . . . . 360 mW
Storage Temperature Range . . . . . –65°C to +135°C
Lead Temperature (1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C)

		Characteristic		Min	Typ	Max	Unit	Test Conditions
1	STATIC	I_R Reverse Current (Note 1)	JPAD50			–50	pA	V_R = –20 V
2			JPAD100			–100		
3			JPAD200			–200		
4			JPAD500			–500		
5		BV_R Breakdown Voltage (Reverse)		–35	–80		V	I_R = –1 μA
6		V_F Forward Voltage Drop			0.8	1.5	V	I_F = 5 mA
7	DYN	C_R Capacitance			1.5	2.0	pF	V_R = –5 V, f = 1 MHz

NOTE:
1. The JPAD type number denotes its maximum reverse current value in pico amps. Devices with I_R values intermediate to those shown are also available on request.



TO-106

© 1979 Siliconix incorporated

n-channel JFET
designed for . . .

- **Analog Switches**
- **Choppers**
- **Commutators**

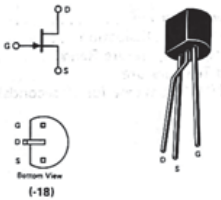
Siliconix

Performance Curves NZF
See Section 5

BENEFITS

- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Very Fast Switching
  - $t_{D(on)} + t_r = 6$ ns Typical
- Short Sample and Hold Aperture Time
  - $C_{gd(off)} < 2$ pF
  - $C_{gs(off)} < 2$ pF

TO-92 Lead-form
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -25 V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		K114 Min	K114 Typ	K114 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-1	nA	V_{DS} = 0, V_{GS} = -15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-3		-10	V	V_{DS} = 5 V, I_D = 1 µA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25			V	V_{DS} = 0, I_G = -1 µA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	15			mA	V_{DS} = 15 V, V_{GS} = 0	
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 1)			1	nA	V_{DS} = 5 V, V_{GS} = -10 V	
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance			150	Ω	$V_{DS} \leq 0.1$ V, V_{GS} = 0	
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance			2	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source-Gate OFF Capacitance			2	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance			8	pF	$V_{DS} = V_{GS}$ = 0	f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		3		ns	Switching Time Test Conditions V_{DD} = 10 V, $V_{GS(off)}$ = -12 V R_L = 1 KΩ, $V_{GS(on)}$ = 0	
11	DYNAMIC	t_r	Rise Time		3		ns		
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		12		ns		
13	DYNAMIC	t_f	Fall Time		8		ns		

NZF

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 300 µs; duty cycle ≤ 3%.

© 1979 Siliconix incorporated

n-channel JFET
designed for . . .

- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

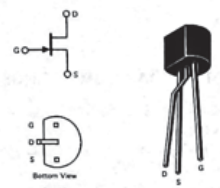
Siliconix

Performance Curves NH
See Section 5

BENEFITS

- Specified for 200 MHz Operation

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage. . . . . 25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		-250	pA	V_{GS} = -20 V, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current		-15	nA	V_{GS} = -20 V, V_{DS} = 0	T_A = +85°C
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = -1 µA, V_{DS} = 0	
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-8.0	V	V_{DS} = 15 V, I_D = 1 µA	
5	STATIC	I_{DSS}	Saturation Drain Current	4.0	25	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance		300	Ω	I_D = 1 mA, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500	10,000	µmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	$Re(y_{fs})$	Common-Source Forward Transconductance	4,000		µmhos	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
9	DYNAMIC	$Re(y_{os})$	Common-Source Output Conductance		150	µmhos	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
10	DYNAMIC	$Re(y_{is})$	Common-Source Input Conductance		800	µmhos	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		6.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		2.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
13		NF	Noise Figure		3.0	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1K Ω	f = 200 MHz
14		NF	Noise Figure		5.0	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω, BW = 5 Hz	f = 10 Hz
15		G_{PS}	Common-Source Power Gain	15		dB	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz

NH

NOTE:
1. Pulse test PW = 300 µs; duty cycle < 3%.

© 1979 Siliconix incorporated

n-channel JFETs
designed for . . .

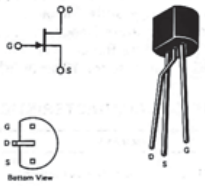
- **General Purpose Amplifiers**

Performance Curves NZF
See Section 5

BENEFITS

- High Gain
  G_{FS} = 7000 μmho Minimum
  (K211-18, K212-18)
- High Input Impedance
  I_{GSS} = 100 pA Maximum
  C_{iss} = 5 pF Typical

TO-92 Lead-form
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		J210			J211			J212			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-100			-100			-100	pA	V_{DS} = 0, V_{GS} = -15 V	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-3	-2.5		-4.5	-4		-6	V	V_{DS} = 15 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	2		15	7		20	15		40	mA	V_{DS} = 15 V, V_{GS} = 0	
5	STATIC	I_G	Gate Current (Note 1)		-10			-10			-10		pA	V_{DG} = 10 V, I_D = 1 mA	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,000		12,000	7,000		12,000	7,000		12,000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	g_{os}	Common-Source Output Conductance			150			200			200	μmho		f = 1 kHz
8	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4			4			4		pF		f = 1 MHz
9	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1			1			1		pF		f = 1 MHz
10	DYNAMIC	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$		f = 1 kHz

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NZF

© 1979 Siliconix Incorporated

n-channel JFET
designed for . . .

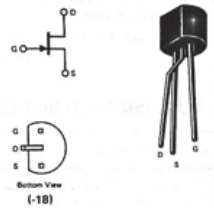
- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZF
See Section 5

BENEFITS

- High Power Gain
  22 dB Typical at 100 MHz
  Common-Source
  17 dB Typical at 100 MHz
  Common-Gate
- Low Noise
  NF = 2 dB Typical at 100 MHz
- High Dynamic Range Greater than 100 dB

TO-92 Lead-form
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25V
Gate Current (FWD) . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-500	pA	V_{GS} = -15 V, V_{DS} = 0	
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1		-6	V	V_{DS} = 10 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-25			V	V_{DS} = 0, I_G = -1 μA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	6		30	mA	V_{DS} = 10 V, V_{GS} = 0	
5	STATIC	$V_{GS(f)}$	Gate-Source Forward Voltage			1	V	I_G = 1 mA, V_{DS} = 0	
6	DYN	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,500		9,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
7	DYN	g_{os}	Common-Source Output Transconductance			200	μmho		f = 1 kHz
8	DYN	C_{iss}	Common-Source Input Capacitance		4	5.5	pF	V_{DG} = 10 V, I_D = 5 mA	f = 1 MHz
9	DYN	C_{rss}	Common-Source Reverse Transfer Capacitance		1	1.7	pF		f = 1 MHz
10	DYN	C_{oss}	Common-Source Output Capacitance		1.5		pF		f = 1 MHz
11	HI FREQ	$\|y_{fs}\|$	Common-Source Forward Transadmittance		6,200		μmho	V_{DG} = 15 V, I_D = 5 mA	f = 100 MHz
12	HI FREQ	$\|y_{fs}\|$	Common-Source Forward Transadmittance		6,000		μmho	V_{DG} = 15 V, I_D = 5 mA	f = 450 MHz
13	HI FREQ	$\|y_{fg}\|$	Common-Gate Forward Transadmittance		6,000		μmho	V_{DG} = 15 V, I_D = 5 mA	f = 100 MHz
14	HI FREQ	$\|y_{fg}\|$	Common-Gate Forward Transadmittance		5,500		μmho	V_{DG} = 15 V, I_D = 5 mA	f = 450 MHz
15	HI FREQ	G_{fg}	Common-Gate Power Gain		17		dB		f = 100 MHz (Note 3)
16	HI FREQ	NF	Noise Figure (Single Sideband)		2		dB		f = 100 MHz (Note 3)

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.
3. Typical values for performance at 100 MHz in a common-gate circuit operating 3 dB bandwidth is 2 MHz.

NZF

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

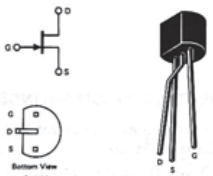
- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NH See Section 5

BENEFITS

- Characterized for Operation at 100 and 400 MHz
- Low Noise
  NF = 1.7 dB Typical at 100 MHz

TO-92 Lead-form
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –30V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		K304-18 Min	K304-18 Typ	K304-18 Max	K305-18 Min	K305-18 Typ	K305-18 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			-100			-100	pA	V_{DS} = 0, V_{GS} = -20 V	
2	STATIC	$V_{GS(off)}$	Gate Source Cutoff Voltage	-2		-6	-0.5		-3	V	V_{DS} = 15 V, I_D = 1 nA	
3	STATIC	BV_{GSS}	Gate Source Breakdown Voltage	-30			-30			V	V_{DS} = 0, I_G = -1 µA	
4	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	5		15	1		8	mA	V_{DS} = 15 V, V_{GS} = 0	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	4,500		7,500	3,000			µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
6	DYNAMIC	g_{os}	Common-Source Output Transconductance			50			50	µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7	DYNAMIC	C_{iss}	Common-Source Input Capacitance		3.5			3.5		pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
8	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		0.85			0.85		pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
9	DYNAMIC	C_{oss}	Common-Source Output Capacitance		1.0			1.0		pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
10	HIGH FREQUENCY	g_{fs}	Common-Source Forward Transconductance					3,000		µmho	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
11	HIGH FREQUENCY	g_{fs}	Common-Source Forward Transconductance		4,200					µmho	V_{DS} = 15 V, V_{GS} = 0	f = 400 MHz
12	HIGH FREQUENCY	g_{oss}	Common-Source Output Conductance		60			60		µmho	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
13	HIGH FREQUENCY	g_{oss}	Common-Source Output Conductance		80					µmho	V_{DS} = 15 V, V_{GS} = 0	f = 400 MHz
14	HIGH FREQUENCY	b_{oss}	Common-Source Output Susceptance		800			800		µmho	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
15	HIGH FREQUENCY	b_{oss}	Common-Source Output Susceptance		3,600					µmho	V_{DS} = 15 V, V_{GS} = 0	f = 400 MHz
16	HIGH FREQUENCY	g_{iss}	Common-Source Input Conductance		80			80		µmho	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
17	HIGH FREQUENCY	g_{iss}	Common-Source Input Conductance		800					µmho	V_{DS} = 15 V, V_{GS} = 0	f = 400 MHz
18	HIGH FREQUENCY	b_{iss}	Common-Source Input Susceptance		2,000			2,000		µmho	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
19	HIGH FREQUENCY	b_{iss}	Common-Source Input Susceptance		7,500					µmho	V_{DS} = 15 V, V_{GS} = 0	f = 400 MHz
20	HIGH FREQUENCY	G_{ps}	Common-Source Power Gain		20					dB	V_{DS} = 15 V, I_D = 5 mA	f = 100 MHz
21	HIGH FREQUENCY	G_{ps}	Common-Source Power Gain		11					dB	V_{DS} = 15 V, I_D = 5 mA	f = 400 MHz
22	HIGH FREQUENCY	NF	Noise Figure (Single Sideband)		1.7					dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ	f = 100 MHz
23	HIGH FREQUENCY	NF	Noise Figure (Single Sideband)		3.8					dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ	f = 400 MHz

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse test duration = 2 ms.

NH

© 1979 Siliconix Incorporated

n-channel JFETs *designed for . . .*

Siliconix

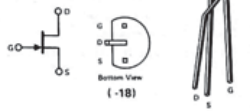
- **VHF/UHF Amplifiers**
- **Oscillators**
- **Mixers**

Performance Curves NZA See Section 5

BENEFITS

- Industry Standard Part
  In Low Cost Plastic Package
- High Power Gain
  11 dB Typical at 450 MHz
  Common-Gate
- Low Noise
  2.7 dB Typical at 450 MHz
- Wide Dynamic Range
  Greater than 100 dB
- Easily Matches to 75 Ω Input

TO-92 Lead-form
See Section 7



* ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		K308 Min	K308 Typ	K308 Max	K309 Min	K309 Typ	K309 Max	K310 Min	K310 Typ	K310 Max	Unit	Test Conditions	
1		BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	I_G = -1 µA, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current			-1.0			-1.0			-1.0	nA	V_{GS} = -15 V, V_{DS} = 0	
3	STATIC	I_{GSS}	Gate Reverse Current			-1.0			-1.0			-1.0	µA	V_{GS} = -15 V, V_{DS} = 0	T = +125°C
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-6.5	-1.0		-4.0	-2.0		-6.5	V	V_{DS} = 10 V, I_D = 1 nA	
5	STATIC	I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
6	STATIC	$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	V_{DS} = 0, I_G = 1 mA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	8,000		20,000	10,000		20,000	8,000		18,000	µmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
8	DYNAMIC	g_{os}	Common-Source Output Conductance			200			200			200	µmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
9	DYNAMIC	g_{fg}	Common-Gate Forward Transconductance		13,000			13,000			12,000		µmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 MHz
10	DYNAMIC	g_{og}	Common-Gate Output Conductance		150			100			150		µmhos	V_{DS} = 10 V, I_D = 10 mA	f = 1 MHz
11	DYNAMIC	C_{gd}	Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
12	DYNAMIC	C_{gs}	Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0	pF	V_{DS} = 0, V_{GS} = -10 V	f = 1 MHz
13	DYNAMIC	$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
14	HI FREQ	$Re(y_{fs})$	Common-Source Forward Transconductance		12			12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
15	HI FREQ	$Re(y_{ig})$	Common-Gate Input Conductance		14			14			14		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
16	HI FREQ	$Re(y_{is})$	Common-Source Input Conductance		0.4			0.4			0.4		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
17	HI FREQ	$Re(y_{os})$	Common-Source Output Conductance		0.15			0.15			0.15		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 105 MHz
18	HI FREQ	G_{pg}	Common-Gate Power Gain at Noise Match		16			16			16		dB		f = 450 MHz
19	HI FREQ	NF	Noise Figure		1.5			1.5			1.5		dB		f = 450 MHz
20	HI FREQ	G_{pg}	Common-Gate Power Gain at Noise Match		11			11			11		dB		f = 450 MHz
21	HI FREQ	NF	Noise Figure		2.7			2.7			2.7		dB		f = 450 MHz

NOTE:
1. Pulse test PW 300 µs, duty cycle ≤ 3%.

NZA

© 1979 Siliconix Incorporated

n-channel JFET
designed for . . .

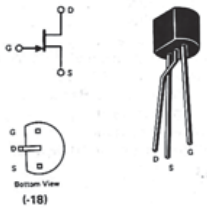
- **VHF Amplifiers**
- **Mixers**

Siliconix

Performance Curves NH
See Section 5

BENEFITS
- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Bandwidth
- Low Cost

TO-92 Lead-form
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –30V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STA	I_{GSS}	Gate Reverse Current		–1.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2	STA	BV_{GSS}	Gate-Source Breakdown Voltage	–30		V	I_G = –1 µA, V_{DS} = 0	
3	STA	$V_{GS(off)}$	Gate-Source Cutoff Voltage		–6	V	V_{DS} = 15 V, I_D = 1 nA	
4	STA	I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
5	DYN	g_{fs}	Common-Source Forward Transconductance (Note 1)	4500	7500	µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
6	DYN	g_{os}	Common-Source Output Conductance		50	µmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7	DYN	C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
8	DYN	C_{iss}	Common-Source Input Capacitance		4	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
9	DYN	C_{oss}	Common-Source Output Capacitance		2	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz

		Characteristic		100 MHz Min	100 MHz Max	400 MHz Min	400 MHz Max	Unit	Test Conditions	
10	HI FREQ	g_{iss}	Common-Source Input Conductance		100		1000	µmho	V_{DS} = 15 V, V_{GS} = 0	
11	HI FREQ	b_{iss}	Common-Source Input Susceptance		2500		10,000	µmho	V_{DS} = 15 V, V_{GS} = 0	
12	HI FREQ	g_{oss}	Common-Source Output Conductance		75		100	µmho	V_{DS} = 15 V, V_{GS} = 0	
13	HI FREQ	b_{oss}	Common-Source Output Susceptance		1000		4000	µmho	V_{DS} = 15 V, V_{GS} = 0	
14	HI FREQ	g_{fs}	Common-Source Forward Transconductance (Note 1)			4000		µmho	V_{DS} = 15 V, V_{GS} = 0	
15	HI FREQ	G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA	R_G = 1K Ω
16	HI FREQ	NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA	R_G = 1K Ω

NOTE:
1. Pulse test duration = 300 µs.

NH

© 1979 Siliconix Incorporated

n-channel JFET
designed for . . .

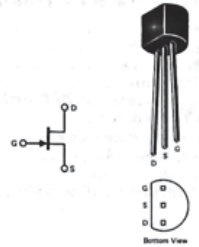
- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

Siliconix

Performance Curves NH
See Section 5

BENEFITS
- Low Cost
- Automatic Insertion Package

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage . . . . . 25 V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–2.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current		–2.0	µA	V_{GS} = –15 V, V_{DS} = 0	T_A = +100°C
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –10 µA, V_{DS} = 0	
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage		–8.0	V	V_{DS} = 15 V, I_D = 2 nA	
5	STATIC	I_{DSS}	Saturation Drain Current	2.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	STATIC	V_{GS}	Gate-Source Voltage	–0.5	–7.5	V	V_{DS} = 15 V, I_D = 200 µA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	7500	µmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8	DYNAMIC	$Re(y_{fs})$	Common-Source Forward Transconductance	1600		µmhos	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
9	DYNAMIC	$Re(y_{os})$	Common-Source Output Conductance		200	µmhos	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
10	DYNAMIC	$Re(y_{is})$	Common-Source Input Conductance		800	µmhos	V_{DS} = 15 V, V_{GS} = 0	f = 100 MHz
11	DYNAMIC	C_{iss}	Common-Source Input Capacitance		7.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
12	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		3.0	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz

NOTE:
1. Pulse test PW = 300 µs; duty cycle < 3%.

NH

© 1979 Siliconix Incorporated

Siliconix

n-channel JFET
designed for . . .

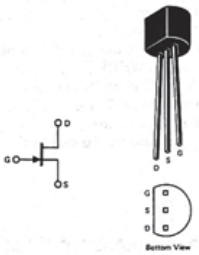
- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

Siliconix

Performance Curves NH
See Section 5

BENEFITS
- Low Cost
- Automatic Insertion Package

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage. . . . . 25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–1.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2					–1.0	μA		T_A = +100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –10 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5	–8.0		V_{DS} = 15 V, I_D = 10 μA	
5		I_{DSS}	Saturation Drain Current	1.5	24	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	7500	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		75			
8		$Re(y_{fs})$	Common-Source Forward Transconductance	1600				f = 100 MHz
9		$Re(y_{os})$	Common-Source Output Conductance		200			
10		$Re(y_{is})$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		6.5	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		2.5			
13		NF	Noise Figure		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz
14					3.0		V_{DS} = 15 V, V_{GS} = 0, R_G = 1K Ω	f = 100 MHz

NOTE:
1. Pulse test, pulse width = 300 μs, duty cycle < 3%.

NH

© 1979 Siliconix incorporated

n-channel JFET
designed for . . .

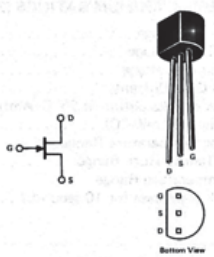
- **General Purpose Amplifiers**
- **Analog Switches**

Siliconix

Performance Curves NRL
See Section 5

BENEFITS
- Low Cost
- Automatic Insertion Package

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage. . . . . 25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–0.01	–1.0	nA	V_{GS} = –15 V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	–25	–60		V	I_G = –10 μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.2		–8.0		V_{DS} = 15 V, I_D = 10 μA	
4		I_{DSS}	Saturation Drain Current	0.5		24	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	800		6000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
6		g_{os}	Common-Source Output Conductance		10	75			
7		C_{iss}	Common-Source Input Capacitance		4.5	7.0	pF		f = 1 MHz
8		C_{rss}	Common-Source Reverse Transfer Capacitance		1.0	3.0			
9		NF	Noise Figure		0.04	2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω	f = 1 kHz

NOTE:
1. Pulse test PW < 630 ms, duty cycle < 10%.

NRL

© 1979 Siliconix incorporated

n-channel JFET
designed for . . .

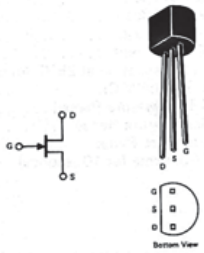
- **General Purpose Amplifiers**
- **Analog Switches**

Siliconix

Performance Curves NRL
See Section 5

BENEFITS
- Low Cost
- Automatic Insertion Package

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage 20V
Source-Gate Voltage 20V
Drain-Source Voltage. 20V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–.01	–100	nA	V_{GS} = –10 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–20			V	I_G = –10 µA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5		–10.0		V_{DS} = 10 V, I_D = 1 µA	
4	STATIC	I_{DSS}	Saturation Drain Current	0.5		20	mA	V_{DS} = 10 V, V_{GS} = 0 (Note 1)	
5	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	500			µmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
6	DYNAMIC	g_{os}	Common-Source Output Conductance		10				
7	DYNAMIC	C_{iss}	Common-Source Input Capacitance		4.5		pF		f = 1 MHz
8	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance		1.0				

NRL

NOTE:
1. Pulse test PW ≤ 630 msec, duty cycle ≤ 10%.

© 1979 Siliconix incorporated

n-channel JFET
designed for . . .

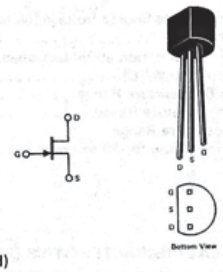
- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

Siliconix

Performance Curves NH
See Section 5

BENEFITS
- Low Cost
- Automatic Insertion Package

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage . . . . . 25 V
Source-Gate Voltage . . . . . 25 V
Drain-Source Voltage. . . . . 25 V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–0.01	–100	nA	V_{GS} = –10 V, V_{DS} = 0	
2	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–25			V	I_G = –10 µA, V_{DS} = 0	
3	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5		–10.0		V_{DS} = 10 V, I_D = 1 µA	
4	STATIC	I_{DSS}	Saturation Drain Current	1		25	mA	V_{DS} = 10 V, V_{GS} = 0, (Note 1)	
5	DYN	g_{fs}	Common-Source Forward Transconductance	1000		7500	µmho	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
6	DYN	$Re(y_{fs})$	Common-Source Forward Transconductance	800					f = 100 MHz
7	DYN	C_{iss}	Common-Source Input Capacitance		3.5		pF		f = 1 MHz
8	DYN	C_{rss}	Common-Source Reverse Transfer Capacitance		0.85				

NH

NOTE:
1. Pulse test PW = 300 µs, duty cycle < 3%.

© 1979 Siliconix incorporated

p-channel JFETs
designed for . . .

Siliconix

- **Analog Switches**
- **Choppers**
- **Commutators**

Performance Curves PS
See Section 5

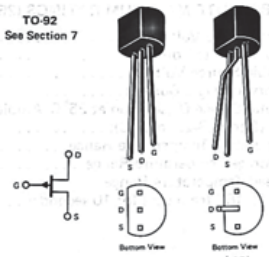
BENEFITS

- Low Insertion Loss
  $R_{DS(on)}$ = 75 Ω Maximum (P1086E)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current . . . . . 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		P1086 Min	P1086 Max	P1087 Min	P1087 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		V	I_G = 1 µA, V_{DS} = 0	
2		I_{GSS}	Gate Reverse Current		2		2	nA	V_{GS} = 15 V, V_{DS} = 0	
3		$I_{D(off)}$	Drain Cutoff Current		–10		–10		V_{DS} = –15 V, V_{GS} = 12 V (P1086E)	
4					–0.5		–0.5	µA	V_{GS} = 7 V (P1087E)	T_A = 85°C
5		I_{DGO}	Drain Reverse Current		2		2	nA	V_{DG} = –15 V, I_S = 0	
					0.1		0.1	µA		T_A = 85°C
6		$V_{GS(off)}$	Gate-Source Cutoff Voltage		10		5	V	V_{DS} = –15 V, I_D = –1 µA	
7		I_{DSS}	Saturation Drain Current	–10		–5		mA	V_{DS} = –20 V, V_{GS} = 0	
8		$V_{DS(on)}$	Drain-Source ON Voltage		–0.5		–0.5	V	V_{GS} = 0, I_D = –6 mA (P1086E), I_D = –3 mA (P1087E)	
9		$r_{DS(on)}$	Static Drain-Source ON Resistance		75		150	Ω	I_D = –1 mA, V_{GS} = 0	
10		$r_{ds(on)}$	Drain-Source ON Resistance		75		150	Ω	I_D = 0, V_{GS} = 0	f = 1 kHz
11	DYN	C_{iss}	Common-Source Input Capacitance		45		45	pF	V_{DS} = –15 V, V_{GS} = 0	f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		10		10		V_{DS} = 0, V_{GS} = 12 V (P1086E) V_{GS} = 7 V (P1087E)	
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		15		15	ns	V_{DD} = –6 V, $V_{GS(on)}$ = 0	
14		t_r	Rise Time		20		75		$V_{GS(off)}$ $I_{D(on)}$ R_L	
15		$t_{d(off)}$	Turn-OFF Delay Time		15		25		P1086E 12 V –6 mA 910 Ω	
16		t_f	Fall Time		50		100		P1087E 7 V –3 mA 1.8K Ω	

NOTE:
1. Due to symmetrical geometry, these units may be operated with source and drain leads interchanged.

PS

© 1979 Siliconix incorporated

n-channel JFETs
designed for . . .

Siliconix

- **Analog Switches**
- **Commutators**
- **Choppers**
- **Integrator Reset Switch**

Performance Curves NC
See Section 5

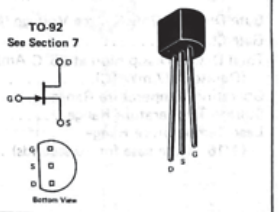
BENEFITS

- Low Insertion Loss
  High Accuracy in Test Systems
  R_{ON} < 30 Ω (PN4091)
- High Off-Isolation
  $I_{D(off)}$ < 200 pA
- High Speed
  t_{rise} < 10 ns (PN4091)
- Short Sample and Hold Aperture Time
  C_{rss} < 5 pF

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage . . . . . –40 V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

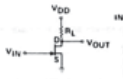
TO-92
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		PN4091 Min	PN4091 Max	PN4092 Min	PN4092 Max	PN4093 Min	PN4093 Max	Unit	Test Conditions		
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–40		–40		–40		V	I_G = –1 µA, V_{DS} = 0		
2		I_{DGO}	Drain Reverse Current		200		200		200	pA	V_{GS} = –20 V, I_S = 0		
3					400		400		400	nA			150°C
4		$I_{D(off)}$	Drain Cutoff Current						200	pA	V_{DS} = 20 V	V_{GS} = – 6 V	
5									400	nA			150°C
6							200			pA		V_{GS} = – 8 V	
7							400			nA			150°C
8					200					pA		V_{GS} = –12 V	
9					400					nA			150°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–5	–10	–2	–7	–1	–5	V	V_{DS} = 20 V, I_D = 1 nA		
11		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8		mA	V_{DS} = 20 V, V_{GS} = 0		
12		$V_{DS(on)}$	Drain-Source ON Voltage						0.2	V	V_{GS} = 0	I_D = 2.5 mA	
13							0.2					I_D = 4 mA	
14					0.2							I_D = 6.6 mA	
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	V_{GS} = 0, I_D = 1 mA		
16	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		30		50		80	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
17		C_{iss}	Common-Source Input Capacitance		16		16		16	pF	V_{DS} = 20 V, V_{GS} = 0		f = 1 MHz
18		C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5		V_{DS} = 0, V_{GS} = –20 V		
19	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		20	ns	V_{DD} = 3 V, $V_{GS(on)}$ = 0		
20		t_r	Rise Time		10		20		40		$I_{D(on)}$ $V_{GS(off)}$ R_L		
21		t_{off}	Turn-OFF Time		40		60		80		PN4091 6.6 mA –12 V 425 Ω		
											PN4092 4 –8 700		
											PN4093 2.5 –6 1120		

NOTE:
1. Pulsewidth = 300 µs, duty cycle ≤ 3%.



INPUT PULSE
RISE TIME < 1 ns
FALL TIME < 1 ns
PULSE WIDTH 1 µs
PULSE DUTY CYCLE < 10%
PULSE GENERATOR IMPEDANCE 50Ω

NC

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.7 pF

© 1979 Siliconix Incorporated

n-channel JFETs
designed for . . .

Siliconix

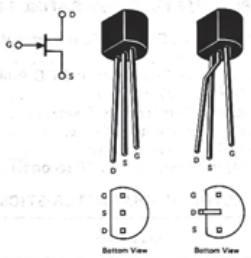
■ **General Purpose Amplifiers**

Performance Curves NP
See Section 5

BENEFITS

- Low Cost
- High Input Impedance
  I_G = 35 pA Typically
- Low Noise
  $\overline{e_n}$ = 5 nV/√Hz Typically @ 1 kHz

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) ..... –30V
Gate Current ..... 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) ..... 360 mW
Operating Temperature Range ..... –55 to 135°C
Storage Temperature Range ..... –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	PN4302 Min	PN4302 Max	PN4303 Min	PN4303 Max	PN4304 Min	PN4304 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)		1		–1		–1	nA	V_{GS} = –10 V, V_{DS} = 0	
2					0.1		–0.1		–0.1	µA		T_A = 85°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–30		–30		–30		V	I_G = –1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–4.0		–6.0		–10		V_{DS} = 20 V, I_D = 10 nA	
5		I_{DSS}	Saturation Drain Current (Note 3)	0.5	5.0	4.0	10	0.5	15	mA		
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	1000		2000		1000		µmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50		50		50			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		6		6		6			
10		C_{DG}	Drain-Gate Capacitance		2		2		2		V_{DG} = 10 V, I_S = 0	f = 140 kHz
11		NF	Noise Figure		2.0		2.0		3.0	dB	V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz, R_{gen} = 1.0M Ω
12		$\|Y_{fs}\|$	Common-Source Short Circuit Forward Transadmittance (Note 3)	700		1400		700		µmho	V_{DS} = 20 V, V_{GS} = 0	f = 10 MHz

NP

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

© 1979 Siliconix Incorporated

n-channel JFETs
designed for . . .

Siliconix

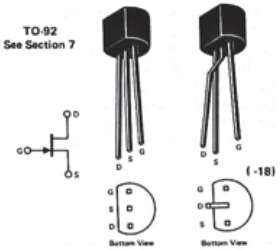
■ **Analog Switches**
■ **Commutators**
■ **Choppers**

Performance Curves NC
See Section 5

BENEFITS

- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Low Cost

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage ..... –40 V
Forward Gate Current ..... 50 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) ..... 360 mW
Operating Temperature Range ..... –55 to 135°C
Storage Temperature Range ..... –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

			Characteristic	PN4391 Min	PN4391 Max	PN4392 Min	PN4392 Max	PN4393 Min	PN4393 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–1.0		–1.0		–1.0	nA	V_{GS} = –20 V, V_{DS} = 0	
2					–200		–200		–200			100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–40		–40		–40		V	I_G = –1 µA, V_{DS} = 0	
4		$I_{D(off)}$	Drain Cutoff Current						1.0	nA	V_{DS} = 20 V	V_{GS} = –5 V
5									200			100°C
6							1.0					V_{GS} = –7 V
7							200					100°C
8					1.0							V_{GS} = –12 V
9					200							100°C
10		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–4	–10	–2	–5	–0.5	–3	V	V_{DS} = 20 V, I_D = 1 nA	
11		I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0	
12		$V_{DS(on)}$	Drain-Source ON Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA
13							0.4					I_D = 6 mA
14					0.4							I_D = 12 mA
15		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA	
16		$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, V_{DS} = 0	f = 1 kHz
17	DYN	C_{iss}	Common-Source Input Capacitance		14		14		14	pF	V_{DS} = 20 V, V_{GS} = 0	
18		C_{rss}	Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0	V_{GS} = –5 V
19							3.5					V_{GS} = –7V
20					3.5							V_{GS} = –12 V
21	SW	$t_{d(on)}$	Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0	
22		t_r	Rise Time		5		5		5			
23		$t_{d(off)}$	Turn-OFF Delay Time		20		35		50			
24		t_f	Fall Time		15		20		30			

	$I_{D(on)}$	$V_{GS(off)}$	R_L
PN4391	12 mA	–12 V	800 Ω
PN4392	6	–7	1.6K
PN4393	3	–5	3.2K

NC

NOTE:
1. Pulse test required, pulse width = 300 µs, duty cycle ≤ 3%.

© 1979 Siliconix Incorporated

n-channel JFETs
designed for . . .

Siliconix

Performance Curves NH See Section 5

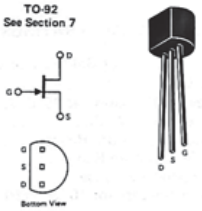
- **VHF Amplifiers**
- **Mixers**

BENEFITS
- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wide Band
  High g_{fs}/C_{iss} Ratio

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –30V
Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 7



		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		1.0	nA	V_{GS} = –15 V, V_{DS} = 0 V	
2								
3		BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = -1 μA, V_{DS} = 0 V	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		-6		V_{DS} = 15 V, I_D = 1 nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0 V	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		f = 1 kHz
7		g_{os}	Common-Source Output Conductance		50			
8		C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
9		C_{iss}	Common-Source Input Capacitance		4			
10		C_{oss}	Common-Source Output Capacitance		2			

		Characteristic		100 MHz Min	100 MHz Max	400 MHz Min	400 MHz Max	Unit	Test Conditions
11	HIGH FREQUENCY	g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0 V
12		b_{iss}	Common-Source Input Susceptance		2500		10,000		
13		g_{oss}	Common-Source Output Conductance		75		100		
14		b_{oss}	Common-Source Output Susceptance		1000		4000		
15		g_{fs}	Common-Source Forward Transconductance			4000			
16		G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
17		NF	Noise Figure		2		4		V_{DS} = 15 V, I_D = 5 mA, R_G = 1K Ω

NH

NOTES:
1. Pulse test duration = 300 μs.

© 1979 Siliconix Incorporated

n-channel JFET
designed for . . .

Siliconix

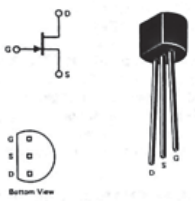
- **Low and Medium Frequency Amplifiers**

BENEFITS
- Low Cost

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –25V
Gate Current (FWD) . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 7



*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions		
1	STATIC	I_{GSS}	Gate Reverse Current		–10	nA	V_{GS} = –15 V, V_{DS} = 0		
2					–0.6	μA			T_A = 85°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–25		V	I_G = –10 μA, V_{DS} = 0		
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.4	–8.0		V_{DS} = 15 V, I_D = 1 μA		
5		V_{GS}	Gate-Source Voltage		–7.5		V_{DS} = 15 V, I_D = 100 μA		
6		I_{DSS}	Saturation Drain Current	1.0	40	mA	V_{DS} = 15 V, V_{GS} = 0		
7		$r_{ds(on)}$	Drain-Source ON Resistance		500	Ω	V_{GS} = 0, I_D = 0		
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	2000	9000	μmho	V_{DS} = 15 V, V_{GS} = 0		f = 1 kHz
9		g_{os}	Common-Source Output Conductance		200				
10		g_{fs}	Common-Source Forward Transconductance	1800					f = 1 MHz
11		C_{iss}	Common-Source Input Capacitance		20	pF			
12		C_{rss}	Common-Source Reverse Transfer Capacitance		5.0				
13		NF	Common-Source Spot Noise Figure		3.0	dB	V_{DS} = 15 V, I_D = 1 mA	R_G = 150k Ω	f = 1 kHz NBW = 150 Hz
14		$\bar{e}_N$	Equivalent Short Circuit Input Noise Voltage		50	$\frac{nV}{\sqrt{Hz}}$			

*JEDEC registered data

© 1979 Siliconix Incorporated

n-channel JFET
designed for . . .

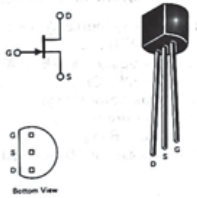
- **VHF/UHF Amplifiers**
- **Mixers**
- **Oscillators**

Siliconix

Performance Curves NH
See Section 5

BENEFITS
- Specified for 200 MHz Operation

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage 30V
Source-Gate Voltage 30V
Drain-Source Voltage. 30V
Forward Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–250	pA	V_{GS} = –20 V, V_{DS} = 0	
2					–15	nA		T_A = +85°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–30		V	I_G = –1 µA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–0.5	–8.0		V_{DS} = 15 V, I_D = 1 µA	
5		I_{DSS}	Saturation Drain Current	4.0	25	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
6		$r_{DS(on)}$	Drain-Source ON Resistance		300	Ω	I_D = 1 mA, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	4,500	10,000	µmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		$Re_{(Yfs)}$	Common-Source Forward Transconductance	4,000				f = 200 MHz
9		$Re_{(Yos)}$	Common-Source Output Conductance		150			
10		$Re_{(Yis)}$	Common-Source Input Conductance		800			
11		C_{iss}	Common-Source Input Capacitance		6.0	pF		f = 1 MHz
12		C_{rss}	Common-Source Reverse Transfer Capacitance		2.0			
13		NF	Noise Figure		3.0	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1K Ω	f = 200 MHz
14					5.0		V_{DS} = 15 V, V_{GS} = 0, R_G = 1M Ω, BW = 5 Hz	f = 10 Hz
15		G_{PS}	Common-Source Power Gain	15			V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz

NH

NOTE:
1. Pulse test PW = 300 µs; duty cycle ≤ 3%.

© 1979 Siliconix Incorporated

n-channel JFETs
designed for . . .

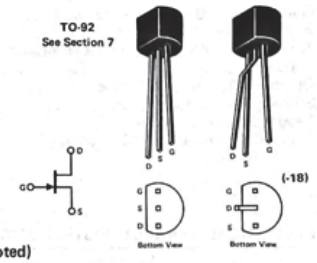
- **Analog Switches**
- **Choppers**
- **Commutators**

Siliconix

Performance Curves NC
See Section 5

BENEFITS
- Low Insertion Loss
  $R_{DS(on)}$ < 30 Ω (U1897E)
- No Error or Offset Voltage Generated by Closed Switch
  Purely Resistive

TO-92
See Section 7



ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –40V
Gate Current. . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C). . . . . 360 mW
Operating Temperature Range. . . . . –55 to 135°C
Storage Temperature Range. . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		U1897 Min	U1897 Max	U1898 Min	U1898 Max	U1899 Min	U1899 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	–40		–40		–40		V	I_G = –1 µA, V_{DS} = 0	
2		BV_{DGO}	Drain-Gate Breakdown Voltage	40		40		40			I_G = –1 µA, I_S = 0	
3		BV_{SGO}	Source-Gate Breakdown Voltage	40		40		40			I_G = –1 µA, I_D = 0	
4		I_{GSS}	Gate Reverse Current		–400		–400		–400	pA	V_{GS} = –20 V, V_{DS} = 0	
5		I_{DGO}	Drain-Gate Leakage Current		200		200		200		V_{DG} = 20 V, I_S = 0	
6		I_{SGO}	Source-Gate Leakage Current		200		200		200		V_{SG} = 20 V, I_D = 0	
7		$I_{D(off)}$	Drain Cutoff Current		200		200		200		V_{DS} = 20 V, V_{GS} = –12 V (U1897E) V_{GS} = –8 V (U1898E) V_{GS} = –6 V (U1899E)	
8					10		10		10	nA		T_A = 85°C
9		$V_{GS(off)}$	Gate-Source Cutoff Voltage	–5.0	–10	–2.0	–7.0	–1.0	–5.0	V	V_{DS} = 20 V, I_D = 1 nA	
10		I_{DSS}	Saturation Drain Current (Note 1)	30		15		8.0		mA	V_{DS} = 20 V, V_{GS} = 0	
11		$V_{DS(on)}$	Drain-Source ON Voltage		0.2		0.2		0.2	V	V_{GS} = 0, I_D = 6.6 mA (U1897E) I_D = 4.0 mA (U1898E), I_D = 2.5 mA (U1899E)	
12		$r_{DS(on)}$	Static Drain-Source ON Resistance		30		50		80	Ω	I_D = 1 mA, V_{GS} = 0	
13	DYNAMIC	C_{DG}	Drain-Gate Capacitance		5		5		5	pF	V_{DG} = 20 V, I_S = 0	
14		C_{SG}	Source-Gate Capacitance		5		5		5		V_{SG} = 20 V, I_D = 0	
15		C_{iss}	Common-Source Input Capacitance		16		16		16		V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
16		C_{rss}	Common-Source Reverse Transfer Capacitance		3.5		3.5		3.5			
17		$t_{d(on)}$	Turn ON Delay Time		15		15		20	ns	Switching Time Test Conditions	
18		t_r	Rise Time		10		20		40			
19		t_{off}	Turn OFF Time		40		60		80			

Switching Time Test Conditions	U1897E	U1898E	U1899E
V_{DD}	3 V	3 V	3 V
$V_{GS(on)}$	0	0	0
$V_{GS(off)}$	–12 V	–8 V	–6 V
R_L	430 Ω	700 Ω	1100 Ω
$I_{D(on)}$	6.6 mA	4 mA	2.5 mA

NC

NOTE:
1. Pulse test pulsewidth = 300 µs; duty cycle ≤ 3%.

© 1979 Siliconix Incorporated

n-channel silicon JFET

Siliconix

designed for . . .

- **VHF Amplifiers**
- **Mixers**

Performance Curves NH
See Section 5

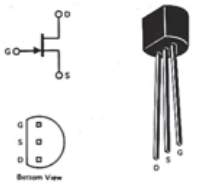
BENEFITS

- Low Noise
  NF = 3 dB Typical at 400 MHz
- Wideband
  High G_{fs}/C_{iss} Ratio
- Specified for Operation at 400 MHz

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . –30V
Forward Gate Current . . . . . 10 mA
Total Device Dissipation at 25°C Ambient
(Derate 3.27 mW/°C) . . . . . 360 mW
Operating Temperature Range . . . . . –55 to 135°C
Storage Temperature Range . . . . . –55 to 150°C
Lead Temperature Range
(1/16" from case for 10 seconds) . . . . . 300°C

TO-92
See Section 7



ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		–100	pA	V_{GS} = –20 V, V_{DS} = 0	
2					–10	nA		T_A = 100°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	–30		V	I_G = –1 μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage		–6	V	V_{DS} = 15 V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	–1.0	–5.5	V	V_{DS} = 15 V, I_D = 500 μA	
6		I_{DSS}	Saturation Drain Current (Note 1)	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	4500	7500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
8		g_{os}	Common-Source Output Conductance		50	μmho		
9		C_{rss}	Common-Source Reverse Transfer Capacitance		1	pF		
10		C_{iss}	Common-Source Input Capacitance		4	pF		f = 1 MHz
11		C_{oss}	Common-Source Output Capacitance		2			

		Characteristic		100 MHz Min	100 MHz Max	400 MHz Min	400 MHz Max	Unit	Test Conditions
12	HI FREQ	g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0
13		b_{iss}	Common-Source Input Susceptance		2500		10,000	μmho	
14		g_{oss}	Common-Source Output Conductance		75		100	μmho	
15		b_{oss}	Common-Source Output Susceptance		1000		4000	μmho	
16		g_{fs}	Common-Source Forward Transconductance (Note 1)			4000		μmho	
17		G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
18		NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1K Ω

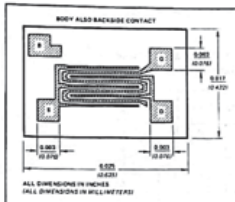
NOTE:
1. Pulse test duration = 300 μs.

NH

© 1979 Siliconix incorporated

geometry
characteristics

index 5



enhancement-type p-channel MOSFET

designed for . . .

- Analog and Digital Switching
- General Purpose Amplifiers
- Smoke Detectors

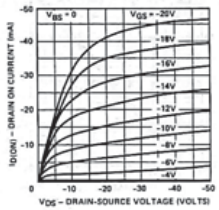
BENEFITS:

- **High Gate Transient Voltage Breakdown Eliminates Need for Gate Protective Diode**
- **Ultra-High Input Impedance**
- **Low Leakage**
- **Normally OFF**

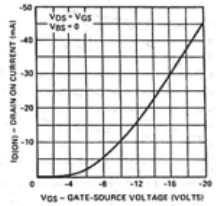
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18	MFE823
Single	TO-72	3N163-64
Single	Chip	3N163-64CHP, MFE823CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

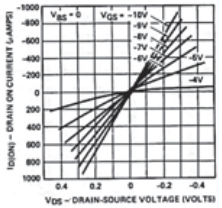
Output Characteristics



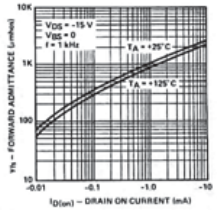
Transfer Characteristic



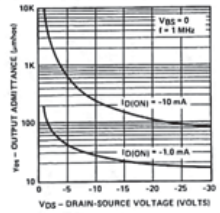
Low-Level Output Characteristics



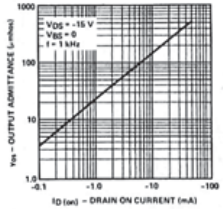
Common-Source, Short-Circuit, Forward Transadmittance vs Drain Current



Common-Source, Short-Circuit, Output Admittance vs Drain Voltage



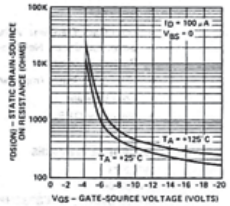
Common-Source, Short-Circuit, Output Admittance vs Drain Current



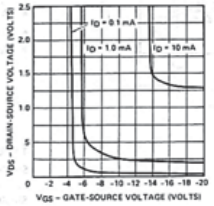
© 1979 Siliconix Incorporated

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

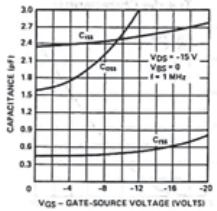
Drain-Source ON Resistance vs Gate-Source Voltage



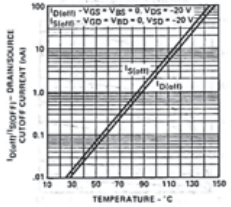
Low-Level ON Drain-Source Voltage vs Gate-Source Voltage



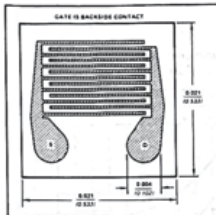
Capacitance vs Gate-Source Voltage



Drain-Source Leakage Current vs Temperature



© 1979 Siliconix incorporated



n-channel JFETs
designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

Siliconix

BENEFITS:

- No Offset or Error Voltages Generated by Closed Switch. Purely Resistive. High Isolation Resistance From Driver
- High Off-Isolation $I_{D(off)}$ < 100 pA
- High Speed t_{ON} < 20 ns

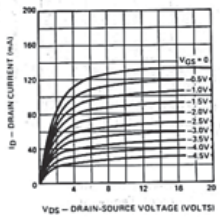
TYPE	PACKAGE
Single	TO-18
Dual	TO-71
Single	TO-92
	To-92 Lead-form
Single	Chip
Dual	Chip

PRINCIPAL DEVICES

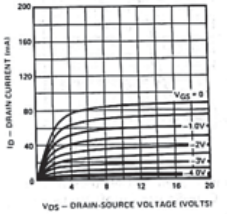
2N3970-72, 2N4091-93, 2N4391-93
2N4856-61, 2N4856A-61A, U200-02, UCR2N
2N5564-66
2N5638-40, 2N5653-54, J111-13, PN4091-93, PN4302-04, PN4391-93, U1897-99
J111-18 - J113-18, PN4302-18 - PN4304-18, PN4391-18 - PN4393-18, U1897-18 - U1899-18
All of above single devices
2N5566 CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

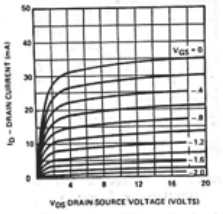
Output Characteristic



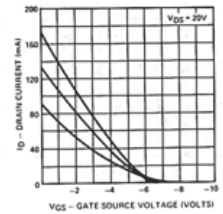
Output Characteristic



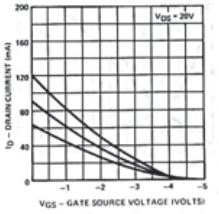
Output Characteristic



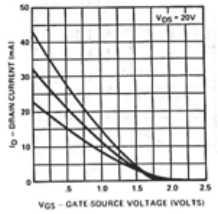
Transfer Characteristics



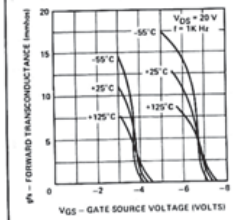
Transfer Characteristics



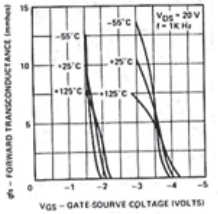
Transfer Characteristics



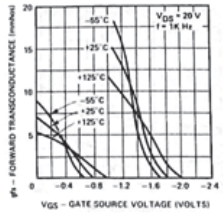
Transconductance Characteristics



Transconductance Characteristics



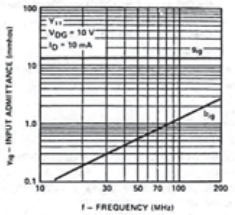
Transconductance Characteristics



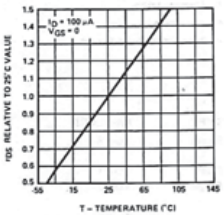
© 1979 Siliconix incorporated

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

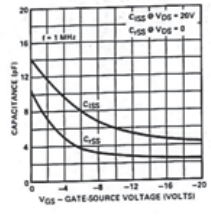
Common-Gate Input Admittance vs Frequency



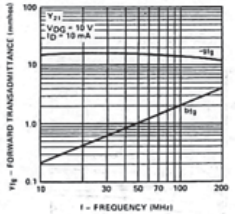
ON Resistance vs Ambient Temperature



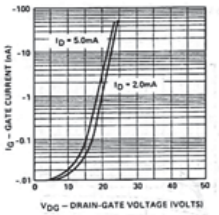
Common-Source Capacitances vs Gate-Source Voltage



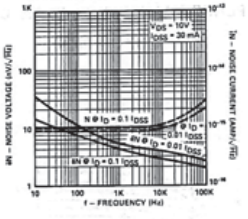
Common-Gate Forward Transadmittance vs Frequency



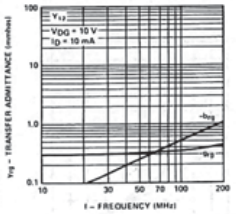
Gate Operating Current vs Drain-Gate Voltage



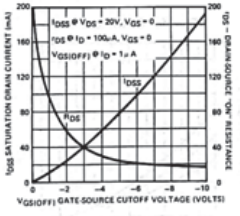
Equivalent Input Noise Voltage and Noise Current vs Frequency



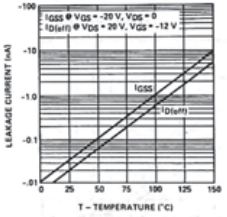
Common-Gate Reverse Transfer Admittance vs Frequency



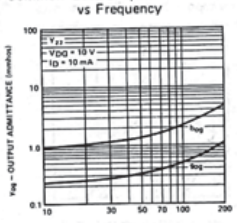
Drain Current & ON Resistance vs Gate-Source Cutoff Voltage



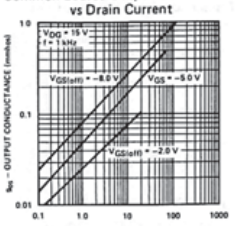
Leakage Current vs Ambient Temperature



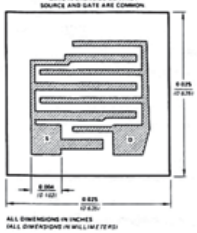
Common-Gate Output Admittance vs Frequency



Common-Source Output Conductance vs Drain Current



© 1979 Siliconix Incorporated



n-channel JFET current regulator diode *designed for . . .*

Siliconix

- Current Regulation
- Current Limiting
- Biasing

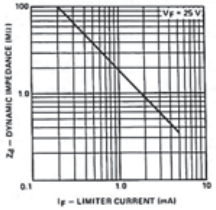
BENEFITS:

- Simple Two Lead Current Source
- Simplifies Floating Current Sources No Power Supplies Required
- Low Cost

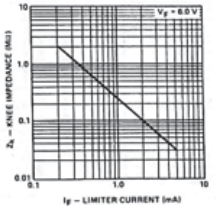
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-92	J500-505, J506-511
Single	Chip	J500CHP-505CHP, J506CHP-511CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

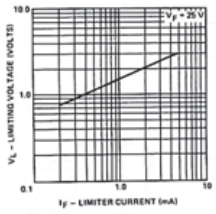
Dynamic Impedance vs Limiter Current



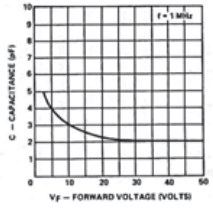
Knee Impedance vs Limiter Current



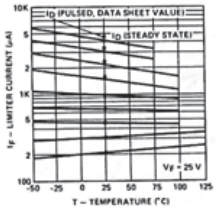
Limiting Voltage at 0.9 I_D vs Limiter Current



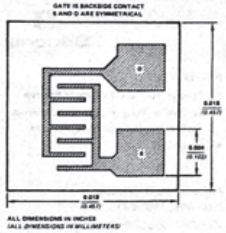
Capacitance vs Forward Voltage



Typical Variation of I_D with Temperature Steady State and Pulsed Value



© 1979 Siliconix Incorporated



n-channel JFET
designed for . . .

Siliconix

- Low and Medium Frequency Single and Differential Amplifiers
- High Input Impedance Amplifiers

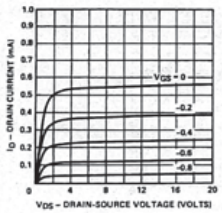
BENEFITS:

- Wide Dynamic Range
  I_G Specified @ V_{DG} = 20 V
- Low Capacitance C_{iss} < 4 pF
- Low Output Conductance

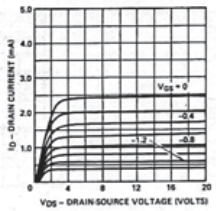
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-71	2N3954, 2N3954A, 2N3955, 2N3955A, 2N3956-8, 2N5452-54
Single	TO-72	2N3684-7
Dual	Chip	2N3955CHP, 2N3956CHP-8CHP, 2N5454CHP
Single	Chip	2N3684CHP-7CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

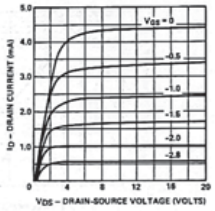
Output Characteristic



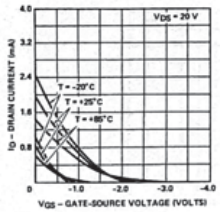
Output Characteristic



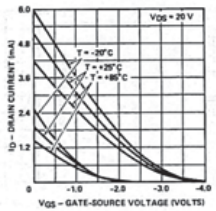
Output Characteristic



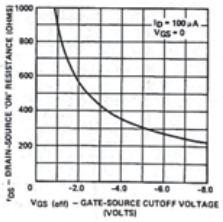
Transfer Characteristics



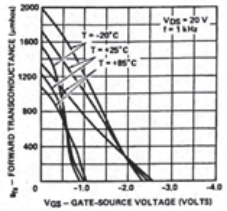
Transfer Characteristics



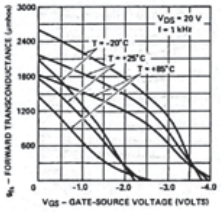
Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



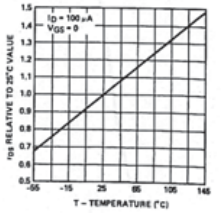
Transconductance Characteristics



Transconductance Characteristics



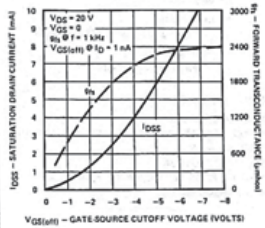
'ON' Resistance vs Ambient Temperature



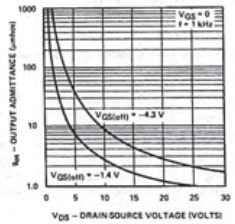
© 1979 Siliconix Incorporated

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

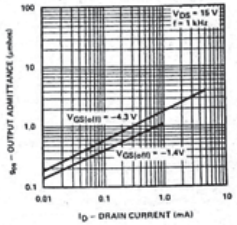
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



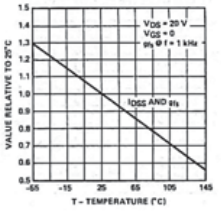
Common-Source Output Conductance vs Drain-Source Voltage



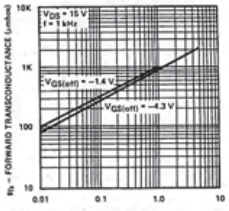
Common-Source Output Conductance vs Drain Current



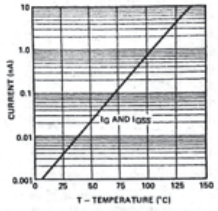
Drain Current and Transconductance vs Ambient Temperature



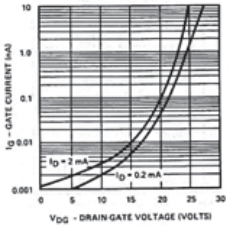
Common-Source Forward Transconductance vs Drain Current



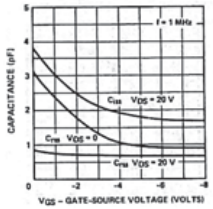
Leakage Currents vs Ambient Temperature



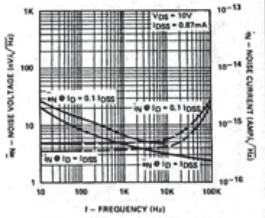
Gate Operating Current vs Drain-Gate Voltage



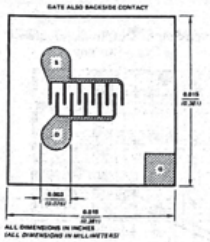
Common-Source Input Capacitance vs Gate-Source Voltage



Equivalent Input Noise Voltage and Noise Current vs Frequency



© 1979 Siliconix Incorporated



n-channel JFET
designed for . . .

- VHF/UHF Amplifiers
- Oscillators
- Mixers
- Low Input Capacitance High Speed Switch

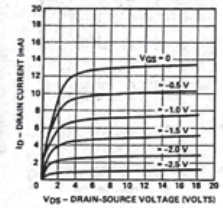
BENEFITS:

- Low Noise
  NF = 3 dB Typical @ 400 MHz
- Wideband
  High g_{fs}/C_{iss} Ratio

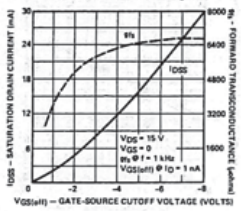
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N3966, 2N4416-16A
Single	TO-92	2N5484-6, 2N5555, 2N5668-70, MPF102, MPF108, MPF112, PN4416, J304-5, U1837, U1994
Single	TO-92 Lead-form	KK4416-18, K304-18, KK305-18, K1837-18
Single	Chip	All of the above devices

PERFORMANCE CURVES (25°C unless otherwise noted)

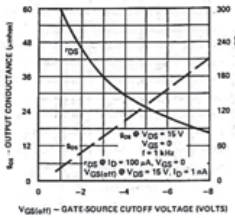
Output Characteristic



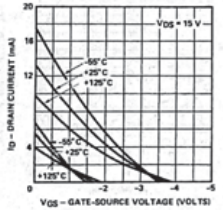
Drain Current & Transconductance vs Gate-Source Voltage



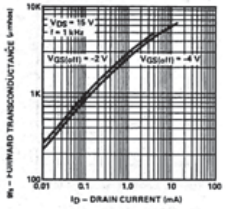
'ON' Resistance & Output Conductance vs Gate-Source Cutoff Voltage



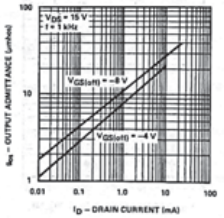
Transfer Characteristics



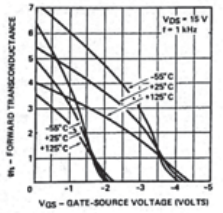
Common-Source Forward Transconductance vs Drain Current



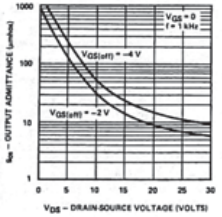
Common-Source Output Conductance vs Drain Current



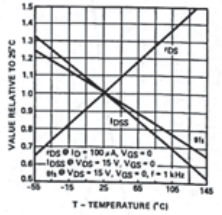
Transconductance Characteristics



Common-Source Output Conductance vs Drain-Source Voltage



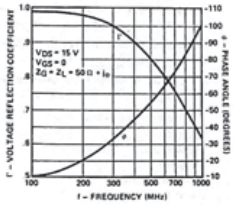
Drain Current, Transconductance and 'ON' Resistance vs Ambient Temperature



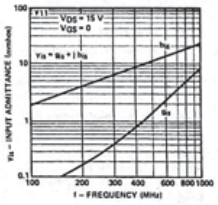
© 1979 Siliconix Incorporated

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

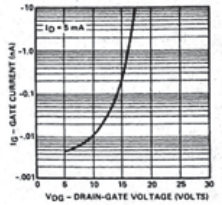
S Parameters S_{11} Common-Source vs Frequency



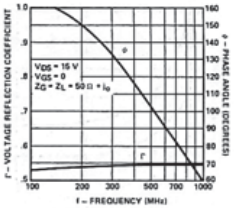
Common-Source Input Admittance vs Frequency



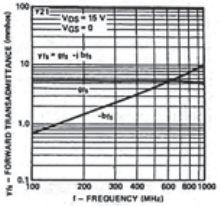
Gate Operating Current vs Drain-Gate Voltage



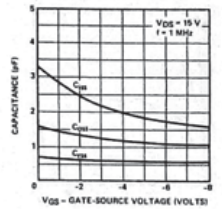
S Parameters S_{21} Common-Source vs Frequency



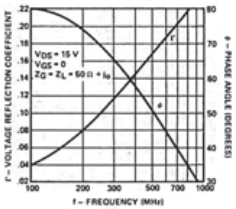
Common-Source Forward Transadmittance vs Frequency



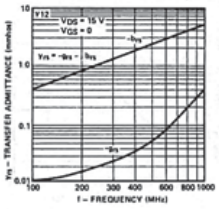
Common-Source Capacitances vs Gate-Source Voltage



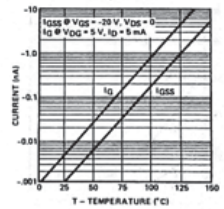
S Parameters S_{12} Common-Source vs Frequency



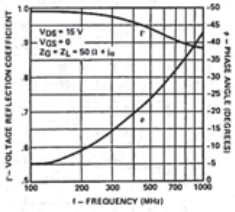
Common-Source Reverse Transfer Admittance vs Frequency



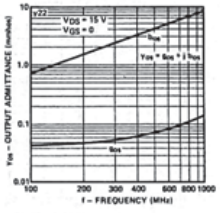
Gate Current vs Ambient Temperature



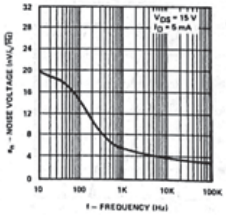
S Parameters S_{22} Common-Source vs Frequency



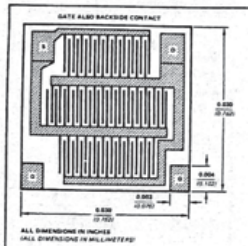
Common-Source Output Admittance vs Frequency



Equivalent Input Noise Voltage vs Frequency



© 1979 Siliconix Incorporated



n-channel JFET

designed for . . .

- Low ON Resistance Analog Switches
- Commutators
- Choppers
- Integrator Reset Capacitors
- Low Noise Audio Amplifiers

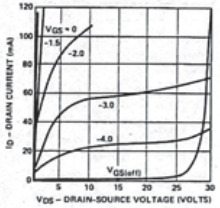
BENEFITS:

- Low Insertion Loss
- Small Error in Measurement Systems
  $V_{DS(on)}$ < 50 mV (2N5432)
- High Off-Isolation $I_{D(off)}$ < 200 pA
- High Speed $t_{d(on)}$ < 4 ns
- Low Noise Audio-Freq Amplification
  e_N < 2 nV/√Hz at 1 kHz

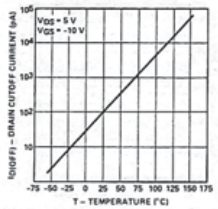
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-39	U320-2
Single	TO-52	2N5432-34
Single	TO-92	J108-10
Single	TO-92 Lead-form	J108-18 -110-18
Single	Chip	All of the above devices

PERFORMANCE CURVES (25°C unless otherwise noted)

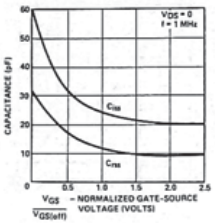
Output Characteristic



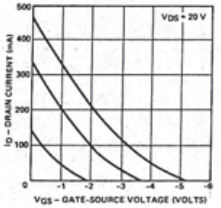
Drain Cutoff Current vs Ambient Temperature



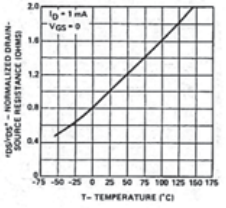
Common-Source Capacitance vs Normalized Gate-Source Voltage



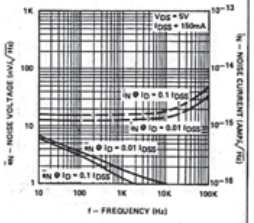
Transfer Characteristics



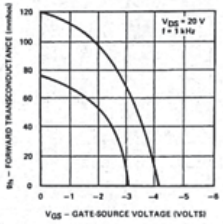
ON Resistance vs Ambient Temperature



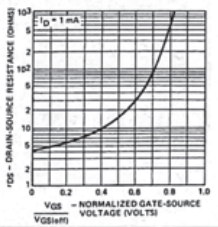
Equivalent Input Noise Voltage and Noise Current vs Frequency



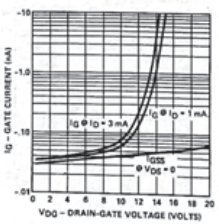
Forward Transconductance vs Drain Current



Resistance vs Normalized Gate-Source Voltage



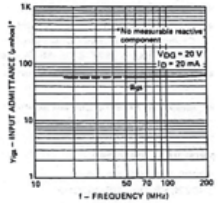
Gate Currents vs Drain-Gate Voltage



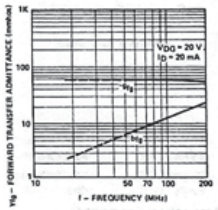
© 1979 Siliconix Incorporated

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

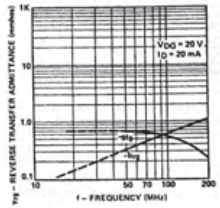
Input Admittance Common Gate vs Frequency



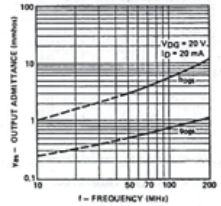
Forward Transfer Admittance Common Gate vs Frequency



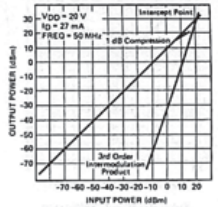
Reverse Transfer Admittance Common Gate vs Frequency



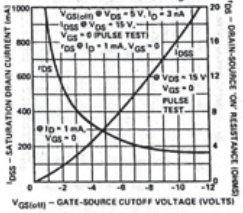
Output Admittance Common Gate vs Frequency



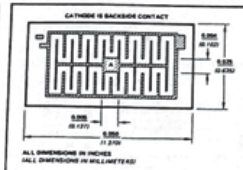
Gain – Intermodulation Characteristics



Drain Current & 'ON' Resistance vs Gate-Source Voltage



© 1979 Siliconix Incorporated



n-channel JFET current regulator diode

designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

Siliconix

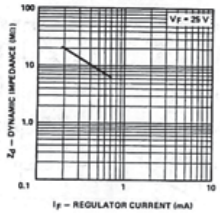
BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

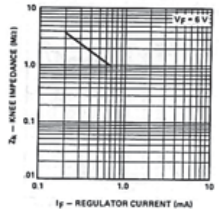
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR022 Thru CR062, U508
Single	Chip	CR022CHP Thru CR062CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

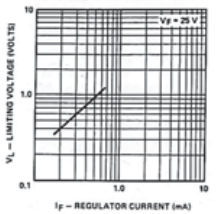
Dynamic Impedance vs Regulator Current



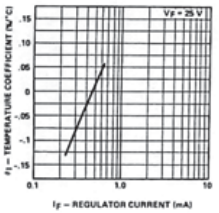
Knee Impedance vs Regulator Current



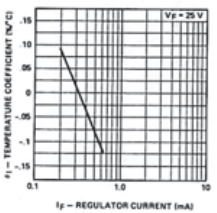
Limiting Voltage @ 0.8 IF vs Regulator Current



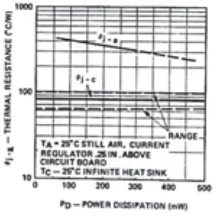
Temperature Coefficient -55°C ≤ Tj ≤ 25°C vs Regulator Current



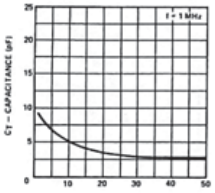
Temperature Coefficient 25°C ≤ Tj ≤ 125°C vs Regulator Current



Thermal Resistance vs Power Dissipation



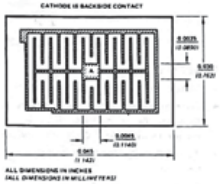
Capacitance vs Forward Voltage



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j-a}P_D = T_{case} + \theta_{j-c}P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j-c}}$ or $\frac{1}{\theta_{j-a}}$ is the derating factor for all devices.

© 1979 Siliconix Incorporated



n-channel JFET current regulator diode

designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

Siliconix

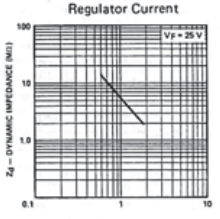
BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

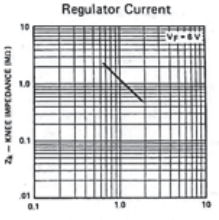
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR068 Thru CR150
Single	Chip	CR068CHP Thru CR150CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

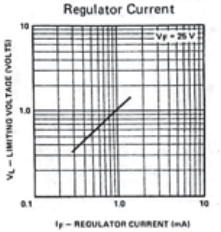
Dynamic Impedance vs Regulator Current



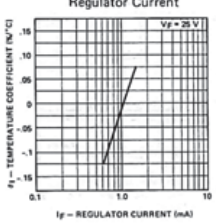
Knee Impedance vs Regulator Current



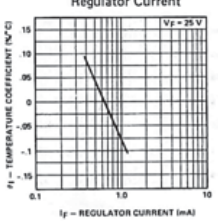
Limiting Voltage @ 0.8 IF vs Regulator Current



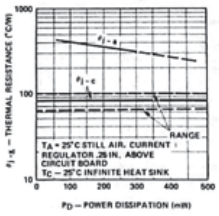
Temperature Coefficient -55°C ≤ Tj ≤ 25°C vs Regulator Current



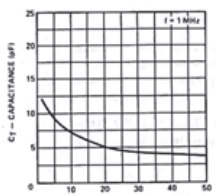
Temperature Coefficient 25°C ≤ Tj ≤ 125°C vs Regulator Current



Thermal Resistance vs Power Dissipation



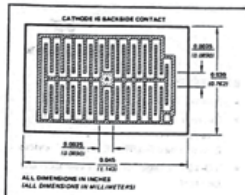
Capacitance vs Forward Voltage



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j-a}P_D = T_{case} + \theta_{j-c}P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j-c}}$ or $\frac{1}{\theta_{j-a}}$ is the derating factor for all devices.

© 1979 Siliconix Incorporated



n-channel JFET current regulator diode

designed for . . .

- Current Regulation
- Current Limiting
- Biasing
- Low Voltage References

Siliconix

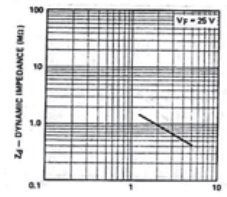
BENEFITS:

- Simple Two Lead Current Source
- Current Insensitive to Temperature Changes. Temperature Coefficient Better Than 0.15%/°C On All Devices
- TO-18 Package for Improved Current Control
- Simplifies Floating Current Sources No Power Supplies Required

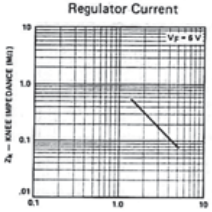
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-18 (2-lead)	CR160 Thru CR470
Single	Chip	CR160CHP Thru CR470CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

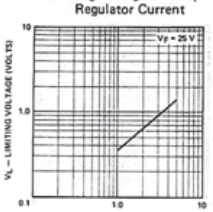
Dynamic Impedance vs Regulator Current



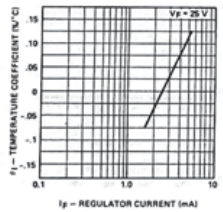
Knee Impedance vs Regulator Current



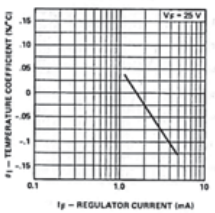
Limiting Voltage @ 0.8 IF vs Regulator Current



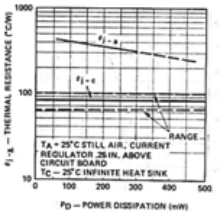
Temperature Coefficient -55°C ≤ Tj ≤ 25°C vs Regulator Current



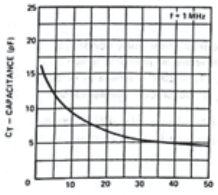
Temperature Coefficient 25°C ≤ Tj ≤ 125°C vs Regulator Current



Thermal Resistance vs Power Dissipation



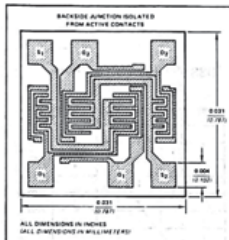
Capacitance vs Forward Voltage



NOTE: I_F, Regulator Current is specified under pulse conditions. In operation, final current will be a function of junction temperature. I_F (steady state) = $I_F \times [1 + \theta_I (T_j - 25°C)]$ where θ_I is the temperature coefficient of I_F and T_j is the junction temperature.

T_j may be found by $T_j = T_{amb} + \theta_{j\text{-}a}P_D = T_{case} + \theta_{j\text{-}c}P_D$. T_j must not exceed 150°C. $\frac{1}{\theta_{j\text{-}c}}$ or $\frac{1}{\theta_{j\text{-}a}}$ is the derating factor for all devices.

© 1979 Siliconix incorporated



monolithic dual n-channel JFET

designed for . . .

- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

Siliconix

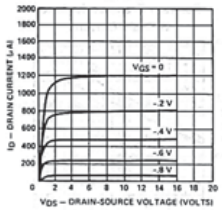
BENEFITS:

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5196)
- Low Drift With Temperature
  5 μV/°C Maximum (2N5196)

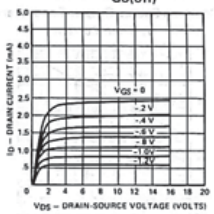
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-71	2N5196-9, 2N5545-47, U231-35
Dual	Chip	2N5199CHP, U232CHP-35CHP 2N5547CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

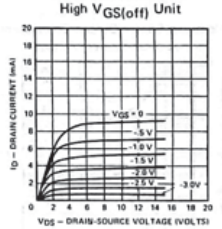
Output Characteristics Low $V_{GS(off)}$ Unit



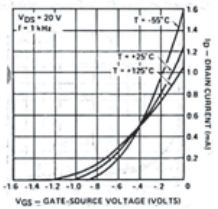
Output Characteristics Medium $V_{GS(off)}$ Unit



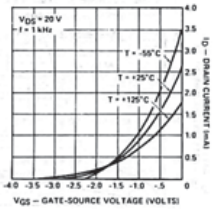
Output Characteristics High $V_{GS(off)}$ Unit



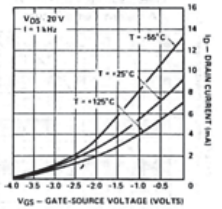
Transfer Characteristics Low $V_{GS(off)}$



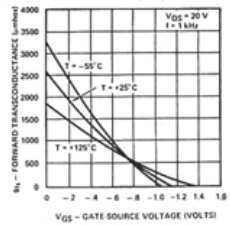
Transfer Characteristics Medium $V_{GS(off)}$



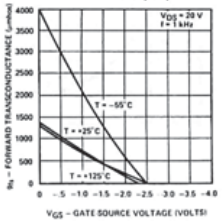
Transfer Characteristics High $V_{GS(off)}$



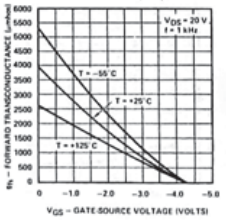
Transconductance Characteristics Low $V_{GS(off)}$



Transconductance Characteristics Medium $V_{GS(off)}$



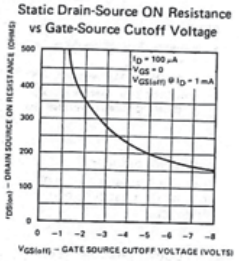
Transconductance Characteristics High $V_{GS(off)}$



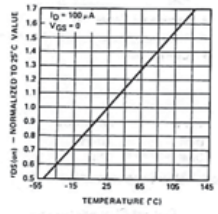
© 1979 Siliconix incorporated

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

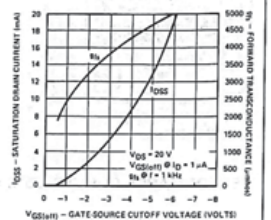
Static Drain-Source ON Resistance vs Gate-Source Cutoff Voltage



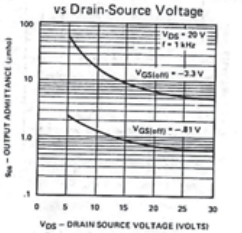
Normalized ON Resistance vs Ambient Temperature



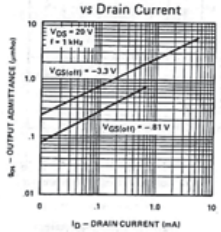
I_{DSS} and g_{fs} vs Gate-Source Cutoff Voltage



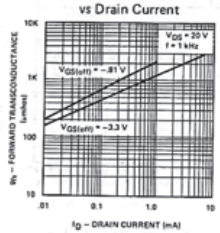
Common-Source Output Conductance vs Drain-Source Voltage



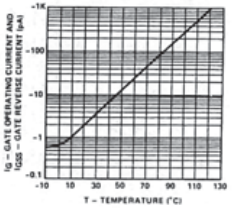
Common-Source Output Conductance vs Drain Current



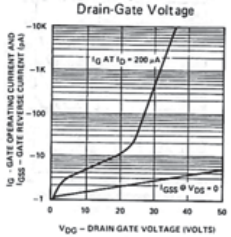
Common Source Forward Transconductance vs Drain Current



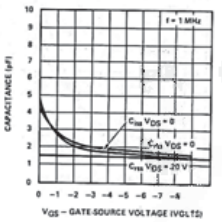
Gate Leakage Currents vs Ambient Temperature



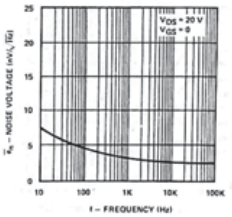
Gate Leakage Currents vs Drain-Gate Voltage



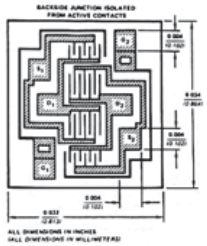
Capacitance vs Gate-Source Voltage



Equivalent Input Noise Voltage vs Frequency



© 1979 Siliconix incorporated



monolithic dual n-channel JFET

designed for . . .

- FET Input Amplifiers
- Low and Medium Frequency Amplifiers
- Impedance Converters
- Precision Instrumentation Amplifiers
- Comparators

BENEFITS:

- Minimum System Error and Calibration
  5 mV Offset Maximum (J401)
  95 dB Minimum CMRR
- Low Drift With Temperature
  10 μV/°C (J401)
- Simplifies Amplifier Design
  Output Conductance < 2 μmho
- Low Noise
  $\overline{e_n}$ = 6 nV/$\sqrt{Hz}$ at 10 Hz Typical

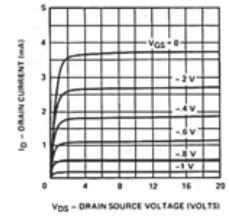
TYPE	PACKAGE
Dual	TO-71
Dual	Chip

PRINCIPAL DEVICES

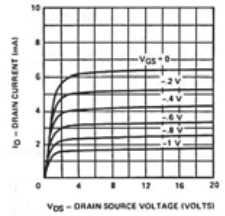
2N3921-2, 2N4084-5, 2N5045-7, U401-6
2N4085CHP, 2N5046CHP-47CHP,
U403CHP-06CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

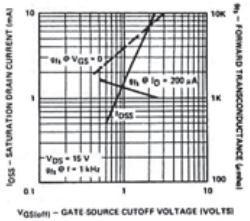
Output Characteristics Low $V_{GS(off)}$ Unit (−1.5 V)



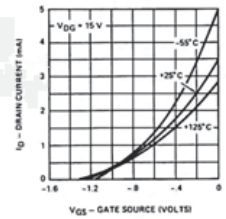
Output Characteristics Medium $V_{GS(off)}$ Unit (−2.2 V)



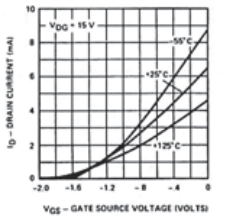
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



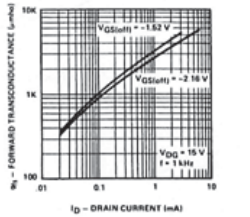
Transfer Characteristics Low $V_{GS(off)}$ Unit (−1.5 V)



Transfer Characteristics Medium $V_{GS(off)}$ Unit (−2.2 V)



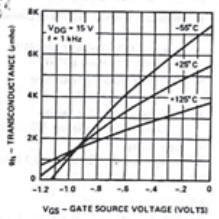
Forward Transconductance vs Drain Current



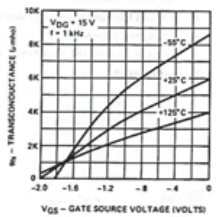
© 1979 Siliconix incorporated

PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

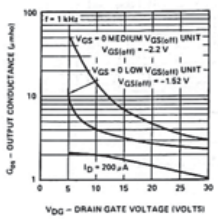
ansconductance vs Gate Source Voltage
Low $V_{GS(off)}$ Unit (−1.5 V)



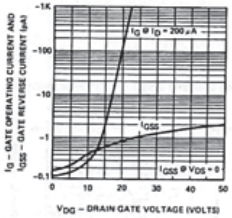
Transconductance vs Gate Source Voltage
Medium $V_{GS(off)}$ Unit (−2.2 V)



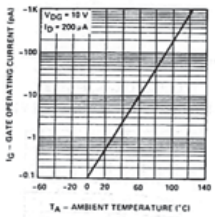
Output Conductance
vs Drain Gate Voltage



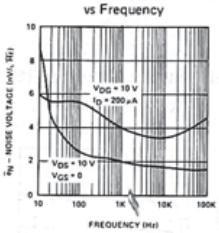
Gate Operating Current
vs Drain Gate Voltage



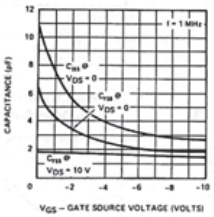
Gate Operating Current
vs Ambient Temperature



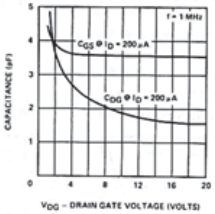
Equivalent Short Circuit Input Noise
vs Frequency



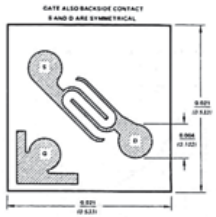
Capacitance vs Gate Source Voltage



Capacitance vs Drain to Gate Voltage



© 1979 Siliconix incorporated



n-channel JFET
designed for . . .

- Small Signal Amplifiers
- Choppers
- Voltage-Controlled Resistors

TYPE	PACKAGE
Single	TO-18
Dual	TO-71
Single	TO-92
Single	TO-92 Lead-form
Single	Chip

Siliconix

BENEFITS:

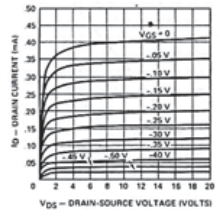
- Low Noise NF < 1 dB at 1 kHz
- Operation From Low Power Supply Voltages, $V_{GS(off)}$ < 1 V (2N4338)
- High Off-Isolation As a Switch $I_{D(off)}$ < 50 pA
- High Input Impedance

PRINCIPAL DEVICES

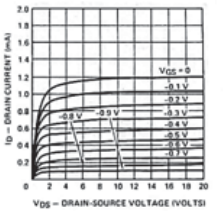
2N3368-70, 2N3436-8, 2N3458-60, 2N4338-41, VCR4N
2N5196-9, U231-5, 2N5545-47
J201-203, J204, PN4302-04
J201-18 - 203-18, J204-18,
All of the above
PN4302-18 - 4304-18

PERFORMANCE CURVES (25°C unless otherwise noted)

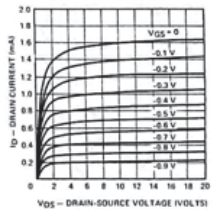
Output Characteristic



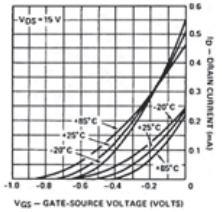
Output Characteristic



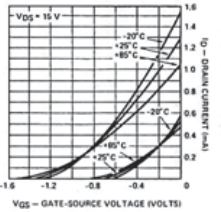
Output Characteristic



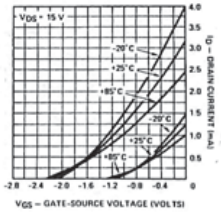
Transfer Characteristics



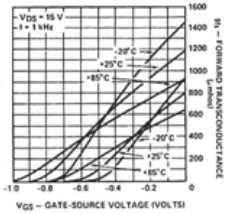
Transfer Characteristics



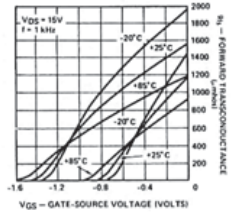
Transfer Characteristics



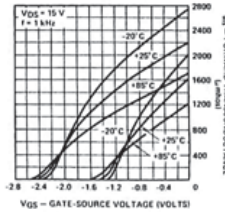
Transconductance Characteristics



Transconductance Characteristics



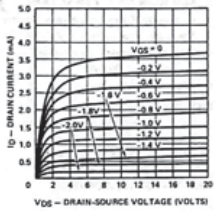
Transconductance Characteristics



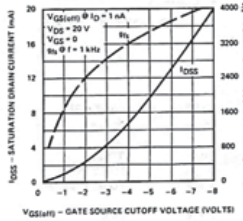
© 1979 Siliconix incorporated

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

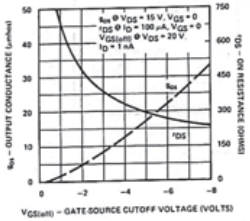
Output Characteristic



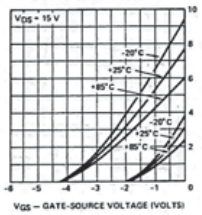
Drain Current and Transconductance vs Gate-Source Cutoff Voltage



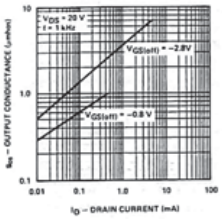
ON Resistance & Output Conductance vs Gate-Source Cutoff Voltage



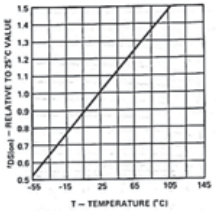
Transfer Characteristics



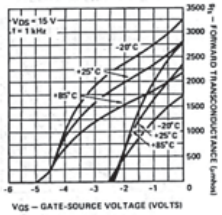
Common-Source Output Conductance vs Drain Current



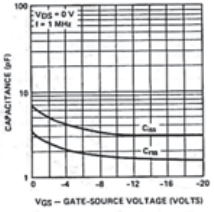
ON Resistance vs Ambient Temperature



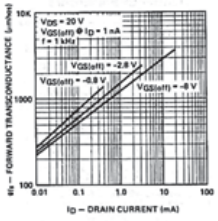
Transconductance Characteristics



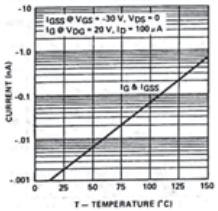
Common-Source Capacitances vs Gate-Source Voltage



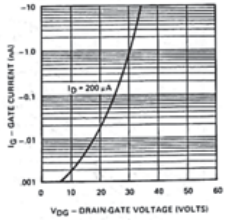
Common-Source Forward Transconductance vs Drain Current



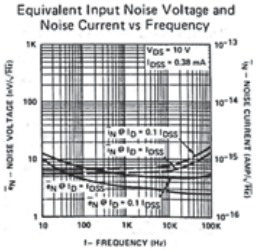
Gate Currents vs Ambient Temperature



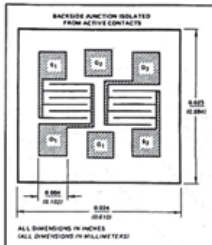
Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage and Noise Current vs Frequency



© 1979 Siliconix incorporated



monolithic dual n-channel JFET

designed for . . .

Siliconix

- General Purpose Differential Amplifiers

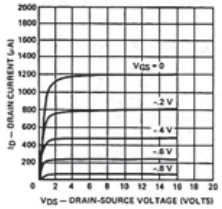
BENEFITS:

- Low Cost
- High Input Impedance

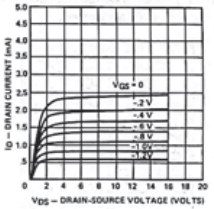
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-71	U410-12
Dual	Chip	U411CHP, U412CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

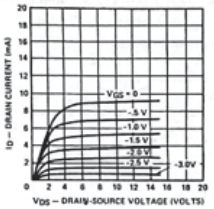
Output Characteristics Low $V_{GS(off)}$ Unit



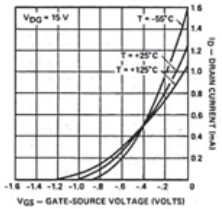
Output Characteristics Medium $V_{GS(off)}$ Unit



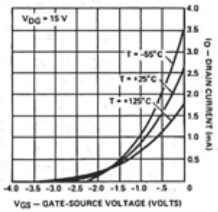
Output Characteristics High $V_{GS(off)}$ Unit



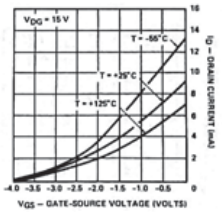
Transfer Characteristics Low $V_{GS(off)}$



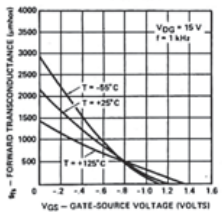
Transfer Characteristics Medium $V_{GS(off)}$



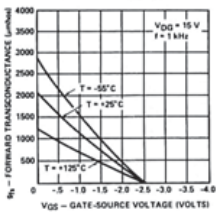
Transfer Characteristics High $V_{GS(off)}$



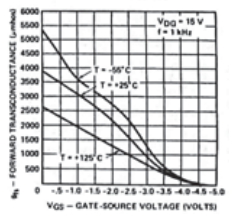
Transconductance Characteristics Low $V_{GS(off)}$



Transconductance Characteristics Medium $V_{GS(off)}$



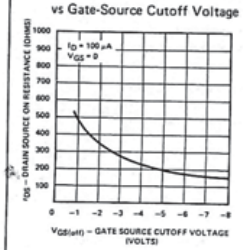
Transconductance Characteristics High $V_{GS(off)}$



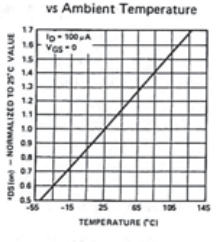
© 1979 Siliconix incorporated

PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

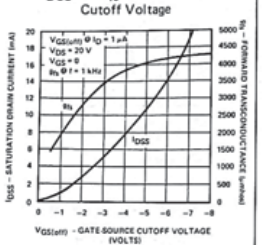
Static Drain-Source ON Resistance vs Gate-Source Cutoff Voltage



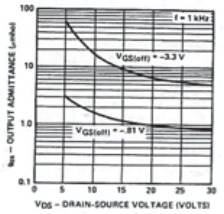
Normalized ON Resistance vs Ambient Temperature



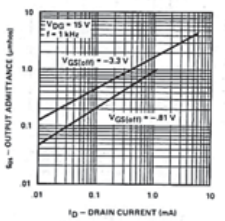
I_{DSS} and g_{fs} vs Gate-Source Cutoff Voltage



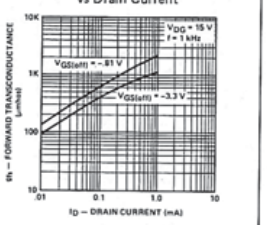
Common Source Output Admittance vs Drain-Source Voltage



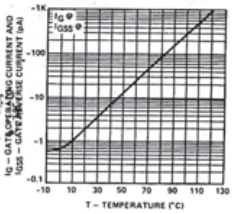
Common-Source Output Conductance vs Drain Current



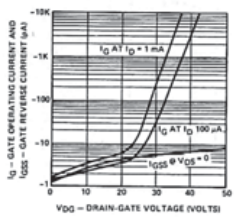
Common Source Forward Transconductance vs Drain Current



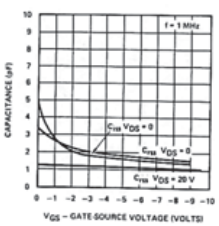
Leakage Current vs Ambient Temperature



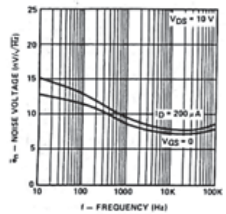
Gate Operating Current vs Drain-Gate Voltage



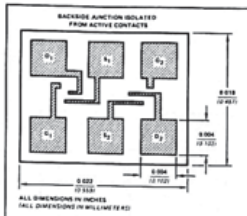
Capacitance vs Gate-Source Voltage



Equivalent Input Noise Voltage vs Frequency



© 1979 Siliconix incorporated



monolithic dual n-channel JFETs
designed for . . .

- Low Leakage FET Input Op Amps
- pH Meters
- Electrometers

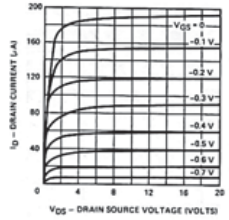
TYPE	PACKAGE
Dual	TO-78
Dual	Chip

BENEFITS:
- Ultra-High Input Impedance
- Good Voltage Gain
- Low Noise

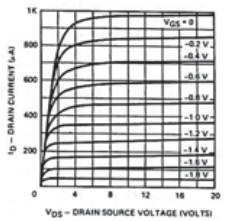
PRINCIPAL DEVICES
U421-6
U422CHP, U423CHP, U425CHP, U426CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

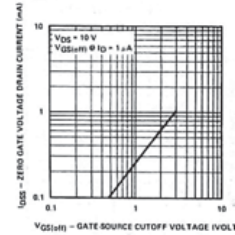
Output Characteristics Low $V_{GS(off)}$ Unit (1.0 V)



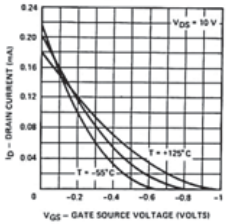
Output Characteristics High $V_{GS(off)}$ Unit (2.5 V)



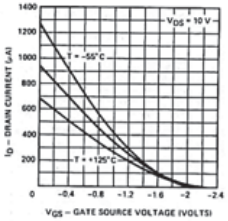
I_{DSS} vs Gate Source Cutoff Voltage



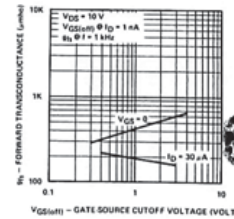
Transfer Characteristics Low $V_{GS(off)}$ Unit (1.0 V)



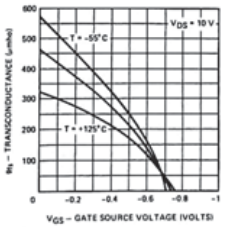
Transfer Characteristics High $V_{GS(off)}$ Unit (2.5 V)



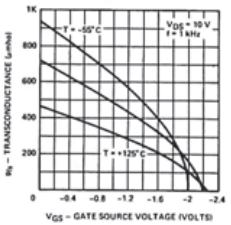
Forward Transconductance vs Gate Source Cutoff Voltage



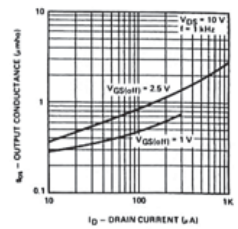
Transconductance vs Gate Source Voltage Low $V_{GS(off)}$ Unit (1.0 V)



Transconductance vs Gate Source Voltage High $V_{GS(off)}$ Unit (2.5 V)



Common-Source Output Conductance vs Drain Current



© 1979 Siliconix incorporated