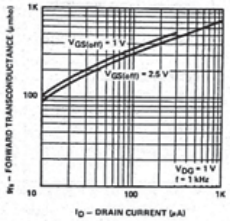
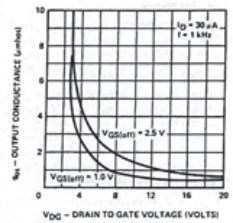
PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

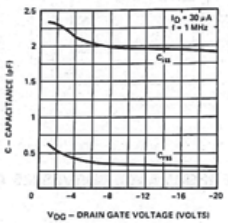
Forward Transconductance vs Drain Current



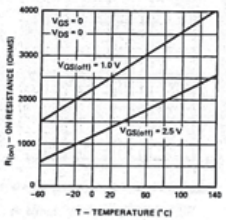
Output Conductance vs Drain to Gate Voltage



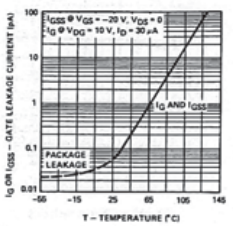
Capacitance vs Drain Gate Voltage



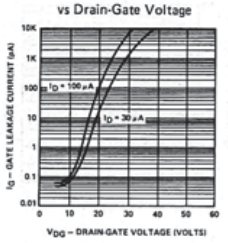
On Resistance vs Ambient Temperature



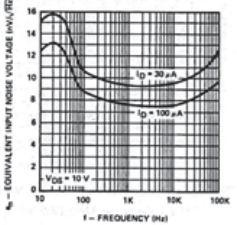
Leakage Current vs Temperature



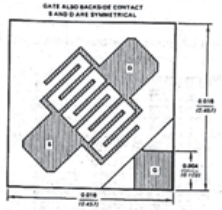
Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage vs Frequency



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n-channel JFET
designed for . . .

- Small Signal Amplifiers
- VHF Amplifiers
- Oscillators
- Mixers
- Switches

TYPE	PACKAGE
Single	TO-72
Single	TO-92
Dual	TO-71
Single	Chip

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BENEFITS:

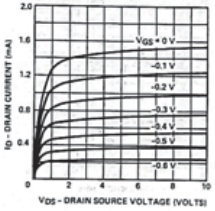
- Wide Input Dynamic Range
  High I_G Breakpoint Voltage
- High Gain
- Low Insertion Loss Switches

PRINCIPAL DEVICES

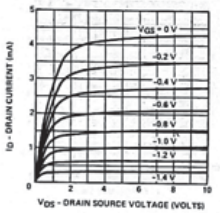
2N3821-4, 2N4220-2, 2N4220A-22A
2N4223-24, 2N5556-58
2N3819, 2N5457-9, MPF109, MPF111
2N3921-2, 2N4084-5, 2N5045-7, U401-6
All of the above except 2N3819

PERFORMANCE CURVES (25°C unless otherwise noted)

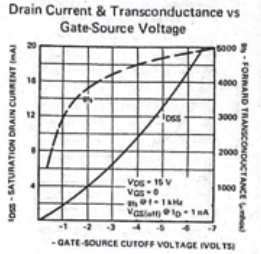
Output Characteristic



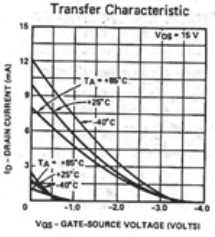
Output Characteristic



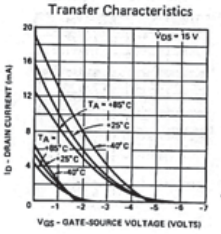
Drain Current & Transconductance vs Gate-Source Voltage



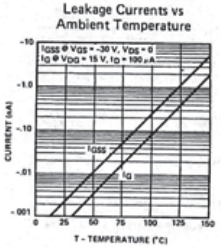
Transfer Characteristic



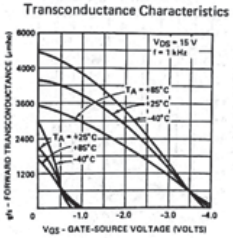
Transfer Characteristics



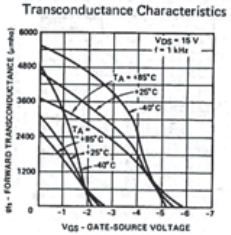
Leakage Currents vs Ambient Temperature



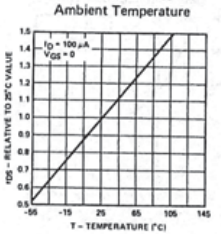
Transconductance Characteristics



Transconductance Characteristics



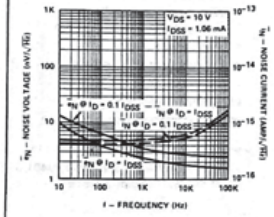
'ON' Resistance vs Ambient Temperature



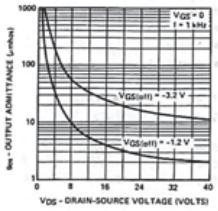
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PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

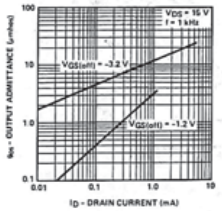
Equivalent Input Noise Voltage and Noise Current vs Frequency



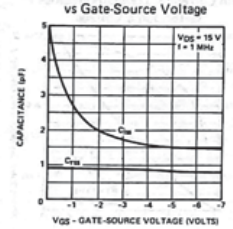
Common-Source Output Admittance vs Drain-Source Voltage



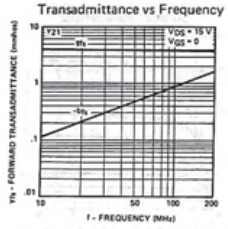
Common-Source Output Admittance vs Drain Current



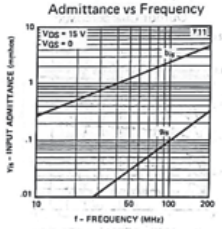
Common-Source Capacitances vs Gate-Source Voltage



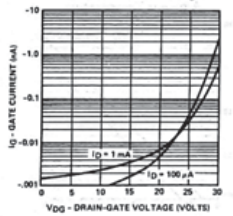
Common-Source Forward Transadmittance vs Frequency



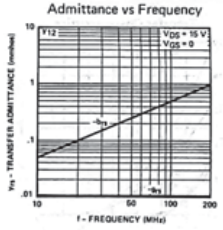
Common-Source Input Admittance vs Frequency



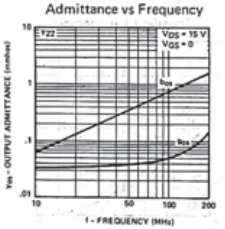
Gate Operating Current vs Drain-Gate Voltage



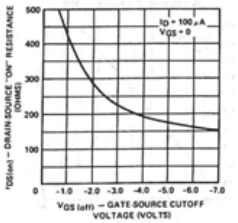
Common-Source Reverse Transfer Admittance vs Frequency



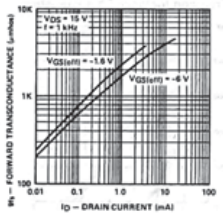
Common-Source Output Admittance vs Frequency



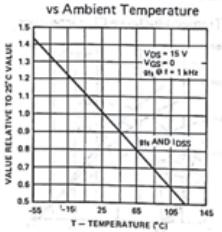
Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



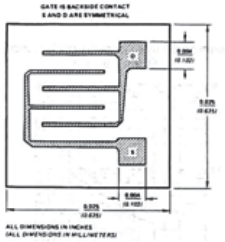
Common-Source Forward Transconductance vs Drain Current



Drain Current and Transconductance vs Ambient Temperature



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n-channel JFET
designed for . . .

- Low Noise Amplifiers
- Single and Differential Amplifiers

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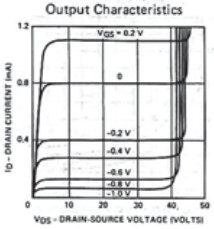
BENEFITS:

- Simplifies Amplifier Design
- Low Output Conductance
- Low 1/f Noise

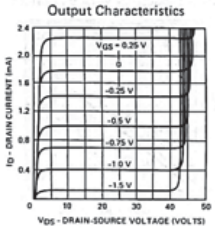
TYPE	PACKAGE	PRINCIPAL DEVICES
Dual	TO-71	2N5515-24
Single	TO-72	2N4867-9, 2N4867A-69A
Single	TO-92	J230-32
Single	TO-92 Lead-form	J230-18 - 232-18
Dual	Chip	2N5518CHP-9CHP, 2N5523CHP-4CHP
Single	Chip	All of the above single devices

PERFORMANCE CURVES (25°C unless otherwise noted)

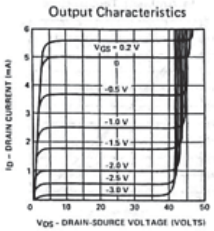
Output Characteristics



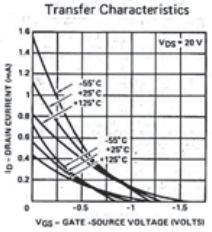
Output Characteristics



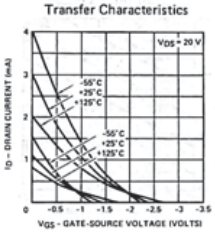
Output Characteristics



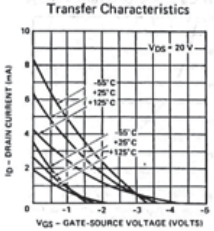
Transfer Characteristics



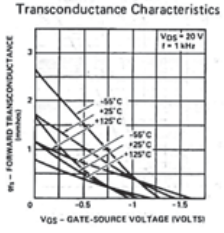
Transfer Characteristics



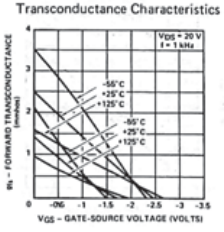
Transfer Characteristics



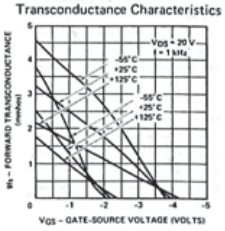
Transconductance Characteristics



Transconductance Characteristics



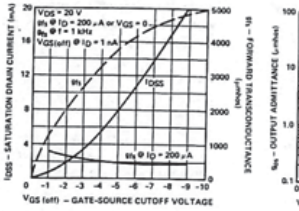
Transconductance Characteristics



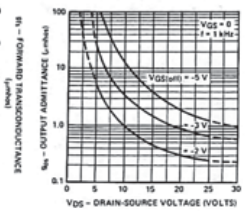
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PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

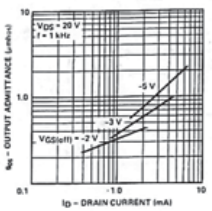
Saturation Drain Current and Forward Transconductance vs. Gate-Source Cutoff Voltage



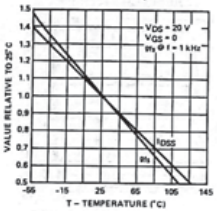
Common-Source Output Conductance vs Drain-Source Voltage



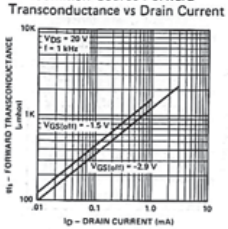
Common-Source Output Conductance vs Drain Current



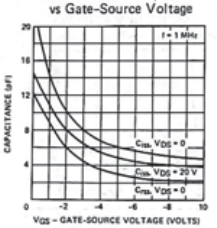
Drain Current & Transconductance vs Ambient Temperature



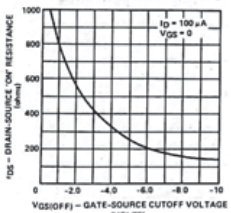
Common-Source Forward Transconductance vs Drain Current



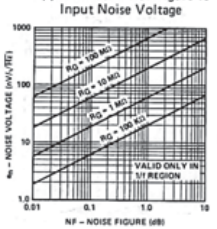
Common-Source Capacitance vs Gate-Source Voltage



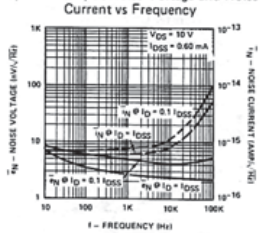
Static Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



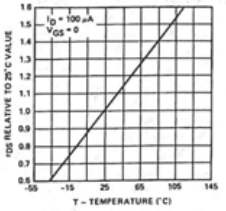
Approximate Noise Figure vs Input Noise Voltage



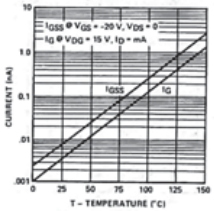
Equivalent Input Noise Voltage and Noise Current vs Frequency



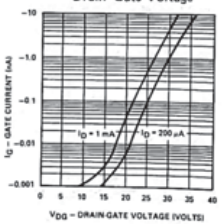
Drain-Source 'ON' Resistance vs Ambient Temperature



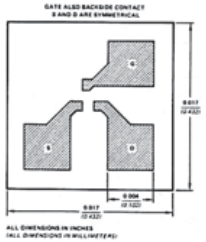
Leakage Currents vs Ambient Temperature



Gate Operating Current vs Drain-Gate Voltage



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n-channel JFET
designed for . . .

Siliconix

- Ultra-High Input Impedance Amplifiers
  - Electrometers
  - pH Meters
  - Smoke Detectors

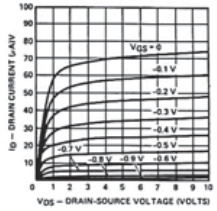
BENEFITS:

- Low Power
  I_{DSS} < 90 μA (2N4117)
- High Input Impedance
  I_G < 1 pA (2N5906-09)

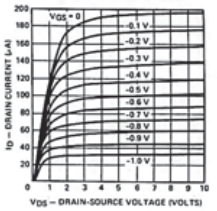
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-72	2N4117-9, 2N4117A-9A, VCR7N
Dual	TO-78	2N5902-9
Single	Chip	2N4117CHP-9CHP, 2N4117ACHP-9ACHP, VCR7NCHP
Dual	Chip	2N5905CHP, 2N5909CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

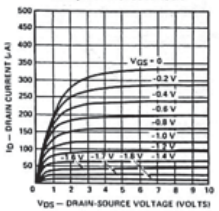
Output Characteristic



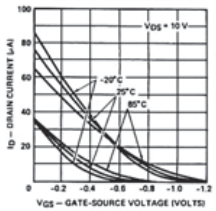
Output Characteristic



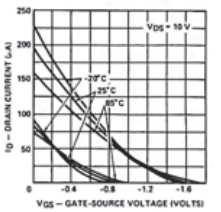
Output Characteristic



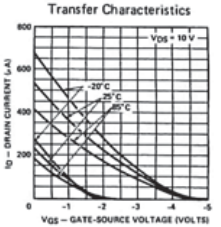
Transfer Characteristics



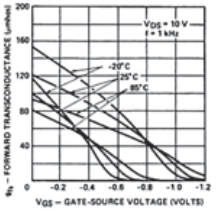
Transfer Characteristics



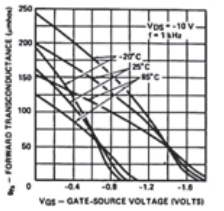
Transfer Characteristics



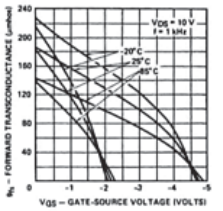
Transconductance Characteristics



Transconductance Characteristics



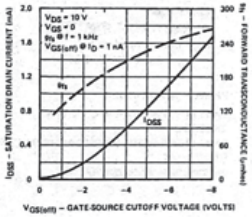
Transconductance Characteristics



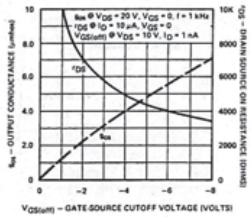
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PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

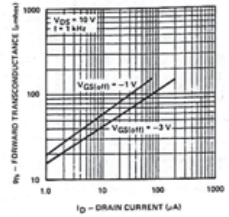
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



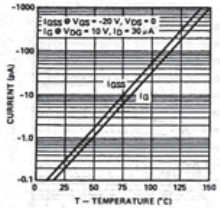
ON Resistance & Output Conductance vs Gate-Source Cutoff Voltage



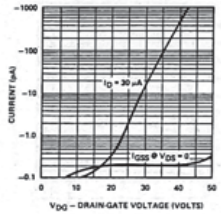
Common-Source Forward Transconductance vs Drain Current



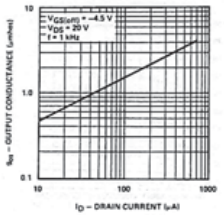
Leakage Currents vs Ambient Temperature



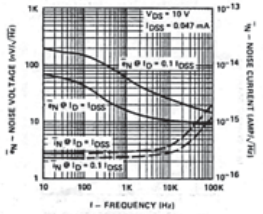
Leakage Currents vs Drain-Gate Voltage



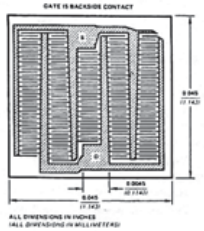
Common-Source Output Conductance vs Drain Current



Equivalent Input Noise Voltage and Noise Current vs Frequency



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n-channel JFET
designed for . . .

- Analog Switches
- Commutators
- Choppers

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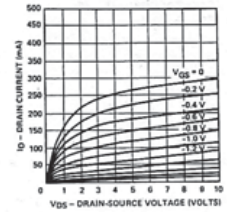
BENEFITS:

- Very Low Insertion Loss
  $R_{DS(on)} < 2.5$ Ohms (U290)
- High Off-Isolation

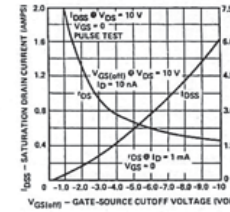
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-52	U290-1
Single	TO-92	J105-7
Single	TO-92 Lead-form	J105-18 - 107-18
Single	Chip	U290CHP-1CHP, J105CHP-7CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

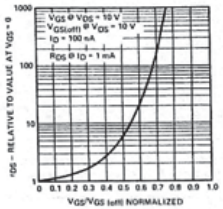
Output Characteristic



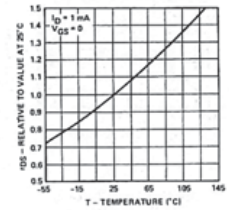
Saturation Drain Current and Drain-Source 'ON' Resistance vs Gate-Source Cutoff Voltage



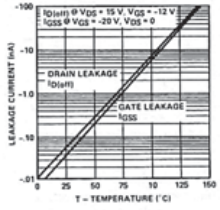
Drain-Source Resistance vs Normalized Gate-Source Voltage



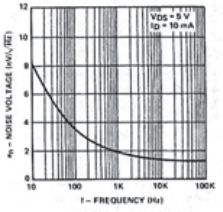
Drain-Source 'ON' Resistance vs Ambient Temperature



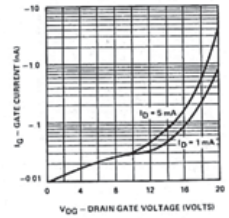
Leakage Currents vs Ambient Temperature



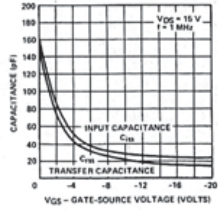
Equivalent Input Noise Voltage vs vs Frequency



Leakage Current vs Drain-Gate Voltage

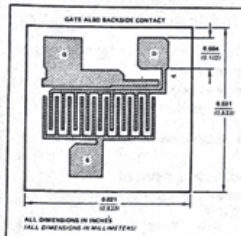


Common-Source Capacitance vs Gate-Source Voltage



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n-channel JFET
designed for . . .

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- VHF/UHF Amplifiers
- Front End High Sensitivity Amplifiers
- Oscillators
- Mixers

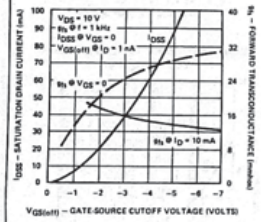
BENEFITS

- Industry Standard
- High Power Gain
  16 dB at 100 MHz, Common Gate
  11 dB at 450 MHz, Common Gate
- Low Noise
  3 dB Noise Figure at 450 MHz
- Wide Dynamic Range
  Greater Than 100 dB
- 75 Ohm Input Match Common Gate

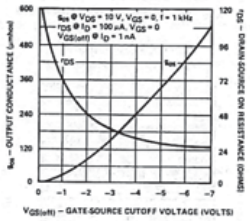
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-52	U308-10
Single	TO-72	U311
Single	TO-92	J308-10
Dual	TO-99	U430-1
Single	TO-92 Lead-form	K308-18 -310-18
Single	Chip	J308CHP-10CHP, U308CHP-10CHP, U311CHP
Dual	Chip	U430CHP-1CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

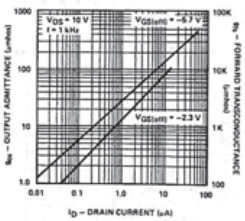
Drain Current & Transconductance vs Gate-Source Cutoff Voltage



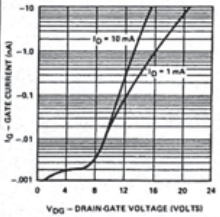
ON Resistance & Output Conductance vs Gate-Source Cutoff Voltage



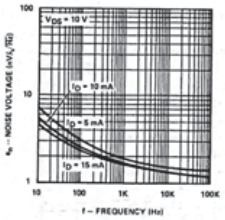
Common-Source Output Conductance vs Drain Current



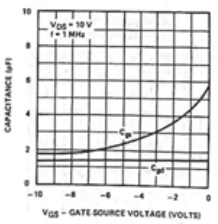
Gate Operating Current vs Drain-Gate Voltage



Equivalent Input Noise Voltage vs Frequency



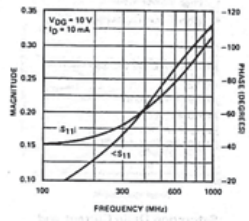
Junction Capacitance vs Gate-Source Voltage



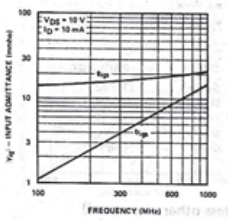
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PERFORMANCE CURVES (Con't) (25°C unless otherwise noted)

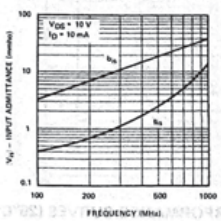
Forward Reflection Coefficient Common Gate



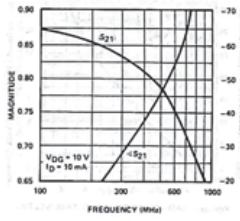
Input Admittance Common Gate



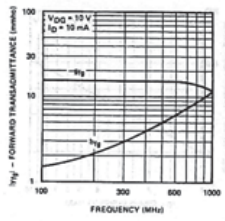
Input Admittance Common Source



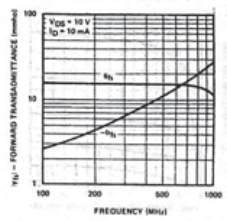
Forward Transmission Coefficient Common Gate



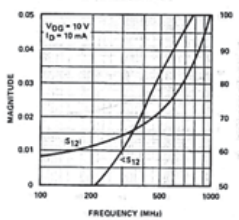
Forward Transfer Admittance Common Gate



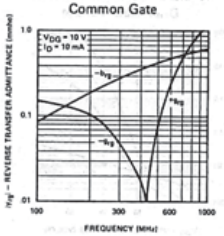
Forward Transfer Admittance Common Source



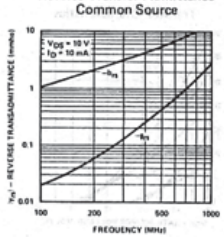
Reverse Transmission Coefficient Common Gate



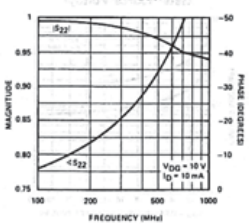
Reverse Transfer Admittance Common Gate



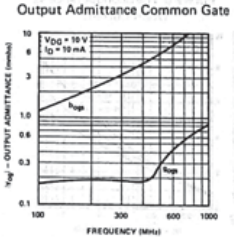
Reverse Transfer Admittance Common Source



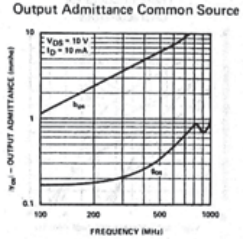
Reverse Reflection Coefficient Common Gate



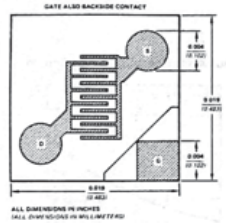
Output Admittance Common Gate



Output Admittance Common Source



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n-channel JFET
designed for . . .

- High Frequency Amplifiers
- Mixers
- Oscillators

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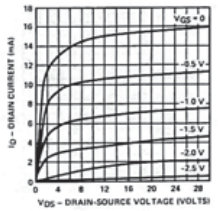
BENEFITS:
- High Power Gain
- Low Input Capacitance

TYPE	PACKAGE
Single	TO-52
Dual	TO-78
Dual	TO-71
Single	Chip
Dual	Chip

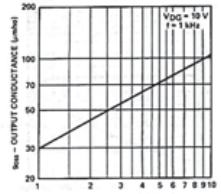
PRINCIPAL DEVICES
U312
2N5911-12, U257
U440-41
U312CHP
2N5912CHP, U257CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

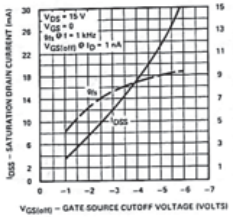
Output Characteristic



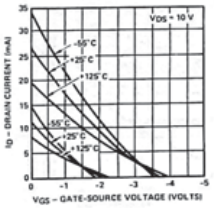
Common-Source Output Conductance vs Drain Current



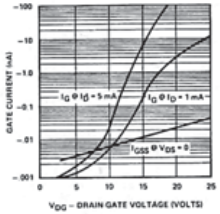
Saturation Drain Current and Forward Transconductance vs Gate-Source Cutoff Voltage



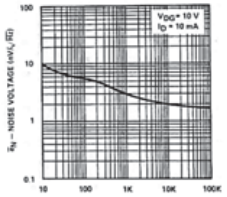
Transfer Characteristics



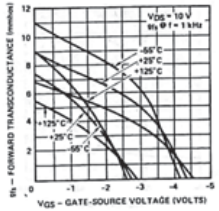
Leakage Currents vs Drain-Gate Voltage



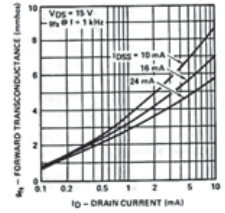
Equivalent Input Noise Voltage vs Frequency



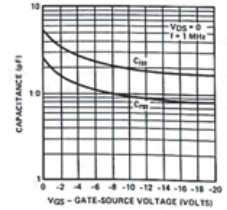
Transconductance Characteristics



Forward Transconductance vs Drain Current



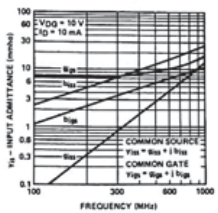
Common-Source Capacitances vs Gate-Source Voltage



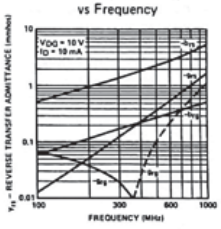
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PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

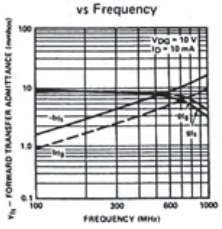
Input Admittance vs Frequency



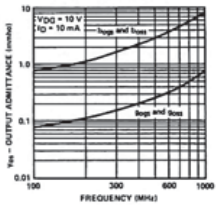
Reverse Transfer Admittance vs Frequency



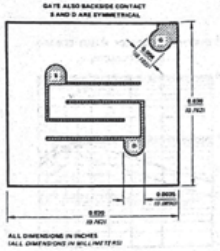
Forward Transfer Admittance vs Frequency



Output Admittance vs Frequency



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- General Purpose Amplifiers and Attenuators

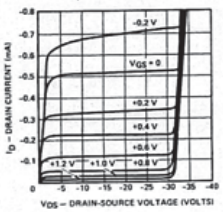
TYPE	PACKAGE
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Single	TO-72
Single	Chip

PRINCIPAL DEVICES

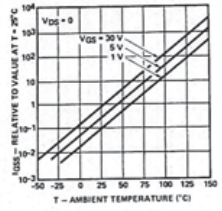
2N2608, 2N2608JAN, 2N2843
2N3329-32, 2N3909, VCR5P
2N2608CHP, 2N2843CHP,
2N3329CHP-32CHP, 2N3909CHP
VCR5PCHP

PERFORMANCE CURVES (25°C unless otherwise noted)

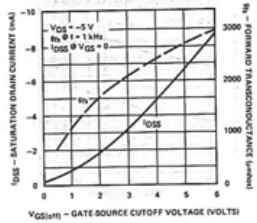
Output Characteristic



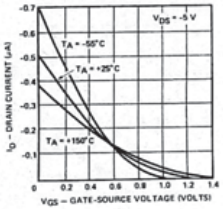
Gate Reverse Current vs Ambient Temperature



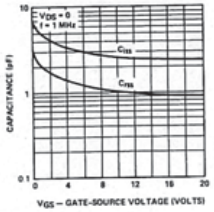
Drain Current & Transconductance vs Gate-Source Voltage



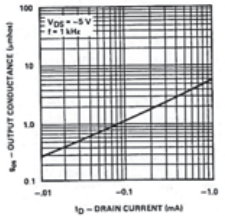
Transfer Characteristic



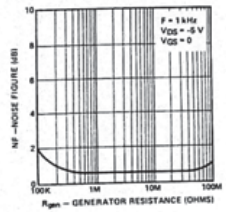
Common-Source Capacitances vs Gate-Source Voltage



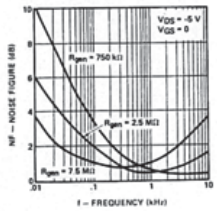
Common-Source Output Conductance vs Drain Current



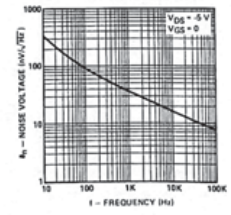
Noise Figure vs Generator Resistance



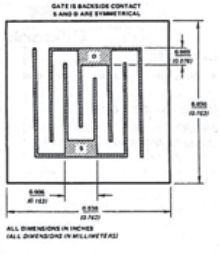
Noise Figure vs Frequency



Equivalent Input Noise Voltage vs Frequency



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p-channel JFET
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- General Purpose Amplifiers

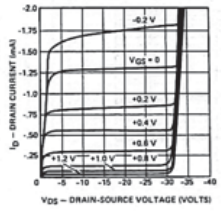
TYPE	PACKAGE
Single	TO-18
Single	Chip

PRINCIPAL DEVICES

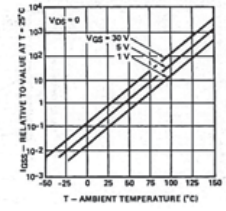
2N2609, 2N2609JAN, 2N2844
2N2609CHP, 2N2844CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

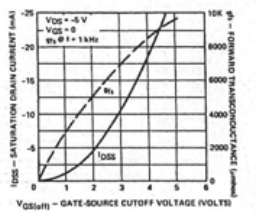
Output Characteristic



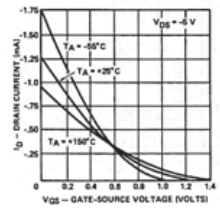
Gate Reverse Current vs Ambient Temperature



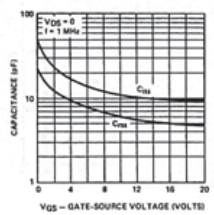
Drain Current & Transconductance vs Gate-Source Voltage



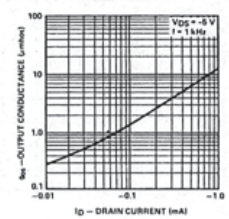
Transfer Characteristic



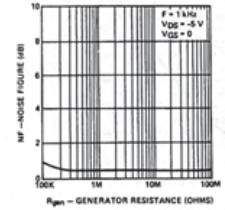
Common-Source Capacitance vs Gate-Source Voltage



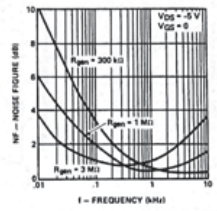
Common-Source Output Conductance vs Drain Current



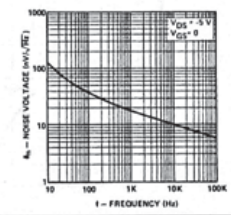
Noise Figure vs Generator Resistance



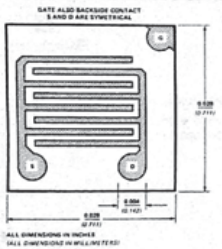
Noise Figure vs Frequency



Equivalent Input Noise Voltage vs Frequency



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p-channel JFET
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- General Purpose Amplifiers
- Switches

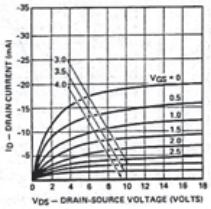
BENEFITS:
- Wide Range of Transconductance

TYPE	PACKAGE
Single	TO-72
Single	Chip

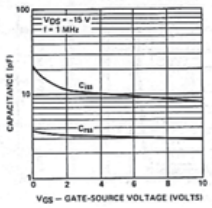
PRINCIPAL DEVICES
2N3382, 2N3384, 2N3386, VCR3P
2N3382CHP-86CHP, VCR3PCHP

PERFORMANCE CURVES (25°C unless otherwise noted)

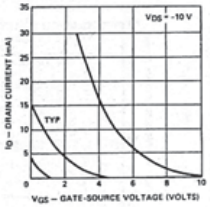
Output Characteristic



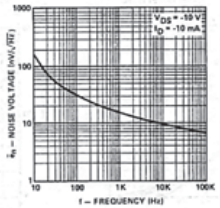
Common-Source Capacitances vs Gate-Source Voltage



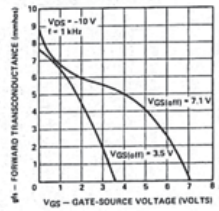
Transfer Characteristics



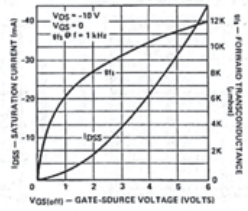
Equivalent Input Noise Voltage vs Frequency



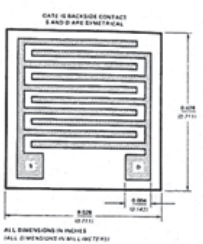
Transconductance Characteristics



Drain Current & Transconductance vs Gate-Source Voltage



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p-channel JFET
designed for . . .

- Analog Switches
- Commutators
- Choppers
- Integrator Reset Switch

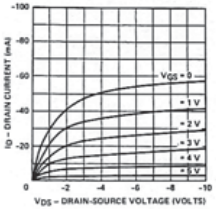
BENEFITS:
- Low Insertion Loss in Switching Systems $R_{ON} < 75\ \Omega$ (2N5114)
- Short Sample and Hold Aperture Time $C_{rss} < 7$ pF
- High Off-Isolation $I_{D(off)} < 500$ pA

TYPE	PACKAGE
Single	TO-18
Single	TO-92
Single	TO-92 Lead-form
Single	Chip

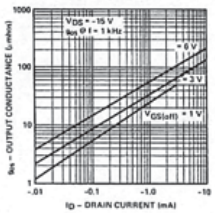
PRINCIPAL DEVICES
2N5018-19, 2N5114-16, U304-6
J174-7, J270-1, P1086-87, P1086E
J174-18 - 177-18, J270-18 - 271-18
P1086-18 - 87-18
2N5018CHP-19CHP, 2N5114CHP-16CHP
U304CHP-6CHP, P1086CHP-87CHP
J270CHP-271CHP

PERFORMANCE CURVES (25°C unless otherwise noted)

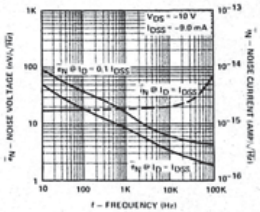
Output Characteristic



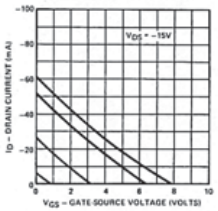
Common-Source Output Conductance vs Drain Current



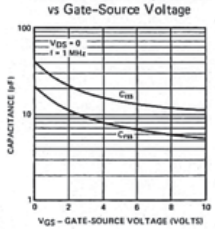
Equivalent Input Noise Voltage and Noise Current vs Frequency



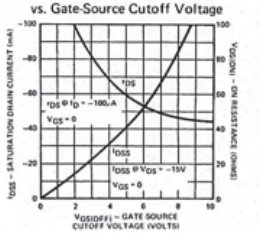
Transfer Characteristics



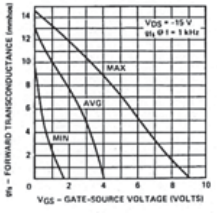
Common-Source Capacitance vs Gate-Source Voltage



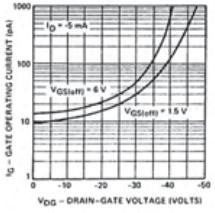
Saturation Drain Current and Drain-Source ON Resistance vs. Gate-Source Cutoff Voltage



Transconductance Characteristics



Gate Operating Current vs Drain-Gate Voltage



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application notes

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APPLICATION NOTE

An Introduction to FETs

INTRODUCTION

The basic principle of the field-effect transistor (FET) has been known since J.E. Lilenfeld's patent of 1925. The theoretical description of a FET made by Schockley in 1952 paved the way for development of a classic electronic device which provides the designer with the means by which he can accomplish nearly every circuit function. The field-effect transistor earlier was known as a "unipolar" transistor, and the term refers to the fact that current is transported by carriers of one polarity (majority), whereas in the conventional bipolar transistor carriers of both polarities (majority and minority) are involved.

This Application Note provides an insight into the nature of the FET, and touches briefly on its basic characteristics, terminology and parameters, and typical applications.

The following list of FET applications indicates the versatility of the FET family:

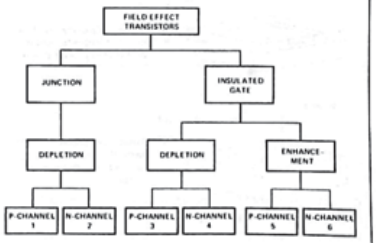
Amplifiers	*Switches*	*Current Limiters*
Small Signal	Chopper-type	*Voltage-Controlled Resistors*
Low Distortion	Analog Gate	*Mixers*
High Gain	Commutator	*Oscillators*
Low Noise		
Selective		
D.C.		
High-Frequency		

This very wide range of FET applications by no means implies that the device will replace the more widely-known bipolar transistor in every case. The simple fact is that FET characteristics – which are very different from those of bipolar devices – can often make possible the design of technically superior (and sometimes cheaper) circuits. This comment applies not only to networks employing discrete devices and conventional components such as resistors and capacitors, but also extends to both linear and digital integrated circuits.

In fact, FET technology today allows a greater packaging density in large-scale integrated circuits (LSI) than would ever be possible with bipolar devices.

(Although there is no industry-accepted definition of LSI, apparently when the equivalent circuit of an IC contains more than 1,000 active elements (500 gates) or is "very complex", the end product may be called LSI. With a typical LSI chip measuring less than 200 x 200 mils, this is high-density packaging indeed.)

The family tree of FET devices (Figure 1) may be divided into two main branches, junction FETs (JFETs) and Insulated Gate FETs (or MOSFETs, *metal-oxide-silicon field-effect transistors*). Junction FETs are inherently depletion-mode devices, and are available in both P- and N-Channel configurations. MOSFETs are available in both enhancement or depletion modes, and exist as both N- and P-Channel devices. The two main FET groups depend on different phenomena for their operation, and will be discussed separately.



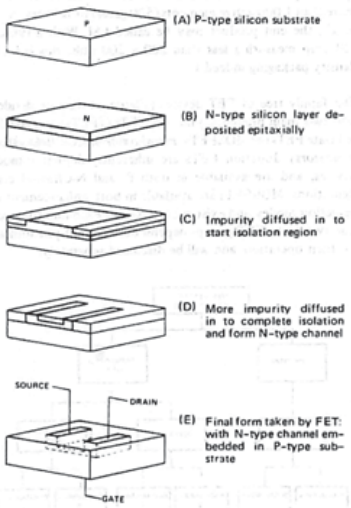
FET Family Tree
Figure 1

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Junction FETs

In its most elementary version, this transistor consists of a piece of high-resistivity semiconductor material (usually silicon) which constitutes a channel for the majority carrier flow. The magnitude of this current is controlled by a voltage applied to a *gate*, which is a reverse-biased PN junction formed along the channel. Implicit in this description is the fundamental difference between FET and bipolar devices: when the FET junction is reverse-biased the gate current is practically zero, whereas the base current of the bipolar transistor is always some value greater than zero. The FET is a high input resistance device, while the input resistance of the bipolar transistor is comparatively low. If the channel is doped with a donor impurity, N-type material is formed and the channel current will consist of electrons. If the channel is doped with an acceptor impurity, P-type material will be formed and the channel current will consist of holes. N-Channel devices have greater conductivity than P-Channel types, since electrons have higher mobility than do holes; thus N-Channel FETs tend to be more efficient conductors than their P-Channel counterparts.

Junction FETs are particularly suited to manufacture by modern planar epitaxial processes. Figure 2 shows this process in an idealized manner. First, N-type silicon is deposited epitaxially (single-crystal condensation surface) onto monocrystalline P-type silicon, so that crystal integrity is maintained. Then a layer of silicon dioxide is grown on the surface of the N-type layer, and the surface is etched so that an acceptor-type impurity can be diffused through into the silicon. The resulting cross-section is shown in Figure 2C, and demonstrates how a P-type annulus has been formed in the layer on N-type silicon. Figure 2D shows how a further sequence of oxide growth, etching, and diffusion can produce a channel of N-type material within the substrate.



Idealized Manufacture of an N-Channel Junction FET
Figure 2

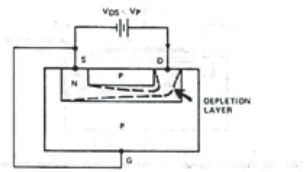
In addition to the channel material, a FET contains two ohmic (non-rectifying) contacts, the *source* and the *drain*. These are shown in Figure 2E. Since a symmetrical geometry is shown in the idealized FET chip, it is immaterial which contact is called the source and which is called the drain; the FET will conduct current equally well in either direction and the source and drain leads are usually interchangeable.

(For certain FET applications, such as amplifiers, an asymmetrical geometry is preferred for lower capacitance and improved frequency response. In these cases, the source and drain leads should not be interchanged.)

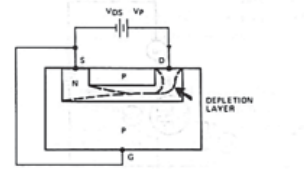
Figure 2E also shows how the N-Channel is embedded in the P-type silicon substrate, so that the gate above the channel becomes part of this substrate. Figure 3 shows how the FET functions. If the gate is connected to the source, then the applied voltage (V_{DS}) will appear between the gate and the drain. Since the PN junction is reverse-biased, little current will flow in the gate connection. The potential gradient established will form a *depletion* layer, where almost all the electrons present in the N-type channel will be swept away. The most depleted portion is in the high field between the gate and the drain, and the least-depleted area is between the gate and the source. Because the flow of current along the channel from the (positive) drain to the (negative) source is really a flow of free electrons from source to drain in the N-type silicon, the magnitude of this current will fall as more silicon becomes depleted of free electrons. There is a limit to the drain current (I_D) which increased V_{DS} can drive through the channel. This limiting current is known as I_{DSS} (*Drain-to-Source* current with the gate *Shorted* to the source). Figure 3B shows the almost complete depletion of the channel under these conditions.

Figure 3C shows the output characteristics of an N-Channel JFET with the gate short-circuited to the source. The initial rise in I_D is related to the buildup of the depletion layer as V_{DS} increases. The curve approaches the level of the limiting current I_{DSS} when I_D begins to be *pinched off*. The physical meaning of this term leads to one definition of *pinch-off voltage*, V_P, which is the value of V_{DS} at which the maximum I_{DSS} flows.

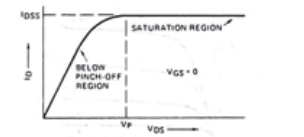
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(A) N-channel FET working below saturation (V_{GS} = 0). (Depletion shown only in channel region).



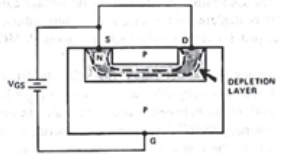
(B) N-channel FET working in saturation retion (V_{GS} = 0)



(C) Idealized output characteristic for V_{GS} = 0.

Figure 3

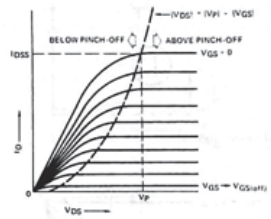
In Figure 4, consider the case where V_{DS} = 0, and where a negative voltage V_{GS} is applied to the gate. Again, a depletion layer has built up. If a small value of V_{DS} were now applied, this depletion layer would limit the resultant channel current to a value lower than would be the case for V_{GS} = 0. In fact, at a value of $|V_{GS}| \geq |V_P|$ the channel current would be almost entirely cut off. This cutoff voltage is referred to as the gate cutoff voltage, and may be expressed by the symbol V_P or by $V_{GS(off)}$. V_P has been widely used in the past, but $V_{GS(off)}$ is now more commonly accepted since it eliminates the ambiguity between gate cut-off and drain pinch-off. $V_{GS(off)}$ and V_P, strictly speaking, are equal in magnitude but opposite in polarity.



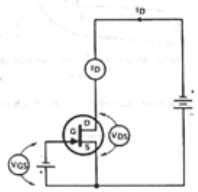
N-channel FET Showing Depletion Due To Gate-Source Voltage (V_{DS} = 0)
Figure 4

The mechanisms of Figure 3 and 4 react together to provide a family of output characteristics as shown in Figure 5A. The area below the pinchoff voltage locus is known as the triode or "below pinchoff" region; the area above pinchoff is often referred to as the pentode or saturation region. FET behavior in these regions is comparable to that of a power grid vacuum tube, and for this reason FETs operating in the saturation region may be used as excellent amplifiers. Note that in the "below pinchoff" region both V_{GS} and V_{DS} control the channel current, while in the saturation region V_{DS} has little effect and V_{GS} essentially controls I_D.

Figure 5B relates the curves of Figure 5A to the actual circuit arrangement, and shows the number of meters which may be connected to display the conditions relevant to any combination of V_{DS} and V_{GS}. Note that the direction of the arrow at the gate gives the direction of current flow for the forward-bias condition of the junction. In practice, however, it is always reverse-biased.



(A) Family of output characteristics for N-channel FET



(B) Circuit arrangement for N-channel FET

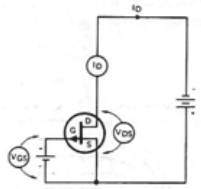
Figure 5

The P-Channel FET works in precisely the same way as does the N-Channel FET. In manufacture, the planar process is essentially reversed, with the acceptor impurity diffused first onto N-type silicon, and the donor impurity diffused later to form a second N-type region and leave a P-type chan-

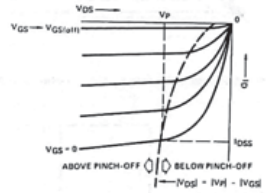
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nel. In the P-Channel FET, the channel current is due to hole movement, rather than to electron mobility. Consequently, all the applied polarities are reversed, along with their directions and the direction of current flow. Figure 6A shows the circuit arrangement for a P-Channel FET, and Figure 6B shows the output characteristics of the device. Note that the curves are shown in another quadrant than those of the N-Channel FET, in order to stress the current directions and polarities involved.

In summary, a junction FET consists essentially of a channel of semiconductor material along which a current may flow whose magnitude is a function of two voltages, V_{DS} and V_{GS}. When V_{DS} is greater than V_P, the channel current is controlled largely by V_{GS} alone, because V_{GS} is applied to a reverse-biased junction. The resulting gate current is extremely small.



(A) Circuit arrangement for P-channel FET

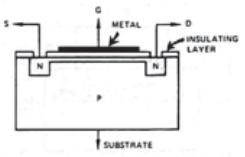


(B) Family of output characteristics for P-channel FET

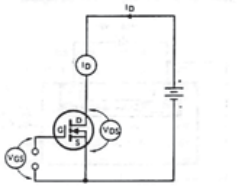
Figure 6

MOSFETs

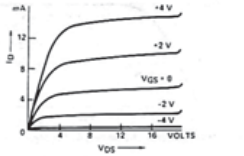
The metal-oxide-silicon FET (MOSFET) depends for its operation on the fact that it is not actually necessary to form a semiconductor junction on the channel of a FET in order to achieve gate control of the channel current. Instead, a metallic gate may be simply isolated from the channel by a thin layer of silicon dioxide, as shown in Figure 7A. Although the bottom of the insulating layer is in contact with the P-type silicon substrate, the physical processes which occur at this interface dictate that free electrons will accumulate at the interface, spontaneously forming an N-type channel. Thus a conducting path exists between the diffused N-type source and drain regions. Further, the MOSFET will behave



(A) Idealized cross-section through an N-channel depletion-type MOSFET



(B) Circuit arrangement for N-channel depletion MOSFET



(C) Family of output characteristics for the Siliconix 2N3631 N-channel depletion MOSFET

Figure 7

in a manner similar to the N-Channel junction FET when a voltage of the correct polarity is applied to the channel, as in Figure 7B.

Output characteristics of an N-Channel MOSFET are shown in Figure 7C. Because there is no junction involved, V_{GS} can be reversed without engendering a gate current; the gate may be made either positive or negative with respect to the source. Under these circumstances, still more free electrons will be attracted to the channel region, and I_D will become greater than I_{DSS}. This mode of operation is represented by the higher members of the family of ourput characteristics. Because the application of a negative gate voltage causes the channel to be depleted of free electrons – thus reducing I_D – the device just described is called a *depletion-mode* MOSFET.

The foregoing has established that the depletion-mode MOSFET is a "normally-ON" device: when $V_{GS} = 0$, a conducting path exists between source and drain. In many circuits a "normally-OFF" device would be useful, a condition which leads to the concept of an *enhancement-mode* MOSFET. In the latter device, an increasing voltage applied to the gate will enhance channel conduction, and depletion will never occur, I_D being zero when $V_{GS} = 0$.

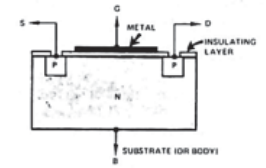
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A P-Channel enhancement-mode MOSFET is shown in Figure 8. Here, an acceptor impurity has been diffused into an N-type substrate to form P-type source and drain regions. No conducting channel exists between the source and the drain, because no matter how the drain-source voltage is applied one of the PN junctions will always be reverse-biased. On the other hand, if a negative voltage is applied to the gate, a field will be set up in such a direction as to attract holes into the upper layer of the substrate and produce a P-type channel. A family of output characteristics for a typical MOSFET is shown in Figure 8C. The idealized cross-section illustrated in Figure 8A may be used to show how the characteristics of Figure 8C come about. Refer to Figure 9 for an extension of this phenomenon.

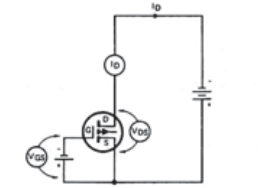
If a constant (negative) gate voltage, ($V_{GS(K)}$) is applied, then an essentially-uniform P-Channel depletion layer will be induced, as in Figure 9A. If a negative drain voltage is applied, then current, I_D, will flow through the drain. As $|V_{DS}|$ increases, I_D also increases. However, the voltage between the drain and the gate decreases, so that the thickness of the channel at the drain end is reduced as in Figure 9B. Therefore, the relationship of I_D versus V_{DS} will eventually reach a limiting value when $V_{DS} = V_{GS}$, and the channel becomes pinched off. This condition is shown in Figure 9C.

Different values of V_{GS} give rise to limiting values of I_D, so that the characteristic family of output curves which was shown in Figure 8 is realized. Characteristics of depletion-mode MOSFETs also come about for the same reason, except that members of the output characteristics family also exist for V_{GS} values of zero or reversed polarity. The P-Channel enhancement-mode MOSFET is currently the most popular member of the FET family in current use, and is in fact the basic element in many LSI integrated circuits.

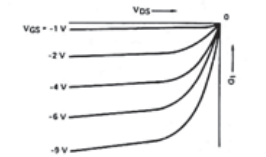
In principle it is possible to manufacture the remaining two members of the MOSFET family, the P-Channel depletion-mode and the N-Channel enhancement-mode devices. Because of the spontaneous formation of an N-Channel at a silicon/silicon-dioxide interface, the fabrication processes involved become quite difficult on a volume production basis. Much work has gone into the development of practical MOSFET processes for these devices, and N-Channel depletion-mode types are now becoming generally available.



(A) Idealized cross-section through a P-channel enhancement MOSFET

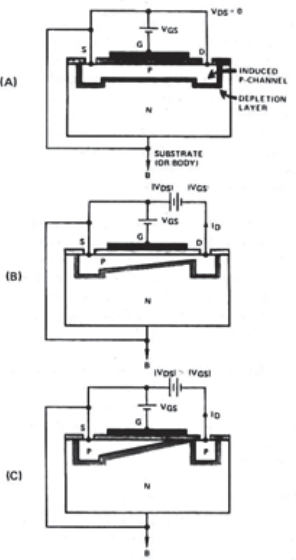


(B) Circuit arrangement for P-channel enhancement MOSFET



(C) Family of output characteristics for a P-channel enhancement MOSFET

Figure 8



Idealized approach of pinch-off,
(A) $V_{DS} = 0$, (B) $|V_{DS}| < |V_{GS}|$, (C) $|V_{DS}| > |V_{GS}|$

Figure 9

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FET Characteristics

The FET enjoys certain inherent advantages over bipolar transistors because of the unique construction and method of operation of the field-effect device. These characteristics include:

- Low noise
- No thermal runaway
- Low distortion and negligible intermodulation products
- High input impedance at low frequencies
- Very high dynamic range (> 100 dB)
- Zero temperature coefficient Q point
- Junction capacitance independent of device current

The transfer function of a FET approximates to a square-law response, and the second and higher-order derivatives of g_m are near zero; thus strong second and negligible higher-order harmonics are produced. Intermodulation products are extremely low.

The input impedance of a FET is simply the impedance of a reverse-biased PN junction, which is on the order of 10^{10} to 10^{12} Ω. In practice, the input impedance is limited by the value of the shunt gate resistor used in a self-bias common-source circuit configuration. At RF frequencies, the input impedance drop is proportional to the square of the frequency; for example, in a 2N4416 FET, the input impedance would be 22K Ω at 100 MHz. Also, the input susceptance increases linearly with frequency, since it is a simple parasitic capacitance.

The FET has very high dynamic range, in excess of 100 dB. Thus it can amplify very small signals because it produces very little noise, or it can amplify very large signals because it has negligible intermodulation distortion products. It also has a zero temperature coefficient bias point (zero TC point) at which changes in temperature do not change the quiescent operating point.

Junction FET capacitances are more constant over wide current variation than are the same parameters in a bipolar device. This inherent stability allows high-frequency (VHF through L-band) oscillators to be built which are far more stable than oscillators using low-frequency crystals and multiplier stages.

FET Terminology and Parameters

Any introduction to the nature, behavior, and applications of field-effect transistors requires that certain questions be answered on FET electrical quantities and parameters – in particular, the most important parameters, and the means by which they can be measured. The following discussion will define specific FET parameters and their associated subscript notations, and present basic test circuits and results.

Major parameters include:

- I_{DSS} – Drain current with the gate shorted to the source
- $V_{GS(off)}$ – Gate-source cutoff voltage
- I_{GSS} – Gate-to-source current with the drain shorted to the source
- BV_{GSS} – Gate-to-source breakdown voltage with the drain shorted to the source
- g_{fs} – Common-source forward transconductance
- C_{gs} – Gate-source capacitance
- C_{gd} – Gate-drain capacitance

Special attention should be given to the subscript "s" because it has two different meanings and three possible uses. In FET notations, an "s" for the first or second subscript identifies the source terminal as a node point for voltage reference or current flow. However, when using triple subscript notation, an "s" for the third subscript does not refer to the FET source terminal. It is an abbreviation for "shorted", and signifies that all terminals not designated by the first two subscripts must be tied together and shorted to the common terminal, which is always the second subscript. Therefore, the term I_{GSS} refers to the gate-source current with the drain tied to the source.

Because of the typical low input and output admittance of the FET, four-pole admittance equations are commonly used to describe electrical characteristics of the FET:

$$I_1 = Y_{11}\ V_{11} + Y_{21}\ V_{22} \qquad (1)$$

When Y_{11}, Y_{21}, Y_{12} and Y_{22} are defined as the input, reverse transfer, forward transconductance, and output admittances respectively, Equation 1 reduces to

$$\begin{aligned} i_1 &= y_i\ v_{11} + y_r\ v_{22} \\ i_2 &= y_f\ v_{11} + y_o\ v_{22} \end{aligned} \qquad (2)$$

For a three-lead FET, 11 usually corresponds to the gate-source terminal and 22 corresponds to the drain-source terminal (i.e., the device is connected in the common-source mode). Thus

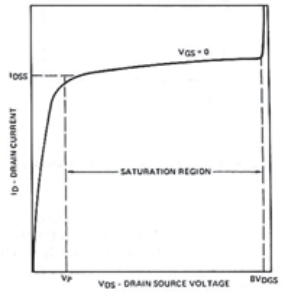
$$\begin{aligned} i_i &= y_{is}\ v_{gs} + y_{rs}\ v_{ds} \\ i_o &= y_{fs}\ v_{gs} + y_{os}\ v_{ds} \end{aligned} \qquad (3)$$

Here, the second subscript for the y parameters designates the source lead as the common or ground terminal.

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I_{DSS} – Drain Current at Zero Gate Voltage (I_D at $V_{GS} = 0$)

By itself, I_{DSS} merely refers to the drain current that will flow for any applied V_{DS} with the gate shorted to the source. However, when a particular value for V_{DS} is given, equal to or greater than V_P (see Figure 10), I_{DSS} indicates the drain saturation current at zero gate voltage. Some FET data sheets label I_{DSS} for V_{DS} greater than V_P as $I_{D(on)}$.



FET Characteristic at $V_{GS} = 0$
Figure 10

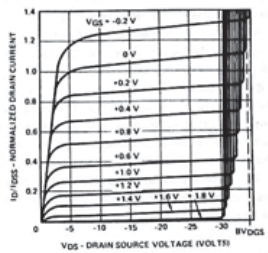
$V_{GS(off)}$ – Gate-Source Cutoff Voltage

The resistance of a semiconductor channel is related to its physical dimensions by $R = \rho L/A$, where

ρ = resistivity
L = length of the channel
A = W x T = cross-sectional area of channel

In the usual FET structure, L and W are fixed by device geometry, while channel thickness T is the distance between the depletion layers. The position of the depletion layer can be varied either by the gate-source bias voltage or by the drain-source voltage. When T is reduced to zero by any combination of V_{GS} and V_{DS}, the depletion layers from the opposite sides come in contact, and the a-c or incremental channel resistance, r_{DS}, approaches infinity. As earlier noted, this condition is referred to as "pinch-off" or "cutoff" because the channel current has been reduced to a very thin sheet, and current will no longer be conducted. Further increases in V_{DS} (up to the junction reverse-bias breakdown) will cause little change in I_D. Accordingly, the pinch-off region is also referred to as the pentode or "constant-current" region.

In Figure 10, pinch-off occurs with $V_{GS} = 0$. In Figure 11, V_{GS} controls the magnitude of the saturated I_D, with increases in V_{GS} resulting in lower values of constant I_D, and smaller values of V_{DS} necessary to reach the "knee" of the curve. The current scale in Figure 11 has been normalized to a specific value of I_{DSS}.



FET I_D vs V_D Output Characteristics
Figure 11

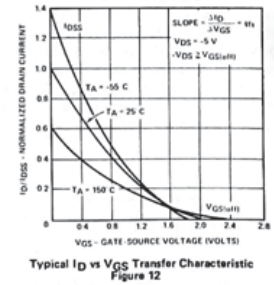
The knee of the curve is important to the circuit designer because he must know what minimum V_{DS} is needed to reach the pinch-off region with $V_{GS} = 0$. When appropriate bias voltage is applied to the gate, it will pinch off the channel so that no drain current can flow; V_{DS} has no effect until breakdown occurs. The specific amount of V_{GS} that produces pinch-off is known as the gate-source cutoff voltage, $V_{GS(off)}$.

$V_{GS(off)}$ Test Procedure

Although the magnitude of $V_{GS(off)}$ is equal to the pinch-off voltage, V_P, defined by the pinch-off knee in Figure 10, rapid curvature in the area makes it difficult to define any precise point as V_P. Taking a second derivative of V_{DS}/I_D would yield a peak corresponding to the inflection point at the knee, which approximates V_P. However, this is not a simple measurement for production quantities of devices. A better measure is to approach the cutoff point of the I_D versus V_{GS} characteristic. This is easier than trying to specify the location of the knee of the I_D versus V_{DS} output characteristic.

A typical transfer characteristic I_D versus V_{GS} is shown in Figure 12. The curve can be closely approximated by

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2 \qquad (4)$$

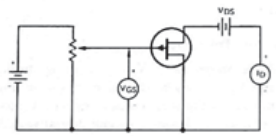


Typical I_D vs V_{GS} Transfer Characteristic
Figure 12

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Equation 4 and Figure 12 indicate that at $V_{GS} = V_{GS(off)}$, $I_D = 0$. In a practical device, this cannot be true because of leakage currents. If I_D is reduced to less than 1 percent of I_{DSS}, V_{GS} will be within 10 percent of the $V_{GS(off)}$ value indicated by Equation 4. If I_D is reduced to 0.1 percent of I_{DSS}, the indicated $V_{GS(off)}$ error will be reduced to about 3 percent. For a true indication of $V_{GS(off)}$, and a realistic picture of the parameters of Figure 12, care must be taken that leakage currents do not result in an error in the $V_{GS(off)}$ reading. Typically, at room temperature, 1 percent of I_{DSS} is still well above leakage currents but is low enough to give a fairly accurate value of $V_{GS(off)}$.

A typical circuit for measuring $V_{GS(off)}$ is shown in Figure 13. At $V_{GS} = 0$, the value of I_{DSS} can be measured. Then, by increasing V_{GS} until I_D is 0.01 percent of I_{DSS}, the value of $V_{GS(off)}$ is obtained. From a production standpoint, it is more convenient to specify I_D at some fixed value (such as 1 nA), rather than as a certain percentage of I_{DSS}. Thus a pinchoff voltage specification may be given as indicated in Table I.



Circuit for Measuring $V_{GS(OFF)}$
Figure 13

Table I
Typical Pinch-Off Voltage Specification

Characteristic		Min	Max	Units
$V_{GS(off)}$	Gate-source pinch-off voltage of: $V_{DS} = -5$ V, $I_D = -1$ µA	1	4	Volts

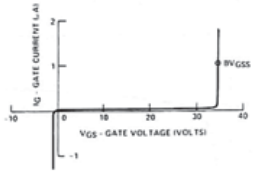
Another method which provides an indirect indication of the maximum value of $V_{GS(off)}$ is shown in Table II. The characteristic specified is $I_{D(off)}$, whereas the parameter of interest is $V_{GS} = 8$ volts. The specification does say that the maximum $V_{GS(off)}$ is approximately 8 volts, but no provision is made for stating a *minimum* $V_{GS(off)}$, as was done in Table I. Therefore, another test must be made if $V_{GS(off)}$ (min) is to be specified.

Table II
Indication of Maximum V_P

Characteristic		Test Conditions	Min	Max	Unit
$I_{D(off)}$	Pinch-off drain current	$V_{DS} = -12$ V, $V_{GS} = 8$ V		-10	µA

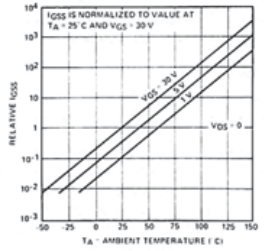
I_{GSS} – Gate-Source Cutoff Current

The input gate of a P-Channel FET appears as a simple PN junction; thus the input d-c input characteristic is analogous to a diode V-I curve, as is shown in Figure 14.



P-Channel FET Input Gate Characteristic
Figure 14

In the normal operating mode, with V_{GS} positive for a P-Channel device, the gate is reverse-biased to a voltage between zero and $V_{GS(off)}$. This results in a d-c gate-source resistance which is typically more than 100M Ω. The gate current is both voltage- and temperature-sensitive. Figure 15 shows this relationship for I_{GSS} versus temperature and V_{GS}.



I_{GSS} vs Temperature
Figure 15

If the gate-source junction becomes forward-biased, (negative voltage in a P-Channel device) or if V_{GS} exceeds the reverse-bias breakdown for the junction, the input resistance will then become very low.

The FET is normally operated with a slight reverse bias applied to the gate-source; hence a good measure of the d-c input characteristic is to check the gate current at a value of gate-channel voltage that is below the junction breakdown rating. In device evaluation, there are three common measurements of gate current: I_{GDO}, I_{GSO}, and the combined measurement I_{GSS}. These measurement circuits are shown in Figure 16.

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The question is, should I_{GDO} and I_{GSO} be measured separately, or will one measurement of I_{GSS} suffice? One thing is certain: $I_{GSO} + I_{GDO} > I_{GSS}$, because the drain and the source are not completely isolated. They are, in fact, electrically connected via channel resistance. For most FETs, if V_G is greater than $V_{GS(off)}$, the difference between $(I_{GSO} + I_{GDO})$ and I_{GSS} is small; therefore, the measurement of I_{GSS} is a realistic means of controlling both I_{GDO} and I_{GSO}.

In a circuit, V_{GD} may be biased between zero and BV_{GDS}, while V_{GS} will be between zero and $V_{GS(off)}$; therefore, I_G is not necessarily the same as I_{GSS}.

BV_{GSS} – Gate-Source Breakdown Voltage

FET input terminals have been previously described as having NP or PN junctions, depending on the channel material. As such, the junction breakdown voltage is a necessary parameter.

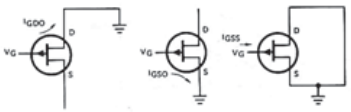
A useful equivalent circuit for a FET is the distributed constant network shown in Figure 17, for a P-Channel FET. If an N-Channel device is being evaluated, the diodes would be reversed. In most applications, the gate-drain voltage is greater than the gate-source voltage; thus the gate-drain breakdown rating is most important. However, it is also possible to consider the gate-source junction breakdown and the apparent drain-source breakdown (i.e., in Figure 17, when a high negative voltage is applied from drain to source, CR_1 will break down while CR_n becomes forward-biased).

Some device manufacturers use a BV_{GDO} rating, which means they are only checking diode CR_1. A better method is to use a BV_{GSS} rating (gate-source breakdown with the drain shorted to the source), because it checks both CR_1 and CR_n, in addition to exposing the *weakest* breakdown path along the entire gate-channel junction. The BV_{GSS} test also allows the user to interchange source and drain lead connections without worry about device breakdown ratings.

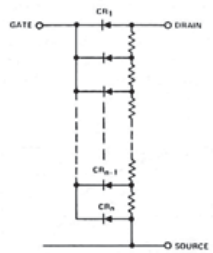
Admittedly, a BV_{GSS} test will reject some units which might pass a BV_{GDO} test; the number rejected, however, will be insignificant compared to the advantage of providing symmetrical operation.

Test Procedures for BV_{GSS}

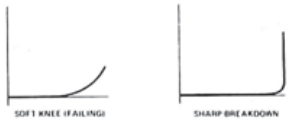
Junctions may break down softly or sharply; junctions with soft knee breakdown are undesirable. Without examining each individual unit on a curve tracer, devices with a soft knee may be eliminated by selecting a low current level for breakdown measurement (see Figure 18).



Three Common Measurement of Gate Current
Figure 16



A Useful FET Equivalent Circuit
Figure 17



Examples of Soft Knee and Sharp Knee Breakdown
Figure 18

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g_{fs} – Transconductance

Transconductance, g_{fs}, is a measure of the effect of gate voltage upon drain current:

$$g_{fs} = \frac{\Delta I_D}{\Delta V_{GS}}, \quad V_{DS} = \text{constant} \tag{5}$$

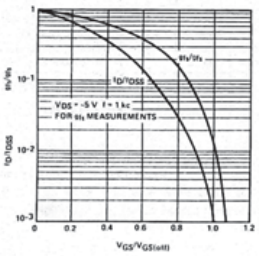
The interrelation of g_{fs} to the parameters I_{DSS} and $V_{GS(OFF)}$ should be noted. Equations 4, 6 and 7 describe the value of I_D and g_{fs} in a FET for any value of V_{GS} between zero and $V_{GS(OFF)}$.

$$g_{fs} = g_{fso}\left(1 - \frac{V_{GS}}{V_{GS(off)}}\right) \tag{6}$$

$$g_{fso} = -\frac{2I_{DSS}}{V_{GS(off)}} \tag{7}$$

where g_{fso} is the value of g_{fs} at $V_{GS} = 0$ and I_{DSS} is the value of I_D at $V_{GS} = 0$. With these equations, the value of g_{fs} can be calculated with a fair degree of accuracy (20 percent) if I_{DSS} and $V_{GS(off)}$ are known.

Figure 19 shows normalized curves for I_D and g_{fs} as functions of V_{GS} in a P-Channel FET. These curves were obtained from actual measurements on typical diffused channel FETs, such as the 2N2606. The curves agree very well with Equations 4 and 6 until $V_{GS(off)}$ is approached. For these curves, $V_{GS(off)}$ was assumed to be the value of V_{GS} where $I_D/I_{DSS} = 0.001$.



Normalized Curves for I_D and g_{fs} as Functions of V_{GS}
Figure 19

The drain current of a JFET operating in the triode (below pinch-off) region can be accurately predicted by using Equation 8, where

$$I_D/\text{triode} = I_{DSS}\left(\frac{V_{DS}}{V_{GS(off)}}\right)^{\frac{1}{2}} \tag{8}$$

Specifications for g_{fs} are shown in Tables III and IV. Note that there is a difference in the test conditions specified for the N-Channel 2N3823 and the P-Channel 2N3329. The gate voltage for the 2N3823 is established as zero. This means that g_{fs} is measured at $I_D = I_{DSS}$, as in Table III.

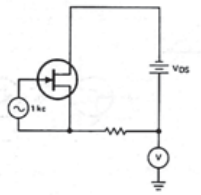
Table III (2N3823)

Characteristic		Test Conditions	Min	Max	Unit
g_{fs}	Small-signal common-source forward transconductance	V_{DS} = 15 V, V_{GS} = 0, f = 1 kHz	3,500	6,500	μmho

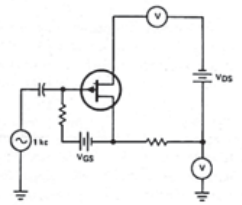
Table IV (2N3329)

Characteristic		Test Conditions	Min	Max	Unit
Y_{fs}	Common-source forward transfer admittance	V_{DS} = –10 V, I_D = –1 mA f = 1 kHz		20	μmho

The test conditions shown in Table IV specify a certain value for I_D (–1 mA for the 2N3329). This means that for each unit tested, V_{GS} is adjusted until I_D equals the specified value. The conditions specified in Table III simplify testing of the g_{fs} parameter by eliminating the necessity of adjusting V_{GS}. Figures 20 and 21 show typical test setups for the two methods.



Test Circuit for g_{fs} with $V_{GS} = 0$
Figure 20



Test Circuit for g_{fs} with I_D Specified
Figure 21

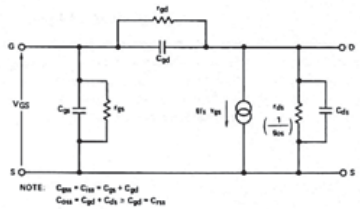
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Junction FET Capacitances

Associated with the junction between the gate and the channel of a FET is a capacitance whose value and geometric distribution are functions of the applied voltages V_{GS} and V_{DS}. Because of the complexity of dealing with such a distributed capacitance, a simplification is made so that two lumped capacitances, C_{gs} and C_{gd}, exist between the gate and the source and drain, respectively. (A much smaller capacitance, C_{ds}, also exists between the drain and the source, stemming mainly from the device package; this header capacitance is small enough so that it can be ignored for most purposes.)

Data sheets quote C_{gs} and C_{gd} (or other capacitances from which they may be derived) for specified operating conditions. Occasionally, graphs are included which show the variations of C_{gs} and C_{gd} as the result of changing conditions of V_{DS}, V_{GS} and temperature. If these data are not presented, an estimate of inter-electrode capacitance values may be made by assuming that these values vary inversely with the square root of the bias voltage. The temperature variations will be very small, because they depend on the –2.2 mV/°C change in junction potential difference.

Assuming that the FET is properly biased – that is, that the d-c conditions are met by the external circuitry – it is possible to construct an incremental equivalent circuit from which the small-signal or a-c performance may be predicted. Such an equivalent circuit is shown in Figure 22.



Incremental Equivalent Circuit for the Junction FET
Figure 22

The equivalent capacitance from the gate to the source, C_{gs}, is shunted by a very large input resistance, r_{gs}, with both of these parameters being characteristic of a reverse-biased junction. Similarly, the equivalent capacitance from the gate to the drain is shunted by the very large resistance r_{gd}. (For most purposes, r_{gs} and r_{gd} may be neglected, and the gate impedance of the FET treated as pure capacitance). At the drain side of the equivalent circuit the small capacitance C_{ds} – which stems from the header material – is shunted by the incremental channel resistance, r_{ds}. This resistance is capable of wide variations, depending on bias conditions. Since the equivalent circuit is fundamentally relevant to the pinch-off or saturated condition, r_{ds} will be on the order of megohms.

The incremental channel current is given by the transconductance, g_{fs}, multiplied by the incremental gate voltage. For the small signal, v_{gs}, this is manifested in the equivalent circuit by the current generator $g_{fs}v_{gs}$. Notice that the conventional direction of flow of this current is such that i_d flows into the FET, in a "positive" direction.

Many circuits can be designed around the equivalent circuit for the junction FET. The actual values of g_{fs} adn r_{ds} can be measured as previously mentioned; there remains only the requirement to establish the methods of determining C_{gs} and C_{gd}.

First, assume that the FET is in operation and that the drain is connected to the source via a large capacitor, i.e., the drain and source are short-circuited to a-c. Under these circumstances, a capacitance measurement between the gate and the source will give

$$C_{gss}\,(\text{or } C_{iss}) = C_{gs} + C_{gd} \tag{9}$$

Second, assume that the gate and source are short-circuited to a-c in a similar manner. A capacitance measurement between the drain and the source will now give

$$C_{dss}\,(\text{or } C_{oss}) \approx C_{gd} \tag{10}$$

The alternative symbols C_{iss} and C_{oss} simply refer to measurements made at the input (gate) and the output (drain) respectively. An alternative symbol for C_{gd} is C_{rss}, which refers to the "reverse" capacitance.

In data sheets, it is customary to state (= C_{iss}) C_{gss} and C_{dss} (= C_{oss}). C_{rss} is often given in place of C_{oss} because if $C_{ds} \ll C_{oss}$, which is usually the case, then $C_{rss} \cong C_{oss}$. Equations (9) and (10) can be used in those instances where it is necessary to extract C_{gs} and C_{gd}, as in

$$C_{gs} = C_{iss} - C_{gd} \approx C_{iss} - C_{rss} \tag{11}$$

and

$$C_{gd} = C_{rss} \tag{12}$$

Remember that all capacitance measurements should be made at the same bias levels, since the capacitances are functions of applied voltages. To indicate the order of the capacitances to be found in a junction FET, consider the values given in the data sheet for the Siliconix E202 N-channel FET. They are given as

C_{iss} (at V_{DS} = 20 V and f = 1 MHz) = 5 pF max.

and

C_{rss} (at V_{DS} = 20 V and F = 1 MHz) = 2 pF max.

Hence, at a drain-source voltage of 20 V and a frequency of 1 MHz, C_{gs} = 5 – 2 = 3 pF maximum. Even though the FET is physically symmetrical, bias conditions have forced the capacitances to be unequal.

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APPLICATION NOTE

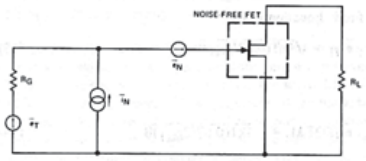
Audio-Frequency Noise Characteristics of Junction FETs

INTRODUCTION

The purpose of this application note is to identify and characterize audio frequency noise in junction field-effect transistors. Emphasis is placed on basic device characteristics rather than on end applications, since it is important for the circuit designer to know the salient noise behavior of the FET, and how those characteristics may be specified by production-oriented test parameters.

Defining FET Noise Figure

For analysis, it is convenient to represent noise in a FET by assuming that an ideal noise-free device has two external noise sources, $\bar{e}_N$ and $\bar{i}_N$. These noise sources are chosen to have the same output as would an actual noisy FET. An equivalent circuit is shown in Figure 1.



Representing Noise in an Ideal FET
Figure 1

A noise factor (F) is a Figure of Merit of a device with respect to the resistance of a generator. To calculate a noise factor, a source resistor R_G, with a thermal noise voltage $\bar{e}_T$, is added to the circuit.

A noise factor (F) may be defined as

$$F = \frac{\text{Total available output noise power}}{\text{Noise power at output due to thermal noise of } R_G}$$

or

$$F = \frac{\text{Noise power output due to } R_G + \text{noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power output due to FET}}{\text{Noise power output due to } R_G}$$

or

$$F = 1 + \frac{\text{Gain X noise power of FET referred to input}}{\text{Gain X noise power due to } R_G}$$

or

$$F = 1 + \frac{\text{Noise power of FET referred to input}}{\text{Noise power due to } R_G}$$

The thermal noise voltage across R_G is[1]

$$\bar{e}_T = \sqrt{4kTR_GB} \qquad (1)$$

where $k = 1.380 \times 10^{-23}$ Joules/°K (Boltzmann's Constant), T = temperature in °K, and B = bandwidth in Hz. Therefore noise power due to R_G is

$$\frac{\bar{e}_T^2}{R_G} = \frac{4kTR_GB}{R_G} = 4kTB \qquad (2)$$

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The noise power of the FET referred to the input is

$$\frac{\bar{e}_N^2}{R_G} + i_N^2 \cdot R_G \quad (3)$$

When expressions for the noise power of both the FET and R_G are substituted, the noise factor becomes

$$F = 1 + \frac{\bar{e}_N^2 + \bar{i}_N^2 R_G^2}{4kTR_GB} \quad (4)$$

A noise figure (NF) expressed in dB indicates the presence of added noise power from the FET or another active device. The noise figure is always given with reference to a standard, specifically the generator resistance R_G:

$$NF = 10 \log_{10} [F] \quad (5)$$

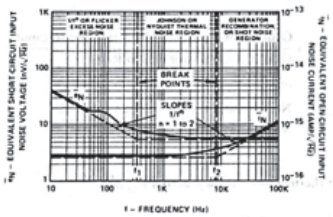
The noise figure of the FET is

$$NF = 10 \log_{10} \left[1 + \frac{\bar{e}_N^2 + \bar{i}_N^2 R_G^2}{4kTR_GB} \right] dB \quad (6)$$

When junction FET noise is expressed in terms of the noise figure (NF), an inherent disadvantage arises in that the noise figure value is dependent upon the value of the generator resistance, R_G. Therefore, the $\bar{e}_N$, $\bar{i}_N$ method remains as the best way to quantitatively express the noise characteristics of the FET itself.

Describing Junction FET Noise Characteristics

Junction FET $\bar{e}_N$ and $\bar{i}_N$ characteristics are frequency-dependent within the audio noise spectrum, and take a form as shown in Figure 2.



Characteristics of Junction FET Noise
Figure 2

$\bar{e}_N$, the equivalent short circuit input noise voltage (with the exception of the $1/f^n$ region), is defined as[2]

$$\bar{e}_N = \sqrt{4kTR_NB} \quad (7)$$

where $R_N \cong 0.67/g_{fs}$, the equivalent resistance for noise. The $\bar{e}_N$, except in the $1/f^n$ region, closely approximates the equivalent thermal noise voltage of the channel resistance.

In the so-called $1/f^n$ region, $\bar{e}_N$ is expressed as

$$\bar{e}_N = \sqrt{4KR_NB(1 + f_1/f^n)} \quad (8)$$

where n varies between 1 and 2 and is device- and lot-oriented.

The characteristic bulge in $\bar{e}_N$ in the $1/f^n$ region has been observed to some extent in all junction FETs submitted to test. The breakpoint or corner frequency shown as f_1 in Figure 2 is lot- and device design-oriented, and varies from about 100 Hz to 1 kHz.

As indicated in Equations (7) and (8), $\bar{e}_N$ is inversely proportional to the square root of the transconductance of the FET ($\bar{e}_N \propto 1/\sqrt{g_{fs}}$). $\bar{e}_N$ can be lowered by a factor of $1/\sqrt{N}$ if N devices with matched electrical characteristics are connected parallel. For example, when

$$N = 2 \quad (9)$$

let

$$\bar{e}_{N1} = \bar{e}_{N2} \quad (10)$$

and let

$$g_{fs1} = g_{fs2} \quad (11)$$

Thus,

$$g_{fs}TOTAL = 2\ g_{fs1} \text{ or } 2\ g_{fs2} \quad (12)$$

From Equation (7)

$$\bar{e}_{N1} = \sqrt{4kT(0.67/g_{fs1})B} \quad (13)$$

and

$$\bar{e}_NTOTAL = \sqrt{4kT(0.67/2g_{fs1})B} \quad (14)$$

Thus,

$$\bar{e}_NTOTAL = \frac{1}{\sqrt{2}} \bar{e}_{N1} \quad (15)$$

A second way to achieve low $\bar{e}_N$ is to use a device with a large gate area. Empirically, $\bar{e}_N$ is inversely proportional to the square of the gate area ($\bar{e}_N \propto 1/A_G^2$), independent of g_{fs}. This large gate area philosophy has been followed in the design of the Siliconix 2N4867A FET, and noise performance of the device is discussed later in this Application Note. A major advantage of this type of design is that $\bar{e}_N$ is significantly lowered and $\bar{i}_N$ also remains at a low value.

The equivalent open-circuit input noise current, $\bar{i}_N$, with the exception of the shot noise region shown in Figure 2, is due to thermally-generated reverse current in the gate channel junction. It is defined as

$$\bar{i}_N = \sqrt{2qI_GB} \quad (16)$$

where $q = 1.602 \times 10^{-19}$ coulomb (the magnitude of the electron charge), I_G is the measured DC operating gate current in amperes, and B is bandwidth in Hz. The expression is accurate only when the measured gate current is the result of bulk device conductance. It is possible for the measured gate current to be due to conductance stemming from contamination across the leads of the semiconductor package.

At higher frequencies, as in the shot noise region shown in Figure 2, $\bar{i}_N$ can be approximated as being equal to the Nyquist thermal noise current generated by a resistor:[3]

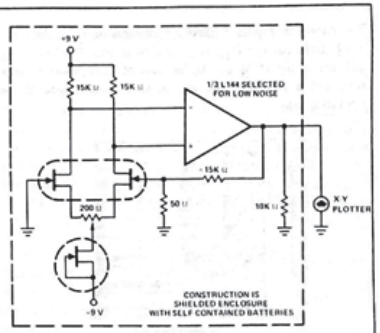
$$\bar{i}_N = \sqrt{\frac{4kTB}{R_p}} \quad (17)$$

where R_p is the real part of the gate-to-source input impedance. The breakpoint or corner frequency f_2 in Figure 2 is lot- and device design-oriented and can vary from 5 kHz to 50 kHz.

Another form of noise found in junction FETs is known as "popcorn" or burst noise; the term popcorn noise was originated in the hearing aid industry because of noise or level shifts which are present in input stages, and which resemble the sound of corn popping.

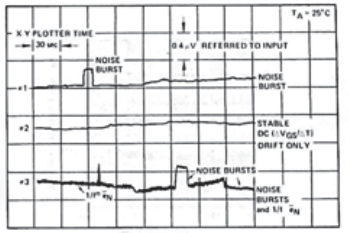
Popcorn noise is a form of random burst input noise current which remains at the same amplitude, and which is confined to frequencies of 10 Hz or lower. The suitability of a FET device is dependent on the amplitude of the burst, its duration, and its repetition rate. The origins of popcorn noise are not completely identified, but are believed to be caused by intermittent contact in aluminum-silicon interfaces and by contamination in the oxidation processes.

A test circuit to measure popcorn noise in differential junction FET amplifiers is shown in Figure 3. In practice, popcorn noise is evaluated on an engineering basis, and not on a production-line basis. No correlation between $1/f^n$ noise at 10 Hz and popcorn noise has yet been found in junction FETs. However, if the amplitude of the burst is large and occurs frequently, then $1/f^n$ noise voltage ($\bar{e}_N$) is masked and difficult to evaluate at 10 Hz.



Test Circuit to Measure Popcorn Noise
Figure 3

The graph in Figure 4 shows "moderate" burst noise observed in a group of junction FET differential amplifiers which were measured in the test circuit.



Popcorn Noise in Differential Amplifiers
Figure 4

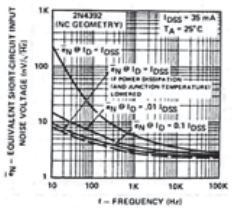
Operating Point Considerations

Unlike bipolar transistors, where $\bar{e}_N$ and $\bar{i}_N$ characteristics vary directly with change in collector current (I_C), similar characteristics in junction FETs will vary only slightly as drain current (I_D) is varied. This is true so long as the FET is biased so that the drain-source voltage is greater than the pinch-off voltage ($V_{DS} > V_p$ or $V_{GS(off)}$).

The $\bar{e}_N$ in junction FETs will be lowest when the devices are operated at $V_{GS} = 0$ ($I_D = I_{DSS}$), where transconductance (g_{fs}) is at its highest value. This will be true only if device dissipation is maintained very low in relation to the total dissipation capability of the FET.

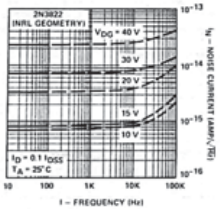
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The curves in Figure 5 illustrate changes in $\bar{e}_N$ as the operating drain current (I_D) is varied. Note that the lowest $\bar{e}_N$ did not occur at V_{GS} = 0, because of high power dissipation and a resultant rise in junction temperature at the operating point.



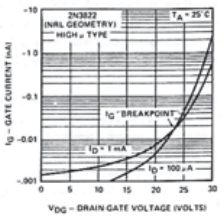
$\bar{e}_N$ Changes vs I_D Variations
Figure 5

The optimum (lowest) $\bar{i}_N$ in depletion-mode junction FETs should occur at V_{GS} = 0 (I_D = I_{DSS}). In practice, very little change will be seen in $\bar{i}_N$ when the operating point is changed, provided that the drain-gate voltage is maintained below the gate current (I_G) breakpoint and power dissipation is kept at a low level. The curves in Figure 6 illustrate $\bar{i}_N$ characteristics as a function of drain-gate voltage at points below, on, and above the I_G breakpoint voltage.

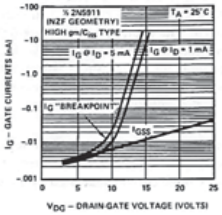


$\bar{i}_N$ Characteristics as Function of Drain-Gate Voltage
Figure 6

In circuit design, particular attention must be paid to drain-gate voltage (V_{DG}) to minimize gate current (I_G) under operating conditions. The critical drain-gate voltage (I_G breakpoint voltage) can be anywhere from 8 to 40 V, depending on device design.[4] Gate operating current (I_G) should not be considered equal to gate reverse current (I_{GSS}) in linear amplifier applications. I_{GSS} is only an indication of reverse-biased junction leakage under non-operating conditions. The Curves in Figures 7 and 8 show how I_G breakpoint is related to basic device design. Device designs with a high g_{fs}/C_{iss} ratio have low breakpoint voltages, typically at V_{DG} = 10 V, whereas high μ devices ($\mu = r_{ds} \cdot g_{fs}$). have much higher I_G breakpoints, typically V_{DG} = 20 – 30 V.



Gate Operating Current vs Drain-Gate Voltage
Figure 7

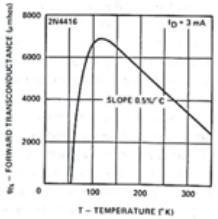


Gate Currents vs Drain-Gate Voltage
Figure 8

Characteristics of $\bar{e}_N$ and $\bar{i}_N$ at Low Temperature

Three equations presented earlier ((7), (16) and (17)) show that $\bar{e}_N$ and $\bar{i}_N$ are temperature dependent. $\bar{e}_N$ and $\bar{i}_N$ are proportional to $\sqrt{T}$, and both will be reduced if the temperature is lowered. In Equation (16), $\bar{i}_N$ is proportional to $\sqrt{I_G}$; I_G will halve for each temperature drop of 10 to 11°C. $\bar{e}_N$ is also proportional to $\sqrt{R_N}$, where $R_N \cong 0.67/g_{fs}$. Thus when g_{fs} is increased, which is typical of junction FETs operating at low temperature, $\bar{e}_N$ will also lower.

In Figure 9, g_{fs} has been plotted vs temperature for a silicon junction FET, and the low temperature limitation caused by a dropoff in g_{fs} is clearly shown.



g_{fs} vs Temperature
Figure 9

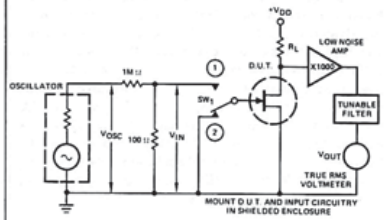
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In connection with the plot of g_{fs} vs temperature, note that the relationship can vary from approximately 0.2% to 1% per degree C. The g_{fs} slope depends upon the basic design of the FET, and upon the proximity of the drain current operating point to I_{DZ}, the zero temperature coefficient point.

The major application for junction FETs at low temperature is in charge-sensitive amplifiers.[5] For best performance in this type of application, a high g_{fs}/C_{iss} ratio is required. Recommended Siliconix FET types for such applications are the 2N4416 (NH geometry) and the U311 (NZA geometry).

Test Measurements

By definition, $\bar{e}_N$ and $\bar{i}_N$ are referred to the input of the device under test. To measure $\bar{e}_N$, the test circuit shown in Figure 10 will prove useful.



Test Circuit to Measure $\bar{e}_N$
Figure 10

The following procedure should be used to make the $\bar{e}_N$ test:

1. Set tunable filter to required f_{low} and f_{high}. Adjust oscillator to mean center frequency ($f_{mean} = [f_{low} \cdot f_{high}]^{1/2}$).
2. Set V_{osc} to 100 mV with Switch 1 in position (1). Compute $V_{in1} = 10^{-1} \times \frac{10^2}{10^6} = 10^{-5}$ V = 10 μV.
3. Measure V_{out1}. Compute overall gain as $A_v = \frac{V_{out1}}{V_{in1}} = \frac{V_{out1}}{10\,\mu V}$.
4. Set Switch 1 to position (2) and measure V_{out2}. Compute V_{in2}, the equivalent short-circuit input noise voltage ($\bar{e}_N$), using A_v from Step 3. $V_{in2} = \frac{V_{out2}}{A_v} = \bar{e}_N$ in volts over bandwidth f_{low} to f_{high}.

An alternate method of performing the above test is to use a Quan-Tech Transistor Noise Analyzer consisting of a Model 2173 Control Unit and a Model 2181 Filter. The analyzer has provision for measuring $\bar{e}_N$ and determining NF with various values of R_G in FET and bipolar devices with selectable test conditions. The measuring system has a constant gain of 10,000. The analyzer records output noise at selected frequencies between 10 Hz and 100 kHz in the device under test, with the scale shown as the actual output divided by 10,000. This is then the output noise referred to the input. The equivalent bandwidth for testing is 1 Hz.

There are certain instances where the test circuit or the Transistor Noise Analyzer are not adequate to measure $\bar{e}_N$ at certain frequencies over certain bandwidths in the $1/f^n$ region. The rms noise over a bandwidth from f_{low} to f_{high}, where there is a $1/f^n$ characteristic over the entire range, can be computed as

$$\bar{e}_N = \left[\bar{e}_N \text{ known}\right] \cdot \left[f_{known} \cdot \ln\left(\frac{f_{high}}{f_{low}}\right)\right]^{1/2n} \qquad (18)$$

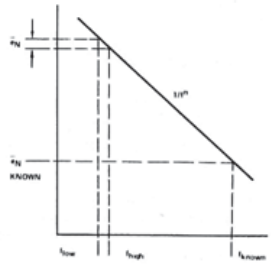
Figure 11 represents this equation graphically. For example, $\bar{e}_N$ known = 70 x 10^{-9} V/√Hz at 10 Hz. How much noise is in the band from 4.5 to 5.5 Hz? The noise has a $1/f^1$ characteristic over the entire range. Thus

$$\bar{e}_N = \left[70 \times 10^{-9}\right] \cdot \left[10 \cdot \ln\left(\frac{5.5}{4.5}\right)\right]^{1/2} \text{ Volts} \qquad (19)$$

or

$$\bar{e}_N = 99.16 \times 10^{-9} \text{ V}/\sqrt{\text{Hz}} \text{ @ } 4.975 \text{ Hz}, \qquad (20)$$

4.975 Hz is the mean center frequency where $f_{mean} = (f_{low} \cdot f_{high})^{1/2}$.



Computing rms Noise Over a Bandwidth
Figure 11

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$\bar{i}_N$ measurements are difficult to implement at best. At frequencies below f_2 in Figure 2, $\bar{i}_N$ is assumed to have a constant level or "white" noise characteristic which may be correlated to gate current, I_G. From Equation (16) I_G is established as the measured bulk gate current. Because measured gate current (I_G) is the result of all conductances at the gate, the resultant gate current and the computed $\bar{i}_N$ due to bulk material can be assumed to be this value or less.

The total equivalent input noise of the FET can be approximated by[6]

$$\bar{e}_{ni}^2 = \bar{e}_T^2 + \bar{e}_N^2 + \bar{i}_N^2 \cdot R_G^2 \quad (21)$$

where $\bar{e}_T^2$ is the thermal noise of the generator resistance R_G and $\bar{e}_{ni}^2$ is the total noise referred to the input. This approximation assumes that the equivalent noise voltage and the current generators vary independently. Equation (21) implies that $\bar{i}_N^2$ can be calculated if $\bar{e}_N^2$, $\bar{e}_T^2$ and total noise $\bar{e}_{ni}^2$ are known. The difficulty here is that in MOS or junction FETs, the R_G must be very large to detect the anticipated small value of $\bar{i}_N$. However, when R_G is very large $\bar{e}_T^2$ is much greater than $\bar{i}_N^2 \cdot R_G^2$. For example, over a 1 Hz bandwidth at 25°C, if R_G is equal to 100 MΩ, then

$$\bar{e}_T^2 = 4kTR_G = 4 \times 1.38 \times 10^{-23} \times 2.95 \times 10^2 \times 10^8 = 1.63 \times 10^{-12}\ V/\sqrt{Hz}. \quad (22)$$

Anticipated $\bar{i}_N$ is

$$\bar{i}_N \approx 10^{-15}\ Amperes/\sqrt{Hz} \quad (23)$$

and

$$\bar{i}_N^2 = 10^{-30}\ Amperes/\sqrt{Hz}. \quad (24)$$

Thus

$$\bar{i}_N^2 \cdot R_G^2 = 10^{-30} \cdot 10^{16} = 10^{-14}\ V/\sqrt{Hz}. \quad (25)$$

Therefore, $\bar{i}_N^2 \cdot R_G^2$ is much less than $\bar{e}_T^2$, which renders this method of finding $\bar{i}_N$ impractical for most common MOS FETs or junction FETs.

An improved method of measuring $\bar{i}_N^2$ is to substitute a low-loss mica capacitor for resistor R_G. The mica capacitor by definition does not have equivalent thermal noise voltage, and thus Equation (21) becomes

$$\bar{e}_{ni}^2 = \bar{e}_N^2 + \bar{i}_N^2 \cdot X_C^2 \quad (26)$$

(where X_C = capacitive reactance)

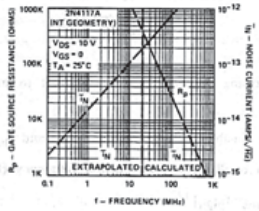
or

$$\bar{i}_N = \frac{(\bar{e}_{ni}^2 - \bar{e}_N^2)^{1/2}}{X_C} \quad (27)$$

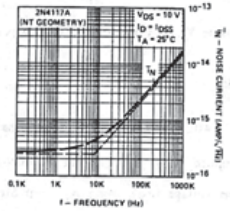
When a 10 pF mica capacitor was used in the evaluation circuit (up to a frequency of 100 Hz) a correlation of from 80 to 90% was obtained when compared to $\bar{i}_N^2$ computed from measured gate current readings.

At frequencies above 100 Hz direct computation of $\bar{i}_N$ via the capacitor method becomes unwieldy because of the rapid decrease in capacitor reactance at these frequencies.

In calculating $\bar{i}_N$ at higher frequencies, an alternate method is to measure (R_p) the real part of the gate-source impedance of the FET.[7] When R_p is measured at various frequencies, the equivalent short-circuit input noise current ($\bar{i}_N$) can be computed as a function of frequency (See Equation (17)). A convenient instrument to measure R_p is the Hewlett-Packard Type 250A Rx meter or equivalent. The Type 250A Rx meter can measure R_p accurately up to 200K ohms. As is shown in Figure 12, this establishes the low frequency limit of 20 MHz for $\bar{i}_N$ computed via direct measurement of R_p for the Siliconix FET Type 2N4117A. For frequencies between 100 Hz and 20 MHz, $\bar{i}_N$ must be extrapolated, as is shown in Figures 12 and 13. For FET types with lower R_p (such as the Siliconix 2N4393) $\bar{i}_N$ can be computed down to 2 MHz, and hence extrapolated $\bar{i}_N$ between 100 Hz and 100 kHz is more accurate.



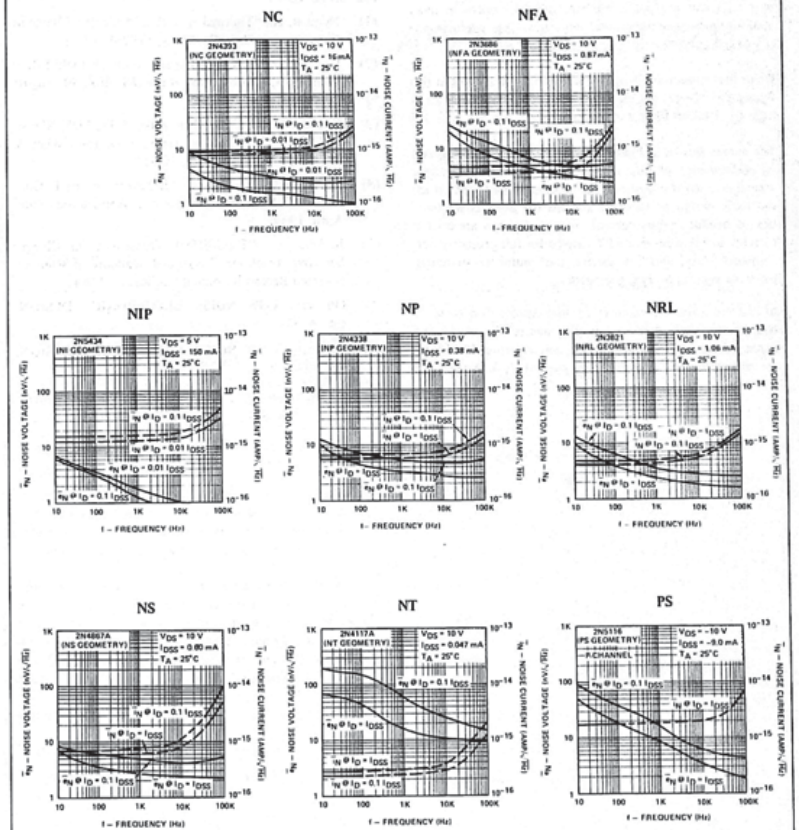
Low Frequency Limit for Calculated $\bar{i}_N$
Figure 12



Extrapolated $\bar{i}_N$ vs Frequency
Figure 13

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The following are representative $\bar{e}_N$, $\bar{i}_N$ curves for Siliconix J-FET products. Of particular importance is the geometry which by its design governs the basic noise characteristics of product types derived from it.



FET Noise Characteristics by Geometry
Figure 14

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CONCLUSION

Contemporary junction FETs have noise voltages ($\bar{e}_N$) equal to those found in low-noise bipolar transistors. Each type of device has a different operating mechanism: the FET is voltage-actuated, while the bipolar transistor is current-actuated. Hence, FETs have an inherently lower noise current ($\bar{i}_N$) and are preferred over bipolar devices in most audio-frequency applications where low-noise performance is a design requirement.

When bias points are properly selected, as described in this Application Note, the excellent low-noise characteristics of high g_{fs} junction FETs can be realized.

The curves shown in Figure 14 are representative of $\bar{e}_N$ and $\bar{i}_N$ performance of Siliconix junction FETs. Of particular importance in these curves is the process geometry by which the basic design of the FET governs the noise characteristics of product types derived from it. Readers are invited to refer to the Siliconix FET catalog for full geometry performance data, and for specific part numbers stemming from the generic process geometries.

In the measurement section of this Application Note, it was shown that direct $\bar{e}_N$ measurements can readily be made. $\bar{i}_N$ can be guaranteed at frequencies below 100 Hz by measuring the DC operating gate current (I_G). When I_G is known, $\bar{i}_N$ can be extrapolated from frequencies below 100 Hz to predict noise performance at frequencies to 100 kHz.

REFERENCES

(1) Nyquist, H., "Thermal Agitation of Electric Charge in Conductors," **Phys. Review** 32 (1928), p 110.

(2) Van der Ziel, A., "Thermal Noise in Field-Effect Transistors," **Proceedings of the IRE**, Vol. 50, August 1962, pp 1808-1812.

(3) Fitchen, F.C. and Motchenbacher, C.D., LOW NOISE ELECTRONIC DESIGN, 1st Edition, John Wiley & Sons, New York, 1973, pp 103-107.

(4) MacDonald, Charles L., "Behavior of FET Gate Current," Siliconix incorporated Application Note, April, 1969.

(5) Radeka, V., "Field-Effect Transistors in Charge-Sensitive Amplifiers," National Academy of Sciences, National Research Council Publication 1184.

(6) Op. cit., LOW NOISE ELECTRONIC DESIGN, pp 30-31.

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APPLICATION NOTE

FETs for Video Amplifiers

INTRODUCTION

The field-effect transistor lends itself well to video amplifier applications. Gain bandwidth products in excess of 250 MHz may be easily achieved using simple one or two transistor circuits. DC input resistances in the tens of megohms range may also be easily achieved while input capacitances may be significantly reduced to less than 1 pF by well known circuit techniques. Video amplifiers have applications in communications and pulse amplifying circuits and normally operate up to 100 MHz.

Behavior of FET Input Resistance

A prime FET parameter, input impedance, has a large effect in determining the frequency response of a FET video amplifier. It is not a simple RC network but one in which the real and imaginary parts are a function of frequency.

The voltage generator source resistance R_g and the FET input impedance Z_{in} form a frequency sensitive attenuation network. The larger the R_g, the worse will be the frequency response, and vice versa. Examining this in greater detail, consider the input equivalent circuit of a FET connected in the common source configuration,

where

R_{gs} and R_{gd} = bulk series gate resistance
C_{gs} and C_{gd} = bulk series gate capacitance
G_{oss} = output conductance

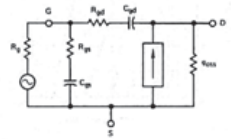


Figure 1

For this analysis the gate source leakage resistance has been ignored due to its high value. Redrawing the input equivalent circuit as a simple parallel RC combination results in

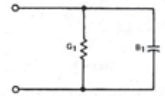


Figure 2

where

$$G_1 = \text{Re}\,|Y_{in}| = \frac{\omega^2[T_1C_1(1+\omega^2T_2^2) + T_2C_2(1+\omega^2T_1^2)]}{1-(\omega^2T_1T_2)^2 + \omega^2(T_1^2+T_2^2)} \quad (1)$$

and

$$B_1 = \text{Im}\,|Y_{in}| = \frac{\omega[C_1(1+\omega^2T_2^2) + C_2(1+\omega^2T_1^2)]}{1-(\omega^2T_1T_2)^2 + \omega^2(T_1^2+T_2^2)} \quad (2)$$

where

$$T_1 = C_{gd}R_{gd}$$
$$T_2 = C_{gs}R_{gs} \quad (3)$$

The input resistance varies inversely with the square of the frequency (see Figures 3 and 4) while the input reactance is inversely proportional to the frequency (see Figure 3).

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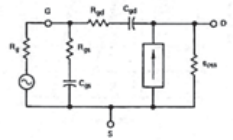


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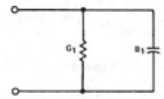


Figure 2

where

$$G_1 = \mathrm{Re}\,|Y_{in}| = \frac{\omega^2[T_1C_1(1+\omega^2T_2^2)+T_2C_2(1+\omega^2T_1^2)]}{1-(\omega^2T_1T_2)^2+\omega^2(T_1^2+T_2^2)} \quad (1)$$

and

$$B_1 = \mathrm{Im}\,|Y_{in}| = \frac{\omega[C_1(1+\omega^2T_2^2)+C_2(1+\omega^2T_1^2)]}{1-(\omega^2T_1T_2)^2+\omega^2(T_1^2+T_2^2)} \quad (2)$$

where

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$$T_2 = C_{gs}R_{gs} \quad (3)$$

The input resistance varies inversely with the square of the frequency (see Figures 3 and 4) while the input reactance is inversely proportional to the frequency (see Figure 3).

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In common-source circuits, $1/G_1$ will typically fall to < 2K ohms at 100 MHz while C_1 remains substantially constant at least up to 1000 MHz. Figures 3 and 4 below exhibit these relationships.

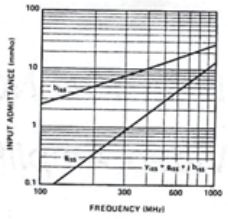


Figure 3

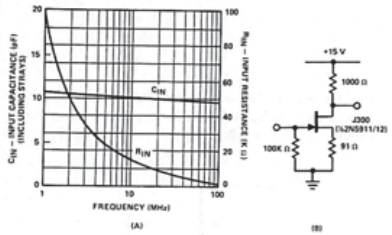


Figure 4

To maintain low input capacitance, and thus a high input impedance over a wide frequency range, feedback may be applied to most circuits. Such techniques are explored in "FET and Bipolar Cascade" section (page 5). The effect of R_g on the frequency response is shown in Figures 6, 9, 11, 13 where various amplifier configurations are investigated.

Circuits to Consider

Five video amplifier circuits are considered. They are:

- Common-Source Configuration
- Shunt-Peaked Common-Source Configuration
- Source Follower
- Cascode Amplifier
- FET and Bipolar Cascade

Common-Source Circuit[1]

The circuit of Figure 5 features high input impedance and high voltage gain. The drain resistor is set at 560 ohms to maintain good bandwidth which, with 50-ohm generator impedance, is determined primarily by the drain load components. These are:

$$R_D = 560\ \Omega \quad (4)$$

$$C_T = C_{gd} + C_D + C_S \quad (5)$$

C_{gd} = 2.0 pF, C_D the VTVM probe, 2.0 pF, and C_S is circuit stray capacitance of 3 pF.

$$C_T = 2 + 2 + 3 = 7\ \text{pF} \quad (6)$$

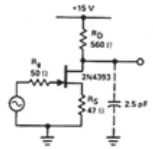


Figure 5

The 3-dB frequency ω_3 is given by:

$$\omega_3 = \frac{1}{C_T R_D} \quad (7)$$

$$= \frac{1}{7 \times 10^{-12} \times 560} \quad (8)$$

$$\omega_3 = 255 \times 10^6 \quad (9)$$

$$f_3 = 39\ \text{MHz} \quad (10)$$

The low frequency voltage gain for this configuration is given by:

$$A_V = \frac{g_{fs} R_D}{1 + g_{fs} R_S} \quad (11)$$

$$A_V = 4.9 \quad (12)$$

where

g_{fs} = 15 mmho when I_D = 12 mA, the quiescent current

$$R_D = 560\ \Omega \quad (13)$$

$$R_S = 47\ \Omega \quad (14)$$

Measured Performance

Figure 6 shows the frequency response of the circuit. The low-frequency gain was measured at 4.5 and the 3-dB bandwidth at 44 MHz giving a gain bandwidth product of 197 MHz. This compares with a calculated gain bandwidth of 191 MHz.

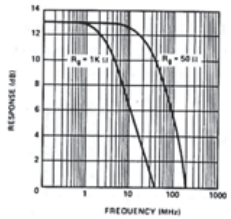


Figure 6

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Effect of Increasing Generator Impedance

If the generator resistance R_g is increased to 1K ohm, the input time constant of the FET is increased. The bandwidth of the amplifier is now determined primarily by the input time constant which consists of generator impedance (R_g = 1K ohm) shunted by C_{in} (see Figure 7).

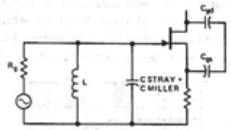


Figure 7

where

$$C_{in} = \left(1 + \frac{g_{fs} R_D}{1 + g_{fs} R_S}\right) C_{gd} + \left(1 - \frac{g_{fs} R_S}{1 + g_{fs} R_S}\right) C_{gs} + \text{Strays}$$

$$= (5.9 \times 3.5) + (0.6 \times 10) + 3. \quad (15)$$

$$C_{in} = 30\ \text{pF} \quad (16)$$

where

$$C_{gd} = 3.5\ \text{pF} \quad (17)$$

$$C_{gs} = 10\ \text{pF} \quad (18)$$

The corresponding 3-dB frequency is given by:

$$\omega_3 = \frac{1}{C_{in} R_g} \quad (19)$$

$$= \frac{1}{30 \times 10^{-12} \times 10^3} = \frac{10^9}{30} \quad (20)$$

$$f_3 = 5.3\ \text{MHz} \quad (21)$$

which agrees closely with the measured bandwidth as shown in Figure 6.

Shunt-Peaked Common-Source Circuit

The frequency response of the resistance-loaded common-source circuit may be significantly extended by shunt peaking at the gate and/or drain. Consider first the gate circuit. Here an inductor may be connected in shunt with the gate and set to such a value that it forms a tuned circuit with the FET input capacitance. The frequency of resonance is determined by:

$$f_o = \frac{1}{2\pi\sqrt{LC_{in}}} \quad (22)$$

where

$$C_{in} = C_{iss} + C_{Stray} + C_{Miller} \quad (23)$$

The response of an input signal of frequency f_o will then be boosted to an extent depending on the loaded Q of the tuned circuit; the loaded Q in turn is dependent on the unloaded Q of inductor L, R_g and the FET input resistance.

Next consider shunt peaking in the drain circuit. In Figure 8 the inductor L is set to such a value that a low Q tuned circuit is formed; the resonating capacitance C is the parallel combination of C_{gd} plus stray and load capacitances. For a flat response, the LC circuit is tuned to the 3-dB frequency of the resistance loaded circuit of Figure 5. (See Appendix.)

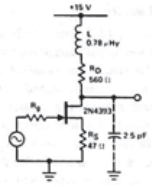


Figure 8

The required value of L is:

$$L = \frac{R_D^2 C}{2}, \text{ and for the circuit in Figure 8.} \quad (24)$$

$$= 0.78\ \mu\text{H} \quad (25)$$

where

$$R_D = 560\ \Omega \quad (26)$$

$$C = C_{gd} + C_{Stray} + C_{VTVM\ PROBE} \quad (27)$$

$$C = 1.2 + 1.3 + 2.5 = 5\ \text{pF} \quad (28)$$

Due to the low circuit Q (about 5), the value of L is not critical.

The 3-dB bandwidth shown in Figure 9 now extends to 67 MHz giving a gain bandwidth product of:

$$67 \times 4.2 \approx 281\ \text{MHz} \quad (29)$$

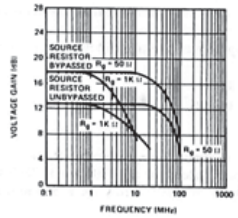


Figure 9

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When R_S is bypassed by a 0.1 capacitor, the low frequency voltage gain is given simply by:

$$A_V = g_{fs} R_D \quad (30)$$

$$= 15 \times 10^{-3} \times 560 \quad (31)$$

$$= 8.4\ (18.5\ dB) \quad (32)$$

The gain bandwidth product tends to remain constant whether R_S is bypassed or not and this effect is shown in Figure 9.

Source-Follower Circuit[2]

A J300 is used in the FET source-follower circuit, Figure 10, because of its low input capacitance and high g_{fs} which remains high at the frequency range of interest. A source follower exhibits a high input impedance and low output impedance. The real part of the output impedance is the reciprocal of g_{fs} which is independent of frequency up to about 600 MHz. The input capacitance is $C_{gd} + C_{gs}(1 - A_V)$ which, in this case, is approximately 1.5 pF maximum. The input capacitance is also independent of frequency and independent of load when the load is larger than the output resistance R_O.

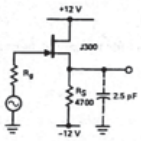


Figure 10

The frequency response is dependent mainly on the generator internal impedance. For example, when R_g is increased to 1K ohm the bandwidth falls to 80 MHz. In this particular circuit, the low-frequency voltage gain is 0.94.

The input resistance is proportional to $1/f^2$ as explained in the section, "Behavior of Input Resistance," and at some high frequency will go negative, particularly if the source resistor is large. For example, with the circuit in Figure 10, the input resistance is high at 10 MHz but in the negative resistance region at 100 MHz. However, when R_S is 1000 ohms, the input resistance is real at this frequency.

The voltage gain of a source follower is given by:

$$A_V = \frac{g_{fs} R_S}{1 + g_{fs} R_S} \quad (33)$$

Thus A_V is almost independent of R_S when R_S is large. Using typical values for the J300 (or ½ 2N5912) in Figure 10, the drain current is 3 mA, g_{fs} is 5 mmho and R_S 4700 ohms,

$A_V = 0.96$

which is near the measured value of 0.94. Measured performance is shown in Figure 11. The output resistance of this source follower is given by:

$$R_o \cong \frac{1}{g_{fs}} = \frac{1}{5 \times 10^{-3}} = 200\ \Omega \quad (34)$$

and in this circuit, R_O was measured at 165 ohms. The source follower is a useful versatile circuit which may be used as an impedance converter, level shifter, buffer stage, or as an input circuit to an op amp or feedback amplifier.

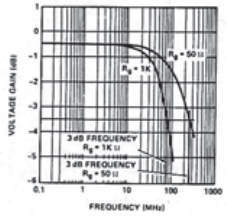


Figure 11

Cascode Circuit

The cascode circuit has applications as a buffer amplifier for use with high stability oscillators or in low level power amplifiers[2] mainly due to its low reverse transfer characteristics. The advantages and considerations of this configuration, Figure 12, are similar to those listed for the common-source circuit. An extra advantage exists in the cascode circuit, namely the low input capacitance:

$$C_{in} = C_{gs} + (1 - A_V) C_{dg} \quad (35)$$

$$C_{in} = C_{iss} + C_{gd} \quad (36)$$

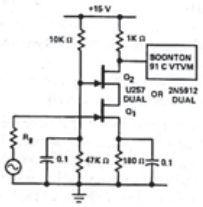


Figure 12

where A_V is the voltage gain from Q_1 gate to Q_1 drain which is essentially unity. C_{iss} for the U257 dual FET is 5 pF and C_{dg} is 1 pF, therefore

$C_{in} = 5 + 1 = 6$ pF, excluding strays of 4 pF

Thus Miller effect is minimized and a good gain bandwidth product is achieved.

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Figure 13 shows cascode frequency response. The voltage gain at low frequency is 15 dB (x 5.6) and the bandwidth is 24.5 MHz with a generator impedance of 50 ohms. Gain bandwidth product is 137 MHz.

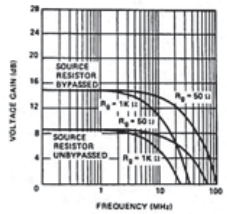


Figure 13

FET and Bipolar Cascade

The FET and bipolar transistor combination of Figure 14 makes a good video amplifier because the FET input provides the voltage gain thus obtaining a superior gain bandwidth product. The feedback capacitor a-c couples the emitter to the drain. The a-c voltage at the gate is nearly equal to that at the source. This source voltage is d-c coupled to the base.

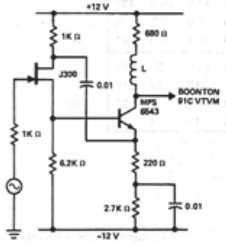


Figure 14

This produces an a-c voltage at the emitter whose amplitude is almost equal to that at the base. Thus at the FET, $v_g \cong v_s \cong v_d$ and all three signals are in phase. In this way Miller effect capacitance is largely eliminated.

The frequency response of this circuit is controlled by the output time constant if f_t of the transistor is much greater than the amplifier bandwidth. In the circuit shown the a-c load is 2.5 pF.

CONCLUSION

The input resistance of a FET is inversely proportional to the frequency squared, while the input capacitance remains constant to at least 1000 MHz.

Several video amplifier configurations are considered. The common-source circuit is considered first: in the example, the low frequency gain is 4.5 and the 30-dB bandwidth 44 MHz (gain bandwidth 197 MHz). By shunt peaking in the drain circuit, gain bandwidth is increased to 260 MHz. The simple source-follower circuit gives a gain near unity with GBW almost 300 MHz and an output resistance of $1/g_{fs}$. The cascode circuit features a low input capacitance and GBW of 137 MHz. The circuit featuring the best gain bandwidth is the FET and bipolar combination. A gain of 11 dB and bandwidth of 90 MHz is achieved.

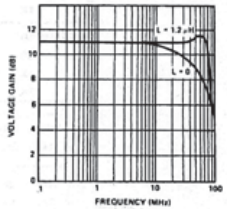


Figure 15

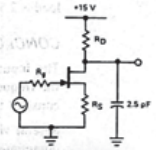
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APPENDIX

Selection of Video Amplifier Designs with Performance Summary

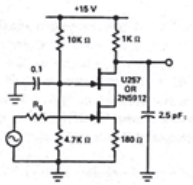
Note. All output voltages measured with Boonton 91C VTVM.

Common Source Stage



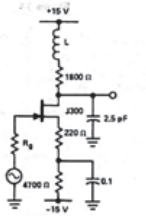
Device	R_g Ω	R_S Bypassed	R_S Ω	R_D Ω	Gain	dB	C_{in} pF	BW MHz	GBW MHz
2N4393	50		47	560	4.5	13.0		44	197
	50	x	47	560	7.5	17.5		40	300
	1K		47	560	4.5	13.0		5.0	22
	1K	x	47	560	7.5	17.5		3.5	26
J300 ½ 2N5912	50		91	1K	3.8	11.6	11.0	27.5	103
	50	x	91	1K	6.3	16.0	14.5	30.0	189
	1K		91	1K	3.8	11.6	11.0	9.5	36
	1K	x	91	1K	6.3	16.0	14.5	6.5	41
2N4416	50		120	1.5K	3.9	11.8	11.5	25	98
	50	x	120	1.5K	6.2	15.8	13	19	118
	1K		120	1.5K	3.9	11.8	11.5	8	31
	1K	x	120	1.5K	6.2	15.8	13	7	44

Cascode



R_g Ω	R_S Bypassed	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50		2.7	8.5	9	27	73
50	x	5.6	15	11.5	27	151
1K		2.7	8.5	9	9.5	73
1K	x	5.6	15	11.5	9.0	51

Common-Source Circuit

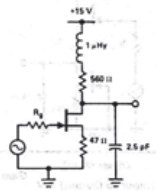


R_g Ω	L µH	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50	0	3.5	11	2	20	70
1K	0	3.5	11	2	11	38.5
50	8	3.5	11	2	37	130
1K	15	3.5	11	2	17	60

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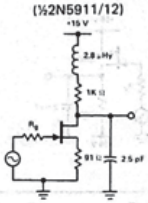
Shunt-Peaked Common-Source Stage

2N4393



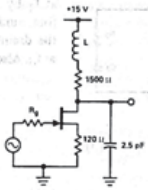
R_g Ω	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50		4.2	12.5	66	277
50	x	7.5	17.5	54	405
1K		4.2	12.5	6.0	25
1K	x	7.5	17.5	3.5	26

J300 (½2N5911/12)



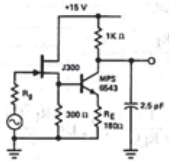
R_g Ω	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50		3.9	11.8	67	262
50	x	6.3	16.0	67	421

2N4416

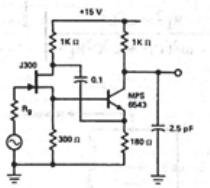


R_g Ω	L µH	R_S Bypassed	Gain	dB	BW MHz	GBW MHz
50	4		3.9	11.8	45	175
50	4	x	6.2	15.8	40	248
50	5	x	6.2	15.8	45	279

Common-Drain Common-Emitter Stage



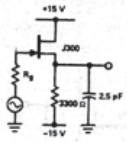
R_g Ω	R_E Bypassed (0.1 µF)	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50		3	9.5	2.0	39	117
50	x	25	28	2.0	21	525
1K		3	9.5	2.0	13	39
1K	x	25	28	2.0	11	275

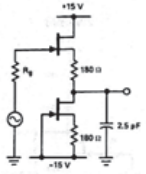


R_g Ω	Gain	dB	C_{in} pF	BW MHz	GBW MHz
50	5.6	15	1.0	32	179
1K	5.6	15	1.0	15	84

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Source-Follower Circuit





R_g Ω	Gain	C_{in} Stray pF	C_{in} Total pF	R_o Ω	BW MHz	GBW MHz
50	0.92	2.2	2.7	165	350	326
1K	0.92	2.2	2.7	165	55	50

Note, R_o = output resistance of the source follower.

Dual FET	R_g Ω	Offset (Max) (Input to Output) mV	Gain	BW MHz	GBW MHz
U257 2N5912	50	100	0.98	70	69
	1K	100	0.98	15	14.7
U232	50	10	0.98	85	83
	1K	10	0.98	13	12.7

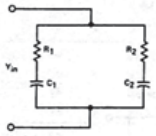
Derivation of Input Admittance Terms

where

$R_1 = R_{gs}$ $C_1 = C_{gs}$ (1)

$R_2 = R_{gd}$ $C_2 = C_{gd}$ (2)

$s = j\omega$



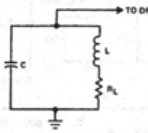
$$Y_{in} = \frac{sC_1}{R_1C_1\,s+1} + \frac{sC_2}{R_2C_2\,s+1} \quad (3)$$

$$= \frac{-\omega^2C_1C_2(R_1+R_2) + s(C_1+C_2)}{(1-\omega^2R_1R_2C_1C_2) + s(C_1R_1+C_2R_2)} \quad (4)$$

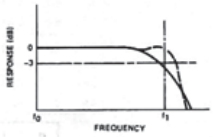
Derivation of Shunt Peaking Formula

The equivalent circuit of the drain load is shown in the Figure below. The total impedance seen by the drain is given by:

$$Z = \left[\frac{R_L{}^2+\omega^2L^2}{(1-\omega^2LC)^2+\omega^2C^2R_L{}^2}\right]^{\frac{1}{2}} \quad (5)$$



The response below shows the "normal" 3-dB frequency without peaking – f_1. It is now required to raise the response at f_1 by 3 dB to achieve a maximally flat response. Therefore, under these conditions the total impedance seen by the drain at f_1 must equal the impedance seen by the drain at f_o. Also at f_1, $X_C = R_L$. Substituting for X_C in Equation 5:



$$R_L{}^2 = \frac{R_L{}^2+\omega^2L^2}{\left(1-\frac{\omega L^2}{R_L}+1\right)} \quad (6)$$

$$R_L{}^2 - 2\omega LR_L + \omega^2L^2 + R_L{}^2 = R_L{}^2 + \omega^2L^2 \quad (7)$$

$$R_L{}^2 = 2\omega LR_L \quad (8)$$

$$R_L = 2\omega L \quad (9)$$

$$L = \frac{R_L}{4\pi f_1} \quad (10)$$

and

$$f_1 = \frac{1}{2\pi R_LC} \quad \therefore L = \frac{R_L{}^2C}{2} \quad (11)$$

REFERENCES

1. Sherwin, J.S., "Liberate Your FET Amplifier," Electronic Design, May 1970.
2. Siliconix Application Tip, "FET Cascade Circuits Reduce Feedback Capacitance," August 1970.

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APPLICATION NOTE

FETs in Balanced Mixers

Ed Oxner

INTRODUCTION

When high-performance, high-frequency junction field-effect transistors (JFETs) are used in the design of active balanced mixers, the resulting FET mixer circuit demonstrates clearly superior characteristics when compared to its popular passive counterpart employing hot-carrier diodes. Comparison of several types of mixers is made in Table I. The advantages and disadvantages of semiconductor devices currently used in various mixer circuits are shown in Table II.

Why an Active Mixer?

Active mixing suggests high-level mixing capability. High level mixing in turn infers that active mixers outperform passive mixer circuits in terms of wide dynamic range and large-signal handling capability. Additionally, the active mixer offers improved conversion efficiency over the passive mixer, permitting relaxation of the IF amplifier gain requirements and even possible elimination of the customary RF amplifier front end.

Initial evaluation of the active FET mixer will imply a disadvantage because of local oscillator drive requirements; bipolar devices in low-level mixers require very little drive power. However, in high-level mixing this disadvantage is overcome in that drive requirements at such mixing levels are generally the same, no matter whether bipolar or FET devices are used.

Why FETs for Balanced Mixers?

The performance priorities of modern communication systems have stringent requirements for wide dynamic range, suppression of intermodulation products, and the effects of cross-modulation. All of the foregoing parameters must be considered before noise figure and gain are taken into account.

Since FETs have inherent transfer characteristics approximating a square-law response, their third-order intermodulation distortion products are generally much smaller than

Table I

Characteristic	MIXER TYPE: Single-Ended	Single Balanced	Double Balanced
Bandwidth	Several decades possible	Decade	Decade
Relative IM Density	1.0	0.5	0.25
Interport Isolation	Little	10-20 dB	>30 dB
Relative L.O. Power	0 dB	+3 dB	+6 dB

Table II

DEVICE	ADVANTAGES	DISADVANTAGES
Bipolar Transistor	Low Noise Figure High Gain Low D.C. Power	High IM Easy Overload Subject to Burnout
Diode	Low Noise Figure High Power Handling High Burn-out Level	High L.O. Drive Interface to I.F. Conversion Loss
JFET	Low Noise Figure Conversion Gain Excellent IM products Square Law Characteristic Excellent Overload High Burn-out Level	Optimum Conversion Gain not possible at Optimum Square Law Response Level High L.O. Power
Dual-Gate MOS FET	Low IM Distortion AGC Square Law Characteristic	High Noise Figure Poor Burnout Level Unstable

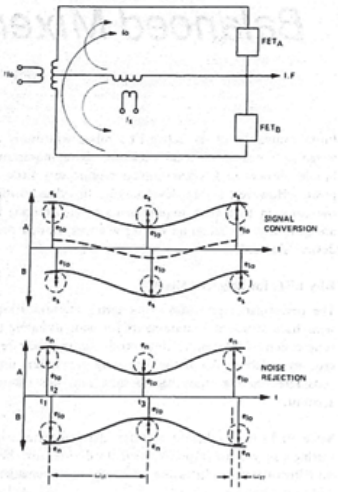
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those of bipolar transistors. Harmonic distortion and cross-modulation effects are third-order-dependent, and thus are greatly reduced when FETs are used in active balanced mixers.

A secondary advantage derives from available conversion gain, so that the FET mixer becomes simultaneously equivalent to both a demodulator and a preamplifier.

First Order Balanced Mixer Theory

Essential details of balanced mixer operation, including signal conversion and local oscillator noise rejection, are best illustrated by signal flow vector diagrams (Figure 1).



Signal and Noise Vectors
Figure 1

Energy conversion into the intermediate frequency (IF) passband is the major concern in mixer operation. In the following analysis, both the signal and noise vectors are shown progressing (rotating) at the IF rate (ω_{if}); the resulting wave occurs through vector addition.

The analysis of local oscillator noise rejection (Figure 1) assumes, for simplicity of explanation, that noise is coherent. Thus at some point in time (t_1) the noise component (e_n) is "in phase" with the local oscillator vector (e_{lo}) and FET "A" (the rectifying element) is ON; the JFET mixer acts as a switch, with the local oscillator acting as the switch drive signal. One-half cycle later, at time t_2, the signal flow is reversed for both the local oscillator vector and the noise component, FET "A" is OFF and FET "B" is ON. Moving ahead an additional one-half of the IF cycle, FET "A" is again ON, but the noise component has advanced 180° ($\omega_{if}t$) through the coupling structure, and is now "out of phase". The process continually repeats itself.

The end result of this averaging (detection) is the cancellation of the noise which originated in the local oscillator, providing that the mixer balance is precise.(1)

The analysis of the conversion of the signal to the IF passband is similar, but the signal is injected into the coupling structure at the equipotential tap. Thus at time t_2, the signal vector (e_s) is "out of phase" with the local oscillator vector, e_{lo}. The resulting envelope develops a cyclic progression at the IF rate, since the signal is "demodulated" by the mixing action of the FETs.

A schematic of a *prototype* balanced mixer is shown in Figure 2. Design criteria, in order of priority, include the following:

(1) Intermodulation and Cross-Modulation
(2) Conversion Gain
(3) Noise Figure
(4) Selecting the Proper FET
(5) Local Oscillator Injection
(6) Designing the Input Transformer
(7) Designing the IF Network

Intermodulation and Cross-Modulation

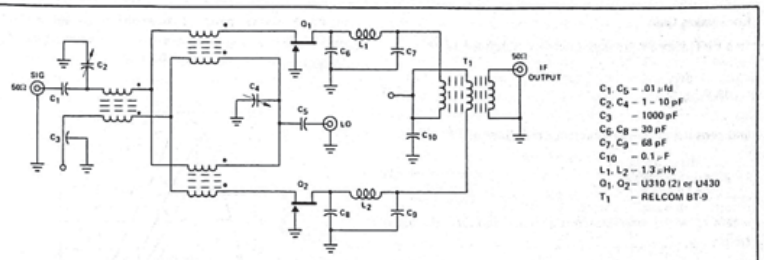
A basic aim in mixer design is to avoid the effects of intermodulation product distortion and crossmodulation. Part of the problem may be resolved by using a balanced mixer circuit.

The active transfer function of the FET is represented by a voltage-controlled current source. For both crossmodulation and intermodulation, the amount of distortion is proportional to the amplitude of the gate-source voltage. Since input power is proportional to input voltage, and inversely proportional to input impedance, the best FET IM and cross-modulation performance is obtained in the common-gate configuration where the impedance is lowest.(2)

When JFETs are used as active mixer elements, it is important that the devices be operated in their square-law region. Operation in the FET square-law region will occur with the device in the depletion mode. Considerable distortion will result if the FET is operated in the enhancement mode (positive, for an N-channel FET); by analogy, the problems encountered are similar to those which arise when positive drive is placed on the grid of a vacuum tube.

Square-law region operation emphasizes the importance of establishing proper drive levels for both quiescent bias and the local oscillator. The maximum conversion transconductance, g_c, is achieved at about 80% of the FET gate cutoff voltage, $V_{GS(off)}$, and amounts to about 25% of the forward transconductance, g_{fs}, of the FET when used as an amplifier.

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Prototype Active Balanced Mixer
Figure 2

Since conversion gain (or loss) must be considered, it is common to equate voltage gain A_v, as:

$$A_v = g_c R_L \qquad (1)$$

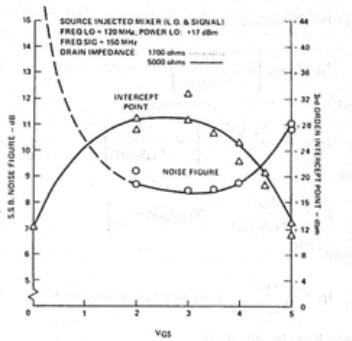
where g_c is the conversion transconductance and R_L is the FET drain load.

An attempt to achieve maximum conversion gain by indiscriminately increasing the drain load resistance will adversely affect any design priority concerning distortion – particularly intermodulation product distortion.

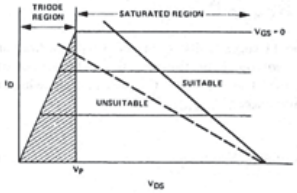
Distortion takes different forms in mixers. Most obvious is that distortion which will occur if the FET is driven into the enhancement mode, as noted earlier. A more pernicious form is drain load distortion. And finally, there is the so-called "varactor effect."

The most frequent cause of poor mixer performance stems from signal overloading in the drain circuit. Excessive drain load impedance degrades the intermodulation characteristics and produces unwanted crossmodulation signals.(3) A characteristic of the FET balanced mixer is that the correct drain load impedance is inversely proportional to the value of the conversion transconductance. Figure 3 shows the improvement in IM characteristics obtained in the prototype mixer with the drain load impedance reduced to 1700 Ω from 5000 Ω. Specifically, the dynamic load line must be plotted so that the signal peaks of the instantaneous peak-to-peak output voltage are not permitted to enter into the non-saturated ("triode") region of the FET. Suitable and unsuitable drain load lines are shown in Figure 4. Load impedance selection is quantified in Equations 18 through 20.

Distortion from the "varactor effect" is of secondary importance, and arises from an excessive peak voltage signal swing, where the changing drain-to-source voltage can cause a change in parasitic capacitance, C_{rss}, and give rise to harmonics.(4) A FET tends to be voltage-dependent when the drain voltage falls appreciably below 6 volts. If the source voltage (from the power supply) is also low and the drain load impedance is high, then distortion will develop. However, if proper steps are taken to prevent drain load distortion, the varactor effect will also be inhibited.



Comparison of Mixer IM Characteristics
Figure 3



Plotting Drain Load Lines
Figure 4

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Conversion Gain

In a FET, forward transconductance is defined as[5]

$$g_{fs} = \frac{dI_D}{dV_{gs}} \quad (2)$$

and conversion transconductance is defined as[6]

$$g_c = \frac{dI_{D(\omega i)}}{dV_{gs(\omega r)}} \quad (3)$$

where ωi = the intermediate frequency and ωr = the signal frequency.

The effects of time-varying local oscillator voltage, V_2, and the much smaller signal voltage, V_1, must be considered:

$$v_{gs} = V_1 \cos \omega_1 t + V_2 \cos \omega_2 t \quad (4)$$

For square law operation[7]

$$V_2 + V_{GS} \leqslant V_{GS(off)} \quad (5)$$

Drain current is approximately defined by[8]

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 \quad (6)$$

or[9]

$$I_D \approx \frac{g_{fso}\, V_{GS(off)}}{2}\left[1 - \frac{v_{gs}}{V_{GS(off)}}\right]^2 \quad (7)$$

or

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}}\left[V_{GS(off)} - v_{gs}\right]^2 \quad (8)$$

then[10]

$$I_D \approx \frac{g_{fso}}{2V_{GS(off)}} \text{ (complex Taylor expansion)} \quad (9)$$

which can be reduced to

$$I_{D(IF)} \approx \frac{g_{fso}}{2V_{GS(off)}} V_1 V_2 \cos(\omega_1 - \omega_2)t \quad (10)$$

and the conversion transductance is

$$g_c = \frac{g_{fso}}{2V_{GS(off)}} |V_2| \quad (11)$$

Equation 11 suggests that g_c increases without limit as V_2 increases without limit. However, to avoid operation of the FET in the "triode" region, the peak-to-peak swing of V_2 should not exceed $V_{GS(off)}$.

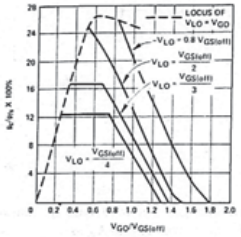
Thus

$$2\,V_2 \text{ peak} \leqslant V_{GS(off)} \quad (12)$$

or

$$V_2 \text{ peak} \leqslant \frac{V_{GS(off)}}{2} \quad (13)$$

Figure 5 shows plots of normalized conversion transconductance, g_c/g_{fs} versus normalized quiescent bias, $V_{GS}/V_{GS(off)}$, for different oscillator injections.

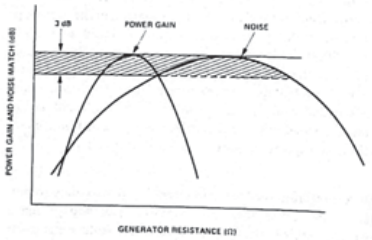


Normalized g_c/g_f vs. $V_{GS}/V_{GS(off)}$
(from "FET RF Mixer Design Technique", S.P. Kwok, WESCON Convention Record (1970) 8/1, p.2.)
Figure 5

Noise Figure

Like the common-gate FET amplifier, the common-gate FET balanced mixer is sensitive to generator resistance, R_g.[11] A change of a decade in R_g can produce a noise figure variation of as much as 3 dB.

In the design of the prototype FET active balanced mixer, the generator resistance of the FETs is established by the hybrid coupling transformer. Two important criteria for the FETs in the circuit are high forward transconductance, and a value of power-match source admittance, g_{igs}, which closely matches the output admittance of the coupling transformer. In the common-gate configuration, match points for optimum power gain and noise do not occur at the same value of generator resistance (Figure 6). Optimum noise match can only be achieved at the sacrifice of bandwidth.



Power Gain and Noise Matching
Figure 6

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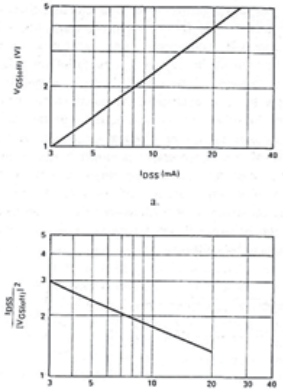
How to Select the Proper FET

Conversion efficiency is determined by conversion transconductance, g_c, which in turn is directly related to such FET parameters are zero-bias saturation current, I_{DSS}, and the gate cutoff voltage, $V_{GS(off)}$:

$$g_c = \frac{I_{DSS}}{V_{GS(off)}^2}|V_2| \quad (14)$$

$$\approx \frac{g_{fso}}{2V_{GS(off)}} \quad (15)$$

Equation 15 appears to indicate that FETs with high I_{DSS} are to be preferred. However, I_{DSS} and $V_{GS(off)}$ are related, and Figures 7A and 7B show that devices from a family selected for high I_{DSS} do *not* provide high conversion transconductance, but actually produce a lower value of g_c.



Relationship of I_{DSS} and $V_{GS(off)}$
Figure 7

Best mixer performance is achieved with "matched pairs" of JFETs. Basic considerations in selecting FETs for this application are gate cutoff voltage, $V_{GS(off)}$, for good conversion transconductance, and zero-bias saturation current, I_{DSS}, for dynamic range. A match to 10% is generally adequate. Among currently available devices, the Siliconix U310 and the dual U431 offer excellent performance in ooth categories; common-gate forward transconductance is 20,000 μmhos max at V_{DS} = 10 V, I_D = 10 mA, and f = 1 kHz.

There is, of course, the possibility that FET cost is a major consideration in evaluating the active balanced mixer approach – the familiar price/performance tradeoff. If this is the case, there are a number of other Siliconix FETs which will provide suitable alternatives to the U310. Remember, however, that conversion transconductance, g_c, can never be more than 25% of forward transconductance. Thus as tradeoff considerations begin, the first sacrifice to be made will be the degree of achievable conversion gain. Intermodulation performance will follow with the third tradeoff being available noise figure. Table III lists a number of possible alternatives to the U310.

Table III

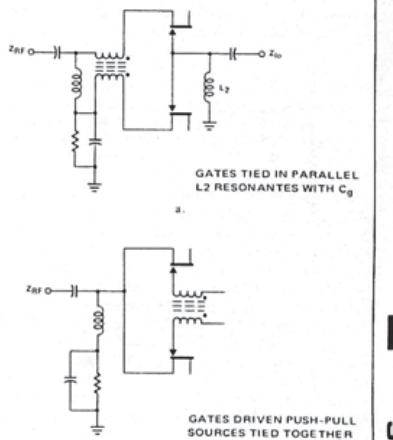
Typical Characteristic	DEVICE TYPE			
	U310*	2N5912	2N4416*	2N3823
g_m	14K	6K	5K	3.5K
I_{DSS}	40 mA	15 mA	10 mA	10 mA

*Similar devices are also available in plastic packages:
U310 (J310)
2N5397 (K300-18)
2N4416 (2N5486, K304-18)

Local Oscillator Injection

Low IM distortion products and noise figure, plus best conversion gain, will be achieved if the voltage swing of the local oscillator across the gate-to-source junction is held to the values presented in Figure 5. V_{LO} is expressed in terms of peak-to-peak voltage, while $V_{GS(off)}$ is a d.c. voltage.

Local oscillator injection can be made either through a brute-force drive into the JFET source through the hybrid input transformer, or through a direct-coupled circuit to the JFET gates where less drive will be required for the desired voltage swing. Two circuits to obtain direct gate coupling are suggested in Figure 8.



Alternate Forms of L.O. Injection
Figure 8

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The source-injection method is used in the design of the present mixer to maintain the inherent stability of a common-gate circuit. A minor disadvantage with the direct-drive method is that the required gate-to-source voltage swing requires considerable local oscillator input power. For source injection through the transformer, best mixer performance is obtained with a local oscillator drive level of +12 to +17 dBm across a 50-ohm load.

Conversely, direct coupling to the FET gates occurs at a higher impedance level and less local oscillator drive power is required. The functional tradeoff resulting when the gates are tied together is that shunt susceptance requires some form of conjugate matching, and thus brings about an undesirable reduction of instantaneous mixer bandwidth.

Designing the Input Transformer

Five criteria are important to the design of the hybrid input coupling transformer for best mixer performance. The impedance transformer must

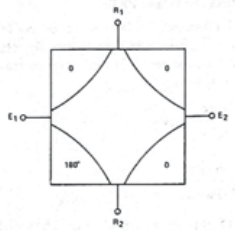
(1) Consist of four single-ended terminals, for the local oscillator, the input signal and FETs A and B

(2) Offer a match between either input to a symmetrical balanced load

(3) Provide as much isolation as possible between the signal and local oscillator ports (Figure 9)

(4) Maintain a differential phase of 180° across the symmetrical balanced loads

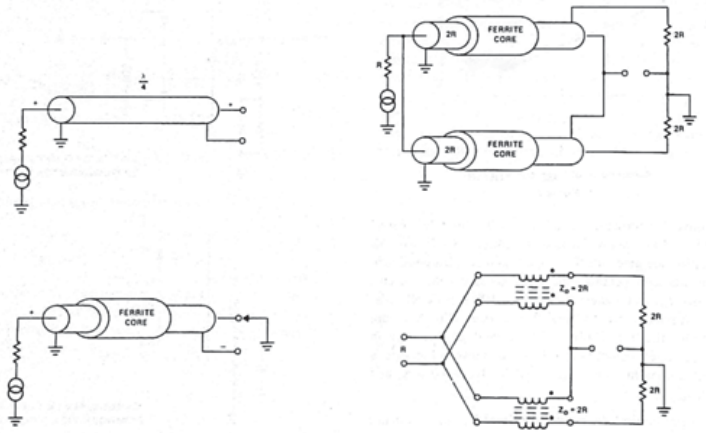
(5) Introduce the least possible amount of loss



4-Port Hybrid with Phase and Isolation

Figure 9

A transformer using ferrite cores and meeting these five requirements is derived from elementary transmission-line theory (Figure 10). Transmission line transformers have a low-frequency cutoff determined by the falloff of primary reactance as frequency is decreased. This reactance is determined by the series inductance of the transmission line conductors. On the other hand, high-frequency performance is enhanced by minimizing the physical length of the transmission line. Minimizing overall line length while maintaining suitable reactance can be accomplished by using a high-permeability core material such as a ferrite.[12] The transformer constructed for the balanced FET mixer closely resembles the balanced 4-port unsymmetrical 180° hybrid device described by Ruthroff.[13]



Hybrid Input Coupling Transformer

Figure 10

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Although Ruthroff does not discuss the method of determining the winding length of bifilar wire, a solution is offered by Pitzalis.[14] The Pitzalis definitions for wire length are as follows (Figure 11):

$$\text{max length} = \frac{7200n}{f_{upper}} \text{ (inches)} \qquad (16)$$

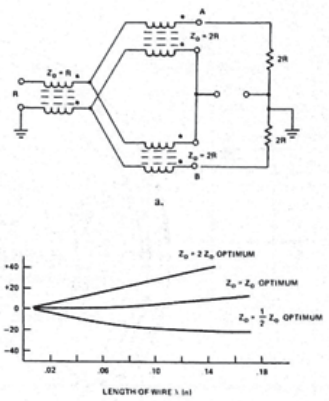
$$\text{min length} = \frac{20\,R_L}{(1 + \mu/\mu_o)\,f_{lower}} \text{ (inches)} \qquad (17)$$

where R_L = the load impedance, μ/μ_o = the relative permeability of the ferrite at the lower frequency, and n = a fractional wavelength determined by the amount of allowable phase error.

Selection of the ferrite core material is determined mainly by performance requirements. A prime consideration for wideband performance is the temperature coefficient of the ferrite, which must have a low loss tangent over the required temperature range, i.e., high Q.

In addition, an important design factor involves the relative permeability of the core, since inductance of a conductor is proportional to the permeability of the surrounding medium.[15] A high permeability material placed close to the transmission line conductors acts upon the external fringe field present, appreciably magnifying the inductance and providing a lower cutoff frequency. Power transferred from input to output is coupled directly through the dielectric medium separating the transmission line condcutors; thus a relatively small cross-section of ferrite material can operate in an unsaturated state at impressively high power levels. For the FET balanced mixer, ferrite core material with a permeability of 40 provides satisfactory operation from 50 to 250 MHz. Figure 11 also demonstrates that a lower transmission line impedance, Z_o, is to be preferred over a higher Z_o. Both 50-ohm and 100-ohm transmission lines are required for the mixer transformer; twisted pairs will provide satisfactory results. A characteristic impedance of 45 Ω is obtained from 3 turns-per-inch of Belden No. 24 AWG enamel wire, while 3½ turns-per-inch of No. 24 (7X32) Belden plastic covered wire provide Z_o = 100 ohms. Each core is wound with 2 inches of the proper twisted pair, with min/max lengths calculated from Pitzalis' data (Formulae 16, 17).

As with all broadband transformers, the coil has an inherent parasitic inductance which must be capacitor-compensated (C_2, C_4, Figure 2).[16] A trim capacitor is required at the two input terminals, and is adjusted *only once* to optimize the differential phase shift across the symmetrical balanced FETs. Phase match of the hybrid structure may be tracked to within ±2 degrees (about 180°) to 250 MHz. Effective resistance transformation is useful from 50 to 550 MHz (Figure 12) – but phase track beyond 250 MHz *may* show too much deterioration.



Toroid Coil Winding Data

Figure 11

Designing the IF Network

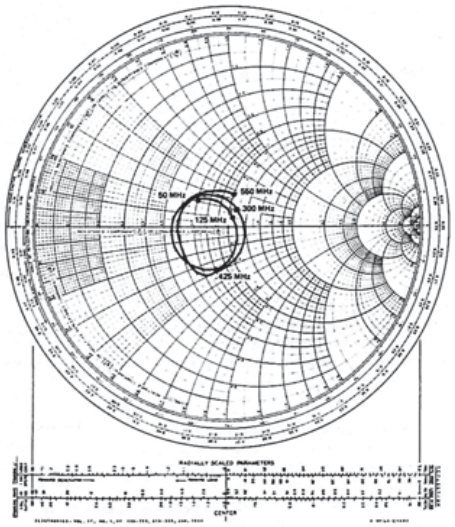
The IF network performs two important functions in the FET balanced mixer circuit. It provides for optimum match between the FETs and the IF amplifier, and it effectively bypasses the circuit RF components (signal and local oscillator).

In network design, it is essential that the RF and local oscillator signals be sufficiently isolated from the intermediate frequency signal to maintain rejection levels of at least 20 dB. If this isolation is not maintained, conversion gain and noise figure are degraded.

The simplest technique for design of the IF network is to use the well-known pi (π) match structure from each FET drain to a common balanced output transformer network.[17] This pi match technique is especially suitable for a narrow-band intermediate frequency output, serving three useful functions. First, it serves to achieve the proper drain load match between the FETs and the IF structure. Second, it provides the very necessary isolation of the intermediate frequency signal. And third, it serves as a simple filter to provide a monotonic decrease in impedance as frequency departs from the IF center frequency, f_o.[18, 19] This third function, shown in Figure 13, prevents the drain load impedance from skyrocketing out of control and giving rise to distortion products.

Selection of the dynamic drain impedance value in the IF network is a critical point in design of the structure. Intermodulation product distortion and crossmodulation will be

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50Ω – 200Ω Balun
Figure 12

both affected by the instantaneous peak-to-peak output voltage of the FETs, if the value of the dynamic drain impedance allows these signal peaks to enter either the pinch-off voltage or breakdown voltage regions of the transistors.(20) If the impedance is too high, the dynamic range of the mixer will be severely limited; if the impedance is too low, useful conversion gain will be sacrificed.

A first-order approximation to establish the proper load impedance may be obtained when

$$R_L = \frac{V_{DD} - 2\,V_{GS(off)}}{i_d} \qquad (18)$$

where

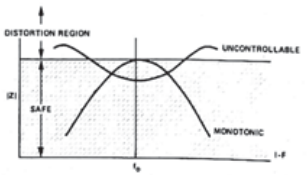
$$i_d = I_{DSS}\left[1 - \frac{v_{gs}}{V_{GS(off)}}\right]^2 \qquad (19)$$

and

$$v_{gs} = V_{GS} + V_1 \sin \omega_1 t \qquad (20)$$

For the U310 FET, the optimum drain load impedance is established at slightly less than 2000 ohms, with sufficient local oscillator drive and gate bias determined from the conversion transconductance curve in Figure 5.

The output IF coupling structure is an 800-ohm CT to 50-ohm trifilar-wound transformer (Relcom BT-9 or equivalent). The pi (π) match into this transformer provided a dynamic drain load impedance of 1700 ohms on each FET; excellent



Pi (π) Match Filter Function
Figure 13

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IM performance was obtained. Value of operating Q was established at 10 as the best compromise to insure that the tolerance of the pi match components would permit the IF output to peak within the allowable bandwidth at the associated IF amplifier. A Q of more than 10 would result in a greatly restricted bandwidth, while a Q of less than 10 would result in excessively high capacitance, excessively low inductance, and unsatisfactory filter performance.

Mixer Performance

Tests of the operational prototype FET balanced mixer demonstrated that the active mixer has several characteristics superior to those of passive mixer counterparts. These comparisons are made in Table IV (measurements of all three mixers were made under laboratory conditions).

Insertion loss measurements on the IF network amounted to 3 dB in the center of the passband, while insertion loss on the hybrid assembly measured 1.2 dB. The network exhibited a Q of 10. Gain and noise figures were measured over the full 50-250 MHz bandwidth, with a single-sideband noise figure ranging from 7.2 dB at 50 MHz to 8.6 dB at 250 MHz. Conversion gain was a flat +2.5 dB.

Two-tone third-order intermodulation is expressed in terms of the intercept point.(21) With two signals 300 kHz apart, the balanced mixer suppressed third-order products –89 dB with both signals at –10 dBm, representing an intercept point of +32 dBm.

Table IV

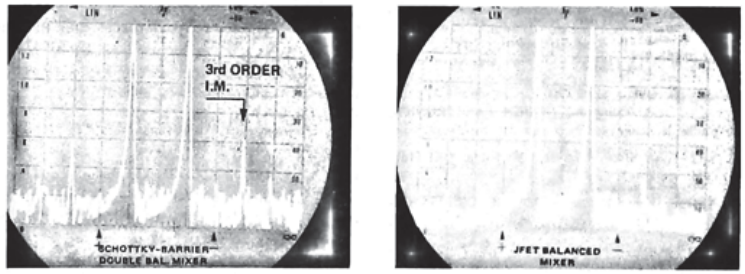
50-250 MHz Mixer Performance Comparison

Characteristic	JFET	Schottky	Bipolar
Intermodulation Intercept Point	+32 dBm	+28 dBm	+12 dBm†
Dynamic Range	100 dB	100 dB	80 dB†
Desensitization Level (the level for an unwanted signal when the desired signal first experiences compression)	+8.5 dBm	+3 dBm	+1 dBm†
Conversion Gain	+2.5 dB*	–6 dB	+18 dB
Single-sideband Noise Figure @ 50 MHz	7.2 dB	6.5 dB	6.0 dB

†Estimated *Conservative minimum

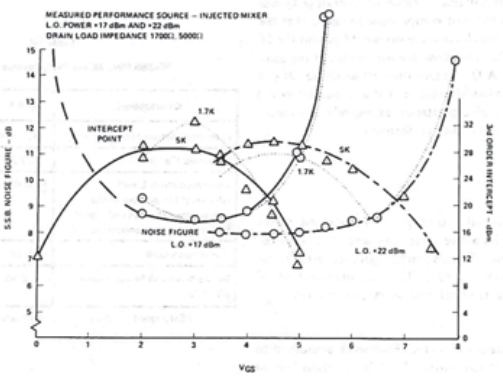
Figure 14 shows a comparison of third-order IM products emanating from both the JFET balanced mixer and a typical low-level double-balanced diode mixer, under similar operating conditions. Noise figure and intercept point are shown at various bias and local oscillator drive levels in Figure 15.

The performance of the active mixer is clearly superior to that of the diode mixers, contributing overall system gain in areas critical to telecommunications practice, and reducing associated amplifier requirements.



Comparison of 3rd Order IM Products
Figure 14

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Noise Figure and Intercept Point Performance
Figure 15

CONCLUSION

The reason for using the three-core bifilar transformer (Figure 11A) in this tutorial article stemmed from the relative analytical simplicity of such a design. An alternative transformer is the single-core trifilar-wound design. The definitions for wire lengths (Equations 16 and 17) are equally applicable to trifilar as they are for bifilar.

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(14) Op. cit., ECOM-2989, July 1968.

(15) Op. cit., ECOM 2989, p. 6.

(16) Op. cit., ECOM 2989, p. 7.

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APPLICATION NOTE

FETs As Voltage-Controlled Resistors

INTRODUCTION

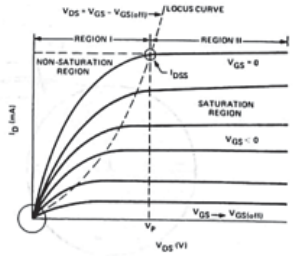
The Nature of VCRs

A voltage-controlled resistor (VCR) may be defined as a three-terminal variable resistor where the resistance value between two of the terminals is controlled by a voltage potential applied to the third.

A junction field-effect transistor (JFET) may be defined as a field-controlled majority carrier device where the conductance in the channel between the source and the drain is modulated by a transverse electric field. The field is controlled by a combination of gate-source bias voltage, V_{GS}, and the net drain-source voltage, V_{DS}.

Under certain operating conditions, the resistance of the drain-source channel is a function of the gate-source voltage alone and the JFET will behave as an almost pure ohmic resistor.(1) Maximum drain-source current, I_{DSS}, and minimum resistance, $r_{DS(on)}$, will exist when the gate-source voltage is equal to zero volts ($V_{GS} = 0$). If the gate voltage is increased (negatively for N-Channel JFETs and positively for P-Channel) the resistance will also increase. When the drain current is reduced to a point where the FET is no longer conductive, the maximum resistance is reached. The voltage at this point is referred to as the pinchoff or cutoff voltage and is symbolized by $V_{GS} = V_{GS(off)}$. Thus the device functions as a voltage-controlled resistor.

Figure 1 details typical operating characteristics of an N-Channel JFET. Most amplification or switching operations of FETs occur in the constant-current (saturated) region, shown as Region II. A close inspection of Region I (the unsaturated or pre-pinchoff area) reveals that the effective slope indicative of conductance across the channel from drain to source is different for each value of gate-source bias voltage.(2) The slope is relatively constant over a range of applied drain voltages, so long as the gate voltage is also constant and the drain voltage is low.



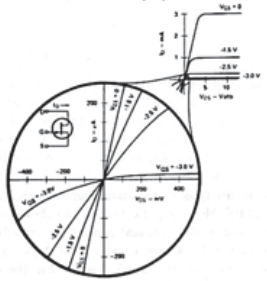
Typical N-Channel JFET Operating Characteristics
Figure 1

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Resistance Properties of FETs

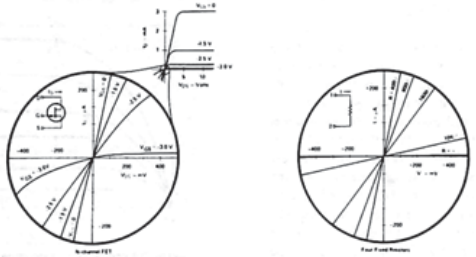
The unique resistance-controlling properties of FETs can be deduced from Figure 2, which is an expanded-scale plot of the encircled area in the lower left-hand corner of Figure 1. The output characteristics all pass through the origin, near which they become almost straight lines so that the incremental value of channel resistance, r_{ds}, is essentially the same as that of d.c. resistance, r_{DS}, and is a function of V_{GS}.(3)

Figure 2 shows extension of the operating characteristics into the third quadrant for a typical N-Channel JFET. While such devices are normally operated with a positive drain-source voltage, small negative values of V_{DS} are possible. This is because the gate-channel PN junction must be slightly forward-biased before any significant amount of gate current flows. The slope of the V_{GS} bias line is equal to $\Delta I_D/\Delta V_{DS} = 1/r_{DS}$. This value is controlled by the amount of voltage applied to the gate. Minimum r_{DS}, usually expressed as $r_{DS(on)}$, occurs at $V_{GS} = 0$ and is dictated by the geometry of the FET. A device with a channel of small cross-sectional area will exhibit a high $r_{DS(on)}$ and a low I_{DSS}. Thus a FET with high I_{DSS} should be chosen where design requirements indicate the need for a low $r_{DS(on)}$.



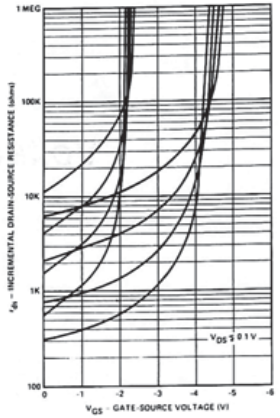
N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$
Figure 2

Figure 3 extends the r_{ds} characteristics of a FET to a comparison with the performance of 4 fixed resistors. Note the pronounced similarity between the two types of devices.



Comparison of FET and Resistor Characteristics
Figure 3

Typical r_{DS} curves for several Siliconix N-channel JFETs are plotted in Figure 4.(4) The graphs are useful in estimating r_{DS} values at any given value of V_{GS}. All quantities given in Figure 4 are for typical units, so some variation should be expected for the full range of production devices. It is therefor deisrable to convert Figure 4 to a normalized plot. This

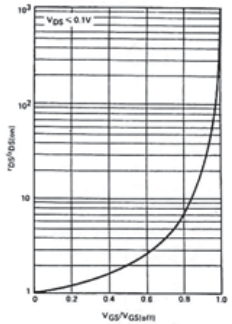


Incremental Drain-Source Resistance for Typical N-Channel FETs
Figure 4

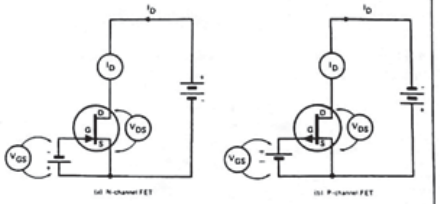
has been done in Figure 5. The resistance is normalized to its specific value at $V_{GS} = 0$ V. The dynamic range of r_{DS} is shown as greater than 100:1, although for best control of r_{DS} a range of 10:1 is normally used.

Siliconix offers a family of FETs specifically intended for use as voltage-controlled resistors. The devices are available in both N-Channel and P-Channel configurations (Figures 6A and 6B) and have $r_{DS(on)}$ values ranging from 20 Ω to 4,000 Ω (Figure 7).

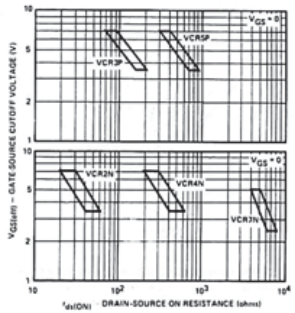
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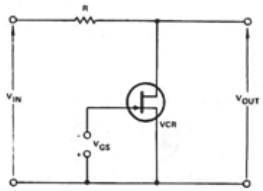
Normalized r_{ds} Data
Figure 5



Circuit Arrangement for Both an N and P Channel FET
Figure 6



$r_{ds(on)}$ (Drain-Source Resistance at $V_{DS} = V_{GS} = 0$)
Varies as an Inverse Function of $V_{GS(off)}$
Figure 7



Simple Attenuator Circuit
Figure 8

Applications for VCRs

The FET is ideal for use as a voltage-controlled resistor in applications requiring high reliability, minimum component size, and circuit simplicity. The FET VCR will conveniently replace numerous elements of conventional resistance control systems, such as servomotors, potentiometers, idler pulleys, and associated linkage. FET power consumption is minimal, packages are very small, and cost comparisons with conventional control schemes are most favorable.

A simple application of a FET VCR is shown in Figure 8, the circuit for a voltage divider attenuator.(5)

The output voltage is

$$v_{OUT} = \frac{V_{in}\, r_{DS}}{R + r_{DS}} \quad (1)$$

It is assumed that the output voltage is not so large as to push the VCR out of the linear resistance region, and that the r_{DS} is not shunted by the load.

The lowest value which v_{OUT} can assume is

$$v_{OUT(min)} = \frac{V_{in}\, r_{DS(on)}}{R + r_{DS(on)}} \quad (2)$$

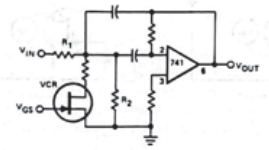
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The highest value is

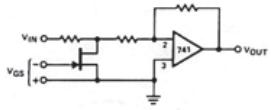
$$v_{OUT(max)} = v_{in} \qquad (3)$$

since r_{DS} can be extremeley large.

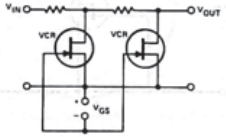
A number of other FET VCR applications are shown in Figures 9-16.



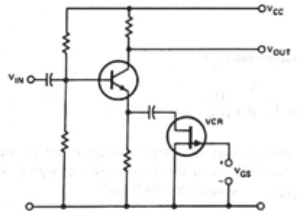
Voltage-Tuned Filter Octave Range with Lowest Frequency at JFET $V_{GS(off)}$ and Tuned by R_2. Upper Frequency is Controlled by R_1
Figure 9



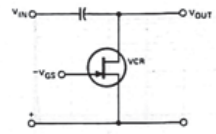
Electronic Gain Control
Figure 10



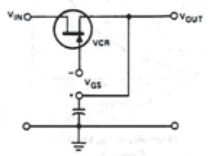
Cascaded VCR Attenuator
Figure 11



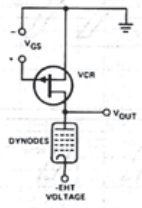
Wide Dynamic Range AGC Circuit. No Gain through FET with Distortion Proportional to Input Signal Level
Figure 12



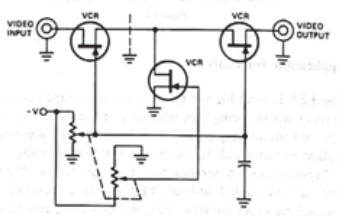
VCR Phase Advance Circuit
Figure 13



VCR Phase Retard Circuit
Figure 14



P-Channel VCR Photomultiplier Load. Required Low Photomultiplier Anode Current (Usually < 1 μA) Implies that VCR will Always Perform in Linear Region Near Origin
Figure 15

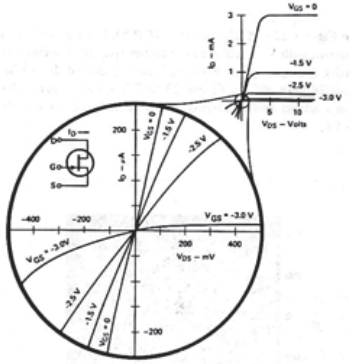


Voltage Controlled Variable Gain Amplifier. The Tee Attenuator Provides for Optimum Dynamic Linear Range Attenuation
Figure 16

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Signal Distortion: Causes

Figure 17A repeats the FET output characteristic curves of Figure 2, to show that the bias lines bend down as V_{DS} increases in a positive direction toward the pinch-off voltage of the FET. The bending of the bias lines results in a change in r_{DS}, and hence the distortion encountered in VCR circuits; note that the distortion occurs in both the first and third quadrants. Distortion results because the channel depletion layer increases as V_{DS} reduces the drain current, so that a pinch-off condition is reached when $V_{DS} = V_{GS} - V_{GS(off)}$. Figure 17B shows how the current has an opposite effect



N-Channel JFET Output Characteristic Enlarged Around $V_{DS} = 0$
Figure 17A

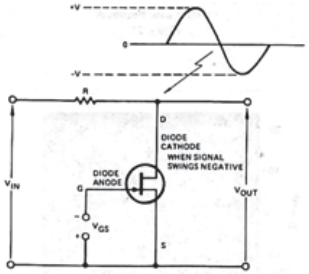


Figure 17B

in the third quadrant, rising negatively with an increasingly negative V_{DS}. This is due to the forward conduction of the gate-to-channel junction when the drain signal exceeds the negative gate bias voltage.

Reducing Signal Distortion

The majority of VCR applications require that signal distortion be kept to a minimum. Also, numerous applications require large signal handling capability. A simple feedback technique may be used to reduce distortion while permitting large signal handling capability; a small amount of drain signal is coupled to the gate through a resistor divider network, as shown in Figure 18.

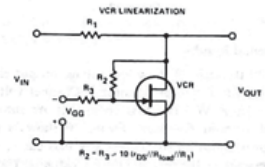


Figure 18

The application of a part of the positive drain signal to the gate causes the channel depletion layer to decrease, with a corresponding increase in drain current. Increasing the drain current for a given drain voltage tends to linearize the V_{GS} bias curves. On the negative half-cycle, a small negative voltage is coupled to the gate to reduce the amount of drain-gate forward bias. This in turn reduces the drain current and linearizes the bias lines. Now the channel resistance is dependent on the DC gate control voltage and not on the drain signal, unless the $V_{DS} = V_{GS} - V_{GS(off)}$ locus is approached. Resistors R_2 and R_3 in Figure 18 couple the drain signal to the gate; the resistor values are equal, so that symmetrical voltage-current characteristics are produced in both quadrants. The resistors must be sufficiently large to provide minimum loading to the circuit:

$$R_2 = R_3 \geq 10\,[R_1 \,||\, r_{ds}\,(max) \,||\, R_L] \qquad (4)$$

Typically, 470K Ω resistors will work well for most applications. R_1 is selected so that the ratio of $r_{DS(on)} \,||\, R_L$ to $[(r_{DS(on)} \,||\, R_L) + R_1]$ gives the desired output voltage, or:

$$e_o = e_i \frac{r_{DS(on)} \,||\, R_L}{(r_{DS(on)} \,||\, R_L) + R_1} \qquad (5)$$

The feedback technique used in Figure 18 requires that the gate control voltage, V_{GG}, be twice as large as V_{GS} in Figure 17B for the same r_{DS} value. Use of a floating supply between the resistor junction and the FET gate will overcome this problem. The circuit is shown in Figure 19, and allows the gate control voltage to be the same value as that voltage used without a feedback circuit, while preserving the advantages to be gained through the feedback technique.

Appendix A to this Application Note is an analytical approximation of VCR FET distortion characteristics, both calculated and measured.

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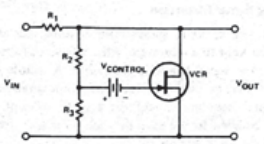


Figure 19

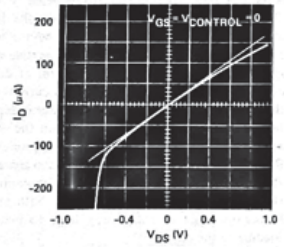
The forward-biased gate-drain PN junction may be seen at approximately −0.6 V, and bending of the bias curve is apparent in the third quadrant. The photo also demonstrates the comparison between a fixed resistor (the linear line superimposed on the bias curve) and the distortion apparent in the VCR without feedback compensation; the VCR signal is unusable with the indicated amount of distortion.

In Figure 21, the same VCR7N FET is shown operating with the addition of the feedback resistors. Distortion has been reduced to less than 0.5%, and the characteristics of the VCR are now closely comparable to those of a fixed resistor.

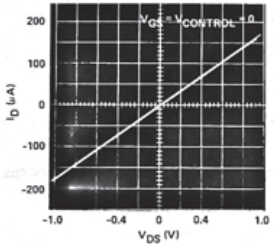
In Figures 22 and 23, the same VCR FET characteristics are shown, with V_{GS} adjusted for higher r_{DS}. No feedback network is employed in Figure 22, and measured distortion is greater than 8%. In Figure 23, the feedback resistors have been added and distortion has been reduced to less than 0.5%.

Experimental Results

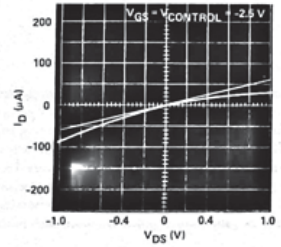
Figures 20 through 23 show low voltage output characteristic curves for a typical Siliconix N-Channel voltage-controlled resistor, VCR7N. Bias conditions are shown both with and without feedback. Figure 20 shows a two-volt peak-to-peak signal on the V_{GS} = 0 V bias curve, with the VCR operating in the first and third quadrants. The VCR is operated without feedback.



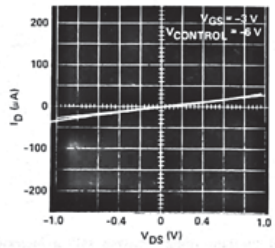
VCR7N with No Feedback
Figure 20



VCR7N with Feedback
Figure 21



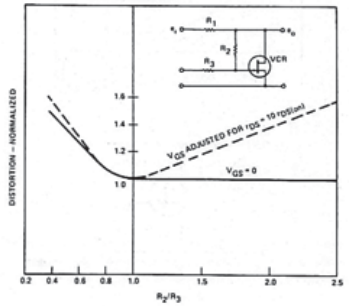
VCR7N with No Feedback
Figure 22



VCR7N with Feedback
Figure 23

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Some degree of non-linearity will be experienced in both the first and third quadrants as V_{GS} approaches the FET cut-off voltage. For this reason, it is important that the feedback resistors be of equal value so that the non-linearities likewise will be equal in both quadrants. Figure 24 shows a curve of distortion vs R_2/R_3, in both quadrants.



Distortion vs R_2/R_3
Figure 24

Distortion resulting from changes in temperature are also minimized by the feedback resistor technique. r_{DS} will change with temperature in an inverse manner to the behavior of FET drain current. Table I presents the result of VCR laboratory performance tests of distortion vs temperature. The VCR7N again was employed. Signal level was 2 V peak-to-peak.

Table I

Temperature (°C)	Without Feedback		With Feedback	
	r_{DS} = $r_{DS(on)}$	r_{DS} = 10 $r_{DS(on)}$	r_{DS} = $r_{DS(on)}$	r_{DS} = 10 $r_{DS(on)}$
+125	>12%	>6%	<0.5%	<0.5%
+ 25	>10%	>5%	<0.5%	<0.5%
− 55	3.9%	3.2%	<0.5%	<0.5%

SUMMARY

This Application Note has presented a brief description of the use of junction field-effect transistors as voltage-controlled resistors, including details of operation, characteristics, limitations, and applications. The VCR is capable of operation as a symmetrical resistor with no DC bias voltage in the signal loop, an ideal characteristic for many applications.

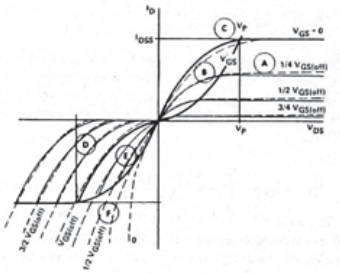
Where large signal-handling capability and minimum distortion are system requirements, the feedback neutralization technique for VCRs is an important tool in achieving either or both ends.

It has also been shown that FETs with high pinch-off voltage require larger drain-to-source voltages to produce drain current saturation. Therefore, FETs with high $V_{GS(off)}$ will have a larger dynamic range in terms of applied signal amplitude, while maintaining a linear resistance. It is advantageous to select FETs with high $V_{GS(off)}$ (compatible with the desired r_{DS} value) if large signal levels are to be encountered.

APPENDIX A — **From proceedings of the IEEE, October, 1968, pp. 1718-1719.**

Abstract — An analytical approximation of FET characteristics for positive and negative voltages is presented. The distortion in an application as a controlled attenuator is calculated, and a method of reducing distortion by a factor of more than 50 is described.

Controlled resistors are used in oscillators, controlled amplifiers, and attenuators.[6,7] The possible control range is much larger for field-effect transistors (FET) than for other elements with comparable time constants (e.g., diodes). The signal-to-noise ratio is considerably improved.



Comparison Between Mathematical Approximation of FET Characteristics (Solid Lines) and Measured Curves (Broken Lines) for a Typical N-Channel JFET
Figure 25

Figure 25 shows idealized and real FET characteristics. In region A (above pinch-off) I_D is independent of V_{DS}.[8]

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad (1)$$

Region B, where $V_{DS} < (V_{GS} - V_P)$, is the so-called triode region. (In the following discussion all the signs (+, −) will be valid for N-Channel FETs.) The characteristics can be

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approximated by a quadratic function, of which the maximum and a second point (the origin) are known. The approximation is

$$I_D = I_{DSS}\left[\left(1-\frac{V_{GS}}{V_P}\right)^2 - \left(1-\frac{V_{GS}-V_{DS}}{V_P}\right)^2\right]$$
$$= \frac{2I_{DSS}}{(V_P)^2}\ V_{DS}\left(V_{GS}-V_P-\frac{V_{DS}}{2}\right) \quad (2)$$

This is the same function that can be found by a simple analysis based on semiconductor theory. The less negative of the two voltages across the junction (V_{GS}, V_{GD}) controls the channel conductance. Under the condition that the FET is symmetrical (drain and source interchangeable), the following consideration is true. If V_{GD} were the controlling voltage and $V_{DS} < 0$, $I_D < 0$, then the characteristics would be the same as in the first quadrant:

$$-I_D = -\frac{2I_{DSS}}{V_P^2}\ V_{DS}\left(V_{GD}-V_P+\frac{V_{DS}}{2}\right) \quad (3)$$

Since the controlling voltage for both regions (B and E) is V_{GS},

$$V_{GD} = V_{GS} - V_{DS} \quad (4)$$

Substituting (4) into (3), we get (2); the same approximation can be used in B and E. The limits of region E where (2) is valid are $V_{GD} = 0$ and $V_{GD} = V_P$. The characteristics in region D can be found from (1) with the same consideration:

$$I_D = -I_{DSS}\left(1-\frac{V_{GS}-V_{DS}}{V_P}\right)^2 \quad (5)$$

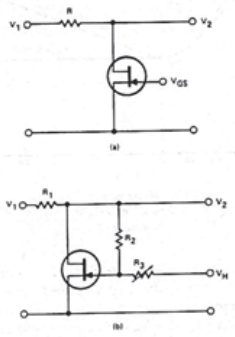
The mathematical approximation is compared with the measured characteristic in Figure 25. In the regions C and F the junction is forward biased. The characteristics are dependent on the internal resistance of the gate voltage source since gate current flows.

The FET as a controlled resistor works in region B and E. The higher the resistance, the more non-linear are the characteristics. For most applications this is undesirable. Based on the simple approximation (2), the relation between distortion, control range, and maximum to minimum attenuation will be described for a simple voltage divider [Figure 26(a)]. Most applications can be based on this simple example. The conductance in any point of region B or E is

$$G_{DS} = \frac{I_D}{V_{DS}} = -\frac{2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$$
$$-\frac{I_{DSS}}{(V_P)^2}\ V_{DS} = g_{DS} + \frac{g_{DSS}V_{DS}}{2V_P} \quad (6)$$

where g_{DS} is the differential conductance at the origin; when $V_{GS} = 0$, then $g_{DS} = g_{DSS}$. The attenuation for the circuit of Figure 26(a) is

$$\frac{V_2}{V_1} = \frac{1}{1+Rg_{DS}} = \left[\frac{1+Rg_{DS}}{+\dfrac{Rg_{DSS}V_1}{2V_P\left(1+Rg_{DS}+\dfrac{2Rg_{DS}V_1}{2V_P(1+Rg_{DS})}\right)}}\right]^{-1} \quad (7)$$



(a) Controlled JFET Attenuator. (b) Controlled Attenuator with "Feedback" Making Characteristics Linear and Symmetrical
Figure 26

To reduce (7) to a more tractable form, the following inequality is introduced:

$$\frac{V_1 Rg_{DSS}}{2V_P[1+Rg_{DS}]^2} \ll 1$$

so that (7) can now be approximated by the expansion

$$V_2 = \frac{V_1}{1+g_{DS}R}\left(1-\frac{Rg_{DS}V_1}{2V_P[1+Rg_{DS}]^2}+\ldots\right) \quad (8)$$

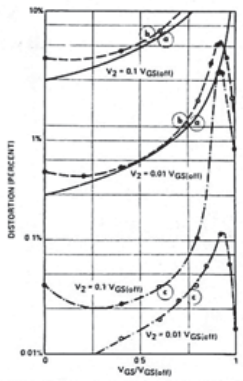
Only the second harmonic will be considered for the distortion since the third is much smaller. For small distortion ($d \ll 1$ and $Rg_{DSS} \gg 1$),

$$d = \frac{V_1 Rg_{DSS}}{4|V_P|[1+Rg_{DS}]^2} \quad (9)$$

If V_2 is held constant,

$$d = \frac{V_2 Rg_{DS}}{4|V_P|[1+Rg_{DS}]} \approx \frac{V_2}{4|V_P - V_{GS}|} \quad (10)$$

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Distortion as a Function of $V_{GS}/V_{GS(off)}$ for Two Different $V_2/V_{GS(off)}$. (a) Theoretical for Figure 26(a). (b) Measured with Circuit of Figure 26(a). (c) Measured with Circuit of Figure 26(b)
Figure 27

Figure 27 shows a comparison of measured and calculated distortion. If V_{GS} approaches V_P, the above restrictions are violated; the expression for the distortion can no longer be applied. If $V_{DS} < 0$, $V_{GS} = 0$, then the FET works in region F; the distortion will be higher than predicted. From (10) we get for a prescribed maximum distortion a maximum amplitude as a function of V_{GS}:

$$V_{2max} = 4d_{max}|V_P - V_{GS}| \quad (11)$$

For a given d_{max} and V_{2max} the ratio of minimum to maximum attenuation is

$$\frac{A_{min}}{A_{max}} = m = \frac{1+Rg_{DSS}}{1+Rg_{DSS}\dfrac{4d_{max}|V_P|}{V_{2max}}} \approx \frac{4d_{max}|V_P|}{V_{2max}} \quad (12)$$

valid only for $m > 1$. Note that the maximum distortion is reached only for minimum attenuation. Examples:

d_{max} = 10 percent $V_{2max} = 0.001\ V_P$ m = 400
d_{max} = 1 percent $V_{2max} = 0.01\ V_P$ m = 4

Although these relations are only first-order approximations, they give a good estimate of FET attenuator characteristics. The maximum amplitude is proportional to V_P. FETs with high V_P are desirable for attenuator applications. Unfortunately, the majority of commercially available FETs are made with low V_P for use in amplifiers.

There are several means of reducing distortion. By connecting two identical FETs in antiparallel or antiseries, nonlinearities can be cancelled out to a certain extent. A better linearization is possible by using one FET with "feedback". It has been shown above that the characteristics would be symmetrical if V_{GD} were the control voltage in the third quadrant. By adding 0.5 V_{DS} to the control voltage, the two voltage V_{GS} and V_{GD} interchange when V_{DS} changes sign:

$$V_{GS} = V_H + 0.5\ V_{DS}$$
$$V_{GD} = V_H - 0.5\ V_{DS} \quad (13)$$

then (13) used in (2) gives

$$I_D = \frac{2I_{DSS}}{V_P^2}\ V_{DS}(V_H - V_P) \quad (14)$$

The resulting characteristic is linear and symmetrical in B and E. The improvement in distortion performance can be seen in Figure 27. A distortion of 12 percent for $V_2 = 0.1\ V_P$ at $V_{GS} = 0.8\ V_P$ is reduced through linearization to 0.1 percent. Figure 26(b) shows a possible circuit. The frequency range of the controlled signal must be much higher than that of the controlling signal V_H to keep the direct interference of V_H on V_2 small. R_3 is set for minimum distortion. If V_2 and V_H are in the same frequency range, a high impedance amplifier must be used. V_2 is at the input; the output is connected to the FET gate. The amplification is approximately 0.5 (adjustable). The control voltage is introduced through a second input so that no direct interference with V_2 occurs.

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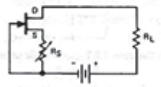
Siliconix

DESIGN IDEA

The FET Constant Current Source

INTRODUCTION

The combination of low associated operating voltage and high output impedance make the FET attractive as a constant current source. An adjustable current source may be built with a FET, a variable resistor and a small battery, Figure 1. For good thermal stability, the FET should be biased near the zero T.C. point.[1]



Field-Effect Transistor Current Source
Figure 1

Whenever the FET is operated in the saturated region, its output conductance is very low. This occurs whenever the drain-source voltage V_{DS} is significantly greater than the cut-off voltage $V_{GS(off)}$. The FET may be biased to operate as a constant current source at any current below its saturation current I_{DSS}.

For a given device where I_{DSS} and $V_{GS(off)}$ are known, the approximate V_{GS} required for a given I_D is

$$V_{GS} = V_{GS(off)} \left[1 - \left(\frac{I_D}{I_{DSS}}\right)^{1/k}\right] \quad (1)$$

where k can vary from 1.7 to 2.0, depending upon device geometry. The series resistor R_S required between source and gate is

$$R_S = \frac{V_{GS}}{I_D} \quad (2)$$

A change in supply voltage, or change in load impedance, will change I_D by only a small factor because of the low output conductance g_{oss}.

$$\Delta I_D = \Delta V_{DS} g_{oss} \quad (3)$$

The value of g_{oss} is an important consideration in the accuracy of a constant current source. As g_{oss} may range from less than 1 μmho to more than 50 μmho according to the FET type, the dynamic impedance can be greater than 1 megohm to less than 20K. This corresponds to a current stability range of 1 μA to 50 μA per volt. The value of g_{oss} depends also on the operating point, being highest at I_{DSS} and at low V_{DS}. Output conductance g_{oss} decreases approximately linearly with I_D, becoming less as the FET is biased toward cut-off. The relationship is

$$\frac{I_D}{I_{DSS}} = \frac{g_{oss}}{g'_{oss}} \quad (4)$$

where

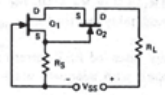
$$g_{oss} = g'_{oss} \quad (5)$$

when

$$V_{GS} = 0 \quad (6)$$

So as $V_{GS} \rightarrow V_{GS(off)}$, $g_{oss} \rightarrow$ zero. For best regulation, I_D must be considerably less than I_{DSS}.

It is possible to achieve much lower g_{oss} per unit I_D by cascading two FETs as shown in Figure 2.



Cascade FET Current Source
Figure 2

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Now, I_D is regulated by Q_1 and $V_{DS1} = -V_{GS2}$. The d-c value of I_D is controlled by R_S and Q_1. However, Q_1 and Q_2 both affect current stability. The circuit output conductance is derived as follows:

Figure 2 is redrawn in Figure 3 for the condition $V_{GS1} = 0$.

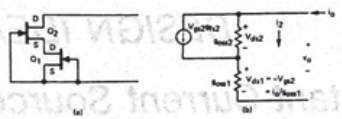


Figure 3

$$i_o = i_2 + v_{gs2}g_{fs2} = v_{ds2}g_{oss2} - i_o\frac{g_{fs2}}{g_{oss1}} \quad (7)$$

$$i_o = \frac{v_{ds2}g_{oss2}g_{oss1}}{g_{oss1} + g_{fs2}} \quad (8)$$

$$v_o = v_{ds1} + v_{ds2} = v_{ds2} + \frac{i_o}{g_{oss1}} \quad (9)$$

$$v_o = v_{ds2}\frac{g_{oss1} + g_{oss2} + g_{fs2}}{g_{oss1} + g_{fs2}} \quad (10)$$

$$g_o = \frac{i_o}{v_o} = \frac{g_{oss1}g_{oss2}}{g_{oss1} + g_{oss2} + g_{fs2}} \quad (11)$$

If $g_{oss1} = g_{oss2}$ (12)

$$g_o = \frac{g_{oss}}{2 + g_{fs}/g_{oss}} \quad (13)$$

When

$R_S \neq 0$ as in Figure 2 (14)

$$g_o = \frac{g_{oss}^2}{2g_{oss} + g_{fs} + R_S(g_{fs}^2 + g_{oss}g_{fs} + g_{oss}^2)} \quad (15)$$

$$\approx \frac{g_{oss}^2}{g_{fs}(1 + R_S g_{fs})} \quad (16)$$

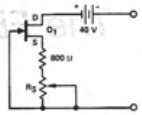
In either case ($R_S = 0$ or $R_S \neq 0$), the circuit output conductance is considerably less than the g_{oss} of a single FET.

In designing any cascaded FET current source, both FETs must be operated with adequate drain-gate voltage V_{DG}. That is,

$V_{DG} > V_{GS(off)}$, preferably $V_{DG} > 2\,V_{GS(off)}$ (17)

If $V_{DG} < 2\,V_{GS(off)}$, the g_{oss} will be significantly increased, and circuit g_o will deteriorate. For example: A 2N4340 has typical $g_{oss} = 4$ μmho at $V_{DS} = -20$ V and $V_{GS} = 0$. At $V_{DS} \approx -V_{GS(off)} = 2$ V, $g_{oss} \approx 100$ μmho.

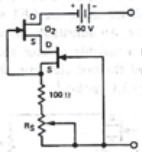
The best FETs for current sources are those having long gates and consequently very low g_{oss}. The Siliconix 2N4869 exhibits typical $g_{oss} = 1$ μmho at $V_{DS} = 20$ V. A single 2N4869 in the circuit of Figure 4 will yield a current source adjustable from 5 μA to 1 mA with internal impedance greater than 2 megohms.



R_S = 1MΩ, 2W

Adjustable Current Source
Figure 4

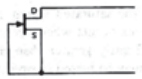
The cascade circuit of Figure 5 provides a current adjustable from 2 μA to 1 mA with internal resistance greater than 10 megohms.



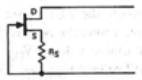
Q_1 = 2N4340
Q_2 = 2N4341
R_S = 1MΩ, 2W

Cascade FET Current Source
Figure 5

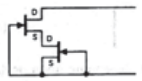
For each circuit discussed, g_{oss} is represented by the following equations:



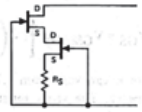
$g_o = g_{oss}$



$$g_o \approx \frac{g_{oss}}{1 + R_S g_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}}$$



$$g_o \approx \frac{g_{oss}^2}{g_{fs}(1 + R_S g_{fs})}$$

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DESIGN IDEA

Wideband UHF Amplifier with High-Performance FETs

Ed Oxner

INTRODUCTION

A new freedom in UHF amplifier design is possible with high-performance "Super FETs" such as the Siliconix U310 Junction FET. Typical advantages include a closely-matched 75 ohm input for extremely low return loss in cable systems, and high spurious response rejection with the 3rd order IM intercept measured at +29 dB.(1)

Additionally, the high common-gate forward transconductance of the U310 (20,000 μmho maximum) makes it possible to design an amplifier with wide bandwidth and good gain, since the figure of merit (g_m/C) of the FET is 2.35 x 10^9 typical – higher than any other known UHF Junction FET.

The amplifier circuit in Figure 1 is designed for 225 MHz center frequency, 1 dB bandwidth of 50 MHz, low input VSWR in a 75-ohm system, and 24 dB gain. Three stages of U310 FETs are used, in a straight forward design.

Typical parameters are taken from the U310 data sheet:

Forward Transconductance		14 mmhos
Input Admittance at 225 MHz	g_{igs}	13 mmhos
	b_{igs}	4 mmhos
Output Admittance at 225 MHz	g_{ogs}	0.27 mmhos
	b_{ogs}	2.6 mmhos

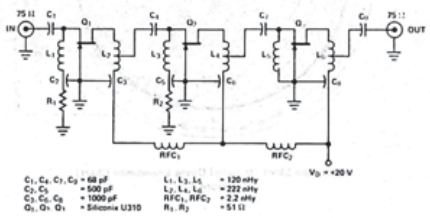


Figure 1

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Input match is simplified because the FET input (real) impedance is nearly 77 ohms. A coupling capacitor is used in the amplifier, rather than a tuned circuit, and thus the values may be determined:

$$R_s\sqrt{\frac{R_{ig}}{R_s}-1} = X_s = 75\sqrt{\frac{77}{75}-1} = 11.85\ \Omega$$

$$C_s = \frac{1}{\omega X_s} \approx 68\ pF$$

$$X_P = \frac{R_s R_p}{X_s} = \frac{75 \times 77}{11.85} = 488\ \Omega$$

$$C_P = 1.47\ pF$$

$$C_T = 4.4\ pF\ (C_T = C_P + C_{igs})$$

$$L_s = \frac{1}{\omega^2 C_T} = 120\ nHy$$

Figure 2 shows that the measured input VSWR in the 75-ohm system indicated an available bandwidth considerably greater than that required for the amplifier design criteria.

Three cascaded synchronous single-tuned stages are used to achieve the desired gain, and thus stage bandwidth and Q are determined:[2]

$$\frac{B/W}{f} = \frac{1}{Q}\sqrt{\left(\frac{E_o}{E}\right)^2 - 1}$$

where:

$$\frac{\text{Bandwidth of 3 Stages}}{\text{Bandwidth of 1 Stage}}^{(3)} = \sqrt{2^{1/3} - 1}$$

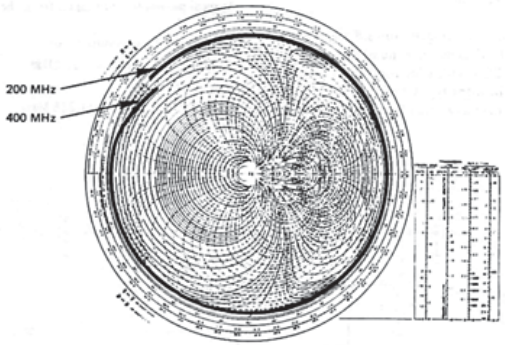
and

$$\left(\frac{E_o}{E}\right) = 1.122\ (1\ dB)$$

giving

$$B/W\ (1\ dB) = 98\ MHz$$

$$Q = 1.15$$



Blanchard Chart (Inverted Circle Impedance Chart)
Figure 2

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With a FET output impedance of 3700 ohms shunted by approximately 2.5 pF (with 0.5 pF allowed for stray capacitance), the total parallel resistance necessary to obtain the desired bandwidth is:

$$Q = \omega C R_t$$

$$R_t = \frac{1.15}{1.415 \times 10^9 \times 2.5 \times 10^{-12}} = 330\ \Omega$$

The tank circuit impedance appearing in shunt with the FET, is therefore calculated to be about 365 ohms. From this, the inductance is:

$$L = \frac{R}{\omega Q} = \frac{365}{\omega 1.15} = 222\ nHy$$

with a turns ratio of 2.3:1 to match to 75 ohms. Since each stage is designed for 75 ohm input and output, three cascaded stages complete the amplifier design.

The computed voltage gain per stage is approximately $g_{fs}\ R_{t/n}$ or 2.22 (7 dB). Measured gain for all three stages is 24 dB. The U310 FET in the final stage operates at I_{DSS}, and thus accounts for the higher measured gain. The gain/bandwidth response of the amplifier is shown in Figure 3.

The 3rd order spurious intercept point is plotted graphically in Figure 4.[4] The importance of a high intercept point becomes apparent in a crowded high-level area of the spectrum where signal purity is of utmost priority.

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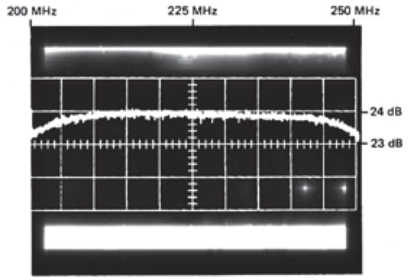


Figure 3

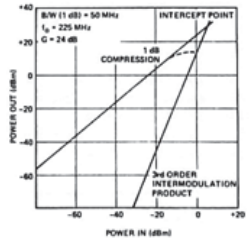


Figure 4

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DESIGN IDEA

High-Performance FETs In Low-Noise VHF Oscillators

Ed Oxner

Most communications receivers are limited in their dynamic range because of saturation in the early stages of RF amplifiers or mixers. However, some receiver designs are available which overcome this limitation by using parametric amplifiers and converters to achieve spectacular increases in dynamic range. There still remain certain limitations in dynamic range which cannot be remedied by parametric devices. In these cases, the problem lies in the heterodyning of noise sidebands which appear on the receiver local oscillator, entering the passband through strong interfering signals.

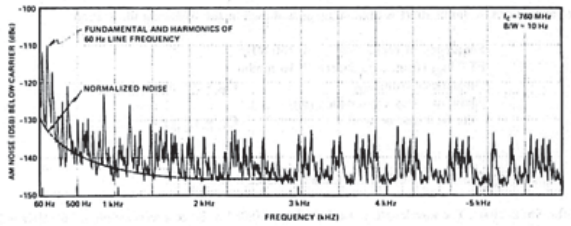
Common Types of Noise

Although noise is often difficult to characterize because of its random or nondeterministic nature, it is possible to differentiate various forms of noise through an understanding of the Gaussian distribution of noise about an RF carrier. Briefly stated, the three major forms of noise are (1) low-frequency noise (1/f); (2) thermal noise (4kTRB); and "shot" noise (i_n). Further, these types of noise can be identified from their relationship to the main RF carrier. For example, low-frequency noise predominates very close to the carrier, and falls to insignificant levels when it is displaced more than 250 Hz from the carrier. Low-frequency noise is associated with surface contamination and other irregularities, such as gate current leakage.

Thermal noise plays the predominant role in the region from the 1/f decay point to approximately 20 kHz from the carrier, and is commonly associated with equivalent resistance where the rms value of noise voltage of the Thevenin generator becomes the classic $(4kTBR)^{1/2}$. Noise appearing beyond the 20 kHz is known as Shot noise, and is directly attributable to noise current. Because of the typically uniform distribution of shot noise it is also referred to as "white noise."

Origins of Oscillator AM Noise

Although an oscillator tends to produce a wave that is nearly sinusoidal, there are other fluctuations present. When the energy in the frequency domain close to the carrier is observed on a spectrum analyzer, noise appears as a modulation phenomenon. This observation would be greatly enhanced if the noise contribution was coherent and consisted of discrete sideband frequencies. Without a doubt, the major component of AM noise is the contribution of low-frequency noise (1/f). Both thermal and shot noise are relatively insignificant segments of AM noise when compared to 1/f. A graph of AM noise vs frequency removed is shown in Figure 1.



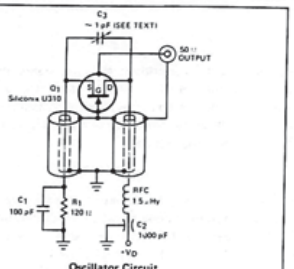
AM Noise vs Frequency Removed from the Carrier
Figure 1

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Design of a VHF Oscillator

The important design considerations for best oscillator performance include using a FET with high forward transconductance, maintaining the gate at ground potential, and keeping a high unloaded tank Q. The high transconductance is necessary to reduce the effective noise resistance. The grounded gate reduces the noise voltage contributions to those of the gate leakage current and the series gate resistance. The high tank circuit Q serves as an effective filter for the sideband noise energy.

The oscillator design is somewhat extraordinary for a circuit employing a FET. The FET chosen was the Siliconix U310, which has a forward transconductance value higher than 18 mmho at zero bias ($V_{GS} = 0$). The oscillator basically consists of two coaxial resonators, one for the FET source and the other for the drain. Oscillation is established by capacity coupling between the two resonators; output coupling is derived from the magnetic coupling which exists at the open ends of the resonators. Optimum resonator Q is achieved by designing the coaxial resonators for a characteristic impedance of 75 ohms. The oscillator circuit is shown in Figure 2, and construction details are shown in Figure 3.



Oscillator Circuit
Figure 2



Oscillator Construction Details
Figure 3

The technique to establish the proper resonator length for the desired frequency is somewhat tricky, and requires a first-order approximation of the anticipated capacitive fringing which derives from both the FET and the feedback network. A short circuited coaxial transmission line is theoretically resonant at a quarter-wave length of the resonating frequency, except for the effects of fringe field capacitance. At resonance

$$X_L = X_C \tag{1}$$

If the fringe capacitance is known, X_C can be calculated as

$$X_C = \frac{1}{\omega C} \tag{2}$$

From this, the resonator length can be determined as

$$X_C = \tan \beta \ell \tag{3}$$

In making these calculations, a Smith chart is invaluable, as is shown in the following illustration:

Frequency of oscillation	= 760 MHz
FET b_{igs} (from data sheet)	= 16 mmho
Capacitance from b_{igs}	C_{gs} = 3.4 pF
Allow for stray capacitance and the feedback network	C_s = 1.5 pF
	4.9 pF

Thus X_C = j 0.57 (normalized to 75 Ω)

Locate 0.57 on the Smith chart. The wavelength toward the load = 0.081 λ. Since a wavelength at 760 MHz is 39.5 cm., then the resonator cavity length is simply

$$39.5 \times 0.081 = 3.20 \text{ cm (1.26 inches)} \tag{4}$$

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In the completed FET coaxial oscillator circuit, the output coupling loop consists of a single turn made fast to the cavity by the BNC flange and the FET itself. Although the feedback network appears somewhat crude, it can be replaced by a small trimmer capacitor for similar operation.

Conclusions

Measured performance of the oscillator is shown in Table IA; AM noise measurements in a 10 Hz bandwidth are shown in Table IB.

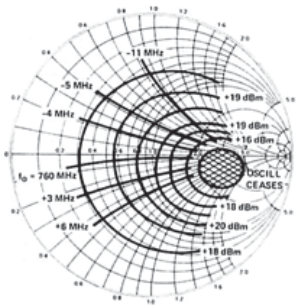
TABLE IA
Oscillator Measured Performance @ 25°C

V_{DD}(V)	+10	+15	+20	+25
I_D (mA)	15	16.2	18.2	21
P_{out} (dBm)	+6.6	+15.2	+18.3	+20
Frequency (MHz)	725	742.7	754.7	762.9

TABLE IB
AM Noise Measurement

Frequency Displaced From Carrier	dBc
50 Hz	-130
500 Hz	-139
1 kHz	-143.5
5 kHz	-146

The Reike diagram shown in Figure 4 makes possible the accurate prediction of expected power output and operating frequency with the oscillator feeding directly into a mismatched load. Expansion of the Reike diagram to show frequency vs transmission line length (in degrees) will allow prediction of the long-line effect on oscillator stability.



Reike Diagram
Figure 4

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TECHNICAL ARTICLE

FET Biasing

James Sherwin

INTRODUCTION

Engineers often design FET amplifiers that are unnecessarily sensitive to device characteristics because they may not be familiar with proper biasing methods.

One way to obtain consistent circuit performance in spite of wide device variations is to use a combination of constant-voltage and self biasing. The combined circuit configuration turns out to be the same as that generally used with bipolar transistors, but its operation and design are quite different.

Three Basic Circuits

Let's examine three basic common-source circuits that can be used to establish a FET's operating point (Q-point) and then see how two of them can be combined to provide greatly improved performance. The three basic biasing schemes are:

- Constant-voltage bias, which is most useful for rf and video amplifiers employing small dc drain resistors.
- Constant-current bias, which is best suited to low-drift dc amplifier applications such as source followers and source-coupled differential pairs.
- Self bias (also called source bias or automatic bias), which is a somewhat universal scheme, particularly valuable for ac amplifiers.

The Q-point established by the intersection of the load line and the V_{GS} = −0.4 V output characteristic of Figure 1 provides a convenient starting point for the circuit comparison. The load line shows that a drain supply voltage, V_{DD}, of 30 V and a drain resistance, R_D, of 39K Ω are being used.

The quiescent drain-to-source voltage, V_{DSQ}, is 15 V, allowing large signal excursions at the drain. Maximum input signal variations of ±0.2 V will produce output voltage swings of ±7.0 V – a voltage gain of 35.

Reprinted From ELECTRONIC DESIGN, May 24, 1970, June 7, 1970.

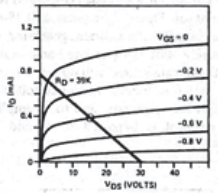


Figure 1. A large dynamic range is provided by the operating point at V_{DSQ} = 15 V, I_{DQ} = 0.39 mA and V_{GSQ} = −0.4 V. The output characteristics are for a typical 2N4339.

The constant-voltage bias circuit (Figure 2) is analyzed by superimposing a line for V_{GG} = constant on the transfer characteristic of the FET.

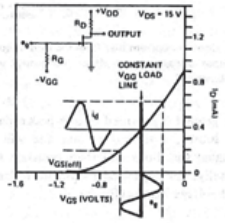


Figure 2. Constant-voltage bias is maintained by the V_{GG} supply as shown on this typical 2N4339 transfer curve. Input signal e_g moves the load line horizontally.

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The transfer characteristic is a plot of I_D vs V_{GS} for constant V_{DS}. Since the curve doesn't change much with changes in V_{DS}, it is quite useful in establishing operating bias points. In fact, it is probably more useful than the output characteristics because its curvature clearly warns of the distortion to be expected with large input signals. Furthermore, when a bias load line is superimposed, allowable signal excursions become evident and input voltage, gate-source signal voltage, and output signal current calculations may be made graphically.

The heavy vertical line at $V_{GS} = -0.4$ V establishes the Q-point of Figure 1. No voltage is dropped across resistor R_G because the gate current is essentially zero. R_G serves mainly to isolate the input signal from the V_{GG} supply.

Excursions of the input signal, e_g, combine in series with V_{GS} so that they add algebraically to the fixed value of −0.4 V. The effect of signal variation is to instantaneously shift the bias line horizontally without changing its slope. The shifting bias line then develops the output signal current as shown in Figure 2.

The constant-current bias approach (Figure 3) for establishing the Q-point of Figure 1 requires a 0.39-mA current source. For an ideal constant-current generator, input signal excursions merely shift the bias line horizontally and produce no resultant gate-source voltage excursion. This bias technique is therefore limited to source followers, source-coupled differential amplifiers, and to ac amplifiers where the source terminal is bypassed to ground at the signal frequency.

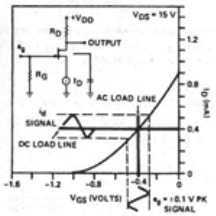


Figure 3. Constant-current bias fixes the output voltage for any R_D. Hence, input signals cannot affect the output unless the current source is bypassed.

If an ac ground is provided by a bypass capacitor across the current source, a vertical ac bias line will be established. Input signal variations will then translate the ac bias line horizontally, and signal development will proceed as with constant-voltage biasing (Figure 3).

Should the bypass capacitor not provide a sufficiently low reactance at the signal frequency, the ac bias line will not be vertical. It will still intersect the transfer curve at the Q-point but with a slope equal to $-(1/X_C) = -\omega C$ (Figure 4).

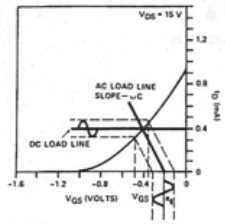


Figure 4. Partial bypassing of the current source (Figure 3) lowers the circuit gain by tilting the ac load line from the vertical. The capacitor drop subtracts from e_g.

This will lower the gain of the amplifier because of signal degeneration at the source. The input signal, e_g, is reduced by the drop across the capacitor:

$$v_{gs} = e_g - v_S = e_g - i_S X_C \qquad (1)$$

It is clear from Figure 4 that the input signal only shifts the operating point by an amount equal to V_{gs}, the effective input signal. As the signal frequency is decreased, the slope of the ac bias line decreases, causing the effective input signal to approach zero.

Self Bias Needs No Extra Supply

The self-bias circuit (Figure 5) establishes the Q-point by applying the voltage dropped across the source resistor, R_S, to the gate. Since no voltage is dropped across R_S when $I_D = 0$, the self-bias load line passes through the origin. Its slope is given by $-1/R_S$. Therefore, the desired Q-point is established by setting $-1/R_S = I_{DQ}/V_{GSQ}$.

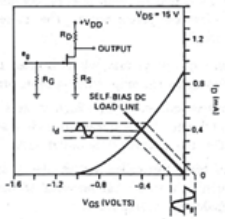


Figure 5. The self-bias load line passes through the origin with a slope $-1/R_S$. Bypassing R_S will steepen the slope and increase the gain of the circuit.

Signal development is the same as in the case of the partially bypassed constant-current scheme except that the load line is a dc bias line. Signal degeneration is described by Equation 1 with X_C replaced by R_S. The ac gain of the circuit can be increased by shunting R_S with a bypass capacitor, as in the constant-current case. The ac load line then passes through the Q-point with a slope $-(1/Z_S) = -(\omega C + 1/R_S)$.

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The circuit is biased automatically at the desired Q-point, requires no extra power supply and provides a degree of current stabilization not possible with constant-voltage biasing.

A fourth biasing method, combining the advantages of constant-current biasing and self biasing, is obtained by combining the constant-voltage circuit with the self-bias circuit (Figure 6). A principal advantage of this configuration is that an approximation may be made to constant-current bias without any additional power supply. The bias load line may be drawn through the selected Q-point and given any desired slope by properly choosing V_{GG}. (The bias line intercepts the V_{GS} axis at V_{GG}.) The larger V_{GG} is made, the larger R_S will be and the better will be the approximation to constant-current biasing.

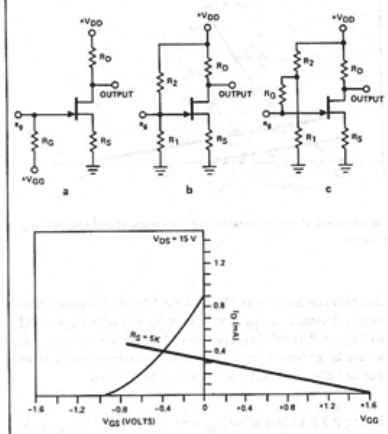


Figure 6. All three combination-bias circuits are equivalent. They add constant-voltage biasing to the self-bias circuit to establish a reasonably flat load line without sacrificing dynamic range.

All three circuits in Figure 6 are equivalent. Circuit 6(a) requires an extra power supply. The need for an additional supply is avoided in 6(b) by deriving V_{GG} from the drain supply. R_1 and R_2 are simply a voltage divider. To maintain the high input impedance of the FET, R_1 and R_2 must both be very large.

Very large resistors cannot always be found in the exact ratio needed to derive the desired V_{GG} in every circuit application. Circuit 6(c) overcomes this problem by placing a large R_G between the center point of the divider and the gate. This allows R_1 and R_2 to be small, without lowering the input impedance.

One point of caution worth remembering is that as V_{GG} is increased, V_S increases, and V_{DS} decreases. Therefore with low V_{DD}, there may be a significant decrease in the allowable output voltage swing.

Biasing for Device Variations

The value of the combination-bias technique becomes apparent when one considers the normal production spread of device characteristics. The problem is illustrated in Figure 7

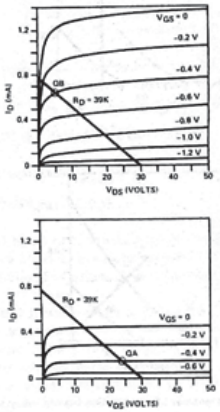


Figure 7. The wide variations in device performance shown by this pair of output characteristics make clear the disadvantages of constant-voltage biasing.

where two limiting sets of output characteristics, representing the actual min-max spread of the Siliconix 2N4339, are presented. Limiting characteristics like these are not normally available. Even if they were, however, they'd be of little help in establishing operating points suitable for all devices with output characteristics lying between the two extremes. The problem is much more easily approached by using the set of limiting transfer characteristics of Figure 8. (See next page.)

Attempting to establish suitable constant-voltage bias conditions for a production spread of devices is practical only for circuits with very small values of dc drain resistance – for example, circuits with inductive loads. As the constant-voltage bias plot of Figure 8 reveals, constant gate bias causes a significant difference in operating I_{DQ} for the extreme limit devices. At $V_{GS} = -0.4$ V, the range of I_{DQ} is 0.13 to 0.69 mA, and V_{DSQ} for a given R_D will vary greatly for most resistance-loaded circuits. For the example of Figure 1, with $R_D = 39\text{K}\ \Omega$ and $V_{DD} = 30$ V, V_{DSQ} varies from near saturation (5 V) to 25 V.

An apparently excellent method of biasing is the constant-current method of Figure 3. Biasing in this manner fixes the operating drain current for all devices and sets V_{DSQ} to $V_{DD} - I_{DQ}R_L$ for any device in the production spread. V_{GS} automatically finds a value to set the appropriate I_{DQ} = constant for all devices. For the constant-current bias plot of Figure 8, with $I_{DQ} = 0.39$ mA, V_{GS} would range from −0.11 to −0.67 V.

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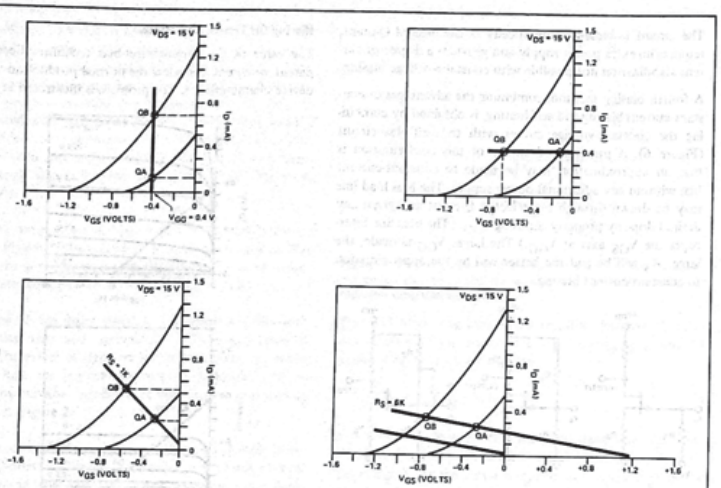


Figure 8. The advantages of combination biasing, when one is working with a spread of device characteristics, are made obvious by plotting the load lines for the various types of biasing on a pair of limiting transfer curves.

Output characteristics are not needed as long as I_{DQ} is chosen to be below the minimum I_{DSS}. With R_D = 39K Ω and V_{DD} = 30 V, V_{DSQ} is 14.8 V for all devices.

The disadvantages of the constant-current method are that it allows no signal to be developed unless the current source is bypassed and, as we shall see, it lacks the flexibility to provide constant gain despite variations in the forward transconductance, g_{fs}, of the devices.

The self-bias scheme is a reasonable choice for single-ended dc amplifiers and for ac amplifiers. In unbypassed or dc circuits, some compromise must be made between the gain loss due to current feedback degeneration and the advantage of current stabilization achieved with high R_S.

An appropriate choice of I_{DQ} limits can be made by using the pair of limiting transfer curves. For example, for R_S = 1K Ω, the load line shown on the self-bias curve of Figure 8 is established. The maximum I_D is 0.52 mA, and the minimum I_D is 0.24 mA. The operating range of V_{DSQ} may be calculated for any value of V_{DD} and R_D. Clearly, for R_D = 39K Ω, the maximum-limit device (device B) would operate with V_{DSQ} = 9.8 V and the minimum-limit device (device A) would operate with V_{DSQ} = 20.6 V. This results in fairly satisfactory operation for all devices. However, such a variation in I_{DQ} imposes severe limitations on the circuit design.

A better approach is illustrated by the combination-bias curve of Figure 8 with V_{GG} = 1.2 V. The range of I_{DQ} for this bias condition is 0.25 mA to 0.32 mA. A similar minimum difference in I_{DQ} could be achieved with R_S = 6K Ω and V_{GG} = 0, (a self-bias condition) but the operating points would be pushed toward the toe of the transfer characteristics and allowable signal input would be reduced.

The upper load line allows v_{gs} = ±1.8 V (limited by I_{DSSA}), while the lower line allows a v_{gs} of only ±0.7 V (limited by $V_{GS(off)A}$). (The subscript letters A and B refer to the minimum and maximum devices, respectively.) The combination circuit allows almost ideal operation over the full production spread of devices. Even with R_D = 62K Ω, the V_{DSQ} would range only between 10 and 15 V.

For this circuit, R_D should be chosen to allow the largest output signal swing for I_{DQ} midway between the two extremes of 0.25 and 0.32 mA; namely 0.285 mA. Setting the voltage drop across R_D at one-half of (V_{DD} – $2V_{GS(off)typ}$) or 14 V, yields R_D = (14 V/0.285 mA) = 49K Ω.

It is helpful, in any design, to know the effect of temperature variations on the transfer curves and transconductance characteristics. Ideally, minimum and maximum transfer characteristics would be plotted at three temperatures: above, below, and at room temperature. Then the design would take all types of variation into account.

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Minimize the Gain Variations

Leaving R_S unbypassed helps reduce gain variations from device to device by providing degenerative current feedback. However, this method for minimizing gain variations is only effective when a substantial amount of gain is sacrificed.

A better approach is to use the combination-bias technique with the bias point selected from the transfer and transconductance curves (Figure 9).

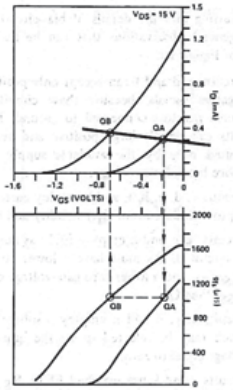


Figure 9. Gain variations are minimized when the load line is designed to intersect the pair of limiting transfer curves (top) at points of equal g_{fs} (bottom).

As Figure 9 shows, it is possible to find an R_S and a V_{GG} that will set I_{DQA} and I_{DQB} to values so that g_{fsQ} will be the same for both devices. The g_{fsQ} of all intermediate devices will be approximately equal to the limiting values. Thus, a constant, or nearly constant, stage gain is obtained even with a bypass capacitor.

The design procedure is as follows:

Step 1. Select a desired I_{DQA} below I_{DSSA}. A good value, allowing for temperature variations, is 60% of I_{DSSA}. This will allow for decreasing I_{DSS} due to temperature variation and for reasonable signal excursions in load current.

Step 2. Enter the transfer curves at $I_{DQA} \cong 0.6\ I_{DSSA}$ (0.3 mA) to find V_{GSQA}. This $V_{GSQA} \cong 0.2$ V for the 2N4339.

Step 3. Drop vertically at V_{GSQA} to the minimum limit transconductance curve to find g_{fsQA}. The value as read from the plot is approximately 1000 μmho.

Step 4. Travel across the g_{fs} plot to the maximum curve to find V_{GSQB} at the same value of g_{fs}. This is $V_{GSQB} \cong -0.7$ V.

Step 5. Travel vertically up to the maximum limit transfer curve to find I_{DQB} at V_{GSQB}. This is $I_{DQB} \cong 0.36$ mA.

Step 6. Construct an R_S bias line through points Q_A and Q_B on the transfer curves. The slope of the line is $1/R_S$, and the intercept with the V_{GS} axis is the required V_{GG}.

As Figure 9 demonstrates, it may be somewhat inconvenient to perform Step 6 graphically. An algebraic solution can then be employed instead. The source resistance is given by

$$R_S = (V_{GSQA} - V_{GSQB})/(I_{DQB} - I_{DQA}) \quad (2)$$

and the bias voltage is

$$V_{GG} = R_S I_{DQB} + V_{GSQB} \quad (3)$$

Care should be taken to maintain the proper algebraic signs in Equations 2 and 3. (For n-channel FETs, V_{GS} is negative and I_D is positive. For p-channel units, the signs are reversed.)

If the transconductance curves of Figure 9 are not available, g_{fs} can be determined by simply measuring the slope of the transfer curve at the desired operating point. Just place a straight-edge tangent to the curve at the Q-point and note the points at which it intercepts the I_D and V_{GS} axes. The slope and g_{fs} are given by:

$$\text{slope} = g_{fs} = I_{D(\text{intercept})} / -V_{GS(\text{intercept})} \quad (4)$$

In designing a constant-gain circuit, simply set the straight-edge tangent to the transfer curve of device A at point Q_A and slide it, without changing its slope, until it is tangent to the curve of device B. The tangency point is Q_B.

Designing Without Output Curves

Although the transfer characteristic has been seen to be extremely valuable in designing a bias circuit, it cannot be used to graphically establish V_{DSQ}. However, if a set of output curves is not available, V_{DSQ} can be determined or selected from the transfer curve by using the following procedure:

Step 1. Establish R_S and limiting values of I_{DQ}, V_{GSQ} and g_{fsQ} from the transfer curve.

Step 2. Establish V_{DD} as available, but in no case greater than BV_{GSS} nor less than several times $V_{GS(off)}$. There are special cases where V_{DD} will be below this limit, but in no case should instantaneous v_{dg} be allowed to fall below 2 x $V_{GS(off)}$ if minimum distortion is to be achieved.

Step 3. Set V_{DSQ} approximately midway between V_{DD} and 2 x $V_{GS(off)}$; lower if large output signals will not be handled.

Step 4. Select R_D to give the appropriate V_{DSQ}. The formula is:

$$R_D = [(V_{DD} - V_{DSQ})/0.5\ I_{DQA} + I_{DQB}] - R_S \quad (5)$$

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In the example of Figure 8, this procedure would have yielded $V_{DSQ} = (30-3)/2 = 13.5$ V and $R_D = (30 - 13.5)/0.5 (0.52 + 0.24)$ mA $- 1K\ \Omega = 42.5K\ \Omega$.

Step 5. Check to ensure that with this R_D, device B is not in a saturated condition $- V_{DQB} = V_{DD} - I_{DBQ} R_D > 2V_{GS(off)} + R_S I_{DBQ}$.

Decrease R_D if this condition is not met.

An alternate method, that selects R_D to provide a specified voltage gain, follows Steps 1 and 2 above and then proceeds as follows:

Step 3. Determine required stage gain, A_v, and set $R_D = A_v/g_{fsQ}$.

Step 4. Calculate V_{DSQ} to ensure that the criteria of Step 2 are not violated:

$$V_{DSQ} = V_{DD} - (R_D + R_S) I_{DQ} \qquad (6)$$

Step 5. If necessary, change I_{DQ}, V_{DD}, A_v and/or R_D to obtain an optimum compromise. ■■

FET SOURCE-FOLLOWER CIRCUITS

Too little knowledge of biasing methods for FET amplifiers sometimes keeps engineers from making maximum use of FETs in circuit designs. The common-drain amplifier, or source follower, is a particularly valuable configuration; its high input impedance and low output impedance make it very useful for impedance transformations between FETs and bipolar transistors.

By considering 10 circuits, which represent virtually every source-follower configuration, the designer can obtain consistent circuit performance despite wide device variations.

There are two basic connections for source followers: with and without gate feedback. Each connection comes in several variations (Figure 10). Circuits 10(a) through 10(e) have no gate feedback; their input impedances, therefore, are equal to R_G. Circuits 10(f) through 10(k) employ feedback to their gates to increase the input impedance above R_G.

Before getting into the details of bias-circuit design, note several general observations that can be made about the circuits of Figure 10:

- Circuits a, d and f can accept only positive and small negative signals, because these circuits have their source resistors connected to ground. The other circuits can handle large positive and negative signals limited only by the available supply voltages and device breakdown voltage.
- Circuits c, d, e, h, j, and k employ current sources to improve drain-current (I_D) stability and increase gain.
- Circuits d, e and k employ FETs as current sources. In circuit d, Q_2 must have a lower cut-off voltage, $V_{GS(off)}$, and a lower zero gate-voltage drain current, I_{DSS}, than Q_1.
- Circuits e, g, h and k employ a source resistor, R_S, which may be selected to set the quiescent output voltage equal to zero.
- Circuits e and k use matched FETs. R_S is selected to set I_D near the specified low-drift operating current. The input-output offset is zero.

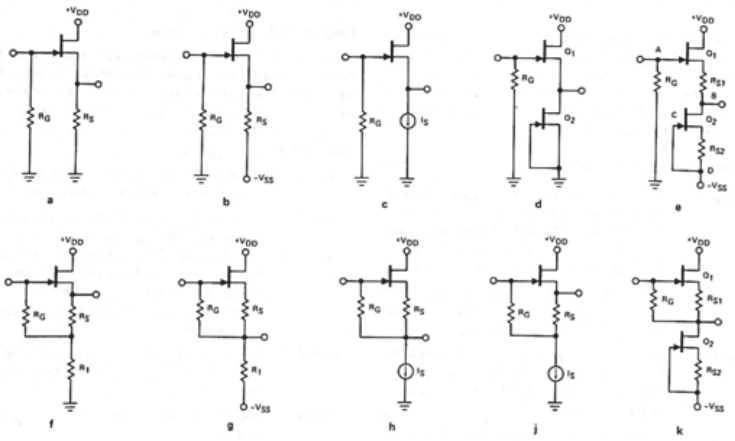


Figure 10. Virtually every practical source-follower configuration is represented in this collection of ten circuits. The configurations in the top row do not employ gate feedback; the corresponding ones in the bottom row do.

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Biasing Without Feedback is Simple

The no-feedback circuits of Figure 10 (circuits 10(a) through 10(e) use simple biasing techniques (see the earlier article). Circuit 10(a) is a self-bias configuration; the voltage drop across R_S biases the gate (which draws essentially zero current) through resistor R_G. Since no gate-to-source voltage, V_{GS}, can be developed when $I_D = 0$, the self-bias load line passes through the origin (Figure 11). For the 2N4339 FET, whose limiting transfer characteristics are used throughout this article, the quiescent drain current is seen to lie between about 0.25 and 0.55 mA when a 1K Ω source resistor is used. The quiescent output voltage lies between +0.25 and +0.55 V.

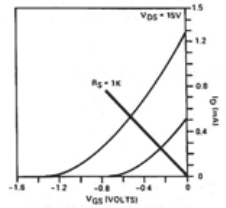


Figure 11. Self biasing (Figure 10a) uses the voltage dropped across the source resistor, R_S to bias the gate. The load line passes through the origin and has a slope of $-1/R_S$.

Circuit 10(b) is another example of source-resistor biasing with a $-V_{SS}$ supply added. The advantage over circuit 10(a) is that the signal voltage can swing negative to approximately $-V_{SS}$. Two bias lines are shown in Figure 12, one for $V_{SS} = -15$ V and the other $V_{SS} = -1.6$ V. For the first case, the quiescent output voltage lies between +0.18 and +0.74 V. For the second, it lies between +0.3 and +0.82 V.

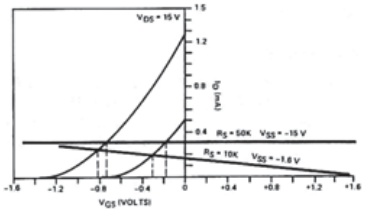


Figure 12. Adding a V_{SS} supply to the self-bias circuit (Figure 10b) allows it to handle large negative signals. The load line's intercept with the V_{GS}-axis is at $V_{GS} = -V_{SS}$. Bias lines are shown for $V_{SS} = -15$ V and $V_{SS} = -1.6$ V.

The bias load line for circuit 10(c) is just a horizontal line (I_D = constant). The quiescent output voltage is between +0.15 and 0.7 V for $I_D = 0.3$ mA.

Circuit 10(d) is similar to 10(c) except that the $V_{GS} = 0$ output characteristic of FET Q_2 is used as a current source. As seen in Figure 13, Q_2 does not supply constant current when its V_{DS} gets very small. This technique should therefore be used only to bias FETs whose $V_{GS(off)}$ is significantly higher than the equivalent $V_{GS(off)}$ of the current-source FET diode.

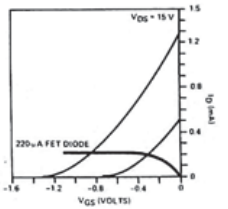


Figure 13. FET Q_2 doesn't behave like an ideal current source when its V_{DS} gets very small (Figure 10d). Therefore, Q_1 should have a significantly larger $V_{GS(off)}$ than Q_2 does.

A pair of matched FETs is used in the circuit of Figure 10(e), one as a source follower and the other as a current source. The operating drain current (I_{DQ}) is set by R_{S2}, as indicated by the load line of Figure 14. The drain current may be anywhere from 0.20 to 0.42 mA, as shown by the limiting transfer characteristic intercepts; however, $V_{GS1} = V_{GS2}$ because the FETs are matched.

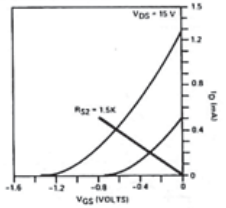


Figure 14. This load line is set by R_{S2} and Q_2 which acts as a current source (Figure 10e). If its components are properly matched, the circuit will have zero or near-zero offset.

Since $I_{D1} = I_{D2}$ and $V_{GS1} = V_{GS2}$, choosing $R_{S1} = R_{S2}$ will ensure that the voltage from point A to B equals the voltage point from point C to D (Figure 10(e)). This source follower, therefore, exhibits zero or near-zero offset. If the FETs are temperature-matched at the operating I_D, the source follower will exhibit zero or near-zero temperature drift.

Biasing With Feedback Increases Z_{in}

Each of the feedback-type source followers (Figure 10(f) through 10(k)) is biased by a method similar to that used with the nonfeedback circuit above it. However, in each case, R_G is returned to a point in the source circuit that provides almost unity feedback to the lower end of R_G. If R_S is chosen so that R_G is returned to zero dc volts (except in circuit 10(f), then the input/output offset is zero. R_1 is usually much larger than R_S.

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Circuit 10(f) is useful principally for ac-coupled circuits. R_S is usually much less than R_1 to provide near-unity feedback. The bias load line is set by R_S (Figure 15). The output load line, however is determined by the sum of $R_S + R_1$. The feedback voltage V_{FB}, measured at the junction of R_S and R_1, is determined by the intercept of the $R_S + R_1$ load line with the V_{GS} axis. The quiescent output voltage is $V_{FB} - V_{GS}$.

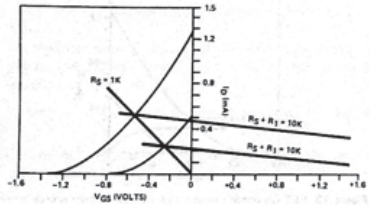


Figure 15. The bias load line is set by R_S but the output load line is determined by $R_S + R_1$ when gate feedback is employed (Figure 10f). The feedback V_{fb} is determined by the intercept of the $R_S + R_1$ load line and the V_{GS} axis.

In the circuit of Figure 10(g), R_S can be trimmed to provide zero offset. As the curves show (Figure 16), R_S will be between 670 ohms and 2.5K Ω. R_S is much less than R_1. The source load line intercepts the V_{GS} axis at $V_{SS} = -V_{GG} = -15$ V.

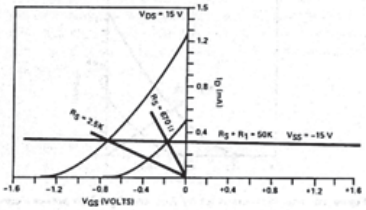


Figure 16. R_S can be trimmed to provide zero offset at some point between 670 ohms and 2.5K Ω (Figure 10g). The source load line intercepts the V_{GS} axis at $V_{SS} = V_{GG} = -15$ V. Note that this load line is not perfectly flat. It has a slope of −1/50K, because the current source is not perfect; it has a finite impedance.

Circuit 10(h) is almost the same as 10(g); the difference is that resistor R_1 is replaced by a current source. Since an ideal current source has infinite impedance, the bias curve of circuit 1(h) differs from that of Figure 10(g) (Figure 16) in that the load line is perfectly flat. In Figure 16 the load line is almost, but not quite, flat; it has a slope of −1/50k.

Circuit 10(j) is similar to 10(h) except that the output is taken from the top of R_S to reduce the output impedance. R_S must be trimmed if the circuit is to work at all properly.

In Figure 17, the constant-current load line represents a 0.3-mA current source, and the effect of a 1K Ω source resistor is shown. The offset voltage is seen to lie between 0.2 and 0.75 V. The intercept of the R_S load line and the V_{GS} axis sets the voltage at the junction of R_S and the current source (V_{FB}). For R_S = 1K Ω, V_{FB} will be between −0.1 V and +0.45 V. Since V_{FB} appears at the gate, it must be zero if the dc input impedance of the circuit is to be preserved.

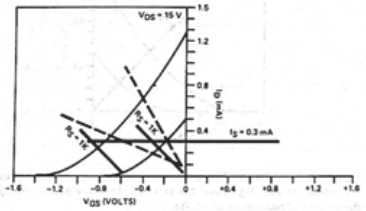


Figure 17. If R_S is not trimmed so that the load line passes through the origin, a voltage will appear at the gate causing a reduction in dc input impedance. The incremental input impedance will not be affected.

This can be done by trimming R_S, as shown dashed in Figure 17. The biasing then becomes the same as for circuit 10(h).

Biasing for circuit 10(k) is identical to that for circuit 10(e) (Figure 14) except that feedback is added to raise the input impedance.■■

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(1) Sherwin, J.S., "How, Why and Where to Use FETs," *Electronic Design*, May 17, 1966, p. 94.

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APPLICATION NOTE

Don't Trade Off Analog Switch Specs. VMOS—A Solution to High Speed, High Current, Low Resistance Analog Switches

Walt Heinzer

INTRODUCTION

For analog switches, Vertical MOS (VMOS) transistors give you a nearly ideal combination of characteristics—without the tradeoffs required by the more conventional components. These devices are now available from two American suppliers: Siliconix and its licensee, Semtech.

Unlike the commonly used N-channel JFETs, VMOS chips that handle more than a few hundred milliamps are also small enough for economical production. Smaller chips lead to lower inherent capacitances. Moreover, the basic VMOS structure provides lower ON resistance.

Some analog switches use relays, bipolar transistors and even triacs. Although electromechanical relays offer the lowest ON resistance initially, their ON resistance will vary with current and degrade with use. Also, relays suffer from mechanical limitations.

Bipolar transistors require base-drive current that causes offset in the switched analog signal. Triacs are only suitable for switching raw power; for analog switching, they introduce too much offset and non-linearity although they easily handle high power.

VMOS Offers High Performance

VMOS devices aren't limited by any of these disadvantages. They can switch 10 W, linearly, over a wide dynamic range. In addition, VMOS input impedance is very high, and only input voltage (no current) turns the transistors OFF or ON. And since the drain-to-source channel is purely resistive while ON, you get low distortion.

VMOS transistors in analog switches offer several more advantages, including

- 1.8 Ω ON resistance, which results in low insertion loss in low-impedance systems
- 2.0 A DC current capability—paralleling three VMOS devices increases this capability to 6.0 A and unlike other devices, paralleled VMOS do not require power-wasting ballast resistors
- 3 A peak current, which makes VMOS super for driving capacitive lines and quickly charging and discharging capacitors in high speed A/D converters, sample and hold circuits, and integrators
- 60 dB isolation at 10 MHz and 500 nA DC leakage in the OFF state
- Enhancement-mode operation with a 0.8 to 2.0 V threshold, which gives VMOS direct compatibility with CMOS and TTL. And the logic gates aren't loaded by the VMOS.
- Linear ON resistance, which results in low total harmonic and intermodulation distortion

What's more, all these capabilities come in a TO-202AA package.

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Examine the output characteristics of a low resistance VMOS device like the Siliconix VN46AF. A look at the transfer characteristic in Figure 1A reveals that varying the gate-to-source voltage from 0 to +10 V switches the VN46AF from OFF to ON–with a 3 Ω ON resistance. From the curve you can see that the device turns OFF well before zero volts, which eases interfacing with logic.

In the VN46AF schematic in Figure 1B, note that the body and source are internally connected. Figure 1C and 1D, respectively, show simplified models of the VN46AF's OFF and ON states. Diode D_1 is the body-to-drain PN junction. When the VN46AF is OFF, its drain current vs drain-to-source voltage characteristics (Figure 1E) is essentially the curve for D_1.

The breakdown for D_1 is 40 V, and the diode exhibits forward conduction for drain-to-source potential as low as – 0.6 V. This diode therefore constrains the analog voltage, which a simple switch (one VMOS transistor) can handle, to between –0.6 and +40 V.

When the VN46AF is ON, a 2 Ω resistance is in parallel with D_1. Maximum continuous current in either direction is 2.0 A, even though the diode is forward-biased for currents over 0.5 A.

One VMOS Device Makes an Analog Gate

VMOS characteristics are put to good use in the analog switch of Figure 1F. In the ON state, the gate of the VN46AF is positive with respect to the source. In the OFF state, the gate-to-source voltage is zero. The 2.0 A capability and the 3 Ω ON resistance of the VMOS transistor can be fully exploited in this circuit. The input signal, however, is restricted to positive voltages and must always be greater than the output voltage. Otherwise, OFF isolation is impaired.

Both ON and OFF switching takes 200 ns, charge feed-through during the ON-to-OFF transition is 80 pC with a 50 Ω load. Charge transfer is, of course, especially important in sample and hold systems. For example, 80 pC into 0.01 μF causes an offset of 8 mV.

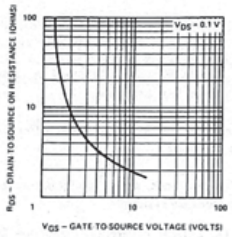
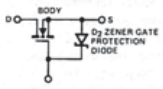
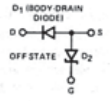


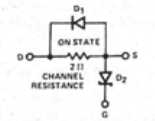
Figure 1A



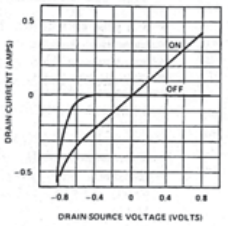
Schematic Symbol of VN46AF
Figure 1B



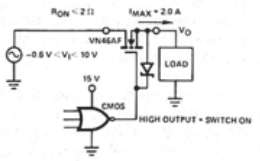
Equivalent OFF Condition (V_{GS} = 0)
Figure 1C



Equivalent ON Condition
(V_{GS} = 10 V)
Figure 1D



Small Signal Characteristics of VN46AF
Figure 1E



A Simple Unidirectional VMOS Analog Switch ($v_i > v_o$)
Figure 1F

The VN46AF switches from OFF to ON with a 3 Ω drain-to-source resistance, when its gate-to-source potential swings from 0 to +10 V. The device turns OFF at about 1 V (A). Some VMOS transistors (B) carry an on-board zener diode that protects the gate-to-source junction. A VMOS transistor is equivalent to two diodes in the OFF state (C), when the gate-to-source voltage is less than the threshold value. The equivalent diode, D_1 is shunted by 3 Ω when the VMOS device is ON (D), with the gate-to-source potential at +10 V. The small signal drain-to-source voltage vs current characteristic (E) is essentially determined by the body-to-drain diode. The input is restricted to positive voltages in the single-VMOS analog gate (F).

Figure 1

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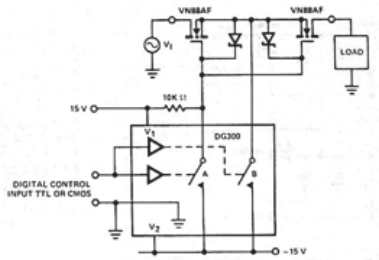
In Series, They Switch Both Polarities

To increase the switch's dynamic range, connect two VN88AF's in series (Figure 2A). In the ON state, both halves of the DG300 analog switch are open, so the gates of both VN88AF's are pulled to +15 V through the 10K Ω resistor. The ON resistance of this analog switch is twice as high as the drain-to-source resistance of a single VN88AF. The maximum current that this two-transistor switch can handle is the same as that for a single-transistor switch (2.0 A).

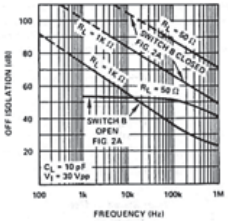
The switch is turned OFF by shorting the gates to the negative supply, thereby reducing the gate-to-source voltage to less than the threshold of 0.8 V. The second section of the DG300 adds 30 dB OFF isolation by shunting the signal-leakage path (through both sources) to the negative supply. OFF-isolation curves (Figure 2B) show that the DG300 raises the circuit's isolation and that decreasing the load resistance increases isolation.

Since the two transistors are back-to-back, one body-to-drain diode is always reverse-biased. This eliminates the OFF-state problem caused by forward-biasing the diode.

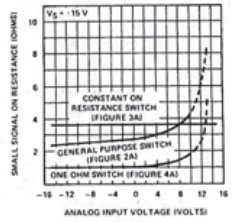
Since the bidirectional switch's gate drive is referenced to a fixed supply, its ON resistance varies with the input analog voltage (Figure 2C). This variation introduces distortion when you're driving low-impedance loads such as speakers or transmission lines. For constant ON resistance, use the circuit in Figure 3A.



A General Purpose Bidirectional Analog Switch
Figure 2A



OFF Isolation vs Frequency
Figure 2B



Small Signal ON Resistance vs Analog Input Voltage
Figure 2C

ON resistance is doubled in the two-VMOS switch (A), but inputs of both polarities are handled without losing isolation. The DG300 analog gate (B) raises the circuit's isolation by 30 dB. Decreasing load resistance also improves isolation. With the gate drive referenced to a fixed voltage (C), the ON resistance varies undesirably with the input, and generates distortion, especially with low impedance loads like speakers and transmission lines.

Figure 2

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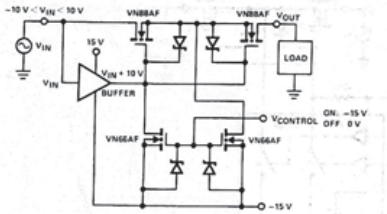
Bootstrapping Adds Linearity

In the ON state, a bootstrap voltage that tracks the input drives the gates of the VN88AF's. This bootstrapping keeps the VMOS's gate-to-source voltage constant and independent of the input signal. So, changes in the input-signal level do not modulate the ON resistance of the switch.

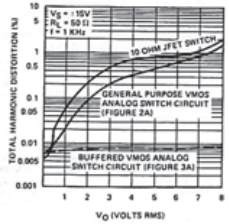
The buffer circuit reduces the computed total harmonic distortion from 1.5% to 0.005%, for 8 Vrms at 1 kHz into 50 Ω (Figure 3B). The popular 10 Ω DG186 JFET analog switch generates a higher total harmonic distortion of about 2%.

The two buffer circuits shown in Figures 3C and 3D isolate the input signal and employ a zener diode to provide a fixed gate-to-source voltage. The general-purpose buffer of Figure 3C has a flat frequency response of up to 300 kHz and accepts inputs ranging between ±15 V. The buffer of Figure 3D, VN66AK source follower, has its frequency response extended to 50 MHz and, when operated from ±30 V supplies, increases the signal range to ± 30 V.

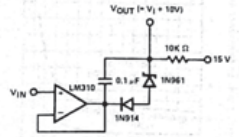
The VN66AK and VN88AF do not have on-board zener diodes like the VN66AF transistor. At the expense of the diode protection, the VN66AK and VN88AF gain lower capacitance from gate-to-source and reduced DC "see through" from driver to signal path. Bootstrapping the switch's gate circuits with a buffer permits the switch to operate with low distortion even as the signal amplitude comes close to the positive supply voltage.



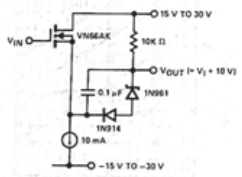
Low Distortion Constant ON Resistance Switch
Figure 3A



Distortion Improvement Using the Buffered Analog Switch
Figure 3B



General Purpose Buffer
Figure 3C



High Speed Buffer
Figure 3D

Bootstrapping the gate and input cuts distortion by holding the ON resistance constant (A). The buffered bootstrap circuit (A) distorts less than either a JFET or a nonbootstrapped VMOS analog switch (B). A general-purpose buffer (C) using the LM310 op amp is suitable for low speed switches, but when you need a fast analog switch, use the VN66AK buffer (D). In addition to speed, this buffer gives you increased isolation.

Figure 3

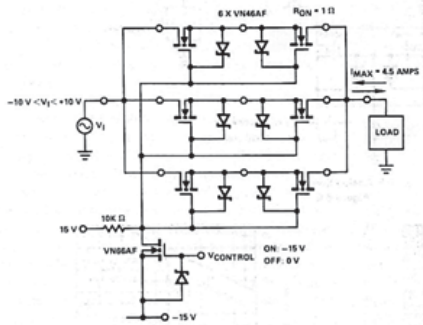
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VMOS Devices Parallel Without Padding

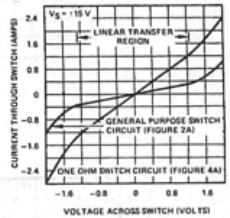
Paralleling devices lowers the total ON resistance. For example, three paralleled legs, each with two VN46AF's in series, make a 1 Ω switch (Figure 4A). Because VMOS devices are immune to current hogging, no ballast or balance resistors are needed. Negative tempcos, a VMOS feature, cause these devices to draw less current as they heat up. As a result, excess current is automatically shared by paralleled VMOS devices.

Paralleling three VN46AF's not only decreases ON resistance, but also increases the current capability to 6.0 A and extends the linear range of the large signal transfer characteristic from 0.3 to 1.2 A (Figure 4B).

The voltage range of the basic analog switch can also be increased. Simply use a higher breakdown VMOS unit (Figure 5). The VN98AK's have a 90 V breakdown, which allows up to ±40 V of voltage swing capability. However, these higher voltage devices do carry a penalty—the ON resistance is higher: 3.5 Ω vs 3.0 Ω for the VN46AF. Zener diode D_1 limits the gate-to-source potential to 30 V, and thereby prevents a possible gate-oxide rupture. Diode CR110 limits the current from the 50 V gate-bias supply.



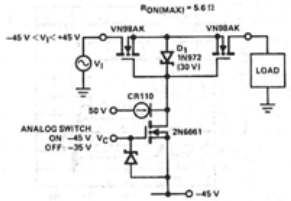
Ultra Low Resistance Switch (1 Ohm)
Figure 4A



Large Signal Transfer Characteristics
Figure 4B

No ballast or balance resistors are needed when VMOS devices are paralleled (A) because negative tempcos immunize them from current hogging. Paralleling extends the linear range from 0.3 to 1.2A (B) as it decreases the ON resistance of the analog switch to 1 Ω and increases its current-handling capability to 4.5 A.

Figure 4



90 V Peak to Peak Analog Switch

You pay for 90 V breakdown in the VN98AK with 3.0 Ω ON resistance, which allows swings of ±40 V. The zener diode limits the gate to-source potentials to 30 V.

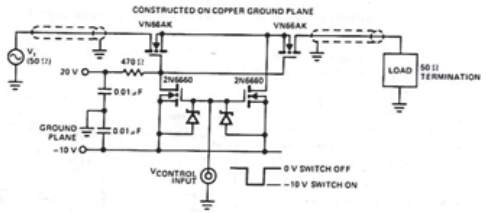
Figure 5

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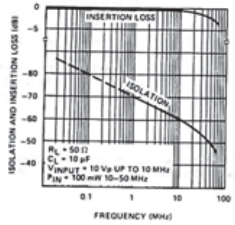
For the Ultimate in Switching Speed

The high power RF switch shown in Figure 6A performs very well up to 50 MHz–with turn-ON and turn-OFF times of 50 ns. At 10 MHz, isolation is 60 dB with a 20 V pk-pk input signal. Insertion loss is only 1 dB with a 50 Ω load (Figure 6B). The gain vs input power curve in Figure 6C shows that the RF analog switch using VN66AK's can put 1 W into a 50 Ω load at 14 MHz. The two-tone, third order, intermodulation product curves show a 42 dB intercept point with 1 dB of gain compression at 25 dBm input power.

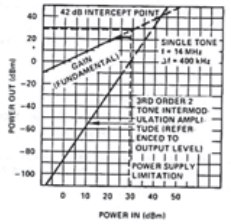
Turn-ON time of the switch (Figure 6D) is determined by the passive pull-up resistor combined with the capacitance at the gates of the VN66AK's. The negative turn-OFF transient is caused by charge-coupling to the output through the output capacitance of the VN66AK.



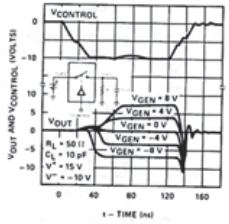
RF Analog Switch
Figure 6A



Insertion Loss and Isolation vs Frequency of RF Analog Switch
Figure 6B



Gain and Two Tone 3rd Order Intermodulation
Figure 6C



Switching Response of RF Switch into 50 Ohm Load
Figure 6D

The VN66AK switches high power at RF (A). At 10 MHz, a 20 V pk-pk signal is attenuated by 60 dB and the insertion loss is only 1 dB into 50 Ω and 10 pF (B). Third-order intermodulation distortion is given by the 42 dB intercept point, and 1 dB gain compression occurs at 25 dBm input for 14 MHz (C). The negative turn-OFF transient (D) is caused by charge-coupling to the output through the output capacitance of the VN66AK.

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APPLICATION NOTE

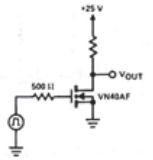
Driving VMOS Power FETs

Dave Hoffman
January 1979

INTRODUCTION

Using VMOS Power FETs you can achieve performance never before possible–if you drive them properly. This article describes circuits and suggests design methods to be used in order to obtain the performance from VMOS that you need.

When designing with VMOS there are some facts that must be kept in mind in order to get optimum results with every circuit. The first fact is that VMOS is a very high frequency device. The cut-off frequency for all VMOS FETs is several hundred megahertz. Most power designers are not used to designing with extremely high frequency devices because with bipolars the frequency response decreases as the power increases. The very high frequency response of VMOS is the basis for many of its advantages but it must be kept in mind while designing. With improper circuit design VMOS can oscillate. This oscillation can be eliminated, though, by exercising two simple precautions. First, minimize lead and trace lengths whenever possible, especially leads associated with the gate of the FET. If it is not possible to have short leads to the gate place a ferrite bead on the gate lead or a small resistor in series with the gate. The ferrite bead or the resistor must be very close to the gate. Second, because of the extremely high input impedance of VMOS (in excess of 10^{12} Ω) drive circuits may be designed which are very high impedance. Under these conditions it is possible for the gate node to get enough positive feedback from the gate-to-drain capacitance or just from stray fields in the circuit to cause oscillation. This must be kept in mind in the design of the circuit.



A Typical VMOS Switching Circuit
Figure 1

When driving VMOS it must be kept in mind that the dynamic input impedance is very different than the static input impedance. The input of a VMOS device is capacitive. The DC input impedance is very high but the AC input impedance varies with frequency. Because of this effect, the rise and fall times of VMOS are dependent on the output impedance of the circuit driving it. The first approximation of the rise or fall time is simply

$$t_r \text{ or } t_f = 2.2 \cdot R_{OUT} \cdot C_{iss} \quad (1)$$

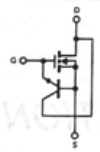
where R_{OUT} is the output impedance of the drive circuit. This equation is valid only if the drain load resistance is much larger than R_{OUT}. Knowing this fact, along with the fact that there is no storage or delay time with VMOS, it is very easy to calculate the rise and fall times and set them to any desired value. For example, if you wanted to calculate the 10% to 90% rise or fall time for the circuit shown in Figure 1 using Equation 1 the rise time is equal to:

$$t_r = (2.2)\,(500)\,(50 \times 10^{-12}) = 55 \text{ nsec}$$

The dynamic input characteristics of VMOS are covered very thoroughly in Siliconix' application note AN79-3.[1]

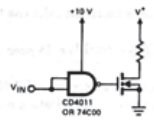
A last thing to remember when you are driving VMOS is the input protection zener diode. When putting a positive voltage on the gate with respect to the source, the maximum voltage rating of the zener diode should not be exceeded. It is more important, however, that you do not forward bias the zener diode by putting a negative voltage on the gate while the VMOS is operating in a circuit. The reason for this is most easily explained by referring to Figure 2. As can be seen in the figure, the zener diode is actually the base-emitter junction of a bipolar transistor. If a negative voltage greater than 0.6 V is placed on the gate, the base-emitter junction of the bipolar will be forward biased which will turn on the bipolar transistor. When the bipolar is turned on, current will flow from the drain through the bipolar and out the gate. This operating condition is very likely to be destructive. If negative voltages must be placed on the gate it is recommended that you use a VMOS part that does not have an input zener diode. Non-zenered equivalents are available for most of Siliconix' zenered devices.

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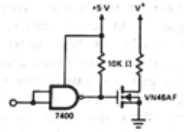


A Parasitic NPN Transistor in Zener Protected MOSFETS
Figure 2

Of all operating modes the common-source configuration is the simplest to drive. Because of the high input impedance of VMOS it can be driven directly from many logic families. When driving from a CMOS gate as shown in Figure 3, rise and fall times of about 60 nsec can be expected due to the limited source and sink currents available from the CMOS gate.[2] If faster rise and fall times are required there are several ways to obtain them. One easy way is if there are extra gates in the package that is driving the VMOS simply put the extra gates in parallel with the gate already being used. The additional current available will cut down the rise and fall times. If no extra gates are available an emitter-follower buffer can be used as shown in Figure 4. With this circuit the current available to the VMOS will be the output current of the CMOS multiplied by the beta of the bipolars. Because the bipolars are operating as emitter-followers there will still be no storage time to worry about and the frequency limit will be determined by either the CMOS gate or the f_T of the bipolars, whichever comes first.



Driving VMOS with a CMOS Gate
Figure 3

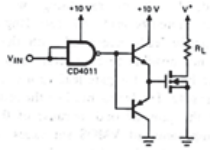


Pulling Up a TTL Output Will Increase the Sink Current of the VMOS
Figure 5

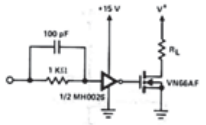
VMOS can also be driven directly from TTL gates. Because the output voltage of TTL is limited, the output current of the VMOS will be limited to some value less than its maximum rated current. The output current that can be expected can be determined from the transfer characteristic of the device being used. For example, if a TTL gate is driving VN46AF the minimum output current of the VMOS will be approximately 250 mA. This value was obtained by using the minimum output voltage of the TTL gate (3.2 V) for a high level output and referring to the transfer characteristic for the VNAZ which is the VMOS geometry used in the VN46AF. If more than 250 mA is required the output of a standard VMOS gate can be pulled up to the 5 V rail as shown in Figure 5. With a full 5 V on the gate the VN46AF will typically sink 600 mA.

For very high speeds a capacitive driver such as the MH0026 can be used as shown in Figure 6. With this drive configuration typical rise and fall times are less than 10 nsec.

When operated in the common-drain mode VMOS is somewhat more difficult to drive than when in the common-source mode. Because of VMOS' high input impedance, though, it is considerably easier to drive common-drain than a bipolar would be when operated common collector. Common-drain circuits can be used when the load needs to be connected to ground, when an active pull-up and pull-down is required (totem pole circuit), or in bridge type circuits. For the purpose of this discussion all examples will be shown with totem pole circuits.



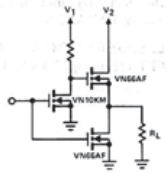
An Emitter-Follower Circuit Will Decrease VMOS Rise and Fall Times
Figure 4



Using an MOS Clock Driver to Drive VMOS
Figure 6

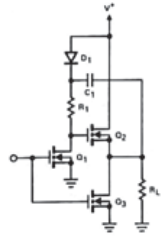
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The difficulty with common-drain circuits occurs because as the voltage across the load increases the enhancement voltage of the common-drain device decreases. Referring to Figure 7, as the voltage across R_L approaches V_2 the enhancement voltage for the upper VN66AF decreases. If V_1 is not greater than V_2 then the voltage across R_L can never reach V_2. For this reason whenever a common-drain circuit is used it is always necessary to have or to generate a voltage that is greater than the voltage which is desired to be impressed across the load. The amount the voltage has to be above the desired drain voltage is dependent upon the current the VMOS must source and can be determined from the transfer characteristic of the VMOS being used. If no supply voltage is available other than the one the load is to be pulled up to, one can be generated. This can be done very easily because of the very low drive current requirements of the VMOS.

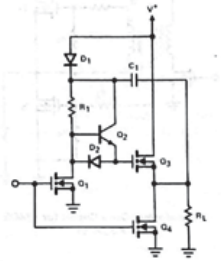


VMOS in Totem-Pole Configuration
Figure 7

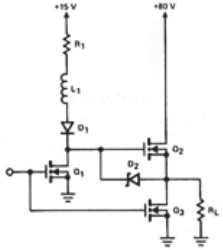
One way of generating the required gate voltage is the bootstrap circuit shown in Figure 8. In the circuit, when Q_1 and Q_3 are on, C_1 is charged to the supply rail through D_1. When Q_1 and Q_3 are turned off, the gate voltage on Q_2 goes to the supply rail. As the source of Q_2 begins to pull R_L up, the voltage across C_1 will be maintained, therefore, the gate-to-source voltage of Q_2 will be maintained. The size of C_1 should be large enough so that when it charges the gate capacitance of Q_2 a minimum voltage equal to the required enhancement voltage of Q_2 will be maintained across it. A good rule of thumb is to make C_1 equal to ten times the C_{iss} of the FET. Figure 9 shows the same bootstrap circuit with some added components to improve the rise and fall times. In the circuit Q_2 acts as an emitter-follower to increase the peak gate current to Q_3. D_2 will be forward biased when Q_1 turns on and serves as a low impedance path to discharge the gate of Q_3.



VMOS Bootstrap Circuit
Figure 8



Bootstrap Circuit with Emitter-Follower for Improved Rise Times
Figure 9

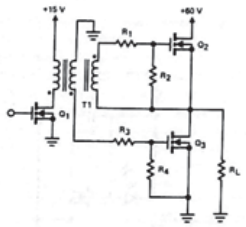


Inductive Kickback Drive Circuit
Figure 10

Another method to drive a common-drain VMOS FET is shown in Figure 10. Rather than charging a capacitor and then feeding a signal back from the output as was done in the bootstrap circuit, this circuit stores the required charge in an inductor. When Q_1 is turned off a flyback voltage is generated across the inductor. This voltage is used to maintain an enhancement voltage equal to the voltage of zener diode D_2 across the VMOS FET. Once the Q_2 has been fully turned on and the voltage on R_L is at the rail a negligible amount of energy is required to keep Q_2 on. Q_2 will remain on until Q_1 is turned on, or until the leakage currents of Q_1 and D_2 discharge the gate capacitance of Q_2.

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Another method that can be used to drive a common-drain VMOS is transformer drive. A transformer drive circuit is shown in Figure 11. In this circuit the transformer is used in the flyback mode when turning on the upper FET. R_1 and R_3 are used to suppress ringing and R_2 and R_4 are used to assist with turn-off of the FETs. When driving with a transformer, care must be taken to design the transformer so that the secondary inductance in conjunction with the input capacitance of the FET does not create ringing of oscillation problems.



Transformer Drive Circuit for VMOS
Figure 11

SUMMARY

The very high input impedances of VMOS Power FETs greatly simplify the drive requirements as compared to bipolars. The input drive requirements for both common-source and common-drain configurations were discussed in detail. With common-source circuits the requirement that needs to be kept in mind is the rise and fall time required. With common-drain circuits a method of maintaining an adequate enhancement voltage must be considered in addition to required rise and fall time requirements.

REFERENCES

1. A. Evans, D. Hoffman, "Dynamic Input Characteristics of a VMOS Power Switch" AN79-3.
2. D. Hoffman, L. Schaeffer, "VMOS – A Breakthrough in Power MOSFET Technology" AN76-3.

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_____	OEM Pricing/Product Information Selector Guide

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_____	Siliconix, Inc. Annual Report, 1979

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glossary of terms and abbreviations

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1. Upper case letters indicate DC voltages and currents.
2. Lower case letters indicate AC voltages and currents.
3. Subscripts can refer to the terminals used in the measurements, i.e., V_G = Gate Voltage; or simply help define the symbol, i.e., t_f = Fall Time, t_r = Rise Time.
4. Triple subscripts are used for terminal references only. The first subscript is the object terminal. The second subscript is the common terminal. The third gives the condition of the remaining terminal(s). S = Short, 0 = open and X = neither open nor short (refer to the test conditions). Example: BV_{GSS} = Breakdown Voltage from gate to source with the drain shorted to the source.

b_{fg}	= Common-Gate Forward Susceptance
b_{fs}	= Common-Source Forward Susceptance
b_{igs}	= Common-Gate Input Susceptance
b_{iss}	= Common-Source Input Susceptance
b_{ogs}	= Common-Gate Output Susceptance
b_{oss}	= Common-Source Output Susceptance
b_{rg}	= Common-Gate Reverse Susceptance
b_{rs}	= Common-Source Reverse Susceptance
BV_{DGO}	= Drain-Gate Breakdown Voltage
BV_{DSS}	= Drain-Source Breakdown Voltage
BV_{SDX}	= Drain-Source Breakdown Voltage
BV_{G1G2}	= Gate-Gate Breakdown Voltage
BV_{G1SS}	= Gate 1 to Source Breakdown Voltage
BV_{G2SS}	= Gate 2 to Source Breakdown Voltage
BV_{GBS}	= Gate-Body Breakdown Voltage
BV_{GSS}	= Gate-Source Breakdown Voltage
BV_{SDS}	= Source-Drain Breakdown Voltage
BV_{SGO}	= Source-Gate Breakdown Voltage
C_{db}	= Drain-Body Capacitance
C_{dgo}	= Drain-Gate Capacitance
C_{gb}	= Gate-Body Capacitance
C_{gd}	= Gate-Drain Capacitance
C_{gs}	= Gate- Source Capacitance
C_{iss}	= Common-Source Input Capacitance
C_{oss}	= Common-Source Output Capacitance
C_{rss}	= Common-Source Reverse Transfer Capacitance
C_{sb}	= Source-Body Capacitance
C_{sd}	= Source-Drain Capacitance
C_{sgo}	= Source-Gate Capacitance
D	= Drain
$\bar{e}_N$	= Equivalent Short Circuit Input Noise Voltage
f_m	= Figure of Merit
G	= Gate
g_{fg}	= Common-Gate Forward Transconductance
g_{fs}	= Common-Source Forward Transconductance
g_{fso}	= Common-Source Forward Transconductance @ V_{GS} = 0
g_{fs1}/g_{fs2}	= Common-Source Forward Transconductance Ratio
g_{ig}	= Common-Gate Input Conductance
g_{is}	= Common-Source Input Conductance
g_{og}	= Common- Gate Output Conductance
g_{os}	= Common-Source Output Conductance
g_{oss}	= Common Source Output Conductance @ V_{GS} = 0
g_{os1}-g_{os2}	= Differential Output Conductance
G_{pg}	= Common-Gate Power Gain
G_{ps}	= Common-Source Power Gain
$I_{D(off)}$	= Drain Cutoff Current
$I_{D(on)}$	= Drain ON Current
I_{DGO}	= Drain-Gate Leakage

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glossary of terms and abbreviations (cont'd)

I_{DSS}	= Saturation Drain Current
I_{DSS1}/I_{DSS2}	= Saturation Drain Current Ratio
I_F	= Forward Current
I_G	= Gate Operating Current
I_{G1G2}	= Gate to Gate Leakage Current
$\lvert I_{G1}-I_{G2}\rvert$	= Differential Gate Operating Currents
I_{GBS}	= Gate to Body Leakage Current
$I_{G(f)}$	= Gate Forward Current
I_{GSS}	= Gate Reverse Current
I_{G1SS}	= Gate 1 to Source Leakage Current
I_{G2SS}	= Gate 2 to Source Leakage Current
I_{G1SSR}	= Gate 1 to Source Reverse Leakage Current
I_{G2SSR}	= Gate 2 to Source Reverse Leakage Current
$\bar{i}_n$	= Equivalent Open-Circuit Noise Current
I_P	= Pinch-Off Current
NF	= Noise Figure
P_D	= Continuous Power Dissipation
P_{OV}	= Peak Operating Voltage
$r_{ds(on)}$	= Drain-Source ON Resistance
$r_{DS(on)}$	= Static Drain-Source ON Resistance
$Re\ (Y_{fg})$	= Common-Gate Forward Transconductance
$Re\ (Y_{fs})$	= Common-Source Forward Transconductance
$Re\ (Y_{ig})$	= Common-Gate Input Conductance
$Re\ (Y_{is})$	= Common-Gate Output Conductance
$Re\ (Y_{os})$	= Common-Source Output Conductance
$Re\ (Y_{rg})$	= Common-Gate Reverse Transconductance
$Re\ (Y_{rs})$	= Common-Source Reverse Transconductance
r_{GS}	= Common-Source Input Resistance
S	= Source
t_d	= Delay Time
$t_{d(off)}$	= Turn-Off Delay Time
$t_{d(on)}$	= Turn-On Delay Time
t_f	= Fall Time
T_j	= Junction Temperature
t_{off}	= Turn-Off Time
t_{on}	= Turn-On Time
T_l	= Lead Temperature
t_r	= Rise Time
T_{stg}	= Storage Temperature
V_B	= Body Voltage
V_{BB}	= Body Supply Voltage
V_D	= Drain Voltage
V_{DD}	= Drain Supply Voltage
$V_{DS(on)}$	= Drain-Source ON Voltage
V_G	= Gate Voltage
V_{GG}	= Gate Supply Voltage
V_{GS}	= Gate-Source Voltage
$\lvert V_{GS1}-V_{GS2}\rvert$	= Differential Gate-Source Voltage
ΔV_{GS}	= Differential Gate-Source Voltage
$\frac{\Delta\lvert V_{gs1}-V_{gs2}\rvert}{\Delta T}$	= Differential Gate-Source Voltage Change with Temperature
$V_{GS(f)}$	= Gate-Source Forward Voltage
$V_{GS(th)}$	= Gate Threshold Voltage
$V_{GS(off)}$	= Gate Source Cutoff Voltage
$V_{G1S(off)}$	= Gate 1 to Source Cutoff Voltage
$V_{G2S(off)}$	= Gate 2 to Source Cutoff Voltage
V_S	= Source Voltage
V_{SS}	= Source Supply Voltage
Z_d	= Dynamic Impedance
Z_k	= Knee AC Impedance
θ_I	= Current Temperature Coefficient
θ_{J-A}	= Junction to Ambient Thermal Resistance
θ_{J-C}	= Junction to Case Thermal Resistance

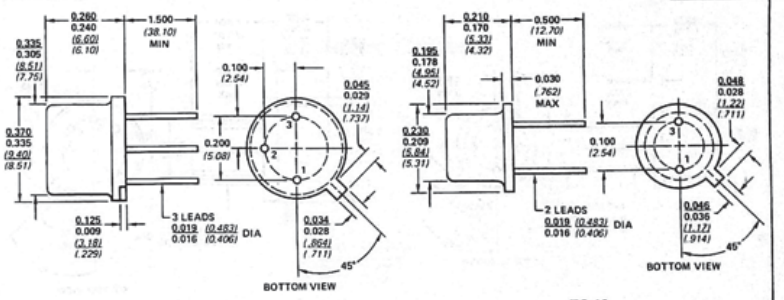
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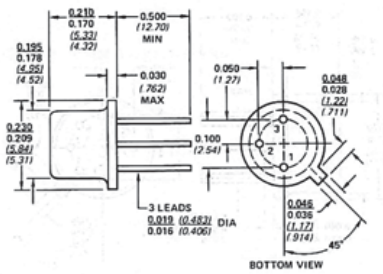
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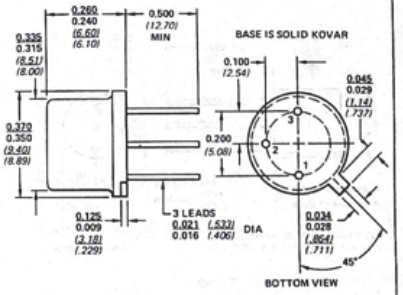


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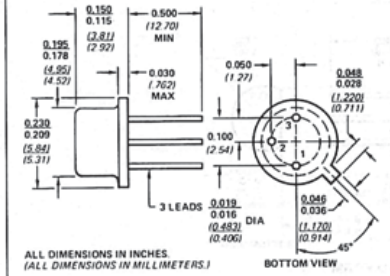
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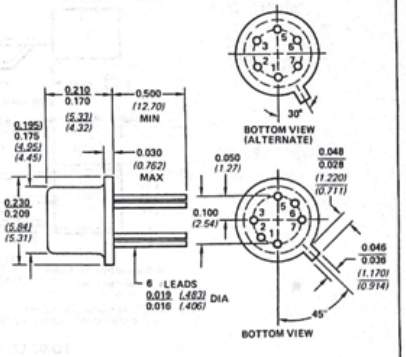


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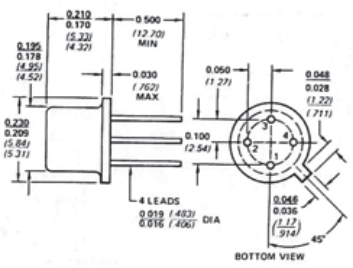


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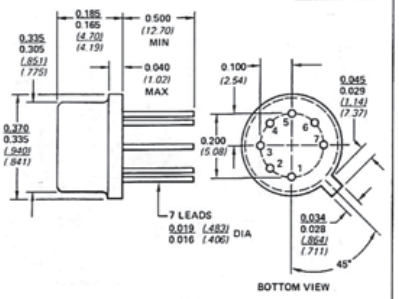
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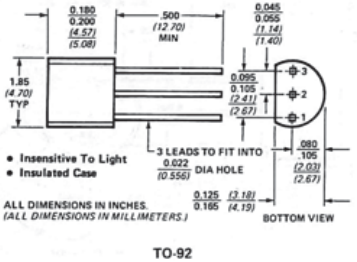
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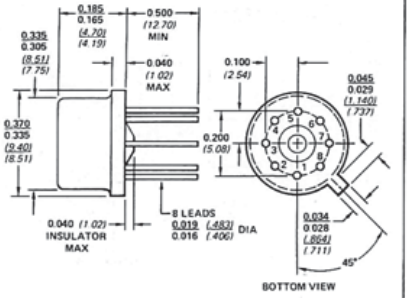
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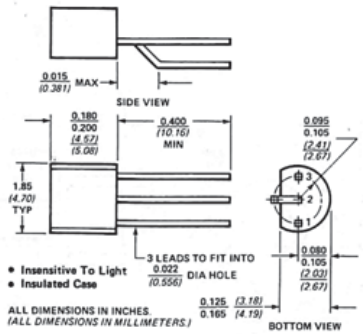
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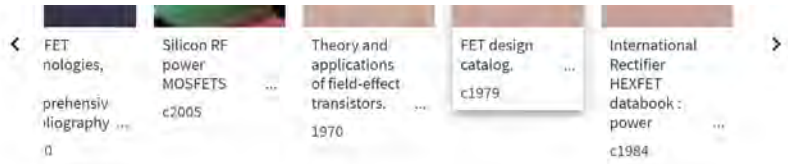
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949 a| QC176.A1I3 v.26 no.10-12 1991 w| LCPER c| 1 i| 26090101018 d| 5/24/2024 e| 5/14/2024 l| CATO-PARK m| UP-ANNEX n| 1 r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 018

949 a| QC176.A1I3 v.27 no.4-6 1992 w| LCPER c| 1 i| 26090101020 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 020

949 a| QC176.A1I3 v.27 no.7-10 1992 w| LCPER c| 1 i| 26090101021 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 021

949 a| QC176.A1I3 v.27 no.11-12 1992 w| LCPER c| 1 i| 26090101022 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 022

949 a| QC176.A1I3 v.28 no.1-6 1993 w| LCPER c| 1 i| 26090101023 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 023

949 a| QC176.A1I3 v.28 no.7-12 1993 w| LCPER c| 1 i| 26090101024 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 024

949 a| QC176.A1I3 v.29 no.1-6 1994 w| LCPER c| 1 i| 26090101025 d| 7/3/2019 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 025

949 a| QC176.A1I3 v.29 no.7-12 1994 w| LCPER c| 1 i| 26090101026 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 026

949 a| QC176.A1I3 v.30 no.1-6 1995 w| LCPER c| 1 i| 26090101027 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 027

949 a| QC176.A1I3 v.30 no.7-12 1995 w| LCPER c| 1 i| 26090101028 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 028

949 a| QC176.A1I3 v.31 no.1-6 1996 w| LCPER c| 1 i| 26090101029 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 029

949 a| QC176.A1I3 v.31 no.7-9 1996 w| LCPER c| 1 i| 26090101030 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 030

949 a| QC176.A1I3 v.31 no.10-12 1996 w| LCPER c| 1 i| 26090101031 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 031

949 a| QC176.A1I3 v.32 no.1-6 1997 w| LCPER c| 1 i| 26090101032 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 032

949 a| QC176.A1I3 v.32 no.7-12 1997 w| LCPER c| 1 i| 26090101033 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 033

949 a| QC176.A1I3 v.33 no.1-6 1998 w| LCPER c| 1 i| 26090101034 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 034

949 a| QC176.A1I3 v.33 no.7-12 1998 w| LCPER c| 1 i| 26090101035 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 035

949			a| QC176.A1I3 v.34 no.1-6 1999 w| LCPER c| 1 i| 26090101036 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 036
949			a| QC176.A1I3 v.34 no.7-12 1999 w| LCPER c| 1 i| 26110101017 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2611 0| 0101 1| 017
949			a| QC176.A1I3 v.35 no.1-6 2000 w| LCPER c| 1 i| 26110101018 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2611 0| 0101 1| 018
949			a| QC176.A1I3 v.35 no.7-12 2000 w| LCPER c| 1 i| 26110101019 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 11/1/2001 x| D z| 2611 0| 0101 1| 019
949			a| QC176.A1I3 v.36 no.1-6 2001 w| LCPER c| 1 i| 26110101020 d| 6/28/2003 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 7/18/2002 x| D z| 2611 0| 0101 1| 020
949			a| QC176.A1I3 v.36 no.7-12 2001 w| LCPER c| 1 i| 26110101021 d| 6/28/2003 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 7/18/2002 x| D z| 2611 0| 0101 1| 021
949			a| QC176.A1I3 v.37 no.1-6 2002 w| LCPER c| 1 i| 26110101022 d| 12/19/2024 e| 11/14/2024 l| CATO-PARK m| UP-ANNEX n| 2 q| 1 r| Y s| Y t| PERIODICAL u| 3/4/2003 x| D z| 2611 0| 0101 1| 022
949			a| QC176.A1I3 v.37 no.7-12 2002 w| LCPER c| 1 i| 26110101023 d| 12/17/2024 e| 11/14/2024 l| CATO-PARK m| UP-ANNEX n| 2 q| 1 r| Y s| Y t| PERIODICAL u| 3/4/2003 x| D z| 2611 0| 0101 1| 023
949			a| QC176.A1I3 v.38 no.1-6 2003 w| LCPER c| 1 i| 26110101024 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 12/5/2003 x| D z| 2611 0| 0101 1| 024
949			a| QC176.A1I3 v.38 no.7-12 2003 w| LCPER c| 1 i| 26110101025 d| 11/29/2004 e| 9/23/2004 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 9/7/2004 x| D z| 2611 0| 0101 1| 025
949			a| QC176.A1I3 v.39 no.1-6 2004 w| LCPER c| 1 i| 26110101026 d| 11/29/2004 l| CATO-PARK m| UP-ANNEX q| 1 r| Y s| Y t| PERIODICAL u| 9/7/2004 x| D z| 2611 0| 0101 1| 026
949			a| QC176.A1I3 v.39 no.7-9 2004 w| LCPER c| 1 i| 26110101027 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/22/2005 x| D z| 2611 0| 0101 1| 027
949			a| QC176.A1I3 v.39 no.10-12 2004 w| LCPER c| 1 i| 26110101028 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/22/2005 x| D z| 2611 0| 0101 1| 028
949			a| QC176.A1I3 v.40 no.1-3 2005 w| LCPER c| 1 i| 26110101029 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/22/2005 x| D z| 2611 0| 0101 1| 029
949			a| QC176.A1I3 v.40 no.4-6 2005 w| LCPER c| 1 i| 26110101030 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 9/22/2005 x| D z| 2611 0| 0101 1| 030
949			a| QC176.A1I3 v.40 no.7-9 2005 w| LCPER c| 1 i| 26110101031 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 7/25/2006 x| D z| 2611 0| 0101 1| 031
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949			a| QC176.A1I3 v.27 no.1-3 1992 w| LCPER c| 1 i| 26090101019 l| CATO-PARK m| UP-ANNEX r| Y s| Y t| PERIODICAL u| 6/19/2002 x| D z| 2609 0| 0101 1| 019
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866		0	8| 0 a| v.15(1980)-v.34(1999)
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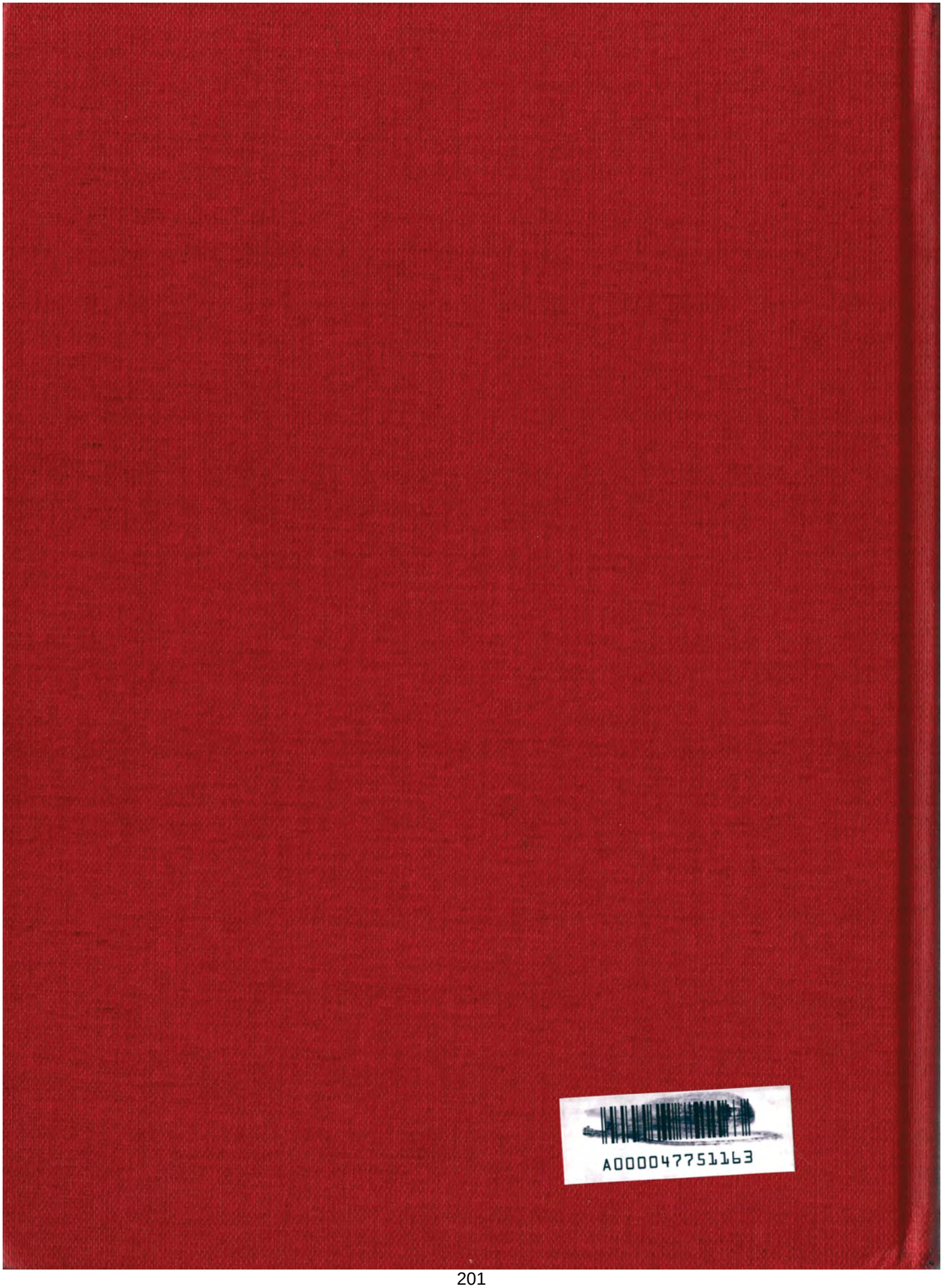
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The MICROMIXER: A Highly Linear Variant of the Gilbert Mixer Using a Bisymmetric Class-AB Input Stage

Barrie Gilbert, *Fellow, IEEE*

***Abstract*—This paper outlines the basic theory of a development of the Gilbert mixer. The bipolar junction transistor (BJT) differential pair widely used as the RF input stage is replaced by a bisymmetric Class-AB topology based on translinear principles. It does not have inherent gain compression, affording a greatly extended signal capacity. The linearity of variants of the basic form is excellent, providing two-tone intermodulation intercepts as high as +30 dBm, without the expenditure of high bias currents. It can operate on supplies as low as 2.2 V, with a power consumption of under 5 mW. The input impedance of this mixer is accurately controllable (typically 50 Ω) and provides a true broadband match. The noise figure depends on design details and is generally not as low as in mixers specifically optimized for noise performance, although acceptable for many receiver applications. Inductively degenerated variants can be tuned to a narrowband match at microwave frequencies and provide full-mixing SSB noise figures as low as 6.5 dB. Practical realizations are in use in applications to 1.9 GHz.**

***Index Terms*— Active mixers, Class-AB RF cells, linear transconductance, microwave mixers, modulation.**

I. Introduction

MIXERS have for decades played an indispensable role in communications systems as frequency-translation devices. At high microwave frequencies, rudimentary mixers based on a single diode are used. Below 1 GHz, discrete diode- and FET-ring mixers, various single-transistor forms (bipolar, MOS, and GaAs), and dual-gate MOSFET types are very much in evidence. Systems integrated monolithically often use a topology called the *Gilbert mixer*,[1] which dates to the mid-1960's. Its RF input stage, usually a simple differential pair (sometimes using emitter degeneration in the bipolar case) sets fundamental limits to the attainable dynamic range. This and other limitations of the standard form are reviewed in Section II.

The small-signal linearity of this input stage, and thus the third-order intercept, can be greatly improved using several techniques, notably, the multi-tanh doublet and triplet [1]. However, the 1-dB gain compression point still falls short of what may be required in handling large input signals without significant intermodulation. Further, these RF stages do not provide an accurate match to the source, even when using various types of impedance-transformation methods.

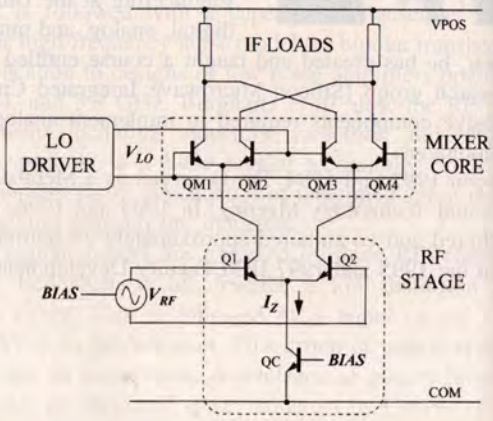


Fig. 1. Main elements of the standard form of the Gilbert mixer.

Accordingly, in Section III of this paper we present a basic topology, dubbed the MICROMIXER for reference purposes [2], [3]. It follows the general form of the Gilbert mixer, except for the use of a bisymmetric Class-AB RF stage. This provides a well-defined matching impedance and much lower input-related nonlinearity. There is no gain compression: rather, the gain increases at high input levels. Section IV presents ways to further improve the linearity and large-signal matching through the use of optimal resistive and inductive padding. These techniques provide exceptionally high intermodulation intercepts. This section also discusses suitable biasing means.

II. Background

Fig. 1 shows the main elements of the *standard form* of a Gilbert mixer. The inherently balanced structure and the use of differential-mode signals is apparent. Mixers of this sort have been widely implemented in silicon IC's and more recently using GaAs MESFET's, SiGe or GaAs HBT's, or MOS devices. While this paper discusses silicon bipolar embodiments, it will be apparent that other technologies may be utilized, and in the case of SiGe HBT, with no modification to the theory.

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[1] Prior art by H. E. Jones was discovered following a patent application by the author for what is now called a Gilbert mixer, but that invention differed in several ways from the mixer shown in Fig. 1, having been developed as a "synchronous demodulator," and many of the claims dealt with its various auxiliary details. Nevertheless, credit must be given to Jones for having been the first to patent this basic form.

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The actual mixing process—ideally, pure biphase multiplication—is implemented in the current-steering cell, QM1–QM4, the *mixer core*. This is driven by V_{LO}, the differential-mode local oscillator (LO) voltage at its bases, typically about 100 mV in amplitude, which is arranged to have a suitable common-mode level. The IF output is produced at its collectors in differential current-mode form and is converted to a voltage at the IF load, whose impedance usually is chosen to provide maximum IF power consistent with the voltage swing range allowable at the collectors, with compression considerations in mind. Underneath this is the *RF stage*, comprising Q1 and Q2 biased by current-source QC. The RF voltage-mode signal is converted to differential current-mode form by this transconductance stage and presented to the common-emitter nodes of the mixer core. The noise and linearity of the RF stage are crucial to mixer performance. A useful aspect of this cell is that, in the absence of emitter degeneration, the bias current I_Z may be used to precisely control the conversion gain.

The focus of this paper will be on circuit cells that replace the Class-A (limited range) type of RF stage of the standard form with a Class-AB cell, which imposes basically no limitations on the maximum input amplitude. The combination of these RF input cells with the mixer core of the standard form has been named a MICROMIXER. Though our emphasis here is on the fundamentals, practical realizations will be constrained by the finite supply voltages (which, among other things, set a limit on the permissible IF swing), the limited current-handling capacity in the active devices (determined largely by the SPICE parameters IKF and RC), and the input compression levels of the following IF stage or second mixer.

A. Limitations of the Standard Form

The upper extent of the dynamic range is conventionally defined[2] by the 1 dB-compression point (usually expressed in power form, P_{1dB}), which bounds the mixer's capacity to cope with large signal amplitudes, while extrapolated intermodulation intercepts, notably, the two-tone third-harmonic intercept, I2P3, provide a basis for the calculation of the intermodulation in a complete signal chain. These metrics are notoriously misleading. Most modern RF stages do not conform to classical ideas about distortion, in particular, the notion that it is generated by an essentially *cubic* nonlinearity. Thus, the I2P3 is a function of the test level and may even improve at high input levels due to distortion cancellation. Further, the gain may actually increase again above the P_{1dB} point. The 1-dB compression point of the MICROMIXER will often be determined by limitations on the output (IF) signal-amplitude, rather than by the RF stage.

The input port of the mixer shown in Fig. 1 does not accurately match the source, since its impedance is fairly high and rather poorly controlled, being a function of the HF beta. On the other hand, the simpler grounded-base stage sometimes used in the singly-balanced mixer form, or a differential grounded-base input (often driven via a balun) can provide input matching, which may be quite precise for small signals near the sensitivity limit.[3] However, this match rapidly deteriorates for large signals, contributing to mismatch-related nonlinearity.

The lower reaches of the dynamic range are constrained by the input-referred wideband noise, usually expressed in terms of noise figure. This too can be a misleading indicator when input matching is imperfect. Additional noise due to the switching of the four-transistor core and spectrum folding (notably image noise) must also be considered. Though there are many distinctly different noise mechanisms, their separate identity is often lost in practical measurements. In the design of monolithic mixers, it is important to understand, and thereby control, these noise sources individually.

Mixer conversion gain is also an important parameter. This impacts the required noise and signal-handling performance of the subsequent first IF amplifier stage. The nonmixing ("amplifier-mode") gain, exhibited when the mixer core is put into a simple "cascode" state by application of a large dc bias at the LO input, is determined by the ratio of the IF load impedance Z_{IF} to the input matching impedance Z_{IN}, and can be more rapidly determined in preliminary simulation studies than the mixing conversion gain, which will be approximately 4 dB ($\pi/2$) below the nonmixing gain, assuming that the core is operating in an essentially binary (sign-switching) fashion.

B. Signal Capacity of a BJT Pair

Consider the RF stage in Fig. 1. It is well known that the dc transfer characteristic of a simple bipolar junction transistor (BJT) differential pair is a hyperbolic tangent function. The voltage input V_{RF} may be expressed by the normalized variable $u = V_{RF}/2V_T$. The incremental gain is the derivative of the $\tanh(u)$ function, and has the form $G(u) = G_0\mathrm{sech}^2(u)$, where G_0 is the peak gain, which occurs when $V_{RF} = 0$. $G(u)$ is 10% lower than G_0 for a dc input $V_{RF} \approx 17$ mV at a temperature[4] of 300 K ($u = 0.327$). This characteristic voltage is proportional to absolute temperature (PTAT); to remind us of that, we will write the value as 17 mVP. Note that it does not depend on the bias current I_Z.

The third harmonic distortion, and thus the simple third-order intercept PH_3 can be found as follows. Let u represent the normalized amplitude $E/2V_T$ of a sinusoid RF input $E\sin\omega t$. Using a truncated power-series expansion for tanh we can write

$$\tanh(u\sin\omega t) \approx u\sin\omega t - (u\sin\omega t)^3/3\cdots$$
$$= u(1-u^2/4)\sin\omega t + (u^3/12)\sin 3\omega t. \quad (1)$$

The output of the RF stage comprises a fundamental term of relative magnitude $H_1 = u(1-u^2/4)$ and the third harmonic, $H_3 = u^3/12$. For a "test" input of $u = 0.01$ (that is, $E = 0.01 * 51.7$ mV $= 517$ μV), $H_1 = 9.999\,75 \times 10^{-3}$,

[2] Throughout this paper we will assume that these figures are referred to the *input* of the mixer, since this is where the fundamental nonlinearity arises for these structures; incidental compression may or may not occur at the IF load.

[3] Depending on the accuracy with which the bias current can be controlled, thus directly on the resistor technology.

[4] In considering operation over a wide temperature range, it is important to remember that most mixer parameters (gain-compression point, intermodulation intercepts, noise figure, etc.) are fundamentally strong functions of temperature.

while $H_3 = 83.3 \times 10^{-9}$, which is 101.6 dB lower. Expressed as a power in 50 Ω, a sine amplitude of 517 μV corresponds to −55.7 dBm, so the PH_3 occurs at −4.9 dBm. An HD3 of −40 dBc (1%) is generated by an input of about 18 mVP (−24.9 dBm re. 50 Ω).

We can determine the 1-dB compression point by setting $(1 - u^2/4) = 10^{-1/20}$, yielding $u = 0.66$. This corresponds to an amplitude of 34 mVP, or −19.35 dBm. Using a higher order expansion for the tanh function, we find $u = 0.718$, corresponding to an input of 37 mVP, or an input power of −18.6 dBm (the P_{1dB}) *if* the input were matched to 50 Ω. Of course, in the standard form of the Gilbert mixer, the Z_{IN} will be much higher. When the input is matched to the source (and this can only be approximate) through an impedance transformation, the P1 dB will be considerably lower.

C. Noise in the BJT Pair

In order to compare the fundamental noise performance of the MICROMIXER, we will further examine the RF stage of Fig. 1. For an ideal BJT, having no ohmic resistances, all the input noise would be generated by shot-noise processes. For the differential pair it is readily shown [1] that the collector noise currents $\sqrt{qI_Z}$ acting on the r_e's of $2V_T/I_Z$ generate an equivalent voltage noise spectral density (NSD) of

$$E_{SN} = \frac{0.925 \text{ nV}/\sqrt{\text{Hz}}}{\sqrt{I_Z}} \quad \text{at } T = 300 \text{ K} \tag{2}$$

where I_Z is expressed in milliamps. Thus, the *short-circuit* input voltage noise of the BJT pair can be lowered in only one way: by increasing the bias current I_Z. There are two practical limits to how far the noise can be reduced by this means. First, there will often be constraints on power expenditure: to halve the noise voltage requires quadrupling the bias current. Second, above a certain value, another source of noise becomes troublesome, namely, that due to the base currents of Q1 and Q2 flowing in the source impedance, Z_S, which may itself be purely reactive, that is, noise-free.[5]

The ac base current noise for a single transistor operating at a collector current of I_C is $(\sqrt{2qI_C})/\beta(\omega)$, where $\beta(\omega)$ is beta of the transistor at some frequency of interest. The resulting voltage noise is therefore $(Z_S\sqrt{2qI_C})/\beta(\omega)$, which is seen to *increase* with the square-root of bias current. It is well known that for a given Z_S and $\beta(\omega)$ there will be an optimal value of I_C. The shot noise in the current-source transistor is not usually problematical, provided that the IF outputs are processed as a *differential* signal; this noise is common-mode and causes only an inconsequential modulation of the g_m. However, this noise becomes extremely troublesome when only one of the two IF outputs are used (single-sided loading). It can also be translated into the IF band by a strong blocking signal, sometimes posing a more important limitation to receiver sensitivity than intermodulation effects [6].

[5]If the source is a real resistance of, say, 50 Ω, the voltage noise induced by the base-current shot noise will calculate the same, but we then need to also include the resistor noise.

D. Emitter Degeneration

The linear range of the basic BJT differential pair in the RF stage is often extended by the addition of emitter degeneration resistors. These also introduce noise, so the question arises as to whether the overall dynamic range can be improved. A study of this issue [1] shows a theoretical improvement is possible, by an amount

$$20 \lg t \frac{(1 + 1.7\sigma)}{\sqrt{(1 + 2\sigma)}} \text{ dB} \tag{3}$$

where $\sigma = I_Z R_E / 2V_T$ and R_E is the resistor added into each emitter. For example, let $\sigma = 10$ and $I_Z = 1$ mAP, requiring $R_E = 517$ Ω. The input-short-circuited noise spectral-density would be up from 0.925 nV/√Hz to 4.25 nV/√Hz, a factor of 4.6, while the V_{1dB} would be raised from 37 mVP to about 663 mVP, a factor of 18.

Thus, there is nearly a 12-dB improvement in dynamic range under these conditions. The effective input impedance of the RF stage is about $2\beta(\omega)(2R_E + 4V_T/I_Z)$, higher than before, making noise-matching even more difficult. The use of inductive degeneration is an obvious possibility in narrowband applications, without a noise penalty. Such also serves to transform the input impedance to an essentially resistive form, at frequencies where the ac beta is essentially f/f_T. Note, however, that the linear dependence of the g_m to the bias current of the RF stage in the standard form, useful in realizing variable-gain mixers, is invalidated by all forms of degeneration.

E. Multi-tanh Techniques

As noted earlier, the incremental g_m of a BJT differential pair varies considerably with the instantaneous voltage between the bases. Emitter degeneration reduces this dependence, but does not result in exactly constant incremental gain. A different linearizing technique uses the multi-tanh principle [1]. It can exhibit very low distortion for moderate signal amplitudes and provide an extended V_{1dB} while the noise figure increases only slightly and the variable-gain capability is preserved. Only the briefest review is appropriate here.

The basic multi-tanh doublet uses two differential pairs, with opposing emitter-area ratios of A, which introduce an offset voltage[6] of $\pm V_T \log A$. The offsets split the two tanh functions apart, and, with the correct choice of A, the resulting composite transfer function can exhibit a region close to $V_{RF} = 0$ over which the incremental gain is essentially flat, resulting in essentially zero distortion for moderate inputs. It has been shown [5] that this unique condition occurs for $A = 3.732$. The integer ratio 15 : 4 (3.75) is close, and may be a good choice, since a low-noise RF stage will probably use multistripe transistor geometries (15e and 4e) to achieve low values of $r_{bb'}$. If we measure the dynamic range in terms of the ratio of the V_{1dB} to the total input-referred noise-spectral density, we find that it is improved by nearly 5 dB for $A = 4$.

[6]These offset voltages can be introduced in several other ways, for example using input emitter-followers with or without emitter resistances and PTAT biases (see [1]), but this method is convenient in a monolithic context.

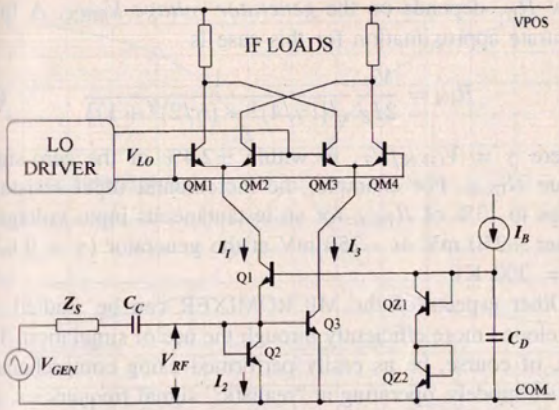


Fig. 2. The minimal MICROMIXER.

Many variants of the doublet have been used in mixer applications. For example, fixed-g_m realizations have been devised which combine the offset principle with emitter degeneration to achieve ultra-linear behavior. The idea can be extended to three (or more) pairs of transistors; the multi-tanh triplet is a very useful cell, providing further extension in the linear range. But the extension in V_{1dB} comes about only slowly with increasing complexity. Furthermore, none of these variants readily match to 50 Ω and require impedance transformation at their input.

III. The Basic Micromixer

The MICROMIXER uses a quite different approach to extending the linear range. The mixer core is identical to that of the standard Gilbert mixer. The important differences lie in the RF stage and the way it handles large signal amplitudes. Fig. 2 shows the circuit in its minimal form. Q1 can be viewed as a grounded-base stage. It delivers its output I_1 to the mixer pair QM1–QM2 in-phase. It can, *in principle*, handle unlimited amounts of current during large *negative* excursions of V_{GEN}. On the other hand, the current-mirror subcell Q2–Q3 can handle essentially unlimited amounts of current during *positive* excursions of V_{GEN} both at its input node and at its inverted-phase current output I_3, which drives QM3–QM4. Acting together, these two subcells provide an overall transfer characteristic which is symmetrical to both positive and negative inputs, and which is *in principle* not limited by the choice of bias level. The differential current output $I_1 - I_3$ is linear with I_{RF}, although, as we shall see, the individual currents are quite nonlinear.

A. Biasing and Small-Signal Behavior

To assess the fundamental *shape* of the behavior, we will assume ideal transistors; greater realism can be added later, in progressive layers. Thus, at this point, we will conveniently ignore base currents. The adjunct branch comprising QZ1 and QZ2 is biased by I_B. The bias decoupling capacitor C_D provides a low-impedance ac ground for the base of Q1 and ensures that the HF bias noise is suppressed.

The translinear principle [4] states that, in a closed loop containing an equal number of clockwise-facing and counter-clockwise-facing junctions, obeying an ideal exponential law, the product of the current-densities in each direction is equal. Applied to Fig. 2, we find that

$$I_Z^2/(A_1A_2) = I_B^2/(A_{Z1}A_{Z2}) \tag{4}$$

where I_Z is the zero-signal bias current in Q1–Q3, and A_K is the emitter area of transistor Q_K. Fairly large transistors will be used for Q1–Q3 in order to minimize Johnson noise. If we assume their emitter area is M times that of QZ1 and QZ2, the quiescent bias in the RF stage will be simply $I_Z = MI_B$. The small-signal input resistance is the parallel sum of the r_e's of Q1 and Q2, which are each V_T/I_Z. It follows that the incremental input resistance is

$$R_{IN} = \frac{V_T}{2I_Z}. \tag{5}$$

For a 50-Ω input resistance, the unique value of $I_Z = 258.5\ \mu$A must be used. Because of its pervasive importance, we will name this bias value I_{Z0}. To maintain a given R_{IN} over a wide temperature range, the bias currents should be PTAT, although closer analysis will show that some more subtle shaping should be used to compensate for such device parameters as dc beta and junction resistances. The bias will often be generated by a delta-V_{BE} cell and converted to a current by a resistor therein, whose temperature-coefficient immediately becomes that of R_{IN}.

The noise for the ideal case can be found by simply combining the shot-noise components in Q1–Q3. Expressed as a current, these are found to sum to

$$I_{SN} = \sqrt{(3/2)}\sqrt{2qI_Z} = \sqrt{3qI_Z}. \tag{6}$$

Assuming the source resistance R_S is matched directly by an equal incremental input resistance of R_{IN} given by (5), the total input noise voltage due to the input cell is

$$E_{SN} = 2R_{IN}I_{SN} = \frac{V_T}{I_Z}\sqrt{3qI_Z} = V_T\sqrt{(3q/I_Z)} \tag{7}$$

which evaluates to

$$E_{SN} = \frac{0.566\ \text{nV}/\sqrt{\text{Hz}}}{\sqrt{I_Z}} \quad \text{at } T = 300\ \text{K} \tag{8}$$

when I_Z is expressed in mA. For $I_Z = I_{Z0} = 258.5\ \mu$A, this amounts to 1.114 nV/$\sqrt{\text{Hz}}$, to which we must yet add the Johnson noise of the source, which is 0.912 nV/$\sqrt{\text{Hz}}$ for the 50-Ω case, resulting in a total generator-referred noise of 1.44 nV/$\sqrt{\text{Hz}}$. This corresponds to a nonmixing noise figure of 3.96 dB, a value which is easily shown to be independent

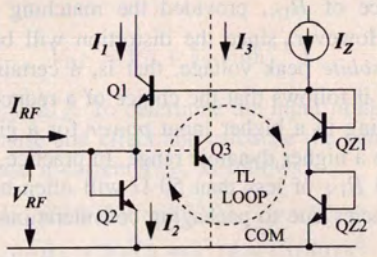


Fig. 3. Simplified input circuit.

of the choice of R_{IN}, provided the matching condition is preserved. However, since the distortion will be a function of some *absolute* peak voltage, that is, a certain number of units of V_T, it follows that the choice of a reduced R_{IN}, say, 25 Ω, resulting in a higher input *power* for a given voltage, will result in a higher dynamic range. In practice, maintaining a broadband R_{IN} of less than 50 Ω will often be difficult at high frequencies due to packaging considerations.

B. Large-Signal Behavior

We can begin an exploration of the large signal behavior of this cell by considering first its response to a pure current drive I_{RF} applied to the input node. Fig. 3 shows the main translinear loop[7] embracing Q1, Q2, QZ1, and QZ2. To simplify this analysis, without any loss of generality, we can assume that all transistors are the same size and the primary bias current is now I_Z. In general, the input current will cause the collector current of Q1 to assume some value $I_1 \neq I_Z$, while I_2 must be simply $I_1 + I_{RF}$.

Applying the translinear principle to this loop, we have

$$I_Z I_Z = I_1 I_2 = I_1(I_1 + I_{RF}). \tag{9}$$

The solution can be expressed most compactly by defining a modulation factor $\lambda = I_{RF}/2I_Z$. We find

$$I_1 = I_Z\{\sqrt{(\lambda^2+1)} - \lambda\} \tag{10a}$$

$$I_2 = I_Z\{\sqrt{(\lambda^2+1)} + \lambda\}. \tag{10b}$$

Note that λ may be of either polarity and is not in principle bounded by the value of I_Z. These currents are individually nonlinear, as must be the case for any Class-AB circuit. However, provided that the current mirror section (Q2–Q3 in Fig. 2) is linear, and assuming otherwise ideal devices, the differential drive to the mixer core is

$$I_1 - I_3 = 2\lambda I_Z = I_{RF}. \tag{11}$$

The voltage at the RF input node is

$$\begin{aligned} V_{RF} &= V_{BEZ} + V_T \log(I_{C2}/I_Z) \\ &= V_{BEZ} + V_T \log\{\sqrt{(\lambda^2+1)} + \lambda\} \\ &= V_{BEZ} + V_T \sinh^{-1}\lambda \end{aligned} \tag{12}$$

where V_{BEZ} is the base-emitter voltage at the quiescent current I_Z. It follows that the large-signal incremental input resistance is

$$R_{IN}(\lambda) = \frac{V_T}{2I_Z}\frac{1}{\sqrt{(\lambda^2+1)}}. \tag{13}$$

This predicts that for a signal current I_{RF} equal in magnitude to three times the quiescent bias, R_{IN} will be only 10% of its zero-signal value. The analysis becomes transcendental as soon as the source resistance is included, in seeking to determine how R_{IN} depends on the *generator voltage* V_{GEN}. A fairly accurate approximation for this case is

$$R_{IN} = \frac{V_T}{2I_Z}\frac{1}{\sqrt{\{(\gamma/4)^4 + (\gamma/2)^2 + 1\}}} \tag{14}$$

where $\gamma = V_{GEN}/V_T$, to within ±2.4% of the zero-signal value R_{IN_0}. For example, the incremental input resistance drops to 13% of R_{IN_0} for an instantaneous input voltage of either +250 mV or −250 mV at the generator ($\gamma = 9.67$ at $T = 300$ K).

Other aspects of the MICROMIXER can be studied and developed more efficiently through the use of simulation. This can, of course, be as easily performed using comprehensive device models, operating at "realistic" signal frequencies, and can include all package parasitics and numerous other practical complications. But our first objective remains to explore the *basic personality* of these cells, and it will be instructive, for the present, to continue to use highly idealized translinear models.[8]

C. Swept-V_{GEN} Exploration

For the simulation studies, the high side of V_{GEN} is coupled directly to the input node via a source resistance R_S (that is, C_C is shorted) and the bias voltage at node B is buffered by an ideal voltage-follower to which the "low" side of V_{GEN} is connected. Provided that the easy condition $A_1 A_{Z1} = A_2 A_{Z2}$ is met, the voltage at B will be equal to that at the mixer's input node when $V_{GEN} = 0$. A further detail is important in noise studies, namely, that node B, as well as the primary base node, must be well-decoupled by a grounded capacitor. Using this temporary artifice of a dc-coupled signal path, we can probe the incremental values of important circuit variables as a function of the instantaneous value of the RF voltage, V_{GEN}, which here refers to the dc (perturbation) value to which is added a zero-amplitude ac component.

Experimental techniques of this sort can generate valuable insights by exploring the large-signal properties of an RF cell. Here, V_{GEN} was swept while observing the incremental ac gain and input resistance and input-referred noise. The mixer core was "hung" in an extreme drive state ($V_{LO} = 200$ mV dc). The IF loading circuit was given an effective transimpedance of 100 Ω using noise-free resistors (Z-elements) of low value followed by an ideal differential-to-single-sided converter; this interim test scheme avoids compression at the IF load, which can be studied separately.

Fig. 4 shows some typical results using an arbitrary test frequency of 300 MHz. The incremental gain increases with the magnitude of V_{GEN} since for either polarity of input swing, the r_e of either Q1 or Q2 decreases. As noted above, at very high RF drive levels the incremental R_{IN} becomes asymptotic to zero, as either I_1 or I_2 becomes very high. Consequently, the incremental gain increases asymptotically toward +6 dB, suggesting that *this RF stage will not exhibit gain compression*, but rather an *expansion* in the main-carrier output at high drive levels. This is one of several unusual aspects of the

[7] It is interesting to note that this four-junction loop is identical to that found in a simple translinear multiplier cell, in vector arithmetic circuits, as the input stage of a common current-conveyor topology (using complementary devices), and even in the Class AB output stage found in numerous op-amp designs.

[8] This method of layered discovery and development, particularly well-suited to bipolar technologies, has been named *Foundation Design* by the author.

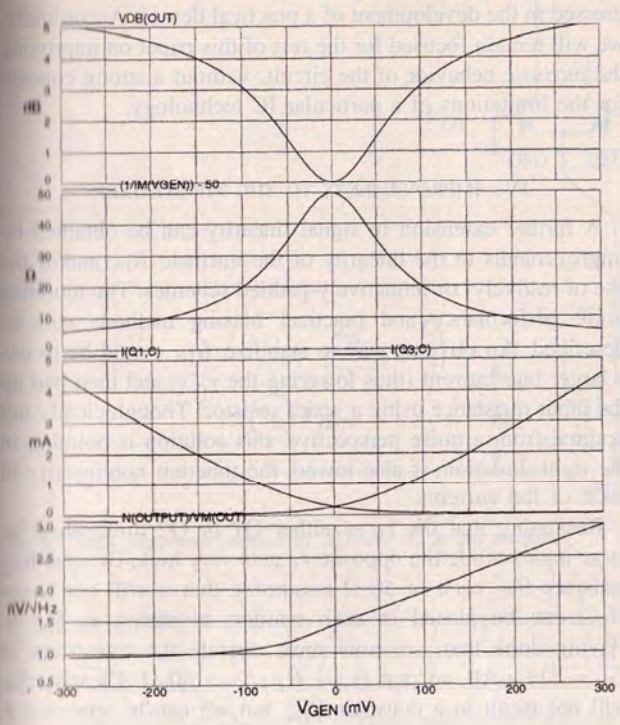


Fig. 4. Swept-V_{GEN} results for basic cell. Top to bottom: incremental gain; incremental R_{IN}; collector currents of Q_1, Q_3; input-referred noise.

MICROMIXER. The input-referred NSD for $V_{GEN} = 0$ is 1.44 nV/$\sqrt{\text{Hz}}$, as predicted by the first-order theory, but it varies asymmetrically with V_{GEN} for reasons given later. Relative to the noise of $R_S = 50\ \Omega$ (0.912 nV/$\sqrt{\text{Hz}}$), the amplifier-mode noise figure evaluates to $20\,\text{lgt}(1.44/0.921) = 3.96$ dB. Operating as a mixer,[9] folding and harmonic noise will raise the single sideband (SSB) noise figure to about 8 dB.

D. Distortion of the MICROMIXER

Fig. 4 also shows the currents I_1 and I_3. Their individual nonlinearity is apparent. When driven at very high input levels *only one* of the two outputs will be active at any time (that is, during the polarity reversals of the RF input). These signal components recombine in-phase at the IF output, after each has traversed *one half* of the mixer core. We need to consider how this might impact the overall mixer integrity.[10] It was shown above that the signal of importance—the algebraic difference in these two currents—is linear with respect to the input current I_{RF}. Thus, the signal distortion (for the idealized case) will be almost entirely due to the nonlinearity between V_{GEN} and I_{RF}. It is for this reason that the greatest attention is given in this paper to the linearity of R_{IN}.

We have already found that the voltage generated at the input V_{RF} can be expressed with reference to the fixed voltage V_B as

$$V_{RF} = V_B + V_T \sinh^{-1} \lambda \tag{12a}$$

where $\lambda = I_{RF}/2I_Z$. To determine the input nonlinearity, we can reverse cause and effect and calculate the value of V_{GEN} needed to cause a current I_{RF}, as follows:

$$\begin{aligned} V'_{GEN} &= I_{RF}R_S + V_T \sinh^{-1} \lambda \\ &= I_{RF}R_S + V_T\{\lambda + \lambda^3/6 + (3/40)\lambda^5 \cdots\} \\ &\approx I_{RF}R_S + V_T\lambda + V_T\lambda^3/6 \cdots . \end{aligned} \tag{15}$$

Now taking λ to have a sinusoidal waveform, and noting that for the matched condition $R_S = R_{IN} = V_T/2I_Z$, we find

$$V'_{GEN}/V_T = \{2\lambda - (\lambda^3/8)\} \sin \omega t + (\lambda^3/24) \sin 3\omega t. \tag{16}$$

The ratio of the third harmonic to the fundamental in V'_{GEN}, that is, the third harmonic distortion HD3, is thus approximately $\gamma^2/48$.

To a close approximation, the peak value of I_{RF} for a -30 dBm/50 Ω input is ± 200 μA. Thus, at $T = 300$ K, when $I_Z = I_{Z0} = 258.5$ μA, the peak value of λ is 0.387, and the theoretical HD3, which has not taken into account the many other distortion effects that will arise at high frequencies, evaluates to 3.1×10^{-3}, or -50.1 dBc, from which we can estimate that the simple third-harmonic intercept PH3 will be at about $-30 + (50.1/2) = -4.95$ dBm/50 Ω.

E. Large-Signal Measurements

Classical approaches to RF design and circuit analysis are based on the assumption that the active device parameters remain constant throughout the signal cycle; the perturbations in operating point caused by the signal are ignored. This assumption allows one to use small-signal modeling concepts, such as S-parameters. In practice, however, this naïve assumption is not valid in *any* mixer, which is inherently very nonlinear when treated in its entirety. In a Class-AB input structure, the "stable parameter" assumption is even less true. The intrinsic device speed when driven to low currents will be degraded, leading to nonlinear phase effects, which may result in a failure of the signal fragments to add correctly at the IF output. However, though clearly of concern, all mixers suffer from such large-signal aberrations. Thus, in the simple Class-A RF stage of the Fig. 1 mixer, Q1 and Q2 undergo a significant modulation in their dynamic parameters at high input levels. Using modern low-inertia devices at signal frequencies well below their maximum performance capabilities, these dynamic nonlinearities are often tolerable.

Fig. 5 shows what we will call the *harmonic signature* for the basic MICROMIXER,[11] for a single-tone 300 MHz input ranging from -30 dBm to $+15$ dBm, re. 50 Ω. The top panel shows the difference between the actual value (H_1) and the extrapolated value (EH_1) of the fundamental output on an expanded scale. As predicted from the swept-V_{GEN} results, it becomes too high for increasing input levels. At very high levels, where the average R_{IN} over each cycle drops to almost

[9] Neglecting the additional noise due to the switching action in the mixer core; see [1] for an analysis.

[10] Note in passing that the widely used singly balanced mixer, having an RF stage that is simply a grounded-base or grounded-emitter transistor, is not only very nonlinear but is completely missing one signal polarity in its output at very high drive levels.

[11] The small amount of incidental second-harmonic distortion has been omitted from these results for reasons of clarity.

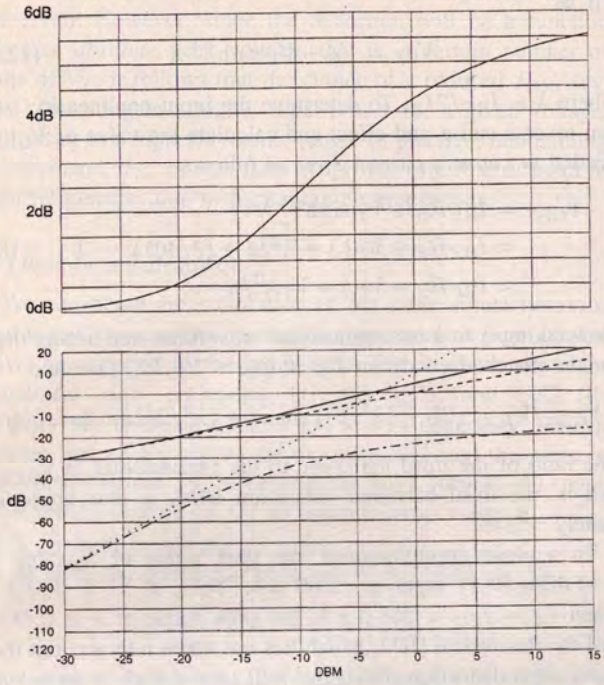


Fig. 5. The harmonic signature for the minimal MICROMIXER (I_Z = 258.5 μA). Top panel: Gain error of fundamental; bottom panel: fundamental, actual HD3, and extrapolations.

zero, the incremental gain doubles. It follows that we cannot define a P_{1dB}, unless we stretch the definition to mean a 1 dB gain *error* (either high *or* low), in which case, it occurs at -13 dBm.

The third harmonic component H_3 is well below the extrapolated line EH_3, and its magnitude relative to the fundamental actually *decreases* at high inputs. The simple third-harmonic intercept PH_3 is at -4.5 dBm, extrapolating from the -30 dBm level, where H_3 is -51 dBc. It is shown in [1] that, assuming a cubic nonlinearity, the input-referred two-tone third-order intermodulation intercept I2P3 is 4.8 dB below the single-tone intercept PH_3. This is a useful rule-of-thumb, allowing shorter simulation times in preliminary evaluations. Here, the predicted I2P3 is -9.3 dBm; however, actual two-tone measurements on Si and SiGe MICROMIXERs show considerably better values, for example, -3.7 dBm at 1.8 GHz.

As noted, the incremental input *resistance* R_{IN} of the MICROMIXER can be set to 50 Ω, or to higher or lower values by appropriate choice of bias current, and drops to very low values at large positive or negative excursions of the input voltage. In practice, the inertial aspects of the transistor will affect the input impedance Z_{IN} at frequencies above about 5% of the f_T of the transistor. Just as importantly, the package parasitics will play a major role in determining the actual input impedance in, say, L-Band operation. Attention must be given to the two loops involving a) input node $\rightarrow$ base of $Q_1 \rightarrow C_D \rightarrow$ ground return and b) input node $\rightarrow$ emitters of Q_2 and $Q_3 \rightarrow$ ground return.

These are well-known practical aspects of layout and packaging for microwave circuits, and it is assumed that whatever the final topology of the mixer, such issues need to be addressed in the development of a practical device. Accordingly, we will remain focused for the rest of this paper on improving the *intrinsic* behavior of the circuit, without a strong concern for the limitations of a particular IC technology.

IV. Improvements to the Micromixer

A further extension in signal linearity can be obtained by improvements to the linearity of the intrinsic R_{IN} and/or the use of restively- or inductively-padded schemes. The modified noise performance and practical biasing methods will be described. An obvious way to stabilize R_{IN} would be to use a larger bias current (thus lowering the r_e's) and then pad up the input resistance using a series resistor. Though clearly not optimal from a noise perspective, this solution is pointing in the right direction; it also lowers the inherent nonlinearity in each of the currents.

Reasoning that the r_e of either Q1 or Q2 diminishes for large inputs while the opposite r_e gets very high, two padding resistors R_P, each of 50 Ω (assuming that is still our target R_{IN}) can be placed in each emitter, as shown in Fig. 6. Having done that, we now must operate the transistors at $I_Z = 517$ μAP, so that $(r_e + R_P)/2 = 50$ Ω. Clearly, this will not result in a constant R_{IN}, but we can be sure that it will be precisely 50 Ω for arbitrarily large positive or negative values of V_{GEN} as well as for $V_{GEN} = 0$. The current mirror can now be converted to an emitter-degenerated form, which improves its accuracy and reduces the effect of shot noise. These resistors introduce a bias drop of $I_Z R_P$ (here, one V_T), and we need to add corresponding resistors in the bias branch.

The simulation results of Fig. 7 show that R_{IN} is 50 Ω for $V_{GEN} = 0$ and is again asymptotic to 50 Ω for very large instantaneous inputs (± 1 V), but it now peaks to 60.13 Ω at ± 210 mV. Such a modulation of R_{IN} is probably not catastrophic, though as we shall see very shortly, better solutions can readily be found. The gain now dips *down* by -0.83 dB (compare this to the *increase* seen in the minimal MICROMIXER) at this same value of V_{GEN} before creeping back up to 0 dB at very large inputs (rather than to +6 dB). This intriguing result suggests that there may be some intermediate padding arrangement which exhibits even more constant input impedance and gain over moderate ranges of V_{GEN}. The total input-referred zero-signal noise, including the resistive source $R_S = 50$ Ω, is up to about 1.64 nV/$\sqrt{\text{Hz}}$, so the amplifier-mode noise figure is 5.1 dB.

The harmonic signature for this case (Fig. 8) has some interesting artifacts. First, the gain at the fundamental frequency never drops below 0.55 dB of the ideal extrapolation, and at high inputs it is asymptotic to 0 dB. Once again, there is no 1-dB compression point, but neither is there any gain expansion. Second, the H_3 is lower than for the minimal MICROMIXER, resulting in a higher PH_3 of +7 dBm; the high-level H_3 is well below the extrapolation, so this figure may give a somewhat pessimistic view of the performance. There is a deep notch in H_3 close to 0 dBm.

A value of 50 Ω was used for R_P in conjunction with a bias current of $I_Z = 2I_{Z0} = 517$ μAP, since we could

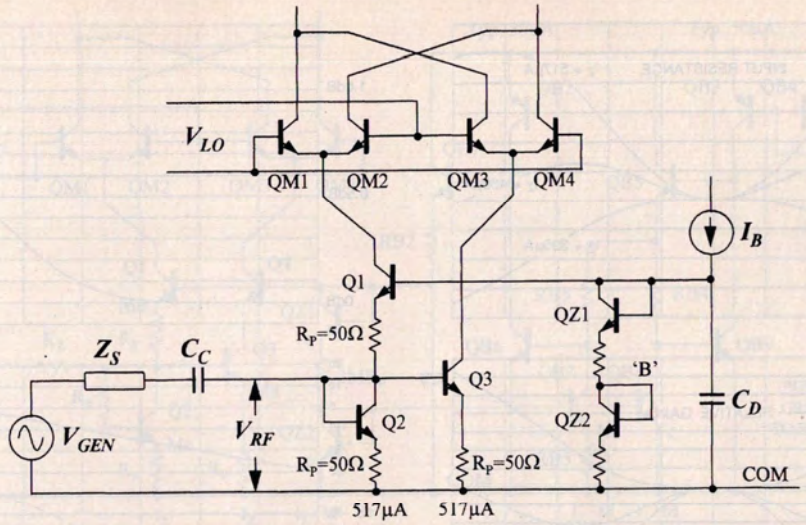


Fig. 6. Input impedance padded by addition of emitter resistors.

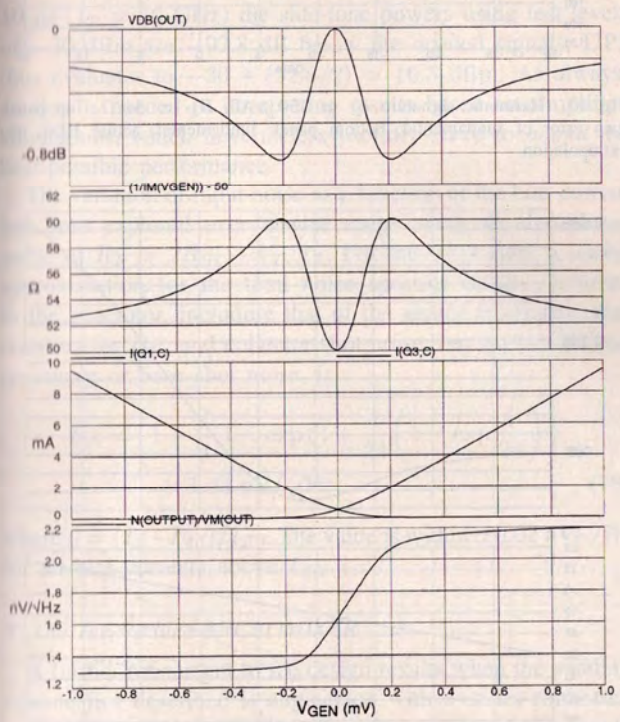


Fig. 7. Swept-V_{GEN} results for 50-Ω-padded MICROMIXER ($I_Z = 517\ \mu$A). Compare with Fig. 4.

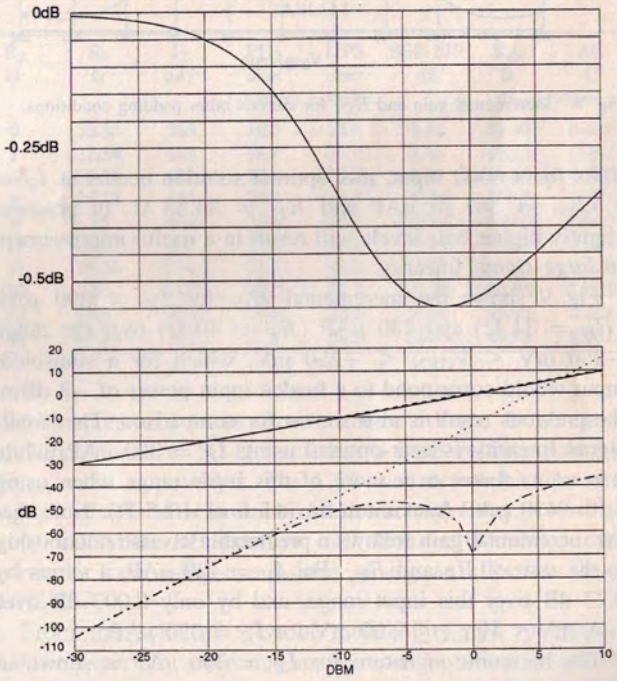


Fig. 8. Harmonic signature for the 50-Ω-padded MICROMIXER ($I_Z = 517\ \mu$A). Top panel: gain error of fundamental; bottom panel: fundamental, actual HD3, and extrapolation.

foresee that would result in the net R_{IN} at high drives being asymptotic to 50 Ω. But a moment's reflection shows that a *higher* value of R_P could be used, up to nearly 100 Ω for a 50-Ω match, by increasing I_Z *above* $2I_{Z0}$. Within the range $50\Omega \leq R_P \leq 100\ \Omega$, the higher bias currents might actually be useful in extending the bandwidth when using large (low-$r_{bb'}$) transistors. However, the higher bias currents require larger voltage drops across these resistors, which will eventually impact the minimum permissible supply voltage, and the noise figure worsens.

A. The Optimal MICROMIXER

We will now explore the alternative option, namely, to choose R_P *inside* the range 0 to 50 Ω, using an I_Z in the range I_{Z0} to $2I_{Z0}$ (258.5–517 μAP). It is easily shown that the derivative of the input resistance is uniquely zero (that is, conversion from the generator voltage to the signal current is perfectly linear) when a simple condition is met, namely

$$I_Z = \frac{3}{4}\frac{V_T}{R_{\mathrm{IN}}} \tag{17}$$

at which point the bias drop across each resistor is $V_T/2$.

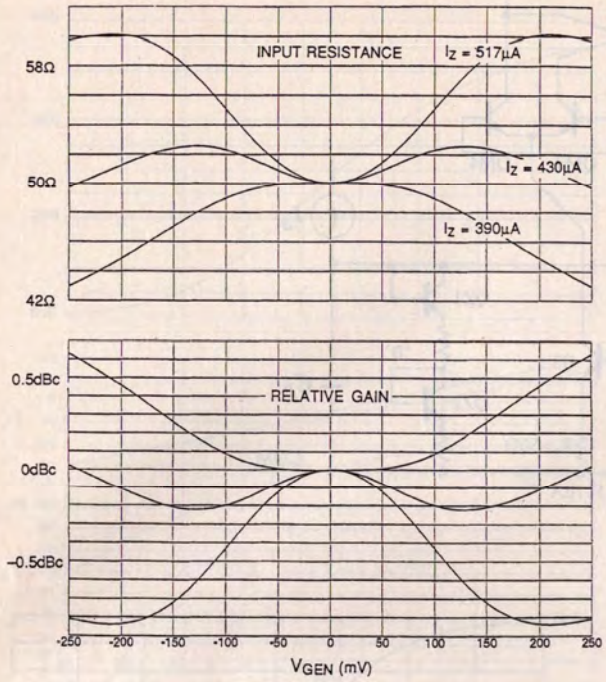


Fig. 9. Incremental gain and R_{IN} for various other padding conditions.

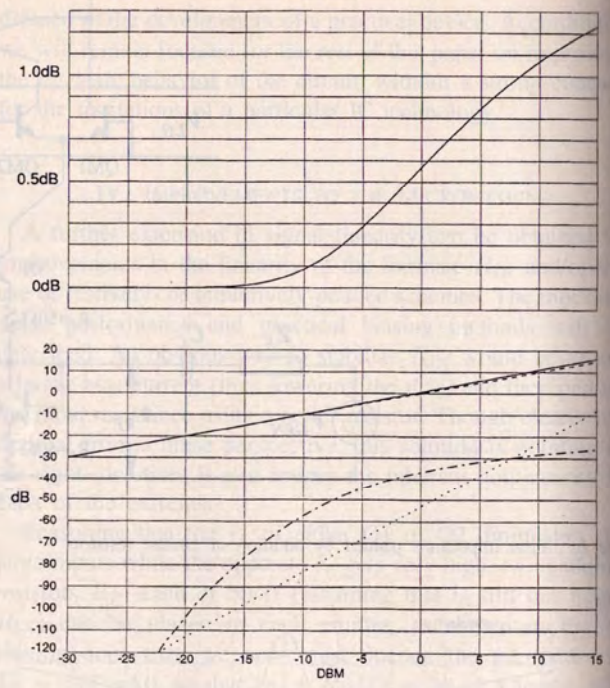


Fig. 10. Harmonic signature $I_Z = 390$ μAP, $R_P = 34$ Ω. Top panel: gain error of fundamental; bottom panel: fundamental, actual HD3, and extrapolation.

Thus for a 50-Ω input, this optimal solution occurs at $I_Z = 1.5\,I_{Z0} = 387.75$ μAP and $R_P = 33.33$ Ω. In practice, slightly higher bias levels will result in a useful improvement in *large-signal* linearity.

Fig. 9 shows the incremental R_{IN} for $I_Z = 390$ μAP ($R_P = 34$ Ω) and 430 μAP ($R_P = 40$ Ω) over the range -250 mV $\leq V_{GEN} \leq +250$ mV, which for a sinusoidal input would correspond to a loaded input power of -8 dBm; the previous result is also shown for comparison. The small-signal linearity is near-optimal using $I_Z = 390$ μAP, while it remains flatter over more of this input range when using $I_Z = 430$ μAP (maximum deviation of +2.5 Ω). Note that the incremental gain follows a predictable inverse relationship to the sum of R_S and R_{IN}. For $I_Z = 430$ μAP, it varies by 0.22 dB over this input range, and by only 0.003 dB over -50 mV $\leq V_{GEN} \leq +50$ mV for $I_Z = 390$ μAP.

The harmonic signature for $I_Z = 390$ μAP is shown in Fig. 10. Again there is no 1 dB gain compression point; instead, the gain increases to +1.2 dB at +15 dBm and is 0.57 dB high at 0 dBm. The H_3 is extremely low, being -98 dBc at -22 dBm, resulting in a PH_3 of +27 dBm. An unwelcome artifact of this response is that over the signal range -22 dBm to +7.5 dBm the H_3 now lies *above* the extrapolated line. Fig. 11 shows the results for $I_Z = 430$ μAP. The fundamental output is even more constant, dropping by only -0.12 dB at -9 dBm and rising to +0.63 dB at +15 dBm. The H_3 remains very low, now -78 dBc at -30 dBm, resulting in a PH_3 of +9 dBm. Furthermore, now both the H_2 (not shown) and H_3 always remain below the extrapolations, and the H_3 is notably lower than for the last case at high signal levels, being only -42 dBc at an input power of +15 dBm.

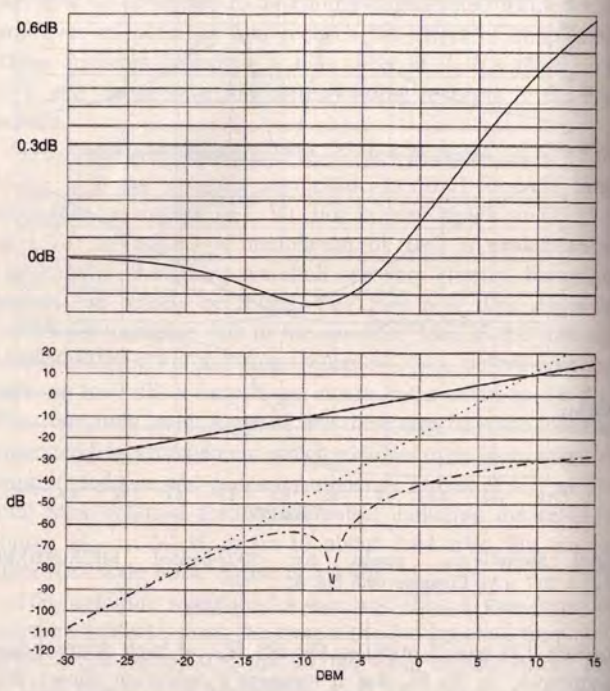


Fig. 11. Harmonic signature $I_Z = 430$ μAP, $R_P = 40$ Ω. Top panel: gain error of fundamental; bottom panel: fundamental, actual HD3, and extrapolation.

Numerous simulation studies have been carried out to explore the intermodulation properties of this cell using a two-tone test input. Using the "optimal" bias of 390 μAP, test tones of 320 MHz and 340 MHz and a transistor with a TF of

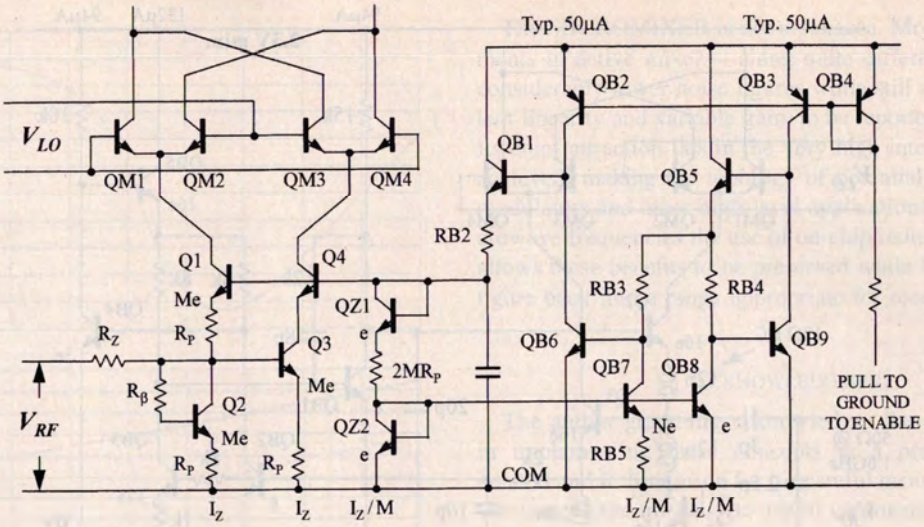


Fig. 12. The T-padded form and bias details.

10 ps (f_T = 16 GHz) the side-tone powers using test levels of −30 dBm are −92.8 dB below the wanted signals; I2P3 thus evaluates to $-30 + (92.8/2) = 16.5$ dBm. As always, caution is needed in interpreting results based on simplified simulations, which nevertheless usefully serve to *bound* the best-possible performance.

The variation of input noise as a function of the bias current has been explored over a wide range using an algorithmic value of $R_F = 2R_{IN} - V_T/I_Z$. For the 50-Ω case, a useful approximation for the total noise spectral density, referred to the generator, including that of the source resistance, real resistors for R_F, and collector shot noise, but excluding base resistance or base shot noise, is

$$E_N = \left\{1 + \frac{2}{9}(1 - \exp\xi) + \frac{1}{24}\left(1 - \exp\frac{\xi}{24}\right)\right\} \times 1.44 \text{ nV}/\sqrt{\text{Hz}} \quad (18)$$

where $\xi = (I_Z - I_{Z0})/I_{Z0}$. The value is within ±0.02 nV/$\sqrt{\text{Hz}}$ for all bias currents above I_{Z0}.

B. The Tee-Padded MICROMIXER

A further refinement to the design results when the padding scheme just described is augmented with a series-connected input resistor. The left-hand side of Fig. 12 shows this simple modification. The addition of R_Z alters the required value of R_P. Having chosen R_Z, considerable latitude remains in the choice of I_Z. Thus, the optimization space is rather large. The cascode Q4 is added to equalize the V_{CE} of Q2 and Q3; it also reduces the amount of LO voltage appearing at the emitters of QM3 and QM4 that couples back to the input. In practice, however, the incidental inequality of V_{CE} may help to recover some of the current gain in the mirror lost by reason of its finite ac beta, and the cascode may be contraindicated.

The approach used in studying this circuit has been to choose combinations that result in a null in the derivative $\partial G/\partial V_{GEN}$ at $V_{GEN} = 0$, that is, in flat gain versus instantaneous input voltage for small signals. Table I lists some

TABLE I

R_Z Ω	R_P Ω	I_Z μAP	PH_3 dBm (−30dBm)	I2P3 dBm (−30dBm)	SSB NF dB	R_{IN} Ω (V_{RF} = ±100mV)	ΔG dB
0	33.33	388	16.3	15.5	9.64	49.00	0.088
2	32.14	405	16.7	16.6	9.75	49.23	0.067
4	30.71	422	17.4	17.0	9.87	49.31	0.060
6	29.35	441	18.0	17.5	10.00	49.42	0.051
8	28	462	18.6	18.2	10.14	49.52	0.042
10	26.67	485	19.3	18.8	10.30	49.61	0.034
15	23.33	554	21.1	20.6	10.75	49.80	0.020
20	**20**	**647**	**23.3**	**22.4**	**11.25**	**49.90**	**0.008**
25	16.67	776	24.5	25.3	11.90	49.95	0.004
30	13.33	970	27.1	28.5	12.75	49.98	0.001

combinations and various performance criteria. In all cases an input match to 50 Ω (and thus a 0-dB relative gain) at $V_{GEN} = 0$ is provided. The I2P3 was determined for test signals of 320 MHz and 340 MHz, each of either −30 dBm (±10 mV at the RF input) or −10 dBm (±100 mV), in this particular case using a transistor having an effective f_T of 16 GHz.

From the point of view of realizability and robustness, we are especially interested in solutions resulting in resistor combinations that are integer multiples of a unit element. One in particular stands out, namely, I_Z = 647 μAP, $R_Z = R_P$ = 20 Ω. For this case, R_{IN} varies from 50 Ω at $V_{GEN} = 0$ and falls only slightly to 49.9 Ω at V_{GEN} = ±200 mV (V_{RF} = ±100 mV); the gain theoretically varies by only 0.008 dB. This points toward very linear performance as a mixer, as evidenced by the excellent two-tone (320/340 MHz) results. The noise figure in SSB full-mixing mode is a moderate 11.25 dB.

A practical biasing system is also shown on the right of Fig. 12. It is based on an all-NPN delta-V_{BE} (PTAT) cell [7] tightly integrated into the RF stage, resulting in precise biasing. In an optimal realization, all resistors would be thin-film, having good absolute accuracy and near-zero temperature-coefficient, for excellent control of R_{IN}. The core of this cell is

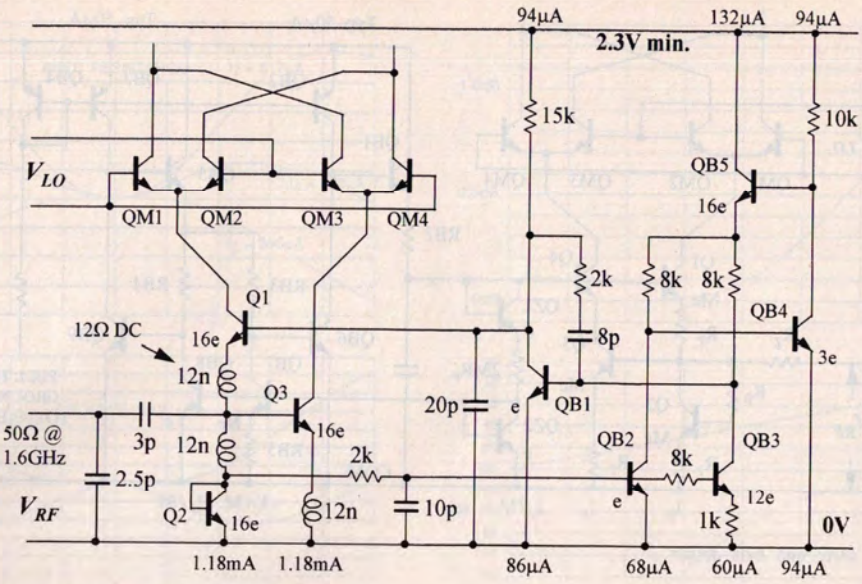


Fig. 13. L-band mixer using inductive degeneration.

QB7, QB8, and RB5. Loads RB3 and RB4 are equal. The dual-loop amplifier establishes $I_{C7} = I_{C8} = (V_T \log N)/R_{B5}$. The current-density in QB8 is replicated in QZ2, and becomes M times larger in Q1–Q4. Thus, $R_{IN} = R_Z + \{R_{B5}/M \log(N) + R_P\}/2$. The PNP transistors QB2–QB4 provide a cell-enable feature. They are entirely noncritical, operating at low currents, and may be lateral devices; they may be optionally replaced by resistors if the enable feature is not required.

Many subtle design issues remain. For example, we have noted the importance of cancellation of the individual nonlinearities of the two output currents I_1 and I_3, but not yet addressed the effect of the finite ac beta (which is often very low, being roughly f/f_T), particularly in the current mirror section. This is addressed in the circuit shown in Fig. 12 by the inclusion of the resistor R_β in the base of Q2, whose theoretical value should be $2V_T/I_Z$. This restores the overall unity ratio of the mirror, while it also slightly raises the input impedance of the mirror section, particularly at high frequencies, which has the further useful effect of compensating for the finite alpha of Q1. However, there is a significant noise penalty, and a lower value may be necessary to achieve a compromise between a reduction of beta-sensitivity and the increase in noise.

C. Microwave Variants

The use of monolithic inductors in place of the degeneration resistors R_F is clearly a useful alternative in microwave applications. A low Q is not a disadvantage here. Using typical metallization technologies, the series resistance is of the order of 1 Ω per nanohenry. Thus, the inductive reactance and resistance have the same magnitude at a frequency which is the solution of the equation $2\pi fx\ (\text{nH}) = x\ (\Omega)$, or, $f \approx 160$ MHz. Accordingly, these components remain essentially inductive above about 1 GHz. Note in passing that the metallization resistance is roughly PTAT, so the Johnson noise increases in direct proportion to temperature, not as the square root.

The component values shown in Fig. 13 provide a purely resistive input impedance of 50 Ω at 1.6 GHz, for the optimum bias current of 1.18 mAP, at which current-density the transistors used in these experiments exhibit an f_T of about 18 GHz. In this bias scheme the current in Q2 is set up by using it as the current-sensor in the loop enclosing the delta-V_{BE} cell, QB2–QB3. This method eliminates the effect of the inductor resistance. An RF filter (2 kΩ/10 pF) and beta compensation (the 8 kΩ in the base of QB3) are included. The bias loop needs special attention to HF compensation. This bias system can operate at supply voltages of under 2.5 V.

Slight compression is evident in the harmonic signature (Fig. 14): the fundamental dips to −0.93 dB at an input of about −2 dBm before rising again. The input-referred single-tone third-order intercept is at +10.2 dBm, and the noise-spectral-density is 1.22 nV/$\sqrt{\text{Hz}}$ for an amplifier-mode noise-figure of 2.6 dB.

Precise linearity matching of the separate sections handling the positive and negative input excursions will always be a critical factor in any Class-AB RF structure. It will be obvious that two of these RF stages may be combined in a differential manner to effect further improvement in linearity through a cancellation process based on symmetry and component matching. The input impedance—now measured between the two "floating" input nodes—may be readjusted to any desired value; the input port must now be driven differentially, typically using a balun. Both the noise spectral density and the signal handling capacity will increase. Further considerations relate to embedding this cell into an integrated circuit package, which brings with it numerous important complications arising from lead inductances and their mutual coupling, and the many parasitic capacitances associated with the input path, including those due to ESD devices. These and other issues lie

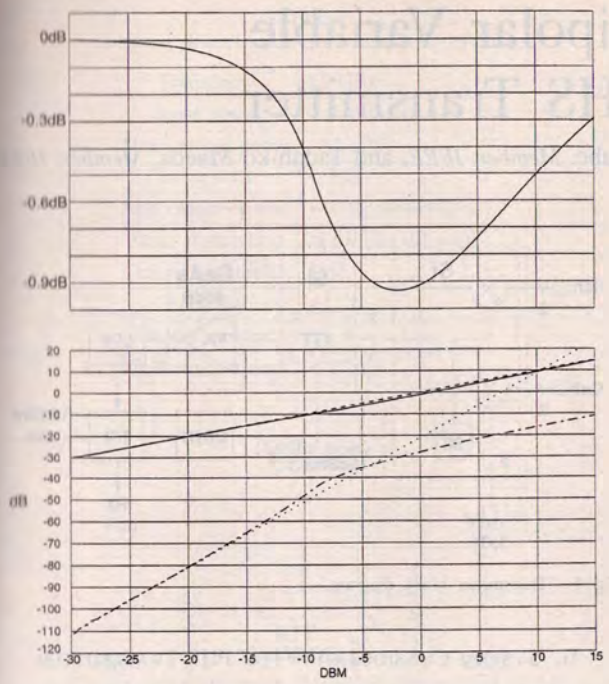


Fig. 14. Harmonic signature for the L-band variant ($I_Z = 1.18$ mA). Top panel: gain error of fundamental; bottom panel: fundamental, actual HD3, and extrapolation.

beyond the primary objective of this paper, which has been to outline the general conceptual and theoretical framework of the MICROMIXER and point to some new areas for development.

V. Conclusion

The MICROMIXER topology provides an accurate input impedance, high intermodulation intercepts, and an almost unlimited signal capacity at its input, arising from the use of a Class-AB topology, while maintaining acceptable noise performance. This paper has provided a brief overview of its potential. The results are based largely on simple models of the devices, in order to better compare the variants on a similar basis, without the coloration introduced by complex dynamic effects, and as an aid to the development of insights leading to improved topologies. It is clear that if the fundamentals are not right, there is little benefit in proceeding to the later steps of adding the greater realism captured in the full transistor model.

Nonetheless, for modern low-inertia transistors (that is, having few-picosecond transit times and few-femtofarad capacitances) operating at sensible bias currents, the "low frequency" predictions are reliable out to many hundreds of megahertz and still useful as a comparative tool in the microwave range. In practice, package parasitics, biasing-current errors, and instrumentation issues will have a much greater impact on determining mixer performance at microwave frequencies, provided that due care is taken in the design and layout of the monolithic circuit.

The MICROMIXER is not a panacea. More recent developments in active mixers—along quite different lines—provide considerably lower noise figures while still maintaining excellent linearity and variable gain, to be reported at a future time. Its chief attraction lies in the very high intercepts that can be achieved, making the topology of potential value in transmit modulators and other high-level applications. However, at microwave frequencies the use of on-chip inductive degeneration allows these benefits to be preserved while lowering the noise figure back into a range appropriate for receiver applications.

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The author gratefully acknowledges the work of G. Dawe in implementing these concepts in a practical monolithic context and R. Simonson for his careful measurements on early versions of the mixer. The useful comments of the reviewers have also been noted.

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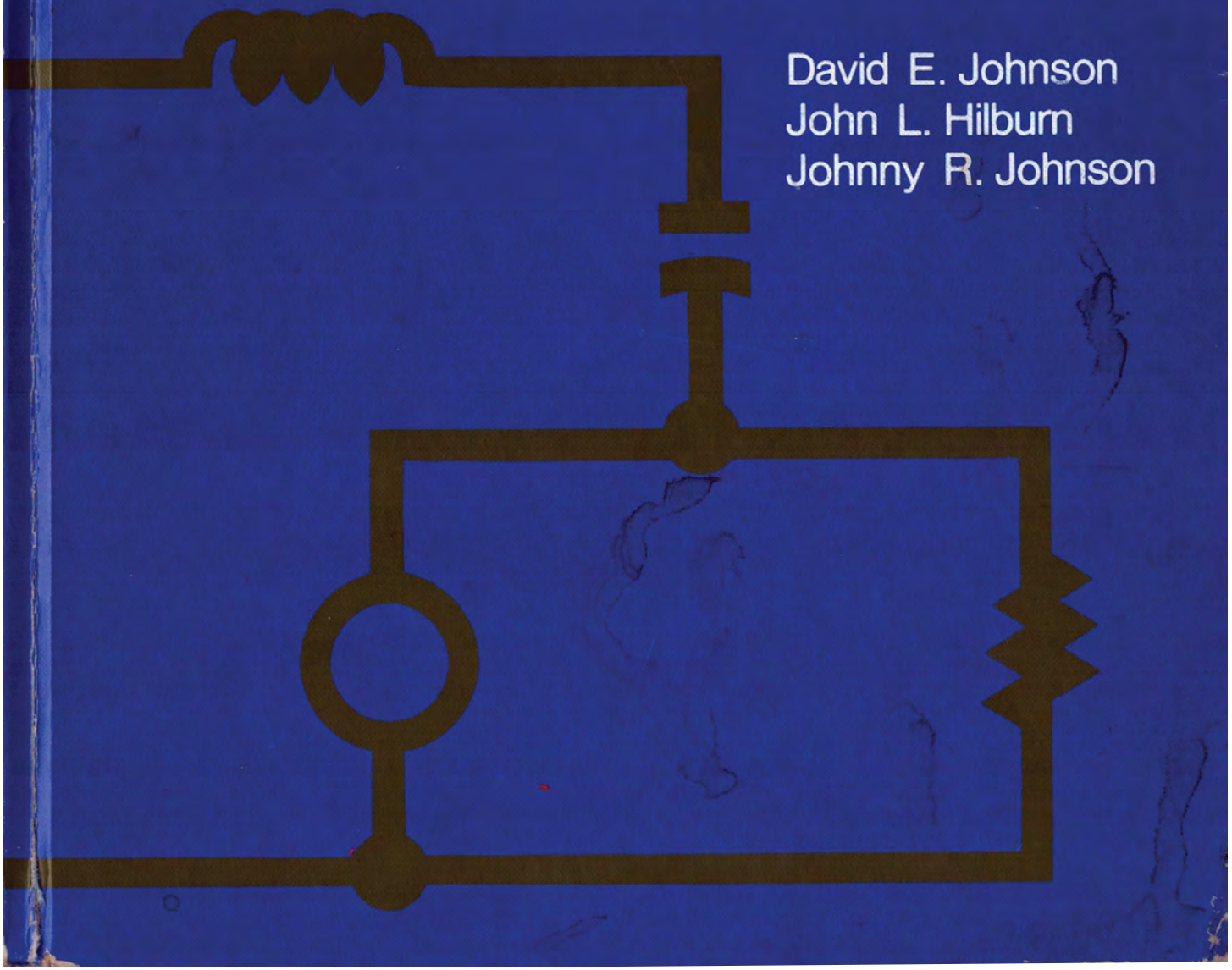
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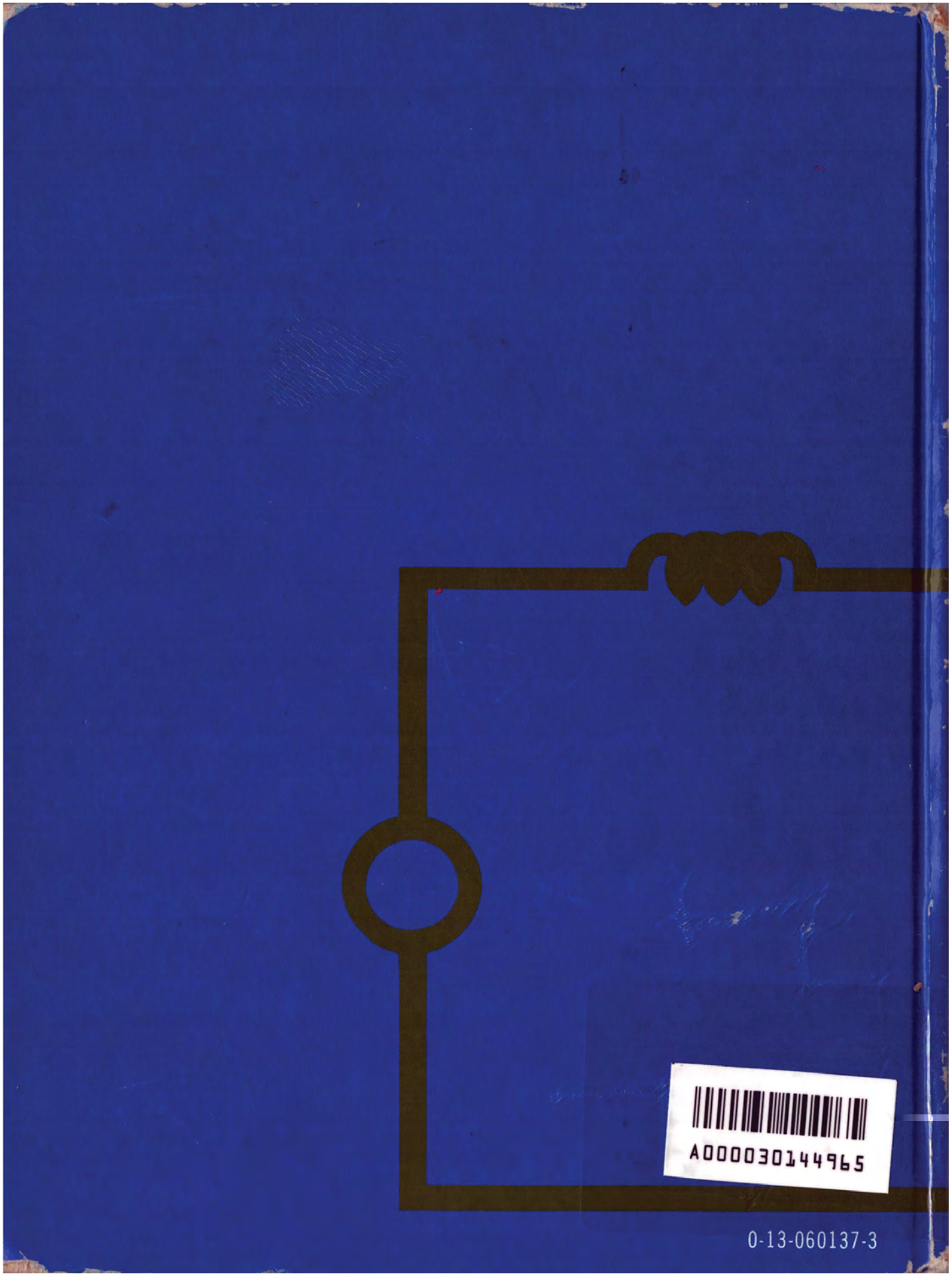
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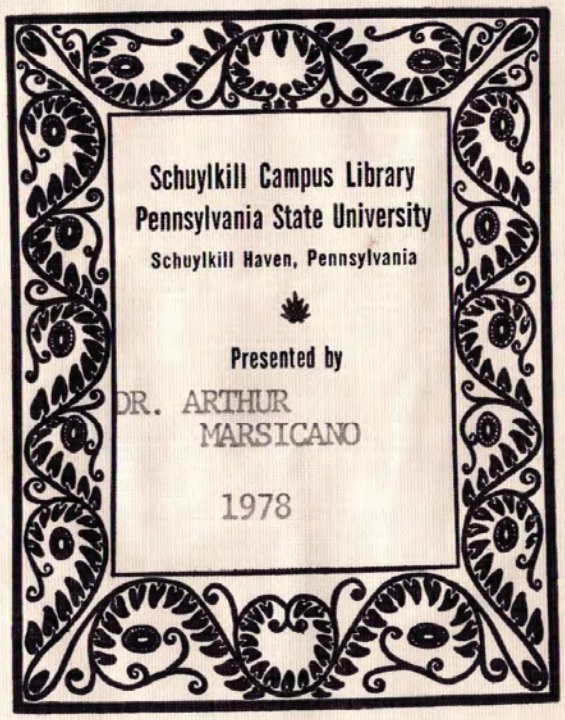



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Johnson, David E.
Basic electric circuit analysis / D. E. Johnson, J. L. Hilburn, J. R. Johnson. Englewood Cliffs, N.J. : Prentice-Hall, 1978.
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course, mind-boggling numbers, but their sizes enable us to use more manageable numbers, such as 2 C, in the circuit theory to follow.

The symbol for charge will be taken as Q or q, the capital letter usually denoting constant charges such as $Q = 4$ C, and the lowercase letter indicating a time-varying charge. In the latter case we may emphasize the time dependency by writing $q(t)$. This practice involving capital and lowercase letters will be carried over to the other electrical quantities as well.

The primary purpose of an electric circuit is to move or transfer charges along specified paths. This motion of charges constitutes an *electric current*, denoted by the letters i or I, taken from the French word "intensité." Formally, current is the time rate of change of charge, given by

$$i = \frac{dq}{dt} \tag{1.1}$$

The basic unit of current is the *ampere* (A), named for André Marie Ampère (1775–1836), a French mathematician and physicist who formulated laws of electromagnetics in the 1820s. An ampere is 1 coulomb per second.

In circuit theory current is generally thought of as the movement of positive charges. This convention stems from Benjamin Franklin (1706–1790), who guessed that electricity traveled from positive to negative. We now know that in metal conductors the current is the movement of electrons that have been pulled loose from the orbits of the atoms of the metal. Thus we should distinguish *conventional* current (the movement of positive charges), which is used in electric network theory, and *electron* current. Unless otherwise stated, our concern will be with conventional current.

As an example, suppose the current in the wire of Fig. 1.3(a) is $I = 3$ A. That is, 3 C/s pass some specific point in the wire. This is symbolized by the arrow labeled 3 A, whose direction indicates that the motion is from left to right. This situation is equivalent to that depicted by Fig. 1.3(b), which indicates -3 C/s or -3 A in the direction from right to left.

Figure 1.4 represents a general circuit element with a current i flowing from the left toward the right terminal. The total charge entering the element between time t_0 and t is found by integrating (1.1). The result is

$$q_T = q(t) - q(t_0) = \int_{t_0}^{t} i\, dt \tag{1.2}$$

We should note at this point that we are considering the network elements to be *electrically neutral*. That is, no net positive or negative charge can accumulate in the element. A positive charge entering must be accompanied by an equal positive

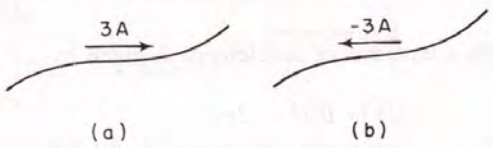


FIGURE 1.3 *Two representations of the same current*

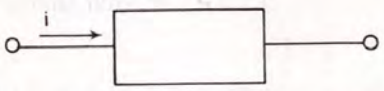


FIGURE 1.4 *Current flowing in a general element*

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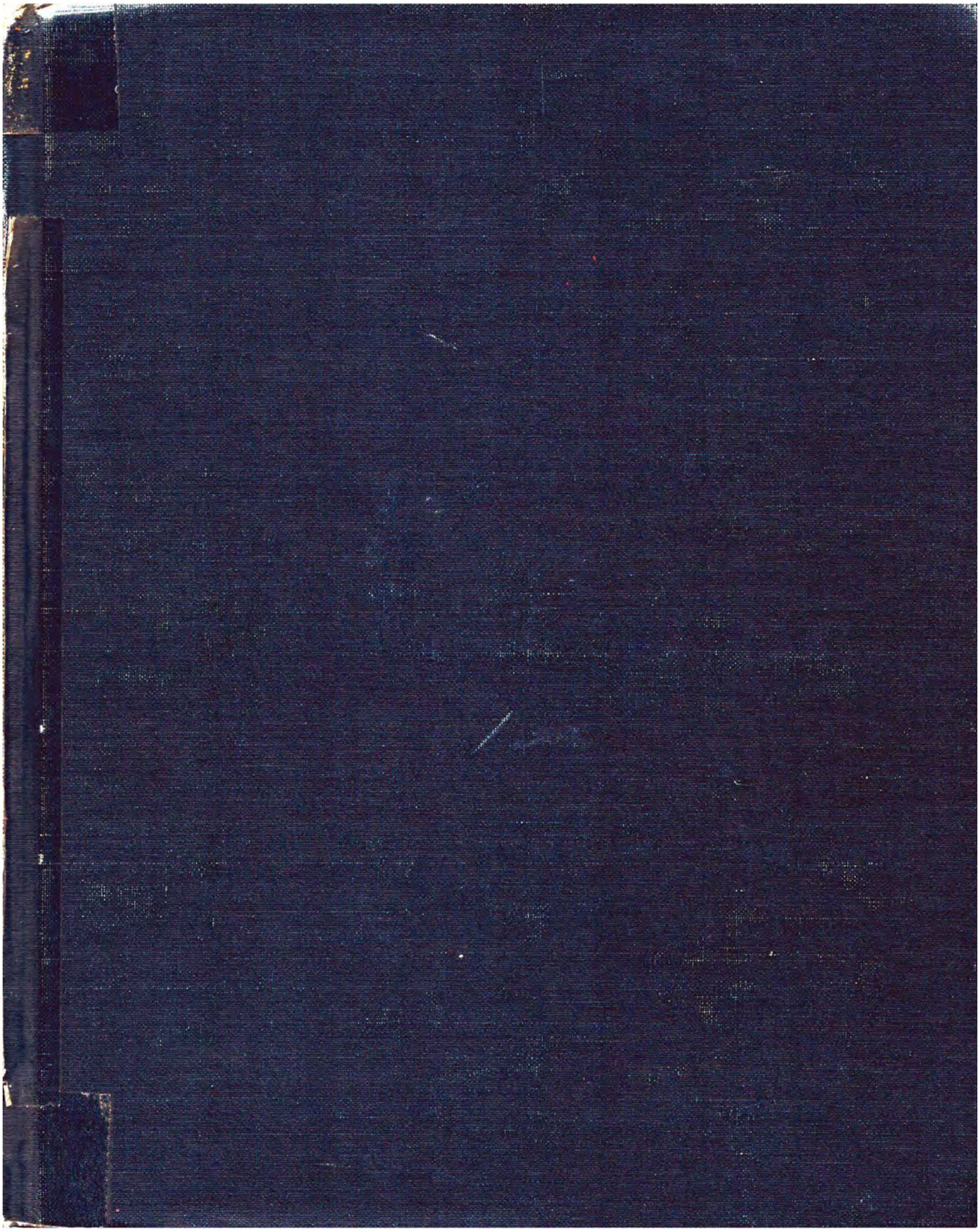
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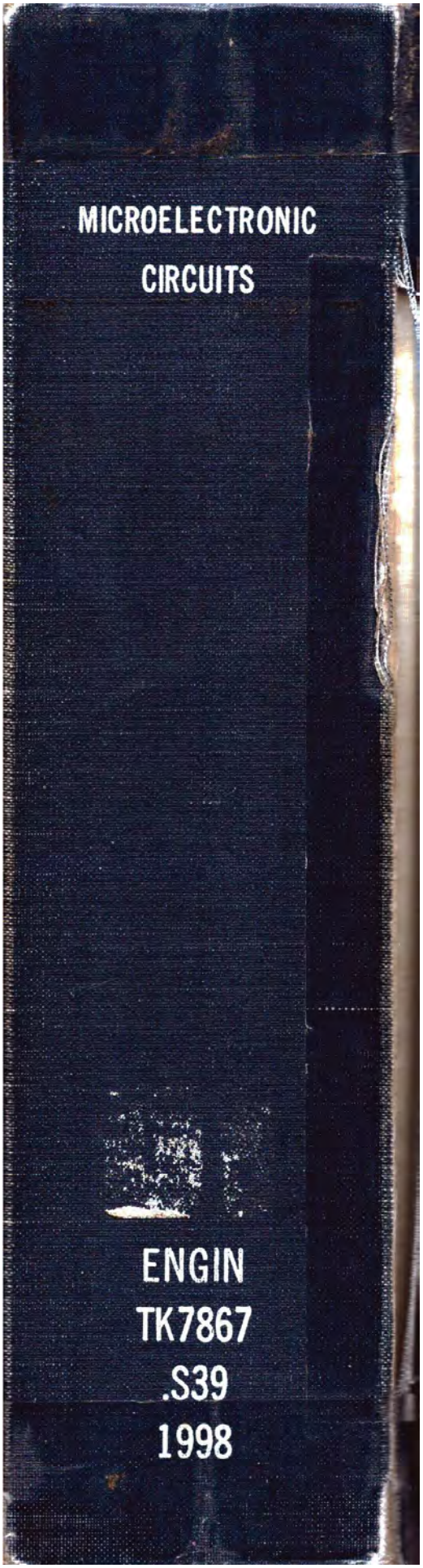
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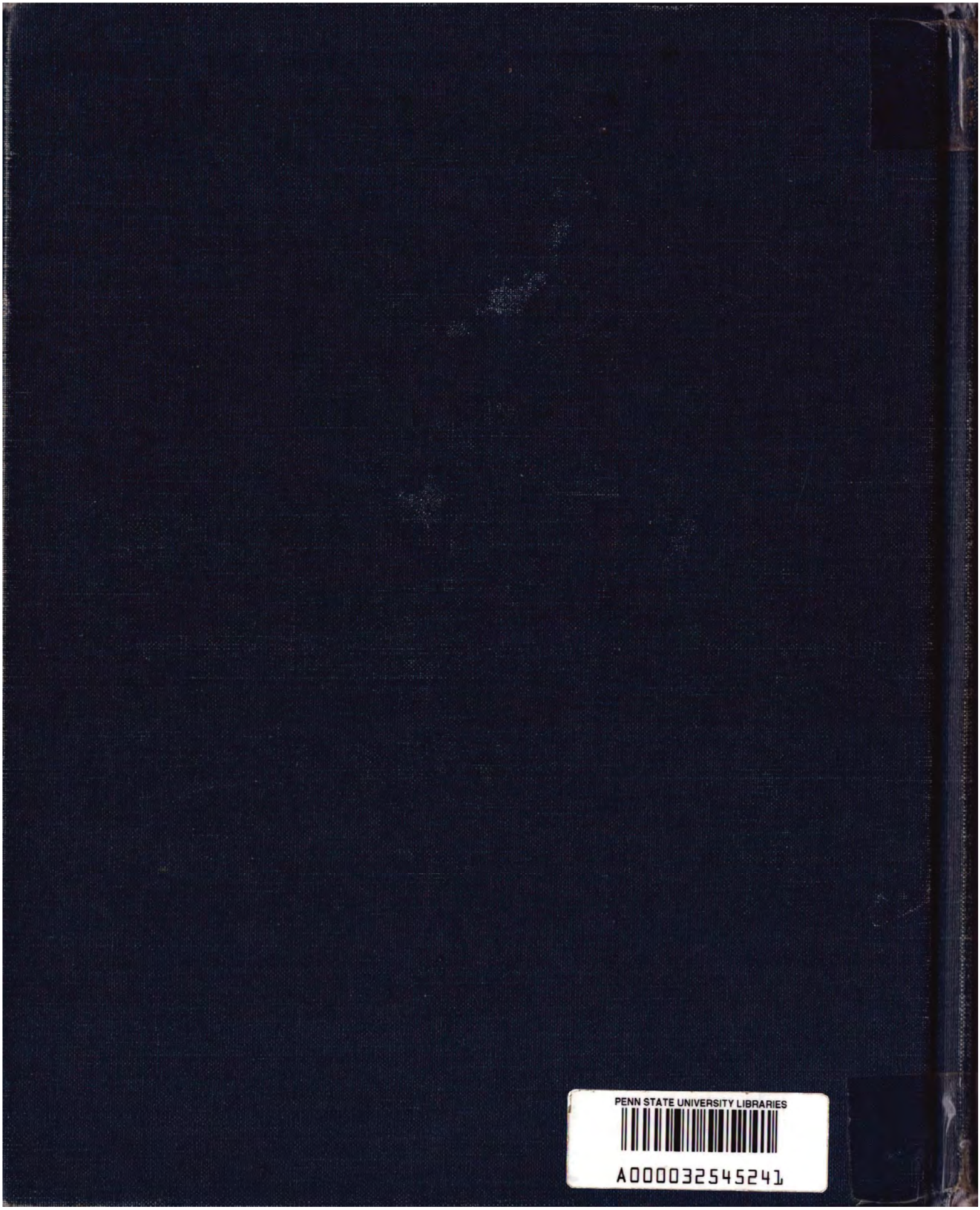
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