CHAPTER 1

Introduction to Electronics

Introduction
1.1 Signals
1.2 Frequency Spectrum of Signals
1.3 Analog and Digital Signals
1.4 Amplifiers
1.5 Circuit Models for Amplifiers
1.6 Frequency Response of Amplifiers
1.7 The Digital Logic Inverter
Summary
Bibliography
Problems

INTRODUCTION

The subject of this book is modern electronics, a field that has come to be known as **microelectronics. Microelectronics** refers to the integrated-circuit (IC) technology that at the time of this writing is capable of producing circuits that contain millions of components in a small piece of silicon (known as a **silicon chip**) whose area is in the order of 100 mm^2. One such microelectronic circuit, for example, is a complete digital computer, which accordingly is known as a **microcomputer** or, more generally, a **microprocessor.**

In this book we shall study electronic devices that can be used singly (in the design of **discrete circuits**) or as components of an **integrated-circuit (IC)** chip. We shall study the design and analysis of interconnections of these devices, which form discrete and integrated circuits of varying complexity and perform a wide variety of functions. We shall also learn about available IC chips and their application in the design of electronic systems.

The purpose of this first chapter is to introduce some basic concepts and terminology. In particular, we shall learn about signals and about one of the most important signal-processing functions electronic circuits are designed to perform, namely, signal amplification. We shall then look at models for linear amplifiers. These models will be employed in subsequent chapters in the design and analysis of actual amplifier circuits.

Whereas the amplifier is the basic element of analog circuits, the logic inverter plays this role in digital circuits. We shall therefore take a preliminary look at the digital inverter, its circuit function, and important characteristics.

In addition to motivating the study of electronics, this chapter serves as a bridge between the study of linear circuits and that of the subject of this book: the design and analysis of electronic circuits.

1.1 SIGNALS

Signals contain information about a variety of things and activities in our physical world. Examples abound: Information about the weather is contained in signals that represent the air temperature, pressure, wind speed, etc. The voice of a radio announcer reading the news into a microphone provides an acoustic signal that contains information about world affairs. To monitor the status of a nuclear reactor, instruments are used to measure a multitude of relevant parameters, each instrument producing a signal.

To extract required information from a set of signals, the observer (be it a human or a machine) invariably needs to **process** the signals in some predetermined manner. This **signal processing** is usually most conveniently performed by electronic systems. For this to be possible, however, the signal must first be converted into an electric signal, that is, a voltage or a current. This process is accomplished by devices known as **transducers.** A variety of transducers exist, each suitable for one of the various forms of physical signals. For instance, the sound waves generated by a human can be converted into electric signals using a microphone, which is in effect a pressure transducer. It is not our purpose here to study transducers; rather, we shall assume that the signals of interest already exist in the electrical domain and represent them by one of the two equivalent forms shown in Fig. 1.1. In Fig. 1.1(a) the signal is represented by a voltage source $v_s(t)$ having a source resistance R_s. In the alternate representation of Fig. 1.1(b) the signal is represented by a current source $i_s(t)$ having a source resistance R_s. Although the two representations are equivalent, that in Fig. 1.1(a) (known as the Thévenin form) is preferred when R_s is low. The representation of Fig. 1.1(b) (known as the Norton form) is preferred when R_s is high.

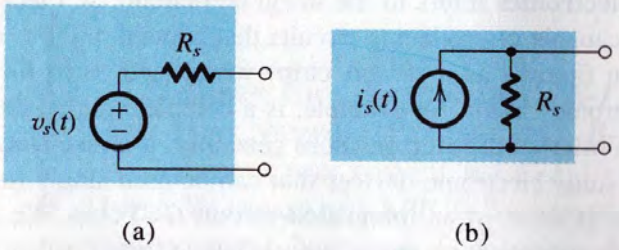


Fig. 1.1 Two alternative representations of a signal source: **(a)** the Thévenin form, and **(b)** the Norton form.

From the discussion above, it should be apparent that a signal is a time-varying quantity that can be represented by a graph such as that shown in Fig. 1.2. In fact, the information content of the signal is represented by the changes in its magnitude as time progresses; that is, the information is contained in the "wiggles" in the signal waveform. In general, such waveforms are difficult to characterize mathematically. In other words, it is not easy to describe succinctly an arbitrary looking waveform such as that of Fig. 1.2. Of course, such a description is of great importance for the purpose of designing appropriate signal-processing circuits that perform desired functions on the given signal.

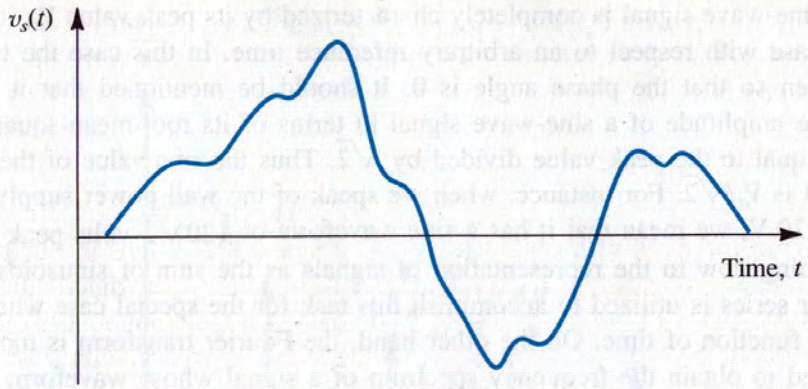


Fig. 1.2 An arbitrary voltage signal $v_s(t)$.

1.2 FREQUENCY SPECTRUM OF SIGNALS

An extremely useful characterization of a signal, and for that matter of any arbitrary function of time, is in terms of its **frequency spectrum.** Such a description of signals is obtained through the mathematical tools of **Fourier series** and **Fourier transform.**[1] We are not interested at this point in the details of these transformations; suffice it to say that they provide the means for representing a voltage signal $v_s(t)$ or a current signal $i_s(t)$ as the sum of sine-wave signals of different frequencies and amplitudes. This makes the sine wave a very important signal in the analysis, design, and testing of electronic circuits. Therefore, we shall briefly review the properties of the sinusoid.

Figure 1.3 shows a sine-wave voltage signal $v_a(t)$,

$$v_a(t) = V_a \sin \omega t \tag{1.1}$$

where V_a denotes the peak value or amplitude in volts and ω denotes the angular frequency in radians per second; that is, $\omega = 2\pi f$ rad/s, where f is the frequency in hertz, $f = 1/T$ Hz, and T is the period in seconds.

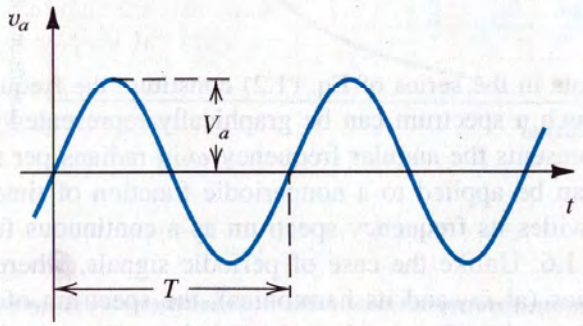


Fig. 1.3 Sine-wave voltage signal of amplitude V_a and frequency $f = 1/T$ Hz. The angular frequency $\omega = 2\pi f$ rad/s.

[1] The reader who has not yet studied these topics should not be alarmed. No detailed application of this material will be made until Chapter 7. Nevertheless, a general understanding of Section 1.2 should be very helpful when studying early parts of this book.

The sine-wave signal is completely characterized by its peak value V_a, its frequency ω, and its phase with respect to an arbitrary reference time. In this case the time origin has been chosen so that the phase angle is 0. It should be mentioned that it is common to express the amplitude of a sine-wave signal in terms of its root-mean-square (rms) value, which is equal to the peak value divided by $\sqrt{2}$. Thus the rms value of the sinusoid $v_a(t)$ of Fig. 1.3 is $V_a/\sqrt{2}$. For instance, when we speak of the wall power supply in our homes as being 120 V, we mean that it has a sine waveform of $120\sqrt{2}$ volts peak value.

Returning now to the representation of signals as the sum of sinusoids, we note that the Fourier series is utilized to accomplish this task for the special case when the signal is a periodic function of time. On the other hand, the Fourier transform is more general and can be used to obtain the frequency spectrum of a signal whose waveform is an arbitrary function of time.

The Fourier series allows us to express a given periodic function of time as the sum of an infinite number of sinusoids whose frequencies are harmonically related. For instance, the symmetrical square-wave signal in Fig. 1.4 can be expressed as

$$v(t) = \frac{4V}{\pi}(\sin \omega_0 t + \tfrac{1}{3} \sin 3\omega_0 t + \tfrac{1}{5} \sin 5\omega_0 t + \cdots) \tag{1.2}$$

where V is the amplitude of the square wave and $\omega_0 = 2\pi/T$ (T is the period of the square wave) is called the **fundamental frequency.** Note that because the amplitudes of the harmonics progressively decrease, the infinite series can be truncated, with the truncated series providing an approximation to the square waveform.

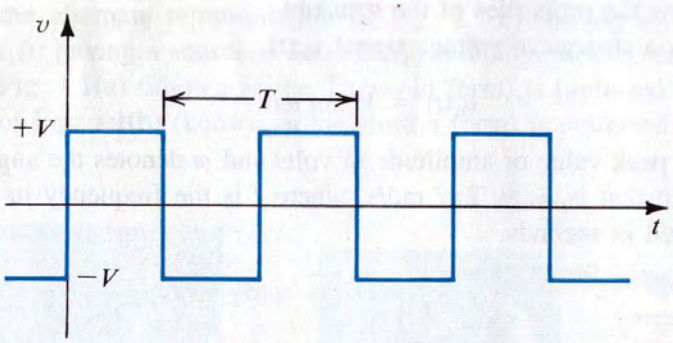


Fig. 1.4 A symmetrical square-wave signal of amplitude V.

The sinusoidal components in the series of Eq. (1.2) constitute the frequency spectrum of the square-wave signal. Such a spectrum can be graphically represented as in Fig. 1.5, where the horizontal axis represents the angular frequency ω in radians per second.

The Fourier transform can be applied to a nonperiodic function of time, such as that depicted in Fig. 1.2, and provides its frequency spectrum as a continuous function of frequency, as indicated in Fig. 1.6. Unlike the case of periodic signals, where the spectrum consists of discrete frequencies (at ω_0 and its harmonics), the spectrum of a nonperiodic signal contains in general all possible frequencies. Nevertheless, the essential parts of the spectra of practical signals are usually confined to relatively short segments of the frequency (ω) axis—an observation that is very useful in the processing of such signals. For instance, the spectrum of audible sounds such as speech and music extends from about 20 Hz to about 20 kHz—a frequency range known as the **audio band.** Here we should note that

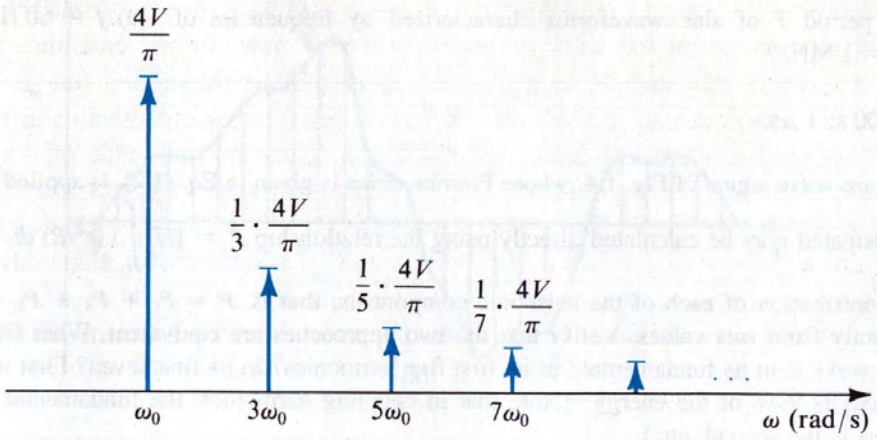


Fig. 1.5 The frequency spectrum (also known as the line spectrum) of the periodic square wave of Fig. 1.4.

although some musical tones have frequencies above 20 kHz, the human ear is incapable of hearing frequencies that are much above 20 kHz.

We conclude this section by noting that a signal can be represented either by the manner in which its waveform varies with time, as for the voltage signal $v_a(t)$ shown in Fig. 1.2, or in terms of its frequency spectrum, as in Fig. 1.6. The two alternative representations are known as the time-domain representation and the frequency-domain representation, respectively. The frequency-domain representation of $v_a(t)$ will be denoted by the symbol $V_a(\omega)$.

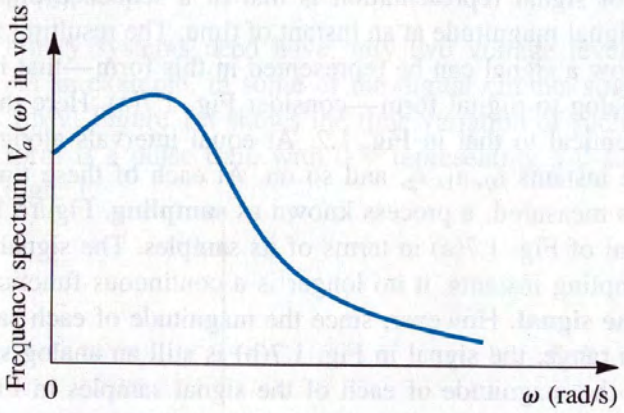


Fig. 1.6 The frequency spectrum of an arbitrary waveform such as that in Fig. 1.2.

Exercises

1.1 Find the frequencies f and ω of a sine-wave signal with a period of 1 ms.

Ans. $f = 1000$ Hz; $\omega = 2\pi \times 10^3$ rad/s

1.2 What is the period T of sine waveforms characterized by frequencies of (a) $f = 60$ Hz? (b) $f = 10^{-3}$ Hz? (c) $f = 1$ MHz?

Ans. 16.7 ms; 1000 s; 1 μs

1.3 When the square-wave signal of Fig. 1.4, whose Fourier series is given in Eq. (1.2), is applied to a resistor, the total power dissipated may be calculated directly using the relationship $P = 1/T \int_0^T (v^2/R)\, dt$, or indirectly by summing the contribution of each of the harmonic components, that is, $P = P_1 + P_3 + P_5 + \cdots$, which may be found directly from rms values. Verify that the two approaches are equivalent. What fraction of the energy of a square wave is in its fundamental? In its first five harmonics? In its first seven? First nine? In what number of harmonics is 90% of the energy? (Note that in counting harmonics, the fundamental at ω_0 is the first, the one at $2\omega_0$ is the second, etc.)

Ans. 0.81; 0.93; 0.95; 0.96; 3

1.3 ANALOG AND DIGITAL SIGNALS

The voltage signal depicted in Fig. 1.2 is called an **analog signal.** The name derives from the fact that such a signal is analogous to the physical signal that it represents. The magnitude of an analog signal can take on any value; that is, the amplitude of an analog signal exhibits a continuous variation over its range of activity. The vast majority of signals in the world around us are analog. Electronic circuits that process such signals are known as **analog circuits.** A variety of analog circuits will be studied in this book.

An alternative form of signal representation is that of a sequence of numbers, each number representing the signal magnitude at an instant of time. The resulting signal is called a **digital signal.** To see how a signal can be represented in this form—that is, how signals can be converted from analog to digital form—consider Fig. 1.7(a). Here the curve represents a voltage signal, identical to that in Fig. 1.2. At equal intervals along the time axis we have marked the time instants t_0, t_1, t_2, and so on. At each of these time instants the magnitude of the signal is measured, a process known as **sampling.** Figure 1.7(b) shows a representation of the signal of Fig. 1.7(a) in terms of its samples. The signal of Fig. 1.7(b) is defined only at the sampling instants; it no longer is a continuous function of time, but rather, it is a **discrete-time signal.** However, since the magnitude of each sample can take any value in a continuous range, the signal in Fig. 1.7(b) is still an analog signal.

Now if we represent the magnitude of each of the signal samples in Fig. 1.7(b) by a number having a finite number of digits, then the signal amplitude will no longer be continuous; rather, it is said to be **quantized, discretized,** or **digitized.** The resulting digital signal then is simply a sequence of numbers that represent the magnitudes of the successive signal samples.

The choice of number system to represent the signal samples affects the type of digital signal produced and has a profound effect on the complexity of the digital circuits required to process the signals. It turns out that the **binary** number system results in the simplest possible digital signals and circuits. In a binary system, each digit in the number takes on one of only two possible values, denoted 0 and 1. Correspondingly, the digital signals in

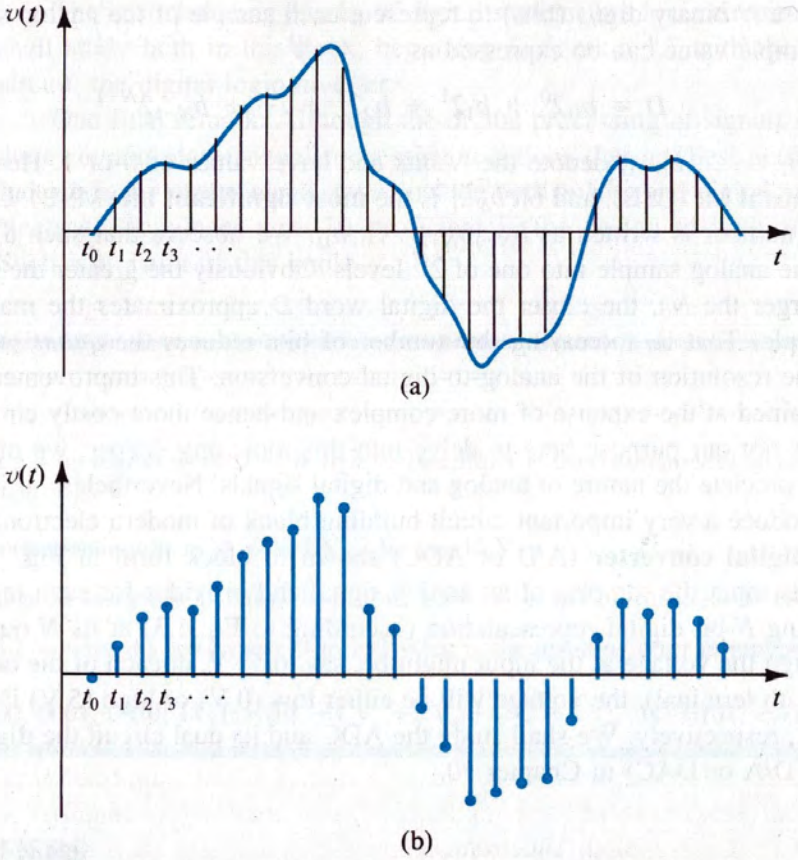


Fig. 1.7 Sampling the continuous-time analog signal in **(a)** results in the discrete-time signal in **(b)**.

binary systems need have only two voltage levels, which can be labeled low and high. As an example, in some of the digital circuits studied in this book, the levels are 0 V and +5 V. Figure 1.8 shows the time variation of such a digital signal. Observe that the waveform is a pulse train with 0 V representing a 0 signal, or logic 0, and +5 V representing logic 1.

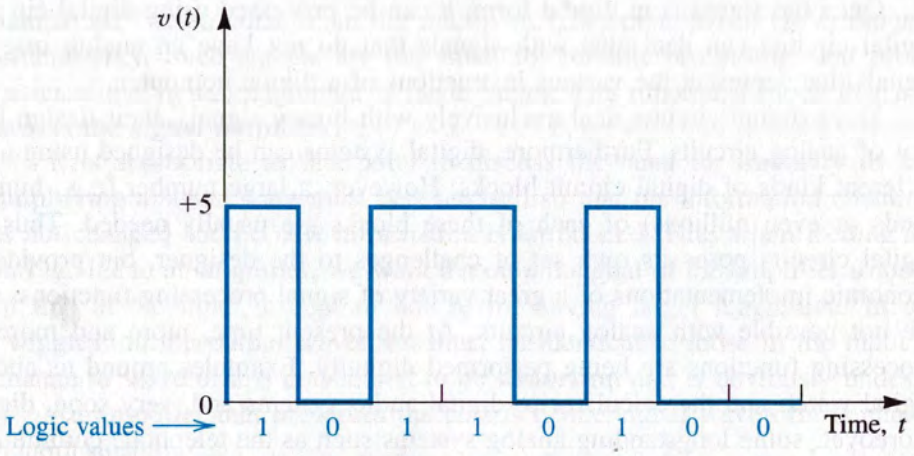


Fig. 1.8 Variation of a particular binary digital signal with time.

If we use N *b*inary dig*its* (bits) to represent each sample of the analog signal, then the digitized sample value can be expressed as

$$D = b_0 2^0 + b_1 2^1 + b_2 2^2 + \cdots + b_{N-1} 2^{N-1} \tag{1.3}$$

where $b_0, b_1, \ldots, b_{N-1}$, denote the N bits and have values of 0 or 1. Here bit b_0 is the **least significant bit** (LSB), and bit b_{N-1} is the **most significant bit** (MSB). Conventionally, this binary number is written as $b_{N-1}b_{N-2} \ldots b_0$. We observe that such a representation quantizes the analog sample into one of 2^N levels. Obviously the greater the number of bits (i.e., the larger the N), the closer the digital word D approximates the magnitude of the analog sample. That is, increasing the number of bits reduces the *quantization error* and increases the resolution of the analog-to-digital conversion. This improvement is, however, usually obtained at the expense of more complex and hence more costly circuit implementations. It is not our purpose here to delve into this topic any deeper; we merely want the reader to appreciate the nature of analog and digital signals. Nevertheless, it is an opportune time to introduce a very important circuit building block of modern electronic systems: the **analog-to-digital converter** (A/D or ADC) shown in block form in Fig. 1.9. The ADC accepts at its input the samples of an analog signal and provides for each input sample the corresponding N-bit digital representation (according to Eq. 1.3) at its N output terminals. Thus although the voltage at the input might be, say, 6.51 V, at each of the output terminals (say, at the ith terminal), the voltage will be either low (0 V) or high (5 V) if b_i is supposed to be 0 or 1, respectively. We shall study the ADC and its dual circuit the **digital-to-analog converter** (D/A or DAC) in Chapter 10.

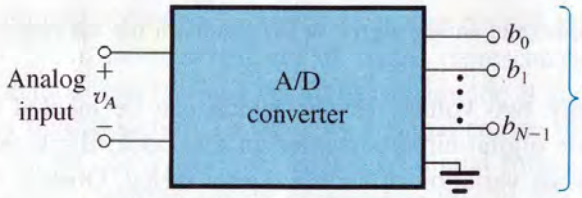


Fig. 1.9 Block-diagram representation of the analog-to-digital converter (ADC).

Once the signal is in digital form, it can be processed using digital circuits. Of course digital circuits can deal also with signals that do not have an analog origin such as the signals that represent the various instructions of a digital computer.

Since digital circuits deal exclusively with binary signals, their design is simpler than that of analog circuits. Furthermore, digital systems can be designed using a relatively few different kinds of digital circuit blocks. However, a large number (e.g., hundreds of thousands or even millions) of each of these blocks are usually needed. Thus the design of digital circuits poses its own set of challenges to the designer, but provides reliable and economic implementations of a great variety of signal processing functions, some of which are not possible with analog circuits. At the present time, more and more of the signal processing functions are being performed digitally. Examples around us abound: from the digital watch and the calculator to digital audio systems and, very soon, digital television. Moreover, some longstanding analog systems such as the telephone communication system are now almost entirely digital. And we should not forget the most important of all digital systems, the digital computer.

The basic building blocks of digital systems are logic circuits and memory circuits. We shall study both in this book, beginning in Section 1.7 with the most fundamental digital circuit, the digital logic inverter.

One final remark: Although the digital processing of signals is at present all-pervasive, there remain many signal processing functions that are best performed by analog circuits. Indeed, many electronic systems include both analog and digital parts. It follows that a good electronics engineer must be proficient in the design of both analog and digital circuits. Such is the aim of this book.

Exercise

1.4 Consider a 4-bit digital word $D = b_3b_2b_1b_0$ (see Eq. 1.3) used to represent an analog signal v_A that varies between 0 V and +15 V.

(a) Give D corresponding to $v_A = 0$ V, 1 V, 2 V, and 15 V.

(b) What change in v_A causes a change from 0 to 1 in: (i) b_0, (ii) b_1, (iii) b_2, and (iv) b_3?

(c) If $v_A = 5.2$ V, what do you expect D to be? What is the resulting error in representation?

Ans. (a) 0000, 0001, 0010, 1111; (b) +1 V, +2 V, +4 V, +8 V; (c) 0101, −4%

1.4 AMPLIFIERS

In this section, we shall introduce a fundamental signal-processing function that is employed in some form in almost every electronic system, namely, signal amplification.

Signal Amplification

From a conceptual point of view the simplest signal-processing task is that of **signal amplification.** The need for amplification arises because transducers provide signals that are said to be "weak," that is, in the microvolt (μV) or millivolt (mV) range and possessing little energy. Such signals are too small for reliable processing, and processing is much easier if the signal magnitude is made larger. The functional block that accomplishes this task is the **signal amplifier.**

It is appropriate at this point to discuss the need for **linearity** in amplifiers. When amplifying a signal, care must be exercised so that the information contained in the signal is not changed and no new information is introduced. Thus when feeding the signal shown in Fig. 1.2 to an amplifier, we want the output signal of the amplifier to be an exact replica of that at the input, except of course for having larger magnitude. In other words, the "wiggles" in the output waveform must be identical to those in the input waveform. Any change in waveform is considered to be **distortion** and is obviously undesirable.

An amplifier that preserves the details of the signal waveform is characterized by the relationship

$$v_o(t) = Av_i(t) \tag{1.4}$$

where v_i and v_o are the input and output signals, respectively, and A is a constant representing the magnitude of amplification, known as **amplifier gain.** Equation (1.4) is a linear relationship; hence the amplifier it describes is a **linear amplifier.** It should be easy to see that if the relationship between v_o and v_i contains higher powers of v_i, then the waveform of v_o will no longer be identical to that of v_i. The amplifier is then said to exhibit **nonlinear distortion.**

The amplifiers discussed so far are primarily intended to operate on very small input signals. Their purpose is to make the signal magnitude larger and therefore are thought of as **voltage amplifiers.** The **preamplifier** in the home stereo system is an example of a voltage amplifier. However, it usually does more than just amplify the signal; specifically, it performs some shaping of the frequency spectrum of the input signal. This topic, however, is beyond our need at this moment.

At this time we wish to mention another type of amplifier, namely, the power amplifier. Such an amplifier may provide only a modest amount of voltage gain but substantial current gain. Thus while absorbing little power from the input signal source to which it is connected, often a preamplifier, it delivers large amounts of power to its load. An example is found in the power amplifier of the home stereo system, whose purpose is to provide sufficient power to drive the loudspeaker. Here we should note that the loudspeaker is the output transducer of the stereo system; it converts the electric output signal of the system into an acoustic signal. A further appreciation of the need for linearity can be acquired by reflecting on the power amplifier. A linear power amplifier causes both soft and loud music passages to be reproduced without distortion.

Amplifier Circuit Symbol

The signal amplifier is obviously a two-port network. Its function is conveniently represented by the circuit symbol of Fig. 1.10(a). This symbol clearly distinguishes the input and output ports and indicates the direction of signal flow. Thus, in subsequent diagrams it will not be necessary to label the two ports "input" and "output." For generality we have shown the amplifier to have two input terminals that are distinct from the two output terminals. A more common situation is illustrated in Fig. 1.10(b), where a common terminal exists between the input and output ports of the amplifier. This common terminal is used as a reference point and is called the **circuit ground.**

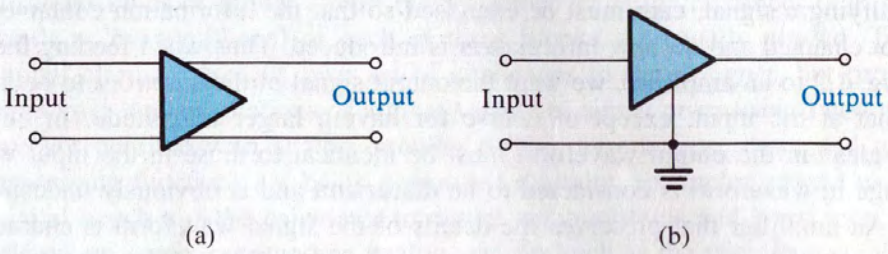


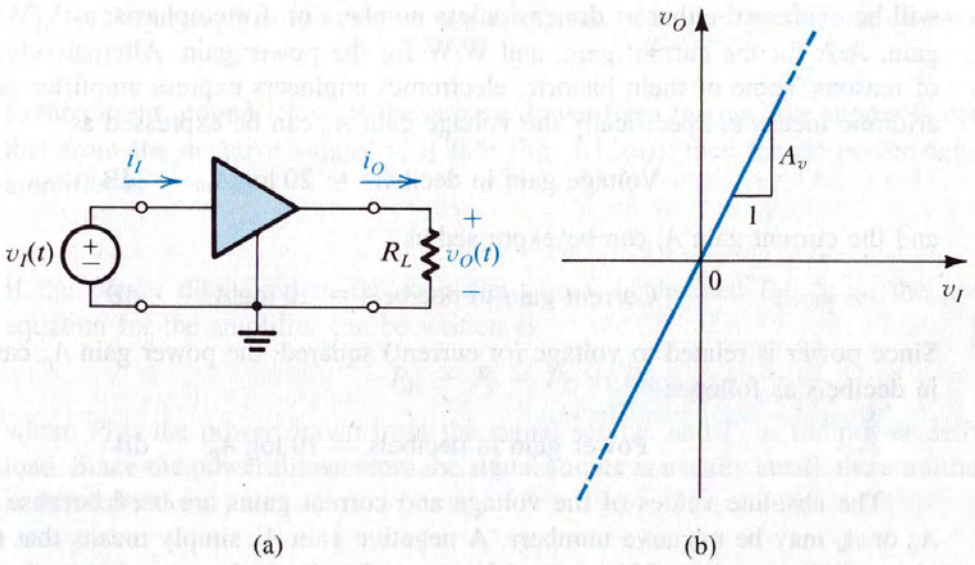
Fig. 1.10 **(a)** Circuit symbol for amplifier. **(b)** An amplifier with a common terminal (ground) between the input and output ports.

Voltage Gain

A linear amplifier accepts an input signal $v_I(t)$ and provides at the output, across a load resistance R_L (see Fig. 1.11(a)), an output signal $v_O(t)$ that is a magnified replica of $v_I(t)$. The **voltage gain** of the amplifier is defined by

$$\text{Voltage gain } (A_v) \equiv \frac{v_O}{v_I} \tag{1.5}$$

Fig. 1.11(b) shows the **transfer characteristic** of a linear amplifier. If we apply to the input of this amplifier a sinusoidal voltage of amplitude $\hat{V}$, we obtain at the output a sinusoid of amplitude $A_v\hat{V}$.



(a) (b)

Fig. 1.11 **(a)** A voltage amplifier fed with a signal $v_I(t)$ and connected to a load resistance R_L. **(b)** Transfer characteristic of a linear voltage amplifier with voltage gain A_v.

Power Gain and Current Gain

An amplifier increases the signal power, an important feature that distinguishes an amplifier from a transformer. In the case of a transformer, although the voltage delivered to the load could be greater than the voltage feeding the input side (the primary), the power delivered to the load (from the transformer secondary) is less than or at most equal to the power supplied by the signal source. On the other hand, an amplifier provides the load with power greater than that obtained from the signal source. That is, amplifiers have power gain. The **power gain** of the amplifier in Fig. 1.11(a) is defined as

$$\text{Power gain } (A_p) \equiv \frac{\text{load power } (P_L)}{\text{input power } (P_I)} \tag{1.6}$$

$$= \frac{v_O i_O}{v_I i_I} \tag{1.7}$$

where i_O is the current that the amplifier delivers to the load (R_L), $i_O = v_O/R_L$, and i_I is the current the amplifier draws from the signal source. The **current gain** of the amplifier is defined as

$$\text{Current gain } (A_i) \equiv \frac{i_O}{i_I} \tag{1.8}$$

From Eqs. (1.5) to (1.8) we note that

$$A_p = A_v A_i \tag{1.9}$$

Expressing Gain in Decibels

The amplifier gains defined above are ratios of similarly dimensioned quantities. Thus they will be expressed either as dimensionless numbers or, for emphasis, as V/V for the voltage gain, A/A for the current gain, and W/W for the power gain. Alternatively, for a number of reasons, some of them historic, electronics engineers express amplifier gain with a logarithmic measure. Specifically the voltage gain A_v can be expressed as

$$\text{Voltage gain in decibels} = 20 \log|A_v| \quad \text{dB}$$

and the current gain A_i can be expressed as

$$\text{Current gain in decibels} = 20 \log|A_i| \quad \text{dB}$$

Since power is related to voltage (or current) squared, the power gain A_p can be expressed in decibels as follows:

$$\text{Power gain in decibels} = 10 \log A_p \quad \text{dB}$$

The absolute values of the voltage and current gains are used because in some cases A_v or A_i may be negative numbers. A negative gain A_v simply means that there is a 180° phase difference between input and output signals; it does not imply that the amplifier is **attenuating** the signal. On the other hand, an amplifier whose voltage gain is, say, −20 dB is in fact attenuating the input signal by a factor of 10 (that is, $A_v = 0.1$ V/V).

The Amplifier Power Supplies

Since the power delivered to the load is greater than the power drawn from the signal source, the question arises as to the source of this additional power. The answer is found by observing that amplifiers need dc power supplies for their operation. These dc sources supply the extra power delivered to the load as well as any power that might be dissipated in the internal circuit of the amplifier (such power is converted to heat). In Fig. 1.11(a) we have not explicitly shown these dc sources.

Figure 1.12(a) shows an amplifier that requires two dc sources: one positive of value V_1 and one negative of value V_2. The amplifier has two terminals, labeled V^+ and V^-, for connection to the dc supplies. For the amplifier to operate, the terminal labeled V^+ has to be connected to the positive side of a dc source whose voltage is V_1 and whose negative side is connected to the circuit ground. Also, the terminal labeled V^- has to be connected to the negative side of a dc source whose voltage is V_2 and whose positive side is connected

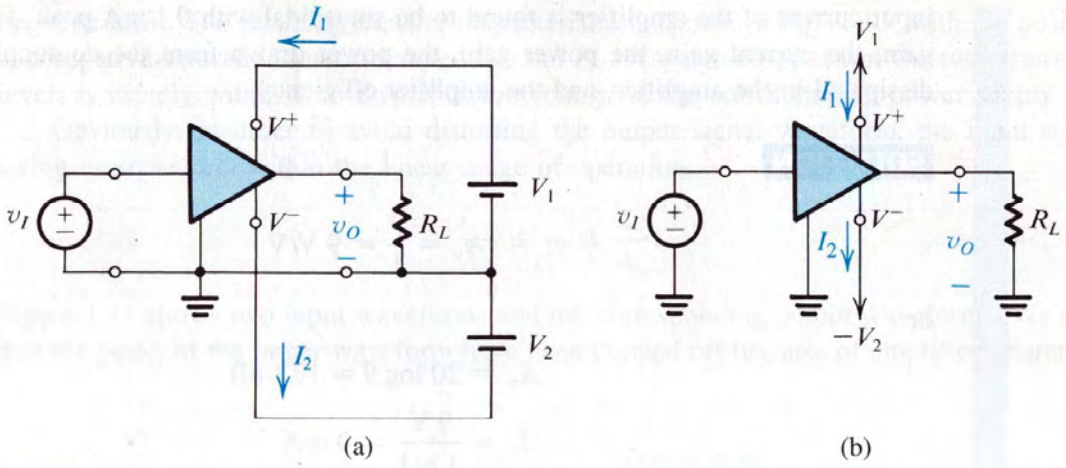


Fig. 1.12 An amplifier that requires two dc supplies (shown as batteries) for operation.

to the circuit ground. Now, if the current drawn from the positive supply is denoted I_1 and that from the negative supply is I_2 (see Fig. 1.12(a)), then the dc power delivered to the amplifier is

$$P_{dc} = V_1 I_1 + V_2 I_2$$

If the power dissipated in the amplifier circuit is denoted $P_{dissipated}$, the power-balance equation for the amplifier can be written as

$$P_{dc} + P_I = P_L + P_{dissipated}$$

where P_I is the power drawn from the signal source, and P_L is the power delivered to the load. Since the power drawn from the signal source is usually small, the amplifier **efficiency** is defined as

$$\eta \equiv \frac{P_L}{P_{dc}} \times 100 \tag{1.10}$$

The power efficiency is an important performance parameter for amplifiers that handle large amounts of power. Such amplifiers, called power amplifiers, are used, for example, as output amplifiers of stereo systems.

In order to simplify circuit diagrams, we shall adopt the convention illustrated in Fig. 1.12(b). Here the V^+ terminal is shown connected to an arrowhead pointing upward and the V^- terminal to an arrowhead pointing downward. The corresponding voltage is indicated next to each arrowhead. Note that in many cases we will not explicitly show the connections of the amplifier to the dc power sources. Finally, we note that some amplifiers require only one power supply.

EXAMPLE 1.1

Consider an amplifier operating from ±10-V power supplies. It is fed with a sinusoidal voltage having 1 V peak and delivers a sinusoidal voltage output of 9 V peak to a 1-kΩ load. The amplifier draws a current of 9.5 mA from each of its two power supplies. The

input current of the amplifier is found to be sinusoidal with 0.1 mA peak. Find the voltage gain, the current gain, the power gain, the power drawn from the dc supplies, the power dissipated in the amplifier, and the amplifier efficiency.

SOLUTION

$$A_v = \frac{9}{1} = 9 \text{ V/V}$$

or

$$A_v = 20 \log 9 \simeq 19.1 \text{ dB}$$

$$\hat{I}_o = \frac{9 \text{ V}}{1 \text{ k}\Omega} = 9 \text{ mA}$$

$$A_i = \frac{\hat{I}_o}{\hat{I}_i} = \frac{9}{0.1} = 90 \text{ A/A}$$

or

$$A_i = 20 \log 90 = 39.1 \text{ dB}$$

$$P_L = V_{o_{\text{rms}}} I_{o_{\text{rms}}} = \frac{9}{\sqrt{2}} \frac{9}{\sqrt{2}} = 40.5 \text{ mW}$$

$$P_I = V_{i_{\text{rms}}} I_{i_{\text{rms}}} = \frac{1}{\sqrt{2}} \frac{0.1}{\sqrt{2}} = 0.05 \text{ mW}$$

$$A_p = \frac{P_L}{P_I} = \frac{40.5}{0.05} = 810 \text{ W/W}$$

or

$$A_p = 10 \log 810 = 29.1 \text{ dB}$$

$$P_{\text{dc}} = 10 \times 9.5 + 10 \times 9.5 = 190 \text{ mW}$$

$$P_{\text{dissipated}} = P_{\text{dc}} + P_I - P_L$$
$$= 190 + 0.05 - 40.5 = 149.6 \text{ mW}$$

$$\eta = \frac{P_L}{P_{\text{dc}}} \times 100 = 21.3\%$$

From the above example we observe that the amplifier converts some of the dc power it draws from the power supplies to signal power that it delivers to the load.

Amplifier Saturation

Practically speaking, the amplifier transfer characteristic remains linear over only a limited range of input and output voltages. For an amplifier operated from two power supplies the output voltage cannot exceed a specified positive limit and cannot decrease below a specified

negative limit. The resulting transfer characteristic is shown in Fig. 1.13, with the positive and negative saturation levels denoted L_+ and L_-, respectively. Each of the two saturation levels is usually within 1 or 2 volts of the voltage of the corresponding power supply.

Obviously, in order to avoid distorting the output signal waveform, the input signal swing must be kept within the linear range of operation.

$$\frac{L_-}{A_v} \leq v_I \leq \frac{L_+}{A_v}$$

Figure 1.13 shows two input waveforms and the corresponding output waveforms. We note that the peaks of the larger waveform have been clipped off because of amplifier saturation.

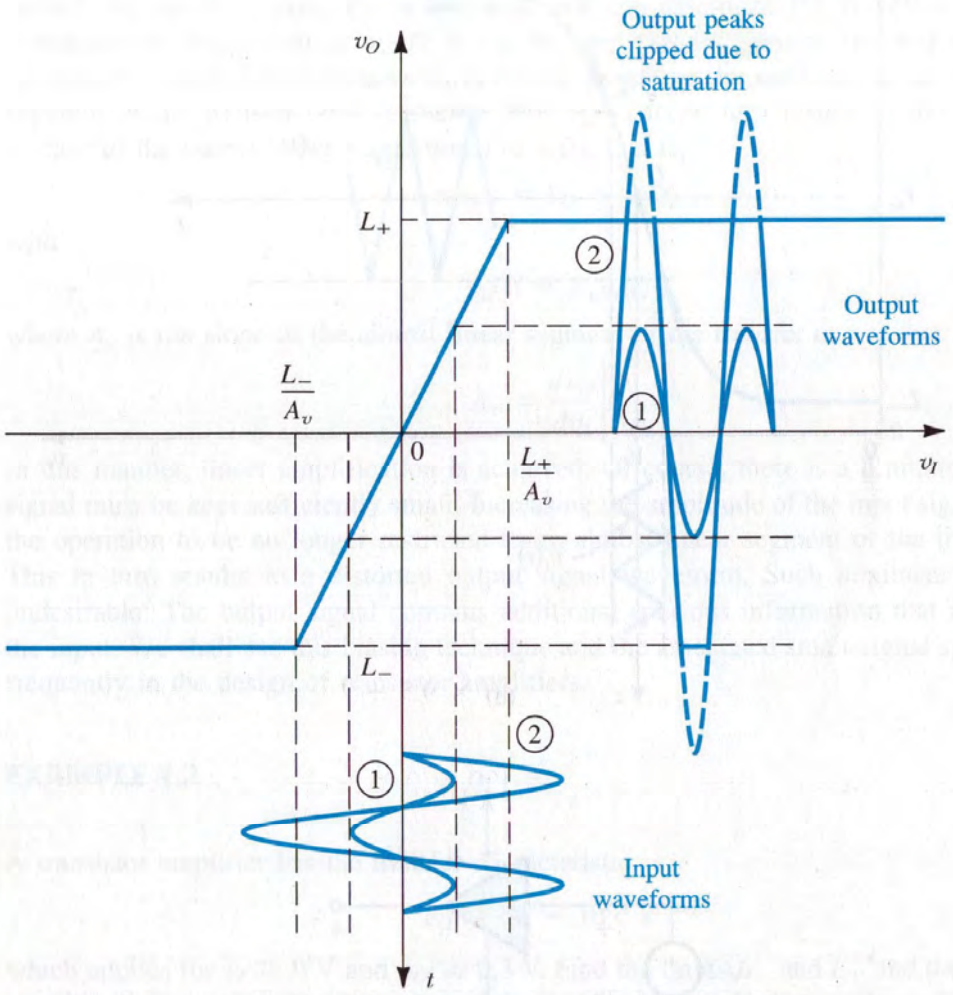
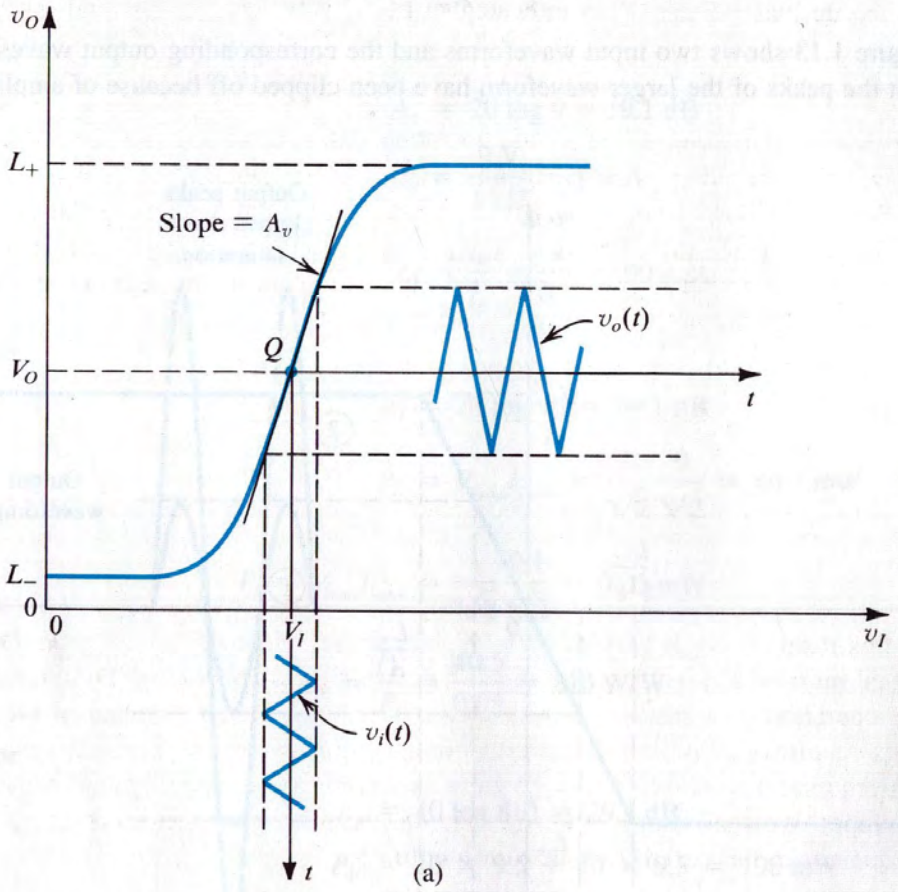


Fig. 1.13 An amplifier transfer characteristic that is linear except for output saturation.

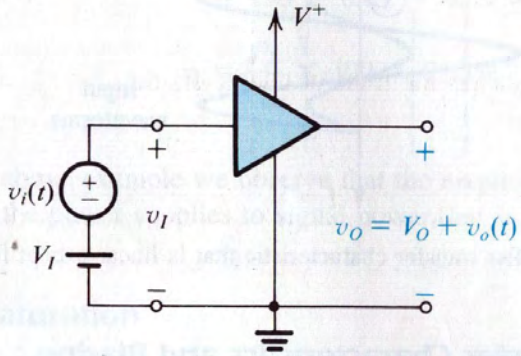
Nonlinear Transfer Characteristics and Biasing

Except for the output saturation effect discussed above, the amplifier transfer characteristics have been assumed to be perfectly linear. In practical amplifiers the transfer characteristic

may exhibit nonlinearities of various magnitudes, depending on how elaborate the amplifier circuit is, and on how much effort has been expended in the design to ensure linear operation. Consider as an example the transfer characteristic depicted in Fig. 1.14. Such a characteristic is typical of simple amplifiers that are operated from a single (positive) power supply. The transfer characteristic is obviously nonlinear and, because of the single-supply operation, is



(a)



(b)

Fig. 1.14 **(a)** An amplifier transfer characteristic that shows considerable nonlinearity. **(b)** To obtain linear operation the amplifier is biased as shown, and the signal amplitude is kept small.

not centered around the origin. Fortunately, a simple technique exists for obtaining linear amplification from an amplifier with such a nonlinear transfer characteristic.

The technique consists of first **biasing** the circuit to operate at a point near the middle of the transfer characteristic. This is achieved by applying a dc voltage V_I, as indicated in Fig. 1.14, where the operating point is labeled Q and the corresponding dc voltage at the output is V_O. The point Q is known as the **quiescent point,** the **dc bias point,** or simply the **operating point.** The time-varying signal to be amplified, $v_i(t)$, is then superimposed on the dc bias voltage V_I as indicated in Fig. 1.14. Now, as the total instantaneous input $v_I(t)$,

$$v_I(t) = V_I + v_i(t)$$

varies around V_I, the instantaneous operating point moves up and down the transfer curve around the operating point Q. In this way, one can determine the waveform of the total instantaneous output voltage $v_O(t)$. It can be seen that by keeping the amplitude of $v_i(t)$ sufficiently small, the instantaneous operating point can be confined to an almost linear segment of the transfer curve centered about Q. This in turn results in the time-varying portion of the output being proportional to $v_i(t)$; that is,

$$v_O(t) = V_O + v_o(t)$$

with

$$v_o(t) = A_v v_i(t)$$

where A_v is the slope of the almost linear segment of the transfer curve; that is,

$$A_v = \left.\frac{dv_O}{dv_I}\right|_{\text{at}Q}$$

In this manner, linear amplification is achieved. Of course, there is a limitation: The input signal must be kept sufficiently small. Increasing the amplitude of the input signal can cause the operation to be no longer restricted to an almost linear segment of the transfer curve. This in turn results in a distorted output signal waveform. Such nonlinear distortion is undesirable: The output signal contains additional spurious information that is not part of the input. We shall use this biasing technique and the associated small-signal approximation frequently in the design of transistor amplifiers.

EXAMPLE 1.2

A transistor amplifier has the transfer characteristic

$$v_O = 10 - 10^{-11}e^{40v_I} \tag{1.11}$$

which applies for $v_I \geq 0$ V and $v_O \geq 0.3$ V. Find the limits L_- and L_+ and the corresponding values of v_I. Also, find the value of the dc bias voltage V_I that results in $V_O = 5$ V and the voltage gain at the corresponding operating point.

SOLUTION

The limit L_- is obviously 0.3 V. The corresponding value of v_I is obtained by substituting $v_O = 0.3$ V in Eq. (1.10); that is,

$$v_I = 0.690 \text{ V}$$

The limit L_+ is determined by $v_I = 0$ and is thus given by

$$L_+ = 10 - 10^{-11} \simeq 10 \text{ V}$$

To bias the device so that $V_O = 5$ V we require a dc input V_I whose value is obtained by substituting $v_O = 5$ V in Eq. (1.10) to find:

$$V_I = 0.673 \text{ V}$$

The gain at the operating point is obtained by evaluating the derivative dv_O/dv_I at $v_I = 0.673$ V. The result is

$$A_v = -200 \text{ V/V}$$

which indicates that this amplifier in an inverting one, that is, the output is 180° out of phase with the input. A sketch of the amplifier transfer characteristic (not to scale) is shown in Fig. 1.15, from which we observe the inverting nature of the amplifier.

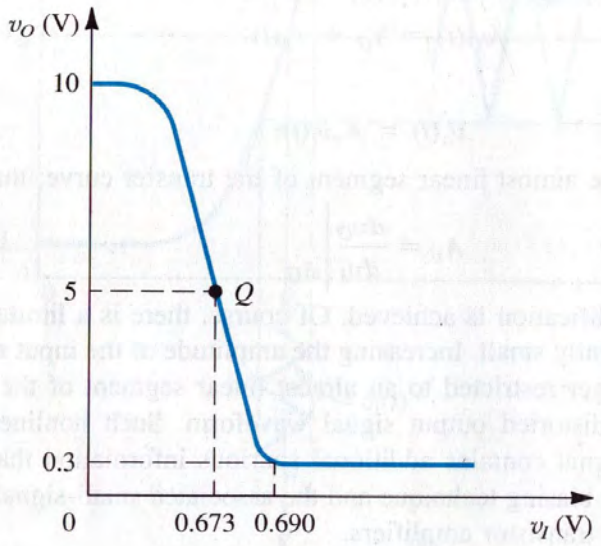


Fig. 1.15 A sketch of the transfer characteristic of the amplifier of Example 1.2. Note that this amplifier is inverting (that is, with a gain that is negative).

Once an amplifier is properly biased and the input signal is kept sufficiently small, the operation is assumed to be linear. We can then employ the techniques of linear circuit analysis to analyze the signal operation of the amplifier circuit. The following two sections provide a review and application of these analysis techniques.

Symbol Convention

At this point, we draw the reader's attention to the terminology used above and which we shall employ throughout the book. Total instantaneous quantities are denoted by a lowercase symbol with an uppercase subscript, for example, $i_A(t)$, $v_C(t)$. Direct-current (dc) quantities will be denoted by an uppercase symbol with an uppercase subscript, for example, I_A, V_C. Finally, incremental signal quantities will be denoted by a lowercase symbol with a lowercase subscript, for example $i_a(t)$, $v_c(t)$. This notation is illustrated in Fig. 1.16.

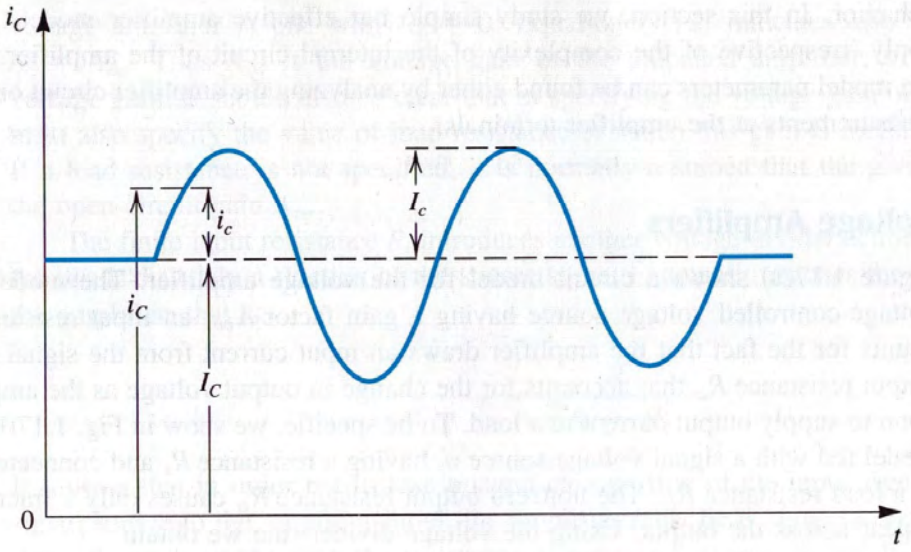


Fig. 1.16 Symbol convention employed throughout the book.

Exercises

1.5 An amplifier has a voltage gain of 100 V/V and a current gain of 1000 A/A. Express the voltage and current gains in decibels and find the power gain.

Ans. 40 dB; 60 dB; 50 dB

1.6 An amplifier operating from a single 15-V supply provides a 12-V peak-to-peak sine-wave signal to a 1-kΩ load, and draws negligible input current from the signal source. The dc current drawn from the 15-V supply is 8 mA. What is the power dissipated in the amplifier and what is the amplifier efficiency?

Ans. 102 mW; 15%

1.7 The objective of this exercise is to investigate the limitation of the small-signal approximation. Consider the amplifier of Example 1.2 with a positive input signal of 1 mV superimposed on the dc bias voltage V_I. Find the corresponding signal at the output for two situations: (a) Assume the amplifier is linear around the operating point; that is, use the value of gain evaluated in Example 1.2. (b) Use the transfer characteristic of the amplifier. Repeat for input signals of 5 mV and 10 mV.

Ans. −0.2 V, −0.204 V; −1 V, −1.107 V; −2 V, −2.459 V

1.5 CIRCUIT MODELS FOR AMPLIFIERS

A good part of this book is concerned with the design of amplifier circuits using transistors of various types. Such circuits will vary in complexity from those using a single transistor to those with 20 or more devices. In order to be able to apply the resulting amplifier circuit as a building block in a system, one must be able to characterize, or **model,** its terminal

behavior. In this section, we study simple but effective amplifier models. These models apply irrespective of the complexity of the internal circuit of the amplifier. The values of the model parameters can be found either by analyzing the amplifier circuit or by performing measurements at the amplifier terminals.

Voltage Amplifiers

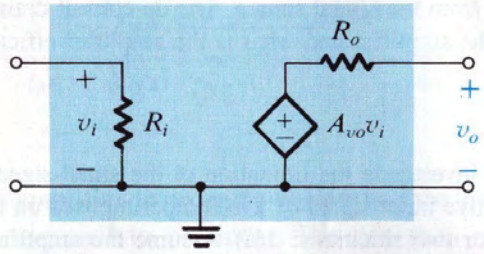
Figure 1.17(a) shows a circuit model for the voltage amplifier. The model consists of a voltage-controlled voltage source having a gain factor A_{vo}, an input resistance R_i that accounts for the fact that the amplifier draws an input current from the signal source, and an output resistance R_o that accounts for the change in output voltage as the amplifier is called upon to supply output current to a load. To be specific, we show in Fig. 1.17(b) the amplifier model fed with a signal voltage source v_s having a resistance R_s and connected at the output to a load resistance R_L. The nonzero output resistance R_o causes only a fraction of $A_{vo}v_i$ to appear across the output. Using the voltage-divider rule we obtain

$$v_o = A_{vo}v_i\frac{R_L}{R_L + R_o}$$

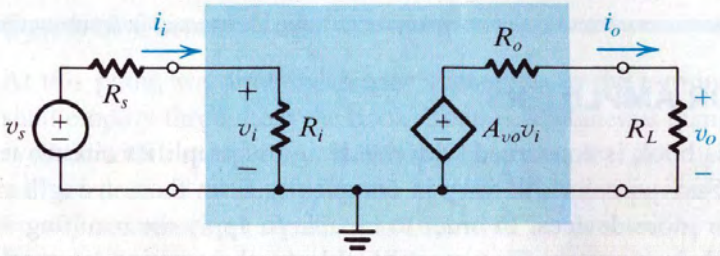
Thus the voltage gain is given by

$$A_v \equiv \frac{v_o}{v_i} = A_{vo}\frac{R_L}{R_L + R_o} \tag{1.12}$$

It follows that in order not to lose gain in coupling the amplifier output to a load, the output resistance R_o should be much smaller than the load resistance R_L. In other words, for a given R_L one must design the amplifier so that its R_o is much smaller than R_L. An ideal



(a)



(b)

Fig. 1.17 **(a)** Circuit model for the voltage amplifier. **(b)** The voltage amplifier with input signal source and load.

voltage amplifier is one with $R_o = 0$. Equation (1.12) indicates also that for $R_L = \infty$, $A_v = A_{vo}$. Thus A_{vo} is the voltage gain of the unloaded amplifier, or the **open-circuit voltage gain.** It should also be clear that in specifying the voltage gain of an amplifier, one must also specify the value of load resistance at which this gain is measured or calculated. If a load resistance is not specified, it is normally assumed that the given voltage gain is the open-circuit gain A_{vo}.

The finite input resistance R_i introduces another voltage-divider action at the input, with the result that only a fraction of the source signal v_s actually reaches the input terminals of the amplifier; that is,

$$v_i = v_s \frac{R_i}{R_i + R_s} \tag{1.13}$$

It follows that in order not to lose a significant portion of the input signal in coupling the signal source to the amplifier input, the amplifier must be designed to have an input resistance R_i much greater than the resistance of the signal source, $R_i \gg R_s$. An ideal voltage amplifier is one with $R_i = \infty$. In this ideal case both the current gain and power gain become infinite.

The overall voltage gain (v_o/v_s) can be found by combining Eqs. (1.12) and (1.13),

$$\frac{v_o}{v_s} = A_{vo} \frac{R_i}{R_i + R_s} \frac{R_L}{R_L + R_o}$$

There are situations in which one is interested not in voltage gain but only in a significant power gain. For instance, the source signal can have a respectable voltage but a source resistance which is much greater than the load resistance. Connecting the source directly to the load would result in significant signal attenuation. In such a case, one requires an amplifier with a high input resistance (much greater than the source resistance) and a low output resistance (much smaller than the load resistance) but with a modest voltage gain (or even unity gain). Such an amplifier is referred to as a **buffer amplifier.** We shall encounter buffer amplifiers often throughout this book.

EXAMPLE 1.3

Figure 1.18 depicts an amplifier composed of a cascade of three stages. The amplifier is fed by a signal source with a source resistance of 100 kΩ and delivers its output into a load resistance of 100 Ω. The first stage has a relatively high input resistance and a modest gain factor of 10. The second stage has a higher gain factor but lower input resistance. Finally, the last, or output, stage has unity gain but a low output resistance. We wish to evaluate the overall voltage gain, that is, v_L/v_s, the current gain, and the power gain.

SOLUTION

The fraction of source signal appearing at the input terminals of the amplifier is obtained using the voltage-divider rule at the input, as follows:

$$\frac{v_{i1}}{v_s} = \frac{1\ \text{MΩ}}{1\ \text{MΩ} + 100\ \text{kΩ}} = 0.909$$

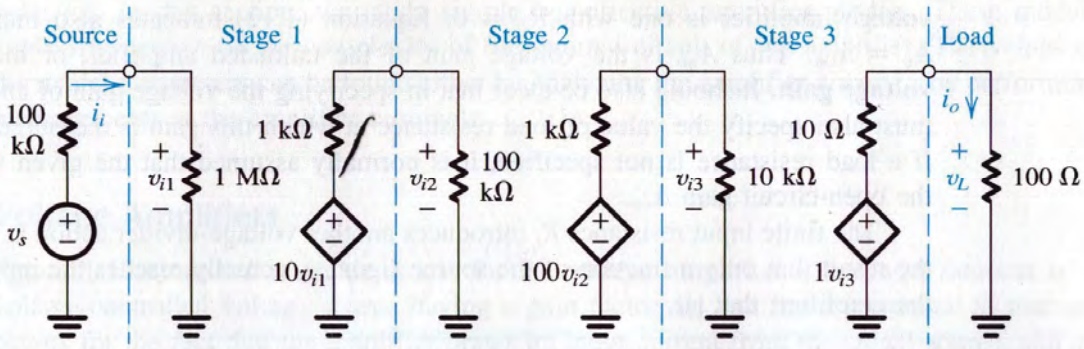


Fig. 1.18 Three-stage amplifier for Example 1.3.

The voltage gain of the first stage is obtained by considering the input resistance of the second stage to be the load of the first stage; that is,

$$A_{v1} \equiv \frac{v_{i2}}{v_{i1}} = 10\frac{100\ \text{k}\Omega}{100\ \text{k}\Omega + 1\ \text{k}\Omega} = 9.9\ \text{V/V}$$

Similarly, the voltage gain of the second stage is obtained by considering the input resistance of the third stage to be the load of the second stage,

$$A_{v2} \equiv \frac{v_{i3}}{v_{i2}} = 100\frac{10\ \text{k}\Omega}{10\ \text{k}\Omega + 1\ \text{k}\Omega} = 90.9\ \text{V/V}$$

Finally, the voltage gain of the output stage is as follows:

$$A_{v3} \equiv \frac{v_L}{v_{i3}} = 1\frac{100\ \Omega}{100\ \Omega + 10\ \Omega} = 0.909\ \text{V/V}$$

The total gain of the three stages in cascade can be now found from

$$A_v \equiv \frac{v_L}{v_{i1}} = A_{v1}A_{v2}A_{v3} = 818\ \text{V/V}$$

or 58.3 dB.

To find the voltage gain from source to load we multiply A_v by the factor representing the loss of gain at the input; that is,

$$\frac{v_L}{v_s} = \frac{v_L}{v_{i1}}\frac{v_{i1}}{v_s} = A_v\frac{v_{i1}}{v_s}$$
$$= 818 \times 0.909 = 743.6\ \text{V/V}$$

or 57.4 dB.

The current gain is found as follows:

$$A_i \equiv \frac{i_o}{i_i} = \frac{v_L/100\ \Omega}{v_{i1}/1\ \text{M}\Omega}$$
$$= 10^4 \times A_v = 8.18 \times 10^6\ \text{A/A}$$

or 138.3 dB.

The power gain is found from

$$A_p \equiv \frac{P_L}{P_I} = \frac{v_L i_o}{v_{i1} i_i}$$
$$= A_v A_i = 818 \times 8.18 \times 10^6 = 66.9 \times 10^8 \text{ W/W}$$

or 98.3 dB. Note that

$$A_p(\text{dB}) = \tfrac{1}{2}[A_v(\text{dB}) + A_i(\text{dB})]$$

Exercises

1.8 A transducer characterized by a voltage of 1 V rms and a resistance of 1 MΩ is available to drive a 10-Ω load. If connected directly, what voltage and power levels result at the load? If a unity-gain (that is, $A_{vo} = 1$) buffer amplifier with 1-MΩ input resistance and 10-Ω output resistance is interposed between source and load, what do the output voltage and power levels become? For the new arrangement find the voltage gain from source to load, and the power gain (both expressed in decibels).

Ans. 10 μV rms; 10^{-11} W; 0.25 V; 6.25 mW; −12 dB; 44 dB

1.9 The output voltage of a voltage amplifier has been found to decrease by 20% when a load resistance of 1 kΩ is connected. What is the value of the amplifier output resistance?

Ans. 250 Ω

1.10 An amplifier with a voltage gain of +40 dB, an input resistance of 10 kΩ, and an output resistance of 1 kΩ is used to drive a 1-kΩ load. What is the value of A_{vo}? Find the value of power gain in dB.

Ans. 100 V/V; 44 dB

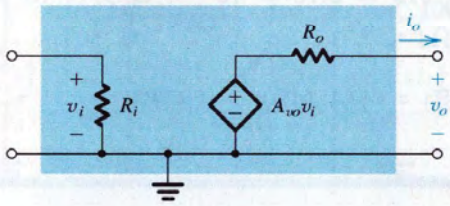
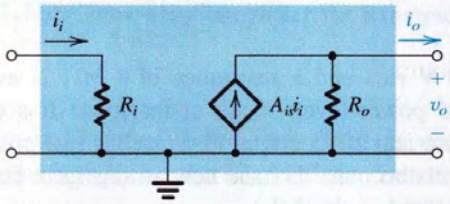
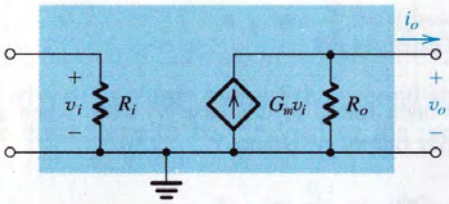
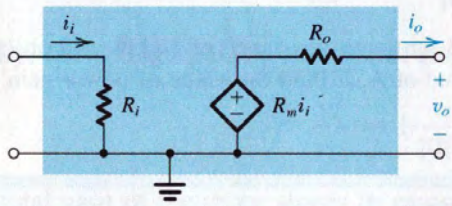
Other Amplifier Types

In the design of an electronic system, the signal of interest—whether at the system input, at an intermediate stage, or at the output—can be either a voltage or a current. For instance, some transducers have very high output resistances and can be more appropriately modeled as current sources. Similarly, there are applications in which the output current rather than the voltage is of interest. Thus, although it is the most popular, the voltage amplifier considered above is just one of four possible amplifier types. The other three are the current amplifier, the transconductance amplifier, and the transresistance amplifier. Table 1.1 shows the four amplifier types, their circuit models, the definition of their gain parameters, and the ideal values of their input and output resistances.

Relationships Between the Four Amplifier Models

Although for a given amplifier a particular one of the four models in Table 1.1 is most preferable, *any of the four can be used to model the amplifier.* In fact, simple relationships

Table 1.1 THE FOUR AMPLIFIER TYPES

Type	Circuit Model	Gain Parameter	Ideal Characteristics
Voltage Amplifier		Open-Circuit Voltage Gain $A_{vo} \equiv \left.\frac{v_o}{v_i}\right\|_{i_o = 0}$ (V/V)	$R_i = \infty$ $R_o = 0$
Current Amplifier		Short-Circuit Current Gain $A_{is} \equiv \left.\frac{i_o}{i_i}\right\|_{v_o = 0}$ (A/A)	$R_i = 0$ $R_o = \infty$
Transconductance Amplifier		Short-Circuit Transconductance $G_m \equiv \left.\frac{i_o}{v_i}\right\|_{v_o = 0}$ (A/V)	$R_i = \infty$ $R_o = \infty$
Transresistance Amplifier		Open-Circuit Transresistance $R_m \equiv \left.\frac{v_o}{i_i}\right\|_{i_o = 0}$ (V/A)	$R_i = 0$ $R_o = 0$

can be derived to relate the parameters of the various models. For instance, the open-circuit voltage gain A_{vo} can be related to the short-circuit current gain A_{is} as follows: The open-circuit output voltage given by the voltage amplifier model of Table 1.1 is $A_{vo}v_i$. The current amplifier model in the same table gives an open-circuit output voltage of $A_{is}i_iR_o$. Equating these two values and noting that $i_i = v_i/R_i$ gives

$$A_{vo} = A_{is}\left(\frac{R_o}{R_i}\right) \tag{1.14}$$

Similarly, we can show that

$$A_{vo} = G_mR_o \tag{1.15}$$

and

$$A_{vo} = \frac{R_m}{R_i} \tag{1.16}$$

The expressions in Eqs. (1.14) to (1.16) can be used to relate any two of the gain parameters A_{vo}, A_{is}, G_m, and R_m.

From the amplifier circuit models given in Table 1.1, we observe that the input resistance R_i of the amplifier can be determined by applying an input voltage v_i and measuring (or calculating) the input current i_i; that is, $R_i = v_i/i_i$. The output resistance is found as the ratio of the open-circuit output voltage to the short-circuit output current. Alternatively, the output resistance can be found by eliminating the input signal source (then i_i and v_i will both be zero) and applying a voltage signal v_x to the output of the amplifier. If we denote the current drawn from v_x *into* the output terminals as i_x (note that i_x is opposite in direction to i_o), then $R_o = v_x/i_x$. Although these techniques are conceptually correct, in actual practice more refined methods are employed in measuring R_i and R_o.

The amplifier models considered above are **unilateral;** that is, signal flow is unidirectional, from input to output. Most real amplifiers show some reverse transmission, which is usually undesirable but must nonetheless be modeled. We shall not pursue this point further at this time except to mention that more complete models for linear two-port networks are given in Appendix B.

EXAMPLE 1.4

The **bipolar junction transistor (BJT)** is a three-terminal device having the circuit symbol shown in Fig. 1.19(a) with the terminals called **emitter** (E), **base** (B), and **collector** (C). The device is basically nonlinear; thus the relationships between the total instantaneous terminal currents and voltages are generally nonlinear. Nevertheless, the linearization technique discussed in Section 1.4 can be used to provide linear operation for small signals—that is, incremental variations in currents and voltages around a bias or quiescent point. Thus the total instantaneous quantities can be expressed as the sums of dc or bias quantities and signal quantities as

$$v_{BE} = V_{BE} + v_{be} \qquad i_B = I_B + i_b$$
$$v_{CE} = V_{CE} + v_{ce} \qquad i_C = I_C + i_c$$
$$i_E = I_E + i_e$$

It will be shown in Chapter 4 that under the small-signal approximation the relationships between the signal quantities are linear and that the three-terminal transistor can be represented by one of the equivalent circuit models of Fig. 1.19(b), (c), and (d). If these models are equivalent, we wish to find expressions for the parameters of the models in Figs. 1.19(c) and (d) in terms of the parameters of the model in Fig. 1.19(b).

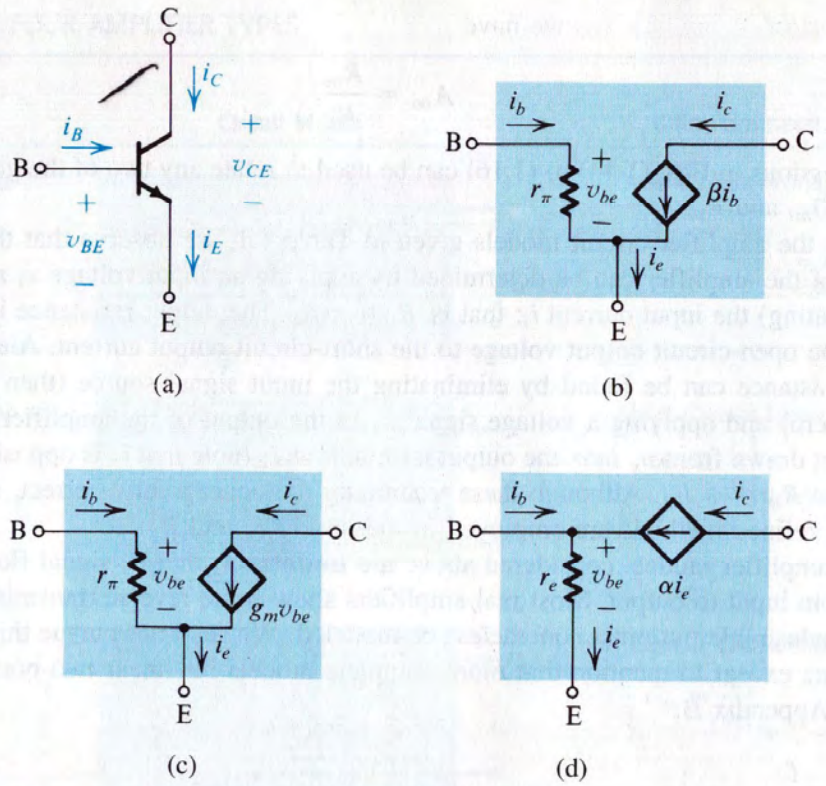


Fig. 1.19 **(a)** Circuit symbol for the bipolar junction transistor (BJT), illustrating the definition of the total instantaneous terminal quantities. **(b, c, d)** Equivalent circuit models for the small-signal linear operation of the BJT.

SOLUTION

For the model in Fig. 1.19(b) we have

$$i_b = \frac{v_{be}}{r_\pi} \tag{1.17}$$

$$i_c = \beta i_b \tag{1.18}$$

$$i_e = (\beta + 1) i_b \tag{1.19}$$

For the model in Fig. 1.19(c) we have

$$i_c = g_m v_{be} \tag{1.20}$$

Use of Eqs. (1.17), (1.18), and (1.20) gives

$$g_m = \frac{\beta}{r_\pi}$$

For the model in Fig. 1.19(d) we have

$$i_b = (1 - \alpha) i_e \tag{1.21}$$

$$i_c = \alpha i_e \tag{1.22}$$

$$i_e = \frac{v_{be}}{r_e} \tag{1.23}$$

Use of Eqs. (1.18) and (1.19) gives

$$\frac{i_c}{i_e} = \frac{\beta}{\beta + 1}$$

Comparing this result with Eq. (1.22), we get

$$\alpha = \frac{\beta}{\beta + 1}$$

Equations (1.17) and (1.19) can be combined to yield

$$i_e = \frac{\beta + 1}{r_\pi} v_{be}$$

Comparison of this result with Eq. (1.23) provides

$$r_e = \frac{r_\pi}{\beta + 1}$$

We have thus obtained expressions for the parameters of the models in Fig. 1.19(c) and (d) in terms of those for the model in Fig. 1.19(b).

Exercises

1.11 Consider a current amplifier having the model shown in the second row of Table 1.1. Let the amplifier be fed with a signal current-source i_s having a resistance R_s, and let the output be connected to a load resistance R_L. Show that the overall current gain is given by

$$\frac{i_o}{i_s} = A_{is} \frac{R_s}{R_s + R_i} \frac{R_o}{R_o + R_L}$$

1.12 Consider the transconductance amplifier whose model is shown in the third row of Table 1.1. Let a voltage signal-source v_s with a source resistance R_s be connected to the input and a load resistance R_L be connected to the output. Show that the overall voltage-gain is given by

$$\frac{v_o}{v_s} = G_m \frac{R_i}{R_i + R_s} (R_o \| R_L)$$

1.13 Consider a transistor modeled as in Fig. 1.19(b) with E connected to ground. Let a voltage source with a 1-kΩ source resistance be connected between B and ground and a load resistance of 1 kΩ be connected

between C and ground. Let $r_\pi = 2\ \text{k}\Omega$ and $\beta = 90$. Calculate the voltage gain (v_c/v_s) and the current gain (i_c/i_b) as ratios. Also give the power gain in decibels.

Ans. −30 V/V; 90 A/A; 36.1 dB

1.14 Find the input resistance between terminals B and G in the circuit shown in Fig. E1.14. The voltage

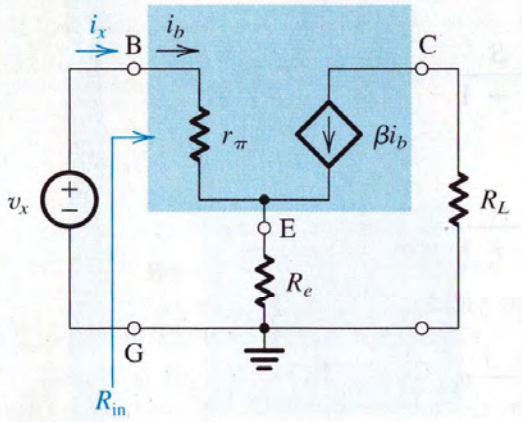


Fig. E1.14

v_x is a test voltage with the input resistance R_{in} defined as $R_{in} \equiv v_x/i_x$.

Ans. $R_{in} = r_\pi + (\beta + 1)R_e$

1.6 FREQUENCY RESPONSE OF AMPLIFIERS

From Section 1.2 we know that the input signal to an amplifier can always be expressed as the sum of sinusoidal signals. It follows that an important characterization of an amplifier is in terms of its response to input sinusoids of different frequencies. Such a characterization of amplifier performance is known as the amplifier frequency response.

Measuring the Amplifier Frequency Response

We shall introduce the subject of amplifier frequency response by showing how it can be measured. Figure 1.20 depicts a linear voltage amplifier fed at its input with a sine-wave

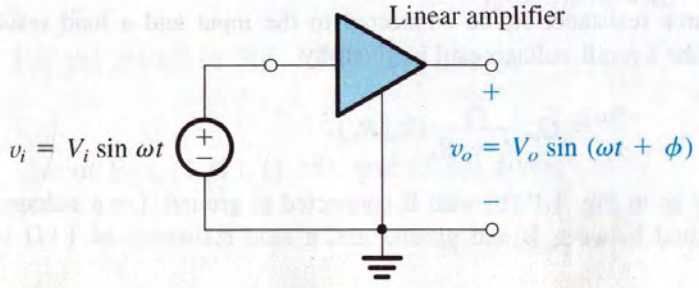


Fig. 1.20 Measuring the frequency response of a linear amplifier. At the test frequency ω, the amplifier gain is characterized by its magnitude (V_o/V_i) and phase ϕ.

signal of amplitude V_i and frequency ω. As the figure indicates, the signal measured at the amplifier output also is sinusoidal with exactly the same frequency ω. This is an important point to note: Whenever a sine-wave signal is applied to a linear circuit, the resulting output is sinusoidal with the same frequency as the input. In fact, the sine wave is the only signal that does not change shape as it passes through a linear circuit. Observe, however, that the output sinusoid will in general have a different amplitude and will be shifted in phase relative to the input. The ratio of the amplitude of the output sinusoid (V_o) to the amplitude of the input sinusoid (V_i) is the magnitude of the amplifier gain (or transmission) at the test frequency ω. Also, the angle ϕ is the phase of the amplifier transmission at the test frequency ω. If we denote the **amplifier transmission,** or **transfer function** as it is more commonly known, by $T(\omega)$ then

$$|T(\omega)| = \frac{V_o}{V_i}$$

$$\angle T(\omega) = \phi$$

The response of the amplifier to a sinusoid of frequency ω is completely described by $|T(\omega)|$ and $\angle T(\omega)$. Now, to obtain the complete frequency response of the amplifier we simply change the frequency of the input sinusoid and measure the new value for $|T|$ and $\angle T$. The end result will be a table and/or graph of gain magnitude [$|T(\omega)|$] versus frequency, and a table and/or graph of phase angle [$\angle T(\omega)$] versus frequency. These two plots together constitute the frequency response of the amplifier; the first is known as the magnitude or amplitude response, and the second is the phase response.

Amplifier Bandwidth

Figure 1.21 shows the magnitude response of an amplifier. It indicates that the gain is almost constant over a wide frequency range, roughly between ω_1 and ω_2. Signals whose frequencies are below ω_1 or above ω_2 will experience lower gain, with the gain decreasing as we move farther away from ω_1 and ω_2. The band of frequencies over which the gain of the amplifier is almost constant, to within a certain number of decibels (usually 3 dB), is called

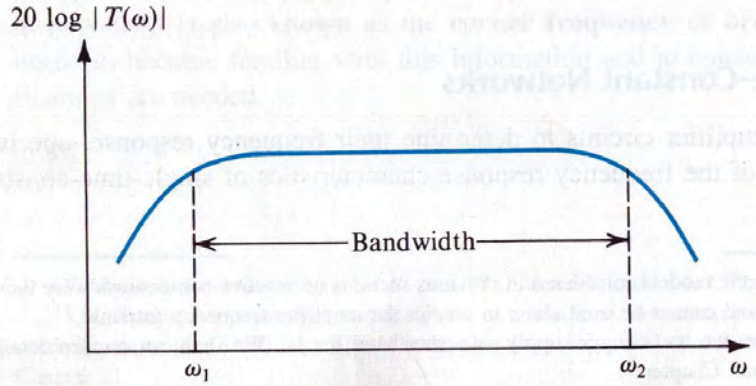


Fig. 1.21 Typical magnitude response of an amplifier. $T(\omega)$ is the amplifier transfer function—that is, the ratio of the output $V_o(\omega)$ to the input $V_i(\omega)$.

the **amplifier bandwidth.** Normally the amplifier is designed so that its bandwidth coincides with the spectrum of the signals it is required to amplify. If this were not the case, the amplifier would *distort* the frequency spectrum of the input signal, with different components of the input signal being amplified by different amounts.

Evaluating the Frequency Response of Amplifiers

Above, we described the method used to measure the frequency response of an amplifier. We now briefly discuss the method for analytically obtaining an expression for the frequency response. What we are about to say is just a preview of this important subject, whose detailed study starts in Chapter 7.

To evaluate the frequency response of an amplifier one has to analyze the amplifier equivalent circuit model, taking into account all reactive components.[2] Circuit analysis proceeds in the usual fashion but with inductances and capacitances represented by their reactances. An inductance L has a reactance or impedance $j\omega L$, and a capacitance C has a reactance or impedance $1/j\omega C$ or, equivalently, a susceptance or admittance $j\omega C$. Thus in a *frequency-domain* analysis we deal with impedances and/or admittances. The result of the analysis is the amplifier transfer function $T(\omega)$,

$$T(\omega) = \frac{V_o(\omega)}{V_i(\omega)}$$

where $V_i(\omega)$ and $V_o(\omega)$ denote the input and output signals, respectively. $T(\omega)$ is generally a complex function whose magnitude $|T(\omega)|$ gives the magnitude of transmission or the magnitude response of the amplifier. The phase of $T(\omega)$ gives the phase response of the amplifier.

In the analysis of a circuit to determine its frequency response, the algebraic manipulations can be considerably simplified by using the **complex frequency variable** s. In terms of s, the impedance of an inductance L is sL and that of a capacitance C is $1/sC$. Replacing the reactive elements with their impedances and performing standard circuit analysis, we obtain the transfer function $T(s)$ as

$$T(s) \equiv \frac{V_o(s)}{V_i(s)}$$

Subsequently, we replace s by $j\omega$ to determine the network transfer function for **physical frequencies,** $T(j\omega)$. Note that $T(j\omega)$ is the same function we called $T(\omega)$ above;[3] the additional j is included in order to emphasize that $T(j\omega)$ is obtained from $T(s)$ by replacing s with $j\omega$.

Single-Time-Constant Networks

In analyzing amplifier circuits to determine their frequency response, one is greatly aided by knowledge of the frequency response characteristics of single-time-constant (STC) net-

[2] Note that in the models considered in previous sections no reactive components were included. These were simplified models and cannot be used alone to predict the amplifier frequency response.

[3] At this stage, we are using s simply as a shorthand for $j\omega$. We shall not require detailed knowledge of s-plane concepts until Chapter 7.

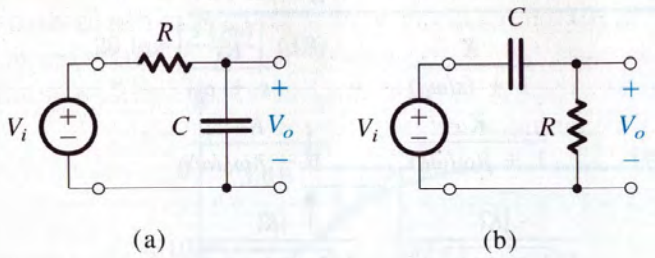


Fig. 1.22 Two examples of STC networks: **(a)** a low-pass network and **(b)** a high-pass network.

works. An STC network is one that is composed of, or can be reduced to, one reactive component (inductance or capacitance) and one resistance. Examples are shown in Fig. 1.22. An STC network formed of an inductance L and a resistance R has a time constant $\tau = L/R$. The time constant τ of an STC network composed of a capacitance C and a resistance R is given by $\tau = CR$.

Appendix F presents a study of STC networks and their responses to sinusoidal, step, and pulse inputs. Knowledge of this material will be needed at various points throughout this book, and the reader will be encouraged to refer to the Appendix. At this point we need in particular the frequency response results; we will, in fact, briefly discuss this important topic, now.

Most STC networks can be classified into two categories:[4] **low pass (LP)** and **high pass (HP),** with each of the two categories displaying distinctly different signal responses. As an example, the STC network shown in Fig. 1.22(a) is of the *low-pass* type, and that in Fig. 1.22(b) is of the *high-pass* type. To see the reasoning behind this classification, observe that the transfer function of each of these two circuits can be expressed as a voltage-divider ratio, with the divider composed of a resistor and a capacitor. Now recalling how the impedance of a capacitor varies with frequency ($Z = 1/j\omega C$) it is easy to see that the transmission of the circuit in Fig. 1.22(a) will decrease with frequency and approach zero as ω approaches ∞. Thus the circuit of Fig. 1.22(a) acts as a **low-pass filter;**[5] it passes low-frequency sine-wave inputs with little or no attenuation (at $\omega = 0$, the transmission is unity) and attenuates high-frequency input sinusoids. The circuit of Fig. 1.22(b) does the opposite; its transmission is unity at $\omega = \infty$ and decreases as ω is reduced, reaching 0 for $\omega = 0$. The latter circuit, therefore, performs as a **high-pass filter.**

Table 1.2 provides a summary of the frequency response results for STC networks of both types. Also, sketches of the magnitude and phase responses are given in Figs. 1.23 and 1.24. These frequency response diagrams are known as **Bode plots** and the 3-dB frequency (ω_0) is also known as the **corner frequency** or **break frequency.** The reader is urged to become familiar with this information and to consult Appendix F if further clarifications are needed.

[4] An important exception is the *all-pass* STC network studied in Chapter 11.

[5] A filter is a circuit that passes signals in a specified frequency band (the filter passband) and stops or severely attenuates (filters out) signals in another frequency band (the filter stopband). Filters will be studied in Chapter 11.

Table 1.2 FREQUENCY RESPONSE OF STC NETWORKS

	Low-Pass (LP)	High-Pass (HP)
Transfer Function $T(s)$	$\dfrac{K}{1 + (s/\omega_0)}$	$\dfrac{Ks}{s + \omega_0}$
Transfer Function (for physical frequencies) $T(j\omega)$	$\dfrac{K}{1 + j(\omega/\omega_0)}$	$\dfrac{K}{1 - j(\omega_0/\omega)}$
Magnitude Response $\lvert T(j\omega)\rvert$	$\dfrac{\lvert K\rvert}{\sqrt{1 + (\omega/\omega_0)^2}}$	$\dfrac{\lvert K\rvert}{\sqrt{1 + (\omega_0/\omega)^2}}$
Phase Response $\angle T(j\omega)$	$-\tan^{-1}(\omega/\omega_0)$	$\tan^{-1}(\omega_0/\omega)$
Transmission at $\omega = 0$ (dc)	K	0
Transmission at $\omega = \infty$	0	K
3-dB Frequency	$\omega_0 = 1/\tau$; $\tau \equiv$ time constant $\tau = CR$ or L/R	
Bode Plots	in Fig. 1.23	in Fig. 1.24

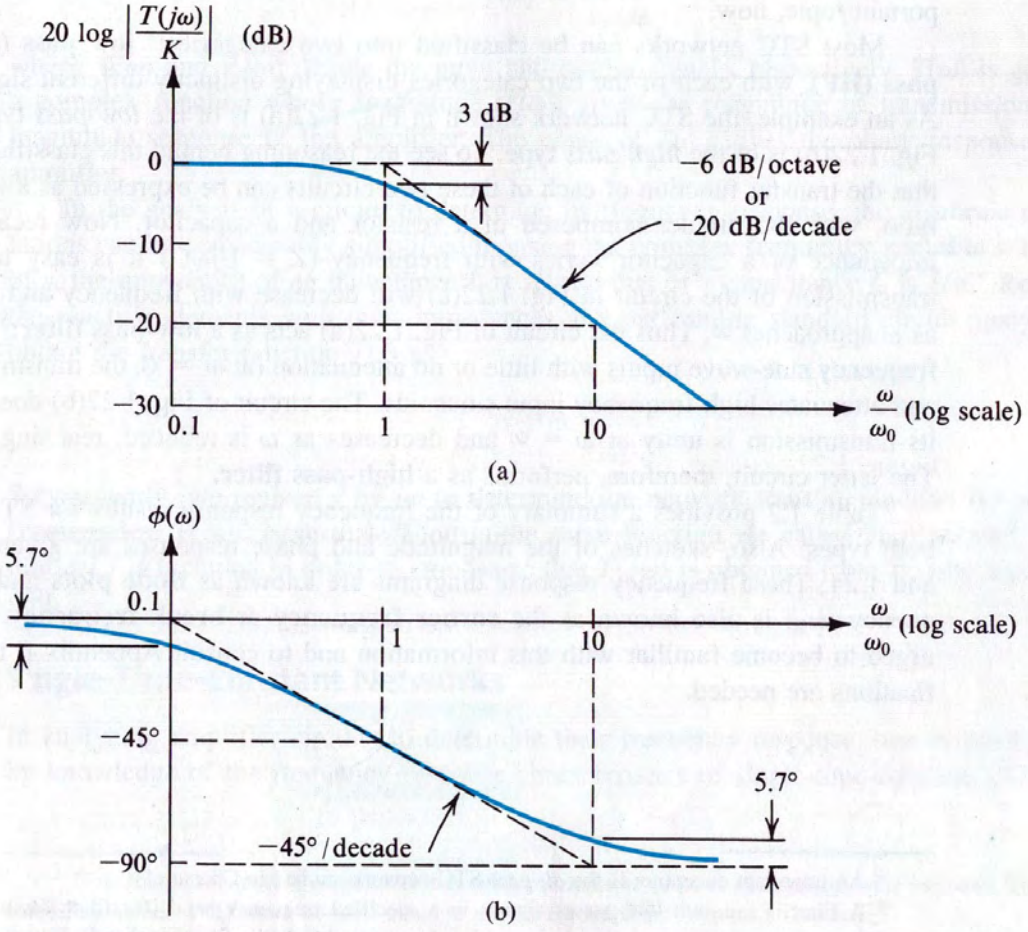


Fig. 1.23 **(a)** Magnitude and **(b)** phase response of STC networks of the low-pass type.

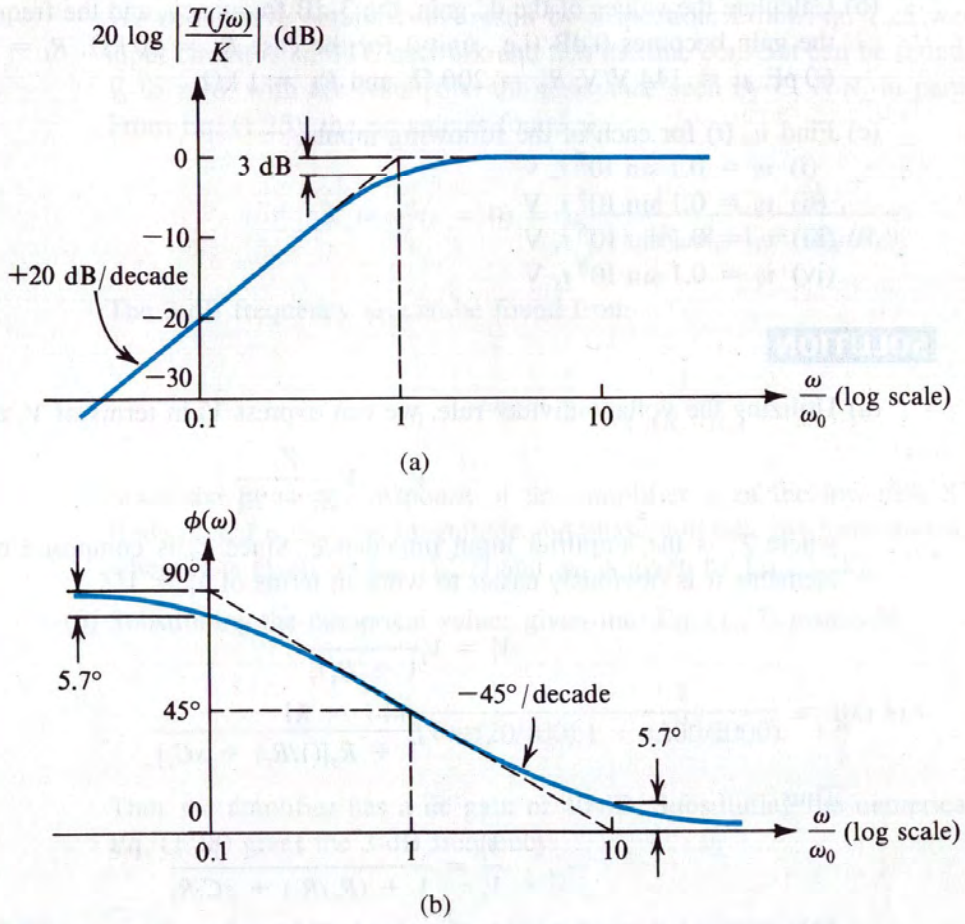


Fig. 1.24 **(a)** Magnitude and **(b)** phase response of STC networks of the high-pass type.

EXAMPLE 1.5

Figure 1.25 shows a voltage amplifier having an input resistance R_i, an input capacitance C_i, a gain factor μ, and an output resistance R_o. The amplifier is fed with a voltage source V_s having a source resistance R_s, and a load of resistance R_L is connected to the output.

(a) Derive an expression for the amplifier voltage gain V_o/V_s as a function of frequency. From this find expressions for the dc gain and the 3-dB frequency.

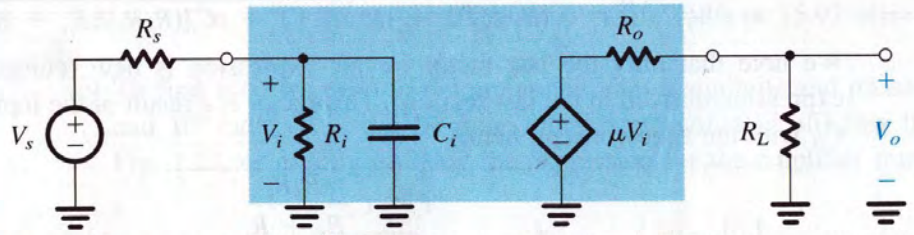


Fig. 1.25 Circuit for Example 1.5.

(b) Calculate the values of the dc gain, the 3-dB frequency, and the frequency at which the gain becomes 0 dB (i.e., unity) for the case $R_s = 20\ \text{k}\Omega$, $R_i = 100\ \text{k}\Omega$, $C_i = 60\ \text{pF}$, $\mu = 144\ \text{V/V}$, $R_o = 200\ \Omega$, and $R_L = 1\ \text{k}\Omega$.

(c) Find $v_o(t)$ for each of the following inputs:
(i) $v_i = 0.1 \sin 10^2 t$, V
(ii) $v_i = 0.1 \sin 10^5 t$, V
(iii) $v_i = 0.1 \sin 10^6 t$, V
(iv) $v_i = 0.1 \sin 10^8 t$, V

SOLUTION

(a) Utilizing the voltage-divider rule, we can express V_i in terms of V_s as follows

$$V_i = V_s \frac{Z_i}{Z_i + R_s}$$

where Z_i is the amplifier input impedance. Since Z_i is composed of two parallel elements it is obviously easier to work in terms of $Y_i = 1/Z_i$,

$$V_i = V_s \frac{1}{1 + R_s Y_i}$$
$$= V_s \frac{1}{1 + R_s[(1/R_i) + sC_i]}$$

Thus,

$$\frac{V_i}{V_s} = \frac{1}{1 + (R_s/R_i) + sC_iR_s}$$

This expression can be put in the standard form for a low-pass STC network (see the top line of Table 1.2) by extracting $[1 + (R_s/R_i)]$ from the denominator; thus we have

$$\frac{V_i}{V_s} = \frac{1}{1 + (R_s/R_i)} \frac{1}{1 + sC_i[(R_sR_i)/(R_s + R_i)]} \tag{1.24}$$

At the output side of the amplifier we can write

$$V_o = \mu V_i \frac{R_L}{R_L + R_o}$$

This equation can be combined with Eq. (1.24) to obtain the amplifier transfer function as

$$\frac{V_o}{V_s} = \mu \frac{1}{1 + (R_s/R_i)} \frac{1}{1 + (R_o/R_L)} \frac{1}{1 + sC_i[(R_sR_i)/(R_s + R_i)]} \tag{1.25}$$

We note that only the last factor in this expression is new (compared with the expression derived in the last section). This factor is a result of the input capacitance C_i, with the time constant being

$$\tau = C_i \frac{R_sR_i}{R_s + R_i}$$
$$= C_i(R_s // R_i) \tag{1.26}$$

We could have obtained this result by inspection: From Fig. 1.25 we see that the input circuit is an STC network and that its time constant can be found by reducing V_s to zero, with the result that the resistance seen by C_i is R_i in parallel with R_s. From Eq. (1.25), the dc gain is found as

$$K \equiv \frac{V_o}{V_s}(s = 0) = \mu \frac{1}{1 + (R_s/R_i)} \frac{1}{1 + (R_o/R_L)} \tag{1.27}$$

The 3-dB frequency ω_0 can be found from

$$\omega_0 = \frac{1}{\tau} = \frac{1}{C_i(R_s // R_i)} \tag{1.28}$$

Since the frequency response of this amplifier is of the low-pass STC type, the Bode plots for the gain magnitude and phase will take the form shown in Fig. 1.23, where K is given by Eq. (1.27) and ω_0 is given by Eq. (1.28).

(b) Substituting the numerical values given into Eq. (1.27) results in

$$K = 144 \frac{1}{1 + (20/100)} \frac{1}{1 + (200/1000)} = 100 \text{ V/V}$$

Thus the amplifier has a dc gain of 40 dB. Substituting the numerical values into Eq. (1.28) gives the 3-dB frequency

$$\omega_0 = \frac{1}{60 \text{ pF} \times (20 \text{ k}\Omega // 100 \text{ k}\Omega)}$$

$$= \frac{1}{60 \times 10^{-12} \times (20 \times 100/(20 + 100)) \times 10^3} = 10^6 \text{ rad/s}$$

Thus,

$$f_0 = \frac{10^6}{2\pi} = 159.2 \text{ kHz}$$

Since the gain falls off at the rate of -20 dB/decade, starting at ω_0 (see Fig. 1.23a) the gain will reach 0 dB in two decades; thus we have

$$\text{Unity-gain frequency} = 10^8 \text{ rad/s or } 15.92 \text{ MHz}$$

(c) To find $v_o(t)$ we need to determine the gain magnitude and phase at 10^2, 10^5, 10^6, and 10^8 rad/s. This can be done either approximately utilizing the Bode plots of Fig. 1.23, or exactly utilizing the expression for the amplifier transfer function,

$$T(j\omega) \equiv \frac{V_o}{V_s}(j\omega) = \frac{100}{1 + j(\omega/10^6)}$$

We shall do both:

(i) For $\omega = 10^2$ rad/s, which is $(\omega_0/10^4)$, the Bode plots of Fig. 1.23 suggest that $|T| \simeq K = 100$ and $\phi = 0°$. The transfer function expression gives $|T| \simeq 100$ and $\phi = -\tan^{-1} 10^{-4} \simeq 0°$. Thus

$$v_o(t) = 10 \sin 10^2 t, \text{ V}$$

(ii) For $\omega = 10^5$ rad/s, which is $(\omega_0/10)$, the Bode plots of Fig. 1.23 suggest that $|T| \simeq K = 100$ and $\phi = -5.7°$. The transfer function expression gives $|T| = 99.5$ and $\phi = -\tan^{-1} 0.1 = -5.7°$. Thus

$$v_o(t) = 9.95 \sin(10^5 t - 5.7°), \text{ V}$$

(iii) For $\omega = 10^6$ rad/s $= \omega_0$, $|T| = 100/\sqrt{2} = 70.7$ V/V or 37 dB and $\phi = -45°$. Thus

$$v_o(t) = 7.07 \sin(10^6 t - 45°), \text{ V}$$

(iv) For $\omega = 10^8$ rad/s, which is $(100\ \omega_0)$, the Bode plots suggest that $|T| = 1$ and $\phi = -90°$. The transfer function expression gives

$$|T| \simeq 1 \text{ and } \phi = -\tan^{-1} 100 = -89.4°,$$

Thus

$$v_o(t) = 0.1 \sin(10^8 t - 89.4°), \text{ V}$$

Classification of Amplifiers Based on Frequency Response

Amplifiers can be classified based on the shape of their magnitude-response curve. Figure 1.26 shows typical frequency response curves for various amplifier types. In Fig. 1.26(a) the gain remains constant over a wide frequency range but falls off at low and high frequencies. This is a common type of frequency response found in audio amplifiers.

As will be shown in Chapter 7, **internal capacitances** in the device (a transistor) cause the falloff of gain at high frequencies, just as C_i did in the circuit of Example 1.5. On the other hand, the falloff of gain at low frequencies is usually caused by **coupling capacitors** used to connect one amplifier stage to another, as indicated in Fig. 1.27. This practice is usually adopted to simplify the design process of the different stages. The coupling capacitors are usually chosen quite large (a fraction of a microfarad to a few tens of microfarads) so that their reactance (impedance) is small at the frequencies of interest. Nevertheless, at sufficiently low frequencies the reactance of a coupling capacitor will become large enough to cause part of the signal being coupled to appear as a voltage drop across the coupling capacitor and thus not reach the subsequent stage. Coupling capacitors will thus cause loss of gain at low frequencies and cause the gain to be zero at dc.

There are many applications in which it is important that the amplifier maintain its gain at low frequencies down to dc. Furthermore, monolithic integrated-circuit (IC) technology does not allow the fabrication of large coupling capacitors. Thus IC amplifiers are usually

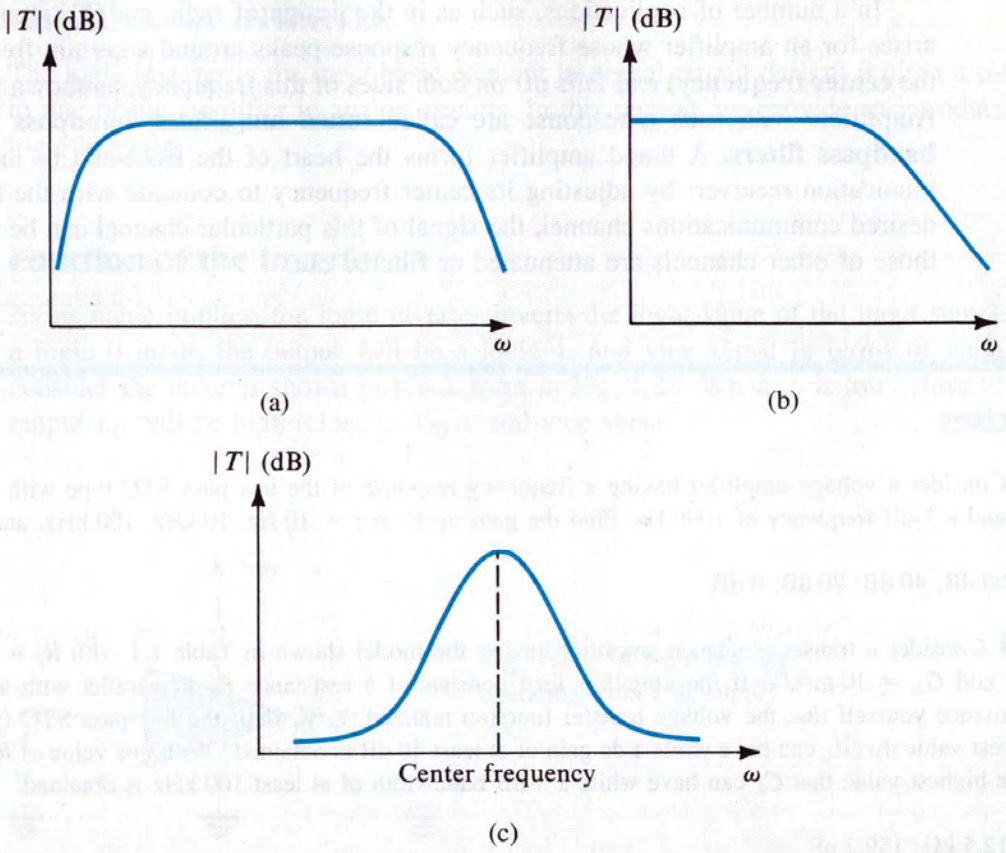


Fig. 1.26 Frequency response for **(a)** a capacitively coupled amplifier, **(b)** a direct-coupled amplifier, and **(c)** a tuned or bandpass amplifier.

designed as **directly coupled** or **dc amplifiers** (as opposed to **capacitively coupled** or **ac amplifiers**). Figure 1.26(b) shows the frequency response of a dc amplifier. Such a frequency response characterizes what is referred to as a **low-pass amplifier.** Although it is not very appropriate, the term low-pass amplifier is also often used to refer to the amplifier whose response is shown in Fig. 1.26(a).

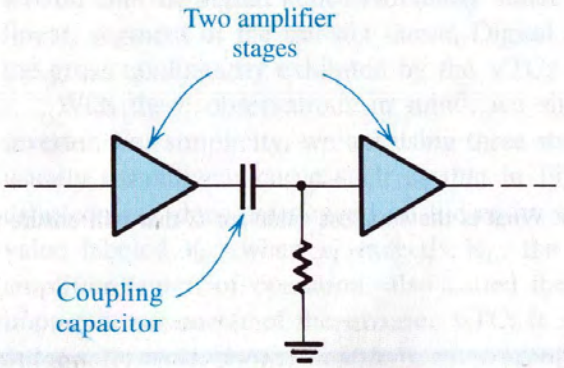


Fig. 1.27 Use of a capacitor to couple amplifier stages.

In a number of applications, such as in the design of radio and TV receivers, the need arises for an amplifier whose frequency response peaks around a certain frequency (called the **center frequency**) and falls off on both sides of this frequency, as shown in Fig. 1.26(c). Amplifiers with such a response are called **tuned amplifiers, bandpass amplifiers,** or **bandpass filters.** A tuned amplifier forms the heart of the front-end or tuner of a communication receiver; by adjusting its center frequency to coincide with the frequency of a desired communications channel, the signal of this particular channel can be received while those of other channels are attenuated or filtered out.

Exercises

1.15 Consider a voltage amplifier having a frequency response of the low-pass STC type with a dc gain of 60 dB and a 3-dB frequency of 1000 Hz. Find the gain in dB at f = 10 Hz, 10 kHz, 100 kHz, and 1 MHz.

Ans. 60 dB; 40 dB; 20 dB; 0 dB

D1.16 Consider a transconductance amplifier having the model shown in Table 1.1 with $R_i = 5\ \text{k}\Omega$, $R_o = 50\ \text{k}\Omega$, and $G_m = 10\ \text{mA/V}$. If the amplifier load consists of a resistance R_L in parallel with a capacitance C_L, convince yourself that the voltage transfer function realized, V_o/V_i, is of the low-pass STC type. What is the lowest value that R_L can have while a dc gain of at least 40 dB is obtained? With this value of R_L connected, find the highest value that C_L can have while a 3-dB bandwidth of at least 100 kHz is obtained.

Ans. 12.5 kΩ; 159.2 pF

D1.17 Consider the situation illustrated in Fig. 1.27. Let the output resistance of the first voltage amplifier be 1 kΩ and the input resistance of the second voltage amplifier (including the resistor shown) be 9 kΩ. The resulting equivalent circuit is shown in Fig. E1.17 where V_s and R_s are the output voltage and output resistance of the first amplifier, C is a coupling capacitor, and R_i is the input resistance of the second amplifier. Convince

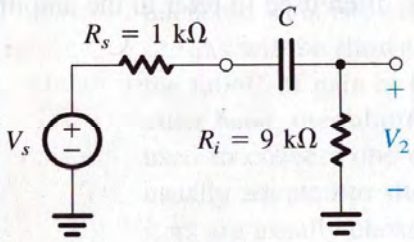


Fig. E1.17

yourself that V_2/V_s is a high-pass STC function. What is the smallest value for C that will ensure that the 3-dB frequency is not higher than 100 Hz?

Ans. 0.16 μF

1.7 THE DIGITAL LOGIC INVERTER

The logic inverter is the most basic element in digital circuit design; it plays a role parallel to that of the amplifier in analog circuits. In this section, we provide an introduction to the logic inverter.

Function of the Inverter

As its name implies, the logic inverter inverts the logic value of the input signal. Thus for a logic 0 input, the output will be a logic 1, and vice versa. In terms of voltage levels, consider the inverter shown in block form in Fig. 1.28: When v_I is low (close to 0 V), the output v_O will be high (close to V_{DD}), and vice versa.

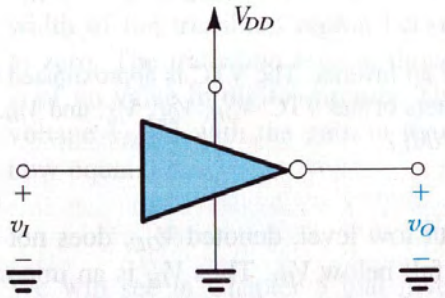


Fig. 1.28 A logic inverter operating from a dc supply V_{DD}.

The Voltage Transfer Characteristic (VTC)

To quantify the operation of the inverter, we utilize its voltage transfer characteristic (VTC, as it is usually abbreviated). First we refer the reader to the amplifier considered in Example 1.2 whose transfer characteristic is sketched in Fig. 1.15. Observe that the transfer characteristic indicates that this inverting amplifier can be used as a logic inverter. Specifically, if the input is high ($v_I > 0.690$ V), v_O will be low at 0.3 V. On the other hand, if the input is low (close to 0 V), the output will be high (close to 10 V). Thus, to use this amplifier as a logic inverter, we utilize its extreme regions of operation. This is exactly the opposite to its use as a signal amplifier where it would be biased at the middle of the transfer characteristic and the signal kept sufficiently small so as to restrict operation to a short, almost linear, segment of the transfer curve. Digital applications, on the other hand, make use of the gross nonlinearity exhibited by the VTC.

With these observations in mind, we show in Fig. 1.29 a possible VTC of a logic inverter. For simplicity, we are using three straight lines to approximate the VTC, which is usually a nonlinear curve such as that in Fig. 1.15. Observe that the output high level, denoted V_{OH}, does not depend on the exact value of v_I as long as v_I does not exceed the value labeled V_{IL}; when v_I exceeds V_{IL}, the output decreases and the inverter enters its amplifier region of operation, also called the **transition region.** It follows that V_{IL} is an important parameter of the inverter VTC: It is the *maximum value that v_I can have while being interpreted by the inverter as representing a logic 0.*

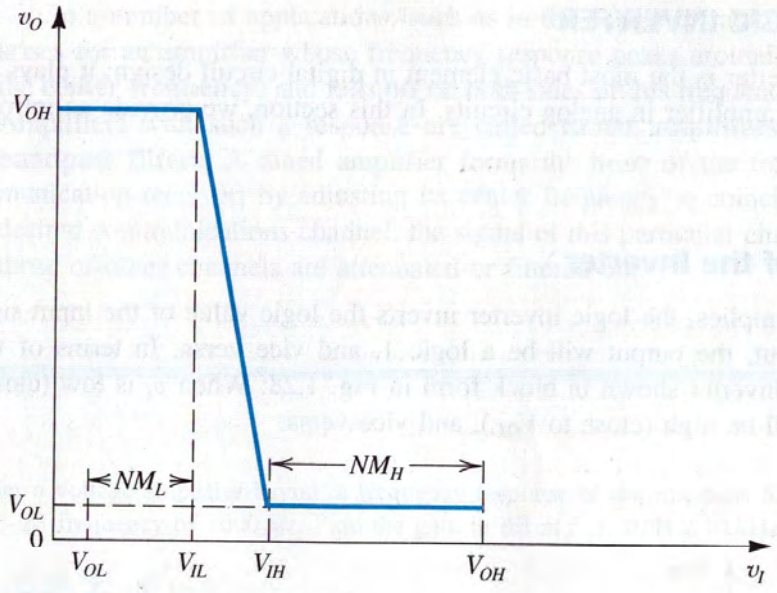


Fig. 1.29 Voltage transfer characteristic of an inverter. The VTC is approximated by three straight-line segments. Note the four parameters of the VTC: V_{OH}, V_{OL}, V_{IL}, and V_{IH}, and their use in determining the noise margins NM_H and NM_L.

Similarly, we observe that the output low level, denoted V_{OL}, does not depend on the exact value of v_I as long as v_I does not fall below V_{IH}. Thus V_{IH} is an important parameter of the inverter VTC: It is the *minimum value that v_I can have while being interpreted by the inverter as representing a logic 1.*

Noise Margins

The insensitivity of the inverter output to the exact value of v_I within allowed regions is a great advantage that digital circuits have over analog circuits. To quantify this insensitivity property, consider the situation that occurs often in a digital system where an inverter (or a logic gate based on the inverter circuit) is driving another similar inverter. If the output of the driving inverter is high at V_{OH}, we see that we have a "margin of safety" equal to the difference between V_{OH} and V_{IH} (see Fig. 1.29). In other words, if for some reason, a disturbing signal (called "electric noise," or simply **noise**) is superimposed on the output of the driving inverter, the driven inverter would not be "bothered" so long as this noise does not decrease the voltage at its input below V_{IH}. Thus we can say that the inverter has a **noise margin for high input,** NM_H, of

$$NM_H = V_{OH} - V_{IH} \tag{1.29}$$

Similarly, if the output of the driving inverter is low at V_{OL}, the driven inverter will provide a high output even if noise corrupts the V_{OL} level at its input, raising it up to nearly V_{IL}. Thus we can say that the inverter exhibits a **noise margin for low input,** NM_L, of

$$NM_L = V_{IL} - V_{OL} \tag{1.30}$$

In summary, four parameters, V_{OH}, V_{OL}, V_{IH}, and V_{IL}, define the VTC of an inverter and determine its noise margins, which in turn measure the ability of the inverter to tolerate

variations in the input signal levels. In this regard, observe that changes in the input signal level within the noise margins are *rejected* by the inverter. Thus noise is not allowed to propagate further through the system. Alternatively, we can think of the inverter as *restoring* the signal levels to standard values (V_{OL} and V_{OH}) even when it is presented with corrupted signal levels (within the noise margins).

The Ideal VTC

The question naturally arises as to what constitutes an ideal VTC for an inverter. The answer follows directly from the preceding discussion: An ideal VTC is one that maximizes the noise margins and distributes them equally between the low and high input regions. Such a VTC is shown in Fig. 1.30 for an inverter operated from a dc supply V_{DD}. Observe that the output high level V_{OH} is at its maximum possible value of V_{DD}, and the output low level is at its minimum possible value of 0 V. Observe also that the threshold voltages V_{IL} and V_{IH} are equalized and placed at the middle of the power supply voltage ($V_{DD}/2$). Thus the width of the transition region between the high and low output regions has been reduced to zero. The transition region, though obviously very important for amplifier applications, is of no value in digital circuits. The ideal VTC exhibits a steep transition at the threshold voltage $V_{DD}/2$ with the gain in the transition region being infinite. The noise margins are now equal:

$$NM_H = NM_L = V_{DD}/2 \tag{1.31}$$

We will see in Chapter 5 that inverter circuits designed using the complementary metal-oxide-semiconductor (or CMOS) technology come very close to realizing the ideal VTC.

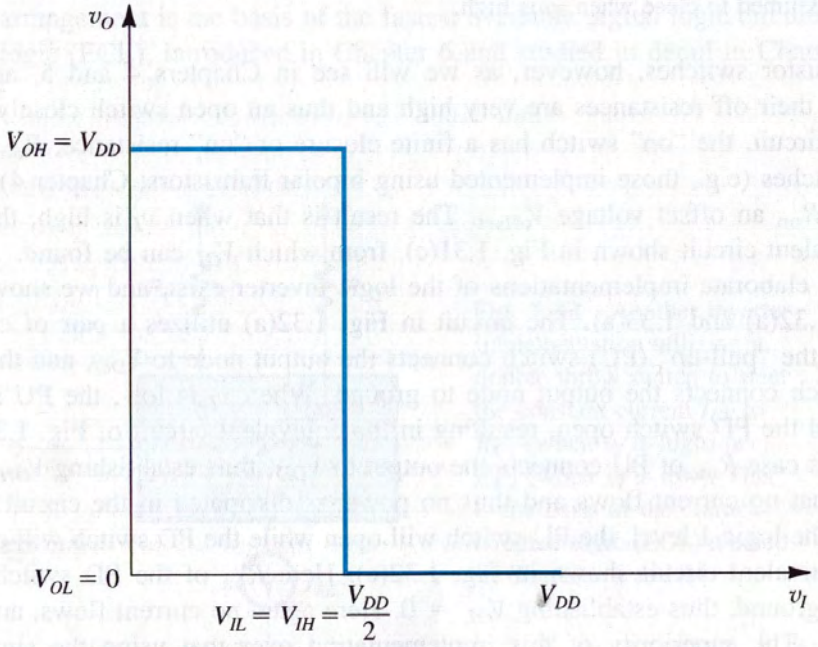


Fig. 1.30 The VTC of an ideal inverter.

Inverter Implementation

Inverters are implemented using transistors (Chapters 4 and 5) operating as voltage-controlled switches. The simplest inverter implementation is shown in Fig. 1.31. The switch is controlled by the inverter input voltage v_I. When v_I is low, the switch will be open and $v_O = V_{DD}$ since no current flows through R. When v_I is high, the switch will be closed and, assuming an ideal switch, $v_O = 0$.

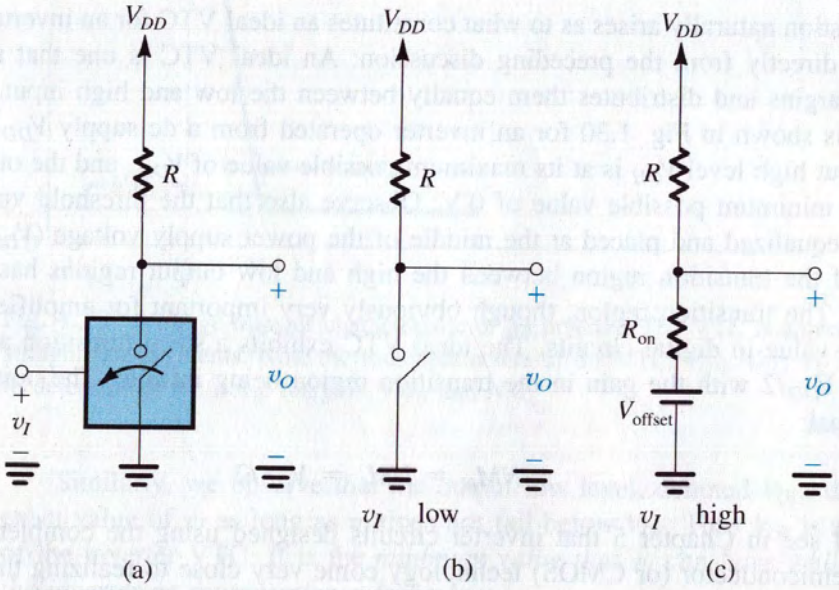


Fig. 1.31 **(a)** The simplest implementation of a logic inverter using a voltage-controlled switch; **(b)** equivalent circuit when v_I is low; and **(c)** equivalent circuit when v_I is high. Note that the switch is assumed to close when v_I is high.

Transistor switches, however, as we will see in Chapters 4 and 5, are not perfect. Although their off resistances are very high and thus an open switch closely approximates an open circuit, the "on" switch has a finite closure or "on" resistance, R_{on}. Furthermore, some switches (e.g., those implemented using bipolar transistors; Chapter 4) exhibit in addition to R_{on} an offset voltage V_{offset}. The result is that when v_I is high, the inverter has the equivalent circuit shown in Fig. 1.31(c), from which V_{OL} can be found.

More elaborate implementations of the logic inverter exist, and we show two of these in Figs. 1.32(a) and 1.33(a). The circuit in Fig. 1.32(a) utilizes a pair of complementary switches, the "pull-up" (PU) switch connects the output node to V_{DD}, and the "pull-down" (PD) switch connects the output node to ground. When v_I is low, the PU switch will be closed and the PD switch open, resulting in the equivalent circuit of Fig. 1.32(b). Observe that in this case R_{on} of PU connects the output to V_{DD}, thus establishing $V_{OH} = V_{DD}$. Also observe that no current flows and thus no power is dissipated in the circuit. Next, if v_I is raised to the logic 1 level, the PU switch will open while the PD switch will close, resulting in the equivalent circuit shown in Fig. 1.32(c). Here R_{on} of the PD switch connects the output to ground, thus establishing $V_{OL} = 0$. Here again no current flows, and no power is dissipated. The superiority of this implementation over that using the single pull-down switch and a resistor (known as a pull-up resistor) should be obvious. This circuit constitutes the basis of the CMOS inverter that we will study in Section 5.9. Note that we have not

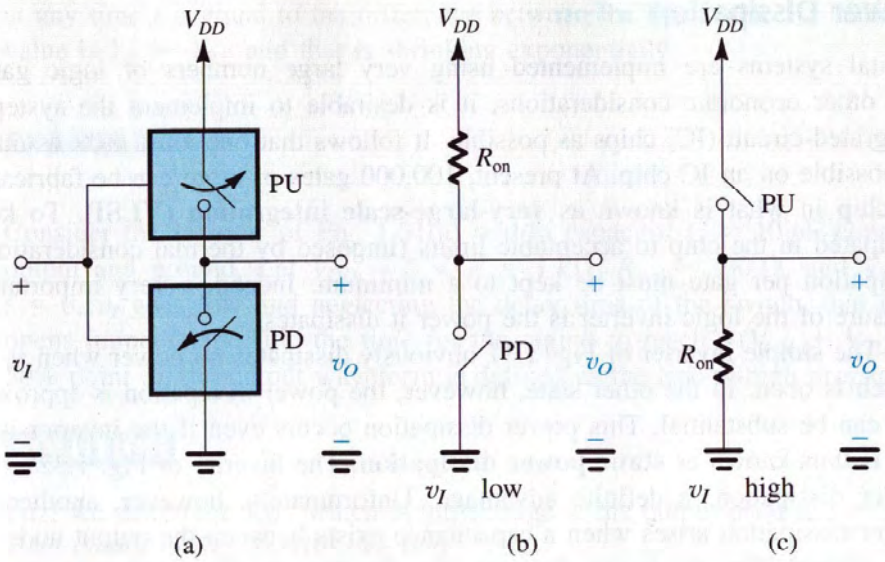


Fig. 1.32 A more elaborate implementation of the logic inverter utilizing two complementary switches. This is the basis of the CMOS inverter studied in Section 5.9.

included offset voltages in the equivalent circuits because MOS switches do not exhibit a voltage offset (Chapter 5).

Finally, consider the inverter implementation of Fig. 1.33. Here a double-throw switch is used to steer the constant current I_{EE} into one of two resistors connected to the positive supply V_{CC}. The reader is urged to show that if a high v_I results in the switch being connected to R_{C1}, then a logic inversion-function is realized at v_{O1}. Note that the output voltage is independent of the switch resistance. This *current-steering* or *current-mode* logic arrangement is the basis of the fastest available digital logic circuits, called emitter-coupled logic (ECL), introduced in Chapter 6 and studied in detail in Chapter 14.

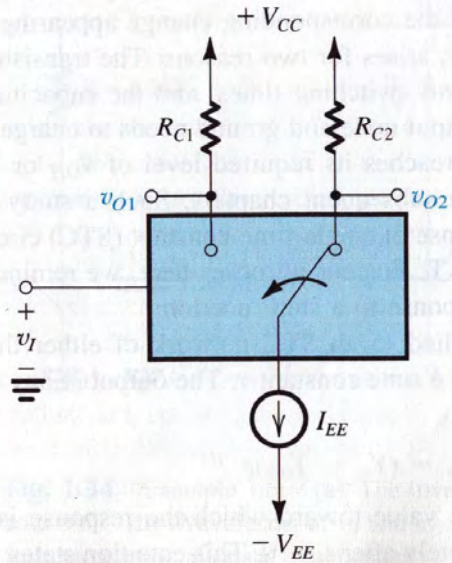


Fig. 1.33 Another inverter implementation utilizing a double-throw switch to steer the constant current I_{EE} to R_{C1} (when v_I is high) or R_{C2} (when v_I is low). This is the basis of the emitter-coupled logic (ECL) studied in Chapters 6 and 14.

Power Dissipation

Digital systems are implemented using very large numbers of logic gates. For space and other economic considerations, it is desirable to implement the system with as few integrated-circuit (IC) chips as possible. It follows that one must pack as many logic gates as possible on an IC chip. At present, 100,000 gates or more can be fabricated on a single IC chip in what is known as **very-large-scale integration (VLSI).** To keep the power dissipated in the chip to acceptable limits (imposed by thermal considerations), the power dissipation per gate must be kept to a minimum. Indeed, a very important performance measure of the logic inverter is the power it dissipates.

The simple inverter of Fig. 1.31 obviously dissipates no power when v_I is low and the switch is open. In the other state, however, the power dissipation is approximately V_{DD}^2/R and can be substantial. This power dissipation occurs even if the inverter is not switching and is thus known as **static power dissipation.** The inverter of Fig. 1.32 exhibits no static power dissipation, a definite advantage. Unfortunately, however, another component of power dissipation arises when a capacitance exists between the output node of the inverter and ground. This is always the case, for the devices that implement the switches have internal capacitances, the wires that connect the inverter output to other circuits have capacitance, and, of course, there is the input capacitance of whatever circuit the inverter is driving. Now, as the inverter is switched from one state to another, current must flow through the switch(es) to charge (and discharge) the load capacitance. These currents give rise to power dissipation in the switches, called **dynamic power.** In Chapter 5, we shall study dynamic power dissipation in the CMOS inverter, and we shall show that an inverter switched at a frequency f Hz exhibits a dynamic power dissipation

$$P_{\text{dynamic}} = fCV_{DD}^2 \tag{1.32}$$

where C is the capacitance between the output node and ground, and V_{DD} is the power-supply voltage. This result applies (approximately) to all inverter circuits.

Propagation Delay

Whereas the dynamic behavior of amplifiers is specified in terms of their frequency response, that of inverters is characterized in terms of the time delay between switching of v_I (from low to high or vice versa) and the corresponding change appearing at the output. Such a delay, called **propagation delay,** arises for two reasons: The transistors that implement the switches exhibit finite (nonzero) switching times, and the capacitance that is inevitably present between the inverter output node and ground needs to charge (or discharge, as the case may be) before the output reaches its required level of V_{OH} or V_{OL}. We shall analyze the inverter switching times in subsequent chapters. Such a study depends on a thorough familiarity with the time response of single-time-constant (STC) circuits. A review of this subject is presented in Appendix F. For our purposes here, we remind the reader of the key equation in determining the response to a step function:

Consider a step-function input applied to an STC network of either the low-pass or high-pass type, and let the network have a time constant τ. The output at any time t is given by

$$y(t) = Y_\infty - (Y_\infty - Y_{0+})e^{-t/\tau} \tag{1.33}$$

where Y_∞ is the final value, that is, the value toward which the response is heading, and Y_{0+} is the value of the response immediately after $t = 0$. This equation states that the output

at any time t is equal to the difference between the final value Y_∞ and a gap whose initial value is $Y_\infty - Y_{0+}$ and that is shrinking exponentially.

EXAMPLE 1.6

Consider the inverter of Fig. 1.31(a) with a capacitor $C = 10$ pF connected between the output and ground. Let $V_{DD} = 5$ V, $R = 1$ kΩ, $R_{on} = 100\ \Omega$, and $V_{offset} = 0.1$ V. If at $t = 0$, v_I goes low and neglecting the delay time of the switch, that is, assuming that it opens immediately, find the time for the output to reach $\frac{1}{2}(V_{OH} + V_{OL})$. The time to this 50% point on the output waveform is defined as the low-to-high propagation delay, t_{PLH}.

SOLUTION

First we determine V_{OL}, which is the voltage at the output prior to $t = 0$. From the equivalent circuit in Fig. 1.31(b), we find

$$V_{OL} = V_{offset} + \frac{V_{DD} - V_{offset}}{R + R_{on}} R_{on}$$
$$= 0.1 + \frac{5 - 0.1}{1.1} \times 0.1 = 0.55\ \text{V}$$

Next, when the switch opens at $t = 0$, the circuit takes the form shown in Fig. 1.34(a). Since the voltage across the capacitor cannot change instantaneously, at $t = 0+$ the output

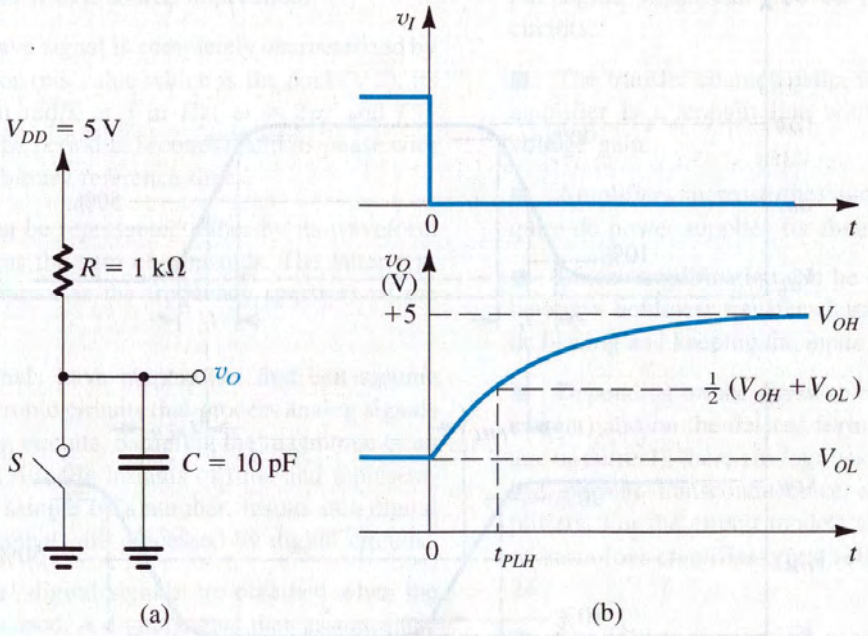


Fig. 1.34 Example 1.6: **(a)** The inverter circuit after the switch opens (i.e., for $t \geq 0+$. **(b)** Waveforms of v_I and v_O. Observe that the switch is assumed to operate instantaneously. v_O rises exponentially, starting at V_{OL} and heading toward V_{OH}.

will still be 0.55 V. Then the capacitor charges through R, and v_O rises exponentially toward V_{DD}. The output waveform will be as shown in Fig. 1.34(b), and its equation can be obtained by substituting in Eq. (1.33), $v_O(\infty) = 5$ V and $v_O(0+) = 0.55$ V. Thus

$$v_O(t) = 5 - (5 - 0.55)e^{-t/\tau}$$

where $\tau = CR$. To find t_{PLH}, we substitute

$$v_O(t_{PLH}) = \frac{1}{2}(V_{OH} + V_{OL})$$
$$= \frac{1}{2}(5 + 0.55)$$

The result is

$$t_{PLH} = 0.69\,\tau$$
$$= 0.69\,RC$$
$$= 0.69 \times 10^3 \times 10^{-11}$$
$$= 6.9 \text{ ns}$$

We conclude this section by showing in Fig. 1.35 the formal definition of the propagation delay of an inverter. As shown, an input pulse with finite (nonzero) **rise and fall times** is applied. The inverted pulse at the output exhibits finite rise and fall times (labeled t_{TLH} and t_{THL}, where the subscript T denotes transition, LH denotes low-to-high, and HL denotes high-to-low). There is also a delay time between the input and output forms. The usual way to specify the propagation delay is to take the average of the high-to-low propagation delay, t_{PHL}, and the low-to-high propagation delay, t_{PLH}. As indicated, these delays are measured

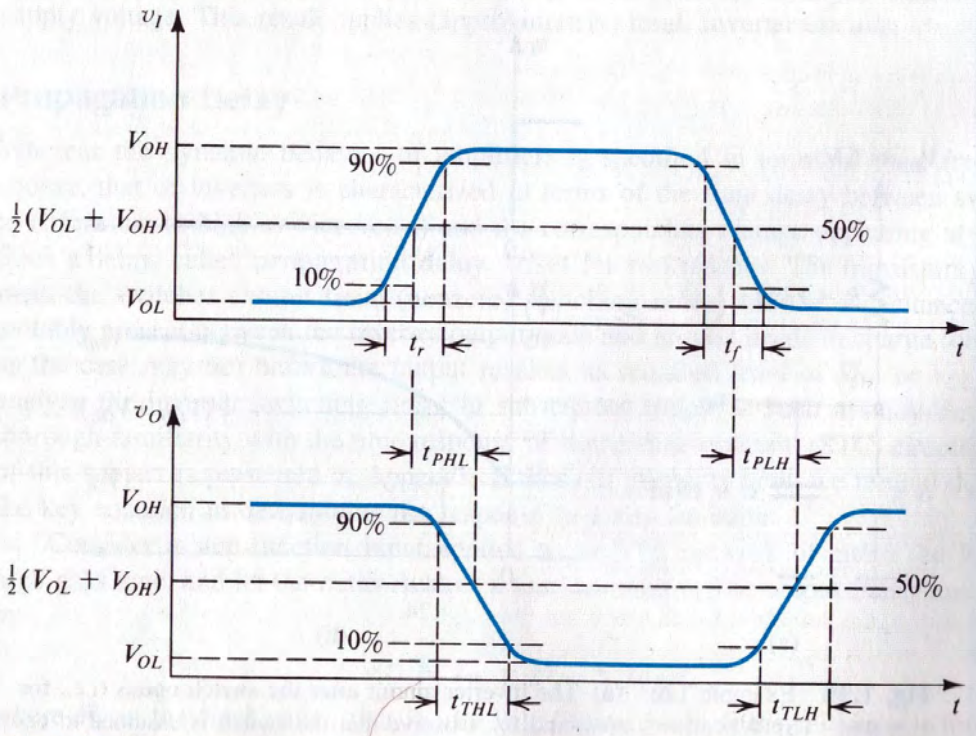


Fig. 1.35 Definitions of propagation delays and transition times of the logic inverter.

between the 50% points of the input and output waveforms. Also note that the transition times are specified using the 10% and 90% points of the output excursion ($V_{OH} - V_{OL}$).

Exercises

1.18 For the inverter in Fig. 1.31, let $V_{DD} = 5$ V, $R = 1$ kΩ, $R_{on} = 100\ \Omega$, $V_{offset} = 0.1$ V, $V_{IL} = 0.8$ V, and $V_{IH} = 1.2$ V. Find V_{OH}, V_{OL}, NM_H, and NM_L. Also find the average static power dissipation assuming that the inverter spends half the time in each of its two states.

Ans. 5 V; 0.55 V; 3.8 V; 0.25 V; 11.1 mW

1.19 Find the dynamic power dissipated in an inverter operated from a 5-V power supply. The inverter has a 2-pF capacitance load and is switched at 50 MHz.

Ans. 2.5 mW

SUMMARY

- An electrical signal source can be represented in either the Thévenin form (a voltage source in series with a source impedance) or the Norton form (a current source in parallel with a source impedance).
- The sine-wave signal is completely characterized by its peak value (or rms value which is the peak/$\sqrt{2}$), its frequency (ω in rad/s or f in Hz; $\omega = 2\pi f$ and $f = 1/T$ where T is the period in seconds), and its phase with respect to an arbitrary reference time.
- A signal can be represented either by its waveform versus time, or as the sum of sinusoids. The latter representation is known as the frequency spectrum of the signal.
- Analog signals have magnitudes that can assume any value. Electronic circuits that process analog signals are called analog circuits. Sampling the magnitude of an analog signal at discrete instants of time and representing each signal sample by a number, results in a digital signal. Digital signals are processed by digital circuits.
- The simplest digital signals are obtained when the binary system is used. A digital signal then assumes one of only two possible values: low and high (say, 0 V and +5 V), corresponding to logic 0 and logic 1, respectively.
- An analog-to-digital converter (ADC) provides at its output the digits of the binary number representing the analog signal sample applied to its inputs. The output digital signal can then be processed using digital circuits.
- The transfer characteristic, v_O versus v_I, of a linear amplifier is a straight line with a slope equal to the voltage gain.
- Amplifiers increase the signal power and thus require dc power supplies for their operation.
- Linear amplification can be obtained from a device having a nonlinear transfer characteristic by employing dc biasing and keeping the input signal amplitude small.
- Depending on the signal to be amplified (voltage or current) and on the desired form of output signal (voltage or current), there are four basic amplifier types: voltage, current, transconductance, and transresistance amplifiers. For the circuit models and ideal characteristics of these four amplifier types, refer to Table 1.1 on page 24.
- Sinusoidal signals are used to measure the frequency response of amplifiers.
- The transfer function $T(s) \equiv V_o(s)/V_i(s)$ of a voltage

amplifier can be determined from circuit analysis. Substituting $s = j\omega$ gives $T(j\omega)$, whose magnitude $|T(j\omega)|$ is the magnitude response, and whose phase $\phi(\omega)$ is the phase response, of the amplifier.

■ Amplifiers are classified according to the shape of their frequency response, $|T(j\omega)|$.

■ Single-time-constant (STC) networks are those networks that are composed of, or can be reduced to, one reactive component (L or C) and one resistance (R). The time constant τ is either L/R or CR.

■ STC networks can be classified into two categories: low-pass (LP) and high-pass (HP). LP networks pass dc and low frequencies and attenuate high frequencies. The opposite is true for HP networks.

■ The gain of an LP (HP) STC circuit drops by 3 dB below the zero-frequency (infinite-frequency) value at a frequency $\omega_0 = 1/\tau$. At high frequencies (low frequencies) the gain falls off at the rate of 6 dB/octave or 20 dB/decade. Refer to Table 1.2 on page 32 and Figs. (1.23) and (1.24).

■ The digital logic inverter is the basic building block of digital circuits, just as the amplifier is the basic building block of analog circuits.

■ The static operation of the inverter is described by its voltage transfer characteristic (VTC). The breakpoints of the transfer characteristic determine the inverter noise margins; refer to Fig. 1.29. In particular, note that $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$.

■ The inverter is implemented using transistors operating as voltage-controlled switches. The arrangement utilizing two switches operated in a complementary fashion results in a high-performance inverter.

■ An important performance parameter of the inverter is the amount of power it dissipates. There are two components of power dissipation: static and dynamic. The first is a result of current flow in either the 0 or 1 state. The second occurs when the inverter is switched and has a capacitor load. Dynamic power dissipation is given approximately by fCV_{DD}^2.

■ Another very important performance parameter of the inverter is its propagation delay (see Fig. 1.35 for definitions).

BIBLIOGRAPHY

E. F. Angelo, Jr., *Electronics: BJTs, FETs, and Microcircuits,* New York: McGraw-Hill, 1969.

L. S. Bobrow, *Elementary Linear Circuit Analysis,* 2nd ed., New York: Holt, Rinehart and Winston, 1987.

W. H. Hayt and J. E. Kemmerly, *Engineering Circuit Analysis,* 3rd ed., New York: McGraw-Hill, 1978.

Scientific American, Special Issue on Microelectronics, Sept. 1977.

M. E. Van Valkenburg, *Network Analysis,* 3rd ed., Englewood Cliffs, N.J.: Prentice-Hall, 1974.

PROBLEMS[1,2]

Section 1.1: Signals

1.1 For the signal-source representations shown in Figs. 1.1(a) and 1.1(b), what are the open-circuit output voltages that would be observed? If, for each, the output terminals are short-circuited (that is, wired together), what current would flow? For the representations to be equivalent, what must the relationship be between v_s, i_s, and R_s?

[1] Somewhat difficult problems are marked with an asterisk (*); more difficult problems are marked with two asterisks (**); and very difficult (and/or time-consuming) problems are marked with three asterisks (***).

[2] Design-oriented problems are marked with a D.

1.2 A signal source has an open-circuit voltage of 10 mV and a short-circuit current of 10 μA. What is the source resistance?

Section 1.2: Frequency Spectrum of Signals

1.3 Give expressions for the sine-wave voltage signals having:
(a) 10-V peak amplitude and 10-kHz frequency.
(b) 120-V rms and 60-Hz frequency.
(c) 0.2-V peak-to-peak and 1000-rad/s frequency.
(d) 100-mV peak and 1-ms period.

1.4 Measurements taken of a square-wave signal using a frequency-selective voltmeter (called a spectrum analyzer) show its spectrum to contain adjacent components (spectral lines) at 98 kHz and 126 kHz, of amplitudes 63 mV and 49 mV, respectively. For this signal, what would direct measurement of the fundamental show its frequency and amplitude to be? What is the rms value of the fundamental? What are the peak-to-peak amplitude and period of the originating square wave?

1.5 For a square-wave audio signal of 10 kHz, what fraction of the available energy is perceived by an average adult listener of age 40 whose hearing extends only to 16 kHz?

1.6 What fraction of the energy contained in a square wave of frequency f and peak-to-peak amplitude 2 V is contained in the harmonic at frequency $9f$?

Section 1.3: Analog and Digital Signals

D1.7 A young engineer, engaged in the early stages of design of a new product, begins to evaluate various techniques available for information presentation. One of the requirements of the design is to display a value proportional to the amount by which an internal voltage variable exceeds zero. Among the many options he considers is the use of a one-digit or two-digit LED display. In either case, the zero value is not displayed. Moreover, in the two-digit case, leading zeros must be suppressed. More than two digits is clearly too costly, uses too much space, and is more precise than needed. Some of the questions he asks himself are the following: In each case: (a) What is the number of distinct values that can be displayed? (b) What is the largest ("full-scale") value? What is the smallest value? What is the "dynamic range" (expressed by the ratio of the largest to smallest displayed value as "L to S," or as an integer)? What is the "precision" (expressed by the ratio of the minimum display change to the full-scale value, as a percentage)?

1.8 Give the binary representation of the following decimal numbers: 0, 7, 12, 33, and 57.

1.9 Consider an N-bit ADC whose analog input varies between 0 and V_{FS} (where the subscript FS denotes "full scale").
(a) Show that the least significant bit (LSB) corresponds to a change in the analog signal of $\frac{V_{FS}}{2^N - 1}$. This is the resolution of the converter.
(b) Convince yourself that the maximum error in the conversion (called the quantization error) is half the resolution, that is, the quantization error $= V_{FS}/2(2^N - 1)$.
(c) For $V_{FS} = 10$ V, how many bits are required to obtain a resolution of 10 mV or better? What is the actual resolution obtained? What is the quantization error resulting?

1.10 Figure P1.10 shows the circuit of an N-bit digital-to-analog converter (DAC). Each of the N bits of the digital word to be converted controls one of the switches. When the bit is 0, the switch is in the position labeled 0; when the bit is 1, the switch is in the position labeled 1. The analog output is the current i_O. V_{ref} is a constant reference voltage.
(a) Show that

$$i_O = \frac{V_{\text{ref}}}{R}\left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N}\right)$$

(b) Which bit is the LSB? Which is the MSB?
(c) For $V_{\text{ref}} = 5$ V, $R = 5$ kΩ, and $N = 4$, find the maximum value of i_O obtained. What is the change in i_O resulting from the LSB changing from 0 to 1?

Section 1.4: Amplifiers

1.11 A particular audio power amplifier requires an input sinusoidal signal of 1 V rms to produce an output of 0.5 V peak. The amplifier's input resistance is 120 kΩ. The load is a small loudspeaker with an equivalent resistance of 8 Ω. What volt-

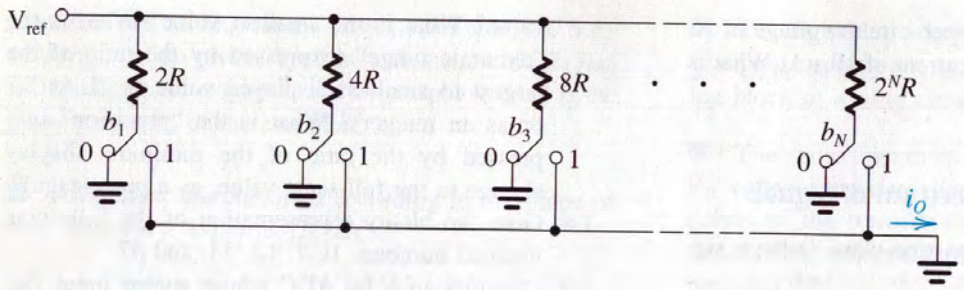


Fig. P1.10

age gain, current gain, and power gain characterize this system? Express each as a ratio and in dB.

1.12 An amplifier has a current gain of 60 dB and a power gain of 50 dB. Find its voltage gain.

1.13 An amplifier operating from ±15-V power supplies delivers an output sine-wave signal of 24 V peak-to-peak to a 2-kΩ load resistance. The amplifier draws an average current of 2 mA from each of its two power supplies and a negligible current from the input signal source. Find the power dissipated in the amplifier circuit.

1.14 An amplifier operating from ±15-V power supplies has a linear transfer characteristic except for output saturation at ±13 V. If the amplifier gain is 100 V/V, find the rms value of the largest sine-wave signal that can be applied at the input without output clipping.

D*1.15 An amplifier designed using a single metal-oxide-semiconductor (MOS) transistor has the transfer characteristic

$$v_O = 10 - 5(v_I - 2)^2$$

where v_I and v_O are in volts. This transfer characteristic applies for $2 \le v_I \le v_O + 2$ and v_O positive. At the limits of this region the amplifier saturates.

(a) Sketch and clearly label the transfer characteristic. What are the saturation levels L_+ and L_- and the corresponding values of v_I?

(b) Bias the amplifier to obtain a dc output voltage of 5 V. What value of input dc voltage V_I is required?

(c) Calculate the value of the small-signal voltage gain at the bias point.

(d) If a sinusoidal input signal is superimposed on the dc bias voltage V_I, that is,

$$v_I = V_I + V_i \cos \omega t$$

find the resulting v_O. Using the trigonometric identity $\cos^2 \theta = \frac{1}{2} + \frac{1}{2} \cos 2\theta$, express v_O as the sum of a dc component, a signal component with frequency ω, and a sinusoidal component with frequency 2ω. The latter component is undesirable and is a result of the nonlinear transfer characteristic of the amplifier. If it is required to limit the ratio of the second-harmonic component to the fundamental component to 1% (this ratio is known as the second-harmonic distortion) what is the corresponding upper limit on V_i?

D1.16 A transistor amplifier has a transfer characteristic that can be described by the equation

$$v_O = 17 - 10\, v_I$$

for $0.3\ \text{V} \le v_O \le 10\ \text{V}$. At the limits of this range, the amplifier saturates. Sketch the transfer characteristic and find the value of the dc input voltage V_I required to bias the amplifier so that the dc output voltage is 5 V. For signals v_i superimposed on the bias voltage V_I, find the amplifier voltage gain. If v_i is sinusoidal find its largest possible amplitude without output clipping.

Section 1.5: Circuit Models for Amplifiers

1.17 Consider the voltage-amplifier circuit model shown in Fig. 1.17(b), in which $A_{v_o} = 10$ V/V under the following conditions:

(a) $R_i = 10R_s$, $R_L = 10R_o$

(b) $R_i = R_s$, $R_L = R_o$

(c) $R_i = R_s/10$, $R_L = R_o/10$

Calculate the overall voltage gain v_o/v_s in each case, expressed both directly and in dB.

1.18 An amplifier with 40 dB of small-signal open-circuit voltage gain, an input resistance of 1MΩ,

and an output resistance of 10 Ω, drives a load of 100 Ω. What voltage and power gains (expressed in dB) would you expect with the load connected? If the amplifier has a peak output-current limitation of 100 mA, what is the rms value of the largest sine-wave input for which an undistorted output is possible? What is the corresponding output power available?

D1.19 A designer is considering a variety of alternatives for using a signal source having a source resistance of 100 kΩ to drive a load resistor of 100 Ω. He has available two types of amplifier modules, each with a no-load gain (A_{vo}) of 100 V/V. Module A has an input resistance of 10 kΩ and an output resistance of 1 kΩ, whereas module B has an input resistance of 1 kΩ and an output resistance of 10 kΩ. Calculate the gain available with a single module of either type. Which module is most effective? What gain can be achieved using two of the "most-effective" modules?

D1.20 A designer has available voltage amplifiers having an input resistance of 10 kΩ, an output resistance of 1 kΩ, and an open-circuit voltage gain of 10. The signal source has a 10-kΩ resistance and provides 10 mV rms signal, and it is required to provide a signal of at least 2 V rms to a 1-kΩ load. How many amplifier stages are required? What is the output voltage actually obtained?

D*1.21 Design an amplifier that provides 0.5 W of signal power to a 100-Ω load resistance. The signal source provides a 30-mV rms signal and has a resistance of 0.5 MΩ. Three types of voltage amplifier stages are available:

(1) a high-input-resistance type with R_i = 1 MΩ, A_{vo} = 10, and R_o = 10 kΩ;

(2) a high-gain type with R_i = 10 kΩ, A_{vo} = 100, and R_o = 1 kΩ;

(3) a low-output-resistance type with R_i = 10 kΩ, A_{vo} = 1, and R_o = 20 Ω.

Design a suitable amplifier using a combination of these stages. Your design should utilize the minimum number of stages. Find the load voltage and power output realized.

D1.22 It is required to design a voltage amplifier to be driven from a signal source having a 10-mV peak amplitude and a source resistance of 10 kΩ to supply a peak output of 3 V across a 1-kΩ load.

(a) What is the required voltage gain from the source to the load?

(b) If the peak current available from the source is 0.1 μA, what is the smallest input resistance allowed? For the design with this value of R_i, find the overall current gain and power gain.

(c) If the amplifier power supply limits the peak value of the output open-circuit voltage to 5 V, what is the largest output resistance allowed?

(d) For the design with R_i as in (b) and R_o as in (c), what is the required value of open-circuit voltage gain $\left(\text{i.e., } \left.\frac{v_o}{v_i}\right|_{R_L=\infty}\right)$ of the amplifier?

(e) If, as a possible design option, you are able to increase R_i to the nearest value of the form 1×10^n Ω and to decrease R_o to the nearest value of the form 1×10^m Ω, find (i) the input resistance achievable; (ii) the output resistance achievable; and (iii) the open-circuit voltage gain now required to meet the specifications.

D1.23 A voltage amplifier having an input resistance of 10 kΩ, an output resistance of 200 Ω, and a gain of 1000 V/V is connected between a 100-kΩ source having an open-circuit voltage of 10 mV and a 100-Ω load. For this situation:

(a) What output voltage results?

(b) What is the voltage gain from source to load?

(c) What is the voltage gain from the amplifier input to the load?

(d) If the output voltage across the load is twice that needed, and there are signs of internal amplifier overload, suggest the location and value of a single resistor that would produce the desired output. Choose an arrangement that would cause minimum disruption to an operating circuit. (*Hint:* Use parallel rather than series connections.)

1.24 A current amplifier for which R_i = 1 kΩ, R_o = 10 kΩ, and A_{is} = 100 A/A is to be connected between a 100-mV source having a resistance of 100 kΩ and a load of 1 kΩ. What are the values of current gain i_o/i_i, of voltage gain v_o/v_s, and of power gain, expressed directly and in dB?

1.25 A transconductance amplifier having R_i = 2 kΩ, G_m = 40 mA/V, and R_o = 20 kΩ is fed with a voltage source having a source resistance

of 2 kΩ and is loaded with a 1-kΩ resistance. Find the voltage gain realized.

D1.26** A designer is required to provide, across a 10-kΩ load, the weighted sum, $v_o = 10v_1 + 20v_2$, of input signals v_1 and v_2, each having a source resistance of 10 kΩ. She has a number of transconductance amplifiers for which the input and output resistances are both 10 kΩ, and G_m = 20 mA/V, together with a selection of suitable resistors. Sketch an appropriate amplifier topology with additional resistors selected to provide the desired result. (*Hint:* In your design, arrange to add currents.)

1.27 Figure P1.27 shows a transconductance amplifier whose output is *fed back* to its input. Find the input resistance R_{in} of the resulting one-port network. (*Hint:* Apply a test voltage v_x between the two input terminals and find the current i_x drawn from the source; then $R_{in} \equiv v_x/i_x$.)

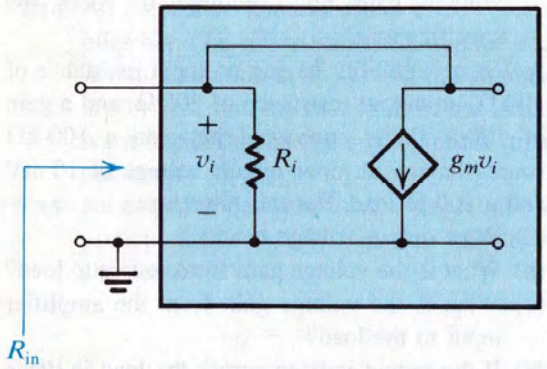


Fig. P1.27

1.28 Refer to Fig. 1.19(c). A BJT, appropriately biased, is used as a so-called common- (or grounded-) emitter amplifier with E grounded, a source voltage v_s with resistance R_s connected to B, and a load resistance R_L connected between C and ground. Derive an expression for the voltage gain v_o/v_s, where v_o is the voltage measured across R_L. Evaluate the voltage gain for the case of R_s = 5 kΩ, r_π = 5 kΩ, g_m = 40 mA/V, and R_L = 5 kΩ.

1.29 Replacing the transistor in the circuit of Fig. P1.29 with the small-signal model of Fig. 1.19(d), find an expression for the voltage gain v_o/v_s of the transistor amplifier, in terms of α and r_e of the transistor, and the values of the external resistors.

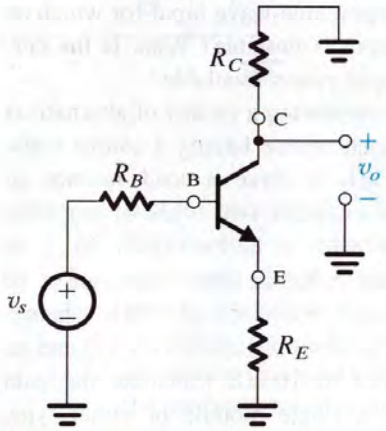


Fig. P1.29

1.30 For the circuit shown in Fig. P1.30 show that

$$\frac{v_c}{v_b} = \frac{-\beta R_L}{r_\pi + (\beta + 1)R_E}$$

and,

$$\frac{v_e}{v_b} = \frac{R_E}{R_E + [r_\pi/(\beta + 1)]}$$

Evaluate these voltage gains for β = 100, r_π = 2.5 kΩ, R_E = 1 kΩ, and R_L = 10 kΩ.

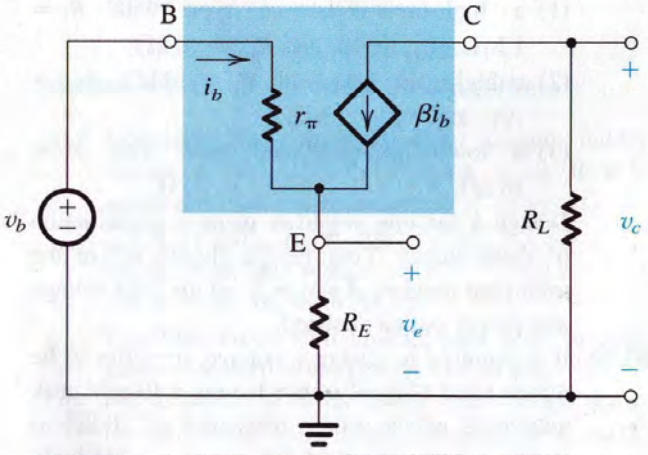


Fig. P1.30

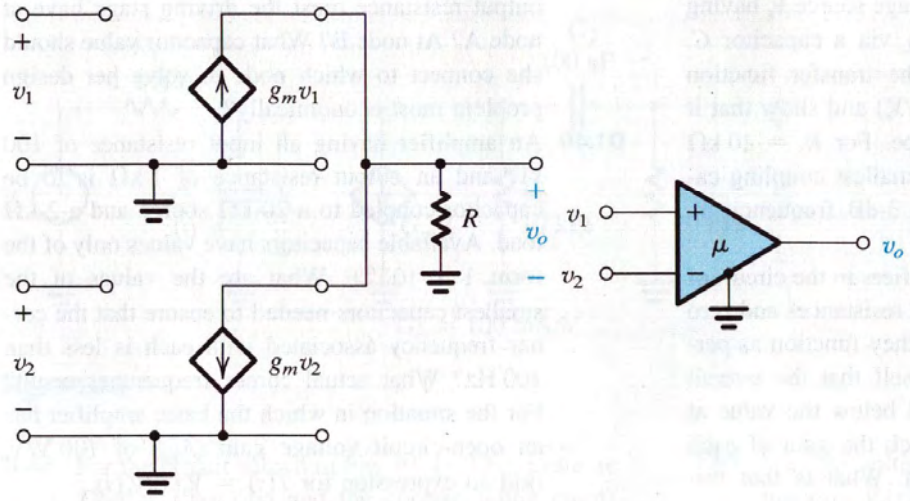


Fig. P1.32

1.31 An amplifier with an input resistance of 10 kΩ, when driven by a current source of 1 μA and a source resistance of 100 kΩ, has a short-circuit output current of 10 mA and an open-circuit output voltage of 10 V. When driving a 4-kΩ load, what are the voltage gain, current gain, and power gain expressed as ratios and in dB?

1.32 Figure P1.32(a) shows two transconductance amplifiers connected in a special configuration. Find v_o in terms of v_1 and v_2. Let $g_m = 100$ mA/V and $R = 5$ kΩ. If $v_1 = v_2 = 1$ V, find the value of v_o. Also find v_o for the case $v_1 = 1.01$ V and $v_2 = 0.99$ V. (*Note:* This circuit is called a **differential amplifier** and is given the symbol shown in Fig. 1.32(b). A particular type of differential amplifier known as an operational amplifier will be studied in Chapter 2.)

Section 1.6: Frequency Response of Amplifiers

1.33 Using the voltage-divider rule derive the transfer functions $T(s) \equiv V_o(s)/V_i(s)$ of the circuits shown in Fig. 1.22, and show that the transfer functions are of the form given at the top of Table 1.2.

1.34 Figure P1.34 shows a signal source connected to the input of an amplifier. Here R_s is the source resistance, and R_i and C_i are the input resistance and input capacitance, respectively, of the amplifier. Derive an expression for $V_i(s)/V_s(s)$ and show that it is of the low-pass STC type. Find the 3-dB frequency for the case $R_s = 10$ kΩ, $R_i = 100$ kΩ, and $C_i = 10$ pF.

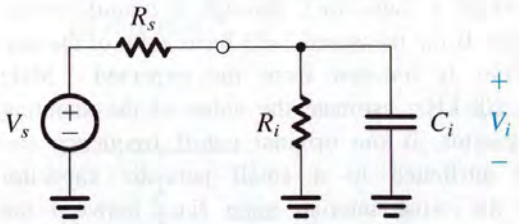


Fig. P1.34

1.35 For the circuit shown in Fig. P1.35, find the transfer function $T(s) = \dfrac{V_o(s)}{V_i(s)}$. (Use the appropriate standard form from Table 1.2.) Is this a high-pass or a low-pass network? What is its transmission at very high frequencies? [Estimate this directly, as well as by letting $s \to \infty$ in your expression for $T(s)$.] What is the corner frequency ω_0? For $R_1 = 10$ kΩ, $R_2 = 20$ kΩ, and $C = 1$ μF, find f_0. What is the value of $|T(j\omega_0)|$?

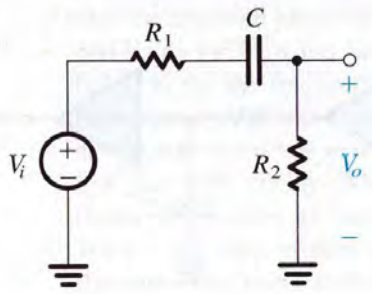


Fig. P1.35

D1.36 It is required to couple a voltage source V_s having a resistance R_s to a load R_L via a capacitor C. Derive an expression for the transfer function from source to load (i.e., V_L/V_s) and show that it is of the high-pass STC type. For $R_s = 10\ \text{k}\Omega$ and $R_L = 40\ \text{k}\Omega$, find the smallest coupling capacitor that will result in a 3-dB frequency no greater than 10 Hz.

***1.37** The unity-gain voltage amplifiers in the circuit of Fig. P1.37 have infinite input resistances and zero output resistances, and thus they function as perfect buffers. Convince yourself that the overall gain V_o/V_i will drop by 3 dB below the value at dc at the frequency for which the gain of each RC circuit is 0.75 dB down. What is that frequency in terms of CR?

1.38 An internal node of a high-frequency amplifier, whose Thévenin-equivalent node resistance is 100 kΩ, is accidentally shunted to ground by a capacitor (i.e., the node is connected to ground through a capacitor), through a manufacturing error. If the measured 3-dB bandwidth of the amplifier is reduced from the expected 5 MHz to 100 kHz, estimate the value of the shunting capacitor. If the original cutoff frequency can be attributed to a small parasitic capacitor at the same internal node (i.e., between the node and ground), what would you estimate it to be?

D*1.39 A designer wishing to lower the overall high-frequency response of a three-stage amplifier to 10 kHz considers shunting one of the two nodes between the output of one stage and the input of the next stage to ground with a small capacitor. While measuring the overall frequency response of the amplifier, she shunts a capacitor of 1 nF, first to node A, then to node B, lowering the 3-dB frequency from 1 MHz to 100 kHz and 20 kHz, respectively. If she knows that each amplifier stage has an input resistance of 100 kΩ, what output resistance must the driving stage have at node A? At node B? What capacitor value should she connect to which node to solve her design problem most economically?

D1.40 An amplifier having an input resistance of 100 kΩ and an output resistance of 1 kΩ is to be capacitor-coupled to a 20-kΩ source and a 2-kΩ load. Available capacitors have values only of the form 1×10^{-n} F. What are the values of the smallest capacitors needed to ensure that the corner frequency associated with each is less than 100 Hz? What actual corner frequencies result? For the situation in which the basic amplifier has an open-circuit voltage gain (A_{vo}) of 100 V/V, find an expression for $T(s) = V_o(s)/V_s(s)$.

***1.41** When measured experimentally, an amplifier is found to have a midband gain of 20 V/V at 5 kHz with a phase shift of 180° at 5 kHz, 135° at 50 Hz, and 225° at 500 kHz. What are its 3-dB frequencies? Find an expression for its transfer function. What is the range of frequencies over which the gain exceeds 23 dB? 0 dB? If the capacitors embedded in each of the two associated single-time-constant networks are doubled in value, what do the two 3-dB frequencies become?

***1.42** A voltage amplifier has the transfer function

$$A_v = \frac{100}{\left(1 + j\frac{f}{10^4}\right)\left(1 + \frac{10^2}{jf}\right)}$$

Using the Bode plots for low-pass and high-pass STC networks (Figs. 1.23 and 1.24) sketch a Bode plot for $|A_v|$. Give approximate values for the gain magnitude at $f = 10$, 10^2, 10^3, 10^4, 10^5, 10^6, and 10^7 Hz. Find the bandwidth of the amplifier (defined as the frequency range over which the gain remains within 3 dB of the maximum value).

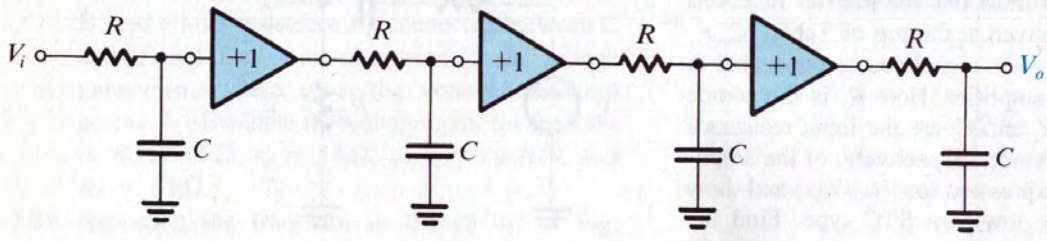


Fig. P1.37

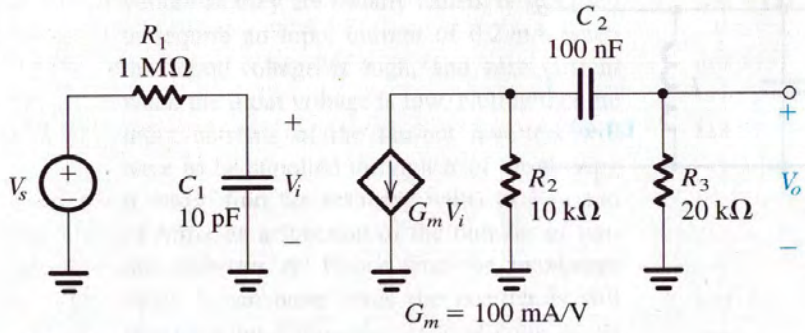


Fig. P1.43

*1.43 For the circuit shown in Fig. P1.43, first, evaluate $T_i(s) = V_i(s)/V_s(s)$ and the corresponding cutoff (corner) frequency. Second, evaluate $T_o(s) = V_o(s)/V_i(s)$ and the corresponding cutoff frequency. Put each of the transfer functions in the standard form (see Table 1.2), and combine them to form the overall transfer function, $T(s) = T_i(s) \times T_o(s)$. Provide a Bode magnitude plot for $|T(j\omega)|$. What is the bandwidth between 3-dB cutoff points?

D**1.44 A transconductance amplifier having the equivalent circuit shown in Table 1.1 is fed with a voltage source V_s having a source resistance R_s, and its output is connected to a load consisting of a resistance R_L in parallel with a capacitance C_L. For given values of R_s, R_L, and C_L it is required to specify the values of the amplified parameters R_i, G_m, and R_o to meet the following design constraints:

(1) At most $x\%$ of the input signal is lost in coupling the signal source to the amplifier (i.e., $V_i \geq [1 - (x/100)]V_s$).
(2) The 3-dB frequency of the amplifier is equal to or greater than a specified value f_{3dB}.
(3) The dc gain V_o/V_s is equal to or greater than a specified value A_0.

Show that these constraints can be met by selecting

$$R_i \geq \left(\frac{100}{x} - 1\right)R_s$$

$$R_o \leq \frac{1}{2\pi f_{3dB} C_L - (1/R_L)}$$

$$G_m \geq \frac{A_0/[1 - (x/100)]}{(R_L // R_o)}$$

Find R_i, R_o, and G_m for $R_s = 10$ kΩ, $x = 20\%$, $A_0 = 80$, $R_L = 10$ kΩ, $C_L = 10$ pF, and $f_{3dB} = 3$ MHz.

1.45 Use the voltage-divider rule to find the transfer function $V_o(s)/V_i(s)$ of the circuit in Fig. P1.45. Show that the transfer function can be made independent of frequency if the condition $C_1R_1 = C_2R_2$ applies. Under this condition the circuit is called a **compensated attenuator.** Find the transmission of the compensated attenuator in terms of R_1 and R_2.

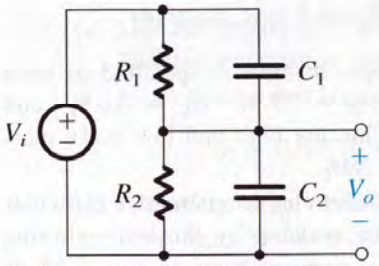


Fig. P1.45

*1.46 An amplifier with a frequency response of the type shown in Fig. 1.21 is specified to have a phase shift of magnitude no greater than 11.4° over the amplifier bandwidth, which extends from 100 Hz to 1 kHz. It has been found that the gain falloff at the low-frequency end is determined by the response of a high-pass STC circuit, and that at the high-frequency end it is determined by a low-pass STC circuit. What do you expect the corner frequencies of these two circuits to be? What is the drop in gain in decibels (relative to the maximum gain) at the two frequencies that define the amplifier bandwidth? What are the frequencies at which the drop in gain is 3 dB?

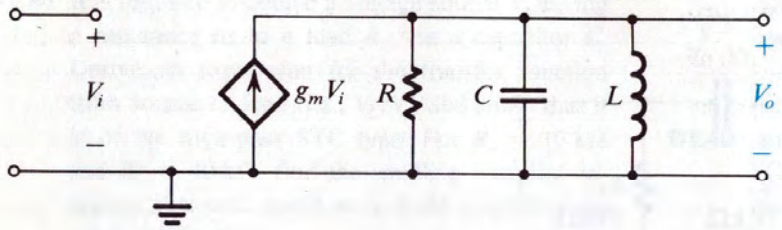


Fig. P1.47

***1.47** Figure P1.47 shows a tuned, or bandpass, amplifier. Derive its transfer function $T(s) \equiv V_o(s)/V_i(s)$ and find $T(j\omega)$ and $|T(j\omega)|$. What is the value of gain at $\omega = 0$ and at $\omega = \infty$? At what frequency is the gain maximum? What is the value of the maximum gain? Find the two frequencies at which the gain drops by 3 dB below the maximum value. The 3-dB bandwidth of the amplifier is the difference between these two frequencies. Find its value. (Hint: the maximum output occurs at the frequency for which the parallel equivalent impedance of L and C is infinite.)

Section 1.7: The Digital Logic Inverter

1.48 A particular logic inverter is specified to have $V_{IL} = 1.5$ V, $V_{IH} = 2.7$ V, $V_{OL} = 0.6$ V, and $V_{OH} = 3.7$ V. Find the high and low noise margins, NM_H and NM_L.

1.49 The voltage transfer characteristic of a particular logic inverter is modeled by three straight-line segments in the manner shown in Fig. 1.29. If $V_{IL} = 1.5$ V, $V_{IH} = 2.5$ V, $V_{OL} = 0.5$ V, and $V_{OH} = 4$ V, find (a) the noise margins, (b) the value of v_I at which $v_O = v_I$ (known as the inverter threshold), and (c) the voltage gain in the transition region.

1.50 For a particular inverter design using a power supply V_{DD}, $V_{OL} = 0.1\,V_{DD}$, $V_{OH} = 0.8\,V_{DD}$, $V_{IL} = 0.4\,V_{DD}$, and $V_{IH} = 0.6\,V_{DD}$. What are the noise margins? What is the width of the transition region? For a minimum noise margin of 1 V, what value of V_{DD} is required?

1.51 A popular logic circuit family studied in Chapter 14 is Transistor-Transistor Logic (TTL). TTL logic gates and other building blocks are available commercially in small-scale integrated (SSI) and medium-scale-integrated (MSI) packages. Such packages can be assembled on printed-circuit boards to implement a digital system. The device data sheets provide the following specifications of the basic TTL inverter (of the SN7400 type):

Logic-1 input level required to ensure a logic-0 level at the output: MIN (minimum) 2 V

Logic-0 input level required to ensure a logic-1 level at the output: MAX (maximum) 0.8 V

Logic-1 output voltage: MIN 2.4 V, TYP (typical) 3.3 V

Logic-0 output voltage: TYP 0.22 V, MAX 0.4 V

Logic-0-level supply current: TYP 3 mA, MAX 5 mA

Logic-1-level supply current: TYP 1 mA, MAX 2 mA

Propagation delay time to logic-0 level (t_{PHL}): TYP 7 ns, MAX 15 ns

Propagation delay time to logic-1 level (t_{PLH}): TYP 11 ns, MAX 22 ns

(a) Find the worst-case values of the noise margins.

(b) Assuming that the inverter is in the 1-state 50% of the time and in the 0-state 50% of the time, find the average static power dissipation in a typical circuit. The power supply is 5 V.

(c) Assuming that the inverter drives a capacitance $C_L = 45$ pF and is switched at a 1-MHz rate, use the formula in Eq. (1.32) to estimate the dynamic power dissipation.

(d) Find the propagation delay t_P.

1.52 Consider an inverter implemented as in Fig. 1.31(a). Let $V_{DD} = 5$ V, $R = 2$ kΩ, $V_{\text{offset}} = 0.1$ V, $R_{\text{on}} = 200\ \Omega$, $V_{IL} = 1$ V, and $V_{IH} = 2$ V.

(a) Find V_{OL}, V_{OH}, NM_H, and NM_L.

(b) The inverter is driving N identical inverters. Each of these load inverters, or **fan-out** in-

verters as they are usually called, is specified to require an input current of 0.2 mA when the input voltage is high, and zero current when the input voltage is low. Noting that the input currents of the fan-out inverters will have to be supplied through R of the driving inverter, find the resulting value of V_{OH} and of NM_H, as a function of the number of fan-out inverters N. Hence find the maximum value N can have while the inverter is still providing an NM_H value at least equal to its NM_L.

(c) Find the static power dissipation in the inverter in the two cases: (i) the output is low, and (ii) the output is high and driving the maximum fan-out found in (b).

1.53 A logic inverter is implemented using the arrangement of Fig. 1.32 with switches having $R_{on} = 1\ \text{k}\Omega$. $V_{DD} = 5$ V and $V_{IL} = V_{IH} = V_{DD}/2$.

(a) Find V_{OL}, V_{OH}, NM_L, and NM_H.

(b) If v_I rises instantaneously from 0 to +5 V and assuming the switches operate instantaneously, that is, at $t = 0$, PU opens, and PD closes, find an expression for $v_O(t)$ assuming that a capacitance C is connected between the output node and ground. Hence find the high-to-low propagation delay (t_{PHL}) for $C = 1$ pF. Also find t_{THL} (see Fig. 1.35).

(c) Repeat (b) for v_I falling instantaneously from +5 to 0 V. Again assume that PD opens and PU closes instantaneously. Find an expression for $v_O(t)$, and hence find t_{PLH} and t_{TLH}.

1.54 For the current-mode inverter shown in Fig. 1.33, let $V_{CC} = 5$ V, $I_{EE} = 1$ mA, and $R_{C1} = R_{C2} = 2\ \text{k}\Omega$. Find V_{OL} and V_{OH}.

1.55 Consider a logic inverter of the type shown in Fig. 1.32. Let $V_{DD} = 5$ V, and let a 10-pF capacitance be connected between the output node and ground. If the inverter is switched at the rate of 100 MHz, use the expression in Eq. (1.32) to estimate the dynamic power dissipation. What is the average current drawn from the dc power supply?

D1.56** We wish to investigate the design of the inverter shown in Fig. 1.31(a). In particular, we wish to determine the value of R. Selection of a suitable value of R is determined by two considerations: propagation delay and power dissipation.

(a) Show that if v_I changes instantaneously from high to low, and assuming that the switch opens instantaneously, the output voltage obtained across a load capacitance C will be

$$v_O(t) = V_{OH} - (V_{OH} - V_{OL})e^{-t/\tau_1}$$

where $\tau_1 = CR$. Hence show that the time required for $v_O(t)$ to reach the 50% point, $\frac{1}{2}(V_{OH} + V_{OL})$, is

$$t_{PLH} = 0.69CR$$

(b) Following a steady state, if v_I goes high and assuming that the switch closes immediately and has the equivalent circuit in Fig. 1.31, show that the output falls exponentially according to

$$v_O(t) = V_{OL} + (V_{OH} - V_{OL})e^{-t/\tau_2}$$

where $\tau_2 = C(R\|R_{on}) \cong CR_{on}$ for $R_{on} \ll R$. Hence show that the time for $v_O(t)$ to reach the 50% point is

$$t_{PHL} = 0.69CR_{on}$$

(c) Use the results of (b) and (c) to obtain the inverter propagation delay, defined as the average of t_{PLH} and t_{PHL} as

$$\tau_P \cong 0.35CR, \text{ for } R_{on} \ll R$$

(d) Assuming V_{offset} of the switch much smaller than V_{DD}, show that for an inverter that spends half the time in the 0 state and half the time in the 1 state, the average static power dissipation is

$$P = \frac{1}{2}\frac{V_{DD}^2}{R}$$

(e) Now that the tradeoffs in selecting R should be obvious, show that for $V_{DD} = 5$ V and $C = 10$ pF to obtain a propagation delay no greater than 10 ns and a power dissipation no greater than 10 mW, R should be in a specific range. Find that range and select an appropriate value for R. Then determine the resulting values of t_P and P.

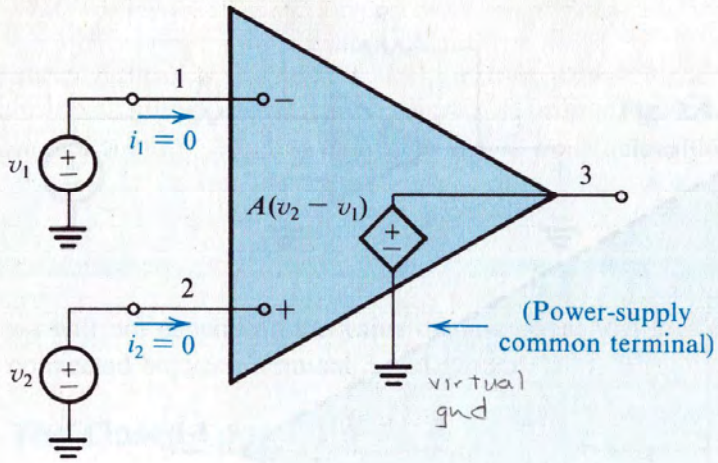


Fig. 2.3 Equivalent circuit of the ideal op amp.

attach to A: the **open-loop gain.** The reason for this name will become obvious later on when we "close the loop" around the op amp and define another gain, the closed-loop gain.

An important characteristic of op amps is that they are direct-coupled devices or dc amplifiers, where dc stands for direct-coupled (it could equally well stand for direct current, since a direct-coupled amplifier is one that amplifies signals whose frequency is as low as zero). The fact that op amps are direct-coupled devices will allow us to use them in many important applications. Unfortunately, though, the direct-coupling property can cause some serious practical problems, as will be discussed in a later section.

How about bandwidth? The ideal op amp has a gain A that remains constant down to zero frequency and up to infinite frequency. That is, ideal op amps will amplify signals of any frequency with equal gain.

We have discussed all of the properties of the ideal op amp except for one, which in fact is the most important. This has to do with the value of A. The ideal op amp should have a gain A whose value is very large and ideally infinite. One may justifiably ask: If the gain A is infinite, how are we going to use the op amp? The answer is very simple: In almost all applications the op amp will *not* be used alone in a so-called open-loop configuration. Rather, we will use other components to apply feedback to close the loop around the op amp, as will be illustrated in detail in Section 2.3.

Exercises

2.2 Consider an op amp that is ideal except that its open-loop gain $A = 10^3$. The op amp is used in a feedback circuit and the voltages appearing at two of its three signal terminals are measured. In each of the following cases, use the measured values to find the expected value of the voltage at the third terminal. (a) $v_2 = 0$ V and $v_3 = 2$ V; (b) $v_2 = +5$ V and $v_3 = -10$ V; (c) $v_1 = 1.002$ V and $v_2 = 0.998$ V; (d) $v_1 = -3.6$ V and $v_3 = -3.6$ V.

Ans. (a) $v_1 = -0.002$ V; (b) $v_1 = +5.01$ V; (c) $v_3 = -4$ V; (d) $v_2 = -3.6036$ V

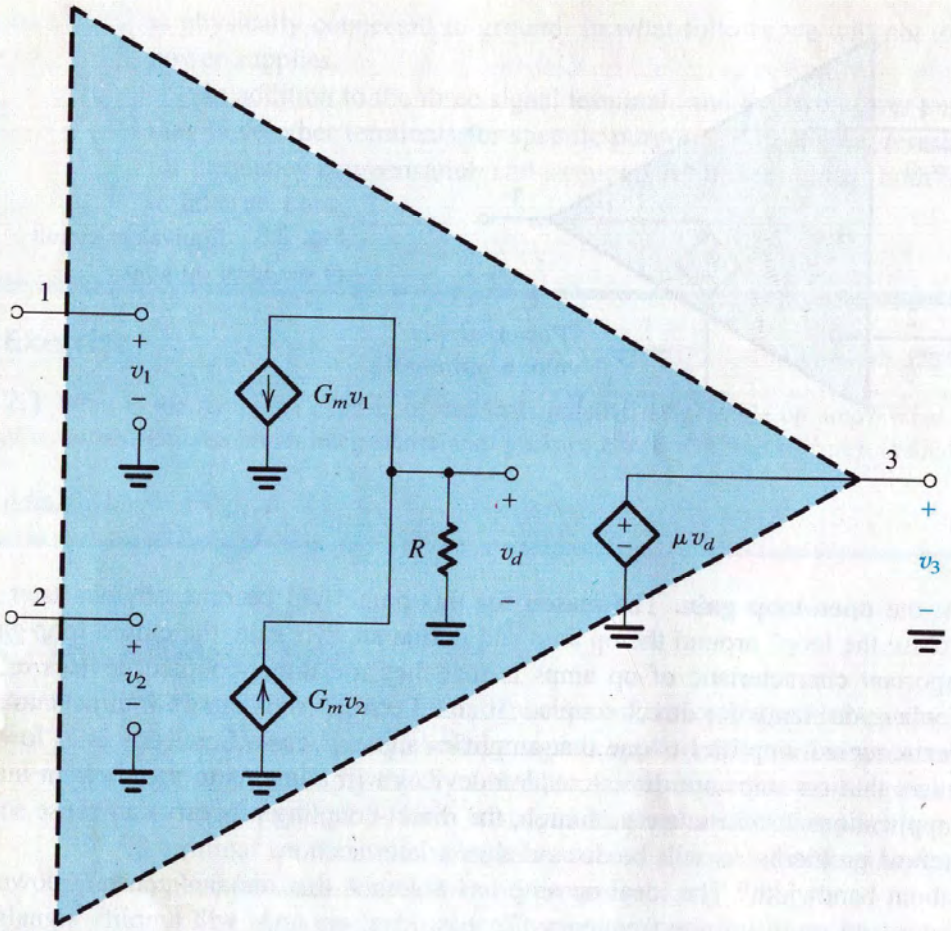


Fig. E2.3

2.3 The internal circuit of a particular op amp can be modeled by the circuit shown in Fig. E2.3. Express v_3 as a function of v_1 and v_2. For the case $G_m = 10\,\text{mA/V}$, $R = 10\,\text{k}\Omega$, and $\mu = 100$, find the value of the open-loop gain A.

Ans. $v_3 = \mu G_m R(v_2 - v_1)$; $A = 10{,}000\ \text{V/V}$

2.3 ANALYSIS OF CIRCUITS CONTAINING IDEAL OP AMPS—THE INVERTING CONFIGURATION

Consider the circuit shown in Fig. 2.4, which consists of one op amp and two resistors R_1 and R_2. Resistor R_2 is connected from the output terminal of the op amp, terminal 3, *back* to the *inverting* or *negative* input terminal, terminal 1. We speak of R_2 as applying **negative feedback;** if R_2 were connected between terminals 3 and 2 we would have called this **positive feedback.** Note also that R_2 *closes the loop* around the op amp. In addition to adding R_2, we have grounded terminal 2 and connected a resistor R_1 between terminal 1 and an input signal source with a voltage v_I. The output of the overall circuit is taken at terminal 3 (that is, between terminal 3 and ground). Terminal 3 is, of course, a convenient point to take the output, since the impedance level there is ideally zero. Thus the voltage

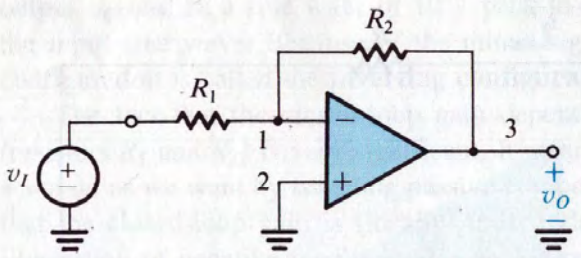


Fig. 2.4 The inverting closed-loop configuration.

v_O will not depend on the value of the current that might be supplied to a load impedance connected between terminal 3 and ground.

The Closed-Loop Gain

We now wish to analyze the circuit in Fig. 2.4 to determine the **closed-loop gain** G, defined as

$$G \equiv \frac{v_O}{v_I}$$

We will do so assuming the op amp to be ideal. Figure 2.5(a) shows the equivalent circuit, and the analysis proceeds as follows: The gain A is very large (ideally infinite). If we assume that the circuit is "working" and producing a finite output voltage at terminal 3, then the voltage between the op amp input terminals should be negligibly small. Specifically, if we call the output voltage v_O, then, by definition,

$$v_2 - v_1 = \frac{v_O}{A} \simeq 0$$

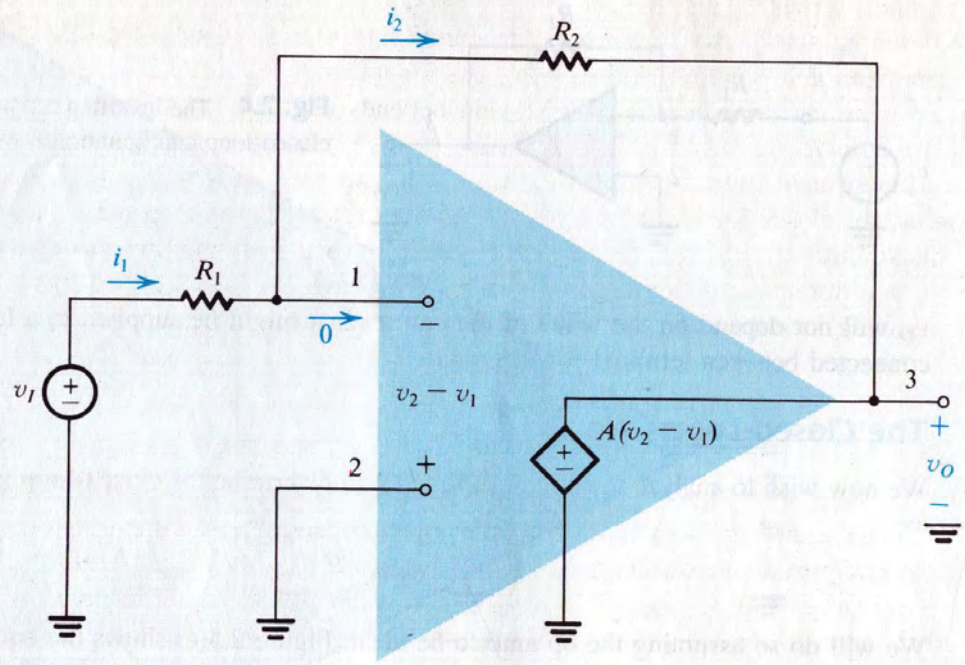
It follows that the voltage at the inverting input terminal (v_1) is given by $v_1 \simeq v_2$. That is, because the gain A approaches infinity, the voltage v_1 approaches v_2. We speak of this as the two input terminals "tracking each other in potential." We also speak of a "virtual short circuit" that exists between the two input terminals. Here, the word *virtual* should be emphasized, and one should *not* make the mistake of physically shorting terminals 1 and 2 together while analyzing a circuit. A **virtual short circuit** means that whatever voltage is at 2 will automatically appear at 1 because of the infinite gain A. But terminal 2 happens to be connected to ground; thus $v_2 = 0$ and $v_1 \simeq 0$. We speak of terminal 1 as being a **virtual ground**—that is, having zero voltage but not physically connected to ground.

Now that we have determined v_1 we are in a position to apply Ohm's law and find the current i_1 through R_1 (see Fig. 2.5) as follows:

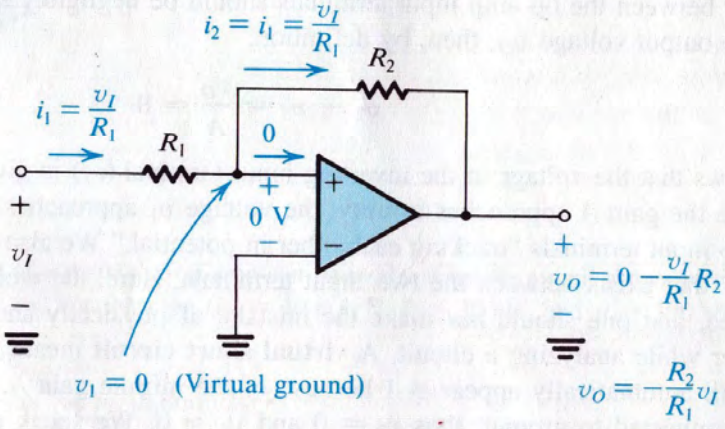
$$i_1 = \frac{v_I - v_1}{R_1} \simeq \frac{v_I}{R_1}$$

Where will this current go? It cannot go into the op amp, since the ideal op amp has an infinite input impedance and hence draws zero current. It follows that i_1 will have to flow through R_2 to the low-impedance terminal 3. We can then apply Ohm's law to R_2 and determine v_O; that is,

$$v_O = v_1 - i_1 R_2$$
$$= 0 - \frac{v_I}{R_1} R_2$$



(a)



(b)

Fig. 2.5 Analysis of the inverting configuration.

Thus

$$\frac{v_O}{v_I} = -\frac{R_2}{R_1}$$

which is the required closed-loop gain. Figure 2.5(b) illustrates some of these analysis steps.

We thus see that the closed-loop gain is simply the ratio of the two resistances R_2 and R_1. The minus sign means that the closed-loop amplifier provides signal inversion. Thus if $R_2/R_1 = 10$ and we apply at the input (v_I) a sine-wave signal of 1 V peak-to-peak, then the

output v_O will be a sine wave of 10 V peak-to-peak and phase-shifted 180° with respect to the input sine wave. Because of the minus sign associated with the closed-loop gain this configuration is called the **inverting configuration.**

The fact that the closed-loop gain depends entirely on external passive components (resistors R_1 and R_2) is very significant. It means that we can make the closed-loop gain as accurate as we want by selecting passive components of appropriate accuracy. It also means that the closed-loop gain is (ideally) independent of the op-amp gain. This is a dramatic illustration of negative feedback: We started out with an amplifier having very large gain A, and through applying negative feedback we have obtained a closed-loop gain R_2/R_1 that is much smaller than A but is stable and predictable. That is, we are trading gain for accuracy.

Effect of Finite Open-Loop Gain

The points just made are more clearly illustrated by deriving an expression for the closed-loop gain under the assumption that the op amp open-loop gain A is finite. Figure 2.6 shows the analysis. If we denote the output voltage v_O, then the voltage between the two input terminals of the op amp will be v_O/A. Since the positive input terminal is grounded, the voltage at the negative input terminal must be $-v_O/A$. The current i_1 through R_1 can now be found from

$$i_1 = \frac{v_I - (-v_O/A)}{R_1} = \frac{v_I + v_O/A}{R_1}$$

The infinite input impedance of the op amp forces the current i_1 to flow entirely through R_2. The output voltage v_O can thus be determined from

$$\begin{aligned} v_O &= -\frac{v_O}{A} - i_1 R_2 \\ &= -\frac{v_O}{A} - \left(\frac{v_I + v_O/A}{R_1}\right) R_2 \end{aligned}$$

Collecting terms, the closed-loop gain G is found as

$$G \equiv \frac{v_O}{v_I} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A} \tag{2.1}$$

We note that as A approaches ∞, G approaches the ideal value of $-R_2/R_1$. Also from Fig. 2.6 we see that as A approaches ∞, the voltage at the inverting input terminal approaches

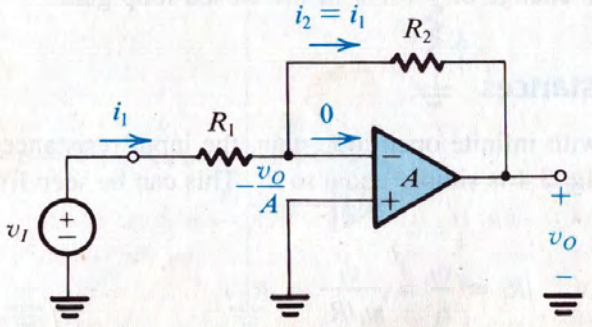


Fig. 2.6 Analysis of the inverting configuration taking into account the finite open-loop gain of the op amp.

zero. This is the virtual-ground assumption we used in our earlier analysis when the op amp was assumed to be ideal. Finally, note that Eq. (2.1) in fact indicates that to minimize the dependence of the closed-loop gain G on the value of the open-loop gain A, we should make

$$1 + \frac{R_2}{R_1} \ll A$$

EXAMPLE 2.1

Consider the inverting configuration with $R_1 = 1\ \text{k}\Omega$ and $R_2 = 100\ \text{k}\Omega$.

(a) Find the closed-loop gain for the cases $A = 10^3$, 10^4, and 10^5. In each case determine the percentage error in the magnitude of G relative to the ideal value of R_2/R_1 (obtained with $A = \infty$). Also determine the voltage v_1 that appears at the inverting input terminal when $v_I = 0.1$ V.

(b) If the open-loop gain A changes from 100,000 to 50,000, what is the corresponding percentage change in the magnitude of the closed-loop gain G?

SOLUTION

(a) Substituting the given values in Eq. (2.1), we obtain the values given in the following table where the percentage error ε is defined as

$$\varepsilon \equiv \frac{|G| - (R_2/R_1)}{(R_2/R_1)} \times 100$$

The values of v_1 are obtained from $v_1 = -v_O/A = Gv_I/A$ with $v_I = 0.1$ V.

A	$\lvert G\rvert$	ε	v_1
10^3	90.83	−9.17%	−9.08 mV
10^4	99.00	−1.00%	−0.99 mV
10^5	99.90	−0.10%	−0.10 mV

(b) Using Eq. (2.1), we find that for $A = 50{,}000$, $|G| = 99.80$. Thus halving the open-loop gain results in a change of −0.1% in the closed-loop gain!

Input and Output Resistances

Assuming an ideal op amp with infinite open-loop gain, the input resistance of the closed-loop inverting amplifier of Fig. 2.4 is simply equal to R_1. This can be seen from Fig. 2.5(b), where

$$R_i \equiv \frac{v_I}{i_1} = \frac{v_I}{v_I/R_1} = R_1$$

Thus to make R_i high, we should select a high value for R_1. However, if the required gain R_2/R_1 is also high, then R_2 could become impractically large (e.g., greater than a few mega ohms). We may conclude that the inverting configuration suffers from a low input resistance. A solution to this problem is discussed in Example 2.2 below. It should also be mentioned that the finite open-loop gain A has a negligible effect on the value of the input resistance of the inverting amplifier configuration (see Problem 2.17).

Since the output of the inverting configuration is taken at the terminals of the ideal voltage source $A(v_2 - v_1)$ (see Fig. 2.5a), it follows that the output resistance of the closed-loop amplifier is zero.

Putting all of the above together, we obtain the circuit shown in Fig. 2.7 as the equivalent circuit model of the inverting-amplifier configuration of Fig. 2.4 (under the assumption that the op amp is ideal).

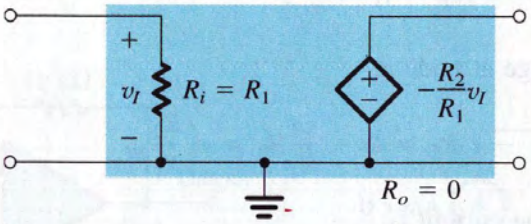


Fig. 2.7 Equivalent circuit model of the inverting-amplifier configuration of Fig. 2.4 (assuming the op amp is ideal).

EXAMPLE 2.2

Assuming the op amp to be ideal, derive an expression for the closed-loop gain v_O/v_I of the circuit shown in Fig. 2.8. Use this circuit to design an inverting amplifier with a gain of 100 and an input resistance of 1 MΩ. Assume that for practical reasons it is required not to use resistors greater than 1 MΩ. Compare your design with that based on the inverting configuration of Fig. 2.4.

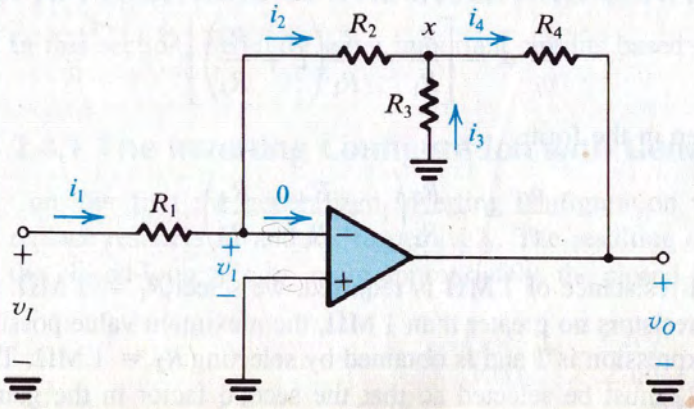


Fig. 2.8 Circuit for Example 2.2.

SOLUTION

The analysis begins at the inverting input terminal of the op amp, where the voltage is

$$v_1 = \frac{-v_O}{A} = \frac{-v_O}{\infty} = 0$$

Here we have assumed that the circuit is "working" and producing a finite output voltage v_O. Knowing v_1, we can determine the current i_1, as follows:

$$i_1 = \frac{v_I - v_1}{R_1} = \frac{v_I - 0}{R_1} = \frac{v_I}{R_1}$$

Since zero current flows into the inverting input terminal, all of i_1 will flow through R_2, and thus

$$i_2 = i_1 = \frac{v_I}{R_1}$$

Now we can determine the voltage at node x:

$$v_x = v_1 - i_2 R_2 = 0 - \frac{v_I}{R_1} R_2 = -\frac{R_2}{R_1} v_I$$

This in turn enables us to find the current i_3,

$$i_3 = \frac{0 - v_x}{R_3} = \frac{R_2}{R_1 R_3} v_I$$

Next, a node equation at x yields i_4,

$$i_4 = i_2 + i_3 = \frac{v_I}{R_1} + \frac{R_2}{R_1 R_3} v_I$$

Finally, we can determine v_O from

$$\begin{aligned} v_O &= v_x - i_4 R_4 \\ &= -\frac{R_2}{R_1} v_I - \left(\frac{v_I}{R_1} + \frac{R_2}{R_1 R_3} v_I \right) R_4 \end{aligned}$$

Thus, the voltage gain is given by

$$\frac{v_O}{v_I} = -\left[\frac{R_2}{R_1} + \frac{R_4}{R_1} \left(1 + \frac{R_2}{R_3} \right) \right]$$

which can be written in the form

$$\frac{v_O}{v_I} = -\frac{R_2}{R_1} \left(1 + \frac{R_4}{R_2} + \frac{R_4}{R_3} \right)$$

Now since an input resistance of 1 MΩ is required, we select $R_1 = 1$ MΩ. Then, with the limitation of using resistors no greater than 1 MΩ, the maximum value possible for the first factor in the gain expression is 1 and is obtained by selecting $R_2 = 1$ MΩ. To obtain a gain of -100, R_3 and R_4 must be selected so that the second factor in the gain expression is

100. If we select the maximum allowed (in this example) value of 1 MΩ for R_4 then the required value of R_3 can be calculated to be 10.2 kΩ. Thus this circuit utilizes three 1-MΩ resistors and a 10.2 kΩ resistor. In comparison, if the inverting configuration were used with $R_1 = 1$ MΩ we would have required a feedback resistor of 100 MΩ, an impractically large value!

Exercises

D2.4 Use the circuit of Fig. 2.4 to design an inverting amplifier having a gain of −10 and an input resistance of 100 kΩ. Give the values of R_1 and R_2.

Ans. $R_1 = 100$ kΩ; $R_2 = 1$ MΩ

2.5 The circuit shown in Fig. E2.5(a) can be used to implement a transresistance amplifier (see Table 1.1 in Section 1.5). Find the value of the input resistance R_i, the transresistance R_m, and the output resistance R_o of

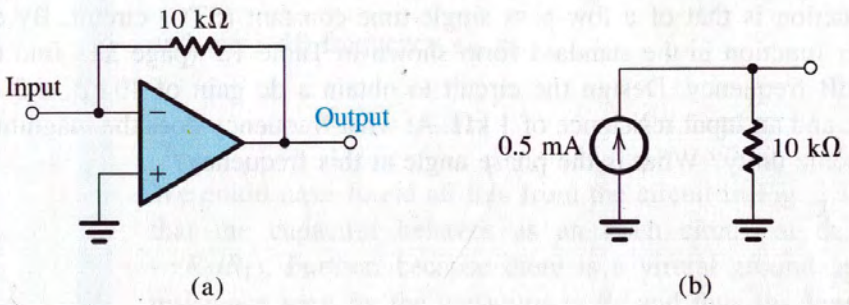


Fig. E2.5

the transresistance amplifier. If the signal source shown in Fig. E2.5(b) is connected to the input of the transresistance amplifier, find its output voltage.

Ans. $R_i = 0$; $R_m = -10$ kΩ; $R_o = 0$; $v_o = -5$ V

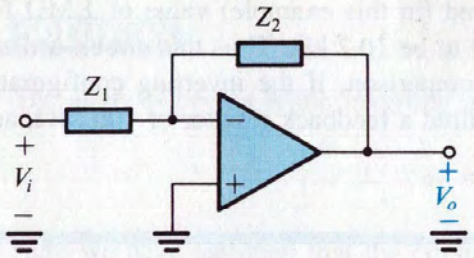
2.4 OTHER APPLICATIONS OF THE INVERTING CONFIGURATION

In this section, we study some important circuits based on the inverting configuration.

2.4.1 The Inverting Configuration with General Impedances Z_1 and Z_2

Consider first the generalized inverting configuration where impedances $Z_1(s)$ and $Z_2(s)$ replace resistors R_1 and R_2, respectively. The resulting circuit is shown in Fig. 2.9 and has the closed-loop gain or, more appropriately, the closed-loop transfer function

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)} \tag{2.2}$$



$$\frac{V_o}{V_i} = -\frac{Z_2}{Z_1}$$

Fig. 2.9 The inverting configuration with general impedances in the feedback and at the input.

As explained in Section 1.6, replacing s by $j\omega$ provides the transfer function for physical frequencies ω, that is, the transmission magnitude and phase for a sinusoidal input signal of frequency ω.

EXAMPLE 2.3

For the circuit in Fig. 2.10, derive an expression for the transfer function $V_o(s)/V_i(s)$. Show that the transfer function is that of a low-pass single-time-constant (STC) circuit. By expressing the transfer function in the standard form shown in Table 1.2 (page 32), find the dc gain and the 3-dB frequency. Design the circuit to obtain a dc gain of 40 dB, a 3-dB frequency of 1 kHz, and an input resistance of 1 kΩ. At what frequency does the magnitude of transmission become unity? What is the phase angle at this frequency?

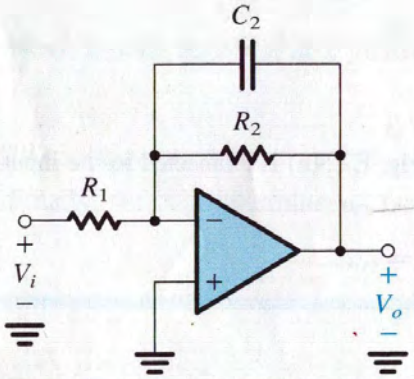


Fig. 2.10 Circuit for Example 2.3.

SOLUTION

To obtain the transfer function of the circuit in Fig. 2.10, we substitute in Eq. (2.2), $Z_1 = R_1$ and $Z_2 = R_2 \| (1/sC_2)$. Since Z_2 is the parallel connection of two components, it is more convenient to work in terms of Y_2, that is, we use the following alternative form of the transfer function:

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{Z_1(s)Y_2(s)}$$

and substitute $Z_1 = R_1$ and $Y_2(s) = \frac{1}{R_2} + sC_2$ to obtain

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{\frac{R_1}{R_2} + sC_2R_1}$$

This transfer function is of first order, has a finite dc gain $\left(\text{at } s = 0, \frac{V_o}{V_i} = -\frac{R_2}{R_1}\right)$, and has zero gain at infinite frequency. Thus, it is the transfer function of a low-pass STC network and can be expressed in the standard form of Table 1.2 as follows:

$$\frac{V_o(s)}{V_i(s)} = \frac{-(R_2/R_1)}{1 + sC_2R_2}$$

from which we find the dc gain K to be

$$K = -\frac{R_2}{R_1}$$

and the 3-dB frequency ω_0 as

$$\omega_0 = \frac{1}{C_2R_2}$$

We could have found all this from the circuit in Fig. 2.10 by inspection. Specifically, note that the capacitor behaves as an open circuit at dc, thus at dc the gain is simply $(-R_2/R_1)$. Further, because there is a virtual ground at the inverting input terminal, the resistance seen by the capacitor is R_2 and thus the time constant of the STC network is C_2R_2.

Now to obtain a dc gain of 40 dB, that is, 100 V/V, we select $R_2/R_1 = 100$. For an input resistance of 1 kΩ, we select $R_1 = 1$ kΩ, and thus $R_2 = 100$ kΩ. Finally, for a 3-dB frequency $f_0 = 1$ kHz, we select C_2 from

$$2\pi \times 1 \times 10^3 = \frac{1}{C_2 \times 100 \times 10^3}$$

which yields $C_2 = 1.59$ nF.

The circuit has gain and phase Bode plots of the standard form in Fig. 1.23. As the gain falls off at the rate of 20 dB/decade, it will reach 0 dB in two decades, that is, at $f = 100f_0 = 100$ kHz. As Fig. 1.23(b) indicates, at such a frequency which is much greater than f_0, the phase is approximately −90°. To this, however, we must add the 180° arising from the inverting nature of the amplifier (i.e., the negative sign in the transfer function expression). Thus at 100 kHz, the total phase shift will be −270° or, equivalently, +90°.

2.4.2 The Inverting Integrator

By placing a capacitor in the feedback path (i.e., in place of Z_2 in Fig. 2.9) and a resistor at the input (in place of Z_1), we obtain the circuit of Fig. 2.11(a). We shall now show that

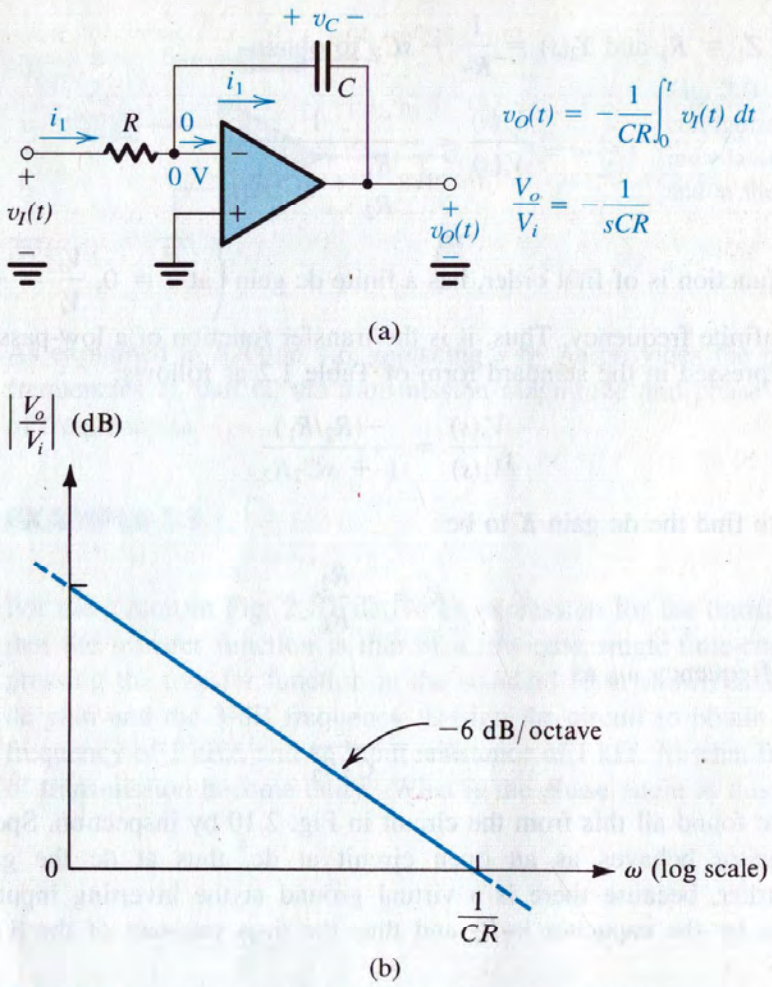


Fig. 2.11 **(a)** The Miller or inverting integrator. **(b)** Frequency response of the integrator.

this circuit realizes the mathematical operation of integration. Let the input be a time-varying function $v_I(t)$. The virtual ground at the inverting op-amp input causes $v_I(t)$ to appear in effect across R, and thus the current $i_1(t)$ will be $v_I(t)/R$. This current flows through the capacitor C, causing charge to accumulate on C. If we assume that the circuit begins operation at time $t = 0$, then at an arbitrary time t the current $i_1(t)$ will have deposited on C a charge equal to $\int_0^t i_1(t)\,dt$. Thus the capacitor voltage $v_C(t)$ will change by $\frac{1}{C}\int_0^t i_1(t)\,dt$. If the initial voltage on C (at $t = 0$) is denoted V_C, then

$$v_C(t) = V_C + \frac{1}{C}\int_0^t i_1(t)\,dt$$

Now the output voltage $v_O(t) = -v_C(t)$, thus

$$v_O(t) = -\frac{1}{CR}\int_0^t v_I(t)\,dt - V_C \tag{2.3}$$

Thus the circuit provides an output voltage that is proportional to the time-integral of the input, with V_C being the initial condition of integration and CR the **integrator time-constant.** Note that as expected there is a negative sign attached to the output voltage, and thus this integrator circuit is said to be an inverting integrator. It is also known as a **Miller integrator** after an early worker in this area.

The operation of the integrator circuit can be described alternatively in the frequency domain by substituting $Z_1(s) = R$ and $Z_2(s) = 1/sC$ in Eq. (2.2) to obtain the transfer function

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{sCR} \tag{2.4}$$

For physical frequencies, $s = j\omega$ and

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega CR} \tag{2.4a}$$

Thus the integrator transfer function has magnitude

$$\left|\frac{V_o}{V_i}\right| = \frac{1}{\omega CR} \tag{2.4b}$$

and phase

$$\phi = +90° \tag{2.4c}$$

The Bode plot for the integrator magnitude response can be obtained by noting from Eq. (2.4b) that as ω doubles (increases by an octave) the magnitude is halved (decreased by 6 dB). Thus the Bode plot is a straight line of slope -6 dB/octave (or equivalently, -20 dB/decade). This line [shown in Fig. 2.11(b)] intercepts the 0-dB line at the frequency that makes $|V_o/V_i| = 1$, which from Eq. (2.4b) is

$$\omega_{int} = \frac{1}{CR} \tag{2.5}$$

The frequency ω_{int} is known as the **integrator frequency** and is simply the inverse of the integrator time constant.

Comparison of the frequency response of the integrator to that of an STC low-pass network indicates that the integrator behaves as a low-pass filter with a corner frequency at zero. Observe also that at $\omega = 0$, the magnitude of the integrator transfer function is infinite. This indicates that at dc the op amp is operating with an open loop. This should also be obvious from the integrator circuit itself; reference to Fig. 2.11(a) shows that the feedback element is a capacitor, and thus at dc where the capacitor behaves as an open circuit, there is no negative feedback! This is a very significant observation and one that indicates a source of problems with the integrator circuit: Any tiny dc component in the input signal will theoretically produce an infinite output. Of course, no infinite output voltage results in practice; rather, the output of the amplifier saturates at a voltage close to the op-amp positive or negative power supply, depending on the polarity of the input dc signal. That real op

amps saturate should come as no surprise. Although we have not yet discussed op-amp saturation, we did study the saturation of amplifiers in general in Section 1.4 (see Fig. 1.13).

The problem of infinite or very high dc gain of the integrator (equal to the open-loop gain of the op amp) is solved by connecting a resistor R_F in parallel with the integrator capacitor C, as shown in Fig. 2.12. Resistor R_F closes the feedback loop at dc and provides the integrator with a finite dc gain of $-R_F/R$. Unfortunately, though, the resulting integrator is no longer ideal. The reader can show that R_F gives the integrator transfer-function a 3-dB frequency at $1/R_FC$. Thus, the integrator now behaves exactly as an STC low-pass network (see Example 2.3). To minimize the imperfection in integrator function introduced by R_F, we select as large an R_F as possible. The following example illustrates the effect of R_F on the time-domain performance of the integrator. We will have more to say about R_F in Section 2.9.

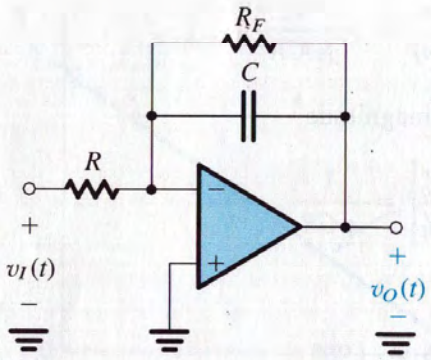


Fig. 2.12 The Miller integrator with a large resistance R_F connected in parallel with C in order to provide negative feedback at dc.

EXAMPLE 2.4

Find the output produced by a Miller integrator in response to an input pulse of 1-V height and 1-ms width [Fig. 2.13(a)]. Let $R = 10\ \text{k}\Omega$ and $C = 10\ \text{nF}$. If the integrator capacitor is shunted by a 1-MΩ resistor, how will the response be modified?

SOLUTION

In response to a 1-V, 1-ms input pulse, the integrator output will be

$$v_O(t) = -\frac{1}{CR}\int_0^t 1.dt, \qquad 0 \le t \le 1\ \text{ms}$$

where we have assumed that the initial voltage on the integrator capacitor is 0. For $C = 10\ \text{nF}$ and $R = 10\ \text{k}\Omega$, $CR = 0.1\ \text{ms}$, and

$$v_O(t) = -10t, \qquad 0 \le t \le 1\ \text{ms}$$

which is the linear ramp shown in Fig. 2.13(b). It reaches a magnitude of -10 V at $t = 1$ ms and remains constant thereafter.

That the output is a linear ramp should also be obvious from the fact that the 1-V input pulse produces a $1\ \text{V}/10\ \text{k}\Omega = 0.1\ \text{mA}$ constant current through the capacitor. This constant

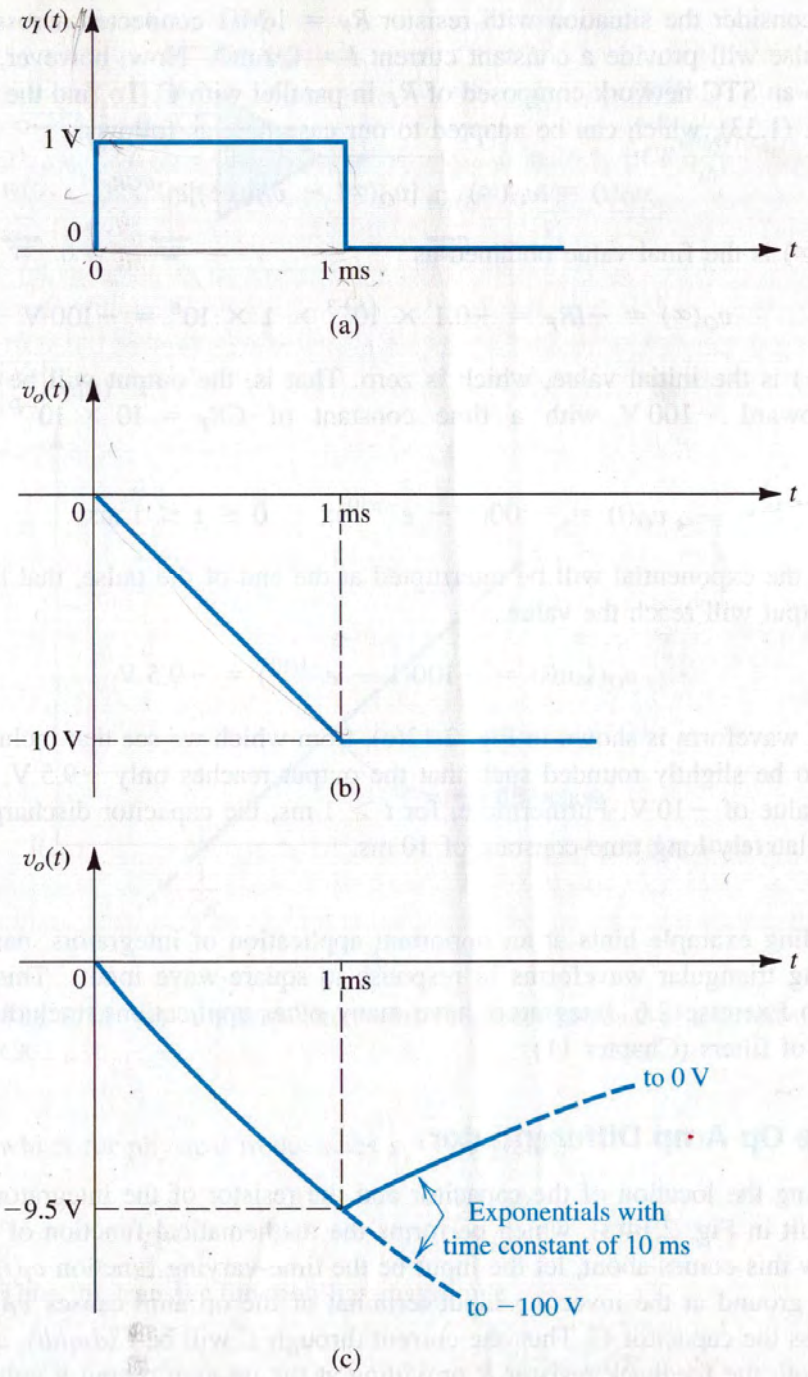


Fig. 2.13 Waveforms for Example 2.4: **(a)** Input pulse. **(b)** Output linear ramp of ideal integrator with time constant of 0.1 ms. **(c)** Output exponential ramp with resistor R_F connected across integrator capacitor.

current $I = 0.1$ mA supplies the capacitor with a charge It, and thus the capacitor voltage changes linearly as (It/C), resulting in $v_O = -\frac{I}{C}t$. It is worth remembering that charging a capacitor with a constant current produces a linear voltage across it.

Next consider the situation with resistor $R_F = 1\ \text{M}\Omega$ connected across C. As before, the 1-V pulse will provide a constant current $I = 0.1$ mA. Now, however, this current is supplied to an STC network composed of R_F in parallel with C. To find the output voltage, we use Eq. (1.33), which can be adapted to our case here as follows:

$$v_O(t) = v_O(\infty) - [v_O(\infty) - v_O(0+)]e^{-t/CR_F}$$

where $v_O(\infty)$ is the final value obtained as

$$v_O(\infty) = -IR_F = -0.1 \times 10^{-3} \times 1 \times 10^6 = -100\ \text{V}$$

and $v_O(0+)$ is the initial value, which is zero. That is, the output will be an exponential heading toward -100 V with a time constant of $CR_F = 10 \times 10^{-9} \times 1 \times 10^6 = 10$ ms,

$$v_O(t) = -100(1 - e^{-t/10}), \qquad 0 \le t \le 1\ \text{ms}$$

Of course, the exponential will be interrupted at the end of the pulse, that is, at $t = 1$ ms, and the output will reach the value

$$v_O(1\ \text{ms}) = -100(1 - e^{-1/10}) = -9.5\ \text{V}$$

The output waveform is shown in Fig. 2.13(c), from which we see that including R_F causes the ramp to be slightly rounded such that the output reaches only -9.5 V, 0.5 V short of the ideal value of -10 V. Furthermore, for $t > 1$ ms, the capacitor discharges through R_F with the relatively long time-constant of 10 ms.

The preceding example hints at an important application of integrators, namely, their use in providing triangular waveforms in response to square-wave inputs. This application is explored in Exercise 2.6. Integrators have many other applications, including their use in the design of filters (Chapter 11).

2.4.3 The Op Amp Differentiator

Interchanging the location of the capacitor and the resistor of the integrator circuit results in the circuit in Fig. 2.14(a), which performs the mathematical function of differentiation. To see how this comes about, let the input be the time-varying function $v_I(t)$, and note that the virtual ground at the inverting input terminal of the op amp causes $v_I(t)$ to appear in effect across the capacitor C. Thus the current through C will be $C(dv_I/dt)$, and this current flows through the feedback resistor R providing at the op-amp output a voltage $v_O(t)$,

$$v_O(t) = -CR\frac{dv_I(t)}{dt} \tag{2.6}$$

The frequency-domain transfer function of the differentiator circuit can be found by substituting in Eq. (2.2), $Z_1(s) = 1/sC$ and $Z_2(s) = R$ to obtain

$$\frac{V_o(s)}{V_i(s)} = -sCR \tag{2.7}$$

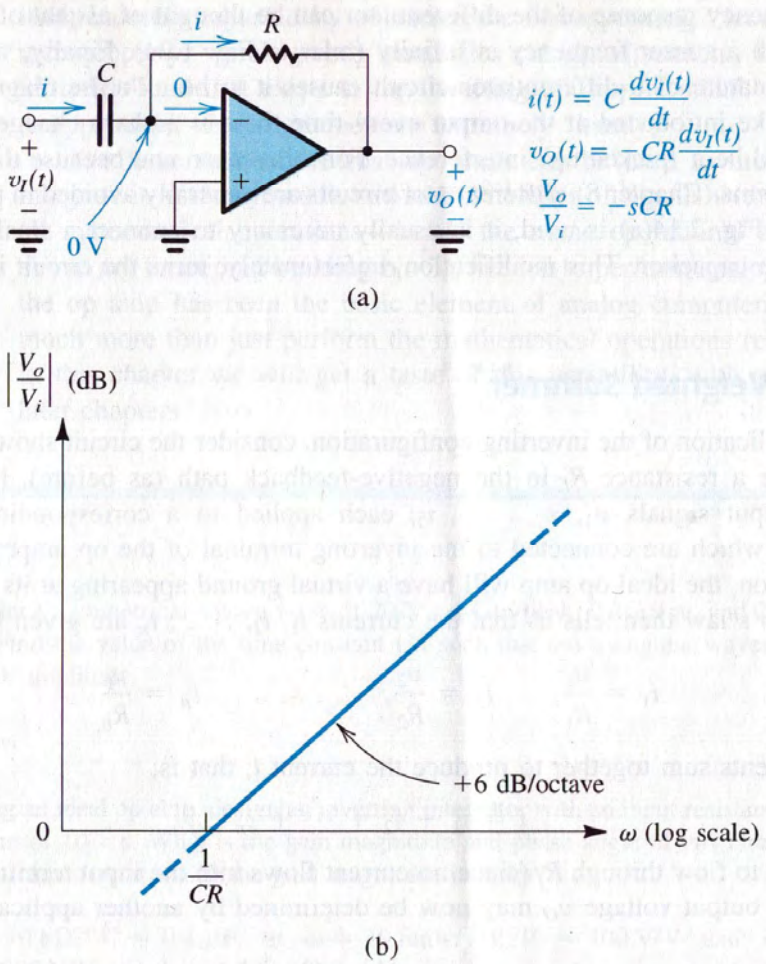


Fig. 2.14 **(a)** A differentiator. **(b)** Frequency response of a differentiator with a time constant CR.

which for physical frequencies $s = j\omega$ yields,

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega CR \tag{2.7a}$$

Thus the transfer function has magnitude

$$\left|\frac{V_o}{V_i}\right| = \omega CR \tag{2.7b}$$

and phase

$$\phi = -90° \tag{2.7c}$$

The Bode plot of the magnitude response can be found from Eq. (2.7b) by noting that for an octave increase in ω, the magnitude doubles (increases by 6 dB). Thus the plot is simply a straight line of slope +6 dB/octave (or equivalently, +20 dB/decade) intersecting the 0-dB line (where $|V_o/V_i| = 1$) at $\omega = 1/CR$, where CR is the **differentiator time-constant** [see Fig. 2.14(b)].

The frequency response of the differentiator can be thought of as that of an STC high-pass filter with a corner frequency at infinity (refer to Fig. 1.24). Finally, we should note that the very nature of a differentiator circuit causes it to be a "noise magnifier." This is due to the spike introduced at the output every time there is a sharp change in $v_I(t)$; such a change could be a "picked up" interference. For this reason and because they suffer from stability problems (Chapter 8), differentiator circuits are generally avoided in practice. When the circuit of Fig. 2.14(a) is used, it is usually necessary to connect a small resistance in series with the capacitor. This modification, unfortunately, turns the circuit into a nonideal differentiator.

2.4.4 The Weighted Summer

As a final application of the inverting configuration, consider the circuit shown in Fig. 2.15. Here we have a resistance R_f in the negative-feedback path (as before), but we have a number of input signals $v_1, v_2, \ldots, v_n$ each applied to a corresponding resistor R_1, $R_2, \ldots, R_n$, which are connected to the inverting terminal of the op amp. From our previous discussion, the ideal op amp will have a virtual ground appearing at its negative input terminal. Ohm's law then tells us that the currents $i_1, i_2, \ldots, i_n$ are given by

$$i_1 = \frac{v_1}{R_1}, \qquad i_2 = \frac{v_2}{R_2}, \qquad \ldots, \qquad i_n = \frac{v_n}{R_n}$$

All these currents sum together to produce the current i; that is,

$$i = i_1 + i_2 + \cdots + i_n \tag{2.8}$$

will be forced to flow through R_f (since no current flows into the input terminals of an ideal op amp). The output voltage v_O may now be determined by another application of Ohm's law,

$$v_O = 0 - iR_f = -iR_f$$

Thus

$$v_O = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n\right) \tag{2.9}$$

That is, the output voltage is a weighted sum of the input signals $v_1, v_2, \ldots, v_n$. This circuit is therefore called a **weighted summer.** Note that each summing coefficient may be

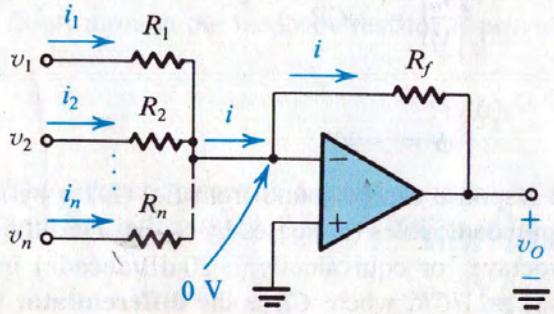


Fig. 2.15 A weighted summer.

$$v_O = -\left(\frac{R_f}{R_1}v_1 + \frac{R_f}{R_2}v_2 + \cdots + \frac{R_f}{R_n}v_n\right)$$

independently adjusted by adjusting the corresponding "feed-in" resistor (R_1 to R_n). This nice property, which greatly simplifies circuit adjustment, is a direct consequence of the virtual ground that exists at the inverting op amp terminal. As the reader will soon come to appreciate, virtual grounds are extremely "handy."

We have seen above that op amps can be used to multiply a signal by a constant, integrate it, differentiate it, and sum a number of signals with prescribed weights. These are all mathematical operations—hence the name operational amplifier. In fact, the circuits above are functional building blocks needed to perform analog computation. For this reason the op amp has been the basic element of analog computers. Op amps, however, can do much more than just perform the mathematical operations required in analog computation. In this chapter we will get a taste of this versatility, with other applications presented in later chapters.

Exercises

2.6 Consider a symmetrical square wave of 20-V peak-to-peak, 0 average, and 2-ms period applied to a Miller integrator. Find the value of the time constant CR such that the triangular waveform at the output has a 20-V peak-to-peak amplitude.

Ans. 0.5 ms

D2.7 Using an ideal op amp, design an inverting integrator with an input resistance of 10 kΩ and an integration time constant of 10^{-3} s. What is the gain magnitude and phase angle of this circuit at 10 rad/s and at 1 rad/s? What is the frequency at which the gain magnitude is unity?

Ans. $R = 10\,\text{k}\Omega$, $C = 0.1\,\mu\text{F}$; at $\omega = 10$ rad/s: $|V_o/V_i| = 100$ V/V and $\phi = +90°$; at $\omega = 1$ rad/s: $|V_o/V_i| = 1{,}000$ V/V and $\phi = +90°$; 1000 rad/s

D2.8 Design a differentiator to have a time constant of 10^{-2} s and an input capacitance of 0.01 μF. What is the gain magnitude and phase of this circuit at 10 rad/s, and at 10^3 rad/s? In order to limit the high-frequency gain of the differentiator circuit to 100, a resistor is added in series with the capacitor. Find the required resistor value.

Ans. $C = 0.01\,\mu\text{F}$; $R = 1\,\text{M}\Omega$; at $\omega = 10$ rad/s: $|V_o/V_i| = 0.1$ V/V and $\phi = -90°$; at $\omega = 1000$ rad/s: $|V_o/V_i| = 10$ V/V and $\phi = -90°$; 10 kΩ

D2.9 Design an inverting op-amp circuit to form the weighted sum v_O of two inputs v_1 and v_2. It is required that $v_O = -(v_1 + 5v_2)$. Choose values for R_1, R_2, and R_f so that for a maximum output voltage of 10 V the current in the feedback resistor will not exceed 1 mA.

Ans. A possible choice: $R_1 = 10\,\text{k}\Omega$, $R_2 = 2\,\text{k}\Omega$, and $R_f = 10\,\text{k}\Omega$

2.5 THE NONINVERTING CONFIGURATION

The second closed-loop configuration we shall study is shown in Fig. 2.16. Here the input signal v_I is applied directly to the positive input terminal of the op amp while one terminal of R_1 is connected to ground.

is physically connected to ground. In what follows we will not explicitly show the op-amp power supplies.

In addition to the three signal terminals and the two power-supply terminals, an op amp may have other terminals for specific purposes. These other terminals can include terminals for frequency compensation and terminals for offset nulling: both functions will be explained in later sections.

Exercise

2.1 What is the minimum number of terminals required by a single op amp? What is the minimum number of terminals required on an integrated-circuit package containing four op amps (called a quad op amp)?

Ans. 5; 14

2.2 THE IDEAL OP AMP

We now consider the circuit function of the op amp. The op amp is designed to sense the difference between the voltage signals applied at its two input terminals (that is, the quantity $v_2 - v_1$), multiply this by a number A, and cause the resulting voltage $A(v_2 - v_1)$ to appear at output terminal 3. Here it should be emphasized that when we talk about the voltage at a terminal we mean the voltage between that terminal and ground; thus v_1 means the voltage applied between terminal 1 and ground.

The ideal op amp is not supposed to draw any input current; that is, the signal current into terminal 1 and the signal current into terminal 2 are both zero. In other words, the input impedance of an ideal op amp is supposed to be infinite.

How about the output terminal 3? This terminal is supposed to act as the output terminal of an ideal voltage source. That is, the voltage between terminal 3 and ground will always be equal to $A(v_2 - v_1)$ and will be independent of the current that may be drawn from terminal 3 into a load impedance. In other words, the output impedance of an ideal op amp is supposed to be zero.

Putting together all of the above, we arrive at the equivalent circuit model shown in Fig. 2.3. Note that the output is in phase with (has the same sign as) v_2 and out of phase with (has the opposite sign of) v_1. For this reason, input terminal 1 is called the **inverting input terminal** and is distinguished by a "−" sign, while input terminal 2 is called the **noninverting input terminal** and is distinguished by a "+" sign.

As can be seen from the above description, the op amp responds only to the *difference* signal $v_2 - v_1$ and hence ignores any signal *common* to both inputs. That is, if $v_1 = v_2 = 1$ V, then the output will—ideally—be zero. We call this property **common-mode rejection,** and we conclude that an ideal op amp has infinite common-mode rejection. We will have more to say about this point later. For the time being note that the op amp is a **differential-input, single-ended-output** amplifier, with the latter term referring to the fact that the output appears between terminal 3 and ground. Furthermore, gain A is called the **differential gain,** for obvious reasons. Perhaps not so obvious is another name that we will

An even simpler and more direct bias arrangement is shown in Fig. 5.39(c). Here, a constant-current source I feeds the source terminal, thus establishing $I_D = I$. We shall shortly study MOSFET circuits that implement constant-current sources. Resistors R_G and R_D serve the same purposes as in the two previous circuits.

Finally, the circuit in Fig. 5.39(d) employs a large feedback resistor R_G that forces the dc voltage at the gate to be equal to that at the drain (because $I_G = 0$). The input signal can be capacitively coupled to the gate and the output taken from the drain, resulting in a simple common-source amplifier. We have studied such a design in Example 5.8. Observe that in this circuit the output signal swing should be limited in the negative direction to $|V_t|$, otherwise the drain voltage falls below $V_{GS} - V_t$ and the device leaves the saturation region. Finally, note that although the circuits in Fig. 5.39 are shown for the case of n-channel devices, complementary circuits can be easily sketched for p-channel MOSFETs. We urge the reader to do this.

Exercises

5.22 Design the circuit of Fig. 5.39(b) for a MOSFET having $k_n'(W/L) = 0.5\ \text{mA/V}^2$ and $V_t = 2\ \text{V}$, and utilizing two power supplies of $\pm 10\ \text{V}$. Design for $I_D = 1\ \text{mA}$ and allow for a signal swing at the drain of $\pm 2\ \text{V}$. The amplifier is required to present a 1-MΩ input resistance to a signal source that is capacitively coupled to the gate. Assume $\lambda = 0$.

Ans. $R_G = 1\ \text{M}\Omega$, $R_S = 6\ \text{k}\Omega$, $R_D = 10\ \text{k}\Omega$

5.23 In the circuit designed in Exercise 5.22, find the change in drain current resulting from replacing the MOSFET with another having $V_t = 3\ \text{V}$.

Ans. −14%

5.6.2 Biasing in Integrated-Circuit MOS Amplifiers

Basic Philosophy. The circuits of Fig. 5.39 are not suitable for biasing MOSFET amplifiers that are to be fabricated using integrated-circuit (IC) technology. This is because they make extensive use of resistors. In MOS integrated-circuit design, the use of resistors is discouraged, for a resistor of even a modest value requires a relatively large area of the silicon chip and thus is considered "expensive" in terms of the economics of IC fabrication, which are based on the cost of "silicon real estate." Furthermore, without additional expensive processing steps, the values of IC resistors exhibit large tolerances. By contrast, a MOSFET can be fabricated in a very small area on the IC chip, and its parameters are relatively well controlled. It follows that the basic philosophy in IC design is to minimize the number (and more importantly, the total value) of resistors, and instead utilize transistors to perform the wide variety of functions required in the design of electronic circuits.

Another reason that the biasing arrangements of Fig. 5.39 are not suitable for IC amplifiers is that the circuits shown anticipate that the input signal source would be capacitively coupled to the amplifier input, that the output signal would be capacitively coupled to either

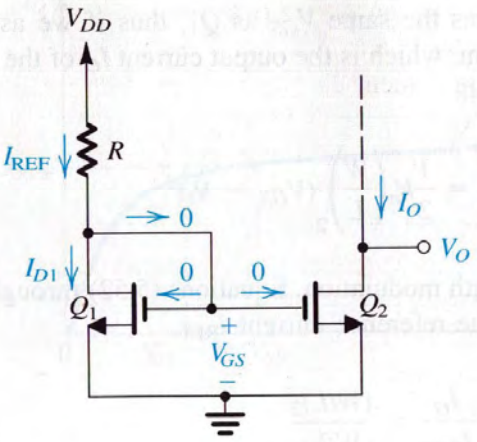


Fig. 5.40 Circuit for a basic MOSFET constant-current source.

another amplifier stage or an actual load, and that bypass capacitors would be employed to establish ac grounds as required. Indeed, we have seen these methods utilized in discrete BJT amplifiers in Chapter 4. Although capacitors can be fabricated in IC form, chip-area considerations limit the total capacitance on a chip to a few picofarads or at most a few tens of picofarads. This obviously rules out the use of large coupling and bypass capacitors. Rather, different methods are used in the design of IC MOS and BJT amplifiers, as will be shown in later sections and chapters.

The Basic MOSFET Current Source. Biasing of IC MOS amplifiers utilizes constant-current sources. Specifically, a constant current is generated and is then replicated at various locations in the IC in order to provide dc bias currents for the various amplifier stages.

Figure 5.40 shows the circuit of a simple MOS constant-current source. The heart of the circuit is transistor Q_1 whose drain is shorted to its gate[6] and thus is operating in the saturation region, such that

$$I_{D1} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2 \tag{5.52}$$

where we have neglected channel-length modulation (i.e., assumed $\lambda = 0$). The drain current of Q_1 is supplied by V_{DD} through resistor R (which in some cases would be outside the IC chip). Since the gate currents are zero,

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R} \tag{5.53}$$

where the current through R is considered to be the reference current of the current source and is denoted I_{REF}. Given the parameter values of Q_1, and a desired value for I_{REF}, Eqs. (5.52) and (5.53) can be used to determine the value required for R.

[6] Since this turns the three-terminal transistor into a two-terminal device, the transistor is said to be diode connected. More on this in Section 5.7.

Now consider transistor Q_2: It has the same V_{GS} as Q_1, thus if we assume that it is operating in saturation, its drain current, which is the output current I_O of the current source, will be

$$I_O = I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2 \tag{5.54}$$

where we have neglected channel-length modulation. Equations (5.52) through (5.54) enable us to relate the output current I_O to the reference current I_{REF},

$$\frac{I_O}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \tag{5.55}$$

This is a simple and attractive relationship. The special connection of Q_1 and Q_2 provides an output current I_O that is related to the reference current I_{REF} by the ratio of the aspect ratios of the transistors; that is, the relationship between I_O and I_{REF} is solely determined by the geometry of the transistors. In the special case of identical transistors, $I_O = I_{REF}$, and the circuit simply replicates or *mirrors* the reference current in the output terminal. This has given the circuit composed of Q_1 and Q_2 the name **current mirror**, a name that is used irrespective of the ratio of device dimensions.

Figure 5.41 shows the current-mirror circuit with the input reference current shown as being supplied by a current source, for simplicity. The *current gain* or *current transfer ratio* of the current mirror is given by Eq. (5.55). The reader will recall a similar current-mirror circuit implemented with BJTs (see Fig. 4.42b). Finally, it should be noted that the circuit of Fig. 5.41 is the basic form of current-mirror circuits; more advanced circuit implementations of the current-mirroring function in both MOS and BJT technologies will be studied in Chapter 6. Current mirrors are essential building blocks in the design of IC amplifiers.

Effect of V_O on I_O. In the above description of the operation of the current source of Fig. 5.40, we assumed that Q_2 is operating in saturation. This is obviously essential if Q_2

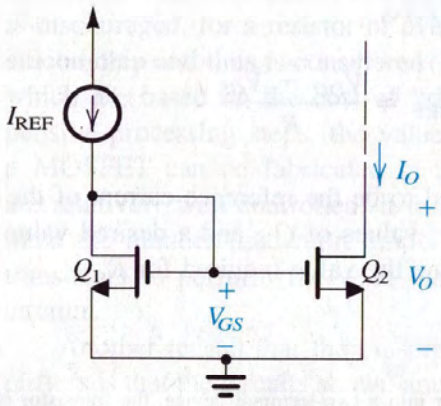


Fig. 5.41 Basic MOSFET current mirror.

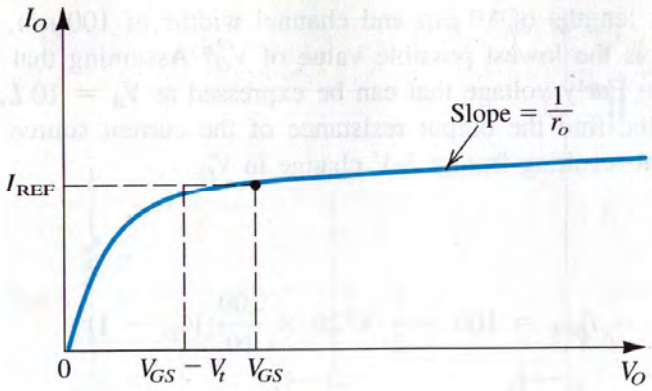


Fig. 5.42 Output characteristic of the current source in Fig. 5.40 and the current mirror of Fig. 5.41 for the case Q_2 is matched to Q_1.

is to supply a constant-current output. To ensure that Q_2 is saturated, the circuit to which the drain of Q_2 is to be connected must establish a drain voltage V_O that satisfies the relationship

$$V_O \geq V_{GS} - V_t \tag{5.56}$$

In other words, the current source will operate properly for voltages V_O as low as $|V_t|$ volts below V_{GS}.

Although thus far neglected, channel-length modulation can have a significant effect on the operation of the current source. Consider for simplicity the case of identical devices Q_1 and Q_2. The drain current of Q_2, I_O, will equal the current in Q_1, I_{REF}, only at the value of V_O that causes the two devices to have the same V_{DS}, that is, at $V_O = V_{GS}$. As V_O is increased above this value, I_O will increase according to the incremental output resistance r_{o2} of Q_2. This is illustrated in Fig. 5.42, which shows I_O versus V_O. Observe that since Q_2 is operating at a constant V_{GS} (determined by passing I_{REF} through the matched device Q_1), the curve in Fig. 5.42 is simply the i_D–v_{DS} characteristic curve of Q_2 for v_{GS} equal to the particular value V_{GS}.

In summary, the current source of Fig. 5.40 and the current mirror of Fig. 5.41 have finite output resistance R_o,

$$R_o = \frac{\Delta V_O}{\Delta I_O} = r_{o2} = \frac{V_{A2}}{I_O} \tag{5.57}$$

where I_O is given by Eq. (5.54) and V_{A2} is the Early voltage of Q_2. Also recall that V_A is proportional to the transistor channel length; thus to obtain high output-resistance values, current sources are usually designed using transistors with long channels.

EXAMPLE 5.9

Given $V_{DD} = 5$ V and using $I_{REF} = 100\ \mu$A, it is required to design the circuit of Fig. 5.40 to obtain an output current whose nominal value is 100 μA. Find R if Q_1 and Q_2 are

APPENDIX LAKER01

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leader  03586cam a2200493 a 4500
001     999395611005961
005     20240711095702.0
008     931215s1994    nyua     b    001 0 eng
010     ##$a   93049574
015     ##$aGB94434946 $2bnb
015     ##$aGB94-34946
019     ##$a1167089490 $a1421144206
020     ##$a007036060X $q(alk. paper)
020     ##$a9780070360600 $q(alk. paper)
020     ##$a0071134581
020     ##$a9780071134583
035     ##$a(OCoLC)29598745 $z(OCoLC)1167089490 $z(OCoLC)1421144206
040     ##$aDLC $beng $cDLC $dDAY $dUKM $dIXA $dBAKER $dBTCTA $dYDXCP $dOCLCG $dZWZ $dZCU $dDEBBG $dTULIB $dILU $dBDX $dOCLCO $dOCLCF $dOCLCQ $dOCLCO $dOCLCQ $dOCLCO $dPHUST $dOCLCO $dOCLCQ $dCPO $dOCLCQ $dLUN $dOCLCO $dOCLCL $dOCLCQ $dLHL
049     ##$aLHLA
050     00$aTK7874 $b.L26 1994
082     00$a621.3815 $220
084     ##$aZN 4920 $2rvk
084     ##$aELT 443f $2stub
084     ##$aELT 346f $2stub
090     ##$aTK7874 $b.L26 1994
100     1#$aLaker, Kenneth R., $d1946- $1https://id.oclc.org/worldcat/entity/E39PCjFcvHkB8p6B9Fc6gwKmkC
245     10$aDesign of analog integrated circuits and systems / $cKenneth R. Laker, Willy M.C. Sansen.
260     ##$aNew York : $bMcGraw-Hill, $c©1994.
300     ##$axxii, 898 pages : $billustrations (some color) ; $c24 cm.
336     ##$atext $btxt $2rdacontent
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520     8#$aOther features include early and complete coverage of feedback and sensitivity concepts; integration of important topics such as noise, nonlinear distortion, and power supply rejection throughout the text; emphasis on design intu
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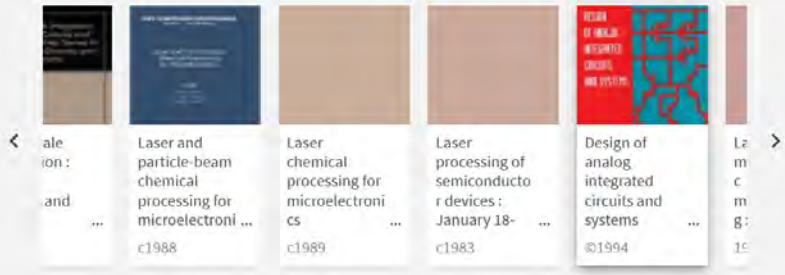
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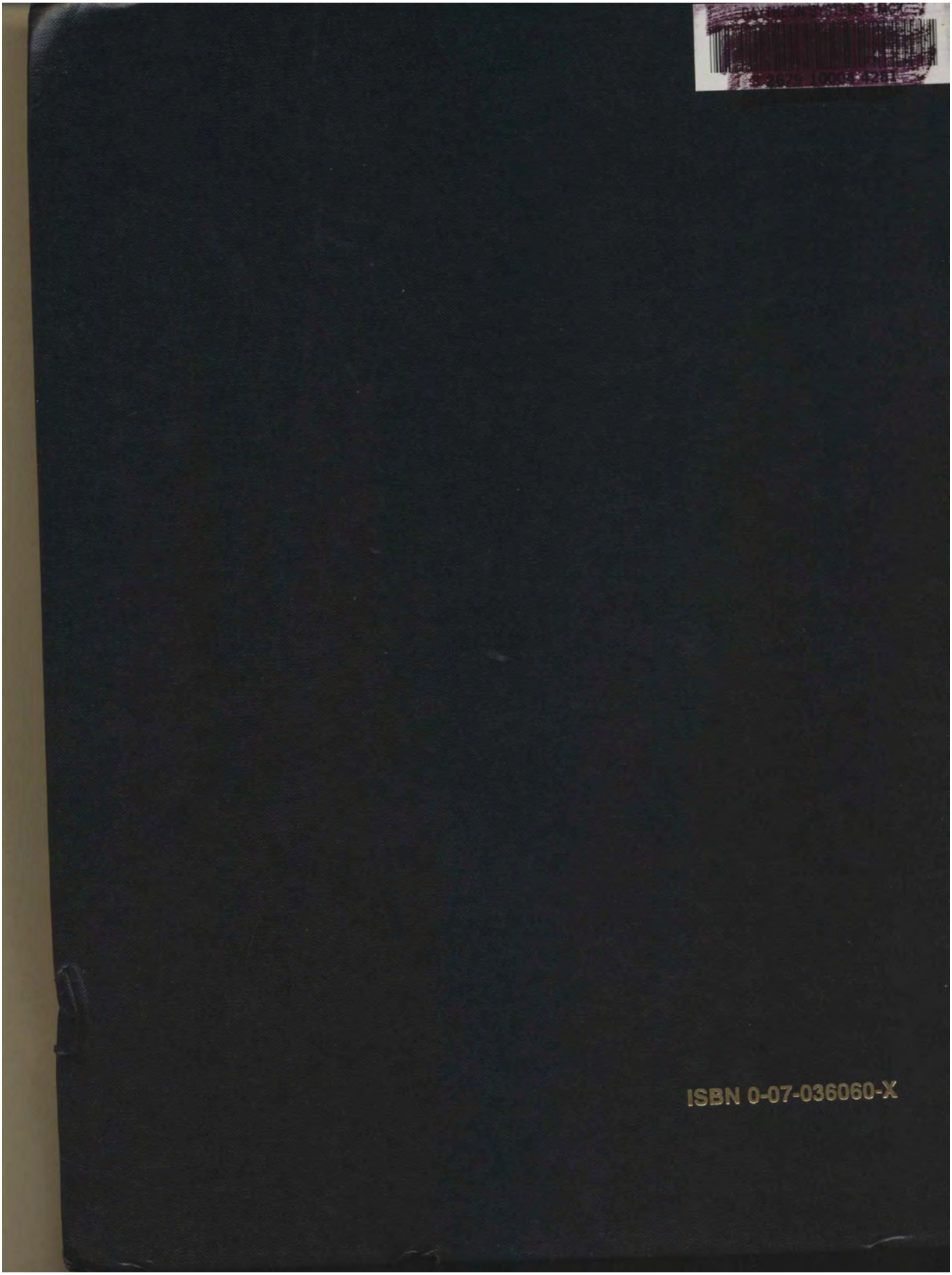
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CONTENTS

Preface xix

1 MOS Transistor Models 1

Introduction 1

1-1 MOSFET and Junction FET 2

1-1-1 JFET 2

1-1-2 MOST 2

1-1-3 nMOST and pMOST 4

1-2 Capacitances and MOST Threshold Voltages 5

1-2-1 MOS Capacitance 5

1-2-2 Junction Capacitance 6

1-2-3 MOST and JFET 7

1-2-4 MOST Threshold Voltage 9

1-2-5 Enhancement and Depletion MOST 12

1-3 MOST Linear Region and Saturation Region 14

1-3-1 Large v_{GS}, Small v_{DS}, and Zero v_{BS} 14

1-3-2 Large v_{GS}, Large v_{DS}, and Zero v_{BS} 15

1-3-3 Large v_{GS}, Small v_{DS}, and Large v_{BS} 17

1-4 MOST Current-Voltage Characteristics 17

1-4-1 Linear Region 17

1-4-2 Linear Region: First-Order Model 18

1-4-3 MOST in Saturation: First-Order Model 19

1-4-4 Parameters K' and n 20

1-4-5 Plots of i_{DS} versus v_{GS} and v_{BS} 22

1-4-6 Effective Channel Length and Width 23

1-5 Small-Signal Model in Saturation 23

1-5-1 Transconductance g_m 25

1-5-2 Bulk Transconductance g_{mb} 26
1-5-3 Output Resistance r_o 26
1-6 Weak Inversion and Velocity Saturation 27
1-6-1 MOST in Weak Inversion 27
1-6-2 Transconductance-Current Ratio 29
1-6-3 Transition Weak-Strong Inversion 30
1-6-4 MOST in Velocity Saturation 32
1-7 Examples of Small-Signal Analysis 32
1-7-1 Example of Transconductance Amplifier 32
1-7-2 Example of Voltage Amplifier with Active Load 33
1-7-3 Example of a MOST Diode 35
1-7-4 Example of Source Follower 36
1-7-5 Example of MOST as a Switch with Resistive Load 38
1-7-6 Example with a MOST as a Switch with Capacitive Load 41
1-8 Capacitances 43
1-8-1 MOST: Oxide Capacitance C_{ox} 45
1-8-2 MOST Junction Capacitances 45
1-8-3 MOST Junction Leakage Currents and Capacitances 47
1-8-4 Interconnect Capacitances 47
1-8-5 Bonding Pad Capacitance 49
1-8-6 Package Pin Capacitance 49
1-8-7 Protection Network Capacitance 50
1-8-8 Total Capacitance Configurations 50
1-9 Higher-Order Models 51
1-9-1 VT0-KP-GAMMA-LAMBDA or TOX-PHI-NSUB-NSS? 52
1-9-2 Parasitic Resistances 52
1-9-3 Mobility Degradation Due to Longitudinal Electric Field 53
1-9-4 Mobility Degradation Due to Transverse Electric Field 55
1-9-5 Channel Width Factor DELTA 56
1-9-6 Static Feedback Effect Parameter ETA 57
1-9-7 Onset of Short-Channel Effects 58
1-9-8 Punchthrough and Substrate Currents 58
1-10 Design Example 60
1-11 Junction FETs 62
1-11-1 JFET Pinchoff Voltage 62
1-11-2 JFET DC Model 65
1-11-3 JFET: DC Model in Linear Region 66
1-11-4 JFET DC Model: Onset of Saturation 67
1-11-5 JFET DC Model in Saturation 69
1-11-6 Model for Wide-Channel JFETs 69
1-11-7 JFET DC Model in Saturation: Subthreshold Region 71
1-11-8 JFET Small-Signal Models 71
1-11-9 JFET Example: MESFET 73
1-11-10 JFET Design Example 74
1-12 Noise Sources in FET 74
1-12-1 Thermal or Johnson Noise 77
1-12-2 Shot Noise 78
1-12-3 $1/f$ Noise or Flicker Noise 79

1-12-4 Other Noise Sources 81
1-12-5 Total Noise 81
1-12-6 FET Noise Models 83
1-12-7 $1/f$ Noise in SPICE 84
1-12-8 Equivalent Input Noise Current 85
1-12-9 Gate Leakage Noise 86
Summary 86
Exercises 86
Appendix 1-1: Notation of Symbols 90
References 91

2 Bipolar Transistor Models 92

2-1 Bipolar Transistor Operation 92
2-1-1 Structure 92
2-1-2 Depletion Layers 96
2-1-3 Base Doping 96
2-1-4 Forward Biasing 96
2-1-5 Base Transit Time 100
2-2 The Transistor Beta (β) 101
2-2-1 Beta Caused by Injection in the Emitter β_{IE} 102
2-2-2 Beta Caused by Recombination in the Base β_{RB} 102
2-2-3 Beta Caused by Recombination in the *EB* Space Charge Layer 102
2-2-4 AC Beta β_{AC} 103
2-3 The Hybrid-π Small-Signal Model 106
2-3-1 Transconductance g_m 106
2-3-2 Input Resistance r_π 106
2-3-3 Output Resistance r_o 107
2-3-4 Voltage Gain of Small-Signal Gain Stage 110
2-3-5 Junction Capacitances 110
2-3-6 Diffusion Capacitance C_D 112
2-3-7 Common-Emitter Configuration with Current Drive 112
2-3-8 Common-Emitter Configuration with Voltage Drive 116
2-3-9 Common-Collector and Common-Base Configurations 117
2-4 The Ohmic Resistances 121
2-4-1 The Base Resistance 121
2-4-2 Extrinsic Base Resistance 121
2-4-3 Intrinsic Base Resistance 121
2-4-4 The Collector Resistances 125
2-4-5 The Emitter Resistance 126
2-5 High-Injection and Other Second-Order Effects 126
2-5-1 High-Injection Effects in the Base 127
2-5-2 High-Injection Model of Beta 130
2-5-3 Base Resistance Effects 131
2-5-4 Graded Base 131
2-5-5 Collector Current Spreading 131
2-5-6 High-Injection Effects in the Collector 132
2-5-7 Bipolar Transistors for VLSI 132
2-6 Lateral *pnp* Transistors 134
2-6-1 Substrate *pnp* Transistors 134

2-6-2 Lateral *pnp* Transistors 137
2-6-3 Base Width, Early Voltage, and Punchthrough 139
2-6-4 Base Resistance and Emitter Crowding 139
2-6-5 Applications with *pnp*'s 139
2-7 Noise 142
2-7-1 Input Noise Sources 142
2-7-2 Equivalent Input Noise Sources 143
2-7-3 Noise Figure 144
2-7-4 Optimum R_S 145
2-7-5 Optimum NF 146
2-7-6 Optimum I_C 146
2-8 Design Example 147
2-9 Other Components 147
2-9-1 Base Diffusion Resistors 147
2-9-2 Other Resistors 149
2-9-3 Temperature Coefficient 150
2-9-4 Voltage Coefficient 151
2-9-5 Frequency Dependence 151
2-9-6 Absolute and Relative Accuracy 152
2-9-7 Resistors in a CMOS Process 153
2-9-8 Thin Film Resistors 153
2-9-9 Capacitors 153
2-9-10 Inductors 155
2-10 Comparison between MOSTs and Bipolar Transistors 156
2-10-1 Input Current 157
2-10-2 DC Saturation Voltage 157
2-10-3 Transconductance-Current Ratio 159
2-10-4 Design Planning 160
2-10-5 Current Range 160
2-10-6 Maximum Frequency of Operation 160
2-10-7 Noise 161
Summary 162
Exercises 162
Appendix 2-1 164
References 169

3 Feedback and Sensitivity in Analog Integrated Circuits 170

Introduction 170
3-1 Feedback Theory 172
3-1-1 Basic Feedback Concepts and Definitions 177
3-1-2 Feedback Configurations and Classifications 185
3-2 Analysis of Feedback Amplifier Circuits 188
3-2-1 Analysis When the Feedback Network is One of the Four Basic Configurations in Fig. 3-7 189
3-2-2 Blackman's Impedance Relation 194
3-2-3 The Asymptotic Gain Relation 198
3-3 Stability Considerations in Linear Feedback Systems 200
3-3-1 Effect of Feedback on the System Natural Frequencies 202
3-3-2 The Use of Bode Plots in Stability Analysis 212

3-4 Sensitivity, Component Matching and Yield 219
3-4-1 Component Matching 221
3-4-2 Sensitivity Problem in Precision Analog Circuits 222
3-4-3 Yield Considerations in Analog Integrated Circuits 226
Summary 231
Exercises 232
Appendix 3-1: Approximate Calculations for a Two-Pole System when the Poles are Real and Widely Separated 238
Appendix 3-2: Exact Calculation of the Bode Diagram for Two-Pole Systems 241
References 244

4 Elementary Transistor Stages 245
Introduction 245
4-1 MOST Single-Transistor Amplifying Stages 247
4-1-1 Biasing 247
4-1-2 Low Frequency Gain 249
4-1-3 Bandwidth 252
4-1-4 Full Circuit Performance at High Frequencies 261
4-1-5 Unity-Gain Frequency and Gain-Bandwidth Product 269
4-1-6 Noise Performance 276
4-2 Bipolar Single-Transistor Amplifying Stages 277
4-2-1 Biasing 277
4-2-2 Gain for Voltage Drive and Current Drive 280
4-2-3 Frequency Performance 281
4-2-4 Gain-Bandwidth Product 283
4-2-5 Input Impedance 288
4-3 Source and Emitter Followers 291
4-3-1 Source Followers 292
4-3-2 Emitter Followers 300
4-3-3 Noise Performance 307
4-4 Cascode Transistors 308
4-4-1 MOST Cascodes 308
4-4-2 Bipolar Transistor Cascodes 313
4-4-3 Noise Performance 314
4-5 CMOS Inverter Stages 316
4-5-1 DC Analysis of CMOS Inverters 316
4-5-2 Low Frequency Gain 324
4-5-3 Bandwidth 326
4-5-4 Current Capability and Slew Rate 329
4-5-5 Design Procedure 332
4-5-6 Other MOST Inverters 334
4-5-7 Bipolar Transistor Inverter Stages 337
4-5-8 Noise Performance 341
4-6 Cascode Stages 343
4-6-1 Cascode Configurations 343
4-6-2 Bandwidth of Cascode with Low R_L 345
4-6-3 Cascode with Active Load 346
4-6-4 Noise Performance 352
4-6-5 High Voltage Cascode 353

4-6-6 Cascode Stages with Bipolar Transistors 354
4-6-7 Feedforward in Cascode Amplifiers 355
4-7 Differential Stages 357
4-7-1 Definitions 357
4-7-2 MOST Differential Stages 359
4-7-3 Bipolar Transistor Differential Stages 372
4-8 Current Mirrors 378
4-8-1 Definitions 378
4-8-2 Simple MOST Current Mirror 379
4-8-3 Other MOST Current Mirrors 381
4-8-4 Bipolar Transistor Current Mirrors 383
4-8-5 Noise Output of Current Mirrors 387
Summary 391
Exercises 393
Appendix 4-1: The Pole-Zero Diagram: Evaluation of a Transfer Characteristic for Different Parameters 401
References 407

5 Behavioral Modeling of Operational and Transconductance Amplifiers 408
Introduction 408
5-1 The Op Amp Schematic Symbol and Ideal Model 410
5-2 Analysis of Circuits Involving Op Amps 414
5-2-1 Inverting Configuration 414
5-2-2 Noninverting Configuration 425
5-3 Practical Op Amp Characteristics and Model 434
5-3-1 Gain-Bandwidth and Compensation 434
5-3-2 Step Response and Settling 442
5-3-3 Slew Rate and Full Power Bandwidth 444
5-3-4 DC Offsets and DC Bias Currents 448
5-3-5 Common Mode Signals 452
5-3-6 Noise 453
5-4 Differential and Balanced Configurations 456
5-5 The Operational Transconductance Amplifier (OTA) 462
5-5-1 Ideal Model 463
5-5-2 OTA Building Block Circuits 464
5-5-3 Practical Considerations 465
Summary 467
Exercises 467
References 474

6 Operational Amplifier Design 475
Introduction 475
6-1 Design of a Simple CMOS OTA 477
6-1-1 Gain of the Simple CMOS OTA 478
6-1-2 The *GBW* and Phase-Margin 479
6-1-3 Design Plan 482
6-1-4 Optimization for Maximum *GBW* 482
6-2 The Miller CMOS OTA 486

	6-2-1	Operating Principles and Biasing	486
	6-2-2	Gain of the Miller OTA	489
	6-2-3	Gain-Bandwidth Product and Phase-Margin	491
	6-2-4	Design Plan	497
	6-2-5	Miller BICMOS OTAs	500
6-3	Full Set of Characteristics of the Miller OTA		500
	6-3-1	Full DC Analysis: Common-Mode Input Voltage Range versus Supply Voltage	502
	6-3-2	Full DC Analysis: Output Range versus Supply Voltage	503
	6-3-3	Full DC Analysis: Maximum Output Current (Source and Sink)	504
	6-3-4	AC Analysis: Low Frequencies	505
	6-3-5	Gain-Bandwidth versus Biasing Current	507
	6-3-6	Slew Rate versus Load Capacitance	510
	6-3-7	Output Voltage Range versus Frequency	511
	6-3-8	Settling Time	513
	6-3-9	Input Impedance	515
	6-3-10	Output Impedance	519
	6-3-11	Temperature Effects	522
6-4	Noise Analysis of OTAs		523
	6-4-1	Noise Performance at Low Frequencies	524
	6-4-2	Noise Performance at High Frequencies	527
	6-4-3	Total Integrated Output Noise	532
6-5	Matching Specifications		535
	6-5-1	Transistor Mismatch Model	535
	6-5-2	Offset Voltage Definition	537
	6-5-3	Mismatch Effects on a Current Mirror	539
	6-5-4	Differential Stage with Active Load	540
	6-5-5	Offset Drift	543
	6-5-6	*CMRR*	544
	6-5-7	Relation between Random V_{osr} and $CMRR_r$	546
	6-5-8	Relation between Systematic V_{oss} and $CMRR_r$	546
	6-5-9	*CMRR* versus Frequency	548
	6-5-10	Offset and *CMRR* of the Miller CMOS OTA	548
	6-5-11	Design for Low Offset and Drift	552
	6-5-12	Offset in JFET Differential Amplifier	556
	6-5-13	Offset and *CMRR* in Bipolar Differential Amplifier	556
	6-5-14	Bias Current, Offset, and Drift	558
6-6	Power Supply Rejection Ratio		562
	6-6-1	$PSRR_{DD}$ of Simple CMOS OTA	563
	6-6-2	$PSRR_{SS}$ of Simple CMOS OTA	567
	6-6-3	$PSRR_{DD}$ of the Miller CMOS OTA	569
	6-6-4	$PSRR_{SS}$ of the Miller CMOS OTA	572
6-7	Design of Other OTAs		575
	6-7-1	Symmetrical CMOS OTA	575
	6-7-2	Cascode Symmetrical CMOS OTA	583
	6-7-3	Symmetrical Miller CMOS OTA with High *PSRR*	585
	6-7-4	Folded-Cascode CMOS OTA	587
	6-7-5	Operational Current Amplifier (OCA)	591

6-8 Design Options 595
6-8-1 Design for Optimum *GBW* or *SR* 595
6-8-2 Compensation of Positive Zero 598
6-8-3 Fully Differential or Balanced OTAs 601
6-9 Op Amp Examples 607
6-9-1 CMOS op Amp Configurations 607
6-9-2 Bipolar Op Amp Configurations 608
6-9-3 BIMOS and BIFET Op Amp Configurations 610
Summary 612
Exercises 612
Appendix 6-1: Pole-Zero Doublets and Settling Time 622
Appendix 6-2: Amplifier Configurations 628
References 646

7 Fundamentals of Continuous-Time and Sampled-Data Active Filters 648
Introduction 648
7-1 Linear Filtering Concepts and Definitions 649
7-2 Schemes for Integrated Analog Filters 652
7-2-1 Active-RC and Active G_m/C Filters 652
7-2-2 Active-SC Filters 657
7-3 Filter Types and Frequency Response Specifications 666
7-3-1 Lowpass 668
7-3-2 Highpass 670
7-3-3 Bandpass 671
7-3-4 Band-Reject 672
7-3-5 Allpass or Delay Equalizer 672
7-3-6 Basic Filter Specifications 675
7-4 Determining a Nominal H 678
7-4-1 Maximally-Flat or Butterworth Filters 679
7-4-2 Equi-Ripple (Chebyshev) Filters 681
7-4-3 Cauer (Elliptic) Filters 684
7-4-4 Bessel (Linear Phase) Filters 685
7-5 Frequency Transforms 686
7-5-1 s-to-s Transforms 687
7-5-2 s-to-z Transforms 688
7-6 Noise, DC Offset, Harmonic Distortion and Dynamic Range 690
7-7 Sensitivity, Variability, and Yield 696
7-8 Modeling and Analysis of Switched-Capacitor Filters 703
7-8-1 Periodic Time-Variance in Biphase *SC* Filters 704
7-8-2 ϕ^e and ϕ^o Decomposition 708
7-8-3 Switched-Capacitor z-Domain Models 713
7-8-4 Active *SC* Integrators 718
Summary 723
Exercises 724
Appendix 7-1: Sampled-Data Signals and Systems 732
References 756

8 Design and Implementation of Integrated Active Filters 758

Introduction 758

8-1 Parasitic Capacitances in Integrated Filters 761

8-2 Design of Practical Integrated Filter Components 764

8-2-1 Poly 1-Poly 2 Capacitor 764

8-2-2 MOST Analog Switch 765

8-2-3 Linearized MOST Resistor 767

8-2-4 Linearized OTA Transconductance 772

8-3 Parasitics and Filter Precision 777

8-3-1 Reducing the Effect of Parasitics on Filter Precision 778

8-3-2 Parasitic Insensitive Switched-Capacitor Structures 782

8-4 Automatic On-Chip Tuning 786

8-4-1 On-Chip Tuning Strategies 787

8-4-2 Frequency Tuning with PLL 794

8-4-3 Q tuning with MLL 796

8-5 *PSRR*, Clock Feedthrough and DC Offset 798

8-5-1 Clock Feedthrough and DC Offset Cancellation 799

8-5-2 Layout Measures to Improve *PSRR* 803

8-5-3 Balanced Active-RC and SC Design 808

8-6 First-Order and Biquadratic Filter Stage Realizations 808

8-6-1 Realizing Real Poles and Zeros 809

8-6-2 Types of Biquads 815

8-7 Fleischer-Laker Active-SC Biquads 822

8-7-1 Evaluation of the General Active-SC Biquad 826

8-7-2 Synthesis of Practical Active-SC Biquads 830

8-7-3 Examples 837

8-8 Integrated Continuous-Time Fleischer-Laker Type Biquads 843

8-8-1 Active-RC Biquads using MOST-R's 843

8-8-2 Active-G_m/C Biquads using MOST-G_m's 847

8-9 High-Order Filter Implementation Using Cascaded Stages 849

8-9-1 Cascading First- and Second-Order Filter Stages 849

8-9-2 Time-Staggered Active-SC Stages 852

8-9-3 Settling Error Analysis of Delay Equalizers Realized as a Cascade of Active-SC AP Stages 856

8-10 High-Order Filter Implementation Using Active Ladders 858

8-10-1 Sensitivity 860

8-10-2 Realization Using Signal Flow Graphs 862

8-10-3 Realizing All-Pole LP Filters 865

8-10-4 Realizing Symmetric All-Pole BP Filters 870

8-10-5 Realizing Finite Transmission Zeros 872

Summary 874

Exercises 876

References 885

Index 889

Example 2-13

What is the cutoff frequency for a 1 kΩ resistor, realized in p-base diffusion with $R_R = 130\ \Omega/\square$ and $C_R = 0.2$ pF/□. Calculate the frequency at which the parasitic capacitance causes a phase shift of 10° with respect to low frequencies.

Solution. For 1 kΩ, 8 squares are needed. As a result, $f_{RC} = 15\ \text{GHz}/(L/W)^2$ or 15 GHz/64 = 230 MHz. A phase shift of 10° is reached at the frequency f_{10} where $tg(10°) = f_{10}/f_{RC}$ or at about 40 MHz.

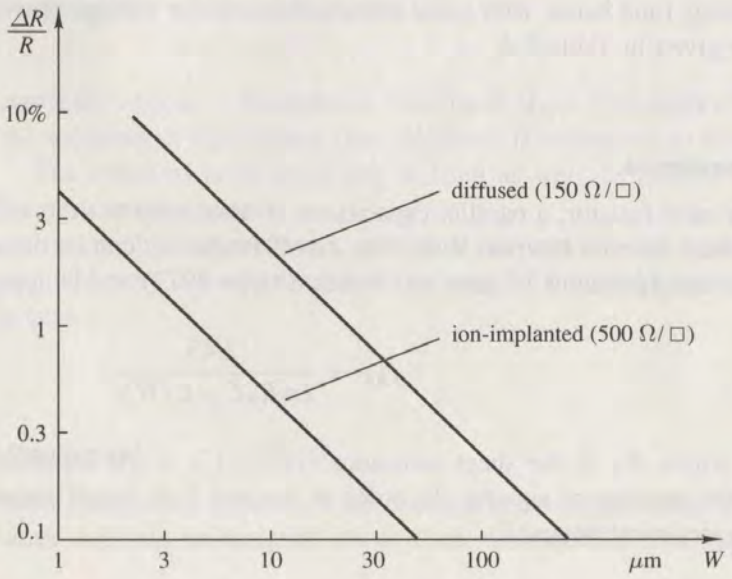
2-9-6 Absolute and Relative Accuracy

To realize a resistor with absolute accuracy is difficult, but layout tricks can be applied to reduce the uncertainties. For example, the contact and corner areas can be covered with $p+$ islands. Nevertheless, good design must never be based on absolute values. Relative values such as resistor ratios must be used. The relative errors obtained are about one-tenth of the absolute accuracies given in Table 2-6. Obviously, the larger the dimensions, the better the relative accuracy that can be achieved.

This is illustrated in Fig. 2-31 for both diffused (base diffusion: 150 Ω/□) resistors. The relative accuracy improves more or less proportionally to the resistor width. Moreover, the relative error is approximately a factor of three smaller for ion-implanted devices than for diffused ones. In order to reach a relative error of 0.1 percent, ion-implanted resistances must be taken with about 40 μm width.

Many other layout tricks (see Sec. 6-7) can be applied to improve matching.

FIGURE 2-31 Matching of resistors with width W.



2-9-7 Resistors in a CMOS Process

In a conventional n-well CMOS process, several resistances are available. They are the source/drain resistance, the polysilicon gate and the n-well region. However, none of these are intended to be used as a resistor. The control on the accuracy of the resistivity is very poor (see Table 2-6). An analog CMOS process quite often includes an additional polysilicon resistor with excellent properties. Its temperature and voltage coefficient are then low as well.

2-9-8 Thin Film Resistors

On top of a chip, a thin-film resistor can be easily deposited. Actually, the aluminium metallization layer is such a resistor, albeit with very low resistivity. A higher resistivity is obtained with NiCr or Ta, which yield values from 100 to 4 k $\Omega/\square$. The control on its resistivity is excellent and so are its temperature and voltage coefficient. This is why they are used for very high precision circuits and for circuits at very high frequencies.

2-9-9 Capacitors

In a bipolar process, junction capacitance is available at each junction. The most useful is the collector-base junction capacitance (see Table 2-7), shown in Fig. 2-32. It is not very accurate, however, and it is very voltage dependent (see Table 1-5). This applies to all other junction capacitances as well.

Note that the capacitance on the bottom side is always connected by a parasitic capacitance C_p to the substrate. This capacitance is always a fixed fraction of the useful capacitance and cannot be avoided.

Much more accuracy can be obtained with a MOS capacitance in a CMOS process (see Fig. 2-33). Not only is its value larger, but its accuracy is much higher, especially for the poly-to-poly capacitance. Also, the temperature and voltage coefficients are quasi-nihil. Its parasitic capacitance from the bottom plate to ground is decreased to

TABLE 2-7 CAPACITORS

Process	Type	C nF/cm^2	absolute accuracy percent	temperature coefficient percent/°C	voltage coefficient percent V	breakdown voltage V
Bipolar	C_{CB}	16	10	0.02	2	50
	C_{EB}	50	10	0.02	1	7
	C_{CS}	8	20	0.01	0.5	60
CMOS	C_{ox}(50 nm)	70	5	0.002	0.005	40
	$C_{m,poly}$	12	10	0.002	0.005	40
	$C_{poly,poly}$	56	2	0.002	0.005	40
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20
	$C_{m,substrate}$	5.2	10	0.01	0.05	20
	$C_{poly,substrate}$	6.5	10	0.01	0.05	20

Many of the parasitic C's, namely, C_{GS}, C_{GD}, C_{jD}, and C_{jS}, are associated with the MOST model described in Chap. 1. The expressions for each, in the three MOST operating regions, are summarized in Table 8-1. Source and drain-to-bulk capacitances C_{jS} and C_{jD} are voltage dependent and consequently enhance nonlinear distortion. The relations for voltage dependent C_{jSB} and C_{jDB} can be found in Table 1-5. All the MOST parasitics scale in direct proportion with the geometric dimensions of the MOST (i.e., W, L_{eff}, L_D, A_S, A_D defined in Chap. 1). Hence, their values are only within the control of the designer insofar as the need to keep the MOSTs as small as a prudent electrical design permits. Recall that the amount of C_{oxt}, the gate-to-channel capacitance, in C_{GS} and C_{GD}, varies with the operating region and $C_{oxt} = C_{ox} W L_{\text{eff}} \gg C_{GS0}, C_{GD0}$.

Parasitic C_R represents the accumulated capacitance formed by the metal interconnect level, i.e., metal-to-substrate over field oxide. It is determined by C_{oxm}, defined in Table 1-7, and the dimensions of the route $L_R \times W_R$. C_R's are very much within the control of the designer, and they can be minimized (at least the critical ones) in a well planned layout. Parasitic C_B is formed by the Poly 1 bottom plate associated with C_A, and the field oxide and substrate. C_B scales directly with the dimensions of the poly 1 bottom plate $L_B \times W_B$, that underlies the entire C_A structure (recall Fig. 7-4*d*). It also depends on C_{oxp}, the capacitance associated with poly 1-to-substrate over field oxide. Hence, the value of C_B is not usually within designer control and will always be a fixed percentage of C_A. The relations for parasitics C_R and C_B are also listed in Table 8-1.

Example 8-1

With $C_{oxp} = 6.5$ nF/cm^2, calculate the bottom-plate parasitic capacitances C_{B1} and C_{B2} for the double-poly capacitors C_1 and C_2 in Fig. 8-5 (*see color plate 1*).

Solution. From the dimensions, the areas for the bottom plates of C_1 and C_2 are, respectively, $A_1 = 778\ \mu\text{m}^2 = 778 \times 10^{-8}$ cm^2 and $A_2 = 7264\ \mu\text{m}^2 = 7264 \times 10^{-8}$ cm^2. Thus, $C_{B1} = C_{oxp} A_1 = 0.05$ pF and $C_{B2} = C_{oxp} A_2 = 0.47$ pF.

TABLE 8-1 PARASITIC CAPACITANCES (WHERE $C_{oxT} = C_{ox} W L_{\text{eff}}$ AS PER TABLE 1-5)

	Region		
	Cutoff	Triode	Saturation
C_{GS}	$C_{GS0} = C_{ox} W L_D$	$C_{GS0} + \frac{1}{2} C_{oxt}$	$C_{ox} W L_D + \frac{2}{3} C_{oxt}$
C_{GD}	$C_{GD0} = C_{ox} W L_D$	$C_{GD0} + \frac{1}{2} C_{oxt}$	C_{GD0}
C_{jS}	$\approx C_{jSB} A_S$	$\approx C_{jSB} A_S + \frac{1}{2} C_{BC}$	$\approx C_{jSB} A_S + \frac{2}{3} C_{BC}$
C_{jD}	$\approx C_{jDB} A_D$	$\approx C_{jDB} A_D + \frac{1}{2} C_{BC}$	$\approx C_{jDB} A_D$
C_R		$C_{oxm} W_R L_R$	
C_B		$C_{oxp} W_B L_B$	

APPENDIX CHO01

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APPENDIX CHO02

TP 13.5 A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones

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Level One Communications, Inc., San Francisco, CA

A high level of integration is critical in lowering the cost of electronics for communication systems such as cellular phones, cordless phones, and wireless LANs. A number of recent papers report increasing levels of transceiver integration. RF, baseband analog, and mixed-signal circuits have been integrated [1]. RF, baseband analog, and voltage-controlled oscillator (VCO) circuits have been realized on a single die [2].

This fully-integrated transceiver incorporates RF circuits, synthesizer, baseband filters, demodulator, and digital signal processing (Figure 13.5.1). The few off-chip components include an ISM band filter, a balun, an RF matching network, an RC loop filter for the PLL, a crystal resonator, and a resistor for biasing. A transmit/receive (T/R) switch is avoided by sharing a single RF port between transmitter and receiver. An offset cancellation method attenuates offsets in the baseband without sacrificing bandwidth in the direct conversion receiver. Careful circuit design, timing, and layout considerations provide isolation between the sensitive RF signals and the digital switching noise. The IC is in 0.6μm CMOS and provides a complete interface between antenna and voiceband codec.

Architectural and circuit techniques make this level of integration possible without sacrificing performance. Time-division duplex (TDD) ensures isolation between transmitter and receiver. Direct conversion eliminates expensive, off-chip radio frequency (RF) image-reject filters and diplexer, and replaces off-chip intermediate frequency (IF) channel select filters with on-chip low pass filters. Active on-chip offset reduction by feedback and feedforward loops is combined with digitally-controlled automatic gain control (AGC) that settles within the 160ms preamble of the receive burst. A fully-differential analog signal path minimizes supply and substrate noise coupling. The burst-mode controller (BMC) uses CMOS logic for low power dissipation and high circuit density. To reduce coupling, CMOS logic gate transitions occur in a 5ns period after sampling instants of switched capacitor circuits. The synthesizer dividers use source-coupled logic to reduce coupling. Automatic calibration allows integration of a 1.8GHz LC VCO with a wide tuning range. The receiver has 104dB maximum gain and -104dBm sensitivity.

The low noise amplifier (LNA) and power amplifier (PA) designs make possible sharing a common RF port, eliminating the external TR switch. The LNA input transistors are not stressed by this arrangement because the fabrication technology is 5V-capable, the supply is 3.3V, and the LNA power-down mode allows the source/drain terminals to float to V_{DD}. The LNA, shown in Figure 13.5.2, is implemented as a cascade of two stages. The first stage employs a capacitively cross-coupled input pair, M1 and M2, that provides both gain and impedance matching in parallel with a differential pair, M3 and M4, for additional gain. The second stage of the LNA is also a differential pair. All gain stages are loaded by on-chip spiral inductors. The combined LNA gain can be set to 12dB or 28dB.

The PA is implemented as a three-stage, class AB amplifier. The first stage is a resistively-loaded differential pair, the second stage is a common-source stage loaded with on-chip spiral inductors, and the output stage consists of large open-drain devices whose drains are connected to the LNA input. The bias currents of the final stage are provided by off-chip RF chokes. The output power, measured at the balun, can be varied from +2dBm to +20dBm.

The mixer uses a double-balanced structure without a tail current source to increase headroom. Biasing for the RF input transistors is by a replica circuit that suppresses transconductance variations with process and temperature. The LO input transistors operate as switches that steer a process and temperature independent current. The output of the mixer is fed to a four-pole Butterworth antialias filter with 2.4MHz cut-off frequency.

Switched-capacitor I and Q baseband filters sample the output of the antialias filter at 24MHz, attenuate adjacent channels, and provide AGC. Each baseband signal path comprises a fourth-order low-pass Chebyshev filter, implemented with two biquad sections, followed by a group-delay equalizer (GDE). The biquads and the GDE have programmable gain of one or four. The filter is followed by a switched-capacitor variable-gain amplifier (VGA) that is programmable with a gain of one, two, or four. This arrangement provides a baseband gain of 0dB to 48dB in 6dB steps.

In a direct conversion receiver, LO leakage can lead to large offsets at the inputs to the baseband filters. Offsets in the switched-capacitor filter sections can accumulate and render the output signal undetectable. To overcome this, feedback integrators cancel offsets in the first biquad and in the GDE (Figure 13.5.1). To prevent baseline wander from causing errors, the integrators are placed in hold mode when data is transferred.

Switched-capacitor peak detectors sample maximum and minimum values of the filtered I and Q signals. The AGC controller uses the peak detector outputs to estimate signal levels and adjusts baseband gain. Offset information, derived from the peak detectors, is filtered and subtracted from the baseband filter output. Offset-cancelled I and Q signals are fed to a BFSK demodulator.

The BFSK demodulator is implemented with switched-capacitor circuits clocked at 6MHz. It generates a digital output based on the direction of rotation of the I/Q constellation. The digital output of the demodulator is processed by an on-chip BMC, comprising over 8000 CMOS standard-cell gates, that performs clock recovery and direct sequence spreading and despreading. The receiver bit error rate (BER), shown in Figure 13.5.3, illustrates receiver sensitivity. Selectivity and blocking are given in Table 13.5.1.

A single frequency synthesizer creates LO and PA input signals for receive and transmit, respectively. The circuit generates channels from 900MHz to 930MHz in 750kHz increments. During receive, a divide-by-two circuit creates I and Q LO signals from the output of a VCO operating at twice the desired frequency in a high-bandwidth PLL. During transmit, the PLL bandwidth is reduced, allowing filtered transmit data to directly modulate the VCO while maintaining a constant center frequency. The transmit spectrum for +20dBm output power is shown in Figure 13.5.4. The VCO, shown in Figure 13.5.5, is a cross-coupled differential pair loaded by spiral inductors and by capacitors. The load capacitors include ac-coupled channel varactors, modulation varactors, and a bank of capacitors for automatic coarse frequency adjustment.

Measured performance is summarized in Table 13.5.1. Figure 13.5.6 is a die photo.

Acknowledgements:
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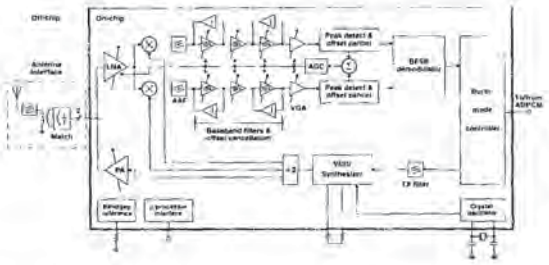


Figure 13.5.1: Transceiver architecture.

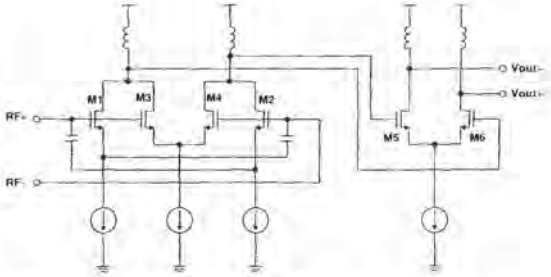


Figure 13.5.2: Low-noise amplifier circuit.

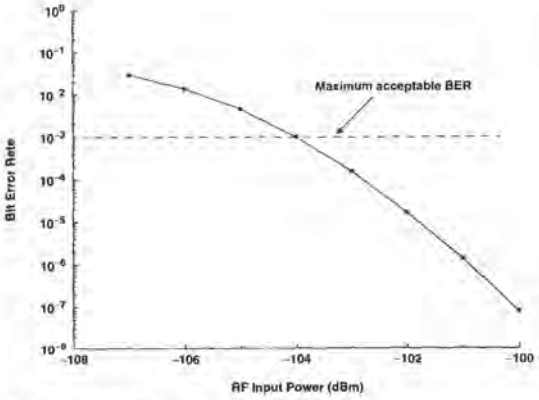


Figure 13.5.3: Measured BER vs. RSL.

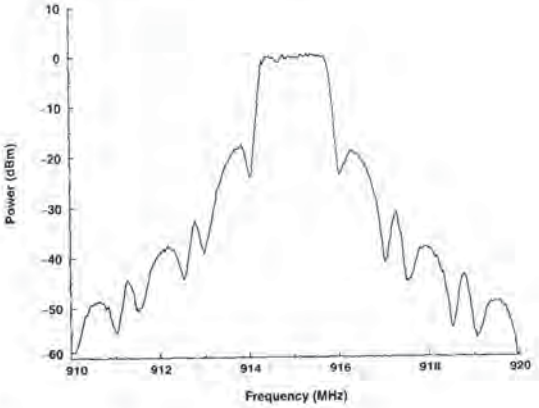


Figure 13.5.4: Measured transmit spectrum.

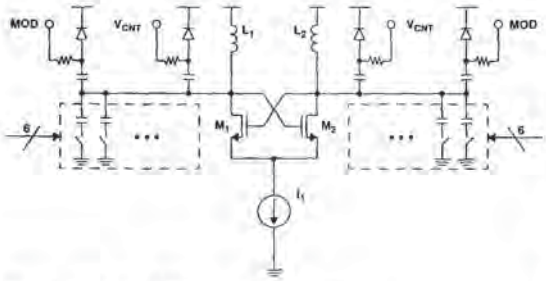


Figure 13.5.5: VCO circuit diagram

Figure 13.5.6: See page 464.

References:
[1] A. Rofougaran, et al., "A Single-Chip 900MHz Spread-Spectrum Wireless Transceiver in 1-mm CMOS - Part I: Architecture and Transmitter Design," IEEE J. of Solid-State Circuits, vol. 33, No. 4, pp. 515-534, Apr. 1998.
[2] M. Steyaert, et al., "A Single-Chip CMOS Transceiver for DCS-1800 Wireless Communications," ISSCC Digest of Technical Papers, pp. 48-49, Feb. 1998.

Receiver	
Sensitivity	-104dBm
Dynamic range	110dB
Noise figure (DSB)	4.5dB
IIP2 (high gain)	+22dBm
IIP3 (high gain)	-21dBm
Selectivity (co-channel 1.5MHz, 3MHz)	3, 23, 57dB
Blocking (4.5MHz)	67dB
Dissipation (3.3V)	525mW
Transmitter	
Output power (into 50Ω)	2, 8, 14dBm
Bandwidth	1.5MHz
Modulation accuracy	±1%
Dissipation (3.3V, 2dBm)	254mW
General	
Technology	0.6μm 2p3m CMOS
Die area	5.4x6.7mm²

Table 13.5.1: Performance summary.

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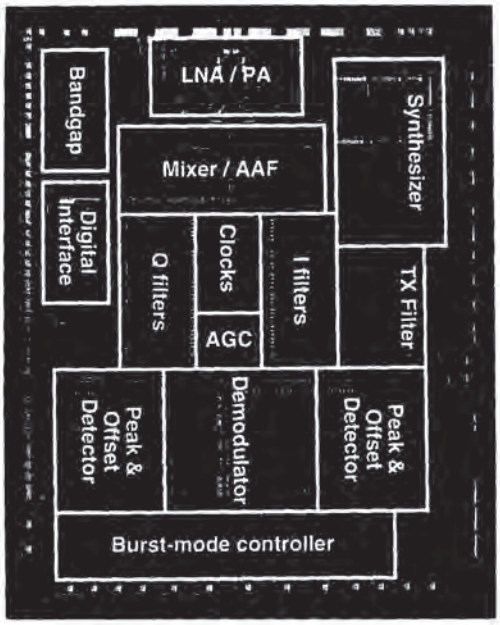


Figure 13.5.6: Die micrograph.

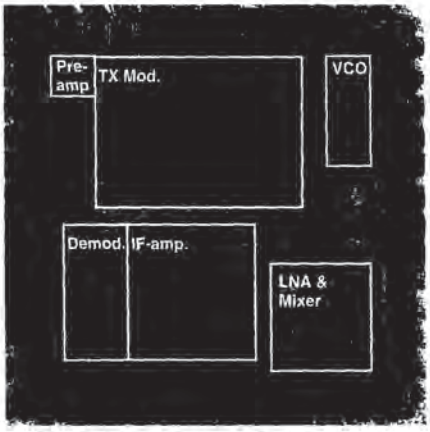


Figure 13.7.7: Die micrograph.

Complete RX (including duplexer and filters)	NF	8.1dB (SSB)
	iIP3	-4dBm
	iCP	-16dBm
	Overall gain	+101dB
	Blocking	+6dBm at 915MHz (w. c.)
LNA	Gain	+15.3dB, -3.7dB
	NF	1.9dB
Mixer	Conv. gm 8.5mS	
	NF	15.6dB (SSB)
IF-Amp	Gain	-20.9 .. +58dB (2dB steps)
	NF	3.8dB
Demodulator	Image suppr.	>43dB ($\Delta\varphi$<1°)
	Gain	16dB
Baseband Filters	Type	Bessel 4th Ord. active RC
	Cut-off freq.	150kHz
	Gain	15.7dB
Modulator	Output power	-17dBm
	LO suppr. >50dB	
	Image suppr.	>31dB
	RMS phase err.	1.6°
Pre-amp	Output power	+3dBm
	Gain	21dB
	oCP	+5.4dBm

Table 13.7.1: Measured transceiver characteristics.



Figure 14.1.7: ADSLC die micrograph.

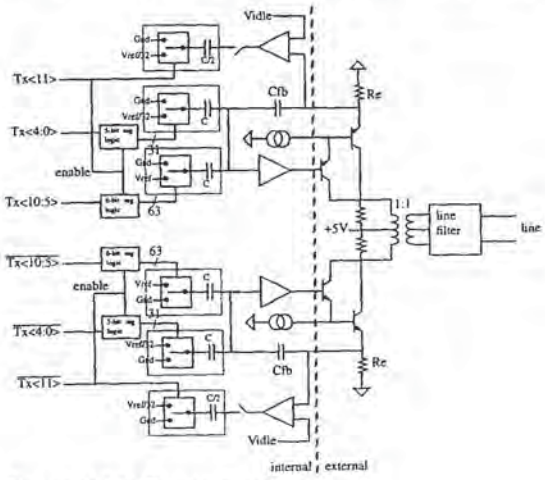


Figure 14.5.2: Transmitter.

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