

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

TEXAS INSTRUMENTS INCORPORATED,
Petitioner

v.

PARKERVISION, INC.,
Patent Owner

Case IPR2024-00934
Patent 7,496,342

THIRD DECLARATION OF DR. IAN GALTON

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I. INTRODUCTION

1. I have been retained by Fish & Richardson P.C. as an independent expert on behalf of Petitioner Texas Instruments (“TI”). I understand that this declaration (“Third Declaration”) will be submitted in support of the Petitioner Reply to Patent Owner’s Response (“POR”) to the Petition for *Inter Partes* Review of U.S. Patent No. 7,496,342 (“’342 Patent”). This Third Declaration is responsive to Dr. Rickett’s ’342 Expert Declaration, EX2021, and addresses the prior art and technology analysis that Dr. Ricketts provided in his declaration.

2. This Third Declaration supplements, and is intended to be read in conjunction with, my earlier declaration (TI-1003) in support of TI’s Petition in IPR2024-00934 and my Second Declaration that I provided to ParkerVision. I am including my Second Declaration as an attachment here (I understand that the Second Declaration is also being submitted as exhibit TI-1042).

3. In writing this Second Declaration, I have considered the following: my own knowledge and experience in electrical engineering, including in the field of RF and other mixed-signal integrated circuits; my teaching and work experience in the above fields; and my experience of working with others involved in those fields. I have also reviewed at least the materials in Section II (Materials Considered) as part of my analysis.

4. The analysis and opinions expressed in my first declarations fully

explain why each and every feature of the '342 Patent's Challenged Claims is provided in the prior art. As I previously described with reference to the applied prior art and corroborating references, the Challenged Claims 19-21 would have been obvious to a POSITA. I understand that Patent Owner has considered my opinions and offered their own, some of which are inconsistent with my view. Below, I provide further testimony in response to Patent Owner's arguments. In responding to Patent Owner's arguments, I have analyzed various publications and materials including materials cited in my First and Second '342 Declarations and additional materials in this Third Declaration. I have also considered Dr. Ricketts's commentary on the DeMaw and Macnally simulations from the First and Second Declarations, and I have considered Dr. Ricketts's own analysis and simulations. The fact that I may not have addressed all of Patent Owner arguments should not be interpreted as agreement with them.

II. MATERIALS CONSIDERED

Exhibit No.	Description
TI-1042	Second Declaration of Dr. Ian Galton
TI-1043	Razavi, <i>A 900-MHz CMOS Direct Conversion Receiver</i> , IEEE Symposium on VLSI Circuits, Kyoto, Japan, 1997, pp. 113-114, doi: 10.1109/VLSIC.1997.623833 ("Razavi")
TI-1044	E. Oxner, Siliconix Application Note AN72-1 "FETs in Balanced Mixers," 1979. ("Oxner")

TI-1045	B. Gilbert, "The MICROMIXER: a highly linear variant of the Gilbert mixer using a bisymmetric Class-AB input stage," in IEEE Journal of Solid-State Circuits, vol. 32, no. 9, Sept. 1997
TI-1046	I. Galton and C. Weltin-Wu, "Understanding Phase Error and Jitter: Definitions, Implications, Simulations, and Measurement," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 1, Jan. 2019
TI-1047	D. E. JOHNSON, J. L. HILBURN, AND J. R. JOHNSON, BASIC ELECTRIC CIRCUIT ANALYSIS, 7th Edition, Prentice-Hall, 1978
TI-1048	ADEL S. SEDRA, KENNETH C. SMITH, MICROELECTRONICS CIRCUITS, 4TH EDITION, Oxford University Press, 1997
TI-1049	K. R. LAKER, W. M. C. SANSEN, DESIGN OF ANALOG INTEGRATED CIRCUITS AND SYSTEMS, McGraw-Hill, Inc., 1994
TI-1050	Cho, E. Dukatz, M. Mack, D. MacNally, M. Marringa, S. Mehta, C. Nilson, L. Plouvier, S. Rabi, "A Single-Chip CMOS Direct-Conversion Transceiver for 900MHz Spread-Spectrum Digital Cordless Phones," IEEE International Solid-State Circuits Conference, Technical Digest, pp. 228-229, 464, February, 1999
TI-1051	Deposition Transcript of Dr. David Ricketts, June 25, 2025

III. DeMaw

5. ParkerVision's characterization of the original simulations containing "material mistakes" is simply wrong. In fact, the simulations contained no material mistakes. What ParkerVision characterizes as material mistakes are merely design choices that, when changed, do not affect the intended operation of

the circuit to down-convert an EM signal by charging and discharging capacitors. I ran new simulations entirely in response to allegations by ParkerVision that I “cherry-picked self-serving values.” POPR, 11. I ran new simulations using several different sets of parameters in an attempt to quiet ParkerVision’s allegations of cherry-picking (as well as their questioning of my integrity in these proceedings). I also provided ParkerVision all of the simulation models and data, none of which ParkerVision has provided to the Board. But as shown in the new simulations and as I explain in my second declaration, the new simulations show that the DeMaw circuit performs all of the method steps of claims 18-21, even when using different circuit and operating parameters. That the circuit functions as intended using different circuit and operational parameters is a feature of the circuit, and not a failing of the simulations. But to be clear, the circuit simulations in my original declaration (and in the Petition) show that DeMaw renders claims 18-21 unpatentable.

A. Original DeMaw Simulations Show the Claimed Circuit Behavior

6. The original DeMaw simulations accurately represent the operation of the DeMaw circuit—and the unpatentability of claims 18-21—even with the generic JFET model.

7. First, that I used a generic JFET model in my original simulations is not a material mistake that rendered the original simulations invalid or unreliable.

Quite the contrary. The totality of the simulations show that the DeMaw circuit is robust enough to operate correctly independent of the type of JFET used.

8. Second, the JFET type shown in DeMaw (Siliconix U430) is not a requirement for the circuit to function. Indeed, the Oxner reference, from where DeMaw derives its circuit, provides many examples of JFETs that would also work, as shown below:

Best mixer performance is achieved with “matched pairs” of JFETs. Basic considerations in selecting FETs for this application are gate cutoff voltage, $V_{GS(off)}$, for good conversion transconductance, and zero-bias saturation current, I_{DSS} , for dynamic range. A match to 10% is generally adequate. Among currently available devices, the Siliconix U310 and the dual U431 offer excellent performance in both categories; common-gate forward transconductance is 20,000 μ mhos max at $V_{DS} = 10$ V, $I_D = 10$ mA, and $f = 1$ kHz.

There is, of course, the possibility that FET cost is a major consideration in evaluating the active balanced mixer approach — the familiar price/performance tradeoff. If this is the case, there are a number of other Siliconix FETs which will provide suitable alternatives to the U310. Remember,

however, that conversion transconductance, g_c , can never be more than 25% of forward transconductance. Thus as tradeoff considerations begin, the first sacrifice to be made will be the degree of achievable conversion gain. Intermodulation performance will follow with the third tradeoff being available noise figure. Table III lists a number of possible alternatives to the U310.

Table III

Typical Characteristic	DEVICE TYPE			
	U310*	2N5912	2N4416*	2N3823
g_m	14K	6K	5K	3.5K
I_{DSS}	40 mA	15 mA	10 mA	10 mA

*Similar devices are also available in plastic packages:

U310 (J310)
2N5397 (K300-18)
2N4416 (2N5486, K304-18)

using any set of matched pairs from the several JFETs listed above supports my conclusion that my original DeMaw circuit simulations using the generic JFET accurately represent the functioning of the DeMaw circuit, and that such operation renders claims 18-21 unpatentable. The generic JFET models are representative of typical JFETs, and they do not exhibit extraordinary characteristics that would materially skew the results of the simulation with respect to the conclusions I have reached in this document. Oxner's options box of JFETs also tells us that the DeMaw circuit is robust enough to operate as intended independent of the specific types of JFETs used. That robustness is also shown by the original and supplemental simulations, where the DeMaw circuit down-converts an RF signal by charging and discharging the respective capacitors using generic JFETs and using the U430 JFETs, both achieving the claimed discharge percentages.

9. Dr. Ricketts criticized the fact that I provided a simulation based on Oxner's component values rather than DeMaw's when I previously said they were different circuits. EX2021, ¶335. The Oxner circuit is presented in full detail in the AN72-1 Application Note (TI-1044), and is referenced in the DeMaw textbook (so a POSITA would have had access to it as early as 1982, the publication date of the DeMaw textbook). As explained in the DeMaw textbook, the circuit of Fig. 6.7 "is similar to a circuit suggested by E. Oxner of Siliconix in Application Note AN72-1." TI-1016, 8. I chose to include it in the set of simulations I provided because

the AN72-1 Application Note provides far more implementation details than the DeMaw textbook provides for the circuit of Fig. 6.7. TI-1042, ¶83. My goal was to avoid further criticism by Dr. Ricketts that I was choosing component values and/or operating conditions simply to get the results he thinks I wanted.

10. Dr. Ricketts further complained that I introduced modifications for certain parameters in Section V of my second declaration where I modified the DeMaw Circuit to match Oxner. EX2021, ¶337. Of course there are modifications, precisely because I used the exact component values specified in the AN72-1 Application Note. TI-1042, ¶83; TI-1044, 6-31. Had I done otherwise, Dr. Ricketts would most likely have criticized me for not adhering to the values specified in the AN72-1 Application Note!

11. It is true that my intention was to use Siliconix U430 JFET models instead of the generic LTSpice JFET models, but the use of different JFETs than those shown in the example design in the DeMaw textbook certainly does not render the results invalid (i.e., this was not a material mistake). *See* EX2021, ¶235. The field is called “circuit design,” not “circuit cut-and-paste.” Exact component values and specific component brand name and model numbers are rarely specified in the circuit diagrams or their explanations in circuit textbooks, patents, and papers, so a POSITA understands that even when a circuit diagram is specified, it is usually necessary to go through the design process of choosing component

values. Indeed, Oxner's application note has an entire section dedicated the various tradeoffs and design considerations for selecting the JFETs for its balanced mixer. TI-1044, 6-33.

12. To be clear, I stand by the original simulations. A POSITA implementing DeMaw's circuit would have started with an initial design (such as the design shown in DeMaw FIG. 6.7), but would likely have improved upon it through routine optimization, including trying different JFETs. This sort of routine optimization was discussed at length in Oxner's application note. TI-1041, 6-33 ("How to Select a Proper FET"). The idea that there was a "correct" JFET is misleading. While it is true that I made a mistake by using generic JFET models in original simulations, that I used the generic JFET model does not render the simulation unreliable or invalid. Quite the opposite: it shows that DeMaw would still render claims 18-21 unpatentable even using generic circuit components.

13. There is no requirement that DeMaw be implemented using a U430 JFET. Because Oxner contemplates using any set of matched pairs from the several JFETs listed above, a POSITA implementing DeMaw would have undergone routine optimization to select the JFET type (and other circuit component values) when implementing the circuit to achieve optimum or workable ranges for the circuit's performance in the particular target application of interest, including the claimed discharge percentages. In fact, the '342 patent states that the capacitors

(not the JFETs) are sized to achieve the claimed discharge percentages. TI-1001, 50:4-25. The discharge rates are related to the down-converted signal. TI-1001, 20:1-11. A POSITA would have understood that such “sizing” would include routine experimentation and analysis to select the correct circuit component values to achieve the correct discharge percentages for the desired down-converted signal magnitude (i.e., to increase signal strength or signal-to-noise ratio).

14. If no U430 model had been available for LTSpice, I would have been required to pick a different JFET model, and the generic JFET models are representative of the performance of common JFETs. Thus, they do not exhibit extraordinary characteristics that might skew the results of the simulation. If anything, inadvertently using the generic JFET model shows the robustness of DeMaw’s circuit to perform RF down-conversion, and to perform the method of claims 18-21, without forcing the circuit to meet my inadvertent use of the generic JFET model in his simulation.

15. Also, I should point out that the switching device in the original simulations is still a JFET. If DeMaw had not provided a specific brand name and model number for the JFET, a POSITA implementing DeMaw would have had to perform the routine optimization to determine which JFET to use. Not only that, but DeMaw recognizes that the U430 itself has a range of valid operational parameters. A POSITA implementing DeMaw would have also performed routine

optimization to determine the best operational parameters, which may have deviated from DeMaw's suggestions when implemented.

16. The only reason Dr. Ricketts is able to criticize our use of the generic LTSpice models is that the DeMaw textbook happened to mention a specific brand name and model number of the JFETs. *See* EX2021, ¶231. Were this not the case, Dr. Ricketts would have had no grounds on which to complain about our use of the generic LTSpice JFET models (they are "generic" because they model common JFETs). The process used to design the simulated circuits is exactly what a POSITA would have done if the JFETs available to the POSITA for the project had the properties of the generic LTSpice JFET models. In any case, the use of different JFETs than those mentioned in the DeMaw textbook did not materially change how the circuit functions with respect to the alleged invention presented in the '342 patent or its underlying principle of operation as is supported by the subsequent simulation results I provided to ParkerVision in my supplementary declaration. I note that ParkerVision has not provided the second declaration to the Board, so I am including it and the supporting simulation materials with this declaration.

17. Another thing to note is that I volunteered the information to ParkerVision during my deposition that I had inadvertently used the generic LTSpice JFET models. EX2034, 44:6–20, 24:21–25:2. Dr. Ricketts implies that a

POSITA would have noticed this from the LTSpice schematics, but 1) I did not notice it myself until I was reviewing my expert declaration in preparation for the deposition, and 2) it is not mentioned in ParkerVision's POPR, so presumably it was not obvious to Dr. Ricketts prior to my deposition. EX2021, ¶230-232.

Instead, ParkerVision's POPR pointed to other minor design differences to assert that "TI/Dr. Galton simply chose values and a waveform to get to the result that they needed." This is certainly not the case, as my subsequent set of simulations prove. Ironically, the fact that using what Dr. Ricketts claims is an "incorrect JFET model [that] materially affects transistor behavior" does not actually lead to different conclusions about the circuit's behavior is additional evidence that it is not the case that I "simply chose values and a waveform to get to the result that [I] needed." *See* EX2021, ¶233.

B. JFET Switching Behavior

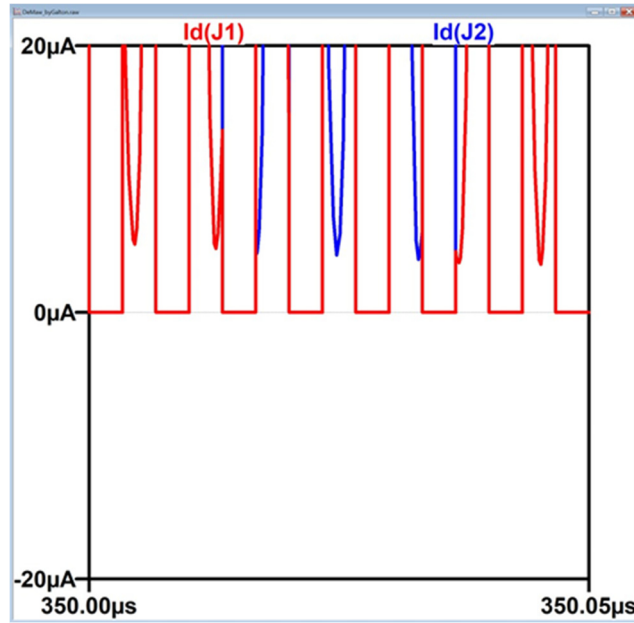
18. Dr. Ricketts uses a construction for the term "switching device" to mean "an electronic device for opening and closing a circuit." EX2021, ¶180. Dr. Ricketts also states that a JFET is an example of a switching device. EX2021, ¶53; *see also* TI-1001, cl.9 (claiming a JFET as a switching device). While I am not offering an opinion on Dr. Ricketts's construction of "switching device," I do agree that a JFET is an example of circuit element that can be used as a switching device. I also agree with Dr. Ricketts that the JFET's $V_{gs}(\text{off})$ establishes the

lowest drain current, which can be non-zero. TI-1051, 17:5-12. I also agree with Dr. Ricketts that JFETs exhibit leakage current. TI-1051, 16:7-24.

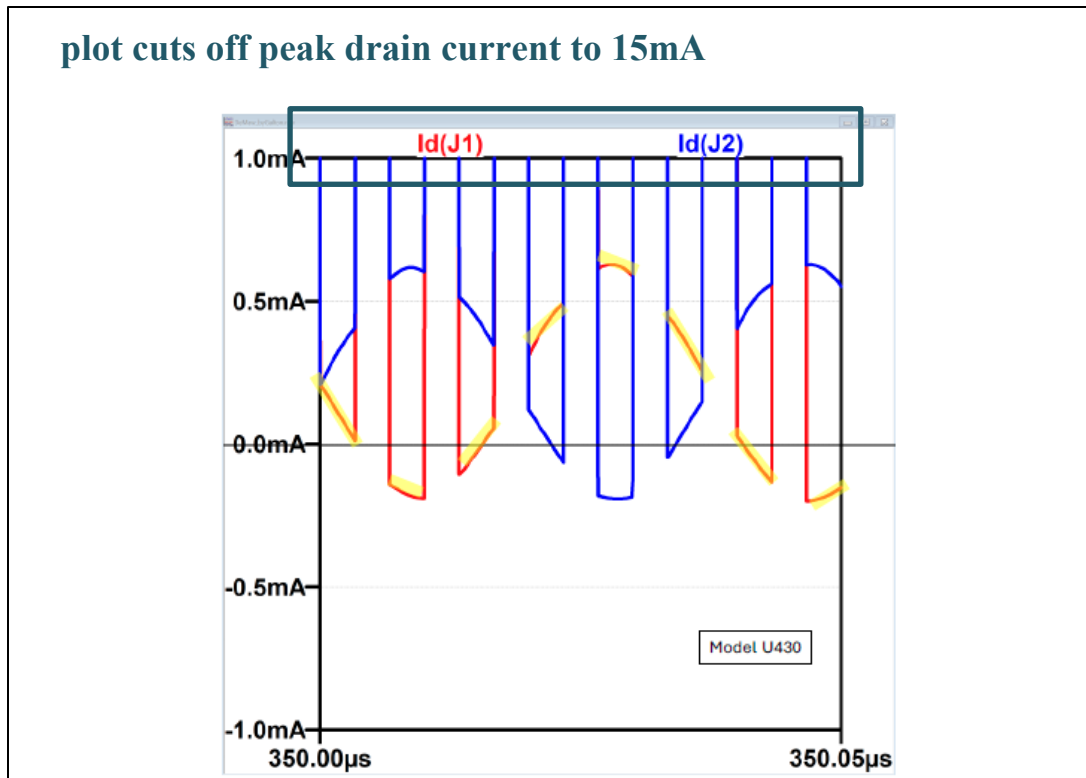
19. There is no such thing as a perfect switch in any practical circuit. All physically implementable transistor switches have a non-zero on-resistance and a non-infinite off-resistance, and all have parasitic capacitance which bypasses the switch regardless of whether the switch is off or on (thereby providing a signal path around the switch even when it is off). Hence, if Dr. Ricketts' position is that the '342 patent applies only to circuits with ideal switches, then the "ideal" operation of the DeMaw circuit would still render claims 18-21 unpatentable. See EX2021, ¶202. However, this seems unlikely to be his position as it would imply that no practical circuit would ever satisfy the requirements of Claims 18-21, i.e., it would not be possible to design a practical circuit that infringes on the '342 patent. The '342 patent contemplates JFETs as "switching devices." *E.g.*, '342 patent, cl.9. Additionally, AN72-1, which describes the Oxner circuit upon which the DeMaw circuit is based, refers to the JFETs as implementing switches. Nevertheless, electrical engineers still refer to a switch as being "off" or "on" even though it is understood that no switch perfectly turns off or on.

20. No switch is ideal, so no matter what type of transistor is used to implement a switch, the switch will conduct some current when the switch is "off". For example, had Dr. Ricketts zoomed in further on the left simulation plot below,

current flow would have been visible even when the switch is in its off state.



Dr. Ricketts' recreation of Dr. Galton's drain current waveform using an NJF-based simulation (EX2021, ¶261)

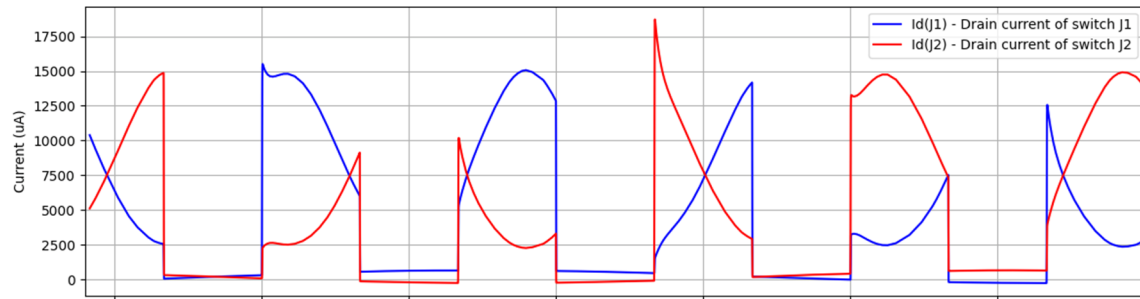


Dr. Ricketts' recreation of Dr. Galton's revised drain current waveform using U430 model (EX2021, ¶261)

21. Dr. Ricketts provided the above plots comparing the drain currents from the generic JFET and U430 simulations. EX2021, ¶261. These plots are misleading because Dr. Ricketts never shows that the closed-state current has an amplitude significantly larger than the open-state amplitude. As shown by the full plot (Dr. Ricketts did not provide his data for this plot, so I have provided my own version of it), which I explain in more detail below, the JFETs conduct far more current when closed than when open.

22. I have provided Dr. Ricketts with revised simulation results as well as all the files I used to generate those results, and one set of these simulation results

was the DeMaw simulation that Dr. Ricketts claims to have run himself and used to generate the bottom simulation plot above. The corresponding plot from the simulation that I provided is:

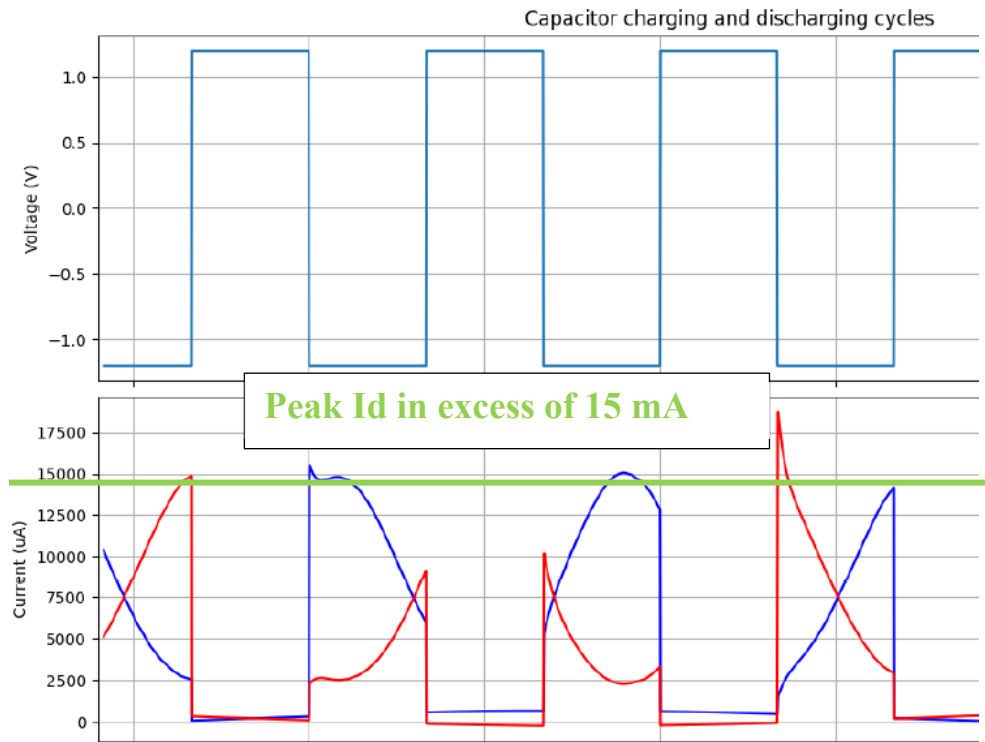


Dr. Galton's plot of the drain current waveform using U430 model

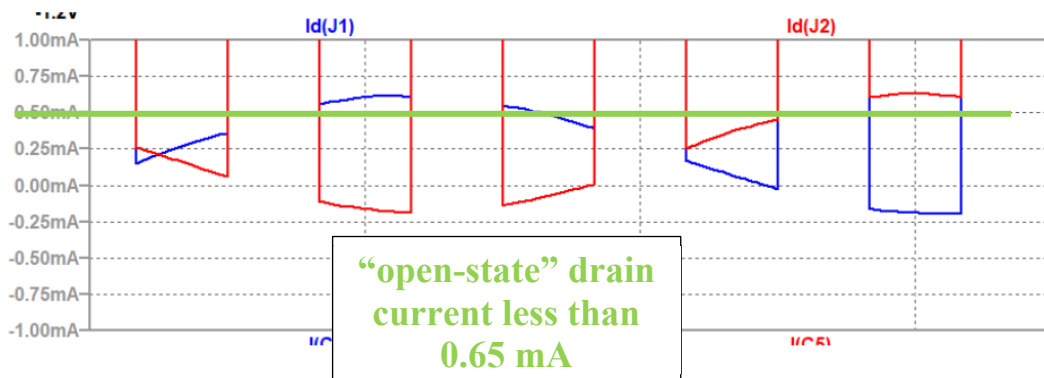
23. This plot looks quite different from the plot above that Dr. Ricketts claims is from the same simulation. As Dr. Ricketts did not provide his simulation files to us, I have no way to determine what mistake he made. Furthermore, he did not identify any issue with my version of the simulation result that would explain the difference. Therefore, in the following I will refer to the plot shown above from my version of the simulation.

24. As can be seen from my simulation plot above, Dr. Ricketts is correct in his observation that some current flows through the JFETs even when they are “effectively” turned off. Dr. Ricketts’ plot cuts off the regions of the waveforms where the JFETs are on, so his plot does not make it clear that the JFETs conduct far more current when on than when off even in his simulation. In fact, the difference between the peak drain current when the switches are closed and when

they are open is significant, being greater than 15mA, and Dr. Ricketts showed that the open-state drain current is under 0.65mA.



TI-1042, DEMA-W-SIM-FIG. 5 (revised) (annotated)



EX2021, ¶285 (annotated)

25. The drain current dropping from a peak value of over 15mA to less

than 0.65mA (a factor of over 20) illustrates that the switches “effectively” turn off, as Dr. Ricketts puts it. EX2021, ¶201. These simulations likewise show a significant drop in drain current for the open-state of the switching devices.

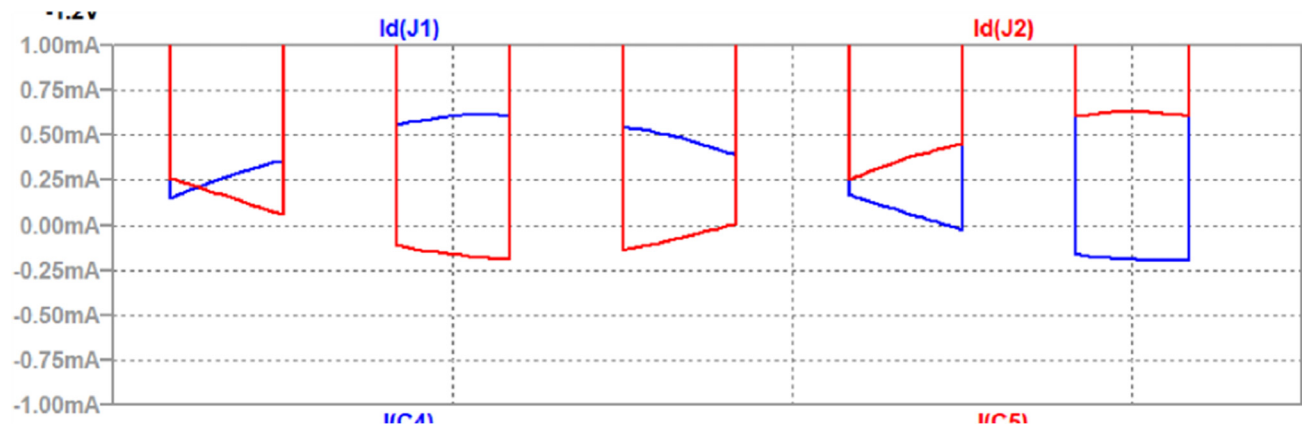
26. Nevertheless, the point is that the JFETs are acting as switches, just not ideal switches.¹ And as I mentioned above, ideal switches do not exist in practice.

27. In the case of the DeMaw circuit, as can be seen from the numerous simulation plots in my declarations (including the original declaration), the JFETs are substantially conductive when on, and significantly restrict current flow when they are off. Therefore, they do act like switches, albeit imperfect switches. This is why Oxner refers to them as switches!

28. No practical switches, e.g., those implemented by transistors (MOS transistors, JFET transistors, bipolar junction transistors, etc.) are ideal. All conduct some current when off, but they conduct far more current when on. The difference between the generic JFETs and the Siliconix U430 JFETs is that the former conduct less current when off (and when on) than the latter. Even the

¹ Oxner also refers to the JFETs as switches. Oxner states that “the JFET mixer acts as a switch, with the local oscillator acting as a switch drive signal.” TI-1044, 6-30.

generic JFETs conduct some current when off, but the amount is just not visible at the level to which Dr. Ricketts zoomed in to his plot:



Dr. Ricketts' drain current plot for a U430-based simulation zoomed in at the 0axis region

29. Even though practical switches are not perfect open circuits when off and are not perfect conductors when on, circuit designers still refer to them as switches and still describe them as “off” when they are in their low-conduction state and “on” when they are in their high-conduction state.

30. In the case of DeMaw, even the Siliconix U430 JFETs conduct far more current when “on” than when “off” so they are indeed acting as switches, just not ideal switches. It is this switching behavior that the DeMaw circuit relies upon to perform down-conversion. For example, as Dr. Ricketts mentioned, the switching operation of the default JFETs inadvertently used in our original simulations of the DeMaw circuit is closer to ideal switching than that of the Siliconix U430 JFETs suggested in the DeMaw textbook, yet the original simulations show excellent down-conversion performance.

31. Moreover, if the JFETs in the DeMaw circuit were replaced by ideal switches, the circuit would work at least as well as the original DeMaw circuit. For example, the switching operation of the default JFETs used in our original simulations of the DeMaw circuit is closer to ideal switching than that of the Siliconix U430 JFETs suggested in the DeMaw textbook, and those simulations show excellent down-conversion performance. In short, it is this switching operation of the JFETs which the DeMaw circuit relies upon to perform down-conversion, Dr. Ricketts' argument to the contrary notwithstanding.

32. In addition, Dr. Ricketts himself states that JFETs can be characterized by a $V_{gs(off)}$ voltage that allows a JFET to conduct a non-zero amount of drain current.

```
5      Q.  What is  $V_{gs(off)}$ ?  
6          What does that mean?  
7      A.  So we're describing here the pinch-off voltage.  
8      And so, my understanding is  $V_{gs(off)}$  would be the state  
9      of the FET when it has its lowest current, which, here in  
10     DeMaw, they may consider to be off. But you have to look  
11     at the specific transistor. But that's the region that  
12     they're, I think, referring to with that  $V_{gs}$ .
```

TI-1051, 17:5-12.

Without opining on the veracity of Dr. Ricketts testimony, his statement suggests that even he recognizes 1) the distinction between ideal and real-world JFET

switching behavior; and 2) that what a POSITA considers to be the “OFF” state of a JFET can be a state that involves non-zero drain current.

C. DeMaw’s Signal and Local Oscillator

33. Dr. Ricketts criticized my model of the LO signal as a square wave because DeMaw states that “ $LO = f_o$, signal frequency = f_s ,” which Dr. Ricketts concludes indicates a “single frequency” component which sinusoidal signals have and square waves do not. EX2021, ¶241. However, this is nonsense. Electrical engineers always refer to the frequency of a periodic signal as a single number, regardless of whether the periodic signal is a sinusoid or square wave, or has any other shape. In such cases, the frequency is defined as the reciprocal of the period of the periodic signal. Even the ’342 patent uses the term “frequency” in this fashion. As one of many examples, it mentions “The frequency of the pulses 508 is determined by the frequency of the input signal” (Column, Lines 41-42), where 508 is a periodic sequence of pulses. As another of many examples, it states that “... the frequency of the control signal 306 would be calculated as follows: $(Freq_{input} - Freq_{IF})/2 = Freq_{control}$ ” (Column 9, Lines 13-15), where said control signal 306 is periodic, but is not sinusoidal. A POSITA would have understood f_0 represents the fundamental frequency of a signal that includes multiple harmonics of the fundamental frequency. In fact, even Dr. Ricketts agrees that a square wave can be characterized by its fundamental frequency. EX2021, at ¶78; TI-1051, 28:3-

16. Likewise, the '342 patent states that even harmonically rich signals, including square waves, have a fundamental frequency. E.g., TI-1001, 13:20-32.

34. Dr. Ricketts further criticizes my use of a square wave by stating it introduced high-frequency components that were not present in DeMaw and force artificial switching behavior and distort the operation's mixer, rendering my simulation unreliable. EX2021, ¶242. This is not correct, but as Dr. Ricketts has not presented any basis for his conclusion that the use of square wave local oscillator signals would render the simulation “unreliable”, it is not possible for me to identify the specific flaw in his reasoning. Furthermore, Dr. Ricketts has not presented any simulations of his own that demonstrate how or why the use of a square wave local oscillator signal would lead to “unreliable” simulation results. In contrast, I presented numerous simulations with both square wave and sinusoidal local oscillator signals that reliably demonstrate that the DeMaw circuit satisfies the requirements of Claims 18-21 of the '342 patent regardless of whether the local oscillator signal is a sinusoid or a square wave.

35. Dr. Ricketts also criticizes my use of a 2019 paper to justify using the “squared-up” LO signals because it “does not show the state-of-the-art knowledge at the time of the '342 patent.” EX2021, ¶239. However, the 2019 paper to which Dr. Ricketts referred is a peer-reviewed tutorial review paper published in a top-tier IEEE journal. It is an “invited paper”, meaning that the editor of the journal

requested that I write it to provide a learning aid to the community of circuit designers. Therefore, it does not contain any “new” results. This is one reason why so many of the references it cites predate the priority date of the ’342 patent.

36. Furthermore, Dr. Ricketts’ whole discussion of sinusoidal versus square wave local oscillator signals is irrelevant because I also provided numerous simulations of the DeMaw circuit with sinusoidal local oscillator signals that reliably demonstrate that the DeMaw circuit with such local oscillator signals still satisfies the requirements of Claims 18-21 of the ’342 patent. TI-1042, §§IV, VI.

37. Dr. Ricketts criticized my interpretation of the “switch open period” as the entire LO high interval by stating that this interpretation inflates the time interval over which voltage is measured, overstates the duration of discharge, and distorts the computed discharge percentage. EX2021, ¶¶436-440. Yet, Dr. Ricketts has not provided any indication of what he considers to be an appropriate “switch open period,” so it is not possible for me to change my post-processing equations to use his preferred interval time. However, as I show in Section III.C.3 (DeMaw Discharges the Claimed Discharge Percentages), the DeMaw discharge percent histograms are non-zero up to at least 200%, so one could easily halve the “switch open period” without missing the claimed percentage regions.

38. The ’342 patent also supports my interpretation of the “switch open period.” The ’342 patent claims discharging when the switches are “open,” not

“off,” and characterizes “open” based on when the control signal is “between apertures.” TI-1001, cl. 19, 38:4-15 (describing that “one or more capacitors are sized to discharge between six percent to about fifty percent of the total charge store therein during a period of time that a switching device is open (**i.e., between apertures**)” (emphasis added)). A POSITA would recognize that the control signal being “between apertures” does not automatically imply an “off” state of the JFET, contrary to what Dr. Ricketts argues. *See, e.g.*, EX2021, ¶117. All of my simulations show that the claimed discharging occurs during the period “between the apertures,” which demonstrates performance of the claims by DeMaw’s circuit, regardless of the JFET model used. TI-1003, ¶114; TI-1042, ¶¶16-144.

1. Operating Frequencies

39. Dr. Ricketts criticized my simulation for using an RF signal at 123.102 MHz and an LO at 150MHz because those values fall outside the 3-30MHz range specified by DeMaw’s transformer design. EX2021, ¶248. However, after receiving ParkerVision’s POPR in which they claimed “TI/Dr. Galton simply chose values and a waveform to get to the result that they needed,” I provided numerous additional simulation results with values and waveforms that more-closely matched those mentioned in the DeMaw textbook. As those subsequent simulations demonstrate (and as a POSITA would expect), the deviations of the RF signal and LO that Dr. Ricketts mentioned did not materially change the results.

40. Dr. Ricketts states that my simulation is physically unrealistic because I used “out-of-band frequencies” of 123.102 MHz for the RF signal and 150MHz for the LO signal. EX2021, ¶295. The circuit to which Dr. Ricketts refers is shown in Figure 6.7 of the DeMaw textbook, and while the textbook does mention that the transformers are suitable for 3 MHz to 30 MHz operation, 1) this does not mean that they will not operate at higher frequencies, and 2) a POSITA would understand that the fundamental behavior of the circuit would not be affected if transformers with higher frequency operation were used.

41. Indeed, our simulations used transformers with characteristics that exhibit negligible degradation at frequencies well above 150 MHz, so Dr. Ricketts is not correct in his assertion that the transformers are problematic in our simulations at the frequencies we chose.

42. A reasonable follow-up question might be whether actual transformers would possibly limit the frequency range as Dr. Ricketts implied. This question is answered in the Siliconix AN72-1 Application Note written by E. Oxner that was referenced in both the DeMaw textbook and my second declaration. TI-1044, 6-35, TI-1042, ¶83. The circuit shown in Figure 6.7 of the DeMaw textbook is very similar to that presented in AN72-1, although DeMaw made some minor simplifications that do not alter its fundamental behavior. Fig. 6.7 of DeMaw provides a slightly simplified textbook example of this type of mixer for teaching

purposes whereas the circuit described in AN72-1 is a slightly more complicated version of the circuit because the purpose of AN72-1 is to provide all implementation details. One such detail provided in AN72-1 is the high-frequency behavior of the transformers. Specifically, regarding the transformers it states that the recommended transformer uses a “ferrite core material with a permeability of 40 [and] provides satisfactory operation from 50 to 250 MHz”. TI-1044, 6-35. Therefore, the transformers are more than capable of operating well at the frequencies of our simulations.

2. LO Amplitudes

43. Dr. Ricketts criticized my use of a 1.2V peak (2.4V peak-to-peak) LO signal instead of using a 0.8V peak (1.6V peak-to-peak). DeMaw recommended, but did not require, that the LO amplitude should be 80% of $V_{GS(OFF)}$, and Dr. Ricketts assumed a pinch-off voltage of 2V, so he claims the peak should be 0.8V. EX2021, ¶296.

44. Dr. Ricketts would be correct if the pinch-off voltage were really restricted to 2 volts. However, DeMaw says that the range for the pinchoff of the Siliconix U430 is from -1 to -4 V, $V_{gs(off)}$ —a fact that Dr. Ricketts acknowledged. TI-1016, 8; TI-1051, 17:13-21, 18:8-21. Our design assumed a 3V pinch-off voltage, which is well within this range. Nevertheless, had we assumed a pinch-off voltage of 2 volts, the general behavior of the circuit and our conclusions

would not have been different. For context, the pinch-off voltage of a junction field-effect transistor (JFET) varies over a wide range over temperature and across different copies of the JFETs. If it were not true that the general behavior of the circuit and our conclusions would remain unchanged had we chosen a pinch-off voltage of 2 volts, then the circuit would not be practical because its fundamental behavior would change with the operating temperature and across different copies of the circuit.

3. DeMaw's Biasing Network

45. My original simulation of the bias circuitry for DeMaw's circuit is simpler to model but provides the same results for the bias voltage as that shown in the DeMaw textbook. The "core" of the mixer is comprised of JFETs J1 and J2. The two identical capacitor-inductor-capacitor bandpass filters at the drains at J1 and J2 are used to pass the desired signal which is frequency-translated to be centered at the IF frequency by the mixing behavior of J1 and J2, while suppressing the undesired higher-order mixing products.

46. There are two separate bias circuits, one is at the input of the mixer, and the other provides power to the circuit. Insofar as the input network performs the correct operation on the RF and LO signals, "Symmetrical feed is used at the mixer input by means of T1, T2, and T3, providing 180 degree phase differential between the two sources of Q1 and Q2" (J1 and J2 in our schematic, respectively),

and sets the desired DC voltage at the sources of J1 and J2, other details are not important. For example, in Dr. Ricketts' response, (EX2021, ¶251), he states, "...frequencies exceed this range by a factor of five...transformers are frequency-dependent components...produces inaccurate behavior". Each of these statements are factually true, yet irrelevant to the patent debate. First, no aspect of the patent or source material indicates that we need to consider any non-ideal (frequency-dependent) transformer behavior. Such non-idealities indeed have practical implications, e.g., the physical size of the circuit components, maximum bias current, etc.. However, none of these effects are modeled, and in Dr. Ricketts' response he does not explain how their inclusion would "materially affect circuit's behavior" (EX2021, ¶255). Indeed, they would not "materially affect circuit's behavior".

47. The power supply network is even easier to address. Typically, power supply networks incorporate filtering to isolate the circuit from external variations in the supply voltage, and/or from variations in the circuit's load current from influencing the external supply. The circuit was simulated in an ideal testbench, i.e., with no other circuits sharing the supply, and the supply itself was represented by an ideal voltage source. As such, the filter's parameters were not relevant in the simulation.

48. A more general point is that it is common practice to include a small

series resistance with every ideal voltage source in a simulation testbench. This is done when using typical circuit simulators to improve simulation convergence. The mechanism of action relates to how the circuit is “solved” by the numerical algorithms within the simulator. The exact value of this small resistor is unimportant; “small” is usually calculated as the largest value such that its impact on real-life circuit behavior is negligible. For example, if a circuit is designed for a nominal 1V supply and draws 1mA, using a 1 ohm series resistor with the 1V supply would drop 1mV, such that the circuit under test only sees a 999mV supply. Almost all reasonably-designed circuits can tolerate such an “inaccuracy.” This technique applies not only to supply voltage sources, but all driving sources (signal inputs, stimuli, etc.).

D. DeMaw Renders Obvious the Claimed Discharge Percentages

49. Dr. Ricketts is essentially claiming that there are two issues regarding the way I calculated the discharge percentages: 1) that the denominator of my discharge percent equation is the charge on the capacitor from the information signal (or inverted information signal) delivered during only the interval over which the corresponding switch was most recently closed, instead of the total charge resulting from the information signal (or inverted information signal) that remains on the capacitor at each time the corresponding switch opens, and 2) that my equation essentially eliminates the bias component of the charge.

50. First, I do not agree with Dr. Ricketts' interpretation of the phrase "total charge stored therein" in Claims 19-21 because he has ignored the phrase "stored therein." EX2021, ¶399. Yet, even if I apply his interpretation, the references I cited satisfy the requirements of Claims 19-21. TI-1003, ¶¶114-116.

51. Nevertheless, I feel that it is important to explain the issue that I see with Dr. Ricketts' interpretation. Specifically, Dr. Ricketts has ignored the phrase "stored therein" when interpreting Claims 19-21. My understanding is that every phrase in a claim is intended to convey a specific meaning, so it is not legitimate to ignore any phrase in a claim. Claim 18 ends with "wherein the information signal is used to store a charge on the first capacitor when the first switching device is closed and the inverted information signal is used to store a charge on the second capacitor when the second switching device is closed." Claim 19 follows with "The method of claim 18, wherein the first capacitor discharges between six percent to fifty percent of the *total charge stored therein* during a period of time that the first switching device is open, and wherein the second capacitor discharges between six percent to fifty percent of the *total charge stored therein* during a period of time that the second switching device is open" (emphasis added). If Claim 19 had been intended to mean that 6% to 50% of the total charge on the two capacitors is discharged during the period of time that the corresponding switch is open, the two instances of "*the total charge stored therein*" would have just been

“its total charge.” The same is true of Claims 20 and 21.

52. Instead, I believe that the *“stored therein”* phrase refers to the charging operation described in Claim 18 that occurred while the switch was last closed. The phrase *“total charge”* in isolation is unambiguous, so if the inventor had intended the discharge percentages mentioned in Claims 19-21 to apply to each capacitor’s *“total charge”* there would be no reason to qualify it as *“the total charge stored therein.”*

53. Nevertheless, as explained below, even if we use Dr. Ricketts’s interpretation of the claim, i.e., even if we replace each occurrence of the phrase *“the total charge stored therein”* with *“its total charge”* in Claims 19-21, DeMaw’s circuit still satisfies the requirements of Claims 19-21.

1. DeMaw Discharges the Claimed Percentages Even Under Dr. Rickett’s Interpretations

54. Dr. Ricketts interpreted the claims to require a calculation of how much of the total charge stored in a capacitor is discharged during the time a switch is open. EX2021, ¶402. It is of note that the amount of charge stored and discharged in a cycle of the circuit is small relative to the bias voltage. As explained above, I do not agree with Dr. Ricketts’ interpretation of the phrase as it ignores the words *“stored therein,”* and I believe I did calculate the discharge percentages correctly. However, the argument is irrelevant because the prior art I cited satisfy the requirements of Claims 19-21 even if I calculate the discharge

percentages as proposed by Dr. Ricketts.

55. Dr. Ricketts also states that I used an incorrect formula to calculate discharge. EX2021, ¶408. Dr. Ricketts used the following formula:

$$\% \text{ discharge} = \frac{\text{Charge discharged during the period switch is open}}{\text{Total charge stored at the beginning of the discharge period}}$$

Dr. Ricketts claims that my formula, i.e.,

$$\% \text{ discharge} = \frac{\text{Charge discharged during the period switch is open}}{\text{Charge stored in the same cycle}}$$

is incorrect. He further wrote:

Since charges on a capacitor are proportional to the voltage across it, i.e., $Q=C*V$, and capacitance (C) is constant, we can directly use voltages to calculate the discharge ratio:

$$\frac{Q_2-Q_1}{Q_1} = \frac{CV_2-CV_1}{CV_1} = \frac{V_2-V_1}{V_1}.$$

EX2021, ¶409²

56. Furthermore, when using his formula, Dr. Ricketts states that a negative result indicates a discharge and a positive value indicates a charge. EX2021, ¶410. I believe that Dr. Ricketts has made a sign error. If a negative result indicates a discharge, then the numerator of the “% discharge” equation

² This equation is actually incorrect because $V_2 - V_2=0$, so the right-most expression evaluates to zero, which makes no sense. For the purpose of this document, I have assumed that Dr. Ricketts intended the numerator of the right-most expression to be $V_2 - V_1$.

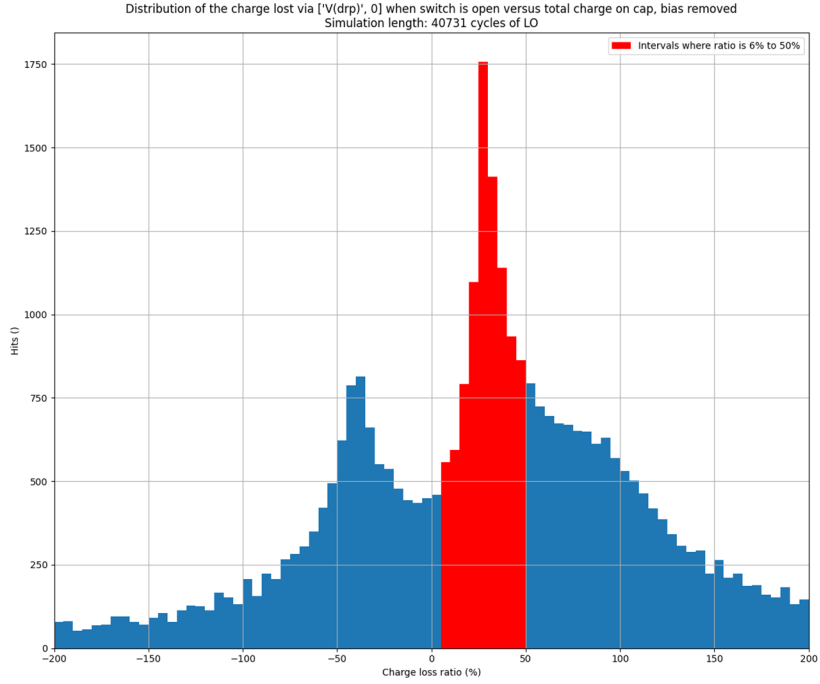
above, and therefore the “% discharge” value would be negative. Above, Dr. Ricketts’ defined “% discharge” over a period of time to be positive when the capacitor ends up with less charge at the end of the period than it had at the start of the period. V_1 and V_2 are the voltages across the capacitor at the start and end of the period, respectively, so if the capacitor discharges over the period then $V_2 < V_1$. Therefore, Dr. Ricketts’ equation is not consistent with his definition.

57. Even though I do not agree with Dr. Ricketts’ definition of the capacitor discharge percentage, I have modified the Python post-processing code to implement it as he asserts is correct. To show that both the DeMaw and Macnally circuits achieve the claimed discharge percentages even when using Dr. Ricketts’ interpretation of Claims 19-21, the Python post-processing code was altered as shown below via images cut-and-pasted from Apple’s FileMerge utility. The left side of each image shows a portion of the original com.py post-processing file provided to ParkerVision along with my supplementary expert declaration, and the right side of the image shows changes that have been made to the code (highlighted in red). All changes to the code are encompassed by the four images shown below.

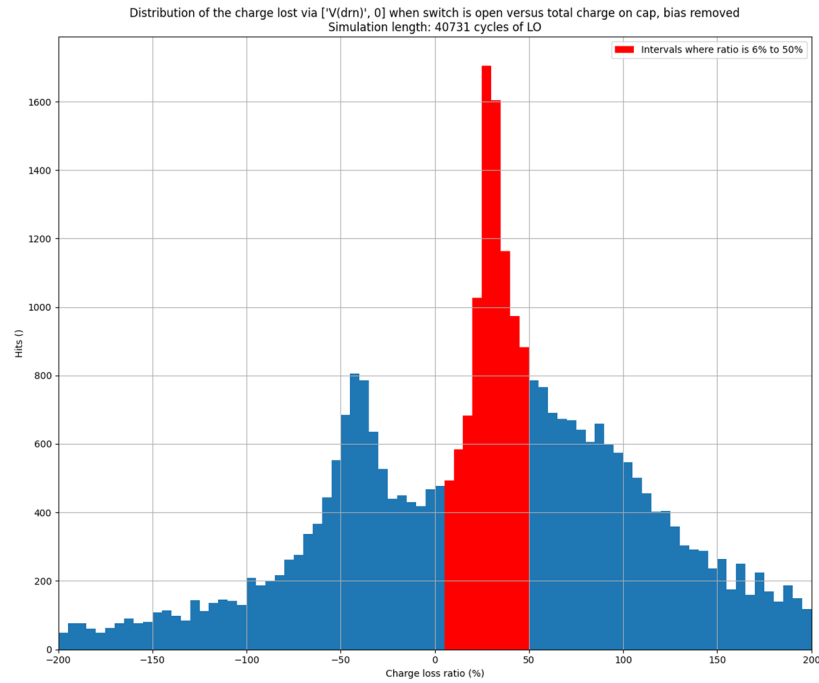
Original Code	Modified Code
<code>def cap_histogram(fd, fn, dat, lo, cap, tstart=60e-6, tend=400e-6, npts=None,</code>	<code>def cap_histogram(fd, fn, dat, lo, cap, tstart=60e-6, tend=400e-6, npts=None,</code>
<code>pct_range=[-200, 200], act_lo=True):</code>	<code>pct_range=[-200, 200], act_lo=True, zero_mean=False):</code>
<code>"""Plot shows the histogram of charge in and out of the capacitor.</code>	<code>"""Plot shows the histogram of charge in and out of the capacitor; use the</code>
<code>Parameters</code>	<code>TOTAL charge on the capacitor right before the switch opens.</code>

<pre> crosses = slice_wave(vlo, cap_sig, act_lo=act_lo) # Get the number of events, subtract one since we need the final crossing nevent = crosses.shape[0] nevent -= 1 # Determine if we should limit the number of points if npts is not None and (npts < nevent): nevent = npts # Compute the total charge delivered to the cap when the switch is on, and </pre>	<pre> crosses = slice_wave(vlo, cap_sig, act_lo=act_lo) # Subtract the average capacitor voltage if zero_mean: vcap_avg = (np.diff(tvec).dot(cap_sig[1:] + cap_sig[:-1]) / (2 * (tvec[-1] - tvec[0]))) cap_sig -= vcap_avg # Get the number of events, subtract one since we need the final crossing nevent = crosses.shape[0] </pre>
<pre> for ii in range(nevent): idx0 = crosses[ii, 0] idx1 = crosses[ii, 1] idx2 = crosses[ii + 1, 0] # Use capacitor voltage, already integrated by spice qin[ii] = cap_sig[idx1] - cap_sig[idx0] # Remove NaN values. This is safe since if qin[ii] is extremely small, # the charge transfer ratio is huge anyway, doesn't matter for this # computation. Just want to suppress divide by 0 warnings </pre>	<pre> for ii in range(nevent): idx0 = crosses[ii, 0] idx1 = crosses[ii, 1] idx2 = crosses[ii + 1, 0] # Use capacitor voltage, already integrated by spice # We are using the Ricketts definition of the discharge ratio, where # the denominator is "Total charge stored at the beginning of the # discharge period" qin[ii] = cap_sig[idx1] qout[ii] = -(cap_sig[idx2] - cap_sig[idx1]) </pre>
<pre> 'versus charge delivered when it is closed') ttl += '\nSimulation length: {} cycles of LO'.format(nevent) ax.set_title(ttl) capstr = ' '.join([str(x) for x in cap]) fh.savefig(fd + '/' + f'{fn}_cap_charge_histogram_{capstr}_{TNOW}.png') </pre>	<pre> 'versus total charge on cap') if zero_mean: ttl += ', bias removed' ttl += '\nSimulation length: {} cycles of LO'.format(nevent) ax.set_title(ttl) capstr = ' '.join([str(x) for x in cap]) fh.savefig(fd + '/' + f'{fn}_cap_charge_histogram_{capstr}_{TNOW}.png') </pre>

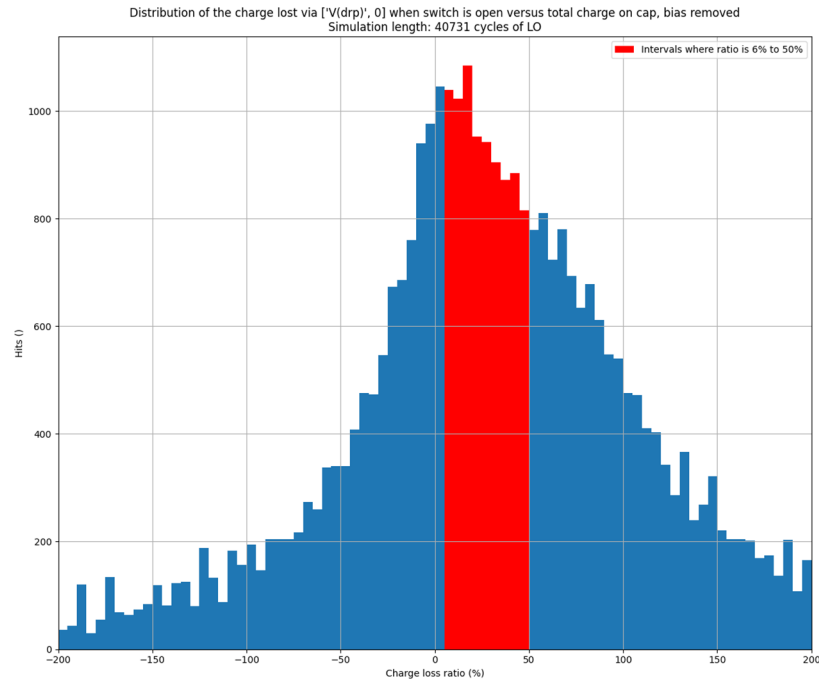
58. Below are histograms obtained by simply post-processing all 20 of the DeMaw circuit simulations described in Sections III through VI of my supplementary expert declaration with com.py modified as shown above. Note that no additional simulations were performed to create the histograms; the histograms were obtained by simply applying the modified Python file to the output files from the original simulations described in my supplemental declaration. As can be seen from the histograms, all still cover the claimed percentage discharge ranges between 6% and 50% (shown in red) even though they conform to Dr. Ricketts' interpretation of how to calculate the discharge percentages.



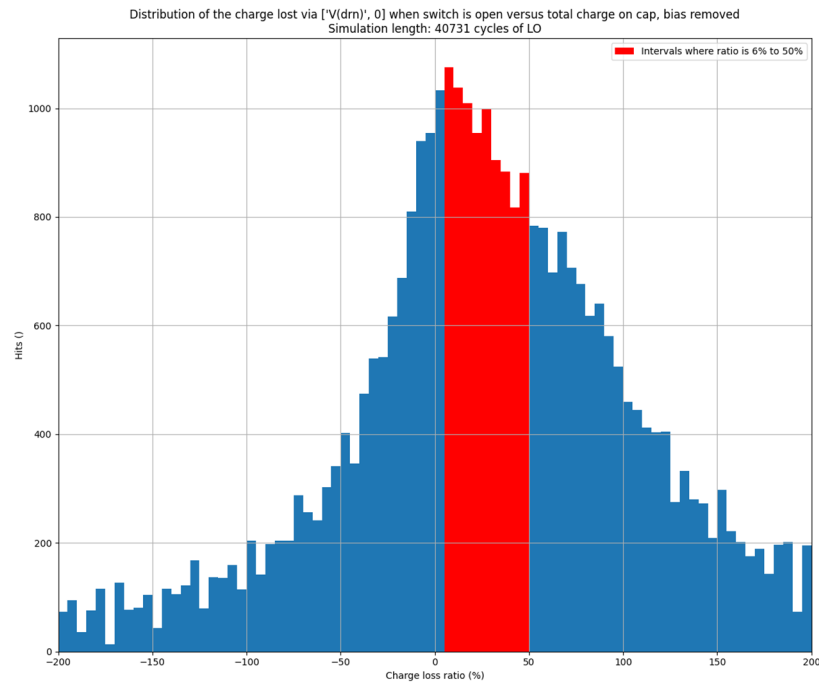
DEMAW-SIM-FIG. 7.2A. Post-processed charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.2).



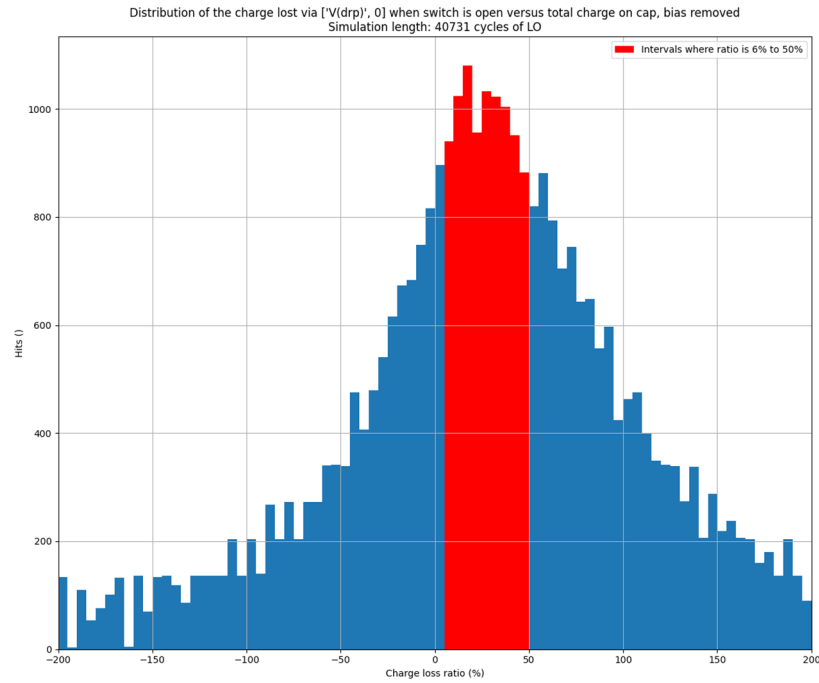
DEMAW-SIM-FIG. 7.2B. Post-processed charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.2).



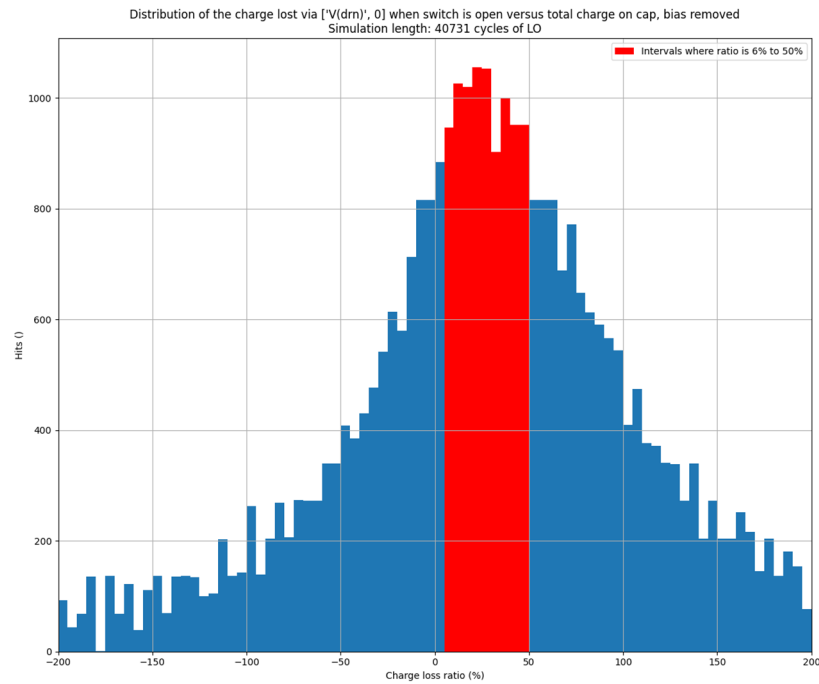
DEMAW-SIM-FIG. 7.3A. Post-processed charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.3).



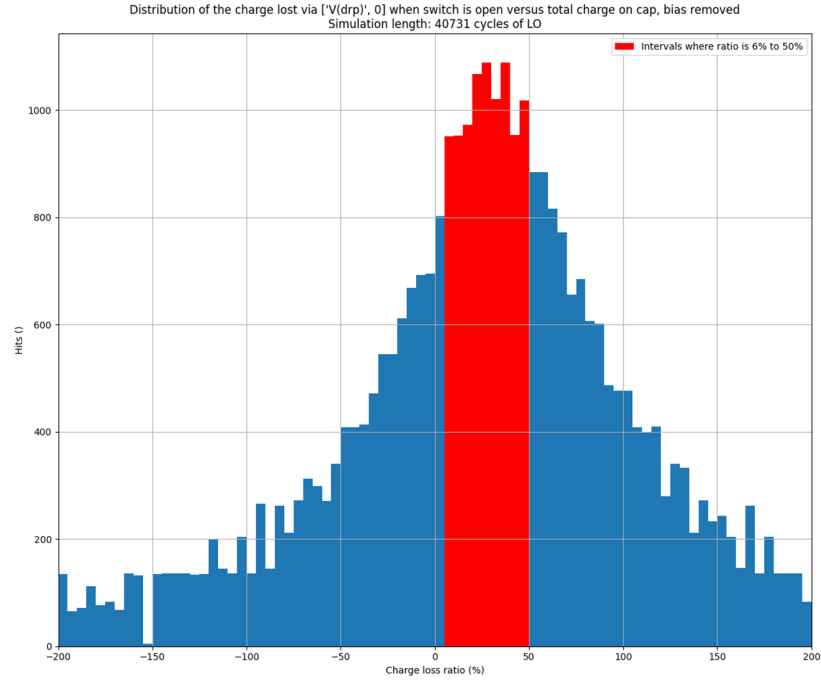
DEMAW-SIM-FIG. 7.3B. Post-processed charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.3).



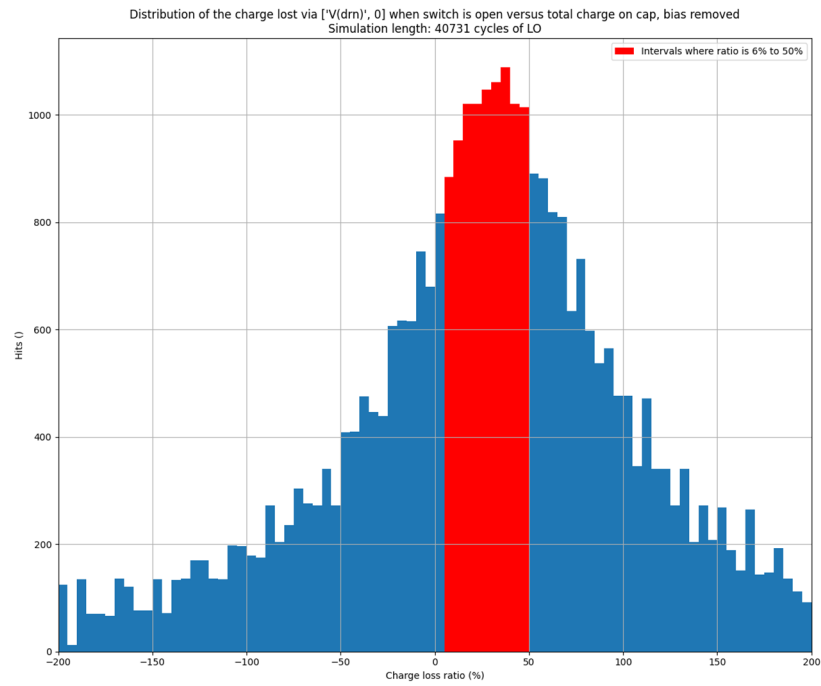
DEMAW-SIM-FIG. 7.4A. Post-processed charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.4).



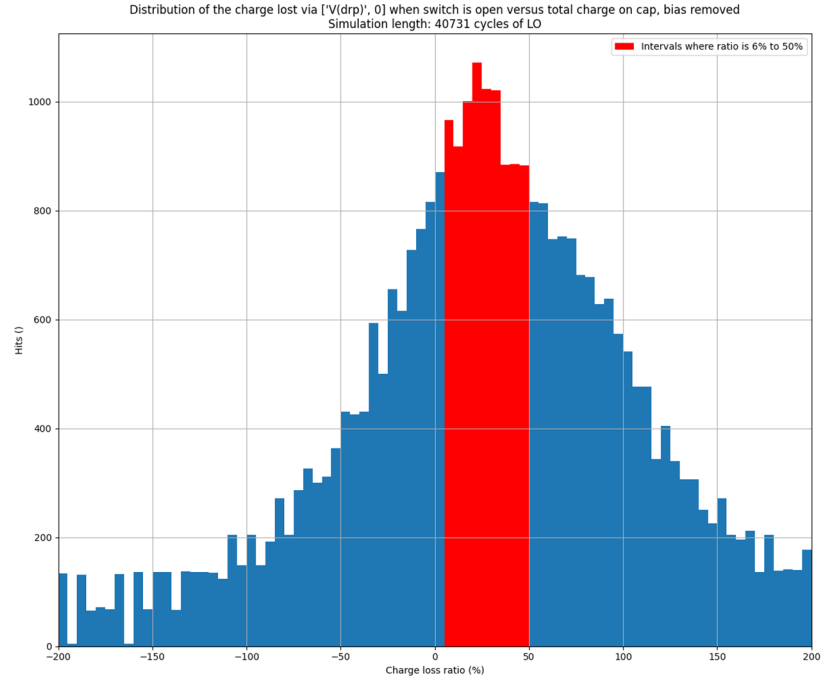
DEMAW-SIM-FIG. 7.4B. Post-processed charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.4).



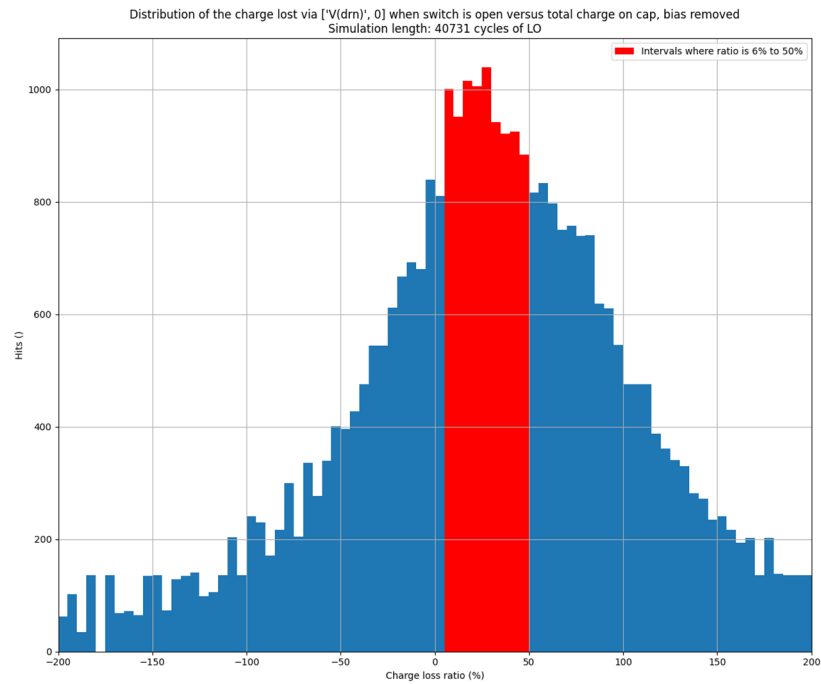
DEMAW-SIM-FIG. 7.5A. Post-processed charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.5).



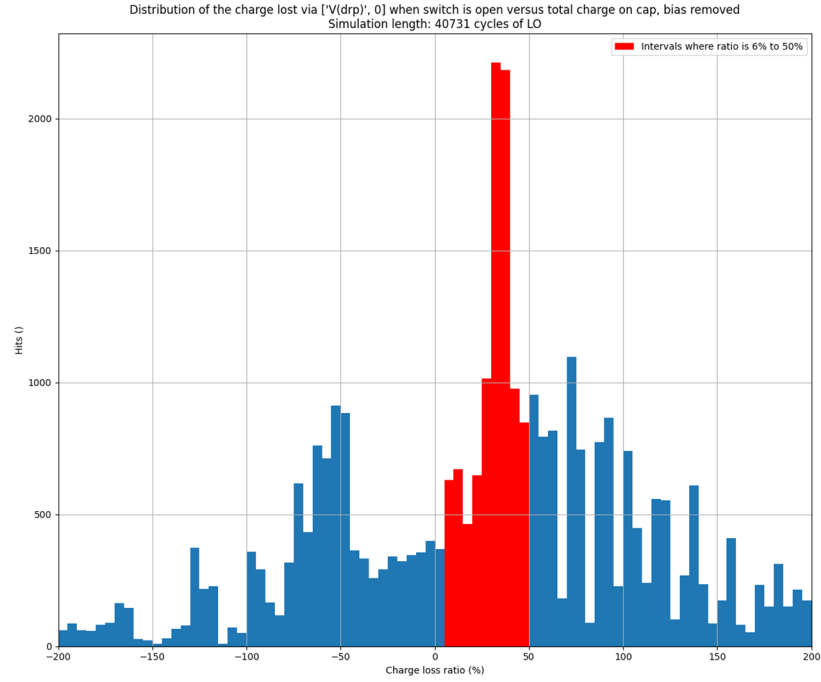
DEMAW-SIM-FIG. 7.5B. Post-processed charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.5).



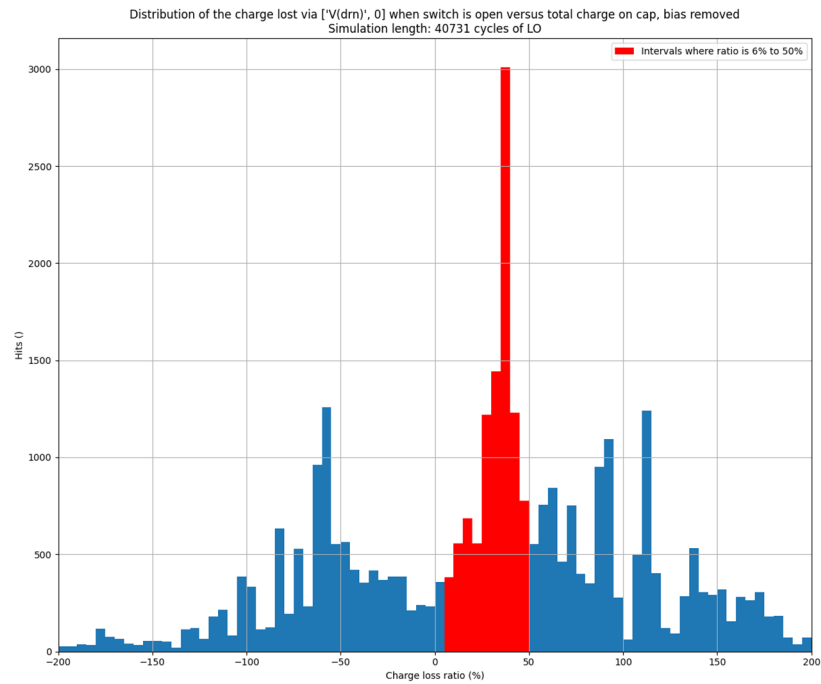
DEMAW-SIM-FIG. 7.6A. Post-processed charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.6).



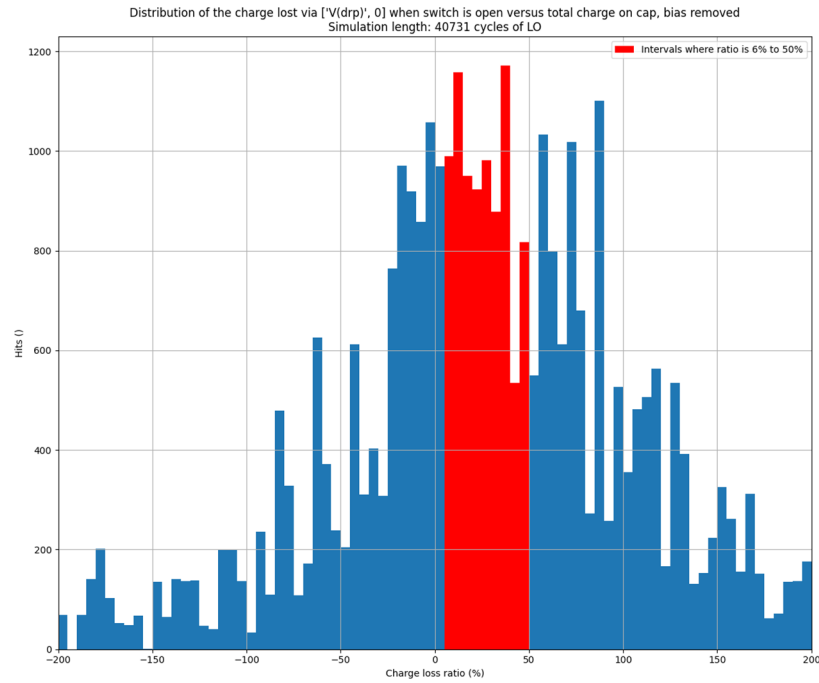
DEMAW-SIM-FIG. 7.6B. Post-processed charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.6).



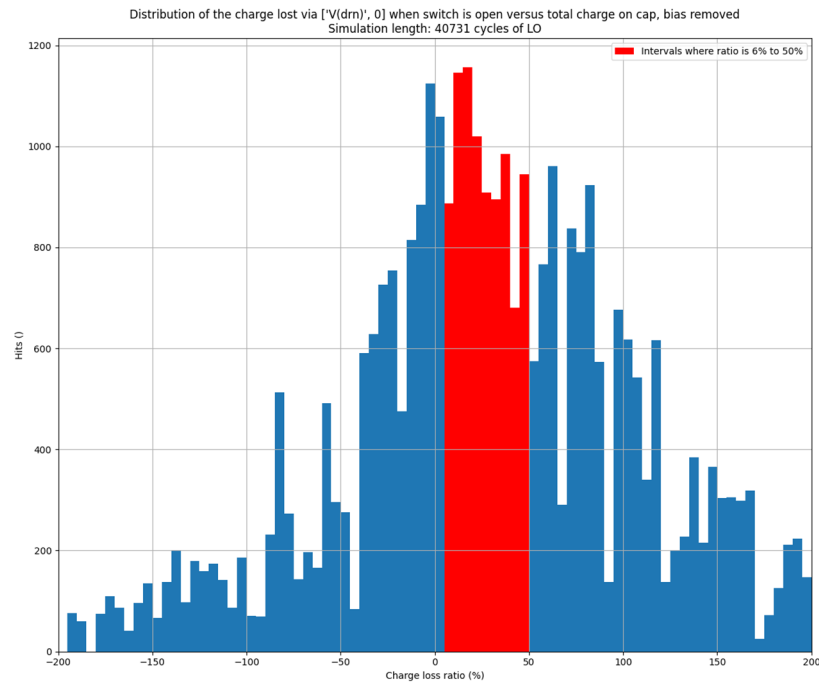
DEMAW-SIM-FIG. 7.7A. Post-processed charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.7).



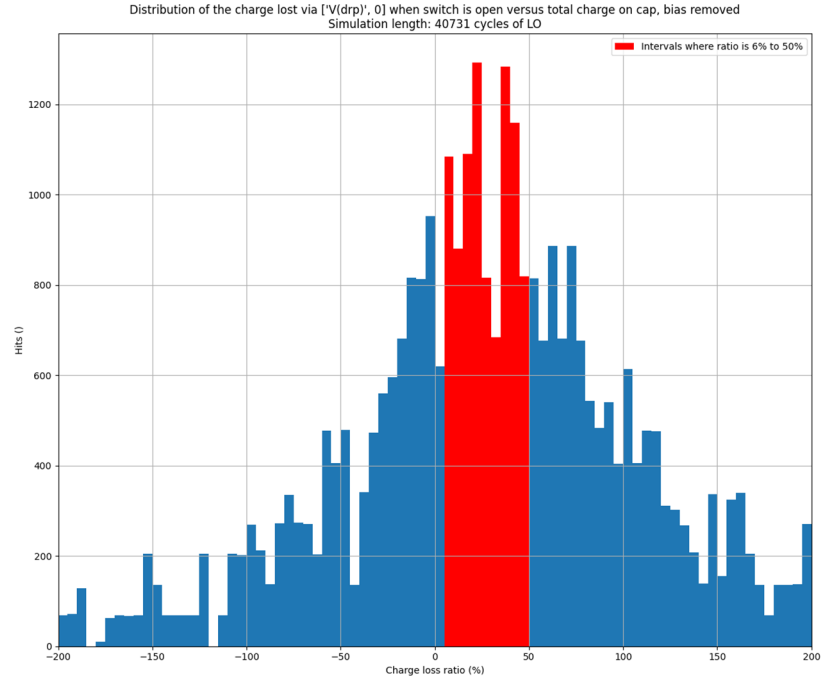
DEMAW-SIM-FIG. 7.7B. Post-processed charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.7).



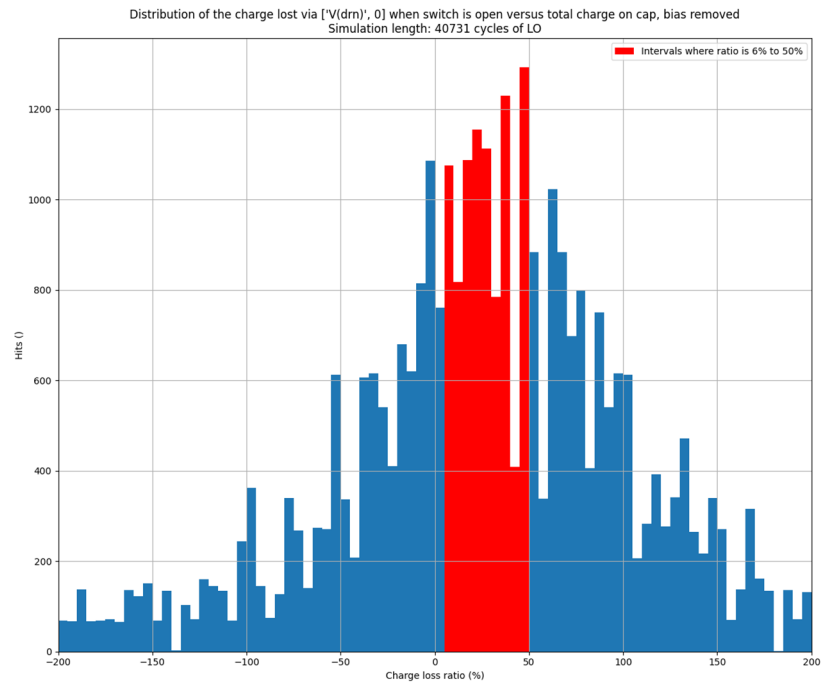
DEMAW-SIM-FIG. 7.8A. Post-processed charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.8).



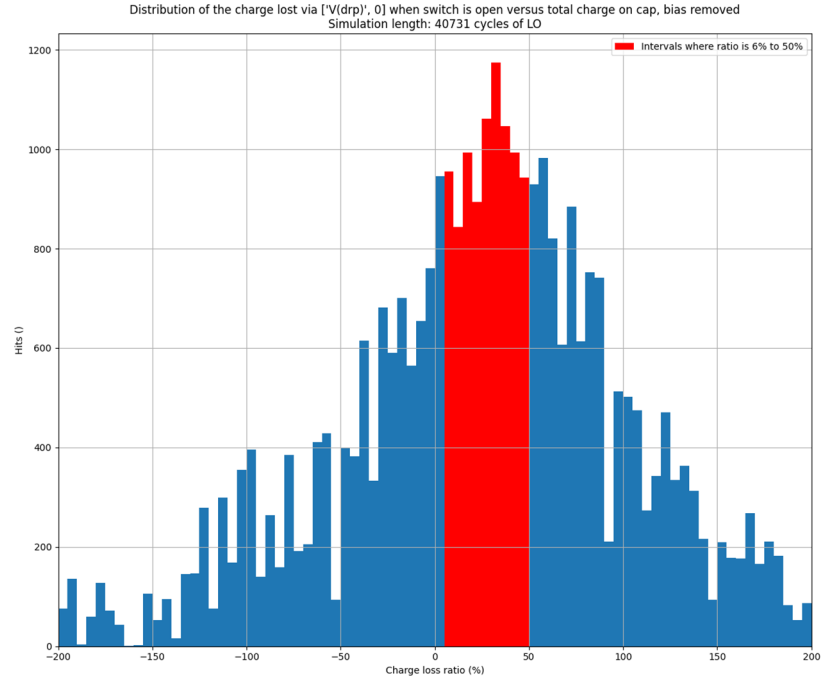
DEMAW-SIM-FIG. 7.8B. Post-processed charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.8).



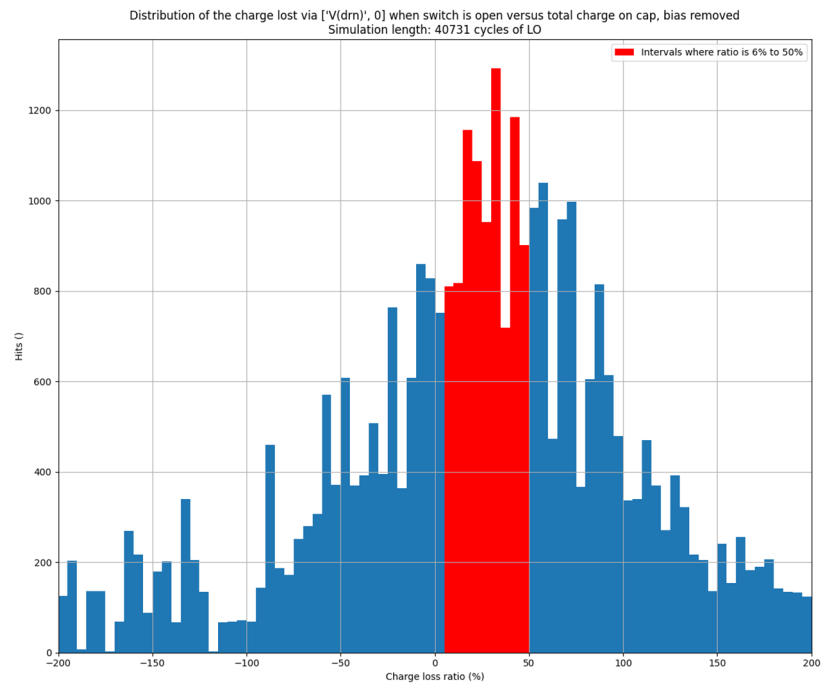
DEMAW-SIM-FIG. 7.9A. Post-processed charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.9).



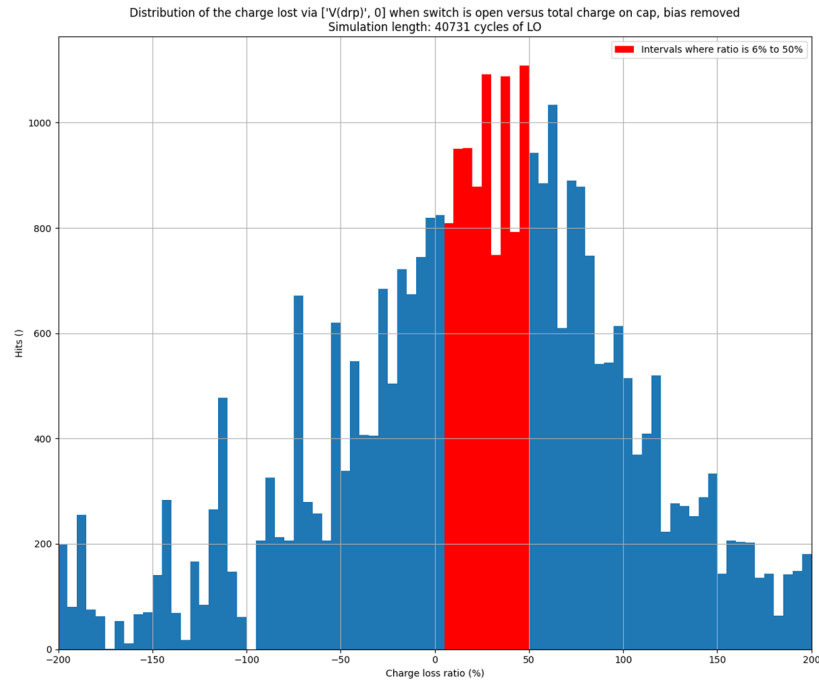
DEMAW-SIM-FIG. 7.9B. Post-processed charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.9).



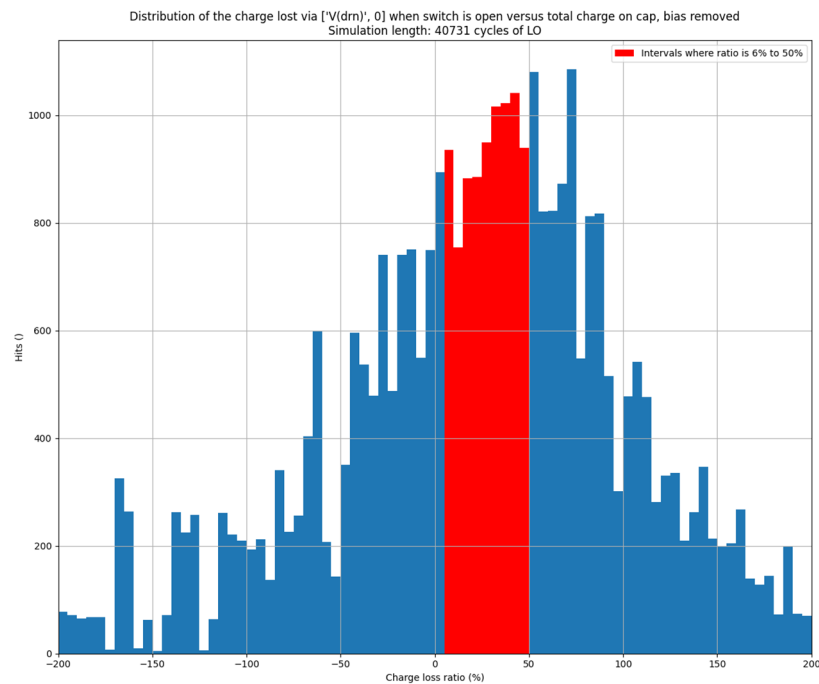
DEMAW-SIM-FIG. 7.10A. Post-processed charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.10).



DEMAW-SIM-FIG. 7.10B. Post-processed charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.10).



DEMAW-SIM-FIG. 7.11A. Post-processed charge loss ratio percentages histogram for capacitor C4 (circuit of DEMAW-SIM-FIG. 1.11).



DEMAW-SIM-FIG. 7.11B. Post-processed charge loss ratio percentages histogram for capacitor C5 (circuit of DEMAW-SIM-FIG. 1.11).

59. Dr. Ricketts states that “that *nearly all* of the percentage discharged

falls outside the ranges set forth in claims 19-21,” which appears to be an implicit admission that some of the percentages he calculated do in fact fall within the claimed ranges, which is all that is necessary to satisfy the claims. EX2021, ¶426. To avoid admitting that the circuit satisfies Claims 19-21 even under his own interpretation of the claims, he falls back to his prior argument that the switches never fully close. But as I have explained, no transistor-based switch is ideal, so one could use the same argument to assert that no practical circuit could satisfy Claims 18-21, including all embodiments of the alleged invention presented in the ’342 patent. Dr. Ricketts seems to agree. TI-1051, 16:7-24. Likewise, Dr. Ricketts agrees that the JFETs can have $V_{gs(off)}$ values that still conduct current. TI-1051, 17:5-12.

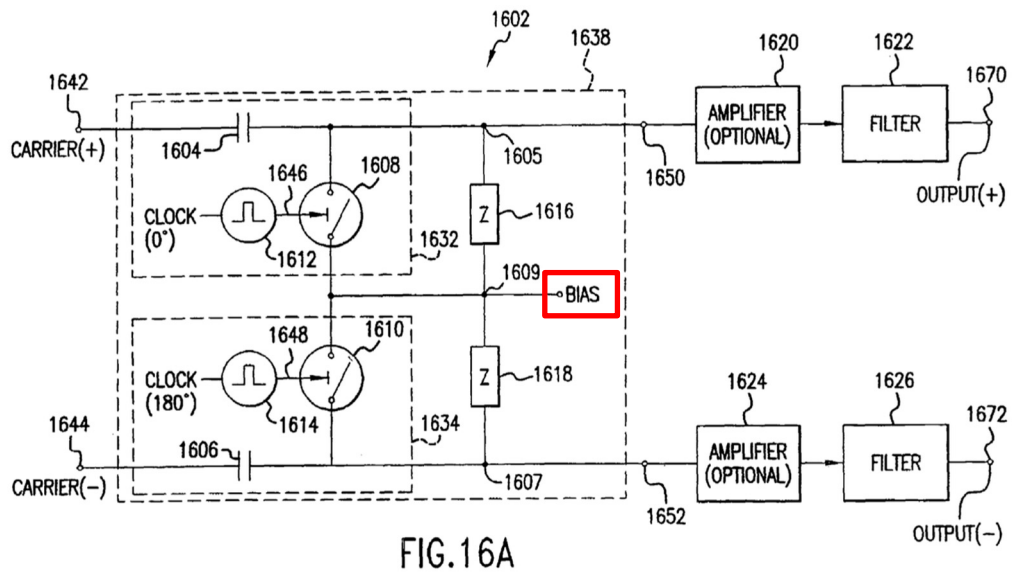
2. Voltage Bias Considerations

60. Dr. Ricketts also argued that my analysis essentially eliminates the bias component of the charge, which he asserts should have been included when calculating the histograms shown below. *See* EX2021, ¶¶411-415. I explain below why his assertion does not make sense in the context of the alleged invention of the ’342 patent.

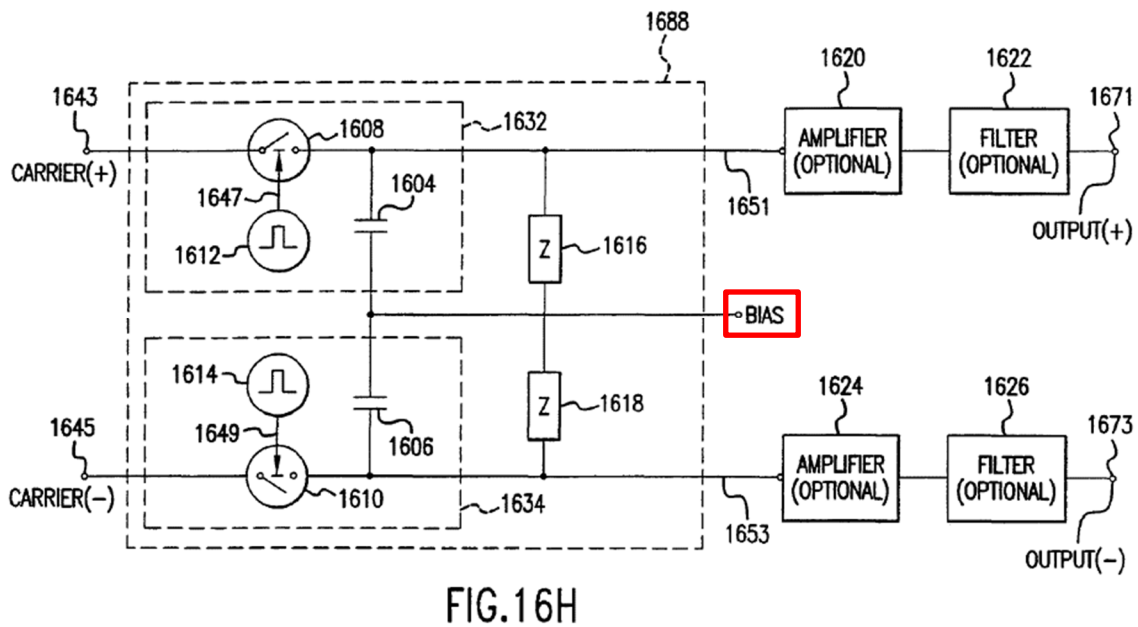
61. Dr. Ricketts states that since the capacitors in DeMaw do not fully discharge between LO cycles, the total charge stored is the cumulative charge on the capacitor, which includes the residual baseline voltage and the charge that has

incrementally accumulated over many cycles. EX2021, ¶406. By “the residual baseline voltage—set by a 12V power supply,” Dr. Ricketts is referring to the bias voltage across each capacitor. Bias voltages are constant by definition. The total voltage across each capacitor is the constant bias voltage plus the voltage waveform resulting from the received signal (i.e., the “information signal” or “inverted information signal” in the terminology of Claim 18). As Dr. Ricketts points out in Paragraph 71 of his declaration, the charge stored on a capacitor is $C \cdot V$, where C is the value of the capacitor and V is the voltage across the capacitor. Therefore, the charge on the capacitor has a constant bias component plus a time-varying signal component resulting from the received signal. Claim 18 clearly states that the charge of interest is the latter, i.e., it states that “the information signal is used to store a charge on the first capacitor when the first switching device is closed and the inverted information signal is used to store a charge on the second capacitor when the second switching device is closed.” Therefore, to properly calculate the discharge percentage of each capacitor in accordance with Claims 18-21, it is necessary to omit the constant charge component caused by the bias voltage across the capacitor (as this voltage component never gets discharged).

62. Many of the embodiments of the alleged invention described in the '342 patent show bias voltages, e.g.,:



TI-1001, FIG. 16A (annotated to show the bias voltage)



TI-1001, FIG. 16H (annotated to show the bias voltage)

63. The '342 patent states that "Fig. 16A is an example two-switch receiver according to an embodiment of the invention." TI-1001, 3:47-48. And

that in FIG. 16A, “A bias voltage is applied to a node 1609.” TI-1001, 26:22; see also, *id.*, 2:27-28 (“The operation of the receiver of FIG. 16H is similar to that of receiver 1602, and thus is not repeated here.”). A POSITA would recognize that the choice of the bias voltage at node 1609 in FIG. 16A would only affect the bias voltage about which the output signal component at each of nodes 1605 and 1607 varies without affecting the signal component itself because capacitors 1604 and 1606 block any DC current from flowing to or from the inputs (the nodes labeled “CARRIER(+)” and “CARRIER(–)” in FIG. 16A, which represent the information signal and the inverted information signal, respectively). Consequently, a POSITA would understand that the choice of bias voltage would not affect how the circuit processes the information signal and the inverted information signal provided at input nodes 1642 and 1644. Hence, the POSITA would interpret the Claim 18 clause “the information signal is used to store a charge on the first capacitor when the first switching device is closed and the inverted information signal is used to store a charge on the second capacitor when the second switching device is closed” to refer to the charge on the capacitor excluding any constant charge resulting from the specific choice of the bias voltage.

64. This is the only interpretation that makes sense. If the discharge percentage were instead interpreted to include the constant charge component resulting from the bias voltage, it would lead to two conclusions that would not be

in ParkerVision's interest. One of the conclusions is that the discharge percentage would depend on the amplitudes of the information signal and the inverted information signal because the bias component of the charge would not be affected by reducing the amplitudes of the information signal and the inverted information signal. Therefore, any embodiment with a non-zero bias component would not infringe on Claims 18-21 for sufficiently small-amplitude information signals (and information signals in such applications tend to have small amplitudes). The other conclusion is that it would be possible to prevent embodiments such as that shown in FIG. 16A from infringing on Claims 18-21 simply by the appropriate choice of the bias voltage. This is because the bias voltage component never gets discharged by load impedances 1616 and 1618, so increasing the bias component would reduce the discharge percentages. Therefore, it is highly unlikely that ParkerVision intended for such an interpretation of Claims 18-21. Nevertheless, Dr. Ricketts' chose not to remove the bias voltage, and his failure to do so is what caused his data to not show the claimed discharge percentages—his bias voltage is sufficiently high to obscure the percentages.

65. Note that the voltage bias considerations only apply to DeMaw, and not to Macnally, as there is no bias component on the capacitors in the Macnally circuit. In other words, the op-amp of Manally's circuit does not impose a bias voltage across Macnally's capacitor. However, neither side of either capacitor in

Macnally is connected to VDD. The op-amp sets its output voltages to ensure that its two input voltages are nearly equal, and the input voltages are set by the Macnally mixer circuit. The constant bias current through the mixer's resistors ensures that the op-amp's input voltages are well below VDD.

66. Further, Dr. Ricketts complains that I use an improper JFET bias configuration—a 1.2V DC supply in series with a 5Ω resistor—rather than following DeMaw's teachings to bias at $0.8 \times V_{GS(OFF)}$. EX2021, ¶292 (erroneously alleging a 2V DC supply being used). However, it is not valid to argue that minor biasing changes and minor component value changes necessarily cause the functionality of a circuit to change fundamentally. As I explained above, the use of a 1.2 V LO amplitude is consistent with the $0.8 \times V_{GS(OFF)}$ teaching of DeMaw given that $V_{GS(OFF)}$ is specified as a range of values. In the simulations I presented in my original declaration, I used a voltage source and a small resistor to implement the bias voltage instead of a large resistor as in DeMaw Fig. 6.7 simply for convenience (dialing in the precise desired bias voltage during simulations is simpler to achieve with a voltage source than adjusting the resistance to achieve the desired bias voltage). The end result is the same in terms of circuit behavior in that both methods achieve the desired bias voltage. When Dr. Ricketts accused me of changing the circuit to achieve the behavior I was trying to show, I submitted a supplementary declaration in which I modified the circuit to closely adhere to that

shown in DeMaw Fig. 6.7, and, as expected, the changes had no material effect on the simulation results.

3. Rebuttal Concerning DeMaw Simulations

67. Dr. Ricketts misinterprets the resulting data and misrepresents my statements about them. For the simulations in Section III of my Second Declaration, Dr. Ricketts alleges that “the circuit introduced in Section III of [my] Second Declaration introduces significant alterations to Dr. Galton’s original simulation, as well as the corrected JFET model simulation in Section II.” EX2021, ¶299 (alleging “a new and materially different simulation.”). As explained above, the simulations in my Section Declaration were provided after the Board’s decision to institute review of the ’342 claims and in response to ParkerVision’s allegation of my First Declaration. Dr. Ricketts quotes my language from my Second Declaration: “DEMAW-SIM-FIGS. 4.2, 5.2, 6.2, 7.2A and 7.2B show the same simulation output from DEMAW-SIM-FIG. 1.2 as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1.2.” EX2021, ¶319 (quoting TI-1042, ¶26). Dr. Ricketts alleges that I intend to “‘show the same simulation output’ as [my] original simulation.” EX2021, ¶300. However, in the context of my Second Declaration and Original Declaration, a POSITA, or any literate person for that matter, would understand the statement to mean that the results shown in DEMAW-SIM-FIG. 4.2, 5.2, 6.2, 7.2A and 7.2B respectively

correspond to those shown in DEMAW-SIM-FIGS. 4, 5, 6, and 7 except that the former were generated by simulating DEMAW-SIM-FIG. 1.2 and the latter were generated by simulating DEMAW-SIM-FIG. 1.

68. Similarly, for the simulations in Section IV of my Second Declaration and corresponding histograms shown above, Dr. Ricketts quotes my language from my Second Declaration: “DEMAW-SIM-FIGS. 4.7, 5.7, 6.7, 7.7A and 7.7B show the same simulation output ... as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusion in my original Declaration regarding the claims...are likewise supported.” EX2021, ¶330 (quoting TI-1042, ¶51). Dr. Ricketts has misread the quoted sentence. A POSITA, or any literate person for that matter, would understand the statement to mean that the results shown in DEMAW-SIM-FIGS. 4.7, 5.7, 6.7, 7.7A and 7.7B respectively *correspond* to those shown in DEMAW-SIM-FIGS. 4, 5, 6, and 7 except that the former were generated by simulating DEMAW-SIM-FIG. 1.7 and the latter were generated by simulating DEMAW-SIM-FIG. 1.

69. For the waveforms in Section V of my Second Declaration and corresponding histograms shown above, Dr. Ricketts quotes my language from my Second Declaration: “DEMAW-SIM-FIGS. 4.12, 5.12, 6.12, 7.12A and 7.12B show the same simulation output ... as DEMAW-SIM-FIGS. 4, 5, 6, and 7 show from DEMAW-SIM-FIG. 1. The conclusions in my original Declaration regarding

the claims ... are likewise supported.” EX2021, ¶343 (quoting TI-1042, ¶84). A POSITA, or any literate person for that matter, would understand the statement to mean that the results shown in DEMA W-SIM-FIGS. 4.12, 5.12, 6.12, 7.12A and 7.12B respectively *correspond* to those shown in DEMA W-SIM-FIGS. 4, 5, 6, and 7 except that the former were generated by simulating DEMA W-SIM-FIG. 1.12 and the latter were generated by simulating DEMA W-SIM-FIG. 1.

70. For the waveforms in Section VI of my Second Declaration and corresponding histograms shown above, Dr. Ricketts quotes my language from my Second Declaration: “DEMA W-SIM-FIGS. 4.17, 5.17, 6.17, 7.17A and 7.17B show the same simulation output ... as DEMA W-SIM-FIGS. 4, 5, 6, and 7 show from DEMA W-SIM-FIG. 1. The conclusions in my original Declaration regarding the claims ... are likewise supported.” EX2021, ¶353 (quoting TI-1042, ¶115). A POSITA, or any literate person for that matter, would understand the statement to mean that the results shown in DEMA W-SIM-FIGS. 4.17, 5.17, 6.17, 7.17A and 7.17B respectively *correspond* to those shown in DEMA W-SIM-FIGS. 4, 5, 6, and 7 except that the former were generated by simulating DEMA W-SIM-FIG. 1.17 and the latter were generated by simulating DEMA W-SIM-FIG. 1.

71. I never wrote nor implied that the simulation results themselves are “the same” and the plots I presented clearly show differences between the simulated results from the two circuits. However, none of those differences change

any of my original conclusions, nor do they represent fundamentally different behavior. Sadly, as Dr. Ricketts is clearly a literate person, the only conclusion I can reach is that he has purposely taken my quote out of context (as I have explained above), just so that he can state without any actual evidence that my previous analysis cannot be relied upon. This is shameful behavior.

72. Furthermore, as I explained in my original declaration, the differences between the circuit I simulated originally and that shown in Fig. 6.7 of the DeMaw textbook or in Oxner's AN72-1 Application Note would have been recognized by a POSITA to be reasonable design choices that would not fundamentally alter the principle of operation of the circuit. Nevertheless, ParkerVision's POPR accused me of having made those design choices to falsely show that the DeMaw circuit is an embodiment of the alleged invention of the '342 patent, i.e., it states "TI/Dr. Galton simply chose values and a waveform to get to the result that they needed". To address this accusation I subsequently submitted simulations which adhere as closely as possible the circuit shown in Fig. 6.7 of the DeMaw textbook and I also submitted simulations which adhere as closely as possible to the circuit shown in the AN72-1 Application Note on which the circuit in Fig. 6.7 of the DeMaw textbook is based. TI-1042, ¶83; TI-1044, 6-31. Now Dr. Ricketts is complaining that I made changes he had previously criticized me for not implementing in the first place.

73. The reality, however, is that the original simulation and the subsequent simulations indicate that the DeMaw and AN72-1 Application Note circuits represent embodiments of the alleged invention of the '342 patent. Furthermore, the results are very robust in that they hold over a wide range of component values and operating conditions.

74. The following summarizes changes in my Second Declaration relative to my Original Declaration:

75. **DeMaw-2, Section III** (DeMaw circuit modified to match DeMaw FIG 6.7 with squared-up LO) and **DeMaw-2, Section IV with difference being sinusoidal LO signal** (DeMaw circuit modified to match DeMaw FIG 6.7 with sinusoidal LO):

Parameter	Original Declaration	Second Declaration	Notes
JFET Model Addressed in section III.B	Default, generic LTspice JFET model	Siliconix U430 JFET	
Bias Network	V4 = 2V Resistor R4 = 5Ω	No V4 Resistor R4 = 1.6kΩ	The 5Ω R4 resistor in my first declaration was chosen for simulator convergence as described above. The R4 resistor value in my second declaration was chosen to achieve a drop of approximately 0.8V _p . The value of V _p was obtained by doing device sweep simulations, and estimating (fitting) the model parameter to the characteristic curve. The datasheet for the device itself does not specify a unique value of V _p , but provides a range of -1 to -4V, also quoted by Dr. Ricketts. EX2021, ¶245.

LO input	No source impedance	Resistor R3 = 50Ω added	This resistor is included in the second simulation to more closely model a realistic driving signal source, which typically has a 50 ohm output impedance. It has no material effect on the functional circuit behavior with respect to the patent claims.
VDD supply resistor	Resistor R2 = 5Ω	Resistor R2 = 33Ω	This resistor, together with capacitor C8, forms a supply decoupling filter. The value of this resistor and the filter pole have has no effect on the circuit behavior as simulated.
Inductors L1, L2, L43, L4, L5, and L6	400 μ H	4 μ H	In the first simulation, the transformer coupling coefficient was 1.0, so only the ratios of the inductance values matter. The values themselves made no difference as there was no leakage inductance. For example, with a coupling coefficient of 1.0, it would be impossible to make measurements of voltages/currents at any point within the circuit and ascertain those inductance values. In the second simulation, the coupling coefficient is again very high so leakage inductance is low. However, the value of 4uH is close to what would be physically achieved according to the device geometry described in the text.
Inductors L9, L10, and L11	600 μ H	4 μ H	
RF Frequency	123.102 MHz	150 MHz	These two values (LO and RF) were chosen to generate an IF around 30MHz. In fact, DeMaw does not specify at all the LO, RF, or IF frequencies. The impedance matching network is a tuned circuit, but DeMaw omits any values for individual components and only specifies the impedance transformation ratio. Rather than making up random values, I have used the values (or very close to the values) specified by Oxner in AN-72. The reason I used non-rounded values such as 119.8MHz versus a nice round 120MHz is to prevent perfect frequency ratios from hiding circuit behavior behind perfect aliasing. In
LO Frequency	150 MHz	119.8 MHz	

			practice, temperature and manufacturing errors always result in very small frequency offsets, so avoiding perfect ratios is a standard engineering practice.
LO Amplitude	1.2V	0.785V	In the revised simulation, we use either 0.785Vpk square wave or 1.0Vpk sine wave. These have equivalent first harmonic amplitudes, with $0.785V * 4 / \pi \approx 1.0V$. According to both DeMaw and Oxner, the peak-peak LO voltage should be less than (approximately 0.8) Vp, so with a Vp of 2-2.2V, these voltages are in the right range.

76. **DeMaw-2, Section V** (DeMaw circuit modified to match Oxner with **Squared-up LO**) and **DeMaw-2, Section VI** (DeMaw circuit modified to match Oxner with Sinusoidal LO):

Parameter	Original Declaration	Second Declaration	Notes
JFET Model Addressed in section III.B	Default, generic LTspice JFET model	Siliconix U430 JFET	
LO input	No source impedance	Resistor R3 = 50Ω added	Same as the corresponding entry in the table above.
VDD supply resistor	Resistor R2 = 5Ω	Resistor R2 = 1Ω	Oxner does not specify a supply filter. As explained above, common practice to improve circuit simulator convergence is to insert a small (small enough to not affect circuit behavior) resistance in series with a voltage source if one is not already present.
Inductors L1, L2, L43, L4, L5, and L6	400 μ H	4 μ H	The answers for entries below are identical to corresponding entries in the table above.
Inductors L9, L10	600 μ H	4 μ H	
RF Frequency	123.102 MHz	150 MHz	

LO Frequency	150 MHz	119.8 MHz	
LO Amplitude	1.2V	0.785V	

77. Other modifications in **Section V** (DeMaw Modified to Match Oxner with squared-up LO) not present in sections III or IV

Parameter	Original Declaration	Second Declaration	Notes
Bias Network	Resistor R4 = 5Ω	Resistor R4 = 1Ω	As explained above, small series resistances help simulator convergence. Moreover, this is more realistic.
VDD supply resistor Matches values in table above for Section V	Resistor R2 = 5Ω	Resistor R2 = 1Ω	
Inductors L11	600 μ H	1 μ H	The Oxner circuit uses a 4:1 impedance ratio in the output transformer, so this value is determined once the other winding (two series 4uH inductors) is determined.
Capacitors C4, C5	31p	30p	Use exact values specified by Oxner.
Capacitors C6, C7	120p	68p	

IV. Macnally

A. General functioning of Macnally

78. Dr. Ricketts argues that the local oscillator signal in Macnally is sinusoidal, thereby implying that transistors M5, M6, M7, and M8 in the mixer circuit do not act like switches. EX2021, ¶¶209-210. However, this is not correct, as Dr. Ricketts himself makes clear in Paragraph 210 in which he points out that

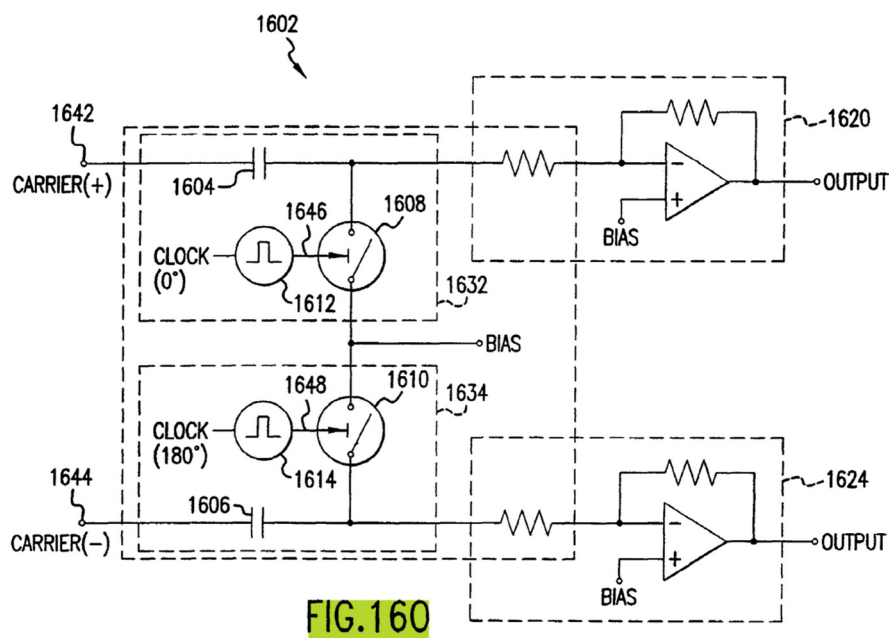
the Macnally patent provides the unambiguous statement: “The LO input transistors [M5, M6, M7, M8] *operate as switches* that steer a process and temperature independent current.” ’342 patent, 7:12-14 (emphasis added).

79. Similarly, Dr. Ricketts criticizes my simulation for using a full-swing LO clock signal that was “neither taught nor suggested by the patent.” EX2021, ¶365. However, the Macnally patent states that the “LO input transistors operate as switches” which implies that the LO signal approximates a square wave, and that the amplitude of the square wave is large enough to ensure this behavior. The easiest way to do this, and, therefore, the most likely way that Macnally did it, is to use a full-swing LO clock signal.

80. Dr. Ricketts also complains that I simulated down-conversion of a 1.0 GHz sinusoidal carrier amplitude modulated (AM) 10% by a 425.3 kHz sinusoidal message signal instead of using BFSK modulation. EX2021, ¶366. Mixers are designed to shift the spectrum of an input signal from one center frequency to another, and the details of the spectrum aside from its bandwidth, power, and center frequency are not relevant to their operation. Amplitude modulated (AM) signals are easier to visualize and understand than BFSK signals, so I chose to use an AM signal for demonstration purposes. ParkerVision’s POPR criticized me for making this choice and suggested I would have reached different conclusions had I used a BFSK signal, so I subsequently submitted an additional simulation with a

BFSK signal to show that this is not the case.

81. Dr. Ricketts further states, “Because Macnally’s mixer circuit provides gain, a POSITA would understand that the mixer is an active non-sampling mixer, using the NMOS FETs as voltage-controlled current sources, thereby allowing the circuit to amplify the signal while performing frequency conversion.” EX2021, ¶211. This statement is also not true, and is contradicted by the ’342 patent itself. As one example, FIG. 16O in the ’342 patent is an embodiment of the alleged invention:



’342 patent, Fig. 16O

As stated in the ’342 patent: “For the embodiment of the invention shown in Fig. 16O, the carrier signal riding on the downconverted signal is removed using amplifiers 1620 and 1624.” ’342 patent, 50:40-42. Therefore, this embodiment of

the alleged invention performs amplification, despite Dr. Ricketts assertions that 1) the alleged invention is a sampling mixer and 2) that sampling mixers do not provide gain.³ EX2021, ¶211.

82. Dr. Ricketts also criticizes my original simulation for modeling the active load transistors with LTSpice default devices, which have no defined electrical parameters. EX2021, ¶371. Additionally, Dr. Ricketts criticizes my revised simulation for removing the transistors and replacing them with resistors. EX2021, ¶371. Circuit diagrams published in papers, patents, and textbooks often represent current sources as resistors for simplicity because they affect the signal components of a circuit in the same way as large resistors. TI-1048, 4, 402-405. This simplifies the circuit diagrams and makes it easier to understand the behavior of the circuit, but the use of actual large resistors is often problematic in practice.

³ Note that 1620 and 1624 are essentially the same op-amp based amplifiers used by Tayloe, and referring to Fig. 16O, the '342 patent states that "impedances 1616 and 1618 [of Fig. 16A, which are low impedance loads] are a part of optional amplifiers 1620 and 1624, and thus there are no separate impedance devices 1616 and 1618." '342 patent, 18:24-27. This contradicts the argument made by Dr. Ricketts in his declarations for '177 and '528 that such amplifiers must have high impedance inputs.

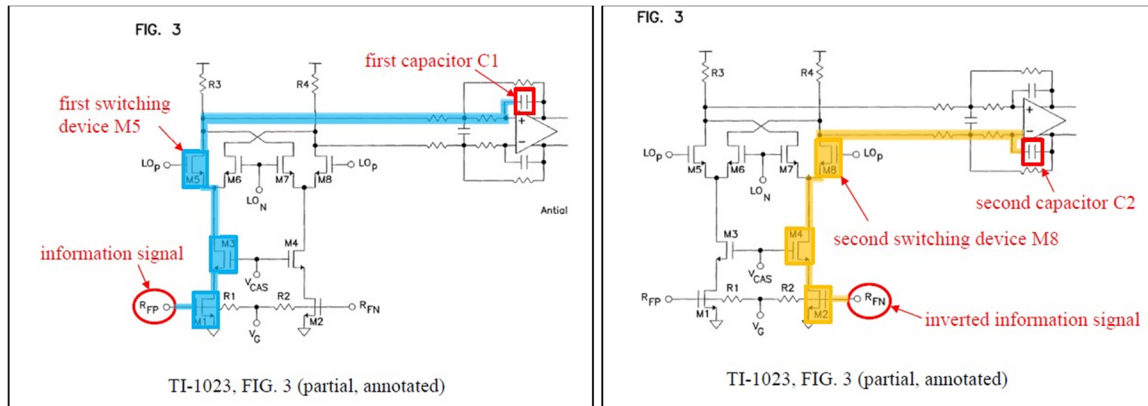
While it is often desirable to have large resistances to achieve a high gain, large resistors through which bias current flows have large voltage drops across them, which can limit the available signal swing, and they also tend to have large areas, which makes them expensive. Current sources provide a way of achieving large resistances without large voltage drops or large circuit areas. As the gain of the Macnally mixer is relatively high (14.2 dB), I assumed (and still believe) that R3 and R4 in the Macnally circuit were actually implemented as current sources. Transistors M12 and M13 in the figure above implement the current sources, and the 10 K Ω resistors R5 and R6 are used as part of a feedback network to ensure that they are biased correctly. This would have been a very common design choice for a POSITA since long before the time of the priority date of the '342 patent, and I do believe that the actual Macnally implementation took such an approach.

83. However, ParkerVision's POPR criticized this choice, so I subsequently submitted a simulation of a version of the circuit in which I used actual resistors instead of current sources. As I had predicted in my original expert declaration, this change did not materially affect my conclusions regarding the circuit.

B. Electrically Coupling the Information Signal

84. Dr. Ricketts disagrees with my assertion that in Macnally, (1) the RFP input (shown in blue below above) is the information signal that is "electrically

coupled” to capacitor C1 through first switching device M5, and (1) the RFN input (shown in orange) in the inverted information signal that is “electrically coupled” to capacitor C2 through second switching device M8. EX2021, ¶¶446-447.



85. The question, however, is not whether an information and inverted information signal is electrically coupled to the capacitor; rather, it is “what is an information signal and inverted information signal?” Claim 18 of the ’342 patent describes a “method for down-converting an electromagnetic signal, comprising the steps of: (1) receiving an information signal; (2) inverting the information signal to generate an inverted information signal ...” Therefore, it distinguishes between the “electromagnetic signal,” i.e., the “RF input signal itself” as Dr. Ricketts calls it, and the “information signal” and the “inverted information signal.” See EX2021, ¶212. Thus, the claim does not require that the transferred energy comes “from sampled energy of the RF input signal itself,” as Dr. Ricketts claims. See EX2021, ¶212.

86. A POSITA would understand that the information signal applied at the gate-side of M1 and M2 is essentially the same information signal on the drain current flowing through M1 and M2. The RF_P input signal causes M1 to behave like a variable current source, which consequently causes the otherwise constant bias current through M1 to vary in proportion to the RF_P input signal. Same for RF_N and M2, the inverted information signal. Thus, the information and inverted information carried by the RF_P and RF_N inputs are translated to the current flowing in the mixer. But the information is preserved. Pet. 61-62. I note that Dr. Ricketts admits that Macnally uses a 50% duty cycle LO, which is a non-negligible aperture. EX2021, ¶216. Thus, Macnally transfers non-negligible amounts of energy from the information signal to the capacitors. Additionally, in both my first and second declarations, all of the LO signals use a 50% duty cycle signal, which is a non-negligible aperture necessary to perform energy transfer. See TI-1001, 11:3-12, 38-42.

87. In the Macnally circuit, the information signal is the non-bias component of the drain current of transistor M1 and the inverted information signal is the non-bias component drain current of transistor M2. Therefore, the fact that some of the energy used to create the information signal and inverted information signal comes from the power supply is not relevant to Claim 18 and its dependent claims.

88. Furthermore, if Dr. Ricketts' assertion were correct, it would imply that any receiver which uses a low noise amplifier (LNA) prior to circuitry that otherwise satisfies the requirements of Claim 18 cannot infringe the '342 patent. Yet, nearly all wireless receivers use LNAs, including the TI's receivers that ParkerVision alleges infringe on the '342 patent.

89. Dr. Ricketts claims that the M1 and M2 transistors do not themselves supply current to the capacitors. EX2021, ¶458. As I have explained above, the drain current of M1 is the information signal plus a constant bias component, and the drain current of M2 is the inverted information signal plus a constant bias current. A POSITA would recognize that the information signal and the inverted information signal are currents that can take on positive and negative values. The '342 patent also acknowledges this concept. For example, it describes an embodiment in which "the information signal is combined with a bias signal to create the reference signal" (Column 2, Lines 35-36), so in the context of the Macnally circuit the "reference signal" would be the drain current of M2.

90. Therefore, the information signal and the inverted information signal do in fact satisfy ParkerVision's preferred interpretation of "*electrically coupling* the information signal to a first capacitor and the inverted information signal to a second capacitor."

91. Note that Dr. Ricketts did not provide a construction for the term

“information signal.” As I discussed above, the ’342 patent contemplates the information signal is a term that is used for a signal before and after amplification by an LNA and/or filtering. *E.g.*, ’342 patent, 49:37-46.

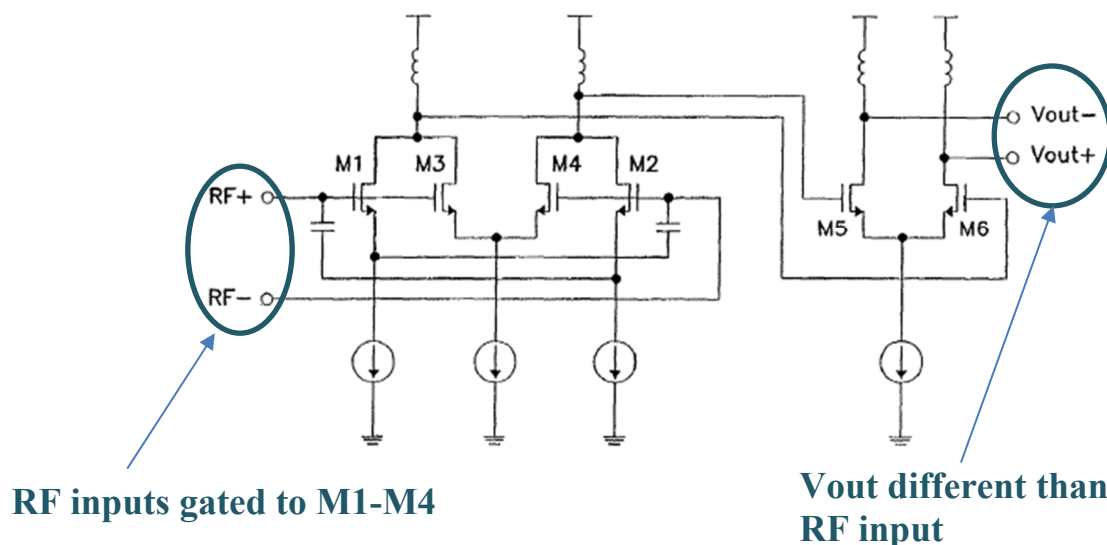
92. Importantly, ParkerVision does not propose any construction for “information signal,” despite relying on an interpretation of it when discussing Macnally. The term “information signal” is broad. Contrary to Dr. Rickett’s argument, there is no requirement in the claims or the specification that the information signal be the same signal as the received EM input signal. *E.g.*, EX2021, ¶212. Quite the opposite: the ’342 patent clearly states that the information signal “may be *amplified using a low-noise amplifier and/or filtered* after it is received.” ’342 Patent, 49:37-42 (emphasis added). The ’342 patent refers to the “RF information signal” both before and after the signal passes through the low-noise amplifier (LNA). TI-1001, 49:29-46:

In step 6202, a RF information signal is received. The RF signal can be received by any known means, for example, using an antenna or a cable. In embodiments, the RF signal may be amplified using a low-noise amplifier and/or filtered 40 after it is received. These steps, however, are not required in accordance with method 6200.

In step 6204, the received RF information signal is electrically coupled to a capacitor. For the receiver shown in FIG. 16O, the RF signal is electrically coupled to the carrier(+) 45 port of receiver 1602 and capacitor 1604. When used herein, the phrase “A is electrically coupled to B” does not foreclose the possibility that there may be other components physically between A and B. For receiver 1602, the received RF signal is

The '342 patent uses the same term to describe two different signals. Thus, there is no requirement in the '342 patent or claim 18 that the information signal that is electrically coupled to the capacitor be the same signal as the RF input signal.

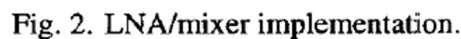
93. A POSITA would have recognized that the output signal from an LNA is a different signal than the signal input to the LNA. For example, Macnally provides an example circuit schematic for an LNA:



Macnally, FIG. 2 (annotated)

See also, id., 2:22-23 (“FIG. 2 illustrates the low noise amplifier according to the present invention;”), 6:57-64 (describing that the LNA 138 “employs a capacitively cross-coupled input pair, M1 and M2, that provides both gain and impedance matching in parallel with a differential pair, M3 and M4, for additional gain”). As can be seen, the LNA receives the RF input signal at gates of M1-M4,

94. As another example, Razavi's LNA has an RF input signal and outputs an amplified signal with power provided by the power supply:



95. Claim 18 of the '342 patent describes a “method for down-converting an electromagnetic signal, comprising the steps of: (1) receiving an information signal; (2) inverting the information signal to generate an inverted information signal” There is no requirement in the claims that the claimed information

signal be the same signal as the RF input signal, as Dr. Ricketts calls it. *See* EX2021, ¶212; *e.g.*, TI-1001, 49:37-46 (describing that the RF information signal is amplified by an LNA and is then electrically coupled to the capacitor, meaning that a different signal is received than is what is coupled to the capacitor). So the claim does not require that the transferred energy comes “from sampled energy of the RF input signal itself.” *See* EX2021, ¶212. In the Macnally circuit, the information signal is the non-bias component of the drain current of transistor M1 and the inverted information signal is the non-bias component drain current of transistor M2. Therefore, the fact that the energy used to create the information signal and inverted information signal comes largely from the power supply is not relevant to Claim 18 and its dependent claims.

96. Furthermore, if Dr. Ricketts’ assertion that the transferred energy must come “from sampled energy of the RF input signal itself” were correct, it would imply that any receiver that uses a LNA prior to the claimed down-conversion circuitry that otherwise satisfies the requirements of Claim 18 **cannot** infringe the ’342 patent. *See* EX2021, ¶ 212. I suspect that this is why Dr. Ricketts did not argue that outputs of the LNAs in the Macnally and Razavi circuits are distinct from the “information signal” even though his own (incorrect) reasoning would have led to this conclusion; making such an argument would not have been in the ParkerVision’s interest as nearly all wireless receivers incorporate LNAs

prior to frequency down-conversion. But it is not reasonable, or honest, for Dr. Ricketts to selectively apply his reasoning only when it supports the ParkerVision's interests and conveniently ignore his own reasoning when it leads to conclusions that are not in the ParkerVision's interests.

C. Macnally's Current Flow

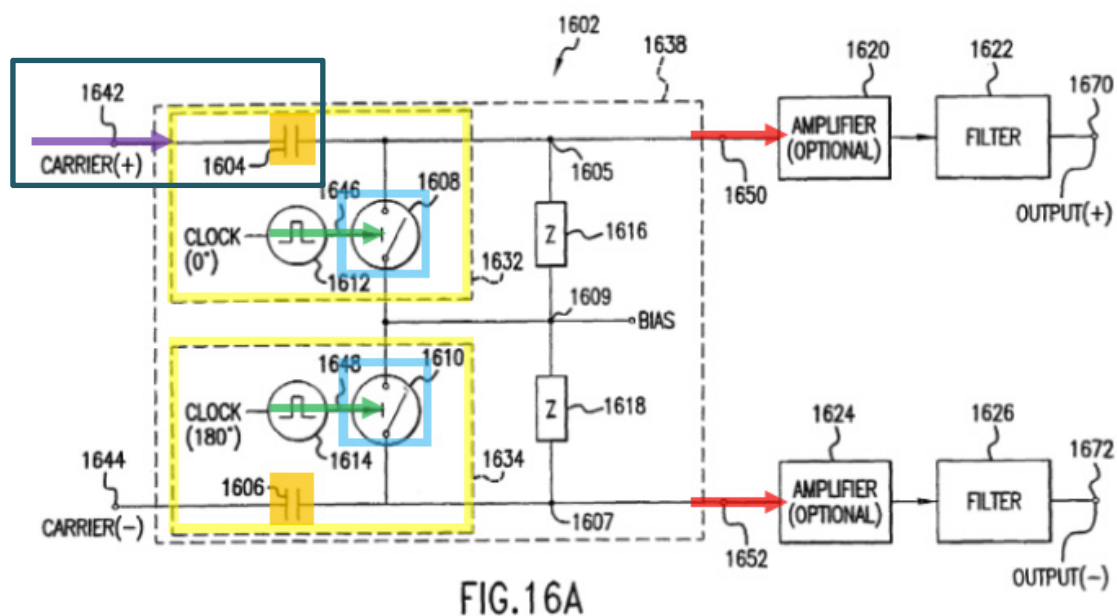
97. Dr. Ricketts' assertion that "the current flowing from the power source to ground must be direct current (DC)," which is "the non-time varying (non-RF) current that provides the bias and operating points for M5, M6 and M7, M8," makes no sense in the context of Macnally's mixer. EX2021, ¶217. A POSITA knows that a DC current is a constant current by definition, and if the current flowing from the power supply (though resistors R3 and R4 in the Macnally mixer) were really a DC current, then the output voltages of the mixer would be constant. In this case, no signal would ever get to the antialias filter, so the receiver would not function.

98. Dr. Ricketts' assertion that "no current flows from the gate into the drain" is not correct. EX2021, ¶222. All MOS transistors have a non-zero gate-to-drain capacitance, as well as the gate-to-source capacitance, which Dr. Ricketts mentioned (and there is no way he would not know this). EX2021, FN8, ¶¶221, 62. Therefore, some current actually does flow from the gate to the drain of transistor M1, and the same is true of transistor M2. So while I do not agree that it

is necessary for the information signal to contain energy from the EM input signal, this capacitance nevertheless implies that the information signal does in fact contain some energy from the EM input signal.

D. Switches opening/closing

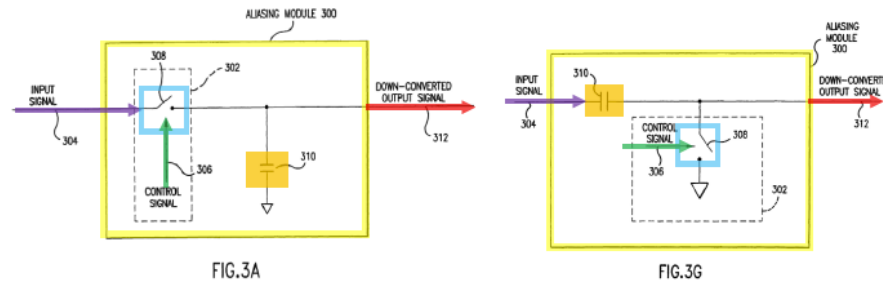
99. Dr. Ricketts argues, “If transistor M5 or M8 operated as switches in a sampling system, turning them OFF would isolate the capacitor from the signal path” EX2021, ¶464. The ’342 patent, however, describes an embodiment of the invention where an input signal is coupled to the capacitor directly:



EX2021, ¶¶144-146 (’342 patent, FIG. 16A ([annotated](#)))

In FIG. 16A, the switch 1608 is connected downstream and in parallel to the capacitor 1604. Dr. Ricketts describes that capacitors 1604 and 1606 (orange) and switching devices 1608 and 1614 (blue) “operate under the control of an aperture

generator 1612, 1614, respectively.” EX2021, ¶146. Likewise, Dr. Ricketts cites FIG. 3G, which shows a similar design:



EX2021, ¶140 (citing '342 patent, FIGS. 3A & 3G)

Both FIGS. 3G and 16A show the switch downstream and in parallel to the capacitor. If Dr. Ricketts interpretations were correct, then it would exclude preferred embodiments of the patent. Note that Dr. Ricketts discussion of Macnally contradicts his discussion of the '342 patent. Dr. Ricketts states that “the configurations of Figures 3A/3G will operate in the same way.” EX2021, ¶143.

100. Although his explanation does not make this explicit, perhaps Dr. Ricketts is referring to the fact that shortly after M5 and M8 turn off (which is only possible because they act as switches!) transistors M6 and M7 turn on and vice versa. When M5 is on, the information signal is coupled to the red-highlighted capacitor in the annotated copy of Macnally Fig. 3 below, and when M7 is on, the inverted information signal is coupled to that capacitor. Similarly, when M8 is on, the inverted information signal is coupled to the blue-highlighted capacitor in the annotated copy of Macnally Fig. 3 below, and when M6 is turned on, the (non-

[illegible]

V. Macnally Simulations

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depends strongly on R3 and R4), so the simulation results imply that the resistor values were chosen correctly. If necessary, I can provide an explanation of the method by which I chose the specific values, but the method is something that a POSITA would know as it is just a standard design method, so I did not feel it was necessary to include it in my supplemental declaration.

103. It is true that the Macnally patent does not mention the 8.5 mS value, but Macnally published exactly the same circuit in the 1999 IEEE International Solid State Circuits Conference, and the 8.5 mS value is mentioned in that conference paper. TI-1050, 228-229, 464; EX2021, ¶382. Specifically, it is listed in Table 13.7.1 of the paper:

Complete RX (including duplexer and filters)	NF	8.1dB (SSB)
	iIP3	-4dBm
	iCP	-16dBm
	Overall gain	+101dB
LNA	Blocking	+6dBm at 915MHz (w. c.)
	Gain	+15.3dB, -3.7dB
	NF	1.9dB
Mixer	Conv. gm	8.5mS
	NF	15.6dB (SSB)
IF-Amp	Gain	-20.9 .. +58dB (2dB steps)
	NF	3.8dB
Demodulator	Image suppr.	>43dB ($\Delta\phi < 1^\circ$)
	Gain	16dB
Baseband Filters	Type	Bessel 4th Ord. active RC
	Cut-off freq.	150kHz
	Gain	15.7dB
Modulator	Output power	-17dBm
	LO suppr.	>50dB
	Image suppr.	>31dB
Pre-amp	RMS phase err.	1.6°
	Output power	+3dBm
	Gain	21dB
	oCP	+5.4dBm

Table 13.7.1: Measured transceiver characteristics.

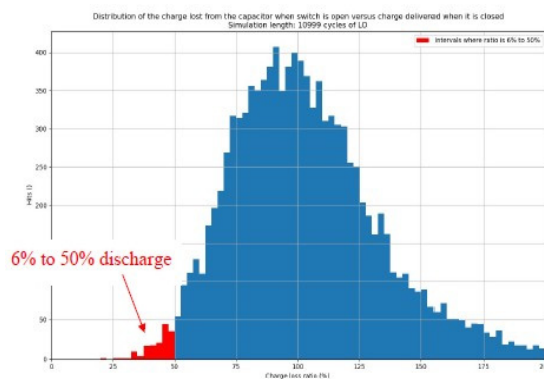
104. The line that starts with “Mixer” contains “Conv. Gm 8.5mS” where “Conv.” stands for “conversion” and “gm” is a standard symbol for “transconductance.”

105. It is also true that the Macnally patent does not mention “cross-conducting,” but this is a standard term that a POSITA would know. In the case of the Macnally mixer circuit, cross-conducting is said to occur if transistors M5, M6, M7, and M8 happen to simultaneously conduct current, and a POSITA would understand that such cross-conducting is highly undesirable because it shorts the output of the mixer and reduces the mixer’s gain. EX2021, ¶382.

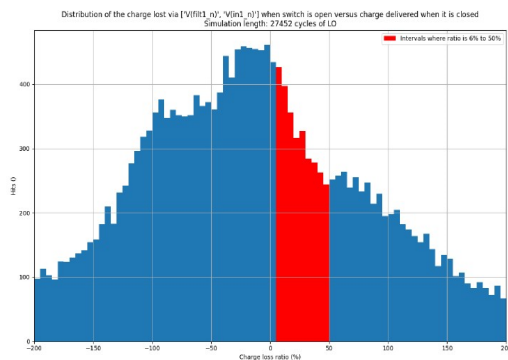
106. Therefore, Dr. Ricketts criticism might seem reasonable at face value, but it is not reasonable. Moreover, it is not consistent with several of his prior criticisms. For example, he complained that I did not explain how I chose the values of R3 and R4, but the Macnally patent does not explain how they were chosen either. EX2021, ¶381. Therefore, if I had provided an explanation of the standard design process by which I chose the values of R3 and R4, I suspect that Dr. Ricketts would have criticized me for applying a design process that was not mentioned in the Macnally patent, while conveniently ignoring the fact that the design process would be familiar to a POSITA. In the case of the cross-conducting issue, I happened to mention it and that I used the standard design process of adjusting the local oscillator cross-over point to avoid it, and this time he is complaining that I provided extra information about the design process that the Macnally patent happens not to have mentioned (just like the Macnally patent happens not to have mentioned how R3 and R4 were chosen). EX2021, ¶382.

A. Macnally Histograms

107. Dr. Ricketts misinterprets the resulting data and misrepresents my statements about them. For the following histograms, Dr. Ricketts complains, “MACNALLY-SIM-FIGS. 2.1, 3.1, 4.1A and 4.1B show the same simulation output from MACNALLY-SIM-FIG. 1.1 as MACNALLY-SIM-FIGS. 2, 3, 4, 5 and 6 show from MACNALLY-SIM-FIG. 1” as if I meant that nothing has changed in my supplemental simulations. However, I have made clear that my supplemental simulations do not represent “a new and distinct theory,” as alleged by Dr. Ricketts. In fact, I have consistently represented that: “The conclusions in my original Declaration regarding the claims... are likewise supported.” EX2021, ¶390 (quoting TI-1042, ¶146).



MACNALLY-SIM-FIG. 4 (annotated)



MACNALLY-SIM-FIG. 4.1A. Charge loss ratio percentages histogram for capacitor C6 (circuit of MACNALLY-SIM-FIG. 1.1).

EX2021, ¶389

As is clear from the wording, what I meant is that the results shown in MACNALLY-SIM-FIGS. 2.1, 3.1, 4.1A and 4.1B *correspond* to those shown in

MACNALLY-SIM-FIGS. 2, 3, 4, 5 and 6 except that the former were generated by simulating MACNALLYSIM-FIG. 1.1 and the latter were generated by simulating MACNALLY-SIM-FIG. 1.

108. But more importantly, BOTH sets of histograms reveal that, regardless of the operational parameters used for the simulations, the Macnally circuit produces a non-zero set of results for the claimed percentages.

109. As I stated previously, I stand by the original set of circuit modeling and simulations for both DeMaw and Macnally. I provided further sets of simulations only in an effort to quiet allegations of cherry-picking data. Every simulation I have run, shows that the circuits exhibit the claimed behavior. This not only shows that the Macnally circuit operates the same way as the '342 patent claims, but it shows that I did not cherry-pick self-serving simulation parameters.

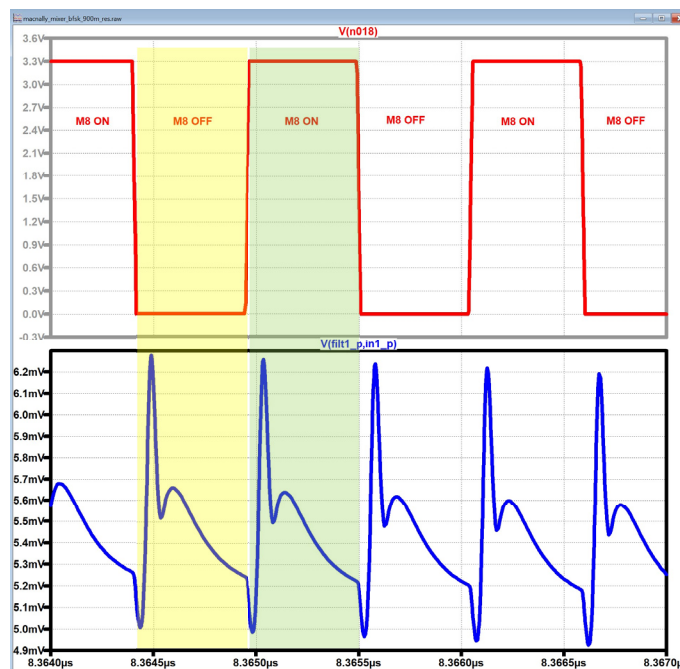
110. It is true that the design choice differences do affect the various waveforms—though immaterially with respect to the '342 claims—but this does not amount to a “new and distinct theory of how Macnally allegedly operates.” Dr. Ricketts has not provided any evidence to the contrary. Simply enumerating design differences and pointing out the obvious consequence that the design differences resulted in waveform differences in no way supports Dr. Ricketts’ “new and distinct theory” assertion. In reality, both versions of the circuit perform down-conversion in the same manner, and the differences in the various

waveforms do not change the conclusions that I reached in my original expert declaration as explained in my supplemental declaration (which I submit, since ParkerVision did not).

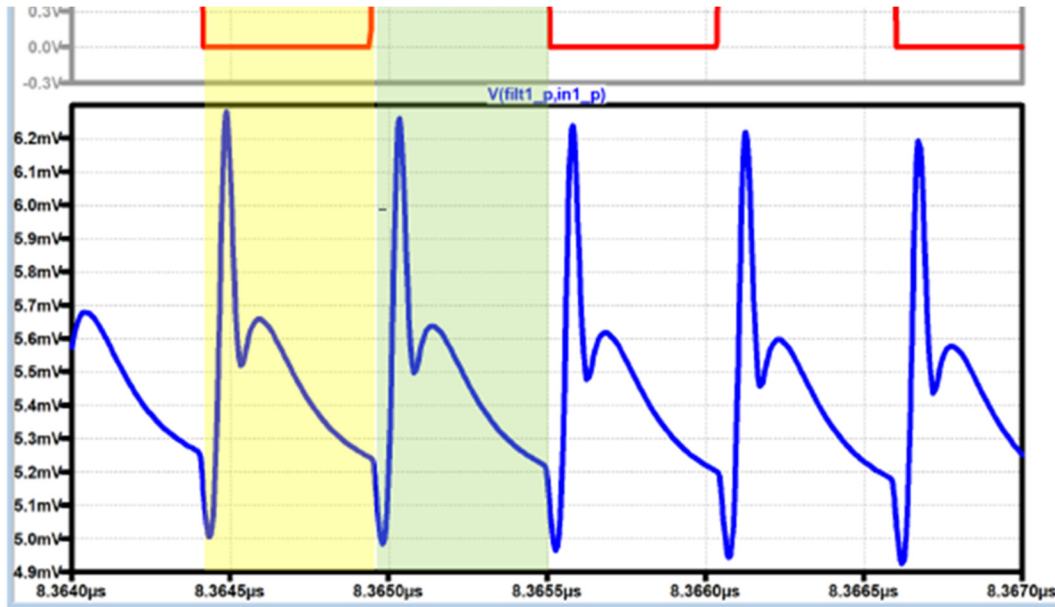
111. Confusingly, Dr. Ricketts says that I provided “no waveforms for charge and discharge of capacitors—only Python-processed calculations.”

EX2021, ¶392. But Dr. Ricketts has all of our simulation and post-processing files, so the waveforms that he claims were not provided to him actually were available to him.

112. Dr. Ricketts also states, “Transistor M8 turns on when the LO_p signal is high. The plot below shows both the LO_p signal and capacitor voltage (V_c). The charge on the capacitor remains materially the same whether M8 is ON or OFF”:



EX2021, ¶394.



EX2021, ¶394 (annotated).

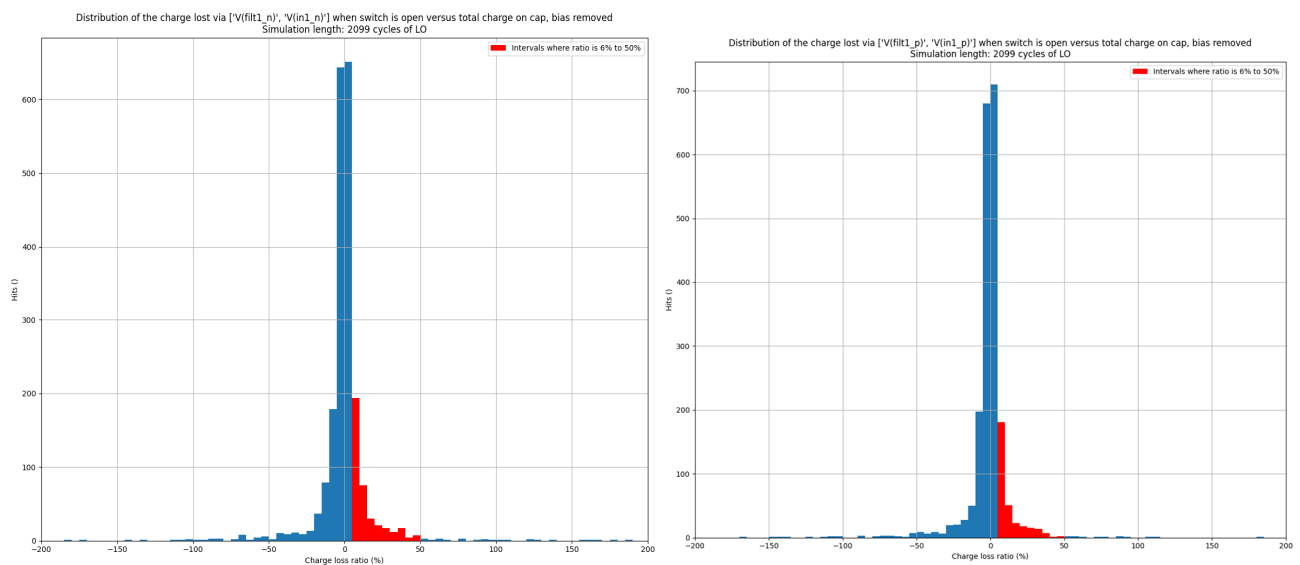
If it were true that the “charge on the capacitor remains materially the same in both phases,” then the circuit would not function as a mixer. Yet, the simulation results I presented in both my original expert declaration and my supplementary expert declaration clearly demonstrate that the circuit functions as a mixer. Indeed, a close comparison of the yellow and green regions in the bottom plot above reveals that the average of the waveform over the yellow region is higher than that over the green region. This difference corresponds to the down-converted signal, so it absolutely is a material difference. The difference may appear small because the bandwidth of the down-converted signal, and therefore its rate of change, is several hundred times lower than the local oscillator signal frequency, but this does not make it insignificant. Also, Dr. Ricketts’s plots are misleading because they do not

reveal the percentages of discharge under his understanding of the claims nor mine. By contrast, I have provided histograms that show that under either interpretation of how discharge percentages are calculated, and under various operating parameters, Macnally's capacitors discharge the claimed percentages.

113. It is not clear to me what point Dr. Ricketts is trying to make in Paragraphs 396-398. Nothing in those paragraphs contradicts the results I presented in my expert declaration or my supplementary expert declaration.

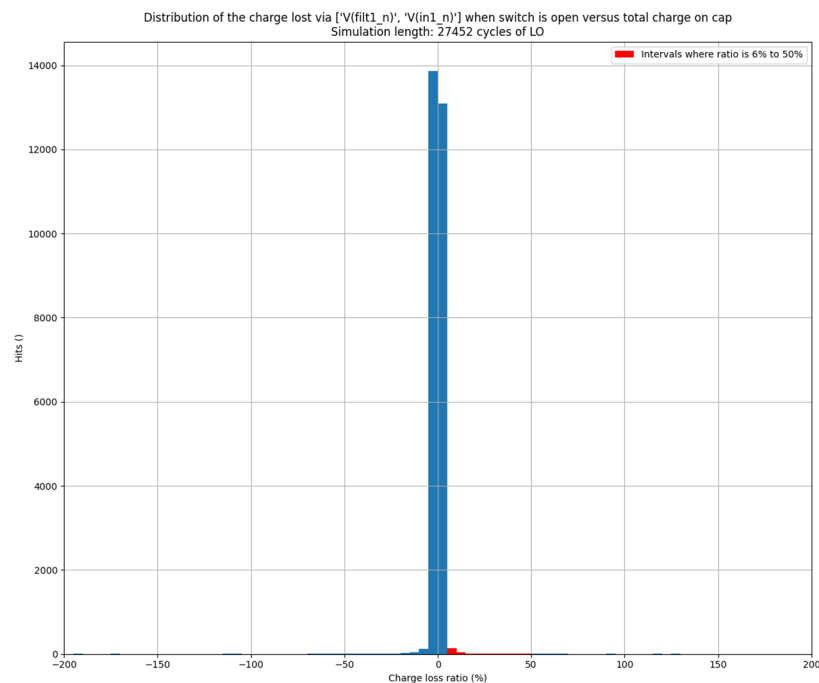
B. Macnally Renders Obvious the Claimed Discharge Percentages

114. I refer back to my discussion in Section III.D (DeMaw Renders Obvious the Claimed Discharge Percentages) for the Python code I used to calculate the discharge percentages under Dr. Ricketts's interpretations of the claims.

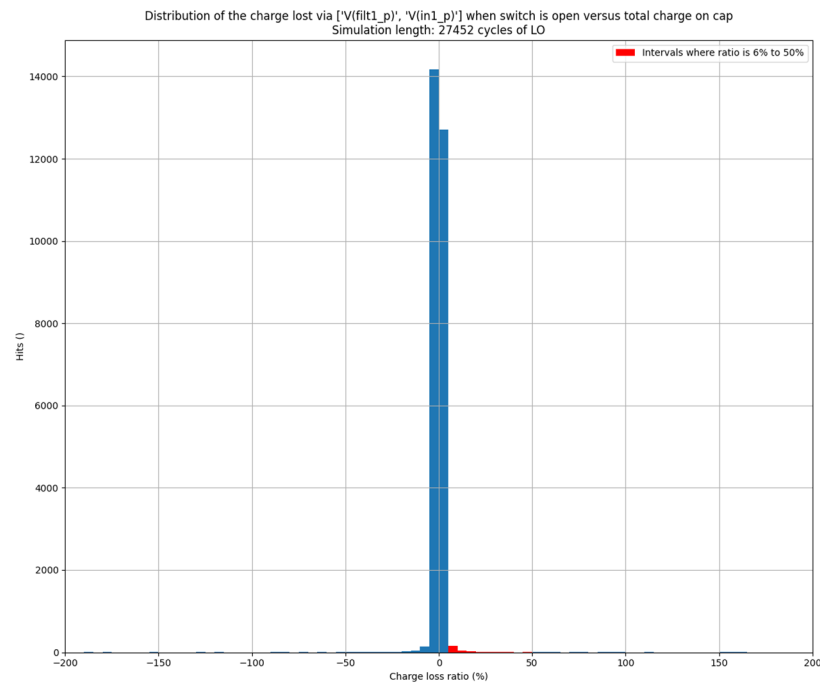


Macnally Histograms for C6 and C7 Under Original Operating Conditions

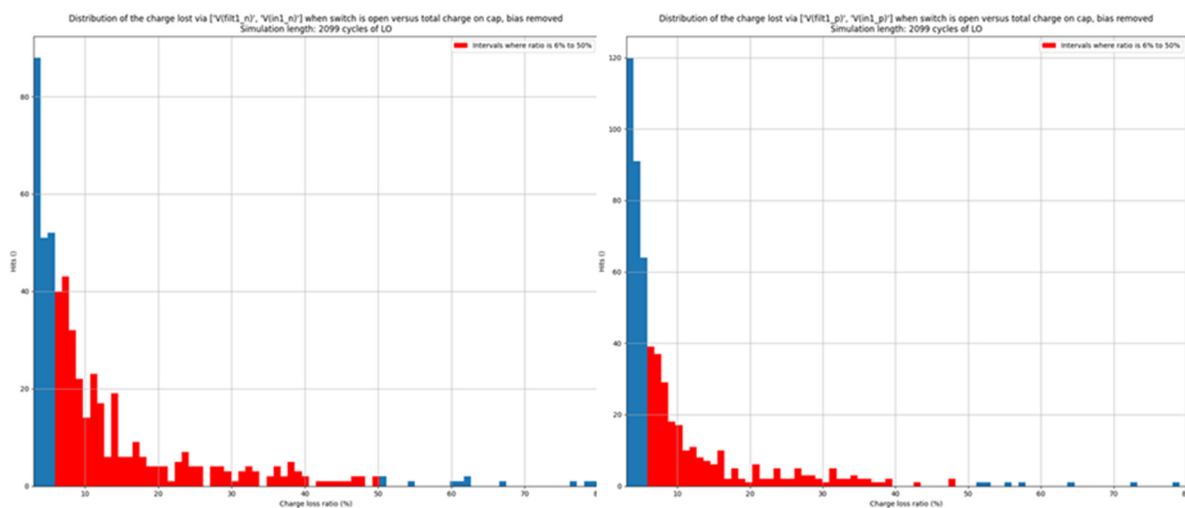
115. Below are histograms obtained by simply post-processing the Macnally circuit simulation described in Section VII of my supplementary expert declaration with com.py modified as shown above. As can be seen from the histograms, both still cover the claimed percentage discharge ranges between 6% and 50% (shown in red). The number of histogram occurrences per bin in the 6% to 50% region is relatively small, but not zero, so it meets the requirements of Claims 19-21. Moreover, if longer simulations were run, the number of occurrences per bin would increase over the whole of both histograms.



MACNALLY-SIM-FIG. 4.1A. Post-processed charge loss ratio percentages histogram for capacitor C6 (circuit of MACNALLY-SIM-FIG. 1.1).



MACNALLY-SIM-FIG. 4.1B. Post-processed charge loss ratio percentages histogram for capacitor C7 (circuit of MACNALLY-SIM-FIG. 1.1).



Close-up views

116. Therefore, if I use Dr. Ricketts' interpretation of discharge percentage

exactly, the Macnally circuit nevertheless satisfies the requirements of Claims 18-21 as demonstrated above. As I similarly demonstrate above, the DeMaw circuit satisfies the requirements of Claims 18-21 if I use Dr. Ricketts' interpretation of discharge percentages, although for the reasons I described in Section III.C.3, it is necessary to omit the constant bias charge on the capacitors in the calculation.

117. Dr. Ricketts states that the capacitor charges rather than discharges in several instances when the switch is off. EX2021, ¶425. This is true, but it is not relevant to either Dr. Ricketts' or my interpretation of Claims 18-21.

C. Transistor Dimensions Updated

118. Dr. Ricketts criticized my revised simulation for being inconsistent because I used a gate length of 600 nm for transistors M8–M11 in the revised simulation but 300 nm gate lengths originally. EX2021, ¶385. In addition, Dr. Ricketts claimed that this inconsistency would materially affect parasitic capacitance, gain, and switching behavior. EX2021, ¶385.

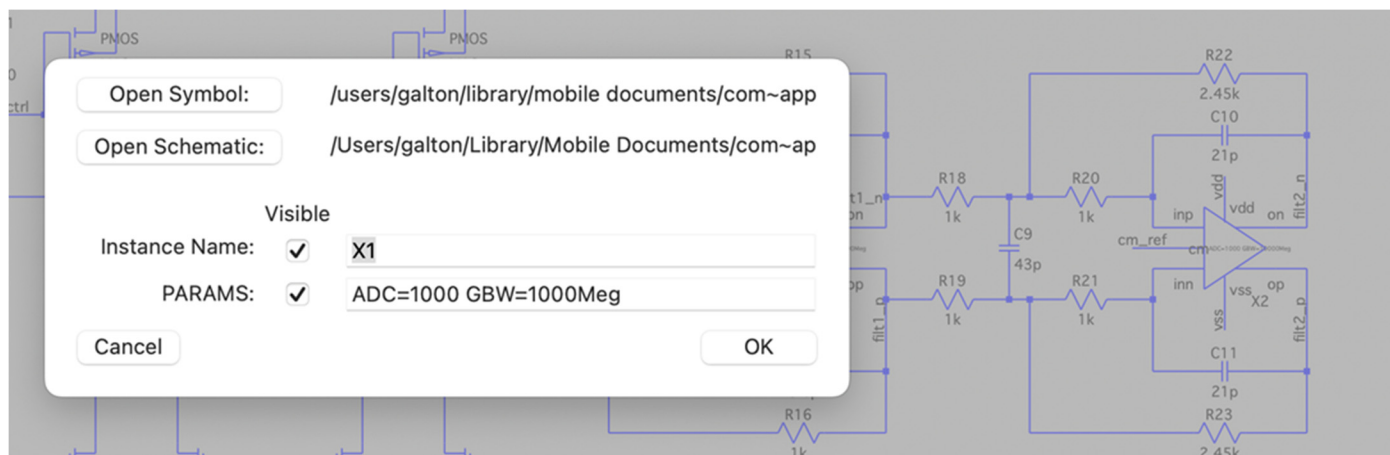
119. The use of 300 nm gate lengths in the original simulations was indeed inadvertent on my part. However, as demonstrated by the subsequent simulation results I submitted, correcting the mistake did not lead to a different conclusion than I presented in my original declaration.

120. Both the initial simulation results and the latter simulation results lead to the same overall conclusion that the Macnally circuit is an embodiment of the

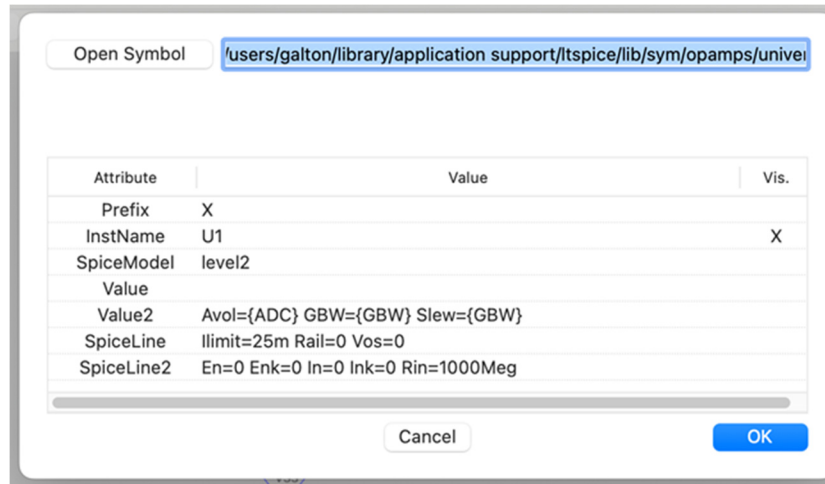
alleged invention of the '342 patent, so the “inconsistency” does not “materially” impact the switching behavior as Dr. Ricketts claimed.

D. Op-Amp Model

121. Dr. Ricketts claimed that the operational amplifier component (universalopamp2) used in my simulation lacked any specified parameter values, so he could not verify whether the op-amp model achieved 60dB of gain. EX2021, ¶¶373-374. However, it appears that Dr. Ricketts did not query the LTSpice simulator correctly, or else there is a problem with his installation of LTSpice. The universalopamp2 component receives its component values from the schematic view of the circuit. Right clicking on the op-amp symbol on the schematic view shows:



Then clicking the “Open Schematic” button on the dialog box followed by right clicking one of the non-differential op-amp symbols shows:



122. This demonstrates that the values Dr. Ricketts thought were not specified actually were specified. As the parameters would have been available to Dr. Ricketts had he queried the simulator correctly, Dr. Ricketts' conclusion above is invalid.

E. Op-Amp Topology Changed

123. Dr. Ricketts further claimed that I used differential macro-model operational amplifiers in my original simulation but replaced them with single-ended op-amps. EX2021, ¶386.

124. I have no idea why Dr. Ricketts is making this assertion. The same op-amp model was used for all of the Macnally simulations. In all the Macnally simulations, each op-amp is a fully-differential op-amp macromodel that incorporates two single-ended op-amp macromodels to achieve fully-differential operation. Dr. Ricketts has access to every simulation file we used; he simply needs to look at the details of the op-amp micromodel we used to see that it is

fully-differential.

F. Transconductance

125. Dr. Ricketts faults my revised simulation for changing the transistor sizes to achieve a transconductance value that is only “allegedly ‘described’” in Macnally. EX2021, ¶387.

126. Macnally does indeed specify the mixer transconductance as I have explained above. More generally, of course the transistor sizes in the revised simulations are different from those in the original simulation. The ParkerVision POPR, presumably on the advice of Dr. Ricketts, complained that some of my design choices for the Macnally circuit version that I simulated originally, e.g., the use of current sources instead of large resistors, did not perfectly match those described in Macnally. Though a POSITA would recognize that the differences would not lead to fundamentally different circuit behavior, and though I believe that the differences are most likely what Macnally actually implemented, I modified the circuit to fully match the circuit diagram and description in both the Macnally patent and in response to the criticism in the POPR. *See* TI-1050, 228-229, 464. This required several adjustments to the transistor sizes. Yet, as demonstrated by every simulation I have run, the simulation results clearly demonstrate that the Macnally circuit satisfies claims 18-21 of the ’342 patent.

127. Despite Dr. Ricketts’s assertions to the contrary, the variations in

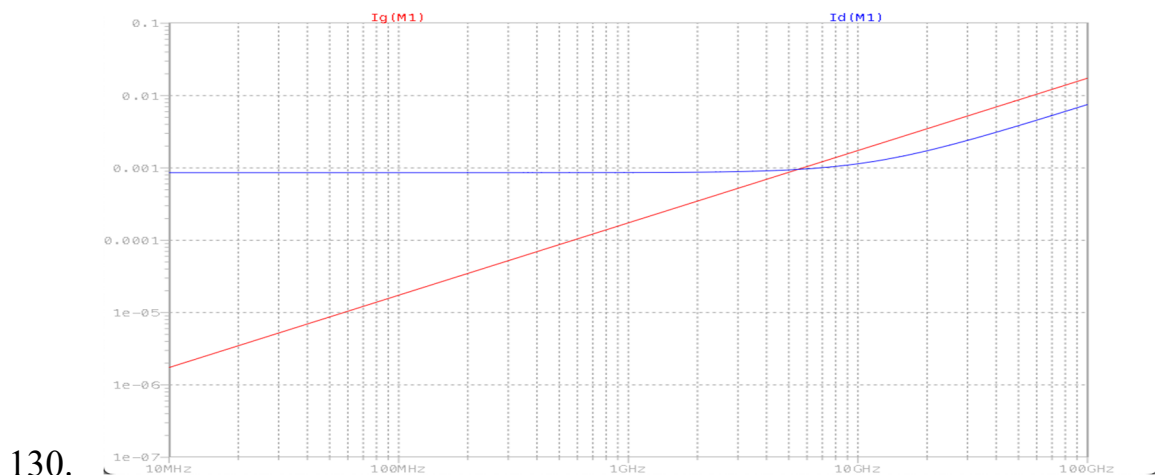
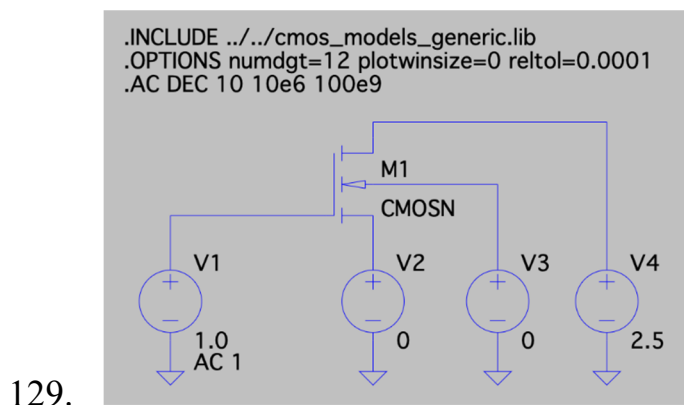
circuit operational parameters do not change the fundamental manner in which the circuit operates, and it is absurd to argue that they “collectively represent a new theory of how Macnally allegedly operates.”⁴ As I have explained above, most papers, textbooks, and patents do not give any component values at all, and the designer is expected to choose the values as needed for each given application. And even when they do provide component values, it is understood that designers are likely to modify those values as needed for a given application. For example, the ‘342 patent mentions some component values for some of the alleged invention embodiments it presents, yet if a designer at another company were to use one of those embodiments without a license but change some of the component values, I have no doubt that ParkerVision would allege that the other company infringed on the ‘342 patent despite the component changes.

G. Parasitic Capacitance

128. Dr. Ricketts ignores realistic JFET switching behavior, but comments on a lack of realism elsewhere. For example, Dr. Ricketts complains about

⁴ The changes, at best, affect the details of the various current and voltage waveforms; but they do not alter the fundamental operation of the circuit, generally, or the specific discharge percentages, specifically, as shown in the totality of my simulations.

missing parasitic capacitances. EX2021, ¶375. This would be a valid criticism if it were true, but it is not true. By “device parasitic capacitances,” Dr. Ricketts is referring to the parasitic capacitances associated with the MOS transistors. TI-1049, 763. I have no idea how Dr. Ricketts reached the conclusion that our MOS transistor models do not include parasitic capacitances, but the following LTSpice AC simulation of a single MOS transistor (using the same transistor model we used previously) clearly demonstrates that the MOS transistor model includes parasitic capacitances:



131. The top image above shows the circuit that was simulated for this

demonstration, and the bottom image shows plots of the simulated gate current, $I_g(M1)$, and the simulated drain current, $I_d(M1)$, as a function of frequency, where $V1$ is the AC input voltage source and the other voltage sources are held constant. The $V4$ source is at a high-enough voltage to ensure that the transistor ($M1$) is in saturation. The gate current increases with frequency, meaning that the transistor model includes gate capacitance (which is the combination of multiple parasitic capacitances). TI-1049, 763. The drain current includes a constant transconductance current component and it also includes a non-constant component corresponding to gate-drain parasitic capacitance. The latter increases with frequency, but the vertical axis of the plot is on a log scale, so the increase only becomes clearly visible on the plot once the current through the gate-drain parasitic capacitance gets large enough that it is at least comparable to the transconductance current magnitude. If device parasitic capacitances were not modeled, then the simulated gate current would be zero and the simulated drain current would be non-zero, but constant, which clearly is not the case. This demonstrates that the parasitic device capacitances are indeed modeled in our simulations, despite Dr. Ricketts' puzzling and unsupported assertion to the contrary. EX2021, ¶375.

VI. Other Rebuttal Topics

A. Dr. Ricketts's DeMaw Simulations Are Flawed

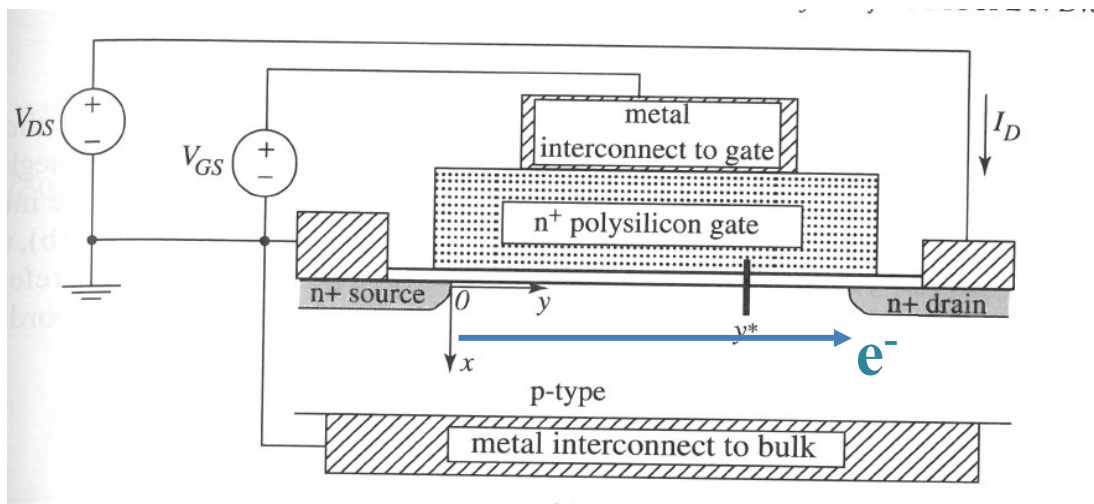
132. Dr. Ricketts provided a few of his own data and plots for the DeMaw circuit. But his data is flawed. First, as I have discussed above, Dr. Ricketts uses the incorrect methodology for determining the claimed discharge percentages by failing to account for the effects of the bias voltage on the calculation of the discharge percentages. Second, Dr. Ricketts provided tabulated discharge percentages over a 2 μ s window over which to compute his interpretation of the discharge percentages. This is a very disingenuous thing to do, especially since Dr. Ricketts claims to have used my data, yet he only picks a very small window that amounts to a statistically insignificant amount. By contrast, I provided data for a 400 μ s time window, which is statistically more significant. And during the longer window, we do see the claimed discharge percentages, which is sufficient to show that DeMaw and Macnally perform within the claimed discharge percentages.

B. JFET Current Behavior

133. Dr. Ricketts assertion that “no current flows from the gate into the drain” is not correct. EX2021, ¶222. All MOS transistors have a non-zero gate-to-drain capacitance as well as the gate-to-source capacitance that Dr. Ricketts mentioned (and there is no way he would not know this). EX2021, ¶222. Therefore, some current actually does flow from the gate to the drain of transistor M1, and the same is true of transistor M2. So while I do not agree that it is

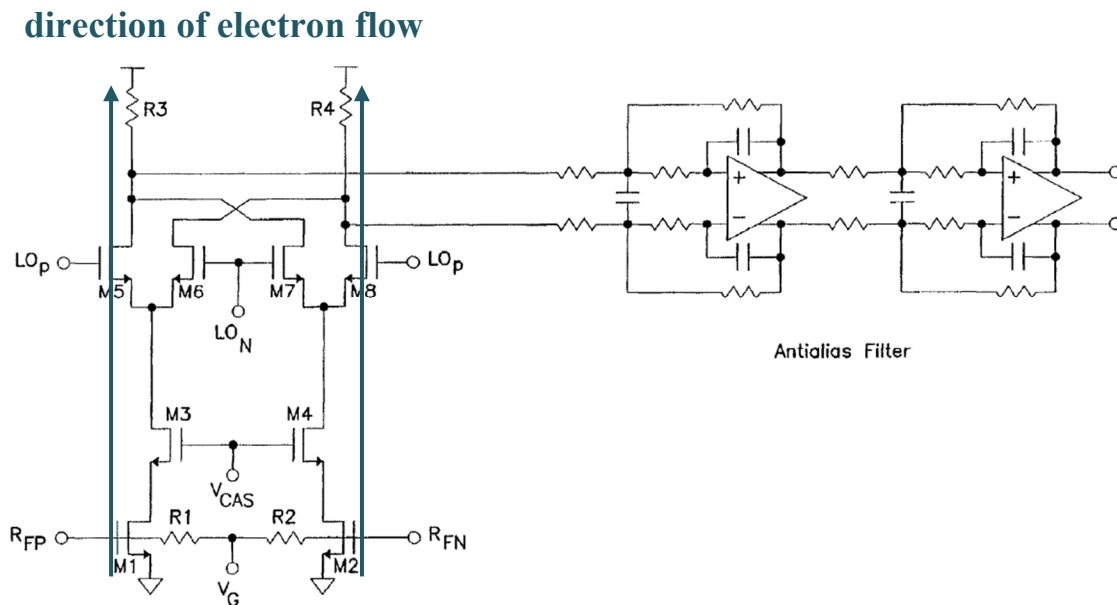
necessary for the information signal to contain energy from the EM input signal, this capacitance nevertheless implies that the information signal does in fact contain some energy from the EM input signal.

134. Dr. Ricketts assertion that “the current remains unidirectional—always flowing downward to ground” is an absurd argument and is based on a fallacy. EX2021, ¶225. Dr. Ricketts acknowledges that current is the flow of electrons, which is correct, but his conclusions about current flow imply that electrons flow through a circuit from the positive power supply terminal to ground, which is not correct. For example, in the nMOS transistor in EX2021, ¶57, its drain terminal connected to a positive power supply voltage and its source terminal connected to ground, and Paragraph 57 claims in reference to the figure that “The electron flow (current) from the drain (D) to the source (S) is controlled by the voltage at the gate (G).”



This is incorrect; in reality, the electron flow is from the source to the drain.

Electrons are negatively charged, so they flow toward the positive supply voltage, not toward ground. Dr. Ricketts's argument presented in Paragraphs 222-225 that current can only flow downward towards ground ignores the fact that electrons actually flow upward through transistors M1–M8 and resistors R3 and R4 toward the positive power supply terminal:



Macnally, FIG. 3 (annotated)

135. A reasonable question then, is how could Dr. Ricketts not know that electrons flow through a circuit toward the positive power supply terminal? He almost certainly does know this, but he has taken advantage of the definition of “conventional current,” so named because it is based on the artificial *convention*

that the direction of current flow is from high to low voltages. In this convention, the *value* of the current resulting from the flow of electrons through a conductor is *defined* to be the *negative* of the rate at which electrons pass through the conductor. The convention originated as the result of a mistake made by Benjamin Franklin in the 18th century. As explained in the *Basic Electric Circuit Analysis* textbook, “This convention stems from Benjamin Franklin (1706–1790), who guessed that electricity traveled from positive to negative. We now know that in metal conductors the current is the movement of electrons that have been pulled loose from the orbits of atoms of the metal. Thus we should distinguish *conventional* current ([which can be thought of as] the movement of positive charges), which is used in electric network theory, and *electron* current.” TI-1047, 5. Hence, Dr. Ricketts has claimed that current flows toward the ground terminal in the Macnally mixer circuit simply because conventional current is *defined* to flow that direction for historical reasons. EX2021, ¶223. The claim might seem reasonable to a layperson, but a POSITA would understand that the flow of electrons, which is the actual current, is toward the positive power supply terminal, so Dr. Ricketts’s argument is extremely misleading, utter nonsense, and contrary to his own declaration. EX2021, ¶¶39-42.

C. Heterodyning

136. Dr. Ricketts’ comment that there “are significant disadvantages to

using mixers with continuously time-varying resistance (e.g., Gilbert cell analog multiplier),” is true but misleading. EX2021, ¶102. Mr. Barrie Gilbert invented the Gilbert cell analog multiplier, which would indeed have the disadvantage Dr. Ricketts mentioned if it were used as a mixer for RF down-conversion. However, Mr. Gilbert also invented the widely-used Gilbert mixer, and it is the Gilbert mixer, not the Gilbert analog multiplier, that is used for RF down-conversion in wireless receivers. The Gilbert mixer does not have the disadvantage that Dr. Ricketts mentioned because it performs multiplication by 1 or -1 at any given time depending on whether the local oscillator voltage is positive or negative at that time. TI-1045, 1412-23. For example, Gilbert’s article in *the IEEE Journal of Solid-State Circuits* refers to the mixer as “operating in an essentially binary (sign-switching) fashion.” TI-1045, 1413. As explained in detail in the tutorial review paper, local oscillators that drive RF down-converter mixers in wireless receivers are designed to be as close to square waves as possible, specifically so that the mixers will implement such binary multiplication. TI-1046, 1-19. This not only avoids the “continuously time-varying resistance” issue mentioned by Dr. Ricketts, but it also reduces the noise introduced by the mixer.

137. Perhaps the reason that Dr. Ricketts included the somewhat cryptic foot-note comment “I note that I am not stating that any mixer that multiplies is a non-linear mixer” as a footnote is that he is aware that a POSITA would know that

down-conversion mixers in wireless receivers ideally perform ± 1 multiplication as opposed to sinusoid multiplication. EX2021, ¶102 n.6. If so, it is disappointing as it would suggest that he is purposely confusing Gilbert mixers with Gilbert analog multipliers to give the appearance of supporting his narrative.

138. Dr. Ricketts also states that Macnally does not disclose the claim elements because it is a heterodyne system so the transistors remain active. EX2021, ¶442. This is not true. The Macnally patent states: “The LO input transistors [M5, M6, M7, and M8 in Fig. 3 of the Macnally patent] operate as switches.” TI-1021, 7:12-14. And a POSITA would understand from Macnally, FIG. 3 that each of transistors M5, M6, M7, and M8, turn off and on for nearly half of each local oscillator (LO) period.

D. Sampling

139. Dr. Ricketts states that there is a “contrast” between heterodyning and sampling-based down-conversion in that sampling-based down-conversion uses pulsed LO signals rather than continuous sinusoidal signals. EX2021, ¶108. As I explained above, local oscillators that drive RF down-conversion mixers in wireless receivers are designed to be as close to square waves as possible, specifically so that the mixers will implement ± 1 multiplication to the maximum extent possible. TI-1045, 14:12-23; TI-1046, 1-19. Hence, the “contrast” between the two cases Dr. Ricketts mentioned above does not exist in reality.

140. Dr. Ricketts claims, “If the capacitor did not continue to drive the low impedance load, there would be gaps in the output signal. As such, the energy transfer system would not work properly, and information would be lost.”

EX2012, ¶118. This is an absurd comment. In the scenario Dr. Ricketts described, the storage module is disconnected from the RF signal whenever the switch is off, so it does not have access to the input signal during the time intervals when the switch is off. In this sense, there are “gaps” in the output signal regardless of whether or not the storage element drives a load during these gaps.

E. Charging/Discharging Cycles

141. Dr. Ricketts states, “Petitioner’s construction requires that the charging/discharging cycles of both first and second capacitors are synchronized. That is not how the technology works.” EX2021, ¶189. This is a made-up issue by Dr. Ricketts. None of our arguments rely on whether or not “the charging/discharging cycles of both first and second capacitors are synchronized.”

142. Dr. Ricketts also claims that I did not point to any express disclosure in Macnally that describes the charging/discharging cycles of capacitors. EX2021, ¶443. However, the LO switches open and close, which affects the current that flows into the capacitors in the first stage of the antialias filter. Therefore, Macnally does implement charging/discharging cycles of the capacitors in accordance with Claim 18, despite Dr. Ricketts’ evidence-free claim to the

contrary. Furthermore, as a POSITA would understand, the mixer would not function otherwise.

143. Dr. Ricketts stated that a POSITA would readily understand the term “controlling a charging and discharging cycle” so it should be given its plain and ordinary meaning. EX2021, ¶182. I agree with Dr. Ricketts on this, but it does not change my conclusions.

144. Additionally, I agree with Dr. Ricketts that it is incorrect to state that “the alleged invention is always either charging or discharging, and never simultaneously both charging and discharging.” EX2021, ¶184.

VII. CONCLUSION

145. I currently hold the opinions set expressed in this declaration. But my analysis may continue, and I may acquire additional information and/or attain supplemental insights that may result in added observations.

146. I declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable under Section 1001 of Title 18 of the United States Code.

Dated: July 7, 2025

By: /Dr. Ian Galton/
Dr. Ian Galton