

Advances in BJT Techniques for High-Performance Transceivers

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ABSTRACT

New low-inertia bipolar junction transistor (BJT) technologies have paved the way for many novel cell designs during the past few years. These IC processes are optimized for operation at low supply voltages and support the high-performance passive components (such as inductors, low-capacitance thin-film resistors and low-resistance metal-oxide-metal capacitors) needed to realize integrated transceivers. This paper presents several circuit concepts, of general value, which have proven useful in the realization of high-performance cellular and cordless telephony applications.

INTRODUCTION

It has become commonplace to see an increasing use of CMOS in telecommunications applications, not only for those parts of a modern transceiver where it is most obviously suited (microprocessor, memory, DSP, ADCs, DACs, codecs and the like) but also in areas which have classically been the almost exclusive domain of bipolar technologies (shared with GaAs). The motivation is usually stated as involving a combination of cost reduction and the desirability of achieving higher levels of integration. However, the real reasons are often a little different, being largely pragmatic: the product developments are conducted in environments where advanced bipolar processes are either not available, or there is a specific objective to find alternatives to bipolar solutions as an academic exercise, with the hope of immediate adoption by industry if certain system objectives can be fully met in CMOS.

It would be both unwise and unjustified to cast doubt on the viability of "doing it all in CMOS", but would be equally inadvisable to presume too much too soon. CMOS has certainly proven to be a worthy challenger to bipolar, in numerous situations, but it would be a mistake to imagine that all the necessary questions have been satisfactorily answered. Analog Devices, like other semiconductor companies with a strong interest in telecommunications, has remained very active in developing new bipolar technologies for both current and emerging IF, RF and microwave applications, as well as ensuring access to state-of-the-art "pure CMOS", down to 0.25 μ m. Several BiCMOS processes have been developed since the mid-70's, the most recent of which combines a 20GHz NPN with a 0.6 μ m CMOS. In the "pure bipolar" domain, the processes in production include a 25GHz junction-isolated technology, and complementary bipolar (CB) technologies using bonded-wafer techniques to provide full dielectric isolation. In these CB processes, all transistors are true three-terminal devices. There are no significant substrate effects: there is no leakage current, no possibility of latch-up, and the collector-substrate capacitance C_{JS} is very much lower than in comparable junction-isolated processes. This capacitance is free from the voltage-modulation of C_{JS} , which has a significant impact on the performance capabilities of many analog cells. For example, VCO pushing, and distortion in low-intermodulation mixers, modulators, demodulators, RF and IF amplifiers, due to the varactor nature of this capacitance in standard BJT technologies, are absent.

The availability of dual-polarity device types in integrated circuit design is one of the key strengths of CMOS, affording, for example, the extensive use of Class-AB techniques to minimize quiescent current consumption, well-known as a major concern in all portable systems, such as cellular and cordless telephones, and pagers. Similar benefits accrue to the use of complementary bipolar processes using dielectric isolation, but with a highly significant difference. The essentially complete isolation of both the NPN device and its high-speed PNP partner, provided by the bonded-wafer technology, stands in strong contrast to what must be faced in the design of CMOS circuits, where substrate effects abound, both DC (for example, back-gate biasing effects) and AC (signal coupling via the substrate or well regions).

Further, these state-of-the-art CB processes provide thin-film resistors, having a sheet resistance of either 100Ω or $1k\Omega$ per square, and a minimum width of $2\mu\text{m}$. They are placed on a thick field oxide, and thus have very low parasitic capacitances, which (if necessary) can be "contained" by the use of planar shielding techniques. They have an extremely low temperature coefficient of resistance (TCR) of about $10\text{-}20\text{ppm}/^\circ\text{C}$, and a matching TCR of under $1\text{ppm}/^\circ\text{C}$, with no voltage nonlinearity and of course no resistance modulation due to an associated junction. While this may seem like the kind of specialized resistor technology needed to realize erstwhile DAC architectures, long-since eclipsed by clever capacitor-based schemes used in contemporary CMOS converters, it should be remembered that all circuit impedances with the dimension of resistance are ultimately traceable to an actual resistor, which, with package pins already in heavy demand, is likely to be on-chip. It is not hard, in bipolar cell design, to transform this "reference" resistor into an "input impedance" of high accuracy. If necessary, one can also lean on laser trimming, to achieve even more accurate impedance control, where needed, as well as attain levels of calibration accuracy (for example, in certain specialized measurement ICs) that are difficult or impossible to achieve when limited by normal manufacturing tolerances. A design technique that will be described in a moment allows one to maintain very accurate gains even when the junction resistances of the transistors would normally lower the gain, sometimes severely. Many of these compensation techniques rely on the subtle analog multiplication properties of the BJT.

These advanced bipolar technologies depend on metallic and dielectric layers of a quality that only a few years ago were thought quite unnecessary for analog integrated circuits. (A passing analogy might be drawn in noting that, to an increasing extent, high-performance MOS memory cells are limited less by the active devices than by storage-capacitor interconnection technologies). The metal-oxide-metal capacitor (MOMCAP) uses a proprietary metal bottom plate, a thin-oxide dielectric and an aluminium top plate. The low sheet resistances of these layers, and the high ratio of top-to-parasitic capacitance (typically 15:1) are important advantages in RF design.

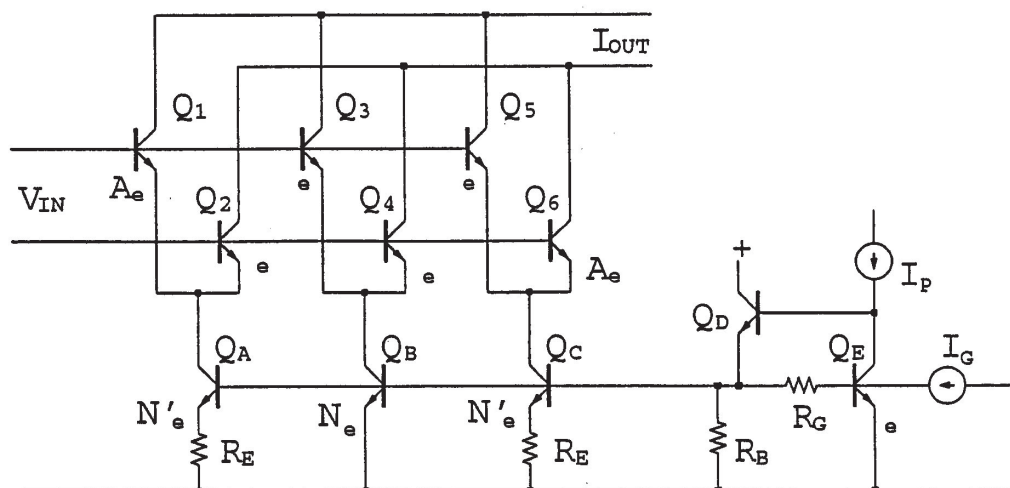
For on-chip spiral inductors, it has long been understood that at moderate frequencies (0.5-2.5GHz) the primary loss mechanism is due to the resistance of the metalization layer. To reduce the loss, it is common to use both levels of a two-layer system. In this way, the typical series resistance is about 1Ω per nanohenry, which means that the element has a zero in its impedance function at 160MHz. More advanced bipolar technologies provide a very thick third level, for use not only in fabricating low-loss inductors, but also as a planar screening layer over very sensitive (or, conversely, highly-energetic) areas of an integrated system. The coming generation of advanced analog processes will take complementary bipolar design into the microwave regime. All of the following examples of new cell concepts, used in a variety of communications applications, can operate on 2.7V supplies at -40°C , and many can operate at lower voltages. However, they do not all use (or need) complementary design techniques.

MIXERS

Two recent advances in monolithic active mixers using BJT technologies are described here. Both follow the standard approach to the realization of a fully-balanced mixer, using an RF stage that performs voltage-to-current conversion, whose differential signal is applied to a standard four-transistor "mixer core" which performs sign-reversal at the LO frequency, and generates the IF at an open-collector output. The first uses Class-A biasing, provides a linear-in-dB variable-gain capability (30dB range), and exhibits a unique "elastic transconductance" feature, which will be explained. The second, called the MICROMIXER uses true Class-AB techniques, provides a precise impedance match at its input, has fixed gain and an extended linear range, leading to high intermodulation intercepts.

Figure 1 shows the variable-gain “Triplus” stage, so called because it comprises a multi-tanh *triplet* [1,2], formed by the differential pairs Q_1/Q_2 , Q_3/Q_4 and Q_5/Q_6 , plus a novel biasing arrangement involving Q_A , Q_B , Q_C . I_{OUT} drives the emitters of the mixer core (not shown here). In the usual triplet, the emitter area ratios, A , of the outer pairs are typically set to between 8 and 15, while the ratio of the bias currents to these pairs to that used in the central pair, which have equal-area emitters, is chosen to maximize the linearity over the required input voltage range. However, such a fixed biasing scheme leads to much elevated noise levels due to the uncorrelated contributions from current-sources Q_A and Q_C , and that of the outer pairs.

A moment's reflection shows that these outer pairs are not needed at high gains (when the signal amplitudes can be assumed to be very small). A better plan, then, is to de-bias them under these conditions, and gradually include them in the overall transconductance as the gain is lowered, corresponding to operation with large input levels. This is the function of the emitter resistors R_E . At maximum gain, when the central current is fairly high, the outer pairs receive a much lower bias current, due to the back-EMF generated across these resistors, while at minimum gain all the currents are small and their ratio is dominated by the emitter area ratios of Q_A , Q_B and Q_C . There is a further advantage to the Triplus stage: since the noise generated in the outer pairs becomes progressively less significant at high gains, these may use very small (thus, low-capacitance, high- f_T) transistors.

Figure 1 The Triplus Variable- g_m Cell, with Linear-in-dB Gain Control

The linear-in-dB gain feature is provided by the transistors in the right-hand area of the cell. The primary bias current I_P is essentially mirrored in the bias transistors, but the voltage drop introduced across R_G by the gain-control current I_G lowers the V_{BE} of these transistors linearly, which causes an *exponential* reduction in the bias current in Q_B . Figure 2 shows the incremental gain vs. the instantaneous input voltage V_{IN} , for five values of I_G . Notice that the signal capacity “stretches” outward as the gain is lowered, while it is much narrower at high gains, leading to the term “elastic transconductance”. The gain law-conformance error is $\pm 0.08\text{dB}$ over 30dB , and the input noise is $0.8\text{nV}/\sqrt{\text{Hz}}$ at full gain.

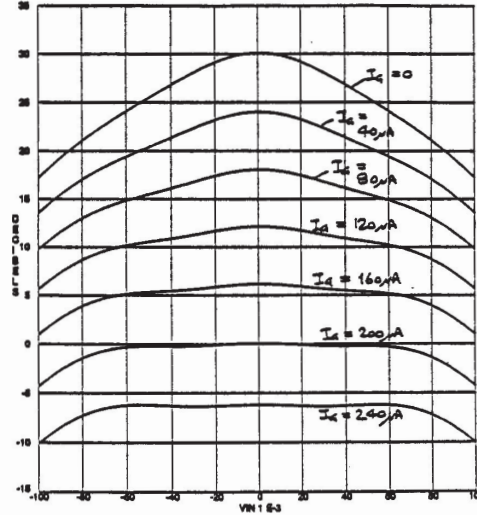


Figure 2 Incremental Gain vs. V_{IN} for the Triplus g_m Cell

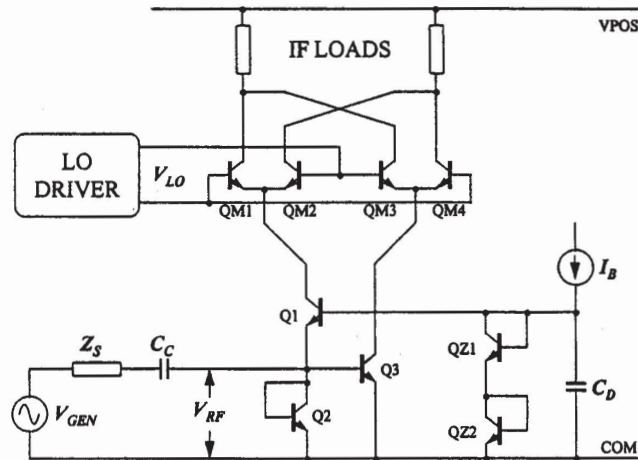


Figure 3 The Minimal MICROMIXER

A quite different approach to the linearization of the RF input stage is used in the MICROMIXER [3,4], the minimal form of which is shown in Figure 3. Here, Q_1 acts essentially like a grounded-base stage, biased by the diode-connected devices Q_{Z1} and Q_{Z2} , and AC-grounded by C_D , while Q_2 and Q_3 form a unity-gain simple current-mirror. The zero-signal current in all these transistors is set by I_Z and the area ratio relative to Q_{Z1} and Q_{Z2} . By setting this current to

The multi-tanh triplet is useful in linear/AGC amplifiers, providing the required high linearity to cope with an insufficiently filtered adjacent-channel signal, which may often be as large as 30dB above the wanted carrier. Figure 5 shows two stages of an IF system each of which provides a gain of typically 0-30dB. Here, the offsets required to synthesize the triplet function are not generated directly by emitter-area ratios, but by equivalent voltages $V_T \log(A)$ (where $V_T = kT/q$) generated across resistors in the emitter-followers which also provide DC level-shifting and additional power gain between stages.

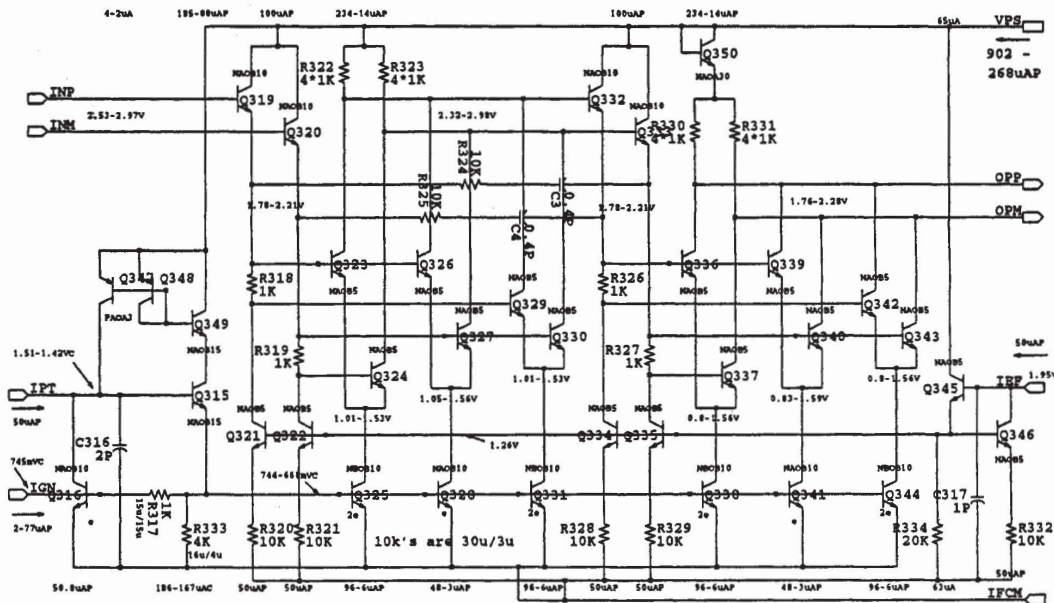


Figure 5 A Variable-Gain IF System Using Multi-tanh Triplets

Although this method introduces noise, it can be used in IF amplifiers because the noise requirements are not so critical as in a mixer. For the same reason, the tail currents, which typically vary over a 30:1 ratio, are now in fixed proportion. The exponentiator needed for the linear-in-dB gain-control function is similar. An analog multiplier (not shown) is used to convert a temperature-stable gain-control voltage, V_G , into a PTAT control current, resulting in stable scaling of the AGC voltage (typically 20mV/dB) and thus of an RSSI output. The gain-control function can be held to within ± 0.2 dB over a total range of 100dB (including a variable-gain mixer). This gain-control technique is much more attractive than those using a "variable cascode" method (a fixed- g_m input cell is followed by a current-steering cell).

Limiter/RSSI (logarithmic) amplifiers follow a different design approach. Five to ten cells are invariably used, each having a fixed small-signal gain G_0 of between 8 to 16dB. Each stage is equipped with a detector. The choice of gain depends on (a) the overall gain-bandwidth needed, and thus, the limiting sensitivity and total dynamic range, (b) the accuracy required of the logarithmic RSSI function, synthesized as essentially a series of piecewise linear segments and (c) total current considerations. Using a G_0 of 12dB, for example, seven cells provide a dynamic range of a little more than 84dB, with a log-conformance (ripple) error of about ± 0.2 dB in a well-designed part. Bandwidths typically range from 25MHz (for 10.7MHz operation, the response shaped to minimize noise) up to 3GHz in specialized applications. Using precision tapered biasing and device-sizing techniques, the first-stage noise figure may be kept below 6dB while conserving the overall power.

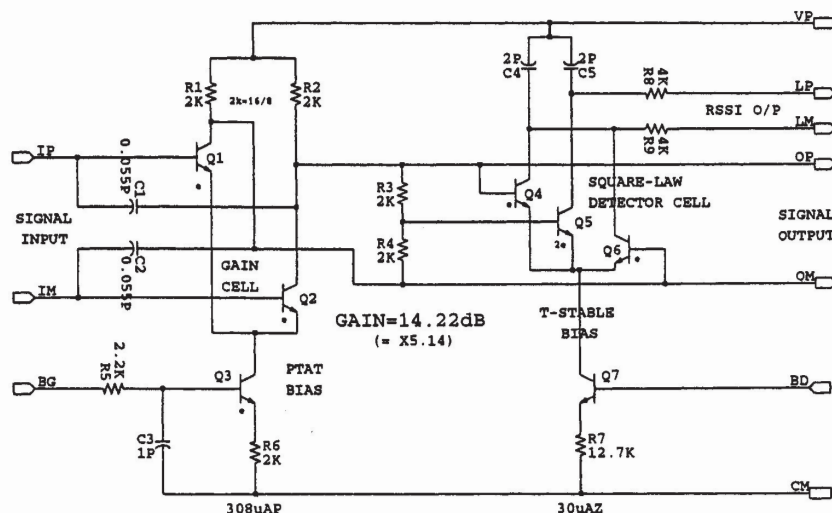


Figure 6 Gain Cell and Detector from a Limiter/RSSI Chain

Figure 6 shows a typical gain cell for this application. It comprises a simple differential pair, Q_1/Q_2 , biased at a fixed tail current, I_T , and loaded by a set of collector resistors, R_1 - R_4 , each of R_L . The small-signal gain for ideal devices, having no ohmic resistances and infinite current gain, is simply $I_T R_L / 4V_T$. However, a robust amplifier design will include several measures to compensate for the several imperfections of real transistors, taking advantage of the fact that this cell is also an analog multiplier, the gain being essentially proportional to I_T . Thus, the bias cell used to generate this current will invoke the very same imperfections as the gain cells in such a way as to eliminate them. This is an aspect of the art of bias design, which, in bipolar practice is very mature and advanced.

The detector cell used here, as part of the RSSI capability, differs from the design often used, which is based on direction rectification of the voltage-mode signal to another voltage-mode output. Here, the detector implements an approximately square-law function in the transconductance domain. This allows the current-mode outputs of all detectors to be simply summed to generate the composite RSSI signal, which can then be converted back to voltage-mode using a final transresistance stage, usually having a low-pass function to eliminate the residual carrier components at multiples of $2f$.

OSCILLATORS

Typical communications ICs require the services of several oscillators: one or two varactor-tuned very-low phase-noise VCOs, with centre frequencies of from 250MHz to about 1.25GHz, for use in the first and second frequency-conversion stages; a less demanding VCO at the second IF for use in demodulation to baseband; perhaps a voltage-controlled temperature-compensated crystal oscillator (VCTXCO) for providing the system clock (13MHz in GSM). Integrated oscillators for such applications are well-developed. In this brief overview, only a single example can be provided.

Figure 7 shows a quadrature voltage-controlled oscillator (QVCO) for use in I/Q demodulation. This oscillator is required to generate essentially a sine and cosine output (though low distortion is not required) with an accurate 90° phase relationship (typically $\pm 1^\circ$) and be voltage-controllable over a moderate range, as part of a phase-locked loop. A fully-differential dual-integrator structure is used, and the outputs, which drive a pair of mixers used for demodulation, are buffered by limiter stages (not shown here).

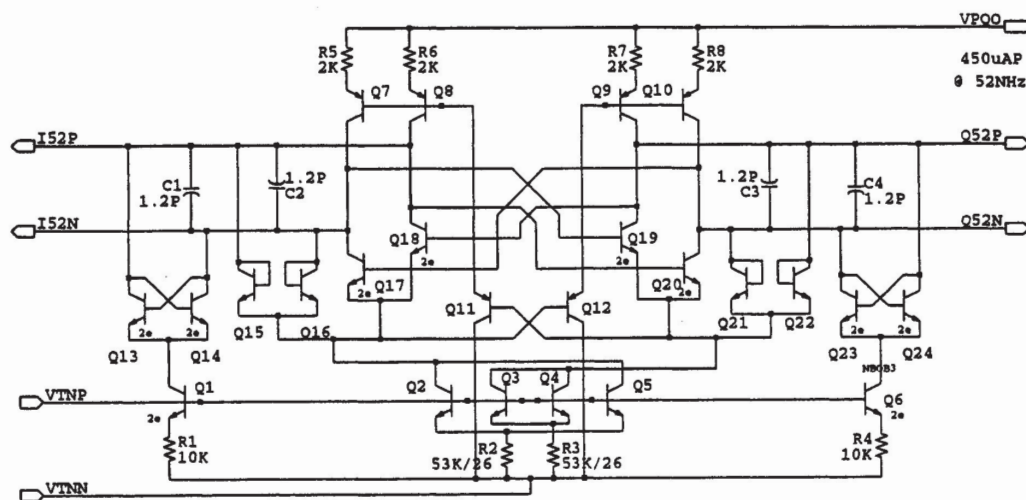


Figure 7 A Tightly-Integrated Quadrature Oscillator

The oscillator core comprises two integrators in a loop, each formed by a g_m cell and a floating capacitor. The frequency is tuned by the tail currents, to which the g_m 's are proportional. Cross-connected common-mode biasing sets the mean V_{CB} of these transistors to zero. Negative-impedance cells place the poles in the right half of the s -plane at start-up; as the amplitude increases, clamping diodes cancel the negative impedance by stealing some of the tail current, until the poles lie exactly on the imaginary axis. This particular design is one of several that address the issue of providing precise amplitude control in recent products. For example, the QVCO in the AD6432 GSM IF Sub-System uses a "Pythagorator", which generates the sum $E^2(\sin^2\omega t + \cos^2\omega t)$ and sets it equal to a reference level, through the action of current-controlled damping cells.

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