these errors can not be corrected by calibration. Common mode rejection of the AD522 is active laser-trimmed to the limits of thin-film resistor stability. Further trimming could improve CMR on a short term basis, but regular readjustment would be necessary to maintain this improvement (see Figure 2). In this example, untrimmed CMR and noise cause a total error of ±0.0065% of full scale and are the major contributors to resolution error.

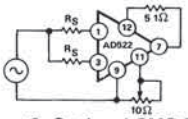


Figure 2. Optional CMR Trim

PERFORMANCE CHARACTERISTICS

Offset Voltage and Current Drift: The AD522 is available in four drift selections. Figure 3 is a graph of maximum RTO offset voltage drift vs. gain for all versions. Errors caused by offset voltage drift can thus be determined for any gain. Offset current drift will cause a voltage error equal to the product of the offset current drift and the source impedance unbalance.

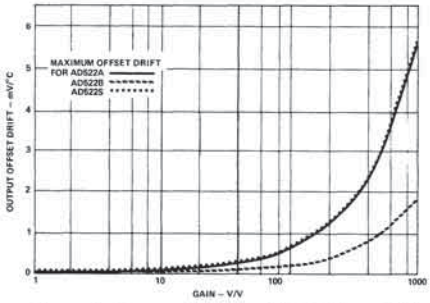


Figure 3. Output Offset Drift (RTO) vs. Gain

Gain Nonlinearity and Noise: Gain nonlinearity increases with gain as the device loop-gain decreases. Figure 4 is a plot of typical nonlinearity vs. gain. The shape of the curve can be safely used to predict worst-case nonlinearity at gains below 100. Noise vs. gain is shown on the same graph.

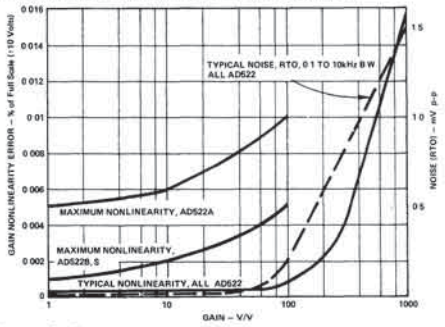


Figure 4. Gain Nonlinearity and Noise (RTO) vs. Gain

Common Mode Rejection: CMR is rated at ±10V and 1kΩ source imbalance. At lower gains, CMR depends mainly on thin-film resistor stability but due to gain-bandwidth considerations, is relatively constant with frequency to beyond 60Hz. The dc CMR improves with increasing gain and is increasingly subject to phase shifts in limited bandwidth high-gain amplifiers. Figure 5 illustrates CMR vs. Gain and Frequency.

Dynamic Performance: Settling time and unity gain bandwidth are directly proportional to gain. As a result, dynamic performance can be predicted from the well-behaved curves of Figure 6.

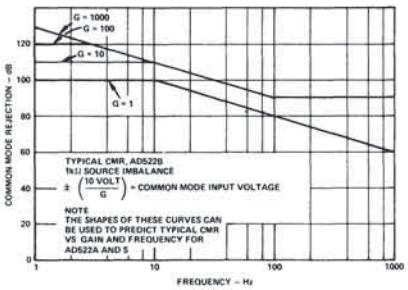


Figure 5. Common Mode Rejection vs. Frequency and Gain

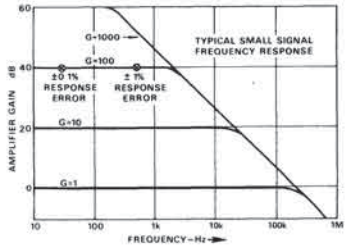


Figure 6. Small Signal Frequency Response (-3dB)

SPECIAL APPLICATIONS

Offset and Gain Trim: Gain accuracy depends largely on the quality of R_G. A precision resistor with a 10ppm/°C temperature coefficient is advised. Offset, like gain, is laser-trimmed to a level suitable for most applications. If further adjustment is required, the circuit shown in Figure 1 is recommended. Note that good quality (25ppm) pots are necessary to maintain voltage drift specifications.

CMR Trim: A short-term CMR improvement of up to 10dB at low gains can be realized with the circuit of Figure 2. Apply a low-frequency 20/G volt peak-to-peak input signal to *both* inputs through their equivalent source resistances and trim the pot for an ac output null .

Sense Output: A sense output is provided to enable remote load sensing or use of an output current booster. Figure 7 illustrates these applications. Being "inside the loop", booster drift errors are minimized. When not used, the sense output should be tied to the output.

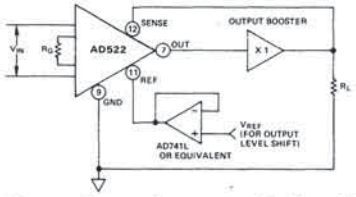


Figure 7. Output Current Booster and Buffered Output Level Shifter

Reference Output: The reference terminal is provided to permit the user to offset or "level shift" the output level to a datum compatible with his load. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset. Furthermore, any reference source resistance will unbalance the CMR trim by the ratio $10k/R_{ref}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 10,000 = 80dB). A buffer amplifier can be used to eliminate this error, as shown in Figure 7, but the drift of the buffer will add to output offset drift. When not used, the reference terminal should be grounded.

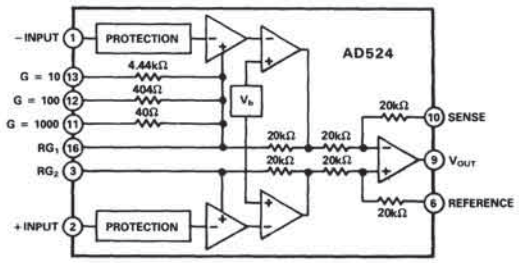
Precision Instrumentation Amplifier

AD524

FEATURES

- Low Noise: 0.3μV p-p 0.1Hz to 10Hz
- Low Nonlinearity: 0.003% (G = 1)
- High CMRR: 120dB (G = 1000)
- Low Offset Voltage: 50μV
- Low Offset Voltage Drift: 0.5μV/°C
- Gain Bandwidth Product: 25MHz
- Pin Programmable Gains of 1, 10, 100, 1000
- Input Protection, Power On – Power Off
- No External Components Required
- Internally Compensated
- MIL-STD-883B, Chips, and Plus Parts Available
- 16-Pin Ceramic DIP Package and 20-Terminal Leadless Chip Carriers Available

AD524 FUNCTIONAL BLOCK DIAGRAM



4

PRODUCT DESCRIPTION

The AD524 is a precision monolithic instrumentation amplifier designed for data acquisition applications requiring high accuracy under worst-case operating conditions. An outstanding combination of high linearity, high common mode rejection, low offset voltage drift, and low noise makes the AD524 suitable for use in many data acquisition systems.

The AD524 has an output offset voltage drift of less than 25μV/°C, input offset voltage drift of less than 0.5μV/°C, CMR above 90dB at unity gain (120dB at G = 1000) and maximum nonlinearity of 0.003% at G = 1. In addition to the outstanding dc specifications the AD524 also has a 25MHz gain bandwidth product (G = 100). To make it suitable for high speed data acquisition systems the AD524 has an output slew rate of 5V/μs and settles in 15μs to 0.01% for gains of 1 to 100.

As a complete amplifier the AD524 does not require any external components for fixed gains of 1, 10, 100 and 1,000. For other gain settings between 1 and 1000 only a single resistor is required. The AD524 input is fully protected for both power on and power off fault conditions.

The AD524 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "A" grade, the low drift "B" grade and lower drift, higher linearity "C" grade are specified from −25°C to +85°C. The "S" grade guarantees performance to specification over the extended temperature range −55°C to +125°C. Devices are available in a 16-pin ceramic DIP package and a 20-terminal leadless chip carrier.

PRODUCT HIGHLIGHTS

1. The AD524 has guaranteed low offset voltage, offset voltage drift and low noise for precision high gain applications.
2. The AD524 is functionally complete with pin programmable gains of 1, 10, 100 and 1000, and single resistor programmable for any gain.
3. Input and output offset nulling terminals are provided for very high precision applications and to minimize offset voltage changes in gain ranging applications.
4. The AD524 is input protected for both power on and power off fault conditions.
5. The AD524 offers superior dynamic performance with a gain bandwidth product of 25MHz, full power response of 75kHz and a settling time of 15μs to 0.01% of a 20V step (G = 100).

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD524A Min	AD524A Typ	AD524A Max	AD524B Min	AD524B Typ	AD524B Max	AD524C Min	AD524C Typ	AD524C Max	AD524S Min	AD524S Typ	AD524S Max	Units
GAIN													
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000			1 to 1000		
Gain Error													
G = 1			±0.05			±0.03			±0.02			±0.05	%
G = 10			±0.25			±0.15			±0.1%			±0.25	%
G = 100			±0.5			±0.35			±0.25			±0.5	%
G = 1000			±2.0			±1.0			±0.5			±2.0	%
Nonlinearity													
G = 1			±0.01			±0.005			±0.003			±0.01	%
G = 10, 100			±0 01			±0 005			±0.003			±0.01	%
G = 1000			±0.01			±0.01			±0.01			±0 01	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 10			15			10			10			10	ppm/°C
G = 100			35			25			25			25	ppm/°C
G = 1000			100			50			50			50	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			250			100			50			100	µV
vs. Temperature			2			0.75			0.5			2.0	µV/°C
Output Offset Voltage			5			3			2.0			3.0	mV
vs. Temperature			100			50			25			50	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	70			75			80			75			dB
G = 10	85			95			100			95			dB
G = 100	95			105			110			105			dB
G = 1000	100			110			115			110			dB
INPUT CURRENT													
Input Bias Current			±50			±25			±15			±50	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
Input Offset Current			±35			±15			±10			±35	nA
vs. Temperature		±100			±100			±100			±100		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common Mode Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_D)		±10			±10			±10			±10		V
Max Common Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		V
Common Mode Rejection dc to 60Hz with 1kΩ Source Imbalance													
G = 1	70			75			80			70			dB
G = 10	90			95			100			90			dB
G = 100	100			105			110			100			dB
G = 1000	110			115			120			110			dB
OUTPUT RATING													
V_{OUT}, R_L = 2kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal −3dB													
G = 1		1			1			1			1		MHz
G = 10		400			400			400			400		kHz
G = 100		150			150			150			150		kHz
G = 1000		25			25			25			25		kHz
Slew Rate		5.0			5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20V Step													
G = 1 to 100		15			15			15			15		µs
G = 1000		75			75			75			75		µs
NOISE													
Voltage Noise, 1kHz													
R.T.I.		7			7			7			7		$nV/\sqrt{Hz}$
R.T O.		90			90			90			90		$nV/\sqrt{Hz}$
R.T.I., 0.1 to 10Hz													
G = 1		15			15			15			15		µV p-p
G = 10		2			2			2			2		µV p-p
G = 100, 1000		0.3			0.3			0.3			0.3		µV p-p
Current Noise													
0.1Hz to 10Hz		60			60			60			60		pA p-p

Model	AD524A			AD524B			AD524C			AD524S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SENSE INPUT													
R_{IN}		20			20			20			20		kΩ ± 20%
I_{IN}		15			15			15			15		μA
Voltage Range	± 10			± 10			± 10			± 10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}		40			40			40			40		kΩ ± 20%
I_{IN}		15			15			15			15		μA
Voltage Range	± 10			± 10			10			10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	25		+ 85	25		+ 85	25		+ 85	55		+ 125	°C
Storage	65		+ 150	65		+ 150	65		+ 150	65		+ 150	°C
POWER SUPPLY													
Power Supply Range	**± 6**	± 15	**± 18**	**± 6**	± 15	**± 18**	**± 6**	± 15	**± 18**	**± 6**	± 15	**± 18**	V
Quiescent Current		3 5	**5.0**		3 5	**5.0**		3 5	**5.0**		3 5	**5.0**	mA
PACKAGE OPTIONS[1]													
16-Pin Ceramic (D-16)		AD524AD			AD524BD			AD524CD			AD524SD		
LCC (E-28A)		AD524AE			AD524BE			AD524CE			AD524SE		

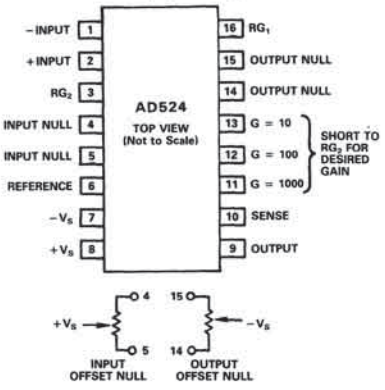
NOTES
[1]See Section 16 for package outline informatin
Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

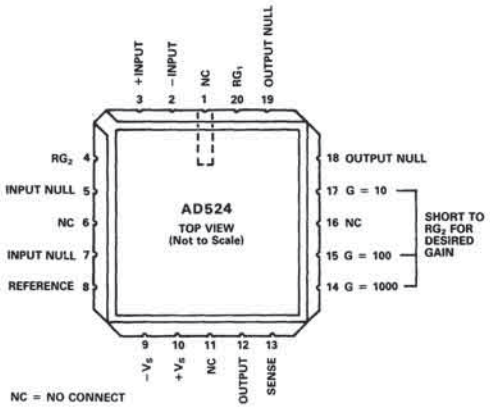
4

CONNECTION DIAGRAMS

Ceramic (D) Package

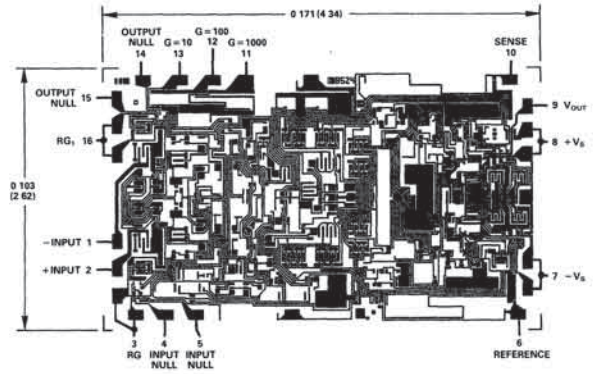


Leadless Chip Carrier (E) Package



METALIZATION PHOTOGRAPH

Dimensions shown in inches and (mm).



PAD NUMBERS CORRESPOND TO PIN NUMBERS FOR THE D16A 16-PIN CERAMIC PACKAGE

Typical Characteristics

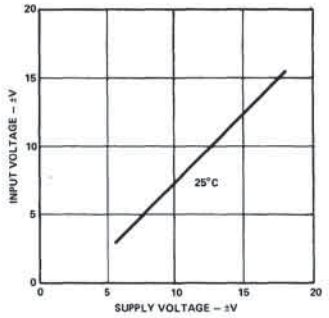


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

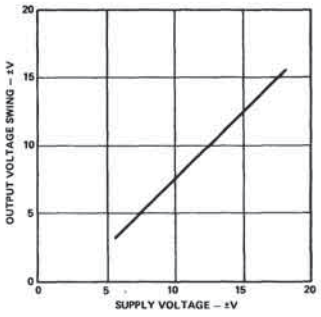


Figure 2. Output Voltage Swing vs. Supply Voltage

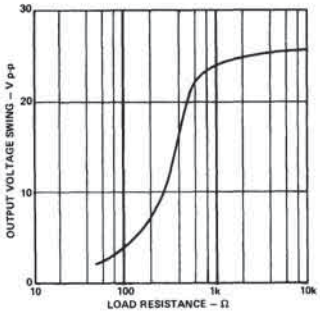


Figure 3. Output Voltage Swing vs. Resistive Load

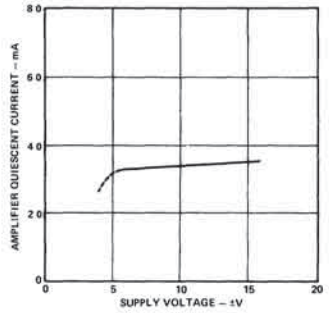


Figure 4. Quiescent Current vs. Supply Voltage

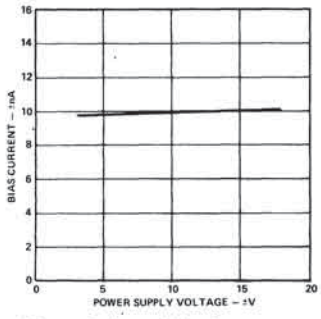


Figure 5. Input Bias Current vs. Supply Voltage

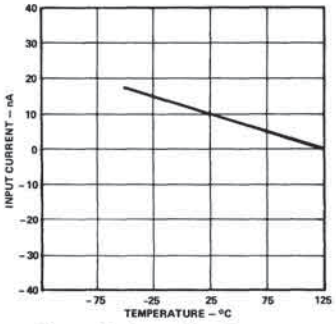


Figure 6. Input Bias Current vs. Temperature

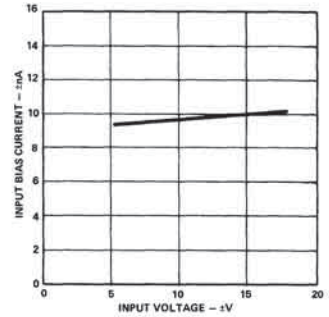


Figure 7. Input Bias Current vs. CMV

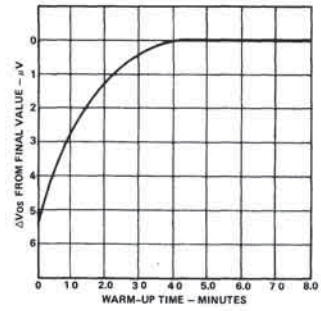


Figure 8. Offset Voltage, RTI, Turn On Drift

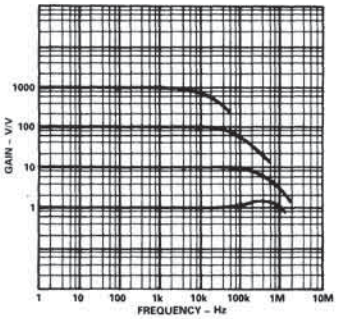


Figure 9. Gain vs. Frequency

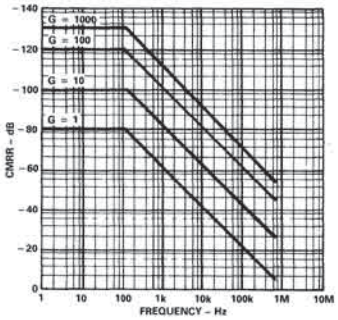


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

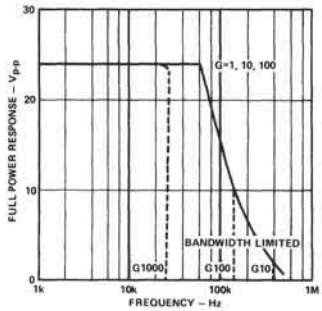


Figure 11. Large Signal Frequency Response

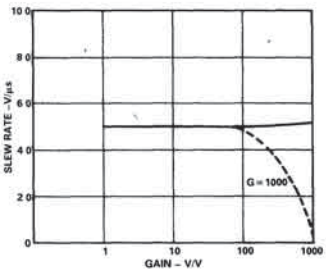


Figure 12. Slew Rate vs. Gain

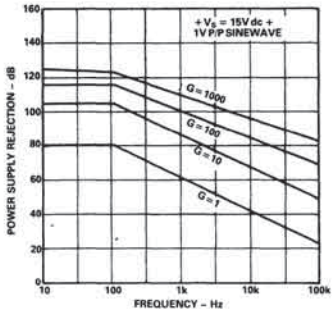


Figure 13. Positive PSRR vs. Frequency

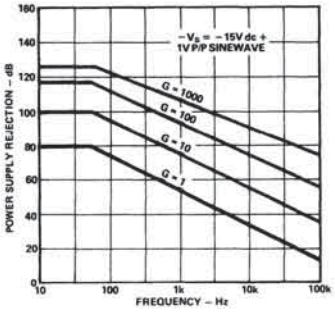


Figure 14. Negative PSRR vs. Frequency

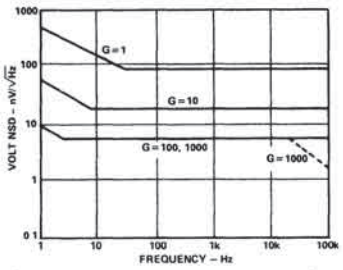


Figure 15. RTI Noise Spectral Density vs. Gain

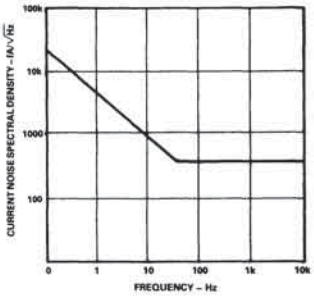


Figure 16. Input Current Noise

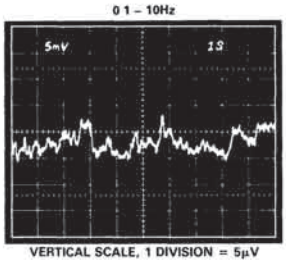


Figure 17. Low Frequency Noise – G = 1 (System Gain = 1000)

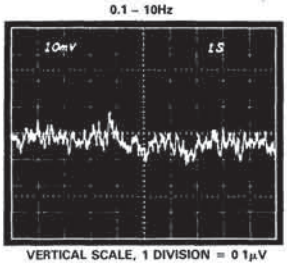


Figure 18. Low Frequency Noise – G = 1000 (System Gain = 100,000)

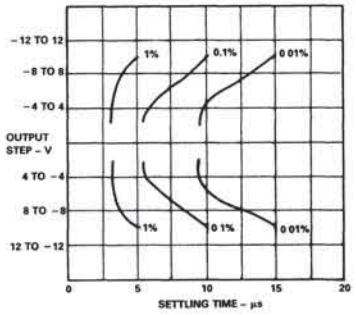


Figure 19. Settling Time Gain = 1

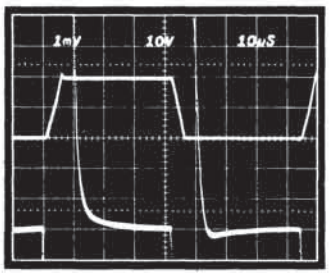


Figure 20. Large Signal Pulse Response and Settling Time – G = 1

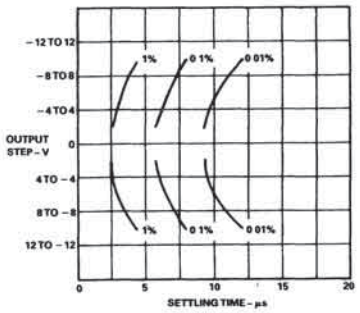


Figure 21. Settling Time Gain = 10

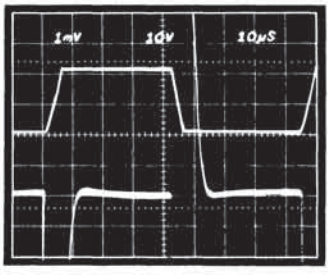


Figure 22. Large Signal Pulse Response and Settling Time G = 10

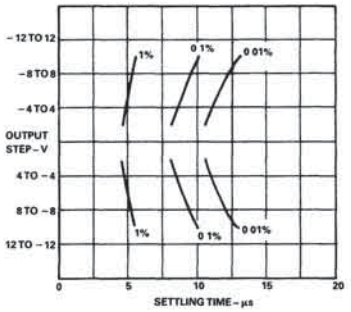


Figure 23. Settling Time Gain = 100

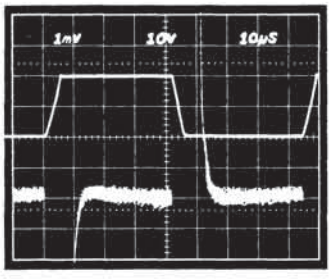


Figure 24. Large Signal Pulse Response and Settling Time G = 100

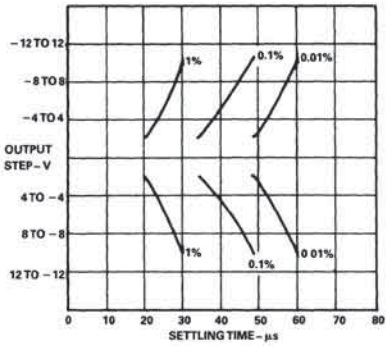


Figure 25. Settling Time Gain = 1000

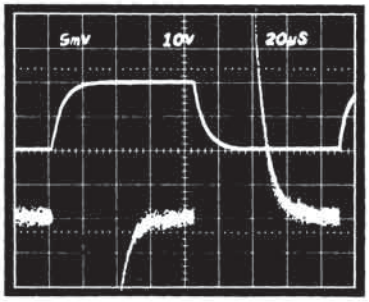


Figure 26. Large Signal Pulse Response and Settling Time G = 1000

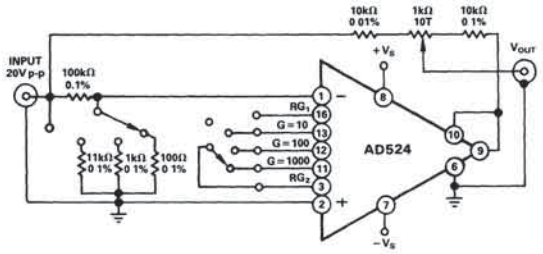


Figure 27. Settling Time Test Circuit

Theory of Operation

The AD524 is a monolithic instrumentation amplifier based on the classic 3 op amp circuit. The advantage of monolithic construction is the closely matched components that enhance the performance of the input preamp. The preamp section develops the programmed gain by the use of feedback concepts. The programmed gain is developed by varying the value of R_G (smaller values increase the gain) while the feedback forces the collector currents Q1, Q2, Q3 and Q4 to be constant which impresses the input voltage across R_G.

As R_G is reduced to increase the programmed gain, the transconductance of the input preamp increases to the transconductance of the input transistors. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 30ppm. Second, the

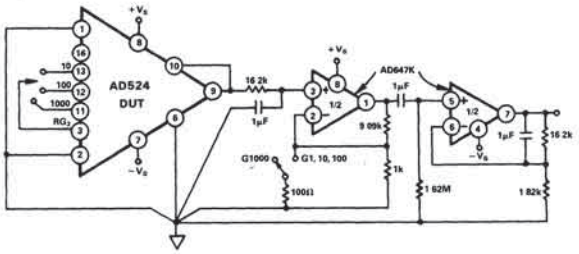


Figure 28. Noise Test Circuit

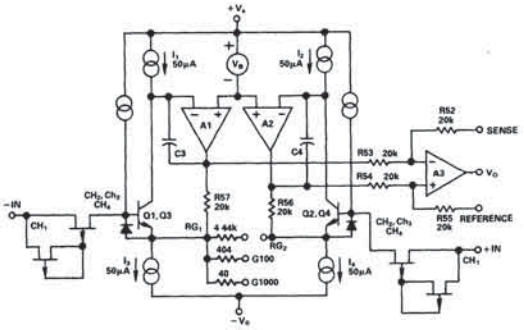


Figure 29. Simplified Circuit of Amplifier; Gain is Defined as ((R56 + R57)/(R_G) + 1. For a Gain of 1, R_G is an Open Circuit

gain bandwith product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of $7nV/\sqrt{Hz}$ at G = 1000.

INPUT PROTECTION

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. At low gains, 10 or less, the gain resistor acts as a current limiting element in series with the inputs. At high gains the lower value of R_G will not adequately protect the inputs from excessive currents. Standard practice would be to place series limiting resistors in each input, but to limit input current to below 5mA with a full differential overload (36V) would require over 7k of resistance which would add $10nV\sqrt{Hz}$ of noise. To provide both input protection and low noise a special series protect FET was used.

A unique FET design was used to provide a bidirectional current limit, thereby, protecting against both positive and negative overloads. Under nonoverload conditions, three channels CH_2, CH_3, CH_4, act as a resistance ($\approx 1k\Omega$) in series with the input as before. During an overload in the positive direction, a fourth channel, CH_1, acts as a small resistance ($\approx 3k\Omega$) in series with the gate, which draws only the leakage current, and the FET limits I_{DSS}. When the FET enhances under a negative overload, the gate current must go through the small FET formed by CH_1 and when this FET goes into saturation, the gate current is limited and the main FET will go into controlled enhancement. The bidirectional limiting holds the maximum input current to 3mA over the 36V range.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and drift comprise two components each; input and output offset and offset drift. Input offset is that component of offset that is directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD524 might have a +250μV output offset and a −50μV input offset. In a unity gain configuration, the *total* output offset would be 200μV or the sum of the two. At a gain of 100, the output offset would be −4.75mV or: +250μV + 100(−50μV) = −4.75mV.

The AD524 provides for both input and output offset adjustment. This simplifies very high precision applications and minimize offset voltage changes in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD524 has internal high accuracy pretrimmed resistors for pin programmable gain of 1, 10, 100 and 1000. One of the preset gains can be selected by pin strapping the appropriate gain terminal and RG_2 together (for G=1 RG_2 is not connected).

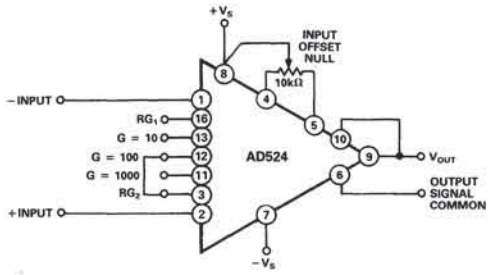


Figure 30. Operating Connections for G = 100

The AD524 can be configured for gains other than those that are internally preset; there are two methods to do this. The first method uses just an external resistor connected between pins 3 and 16 which programs the gain according to the formula $R_G = \frac{40k}{G-1}$ (see Figure 31). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (−50ppm/°C typ).

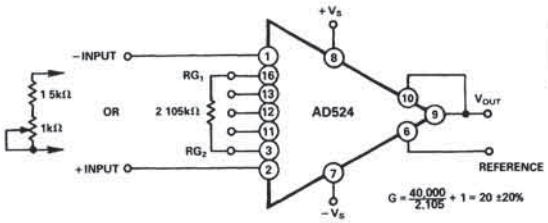


Figure 31. Operating Connections for G = 20

The second technique uses the internal resistors in parallel with an external resistor (Figure 32). This technique minimizes the gain adjustment range and reduces the effects of temperature coefficient sensitivity.

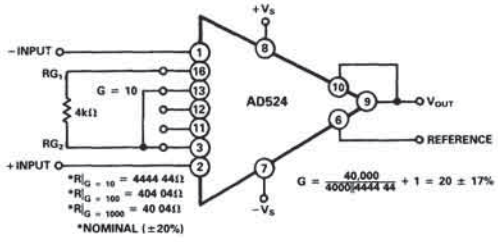


Figure 32. Operating Connections for G = 20, Low Gain T.C. Technique

The AD524 may also be configured to provide gain in the output stage. Figure 33 shows an H pad attenuator connected to the reference and sense lines of the AD524. R1, R2 and R3 should be made as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

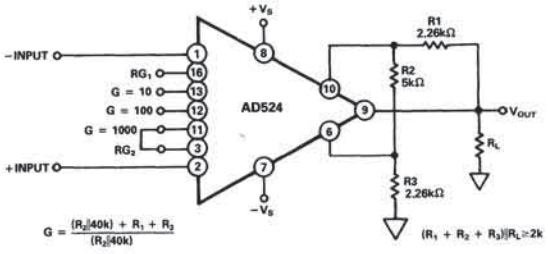


Figure 33. Gain of 2000

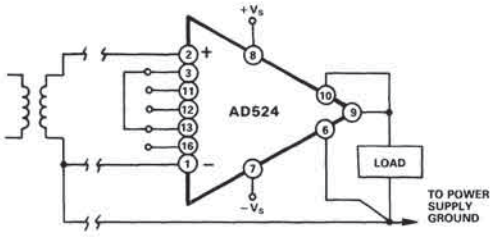
Output Gain	R2	R1,R3	Nominal Gain
2	5kΩ	2.26kΩ	2.02
5	1.05kΩ	2.05kΩ	5.01
10	1kΩ	4.42kΩ	10.1

Table I. Output Gain Resistor Values

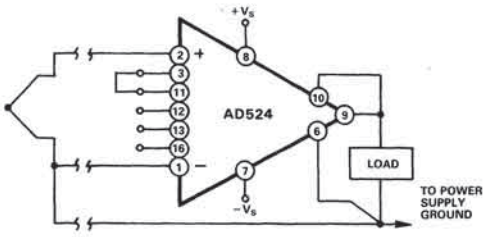
INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in an total error budget. The bias currents when multiplied by the source resistance appear as an offset voltage. What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature. Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source impedance imbalance.

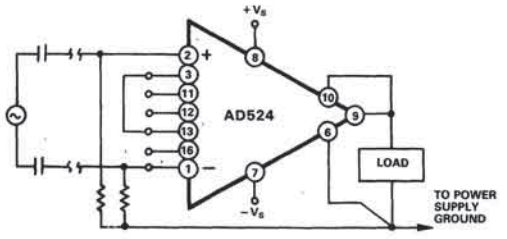
Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground.



a. Transformer Coupled



b. Thermocouple



c. AC Coupled

Figure 34. Indirect Ground Returns for Bias Currents

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common mode rejection errors unless the shield is properly driven. Figures 35 and 36 shows active data guards which are configured to improve ac common mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

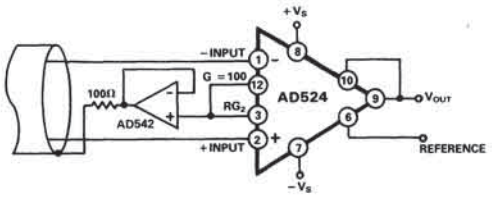


Figure 35. Shield Driver, G ≥ 100

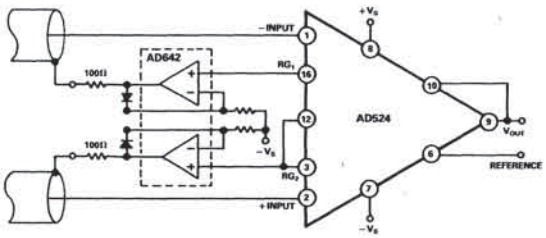


Figure 36. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths

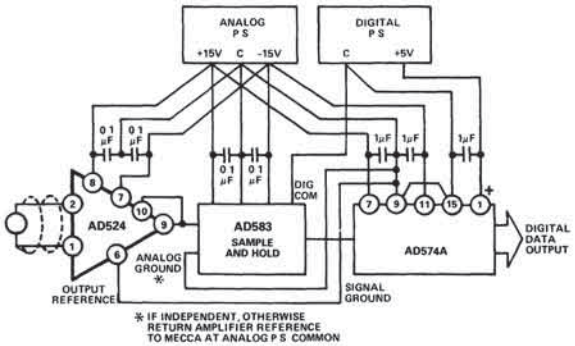


Figure 37. Basic Grounding Practice

have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to minimize the current flow in the path from the sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

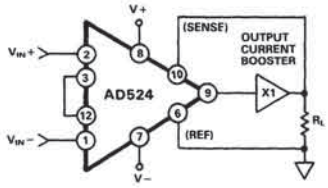


Figure 38. AD524 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 38 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ±10 volts to be shared between signal and reference offset.

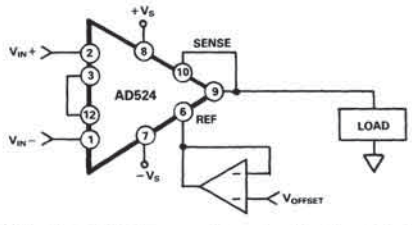


Figure 39. Use of Reference Terminal to Provide Output Offset

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance from the reference terminal to ground increases the gain of the noninverting signal path thereby upsetting the common-mode rejection of the IA.

In the AD524 a reference source resistance will unbalance the CMR trim by the ratio of 20kΩ/R_{REF}. For example, if the reference source impedance is 1Ω, CMR will be reduced to 86dB (20kΩ/1Ω = 86dB). An operational amplifier may be used to provide that low impedance reference point as shown in Figure 39. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 40.

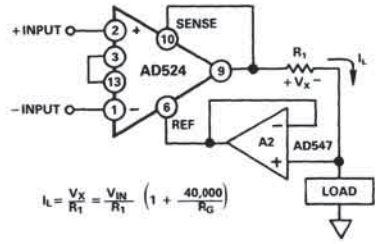


Figure 40. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 41 shows the AD524 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.

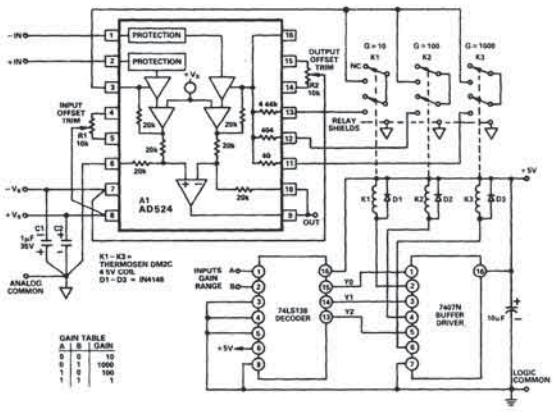


Figure 41. 3 Decade Gain Programmable Amplifier

The AD524 can also be connected for gain in the output stage. Figure 42 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common rejection ratio degradation.

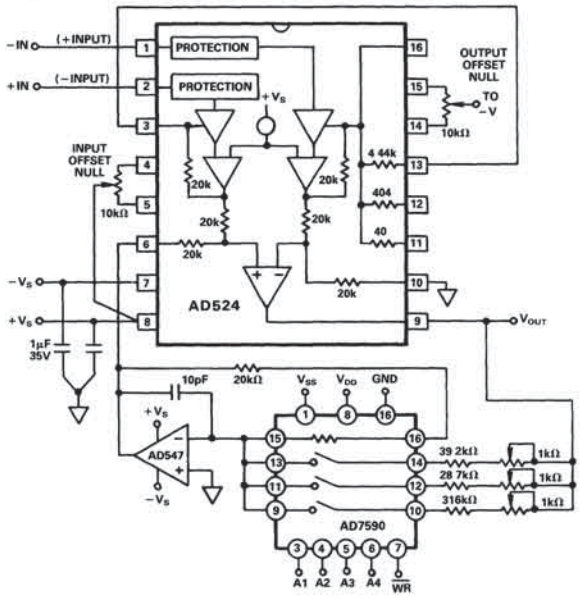


Figure 42. Programmable Output Gain

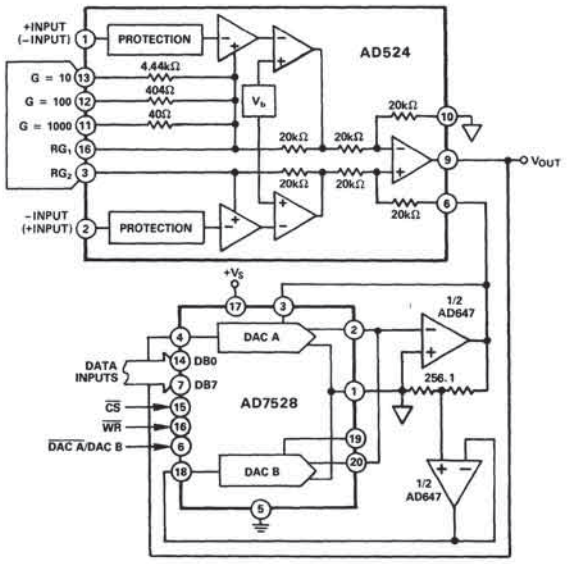


Figure 43. Programmable Output Gain Using a DAC

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 44 show a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

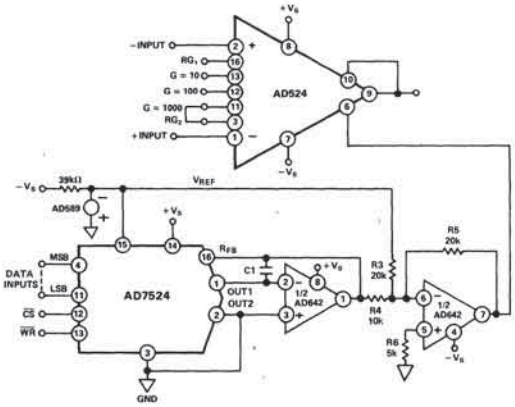


Figure 44. Software Controllable Offset

In many applications complex software algorithms for auto-zero applications are not available. For those applications Figure 45 provides a hardware solution.

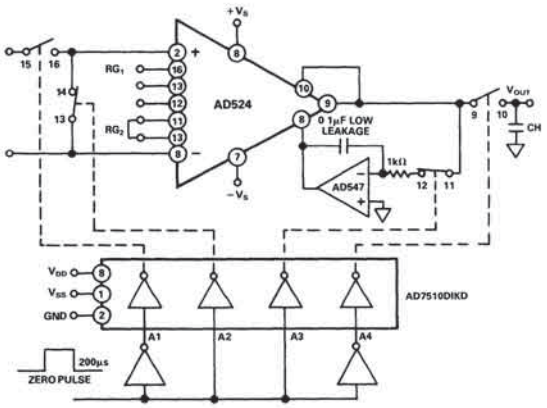


Figure 45. Auto-Zero Circuit

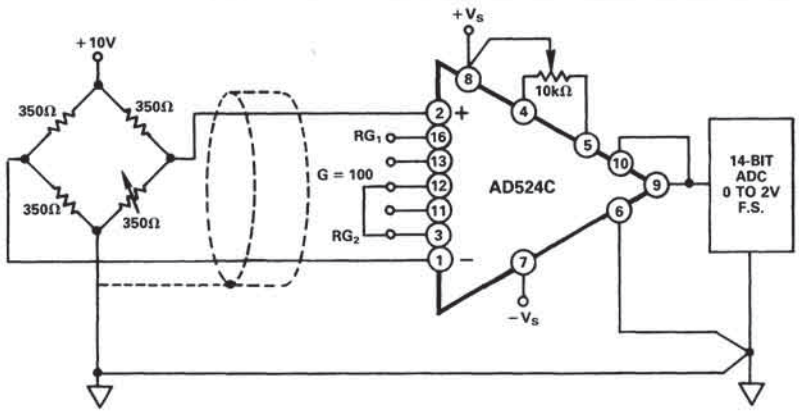


Figure 46. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD524 is required to amplify the output of an unbalanced transducer. Figure 46 shows a differential transducer, unbalanced by 100Ω, supplying a 0 to 20mV signal to an AD524C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is −25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C − 25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (45ppm = 0.004%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.004%.

Error Source	AD524C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.25%	±0.25% = 2500ppm	2500ppm	2500ppm	–
Gain Instability	25ppm	(25ppm/°C)(60°C) = 1500ppm	–	1500ppm	–
Gain Nonlinearity	±0.003%	±0.003% = 30ppm	–	–	30ppm
Input Offset Voltage	±50μV, RTI	±50μV/20mV = ±2500ppm	2500ppm	2500ppm	–
Input Offset Voltage Drift	±0.5μV/°C	(±0.5μV/°C)(60°C) = 30μV 30μV/20mV = 1500ppm	–	1500ppm	–
Output Offset Voltage[1]	±2.0mV	±2.0mV/20mV = 1000ppm	1000ppm	1000ppm	–
Output Offset Voltage Drift[1]	±25μV/°C	(±25μV/°C)(60°C) = 1500μV 1500μV/20mV = 750ppm	–	750ppm	–
Bias Current – Source Imbalance Error	±15nA	(±15nA)(100Ω) = 1.5μV 1.5μV/20mV = 75ppm	75ppm	75ppm	–
Bias Current – Source Imbalance Drift	±100pA/°C	(±100pA/°C)(100Ω)(60°C) = 0.6μV 0.6μV/20mV = 30ppm	–	30ppm	–
Offset Current – Source Imbalance Error	±10nA	(±10nA)(100Ω) = 1μV 1μV/20mV = 50ppm	50ppm	50ppm	–
Offset Current – Source Imbalance Drift	±100pA/°C	(100pA/°C)(100Ω)(60°C) = 0.6μV 0.6μV/20mV = 30ppm	–	30ppm	–
Offset Current – Source Resistance – Error	±10nA	(10nA)(175Ω) = 3.5μV 3.5μV/20mV = 87.5ppm	87.5ppm	87.5ppm	–
Offset Current – Source Resistance – Drift	±100pA/°C	(100pA/°C)(175Ω)(60°C) = 1μV 1μV/20mV = 50ppm	–	50ppm	–
Common Mode Rejection 5V dc	115dB	115dB = 1.8ppm × 5V = 8.8μV 8.8μV/20mV = 444ppm	444ppm	444ppm	–
Noise, RTI (0.1–10Hz)	0.3μV p-p	0.3μV p-p/20mV = 15ppm	–	–	15ppm
		Total Error	6656.5ppm	10516.5ppm	45ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

Table II. Error Budget Analysis of AD524CD in Bridge Application

Figure 47 shows a simple application, in which the variation of the cold-junction voltage of a Type J thermocouple–iron(+)–constantan– is compensated for by a voltage developed in series by the temperature-sensitive output current of an AD590 semiconductor temperature sensor.

The circuit is calibrated by adjusting R_T for proper output voltage with the measuring junction at a known reference temperature and the circuit near 25°C. If resistors with low tempcos are used, compensation accuracy will be to within ±0.5°C, for temperatures between +15°C and +35°C. Other thermocouple types may be accommodated with the standard resistance values shown in the table. For other ranges of ambient temperature, the equation in the figure may be solved for the optimum values of R_T and R_A.

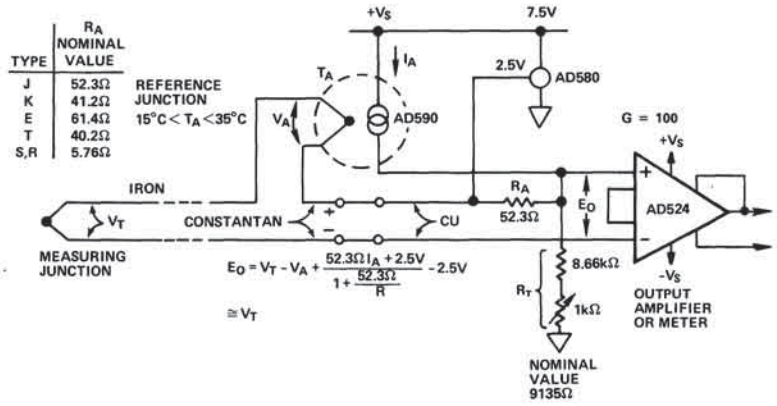


Figure 47. Cold-Junction Compensation

The microprocessor controlled data acquisition system shown in Figure 48 includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

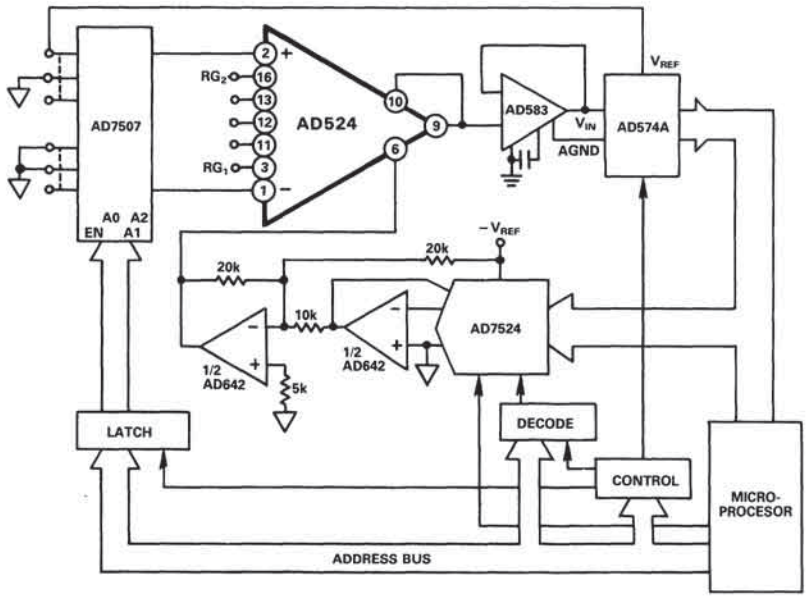


Figure 48. Microprocessor Controlled Data Acquisition System

ANALOG DEVICES

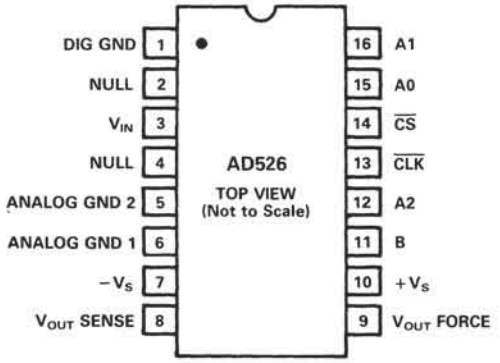
Software Programmable Gain Amplifier

AD526

FEATURES

Digitally Programmable Binary Gains from 1 to 16
Two-Chip Cascade Mode Achieves Binary Gain from 1 to 256
Gain Error:
0.01% max, Gain = 1, 2, 4 (C Grade)
0.02% max, Gain = 8, 16 (C Grade)
0.5ppm/°C Drift Over Temperature
Fast Settling Time
10V Signal Change:
0.01% in 4.5μs (Gain = 16)
Gain Change:
0.01% in 5.6μs (Gain = 16)
Low Nonlinearity: ±0.005% FSR max (J Grade)
Excellent dc Accuracy:
Offset Voltage: 0.5mV max (C Grade)
Offset Voltage Drift: 3μV/°C (C Grade)
TTL Compatible Digital Inputs

AD526 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD526 is a single-ended, monolithic software programmable gain amplifier (SPGA) that provides gains of 1, 2, 4, 8 and 16. It is complete, including amplifier, resistor network and TTL-compatible latched inputs, and requires no external components.

Low gain error and low nonlinearity make the AD526 ideal for precision instrumentation applications requiring programmable gain. The small signal bandwidth is 350kHz at a gain of 16. In addition, the AD526 provides excellent dc precision. The FET-input stage results in a low bias current of 50pA. A guaranteed maximum input offset voltage of 0.5mV max (C grade) and low gain error (0.01%, G=1, 2, 4, C grade) are accomplished using Analog Devices' laser trimming technology.

To provide flexibility to the system designer, the AD526 can be operated in either latched or transparent mode. The force/sense configuration preserves accuracy when the output is connected to remote or low impedance loads.

The AD526 is offered in one commercial (0 to +70°C) grade, J, and three industrial grades, A, B and C, which are specified from −40°C to +85°C. The S grade is specified from −55°C to +125°C. The military version is available processed to MIL-STD 883B, Rev C. The J grade is supplied in a 16-pin plastic DIP, and the other grades are offered in a 16-pin hermetic side-brazed ceramic DIP.

APPLICATION HIGHLIGHTS

1. **Dynamic Range Extension for ADC Systems:** A single AD526 in conjunction with a 12-bit ADC can provide 96dB of dynamic range for ADC systems.
2. **Gain Ranging Pre-Amps:** The AD526 offers complete digital gain control with precise gains in binary steps from 1 to 16. Additional gains of 32, 64, 128 and 256 are possible by cascading two AD526s.

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD526J Min	AD526J Typ	AD526J Max	AD526A Min	AD526A Typ	AD526A Max	AD526B/S Min	AD526B/S Typ	AD526B/S Max	AD526C Min	AD526C Typ	AD526C Max	Units
GAIN													
Gain Range													
(Digitally Programmable)		1, 2, 4, 8, 16			1, 2, 4, 8, 16			1, 2, 4, 8, 16			1, 2, 4, 8, 16		
Gain Error													
G = 1			**0.05**			**0.02**			**0.01**			**0.01**	%
G = 2			**0.05**			**0.03**			**0.02**			**0.01**	%
G = 4			**0.10**			**0.03**			**0.02**			**0.01**	%
G = 8			**0.15**			**0.07**			**0.04**			**0.02**	%
G = 16			**0.15**			**0.07**			**0.04**			**0.02**	%
Gain Error Drift													
Over Temperature													
G = 1		0.5	2.0		0.5	2.0		0.5	2.0		0.5	2.0	ppm/°C
G = 2		0.5	2.0		0.5	2.0		0.5	2.0		0.5	2.0	ppm/°C
G = 4		0.5	3.0		0.5	3.0		0.5	3.0		0.5	3.0	ppm/°C
G = 8		0.5	5.0		0.5	5.0		0.5	5.0		0.5	5.0	ppm/°C
G = 16		1.0	5.0		1.0	5.0		1.0	5.0		1.0	5.0	ppm/°C
Gain Error (T_{min} to T_{max})													
G = 1			0.06			**0.03**			**0.02**			**0.015**	%
G = 2			0.06			**0.04**			**0.03**			**0.015**	%
G = 4			0.12			**0.04**			**0.03**			**0.015**	%
G = 8			0.17			**0.08**			**0.05**			**0.03**	%
G = 16			0.17			**0.08**			**0.05**			**0.03**	%
Nonlinearity													
G = 1			**0.005**			**0.005**			**0.005**			**0.0035**	% FSR
G = 2			0.001			0.001			0.001			0.001	% FSR
G = 4			0.001			0.001			0.001			0.001	% FSR
G = 8			0.001			0.001			0.001			0.001	% FSR
G = 16			0.001			0.001			0.001			0.001	% FSR
Nonlinearity (T_{min} to T_{max})													
G = 1			0.01			**0.01**			**0.01**			**0.007**	% FSR
G = 2			0.001			0.001			0.001			0.001	% FSR
G = 4			0.001			0.001			0.001			0.001	% FSR
G = 8			0.001			0.001			0.001			0.001	% FSR
G = 16			0.001			0.001			0.001			0.001	% FSR
VOLTAGE OFFSET, ALL GAINS													
Input Offset Voltage		0.4	**1.5**		0.25	**0.7**		0.25	**0.5**		0.25	**0.5**	mV
Input Offset Voltage Drift Over Temperature		5	20		3	10		3	10		3	10	µV/°C
Input Offset Voltage T_{min} to T_{max}			2.0			**1.0**			**0.8**			**0.8**	mV
Input Offset Voltage vs. Supply (V_S ± 10%)	80			80			84			90			dB
INPUT BIAS CURRENT													
Over Input Voltage Range ± 10V		50	**150**		50	**150**		50	**150**		50	**150**	pA
ANALOG INPUT CHARACTERISTICS													
Voltage Range													
(Linear Operation)	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Capacitance		5			5			5			5		pF
RATED OUTPUT													
Voltage	**±10**	±12		**±10**	±12		**±10**	±12		**±10**	±12		V
Current (V_{OUT} = ±10V)	**±5**	±10		**±5**	±10		**±5**	±10		**±5**	±10		mA
Short-Circuit Current	**15**	30		**15**	30		**15**	30		**15**	30		mA
DC Output Resistance		0.002			0.002			0.002			0.002		Ω
Load Capacitance (For Stable Operation)		700			700			700			700		pF
NOISE, ALL GAINS													
Voltage Noise, RTI													
0.1Hz to 10Hz		3			3			3			3		µV p-p
Voltage Noise Density, RTI													
f = 10Hz		70			70			70			70		nV/√Hz
f = 100Hz		60			60			60			60		nV/√Hz
f = 1kHz		30			30			30			30		nV/√Hz
f = 10kHz		25			25			25			25		nV/√Hz

Model	AD526J Min	AD526J Typ	AD526J Max	AD526A Min	AD526A Typ	AD526A Max	AD526B/S Min	AD526B/S Typ	AD526B/S Max	AD526C Min	AD526C Typ	AD526C Max	Units
DYNAMIC RESPONSE													
– 3dB Bandwidth (Small Signal)													
G = 1		4.0			4.0			4.0			4.0		MHz
G = 2		2.0			2.0			2.0			2.0		MHz
G = 4		1.5			1.5			1.5			1.5		MHz
G = 8		0.65			0.65			0.65			0 65		MHz
G = 16		0 35			0.35			0.35			0.35		MHz
Signal Settling Time to 0.01% (ΔV_{OUT} = ± 10V)													
G = 1		2 1	4		2.1	4		2.1	4		2.1	4	µs
G = 2		2.5	5		2.5	5		2.5	5		2.5	5	µs
G = 4		2.7	5		2.7	5		2.7	5		2 7	5	µs
G = 8		3.6	7		3.6	7		3.6	7		3.6	7	µs
G = 16		4.1	7		4.1	7		4.1	7		4.1	7	µs
Full Power Bandwidth													
G = 1, 2, 4		0.10			0.10			0.10			0.10		MHz
G = 8, 16		0.35			0.35			0.35			0.35		MHz
Slew Rate													
G = 1, 2, 4	**4**	6		**4**	6		**4**	6		**4**	6		V/µs
G = 8, 16	**18**	24		**18**	24		**18**	24		**18**	24		V/µs
DIGITAL INPUTS (T_{min} to T_{max})													
Input Current (V_H = 5V)	60	100	140	60	100	140	60	100	140	60	100	140	µA
Logic "1"	2		6	2		6	2		6	2		6	V
Logic "0"	0		0.8	0		0.8	0		0.8	0		0.8	V
TIMING[1] (V_L = 0.2V, V_H = 3.7V)													
A0, A1, A2													
T_C	50			50			50			50			ns
T_S	30			30			30			30			ns
T_H	30			30			30			30			ns
B													
T_C	50			50			50			50			ns
T_S	40			40			40			40			ns
T_H	10			10			10			10			ns
TEMPERATURE RANGE													
Specified Performance	0		+70	– 40		+85	– 40/ – 55		+85/ + 125	– 40		+85	°C
Storage	– 65		+ 125	– 65		+ 150	– 65		+ 150	– 65		+ 150	°C
POWER SUPPLY													
Operating Range	±4.5		±16.5	±4.5		±16.5	±4.5		±16.5	±4.5		±16.5	V
Positive Supply Current		10	**14**		10	**14**		10	**14**		10	**14**	mA
Negative Supply Current		10	**13**		10	**13**		10	**13**		10	**13**	mA
PACKAGE OPTIONS[2]													
Plastic (N-16)	AD526JN												
Ceramic DIP (D-16)				AD526AD			AD526BD AD526SD AD526SD/883B			AD526CD			

NOTE
[1]Refer to Figure 35 for definitions.
FSR = Full-Scale Range = 20V
RTI = Referred to Input.
[2]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Typical Characteristics

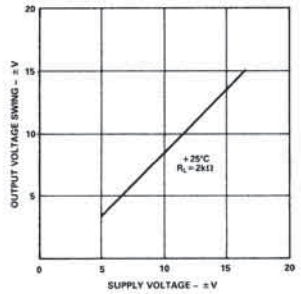


Figure 1. Output Voltage vs. Supply Voltage, G = 16

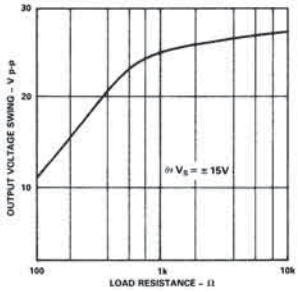


Figure 2. Output Voltage Swing vs. Resistive Load

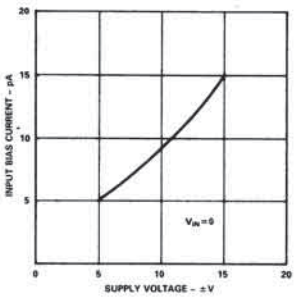


Figure 3. Input Bias Current vs. Supply Voltage

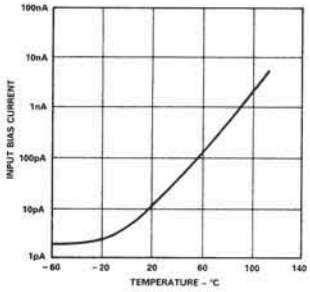


Figure 4. Input Bias Current vs. Temperature

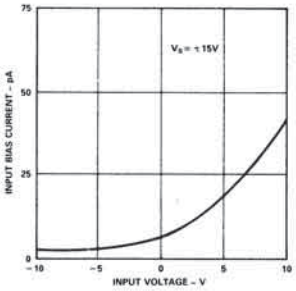


Figure 5. Input Bias Current vs. Input Voltage

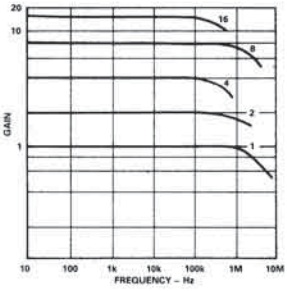


Figure 6. Gain vs. Frequency

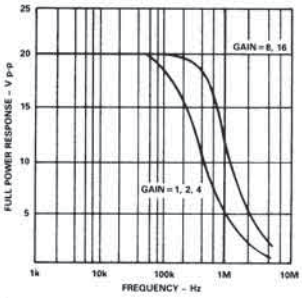


Figure 7. Large Signal Frequency Response

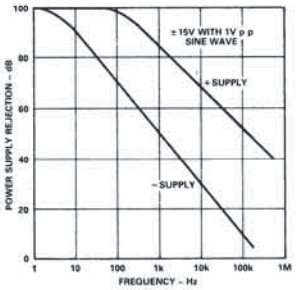


Figure 8. PSRR vs. Frequency

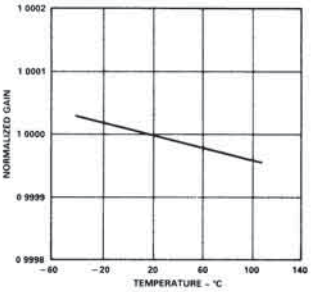


Figure 9. Normalized Gain vs. Temperature, Gain = 1

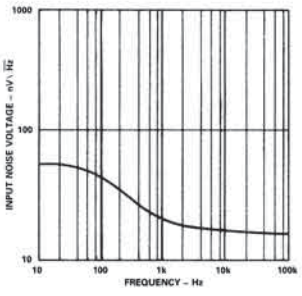


Figure 10. Noise Spectral Density

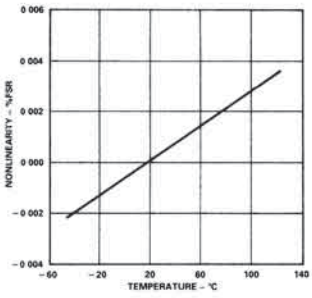


Figure 11. Nonlinearity vs. Temperature, Gain = 1

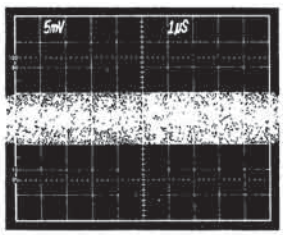


Figure 12. Wideband Output Noise, G = 16 (Amplified by 10)

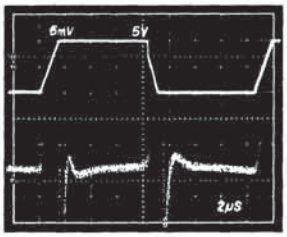


Figure 13. Large Signal Pulse Response and Settling Time*, G = 1

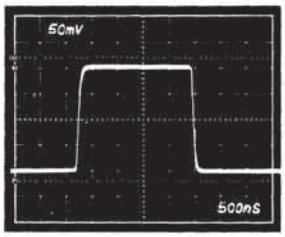


Figure 14. Small Signal Pulse Response, G = 1

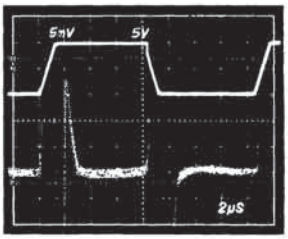


Figure 15. Large Signal Pulse Response and Settling Time*, G = 2

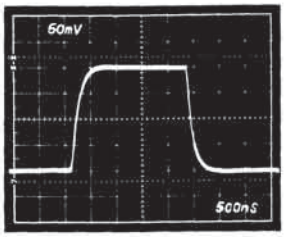


Figure 16. Small Signal Pulse Response, G = 2

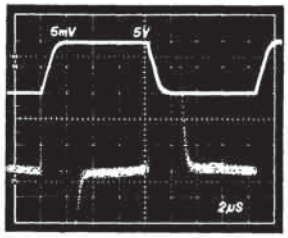


Figure 17. Large Signal Pulse Response and Settling Time*, G = 4

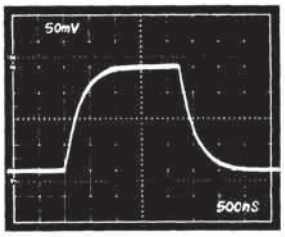


Figure 18. Small Signal Pulse Response, G = 4

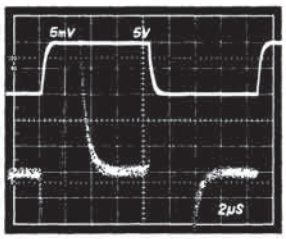


Figure 19. Large Signal Pulse Response and Settling Time*, G = 8

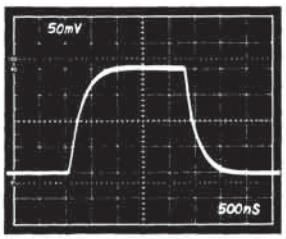


Figure 20. Small Signal Pulse Response, G = 8

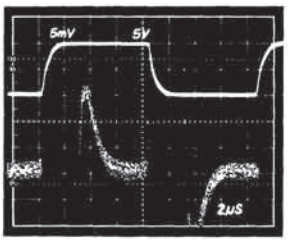


Figure 21. Large Signal Pulse Response and Settling Time*, G = 16

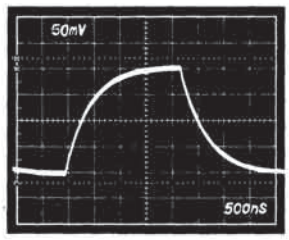


Figure 22. Small Signal Pulse Response, Gain = 16

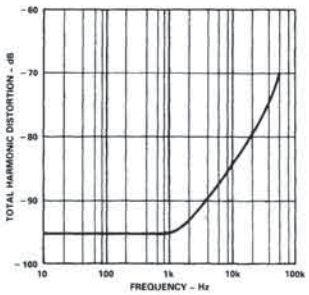


Figure 23. Total Harmonic Distortion vs. Frequency, Gain = 16

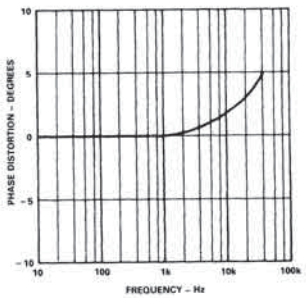


Figure 24. Phase Distortion vs. Frequency, Gain = 16

*For Settling Time Traces, 0.01% = 1/2 Vertical Division

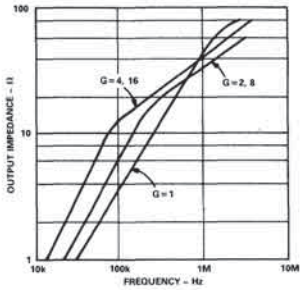


Figure 25. Output Impedance vs. Frequency

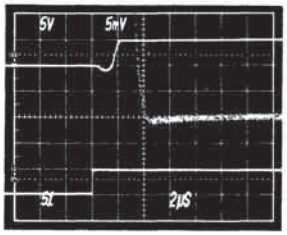


Figure 26. Gain Change Settling Time, Gain Change: 1 to 2*

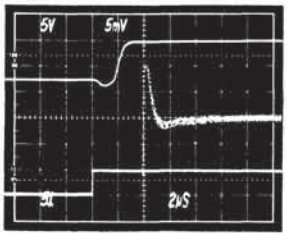


Figure 27. Gain Change Settling Time, Gain Change 1 to 4*

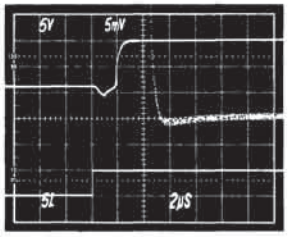


Figure 28. Gain Change Settling Time, Gain Change 1 to 8*

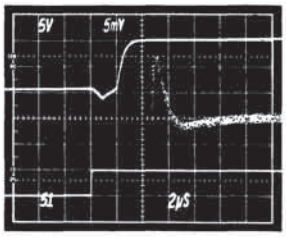


Figure 29. Gain Change Settling Time, Gain Change 1 to 16*

*Scope Traces are:
Top: Output Transition
Middle: Output Settling
Bottom: Digital Input

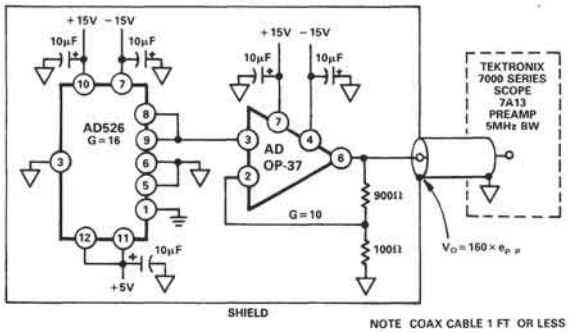


Figure 30. Wideband Noise Test Circuit

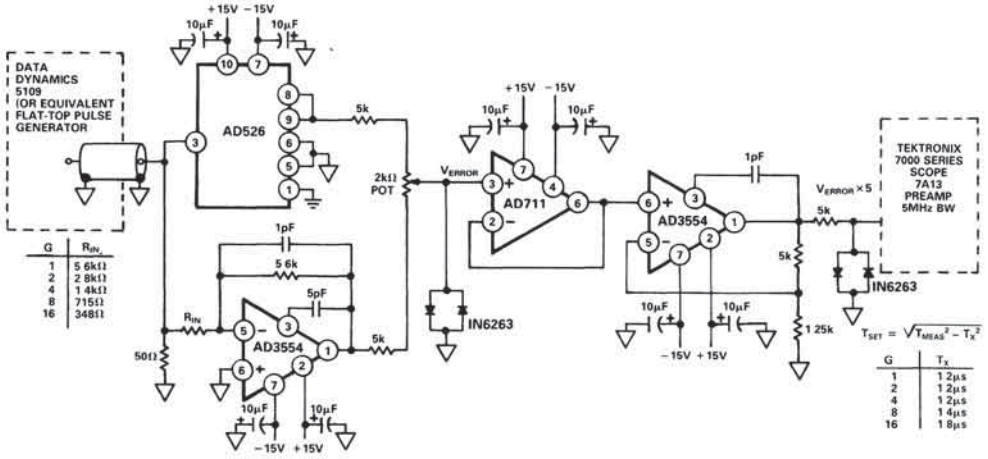


Figure 31. Settling Time Test Circuit

THEORY OF OPERATION

The AD526 is a complete software programmable gain amplifier (SPGA) implemented monolithically with a drift-trimmed BiFET amplifier, a laser wafer trimmed resistor network, JFET analog switches and TTL compatible gain code latches.

A particular gain is selected by applying the appropriate gain code (see Table I) to the control logic. The control logic turns on the JFET switch that connects the correct tap on the gain network to the inverting input of the amplifier; all unselected JFET gain switches are off (open). The "on" resistance of the gain switches causes negligible gain error since only the amplifier's input bias current, which is less than 150pA, actually flows through these switches.

The AD526 is capable of storing the gain code, (latched mode), B, A0, A1, A2, under the direction of control inputs $\overline{CLK}$ and $\overline{CS}$. Alternatively, the AD526 can respond directly to gain code changes if the control inputs are tied low (transparent mode).

For gains of 8 and 16, a fraction of the frequency compensation capacitance (C1 in Figure 32) is automatically switched out of the circuit. This increases the amplifier's bandwidth and improves its signal settling time and slew rate.

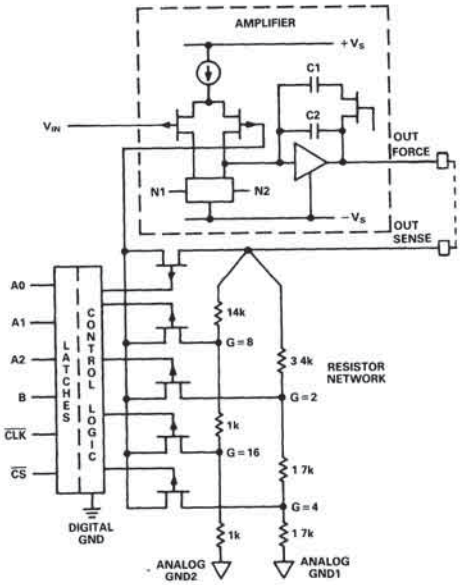


Figure 32. Simplified Schematic of the AD526

TRANSPARENT MODE OF OPERATION

In the transparent mode of operation, the AD526 will respond directly to level changes at the gain code inputs (A0, A1, A2) if B is tied high and both $\overline{CS}$ and $\overline{CLK}$ are allowed to float low.

After the gain codes are changed, the AD526's output voltage typically requires 5.5μs to settle to within 0.01% of the final value. Figures 26 to 29 show the performance of the AD526 for positive gain code changes.

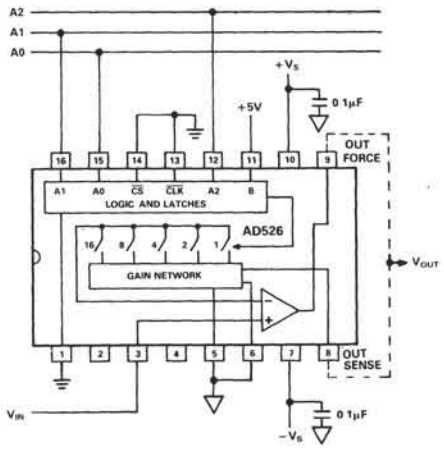


Figure 33. Transparent Mode

LATCHED MODE OF OPERATION

The latched mode of operation is shown in Figure 34. When either $\overline{CS}$ or $\overline{CLK}$ go to a logic "1," the gain code (A0, A1, A2, B) signals are latched into the registers and held until both $\overline{CS}$ and $\overline{CLK}$ return to "0." *Unused $\overline{CS}$ or $\overline{CLK}$ inputs should be tied to ground.* The $\overline{CS}$ and $\overline{CLK}$ inputs are functionally and electrically equivalent.

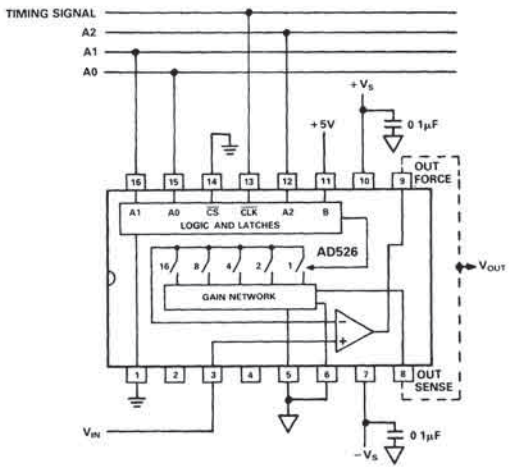


Figure 34. Latched Mode

TIMING AND CONTROL

GAIN CODE				CONTROL	CONDITION	
A2	A1	A0	B	$\overline{CLK}$ ($\overline{CS}$ = 0)	Gain	Condition
X	X	X	X	1	Previous State	Latched
0	0	0	1	0	1	Transparent
0	0	1	1	0	2	Transparent
0	1	0	1	0	4	Transparent
0	1	1	1	0	8	Transparent
1	X	X	1	0	16	Transparent
X	X	X	0	0	1	Transparent
X	X	X	0	1	1	Latched
0	0	0	1	1	1	Latched
0	0	1	1	1	2	Latched
0	1	0	1	1	4	Latched
0	1	1	1	1	8	Latched
1	X	X	1	1	16	Latched

NOTE: X = Don't Care

Table I. AD526 Logic Input Truth Table

The specifications on page 3 in combination with Figure 35 give the timing requirements for loading new gain codes.

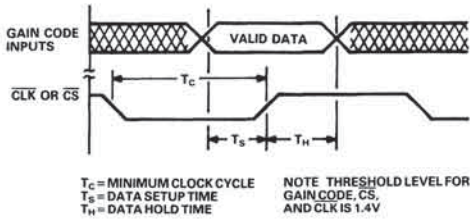


Figure 35. AD526 Timing

DIGITAL FEEDTHROUGH

With either $\overline{CS}$ or $\overline{CLK}$ or both held high, the AD526 gain state will remain constant regardless of the transitions at the A0, A1, A2 or B inputs. However, high-speed logic transitions will unavoidably feed through to the analog circuitry within the AD526 causing spikes to occur at the signal output.

This feedthrough effect can be completely eliminated by operating the AD526 in the transparent mode and latching the gain code in an external bank of latches (Figure 36).

To operate the AD526 using serial inputs, the configuration shown in Figure 36 can be used with the 74LS174 replaced by a serial-in/parallel-out latch, such as the 54LS594.

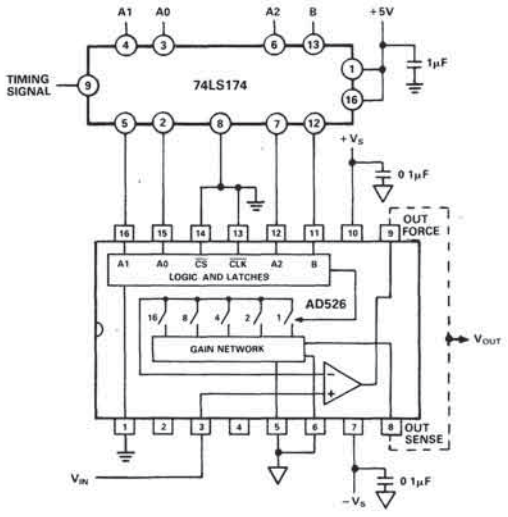


Figure 36. Using an External Latch to Minimize Digital Feedthrough

GROUNDING AND BYPASSING

Proper signal and grounding techniques must be applied in board layout so that specified performance levels of precision data acquisition components, such as the AD526, are not degraded.

As is shown in Figure 37, logic and signal grounds should be separate. By connecting the signal source ground locally to the AD526 analog ground Pins 5 and 6, gain accuracy of the AD526 is maintained. This ground connection should not be corrupted by currents associated with other elements within the system.

Utilizing the force and sense outputs of the AD526, as shown in Figure 38, avoids signal drops along etch runs to low impedance loads.

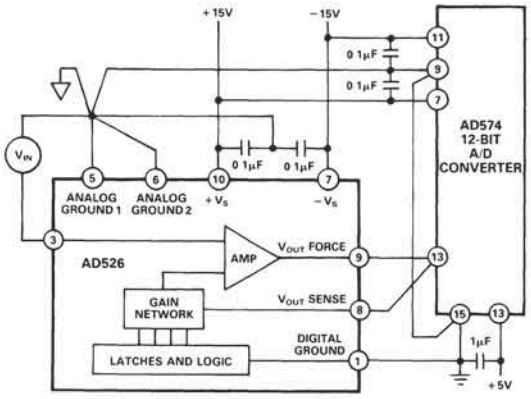


Figure 37. Grounding and Bypassing

CASCADED OPERATION

A cascade of two AD526s can be used to achieve binarily weighted gains from 1 to 256. If gains from 1 to 128 are needed, no additional components are required. This is accomplished by using the B pin as shown in Figure 38. When the B pin is low, the AD526 is held in a unity gain stage independent of the other gain code values.

V_{OUT}/V_{IN}	A2	A1	A0
1	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
16	1	0	0
32	1	0	1
64	1	1	0
128	1	1	1

Table II. Logic Table for Figure 38

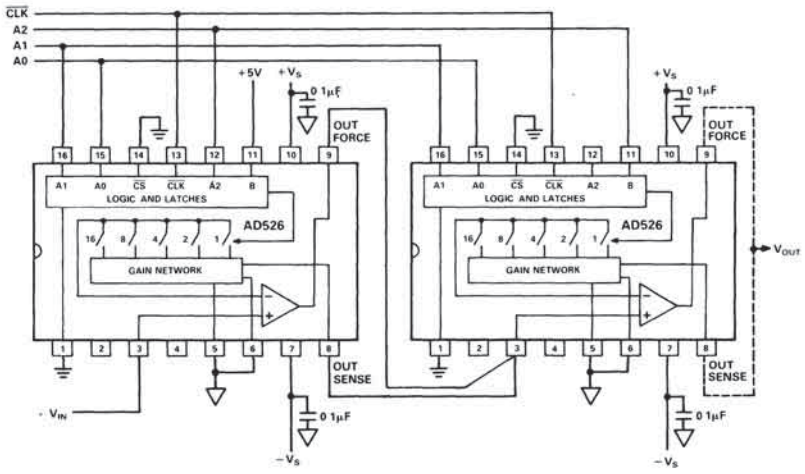


Figure 38. Cascaded Operation

OFFSET NULLING

Input voltage offset nulling of the AD526 is best accomplished at a gain of 16, since the referred-to-input (RTI) offset is amplified the most at this gain and therefore is most easily trimmed. The resulting trimmed value of RTI voltage offset typically varies less than 3μV across all gain ranges.

Note that the low input current of the AD526 minimizes RTI voltage offsets due to source resistance.

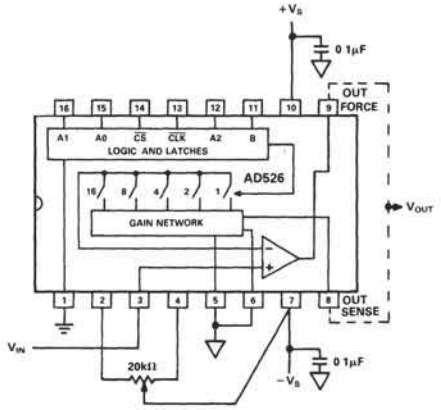


Figure 39. Offset Voltage Null Circuit

OUTPUT CURRENT BOOSTER

The AD526 is rated for a full ±10V output voltage swing into 2kΩ. In some applications, the need exists to drive more current into heavier loads. As shown in Figure 40, a high current booster may be connected "inside the loop" of the SPGA to provide the required current boost without significantly degrading overall performance. Nonlinearities, offset and gain inaccuracies of the buffer are minimized by the loop gain of the AD526 output amplifier.

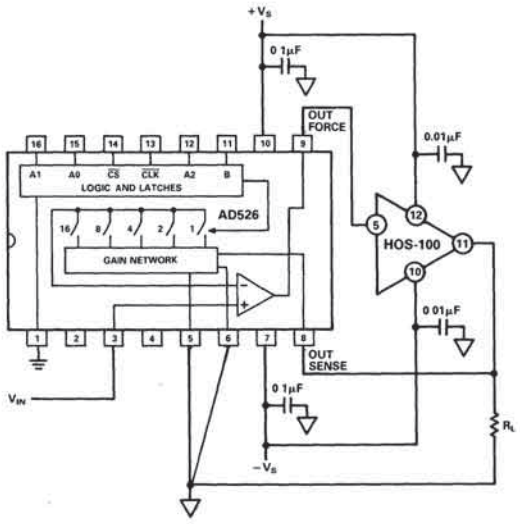


Figure 40. Current Output Boosting

OFFSET NULLING WITH A D/A CONVERTER

Figure 41 shows the AD526 with offset nulling accomplished with an 8-bit D/A converter (AD7524) circuit instead of the potentiometer shown in Figure 39. The calibration procedure is the same as before except that instead of adjusting the potentiometer, the D/A converter corrects for the offset error. This calibration circuit has a number of benefits in addition to eliminating the trimpot. The most significant benefit is that calibration can be under the control of a microprocessor and therefore can be implemented as part of an autocalibration scheme. Secondly, dipswitches or RAM can be used to hold the 8-bit word after its value has been determined. In Figure 42 the offset null sensitivity, at a gain of 16, is 80μV per LSB of adjustment, which guarantees dc accuracy to the 16-bit performance level.

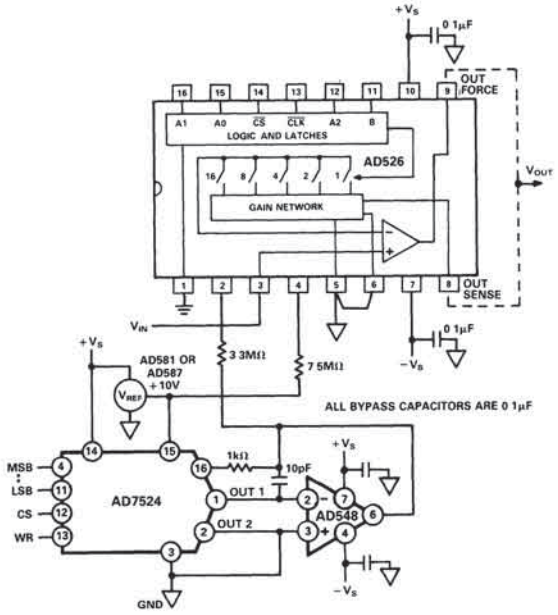


Figure 41. Offset Nulling Using a DAC

FLOATING-POINT CONVERSION

High resolution converters are used in systems to obtain high accuracy, improve system resolution or increase dynamic range. There are a number of high resolution converters available with throughput rates of 66.6kHz that can be purchased as a single component solution; however in order to achieve higher throughput rates, alternative conversion techniques must be employed. A floating point A/D converter can improve both throughput rate and dynamic range of a system.

In a floating point A/D converter (Figure 42), the output data is presented as a 16-bit word, the lower 12 bits from the A/D converter form the mantissa and the upper 4 bits from the digital signal used to set the gain form the exponent. The AD526 programmable gain amplifier in conjunction with the comparator circuit scales the input signal to a range between half scale and full scale for the maximum usable resolution.

The A/D converter diagrammed in Figure 42 consists of a pair of AD585 sample/hold amplifiers, a flash converter, a five-range programmable gain amplifier (the AD526) and a fast 12-bit A/D converter (the AD7572). The floating-point A/D converter achieves its high throughput rate of 125kHz by overlapping the acquisition time of the first sample/hold amplifier and the settling time of the AD526 with the conversion time of the A/D converter. The first sample/hold amplifier holds the signal for the flash autoranger, which determines which binary quantum the input falls within, relative to full scale. Once the AD526 has settled to the appropriate level, then the second sample/hold amplifier can be put into hold which holds the amplified signal while the AD7572 performs its conversion routine. The acquisition time for the AD585 is 3μs, and the conversion time for the AD7572 is 5μs for a total of 8μs, or 125kHz. This performance relies on the fast settling characteristics of the AD526 after the flash autoranging (comparator) circuit quantizes the input signal. A 16-bit register holds the 3-bit output from the flash autoranger and the 12-bit output of the AD7572.

The A/D converter in Figure 42 has a dynamic range of 96dB. The dynamic range of a converter is the ratio of the full-scale input range to the LSB value. With a floating-point A/D converter the smallest value LSB corresponds to the LSB of the monolithic converter divided by the maximum gain of the PGA. The floating point A/D converter has a full-scale range of 5V, a maximum gain of 16V/V from the AD526 and a 12-bit A/D converter; this produces:

LSB = ([FSR/2^N]/Gain) = ([5V/4096]/16) = 76μV. The dynamic range in dBs is based on the log of the ratio of the full-scale input range to the LSB; dynamic range = 20log(5V/76μV) = 96dB.

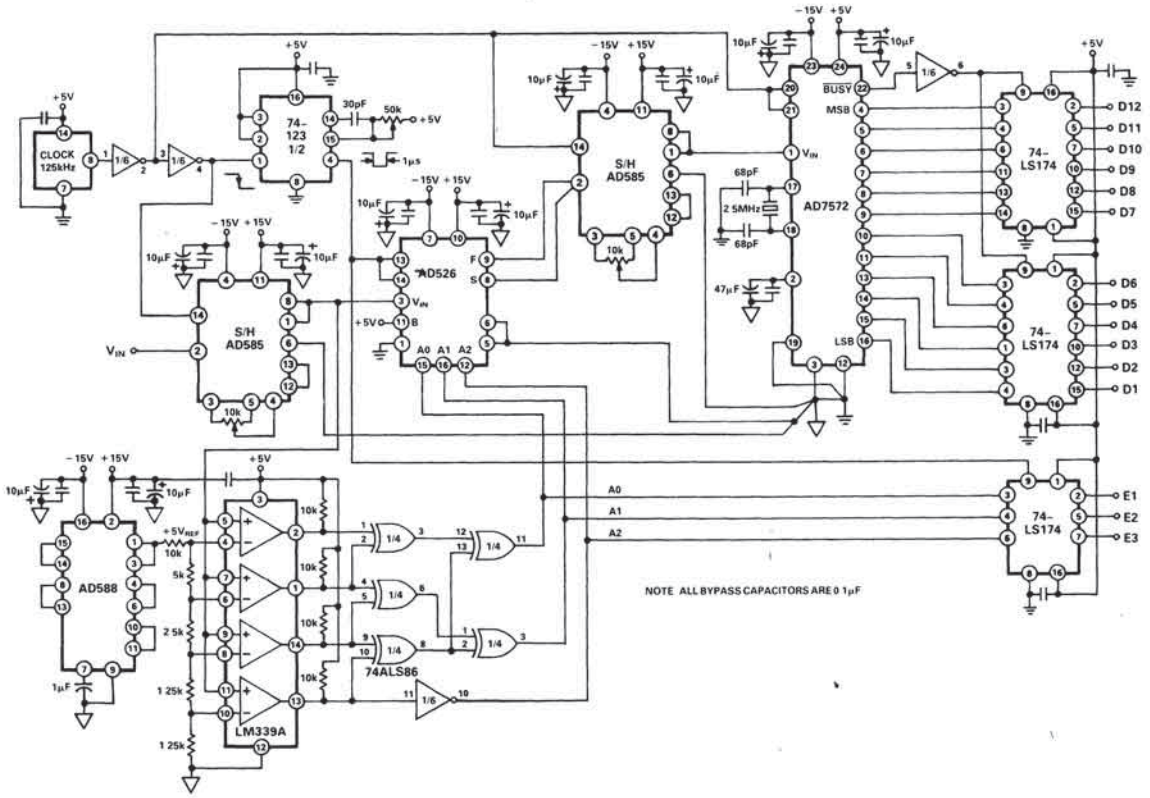


Figure 42. Floating-Point A/D Converter

HIGH ACCURACY A/D CONVERTERS

Very high accuracy and high resolution floating-point A/D converters can be achieved by the incorporation of offset and gain calibration routines. There are two techniques commonly used for calibration, a hardware circuit as shown in Figure 43 and/or a software routine. In this application the microprocessor is functioning as the autoranging circuit, requiring software overhead; therefore, a hardware calibration technique was applied which reduces the software burden. The software is used to set the gain of the AD526. In operation the signal is converted, and if the MSB of the AD574 is not equal to a logical 1, the gain is increased by binary steps, up to the maximum gain. This maximizes the full-scale range of the conversion process and insures a wide dynamic range.

The calibration technique uses two point correction, offset and gain. The hardware is simplified by the use of programmable magnitude comparators, the 74ALS528s, which can be "burned" for a particular code. In order to prevent under or over range hunting during the calibration process, the reference offset and gain codes should be different from the endpoint codes. A calibration cycle consists of selecting whether gain or offset is to be calibrated then selecting the appropriate multiplexer channel to apply the reference voltage to the signal channel. Once the operation has been initiated, the counter, a 74ALS869, drives the D/A converter in a linear fashion providing a small correction voltage to either the gain or offset trim point of the AD574. The output of the A/D converter is then compared to the value preset in the 74ALS528 to determine a match. Once a match is detected, the 74ALS528 produces a low going pulse which stops the counter. The code at the D/A converter is latched until the next calibration cycle. Calibration cycles are under the control of the microprocessor in this application and should be implemented only during periods of converter inactivity.

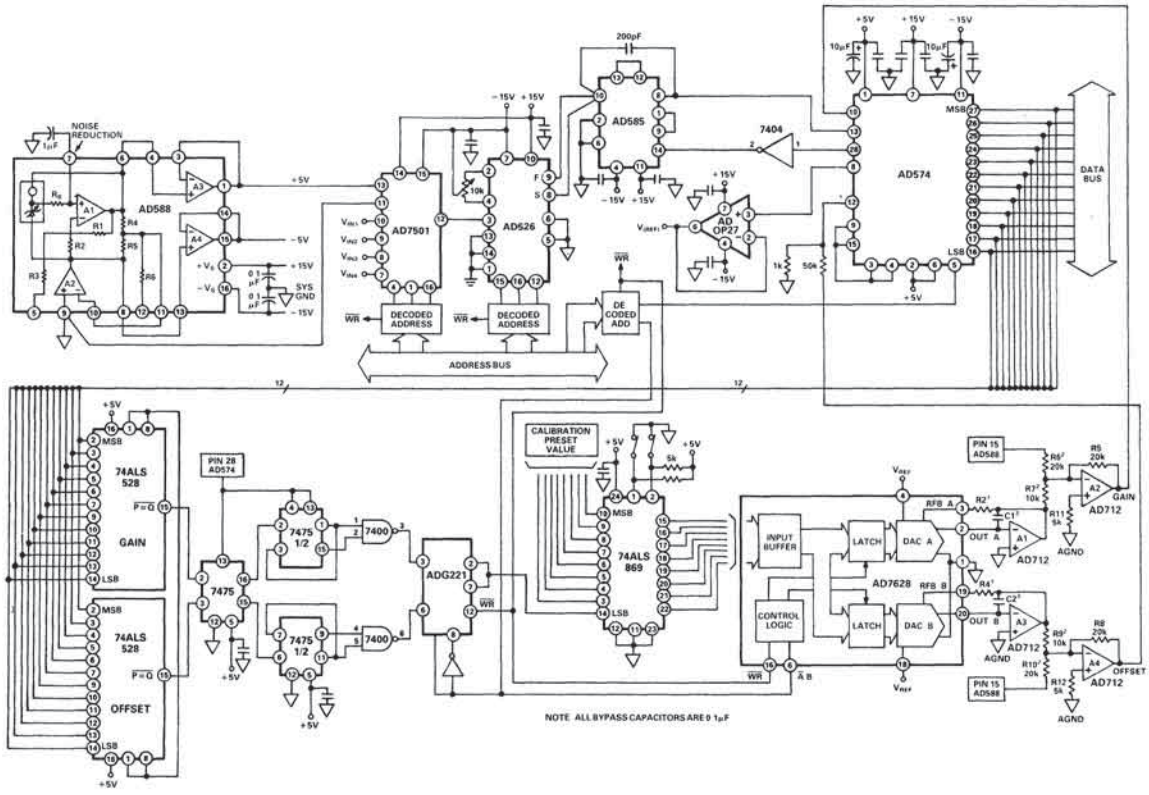


Figure 43. High Accuracy A/D Converter

ANALOG DEVICES

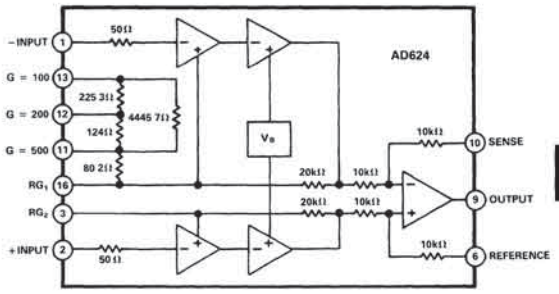
Precision Instrumentation Amplifier

AD624

FEATURES

Low Noise: 0.2μV p-p 0.1Hz to 10Hz
Low Gain TC: 5ppm max (G = 1)
Low Nonlinearity: 0.001% max (G = 1 to 200)
High CMRR: 130dB min (G = 500 to 1000)
Low Input Offset Voltage: 25μV, max
Low Input Offset Voltage Drift: 0.25μV/°C max
Gain Bandwidth Product: 25MHz
Pin Programmable Gains of 1, 100, 200, 500, 1000
No External Components Required
Internally Compensated

AD624 FUNCTIONAL BLOCK DIAGRAM



4

PRODUCT DESCRIPTION

The AD624 is a high precision low noise instrumentation amplifier designed primarily for use with low level transducers, including load cells, strain gauges and pressure transducers. An outstanding combination of low noise, high gain accuracy, low gain temperature coefficient and high linearity make the AD624 ideal for use in high resolution data acquisition systems.

The AD624C has an input offset voltage drift of less than 0.25μV/°C, output offset voltage drift of less than 10μV/°C, CMRR above 80dB at unity gain (130dB at G=500) and a maximum nonlinearity of 0.001% at G=1. In addition to these outstanding dc specifications the AD624 exhibits superior ac performance as well. A 25MHz gain bandwidth product, 5V/μs slew rate and 15μs settling time permit the use of the AD624 in high speed data acquisition applications.

The AD624 does not need any external components for pre-trimmed gains of 1, 100, 200, 500 and 1000. Additional gains such as 250 and 333 can be programmed within one percent accuracy with external jumpers. A single external resistor can also be used to set the 624's gain to any value in the range of 1 to 10,000.

PRODUCT HIGHLIGHTS

1. The AD624 offers outstanding noise performance. Input noise is typically less than 4nV/$\sqrt{\text{Hz}}$ at 1kHz.
2. The AD624 is a functionally complete instrumentation amplifier. Pin programmable gains of 1, 100, 200, 500 and 1000 are provided on the chip. Other gains are achieved through the use of a single external resistor.
3. The offset voltage, offset voltage drift, gain accuracy and gain temperature coefficients are guaranteed for all pre-trimmed gains.
4. The AD624 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effect of offset voltage in gain ranging applications.
5. A sense terminal is provided to enable the user to minimize the errors induced through long leads. A reference terminal is also provided to permit level shifting at the output.

SPECIFICATIONS (@ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

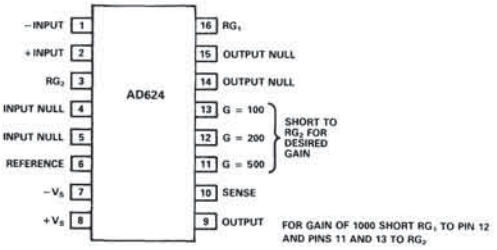
Model	AD624A			AD624B			AD624C			AD624S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN													
Gain Equation (External Resistor Gain Programming)		$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$			$\left[\frac{40{,}000}{R_G}+1\right]\pm 20\%$		
Gain Range (Pin Programmable)		1 to 1000			1 to 1000			1 to 1000			1 to 1000		
Gain Error													
G = 1			±0.05			±0.03			±0.02			±0.05	%
G = 100			±0.25			±0.15			±0.1			±0.25	%
G = 200, 500			±0.5			±0.35			±0.25			±0.5	%
G = 1000			±1.0			±1.0			±1.0			±1.0	%
Nonlinearity													
G = 1			±0.005			±0.003			±0.001			±0.005	%
G = 100, 200			±0.005			±0.003			±0.001			±0.005	%
G = 500, 1000			±0.005			±0.005			±0.005			±0.005	%
Gain vs. Temperature													
G = 1			5			5			5			5	ppm/°C
G = 100, 200			10			10			10			10	ppm/°C
G = 500, 1000			25			15			15			15	ppm/°C
VOLTAGE OFFSET (May be Nulled)													
Input Offset Voltage			200			75			25			75	µV
vs. Temperature			2			0.5			0.25			2.0	µV/°C
Output Offset Voltage			5			3			2			3	mV
vs. Temperature			50			25			10			50	µV/°C
Offset Referred to the Input vs. Supply													
G = 1	70			75			80			75			dB
G = 100, 200	95			105			110			105			dB
G = 500, 1000	100			110			115			110			dB
INPUT CURRENT													
Input Bias Current			±50			±25			±15			±50	nA
vs. Temperature		±50			±50			±50			±50		pA/°C
Input Offset Current			±35			±15			±10			±35	nA
vs. Temperature		±20			±20			±20			±20		pA/°C
INPUT													
Input Impedance													
Differential Resistance		10^9			10^9			10^9			10^9		Ω
Differential Capacitance		10			10			10			10		pF
Common-Mode Resistance		10^9			10^9			10^9			10^9		Ω
Common-Mode Capacitance		10			10			10			10		pF
Input Voltage Range													
Max Differ. Input Linear (V_D)		±10			±10			±10			±10		V
Max Common-Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		V
Common-Mode Rejection dc to 60Hz with 1kΩ Source Imbalance													
G = 1	70			75			80			70			dB
G = 100, 200	100			105			110			100			dB
G = 500, 1000	110			120			130			110			dB
OUTPUT RATING													
V_{OUT}, R_L = 2kΩ		±10			±10			±10			±10		V
DYNAMIC RESPONSE													
Small Signal −3dB													
G = 1		1			1			1			1		MHz
G = 100		150			150			150			150		kHz
G = 200		100			100			100			100		kHz
G = 500		50			50			50			50		kHz
G = 1000		25			25			25			25		kHz

Model	AD624A Min	AD624A Typ	AD624A Max	AD624B Min	AD624B Typ	AD624B Max	AD624C Min	AD624C Typ	AD624C Max	AD624S Min	AD624S Typ	AD624S Max	Units
Slew Rate		5 0			5 0			5 0			5.0		V/μs
Settling Time to 0.01%, 20V Step													
G = 1 to 200		15			15			15			15		μs
G = 500		35			35			35			35		μs
G = 1000		75			75			75			75		μs
NOISE													
Voltage Noise, 1kHz													
R T.I.		4			4			4			4		nV/√Hz
R T O.		75			75			75			75		nV/√Hz
R.T I , 0.1 to 10Hz													
G = 1		10			10			10			10		μV p-p
G = 100		0.3			0 3			0 3			0 3		μV p-p
G = 200, 500, 1000		0 2			0 2			0 2			0 2		μV p-p
Current Noise													
0.1Hz to 10Hz		60			60			60			60		pA p-p
SENSE INPUT													
R_{IN}	8	10	12	8	10	12	8	10	12	8	10	12	kΩ
I_{IN}		30			30			30			30		μA
Voltage Range	± 10			± 10			± 10			± 10			V
Gain to Output		1			1			1			1		%
REFERENCE INPUT													
R_{IN}	16	20	24	16	20	24	16	20	24	16	20	24	kΩ
I_{IN}		30			30			30			30		μA
Voltage Range	± 10			± 10			± 10			± 10			V
Gain to Output		1			1			1			1		%
TEMPERATURE RANGE													
Specified Performance	− 25		+ 85	− 25		+ 85	− 25		+ 85	− 55		+ 125	°C
Storage	− 65		+ 150	− 65		+ 150	− 65		+ 150	− 65		+ 150	°C
POWER SUPPLY													
Power Supply Range	**± 6**	± 15	**± 18**	**± 6**	± 15	**± 18**	**± 6**	± 15	**± 18**	**± 6**	± 15	**± 18**	V
Quiescent Current		3 5	5		3.5	5		3 5	5		3 5	5	mA
PACKAGE[1]													
Ceramic (D-16)		AD624A			AD624B			AD624C			AD624S		

NOTES
[1]See Section 16 for package outline information
Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units

PIN CONFIGURATION



Typical Characteristics

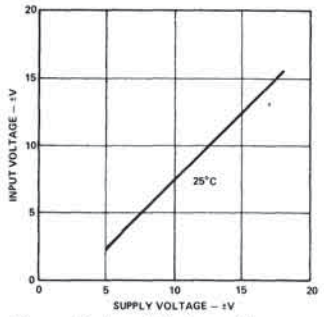


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

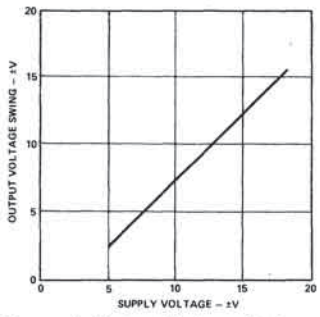


Figure 2. Output Voltage Swing vs. Supply Voltage

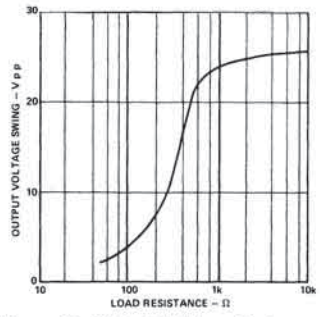


Figure 3. Output Voltage Swing vs. Resistive Load

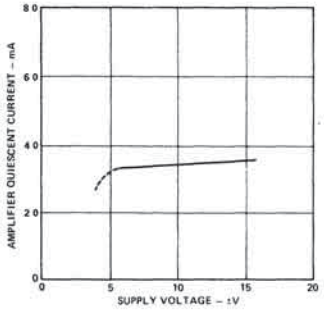


Figure 4. Quiescent Current vs. Supply Voltage

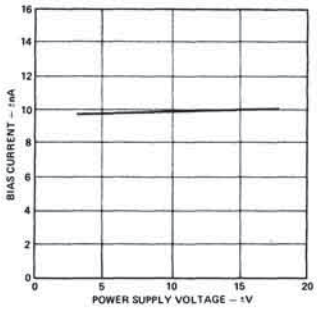


Figure 5. Input Bias Current vs. Supply Voltage

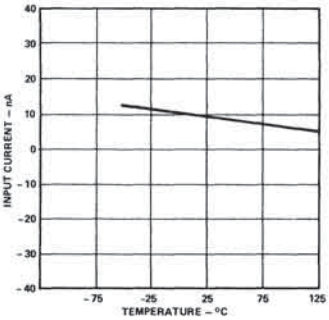


Figure 6. Input Bias Current vs. Temperature

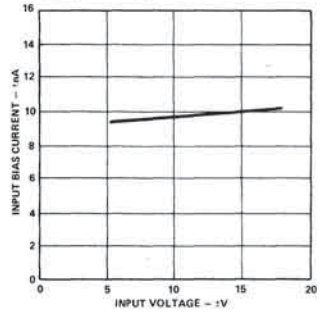


Figure 7. Input Bias Current vs. CMV

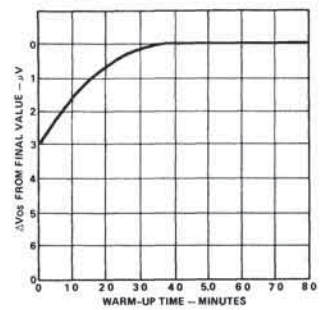


Figure 8. Offset Voltage, RTI, Turn On Drift

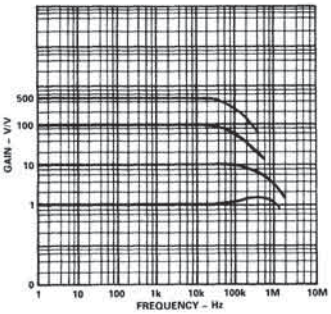


Figure 9. Gain vs. Frequency

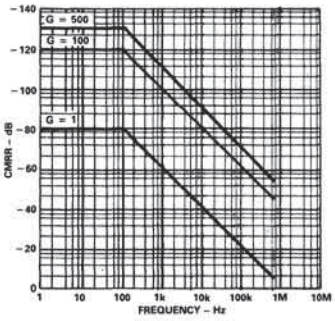


Figure 10. CMRR vs. Frequency RTI, Zero to 1k Source Imbalance

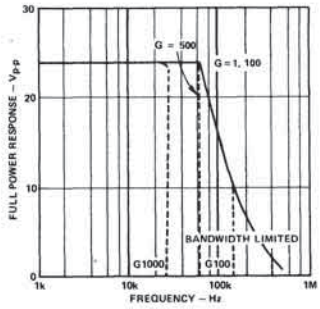


Figure 11. Large Signal Frequency Response

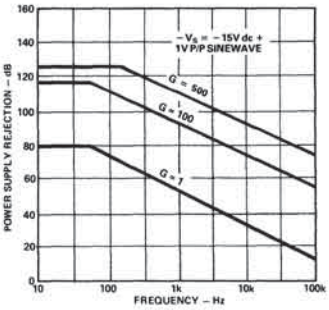


Figure 12. Positive PSRR vs. Frequency

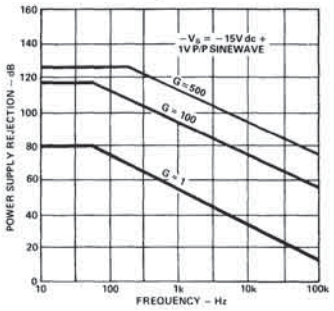


Figure 13. Negative PSRR vs. Frequency

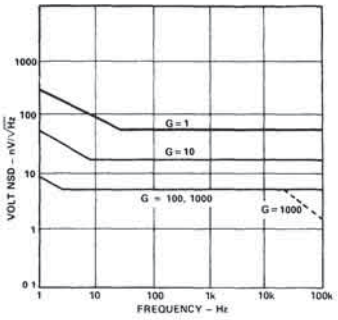


Figure 14. RTI Noise Spectral Density vs. Gain

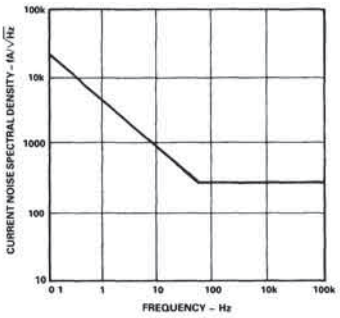


Figure 15. Input Current Noise

4

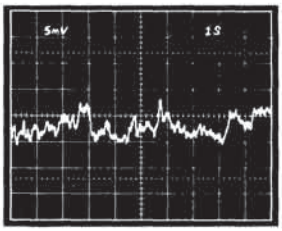


Figure 16. Low Frequency Voltage Noise – G = 1 (System Gain = 1000)

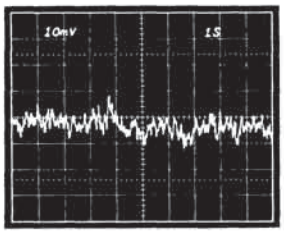


Figure 17. Low Frequency Voltage Noise – G = 1000 (System Gain = 100,000)

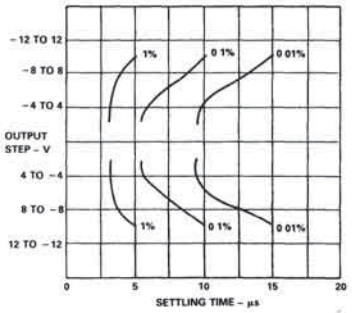


Figure 18. Settling Time Gain = 1

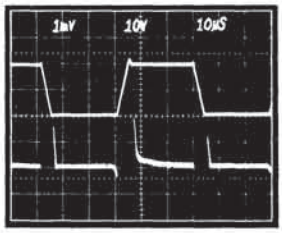


Figure 19. Large Signal Pulse Response and Settling Time – G = 1

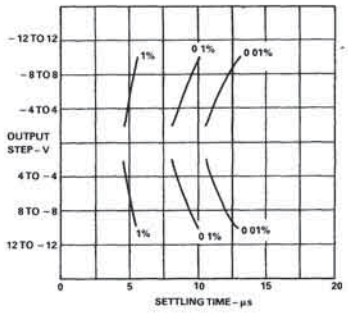


Figure 20. Settling Time Gain = 100

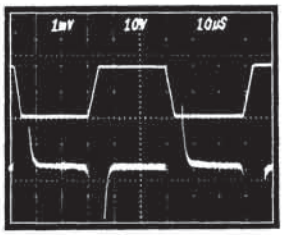


Figure 21. Large Signal Pulse Response and Settling Time G = 100

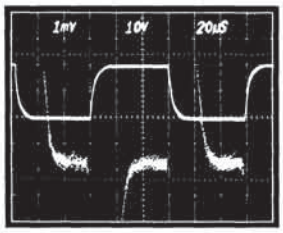


Figure 22. Range Signal Pulse Response and Settling Time G = 500

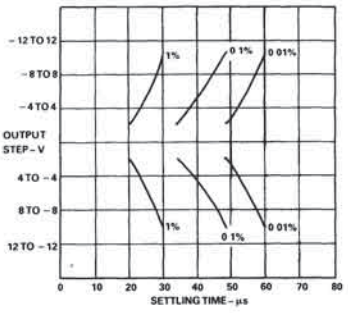


Figure 23. Settling Time Gain = 1000

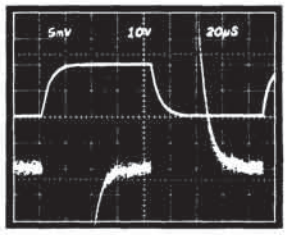


Figure 24. Large Signal Pulse Response and Settling Time G = 1000

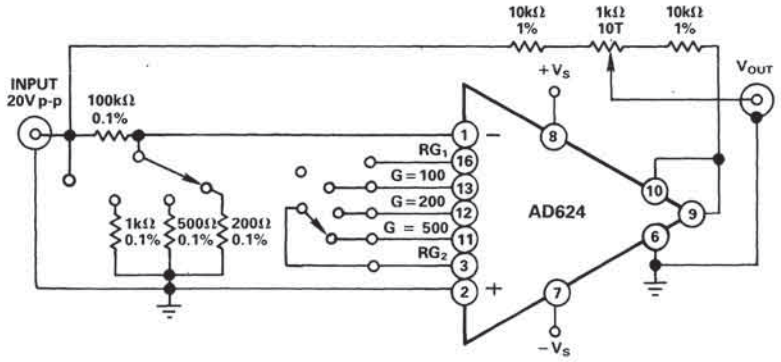


Figure 25. Settling Time Test Circuit

Theory of Operation

The AD624 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp instrumentation amplifier. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components and the high level of performance that this circuit architecture is capable of.

A preamp section (Q1–Q4) develops the programmed gain by the use of feedback concepts. Feedback from the outputs of A1 and A2 forces the collector currents of Q1–Q4 to be constant thereby impressing the input voltage across R_G.

The gain is set by choosing the value of R_G from the equation, Gain $= \frac{40k}{R_G} + 1$. The value of R_G also sets the transconductance of the input preamp stage increasing it asymptotically to the transconductance of the input transistors as R_G is reduced for larger gains. This has three important advantages. First, this approach allows the circuit to achieve a very high open loop gain of 3×10^8 at a programmed gain of 1000 thus reducing gain related errors to a negligible 3ppm. Second, the gain bandwidth product which is determined by C3 or C4 and the input transconductance, reaches 25MHz. Third, the input voltage noise reduces to a value determined by the collector current of the input transistors for an RTI noise of $4nV/\sqrt{Hz}$ at $G \geq 500$.

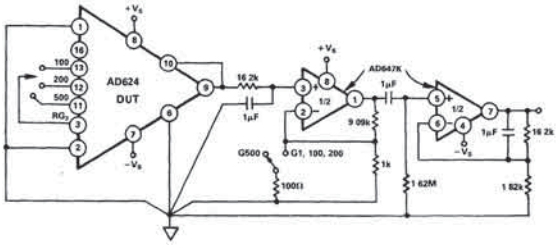


Figure 26. Noise Test Circuit

INPUT CONSIDERATIONS

Under input overload conditions the user will see $R_G + 100\Omega$ and two diode drops (~1.2V) between the plus and minus inputs, in either direction. If safe overload current under all conditions is assumed to be 10mA, the maximum overload voltage is ~ ±2.5V. While the AD624 can withstand this continuously, momentary overloads of ±10V will not harm the device. On the other hand the inputs should never exceed the supply voltage.

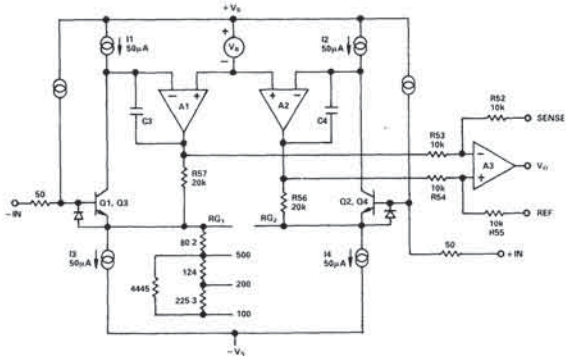


Figure 27. Simplified Circuit of Amplifier; Gain is Defined as ((R56 + R57)/(R_G) + 1. For a Gain of 1, R_G is an Open Circuit.

The AD524 should be considered in applications that require protection from severe input overload. If this is not possible, external protection resistors can be put in series with the inputs of the AD624 to augment the internal (50Ω) protection resistors. This will most seriously degrade the noise performance. For this reason the value of these resistors should be chosen to be as low as possible and still provide 10mA of current limiting under maximum continuous overload conditions. In selecting the value of these resistors, the internal gain setting resistor and the 1.2 volt drop need to be considered. For example, to protect the device from a continuous differential overload of 20V at a gain of 100, 1.9kΩ of resistance is required. The internal gain resistor is 404Ω; the internal protect resistor is 100Ω. There is a 1.2V drop across D1 or D2 and the base-emitter junction of either Q1 and Q3 or Q2 and Q4 as shown in Figure 27, 1400Ω of external resistance would be required (700Ω in series with each input). The RTI noise in this case would be $\sqrt{4KTR_{ext.} + (4nV/\sqrt{Hz})^2} = 6.2nV/\sqrt{Hz}$.

INPUT OFFSET AND OUTPUT OFFSET

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and offset drift each have two components; input and output. Input offset is that component of offset that is

directly proportional to gain i.e., input offset as measured at the output at G = 100 is 100 times greater than at G = 1. Output offset is independent of gain. At low gains, output offset drift is dominant, while at high gains input offset drift dominates. Therefore, the output offset voltage drift is normally specified as drift at G = 1 (where input effects are insignificant), while input offset voltage drift is given by drift specification at a high gain (where output offset effects are negligible). All input-related numbers are referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Voltage offset vs. power supply is also specified at one or more gain settings and is also RTI.

By separating these errors, one can evaluate the total error independent of the gain setting used. In a given gain configuration both errors can be combined to give a total error referred to the input (R.T.I.) or output (R.T.O.) by the following formula:

Total Error R.T.I. = input error + (output error/gain)

Total Error R.T.O. = (Gain × input error) + output error

As an illustration, a typical AD624 might have a +250μV output offset and a −50μV input offset. In a unity gain configuration, the *total* output offset would be 200μV or the sum of the two. At a gain of 100, the output offset would be −4.75mV or: +250μV + 100(−50μV) = −4.75mV.

The AD624 provides for both input and output offset adjustment. This optimizes nulling in very high precision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1.

GAIN

The AD624 includes high accuracy pre-trimmed internal gain resistors. These allow for single connection programming of gains of 1, 100, 200 and 500. Additionally, a variety of gains including a pre-trimmed gain of 1000 can be achieved through series and parallel combinations of the internal resistors. Table I shows the available gains and the appropriate pin connections and gain temperature coefficients.

The gain values achieved via the combination of internal resistors are extremely useful. The temperature coefficient of the gain is dependent primarily on the mismatch of the temperature coefficients of the various internal resistors. Tracking of these resistors is extremely tight resulting in the low gain TC's shown in Table I.

If the desired value of gain is not attainable using the internal resistors, a single external resistor can be used to achieve any gain between 1 and 10,000. This resistor connected between

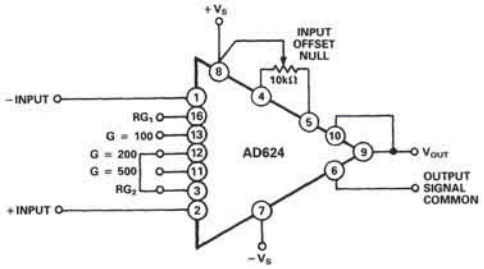


Figure 28. Operating Connections for G = 200

Gain (Nominal)	Temperature Coefficient (Nominal)	Pin 3 to Pin	Connect Pins
1	−1.5ppm/°C	–	–
100	−1.5ppm/°C	13	–
125	−5ppm/°C	13	11 to 16
137	−5.5ppm/°C	13	11 to 12
186.5	−6.5ppm/°C	13	11 to 12 to 16
200	−3.5ppm/°C	12	–
250	−5.5ppm/°C	12	11 to 13
333	−15ppm/°C	12	11 to 16
375	−0.5ppm/°C	12	13 to 16
500	−10ppm/°C	11	–
624	−5ppm/°C	11	13 to 16
688	−1.5ppm/°C	11	11 to 12; 13 to 16
831	+4ppm/°C	11	16 to 12
1000	0ppm/°C	11	16 to 12; 13 to 11

Table I.

pins 3 and 16 programs the gain according to the formula $R_G = \frac{40k}{G-1}$ (see Figure 29). For best results R_G should be a precision resistor with a low temperature coefficient. An external R_G affects both gain accuracy and gain drift due to the mismatch between it and the internal thin-film resistors R56 and R57. Gain accuracy is determined by the tolerance of the external R_G and the absolute accuracy of the internal resistors (±20%). Gain drift is determined by the mismatch of the temperature coefficient of R_G and the temperature coefficient of the internal resistors (−15ppm/°C typ), and the temperature coefficient of the internal interconnections.

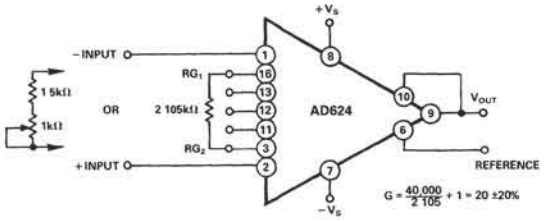


Figure 29. Operating Connections for G = 20

The AD624 may also be configured to provide gain in the output stage. Figure 30 shows an H pad attenuator connected to the reference and sense lines of the AD624. The values of R1, R2 and R3 should be selected to be as low as possible to minimize the gain variation and reduction of CMRR. Varying R2 will precisely set the gain without affecting CMRR. CMRR is determined by the match of R1 and R3.

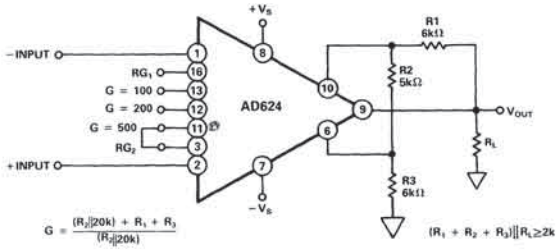


Figure 30. Gain of 2500

NOISE

The AD624 is designed to provide noise performance near the theoretical noise floor. This is an extremely important design criteria as the front end noise of an instrumentation amplifier is the ultimate limitation on the resolution of the data acquisition system it is being used in. There are two sources of noise in an instrument amplifier, the input noise, predominantly generated by the differential input stage, and the output noise, generated by the output amplifier. Both of these components are present at the input (and output) of the instrumentation amplifier. At the input, the input noise will appear unaltered; the output noise will be attenuated by the closed loop gain (at the output, the output noise will be unaltered; the input noise will be amplified by the closed loop gain). Those two noise sources must be root sum squared to determine the total noise level expected at the input (or output).

The low frequency (0.1 to 10Hz) voltage noise due to the output stage is 10μV p-p, the contribution of the input stage is 0.2μV p-p. At a gain of 10, the RTI voltage noise would be 1μV p-p, $\sqrt{\left(\frac{10}{G}\right)^2 + (0.2)^2}$. The RTO voltage noise would be 10.2μV p-p, $\sqrt{10^2 + (0.2\ (G))^2}$. These calculations hold for applications using either internal or external gain resistors.

INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. Bias currents are an additional source of input error and must be considered in an total error budget. The bias currents when multiplied by the source resistance imbalance appear as an additional offset voltage. (What is of concern in calculating bias current errors is the change in bias current with respect to signal voltage and temperature.) Input offset current is the difference between the two input bias currents. The effect of offset current is an input offset voltage whose magnitude is the offset current times the source resistance.

Although instrumentation amplifiers have differential inputs, there must be a return path for the bias currents. If this is not provided, those currents will charge stray capacitances, causing the output to drift uncontrollably or to saturate. Therefore, when amplifying "floating" input sources such as transformers and thermocouples, as well as ac-coupled sources, there must still be a dc path from each input to ground, (see Figure 31).

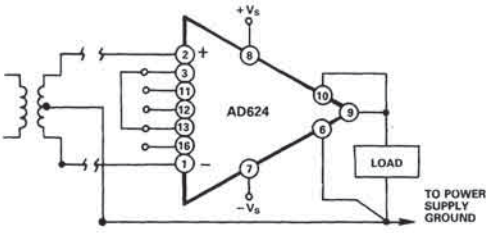


Figure 31a. Transformer Coupled

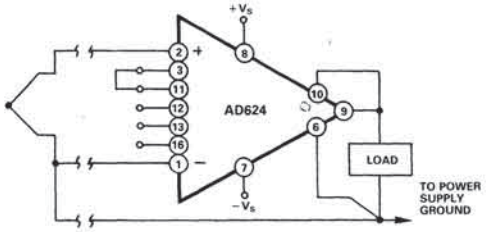


Figure 31b. Thermocouple

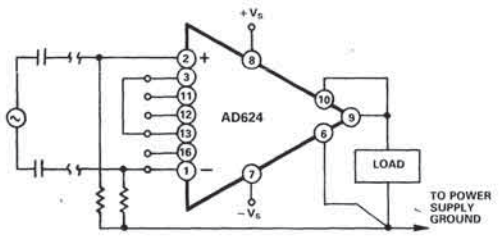


Figure 31c. AC Coupled

Figure 31. Indirect Ground Returns for Bias Currents

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance. "Common-Mode Rejection Ratio" (CMRR) is a ratio expression while "Common-Mode Rejection" (CMR) is the logarithm of that ratio. For example, a CMRR of 10,000 corresponds to a CMR of 80dB.

In an instrumentation amplifier, ac common-mode rejection is only as good as the differential phase shift. Degradation of ac common-mode rejection is caused by unequal drops across differing track resistances and a differential phase shift due to varied stray capacitances or cable capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figures 32 and 33 shows active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

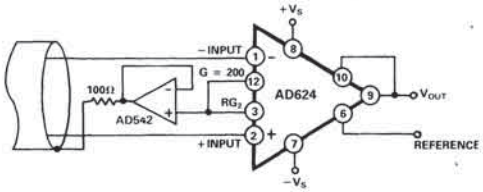


Figure 32. Shield Driver, G ≥ 100

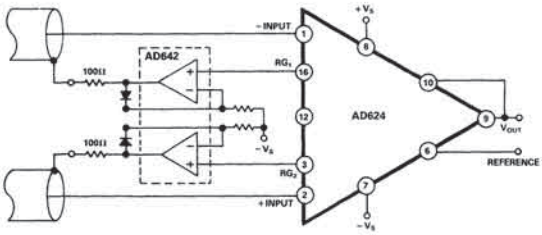


Figure 33. Differential Shield Driver

GROUNDING

Many data-acquisition components have two or more ground pins which are not connected together within the device. These grounds must be tied together at one point, usually at the system power supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the data acquisition components. Separate ground returns should be provided to

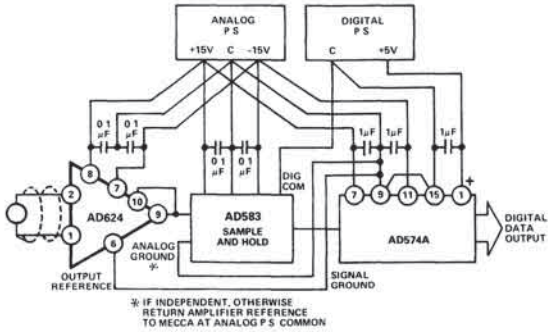


Figure 34. Basic Grounding Practice

minimize the current flow in the path from the most sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors (see Figure 34).

Since the output voltage is developed with respect to the potential on the reference terminal an instrumentation amplifier can solve many grounding problems.

SENSE TERMINAL

The sense terminal is the feedback point for the instrument amplifier's output amplifier. Normally it is connected to the instrument amplifier output. If heavy load currents are to be drawn through long leads, voltage drops due to current flowing through lead resistance can cause errors. The sense terminal can be wired to the instrument amplifier at the load thus putting the IxR drops "inside the loop" and virtually eliminating this error source.

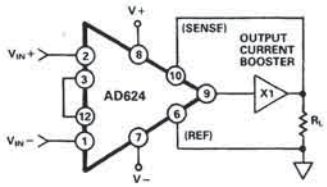


Figure 35. AD624 Instrumentation Amplifier with Output Current Booster

Typically, IC instrumentation amplifiers are rated for a full ±10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 35 shows how a current booster may be connected "inside the loop" of an instrumentation amplifier to provide the required current without significantly degrading overall performance. The effects of nonlinearities, offset and gain inaccuracies of the buffer are reduced by the loop gain of the IA output amplifier. Offset drift of the buffer is similarly reduced.

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ±10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. It must be remembered that the total output swing is ±10 volts, from ground, to be shared between signal and reference offset.

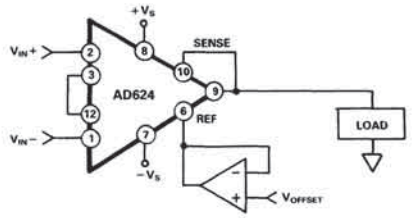


Figure 36. Use of Reference Terminal to Provide Output Offset

When the IA is of the three-amplifier configuration it is necessary that nearly zero impedance be presented to the reference terminal. Any significant resistance, including those caused by PC layouts or other connection techniques, which appears between the reference pin and ground will increase the gain of the noninverting signal path, thereby upsetting the common-mode rejection of the IA. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD624 a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB ($10k\Omega/1\Omega = 80dB$). An operational amplifier may be used to provide that low impedance reference point as shown in Figure 36. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 37.

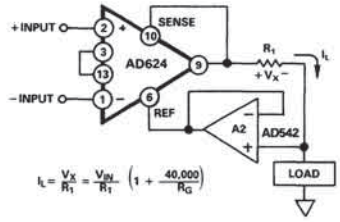


Figure 37. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A_2, the forced current I_L will largely flow through the load. Offset and drift specifications of A_2 must be added to the output offset and drift specifications of the IA.

PROGRAMMABLE GAIN

Figure 38 shows the AD624 being used as a software programmable gain amplifier. Gain switching can be accomplished with mechanical switches such as DIP switches or reed relays. It should be noted that the "on" resistance of the switch in series with the internal gain resistor becomes part of the gain equation and will have an effect on gain accuracy.

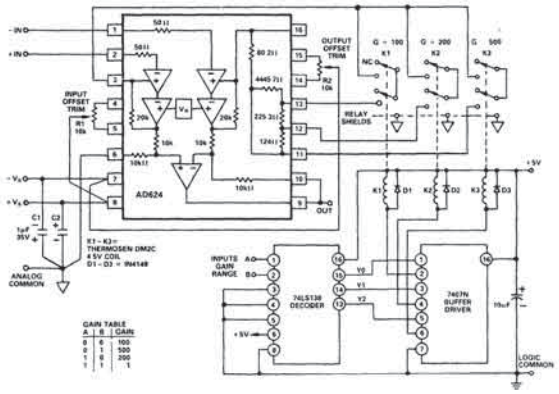


Figure 38. Gain Programmable Amplifier

A significant advantage in using the internal gain resistors in a programmable gain configuration is the minimization of thermocouple signals which are often present in multiplexed data acquisition systems.

If the full performance of the AD624 is to be achieved, the user must be extremely careful in designing and laying out his circuit to minimize the remaining thermocouple signals.

The AD624 can also be connected for gain in the output stage. Figure 39 shows an AD547 used as an active attenuator in the output amplifier's feedback loop. The active attenuation presents a very low impedance to the feedback resistors therefore minimizing the common-mode rejection ratio degradation.

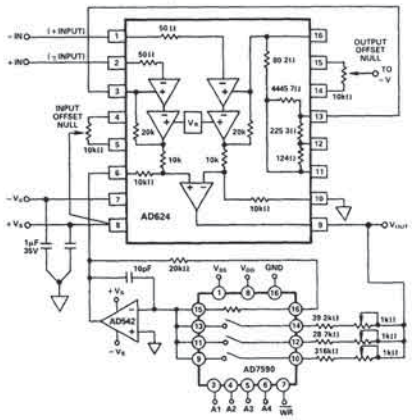


Figure 39. Programmable Output Gain

Another method for developing the switching scheme is to use a DAC. The AD7528 dual DAC which acts essentially as a pair of switched resistive attenuators having high analog linearity and symmetrical bipolar transmission is ideal in this application. The multiplying DAC's advantage is that it can handle inputs of either polarity or zero without affecting the programmed gain. The circuit shown uses an AD7528 to set the gain (DAC A) and to perform a fine adjustment (DAC B).

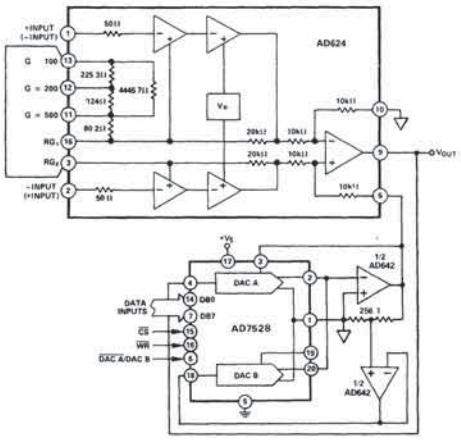


Figure 40. Programmable Output Gain Using a DAC

AUTO-ZERO CIRCUITS

In many applications it is necessary to provide very accurate data in high gain configurations. At room temperature the offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. The circuit of Figure 41 shows a CMOS DAC operating in the bipolar mode and connected to the reference terminal to provide software controllable offset adjustments.

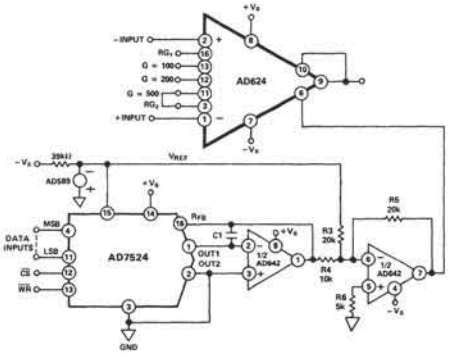


Figure 41. Software Controllable Offset

In many applications complex software algorithms for auto-zero applications are not available. For these applications Figure 42 provides a hardware solution.

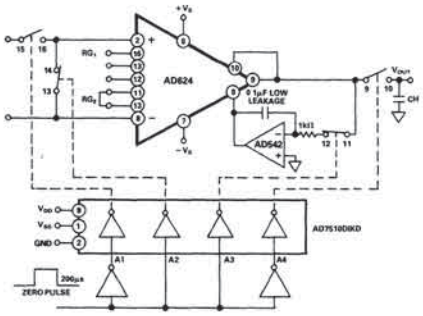


Figure 42. Auto-Zero Circuit

The microprocessor controlled data acquisition system shown in Figure 43 includes includes both auto-zero and auto-gain capability. By dedicating two of the differential inputs, one to ground and one to the A/D reference, the proper program calibration cycles can eliminate both initial accuracy errors and accuracy errors over temperature. The auto-zero cycle, in this application, converts a number that appears to be ground and then writes that same number (8 bit) to the AD7524 which eliminates the zero error since its output has an inverted scale. The auto-gain cycle converts the A/D reference and compares it with full scale. A multiplicative correction factor is then computed and applied to subsequent readings.

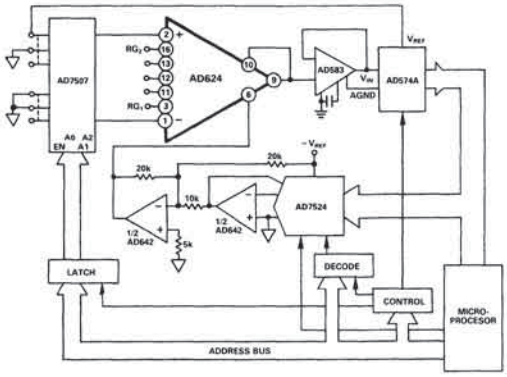


Figure 43. Microprocessor Controlled Data Acquisition System

WEIGH SCALE

Figure 44 shows an example of how an AD624 can be used to condition the differential output voltage from a load cell. The 10% reference voltage adjustment range is required to accommodate the 10% transducer sensitivity tolerance. The high linearity and low noise of the AD624 make it ideal for use in applications of this type particularly where it is desirable to measure small changes in weight as opposed to the absolute value. The addition of an auto gain/auto tare cycle will enable the system to remove offsets, gain errors, and drifts making possible true 14-bit performance.

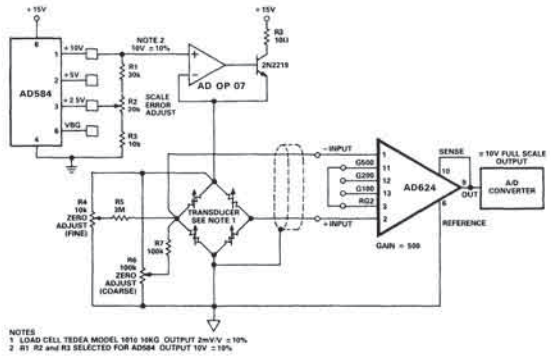


Figure 44. AD624 Weigh Scale Application

AC BRIDGE

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, l/f noise, dc drifts in the electronics, and line noise pick-up. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

Figure 45 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The oscilloscope photograph shows the results of a 0.05% bridge imbalance caused by the 1Meg resistor in parallel with one leg of the bridge. The top trace represents the bridge excitation, the upper middle trace is the amplified bridge output, the lower-middle trace is the output of the synchronous demodulator and the bottom trace is the filtered dc system output.

This system can easily resolve a 0.5ppm change in bridge impedance. Such a change will produce a 6.3mV change in the low pass filtered dc output, well above the RTO drifts and noise.

The AC-CMRR of the AD624 decreases with the frequency of the input signal. This is due mainly to the package-pin capacitance associated with the AD624's internal gain resistors. If AC-CMRR is not sufficient for a given application, it can be trimmed by using a variable capacitor connected to the amplifier's RG_2 pin as shown in Figure 45.

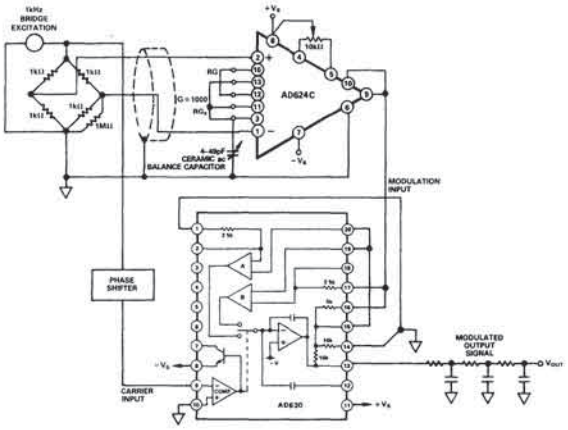


Figure 45. AC Bridge

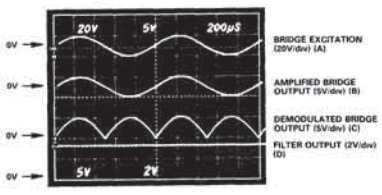


Figure 46. AC Bridge Waveforms

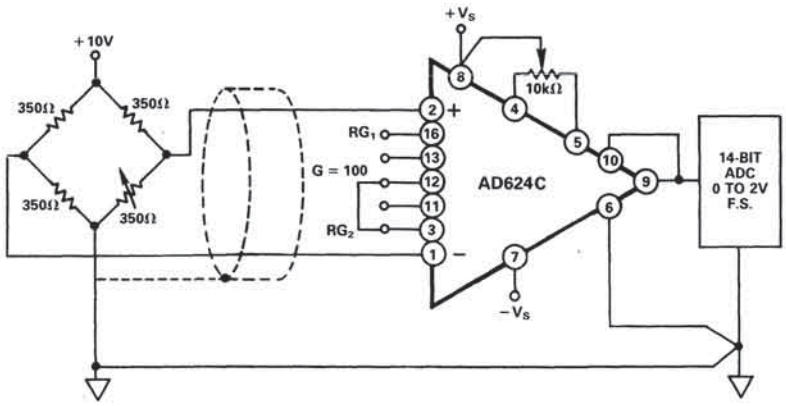


Figure 47. Typical Bridge Application

ERROR BUDGET ANALYSIS

To illustrate how instrumentation amplifier specifications are applied, we will now examine a typical case where an AD624 is required to amplify the output of an unbalanced transducer. Figure 47 shows a differential transducer, unbalanced by ≈5Ω, supplying a 0 to 20mV signal to an AD624C. The output of the IA feeds a 14-bit A to D converter with a 0 to 2 volt input voltage range. The operating temperature range is −25°C to +85°C. Therefore, the largest change in temperature ΔT within the operating range is from ambient to +85°C (85°C − 25°C = 60°C).

In many applications, differential linearity and resolution are of prime importance. This would be so in cases where the absolute value of a variable is less important than changes in value. In these applications, only the irreducible errors (20ppm = 0.002%) are significant. Furthermore, if a system has an intelligent processor monitoring the A to D output, the addition of a auto-gain/auto-zero cycle will remove all reducible errors and may eliminate the requirement for initial calibration. This will also reduce errors to 0.002%.

Error Source	AD624C Specifications	Calculation	Effect on Absolute Accuracy at T_A = 25°C	Effect on Absolute Accuracy at T_A = 85°C	Effect on Resolution
Gain Error	±0.1%	±0.1% = 1000ppm	1000ppm	1000ppm	–
Gain Instability	10ppm	(10ppm/°C)(60°C) = 600ppm	–	600ppm	–
Gain Nonlinearity	±0.001%	±0.001% = 10ppm	–	–	10ppm
Input Offset Voltage	±25μV, RTI	±25μV/20mV = ±1250ppm	1250ppm	1250ppm	–
Input Offset Voltage Drift	±0.25μV/°C	(±0.25μV/°C)(60°C) = 15μV 15μV/20mV = 750ppm	–	750ppm	–
Output Offset Voltage[1]	±2.0mV	±2.0mV/20mV = 1000ppm	1000ppm	1000ppm	–
Output Offset Voltage Drift[1]	±10μV/°C	(±10μV/°C)(60°C) = 600μV 600μV/20mV = 300ppm	–	300ppm	–
Bias Current – Source Imbalance Error	±15nA	(±15nA)(5Ω) = 0.075μV 0.075μV/20mV = 3.75ppm	3.75ppm	3.75ppm	–
Offset Current – Source Imbalance Error	±10nA	(±10nA)(5Ω) = 0.050μV 0.050μV/20mV = 2.5ppm	2.5ppm	2.5ppm	–
Offset Current – Source Resistance – Error	±10nA	(10nA)(175Ω) = 3.5μV 3.5μV/20mV = 87.5ppm	87.5ppm	87.5ppm	–
Offset Current – Source Resistance – Drift	±100pA/°C	(100pA/°C)(175Ω)(60°C) = 1μV 1μV/20mV = 50ppm	–	50ppm	–
Common Mode Rejection 5V dc	115dB	115dB = 1.8ppm × 5V = 9μV 9μV/20mV = 444ppm	450ppm	450ppm	–
Noise, RTI (0.1–10Hz)	0.22μV p-p	0.22μV p-p/20mV = 10ppm	–	–	10ppm
		Total Error	3793.75ppm	5493.75ppm	20ppm

[1]Output offset voltage and output offset voltage drift are given as RTI figures.

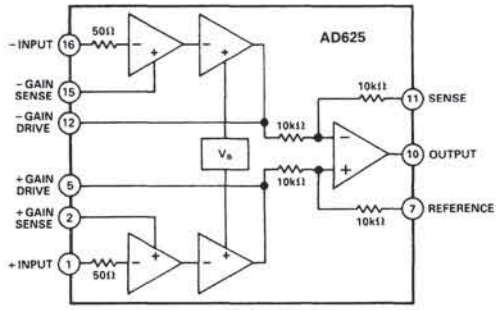
Table II. Error Budget Analysis of AD624CD in Bridge Application

Programmable Gain Instrumentation Amplifier

AD625

FEATURES
User Programmed Gains of 1 to 10,000
Low Gain Error: 0.02% max
Low Gain TC: 5ppm/°C max
Low Nonlinearity: 0.001% max
Low Offset Voltage: 25μV
Low Noise 4nV/√Hz (at 1kHz) RTI
Gain Bandwidth Product: 25MHz
16-Pin Ceramic or Plastic DIP Package
MIL-Standard Parts Available
Low Cost

AD625 FUNCTIONAL BLOCK DIAGRAM



4

PRODUCT DESCRIPTION

The AD625 is a precision instrumentation amplifier specifically designed to fulfill two major areas of application:
1) Circuits requiring nonstandard gains (i.e., gains not easily achievable with devices such as the AD524 and AD624).
2) Circuits requiring a low cost, precision software programmable gain amplifier.

For low noise, high CMRR, and low drift the AD625JN is the most cost effective instrumentation amplifier solution available. An additional three resistors allow the user to set any gain from 1 to 10,000. The error contribution of the AD625JN is less than 0.05% gain error and under 5ppm/°C gain TC; performance limitations are primarily determined by the external resistors. Common-mode rejection is independent of the feedback resistor matching.

A software programmable gain amplifier (SPGA) can be configured with the addition of a CMOS multiplexer (or other switch network), and a suitable resistor network. Because the ON resistance of the switches is removed from the signal path, an AD625 based SPGA will deliver 12-bit precision, and can be programmed for any set of gains between 1 and 10,000, with completely user selected gain steps.

For the highest precision the AD625C offers an input offset voltage drift of less than 0.25μV/°C, output offset drift below 15μV/°C, and a maximum nonlinearity of 0.001% at G = 1. All grades exhibit excellent ac performance; a 25MHz gain bandwidth product, 5Vμs slew rate and 15μs settling time.

The AD625 is available in three accuracy grades (A, B, C) for industrial (−25°C to +85°C) temperature range, two grades (J, K) for commercial (0 to +70°C) temperature range, and one (S) grade rated over the extended (−55°C to +125°C) temperature range.

PRODUCT HIGHLIGHTS

1. The AD625 affords up to 16-bit precision for user selected fixed gains from 1 to 10,000. Any gain in this range can be programmed by 3 external resistors.
2. A 12-bit software programmable gain amplifier can be configured using the AD625, a CMOS multiplexer and a resistor network. Unlike previous instrumentation amplifier designs, the ON resistance of a CMOS switch does not affect the gain accuracy.
3. The gain accuracy and gain temperature coefficient of the amplifier circuit are primarily dependent on the user selected external resistors.
4. The AD625 provides totally independent input and output offset nulling terminals for high precision applications. This minimizes the effects of offset voltage in gain-ranging applications.
5. The proprietary design of the AD625 provides input voltage noise of 4nV/√Hz at 1kHz.
6. External resistor matching is not required to maintain high common-mode rejection.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = +25°C unless otherwise specified)

Model	AD625A/J/S Min	AD625A/J/S Typ	AD625A/J/S Max	AD625B/K Min	AD625B/K Typ	AD625B/K Max	AD625C Min	AD625C Typ	AD625C Max	Units
GAIN										
Gain Equation		$\frac{2\,R_F}{R_G}+1$			$\frac{2\,R_F}{R_G}+1$			$\frac{2\,R_F}{R_G}+1$		
Gain Range	1		10,000	1		10,000	1		10,000	
Gain Error[1]		±.035	**±0.05**		±0.02	**±0.03**		±0.01	**±0.02**	%
Nonlinearity, Gain = 1-256			±0.005			±0.002			±0.001	%
Gain>256			±0.01			±0.008			±0.005	%
Gain vs. Temp. Gain<1000[1]			5			5			5	ppm/°C
GAIN SENSE INPUT										
Gain Sense Current		300	**500**		150	**250**		50	**100**	nA
vs. Temperature		5	20		2	15		2	10	nA/°C
Gain Sense Offset Current		150	**500**		75	**250**		50	**100**	nA
vs. Temperature		2	15		1	10		1	5	nA/°C
VOLTAGE OFFSET (May be Nulled)										
Input Offset Voltage		50	**200**		25	**50**		10	**25**	µV
vs. Temperature		1	2/2		0.25	**0.50/1**		0.1	**0.25**	µV/°C
Output Offset Voltage		4	**5**		2	**3**		1	**2**	mV
vs. Temperature		20	50/**50**		10	**25/40**		10	**15**	µV/°C
Offset Referred to the Input vs. Supply										
G = 1	**70**	75		**75**	85		**80**	90		dB
G = 10	85	95		90	100		95	105		dB
G = 100	95	100		105	110		110	120		dB
G = 1000	**100**	110		**110**	120		**115**	140		dB
INPUT CURRENT										
Input Bias Current		±30	**±50**		±20	**±25**		±10	**±15**	nA
vs. Temperature		±50			±50			±50		pA/°C
Input Offset Current		±2	**±35**		±1	**±15**		±1	**±5**	nA
vs. Temperature		±20			±20			±20		pA/°C
INPUT										
Input Impedance										
Differential Resistance		1			1			1		GΩ
Differential Capacitance		4			4			4		pF
Common-Mode Resistance		1			1			1		GΩ
Common-Mode Capacitance		4			4			4		pF
Input Voltage Range										
Differ. Input Linear (V_D)			±10			±10			±10	V
Common-Mode Linear (V_{CM})		$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$			$12V-\left(\frac{G}{2}\times V_D\right)$		
Common-Mode Rejection Ratio dc to 60Hz with 1kΩ Source Imbalance										
G = 1	**70**	75		**75**	85		**80**	90		dB
G = 10	90	95		95	105		100	115		dB
G = 100	100	105		105	115		110	125		dB
G = 1000	**110**	115		**115**	125		**120**	140		dB
OUTPUT RATING		±10V @5mA			±10V @5mA			±10V @5mA		
DYNAMIC RESPONSE										
Small Signal – 3dB										
G = 1 (R_F = 20kΩ)		650			650			650		kHz
G = 10		400			400			400		kHz
G = 100		150			150			150		kHz
G = 1000		25			25			25		kHz
Slew Rate		5.0			5.0			5.0		V/µs
Settling Time to 0.01%, 20V Step										
G = 1 to 200		15			15			15		µs
G = 500		35			35			35		µs
G = 1000		75			75			75		µs
NOISE										
Voltage Noise, 1kHz										
R.T.I.		4			4			4		$nV/\sqrt{Hz}$
R.T.O.		75			75			75		$nV/\sqrt{Hz}$
R.T.I., 0.1 to 10Hz										
G = 1		10			10			10		µV p-p
G = 10		1.0			1.0			1.0		µV p-p
G = 100		0.3			0.3			0.3		µV p-p
G = 1000		0.2			0.2			0.2		µV p-p
Current Noise										
0.1Hz to 10Hz		60			60			60		pA p-p

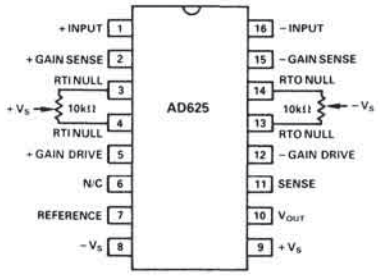
Model	AD625A/J/S Min	Typ	Max	AD625B/K Min	Typ	Max	AD625C Min	Typ	Max	Units
SENSE INPUT										
R_{IN}		10			10			10		kΩ
I_{IN}		30			30			30		μA
Voltage Range	±10			±10			±10			V
Gain to Output		1 ± 0.01			1 ± 0.01			1 ± 0.01		%
REFERENCE INPUT										
R_{IN}		20			20			20		kΩ
I_{IN}		30			30			30		μA
Voltage Range	±10			±10			±10			V
Gain to Output		1 ± 0.01			1 ± 0.01			1 ± 0.01		%
TEMPERATURE RANGE										
Specified Performance										
J/K Grades	0		+70	0		+70				°C
A/B/C Grades	−25		+85	−25		+85	−25		+85	°C
S Grade	−55		+125							
Storage	−65		+150	−65		+150	−65		+150	°C
POWER SUPPLY										
Power Supply Range		±6 to ±18			±6 to ±18			±6 to ±18		V
Quiescent Current		3.5	5		3.5	5		3.5	5	mA
PACKAGE OPTIONS[2]										
Ceramic (D-16)		AD625AD/SD			AD625BD			AD625CD		
Plastic DIP (N-16)		AD625JN			AD625KN					

NOTES
[1]Gain error and gain TC are for the AD625 only. Resistor network errors will add to the specified errors.
[2]See Section 16 for package outline information.

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

PIN CONFIGURATION



Typical Characteristics

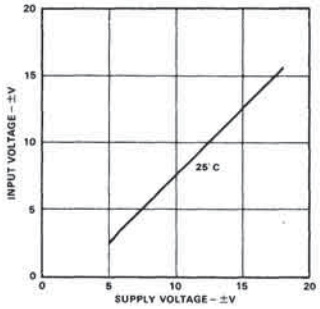


Figure 1. Input Voltage Range vs. Supply Voltage, G = 1

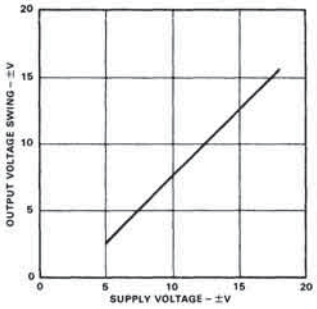


Figure 2. Output Voltage Swing vs. Supply Voltage

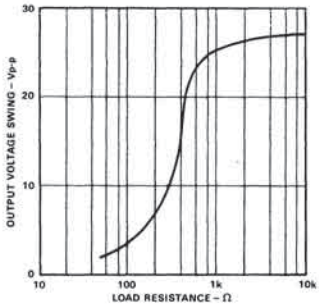


Figure 3. Output Voltage Swing vs. Resistive Load

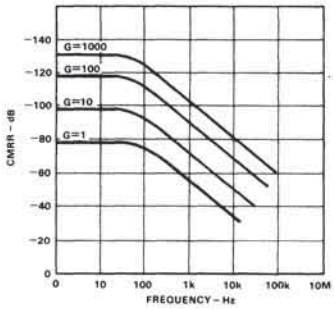


Figure 4. CMRR vs. Frequency RTI, Zero to 1kΩ Source Imbalance

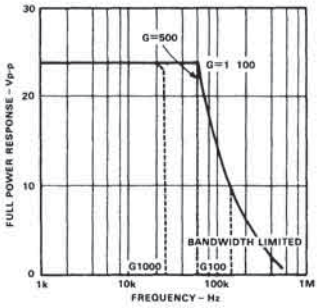


Figure 5. Large Signal Frequency Response

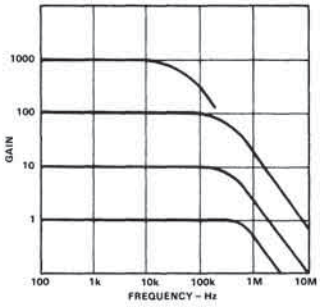


Figure 6. Gain vs. Frequency

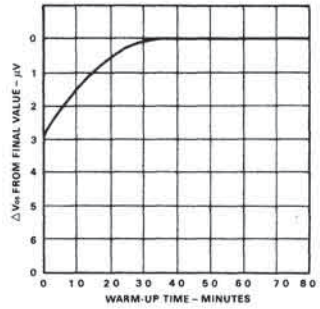


Figure 7. Offset Voltage, RTI, Turn On Drift

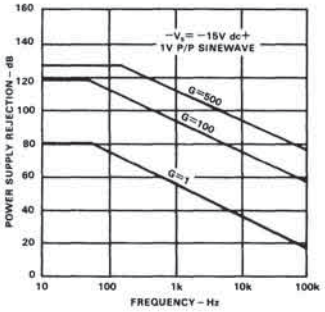


Figure 8. Negative PSRR vs. Frequency

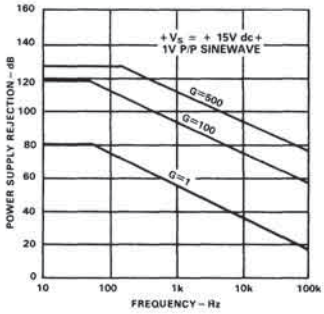


Figure 9. Positive PSRR vs. Frequency

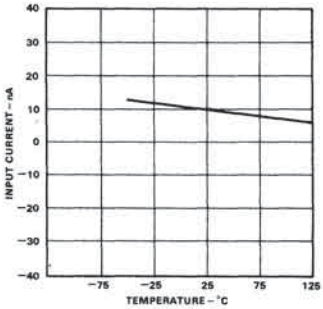


Figure 10. Input Bias Current vs. Temperature

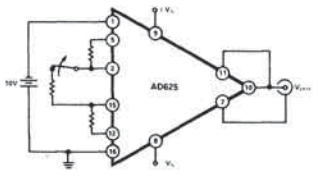


Figure 11. Overange and Gain Switching Test Circuit (G=8, G=1)

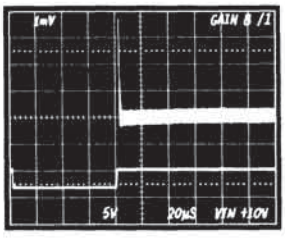


Figure 12. Gain Overange Recovery

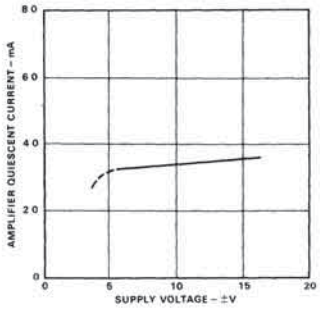


Figure 13. Quiescent Current vs. Supply Voltage

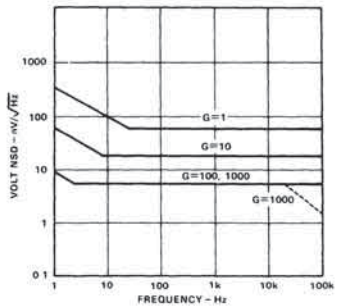


Figure 14. RTI Noise Spectral Density vs. Gain

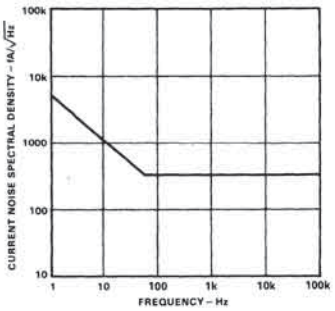


Figure 15. Input Current Noise

4

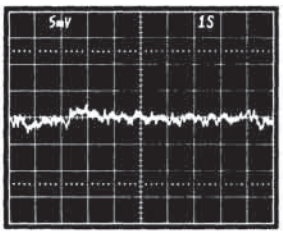


Figure 16. Low Frequency Voltage Noise, G=1 (System Gain=1000)

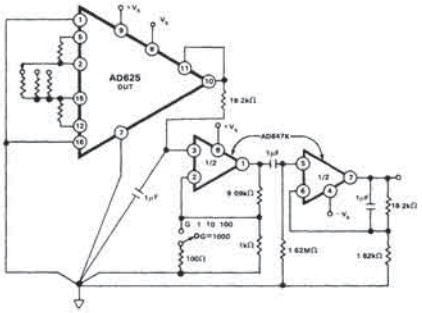


Figure 17. Noise Test Circuit

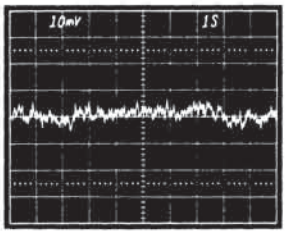


Figure 18. Low Frequency Voltage Noise, G=1000 (System Gain=100,000)

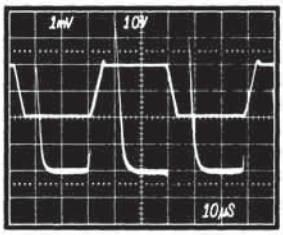


Figure 19. Large Signal Pulse Response and Settling Time, G=1

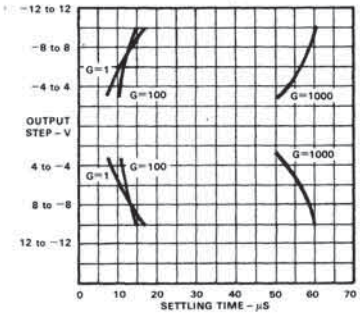


Figure 20. Settling Time to 0.01%

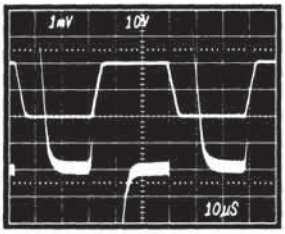


Figure 21. Large Signal Pulse Response and Settling Time, G = 100

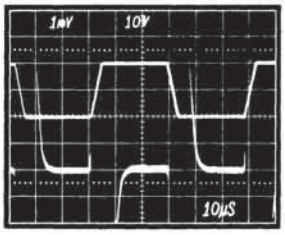


Figure 22. Large Signal Pulse Response and Settling Time, G = 10

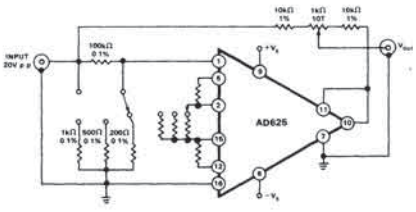


Figure 23. Settling Time Test Circuit

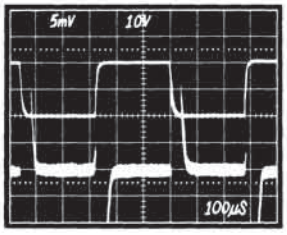


Figure 24. Large Signal Pulse Response and Settling Time, G=1000

Theory of Operation

The AD625 is a monolithic instrumentation amplifier based on a modification of the classic three-op-amp approach. Monolithic construction and laser-wafer-trimming allow the tight matching and tracking of circuit components. This insures the high level of performance inherent in this circuit architecture.

A preamp section (Q1-Q4) provides additional gain to A1 and A2. Feedback from the outputs of A1 and A2 forces the collector currents of Q1-Q4 to be constant, thereby, impressing the input voltage across R_G. This creates a differential voltage at the outputs of A1 and A2 which is given by the gain ($2R_F/R_G + 1$) times the differential portion of the input voltage. The unity gain subtractor, A3, removes any common-mode signal from the output voltage yielding a single ended output, V_{OUT}, referred to the potential at the reference pin.

The value of R_G is the determining factor of the transconductance of the input preamp stage. As R_G is reduced for larger gains the transconductance increases. This has three important advantages. First, this approach allows the circuit to achieve a very high open-loop gain of (3×10^8 at programmed gains $\geq$ 500) thus reducing gain related errors. Second, the gain-bandwidth product, which is determined by C3, C4, and the input transconductance, increases with gain, thereby, optimizing frequency response. Third, the input voltage noise is reduced to a value determined by the collector current of the input transistors ($4nV/\sqrt{Hz}$).

INPUT PROTECTION

Differential input amplifiers frequently encounter input voltages outside of their linear range of operation. There are two considerations when applying input protection for the AD625; 1) that continuous input current must be limited to less than 10mA and 2) that input voltages must not exceed either supply by more than one diode drop (approximately 0.6V @ 25°C).

Under differential overload conditions there is ($R_G + 100$)Ω in series with two diode drops (approximately 1.2V) between the plus and minus inputs, in either direction. With no external protection and R_G very small (i.e., 40Ω), the maximum overload voltage the AD625 can withstand, continuously, is approximately ±2.5V. Figure 26A shows the external components necessary to protect the AD625 under all overload conditions at any gain.

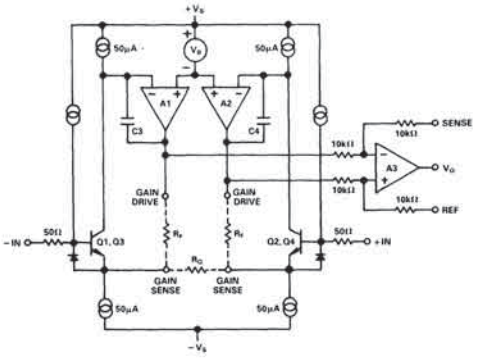


Figure 25. Simplified Circuit of the AD625

The diodes to the supplies are only necessary if input voltages outside of the range of the supplies are encountered. In higher gain applications where differential voltages are small, back-to-back zener diodes and smaller resistors, as shown in Figure 26b, provides adequate protection. Figure 26c shows low cost FETs with a maximum ON resistance of 300Ω configured to offer input protection with minimal degradation to noise, ($5.2nV/\sqrt{Hz}$ compared to normal noise performance of $4nV/\sqrt{Hz}$).

During differential overload conditions, excess current will flow through the gain sense lines (pins 2 and 15). This will have no effect in fixed gain applications. However, if the AD625 is being used in an SPGA application with a CMOS multiplexer, this current should be taken into consideration. The current capabilities of the multiplexer may be the limiting factor in allowable overflow current. The ON resistance of the switch should be included as part of R_G when calculating the necessary input protection resistance.

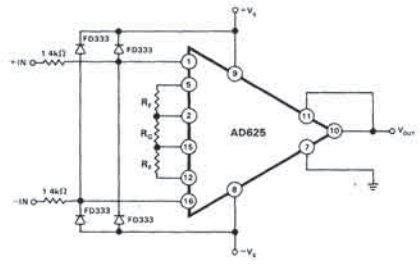


Figure 26a. Input Protection Circuit

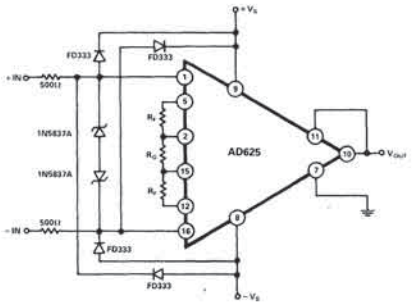


Figure 26b. Input Protection Circuit for G>5

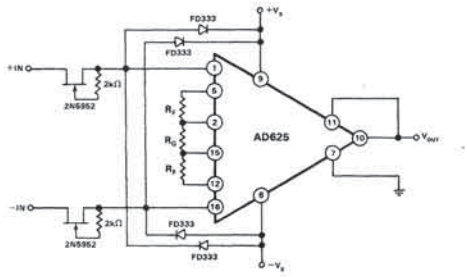


Figure 26c. Input Protection Circuit

Any resistors in series with the inputs of the AD625 will degrade the noise performance. For this reason the circuit in Figure 26b should be used if the gains are all greater than 5. For gains less than 5, either the circuit in Figure 26a or in Figure 26c can be used. The two 1.4kΩ resistors in Figure 26a will degrade the noise performance to:

$$\sqrt{4kTR_{ext} + (4nV/\sqrt{Hz})^2} = 7.9nV/\sqrt{Hz}$$

RESISTOR PROGRAMMABLE GAIN AMPLIFIER

In the resistor-programmed mode (Figure 27), only three external resistors are needed to select any gain from 1 to 10,000. Depending on the application, discrete components or a pretrimmed network can be used. The gain accuracy and gain TC are primarily determined by the external resistors since the AD625C contributes less than 0.02% to gain error and under 5ppm/°C gain TC. The gain sense current is insensitive to common-mode voltage, making the CMRR of the resistor programmed AD625 independent of the match of the two feedback resistors, R_F.

Selecting Resistor Values

As previously stated each R_F provides feedback to the input stage and sets the unity gain transconductance. These feedback resistors are provided by the user. The AD625 is tested and specified with a value of 20kΩ for R_F. Since the magnitude of RTO errors increases with increasing feedback resistance, values much above 20kΩ are not recommended (values below 10kΩ for R_F may lead to instability). Refer to the graph of RTO noise, offset, drift, and bandwidth (Figure 28) when selecting the feedback resistors. The gain resistor (R_G) is determined by the formula $R_G = 2R_F/(G-1)$.

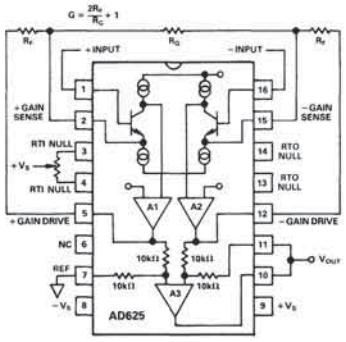


Figure 27. AD625 in Fixed Gain Configuration

A list of standard resistors which can be used to set some common gains is shown in Table I.

For single gain applications, only one offset null adjust is necessary; in these cases the RTI null should be used.

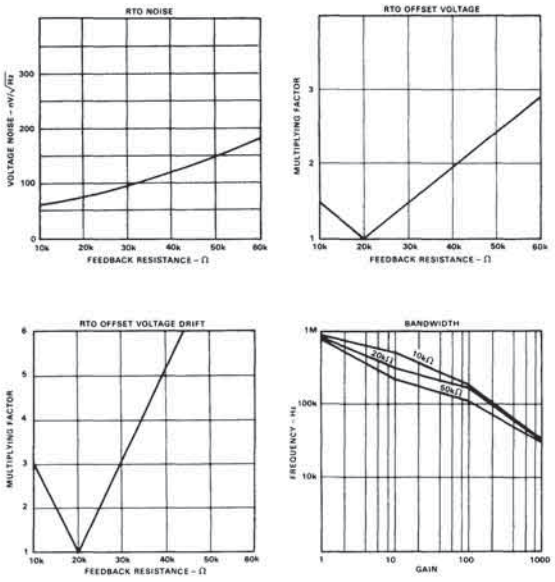


Figure 28. RTO Noise, Offset, Drift, and Bandwidth vs. Feedback Resistance Normalized to 20kΩ

GAIN	R_F	R_G
1	20kΩ	∞
2	19.6kΩ	39.2kΩ
5	20kΩ	10kΩ
10	20kΩ	4.42kΩ
20	20kΩ	2.1kΩ
50	19.6kΩ	806Ω
100	20kΩ	402Ω
200	20.5kΩ	205Ω
500	19.6kΩ	78.7Ω
1000	19.6kΩ	39.2Ω
4	20kΩ	13.3kΩ
8	19.6kΩ	5.62kΩ
16	20kΩ	2.67kΩ
32	19.6kΩ	1.27kΩ
64	20kΩ	634Ω
128	20kΩ	316Ω
256	19.6kΩ	154Ω
512	19.6kΩ	76.8Ω
1024	19.6kΩ	38.3Ω

Table I. Common Gains Nominally within ±0.5% Error Using Standard 1% Resistors

SENSE TERMINAL

The sense terminal is the feedback point for the AD625 output amplifier. Normally it is connected directly to the output. If heavy load currents are to be drawn through long leads, voltage drops through lead resistance can cause errors. In these instances the sense terminal can be wired to the load thus putting the I × R drops "inside the loop" and virtually eliminating this error source.

Typically, IC instrumentation amplifiers are rated for a full ± 10 volt output swing into 2kΩ. In some applications, however, the need exists to drive more current into heavier loads. Figure 29 shows how a high-current booster may be connected "inside the loop" of an instrumentation amplifier. By using an external power boosting circuit, the power dissipated by the AD625 will remain low, thereby, minimizing the errors induced by self-heating. The effects of nonlinearities, offset and gain inaccuracies of the buffer are reduced by the loop gain of the AD625's output amplifier.

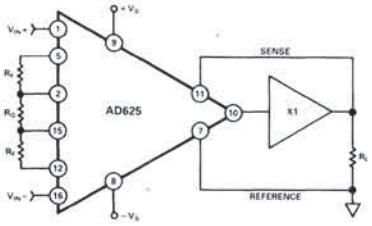


Figure 29. AD625 Instrumentation Amplifier with Output Current Booster

REFERENCE TERMINAL

The reference terminal may be used to offset the output by up to ± 10V. This is useful when the load is "floating" or does not share a ground with the rest of the system. It also provides a direct means of injecting a precise offset. However, it must be remembered that the total output swing is ± 10 volts, from ground, to be shared between signal and reference offset.

The AD625 reference terminal must be presented with nearly zero impedance. Any significant resistance, including those caused by PC layouts or other connection techniques, will increase the gain of the noninverting signal path, thereby, upsetting the common-mode rejection of the In-Amp. Inadvertent thermocouple connections created in the sense and reference lines should also be avoided as they will directly affect the output offset voltage and output offset voltage drift.

In the AD625 a reference source resistance will unbalance the CMR trim by the ratio of $10k\Omega/R_{REF}$. For example, if the reference source impedance is 1Ω, CMR will be reduced to 80dB (10kΩ/1Ω = 80dB). An operational amplifier may be used to provide the low impedance reference point as shown in Figure 30. The input offset voltage characteristics of that amplifier will add directly to the output offset voltage performance of the instrumentation amplifier.

The circuit of Figure 30 also shows a CMOS DAC operating in the bipolar mode and connnected to the reference terminal to provide software controllable offset adjustments. The total offset range is equal to $\pm(V_{REF}/2 \times R_5/R_4)$, however, to be symmetrical about 0V $R_3 = 2 \times R_4$.

The offset per bit is equal to the total offset range divided by 2^N, where N = number of bits of the DAC. The range of offset for Figure 30 is ± 120mV, and the offset is incremented in steps of 0.9375mV/LSB.

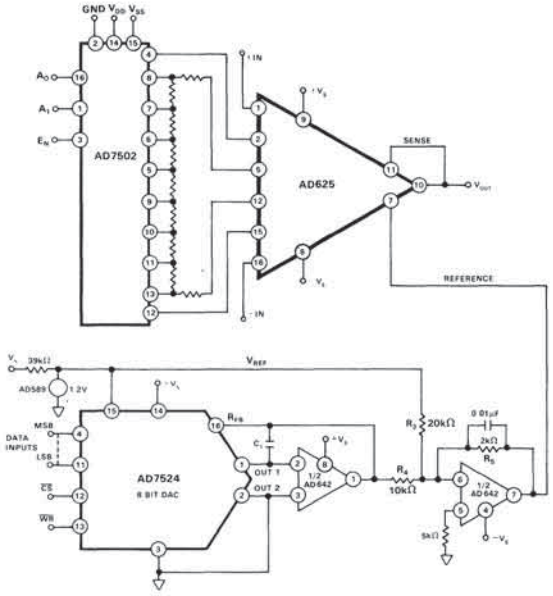


Figure 30. Software Controllable Offset

An instrumentation amplifier can be turned into a voltage-to-current converter by taking advantage of the sense and reference terminals as shown in Figure 31.

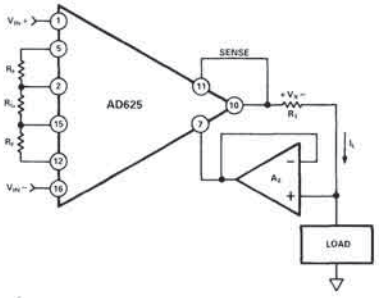


Figure 31. Voltage-to-Current Converter

By establishing a reference at the "low" side of a current setting resistor, an output current may be defined as a function of input voltage, gain and the value of that resistor. Since only a small current is demanded at the input of the buffer amplifier A1, the forced current I_L will largely flow through the load. Offset and drift specifications of A2 must be added to the output offset and drift specifications of the In-Amp.

INPUT AND OUTPUT OFFSET VOLTAGE

Offset voltage specifications are often considered a figure of merit for instrumentation amplifiers. While initial offset may be adjusted to zero, shifts in offset voltage due to temperature variations will cause errors. Intelligent systems can often correct for this factor with an auto-zero cycle, but this requires extra circuitry.

Offset voltage and offset voltage drift each have two components: input and output. Input offset is that component of offset that is generated at the input stage. Measured at the output it is directly proportional to gain, i.e., input offset as measured at the output at G = 100 is 100 times greater than that measured at G = 1. Output offset is generated at the output and is constant for all gains.

The input offset and drift are multiplied by the gain, while the output terms are independent of gain, therefore, input errors dominate at high gains and output errors dominate at low gains. The output offset voltage (and drift) is normally specified at G = 1 (where input effects are insignificant), while input offset (and drift) is given at a high gain (where output effects are negligible). All input-related parameters are specified referred to the input (RTI) which is to say that the effect on the output is "G" times larger. Offset voltage vs. power supply is also specified as an RTI error.

By separating these errors, one can evaluate the total error independent of the gain. For a given gain, both errors can be combined to give a total error referred to the input (RTI) or output (RTO) by the following formula:

Total Error RTI = input error + (output error/gain)

Total Error RTO = (Gain × input error) + output error

The AD625 provides for both input and output offset voltage adjustment. This simplifies nulling in very high perecision applications and minimizes offset voltage effects in switched gain applications. In such applications the input offset is adjusted first at the highest programmed gain, then the output offset is adjusted at G = 1. If only a single null is desired, the input offset null should be used. The most additional drift when using only the input offset null is 0.9μV/°C, RTO.

COMMON-MODE REJECTION

Common-mode rejection is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

In an instrumentation amplifier, degradation of common-mode rejection is caused by a differential phase shift due to differences in distributed stray capacitances. In many applications shielded cables are used to minimize noise. This technique can create common-mode rejection errors unless the shield is properly driven. Figures 32 and 33 show active data guards which are configured to improve ac common-mode rejection by "bootstrapping" the capacitances of the input cabling, thus minimizing differential phase shift.

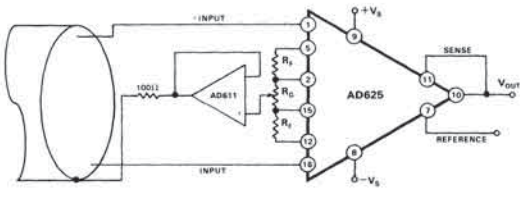


Figure 32. Common-Mode Shield Driver

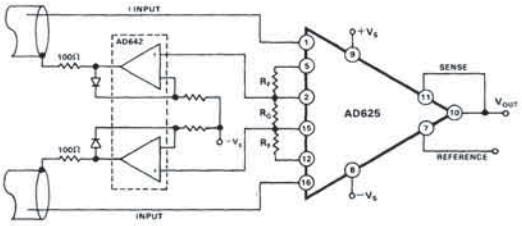


Figure 33. Differential Shield Driver

GROUNDING

In order to isolate low level analog signals from a noisy digital environment, many data-acquisition components have two or more ground pins. These grounds must eventually be tied together at one point. It would be convenient to use a single ground line, however, current through ground wires and pc runs of the circuit card can cause hundreds of millivolts of error. Therefore, separate ground returns should be provided to minimize the current flow from the sensitive points to the system ground (see Figure 34). Since the AD625 output voltage is developed with respect to the potential on the reference terminal, it can solve many grounding problems.

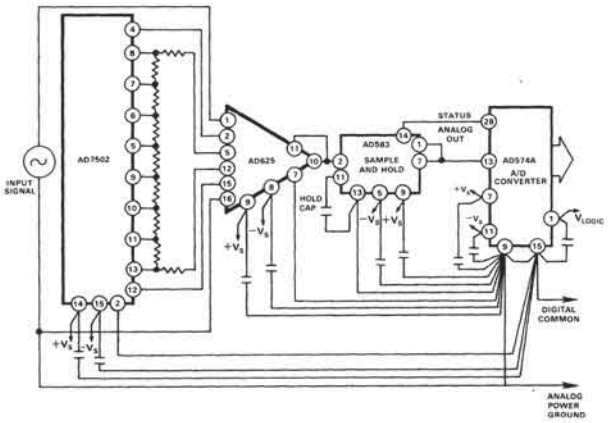


Figure 34. Basic Grounding Practice for a Data Acquisition System

GROUND RETURNS FOR BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of a dc amplifier. There must be a direct return path for these currents, otherwise they will charge external capacitances, causing the output to drift uncontrollably or saturate. Therefore, when amplifying "floating" input sources such as transformers, or ac-coupled sources, there must be a dc path from each input to ground as shown in Figure 35.

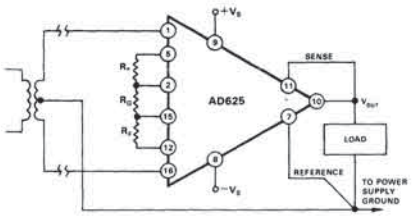


Figure 35a. Ground Returns for Bias Currents with Transformer Coupled Inputs

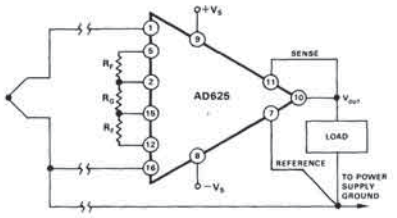


Figure 35b. Ground Returns for Bias Currents with Thermocouple Input

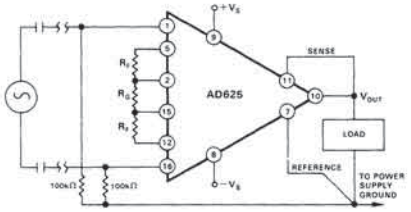


Figure 35c. Ground Returns for Bias Currents with AC Coupled Inputs

AUTO-ZERO CIRCUITS

In many applications it is necessary to maintain high accuracy. At room temperature, offset effects can be nulled by the use of offset trimpots. Over the operating temperature range, however, offset nulling becomes a problem. For these applications the auto-zero circuit of Figure 36 provides a hardware solution.

OTHER CONSIDERATIONS

One of the more overlooked problems in designing ultra-low-drift dc amplifiers is thermocouple induced offset. In a circuit comprised of two dissimilar conductors (i.e., copper, kovar), a current flows when the two junctions are at different temperatures. When this circuit is broken, a voltage known as the "Seebeck" or thermocouple emf can be measured. Standard IC lead material (kovar) and copper form a thermocouple with a high thermoelectric potential (about 35μV°C). This means that care must be taken to insure that all connections (especially those in the input circuit of the AD625) remain isothermal. This includes the input leads (1, 16) and the gain sense lines (2, 15). These pins were chosen for symmetry, helping to desensitize the input circuit to thermal gradients. In addition, the user should also avoid air currents

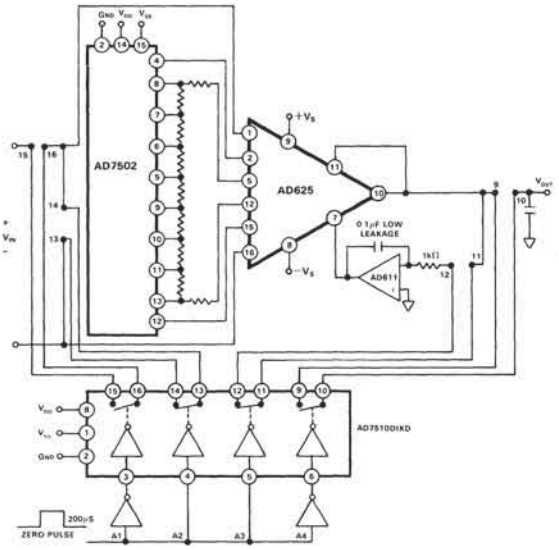


Figure 36. Auto-Zero Circuit

over the circuitry since slowly fluctuating thermocouple voltages will appear as "flicker" noise. In SPGA applications relay contacts and CMOS mux leads are both potential sources of additional thermocouple errors.

The base emitter junction of an input transistor can rectify out of band signals (i.e., RF interference). When amplifying small signals, these rectified voltages act as small dc offset errors. The AD625 allows direct access to the input transistors' bases and emitters enabling the user to apply some first order filtering to these unwanted signals. In Figure 37, the RC time constant should be chosen for desired attenuation of the interfering signals. In the case of a resistive transducer, the capacitance alone working against the internal resistance of the transducer may suffice.

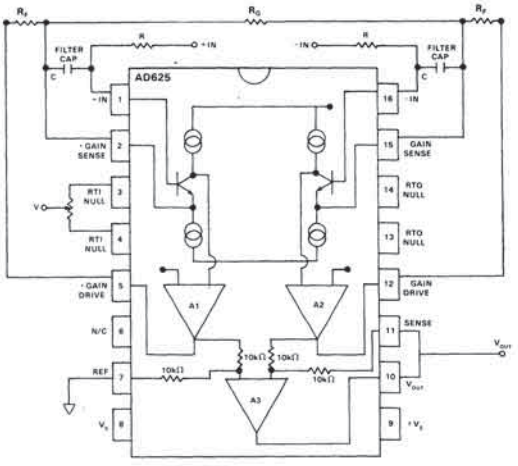


Figure 37. Circuit to Attenuate RF Interference

These capacitances may also be incorporated as part of the external input protection circuit (see section on input protection). As a general practice every effort should be made to match the extraneous capacitance at pins 15 and 2, and pins 1 and 16, to preserve high ac CMR.

SOFTWARE PROGRAMMABLE GAIN AMPLIFIER

An SPGA provides the ability to externally program precision gains from digital inputs. Historically, the problem in systems requiring electronic switching of gains has been the ON resistance (R_{ON}) of the multiplexer, which appears in series with the gain setting resistor R_G. This can result in substantial gain errors and gain drifts. The AD625 eliminates this problem by making the gain drive and gain sense pins available (pins 2, 15, 5, 12; see Figure 39). Consequently the multiplexer's ON resistance is removed from the signal current path. This transforms the ON resistance error into a small nullable offset error. To clarify this point, an error budget analysis has been performed in Table II based on the SPGA configuration shown in Figure 39.

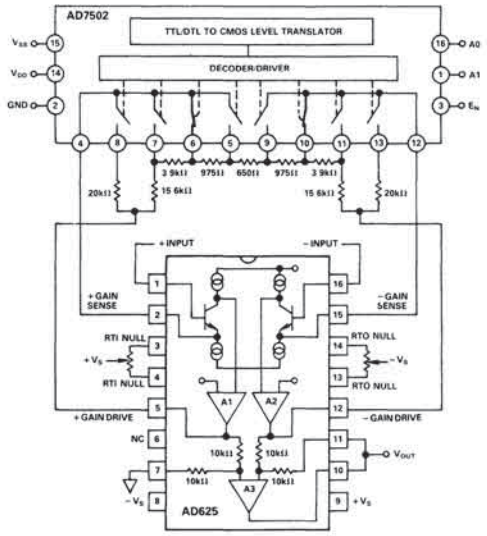


Figure 38. SPGA in a Gain of 16

Figure 38 shows an AD625 based SPGA with possible gains of 1, 4, 16, 64. R_G equals the resistance between the gain sense lines (pins 2 and 15) of the AD625. In Figure 38, R_G equals the sum of the two 975Ω resistors and the 650Ω resistor, or 2600Ω. R_F equals the resistance between the gain sense and the gain drive pins (pins 12 and 15, or pins 2 and 5), that is R_F equals the 15.6kΩ resistor plus the 3.9kΩ resistor, or 19.5kΩ. The gain, therefore equals:

$$\frac{2R_F}{R_G} + 1 = \frac{2(19.5k\Omega)}{(2.6k\Omega)} + 1 = 16$$

As the switches of the differential multiplexer proceed synchronously, R_G and R_F change, resulting in the various programmed gain settings.

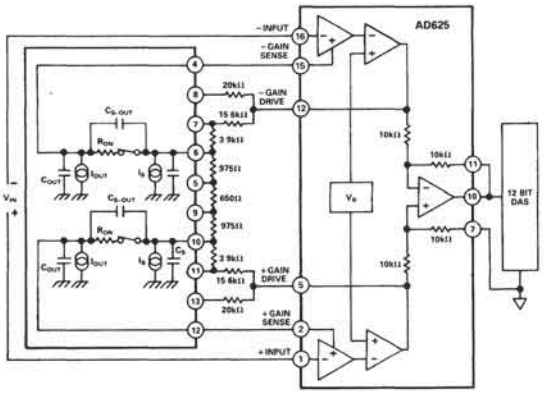


Figure 39. SPGA with Multiplexer Error Sources

Figure 39 shows a complete SPGA feeding a 12-bit DAS with a 0–10V input range. This configuration was used in the error budget analysis shown in Table II. The gain used for the RTI calculations is set at 16. As the gain is changed, the ON resistance of the multiplexer and the feedback resistance will change, which will slightly alter the values in the table.

Induced Error	Specification AD625C	Specification AD7502KN	Calculation	Voltage Offset Induced RTI
RTI Offset Voltage	Gain Sense Offset Current 40nA	Switch Resistance 170Ω	40nA × 170Ω = 6.8μV	6.8μV
RTI Offset Voltage	Gain Sense Current 60nA	Differential Switch Resistance 6.8Ω	60nA × 6.8Ω = 0.41μV	0.41μV
RTO Offset Voltage	Feedback Resistance 20kΩ[1]	Differential Leakage Current $(I_S)^2$ +0.2nA −0.2nA	2(0.2nA × 20kΩ) = 8μV/16	0.5μV
RTO Offset Voltage	Feedback Resistance 20kΩ[1]	Differential Leakage Current $(I_{OUT})^2$ +1nA −1nA	2(1nA × 20kΩ) = 40μV/16	2.5μV
Total error induced by a typical CMOS multiplexer to an SPGA at 25°C				**10.21μV**

NOTES
[1]The resistor for this calculation is the user provided feedback resistance (R_F). 20kΩ is recommended value (see resistor programmable gain amplifier section).
[2]The leakage currents (I_S and I_{OUT}) will induce an offset voltage, however, the offset will be determined by the difference between the leakages of each "half" of the differential multiplexer. The differential leakage current is multiplied by the feedback resistance (see Note 1),to determine offset voltage Because differential leakage curent is not a parameter specified on multiplexer data sheets, the most extreme difference (one most positive and one most negative) was used for the calculations in Table II. Typical performance will be much better.
*The frequency response and settling will be affected by the ON resistance and internal capacitance of the multiplexer Figure 40 shows the settling time vs. ON resistance at different gain settings for an AD625 based SPGA.
**Switch resistance and leakage current errors can be reduced by using relays.

Table II. Errors Induced by Multiplexer to an SPGA

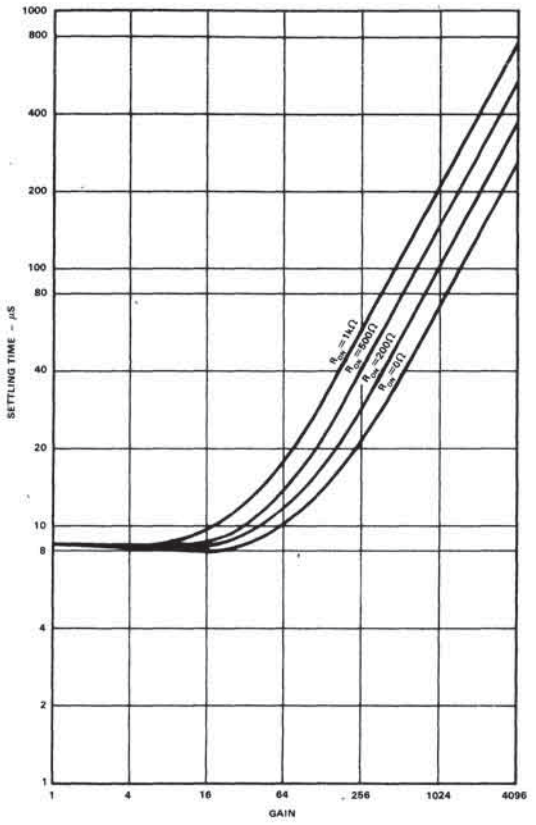


Figure 40. Settling Time to 0.01% of a 20V Step Input for SPGA with AD625

DETERMINING SPGA RESISTOR NETWORK VALUES

The individual resistors in the gain network can be calculated sequentially using the formula given below. The equation determines the resistors as labeled in Figure 41. The feedback resistors and the gain setting resistors are interactive, therefore; the formula must be a series where the present term is dependent on the preceding term(s). The formula

$$R_{F_{i+1}} = (20k\Omega - \sum_{j=0}^{i} R_{F_j})(1 - \frac{G_i}{G_{i+1}}) \qquad \begin{matrix} G_0 = 1 \\ R_{F_0} = 0 \end{matrix}$$

can be used to calculate the necessary feedback resistors for any set of gains. This formula yields a network with a total resistance of 40kΩ. A dummy variable (j) serves as a counter to keep a running total of the preceding feedback resistors. To illustrate how the formula can be applied, an example similar to the calculation used for the resistor network in Figure 38 is examined below.

1) Unity gain is treated as a separate case. It is implemented with separate 20kΩ feedback resistors as shown in Figure 41. It is then ignored in further calculations.

2) Before making any calculations it is advised to draw a resistor network similar to the network in Figure 41. The network will have (2 × M) + 1 resistors, where M = number of gains. For Figure 38 M = 3 (4, 16, 64), therefore, the resistor string will have 7 resistors (plus the two 20kΩ "side" resistors for unity gain).

3) Begin all calculations with $G_0 = 1$ and $R_{F_0} = 0$.

$R_{F_1} = (20k\Omega - R_{F_0})(1 - 1/4)$: $R_{F_0} = 0 \therefore R_{F_1} = 15k\Omega$

$R_{F_2} = [20k\Omega - (R_{F_0} + R_{F_1})](1 - 4/16)$:

$R_{F_0} + R_{F_1} = 15k\Omega \therefore R_{F_2} = 3.75k\Omega$

$R_{F_3} = [20k\Omega - (R_{F_0} + R_{F_1} + R_{F_2})](1 - 16/64)$:

$R_{F_0} + R_{F_1} + R_{F_2} = 18.75k\Omega \therefore R_{F_3} = 937.5\Omega$

4) The center resistor (R_G of the highest gain setting), is determined last. Its value is the remaining resistance of the 40kΩ string, and can be calculated with the equation:

$$R_G = (40k\Omega - 2\sum_{j=0}^{M} R_{F_j})$$

$$R_G = 40k\Omega - 2(R_{F_0} + R_{F_1} + R_{F_2} + R_{F_3})$$

$$40k\Omega - 39.375k\Omega = 625\Omega$$

5) If different resistor values are desired, all the resistors in the network can be scaled by some convenient factor. However, raising the impedance will increase the RTO errors, lowering the total network resistance below 20kΩ can result in amplifier instability. More information on this phenomenon is given in the RPGA section of the data sheet. The scale factor will not affect the unity gain feedback resistors. The resistor network in Figure 38 has a scaling factor of 650/625 = 1.04, if this factor is used on R_{F_1}, R_{F_2}, R_{F_3}, and R_G, then the resistor values will match exactly.

6) Round off errors can be cumulative, therefore, it is advised to carry as many significant digits as possible until all the values have been calculated.

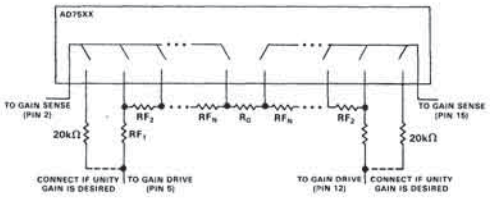


Figure 41. Resistors for a Gain Setting Network

Isolation Amplifiers
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AD210 – Precision, Wide Bandwidth, 3-Port Isolation Amplifier . . . . . 5 – 19
AD295 – Precision Hybrid Isolation Amplifier . . . . . 5 – 27
284J – Economy, High Performance, Self-Contained Isolation Amplifier . . . . . 5 – 33
286J/281 – High CMV, High Performance, Synchronized Isolation Amplifiers . . . . . 5 – 39
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290A/292A – Low Cost, Single and Multichannel Isolation Amplifiers . . . . . 5 – 51

5

Selection Guide
Isolation Amplifiers

Model	CMV In/Out V pk	Gain Range V/V	Frequency Response kHz	Page	Notes
281 (External oscillator for 286 or 292A isolation amplifiers)				5 – 39	
284	2500	1–10	1	5 – 33	
286	2500	1–100	1	5 – 39	External oscillator (281)
289	2500	1–100	20	5 – 45	3-port isolation
290	1500	1–100	2.5	5 – 51	
292A	1500	1–100	2.5	5 – 51	External oscillator (281)
AD202	2000	1–100	1.5	5 – 7	
AD204	2000	1–100	5	5 – 7	External oscillator, uses AD246 clock
AD210	3500	1–100	20	5 – 19	3-port isolation
AD295	2500	1–1000	4.5	5 – 27	3-port isolation

5

Orientation
Isolation Amplifiers

The *isolation amplifier* (or isolator) has an input circuit that is galvanically isolated from the power supply and the output circuit. In the basic *two-port* form, the output and power circuits are not isolated from one another; in *three-port* isolators (see the figure), the input circuits, output circuits, and power source are all isolated from one another. In some 3-port isolators, the power for the output stage must be furnished from the signal's destination; however, in the device shown in Figure 1, all internal power is furnished by its own power source; in addition, a modicum of auxiliary power is available to power external input *and output* circuitry.

Isolators are intended for applications requiring safe, accurate measurement of dc and low-frequency voltage or current in the presence of high common-mode voltage (to thousands of volts) with high CMR, line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measurements where dc and line-frequency leakage must be maintained at levels well below certain mandated minima.* Principal applications are in electrical environments of the kind associated with medical equipment conventional and nuclear power plants, automatic test equipment and industrial process-control systems.

Analog Devices Isolators described in this section (and in the *Signal Conditioner* section) use electromagnetically coupled high-frequency carrier techniques for communication of power to and signals from the input (and in some cases the *output*) circuit.

CHOOSING AN ISOLATOR

The choice of isolator depends on the desired *functional characteristics* and the required *specifications*. Functional characteristics include such considerations as number of channels in the system, range of output common-mode (output to power supply), nature of the front-end amplifier (amplification only or general op-amp functioning) and the availability of isolated power for additional external front-end (or back-end) circuitry. Key specifications include performance specs and "absolute max/min" mandated safety specifications. Definitions of specifications follow this section. In addition to the products listed here, which are recommended for new designs, a number of older products are still available; data sheets are available upon request. In addition to the useful applications information on the data sheets published here, an applications guide[1], available upon request, provides information useful to the circuit designer.

The devices described in this section are all voltage-output isolation amplifiers, useful in general-purpose circuit applications for instrumentation amplifiers or op amps where isolation is a necessity. In addition to these devices, there are a growing number of isolators available from Analog Devices that perform dedicated functions, for use where isolation is necessary or desirable. Some of their applications can be seen in the Signal Conditioner section of this book and the *Transducer Interfacing Handbook*[2]. Power Supplies and DC-DC Converters, usually transformer-coupled, also provide isolation.

***Examples of such requirements may be found in UL STD 544 and SWC (Surge Withstand Capability) in IEEE Standard for Transient Voltage Protection 472-1974.**

[1]*Analog Devices Applications Guide to Isolation Amplifiers and Signal Conditioners*

[2]Sheingold, D.H., ed, *Transducer Interfacing Handbook – A guide to analog signal conditioning*. Norwood, MA 02062 (P.O. Box 796): Analog Devices, Inc., 1980, $14.50

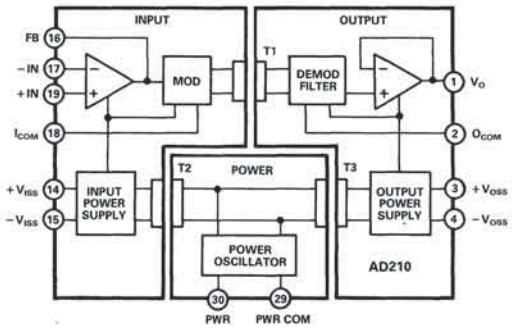


Figure 1. AD210 Block Diagram

Functional Characteristics: The figure shows the circuit architecture of a self-contained isolator, Model AD210. The various models differ, but their properties can be discussed in terms of the device shown. An isolator of this type requires power from a two-terminal dc supply. An internal oscillator converts the dc power to ac, which is transformer-coupled to the shielded input section, then converted to dc for the input stage and the auxiliary power output. The ac carrier is also modulated by the amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered and buffered, using isolated dc power (also available for auxiliary circuitry) derived from the carrier.

The amplifier in this example is an uncommitted op amp, specified for programmable gains from 1 to 100V/V, as determined by its feedback circuitry. Since both input terminals are floating, the amplifier functions effectively as an instrumentation amplifier. Most of the other devices in this series require just a single external resistor to set the gain.

In the figure it can be seen that ac power is magnetically coupled from the oscillator to the output stage. This permits the output to operate at a dc common-mode potential with respect to power common. An isolator of this type is said to provide *three-port* isolation, because there are three isolated ports: input, power supply and output. Two-port devices are those in which there is a dc connection between the oscillator power supply and the output stage.

The AD210, as can be seen, is a completely self-contained device. There are applications for which a degree of "unbundling" can lead to economy and improved performance. For example, if there are many input channels to be isolated, economies can be realized by the use of a common oscillator. In addition, the common oscillator makes it possible to avoid the possibility of small errors due to beat frequencies developed by small amounts of crosstalk in older amplifier designs.

Several synchronized multichannel devices are available. Model 204 is essentially a 202A with a power converter instead of an oscillator. It requires a pair of leads for an oscillator input, which can be furnished by an AD246 clock.

SPECIFICATIONS

The illustration on the next page shows a typical specification block; the specifications of key interest are defined.

For an initial choice of data sheets to inspect for a given application, the Selection Guide permits comparison on the basis of these key characteristics: common-mode voltage, specified gain range and frequency response. The "Notes" column indicates which devices require external oscillators (for lower cost in many-channel applications) and identifies devices that are three-port isolated. Good starting points are: for high performance, the AD210; for lowest cost, the AD202 and AD204, depending on whether the application calls for few or many channels.

NONLINEARITY – This is the peak deviation from a best straight line, expressed as a % of peak-to-peak output. Should be considered when signal fidelity is of prime importance.

MAX SAFE DIFFERENTIAL INPUT – Max voltage that can be safely applied across input terminals. Important to consider for fail-safe designs in the presence of high voltages.

INPUT NOISE – Total noise, referred to the input. Facilitates comparison with expected signal input levels.

ISOLATED POWER OUTPUTS – Dual supply voltages, completely isolated from the input power supply terminals, provide the capability to excite floating input and output signal conditioners, front-end amplifiers, as well as remote transducers.

SPECIFICATIONS (typical @ + 25°C, & V_S = + 15V unless otherwise specified)

MODEL	AD210AN	AD210BN
GAIN		
Range	1V/V – 100V/V	*
Error	± 2% max	± 1% max
vs Temperature (0 to + 70°C)	± 25ppm/°C max	*
(– 25°C to + 85°C)	± 50ppm/°C max	*
vs Supply Voltage	± 0 002%/V	*
Nonlinearity[1]	± 0 025% max	± 0 012% max
INPUT VOLTAGE RATINGS		
Linear Differential Range	± 10V	*
Maximum Safe Differential Input	± 15V	*
Max CMV Input-to-Output		
ac, 60Hz, Continuous	2500V rms	*
dc, Continuous	± 3500V peak	*
Common-Mode Rejection		
60Hz, G = 100V/V		
$R_S \leq 500\Omega$ Impedance Imbalance	120dB	*
Leakage Current Input-to-Output		
@ 240Vrms, 60Hz	2μA rms max	*
INPUT IMPEDANCE		
Differential	$10^{12}\Omega$	*
Common Mode	$5G\Omega \| 5pF$	*
INPUT BIAS CURRENT		
Initial, @ + 25°C	30pA typ (400pA max)	*
vs Temperature (0 to + 70°C)	10nA max	*
(– 25°C to + 85°C)	30nA max	*
INPUT DIFFERENCE CURRENT		
Initial, @ + 25°C	5pA typ (200pA max)	*
vs Temperature (0 to + 70°C)	2nA max	*
(– 25°C to + 85°C)	10nA max	*
INPUT NOISE		
Voltage (1kHz)	$18nV/\sqrt{Hz}$	*
(10Hz to 10kHz)	4μV rms	*
Current (1kHz)	$0\ 01pA/\sqrt{Hz}$	*
FREQUENCY RESPONSE		
Bandwidth (– 3dB)		
G = 1V/V	20kHz	*
G = 100V/V	15kHz	*
Settling Time (± 10mV, 20V Step)		
G = 1V/V	150μs	*
G = 100V/V	500μs	*
Slew Rate (G = 1V/V)	1V/μs	*
OFFSET VOLTAGE (RTI)[2]		
Initial, @ + 25°C	(± 15 ± 45/G)mV max	(± 5 ± 15/G)mV max
vs Temperature (0 to + 70°C)	(± 10 ± 30/G)μV/°C	*
(– 25°C to + 85°C)	(± 10 ± 50/G)μV/°C	*
RATED OUTPUT[3]		
Voltage, 2kΩ Load	± 10V min	*
Impedance	1Ω max	*
Ripple, (Bandwidth = 100kHz)	10mV p-p max	*
ISOLATED POWER OUTPUTS		
Voltage, No Load	± 15V	*
Accuracy	± 10%	*
Current	± 5mA	*
Regulation, No Load to Full Load	See Text	*
Ripple	See Text	*
POWER SUPPLY		
Voltage, Rated Performance	+ 15V dc ± 5%	*
Voltage, Operating	+ 15V dc ± 10%	*
Current, Quiescent	50mA	*
Current, Full Load – Full Signal	80mA	*
TEMPERATURE RANGE		
Rated Performance	– 25°C to + 85°C	*
Operating	– 40°C to + 85°C	*
Storage	– 40°C to + 85°C	*
PACKAGE DIMENSIONS		
Inches	1 00 × 2 10 × 0 350	*
Millimeters	25 4 × 53 3 × 8 9	*

NOTES
*Specifications same as AD210AN
[1]Gain nonlinearity increases by ± 0 002%/mA when the isolated power outputs are used
[2]RTI – Referred to Input
[3]A reduced signal swing is recommended when both $\pm V_{ISS}$ and $\pm V_{OSS}$ supplies are fully loaded, due to supply voltage reduction
Specifications subject to change without notice

Figure 2. Typical Isolator Specifications

CMV, INPUTS TO OUTPUTS – Voltage that may be safely applied to *both* inputs with respect to outputs or power common. Necessary consideration in applications with high CMV input or when high voltage transients may occur at the input.

CMR, INPUTS TO OUTPUTS – Indicates ability to reject common-mode voltages between inputs and outputs. Important when processing small signals riding on high common-mode voltages.

LEAKAGE CURRENT – Maximum input leakage current when power-line voltage is impressed on inputs. Vital consideration for patient safety in medical applications.

OFFSET VOLTAGE REFERRED TO INPUT – Total input drift is composed of two sources (input and output stage drifts) and is gain (G) dependent. Referring offsets to the input allows them to be compared to signal levels.

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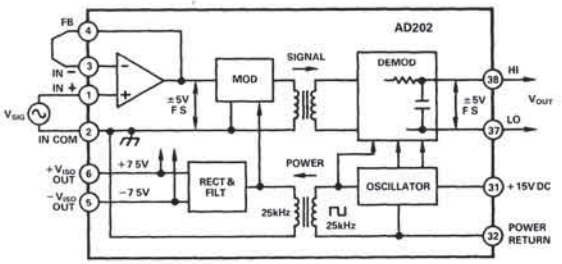
Low Cost, Miniature Isolation Amplifiers

AD202/AD204

FEATURES
Small Size: 4 Channels/Inch
Low Power: 35mW (AD204)
High Accuracy: ±0.025% max Nonlinearity (K Grade)
High CMR: 130dB (Gain = 100 V/V)
Wide Bandwidth: 5kHz Full-Power (AD204)
High CMV Isolation: ±2000 V pk Continuous (K Grade) (Signal and Power)
Isolated Power Outputs
Uncommitted Input Amplifier

APPLICATIONS
Multichannel Data Acquisition
Current Shunt Measurements
Motor Controls
Process Signal Isolation
High Voltage Instrumentation Amplifier

AD202 FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

The AD202 and AD204 are members of a new generation of low cost, high performance isolation amplifiers. A new circuit design, novel transformer construction, and the use of surface-mounted components in an automated assembly process result in remarkably compact, economical isolators whose performance in many ways exceeds that previously available from very expensive devices. The primary distinction between the AD202 and AD204 is that the AD202 is powered directly from +15V dc while the AD204 is powered by an externally supplied clock (AD246).

The AD202 and AD204 employ transformer coupling and do not require the design compromises that must be made when optical isolators are used: each provides a complete isolation function, with both signal and power isolation internal to the module, and they exhibit no long-term parameter shifts under sustained common-mode stress. Power consumption, nonlinearity, and drift are each an order of magnitude lower than can be obtained from other isolation techniques, and these advantages are obtained without sacrifice of bandwidth or noise performance.

The design of the AD202 and AD204 emphasizes ease of use in a broad range of applications where signals must be measured or transmitted without a galvanic connection. In addition, the low cost and small size of these isolators makes component-level circuit applications of isolation practical for the first time.

PRODUCT HIGHLIGHTS

The AD202 and AD204 are full-featured isolators offering numerous benefits to the user:

Small Size: The AD202 and AD204 are available in SIP and DIP form packages. The SIP package is just 0.25" wide, giving the user a channel density of four channels per inch. The isolation barrier is positioned to maximize input to output spacing. For applications requiring a low profile, the DIP package provides a height of just 0.350".

High Accuracy: With a maximum nonlinearity of ±0.025% for the AD202K/AD204K (±0.05% for the AD202J/AD204J) and low drift over temperature, the AD202 and AD204 provide high isolation without loss of signal integrity.

Low Power: Power consumption of 35mW (AD204) and 75mW (AD202) over the full signal range makes these isolators ideal for use in applications with large channel counts or tight power budgets.

Wide Bandwidth: The AD204's full-power bandwidth of 5kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Excellent Common-Mode Performance: The AD202K/AD204K provide ±2000V pk continuous common-mode isolation, while the AD202J/AD204J provide ±1000V pk continuous common-mode isolation. All models have a total common-mode input capacitance of less than 5pF inclusive of power isolation. This results in CMR ranging from 130dB at a gain of 100 to 104dB (minimum at unity gain) and very low leakage current (2μA maximum).

Flexible Input: An uncommitted op amp is provided at the input of all models. This provides buffering and gain as required, and facilitates many alternative input functions including filtering, summing, high-voltage ranges, and current (transimpedance) input.

Isolated Power: The AD204 can supply isolated power of ±7.5V at 2mA. This is sufficient to operate a low-drift input preamp, provide excitation to a semiconductor strain gage, or to power any of a wide range of user-supplied ancillary circuits. The AD202 can supply ±7.5V at 0.4mA which is sufficient to operate adjustment networks or low-power references and op amps, or to provide an open-input alarm.

SPECIFICATIONS (typical @ +25°C and V_S = +15V unless otherwise noted)

Model	AD204J	AD204K	AD202J	AD202K
GAIN				
Range	1V/V-100V/V	*	*	*
Error	±0.5% typ (±4% max)	*	*	*
vs. Temperature	±20ppm/°C typ (±45ppm/°C max)	*	*	*
vs. Time	±50ppm/1000 Hours	*	*	*
vs. Supply Voltage	±0.001%/V	±0.001%/V	±0.01%/V	±0.01%/V
Nonlinearity (G = 1V/V)[1]	±0.05% max	±0.025% max	±0.05% max	±0.025% max
INPUT VOLTAGE RATINGS				
Linear Differential Range	±5V	*	*	*
Max CMV Input to Output				
ac, 60Hz, Continuous	750V rms	1500V rms	750V rms	1500V rms
Continuous (dc and ac)	±1000V peak	±2000V peak	±1000V peak	±2000V peak
Common-Mode Rejection (CMR), @ 60Hz				
R_S = ≤100Ω (HI & LO Inputs) G = 1	110dB	110dB	105dB	105dB
G = 100	130dB	*	*	*
R_S = ≤1kΩ (Input HI, LO, or Both) G = 1	104dB min	104dB min	100dB min	100dB min
G = 100	110dB min	*	*	*
Leakage Current Input to Output				
@240V rms, 60Hz	2μA rms max	*	*	*
INPUT IMPEDANCE				
Differential (G = 1V/V)	10^{12} Ω	*	*	*
Common Mode	2GΩ‖4.5pF	*	*	*
INPUT BIAS CURRENT				
Initial, @ +25°C	±30pA	*	*	*
vs. Temperature (0 to +70°C)	±10nA	*	*	*
INPUT DIFFERENCE CURRENT				
Initial, @ +25°C	±5pA	*	*	*
vs. Temperature (0 to +70°C)	±2nA	*	*	*
INPUT NOISE				
Voltage, 0.1 to 100Hz	4μV p-p	*	*	*
f>200Hz	50nV/$\sqrt{Hz}$	*	*	*
FREQUENCY RESPONSE				
Bandwidth (V_O ≤10V p-p, G = 1-50V/V)	5kHz	5kHz	2kHz	2kHz
Settling Time, to ±10mV (10V Step)	1ms	*	*	*
OFFSET VOLTAGE (RTI)				
Initial, @ +25°C Adjustable to Zero	(±15 ±15/G)mV max	(±5 ±5/G)mV max	(±15 ±15/G)mV max	(±5 ±5/G)mV max
vs. Temperature (0 to +70°C)	$\left(\pm 10 \pm \frac{10}{G}\right)$μV/°C	*	*	*
RATED OUTPUT				
Voltage (Out HI to Out LO)	±5V	*	*	*
Voltage at Out HI or Out LO (Ref. Pin 32)	±6.5V	*	*	*
Output Resistance	3kΩ	3kΩ	7kΩ	7kΩ
Output Ripple, 100kHz Bandwidth	10mV pk-pk	*	*	*
5kHz Bandwidth	0.5mV rms	*	*	*
ISOLATED POWER OUTPUT[2]				
Voltage, No Load	±7.5V	*	*	*
Accuracy	±10%	*	*	*
Current	2mA (Either Output)[3]	2mA (Either Output)[3]	400μA Total	400μA Total
Regulation, No Load to Full Load	5%	*	*	*
Ripple	100mV pk-pk	*	*	*
OSCILLATOR DRIVE INPUT				
Input Voltage	15V pk-pk nominal	15V pk-pk nominal	N/A	N/A
Input Frequency	25kHz nominal	25kHz nominal	N/A	N/A
POWER SUPPLY (AD202 Only)				
Voltage, Rated Performance	N/A	N/A	+15V ±5%	+15V ±5%
Voltage, Operating	N/A	N/A	+15V ±10%	+15V ±10%
Current, No Load (V_S = +15V)	N/A	N/A	5mA	5mA
TEMPERATURE RANGE				
Rated Performance	0 to +70°C	*	*	*
Operating	−40°C to +85°C	*	*	*
Storage	−40°C to +85°C	*	*	*
PACKAGE DIMENSIONS[4]				
SIP Package (Y)	2.08" × 0.250" × 0.625"	*	*	*
DIP Package (N)	2.10" × 0.700" × 0.350"	*	*	*

NOTES
*Specifications same as AD204J.
[1]Nonlinearity is specified as a % deviation from a best straight line.
[2]1.0μF min decoupling required (see text)
[3]3mA with one supply loaded
[4]Width is 0.25" typ, 0.26" max
Specifications subject to change without notice

PIN DESIGNATIONS

AD202/AD204 SIP PACKAGE

PIN	FUNCTION
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	−INPUT
4	INPUT FEEDBACK
5	−V_{ISO} OUTPUT
6	+V_{ISO} OUTPUT
31	+15V POWER IN (AD202 ONLY)
32	CLOCK/POWER COMMON
33	CLOCK INPUT (AD204 ONLY)
37	OUTPUT LO
38	OUTPUT HI

AD202/AD204 DIP PACKAGE

PIN	FUNCTION
1	+INPUT
2	INPUT/V_{ISO} COMMON
3	−INPUT
18	OUTPUT LO
19	OUTPUT HI
20	+15V POWER IN (AD202 ONLY)
21	CLOCK INPUT (AD204 ONLY)
22	CLOCK/POWER COMMON
36	+V_{ISO} OUTPUT
37	−V_{ISO} OUTPUT
38	INPUT FEEDBACK

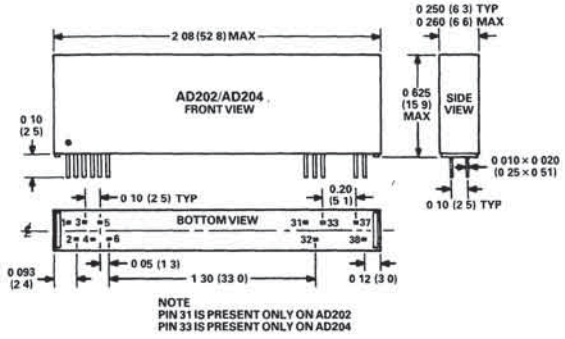
AD202/AD204 ORDERING GUIDE

Model	Package Option	Max Common-Mode Voltage (Peak)	Max Linearity
AD202JY	SIP	1000V	±0.05%
AD202KY	SIP	2000V	±0.025%
AD202JN	DIP	1000V	±0.05%
AD202KN	DIP	2000V	±0.025%
AD204JY	SIP	1000V	±0.05%
AD204KY	SIP	2000V	±0.025%
AD204JN	DIP	1000V	±0.05%
AD204KN	DIP	2000V	±0.025%

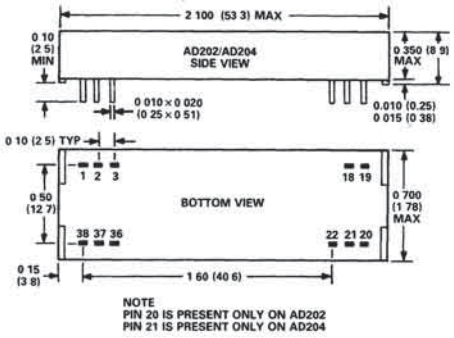
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

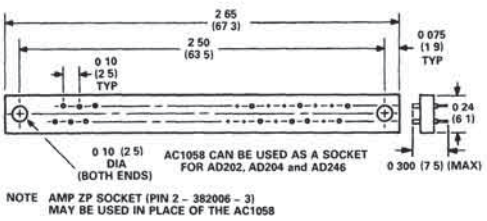
AD202/AD204 SIP PACKAGE



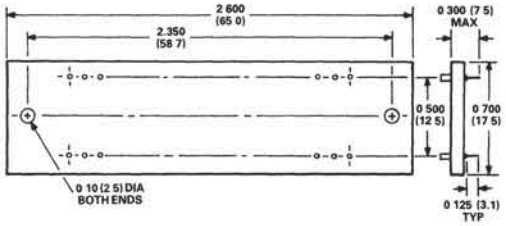
AD202/AD204 DIP PACKAGE



AC1058 MATING SOCKET



AC1060 MATING SOCKET



SPECIFICATIONS

(typical @ +25°C and V_S = +15V unless otherwise noted)

Model	AD246JY	AD246JN
OUTPUT[1]		
Frequency	25kHz nominal	*
Voltage	15V p-p nominal	*
Fan-Out	32 max	*
POWER SUPPLY REQUIREMENTS		
Input Voltage	+15V ±5%	*
Supply Current		
Unloaded	3.5mA	*
Each AD204 Adds	2.2mA	*
Each 1mA Load on AD204 +V_{ISO} or −V_{ISO} Adds	0.7mA	*

NOTES

*Specifications the same as the AD246JY.

[1]The high current drive output will not support a short to ground.

Specifications subject to change without notice.

AD246 PIN DESIGNATIONS

PIN (Y)	PIN (N)	FUNCTION
1	12	+15V POWER IN
2	1	CLOCK OUTPUT
12	14	COMMON
13	24	COMMON



CAUTION

ESD (Electro-Static-Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

DIFFERENCES BETWEEN THE AD202 AND AD204

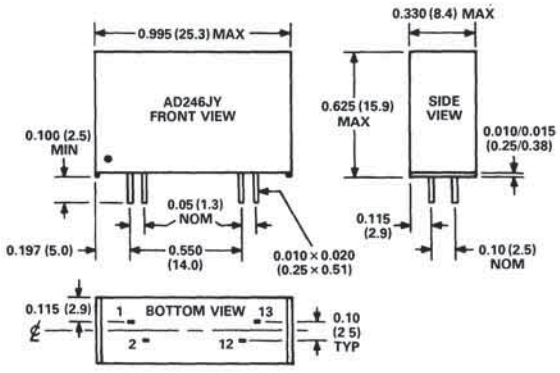
The primary distinction between the AD202 and AD204 is in the method by which they are powered: the AD202 operates directly from +15V dc while the AD204 is powered by a non-isolated externally-supplied clock (AD246) which can drive up to 32 AD204s. The main advantages of using the externally-clocked AD204 over the AD202 are reduced cost in multichannel applications, lower power consumption, and higher bandwidth. In addition, the AD204 can supply substantially more isolated power than the AD202.

Of course, in a great many situations, especially where only one or a few isolators are used, the convenience of stand-alone operation provided by the AD202 will be more significant than any of the AD204's advantages. There may also be cases where it is desirable to accommodate either device interchangeably, so the pinouts of the two products have been designed to make that easy to do.

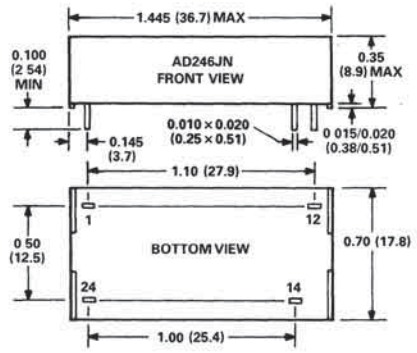
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

AD246JY PACKAGE



AD246JN PACKAGE



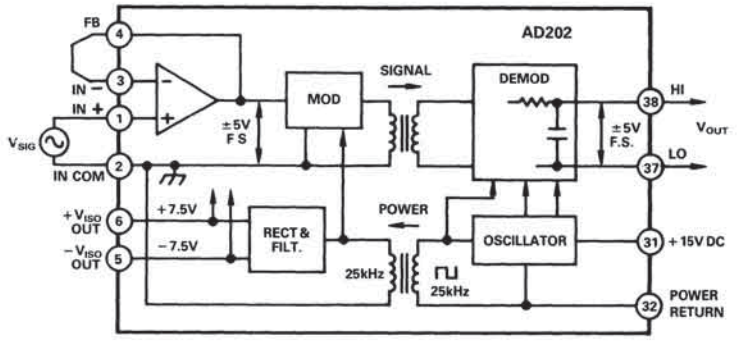


Figure 1a. AD202 Functional Block Diagram

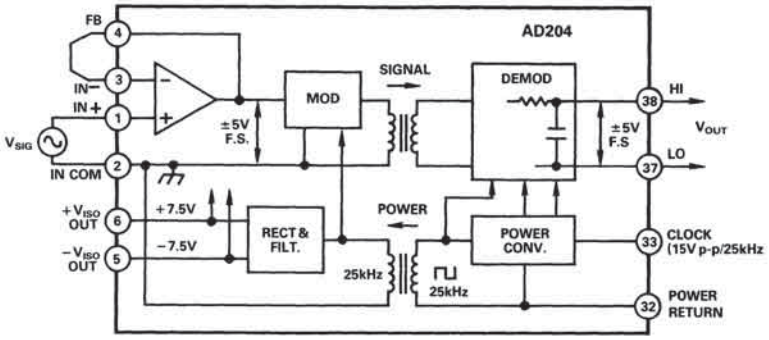


Figure 1b. AD204 Functional Block Diagram

5

INSIDE THE AD202 AND AD204

The AD202 and AD204 use an amplitude modulation technique to permit transformer coupling of signals down to dc (Figure 1a and 1b). Both models also contain an uncommitted input op amp and a power transformer which provides isolated power to the op amp, the modulator, and any external load. The power transformer primary is driven by a 25kHz, 15V p-p square wave which is generated internally in the case of the AD202, or supplied externally for the AD204.

Within the signal swing limits of approximately ±5V, the output voltage of the isolator is equal to the output voltage of the op amp; that is, the isolation barrier has unity gain. The output signal is not internally buffered, so the user is free to interchange the output leads to get signal inversion. Additionally, in multi-channel applications, the unbuffered outputs can be multiplexed with one buffer following the mux. This technique minimizes offset errors while reducing power consumption and cost. The output resistance of the isolator is typically 3kΩ for the AD204 (7kΩ for AD202) and varies with signal level and temperature, so it should not be loaded (see Figure 2 for the effects of load upon nonlinearity and gain drift). In many cases a high-impedance load will be present or a following circuit such as an output filter can serve as a buffer, so that a separate buffer function will not often be needed.

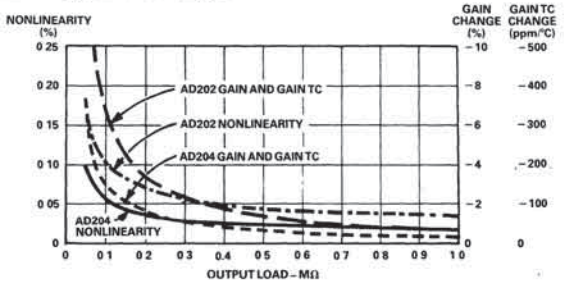


Figure 2. Effects of Output Loading

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

USING THE AD202 AND AD204

Powering the AD202. The AD202 requires only a single +15V power supply connected as shown in Figure 3a. A bypass capacitor is provided in the module.

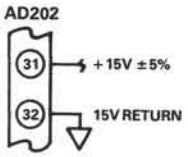


Figure 3a.

Powering the AD204. The AD204 gets its power from an externally supplied clock signal (a 15V p-p square wave with a nominal frequency of 25kHz) as shown in Figure 3b.

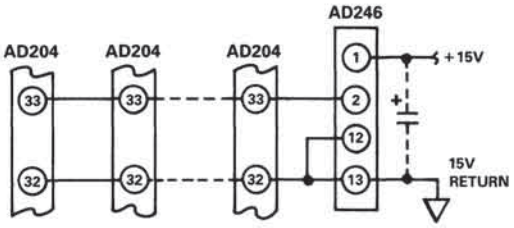


Figure 3b.

AD246 Clock Driver. The AD246 is a compact, inexpensive clock driver that can be used to obtain the required clock from a single 15V supply. Alternatively, the circuit shown in Figure 4 (essentially an AD246) can be used. In either case, one clock circuit can operate at least 32 AD204s at the rated minimum supply voltage of 14.25V and one additional isolator can be operated for each 40mV increase in supply voltage up to 15V. A supply bypass capacitor is included in the AD246, but if many AD204s are operated from a single AD246, an external bypass capacitor should be used with a value of at least 1μF for every five isolators used. Place the capacitor as close as possible to the clock driver.

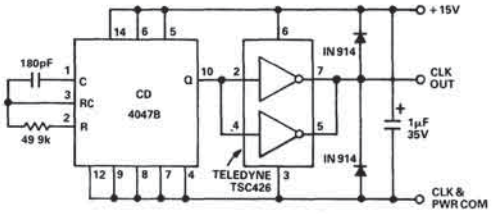


Figure 4. Clock Driver

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

Input Configurations. The AD202 and AD204 have been designed to be very easy to use in a wide range of applications. The basic connection for standard unity gain applications, useful for signals up to ±5V, is shown in Figure 5; some of the possible variations are described below. When smaller signals must be

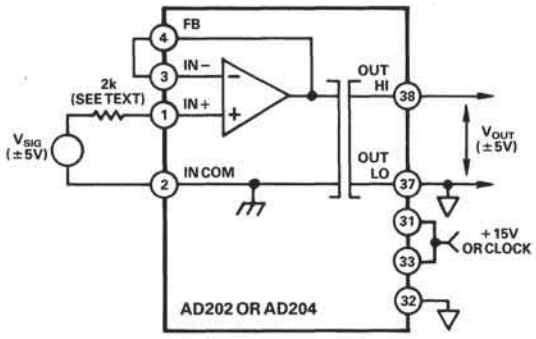


Figure 5. Basic Unity-Gain Application

handled, Figure 6 shows how to get gain while preserving a very high input resistance. The value of feedback resistor R_F should be kept above 20kΩ for best results. Whenever a gain of more than five is taken, a 100pF capacitor from FB to IN COM is required. At lower gains this capacitor is unnecessary, but it will not adversely affect performance if used.

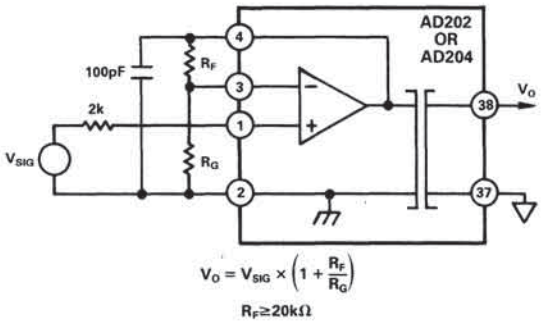


Figure 6. Input Connections for Gain > 1

The "noninverting" circuit of Figures 5 and 6 can also be used to advantage when a signal inversion is needed: just interchange either the input leads or the output leads to get inversion. This approach retains the high input resistance of the "noninverting" circuit, and at unity gain no gain-setting resistors are needed.

When the isolator is not powered, a negative input voltage of more than about 2V will cause an input current to flow. If the signal source can supply more than a few mA under such conditions, the 2kΩ resistor shown in series with IN+ should be used to limit current to a safe value. This is particularly important with the AD202, which may not start if a large input current is present.

Figure 7 shows how to accommodate current inputs or sum currents or voltages. This circuit can also be used when the input signal is larger than the ±5V input range of the isolator; for example, a ±50V input span can be accommodated with R_F = 20k and R_S = 200k. Once again, a capacitor from FB to IN COM is required for gains above 5.

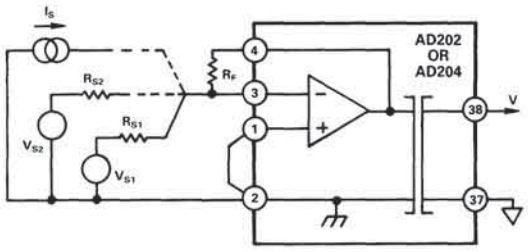


Figure 7. Connections for Summing or Current Inputs

Adjustments. When gain and zero adjustments are needed, the circuit details will depend on whether adjustments are to be made at the isolator input or output, and (for input adjustments) on the input circuit used. Adjustments are usually best done on the input side, because it is better to null the zero ahead of the gain, and because gain adjustment is most easily done as part of the gain-setting network. Input adjustments are also to be preferred when the pots will be near the input end of the isolator (to minimize common-mode strays). Adjustments on the output side might be used if pots on the input side would represent a hazard due to the presence of large common-mode voltages during adjustment.

Figure 8a shows the input-side adjustment connections for use with the "noninverting" connection of the input amplifier. The zero adjustment circuit injects a small adjustment voltage in series with the low side of the signal source. (This will not work if the source has another current path to input common or if current flows in the signal source LO lead). Since the adjustment voltage is injected ahead of the gain, the values shown will work for any gain. Keep the resistance in series with input LO below a few hundred ohms to avoid CMR degradation.

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

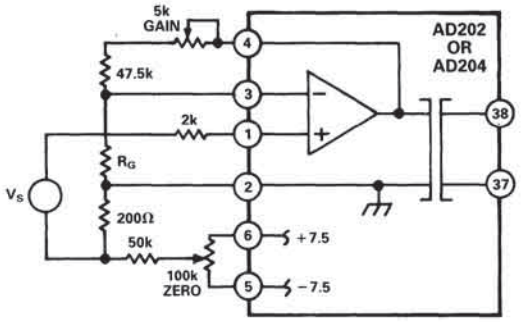


Figure 8a. Adjustments for Noninverting Connection of Op Amp

Also shown in Figure 8a is the preferred means of adjusting the gain-setting network. The circuit shown gives a nominal R_F of 50kΩ, and will work properly for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G = 2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G = 1 (follower) the gain cannot be adjusted downward without compromising input resistance; it is better to adjust gain at the signal source or after the output.

Figure 8b shows adjustments for use with inverting input circuits. The zero adjustment nulls the voltage at the summing node. This method is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is again done in the feedback; but in this case it will work all the way down to unity gain (and below) without alteration.

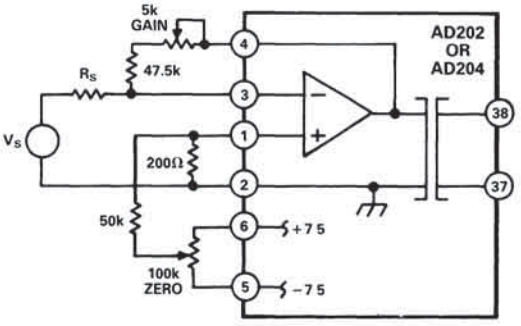


Figure 8b. Adjustments for Summing or Current Input

Figure 9 shows how zero adjustment is done at the output by taking advantage of the semi-floating output port. The range of this adjustment will have to be increased at higher gains; if that is done, be sure to use a suitably stable supply voltage for the pot circuit.

There is no easy way to adjust gain at the output side of the isolator itself. If gain adjustment must be done on the output side, it will have to be in a following circuit such as an output buffer or filter.

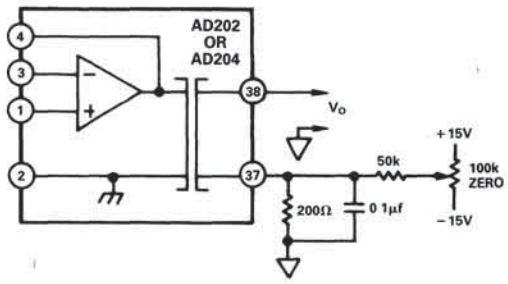


Figure 9. Output-Side Zero Adjustment

Common-Mode Performance. Figures 10a and 10b show how the common-mode rejection of the AD202 and AD204 varies with frequency, gain, and source resistance. For these isolators, the significant resistance will normally be that the path from the source of the common-mode signal to IN COM. The AD202 and AD204 also perform well in applications requiring rejection of fast common-mode steps, as described in the Applications section.

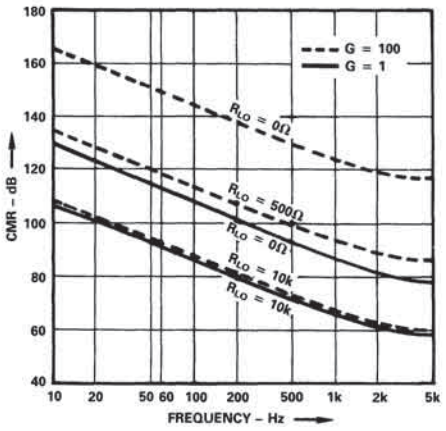


Figure 10a. AD204

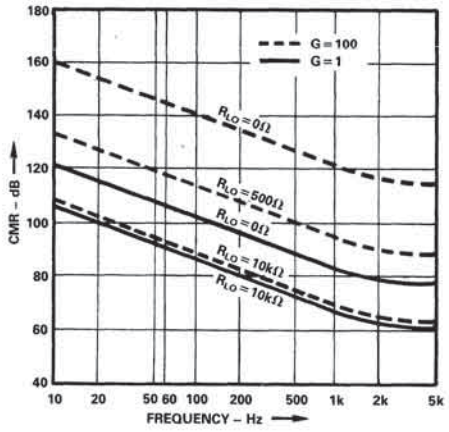


Figure 10b. AD202

Dynamics and Noise. Frequency response plots for the AD202 and AD204 are given in Figure 11. Since neither isolator is slew-rate limited, the plots apply for both large and small signals. Capacitive loads of up to 470pF will not materially affect frequency response. When large signals beyond a few hundred Hz will be present, it is advisable to bypass $-V_{ISO}$ and $+V_{ISO}$ to IN COM with 1μF tantalum capacitors even if the isolated supplies are not loaded.

At 50/60Hz, phase shift through the AD202/AD204 is typically 0.8°C (lagging). Typical unit – unit variation is ±0.2°C (lagging).

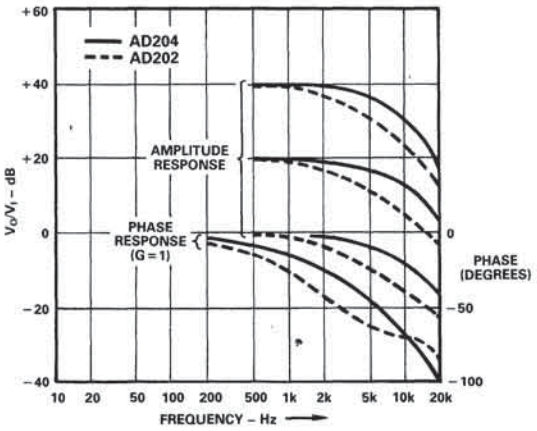


Figure 11. Frequency Response at Several Gains

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

The step response of the AD204 for very fast input signals can be improved by the use of an input filter, as shown in Figure 12. The filter limits the bandwidth of the input (to about 5.3kHz) so that the isolator does not see fast, out-of-band input terms that can cause small amounts (±0.3%) of internal ringing. The AD204 will then settle to ±0.1% in about 300 microseconds for a 10V step.

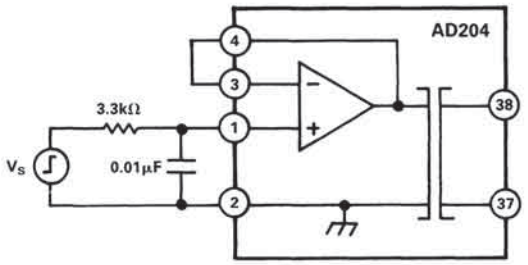


Figure 12. Input Filter for Improved Step Response

Except at the highest useful gains, the noise seen at the output of the AD202 and AD204 will be almost entirely comprised of carrier ripple at multiples of 25kHz. The ripple is typically 2mV p-p near zero output and increases to about 7mV p-p for outputs of ±5V (1MHz measurement bandwidth). Adding a capacitor across the output will reduce ripple at the expense of bandwidth: for example, 0.05μF at the output of the AD204 will result in 1.5mV ripple at ±5V, but signal bandwidth will be down to 1kHz.

When the full isolator bandwidth is needed, the simple two-pole active filter shown in Figure 13 can be used. It will reduce ripple to 0.1mV p-p with no loss of signal bandwith, and also serves as an output buffer.

An output buffer or filter may sometimes show output spikes that do not appear at its input. This is usually due to clock noise appearing at the op amp's supply pins (since most op amps have little or no supply rejection at high frequencies). Another common source of carrier-related noise is the sharing of a ground track by both the output circuit and the power input. Figure 13 shows how to avoid these problems: the clock/supply port of the isolator does not share ground or 15V tracks with any signal circuits, and the op amp's supply pins are bypassed to signal common (note that the grounded filter capacitor goes here as well). Ideally, the output signal LO lead and the supply common meet where the isolator output is actually measured, e.g. at an A/D converter input. If that point is more than a few feet from the isolator, it may be useful to bypass output LO to supply common at the isolator with a 0.1μF capacitor.

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

In applications where more than a few AD204s are driven by a single clock driver, substantial current spikes will flow in the power return line and in whichever signal out lead returns to a low impedance point (usually output LO). Both of these tracks should be made large to minimize inductance and resistance; ideally, output LO should be directly connected to a ground plane which serves as measurement common.

Current spikes can be greatly reduced by connecting a small inductance (68μH–100μH) in series with the clock pin of each AD204. Molded chokes such as the Dale IM-2 series, with dc resistance of about 5Ω, are suitable.

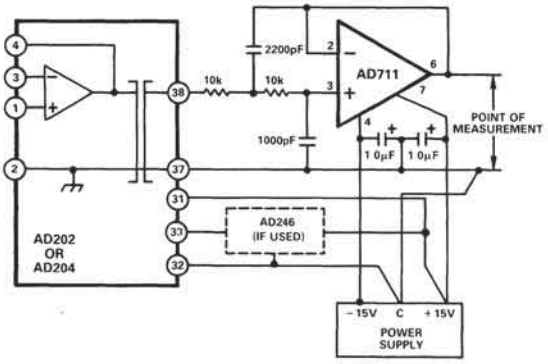


Figure 13. Output Filter Circuit Showing Proper Grounding

Using Isolated Power. Both the AD202 and the AD204 provide ±7.5V power outputs referenced to input common. These may be used to power various accessory circuits which must operate at the input common-mode level; the input zero adjustment pots described above are an example, and several other possible uses are shown in the section titled Application Examples.

The isolated power output of the AD202 (400μA total from either or both outputs) is much more limited in current capacity than that of the AD204, but it is sufficient for operating micropower op amps, low power references (such as the AD589), adjustment circuits, and the like.

The AD204 gets its power from an external clock driver, and can handle loads on its isolated supply outputs of 2mA for each supply terminal (+7.5V and −7.5V) or 3mA for a single loaded output. Whenever the external load on either supply is more than about 200μA, a 1μF tantalum capacitor should be used to bypass each loaded supply pin to input common.

Up to 32 AD204s can be driven from a single AD246 (or equivalent) clock driver when the isolated power outputs of the AD204s are loaded with less than 200μA each, at a worst-case supply voltage of 14.25V at the clock driver. The number of AD204s that can be driven by one clock driver is reduced by one AD204 per 3.5mA of isolated power load current at 7.5V, distributed in any way over the AD204's being supplied by that clock driver. Thus a load of 1.75mA from $+V_{ISO}$ to $-V_{ISO}$ would also count as one isolator because it spans 15V.

It is possible to increase clock fanout by increasing supply voltage above the 14.25V minimum required for 32 loads. One additional isolator (or 3.5mA unit load) can be driven for each 40mV of increase in supply voltage up to 15V. Therefore if the minimum supply voltage can be held to 15V – 1%, it is possible to operate 32 AD204's and 52mA of 7.5V loads. Figure 14 shows the allowable combinations of load current and channel count for various supply voltages.

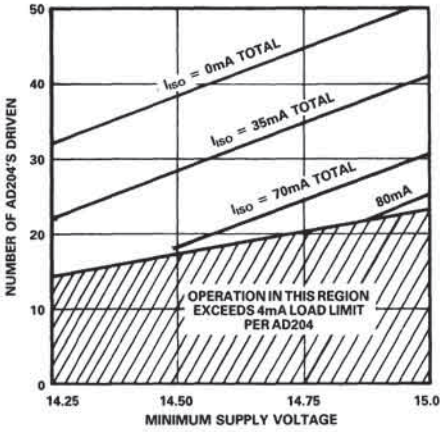


Figure 14. AD246 Fanout Rules

Operation at Reduced Signal Swing. Although the nominal output signal swing for the AD202 and AD204 is ±5V, there may be cases where a smaller signal range may be desirable. When that is done, the fixed errors (principally offset terms and output noise) become a larger fraction of the signal, but nonlinearity is reduced. This is shown in Figure 15.

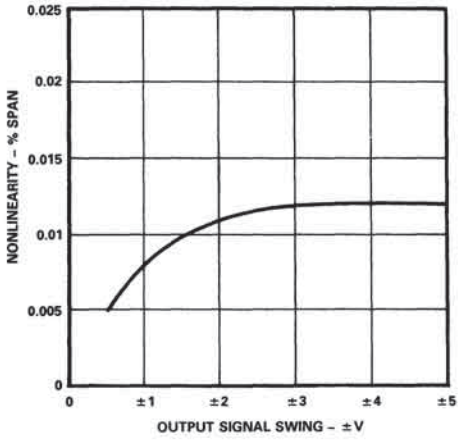


Figure 15. Nonlinearity vs. Signal Swing

PCB Layout for Multichannel Applications. The pinout of the AD204Y has been designed to make very dense packing possible in multichannel applications. Figure 16a shows the recommended printed circuit board (PCB) layout for the simple voltage-follower connection. When gain-setting resistors are present, 0.25″ channel centers can still be achieved, as shown in Figure 16b.

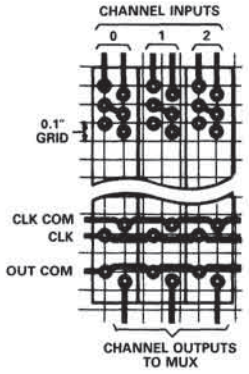


Figure 16a.

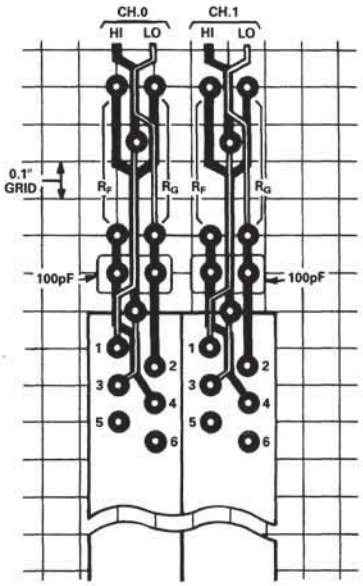


Figure 16b.

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

Synchronization. Since AD204's operate from a common clock, synchronization is inherent. AD202s will normally not interact to produce beat frequencies even when mounted on 0.25-inch centers. Interaction may occur in rare situations where a large number of long, unshielded input cables are bundled together and channel gains are high. In such cases, shielded cable may be required or AD204's can be used.

APPLICATIONS EXAMPLES

Low-Level Sensor Inputs. In applications where the output of low-level sensors such as thermocouples must be isolated, a low-drift input amplifier can be used with an AD204, as shown in Figure 17. A three-pole active filter is included in the design to get normal-mode rejection of frequencies above a few Hz and to provide enhanced common-mode rejection at 60Hz. If offset adjustment is needed, it is best done at the trim pins of the OP-07 itself; gain adjustment can be done at the feedback resistor.

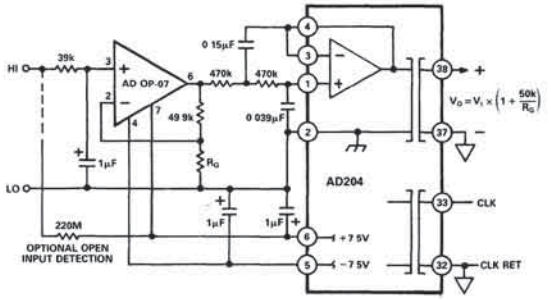


Figure 17. Input Amplifier & Filter for Sensor Signals

Note that the isolated supply current is large enough to mandate the use of 1µF supply bypass capacitors. This circuit can be used with an AD202 if a low-power op amp is used instead of the OP-07.

Process Current Input with Offset. Figure 18 shows an isolator receiver which translates a 4-20mA process current signal into a 0 to +10V output. A 1V to 5V signal appears at the isolator's output, and a −1V reference applied to output LO provides the necessary level shift (in multichannel applications, the reference can be shared by all channels). This technique is often useful for getting offset with a follower-type output buffer.

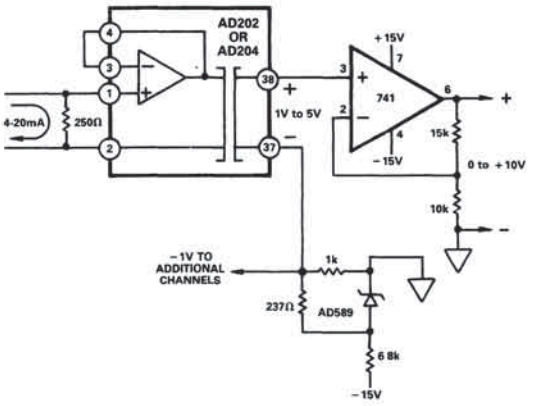


Figure 18. Process Current Input Isolator with Offset

The circuit as shown requires a source compliance of at least 5V, but if necessary that can be reduced by using a lower value of current-sampling resistor and configuring the input amplifier for a small gain.

High-Compliance Current Source. In Figure 19, an isolator is used to sense the voltage across current-sensing resistor R to allow direct feedback control of a high-voltage transistor or FET used as a high-compliance current source. Since the isolator has virtually no response to dc common-mode voltage, the closed-loop current source has a static output resistance greater than $10^{14}\Omega$ even for output currents of several mA. The output current capability of the circuit is limited only by power dissipation in the source transistor.

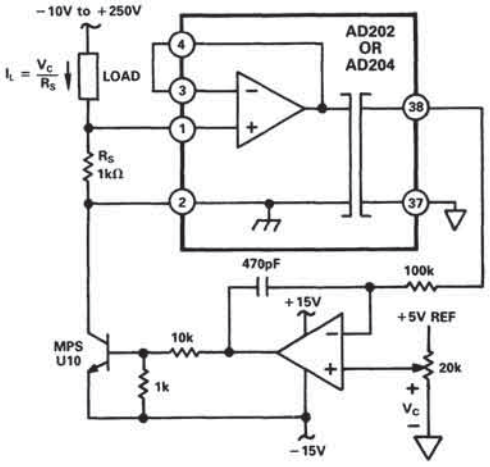


Figure 19. High-Compliance Current Source

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

Motor Control Isolator. The AD202 and AD204 perform very well in applications where rejection of fast common-mode steps is important but bandwidth must not be compromised. Current sensing in a full-wave bridge motor driver (Figure 20) is one example of this class of application. For 200V common-mode steps (1μs rise time) and a gain of 50 as shown, the typical response at the isolator output will be spikes of ±5mV amplitude, decaying to zero in less than 100μs. Spike height can be reduced by a factor of four with output filtering just beyond the isolator's bandwidth.

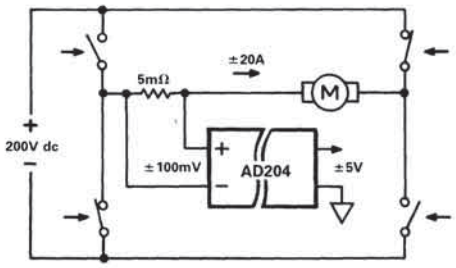


Figure 20. Motor Control Current Sensing

Floating Current Source/Ohmmeter. When a small floating current is needed with a compliance range of up to ±1000V dc, the AD204 can be used to both create and regulate the current. This can save considerable power, since the controlled current does not have to return to ground. In Figure 21, an AD589 reference is used to force a small fixed voltage across R. That sets the current which the input op amp will have to return through the load to zero its input. Note that the isolator's output isn't needed at all in this application; the whole job is done by the input section. However, the signal at the output could be useful: it's the voltage across the load, referenced to ground. Since the load current is known, the output voltage is proportional to load resistance.

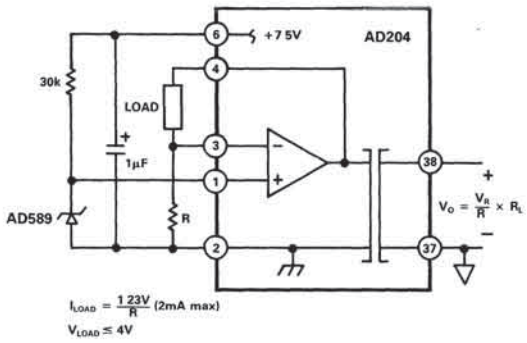


Figure 21. Floating Current Source

Photodiode Amplifier. Figure 22 shows a transresistance connection used to isolate and amplify the output of a photodiode. The photodiode operates at zero bias, and its output current is scaled by R_F to give a +5V full-scale output.

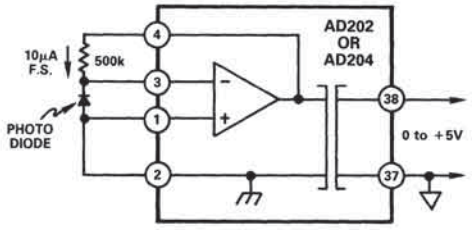


Figure 22. Photodiode Amplifier

(Circuit figures shown on this page are for SIP style packages. Refer to third page of this data sheet for proper DIP package pin-out.)

Precision, Wide Bandwidth, 3-Port Isolation Amplifier

AD210

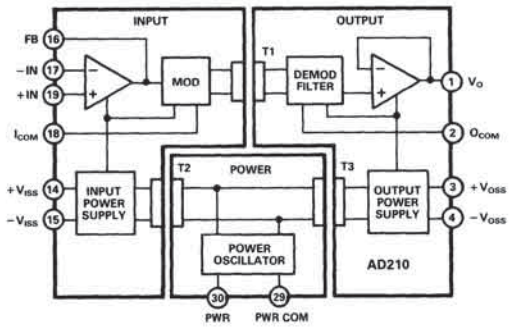
FEATURES

High CMV Isolation: 2500V rms Continuous
±3500V peak Continuous
Small Size: 1.00" × 2.10" × 0.350"
Three-Port Isolation: Input, Output, and Power
Low Nonlinearity: ±0.012% max
Wide Bandwidth: 20kHz Full-Power (−3dB)
Low Gain Drift: ±25ppm/°C max
High CMR: 120dB (G = 100V/V)
Isolated Power: ±15V @ ±5mA
Uncommitted Input Amplifier

APPLICATIONS

Multi-Channel Data Acquisition
High Voltage Instrumentation Amplifier
Current Shunt Measurements
Process Signal Isolation

AD210 FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

The AD210* is the latest member of a new generation of low cost, high performance isolation amplifiers. This three-port, wide bandwidth isolation amplifier is manufactured with surface-mounted components in an automated assembly process. The AD210 combines design expertise with state-of-the-art manufacturing technology to produce an extremely compact and economical isolator whose performance and abundant user features far exceed those offered in more expensive devices.

The AD210 provides a complete isolation function with both signal and power isolation supplied via transformer coupling internal to the module. The AD210's functionally complete design, powered by a single +15V supply, eliminates the need for an external DC/DC converter, unlike optically coupled isolation devices. The true three-port design structure permits the AD210 to be applied as an input or output isolator, in single or multi-channel applications. The AD210 will maintain its high performance under sustained common-mode stress.

Providing high accuracy and complete galvanic isolation, the AD210 interrupts ground loops and leakage paths, and rejects common-mode voltage and noise that may otherwise degrade measurement accuracy. In addition, the AD210 provides protection from fault conditions that may cause damage to other sections of a measurement system.

PRODUCT HIGHLIGHTS

The AD210 is a full-featured isolator providing numerous user benefits including:

High Common-Mode Performance: The AD210 provides 2500V rms (Continuous) and ±3500V peak (Continuous) common-mode voltage isolation between any two ports. Low input capacitance of 5pF results in a 120dB CMR at a gain of 100, and a low leakage current (2μA rms max @ 240V rms, 60Hz).

High Accuracy: With maximum nonlinearity of ±0.012% (B Grade), gain drift of ±25ppm/°C max and input offset drift of (±10±30/G) μV/°C, the AD210 assures signal integrity while providing high level isolation.

Wide Bandwidth: The AD210's full-power bandwidth of 20kHz makes it useful for wideband signals. It is also effective in applications like control loops, where limited bandwidth could result in instability.

Small Size: The AD210 provides a complete isolation function in a small DIP package just 1.00" × 2.10" × 0.350". The low profile DIP package allows application in 0.5" card racks and assemblies. The pinout is optimized to facilitate board layout while maintaining isolation spacing between ports.

Three-Port Design: The AD210's three-port design structure allows each port (Input, Output, and Power) to remain independent. This three-port design permits the AD210 to be used as an input or output isolator. It also provides additional system protection should a fault occur in the power source.

Isolated Power: ±15V @ 5mA is available at the input and output sections of the isolator. This feature permits the AD210 to excite floating signal conditioners, front-end amplifiers and remote transducers at the input as well as other circuitry at the output.

Flexible Input: An uncommitted operational amplifier is provided at the input. This amplifier provides buffering and gain as required, and facilitates many alternative input functions as required by the user.

*Patent Pending

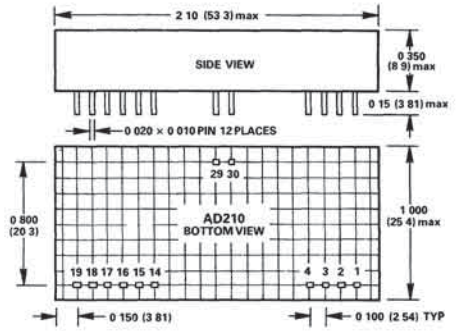
SPECIFICATIONS (typical @ + 25°C, & V_S = +15V unless otherwise specified)

MODEL	AD210AN	AD210BN
GAIN		
Range	1V/V – 100V/V	*
Error	± 2% max	± 1% max
vs. Temperature (0 to + 70°C)	± 25ppm/°C max	*
(– 25°C to + 85°C)	± 50ppm/°C max	*
vs. Supply Voltage	± 0.002%/V	*
Nonlinearity[1]	± 0.025% max	± 0.012% max
INPUT VOLTAGE RATINGS		
Linear Differential Range	± 10V	*
Maximum Safe Differential Input	± 15V	*
Max. CMV Input-to-Output		
ac, 60Hz, Continuous	2500V rms	*
dc, Continuous	± 3500V peak	*
Common-Mode Rejection		
60Hz, G = 100V/V		
$R_S \leq 500\Omega$ Impedance Imbalance	120dB	*
Leakage Current Input-to-Output		
@ 240Vrms, 60Hz	2μA rms max	*
INPUT IMPEDANCE		
Differential	$10^{12}\Omega$	*
Common Mode	$5G\Omega \| 5pF$	*
INPUT BIAS CURRENT		
Initial, @ + 25°C	30pA typ (400pA max)	*
vs. Temperature (0 to + 70°C)	10nA max	*
(– 25°C to + 85°C)	30nA max	*
INPUT DIFFERENCE CURRENT		
Initial, @ + 25°C	5pA typ (200pA max)	*
vs. Temperature (0 to + 70°C)	2nA max	*
(– 25°C to + 85°C)	10nA max	*
INPUT NOISE		
Voltage (1kHz)	$18nV/\sqrt{Hz}$	*
(10Hz to 10kHz)	4μV rms	*
Current (1kHz)	$0.01pA/\sqrt{Hz}$	*
FREQUENCY RESPONSE		
Bandwidth (– 3dB)		
G = 1V/V	20kHz	*
G = 100V/V	15kHz	*
Settling Time (± 10mV, 20V Step)		
G = 1V/V	150μs	*
G = 100V/V	500μs	*
Slew Rate (G = 1V/V)	1V/μs	*
OFFSET VOLTAGE (RTI)[2]		
Initial, @ + 25°C	(± 15 ± 45/G)mV max	(± 5 ± 15/G)mV max
vs. Temperature (0 to + 70°C)	(± 10 ± 30/G)μV/°C	*
(– 25°C to + 85°C)	(± 10 ± 50/G)μV/°C	*
RATED OUTPUT[3]		
Voltage, 2kΩ Load	± 10V min	*
Impedance	1Ω max	*
Ripple, (Bandwidth = 100kHz)	10mV p-p max	*
ISOLATED POWER OUTPUTS[4]		
Voltage, No Load	± 15V	*
Accuracy	± 10%	*
Current	± 5mA	*
Regulation, No Load to Full Load	See Text	*
Ripple	See Text	*
POWER SUPPLY		
Voltage, Rated Performance	+ 15V dc ± 5%	*
Voltage, Operating	+ 15V dc ± 10%	*
Current, Quiescent	50mA	*
Current, Full Load – Full Signal	80mA	*
TEMPERATURE RANGE		
Rated Performance	– 25°C to + 85°C	*
Operating	– 40°C to + 85°C	*
Storage	– 40°C to + 85°C	*
PACKAGE DIMENSIONS		
Inches	1.00 × 2.10 × 0.350	*
Millimeters	25.4 × 53.3 × 8.9	*

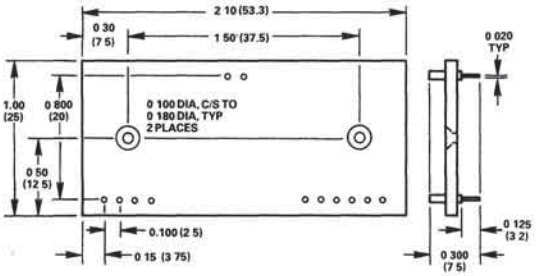
NOTES
*Specifications same as AD210AN.
[1]Gain nonlinearity increases by ± 0.002%/mA when the isolated power outputs are used.
[2]RTI – Referred to Input
[3]A reduced signal swing is recommended when both $\pm V_{ISS}$ and $\pm V_{OSS}$ supplies are fully loaded, due to supply voltage reduction.
[4]See text for detailed information.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1059 MATING SOCKET



AD210 PIN DESIGNATIONS

PIN	DESIGNATION	FUNCTION
1	V_O	Output
2	O_{COM}	Output Common
3	$+V_{OSS}$	+ Isolated Power @ Output
4	$-V_{OSS}$	– Isolated Power @ Output
14	$+V_{ISS}$	+ Isolated Power @ Input
15	$-V_{ISS}$	– Isolated Power @ Input
16	FB	Input Feedback
17	– IN	– Input
18	I_{COM}	Input Common
19	+ IN	+ Input
29	Pwr Com	Power Common
30	Pwr	Power Input



CAUTION
ESD (Electro-Static-Discharge) sensitive device. Permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

INSIDE THE AD210

The AD210 basic block diagram is illustrated in Figure 1. A +15V supply is connected to the power port, and ±15V isolated power is supplied to both the input and output ports via a 50kHz carrier frequency. The uncommitted input amplifier can be used to supply gain or buffering of input signals to the AD210. The fullwave modulator translates the signal to the carrier frequency for application to transformer T1. The synchronous demodulator in the output port reconstructs the input signal. A 20kHz, three-pole filter is employed to minimize output noise and ripple. Finally, an output buffer provides a low impedance output capable of driving a 2kΩ load.

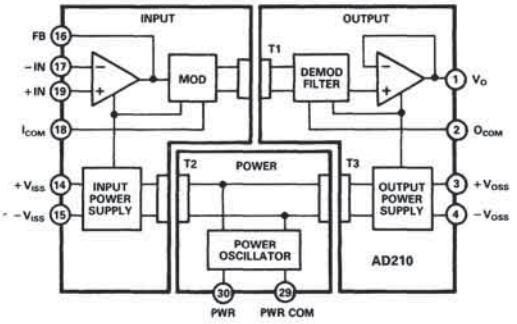


Figure 1. AD210 Block Diagram

USING THE AD210

The AD210 is very simple to apply in a wide range of applications. Powered by a single +15V power supply, the AD210 will provide outstanding performance when used as an input or output isolator, in single and multichannel configurations.

Input Configurations: The basic unity gain configuration for signals up to ±10V is shown in Figure 2. Additional input amplifier variations are shown in the following figures. For smaller signal levels Figure 3 shows how to obtain gain while maintaining a very high input impedance.

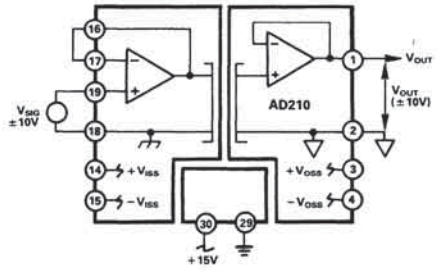


Figure 2. Basic Unity Gain Configuration

The high input impedance of the circuits in Figures 2 and 3 can be maintained in an inverting application. Since the AD210 is a three-port isolator, either the input leads or the output leads may be interchanged to create the signal inversion.

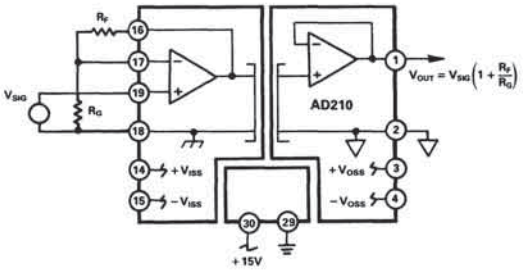


Figure 3. Input Configuration for G>1

Figure 4 shows how to accommodate current inputs or sum currents or voltages. This circuit configuration can also be used for signals greater than ±10V. For example, a ±100V input span can be handled with $R_F = 20k\Omega$ and $R_{S1} = 200k\Omega$.

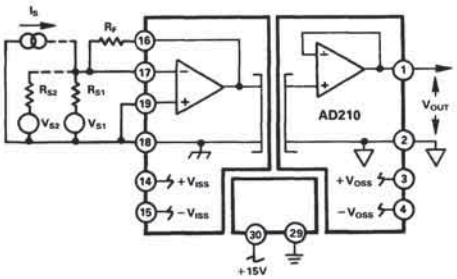


Figure 4. Summing or Current Input Configuration

Adjustments

When gain and offset adjustments are required, the actual circuit adjustment components will depend on the choice of input configuration and whether the adjustments are to be made at the isolator's input or output. Adjustments on the output side might be used when potentiometers on the input side would represent a hazard due to the presence of high common-mode voltage during adjustment. Offset adjustments are best done at the input side, as it is better to null the offset ahead of the gain.

Figure 5 shows the input adjustment circuit for use when the input amplifier is configured in the noninverting mode. This offset adjustment circuit injects a small voltage in series with the

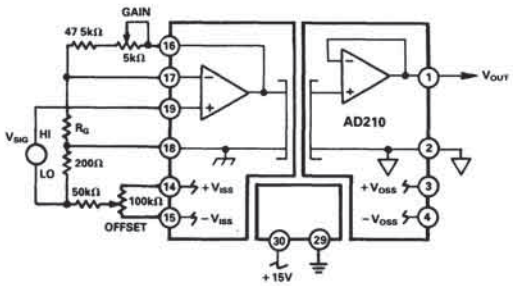


Figure 5. Adjustments for Noninverting Input

low side of the signal source. This will not work if the source has another current path to input common or if current flows in the signal source LO lead. To minimize CMR degradation, keep the resistor in series with the input LO below a few hundred ohms.

Figure 5 also shows the preferred gain adjustment circuit. The circuit shows R_F of 50kΩ, and will work for gains of ten or greater. The adjustment becomes less effective at lower gains (its effect is halved at G=2) so that the pot will have to be a larger fraction of the total R_F at low gain. At G=1 (follower) the gain cannot be adjusted downward without compromising input impedance; it is better to adjust gain at the signal source or after the output.

Figure 6 shows the input adjustment circuit for use when the input amplifier is configured in the inverting mode. The offset adjustment nulls the voltage at the summing node. This is preferable to current injection because it is less affected by subsequent gain adjustment. Gain adjustment is made in the feedback and will work for gains from 1 to 100V/V.

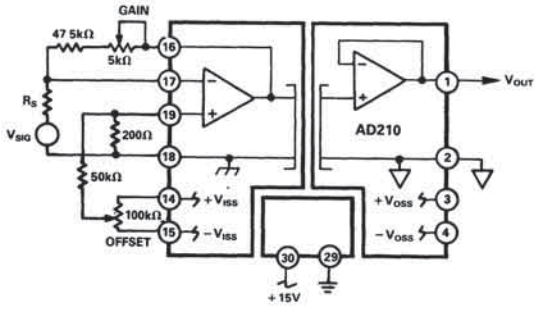


Figure 6. Adjustments for Inverting Input

Figure 7 shows how offset adjustments can be made at the output, by offsetting the floating output port. In this circuit, ±15V would be supplied by a separate source. The AD210's output amplifier is fixed at unity, therefore, output gain must be made in a subsequent stage.

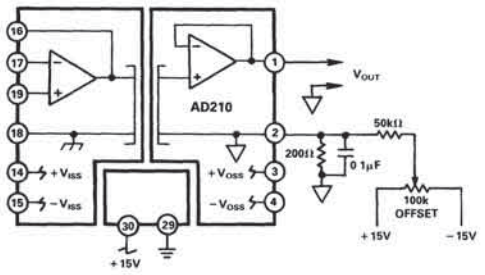


Figure 7. Output-Side Offset Adjustment

PCB Layout for Multichannel Applications: The unique pinout positioning minimizes board space constraints for multichannel applications. Figure 8 shows the recommended printed circuit board layout for a noninverting input configuration with gain.

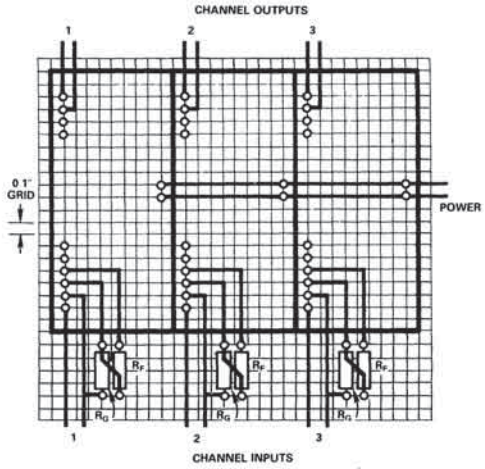


Figure 8. PCB Layout for Multichannel Applications with Gain

Synchronization: The AD210 is insensitive to the clock of an adjacent unit, eliminating the need to synchronize the clocks. However, in rare instances channel to channel pick-up may occur if input signal wires are bundled together. If this happens, shielded input cables are recommended.

PERFORMANCE CHARACTERISTICS

Common-Mode Rejection: Figure 9 shows the common-mode rejection of the AD210 versus frequency, gain and input source resistance. For maximum common-mode rejection of unwanted signals, keep the input source resistance low and carefully lay out the input, avoiding excessive stray capacitance at the input terminals.

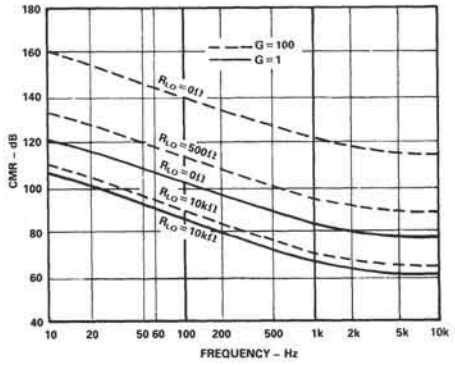


Figure 9. Common-Mode Rejection vs. Frequency

Phase Shift: Figure 10 illustrates the AD210's low phase shift and gain versus frequency. The AD210's phase shift and wide bandwidth performance make it well suited for applications like power monitors and controls systems.

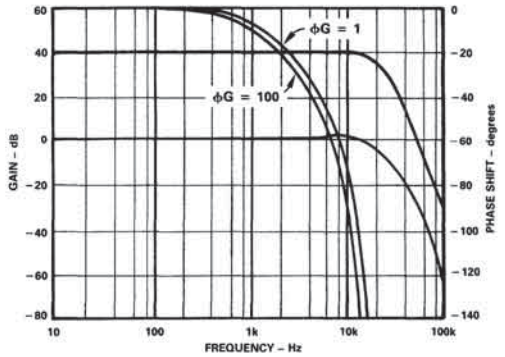


Figure 10. Phase Shift and Gain vs. Frequency

Input Noise vs. Frequency: Voltage noise referred to the input is dependent on gain and signal bandwidth. Figure 11 illustrates the typical input noise in nV/$\sqrt{Hz}$ of the AD210 for a frequency range from 10 to 10kHz.

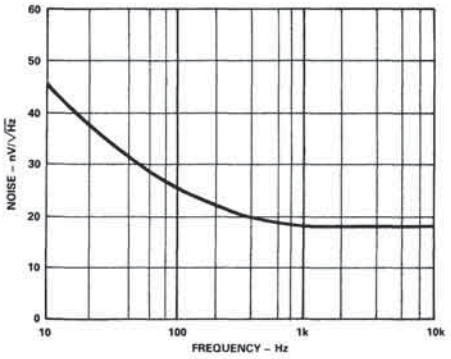


Figure 11. Input Noise vs. Frequency

Gain Nonlinearity vs. Output: Gain Nonlinearity is defined as the deviation of the output voltage from the best straight line, and is specified as % peak-to-peak of output span. The AD210B provides guaranteed maximum nonlinearity of ±0.012% with an output span of ±10V. The AD210's nonlinearity performance is shown in Figure 12.

Gain Nonlinearity vs. Output Swing: The gain nonlinearity of the AD210 varies as a function of total signal swing. When the output swing is less than 20 volts, the gain nonlinearity as a fraction of signal swing improves. The shape of the nonlinearity remains constant. Figure 13 shows the gain nonlinearity of the AD210 as a function of total signal swing.

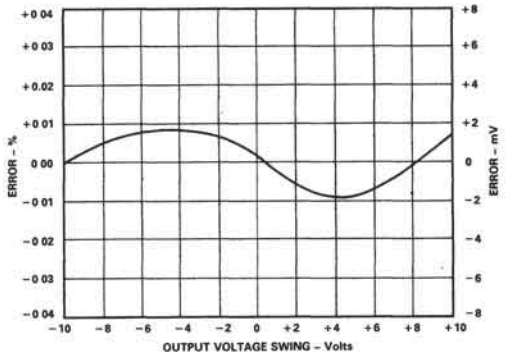


Figure 12. Gain Nonlinearity Error vs. Output

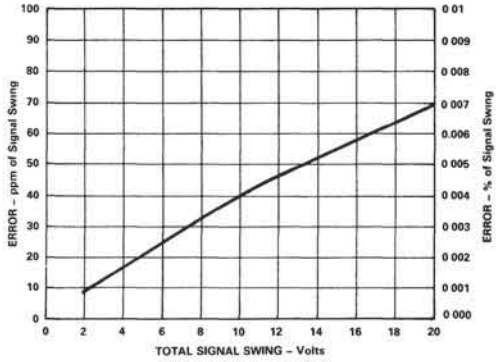


Figure 13. Gain Nonlinearity vs. Output Swing

Gain vs. Temperature: Figure 14 illustrates the AD210's gain vs. temperature performance. The gain versus temperature performance illustrated is for an AD210 configured as a unity gain amplifier.

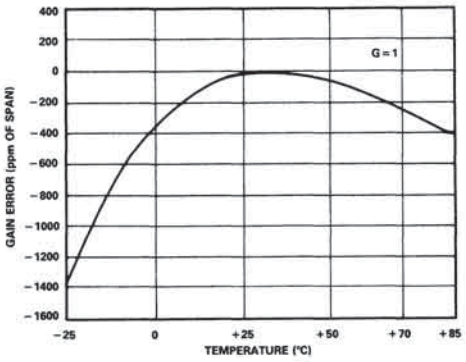


Figure 14. Gain vs. Temperature

Isolated Power: The AD210 provides isolated power at the input and output ports. This power is useful for various signal conditioning tasks. Both ports are rated at a nominal ±15V at 5mA.

The load characteristics of the isolated power supplies are shown in Figure 15. For example, when measuring the load rejection of the input isolated supplies V_{ISS}, the load is placed between $+V_{ISS}$ and $-V_{ISS}$. The curves labeled V_{ISS} and V_{OSS} are the individual load rejection characteristics of the input and the output supplies, respectively.

There is also some effect on either isolated supply when loading the other supply. The curve labeled CROSSLOAD indicates the sensitivity of either the input or output supplies as a function of the load on the opposite supply.

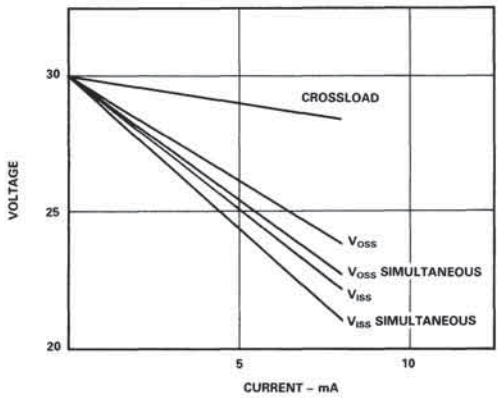


Figure 15. Isolated Power Supplies vs. Load

Lastly, the curves labeled V_{OSS} simultaneous and V_{ISS} simultaneous indicate the load characteristics of the isolated power supplies when an equal load is placed on both supplies.

The AD210 provides short circuit protection for its isolated power supplies. When either the input supplies or the output supplies are shorted to input common or output common, respectively, no damage will be incurred, even under continuous application of the short. However, the AD210 may be damaged if the input and output supplies are shorted simultaneously.

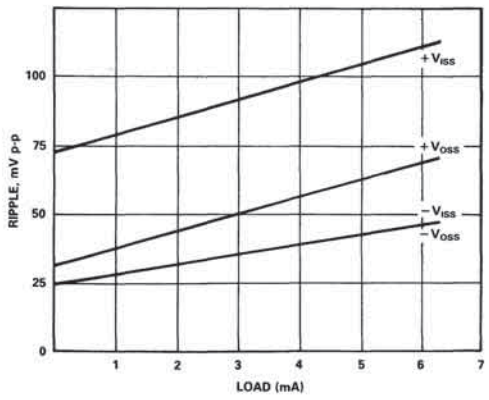


Figure 16a. Isolated Supply Ripple vs. Load (External 4.7μF Bypass)

Under any circumstances, care should be taken to ensure that the power supplies do not accidentally become shorted.

The isolated power supplies exhibit some ripple which varies as a function of load. Figure 16a shows this relationship. The AD210 has internal bypass capacitance to reduce the ripple to a point where performance is not affected, even under full load. Since the internal circuitry is more sensitive to noise on the negative supplies, these supplies have been filtered more heavily. Should a specific application require more bypassing on the isolated power supplies, there is no problem with adding external capacitors. Figure 16b depicts supply ripple as a function of external bypass capacitance under full load.

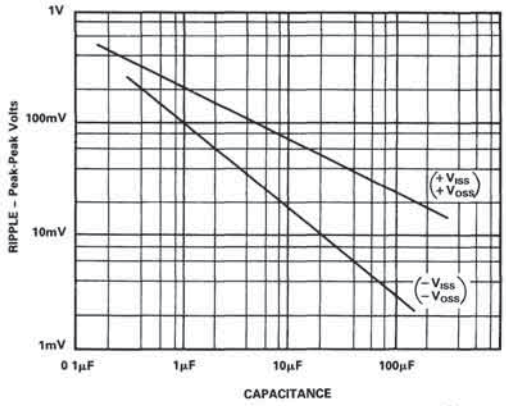


Figure 16b. Isolated Power Supply Ripple vs. Bypass Capacitance (Volts p-p, 1MHz Bandwidth, 5mA Load)

APPLICATIONS EXAMPLES

Noise Reduction in Data Acquisition Systems: Transformer coupled isolation amplifiers must have a carrier to pass both ac and dc signals through their signal transformers. Therefore, some carrier ripple is inevitably passed through to the isolator output. As the bandwidth of the isolator is increased more of the carrier signal will be present at the output. In most cases, the ripple at the AD210's output will be insigificant when compared to the measured signal. However, in some applications, particularly when a fast analog-to-digital converter is used following the isolator, it may be desirable to add filtering; otherwise ripple may cause inaccurate measurements. Figure 17 shows a circuit that will limit the isolator's bandwidth, thereby reducing the carrier ripple.

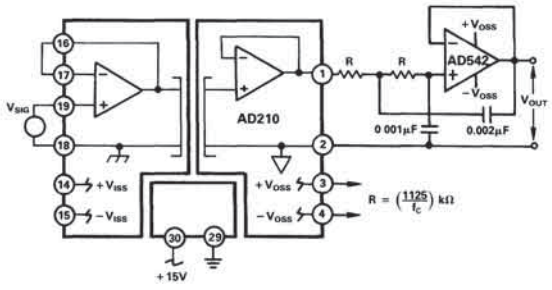


Figure 17. 2-Pole, Output Filter

Self-Powered Current Source

The output circuit shown in Figure 18 can be used to create a self-powered output current source using the AD210. The 2kΩ resistor converts the voltage output of the AD210 to an equivalent current $V_{OUT}/2k\Omega$. This resistor directly affects the output gain temperature coefficient, and must be of suitable stability for the application. The external low power op amp, powered by $+V_{OSS}$ and $-V_{OSS}$, maintains its summing junction at output common. All the current flowing through the 2kΩ resistor flows through the output Darlington pass devices. A Darlington configuration is used to minimize loss of output current to the base. The low leakage diode is used to protect the base-emitter junction against reverse bias voltages. Using $-V_{OSS}$ as a current return allows more than 10V of compliance. Offset and gain control may be done at the input of the AD210 or by varying the 2kΩ resistor and summing a small correction current directly into the summing node. A nominal range of 1-5mA is recommended since the current output cannot reach zero due to reverse bias and leakage currents. If the AD210 is powered from the input potential, this circuit provides a fully isolated, wide bandwidth current output. This configuration is limited to 5mA output current.

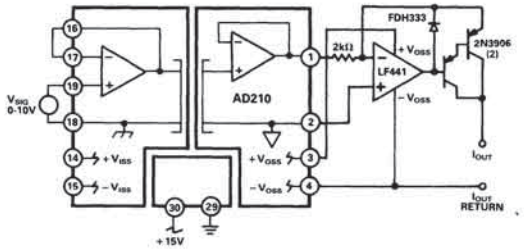


Figure 18. Self-Powered Isolated Current Source

Isolated V-to-I Converter

Illustrated in Figure 19, the AD210 is used to convert a 0 to +10V input signal to an isolated 4-20mA output current. The AD210 isolates the 0 to +10V input signal and provides a proportional voltage at the isolator's output. The output circuit converts the input voltage to a 4-20mA output current, which in turn is applied to the loop load R_{LOAD}.

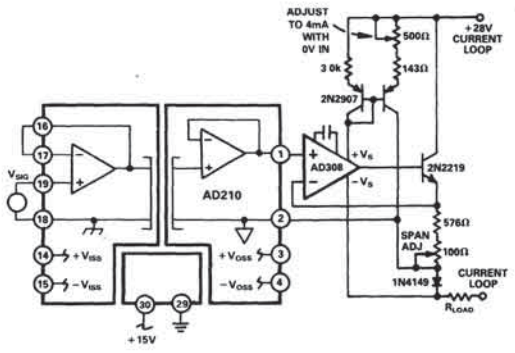


Figure 19. Isolated Voltage-to-Current Loop Converter

Isolated Thermocouple Amplifier

The AD210 application shown in Figure 20 provides amplification, isolation and cold-junction compensation for a standard J type thermocouple. The AD590 temperature sensor accurately monitors the input terminal (cold-junction). Ambient temperature changes from 0 to +40°C sensed by the AD590, are cancelled out at the cold junction. Total circuit gain equals 183; 100 and 1.83, from A1 and the AD210 respectively. Calibration is performed by replacing the thermocouple junction with plain thermocouple wire and a millivolt source set at 0.0000V (0°C) and adjusting R_O for E_{OUT} equal to 0.000V. Set the millivolt source to +0.02185V (400°C) and adjust R_G for V_{OUT} equal to +4.000V. This application circuit will produce a nonlinearized output of about +10mV/°C for a 0 to +400°C range.

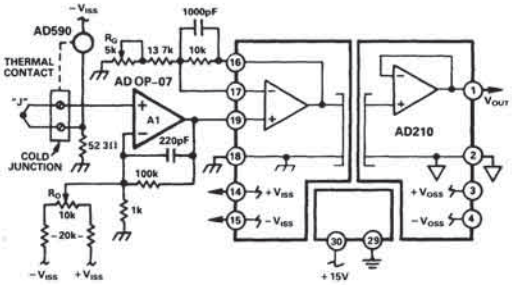


Figure 20. Isolated Thermocouple Amplifier

Precision Floating Programmable Reference

The AD210, when combined with a digital-to-analog converter, can be used to create a fully floating voltage output. Figure 21 shows one possible implementation.

The digital inputs of the AD7541 are TTL or CMOS compatible. Both the AD7541 and AD581 voltage reference are powered by the isolated power supply $+V_{ISS}$. I_{COM} should be tied to input digital common to provide a digital ground reference for the inputs.

The AD7541 is a current output DAC and, as such, requires an external output amplifier. The uncommitted input amplifier internal to the AD210 may be used for this purpose. For best results, its input offset voltage must be trimmed as shown.

The output voltage of the AD210 will go from 0V to −10V for digital inputs of 0 and full scale, respectively. However, since the output port is truly isolated, V_{OUT} and O_{COM} may be freely interchanged to get 0 to +10V.

This circuit provides a precision 0–10V programmable reference with a ±3500V common-mode range.

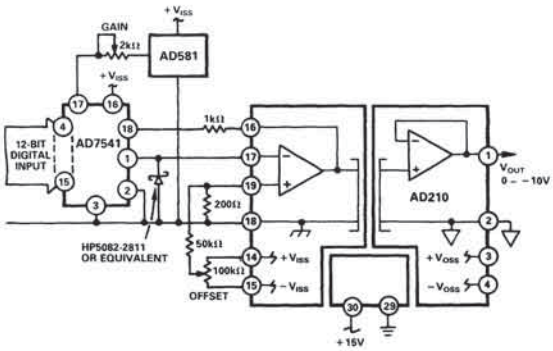


Figure 21. Precision Floating Programmable Reference

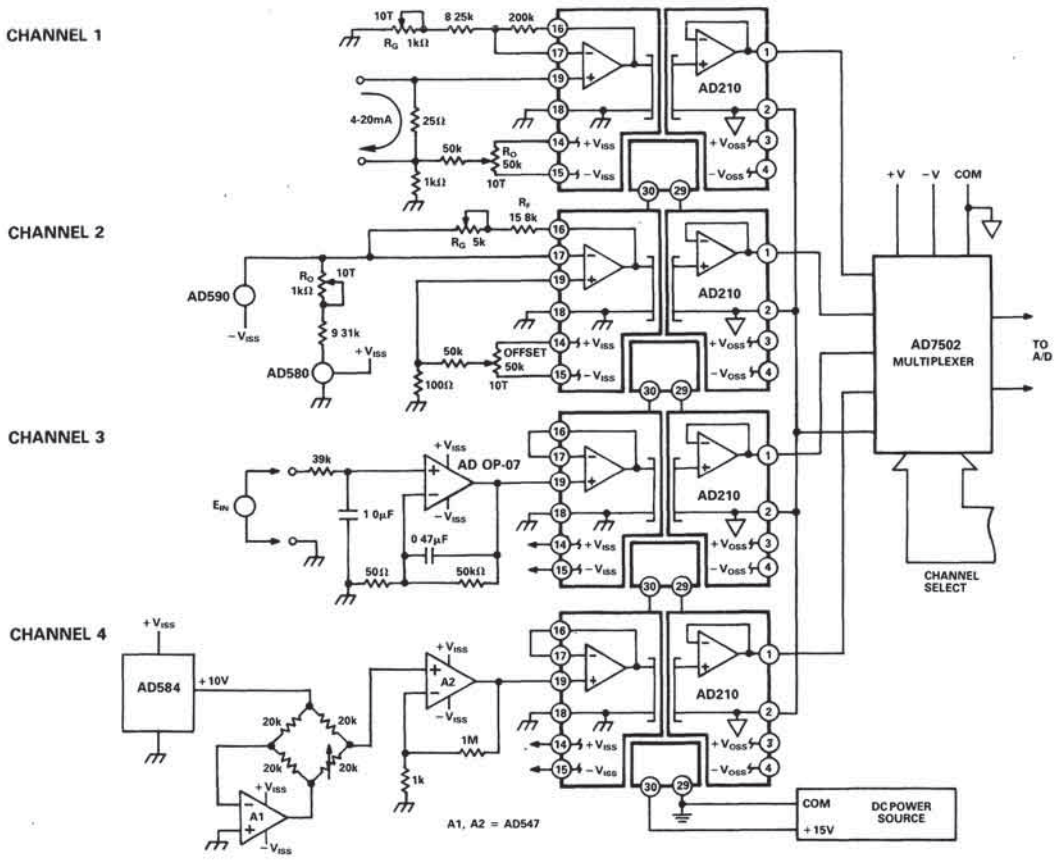


Figure 22. Multichannel Data Acquisition Front-End

MULTICHANNEL DATA ACQUISITION FRONT-END

Illustrated in Figure 22 is a four-channel data acquisition front-end used to condition and isolate several common input signals found in various process applications. In this application, each AD210 will provide complete isolation from input to output as well as channel to channel. By using an isolator per channel, maximum protection and rejection of unwanted signals is obtained. The three-port design allows the AD210 to be configured as an input or output isolator. In this application the isolators are configured as input devices with the power port providing additional protection from possible power source faults.

Channel 1: The AD210 is used to convert a 4-20mA current loop input signal into a 0-10V input. The 25Ω shunt resistor converts the 4-20mA current into a +100 to +500mV signal. The signal is offset by −100mV via R_O to produce a 0 to +400mV input. This signal is amplified by a gain of 25 to produce the desired 0 to +10V output. With an open circuit, the AD210 will show −2.5V at the output.

Channel 2: In this channel, the AD210 is used to condition and isolate a current output temperature transducer, Model AD590. At +25°C, the AD590 produces a nominal current of 298.2μA. This level of current will change at a rate of 1μA/°C. At −17.8°C (0°F), The AD590 current will be reduced by 42.8μA to +255.4μA. The AD580 reference circuit provides an equal but opposite current, resulting in a zero net current flow, producing a 0V output from the AD210. At +100°C (+212°F), the AD590 current output will be 373.2μA minus the 255.4μA offsetting current from the AD580 circuit to yield a +117.8μA input current. This current is converted to a voltage via R_F and R_G to produce an output of +2.12V. Channel 2 will produce an output of +10mV/°F over a 0 to +212°F span.

Channel 3: Channel 3 is a low level input channel configured with a high gain amplifier used to condition millivolt signals. With the AD210's input set to unity and the input amplifier set for a gain of 1000, a ±10mV input will produce a ±10V at the AD210's output.

Channel 4: Channel 4 illustrates one possible configuration for conditioning a bridge circuit. The AD584 produces a +10V excitation voltage, while A1 inverts the voltage, producing negative excitation. A2 provides a gain of 1000V/V to amplify the low level bridge signal. Additional gain can be obtained by reconfiguration of the AD210's input amplifier. $\pm V_{ISS}$ provides the complete power for this circuit, eliminating the need for a separate isolated excitation source.

Each channel is individually addressed by the multiplexer's channel select. Additional filtering or signal conditioning should follow the multiplexer, prior to an analog-to-digital conversion stage.

ANALOG DEVICES

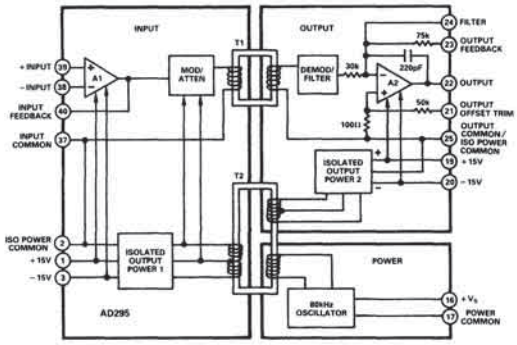
Precision Hybrid Isolation Amplifier

AD295

FEATURES
Low Nonlinearity: ±0.012% max (AD295C)
Low Gain Drift: ±60ppm/°C max
Floating Input and Output Power: ±15V dc @ 5mA
3-Port Isolation: ±2500V CMV (Input to Output)
Complies with NEMA ICS1-111
Gain Adjustable: 1V/V to 1000V/V
User Configurable Input Amplifier

APPLICATIONS
Motor Controls
Process Signal Isolator
High Voltage Instrumentation Amplifier
Multi-Channel Data Acquisition Systems
Off Ground Signal Measurements

AD295 FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

The AD295 is a high accuracy, high reliability hybrid isolation amplifier designed for industrial, instrumentation and medical applications. Three performance versions are available offering guaranteed nonlinearity error at 10V p-p output: ±0.05% max (AD295A), ±0.025% max (AD295B), ±0.012% max (AD295C). Using a pulse width modulation technique the AD295 provides 3-port isolation between input, output and power supply ports. Using this technique, the AD295 interrupts ground loops and leakage paths and minimizes the effect of high voltage transients. Additionally, floating (isolated) power ±15V dc @ 5mA is available at both the input and output. The AD295's gain can be programmed at the input, output or both sections allowing for user flexibility. An uncommitted input amplifier allows configuration as a buffer, inverter, subtractor or differential amplifier.

The AD295 is provided in an epoxy sealed ceramic 40-pin package that insures quality performance, high stability and accuracy. Input/output pin spacing complies with NEMA (ICS1-111) separation specifications required for many industrial applications.

WHERE TO USE THE MODEL AD295

Industrial: The AD295 is designed for measuring signals in harsh industrial environments. The AD295 provides high accuracy with complete galvanic isolation and protection from transients or where ground fault currents or high common-mode voltages are present. The AD295 can be applied in process controllers, current loop receivers, motor controls and weighing systems.

Instrumentation: In data acquisition systems the AD295 provides common-mode rejection for conditioning thermocouples, strain gauges or other low-level signals where high performance and system protection is required.

Medical: In biomedical and patient monitoring equipment like diagnostic systems and blood pressure monitors, the AD295 provides protection from lethal ground fault currents. Low level signal recording and monitoring is achieved with the AD295's low input noise (2μV p-p @ G=1000V/V) and high CMR (106dB @ 60Hz).

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Isolated power supply sections at the input and output provide ±15V dc @ 5mA. Isolated power is load regulated to 4%. This feature permits the AD295 to excite floating signal conditioners, front-end buffer amplifiers and remote transducers at the input and external circuitry at the output. This eliminates the need for a separate dc/dc converter.

Input Amplifier: The uncommitted input amplifier allows the user to configure the input as a buffer, inverter, subtractor or differential amplifier to meet the application need.

Adjustable Gain: Gain can be selected at the input, output or both. Thus, circuit response can be tailored to the user's application. The AD295 provides the user with flexibility for circuit optimization without requiring external active components.

Three-Port Isolation: Provides true galvanic isolation between input, output and power supply ports. Eliminates the need for power supply and output ports being returned through a common ground.

Wide Operating Temperature: The AD295 is designed to operate over the −40°C to +100°C temperature range with rated performance over −25°C to +85°C.

Leakage: The low coupling capacitance between input and output yields a ground leakage current of less than 2μA rms at 115V ac, 60Hz. The AD295 meets standards established by UL STD 544.

SPECIFICATIONS (typical @ +25°C, & V_S = +15V unless otherwise noted)

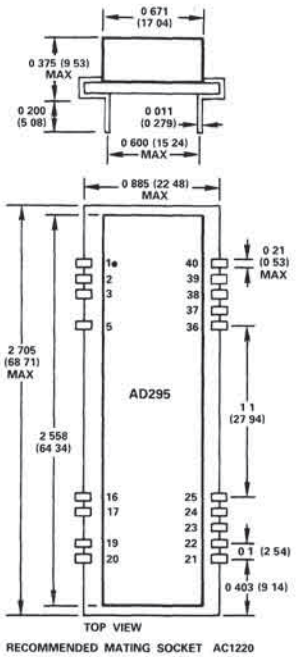
MODEL	AD295A	AD295B	AD295C
GAIN			
Range	1V/V to 1000V/V	*	*
Open Loop	100dB	*	*
Accuracy G = 1V/V	±1.5%	*	*
vs Temperature (−25°C to +85°C)			
G = 1V/V to 100V/V	±60ppm/°C max	*	*
Nonlinearity (±5V Swing) G = 1V–100V/V	±0.05% max	±0.025% max	±0.012% max
INPUT VOLTAGE RATINGS			
Linear Differential Range	±10V min	*	*
Max Safe Differential Input	±15V	*	*
Max CMV (Input to Output)			
Continuous ac or dc	±2500V peak	*	*
ac, 60Hz, 1 Minute Duration	2500V rms	*	*
Max CMV (Input to Power Common/Output to Power Common)			
Continuous ac or dc	±2000V peak	*	*
ac, 60Hz, 1 Minute Duration	2000V rms	*	*
CMR, Input to Output 60Hz, G = 1V/V			
$R_S \leq 1k\Omega$ Balanced Source Impedance	106dB	*	*
$R_S \leq 1k$ Source Impedance Imbalance	103dB min	*	*
Max Leakage Current, Input to Output			
@ 115V ac, 60Hz	2μA rms max	*	*
INPUT IMPEDANCE			
Differential	$5 \times 10^7\Omega \| 33pF$	*	*
Common Mode	$10^8\Omega \| 20pF$	*	*
INPUT BIAS CURRENT			
Initial, @ +25°C	5nA max	*	*
vs Temperature (−25°C to +85°C)	−25pA/°C max	*	*
INPUT DIFFERENCE CURRENT			
Initial, @ +25°C	±2nA max	*	*
vs. Temperature (−25°C to +85°C)	±5pA/°C max	*	*
INPUT NOISE (Gain = 1000V/V)			
Voltage			
0.01Hz to 10Hz	2μV p-p	*	*
10Hz to 1kHz	1μV rms	*	*
Current			
0.01Hz to 10Hz	10pA p-p	*	*
FREQUENCY RESPONSE			
Small Signal (−3dB)			
G = 1V/V to 100V/V	4.5kHz	*	*
G = 1000V/V	600Hz	*	*
Full Power, 20V p-p Output			
G = 1V/V to 100V/V	1.4kHz	*	*
G = 1000V/V	200Hz	*	*
Slew Rate G = 1V/V to 100V/V	0.1V/μs	*	*
Settling Time G = 1V/V			
(to ±0.1% for 10V Step)	550μs	*	*
(to ±0.1% for 20V Step)	700μs	*	*
OFFSET VOLTAGE, REFERRED TO INPUT			
Initial @ +25°C (Adjustable to Zero)	$\left(\pm 3 \pm \frac{15}{G_{IN}}\right)$ mV max	*	*
vs. Temperature (−25°C to +85°C)	$\left(\pm 10 \pm \frac{450}{G_{IN}}\right)\frac{\mu V}{°C}$ max	$\left(\pm 3 \pm \frac{300}{G_{IN}}\right)\frac{\mu V}{°C}$ max	$\left(\pm 1.5 \pm \frac{150}{G_{IN}}\right)\frac{\mu V}{°C}$ max
vs Supply	$\left(\pm 1 \pm \frac{200}{G_{IN}}\right)\mu V/\%$	*	*
RATED OUTPUT			
Voltage, 2kΩ Load	±10V min	*	*
Output Impedance	2Ω (dc to 100Hz)	*	*
Output Ripple (10Hz to 10kHz)	6mV p-p	*	*
(10Hz to 100kHz)	40mV p-p	*	*
ISOLATED POWER SUPPLIES[1] (V_{ISO1} & V_{ISO2})			
Voltage	±15V dc	*	*
Accuracy	±5%	*	*
Current[2]	±5mA max	*	*
Load Regulation (No Load to Full Load)	−4%	*	*
Ripple, 100kHz BW	12mV p-p	*	*
POWER SUPPLY (+V_S)			
Voltage, Rated Performance	+15V dc ±3%	*	*
Voltage, Operating	+12V dc to +16V dc	*	*
Current, Quiescent (V_S = +15V)	40mA	*	*
With V_{ISO} Loaded	45mA	*	*
TEMPERATURE RANGE			
Rated Performance	−25°C to +85°C	*	*
Operating	−40°C to +100°C	*	*
Storage	−40°C to +100°C	*	*
CASE DIMENSIONS	2.7" × 0.88" × 0.375"	*	*

NOTES
[1] V_{ISO2} accuracy and regulation 10%
[2] ±10mA can be supplied by V_{ISO1} if V_{ISO2} is not used

*Specifications same as AD295A
Specifications subject to change without notice

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



RECOMMENDED MATING SOCKET AC1220

PIN DESIGNATIONS

PIN	FUNCTION	PIN	FUNCTION
1	+15V (+V_{ISO1})	40	INPUT FEEDBACK
2	V_{ISO1} COM	39	+INPUT
3	−15V (−V_{ISO1})	38	−INPUT
		37	INPUT COM
5	NO CONNECTION	36	NO CONNECTION
16	+V_S	25	OUTPUT COM/ V_{ISO2} COM
17	POWER COMMON	24	FILTER
		23	OUTPUT FEEDBACK
19	+15V (+V_{ISO2})	22	OUTPUT
20	−15V (+V_{ISO2})	21	OUTPUT OFFSET TRIM

INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of the AD295, care must be taken to keep the capacitance balanced about the input terminals. Use twisted shielded cable for the input signal to reduce inductive and capacitive pick-up. During circuit layout or interassembly connections, twisted wire pairs are recommended for power input and signal output. For basic isolator connections, see Figure 1. Capacitors C1-C5 are required in all applications to achieve the low noise rating and provide adequate filtering of the power supply.

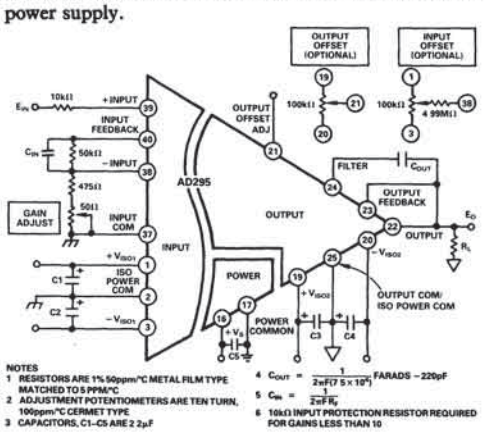


Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The AD295 obtains its outstanding performance from a pulse width modulation technique using transformer coupling. This technique permits both signal and power transfer from input to the output stage of the isolator. Additionally, this technique provides higher noise immunity and lower nonlinearity than obtained from optically coupled or amplitude modulated transformer coupled techniques.

The three basic sections of the AD295 are shown in Figure 2. The power section 80kHz oscillator signal is transferred to the input and output sections via T2. The signal is then rectified and filtered providing dc power for that section's circuitry and for external application use. The input section consists of input amplifier A1 and the input modulator attenuator circuit. A triangular waveform derived from the 80kHz oscillator is sent to the modulator. If the input signal of A1 is zero, the triangle wave remains symmetrical. If A1 moves away from zero, the triangle wave moves positive or negative becoming asymmetrical. These modulated signals are converted to a pulsed waveform and transferred to the output section via T1. In the output section the signals are demodulated and filtered. The output amplifier A2 provides gain and additional filtering.

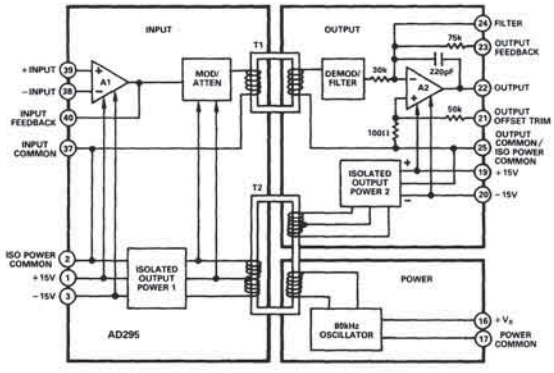


Figure 2. Basic Block Diagram

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance arises from stray coupling capacitance effects between the input terminals and signal output terminals. Each are shunted by leakage resistance values exceeding 50GΩ. Figure 3 illustrates the AD295's capacitance between terminals.

Terminal Ratings: CMV performance is given in both continuous ac, or dc peak ratings. Continuous peak ratings apply from dc up to the normal full power response frequency. Figure 3 illustrates the AD295's ratings between terminals. Note that for the ±2500V rating between the input and output terminals to apply, the AD295 must be used in a three port configuration. If the output common is tied to the power common, the input to output CMV rating is ±2000V.

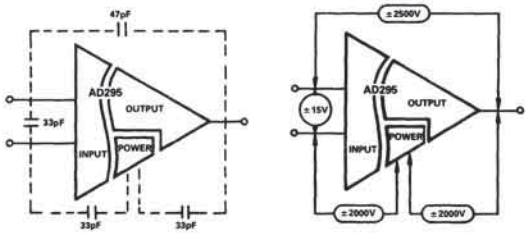


Figure 3. Interelectrode Capacitance and Terminal Ratings

OFFSET AND GAIN ADJUSTMENT PROCEDURE

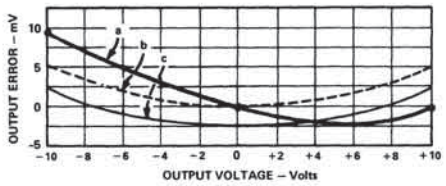
The calibration procedure, illustrated in Circuits 1 and 2, shows the recommended techniques that can be used to minimize output error. In this example, the output span is −10V to +10V.

Offset Adjustment

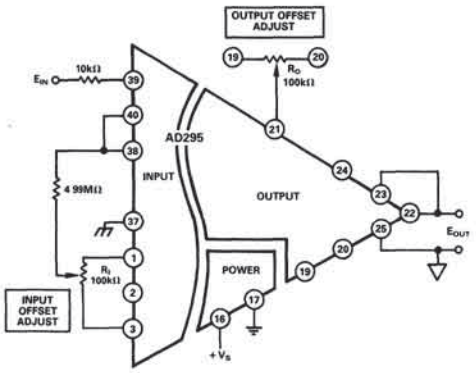
1. Configure the AD295 as shown in Circuit 1. G = 1.
2. Apply E_{IN} = 0V dc and adjust R_O for E_O = 0 volts.
3. Configure the AD295 as shown in Circuit 2. G = 100.
4. Apply E_{IN} = 0V dc and adjust R_I for E_O = 0 volts.
5. Repeat steps 1–4 if necessary.

Gain Adjust

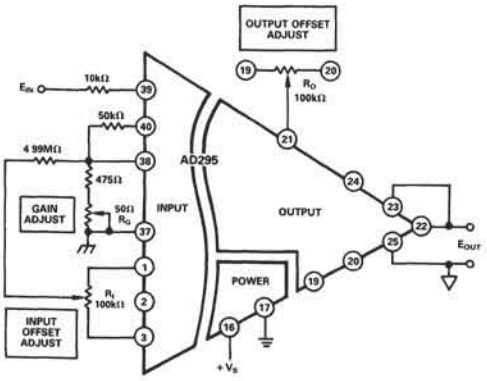
6. Apply E_{IN} = +0.1V dc adjust R_G for E_0 = +10.000V dc.
7. Apply E_{IN} = −0.1V dc and measure the output error (see Curve a.)



8. Adjust R_G until the output error is one half that measured in step 6 (see Curve b).
9. Apply $E_{IN} = +0.1V$ dc and adjust R_O until the output error is one half that measured in step 7 (see Curve c).
10. Repeat steps 6–9 if necessary.



Circuit 1. G = 1



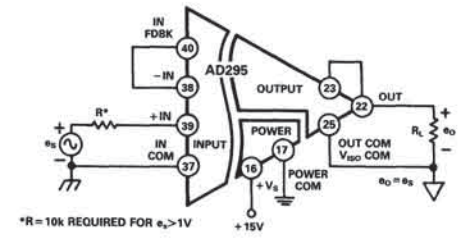
Circuit 2. G = 100

SELECTING GAIN

The AD295 basic gain is unity from input to output. All input signals are attenuated by 2.5 at the input modulator/attenuator then amplified at the output (see Figure 2).

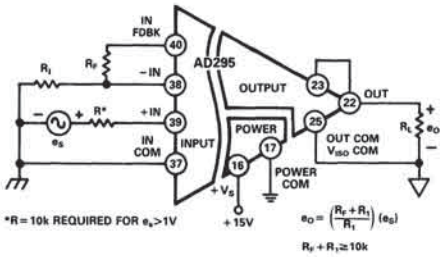
The AD295 contains both input and output amplifiers, the gains of which can be set independently. Figure 4 illustrates the basic gain configurations. Taking input gain helps dilute output stage offset drift and is recommended where offset drift is to be minimized since taking output gain multiplies output drift by the gain taken. Output gain can be used for improved linearity and frequency response at the expense of higher offset drift.

Figure 4a illustrates the basic unity gain configuration. With the uncommitted input amplifier configured as a buffer and pins 22 and 23 of the output amplifier jumpered, $e_O = e_S$.

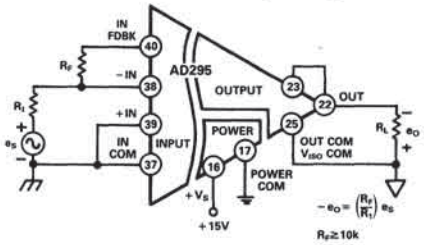


a. Basic Unity Gain Configuration

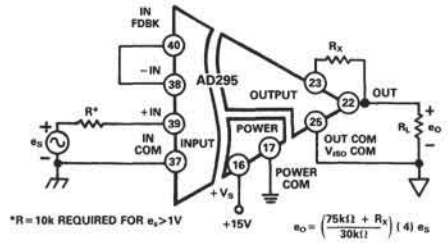
Input to output gain greater than unity can be independently set at the input, output, or both. For input gain configuration see Figures 4b and 4c. Output gain configuration is shown in Figure 4d.



b. Basic Gain Noninverting Configuration



c. Input Gain Inverting Configuration



d. Output Gain Noninverting Configuration

Figure 4. Input/Output Gain Configurations

PERFORMANCE CHARACTERISTICS

Phase Shift vs. Frequency: The phase shift vs. frequency response, for the AD295 is shown in Figure 5.

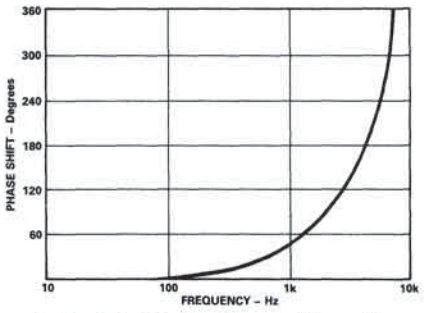


Figure 5. Typical AD295 – Phase Shift vs. Frequency

CMR vs. Frequency: Input-to-output CMR is dependent on source impedance imbalance, input signal frequency and amplifier gain. CMR is rated at 60Hz and 1kΩ source impedance imbalance at a gain of 1V/V. Figure 6 illustrates the CMR vs. frequency for the AD295. CMR approaches 120dB at dc with a source impedance imbalance of 1kΩ.

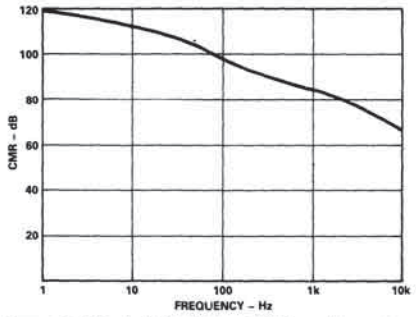


Figure 6. Typical AD295 – CMR vs. Frequency

Input Voltage Noise vs. Bandwidth: Voltage noise referred to the input is dependent on gain and bandwidth. Figure 7 illustrates the typical input noise in μV peak-to-peak in a 10Hz to 10kHz frequency range.

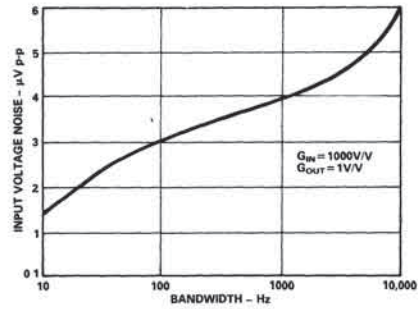


Figure 7. Typical AD295 – Input Voltage Noise vs. Bandwidth

Output Voltage Noise vs. Bandwidth: Voltage noise referred to the output is dependent on gain, bandwidth, input and output noise contributions. Figure 8 illustrates the typical output noise in mV peak-to-peak in a 10Hz to 10kHz frequency range.

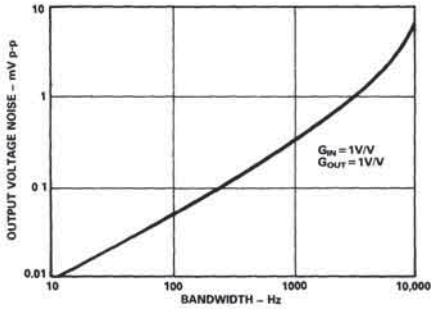


Figure 8. Typical AD295 – Output Voltage Noise vs. Bandwidth

Gain Nonlinearity vs. Output Swing: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as % peak-to-peak of output voltage span, e.g., nonlinearity of model AD295A operating at an output span of 10V peak-to-peak (±5V) is ±0.05% or ±5mV. Figure 9 illustrates the gain nonlinearity for output swing up to ±10V (20V peak-to-peak).

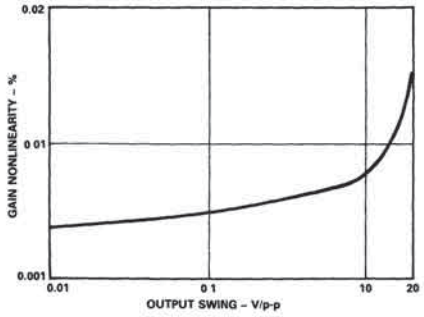


Figure 9. Typical AD295 – Gain Nonlinearity vs. Output Swing

Full Power Bandwidth vs. Gain: Figure 10 illustrates the full power bandwidth vs. gain for the AD295. A 1.4kHz full power response is possible with gain up to 100V/V.

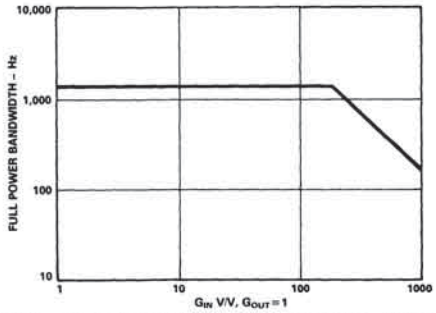


Figure 10. Typical AD295 – Full Power Bandwidth vs. Gain

Small Signal Bandwidth vs. Gain: Figure 11 illustrates the small signal bandwidth vs. gain for the AD295. The small signal response remains at 4.5kHz for gain up to 100V/V.

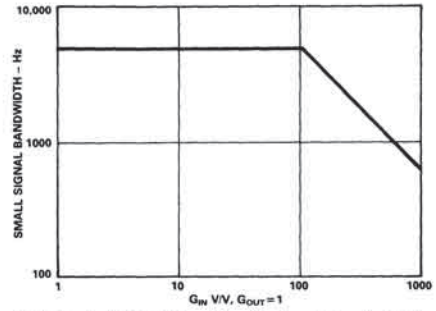


Figure 11. Typical AD295 – Small Signal Bandwidth vs. Gain

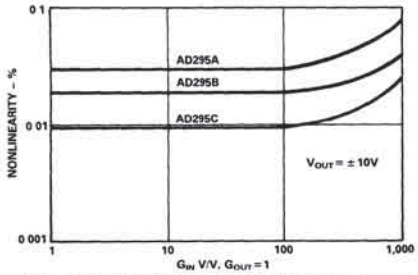


Figure 12. Typical AD295 – Gain Nonlinearity vs. Gain

Isolated Strain Gauge Using Front End of AD295
The AD295 can be used to condition and isolate differential signal sources like those present with strain gauge measurements. Figure 13 illustrates one possible configuration for conditioning a strain gauge. Amplifiers A1 and A2 are powered by the AD295's input isolated power supply. This eliminates the need for a separate dc/dc converter and provides a completely floated differential input. Input gain is selected via R_G and determined by the input gain formula.

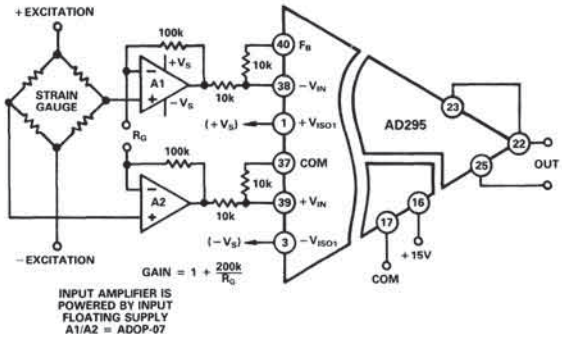


Figure 13. Isolated Strain Gauge Using Front End of AD295

Isolated Temperature Measurement with Cold Junction Compensation
The AD295 can be used to condition, isolate and provide cold junction compensation of thermocouples in temperature measurement applications. With the circuit shown in Figure 14, the AD590 must be thermally connected to the cold junction terminal for an accurate temperature measurement of the terminals. Using this circuit, accurate temperature measurements using the industry's popular J type thermocouple can be made.

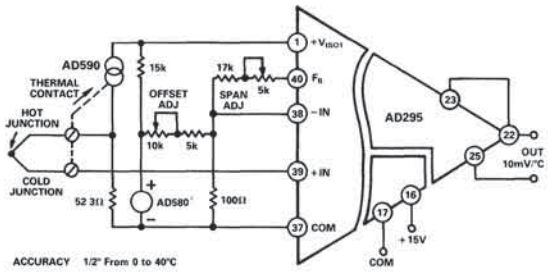


Figure 14. Isolated Temperature Measurement with Cold Junction Compensation

Isolated Voltage-to-Current Loop Converter
Illustrated in Figure 15, the AD295 is used to convert a 0 to +10V input signal to a standard 4-to-20mA current. Here high common-mode rejection and high common-mode voltage suppression are easily obtained with the AD295. The AD295 conditions the 0 to +10V input signal and provides a proportional voltage at the isolator's output. This output signal is converted to a 4-to-20mA current, which in turn is applied to the loop load R_{LOAD}.

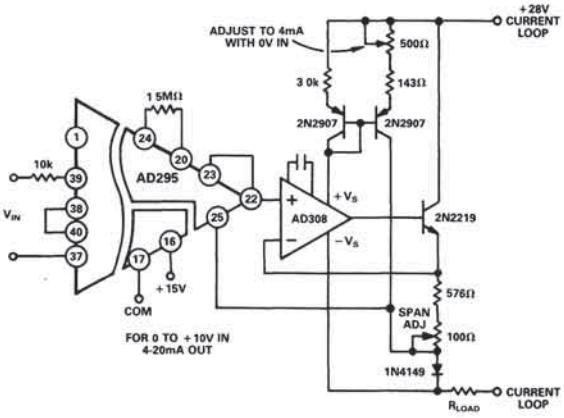


Figure 15. Isolated Voltage-to-Current Loop Converter

Noise Reduction in Data Acquisition Systems
In critical low noise applications like when an isolation amplifier precedes an analog to-digital converter, it may be desirable to add filtration, otherwise output ripple may cause inaccurate conversions. The 2-pole low-pass active filter shown in Figure 16 limits isolator bandwidth of the AD295. The filter will reduce output ripple and provide smoothing of discontinuous high frequency waveforms.

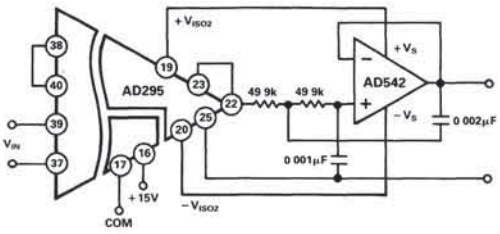


Figure 16. 2-Pole, 2kHz Active Filter

Economy, High Performance, Self-Contained Isolation Amplifier

Model 284J

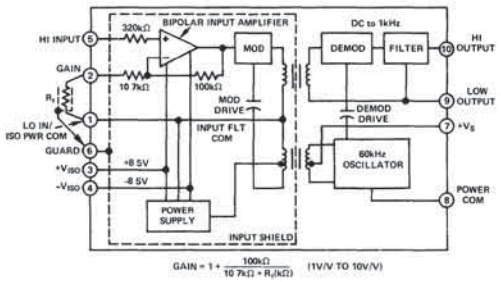
FEATURES

Low Cost
Low Nonlinearity: ±0.05% @ 10V pk-pk Output
High Gain Stability: ±0.0075%/°C, ±0.001%/1000 hours
Isolated Power Supply: ±8.5V dc @ ±5mA
High CMR: 110dB min with 5kΩ Imbalance
High CMV: ±5000V_{pk}, 10ms Pulse; ±2500V dc continuous
Small Size: 1.5″ x 1.5″ x 0.6″
Adjustable Gain: 1 to 10V/V; Single Resistor Adjust
Meets IEEE Std 472: Transient Protection (SWC)
Meets UL Std 544 Leakage: 2.0μA max @ 115V ac, 60Hz

APPLICATIONS

Biomedical and Patient Monitoring Instrumentation
Ground Loop Elimination in Industrial Control
Off-Ground Signal Measurements
4-20mA Isolated Current Loop Receiver

284J FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

Model 284J is a low cost isolation amplifier featuring isolated power, ±8.5V dc @ ±5mA loads, ±2500V dc off-ground isolation (CMV) and 110dB minimum CMR at 60Hz, 5kΩ source imbalance, in a compact 1.5″ x 1.5″ x 0.6″ epoxy encapsulated package. This improved design achieves low nonlinearity of ±0.05% @ 10V pk-pk output, gain stability of ±0.0075%/°C and input offset drift of ±30μV/°C at G = 10V/V. Using modulation techniques with reliable transformer isolation, model 284J will interrupt ground loops, leakage paths and high voltage transients to ±5kV_{pk} (10ms pulse) providing dc to 1kHz (-3dB) response over an adjustable gain range of 1V/V to 10V/V. Model 284J's fully floating guarded input stage and floating isolated power for external input circuitry, offers versatility for both medical and industrial OEM applications.

WHERE TO USE MODEL 284J

Medical Applications: In all biomedical and patient monitoring equipment such as multi-lead ECG recorders and portable diagnostic designs, model 284J offers protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with model 284J's low input noise (8μV p-p) and high CMR (110dB, min).

Industrial Applications: In computer interface systems, process signal isolators and high CMV instrumentation, model 284J offers complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface is afforded with model 284J's 10V pk-pk input signal capability at a gain of 1V/V operation. In portable field designs, model 284J's single supply, low power drain of 85mW @ +12V operation offers long battery operation.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: Dual ±8.5V dc @ ±5mA, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers and remote transducers such as thermistors or bridges.

Adjustable Gain: Model 284J's adjustable gain combined with its 10V pk-pk output signal dynamic range offers compatibility with a wide class of input signals. A single external resistor enables gain adjustment from 1V/V to 10V/V providing the flexibility of applying model 284J in both high level transducer interfacing as well as low level sensor measurements.

Floating, Guarded Front-End: The input stage of model 284J can directly accept floating differential signals, such as ECG biomedical signals, or it may be configured as a high performance instrumentation front-end to accept signals having CMV with respect to input power common.

High Reliability: Model 284J is a conservatively designed, compact module, capable of reliable operation in harsh environments. Model 284J has a calculated MTBF of over 400,000 hours and is designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 284J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

SPECIFICATIONS (typical @ +25°C and V_S = +15V unless otherwise noted)

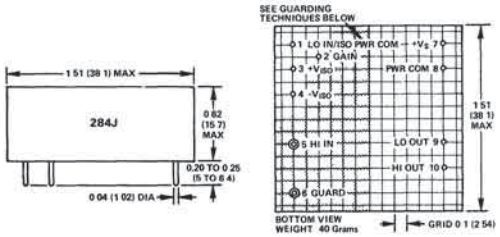
MODEL	284J
GAIN (NON-INVERTING)	
Range (50kΩ Load)	1 to 10V/V
Formula	Gain = $[1 + \frac{100k\Omega}{10\ 7k\Omega + R_1(k\Omega)}]$
Deviation from Formula	±3%
vs. Time	±0 001%/1000 Hours
vs Temperature (0 to +70°C)[1]	±0.0075%/°C
Nonlinearity, G = 1V/V to 10V/V[2]	±0.05%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±5V min
Max Safe Differential Input	
Continuous	$240V_{rms}$
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 6500V_{pk}$ max
Max CMV, Inputs to Outputs	
AC, 60Hz, 1 minute duration	$2500V_{rms}$
Pulse, 10ms duration, 1 pulse/10 sec	$\pm 2500V_{pk}$ max
With 510kΩ in series with Guard	$\pm 5000V_{pk}$ max
Continuous, ac or dc	$\pm 2500V_{pk}$ max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Power Common @ 115V ac, 60Hz	2.0μA rms max
INPUT IMPEDANCE	
Differential	$10^8\ \Omega \| 70pF$
Overload	300kΩ
Common Mode	$5x10^{10}\ \Omega \| 20pF$
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs. Temperature (0 to +70°C)	±0.1nA/°C
INPUT NOISE	
Voltage, G = 10V/V	
0.05Hz to 100Hz	8μV p-p
10Hz to 1kHz	10μV rms
Current	
0.05Hz to 100Hz	5pA p-p
FREQUENCY RESPONSE	
Small Signal, -3dB, G = 1V/V to 10V/V	1kHz
Slew Rate	25mV/μs
Full Power, 10V p-p Output	
Gain = 1V/V	700Hz
Gain = 10V/V	200Hz
Recovery Time, to ±100μV after Application of $\pm 6500V_{pk}$ Differential Input Pulse	200ms
OFFSET VOLTAGE REFERRED TO INPUT	
Initial, @ +25°C, Adjustable to Zero	±(5 + 20/G)mV
vs. Temperature (0 to +70°C)	±(15 + 150/G)μV/°C
vs Supply Voltage	±1mV/%
RATED OUTPUT	
Voltage, 50kΩ Load	±5V min
Output Impedance	1kΩ
Output Ripple, 1MHz Bandwidth	5mV pk-pk
ISOLATED POWER OUTPUTS	
Voltage, ±5mA Load	±8.5V dc
Accuracy	±5%
Current	±5mA min
Regulation, No Load to Full Load	+0, -15%
Ripple, 100kHz Bandwidth	100mV p-p
POWER SUPPLY, SINGLE POLARITY[3]	
Voltage, Rated Performance	+15V dc
Voltage Operating	+(8 to 15 5)V dc
Current, Quiescent	+10mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1 5" x 1 5" x 0 62"

[1] Gain temperature drift is specified as a percentage of output signal level
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span
[3] Recommended power supply, ADI model 904, ±15V @ 50mA output $41 (1–9)

Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



AC1049
SHIELDED MOUNTING SOCKET

INTERCONNECTION AND GUARDING TECHNIQUES

Model 284J can be applied directly to achieve rated performance as shown in Figure 1 below. To preserve the high CMR performance of model 284J, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 284J as illustrated in the outline drawing above (screened area). The GUARD (Pin 6) should be connected to this shield. This guard-shield is provided with the mounting socket, model AC1049. A recommended guarding technique using model AC1049 is illustrated in Figure 1. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to the signal low.

Offset Voltage Trim Adjust: The trim adjust circuit shown in Figure 1 can be used to zero the output offset voltage over the gain range from 1 to 10V/V. The output terminals, HI OUT and LO OUT, can be floated with respect to PWR COM up to $\pm 50V_{pk}$ max, offering three-port isolation. A 0.1μF capacitor is required from LO OUT to PWR COM whenever the output terminals are floated with respect to PWR COM. LO OUT can be connected directly to PWR COM when output offset trimming is not required.

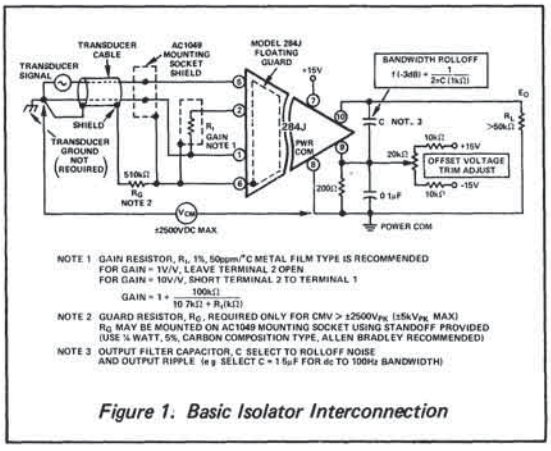


Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of model 284J is derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for model 284J is shown in Figure 2 below.

The 320kΩ input protection resistor limits the differential input current during periods of input amplifier saturation and also limits the differential fault current to approximately 35μA in case the preamplifier fails.

The bipolar input preamplifier operates single-ended (non-inverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 10V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating model 284J at a gain of 10V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry. Only the 20pF leakage capacitance between the floating guarded input section and the rest of the circuitry keeps the CMR from being infinite.

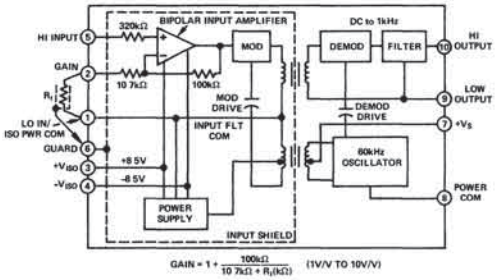


Figure 2. Block Diagram – Model 284J

INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kMΩ. Figure 3 illustrates the CMR ratings at 60Hz and 5kΩ source imbalance between signal input/output terminals, along with their respective capacitance.

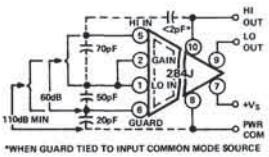


Figure 3. Model 284J Terminal Capacitance and CMR Ratings

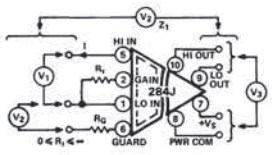


Figure 4. Model 284J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 4 and Table 1 illustrate model 284J's ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	±6500V_{PK} (10ms)	Withstand Voltage, Defibrillator
V1 (cont)	±240V_{RMS}	Withstand Voltage, Steady State
V2 (pulse)	±2500V_{PK} (10ms) R_G = 0	Transient
V2 (pulse)	±5000V_{PK} (10ms) R_G = 510kΩ	Isolation, Defibrillator
V2 (cont)	±2500V_{PK}	Isolation, Steady State
V3 (cont)	±50V_{PK}	Isolation, dc
Z1	50kMΩ‖20pF	Isolation Impedance
I	35μA rms	Input Fault Limit, DC to 60kHz

Table 1. Isolation Ratings Between Terminals

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.0μA rms at 115V ac, 60Hz (or 0.02μA/V ac). As shown in Figure 5, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current of about 5μA rms @ 60kHz. Line frequency leakage current levels are unaffected by the power on or off condition of model 284J.

For medical applications, model 284J is designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies. (e.g. model 284J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment – reference *Leakage Current*, paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, model 284J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

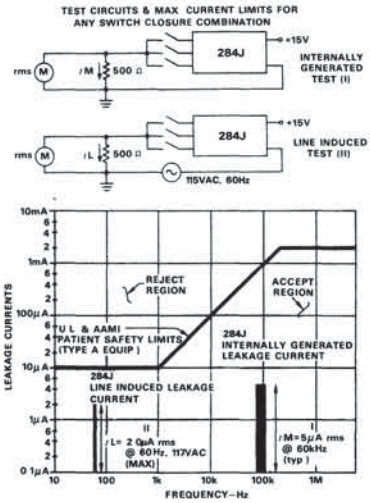


Figure 5. Model 284J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 5kΩ imbalance at a gain of 10V/V. Figure 6 illustrates CMR performance as a function of signal frequency. CMR approaches 146dB at dc with source imbalances as high as 5kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 6dB lower than at a gain of 10V/V.

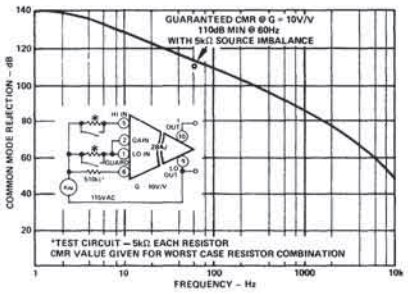


Figure 6. Common Mode Rejection vs. Frequency

Figure 7 illustrates the effect of source imbalance on CMR performance at 60Hz and Gain = 10V/V. CMR is typically 120dB at 60Hz and a balanced source. CMR is maintained greater than 80dB for source imbalances up to 100kΩ.

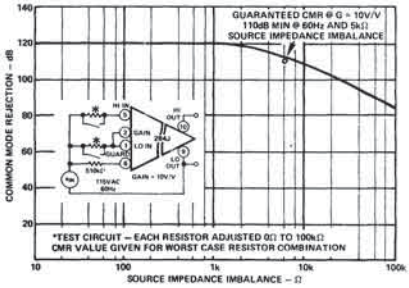


Figure 7. Common Mode Rejection vs. Source Impedance Imbalance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 8. RMS voltage noise is shown in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 10V/V. This value is derived by multiplying the rms value at f = 100Hz shown in Figure 8 (1.2μV rms) by 6.6.

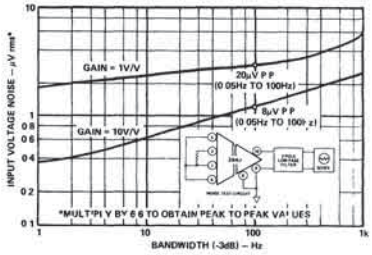


Figure 8. Input Voltage Noise vs. Bandwidth

For lowest noise performance, a low pass filter at the output should be used to selectively roll-off noise, output ripple and undesired signal frequencies beyond the bandwidth of interest (see note 3, Figure 1).

Input Offset Voltage Drift: Total input voltage drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 9 illustrates the total input voltage drift over the gain range of 1 to 10V/V.

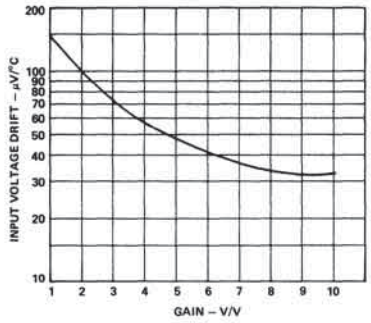
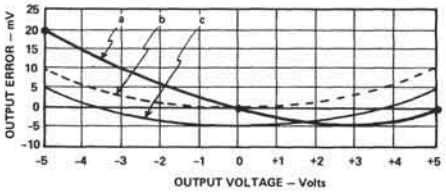


Figure 9. Input Offset Voltage Drift vs. Gain

Gain Nonlinearity: Linearity error is defined as the peak deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g. nonlinearity of model 284J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. In applying model 284J, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error over the operating output voltage span. A calibration technique illustrating how to minimize output error is shown below. In this example, model 284J is operating over an output span of +5V to -5V and a gain of 5V/V.



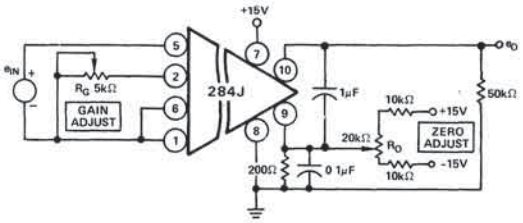


Figure 10. Gain and Offset Adjustment

GROUNDING PRACTICES

The more common sources of electrical noise arise from ground loops, electrostatic coupling and electromagnetic pickup. The guidelines listed below pertain to guarding low level, millivolt signals in hostile environments such as current shunt signals in "heavy industrial" plants.

Guidelines:

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 11 below. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 78dB CMR capability of model 284J between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- To avoid ground loops and excessive hum, signal low, B, or the transducer cable shield, S, should never be grounded at more than one point.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

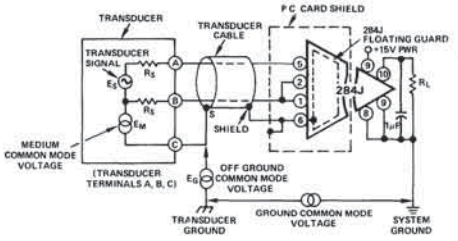


Figure 11. Transducer- Amplifier Interconnection

Isolated Power and Output Voltage Swing: Model 284J offers a floating power supply providing ±8.5V dc outputs with ±5mA output current rating. As shown in Figure 12, the minimum voltage output for $\pm V_{ISO}$, as well as the maximum load capability, is dependent on the input power supply, $+V_S$. Figure 12 also illustrates the typical output voltage range as both input supply, $+V_S$, and the isolated supply loads, $\pm I_L$, are varied. At ±5mA isolated load and V_S = +15V dc, model 284J can provide an output voltage swing of ±7.5V.

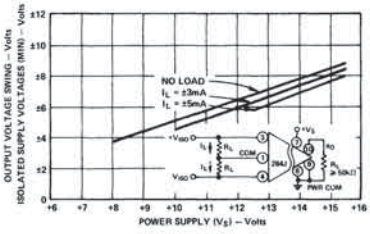


Figure 12. Isolated Power ($\pm V_{ISO}$) and Output Voltage Swing ($\pm E_O$) Versus Power Supply Input (V_S)

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, model 284J can be applied to measure and control off-ground millivolt signals in the presence of ±2500V dc CMV signals. In interface applications such as pH control systems of on-line process measurement systems such as pollution monitoring, model 284J offers complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of this model.

Figure 13 illustrates how model 284J can be combined with a low drift, 1μV/°C max, front-end amplifier, model AD517K, to interface low level transducer signals. Model 284J's isolated ±8.5V dc power and front-end guard eliminate ground loops and preserve high CMR (114dB @ 60Hz).

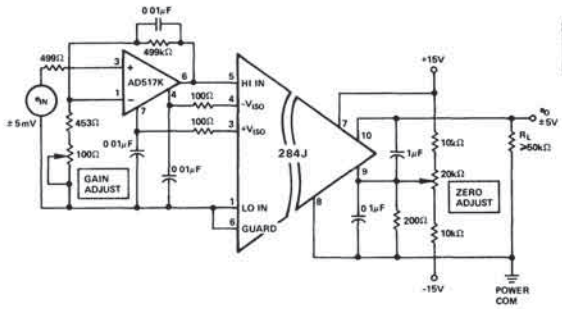


Figure 13. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Instrumentation Amplifier: Model 284J provides a floating guarded input stage capable of directly accepting isolated differential signals. The non-inverting, single-ended input stage offers simple two wire interconnection with floating input signals.

In applications where the isolated power is applied to transducers such as bridges which generate differential input signals with common mode voltages measured with respect to the isolated power common, model 284J can be connected as shown in Figure 14. To achieve high CMR with respect to the ISO PWR COM, the following trim procedure is recommended.

CMR Trim Procedure

1) Connect a 1V pk-pk oscillator between the +IN/-IN and IN COM terminals as shown in Figure 14.
2) Set the input frequency at 0.5Hz and adjust R1 for minimum e_O.
3) Set the input frequency at 60Hz and adjust R2 for minimum e_O.
4) Repeat steps 2 and 3 for best CMR performance.

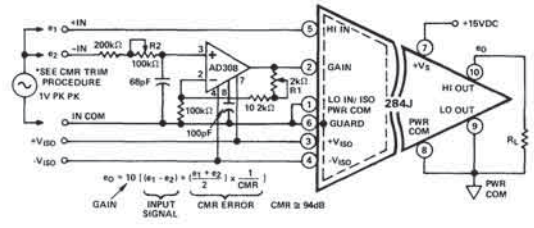


Figure 14. Application of 284J as Instrumentation Amplifier

APPLICATIONS IN BIOMEDICAL DESIGNS

Cardiac Monitoring: Heart signals can be masked by muscle noise, electrochemical noise, residual electrode voltages and 60Hz power line pickup. To achieve high performance in cardiac monitoring, model 284J's design provides high CMR in the dc to 100Hz bandwidth and substantial source impedance — to 5kΩ. An especially demanding ECG requirement is that of fetal heart monitoring as illustrated in Figure 15. The low input noise of model 284J and the dual CMR ratings are exploited in this application to extract the fetal ECG signals. The separation between the mother's and the fetal heartbeat is enhanced by the 78dB of CMR between the input electrodes and guard, while the 110dB of CMR from input to output ground screens out 60Hz pickup and other external interference.

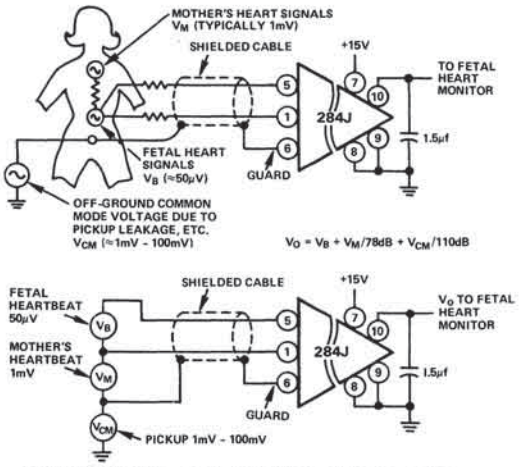


Figure 15. Fetal Heartbeat Monitoring

Single Lead ECG Recorder with Leads Off Indicator: In single lead applications model 284J offers simple two-wire hook-up to the ECG signal as illustrated in Figure 16. The floating signal can be connected directly to the HI IN and LO IN terminals using the GUARD tied to the patients' right leg for best CMR performance. Using the isolated power from model 284J an inexpensive calibration signal is easily provided. In ECG applications, model 284J provides a simple means to determine whenever a "Leads-Off" condition exists at the input. A "Leads-Off" condition ($R_S = \infty$) will cause the HI OUT terminal to be at a negative output saturation level; i.e. e_O = -8.5V to -9.5V @ V_S = +15V.

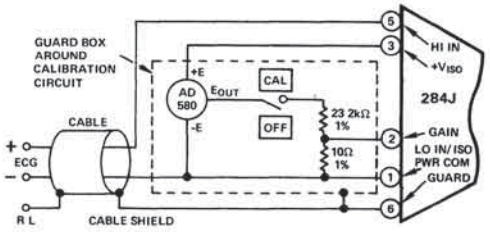


Figure 16. Single Lead ECG Recorder with 1mV Calibration Circuit and Leads Off Indicator

Multi-Lead ECG Recorder with Right Leg Drive: The small size, economy and isolated power makes model 284J an ideal isolation amplifier for application in clinical ECG recorders. Figure 17 illustrates how this new isolator can be applied in a high performance, portable multi-lead ECG recorder. In this application, model 284J's input is configured as an instrumentation amplifier with high CMR to the floating input common. The right leg drive offers improved CMR between input and isolated common by driving to zero any CMV existing between these points. The isolated power, $\pm V_{ISO}$, is used to drive the lead buffer amplifiers and the front-end, 1mV calibration signal.

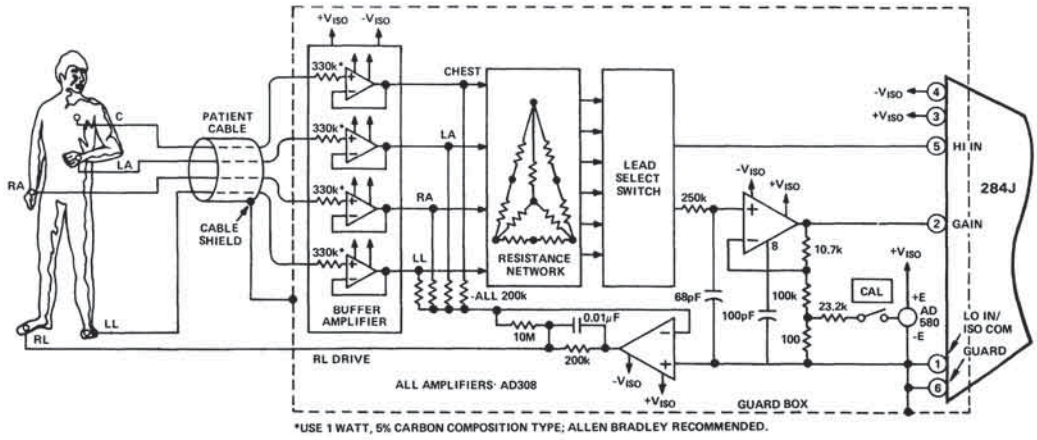


Figure 17. Multi-Lead ECG Recorder Application Using Model 284J with Right Leg Drive Output

High CMV, High Performance, Synchronized Isolation Amplifiers

Models 286J, 281

FEATURES

Low Cost
Single or Multi-Channel Capability Using External Oscillator
Isolated Power Supply: ±15V dc @ ±15mA
Low Nonlinearity: 0.05% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.0075%/°C
Small Size: 1.5″ x 1.5″ x 0.62″
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 2500V dc Continuous
Wide Gain Range: 1 to 100V/V

APPLICATIONS

Ground Loop Elimination in Industrial and Process Control
High Voltage Protection in Data Acquisition Systems
Biomedical and Patient Monitoring Instrumentation
Off-Ground Signal Measurements

GENERAL DESCRIPTION

Model 286J is a low cost, compact, isolation amplifier that is optimized for single or multi-channel use in data acquisition systems for industrial and medical applications. A single external synchronizing oscillator can drive from 1 to 16 model 286J's, or a virtually limitless number of model 286's can be configured using multiple ganged oscillators. The oscillator drive circuit can be supplied by the user of specified in a compact, low cost, epoxy encapsulated module, model 281, which also includes a voltage regulator for operation over a wide single voltage range of +8V to +28V.

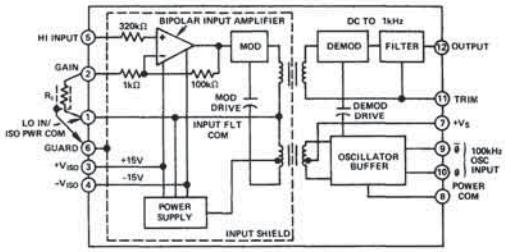
In addition to providing multi-channel operation, this new design features adjustable gain, 1 to 100V/V, dual isolated power, ±15V dc @ ±15mA, ±2500V dc off ground isolation (CMV) and 110dB minimum CMR at 60Hz, 5kΩ source imbalance, in a compact 1.5″ x 1.5″ x 0.6″ epoxy encapsulated package. Model 286J achieves a low input noise of 8μV pk-pk (100Hz bandwidth, G = 100V/V), nonlinearity of ±0.05% @ 10V pk-pk output, and an input/output dynamic range of 20V pk-pk.

Using modulation techniques with reliable transformer isolation, model 286J will interrupt ground loops, leakage paths, and high voltage transients to ±5kV pk (10ms pulse), providing dc to 1kHz (–3dB) response.

WHERE TO USE MODEL 286J

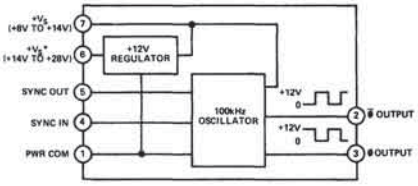
Industrial Applications: In multi-channel data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, model 286J offers complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded with model 286J's 20V pk-pk input signal range at a gain of 1V/V operation. In portable multi-channel designs, model 286J's single supply, wide range operation (+8V to +16V) offers simple battery operation.

MODEL 286J FUNCTIONAL BLOCK DIAGRAM



$$\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_1\,(k\Omega)} \quad (1\text{V/V TO } 100\text{V/V})$$

MODEL 281 FUNCTIONAL BLOCK DIAGRAM



*LEAVE TERMINAL 6 OPEN, WHEN POWER IS APPLIED TO TERMINAL 7

Medical Applications: In biomedical and patient monitoring equipment such as multi-channel VCG, ECG, and polygraph recorders, model 286J offers protection from lethal ground fault currents as well as 5kV defibrillator pulse inputs. Low level bioelectric signal recording is achieved with model 286J's low input noise (8μV pk-pk @ G = 100V/V) and high CMR (110dB, min @ 60Hz).

DESIGN FEATURES AND USER BENEFITS

High Reliability: Model 286J is a conservatively designed, compact module, capable of reliable operation in harsh environments. Model 286J has a calculated MTBF of 392,125 hours and is designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability). As an additional assurance of reliability, every model 286J is factory tested for CMV and input ratings by application of 5kV pk, 10ms pulses, between input terminals as well as input/output terminals.

Isolated Power Supply: Dual ±15V dc @ ±15mA, completely isolated from the input power terminals (±2500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers as well as remote transducers such as thermistors or bridges.

Adjustable Gain: A single external resistor enables gain adjustment from 1V/V to 100V/V providing the flexibility of applying model 286J in both high-level transducer interfacing as well as low-level sensor measurements.

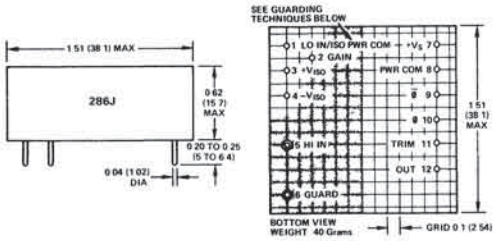
SPECIFICATIONS

MODEL	286J*
GAIN (NONINVERTING)	
Range (50kΩ Load)	1 to 100V/V
Formula	Gain = 1+ [100kΩ/(1kΩ+R_1(kΩ))]
Deviation from Formula	±4%
vs. Temperature (0 to +70°C)[1]	±0.0075%/°C
vs. Time	±0.001%/1000 hours
Nonlinearity,[2] ±5V Output (G = 1 to 100V/V)	±0.05%
Nonlinearity,[2] ±10V Output (G = 1 to 100V/V)	±0.2%
INPUT VOLTAGE RATINGS	
Linear Differential Range, G = 1V/V	±10V min
Max Safe Differntial Input	
Continuous	240V rms
Pulse, 10ms Duration, 1 Pulse/10sec	±6500V pk max
Max CMV, Inputs to Outputs	
ac, 60Hz, 1 Minute Duration	2500V rms
Pulse, 10ms Duration, 1 Pulse/10sec	±2500V pk max
With 510kΩ in series with Guard	±5000V pk max
Continuous, ac or dc	±2500V pk max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 5k\Omega$	
Balanced Source Impedance	114dB
5kΩ Source Impedance Imbalance	110dB min
CMR, Inputs to Guard, 60Hz	
1kΩ Source Impedance Imbalance	78dB
Max Leakage Current, Inputs to Power Common	
@ 115V ac 60Hz	2.5μA rms max
OFFSET VOLTAGE, REFERRED TO INPUT	
Initial, @ +25°C (Adjustable to zero)	±(5 + 45/G) mV
vs. Temperature (0 to +70°C)	
At Gain = 100V/V	±10μV/°C
At Other Gains (1 to 100V/V)	±(7 + 250/G)μV/°C
vs. Supply Voltage	±1mV/%
INPUT IMPEDANCE	
Differential	$10^8\Omega$‖150pF
Overload	300kΩ
Common Mode	$5 \times 10^{10}\Omega$‖20pF
INPUT DIFFERENCE CURRENT	
Initial, @ +25°C	±7nA max
vs Temperature (0 to +70°C)	±0.1nA/°C
INPUT NOISE (Gain = 100V/V)	
Voltage	
0.05Hz to 100Hz	8μV pk-pk
10Hz to 1kHz	3.0μV rms
Current	
0.05Hz to 100Hz	5pA pk-pk
FREQUENCY RESPONSE (Gain 1V/V to 100V/V)	
Small Signal Bandwidth, -3dB	1.0kHz
Slew Rate	25mV/μs
Full Power, 10V pk-pk Output	900Hz
Full Power, 20V pk-pk Output	400Hz
Recovery Time, to ±100μV	200ms
RATED OUTPUT	
Voltage, 50kΩ Load	±10V min
Output Impedance	1kΩ
Output Ripple, 1mHz Bandwidth	20mV pk-pk
OSCILLATOR DRIVE INPUT*	
Input Voltage	(8 to 16)V pk-pk
Input Frequency	100kHz ±5%, max
ISOLATED POWER SUPPLY	
Voltage	±15V dc
Accuracy	0, -6%
Current	±15mA min
Regulation, No Load to Full Load	+0, -10%
Ripple, 100kHz Bandwidth	200mV pk-pk
POWER SUPPLY, SINGLE POLARITY[3]	
Voltage, Rated Performance	+15V dc
Voltage, Operating	+(8V dc to 16V dc)
Current, Quiescent	+13mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
CASE DIMENSIONS	1.5" x 1.5" x 0.62"

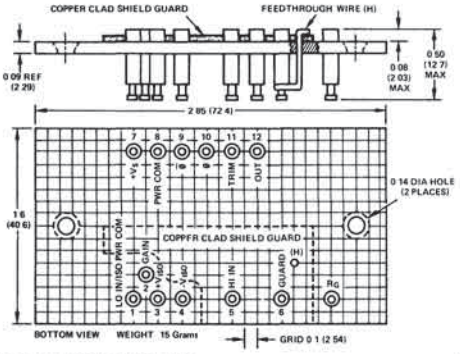
[1] Gain temperature drift is specified as a percentage of output signal level
[2] Gain nonlinearity is specified as a percentage of output signal span.
[3] Recommended power supply, ADI model 904, ±15V @ ±50mA output.
*Specifications are for model 286J when driven by ADI model 281 oscillator circuit (see Figure 12)
Specifications subject to change without notice

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SHIELDED MOUNTING SOCKET AC1054



GUARDING TECHNIQUES

To preserve the high CMR performance of model 286, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 286 as illustrated in the outline drawing above (screened area). The GUARD (pin 6) must be connected to this shield. This shield is provided with the mounting socket, model AC1054 (solder feedthrough wire to the socket guard pin and copper foil surface.) A recommended guarding technique using model AC1054 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable to reduce inductive and capacitive pickup. To reduce effective cable capacitance, cable shield should be connected to the common mode signal source by connecting the shield as close as possible to signal low as shown in Figure 1.

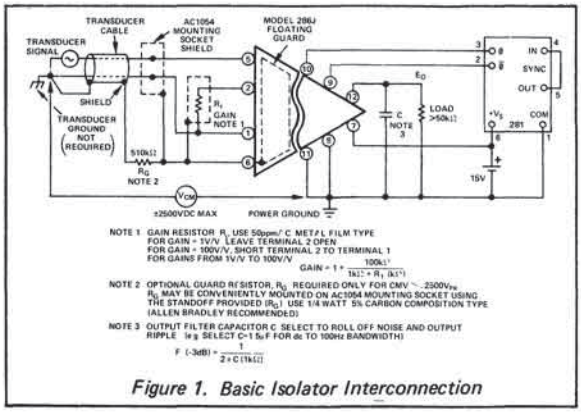


Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of model 286J is derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for model 286J is shown in Figure 2 below.

The 320kΩ input protection resistor limits the differential input current during periods of input amplifier saturation and also limits the differential fault current to approximately 50μA in case the preamplifier fails.

The bipolar input preamplifier operates single-ended (non-inverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 100V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating model 286J at a gain of 100V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry.

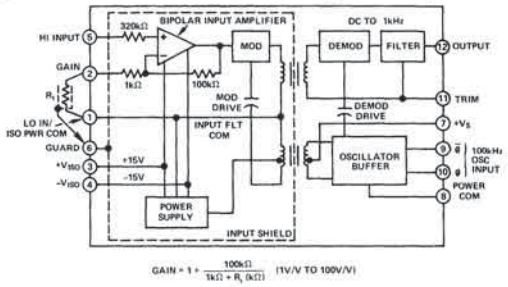


Figure 2. Block Diagram – Model 286J

OPTIONAL TRIM ADJUSTMENTS

Model 286J can be applied directly to achieve rated performance as shown in Figure 1, on previous page. Additional trim adjustment capability for bandwidth, output offset voltage and gain (for gains greater than 100V/V) is easily provided as shown in Figure 3 (below). The OUT and TRIM terminals can be floated with respect to PWR COM up to ±50V pk, max offering three-port isolation.

The TRIM terminal (pin 11) must be connected to the PWR COM terminal (pin 8) when not used to adjust the output offset voltage. A 0.1μF capacitor from pin 11 to PWR COM is recommended whenever the TRIM terminal is used.

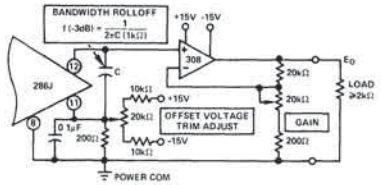


Figure 3. Optional Connections: Offset Voltage Trim Adjust, Bandwidth (-3dB) Rolloff and Gain Adjust (G>100V/V)

INTERELECTRODE CAPACITANCE, TERMINAL RATINGS AND LEAKAGE CURRENTS LIMITS

Capacitance: Interelectrode terminal capacitance arising from stray coupling capacitance effects between the input terminals and the signal output terminals are each shunted by leakage resistance values exceeding 50kMΩ. Figure 4 illustrates the CMR ratings at 60Hz and 5kΩ source imbalance between signal input/output terminals, along with their respective capacitance.

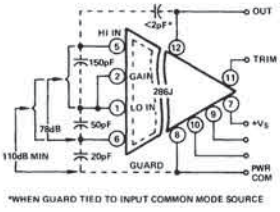


Figure 4. Model 286J Terminal Capacitance and CMR Ratings

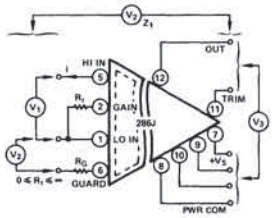


Figure 5. Model 286J Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac or dc peak ratings. Pulse ratings are intended to support defibrillator and other transient voltages. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 5 and Table 1 illustrate model 286J ratings between terminals.

SYMBOL	RATING	REMARKS
V1 (pulse)	±6500V_{PK} (10ms)	Withstand Voltage, Defibrillator
V1 (cont.)	±240V_{RMS}	Withstand Voltage, Steady State
V2 (pulse)	±2500V_{PK} (10ms) R_G = 0	Transient
V2 (pulse)	±5000V_{PK} (10ms) R_G = 510kΩ	Isolation, Defibrillator
V2 (cont.)	±2500V_{PK}	Isolation, Steady State
V3 (cont.)	±50V_{PK}	Isolation, dc
Z1	50kMΩ‖20pF	Isolation Impedance
I	50μA rms	Input Fault Limit, dc to 200kHz

Table 1. Isolation Ratings Between Terminals

Leakage Current Limits: The low coupling capacitance between inputs and output yields a ground leakage current of less than 2.5μA rms at 115V ac, 60Hz (or 0.02μA/V ac). As shown in Figure 6, the transformer coupled modulator signal, through stray coupling, also creates an internally generated leakage current of about 5μA rms @ 100kHz. Line frequency leakage current levels are unaffected by the power on or off condition of model 286J.

For medical applications, model 286J is designed to improve on patient safety current limits proposed by F.D.A., U.L., A.A.M.I. and other regulatory agencies (e.g., model 286J complies with leakage requirements for the Underwriters Laboratory STANDARD FOR SAFETY, MEDICAL AND DENTAL EQUIPMENT as established under UL544 for type A and B patient connected equipment – reference *Leakage Current*, paragraph 27.5).

In patient monitoring equipment, such as ECG recorders, model 286J will provide adequate isolation without exposing the patient to potentially lethal microshock hazards. Using passive components for input protection, this design limits input fault currents even under amplifier failure conditions.

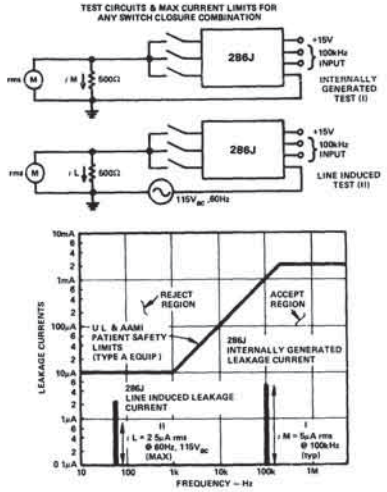


Figure 6. Model 286J Leakage Current Performance from Line Induced and Internally Generated (Modulator) Operating Conditions

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 5kΩ imbalance at a gain of 100V/V. Figure 7 illustrates CMR performance as a function of signal frequency. CMR approaches 156dB at dc with source imbalances as high as 5kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V CMR is typically 6dB lower than at gain of 100V/V.

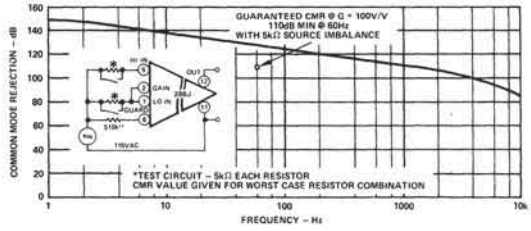


Figure 7. Common Mode Rejection vs. Frequency

Figure 8 illustrates the effect of source imbalance on CMR performance at 60Hz at gains of 1V/V, 10V/V, and 100V/V. CMR is typically 140dB at 60Hz and a balanced source. CMR is maintained greater than 80dB for source imbalances up to 100kΩ.

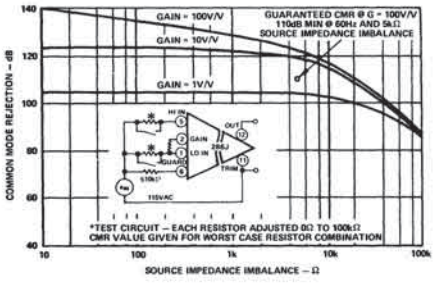


Figure 8. Common Mode Rejection vs. Source Impedance Imbalance

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g., nonlinearity of model 286J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. Figure 9 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V).

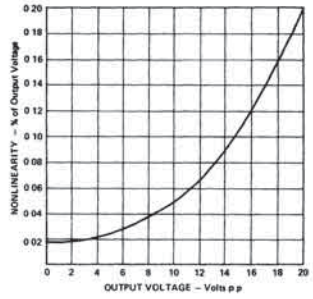


Figure 9. Gain Nonlinearity vs. Output Voltage

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 10. RMS voltage noise is shown in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 100V/V. This value is derived by multiplying the rms value at f = 100Hz shown in Figure 10 (1.2μV rms) by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest (see note 3, Figure 1). Increasing gain will also reduce the input noise.

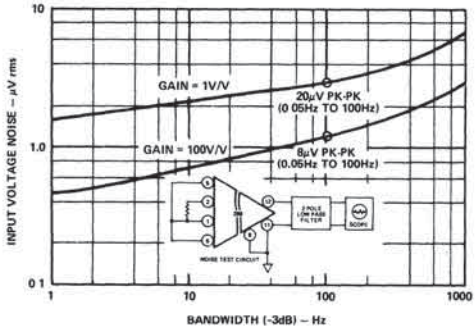


Figure 10. Input Voltage Noise vs. Bandwidth

Input Offset Voltage Drift: Total input drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 11 illustrates total input drift over the gain range of 1 to 100V/V.

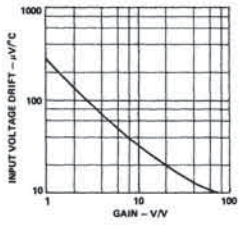


Figure 11. Input Offset Voltage Drift vs. Gain

REFERENCE EXCITATION OSCILLATOR

When applying model 286J, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 12, or purchasing a module from Analog Devices – model 281.

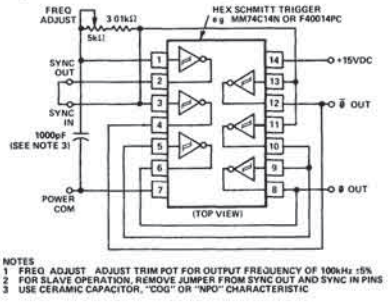


Figure 12. Model 281 100kHz Oscillator – Logic and Interconnection Diagram

The block diagram of model 281 is shown in Figure 13. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.

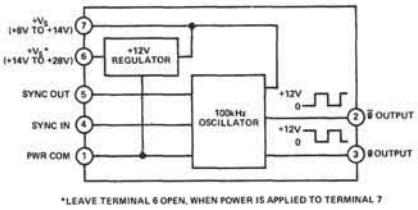


Figure 13. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 286J's as shown in Figure 14. An additional model 281 may be driven in a slave-mode, as shown in Figure 15, to expand the total system channels from 16 to 32. By adding additional model 281's in this manner, systems of over 1000 channels may be easily configured.

EXTERNAL OSCILLATOR INTERCONNECTION

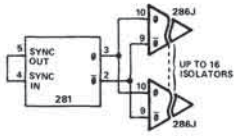


Figure 14. Model 281/286 Connection for Driving from 1 to 16 Isolators

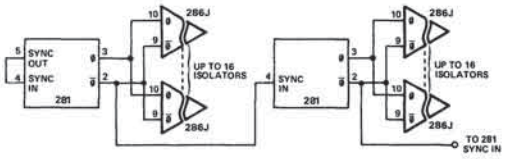


Figure 15. Model 281/286 Connection for Driving > 16 Isolators

SPECIFICATIONS

(typical @ +25° C and V_S = +15V dc unless otherwise noted)

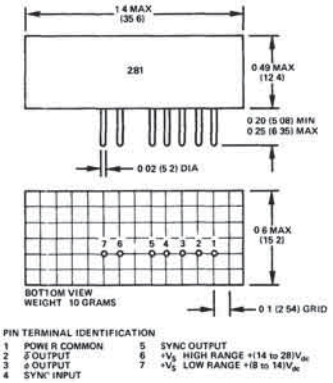
MODEL	281
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage (ϕ and $\bar{\phi}$ terminals)	0 to +12V pk
Fan-Out[1,2]	16 max
POWER SUPPLY RANGE[3]	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N L	+5mA
F L	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N L	+12mA
F L	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C
MECHANICAL	
Case Size	1 4" x 0 6" x 0 49"
Weight	10 grams

[1] Model 286J oscillator drive input represents unity oscillator load
[2] For applications requiring more than 16 286J's, additional 281's may be used in a master/slave mode Refer to Figure 15
[3] Full load consists of 16 model 286J's and 281 oscillator slave
Specifications subject to change without notice

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

MODEL 281



PIN TERMINAL IDENTIFICATION

1	POWER COMMON	5	SYNC OUTPUT
2	ϕ OUTPUT	6	$+V_S$ HIGH RANGE +(14 to 28)V_{dc}
3	ϕ̄ OUTPUT	7	$+V_S$ LOW RANGE +(8 to 14)V_{dc}
4	SYNC INPUT		

MATING SOCKET: CINCH #16 DIP OR EQUIVALENT

GUIDELINES ON EFFECTIVE SHIELDING & GROUNDING PRACTICES

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 16. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 78dB CMR capability of model 286J between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

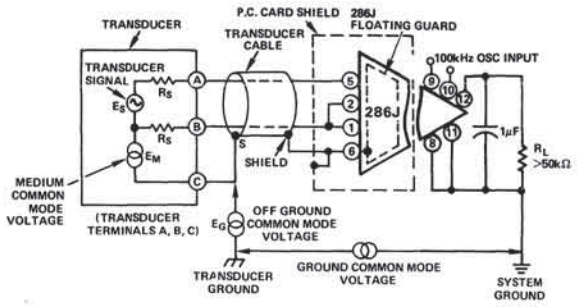
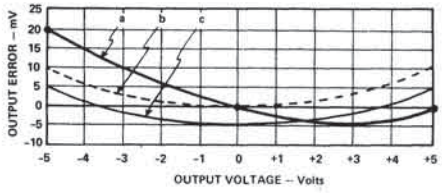


Figure 16. Transducer – Amplifier Interface

GAIN AND OFFSET TRIM PROCEDURE

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to −5V and operation at Gain = 10V/V is desired.

1. Apply e_{IN} = 0 volts and adjust R_O for e_O = 0 volts.
2. Apply e_{IN} = +0.500V dc and adjust R_G for e_O = +5.000V dc.
3. Apply e_{IN} = −0.500V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply +0.500V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).



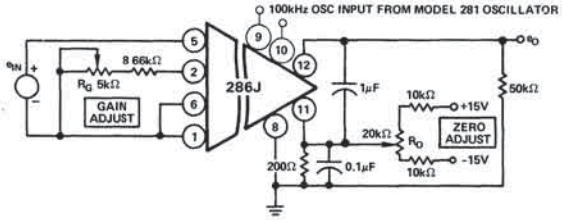


Figure 17. Gain and Offset Adjustment

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, model 286J can be applied to measure and control off-ground millivolt signals in the presence of ±2500V dc CMV signals. In interface applications such as pH control systems or on-line process measurement systems such as pollution monitoring, model 286J offers complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of this model.

Figure 18 illustrates how model 286J can be combined with a low drift, 1µV/°C max, front-end amplifier, model AD510K, to interface low level transducer signals. Model 286J's isolated ±15V dc power and front-end guard eliminate ground loops and preserve high CMR (110dB min @ 60Hz).

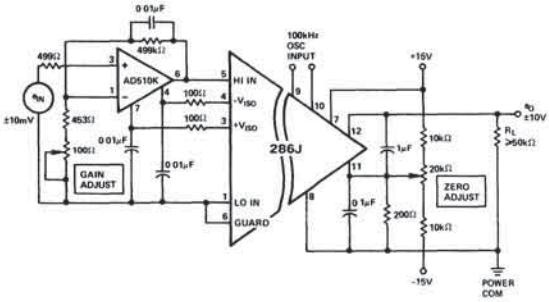


Figure 18. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Current Loop Receiver: Model 286J can be applied to measurement of analog quantities transmitted via 4-20mA current loops over substantial distances through harsh environments. Figure 19 shows an application of model 286J as a current loop receiver. A 25Ω resistor converts the 4–20mA current input from a remote loop to a 100–500mV differential voltage input, which the 286J amplifies, isolates, and translates to a 0 to +5V output level at local system ground.

Among the most-helpful characteristics of the 286J in this kind of measurement are the high common-mode rejection (110dB minimum at 60Hz with 5kΩ source unbalance) and the high common-mode rating (±2500 volts dc). The former means low noise pickup; the latter means excellent isolation and protection against large transients. The high common-mode rejection, permitting relatively low input voltage to be used (0.4V span, in this case), permits the use of a low current-metering resistance, which in turn results in low compliance-voltage loading on the current loop, and therefore permits insertion into existing loops without encountering overrange problems. The gain of 12.5 provides a substantial output span, and the floating output permits biasing to a 0 to 5V range.

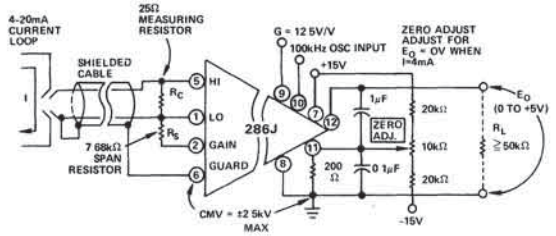


Figure 19. Isolated Analog Interface; 4 to 20mA is Converted to 0 to +5V at the Output, with Up to ±2500V of Isolation

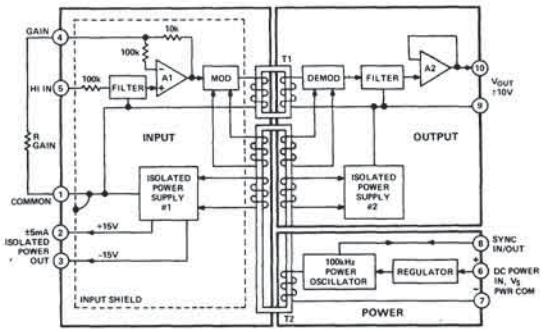
Precision, Wide Bandwidth, Synchronized Isolation Amplifier

Model 289

FEATURES
- Low Nonlinearity: ±0.012% max (289L)
- Frequency Response: (-3dB) dc to 20kHz
  (Full Power) dc to 5kHz
- Gain Adjustable 1 to 100V/V, Single Resistor
- 3-Port Isolation: ±2500V CMV Isolation Input/Output
- Low Gain Drift: ±0.005%/°C max
- Floating Power Output: ±15V @ ±5mA
- 120dB CMR at 60Hz: Fully Shielded Input Stage
- Meets UL Std. 544 Leakage: 2μA rms max, @ 115V ac, 60Hz

APPLICATIONS
- Multi-Channel Data Acquisition Systems
- Current Shunt Measurements
- Process Signal Isolator
- High Voltage Instrumentation Amplifier
- SCR Motor Control

MODEL 289 FUNCTIONAL BLOCK DIAGRAM



5

GENERAL DESCRIPTION

Model 289 is a wideband, accurate, low cost isolation amplifier designed for instrumentation and industrial applications. Three accuracy selections are available offering guaranteed gain nonlinearity error at 10V p-p output: ±0.012% max (289L), ±0.025% max (289K), ±0.05% max (289J). All versions of the 289 provide a small signal frequency response from dc to 20kHz (-3dB) and a large signal response from dc to 5kHz (full power) at a gain of 1V/V. This new design offers true 3-port isolation, ±2500V dc between inputs and outputs (or power inputs), as well as 240V rms between power supply inputs and signal outputs. Using carrier modulation techniques with transformer isolation, model 289 interrupts ground loops and leakage paths and minimizes the effect of high voltage transients. It provides 120dB Common Mode Rejection between input and output common. The high CMV and CMR ratings of the model 289 facilitate accurate measurements in the presence of noisy electrical equipment such as motors and relays.

WHERE TO USE THE MODEL 289

The model 289 is designed to interface single and multichannel data acquisition systems with dc sensors such as thermocouples, strain gauges and other low level signals in harsh industrial environments. Providing high accuracy with complete galvanic isolation, and protection from line transients of fault voltages, model 289's performance is suitable for applications such as process controllers, current loop receivers, weighing systems, high CMV instrumentation and computer interface systems.

Use the model 289 when data must be acquired from floating transducers in computerized process control systems. The photograph above shows a typical multichannel application allowing potential differences or interrupting ground loops, among transducers, or between transducers and local ground.

DESIGN FEATURES AND USER BENEFITS

Isolated Power: The floating power supply section provides isolated ±15V outputs @ ±5mA. Isolated power is regulated to within ±5%. This feature permits model 289 to excite floating signal conditioners, front-end buffer amplifiers and remote transducers such as thermistors or bridges, eliminating the need for a separate isolated dc/dc converter.

Adjustable Gain: A single external resistor adjusts the model 289's gain from 1V/V to 100V/V for applications in high and low level transducer interfacing.

Synchronized: The model 289 provides a synchronization terminal for use in multichannel applications. Connecting the synchronization terminals of model 289s synchronizes their internal oscillators, thereby eliminating the problem of oscillator "beat frequency" interference that sometimes occurs when isolation amplifiers are closely mounted.

Internal Voltage Regulator: Improves power supply rejection and helps prevent carrier oscillator spikes from being broadcast via the isolator power terminal to the rest of the system.

Buffered Output: Prevents gain errors when an isolation amplifier is followed by a resistive load of low impedance. Model 289 can drive a 2kΩ load.

Three-Port Isolation: Provides true galvanic isolation between input, output and power supply ports. Eliminates need for power supply and output ports being returned through a common terminal.

Reliability: Model 289 is conservatively designed to be capable of reliable operation in harsh environments. Model 289 has a calculated MTBF of 271,835 hours. In addition, the model 289 meets UL Std. 544 leakage, 2μA rms @ 115V ac, 60Hz.

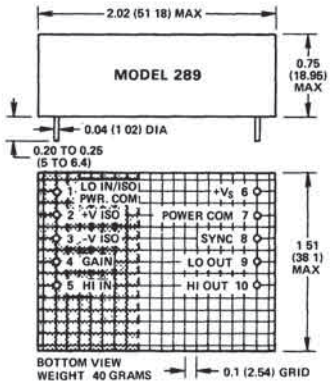
SPECIFICATIONS (typical @ +25°C and V_S = ±14.4V to +25V dc unless otherwise noted)

Model	289J	289K	289L
GAIN (NONINVERTING)			
Range		1 to 100V/V	
Formula		$G = 1 + \frac{10k\Omega}{R_G\,(k\Omega)}$	
Deviation from Formula		±1.5% max	
vs Temperature (0 to +70°C)[1]		15ppm/°C typ (50ppm/°C max)	
Nonlinearity, (±5V Swing)[2,3]	±0.05% max	±0.025% max	±0.012% max
INPUT VOLTAGE RATINGS			
Linear Differential Range (G = 1V/V)		±10V min	
Max Safe Differential Input			
Continuous		120V rms	
1 Minute		240V rms	
Max CMV (Inputs to Outputs)			
Continuous ac or dc		±2500V peak max	
ac, 60Hz, 1 Minute Duration		2500V rms	
CMR, Inputs to Outputs 60Hz			
$R_S \leq 1k\Omega$, Balanced Source Impedance		120dB	
$R_S \leq 1k\Omega$, HI IN Lead Only		104dB min	
Max Leakage Current, Input to Output @			
115V rms, 60Hz ac		2μA rms max	
INPUT IMPEDANCE			
Differential		$33pF \| 10^8\,\Omega$	
Overload		100kΩ	
Common Mode		$20pF \| 5 \times 10^{10}\,\Omega$	
INPUT DIFFERENCE CURRENT			
Initial @ +25°C		10nA (75nA max)	
vs. Temperature (0 to 70°C)		0.15nA/°C	
INPUT NOISE (GAIN = 100V/V)			
Voltage			
0.05Hz to 100Hz		8μV p-p	
10Hz to 1kHz		3μV rms	
Current			
0.05Hz to 100Hz		3pA rms	
FREQUENCY RESPONSE			
Small Signal -3dB			
G = 1V/V		20kHz	
G = 100V/V		5kHz	
Full Power, 10V p-p Output			
G = 1V/V		5kHz	
G = 100V/V		3.5kHz	
Full Power, 20V p-p Output			
G = 1V/V		2.3kHz	
G = 100V/V		2.3kHz	
Slew Rate		0.14V/μs	
Settling Time[4] ±0.05%, ±10V Step		400μs	
OFFSET VOLTAGE, REFERRED TO INPUT			
Initial, @ +25°C		$\pm 5 \pm \frac{10}{G}$ mV max	
vs Temperature (0 to +70°C)	$\pm 20 \pm \frac{200}{G}$ max	$\pm 15 \pm \frac{100}{G}$ max	$\pm 10 \pm \frac{50}{G}$ μV/°C max
vs Supply Voltage (+15V to +20V change)		$\pm 2 \pm \frac{10}{G}$ μV/V	
RATED OUTPUT			
Voltage, 2kΩ Load		±10V min	
Output Impedance		<1Ω(dc to 100Hz)	
Output Ripple, 0.1MHz Bandwidth			
No Signal IN		5mV p-p	
$+10V_{IN}$		50mV p-p	
ISOLATED POWER SUPPLY			
Voltage		±15V dc	
Accuracy		±10%	
Current		±5mA, min	
Regulation No Load to Full Load		±5%	
Ripple, 0.1MHz Bandwidth, No Load		25mV p-p	
Full Load		75mV p-p	
POWER SUPPLY, SINGLE POLARITY[5]			
Voltage, Rated Performance		+14.4V to +25V	
Voltage, Operating		+8.5V to +25V	
Current, Quiescent (@ V_S = +15V)		+25mA	
TEMPERATURE RANGE			
Rated Performance		0 to +70°C	
Operating		-15°C to +75°C	
Storage		-55°C to +85°C	
CASE DIMENSIONS		1.5" X 2.0" X 0.75"	

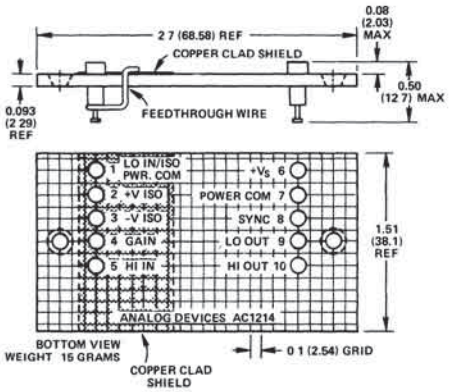
NOTES
[1] Gain temperature drift is specified as a percentage of output signal level
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] When isolated power output is used, nonlinearity increases by ±0.002%/mA of current drawn.
[4] G = 1V/V, with 2-pole, 5kHz output filter (see Figure 13).
[5] Recommended power supply, ADI model 904, ±15V @ 50mA output.
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SHIELDED MATING SOCKET AC1214



INTERCONNECTIONS AND SHIELDING TECHNIQUE

To preserve the high CMR performance of model 289, care must be taken to keep the capacitance balanced about the input terminals. A shield should be provided on the printed circuit board under model 289 as illustrated in the outline drawing above (screened area). The LO IN/ISO PWR COM (pin 1) must be connected to this shield. This shield is provided with the mounting socket, model AC1214 (solder feedthrough wire to the socket pin 1 and copper foil surface). A recommended shielding technique using model AC1214 is illustrated in Figure 1.

Best CMR performance will be achieved by using twisted, shielded cable for the input signal to reduce inductive and capacitive pickup. To further reduce effective cable capacitance, the cable shield should be connected to the common mode signal source as close to signal low as possible (see Figure 1).

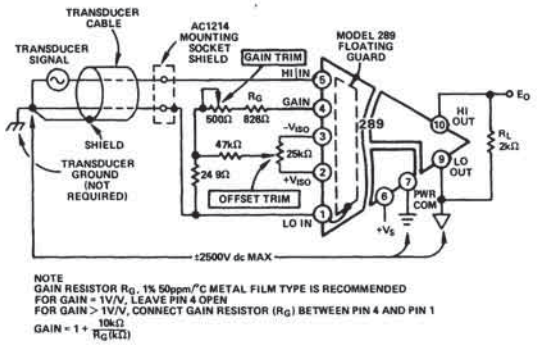


Figure 1. Basic Isolator Interconnection

THEORY OF OPERATION

The remarkable performance of the model 289 is derived from the carrier isolation technique used to transfer both signal and power between the amplifier's input stage and the rest of the circuitry. A block diagram is shown in Figure 2.

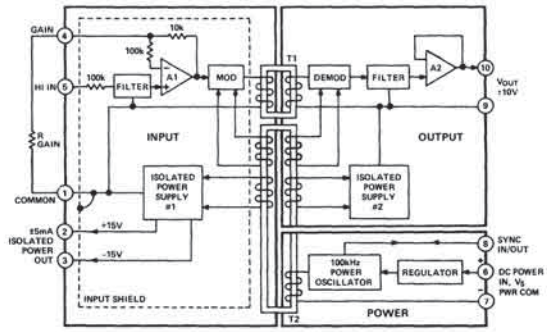


Figure 2. Model 289 Block Diagram

The input signal is filtered and appears at the input of the non-inverting amplifier, A1. This signal is amplified by A1, with its gain determined by the value of resistance connected externally between the gain terminal and the input common terminal. The output of A1 is modulated, carried across the isolation barrier by signal transformer T1, and demodulated. The demodulated voltage is filtered, amplified and buffered by amplifier A2, and applied to the output terminal. The voltage applied to the V_S terminal is set by the regulator to +12V which powers the 100kHz symmetrical square wave power oscillator. The oscillator drives the primary winding of transformer T2. The secondary windings of T2 energize both input and output power supplies, and drives both the modulator and demodulator.

INTERELECTRODE CAPACITANCE AND TERMINAL RATINGS

Capacitance: Interelectrode terminal capacitance, arising from stray coupling capacitance effects between the input terminals and the signal output terminals, are each shunted by leakage resistance values exceeding 50GΩ. Figure 3 illustrates model 289's capacitance, between terminals.

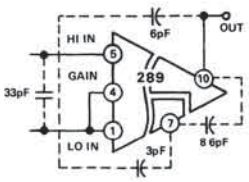


Figure 3. Model 289 Terminal Capacitance

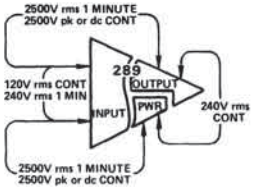


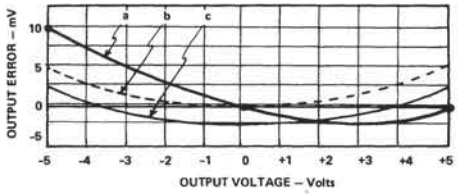
Figure 4. Model 289 Terminal Ratings

Terminal Ratings: CMV performance is given in both peak pulse and continuous ac, or dc peak ratings. Continuous peak ratings apply from dc up to the normal full power response frequencies. Figure 4 illustrates model 289 ratings between terminals.

GAIN AND OFFSET TRIM PROCEDURE

The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to −5V and Gain = 10V/V.

1. Apply E_{IN} = 0 volts and adjust R_O for E_O = 0 volts.
2. Apply E_{IN} = +0.500V dc and adjust R_G for E_O = +5.000V dc.
3. Apply E_{IN} = −0.500V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one-half that measured in step 3 (see curve b).
5. Apply +0.500V dc and adjust R_O until the output error is one-half that measured in step 4 (see curve c).



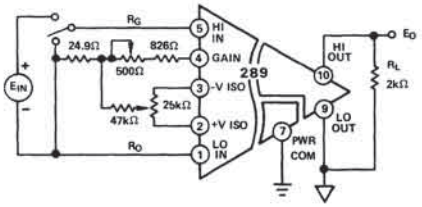


Figure 5a. Recommended Offset and Gain Adjustment for Gains > 1

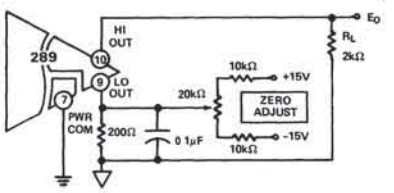


Figure 5b. Recommended Offset Adjustment for G = 1V/V

PERFORMANCE CHARACTERISTICS

Figure 6 shows the phase shift vs. frequency. The low phase shift and wide bandwidth of the model 289 make it suitable for use in SCR Motor Controller and other high frequency applications.

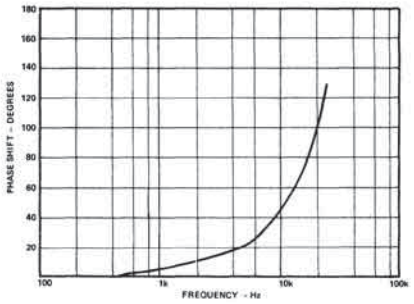


Figure 6. Typical 289 Phase vs. Frequency

Figure 7 illustrates the effect of source impedance imbalance on CMR performance at 60Hz for gains of 1V/V, 10V/V, and 100V/V. CMR is typically 120dB at 60Hz and a balanced source impedance. CMR is >60dB for source impedance imbalances up to 100kΩ.

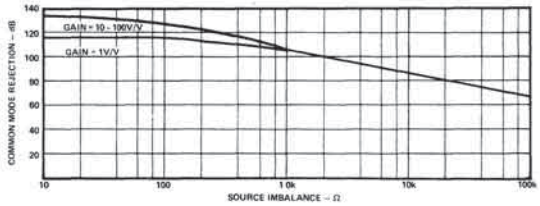


Figure 7. Typical 289 Common Mode Rejection vs. Source Impedance

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth. Figure 8 shows rms voltage noise in a bandwidth from 0.05Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.05Hz to 100Hz is 8μV pk-pk at a gain of 100V/V. The peak-to-peak value is derived by multiplying the rms value at F = 100Hz (1.2μV rms) by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest. Increasing gain will also reduce the noise, referred to input.

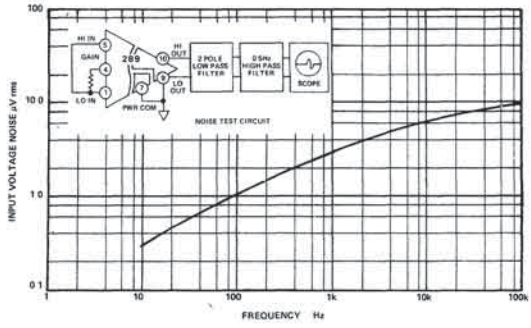


Figure 8. Typical Input Voltage Noise vs. Bandwidth

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % peak-to-peak output voltage span; e.g., nonlinearity of model 289J operating at an output span of 10V pk-pk (±5V) is ±0.05% or ±5mV. Figure 9 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V). Figure 10 shows the effect of gain vs. gain nonlinearity.

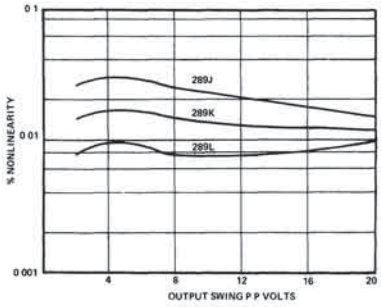


Figure 9. Typical Gain Nonlinearity vs. Output Swing

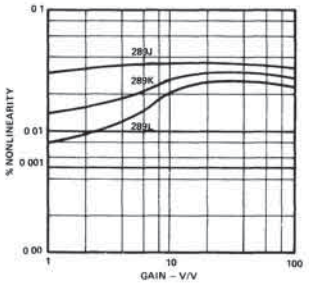


Figure 10. Typical Gain Nonlinearity vs. Gain

Common Mode Rejection: Input-to-output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 1kΩ balanced source at a gain of 100V/V. Figure 11 illustrates CMR performance as a function of signal frequency. CMR approaches 156dB at dc with source imbalance as high as 1kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 6dB lower than at a gain of 100V/V.

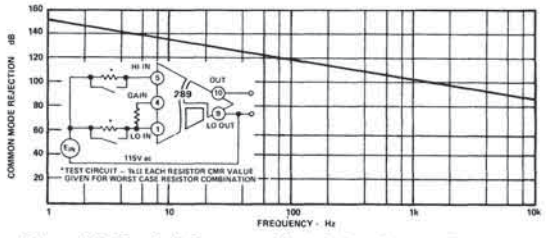


Figure 11. Typical Common Mode Rejection vs. Frequency at a Gain of 1V/V, CMR is typically 6dB Lower than at a Gain of 100V/V

MULTICHANNEL APPLICATIONS

Isolation amplifiers containing internal oscillators may exhibit a slowly varying offset voltage at the output when used in multichannel applications. This offset voltage is the result of adjacent internal oscillators beating together. For example, if two adjacent isolation amplifiers have oscillator frequencies of 100.0kHz and 100.1kHz respectively, a portion of the difference frequency may appear as a slowly varying output offset voltage error. Model 289 eliminates this problem by offering a synchronization terminal (pin 8). When this terminal is interconnected with other model 289 synchronization terminals, the units are synchronized. Alternately, one or more units may be synchronized to an external 100kHz ±2% square-wave generator by the connection of synchronization termial(s) to that generator. The generator output should be 2.5V–5.0V p-p with 1kΩ source impedance to each unit. Use an external oscillator when you need to sync to an external 100kHz source, such as a sub-multiple of a microprocessor clock. A differential line driver, such as SN75158, can be used to drive large clusters of model 289. When using the synchronization pin, keep leads as short as possible and do not use shielded wire. These precautions are necessary to avoid capacitance from the synchronization terminal to other points. It should be noted that units synchronized must share the same power common to ensure a return path.

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Isolated DAS: In data acquisition systems where multiple transducers are powered by a single supply and the magnitude of that supply is low enough for a multiplexer to handle the voltages on all the transducers, it is economical to multiplex ahead of an isolator. The fast settling time of the model 289 makes this configuration practical where slower isolators would not be usable.

Figure 12 shows an application where the difference in voltage between any two terminals of any of the transducers does not exceed 30 volts. Though the input of the model 289 is protected against line voltage, its power terminals are not; neither is the multiplexer so protected. This circuit will not, therefore, withstand the differential application of line voltage.

Multiplexer addressing is binary, an enable providing selection of the circuit shown as a signal source. Optical isolation is provided for digital signals. When several of these circuits are used for several groups of transducers, the model 289's should be synchronized.

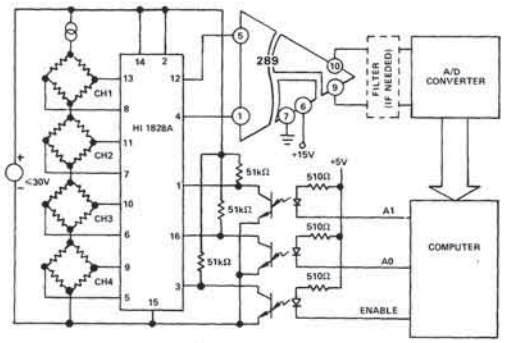


Figure 12. DAS with MUX Ahead of Isolator

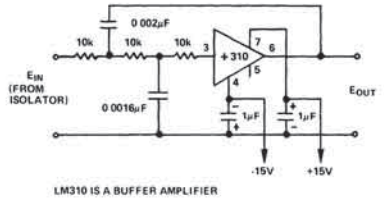


Figure 13. 2-Pole, 5kHz Active Filter

Noise Reduction in Data Acquisition Systems: Transformer coupled isolators must have a carrier to pass dc signals through their signal transformers. Inevitably some carrier frequency ripple passes through to the isolator output. As the bandwidth of an isolator becomes a larger fraction of its carrier frequency, this ripple becomes more difficult to control. Despite this difficulty, the model 289 produces very low ripple; therefore, additional filtration will usually be unnecessary. However, in some applications, particularly where a fast analog-to-digital converter is used following the isolator, it may be desirable to add filtration; otherwise, ripple may cause inaccurate conversions. The 2-pole low-pass shown in Figure 13 limits isolator bandwidth to 5kHz, which is the full power bandwidth of the model 289. Carrier ripple is much reduced. Another beneficial effect of an output filter is smoothing of discontinuous high frequency waveforms.

Motor Control and AC Load Control: Phase shift and bandwidth are important considerations for motor control and ac load control applications. The model 289 possesses sufficient bandwidth and acceptable phase shift for such tasks.

Figure 14 shows two model 289's sensing the armature voltage and current of a motor. Faithful replicas of the waveforms of these variables are applied to the motor control. A1 operates at unity gain from divided R1–R3 to deliver an output that is 1/100 of the armature voltage of the motor. A2 operates at a gain of 100V/V to deliver a voltage 100 times that developed across the current sensing shunt.

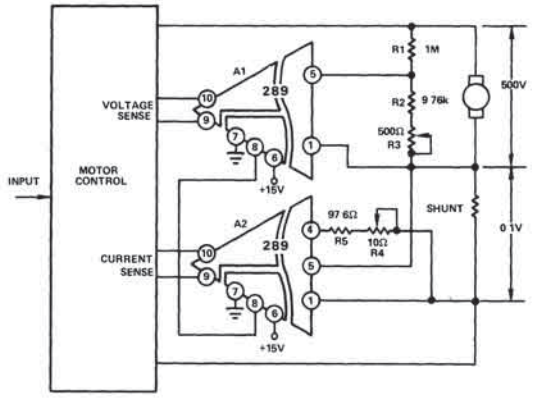


Figure 14. Isolating a Motor Controller

Figure 15 shows three model 289's sensing the voltages on the three phases of an ac load. The Y network shown divides the voltages of the three phases and creates a neutral for the input commons of the isolators. The output of each isolator is a faithful replica of the phase of the waveform it senses. The isolator outputs provide the feedback necessary for the trigger control to correctly fire the triacs. In other applications, the outputs of the isolators might have been fed to rms-to-dc converters.

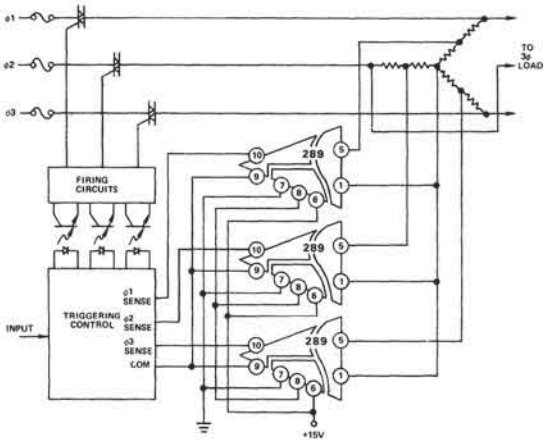


Figure 15. Isolating a 3 Phase Load Controller

Isolated DACs: Figure 16 shows a 12-bit DAC with ±5V isolated output. A buffered -5V reference voltage is provided to the DAC by A1a, A1b and associated circuitry. The digital input causes a proportion of DAC current to flow into OUT1 of the DAC. The remaining DAC current flows into OUT2. Current flowing into OUT1 causes positive voltage at the output of A1c. Current flowing into OUT2 causes a positive voltage at the output of A1d, which in turn causes a negative voltage at the output of A1c. Voltage appearing at the output of A1c is reproduced at the output of the model 289. R5 and R8 must be adjusted to produce less than 0.5mV at OUT1 and OUT2 of the DAC respectively. R15 may be used to adjust gain and R11 to adjust offset with the binary code 1000 0000 0000 to zero.

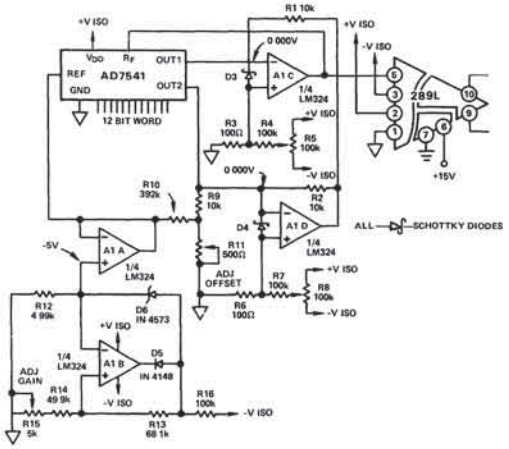


Figure 16. 12-Bit Isolated Voltage DAC

Figure 17 shows the model 289 providing an isolated 4-to-20mA output from a 12-bit DAC. A1a provides a -4V reference to the DAC. The digital input causes a portion of DAC current to flow into OUT1, causing a positive voltage at the output of A1d. A1b produces a voltage across R4 proportional to DAC current. A1c and associated circuitry sink a current which is one-fourth of the full scale current of the DAC, causing a positive voltage of 1 volt at the output of A1d. With the code 1111 1111 1111, +5 volts appears at the output of A1d. Operation is unipolar with a positive offset. The output voltage of A1d is reproduced at the output of the isolator, where the circuitry shown converts it into a 4-to-20mA current which may be applied to the load R_L.

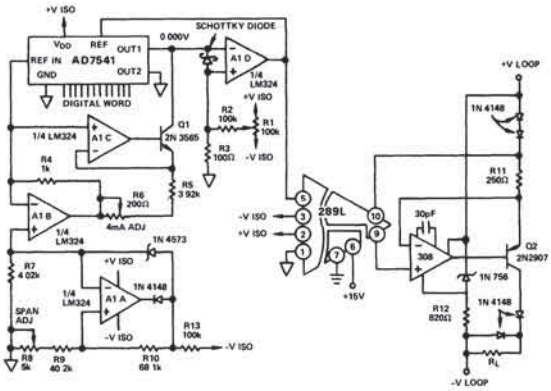


Figure 17. 12-Bit Isolated Process Current DAC

Temperature Measurement: Figure 18 shows the model 289 providing a ground-referred output in an application measuring the temperature of an object floating at a high common mode voltage. The AD590 temperature sensor sinks a current of -1μA/K. This current flows into the gain terminal of the model 289, developing +10mV/K across the internal feedback resistor. This voltage also appears at the output of the model 289.

The circuitry shown connected by a dotted line may be useful if an output of 10mV/°C is desired. A current of +273μA is sourced through the 8.66k resistor and the potentiometer cancelling the AD590 current at 0°C (273K), resulting in 0mV at the output at 0°C.

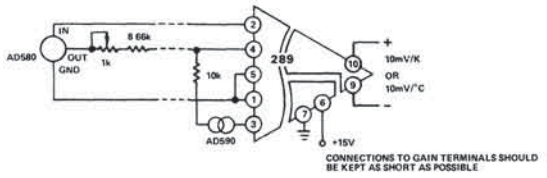


Figure 18. Isolated Temperature Measurement

Low-Cost, Single and Multichannel Isolation Amplifiers

Models 290A/292A

FEATURES

Low Cost
Multichannel Capability Using External Oscillator (292A)
Isolated Power Supply: ±13V dc @ ±5mA (290A) or ±15mA (292A)
Low Nonlinearity: 0.1% @ 10V pk-pk Output
High Gain Stability: 0.001%/1000 Hours; 0.01%/°C
Small Size: 1.5″ × 1.5″ × 0.62″
Low Input Offset Voltage Drift: 10μV/°C (Gain = 100V/V)
Wide Input/Output Dynamic Range: 20V pk-pk
High CMV Isolation: 1500V dc, Continuous
Wide Gain Range: 1 to 100V/V

APPLICATIONS

Ground Loop Elimination in Industrial and Process Control
High Voltage Protection in Data Acquisition Systems
Fetal Heart Biomedical and Monitoring Instrumentation
Off-Ground Signal Measurements

GENERAL DESCRIPTION

Models 290A and 292A are low-cost, compact, isolation amplifiers that are optimized for single and multichannel industrial applications, respectively. The model 290A has a self-contained oscillator and is intended for single channel applications. A single external synchronizing oscillator can drive up to 16 model 292As or, a virtually limitless number of model 292As can be configured using multiple oscillators. The user can supply the external oscillator circuit or specify model 281 oscillator module, which includes a voltage regulator for operation over a wide single supply voltage range of +8V to +28V.

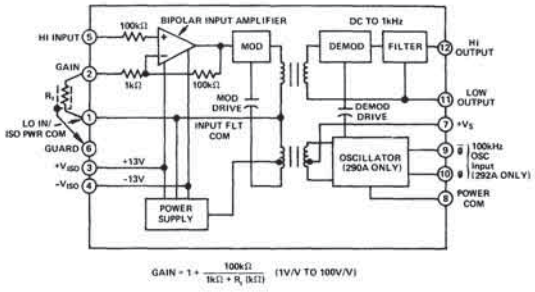
Models 290A and 292A design features include: adjustable gain, from 1 to 100V/V, dual isolated power, ±13V dc, ±1500V dc off ground isolation, 100dB minimum CMR at 60Hz, 1kΩ source imbalance, in a compact 1.5″ × 1.5″ × 0.6″ module. Models 290A and 292A achieve low input noise of 1μV pk-pk (10Hz bandwidth, G = 100V/V), nonlinearity of ±0.1% @ 10V pk-pk output, and an input/output dynamic range of 20V pk-pk.

Using modulation techniques with reliable transformer isolation, models 290A and 292A will interrupt ground loops, leakage paths, and voltage transients, while providing dc to 2kHz (–3dB) response.

WHERE TO USE MODELS 290A AND 292A

Industrial Applications: In data acquisition systems, computer interface systems, process signal isolators and high CMV instrumentation, models 290A and 292A offer complete galvanic isolation and protection against damage from transients and fault voltages. High level transducer interface capability is afforded with 20V pk-pk input signal range at a gain of 1V/V operation. In portable single or multichannel designs, single power supply operation (+8V to +16V) enables battery operation.

MODELS 290A/292A FUNCTIONAL BLOCK DIAGRAM



DESIGN FEATURES AND USER BENEFITS

Isolated Power: Dual ±13V dc output, completely isolated from the input power terminals (±1500V dc isolation), provides the capability to excite floating signal conditioners, front end buffer amplifiers and remote transducers such as thermistors or bridges.

Adjustable Gain: Models 290A and 292A adjustable gain offers compatibility with a wide class of input signals. A single external resistor enables gain adjustment from 1V/V to 100V/V providing flexibility in both high level transducer interfacing as well as low level sensor measurement applications.

Floating, Guarded Front-End: The input stage of models 290A and 292A can directly accept floating differential signals or it may be configured as a high performance instrumentation front-end to accept signals having CMV with respect to input power common.

High Reliability: Models 290A and 292A are conservatively designed, compact modules, capable of reliable operation in harsh environments. They have a calculated MTBF of over 400,000 hours and are designed to meet MIL-STD-202E environmental testing as well as the IEEE Standard for Transient Voltage Protection (472-1974: Surge Withstand Capability).

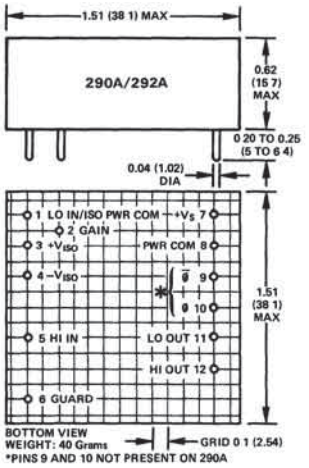
SPECIFICATIONS (typical @ +25°C; G = 100V/V and V_S = +15V unless otherwise noted)

MODEL	290A	292A
GAIN (NONINVERTING)		
Range (50kΩ Load)		1 to 100V/V
Formula		$\text{Gain} = \left[1 + \frac{100k\Omega}{1k\Omega + R_1(k\Omega)}\right]$
Deviation from Formula		±3%
vs. Time		±0.001%/1000 Hours
vs. Temperature (-25°C to +85°C)[1]		±0.0075%/°C
Nonlinearity, G = 1V/V to 100V/V[2]		±0.1% (±0.25%)[3]
INPUT VOLTAGE RATINGS		
Linear Differential Range, G = 1V/V		±5V min (±10V min)[3]
Max Safe Differential Input		
Continuous, 1 min		110V rms
Max CMV, Inputs to Outputs		
ac, 60Hz, 1 Minute Duration		1500V rms max
Continuous, ac		±1000V pk max
Continuous, dc		±1500V pk max
CMR, Inputs to Outputs, 60Hz, $R_S \leq 1k\Omega$		
Balanced Source Impedance		106dB
1kΩ Hi In Lead Only		100dB min
Max Leakage Current, Inputs to Power Common		
@ 115V ac, 60Hz		10μA rms max
INPUT IMPEDANCE		
Differential		$10^8\Omega \| 70pF$
Overload		100kΩ
Common Mode		$5 \times 10^{10}\Omega \| 100pF$
INPUT DIFFERENCE CURRENT		
Initial, @ +25°C		+3nA
vs. Temperature (-25°C to +85°C)		±0.1nA/°C
INPUT NOISE		
Voltage, G = 100V/V		
0.01Hz to 10Hz		1μV p-p
10Hz to 1kHz		1.5μV rms
Current		
0.05Hz to 100Hz		5pA p-p
FREQUENCY RESPONSE		
Small Signal, -3dB, G = 1V/V		2.5kHz
Slew Rate		50mV/μs
Full Power, 10V p-p Output		
Gain - 1V/V thru 100V/V	2.0kHz(1.0kHz)[3]	3.0kHz(1.0kHz)[3]
OFFSET VOLTAGE REFERRED TO INPUT		
Initial, @ +25°C, Adjustable to Zero		±(5 + 50/G)mV
vs. Temperature (-25°C to +85°C)	±(10 + 150/G)μV/°C	±(8 + 250/G)μV/°C
vs. Supply Voltage		±1mV/%
RATED OUTPUT		
Voltage, 50k Load		±5V min (±10V min)[3]
Output Impedance		1kΩ
Output Ripple, 1MHz Bandwidth		10mV pk-pk
OSCILLATOR DRIVE INPUT		
Input Voltage	N/A	8 to 16V pk-pk
Input Frequency	N/A	100kHz ±5%, max
ISOLATED POWER OUTPUTS		
Voltage Full Load		±13V dc
Accuracy		±5%
Current[4]	±5mA min	±15mA min
Regulation, No Load to Full Load		+0, -15%
Ripple, 100kHz Bandwidth	200mV p-p	250mV p-p
POWER SUPPLY, SINGLE POLARITY		
Voltage, Rated Performance		+15V dc
Voltage, Operating		+8V dc to +15.5V dc
Current, Quiescent		+20mA
TEMPERATURE RANGE		
Rated Performance		-25°C to +85°C
Storage		-55°C to +85°C
CASE DIMENSIONS		1.5" X 1.5" X 0.62"

NOTES
[1] Gain temperature drift is specified as a percentage of output signal level.
[2] Gain nonlinearity is specified as a percentage of 10V pk-pk output span.
[3] These specs apply for a 20V pk-pk output span.
[4] Do not load V_{ISO} when operating at output spans greater than 10V pk-pk
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



SHIELDED MOUNTING SOCKET AC1054

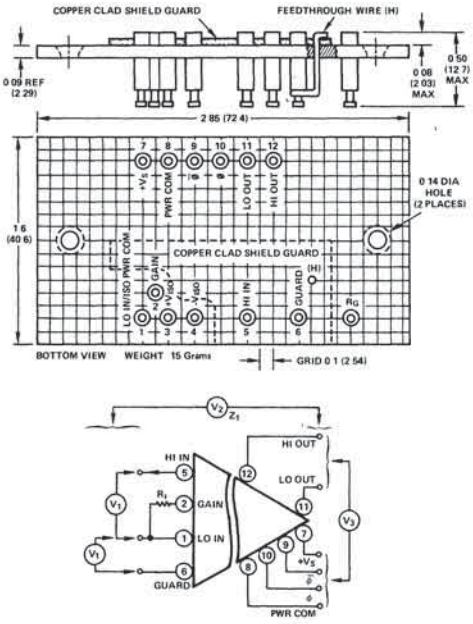


Figure 1. Model 290A and 292A Terminal Ratings

Symbol	Rating	Remarks
V_1	±110V rms (cont.)	Withstand Voltage, Steady State
V_2	±1000V pk (cont.)	Isolation, Steady State, ac
V_2	±1500V pk (cont.)	Isolation, Steady State, dc
V_2	±1500V rms (1 min)	Isolation, ac, 60Hz
V_3	±50V pk (cont.)	Isolation, dc
Z_1	$50G\Omega \| 20pF$	Isolation Impedance

Table I. Isolation Ratings Between Terminals

THEORY OF OPERATION

The remarkable performance of models 290A and 292A are derived from the carrier isolation technique which is used to transfer both signal and power between the amplifier's guarded input stage and the rest of the circuitry. The block diagram for both models is shown in Figure 2 below.

The bipolar input preamplifier operates single-ended (non-inverting). Only a difference bias current flows with zero net bias current. A third wire return path for input bias current is not required. Gain can be set from 1V/V to 100V/V by changing the gain resistor, R_i. *To preserve high CMR, the gain resistor must be guarded.* Best performance is achieved by shorting terminal 2 to terminal 1 and operating the isolator at a gain of 100V/V.

For powering floating input circuitry such as buffer amplifiers, instrumentation amplifiers, calibration signals and transducers, dual isolated power is provided. High CMV isolation is achieved by the low-leakage transformer coupling between the input preamplifier, modulator section and the output circuitry. Only the 10pF leakage capacitance between the floating input section and the rest of the circuitry keeps the CMR from being infinite.

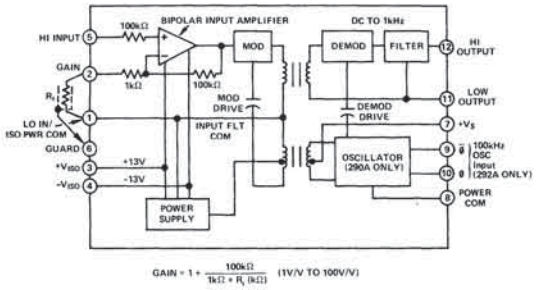


Figure 2. Block Diagram – Models 290A and 292A

GUIDELINES ON EFFECTIVE SHEILDING & GROUNDING PRACTICES

- Use twisted shielded cable to reduce inductive and capacitive pickup.
- Drive the transducer cable shield, S, with the common mode signal source, E_G, to reduce the effective cable capacitance as shown in Figure 3. This is accomplished by connecting the shield point S, as close as possible to the transducer signal low point B. This may not always be possible. In some cases the shield may be separated from signal low by a portion of the medium being measured (e.g. pressure transducer). This will cause a common mode signal, E_M, to be generated by the medium between the shield and the signal low. The 86dB CMR capability of both models between the input terminals (HI IN and LO IN) and GUARD, will work to suppress the common mode signal, E_M.
- Dress unshielded leads short at the connection terminals and reduce the area formed by these leads to minimize inductive pickup.

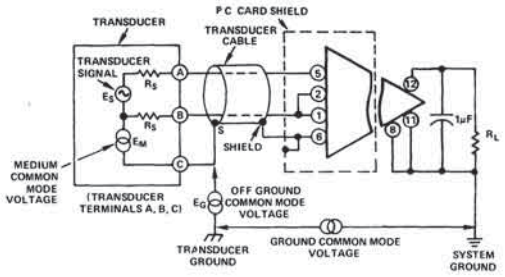
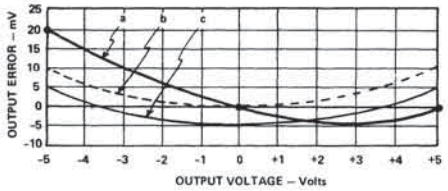


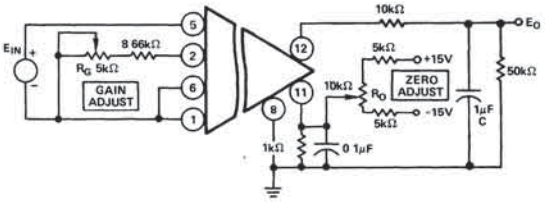
Figure 3. Transducer – Amplifier Interface

GAIN AND OFFSET TRIM PROCEDURE

In applying the isolation amplifier, highest accuracy is achieved by adjustment of gain and offset voltage to minimize the peak error encountered over the selected output voltage span. The following procedure illustrates a calibration technique which can be used to minimize output error. In this example, the output span is +5V to -5V and operation at Gain = 10V/V is desired.

1. Apply E_{IN} = 0 volts and adjust R_O for E_O = 0 volts.
2. Apply E_{IN} = +0.5V dc and adjust R_G for E_O = +5.0V dc.
3. Apply E_{IN} = –0.5V dc and measure the output error (see curve a).
4. Adjust R_G until the output error is one half that measured in step 3 (see curve b).
5. Apply +0.5V dc and adjust R_O until the output error is one half that measured in step 4 (see curve c).





GAIN RESISTOR, R_i, 1%, 50ppm/°C METAL FILM TYPE IS RECOMMENDED
FOR GAIN = 1V/V, LEAVE TERMINAL 2 OPEN.
FOR GAIN = 100V/V, SHORT TERMINAL 2 TO TERMINAL 1

$$\text{GAIN} = 1 + \frac{100k\Omega}{1k\Omega + R_i(k\Omega)}$$

OUTPUT FILTER, 10kΩ RESISTOR AND CAPACITOR, C.
SELECT C TO ROLL-OFF NOISE AND OUTPUT RIPPLE

$$f = (-3dB) = \frac{1}{2\pi C\,(11k\Omega)}$$

Figure 4. Gain and Offset Adjustment

SELECTING BANDWIDTH

In low frequency signal measurements, such as thermocouple temperature measurements, strain gage measurements and geophysical instrumentation, an external filter is used to select bandwidth and minimize output noise.

When used with a buffer amplifier as shown in Figure 5a below, a series resistor (R_S) is used to lower the effective value of the filter capacitor required to achieve very low frequency (under 200Hz) noise filtering.

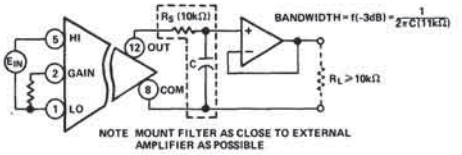


Figure 5a. Selecting Bandwidth with External Capacitor and Buffer

An active filter, as illustrated in Figure 5b will significantly improve 60Hz noise reduction at the output by providing a sharp roll-off characteristic. The 5Hz 3-pole active filter design illustrated in Figure 5b, will increase the 60Hz noise reduction by 50dB. Overall CMR performance of models 290 and 292 and the 5Hz active filter approaches 150dB @ 60Hz and 1kΩ imbalance.

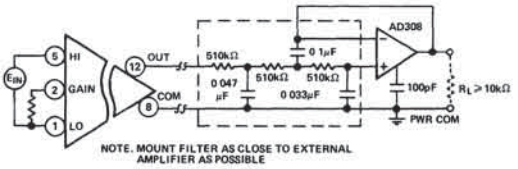


Figure 5b. Selecting Bandwidth with a 3-Pole 5Hz Active Filter

PERFORMANCE CHARACTERISTICS

Common Mode Rejection: Input-to-Output CMR is dependent on source impedance imbalance, signal frequency and amplifier gain. CMR is rated at 115V ac, 60Hz and 1kΩ imbalance at a gain of 100V/V. Figure 6 illustrates CMR performance as a function of signal frequency. CMR approaches 130dB at dc with source imbalances as high as 1kΩ. As gain is decreased, CMR is reduced. At a gain of 1V/V, CMR is typically 12dB lower than at a gain of 100V/V.

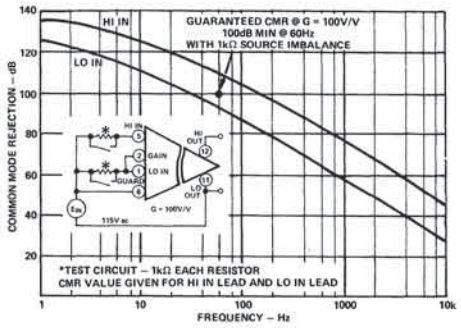


Figure 6. Typical Common Mode Rejection vs. Frequency

Figure 7 illustrates the effect of source imbalance on CMR performance at 60Hz and Gain = 100V/V. CMR is typically 110dB at 60Hz and a balanced source. CMR is maintained greater than 70dB for source imbalances up to 100kΩ.

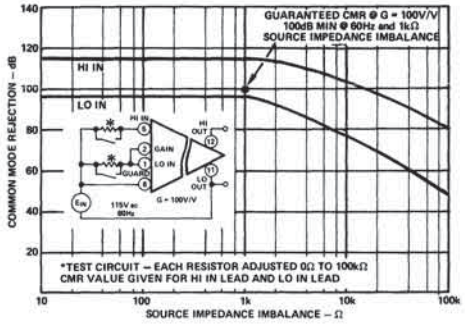


Figure 7. Typical Common Mode Rejection vs. Source Impedance Imbalance

Gain Nonlinearity: Linearity error is defined as the deviation of the output voltage from the best straight line and is specified as a % of peak-to-peak output voltage span; e.g., nonlinearity of models 290A and 292A operating at an output span of 10V pk-pk (±5V) is ±0.1% or ±10mV. Figure 8 illustrates gain nonlinearity for any output span to 20V pk-pk (±10V).

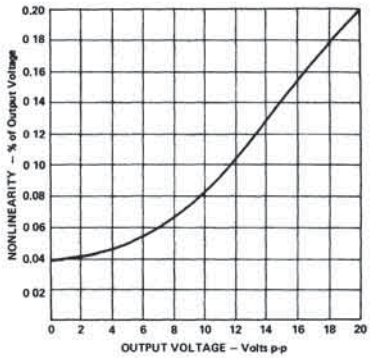


Figure 8. Typical Gain Nonlinearity vs. Output Voltage

Input Voltage Noise: Voltage noise, referred to input, is dependent on gain and bandwidth as illustrated in Figure 9. RMS voltage noise is shown in a bandwidth from 0.01Hz to the frequency shown on the horizontal axis. The noise in a bandwidth from 0.01Hz to 10Hz is 1μV pk-pk at a gain of 100V/V. This value is derived by multiplying the rms value at f = 10Hz shown in Figure 9 by 6.6.

For best noise performance in particular applications, a low pass filter at the output should be used to selectively roll-off noise and undesired signal frequencies beyond the bandwidth of interest. Increasing gain will also reduce the input noise.

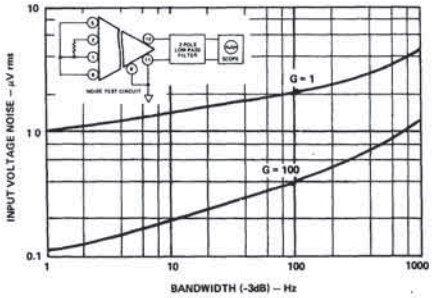


Figure 9. Typical Input Voltage Noise vs. Bandwidth

Input Offset Voltage Drift: Total input drift is composed of two sources, input and output stage drifts and is gain dependent. The curve of Figure 10 illustrates total input drift over the gain range of 1 to 100V/V.

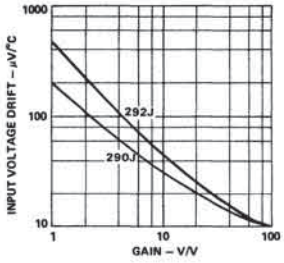


Figure 10. Typical Input Offset Voltage Drift vs. Gain

REFERENCE EXCITATION OSCILLATOR, MODEL 281

When applying model 292A, the user has the option of building a low cost 100kHz excitation oscillator, as shown in Figure 11, or purchasing a module from Analog Devices—model 281.

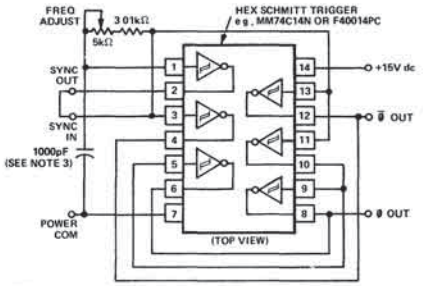


Figure 11. 100kHz Oscillator Interconnection Diagram

The block diagram of model 281 is shown in Figure 12. An internal +12V dc regulator is provided to permit the user the option of operating over two, pin selectable, power input ranges; terminal 6 offers a range of +14V dc to +28V dc; terminal 7 offers an input range of +8V dc to +14V dc.

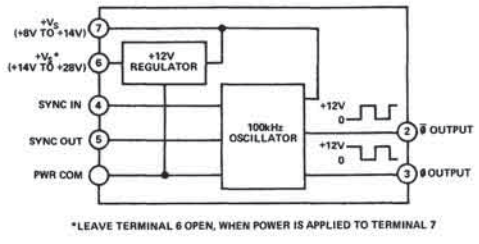


Figure 12. Model 281 Block Diagram

Model 281 oscillator is capable of driving up to 16 model 292As. As shown in Figure 13, an additional model 281 may be driven in a slave-mode to expand the total system channels from 16 to 32. By adding additional model 281's in this manner, systems of over 1000 channels may be easily configured.

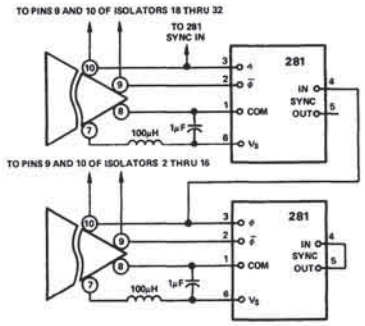


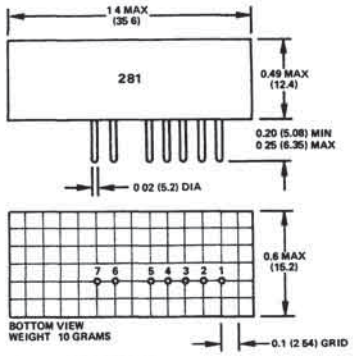
Figure 13. External Oscillator Interconnection

SPECIFICATIONS
(typical @ +25°C and V_S = +15V dc unless otherwise noted)

MODEL	281
OUTPUT	
Frequency	100kHz ±5%
Waveform	Squarewave
Voltage (ϕ and $\bar{\phi}$ terminals)	0 to +12V pk
Fan-Out[1,2]	16 max
POWER SUPPLY RANGE[3]	
High Input, Pin 6	+(14 to 28)V dc
Quiescent Current, N L	+5mA
F L	+16mA
Low Input, Pin 7	+(8 to 14)V dc
Quiescent Current, N L	+12mA
F L	+33mA
TEMPERATURE	
Rated Performance	0 to +70°C
Storage	-55°C to +85°C

[1] Model 292A oscillator drive input represents unity oscillator load.
[2] For applications requiring more than 16 292As, additional 281s may be used in a master/slave mode. Refer to Figure 13.
[3] Full load consists of 16 model 292As and 281 oscillator slave.
Specifications subject to change without notice.

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).



PIN TERMINAL IDENTIFICATION

1	POWER COMMON	5	SYNC OUTPUT
2	$\bar{\phi}$ OUTPUT	6	$+V_S$ HIGH RANGE +(14 to 28)V dc
3	ϕ OUTPUT	7	$+V_S$: LOW RANGE +(8 to 14)V dc
4	SYNC INPUT		

MATING SOCKET:
CINCH #16 DIP OR EQUIVALENT

APPLICATIONS IN INDUSTRIAL MEASUREMENT AND CONTROL SYSTEMS

Remote Sensor Interface: In chemical, nuclear and metal processing industries, models 290A and 292A can be applied to measure and control off-ground millivolt signals in the presence ±1500V dc CMV signals. In interface applications such as pH control systems or on-line process measurement systems such as pollution monitoring, models 290A and 292A offer complete galvanic isolation to eliminate troublesome ground loop problems. Isolated power outputs and adjustable gain add to the application flexibility of these models.

Figure 14 illustrates how model 290A or 292A can be combined with a low drift, 1μV/°C front-end amplifier, model AD517L, to interface low level transducer signals. Both products provide isolated ±13V dc power and front-end guard in addition to eliminating ground loops and preserving high CMR (100dB @ 60Hz).

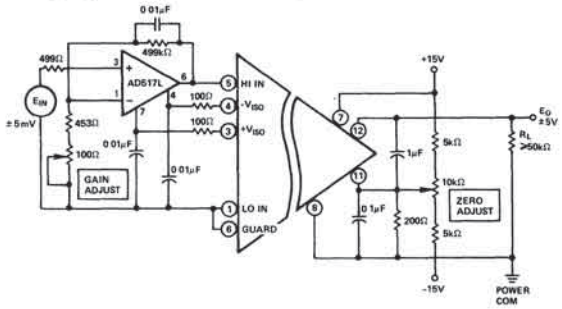


Figure 14. Input Signal Conditioning Using Isolated Power for Transducer Buffer Amplifier

Instrumentation Amplifier: Models 290A and 292A provide a floating guarded input stage capable of directly accepting isolated differential signals. The noninverting, single-ended input stage offers simple two wire interconnection with floating input signals.

In applications where the isolated power is applied to transducers such as bridges which generate differential input signals with common mode voltages measured with respect to the isolated power common, models 290A and 292A can be connected as shown in Figure 15. To achieve high CMR with respect to the ISO PWR COM, the following trim procedure is recommended.

CMR Trim Procedure

1) Connect a 1V pk-pk oscillator between the +IN/–IN and IN COM terminals as shown in Figure 15.
2) Set the input frequency at 0.5Hz and adjust R1 for minimum E_O.
3) Set the input frequency at 60Hz and adjust R2 for minimum E_O.
4) Repeat steps 2 and 3 for best CMR performance.

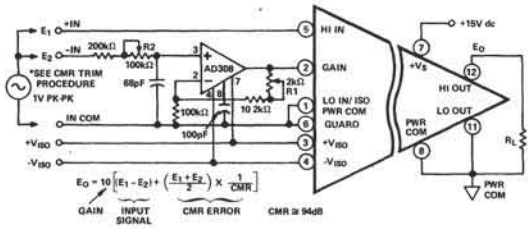


Figure 15. Application of 290A as Instrumentation Amplifier

Isolated Temperature Measurements: Industrial temperature measurements are often performed in harsh environments where line voltages or transients can sometimes be impressed on the temperature sensor. To provide protection for the delicate recording instrumentation, models 290A and 292A can be applied as shown in Figure 16. The Analog Devices' AC2626 probe is a temperature sensor whose output is a current directly proportional to absolute temperature. The isolation amplifier provides the isolated power (+13V dc) as well as the input/output isolation. Zero calibration is performed by placing the AC2626 probe in a zero temperature bath and adjusting R_O for E_O to 0 volts. Full scale output adjustment is performed by placing the AC2626 probe in boiling water (100°C) and adjusting R_S for 1.000V output.

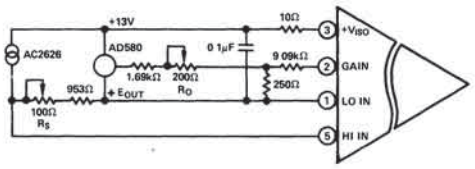


Figure 16. Isolated Temperature Measurements

Current Loop Receiver: Model 290A and 292A can be applied to measurement of analog quantities transmitted via 4-20mA current loops over substantial distances through harsh environments. Figure 17 shows an application of model 290A or 292A as a current loop receiver. A 25Ω resistor converts the 4-20mA current input from a remote loop to a 100–500mV differential voltage input, which the isolator amplifies, isolates, and translates to a 0 to +5V output level at local system ground.

Among the most-helpful characteristics of the isolator in this kind of measurement are the high common-mode rejection (100dB minimum at 60Hz with 1kΩ source unbalance) and the high common-mode rating (±1500 volts dc). The former means low noise pickup; the latter means excellent isolation and protection against large transients. The high common-mode rejection, permitting relatively low input voltage to be used (0.4V span, in this case), permits the use of a low current-metering resistance, which in turn results in low compliance-voltage loading on the current loop, and therefore permits insertion into existing loops without encountering overrange problems. The gain of 12.5 provides a substantial output span, and the floating output permits biasing to a 0 to 5V range.

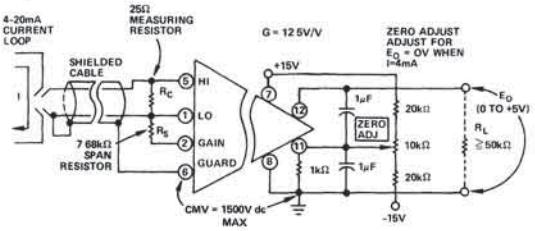


Figure 17. Isolated Analog Interface; 4 to 20mA is Converted to 0 to +5V at the Output, with Up to ±1500V of Isolation

Analog Multipliers/Dividers
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Selection Guide
Analog Multipliers/Dividers

Model	Small Signal Bandwidth MHz	Full-Scale Accuracy %	X Nonlinearity % of FS	Y Nonlinearity % of FS	Full-Scale Output	Page	Notes
AD532	1	1	0.5	0.2	10V	6 – 7	4-quadrant multiplication
AD534	1	0.25	0.12	0.01	10V	6 – 13	4-quadrant multiplication
AD538	0.4	0.5	–	–	10V	6 – 23	Multiplication, division, powers, roots
AD539	30	1	–	–	1mA	6 – 31	2-quadrant multiplication/division
AD632	1	0.5	0.08	0.01	10V	6 – 39	
AD834	500	0.5	–	–	4mA	6 – 43	High frequency 4-quadrant multiplier

Orientation
Analog Multipliers/Dividers

The devices catalogued in this section are high-performance ICs that accept analog voltages and multiply, divide, square and/or square-root them, depending on device properties and connections. Other multiplying devices available from Analog Devices include digital multipliers (in *DSP Products Databook*) and multiplying D/A converters (*Data Conversion Products Databook*).

Multiplication: For two inputs, V_x and V_y, a multiplier will provide the output, $E_{out} = V_x V_y / E_{ref}$, where E_{ref} is a dimensional constant, usually of 10V nominal value. If $E_{ref} = 10V$, $E_{out} = 10V$ when V_x and V_y are 10V. Multipliers are used for modulation and demodulation, fixed and variable remote gain adjustment, power measurement and mathematical operations in analog computing, curve fitting and linearizing.

If the inputs may be of either positive or negative polarity and the output polarity is in a correct relationship for multiplication, the device is called a "four-quadrant" multiplier, reflecting the four quadrants of the X-Y plane.

Squaring: If $V_x = V_y = V_{in}$, a multiplier's output will be V_{in}^2/E_{ref}. A four-quadrant multiplier, used as a squarer, will have an output that is positive whether V_{in} is positive or negative. Squarers are useful in frequency doubling, power measurement of constant loads and mathematical operations.

Division: For a numerator input, V_z, and a denominator input, V_x, an analog divider will provide the output, $E_{out} = E_{ref}(V_z/V_x)$. If $E_{ref} = 10V$, E_{out} will be 10V or less for $V_z \leq V_x$. V_x is of a single polarity and will not provide meaningful results if it approaches zero too closely. If V_z may be of either positive or negative polarity, the device is described as a "two-quadrant" divider, and the output will reflect the polarity of V_z. Analog dividers are used to compute ratios – such as efficiency, attenuation, or gain; they are also used for fixed and variable remote gain adjustment, ratiometric measurements and for mathematical operations in analog computing.

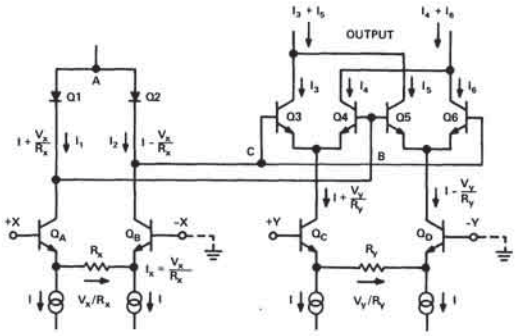
Square Rooting: For a numerator input, V_{in}, and a denominator input, E_o (the output fed back to the denominator input), the output of a divider is $E_o = E_{ref}(V_{in}/E_o)$; hence $E_o = \sqrt{E_{ref} V_{in}}$. A square rooter works in one quadrant; some devices require external diode circuitry to prevent latchup if the input polarity changes, even momentarily. Square roots are used in vector and rms computation, to linearize flowmeters, and for mathematical operations in analog computing.

CHOOSING A MULTIPLIER, DIVIDER, ETC.

A number of devices are listed here, differing in internal ar- architecture, external functional configuration and performance specifications. Most have essentially fixed references; the AD538 is a *multifunction device* that performs the one-quadrant operation, $E_o = V_z/(V_y/V_x)^m$, where m is an exponent adjustable from 1/5 to 5.

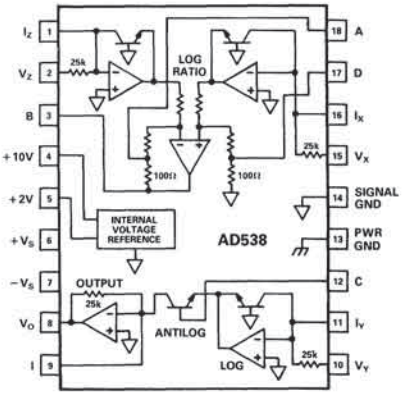
Considerable information on these functions, the nature of devices to perform them and extensive discussions of their applications can be found in the *Nonlinear Circuits Handbook*.[1] A wealth of information is also to be found in the data sheets for the individual devices published in this section. In addition to the products listed here, a number of popular earlier products are still available; data sheets are available upon request.

Internal Architecture: All of the devices in this section rely on the logarithmic properties of silicon P-N junctions. An example of the *translinear* principle that they embrace can be seen in the circuitry of a "Gilbert cell," employed in various forms for analog multiplication. Its four-quadrant multiplying circuitry and performance are described in (1), with further references to the original sources. The input voltages are converted to currents; the currents are multiplied together and divided by a reference, and the net output current, $I_x I_y / I_{ref}$, is converted to voltage by feedback around the output amplifier. The feedback terminals are available as inputs for applications involving division.



Basic Four-Quadrant Variable-Transconductance Multiplier Circuit

$$I_O = (I_3 + I_5) - (I_4 + I_6) = \frac{2 V_X V_Y}{I R_X R_Y}$$



AD538 Functional Block Diagram

In multifunction devices like the AD538, the feedback currents of the V_z and V_x input op amps are used to develop logarithmic voltages across transistor base-emitter junctions; these voltages are differenced to provide the logarithm of the ratio, V_z/V_x.

[1] ***Nonlinear Circuits Handbook*, D.H. Sheingold, ed., 1976, 536pp., $5.95, Analog Devices, Inc., P.O. Box 796, Norwood, MA 02062**

At the user's choice, this log ratio is either amplified (m>1), attenuated (m<1) or unchanged (m = 1), then applied to a product-antilog circuit which adds the logarithm of V_y, then takes the antilogarithm to produce the output equation,

$$V_{OUT} = V_y \left\{ \frac{V_z}{V_x} \right\}^m$$

Wideband Multipliers have bandwidths greatly exceeding 1MHz. The output is generally in the form of current, for maximum bandwidth (current-to-voltage conversion tends to reduce bandwidth and is unnecessary in many applications). The user can choose an appropriate external amplifier – or other circuitry – to meet the needs of the application. The *AD539* is a dual multiplier/divider with two independent two-quadrant signal channels (inputs Y1 and Y2) and a common X-input, which provides linear control of gain for both channels. Signal bandwidth is 30MHz and control bandwidth is 5MHz. The *AD834* is a four-quadrant multiplier with 500MHz large-signal bandwidth and 0.5% static-accuracy specifications. It has differential X and Y inputs and differential open-collector current output. For 1-volt inputs, its differential output current is ±4mA.

External Functional Configuration: Most of the devices listed here can be used for multiplication, division, squaring and/or square-rooting (MDSSR), by the appropriate connection of external jumpers. Performance of pretrimmed devices is optimized in specified modes of operation. The data sheets show how devices are connected for the various modes of operation; where appropriate, the suggested trim circuits and procedures for optimizing performance are provided.

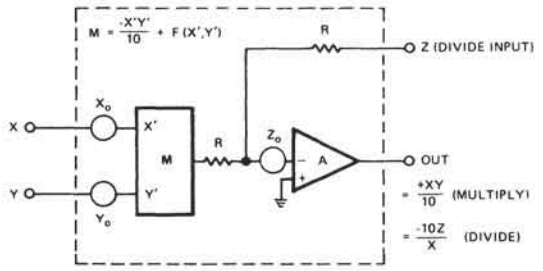
Technologies: The devices described in these two volumes are monolithic integrated circuits. For any application, the user will evaluate a device on the basis of its performance in the desired mode(s). The pretrimmed ICs use laser trimming of thin-film-on-silicon chips at the wafer stage and buried-Zener reference circuitry, as well as thermally balanced input stages and "core" circuitry, for overall maximum errors as low as 0.25%, and high linearities.

Performance: Multiplier performance, specifications and test circuitry are described in great detail in the *Nonlinear Circuits Handbook*. Here is a brief digest of the factors relating to low-frequency performance.

An ideal multiplier has an output which is the product of two input variables, X and Y, divided by the 10V scaling voltage. However, the practical multiplier is subject to various offset errors and nonlinearities which must be accounted for in its application. This discussion is intended to assist the designer in understanding and interpreting multiplier and divider specifications and obtaining insight into device performance.

In practical (see the simplified single-ended multiplier in the figure), a multiplier may be considered as having two parts, one (M) contains the input circuitry and the multiplying cell; the other is a gain-conditioning op amp, A.

Also summed at the op-amp input is the feedback variable, Z. In multiplication, Z is connected to the output circuit. In division, Z and X are the inputs, and Y is connected to the output. The figure shows a model with 10-volt scale factor used for considering



Functional Block Diagram of Typical Multiplier/Divider

errors. X_o and Y_o are input offset voltages, Z_o is the offset-referred-to-the-input of the output amplifier, and f(X′, Y′) is the nonlinearity, viewed as the departure from the ideal multiplication, $\frac{X'Y'}{10R}$. The output equation, including the errors is of the form

$$E_o = \frac{XY}{10B} \pm \left[\underbrace{\frac{X_oY}{10B} \pm \frac{XY_o}{10B}}_{\text{Linear "Y" Feedthrough "X"}} \pm Z_o + f(X,Y) \right]$$

Product; Output offset; Nonlinearity and Feedthrough

The errors are included in the bracketed term, except for gain error, which is the departure of "B", the gain-error term, from its nominal value of unity. The effects of input offsets (called "linear feedthrough") can be set to zero by adding external input biases, the output offset can be set to zero by biasing the output amplifier, and the gain can be externally calibrated by adjusting the reference or the feedback resistance. The remaining departure from the ideal output for any combination of input values is the irreducible *linearity error*, or *nonlinearity*, a function of X and Y that differs from device to device and, with temperature, within a given device. The component of nonlinearity for X = 0 is called "Y feedthrough" and for Y = 0, it is called "X feedthrough".

The "total error" specification includes the effects of all these errors. Although a guide to performance, it may produce an excessively conservative design in some applications. For example, output offset is not important if the output is to be capacitively coupled or the initial offset is nulled. Gain error is not important if system gain is to be adjusted elsewhere in the system or if gain is not a critical factor in system performance. If frequent calibration of offset and scale-factor errors is available (e.g., in a "smart" instrument, via software) nonlinearity becomes the limiting parameter. In such cases, improvements in predicted error can be achieved by using the approximate linearity equation:

$$f(X,Y) \cong |V_x|\epsilon_x + |V_y|\epsilon_y$$

where ϵ_x and ϵ_y are the specified fractional linearity errors (%/100) and V_x and V_Y are the input signals.

When multipliers are fed back for use in division applications, it is important to recognize that maximum multiplication errors are increased approximately in proportion to the inverse of the denominator voltage ($10V/V_x$), and bandwidth is decreased in proportion to denominator voltage. Pretrimmed multipliers used in such applications, with wide dynamic range of X (i.e., >10:1), will always benefit greatly by the trimming of offsets, especially Z_o (affects offsets) and X_o (affects gain), for small values of X.

DEFINITIONS OF SPECIFICATIONS*

Accuracy is defined in terms of *total error* of the multiplier at room temperature and constant nominal supply voltage. *Total error* includes the sum of the effects of input and output dc offsets, nonlinearity, and feedthrough. *Temperature dependence* and *supply-voltage effects* are specified separately.

Scale Factor: The *scale-factor error* (or *gain* error) is the difference between the average scale factor and the ideal scale factor (e.g., $(10V)^{-1}$). It is expressed in percent of the output signal. *Temperature dependence* is specified.

Output Offset refers to the offset voltage at the output-amplifier stage. This offset is usually minimized at manufacture and can be trimmed where high accuracy is desired. Output *offset vs. temperature* is also specified.

Linearity Error or *Nonlinearity* is the maximum difference between actual and "best-straight-line" theoretical output, for all pairs of input values, expressed as a percentage of full scale, with all other dc errors nulled. It is the irreducible minimum error. It is usually expressed in terms of X and Y nonlinearity, with the named input swinging over its full-scale range and the other input at (±) 10V. Y nonlinearity is considerably less than X nonlinearity in simple "Gilbert-cell" multipliers. This specification includes nonlinear feedthrough.

X or Y Feedthrough is the signal at the output for any value of X or Y input in the rated range, when the other input is zero. It has two components, a linear one, corresponding to an *input offset* at the zero input, which can be trimmed out (but can drift and has a *temperature specification*), and a nonlinear one, which is irreducible. *Feedthrough* is usually specified at one frequency (50Hz) for a 20V p-p sine wave input. It increases with frequency, and plots of typical feedthrough vs. frequency are provided on multiplier data sheets.

Noise is specified and measured with both inputs at zero signal and zero impedance (i.e., shorted). For low-frequency applications, filtering the output of the mulitplier may improve small-signal resolution significantly.

Dynamic Parameters include: *small-signal bandwidth, full-power response, slew(ing) rate, small-signal amplitude error* and *settling time*.

Small-Signal Bandwidth is the frequency at which the output is down 3dB from its low-frequency value (i.e., by about 30%) for a nominal output amplitude of 10% of full scale.

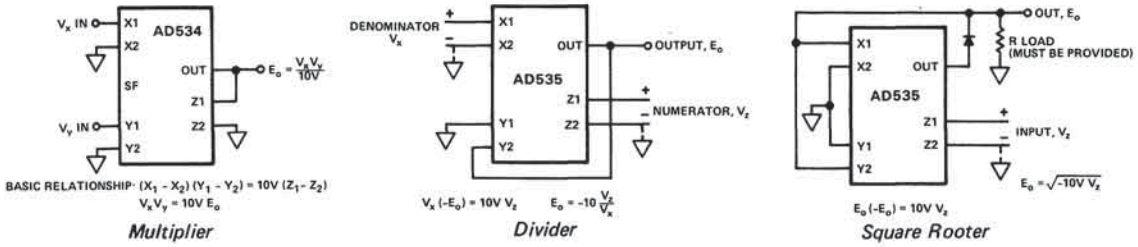
Full-Power Response is the maximum frequency at which the multiplier can produce the full-scale voltage into its rated load without noticeable distortion.

Slew(ing) Rate (V/μs) is the maximum rate of change of output voltage for the product of a full-scale dc voltage and a full-scale step input.

Small-Signal Amplitude Error is defined in relation to the frequency at which the amplitude response, or scale-factor, is in error by 1%, measured with a small (10% of full-scale) signal.

Settling Time, for the product of a ±10V step and 10V dc, is the total length of time the output takes to respond to an input change and stay within some specified error band of its final value. Settling time cannot be accurately predicted from any other dynamic specifications; it is specified in terms of a prescribed measurement.

Vector Error is the most sensitive measure of dynamic error. It is usually specified in terms of the frequency at which a phase error of 0.01 radians (0.57°) occurs.



Multiplier *Divider* *Square Rooter*

***These are general definitions. Further definitions are provided as footnotes to the Specifications tables; they should be read carefully.**

Internally Trimmed Integrated Circuit Multiplier

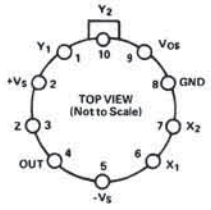
AD532

FEATURES
- Pretrimmed To ±1.0% (AD532K)
- No External Components Required
- Guaranteed ±1.0% max 4-Quadrant Error (AD532K)
- Diff Inputs For $(X_1-X_2)(Y_1-Y_2)/10V$ Transfer Function
- Monolithic Construction, Low Cost

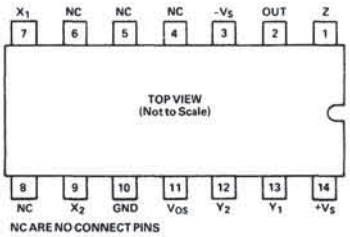
APPLICATIONS
- Multiplication, Division, Squaring, Square Rooting
- Algebraic Computation
- Power Measurements
- Instrumentation Applications
- Available in Chip Form

AD532 PIN CONFIGURATIONS

AD532H



AD532D



NC ARE NO CONNECT PINS

PRODUCT DESCRIPTION

The AD532 is the first pretrimmed single chip monolithic multiplier/divider. It guarantees a maximum multiplying error of ±1.0% and a ±10V output voltage without the need for any external trimming resistors or output op amp. Because the AD532 is internally trimmed, its simplicity of use provides design engineers with an attractive alternative to modular multipliers, and its monolithic construction provides significant advantages in size, reliability and economy. Further, the AD532 can be used as a direct replacement for other IC multipliers that require external trim networks (such as the AD530).

FLEXIBILITY OF OPERATION

The AD532 multiplies in four quadrants with a transfer function of $(X_1-X_2)(Y_1-Y_2)/10V$, divides in two quadrants with a $10VZ/(X_1-X_2)$ transfer function, and square roots in one quadrant with a transfer function of $\pm\sqrt{10VZ}$. In addition to these basic functions, the differential X and Y inputs provide significant operating flexibility both for algebraic computation and transducer instrumentation applications. Transfer functions, such as XY/10V, $(X^2-Y^2)/10V$, $\pm X^2/10V$, and $10VZ/(X_1-X_2)$ are easily attained, and are extremely useful in many modulation and function generation applications, as well as in trigonometric calculations for airborne navigation and guidance applications, where the monolithic construction and small size of the AD532 offer considerable system advantages. In addition, the high CMRR (75dB) of the differential inputs makes the AD532 especially well qualified for instrumentation applications, as it can provide an output signal that is the product of two transducer-generated input signals.

GUARANTEED PERFORMANCE OVER TEMPERATURE

The AD532J and AD532K are specified for maximum multiplying errors of ±2% and ±1% of full scale, respectively at +25°C, and are rated for operation from 0 to +70°C. The AD532S has a maximum multiplying error of ±1% of full scale at +25°C; it is also 100% tested to guarantee a maximum error of ±4% at the extended operating temperature limits of −55°C and +125°C. All devices are available in either the hermetically-sealed TO-100 metal can or TO-116 ceramic DIP.

ADVANTAGES OF ON-THE-CHIP TRIMMING OF THE MONOLITHIC AD532

1. True ratiometric trim for improved power supply rejection.
2. Reduced power requirements since no networks across supplies are required.
3. More reliable since standard monolithic assembly techniques can be used rather than more complex hybrid approaches.
4. High impedance X and Y inputs with negligible circuit loading.
5. Differential X and Y inputs for noise rejection and additional computational flexibility.

SPECIFICATIONS (@ +25°C, $V_S = \pm 15V$, R≥2kΩ V_{OS} grounded)

Model	AD532J			AD532K			AD532S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}$		
Total Error ($-10V \le X, Y \le +10V$)		±1.5	**±2.0**		±0.7	**±1.0**		±0.5	**±1.0**	%
T_A = min to max		±2.5			±1.5				**±4.0**	%
Total Error vs Temperature		±0.04			±0.03			±0.01	**±0.04**	%/°C
Supply Rejection (±15V ±10%)		±0.05			±0.05			±0.05		%/%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.8			±0.5			±0.5		%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.3			±0.2			±0.2		%
Feedthrough, X (Y Nulled, X = 20V pk-pk 50Hz)		50	**200**		30	**100**		30	**100**	mV
Feedthrough, Y (X Nulled, Y = 20V pk-pk 50Hz)		30	**150**		25	**80**		25	**80**	mV
Feedthrough vs. Temp.		2.0			1.0			1.0		mV p-p/°C
Feedthrough vs. Power Supply		±0.25			±0.25			±0.25		mV/%
DYNAMICS										
Small Signal BW (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error		75			75			75		kHz
Slew Rate (V_{OUT} 20 pk-pk)		45			45			45		V/μs
Settling Time (to 2%, ΔV_{OUT} = 20V)		1			1			1		μs
NOISE										
Wideband Noise f = 5Hz to 10kHz		0.6			0.6			0.6		mV (rms)
f = 5Hz to 5MHz		3.0			3.0			3.0		mV (rms)
OUTPUT										
Output Voltage Swing	±10	±13		±10	±13		±10	±13		V
Output Impedance (f≤1kHz)		1			1			1		Ω
Output Offset Voltage		±40				**±30**			**±30**	mV
Output Offset Voltage vs Temp.		0.7			0.7				**2.0**	mV/°C
Output Offset Voltage vs. Supply		±2.5			±2.5			±2.5		mV/%
INPUT AMPLIFIERS (X, Y and Z)										
Signal Voltage Range (Diff. or CM Operating Diff)		±10			±10			±10		V
CMRR	**40**			**50**			**50**			dB
Input Bias Current										
X, Y Inputs		3			1.5	**4**		1.5	**4**	μA
X, Y Inputs T_{min} to T_{max}		10			8			8		μA
Z Input		±10			±5	**±15**		±5	**±15**	μA
Z Input T_{min} to T_{max}		±30			±25			±25		μA
Offset Current		±0.3			±0.1			±0.1		μA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10V\,Z/(X_1-X_2)$			$10V\,Z/(X_1-X_2)$			$10V\,Z/(X_1-X_2)$		
Total Error										
($V_X = -10V$, $-10V \le V_Z \le +10V$)		±2			±1			±1		%
($V_X = -1V$, $-10V \le V_Z \le +10V$)		±4			±3			±3		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10V}$			$\frac{(X_1-X_2)^2}{10V}$			$\frac{(X_1-X_2)^2}{10V}$		
Total Error		±0.8			±0.4			±0.4		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function		$-\sqrt{10VZ}$			$-\sqrt{10VZ}$			$-\sqrt{10VZ}$		
Total Error ($0V \le V_Z \le 10V$)		±1.5			±1.0			±1.0		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	±10		**±18**	±10		**±18**	±10		±22	V
Supply Current										
Quiescent		4	**6**		4	**6**		4	**6**	mA
PACKAGE OPTIONS[1]										
TO-116 (D-14)	AD532JD			AD532KD			AD532SD			
TO-100 (H-10A)	AD532JH			AD532KH			AD532SH			

NOTE
[1]See Section 16 for package outline information.
Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

FUNCTIONAL DESCRIPTION

The functional block diagram for the AD532 is shown in Figure 1, and the complete schematic in Figure 2. In the multiplying and squaring modes, Z is connected to the output to close the feedback around the output op amp. (In the divide mode, it is used as an input terminal.)

The X and Y inputs are fed to high impedance differential amplifiers featuring low distortion and good common mode rejection. The amplifier voltage offsets are actively laser trimmed to zero during production. The product of the two inputs is resolved in the multiplier cell using Gilbert's linearized transconductance technique. The cell is laser trimmed to obtain $V_{out} = (X_1-X_2)(Y_1-Y_2)/10$ volts. The built-in op amp is used to obtain low output impedance and make possible self-contained operation. The residual output voltage offset can be zeroed at V_{OS} in critical applications . . . . otherwise the V_{OS} pin should be grounded.

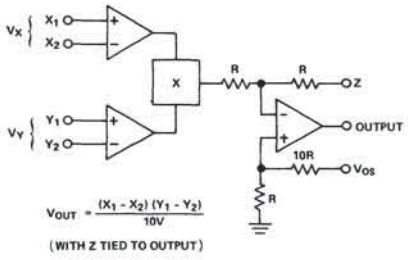


Figure 1. Functional Block Diagram

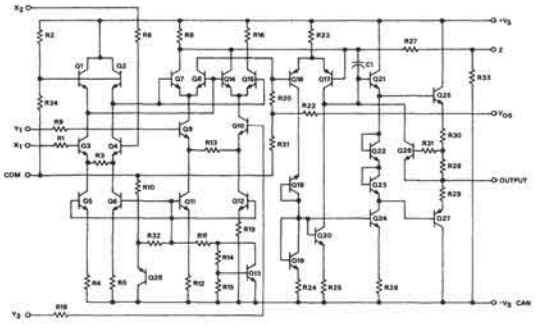


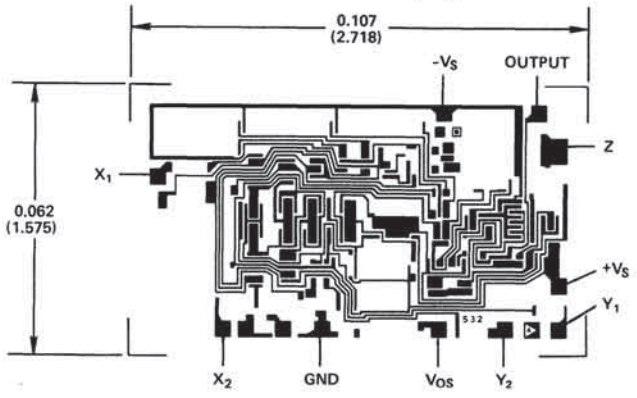
Figure 2. AD532 Schematic Diagram

ORDERING GUIDE

Model	Max Mult Error	Temperature Range	Model	Max Mult Error	Temperature Range
AD532JH	±2.0%	0 to +70°C	AD532SH	±1.0%	-55°C to +125°C
AD532JD	±2.0%	0 to +70°C	AD532SD	±1.0%	-55°C to +125°C
AD532KH	±1.0%	0 to +70°C	AD532SH/883B	±1.0%	-55°C to +125°C
AD532KD	±1.0%	0 to +70°C	AD532SD/883B	±1.0%	-55°C to +125°C

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).



AD532 PERFORMANCE CHARACTERISTICS

Multiplication accuracy is defined in terms of total error at +25°C with the rated power supply. The value specified is in percent of full scale and includes X_{in} and Y_{in} nonlinearities, feedback and scale factor error. To this must be added such application-dependent error terms as power supply rejection, common mode rejection and temperature coefficients (although worst case error over temperature is specified for the AD532S). Total expected error is the rms sum of the individual components, since they are uncorrelated.

Accuracy in the divide mode is only a little more complex. To achieve division, the multiplier cell must be connected in the feedback of the output op amp as shown in Figure 13. In this configuration, the multiplier cell varies the closed loop gain of the op amp in an inverse relationship to the denominator voltage. Thus, as the denominator is reduced, output offset, bandwidth and other multiplier cell errors are adversely affected. The divide error and drift are then $\epsilon_m \cdot 10V/X_1-X_2)$ where ϵ_m represents multiplier full scale error and drift, and (X_1-X_2) is the absolute value of the denominator.

NONLINEARITY

Nonlinearity is easily measured in percent harmonic distortion. The curves of Figures 3 and 4 characterize output distortion as a function of input signal level and frequency respectively, with one input held at plus or minus 10V dc. In Figure 4 the sine wave amplitude is 20V(p-p).

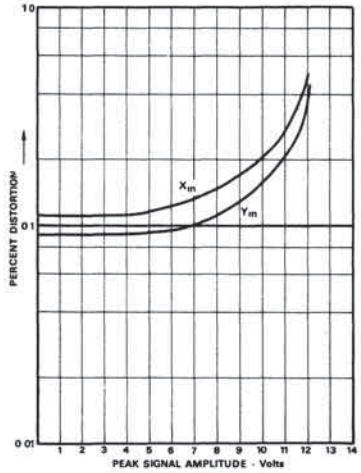


Figure 3. Percent Distortion vs. Input Signal

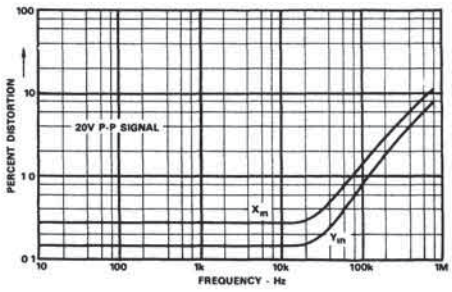


Figure 4. Percent Distortion vs. Frequency

AC FEEDTHROUGH

AC Feedthrough is a measure of the multiplier's zero suppression. With one input at zero, the multiplier output should be zero regardless of the signal applied to the other input. Feedthrough as a function of frequency for the AD532 is shown in Figure 5. It is measured for the condition $V_X = 0$, $V_Y = 20V(p-p)$ and $V_Y = 0$, $V_X = 20V(p-p)$ over the given frequency range. It consists primarily of the second harmonic and is measured in millivolts peak-to-peak.

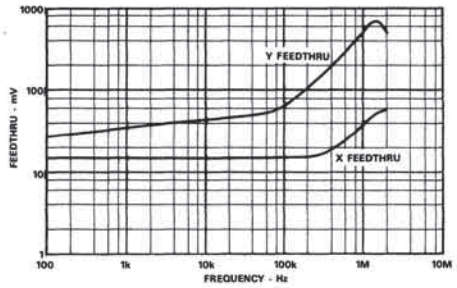


Figure 5. Feedthrough vs. Frequency

COMMON MODE REJECTION

The AD532 features differential X and Y inputs to enhance its flexibility as a computational multiplier/divider. Common mode rejection for both inputs as a function of frequency is shown in Figure 6. It is measured with $X_1 = X_2 = 20V(p-p)$, $(Y_1-Y_2) = \pm 10V$ dc and $Y_1 = Y_2 = 20V(p-p)$, $(X_1-X_2) = \pm 10V$ dc.

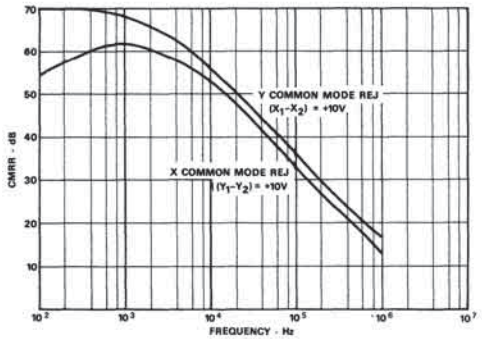


Figure 6. CMRR vs. Frequency

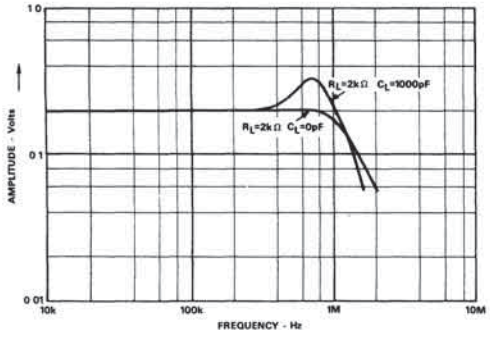


Figure 7. Frequency Response, Multiplying

DYNAMIC CHARACTERISTICS

The closed loop frequency response of the AD532 in the multiplier mode typically exhibits a 3dB bandwidth of 1MHz and rolls off at 6dB/octave thereafter. Response through all inputs is essentially the same as shown in Figure 7. In the divide mode, the closed loop frequency response is a function of the absolute value of the denominator voltage as shown in Figure 8.

Stable operation is maintained with capacitive loads to 1000pF in all modes, except the square root for which 50pF is a safe upper limit. Higher capacitive loads can be driven if a 100Ω resistor is connected in series with the output for isolation.

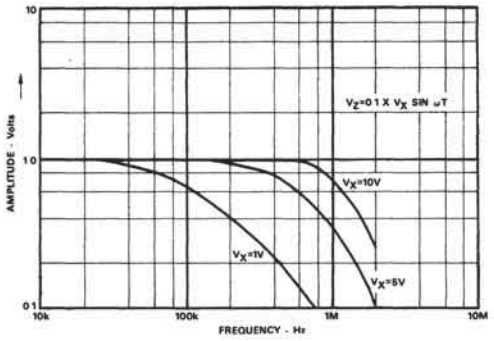


Figure 8. Frequency Response, Dividing

POWER SUPPLY CONSIDERATIONS

Although the AD532 is tested and specified with ±15V dc supplies, it may be operated at any supply voltage from ±10V to ±18V for the J and K versions and ±10V to ±22V for the S version. The input and output signals must be reduced proportionately to prevent saturation, however, with supply voltages below ±15V, as shown in Figure 9. Since power supply sensitivity is not dependent on external null networks as in the AD530 and other conventionally nulled multipliers, the power supply rejection ratios are improved from 3 to 40 times in the AD532.

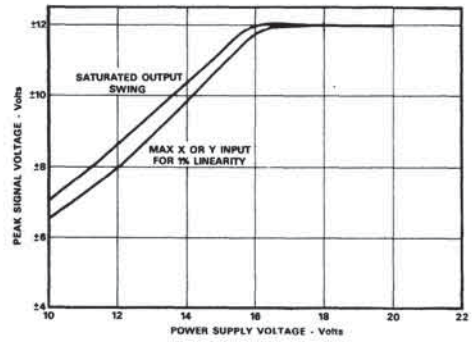


Figure 9. Signal Swing vs. Supply

NOISE CHARACTERISTICS

All AD532s are screened on a sampling basis to assure that output noise will have no appreciable effect on accuracy. Typical spot noise vs. frequency is shown in Figure 10.

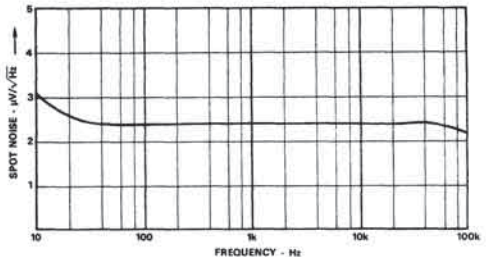


Figure 10. Spot Noise vs. Frequency

APPLICATIONS CONSIDERATIONS

The performance and ease of use of the AD532 is achieved through the laser trimming of thin film resistors deposited directly on the monolithic chip. This trimming-on-the-chip technique provides a number of significant advantages in terms of cost, reliability and flexibility over conventional in-package trimming of off-the-chip resistors mounted or deposited on a hybrid substrate.

First and foremost, trimming on the chip eliminates the need for a hybrid substrate and the additional bonding wires that are required between the resistors and the multiplier chip. By trimming more appropriate resistors on the AD532 chip itself, the second input terminals that were once committed to external trimming networks (e.g., AD530) have been freed to allow fully differential operation at both the X and Y inputs. Further, the requirement for an input attenuator to adjust the gain at the Y input has been eliminated, letting the user take full advantage of the high input impedance properties of the input differential amplifiers. Thus, the AD532 offers greater flexibility for both algebraic computation and transducer instrumentation applications.

Finally, provision for fine trimming the output voltage offset has been included. This connection is optional, however, as the AD532 has been factory-trimmed for total performance as described in the listed specifications.

REPLACING OTHER IC MULTIPLIERS

Existing designs using IC multipliers that require external trimming networks (such as the AD530) can be simplified using the pin-for-pin replaceability of the AD532 by merely grounding the X_2, Y_2 and V_{OS} terminals. (The V_{OS} terminal should always be grounded when unused.)

APPLICATIONS

MULTIPLICATION

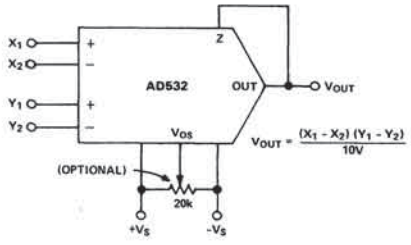


Figure 11. Multiplier Connection

For operation as a multiplier, the AD532 should be connected as shown in Figure 11. The inputs can be fed differentially to the X and Y inputs, or single-ended by simply grounding the unused input. Connect the inputs according to the desired polarity in the output. The Z terminal is tied to the output to close the feedback loop around the op amp (see Figure 1). The offset adjust V_{OS} is optional and is adjusted when both inputs are zero volts to obtain zero out, or to buck out other system offsets.

SQUARE

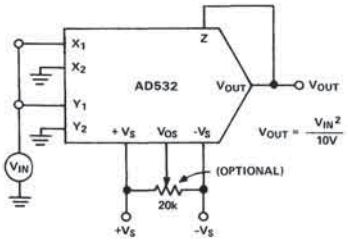


Figure 12. Squarer Connection

The squaring circuit in Figure 12 is a simple variation of the multiplier. The differential input capability of the AD532 can be used, however, to obtain a positive or negative output response to the input....a useful feature for control applications, as it might eliminate the need for an additional inverter somewhere else.

DIVISION

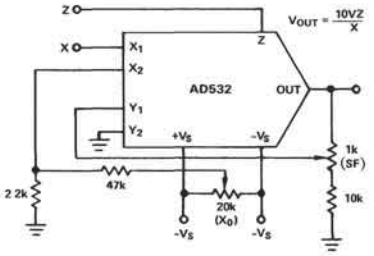


Figure 13. Divider Connection

The AD532 can be configured as a two-quadrant divider by connecting the multiplier cell in the feedback loop of the op amp and using the Z terminal as a signal input, as shown in Figure 13. It should be noted, however, that the output error is given approximately by $10V\epsilon_m/(X_1-X_2)$, where ϵ_m is the total error specification for the multiply mode; and bandwidth by $f_m \cdot (X_1-X_2)/10V$, where f_m is the bandwidth of the multiplier. Further, to avoid positive feedback, the X input is restricted to negative values. Thus for single-ended negative inputs (0V to −10V), connect the input to X and the offset null to X_2; for single-ended positive inputs (0V to +10V), connect the input to X_2 and the offset null to X_1. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

For practical reasons, the useful range in denominator input is approximately $500mV \leq |(X_1-X_2)| \leq 10V$. The voltage offset adjust (V_{os}), if used, is trimmed with Z at zero and (X_1-X_2) at full scale.

SQUARE ROOT

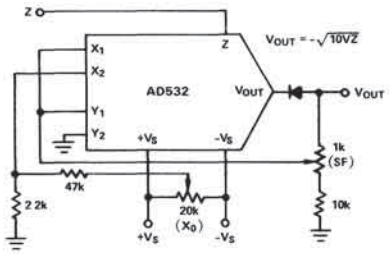


Figure 14. Square Rooter Connection

The connections for square root mode are shown in Figure 14. Similar to the divide mode, the multiplier cell is connected in the feedback of the op amp by connecting the output back to both the X and Y inputs. The diode D_1 is connected as shown to prevent latch-up as Z_{in} approaches 0 volts. In this case, the V_{OS} adjustment is made with Z_{in} = +0.1V dc, adjusting V_{os} to obtain −1.0V dc in the output, $V_{out} = -\sqrt{10VZ}$. For optimum performance, gain (S.F.) and offset (X_0) adjustments are recommended as shown and explained in Table I.

DIFFERENCE OF SQUARES

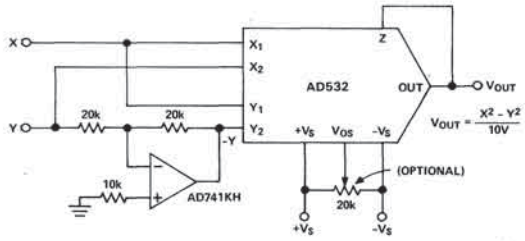


Figure 15. Differential of Squares Connection

The differential input capability of the AD532 allows for the algebraic solution of several interesting functions, such as the difference of squares, $X^2-Y^2/10V$. As shown in Figure 15, the AD532 is configured in the square mode, with a simple unity gain inverter connected between one of the signal inputs (Y) and one of the inverting input terminals ($-Y_{in}$) of the multiplier. The inverter should use precision (0.1%) resistors or be otherwise trimmed for unity gain for best accuracy.

TABLE I

ADJUST PROCEDURE (Divider or Square Rooter)

	DIVIDER			SQUARE ROOTER	
	With:		Adjust for:	With:	Adjust for:
Adjust	X	Z	V_{out}	Z	V_{out}
Scale Factor	−10V	+10V	±10V	+10V	−10V
X_o (Offset)	−1V	+0.1V	±10V	+0.1V	−1V

Repeat if required.

Internally Trimmed Precision IC Multiplier

AD534

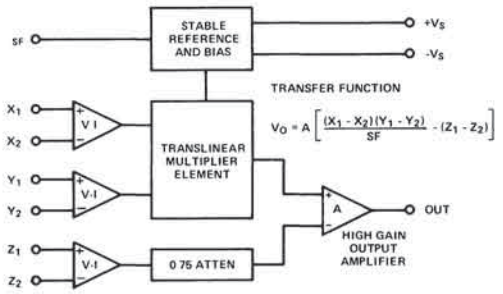
FEATURES

- Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
- All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10V]+Z_2$ Transfer Function
- Scale-Factor Adjustable to Provide up to X100 Gain
- Low Noise Design: 90μV rms, 10Hz–10kHz
- Low Cost, Monolithic Construction
- Excellent Long Term Stability

APPLICATIONS

- High Quality Analog Signal Processing
- Differential Ratio and Percentage Computations
- Algebraic and Trigonometric Function Synthesis
- Wideband, High-Crest rms-to-dc Conversion
- Accurate Voltage Controlled Oscillators and Filters
- Available in Chip Form

AD534 FUNCTIONAL BLOCK DIAGRAM



6

PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00V; by means of an external resistor, this can be reduced to values as low as 3V.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J (±1% max error), AD534K (±0.5% max) and AD534L (±0.25% max) are specified for operation over the 0 to +70°C temperature range. The AD534S (±1% max) and AD534T (±0.5% max) are specified over the extended temperature range, -55°C to +125°C. All grades are available in hermetically sealed TO-100 metal cans and TO-116 ceramic DIP packages.

PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD534 can be very effectively employed as a variable gain differential input amplifier with high common mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: 90μV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

SPECIFICATIONS ($T_A = +25°C$, $\pm V_S = 15V$, $R \geq 2k\Omega$)

Model	AD534J Min	AD534J Typ	AD534J Max	AD534K Min	AD534K Typ	AD534K Max	AD534L Min	AD534L Typ	AD534L Max	Units
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] ($-10V \leq X, Y \leq +10V$)			**±1.0**			**±0.5**			**±0.25**	%
T_A = min to max		±1.5			±1.0			±0.5		%
Total Error vs Temperature		±0.022			±0.015			±0.008		%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02			±0.01			±0.005		%/°C
Supply Rejection (±15V ± 1V)		±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	**±0.3**		±0.10	**±0.12**	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.2			±0.1	**±0.1**		±0.005	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	**±0.3**		±0.05	**±0.12**	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	**±0.1**		±0.003	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±2	**±10**	mV
Output Offset Voltage Drift		200			100			100		µV/°C
DYNAMICS										
Small Signal BW, (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2			2		µs
NOISE										
Noise Spectral-Density SF = 10V		0.8			0.8			0.8		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0.4			0.4			0.4		$\mu V/\sqrt{Hz}$
Wideband Noise f = 10Hz to 5MHz		1			1			1		mV/rms
f = 10Hz to 10kHz		90			90			90		µV/rms
OUTPUT										
Output Voltage Swing	**±11**			**±11**			**±11**			V
Output Impedance (f≤1kHz)		0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]										
Signal Voltage Range (Diff. or CM		±10			±10			±10		V
Operating Diff.)		±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			50		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±2	**±10**	mV
Offset Voltage Drift Z		200			100			100		µV/°C
CMRR	**60**	80		**70**	90		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1			0.05	**0.2**	µA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, $-10V \leq Z \leq +10V$)		±0.75			±0.35			±0.2		%
(X = 1V, $-1V \leq Z \leq +1V$)		±2.0			±1.0			±0.8		%
($0.1V \leq X \leq 10V$, $-10V \leq Z \leq 10V$)		±2.5			±1.0			±0.8		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$		
Total Error ($-10V \leq X \leq 10V$)		±0.6			±0.3			±0.2		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function ($Z_1 \leq Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] ($1V \leq Z \leq 10V$)		±1.0			±0.5			±0.25		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	±8		**±18**	±8		**±18**	±8		**±18**	V
Supply Current										
Quiescent		4	**6**		4	**6**		4	**6**	mA
PACKAGE OPTIONS[6]										
TO-100 (H-10A)		AD534JH			AD534KH			AD534LH		
TO-116 (D-14)		AD534JD			AD534KD			AD534LD		

NOTES

[1]Figures given are percent of full scale, ±10V (i.e., 0.01% = 1mV).

[2]May be reduced down to 3V using external resistor between $-V_S$ and SF

[3]Irreducible component due to nonlinearity excludes effect of offsets

[4]Using external resistor adjusted to give SF = 3V.

[5]See functional block diagram for definition of sections.

[6]See Section 16 for package outline information

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD534S Min	AD534S Typ	AD534S Max	AD534T Min	AD534T Typ	AD534T Max	Units
MULTIPLIER PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] (−10V≤X, Y≤+10V)			±1.0			±0.5	%
T_A = min to max			±2.0			±1.0	%
Total Error vs Temperature			±0.02			±0.01	%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0 25			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02				±0.005	%/°C
Supply Rejection (±15V ± 1V)		±0.01			±0 01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0 2	±0.3	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.2			±0 1	±0.1	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0 15	±0.3	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0 01			±0 01	±0.1	%
Output Offset Voltage		±5	±30		±2	±15	mV
Output Offset Voltage Drift			500			300	µV/°C
DYNAMICS							
Small Signal BW, (V_{OUT} = 0 1 rms)		1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2		µs
NOISE							
Noise Spectral-Density SF = 10V		0.8			0 8		$\mu V/\sqrt{Hz}$
SF = 3V[4]		0 4			0 4		$\mu V/\sqrt{Hz}$
Wideband Noise f = 10Hz to 5MHz		1 0			1 0		mV/rms
f = 10Hz to 10kHz		90			90		µV/rms
OUTPUT							
Output Voltage Swing	±11			±11			V
Output Impedance (f≤1kHz)		0.1			0 1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]							
Signal Voltage Range (Diff. or CM		±10			±10		V
Operating Diff.)		±12			±12		V
Offset Voltage X, Y		±5	±20		±2	±10	mV
Offset Voltage Drift X, Y		100			150		µV/°C
Offset Voltage Z		±5	±30		±2	±15	mV
Offset Voltage Drift Z			500			300	µV/°C
CMRR	60	80		70	90		dB
Bias Current		0.8	2.0		0 8	2.0	µA
Offset Current		0.1			0.1		µA
Differential Resistance		10			10		MΩ
DIVIDER PERFORMANCE							
Transfer Function ($X_1>X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10V, −10V≤Z≤+10V)		±0.75			±0 35		%
(X − 1V, −1V≤Z≤ 1V)		±2.0			±1.0		%
(0.1V≤X≤10V, −10V≤Z≤10V)		±2 5			±1 0		%
SQUARE PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$		
Total Error (−10V≤X≤10V)		±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE							
Transfer Function ($Z_1≤Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] (1V≤Z≤10V)		±1 0			±0 5		%
POWER SUPPLY SPECIFICATIONS							
Supply Voltage							
Rated Performance		±15			±15		V
Operating	±8		±22	±8		±22	V
Supply Current							
Quiescent		4	6		4	6	mA
PACKAGE OPTIONS[6]							
TO-100 Package (H-10A)		AD534SH			AD534TH		
TO-116 Package (D-14)		AD534SD			AD534TD		

NOTES

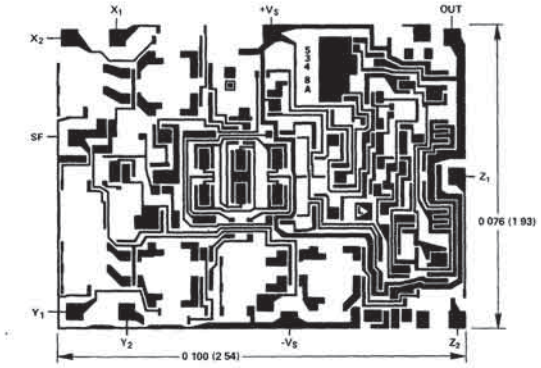
[1]Figures given are percent of full scale, ±10V (i.e., 0 01% = 1mV).
[2]May be reduced down to 3V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets
[4]Using external resistor adjusted to give SF = 3V.
[5]See functional block diagram for definition of sections
[6]See Section 16 for package outline information

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).



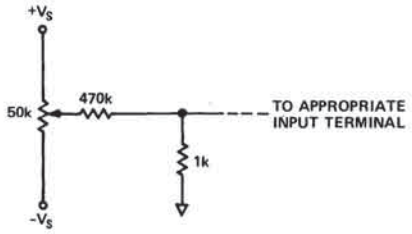
THE AD534 IS AVAILABLE IN LASER TRIMMED CHIP FORM, CONSULT THE CATALOG FOR DETAILS

ABSOLUTE MAXIMUM RATINGS

	AD534J, K, L	AD534S, T
Supply Voltage	±18V	±22V
Internal Power Dissipation	500mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0 to +70°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature, 60s soldering	+300°C	*

*Same as AD534J specs.

OPTIONAL TRIMMING CONFIGURATION



FUNCTIONAL DESCRIPTION

Figure 1 is a functional block diagram of the AD534. Inputs are converted to differential currents by three identical voltage-to-current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique. An on-chip "Buried Zener" provides a highly stable reference, which is laser trimmed to provide an overall scale factor of 10V. The difference between XY/SF and Z is then applied to the high gain output amplifier. This permits various closed loop configurations and dramatically reduces nonlinearities due to the input amplifiers, a dominant source of distortion in earlier designs. The effectiveness of the new scheme can be judged from the fact that under typical conditions as a multiplier the nonlinearity on the Y input, with X at full scale (±10V), is ±0.005% of F.S.; even at its worst point, which occurs when X = ±6.4V, it is typically only ±0.05% of F.S. Nonlinearity for signals applied to the X input, on the other hand, is determined almost entirely by the multiplier element and is parabolic in form. This error is a major factor in determining the overall accuracy of the unit and hence is closely related to the device grade.

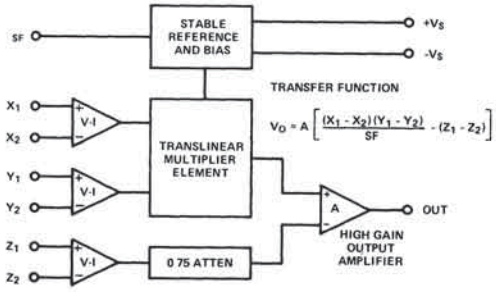


Figure 1. AD534 Functional Block Diagram

The generalized transfer function for the AD534 is given by:

$$V_{OUT} = A\left(\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right)$$

where A = open loop gain of output amplifier, typically 70dB at dc

X, Y, Z = input voltages (full scale = ±SF, peak= ±1.25SF)

SF = scale factor, pretrimmed to 10.00V but adjustable by the user down to 3V.

In most cases the open loop gain can be regarded as infinite, and SF will be 10V. The operation performed by the AD534, can then be described in terms of equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10V\,(Z_1 - Z_2)$$

The user may adjust SF for values between 10.00V and 3V by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\,\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF} by ±25% using the potentiometer. Considerable reduction in bias currents, noise and drift can be achieved by decreasing SF. This has the overall effect of increasing signal gain without the customary increase in noise. Note that the peak input signal is always limited to 1.25SF (i.e., ±5V for SF = 4V) so the overall transfer function will show a maximum gain of 1.25. The performance with small input signals, however, is improved by using a lower SF since the dynamic range of the inputs is now fully utilized. Bandwidth is unaffected by the use of this option.

Supply voltages of ±15V are generally assumed. However, satisfactory operation is possible down to ±8V (see curve 1). Since all inputs maintain a constant peak input capability of ±1.25SF some feedback attenuation will be necessary to achieve output voltage swings in excess of ±12V when using higher supply voltages.

OPERATION AS A MULTIPLIER

Figure 2 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

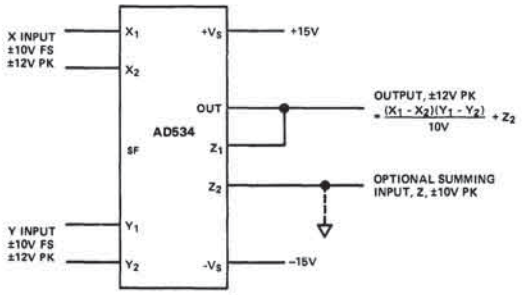


Figure 2. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input (see Optional Trimming Configuration, page 3). Curve 4 shows the typical ac feedthrough with this adjustment mode. Note that the Y input is a factor of 10 lower than the X input and should be used in applications where null suppression is critical.

The high impedance Z_2 terminal of the AD534 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective ground potentials to realize the full accuracy of the AD534.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 3. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F = 200pF. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications. Adjustment is made by connecting a 4.7MΩ resistor between Z_1 and the slider of a pot connected across the supplies to provide ±300mV of trim range at the output.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the high impedance Z_2 terminal where they are amplified by +10 or to the common ground connection where they are amplified by +1. Input signals may also be applied to the lower end of the 10kΩ resistor, giving a gain of -9. Other values of feedback ratio, up to X100, can be used to combine multiplication with gain.

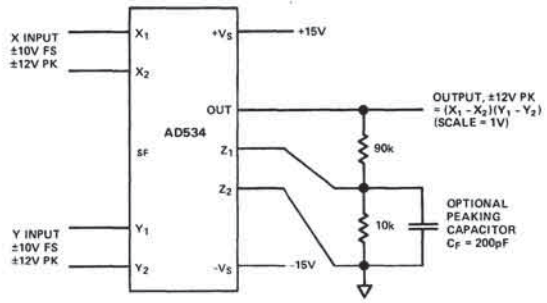


Figure 3. Connections for Scale-Factor of Unity

Occasionally it may be desirable to convert the output to a current, into a load of unspecified impedance or dc level. For example, the function of multiplication is sometimes followed by integration; if the output is in the form of a current, a simple capacitor will provide the integration function. Figure 4 shows how this can be achieved. This method can also be applied in squaring, dividing and square rooting modes by appropriate choice of terminals. This technique is used in the voltage-controlled low-pass filter and the differential-input voltage-to-frequency converter shown in the Applications Section.

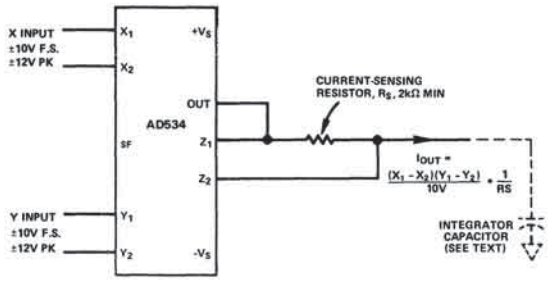


Figure 4. Conversion of Output to Current

OPERATION AS A SQUARER

Operation as a squarer is achieved in the same fashion as the multiplier except that the X and Y inputs are used in parallel. The differential inputs can be used to determine the output polarity (positive for $X_1 = Y_1$ and $X_2 = Y_2$, negative if either one of the inputs is reversed). Accuracy in the squaring mode is typically a factor of 2 better than in the multiplying mode, the largest errors occurring with small values of output for input below 1V.

If the application depends on accurate operation for inputs that are always less than ±3V, the use of a reduced value of SF is recommended as described in the FUNCTIONAL DESCRIPTION section (previous page). Alternatively, a feedback attenuator may be used to raise the output level. This is put to use in the difference-of-squares application to compensate for the factor of 2 loss involved in generating the sum term (see Figure 7).

The difference-of-squares function is also used as the basis for a novel rms-to-dc converter shown in Figure 14. The averaging filter is a true integrator, and the loop seeks to zero its input. For this to occur, $(V_{IN})^2 - (V_{OUT})^2 = 0$ (for signals whose period is well below the averaging time-constant). Hence V_{OUT} is forced to equal the rms value of V_{IN}. The absolute accuracy of this technique is very high; at medium frequencies, and for signals near full scale, it is determined almost entirely by the ratio of the resistors in the inverting amplifier. The multiplier scaling voltage affects only open loop gain. The data shown is typical of performance that can be achieved with an AD534K, but even using an AD534J, this technique can readily provide better than 1% accuracy over a wide frequency range, even for crest-factors in excess of 10.

OPERATION AS A DIVIDER

The AD535, a pin for pin functional equivalent to the AD534, has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications.

Figure 5 shows the connection required for division. Unlike earlier products, the AD534 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in curve 8.

Without additional trimming, the accuracy of the AD534K and L is sufficient to maintain a 1% error over a 10V to 1V denominator range. This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input (see Optional Trimming Configuration). To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2

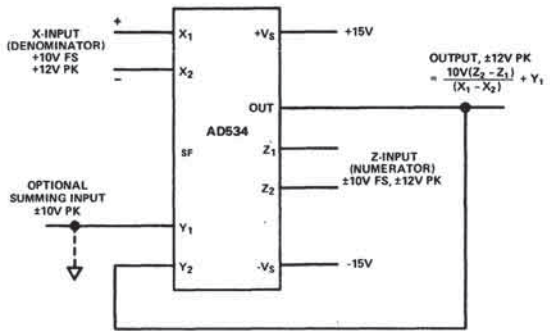


Figure 5. Basic Divider Connection

is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

As with the multiplier connection, overall gain can be introduced by inserting a simple attenuator between the output and Y_2 terminal. This option, and the differential-ratio capability of the AD534 are utilized in the percentage-computer application shown in Figure 11. This configuration generates an output proportional to the percentage deviation of one variable (A) with respect to a reference variable (B), with a scale of one volt per percent.

OPERATION AS A SQUARE ROOTER

The operation of the AD534 in the square root mode is shown in Figure 6. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs.

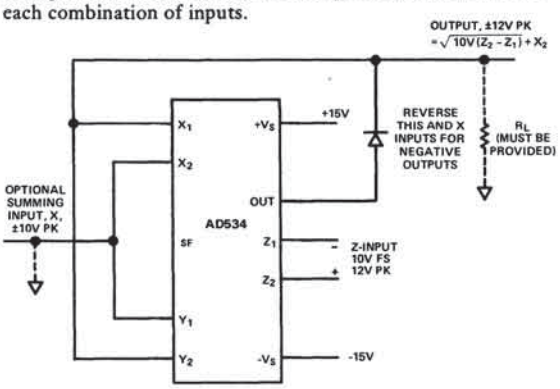


Figure 6. Square-Rooter Connection

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the AD534 is stable with all loads up to at least 1000pF. For critical applications, a small adjustment to the Z input offset (see Optional Trimming Configuration) will improve accuracy for inputs below 1V.

*See the AD535 Data Sheet for more details.

The versatility of the AD534 allows the creative designer to implement a variety of circuits such as wattmeters, frequency doublers and automatic gain controls to name but a few. These applications along with many other such "idea stimulators" are described in detail in the *Multiplier Application Guide*, available upon request from Analog Devices.

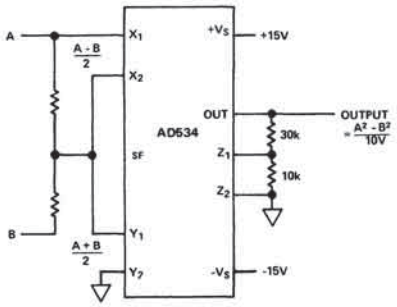
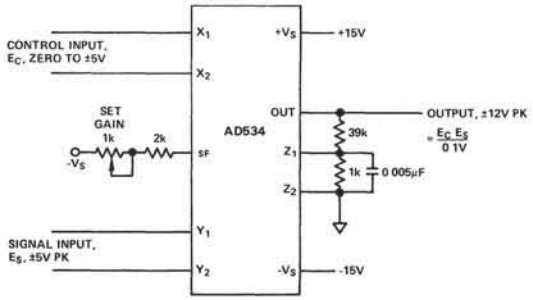
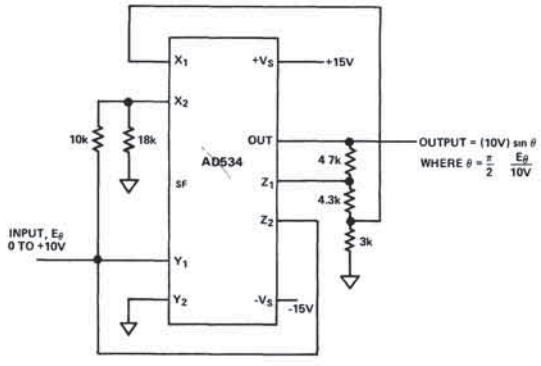


Figure 7. Difference-of-Squares



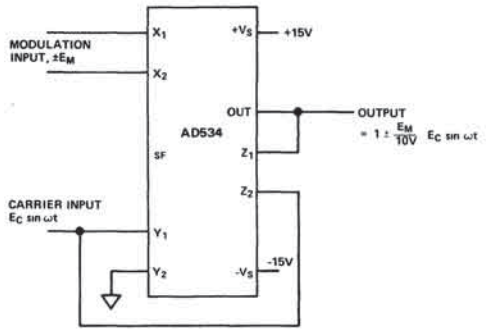
NOTES
1) GAIN IS X10 PER VOLT OF E_C, ZERO TO X50
2) WIDEBAND (10Hz – 30kHz) OUTPUT NOISE IS 3mV RMS, TYP CORRESPONDING TO A F S S/N RATIO OF 70dB
3) NOISE REFERRED TO SIGNAL INPUT, WITH E_C = ±5V, IS 60µV RMS, TYP
4) BANDWIDTH IS DC TO 20kHz, -3dB, INDEPENDENT OF GAIN

Figure 8. Voltage-Controlled Amplifier



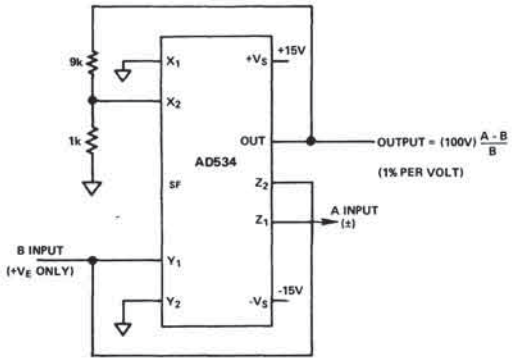
USING CLOSE TOLERANCE RESISTORS AND AD534L, ACCURACY OF FIT IS WITHIN ±0.5% AT ALL POINTS. θ IS IN RADIANS.

Figure 9. Sine-Function Generator



THE SF PIN OR A Z-ATTENUATOR CAN BE USED TO PROVIDE OVERALL SIGNAL AMPLIFICATION OPERATION FROM A SINGLE SUPPLY IS POSSIBLE, BIAS Y_2 TO $V_S/2$.

Figure 10. Linear AM Modulator



OTHER SCALES, FROM 10% PER VOLT TO 0.1% PER VOLT CAN BE OBTAINED BY ALTERING THE FEEDBACK RATIO

Figure 11. Percentage Computer

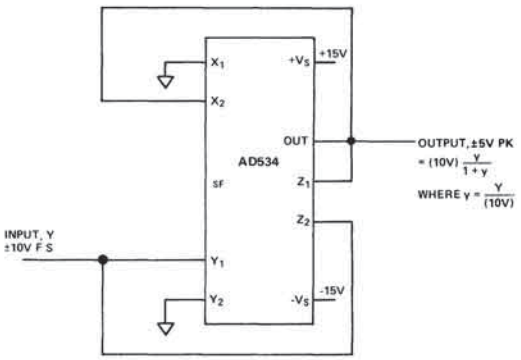
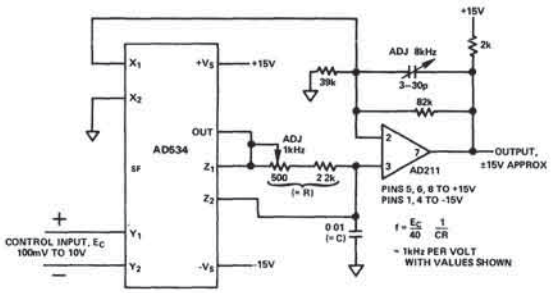


Figure 12. Bridge-Linearization Function



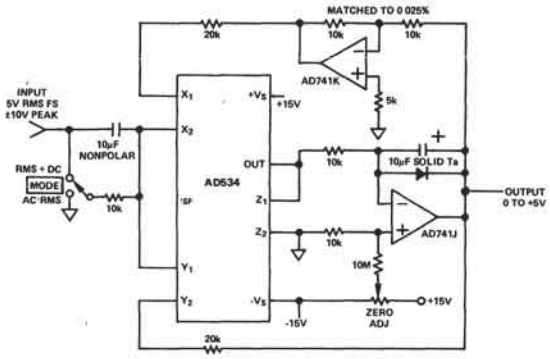
CALIBRATION PROCEDURE.

WITH E_C = 1.0V, ADJUST POT TO SET f = 1.000kHz. WITH E_C = 8.0V, ADJUST TRIMMER CAPACITOR TO SET f = 8.000kHz. LINEARITY WILL TYPICALLY BE WITHIN ±0.1% OF F.S. FOR ANY OTHER INPUT.

DUE TO DELAYS IN THE COMPARATOR, THIS TECHNIQUE IS NOT SUITABLE FOR MAXIMUM FREQUENCIES ABOVE 10kHz. FOR FREQUENCIES ABOVE 10kHz THE AD537 VOLTAGE TO FREQUENCY CONVERTER IS RECOMMENDED

A TRIANGLE-WAVE OF ±5V PK APPEARS ACROSS THE 0.01μF CAPACITOR; IF USED AS AN OUTPUT, A VOLTAGE-FOLLOWER SHOULD BE INTERPOSED.

Figure 13. Differential-Input Voltage-to-Frequency Converter



CALIBRATION PROCEDURE.

WITH 'MODE' SWITCH IN 'RMS + DC' POSITION, APPLY AN INPUT OF +1.00VDC. ADJUST ZERO UNTIL OUTPUT READS SAME AS INPUT. CHECK FOR INPUTS OF ±10V, OUTPUT SHOULD BE WITHIN ±0 05% (5mV)

ACCURACY IS MAINTAINED FROM 60Hz to 100kHz, AND IS TYPICALLY HIGH BY 0.5% AT 1MHz FOR V_{IN} = 4V RMS (SINE, SQUARE OR TRIANGULAR WAVE)

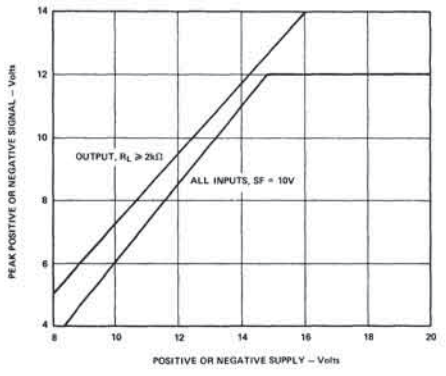
PROVIDED THAT THE PEAK INPUT IS NOT EXCEEDED, CREST-FACTORS UP TO AT LEAST TEN HAVE NO APPRECIABLE EFFECT ON ACCURACY.

INPUT IMPEDANCE IS ABOUT 10kΩ, FOR HIGH (10MΩ) IMPEDANCE, REMOVE MODE SWITCH AND INPUT COUPLING COMPONENTS.

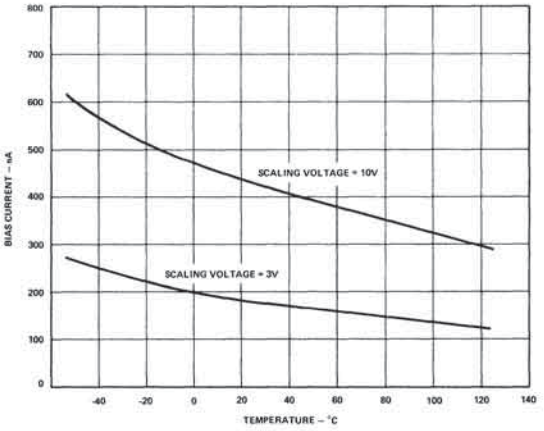
FOR GUARANTEED SPECIFICATIONS THE AD536A AND AD636 IS OFFERED AS A SINGLE PACKAGE RMS-TO-DC CONVERTER

Figure 14. Wideband, High-Crest Factor, RMS-to-DC Converter

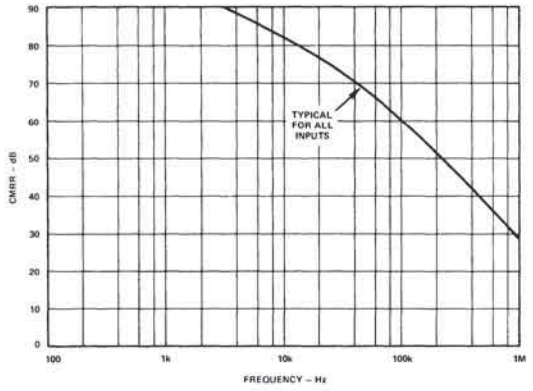
Typical Performance Curves (typical at +25°C, with V_S = ±15V dc, unless otherwise stated)



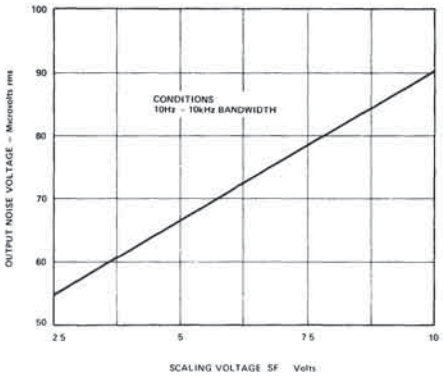
Curve 1. Input/Output Signal Range Vs. Supply Voltages



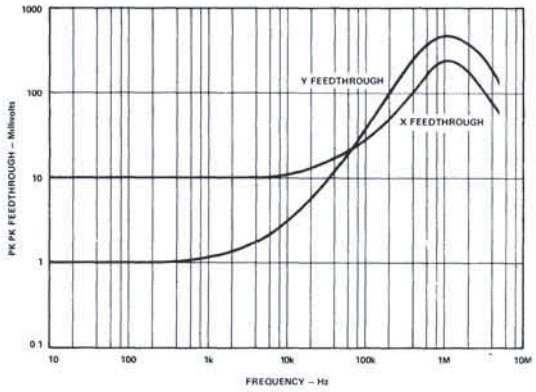
Curve 2. Bias Currents Vs. Temperature (X, Y or Z inputs)



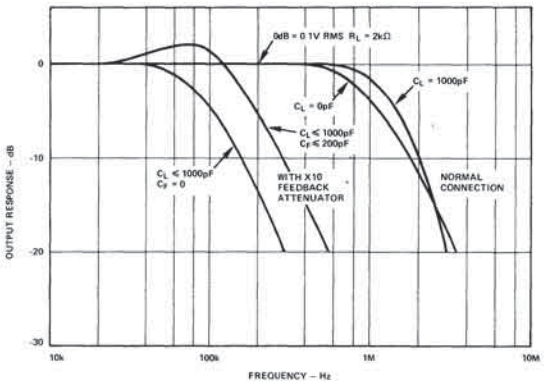
Curve 3. Common-Mode-Rejection-Ratio Vs. Frequency



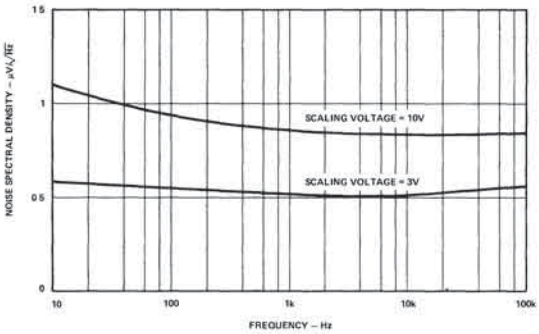
Curve 6. Wideband Noise Vs. Scaling Voltage



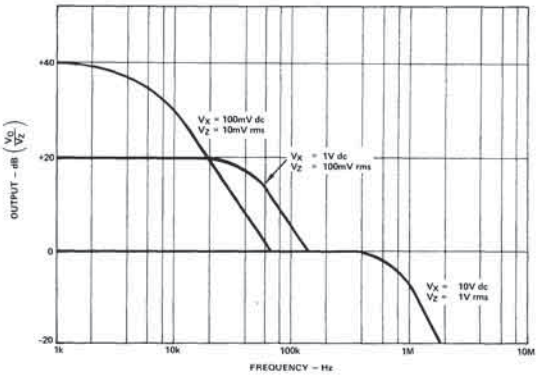
Curve 4. AC Feedthrough Vs. Frequency



Curve 7. Frequency Response as a Multiplier



Curve 5. Noise Spectral Density Vs. Frequency



Curve 8. Frequency Response Vs. Divider Denominator Input Voltage

Real-Time Analog Computational Unit (ACU)

AD538

FEATURES

$V_{OUT} = V_Y\left(\frac{V_Z}{V_X}\right)^m$ Transfer Function

Wide Dynamic Range (Denominator) −1000:1
Simultaneous Multiplication and Division
Resistor-Programmable Powers & Roots
No External Trims Required
Low Input Offsets <100μV
Low Error ±0.25% of Reading (100:1 Range)
+2V and +10V On-Chip References
Monolithic Construction

APPLICATIONS

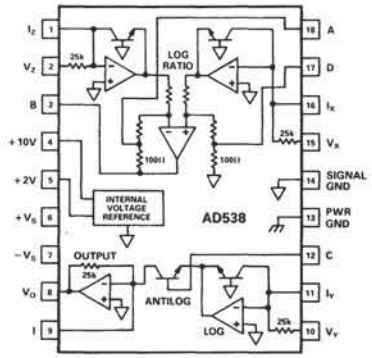
One- or Two-Quadrant Mult/Div
Log Ratio Computation
Squaring/Square Rooting
Trigonometric Function Approximations
Linearization Via Curve Fitting
Precision AGC
Power Functions

PRODUCT DESCRIPTION

The AD538 is a monolithic real-time computational circuit which provides precision analog multiplication, division and exponentiation. The combination of low input and output offset voltages and excellent linearity results in accurate computation over an unusually wide input dynamic range. Laser wafer trimming makes multiplication and division with errors as low as 0.25% of reading possible, while typical output offsets of 100μV or less add to the overall off-the-shelf performance level. Real-time analog signal processing is further enhanced by the device's 400kHz bandwidth.

The AD538's overall transfer function is $V_O = V_Y (V_Z/V_X)^m$. Programming a particular function is via pin strapping. No external components are required for one quadrant (positive input) multiplication and division. Two quadrant (bipolar numerator) division is possible with the use of external level shifting and scaling resistors. The desired scale factor for both multiplication and division can be set using the on-chip +2V or +10V references, or controlled externally to provide simultaneous multiplication and division. Exponentiation with an m value from 0.2 to 5 can be implemented with the addition of one or two external resistors.

AD538 FUNCTIONAL BLOCK DIAGRAM



Direct log ratio computation is possible by utilizing only the log ratio and output sections of the chip. Access to the multiple summing junctions adds further to the AD538's flexibility. Finally, a wide power supply range of ±4.5V to ±18V allows operation from standard ±5V, ±12V and ±15V supplies.

The AD538 is available in two accuracy grades (A and B) over the industrial (−25°C to +85°C) temperature range and one grade (S) over the military (−55°C to +125°C) temperature range. The device is packaged in an 18-pin TO-118 hermetic side-brazed ceramic DIP.

PRODUCT HIGHLIGHTS

1. Real-time analog multiplication, division and exponentiation.
2. High accuracy analog division with a wide input dynamic range.
3. On-chip +2V or +10V scaling reference voltages.
4. Both voltage and current (summing) input modes.
5. Monolithic construction with lower cost and higher reliability than hybrid and modular circuits.

6

SPECIFICATIONS (V_S = ±15V, T_A = 25°C unless otherwise specified)

Parameters	Conditions	AD538AD Min	AD538AD Typ	AD538AD Max	AD538BD Min	AD538BD Typ	AD538BD Max	AD538SD Min	AD538SD Typ	AD538SD Max	Units
MULTIPLIER/DIVIDER PERFORMANCE											
Nominal Transfer Function	$10V \geq V_X, V_Y, V_Z \geq 0$		$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$			$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$			$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$		
	$400\mu A \geq I_X, I_Y, I_Z \geq 0$		$V_O = 25k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$			$V_O = 25k\Omega \times I_Y\left(\frac{I_Z}{I_X}\right)^m$		
Total Error Terms	$100mV \leq V_X \leq 10V$		±0.5	**±1**		±0.25	**±0.5**		±0.5	**±1**	% of Reading +
100:1 Input Range[1]	$100mV \leq V_Y \leq 10V$		±200	**±500**		±100	**±250**		±200	**±500**	μV
	$100mV \leq V_Z \leq 10V$										
	$V_Z \leq 10 V_X$, m = 1.0										
	$T_A = T_{min}$ to T_{max}		±1	**±2**		±0.5	**±1**		±1.25	**±2.5**	% of Reading +
			±450	**±750**		±350	**±500**		±750	**±1000**	μV
Wide Dynamic Range[2]	$10mV \leq V_X \leq 10V$		±1	**±2**		±0.5	**±1**		±1	**±2**	% of Reading +
	$1mV \leq V_Y \leq 10V$		±200	**±500**		±100	**±250**		±200	**±500**	μV +
	$0V \leq V_Z \leq 10V$		±100	**±250**		±750	**±150**		±200	**±250**	$\mu V \times (V_Y + V_Z)/V_X$
	$V_Z \leq 10V_X$, m = 1.0										
	$T_A = T_{min}$ to T_{max}		±1.5	**±3**		±1	**±2**		±2	**±4**	% of Reading +
			±450	**±750**		±350	**±500**		±750	**±1000**	μV +
			±450	**±750**		±350	**±500**		±750	**±1000**	$\mu V \times (V_Y + V_Z)/V_X$
Exponent (m) Range	$T_A = T_{min}$ to T_{max}	0.2		5	0.2		5	0.2		5	
OUTPUT CHARACTERISTICS											
Offset Voltage	$V_Y = 0, V_C = -600mV$		±200	**±500**		±100	**±250**		±200	**±500**	μV
	$T_A = T_{min}$ to T_{max}		±450	**±750**		±350	**±500**		±750	**±1000**	μV
Output Voltage Swing	$R_L = 2k\Omega$	−11		**±11**	−11		**+11**	−11		**+11**	V
Output Current		5	10		5	10		5	10		mA
FREQUENCY RESPONSE											
Slew Rate			1.4			1.4			1.4		V/μs
Small Signal Bandwidth	$100mV \leq V_Y, V_Z, V_X \leq 10V$		400			400			400		kHz
VOLTAGE REFERENCE											
Accuracy	V_{REF} = 10V or 2V		±25	**±50**		±15	**±25**		±25	**±50**	mV
Additional Error	$T_A = T_{min}$ or T_{max}		±20	**±30**		±20	**±30**		±30	**±50**	mV
Output Current	V_{REF} = 10V to 2V	**1**	2.5		**1**	2.5		**1**	2.5		mA
Power Supply Rejection											
+2V = V_{REF}	$\pm 4.5V \leq V_S \leq \pm 18V$		300	**600**		300	**600**		300	**600**	μV/V
+10V = V_{REF}	$\pm 13V \leq V_S \leq \pm 18V$		200	**500**		200	**500**		200	**500**	μV/V
POWER SUPPLY											
Rated	$R_L = 2k\Omega$		±15			±15			±15		V
Operating Range[3]		**±4.5**		**±18**	**±4.5**		**±18**	**±4.5**		**±18**	V
PSRR	$\pm 4.5V < V_S < \pm 18V$		0.05	**0.1**		0.05	**0.1**		0.05	**0.1**	%/V
	$V_X = V_Y = V_Z = 1V$										
	V_{OUT} = 1V										
Quiescent Current			4.5	7		4.5	7		4.5	7	mA
TEMPERATURE RANGE											
Rated		−25		+85	−25		+85	−55		+125	°C
Storage		−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTIONS[4]											
Ceramic (D-18)			AD538AD			AD538BD			AD538SD		

NOTES

[1]Over the 100mV to 10V operating range total error is the sum of a percent of reading term and an output offset. With this input dynamic range the input offset contribution to total error is negligible compared to the percent of reading error. Thus, it is specified indirectly as a part of the percent of reading error.

[2]The most accurate representation of total error with low level inputs is the summation of a percent of reading term, an output offset and an input offset multiplied by the incremental gain $(V_Y + V_Z)/V_X$.

[3]When using supplies below ±13V the 10V reference pin *must* be connected to the 2V pin in order for the AD538 to operate correctly.

[4]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

RE-EXAMINATION OF MULTIPLIER/DIVIDER ACCURACY

Traditionally, the "accuracy" of (actually the errors of) analog multipliers and dividers have been specified in terms of percent of full scale. Thus specified, a 1% multiplier error with a 10V full scale output would mean a worst case error of +100mV at "any" level within its designated output range. While this type of error specification is easy to test, evaluate, and interpret, it can leave the user guessing as to how useful the multiplier actually is at low output levels, those approaching the specified error limit (in this case) 100mV.

The AD538's error sources do not follow the percent of full-scale approach to specification, thus it more optimally fits the needs of the very wide dynamic range applications for which it is best suited. Rather than as a percent of full scale, the AD538's error as a multiplier or divider for a 100:1 (100mV to 10V) input range is specified as the sum of two error components: a percent of reading (ideal output) term plus a fixed output offset. Following this format the AD538AD, operating as a multiplier or divider with inputs down to 100mV, has a maximum error of ±1% of reading ±500μV. Some sample total error calculations for both grades over the 100:1 input range are illustrated in the chart below. This error specification format is a familiar one to designers and users of digital voltmeters where error is specified as a percent of reading ± a certain number of digits on the meter readout.

For operation as a multiplier or divider over a wider dynamic range (>100:1), the AD538 has a more detailed error specification which is the sum of three components: a percent of reading term, an output offset term and an input offset term for the V_Y/V_X log ratio section. A sample application of this specification, taken from the chart below, for the AD538AD with V_Y = 1V, V_Z = 100mV and V_X = 10mV would yield a maximum error of ±2.0% of reading ±500μV ±(1V + 100mV)/10mV × 250μV or ±2.0% of reading ±500μV ± 27.5mV. This example illustrates that with very low level inputs the AD538's incremental gain $(V_Y + V_Z)/V_X$ has increased to make the input offset contribution to error substantial.

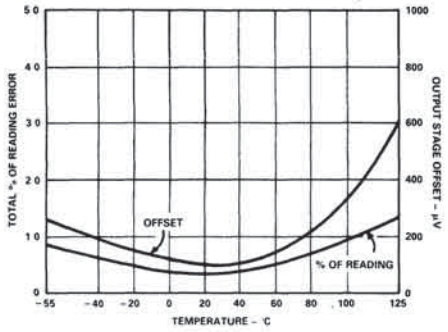
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AD538 SAMPLE ERROR CALCULATION CHART (worst case)

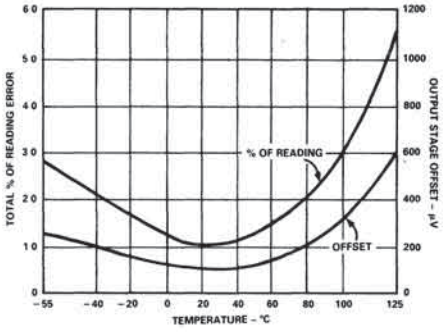
	V_Y Input (in V)	V_Z Input (in V)	V_X Input (in V)	Ideal Output (in V)	Total Offset Error Term (in mV)	% of Reading Error Term (in mV)	Total Error Summation (in mV)	Total Error Summation as a % of the Ideal Output
100:1 INPUT RANGE Total Error = ± % rdg ± Output V_{OS}	10	10	10	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
	10	0.1	0.1	10	0.5 (AD) 0.25 (BD)	100 (AD) 50 (BD)	100.5 (AD) 50.25 (BD)	1.0 (AD) 0.5 (BD)
	1	1	1	1	0.5 (AD) 0.25 (BD)	10 (AD) 5 (BD)	10.5 (AD) 5.25 (BD)	1.05 (AD) 0.5 (BD)
	0.1	0.1	0.1	0.1	0.5 (AD) 0.25 (BD)	1 (AD) 0.5 (BD)	1.5 (AD) 0.75 (BD)	1.5 (AD) 0.75 (BD)
WIDE DYNAMIC RANGE Total Error = ± % rdg ± Output V_{OS} ± Input V_{OS} × $(V_Y+V_Z)/V_X$	1	0.10	0.01	10	28 (AD) 16.75 (BD)	200 (AD) 100 (BD)	228 (AD) 116.75 (BD)	2.28 (AD) 1.17 (BD)
	10	0.05	2	0.25	1.76 (AD) 1 (BD)	5 (AD) 2.5 (BD)	6.76 (AD) 3.5 (BD)	2.7 (AD) 1.4 (BD)
	5	0.01	0.01	5	125.75 (AD) 75.4 (BD)	100 (AD) 50 (BD)	225.75 (AD) 125.4 (BD)	4.52 (AD) 2.51 (BD)
	10	0.01	0.1	1	25.53 (AD) 15.27 (BD)	20 (AD) 10 (BD)	45.53 (AD) 25.27 (BD)	4.55 (AD) 2.53 (BD)

ABSOLUTE MAXIMUM RATINGS

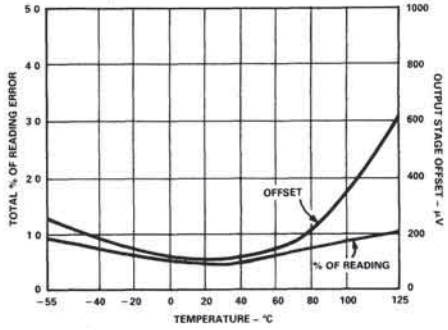
Supply Voltage . . . . . ±18V
Internal Power Dissipation 250mW
Output Short Circuit-to-Ground . . . . . Indefinite
Input Voltages V_X, V_Y, V_Z . . . . . $(+V_S-1V)$, −1V
Input Currents I_X, I_Y, I_Z, I_O 1mA
Operating Temperature Range . . . . . −25°C to +85°C
Storage Temperature Range . . . . . −65°C to +150°
Lead Temperature, Storage . . . . . 60 sec, +300°C



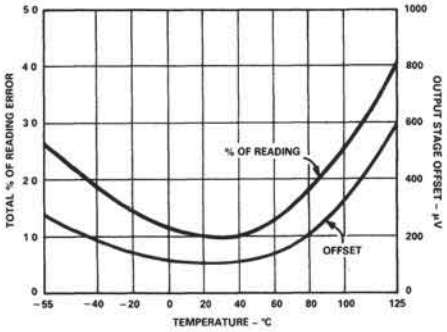
Multiplier Error vs. Temperature
($100mV < V_X, V_Y, V_Z \leq 10V$)



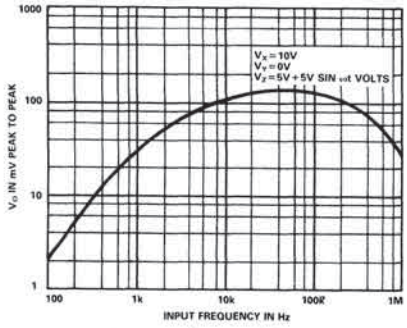
Multiplier Error vs. Temperature
($10mV < V_X, V_Y, V_Z \leq 100mV$)



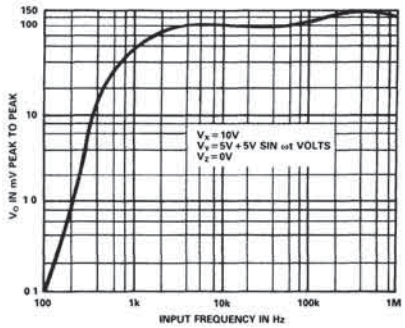
Divider Error vs. Temperature
($100mV < V_X, V_Y, V_Z \leq 10V$)



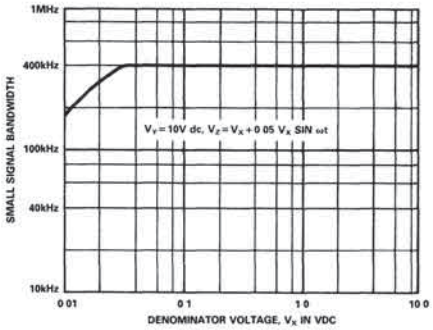
Divider Error vs. Temperature
($10mV \leq V_X, V_Y, V_Z \leq 100mV$)



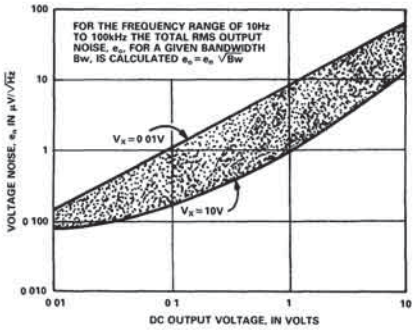
V_Z Feedthrough vs. Frequency



V_Y Feedthrough vs. Frequency



Small Signal Bandwidth vs Denominator Voltage
(One-Quadrant Mult/Div)



1kHz Output Noise Spectral Density vs. dc Output Voltage

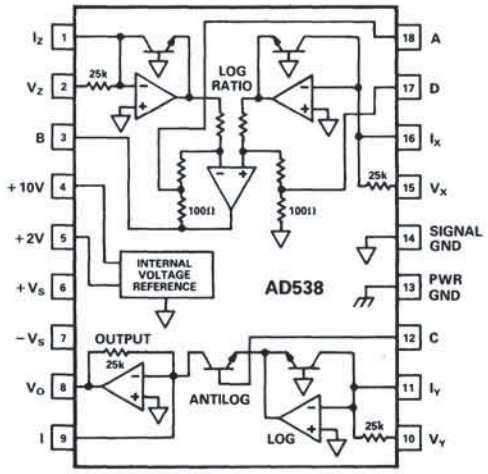


Figure 1. Functional Block Diagram

FUNCTIONAL DESCRIPTION

As shown in Figures 1 and 2, the V_Z and V_X inputs connect directly to the AD538's input log ratio amplifiers. This subsection provides an output voltage proportional to the natural log of input voltage V_Z, minus the natural log of input voltage V_X. The output of the log ratio subsection at B can be expressed by the transfer function:

$$V_B = \frac{kT}{q} \ln\left(\frac{V_Z}{V_X}\right)$$

(where $k = 1.3806 \times 10^{-23}$ J/K, $q = 1.6\ 0219 \times 10^{-19}$ C, T is in Kelvins)

The log ratio configuration may be used alone, if correctly temperature compensated and scaled to the desired output level (see Applications section).

Under normal operation, the log-ratio output will be connected directly to a second functional block at input C, the antilog subsection. This section performs the antilog according to the transfer function:

$$V_O = V_Y e^{\left(V_C \frac{q}{kT}\right)}$$

As with the log-ratio circuit included in the AD538, the user may use the antilog subsection by itself. When both subsections are combined, the output at B is tied to C, the transfer function of the AD538 computational unit is:

$$V_O = V_Y e^{\left[\left(\frac{kT}{q}\right)\left(\frac{q}{kT}\right)\ln\left(\frac{V_Z}{V_X}\right)\right]} \quad ; V_B = V_C$$

which reduces to:

$$V_O = V_Y\left(\frac{V_Z}{V_X}\right)$$

Finally, by increasing the gain or attenuating the output of the log ratio subsection via resistor programming, it is possible to raise the quantity V_Z/V_X to the m^{th} power. Without external programming, m is unity. Thus the overall AD538 transfer function equals:

$$V_O = V_Y\left(\frac{V_Z}{V_X}\right)^m$$

where $0.2 < m < 5$

When the AD538 is used as an analog divider, the V_Y input can be used to multiply the ratio V_Z/V_X by a convenient scale factor. The actual multiplication by the V_Y input signal is accomplished by adding the log of the V_Y input signal to the signal at C which is already in the log domain.

STABILITY PRECAUTIONS

At higher frequencies, the multi-staged signal path of the AD538, as illustrated in Figure 2, can result in large phase shifts. If a condition of high incremental gain exists along that path (e.g., $V_O = V_Y \times V_Z/V_X = 10V \times 10mV/10mV = 10V$ so that $\Delta V_O/\Delta V_X = 1000$), then small amounts of capacitive feedback from V_O to the current inputs I_Z or I_X can result in instability. Appropriate care should be exercised in board layout to prevent capacitive feedback mechanisms under these conditions.

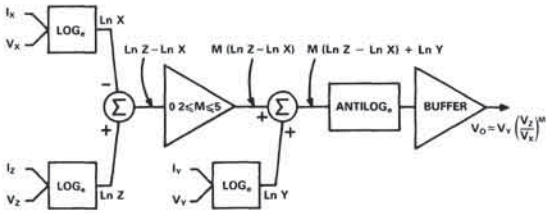


Figure 2. Model Circuit

USING THE VOLTAGE REFERENCES

A stable bandgap voltage reference for scaling is included in the AD538. It is laser-trimmed to provide a selectable voltage output of +10V buffered (Pin 4), +2V unbuffered (Pin 5) or any voltages between +2V and +10.2V buffered as shown in Figure 3. The output impedance at pin 5 is approximately 5kΩ. Note that any loading of this pin will produce an error in the +10V reference voltage. External loads on the +2V output should be greater than 500kΩ to maintain errors less than 1%.

In situations not requiring both reference levels, the +2V output can be converted to a buffered output by tying pins 4 and 5

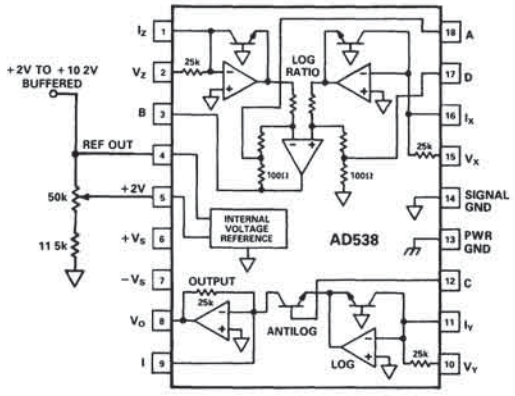


Figure 3. +2V to +10.2V Adjustable Reference

together. If both references are required simultaneously, the +10V output should be used directly and the +2V output should be externally buffered.

ONE-QUADRANT MULTIPLICATION/DIVISION

Figure 4 shows how the AD538 may be easily configured as a precision one-quadrant multiplier/divider. The transfer function $V_{OUT} = V_Y (V_Z/V_X)$ allows "three" independant input variables; a calculation not available with a conventional multiplier. In addition, the 1000:1 (i.e. 10mV to 10V) input dynamic range of the AD538 greatly exceeds that of analog multipliers computing one-quadrant multiplication and division.

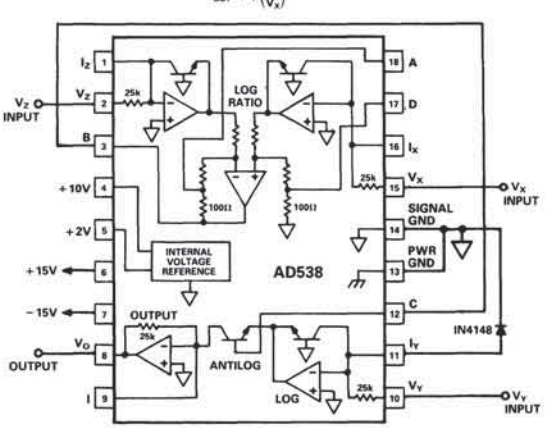


Figure 4. One-Quadrant Combination Multiplier/Divider

By simply connecting the input V_X (pin 15) to the +10V reference (pin 4), and tying the log-ratio output at B to the antilog input at C, the AD538 can be configured as a one-quadrant analog multiplier with 10 volt scaling. If 2 volt scaling is desired, V_X can be tied to the +2V reference.

When the input V_X is tied to the +10V reference terminal the multiplier transfer function becomes:

$$V_O = V_Y \left(\frac{V_Z}{10V}\right)$$

As a multiplier, this circuit provides a typical bandwidth of 400kHz with values of V_X, V_Y or V_Z varying over a 100:1 range (i.e. 100mV to 10V). The maximum error with a 100mV to 10V range for the two input variables will typically be +0.5% of reading. Using the optional Z offset trim scheme, as shown in Figure 5, this error can be reduced to +0.25% of reading.

By using the +10V reference as the V_Y input, the circuit of Figure 4 is configured as a one-quadrant divider with a fixed scale factor. As with the one-quadrant multiplier, the inputs accept only single (positive) polarity signals. The output of the one-quadrant divider with a +10V scale factor is:

$$V_O = 10V \left(\frac{V_Z}{V_X}\right)$$

The typical bandwidth of this circuit is 370kHz with 1V to 10V denominator input levels. At lower amplitudes, the bandwidth gradually decreases to approximately 200kHz at the 2mV input level.

TWO-QUADRANT DIVISION

The two-quadrant linear divider circuit illustrated in Figure 5 uses the same basic connections as the one-quadrant version. However, in this circuit the numerator has been offset in the positive direction by adding the denominator input voltage to it. The offsetting scheme changes the divider's transfer function from:

$$V_O = 10V \left(\frac{V_Z}{V_X}\right)$$

To:

$$V_O = 10V \frac{(V_Z + AV_X)}{V_X} = 10V \left(1A + \frac{V_Z}{V_X}\right)$$

$$= 10A + 10V \left(\frac{V_Z}{V_X}\right); \text{ where } A = \frac{35k\Omega}{25k\Omega}$$

As long as the magnitude of the denominator input is equal to or greater than the magnitude of the numerator input, the circuit will accept bipolar numerator voltages. However, under the conditions of a 0V numerator input, the output would incorrectly equal +14V. The offset can be removed by connecting the +10V reference through resistors R1 and R2 to the output section's summing node I at pin 9 thus providing a gain of 1.4 at the center of the trimpot. The pot R2 adjusts out or corrects this offset, leaving the desired transfer function of 10V (V_Z/V_X).

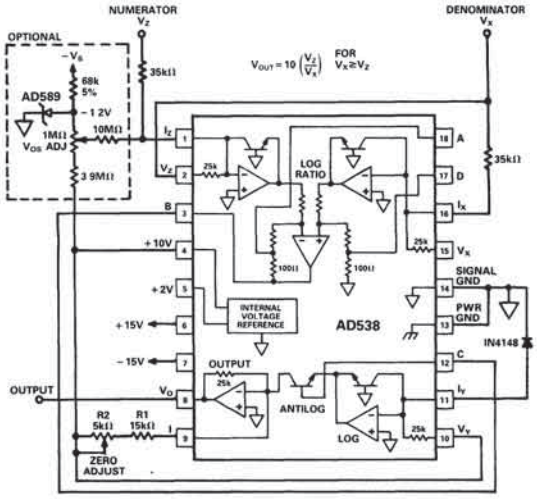


Figure 5. Two-Quadrant Division with 10V Scaling

LOG RATIO OPERATION

Figure 6 shows the AD538 configured for computing the log of the ratio of two input voltages (or currents). The output signal from B is connected to the summing junction of the output amplifier via two series resistors. The 90.9Ω metal film resistor effectively degrades the temperature coefficient of the ±3500ppm/°C resistor to produce a 1.09kΩ +3300ppm/°C equivalent value. In this configuration the V_Y input, must be tied to some voltage less than zero (−1.2V in this case) removing this input from the transfer function.

The 5kΩ potentiometer controls the circuit's scale factor adjustment providing a +1V per decade adjustment. The output offset potentiometer should be set to provide a zero output with $V_X = V_Z = 1V$. The input V_O adjustment should be set for an output of 3V with V_Z = 1mV and V_X = 1V.

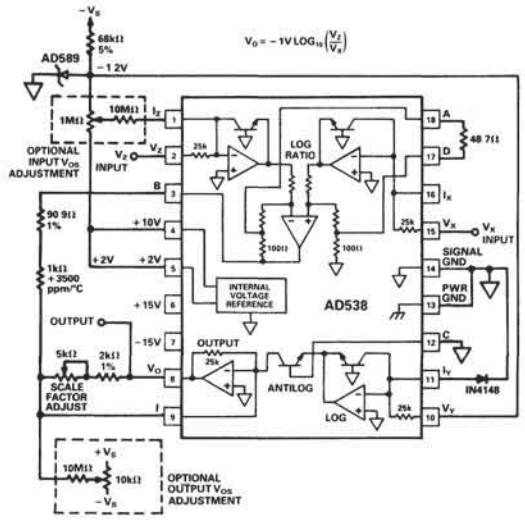


Figure 6. Log Ratio Circuit

The log ratio circuit shown achieves ±0.5% accuracy in the log domain for input voltages within three decades of input range: 10mV to 10V. This error is not defined as a percent of full-scale output, but as a percent of input. For example, using a 1V/decade scale factor, a 1% error in the positive direction at the INPUT of the log ratio amplifier translates into a 4.3mV deviation from the ideal OUTPUT (i.e., 1V × $\log_{10}$ (1.01) = 4.3214mV). An input error 1% in the negative direction is slightly different, giving an output deviation of 4.3648mV.

ANALOG COMPUTATION OF POWERS AND ROOTS

Often it is necessary to raise the quotient of two input signals to a power or take a root. This could be squaring, cubing, square-rooting or exponentiation to some noninteger power. Examples include power series generation. With the AD538, only one or two external resistors are required to set ANY desired power, over the range of 0.2 to 5. Raising the basic quantity V_Z/V_X to a power greater than one requires that the gain of the AD538's log ratio subtractor be increased, via an external resistor between pins A and D. Similarly, a voltage divider which attenuates the log ratio output between points B and C will program the power to a value less than one.

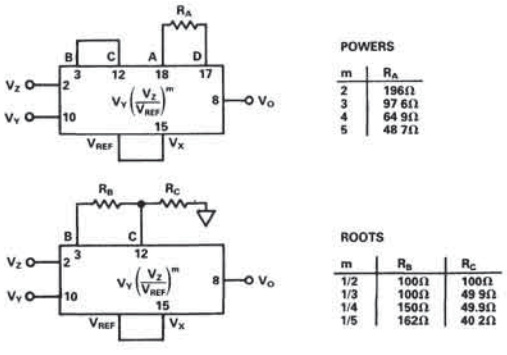


Figure 7. Basic Configurations and Transfer Functions for the AD538

SQUARE ROOT OPERATION

The explicit square root circuit of Figure 8 illustrates a precise method for performing a real time square root computation. For added flexibility and accuracy this circuit has a scale factor adjustment.

The actual square rooting operation is performed in this circuit by raising the quantity V_Z/V_X to the 1/2 power via the resistor divider network consisting of resistors R_B and R_C. For maximum linearity, the two resistors should be 1% (or better) ratio-matched metal film types.

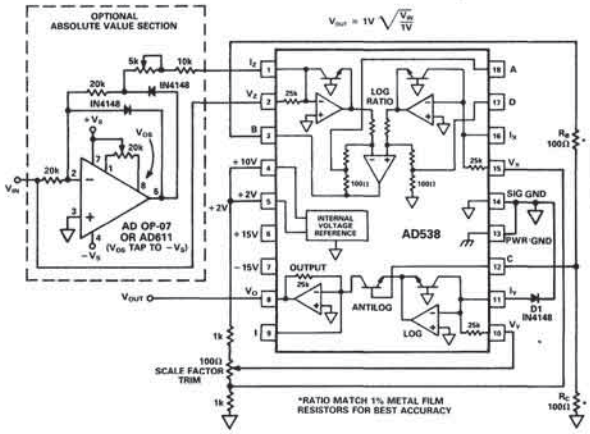


Figure 8. Square Root Circuit

One volt scaling is achieved by dividing-down the 2V reference and applying approximately 1V to both the V_Y and V_X inputs. In this circuit, the V_X input is intentionally set low, to about 0.95V, so that the V_Y input can be adjusted high; permitting a ±5% scale factor trim. Using this trim scheme, the output voltage will be within ±3mV ±0.2% of the ideal value over a 10V to 1mV input range (80dB). For a decreased input dynamic range of 10mV to 10V (60dB) the error is even less; here the output will be within ±2mV ±0.2% of the ideal value. The bandwidth of the AD538 square root circuit is approximately 280kHz with a 1V p-p sinewave with a +2V dc offset.

This basic circuit may also be used to compute the cube, fourth or fifth roots of an input waveform. All that is required for a given root is that the correct ratio of resistors, R_C and R_B, be selected such that their sum is between 150Ω and 200Ω.

The optional absolute value circuit shown preceding the AD538 allows the use of bipolar input voltages. Only one op-amp is required for the absolute value function, because the I_Z input of the AD538 functions as a summing junction. If it is necessary to preserve the sign of the input voltage, the polarity of the op-amp output may be sensed and used after the computation to switch the sign bit of a D.V.M. chip.

TRANSDUCER LINEARIZATION

Many electronic transducers used in scientific, commercial or industrial equipment monitor the physical properties of a device and/or its environment. Sensing (and perhaps compensating for) changes in pressure, temperature, moisture or other physical phenomenon can be an expensive undertaking, particularly where high accuracy and very low nonlinearity are important. In conventional analog systems accuracy may be easily increased by offset and scale factor trims, however, nonlinearity is usually the absolute limitation of the sensing device.

With the ability to easily program a complex analog function, the AD538 can effectively compensate for the nonlinearities of an inexpensive transducer. The AD538 can be connected between the transducer preamplifier output and the next stage of monitoring or transmitting circuitry. The recommended procedure for linearizing a particular transducer is first to find the closest function which best approximates the nonlinearity of the device and then, to select the appropriate exponent resistor value(s).

ARC-TANGENT APPROXIMATION

The circuit of Figure 9 is typical of those AD538 applications where the quantity V_Z/V_X is raised to powers greater than one. In an approximate arc-tangent function, the AD538 will accurately compute the angle that is defined by X and Y displacements represented by input voltages V_X and V_Z. With accuracy to within one degree (for input voltages between 100μV and 10 volts), the AD538 arc-tangent circuit is more precise than conventional analog circuits and is faster than most digital techniques. For a direct arc-tangent computation that requires fewer external components refer to the AD639 data sheet. The circuit shown is set-up for the transfer function:

$$V_\theta = (V_{\theta ref} - V_\theta)\left[\frac{(V_Z)}{(V_X)}\right]^{1.21}$$

$$\text{Where } \theta = \text{Tan}^{-1}\left(\frac{Z}{X}\right)$$

The $(V_{\theta ref} - V_\theta)$ function is implemented in this circuit by adding together the output, V_θ, and an externally applied reference voltage, $V_{\theta ref}$, via an external AD547 op-amp. The 1μF capacitor

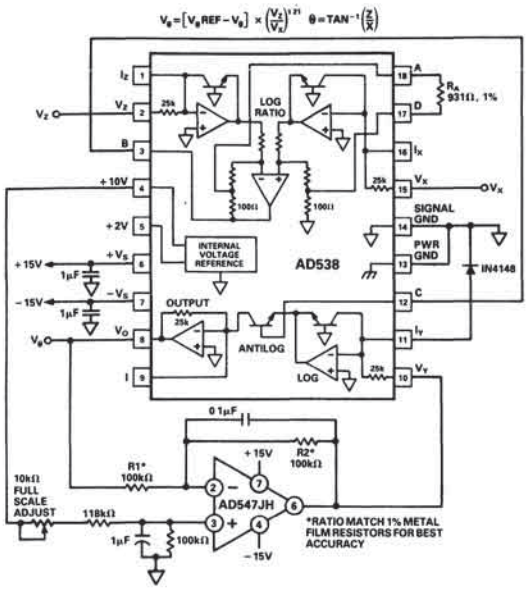


Figure 9. The Arc-Tangent Function

connected around the AD547's 100kΩ feedback resistor frequency compensates the loop (formed by the amplifier between V_θ and V_Y).

The V_B/V_A quantity is calculated in the same manner as in the one-quadrant divider circuit, except that the resulting quotient is raised to the 1.21 power. Resistor R_A (nominally 931Ω) sets the power or m factor.

For the highest arc-tangent accuracy the external resistors R1 and R2 should be ratio matched, however, the offset trim scheme shown in other circuits is not required, since nonlinearity effects are the predominant source of error. Also note, that instability will occur as the output approaches 90° because, by definition, the arc-tangent function is infinite and therefore, the AD538's gain will be extremely high.

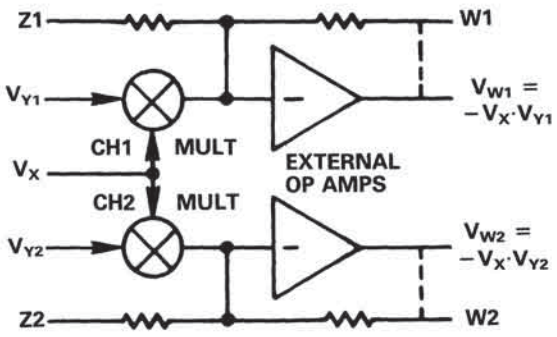
Wideband Dual-Channel Linear Multiplier/Divider

AD539

FEATURES
Two Quadrant Multiplication/Division
Two Independent Signal Channels
Signal Bandwidth of 60MHz (I_{OUT})
Linear Control Channel Bandwidth of 5MHz
Low Distortion (to 0.01%)
Fully-Calibrated, Monolithic Circuit

APPLICATIONS
Precise High Bandwidth AGC and VCA Systems
Voltage-Controlled Filters
Video-Signal Processing
High-Speed Analog Division
Automatic Signal-Leveling
Square-Law Gain/Loss Control

AD539 FUNCTIONAL BLOCK DIAGRAM



6

PRODUCT DESCRIPTION

The AD539 is a low-distortion analog multiplier having two identical signal channels (Y1 and Y2), with a common X-input providing linear control of gain. Excellent ac characteristics up to video frequencies and a 3dB bandwidth of over 60MHz are provided. Although intended primarily for applications where speed is important the circuit exhibits good static accuracy in "computational" applications. Scaling is accurately determined by a band-gap voltage referehce and all critical parameters are laser-trimmed during manufacture.

The full bandwidth can be realized over most of the gain range using the AD539 with simple resistive loads of up to 100Ω. Output voltage is restricted to a few hundred millivolts under these conditions. Using external op amps such as the AD5539 in conjunction with the on-chip scaling resistors, accurate multiplication can be achieved, with bandwidths typically as high as 50MHz.

The two channels provide flexibility. In single-channel applications they may be used in parallel, to double the output current, or in series, to achieve a square-law gain function with a control range of over 100dB, or differentially, to reduce distortion. Alternatively, they may be used independently, as in audio stereo applications, with low crosstalk between channels. Voltage-controlled filters and oscillators using the "state-variable" approach are easily designed, taking advantage of the dual channels and common control. The AD539 can also be configured as a divider with signal bandwidths up to 15MHz.

Power consumption is only 135mW using the recommended ±5V supplies. The AD539 is available in three versions: the "J" and "K" grades are specified for 0 to +70°C operation and "S" grade is guaranteed over the extended range of −55°C to +125°C. The J and K grades are available in either a hermetic ceramic DIP (D) or a low cost plastic DIP (N), while the S grade is available only in ceramic.

DUAL SIGNAL CHANNELS

The signal voltage inputs, V_{Y1} and V_{Y2}, have nominal full-scale (FS) values of ±2V with a peak range to ±4.2V (using a negative supply of 7.5V or greater). For video applications where differential phase is critical a reduced input range of ±1 volt is recommended, resulting in a phase variation of typically ±0.2° at 3.579MHz for full gain. The input impedance is typically 400kΩ shunted by 3pF. Signal channel distortion is typically well under 0.1% at 10kHz and can be reduced to 0.01% by using the channels differentially.

COMMON CONTROL CHANNEL

The control channel accepts positive inputs, V_X, from 0 to +3V FS, ±3.3V peak. The input resistance is 500Ω. An external, grounded capacitor determines the small-signal bandwidth and recovery time of the control amplifier; the minimum value of 3nF allows a bandwidth at mid-gain of about 5MHz. Larger compensation capacitors slow the control channel but improve the high-frequency performance of the signal channels.

FLEXIBLE SCALING

Using either one or two external op amps in conjunction with the on-chip 6kΩ scaling resistors, the output currents (nominally ±1mA FS, ±2.25mA peak) can be converted to voltages with accurate transfer functions of $V_W = -V_X V_Y/2$, $V_W = -V_X V_Y$ or $V_W = -2V_X V_Y$ (where inputs V_X and V_Y and output V_W are expressed in volts), with corresponding full-scale outputs of ±3V, ±6V and ±12V. Alternatively, low-impedance grounded loads can be used to achieve the full signal bandwidth of 60MHz, in which mode the scaling is less accurate.

SPECIFICATIONS ($@ T_A = 25°C$, $V_S = \pm 5V$, unless otherwise specified)

Parameter	Conditions	AD539J Min	AD539J Typ	AD539J Max	AD539K Min	AD539K Typ	AD539K Max	AD539S Min	AD539S Typ	AD539S Max	Units
SIGNAL-CHANNEL DYNAMICS											
Minimal Configuration	Reference Figure 6a										
Bandwidth, −3dB	$R_L = 50\Omega$, $C_C = 0.01\mu F$	30	60		30	60		30	60		MHz
Maximum Output	$+0.1V < V_X < +3V$, $V_{Yac} = 1V$ rms		−10			−10			−10		dBm
Feedthrough, f<1MHz	$V_X = 0$, $V_{Yac} = 1.5V$ rms		−75			−75			−75		dBm
f = 20MHz			−55			−55			−55		dBm
Differential Phase Linearity											
$-1V < V_Y dc < +1V$	f = 3 58MHz, $V_X = +3V$,		±0 2			±0.2			±0.2		Degrees
$-2V < V_Y dc < +2V$	$V_{Yac} = 100mV$		±0.5			±0.5			±0.5		Degrees
Group Delay	$V_X = +3V$, $V_{Yac} = 1V$ rms, f = 1MHz		4			4			4		ns
Standard Dual-Channel Multiplier	Reference Figure 2										
Maximum Output	$V_X = +3V$, $V_{Yac} = 1.5V$ rms		4.5			4.5			4.5		V
Feedthrough, f<100kHz	$V_X = 0$, $V_{Yac} = 1.5V$ rms		1			1			1		mV rms
Crosstalk (CH1 to CH2)	$V_{Y1} = 1V$ rms, $V_{Y2} = 0$										
	$V_X = +3V$, f<100kHz		−40			−40			−40		dB
RTO Noise, 10Hz to 1MHz	$V_X = +1.5V$, $V_Y = 0$, Figure 2		200			200			200		$nV/\sqrt{Hz}$
THD + Noise, $V_X = +1V$,	f = 10kHz, $V_{Yac} = 1V$ rms		0.02			0.02			0.02		%
$V_Y = +3V$	f = 10kHz, $V_{Yac} = 1V$ rms		0.04			0.04			0.04		%
Wide Band Two-Channel Multiplier	Figure 2										
Bandwidth, −3dB (LH0032)	$+0.1V < V_X < +3V$, $V_{Yac} = 1V$ rms		25			25			25		MHz
Maximum Output $V_X = +3V$	$V_{Yac} = 1.5V$ rms, f = 3MHz		4.5			4.5			4.5		V rms
Feedthrough $V_X = 0V$	$V_{Yac} = 1.0V$ rms, f = 3MHz		14			14			14		mV rms
Wide Band Single Channel VCA											
(AD5539)	Reference Figure 8										
Bandwidth, −3dB	$+0.1V < V_X < +3V$, $V_{Yac} = 1V$ rms		50			50			50		MHz
Maximum Output	75Ω Load		±1			±1			±1		V
Feedthrough	$V_X = -0.01$, f = 5MHz		−54			−54			−54		dB
CONTROL CHANNEL DYNAMICS											
Bandwidth, −3dB	$C_C = 3000pF$, $V_X dc = +1.5V$,										
	$V_X ac = 100mV$ rms		5			5			5		MHz
SIGNAL INPUTS, V_{Y1} & V_{Y2}											
Nominal Full-Scale Input			±2			±2			±2		V
Operational Range, Degraded Performance	$-V_S > 7V$	±4.2			±4.2			±4.2			V
Input Resistance			400			400			400		kΩ
Bias Current			10	30		10	20		10	30	μA
Offset Voltage	$V_X = +3V$, $V_Y = 0$		5	20		5	10		5	20	mV
(T_{min} to T_{max})			10			5			15	35	mV
Power Supply Sensitivity	$V_X = +3V$, $V_Y = 0$		2			2			2		mV/V
CONTROL INPUT, V_X											
Nominal Full-Scale Input			+3.0			+3.0			+3.0		V
Operational Range, Degraded Performance		+3.2			+3.2			+3.2			V
Input Resistance[1]			500			500			500		Ω
Offset Voltage			1	4		1	2		1	4	mV
(T_{min} to T_{max})			3			2			2	5	mV
Power Supply Sensitivity			30			30			30		μV/V
Gain	(Figure 2)										
Absolute Gain Error	$V_X = +0.1V$ to $+3\ 0V$ and		0.2	0.4		0 1	0.2		0 2	0.4	dB
(T_{min} to T_{max})	$V_y = \pm 2V$		0.3			0.15			0.25	0.5	dB
CURRENT OUTPUT[1]											
Full-Scale Output Current	$V_X = +3V$, $V_Y = \pm 2V$		±1			±1			±1		mA
Peak Output Current	$V_X = +3.3V$, $V_Y = \pm 5V$, $V_S = \pm 7.5V$	±2	±2.8		±2	±2.8		±2	±2 8		mA
Output Offset Current	$V_X = 0$, $V_Y = 0$		0.2	1.5		0.2	1.5		0.2	1.5	μA
Output Offset Voltage[2]	Figure 2, $V_X = 0$, $V_Y = 0$		3	10		3	10		3	10	mV
Output Resistance[1]			1.2			1.2			1.2		kΩ
Scaling Resistors											
CH1	Z1, W1 to CH1		6			6			6		kΩ
CH2	Z2, W2 to CH2		6			6			6		kΩ
VOLTAGE OUTPUTS, V_{W1} & V_{W2}[2]	(Figure 2)										
Multiplier Transfer Function,			$V_W = -V_X V_Y/V_U$			$V_W = -V_X V_Y/V_U$			$V_W = -V_X V_Y/V_U$		
Either Channel											
Multiplier Scaling Voltage, V_U		0.98	1 0	1.02	0.99	1.0	1.01	0.98	1.0	1.02	V
Accuracy			0 5	2		0.5	1		0.5	2	%
(T_{min} to T_{max})			1			0.5			1.0	3	%
Power Supply Sensitivity			0 04			0.04			0.04		%/V
Total Multiplication Error[3]	$V_X <= +3V$, $-2V < V_Y < 2V$		1	2.5		0.6	1.5		1	2.5	% FSR
T_{min} to T_{max}			2			1			2	4	%
Control Feedthrough	$V_X = 0$ to $+3V$, $V_Y = 0$		25	60		15	30		15	60	mV
T_{min} to T_{max}			30			15			60	120	mV
TEMPERATURE RANGE											
Rated Performance		0		+70	0		+70	−55		+125	°C
POWER SUPPLIES											
Operational Range		±4.5		±16.5	±4 5		±16.5	±4 5		±16.5	V
Current Consumption											
$+V_S$			8.5	10.2		8.5	10.2		8.5	10.2	mA
$-V_S$			18.5	22.2		18 5	22.2		18.5	22.2	mA
PACKAGE OPTIONS[4]											
Plastic (N-16)			AD539JN			AD539KN					
TO-116 (D-16)			AD539JD			AD539KD			AD539SD		

NOTES

[1]Resistance value and absolute current outputs subject to 20% tolerance

[2]Spec assumes the external op amp is trimmed for negligible input offset

[3]Includes all errors

[4]See Section 16 for package outline information.

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

CIRCUIT DESCRIPTION

Figure 1 is a simplified schematic of the AD539. Q1-Q6 are large-geometry transistors designed for low distortion and low noise. Emitter-area scaling further reduces distortion: Q1 is 3 times larger than Q2; Q4, Q5 are each 3 times larger than Q3, Q6, and these transistors are twice as large as Q1, Q2. A stable reference current I_{REF} = 1.375mA is produced by a band-gap reference circuit and applied to the common emitter node of a *controlled-cascode* formed by Q1 and Q2. When V_X = 0, all of I_{REF} flows in Q1, due to the action of the high-gain control amplifier which lowers the voltage on the base of Q2. As V_X is raised the fraction of I_{REF} flowing in Q2 is forced to balance the control current, V_X/2.5k. At the full-scale value of V_X (+3V) this fraction is 0.873. Since the bases of Q1, Q4 and Q5 are at ground potential and the bases of Q2, Q3 and Q6 are commoned, all three controlled-cascodes divide the current applied to their emitter nodes in the same proportion. The control loop is stabilized by the external capacitor, C_C.

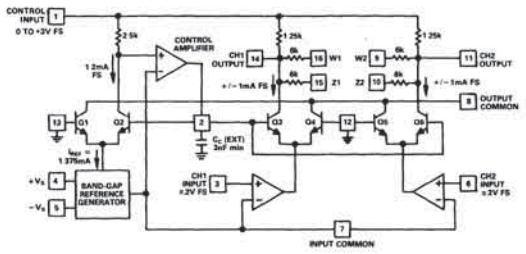


Figure 1. Simplified Schematic of AD539 Multiplier

The signal voltages V_{Y1} and V_{Y2} (generically referred to as V_Y) are first converted to currents by voltage-to-current converters with a g_m of 575μmhos; thus, the full-scale input of ±2V becomes a current of ±1.15mA, which is superimposed on a bias of 2.75mA, and applied to the common emitter node of controlled cascode Q3-Q4 or Q5-Q6. As just explained, the proportion of this current steered to the output node is linearly dependent on V_X. Thus for full-scale V_X and V_Y inputs, a signal of ±1mA (0.873 × ±1.15mA) and a bias component of 2.4mA (0.873 × 2.75mA) appear at the output. The bias component absorbed by the 1.25k resistors also connected to V_X, and the resulting signal current can be applied to an external load resistor (in which case scaling is not accurate) or can be forced into either or both of the 6kΩ feedback resistors (to the Z and W nodes) by an external op amp. In the latter case, scaling accuracy is guaranteed.

GENERAL RECOMMENDATIONS

The AD539 is a high speed circuit and requires considerable care to achieve its full performance potential. A high-quality ground plane should be used with the device either soldered directly into the board or mounted in a low-profile socket. In the figures used here an open triangle denotes a *direct, short* connection to this ground plane; pins 12 and 13 are especially prone to unwanted signal pick-up. Power supply decoupling capacitors of 0.1μF to 1μF should be connected from pins 4 and 5 to the ground plane. In applications using external high-speed op amps, separate supply decoupling should be used. It is good practice to insert small (10Ω) resistors between the primary supply and the decoupling capacitor.

The control amplifier compensation capacitor, C_C, should likewise have short leads to ground and a minimum value of 3nF. Unless maximum control bandwidth is esssential it is advisable to use a larger value of 0.01μF to 0.1μF to improve the signal channel phase response, high-frequency crosstalk and high-frequency distortion. The control bandwidth is inversely proportional to this capacitance, typically 2MHz for C_C = 0.01μF, V_X = 1.7V. The bandwidth and pulse response of the control channel can be improved by using a feedforward capacitor of 5% to 20% the value of C_C between pins 1 and 2. Optimum transient response will result when the rise/fall time of V_X are commensurate with the control-channel response time.

V_X should not exceed the specified range of 0 to +3V. The ac gain is zero for V_x<0 but there remains a feedforward path (see Figure 1) causing control feedthrough. Recovery time from negative values of V_X can be improved by adding a small-signal Schottky diode with its cathode connected to pin 2 and its anode grounded. This constrains the voltage swing on C_C. Above V_X = +3.2V, the ac gain limits at its maximum value, but any overdrive appears as control feedthrough at the output.

The power supplies to the AD539 can be as low as ±4.5V and as high as ±16.5V. The maximum allowable range of the signal inputs, V_Y, is approximately 0.5V above $+V_S$; the minimum value is 2.5V above $-V_S$. To accommodate the peak specified inputs of ±4.2V the supplies should be nominally +5V and −7.5V. While there is no performance advantage in raising supplies above these values, it may often be convenient to use the same supplies as for the op amps. The AD539 can tolerate the excess voltage with only a slight effect on dc accuracy but dissipation at ±16.5V can be as high as 535mW and some form of heat-sink is essential in the interests of reliability.

TRANSFER FUNCTION

In using any analog multiplier or divider careful attention must be paid to the matter of *scaling*, particularly in computational applications. To be *dimensionally consistent* a scaling voltage must appear in the transfer function, which, for each channel of the AD539 in the standard multiplier configuration (Figure 2) is

$$V_W = -V_X V_Y / V_U$$

where the inputs V_X and V_Y, the output V_W and the scaling voltage V_U are expressed in a consistent unit, usually volts. In this case, V_U is fixed by the design to be 1V and it is often acceptable in the interest of simplification to use the less rigorous expression

$$V_W = -V_X V_Y$$

where it is understood that *all signals must be expressed in volts*, that is, they are rendered dimensionless by division by (1V).

The accuracy specifications for V_U allow the use of either of the two feedback resistors supplied with each channel, since these are very closely matched, or they may be used in parallel to half the gain (double the effective scaling voltage), when

$$V_W = -V_X V_Y/2.$$

When an external load resistor, R_L, is used the scaling is no longer exact since the internal thin-film resistors, while trimmed to high *ratiometric* accuracy, have an absolute tolerance of 20%. However, the nominal transfer function is

$$V_W = -V_X V_Y/V_U'$$

where the effective scaling voltage, V_U' can be calculated for each channel using the formula $V_U' = V_U(5R_L + 6.25)/R_L$, where R_L is expressed in kilohms. For example, when R_L = 100Ω, V_U' = 67.5V. Table II provides more detailed data for the case where both channels are used in parallel. The AD539 can also be used with no external load (output pin 11 or 14 open-circuit), when V_U' is quite accurately 5V.

BASIC MULTIPLIER CONNECTIONS

Figure 2 shows the connections for the standard two-channel multiplier, using op amps to provide useful output power and the AD539 feedback resistors to achieve accurate scaling. The transfer function for each channel is

$$V_W = -V_X V_Y$$

where inputs and outputs are expressed in volts (see TRANSFER FUNCTION). At the nominal full-scale inputs of V_X = +3V, V_Y = ±2V the full-scale outputs are ±6V. Depending on the choice of op amp, their supply voltages usually need to be about 2V more than the peak output. Thus, supplies of at least ±8V are required; the AD539 can share these supplies. Higher outputs are possible if V_X and V_Y are driven to their peak values of +3.2V and ±4.2V respectively, when the peak output is ±13.4V. This requires operating the op amps at supplies of ±15V. Under these conditions it is advisable to reduce the supplies to the AD539 to ±7.5V to limit its power dissipation; however, with some form of heat sinking it is permissible to operate the AD539 directly from ±15V supplies.

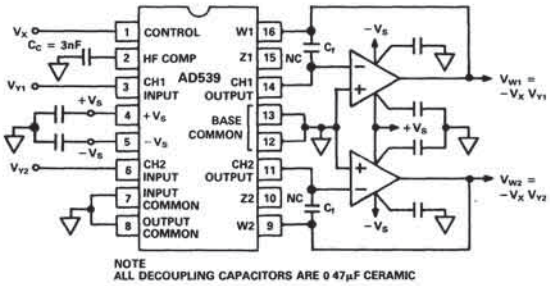


Figure 2. Standard Dual-Channel Multiplier

Viewed as a voltage-controlled amplifier, the decibel gain is simply

$$G = 20 \log V_X$$

where V_X is expressed in volts. This results in a gain of 10dB at V_X = +3.162V, 0dB at V_X = +1V, −20dB at V_X = +0.1V, and so on. In many ac applications the output offset voltage (for V_X = 0 or V_Y = 0) will not be of major concern; however, it can be eliminated using the offset nulling method recommended for the particular op amp, with $V_X = V_Y = 0$.

At small values of V_X the offset voltage of the control channel will degrade the gain/loss accuracy. For example, a ±1mV offset uncertainty will cause the nominal 40dB attenuation at V_X = +0.01V to range from 39.2dB to 40.9dB. Figure 3a shows the maximum gain error boundaries based on the guaranteed control-channel offset voltages of ±2mV for the AD539K and ±4mV for the AD539J. These curves include all scaling errors and apply to all configurations using the internal feedback resistors (W1 and W2; alternatively, Z1 and Z2).

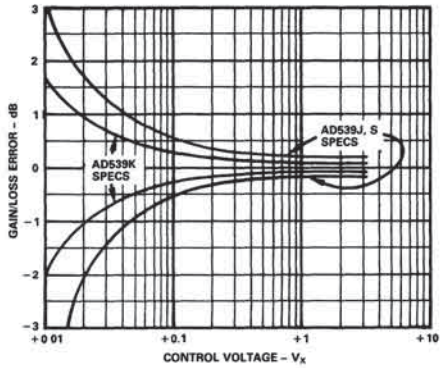


Figure 3a. Maximum ac Gain Error Boundaries

Distortion is a function of the signal input level (V_Y) and the control input (V_X). It is also a function of frequency, although in practice the op amp will generate most of the distortion at frequencies above 100kHz. Figure 3b shows typical results at f = 10kHz as a function of V_X with V_Y = 0.5 and 1.5V rms.

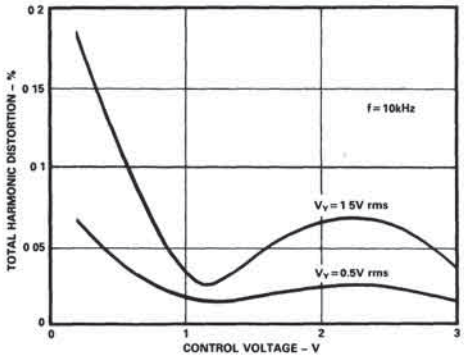


Figure 3b. Total Harmonic Distortion vs. Control Voltage

In some cases it may be desirable to alter the scaling. This can be achieved in several ways. One option is to use both the Z and W feedback resistors (see Figure 1) in parallel, in which case $V_W = -V_X V_Y/2$. This may be preferable where the output swing must be held at ±3V FS (±6.75V pk), for example, to allow the use of reduced supply voltages for the op amps. Alternatively, the gain can be doubled by connecting both channels in parallel and using only a single feedback resistor, in which case $V_W = -2V_X Y_Y$ and the full-scale output is ±12V. Another option is to insert a resistor in series with the control-channel input, permitting the use of a large (for example, 0 to +10V) control voltage. A disadvantage of this scheme is the need to

adjust this resistor to accommodate the tolerance of the nominal 500Ω input resistance at pin 1. The signal channel inputs can also be resistively attenuated to permit operation at higher values of V_Y, in which case it may often be possible to partially compensate for the response roll-off of the op amp by adding a capacitor across the upper arm of this attenuator.

Signal-Channel ac and Transient Response

The HF response is dependent almost entirely on the op amp. Note that the "noise gain" for the op amp in Figure 2 is determined by the value of the feedback resistor (6kΩ) and the 1.25kΩ control-bias resistors (Figure 1). Op amps with provision for external frequency compensation (such as the AD301 and AD518) should be compensated for a closed-loop gain of 6.

The layout of the circuit components is very important if low feedthrough and flat response at low values of V_X is to be maintained (see GENERAL RECOMMENDATIONS).

For wide-bandwidth applications requiring an output voltage swing greater than ±1V, the ADLH0032 hybrid op-amp is recommended. Figure 4a shows the HF response of the circuit of Figure 2 using this amplifier with V_Y = 1V rms and other conditions as shown in Table I. C_F was adjusted for 1dB peaking at V_X = +1V; the −3dB bandwidth exceeds 25MHz. The effect of signal feedthrough on the response becomes apparent at V_X = +0.01V. The minimum feedthrough results when V_X is taken slightly negative to ensure that the residual control-channel offset is exceeded and the dc gain is reliably zero. Measurements show that the feedthrough can be held to −90dB relative to full

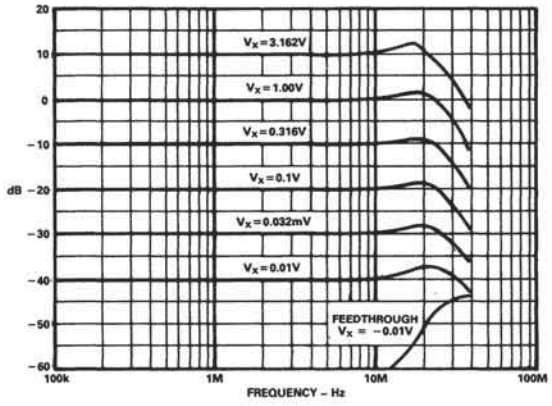
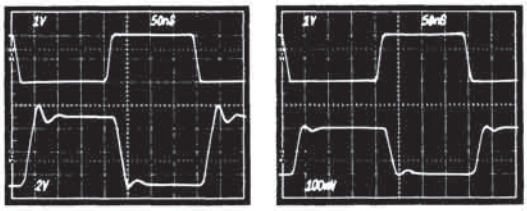


Figure 4a. Multiplier HF Response Using ADLH0032 Op Amps

output at low frequencies and to −60dB up to 20MHz with careful board layout. The corresponding pulse response is shown in Figure 4b for a signal input of V_Y of ±1V and two values of V_X (+3V and +0.1V).



V_X = +3V V_X = +0.1V

Figure 4b. Multiplier Pulse Response Using ADLH0032 Op Amps

	AD711[1]	AD5539[2]	ADLH0032[1]
Op Amp Supply Voltages	±15V	±9V	±10V
Op Amp Compensation Capacitor	None	None	1-5pF
Feedback Capacitor, C_F	None	0.25-1.5pF	1-4pF
−3dB Bandwidth, V_X = +1V	900kHz	50MHz	25MHz
Load Capacitance	<1nF	<10pF	<100pF
HF Feedthrough, V_X = −0.01V, f = 5MHz	N/A	−54dB	−70dB
rms Output Noise, V_X = +1V, BW 10Hz-10kHz	50μV	40μV	30μV
V_X = +1V, BW 10Hz-5MHz	120μV	620μV	500μV

In all cases, 0.47μF ceramic supply-decoupling capacitors were used at each IC pin, the AD539 supplies were ±5V and the control-compensation capacitor C_C was 3nF.

NOTES
[1]For the circuit of Figure 2. [2]For the circuit of Figure 8.

Table I. Summary of Operating Conditions and Performance for the AD539 When Used with Various External Op-Amp Output Amplifiers

Minimal Wide-Band Configurations

The maximum bandwidth can be achieved using the AD539 with simple resistive loads to convert the output currents to voltages. These currents (nominally ±1mA FS, ±2.25mA pk, into short-circuit loads) are shunted by their source resistance of 1.25kΩ (each channel). Calculations of load power and effective scaling-voltage must allow for this shunting effect when using resistive loads. The output power is quite low in this mode, and the device behaves more like a voltage-controlled attenuator than a classical multiplier. The matching of gain and phase between the two channels is excellent. From dc to 10MHz the gains are typically within ±0.025dB (measured using precision 50Ω load resistors) and the phase difference within ±0.1°.

Load Resistance	50Ω	75Ω	100Ω	150Ω	600Ω	O/C
FS Output Voltage	±92.6mV 65.5mV rms	±134mV 94.7mV rms	±172mV 122mV rms	±242mV 171mV rms	±612mV 433mV rms	±1V *
FS Output-Power in Load	0.086mW −10.5dBm	0.12mW −9.2dBm	0.15mW −8.3dBm	0.195mW −7.1dBm	0.312mW −5.05dBm	– –
Pk Output Voltage	±210mV 148mV rms	±300mV 212mV rms	±388mV 274mV rms	±544mV 385mV rms	±1V *	±1V *
Pk Output-Power in Load	0.44mW −7dBm	0.6mW −4.4dBm	0.75mW −2.5dBm	1mW 0dBm	±1V *	±1V *
Effective Scaling Voltage, V_U'	67.5V	46.7V	36.3V	25.8V	10.2V	5V

*Peak negative voltage swing limited by output compliance

Table II. Summary of Performance for Minimal Configuration

For a given load resistance the output power can be quadrupled by using both channels in parallel, as shown in Figure 5a. The small-signal silicon diode D connected between ground and pins 12 and 13 provides extra voltage compliance at the output nodes in the negative direction (to −1V at 25°C); it is not required if the output swing does not exceed −300mV. Table II compares performance for various load resistances, using this configuration.

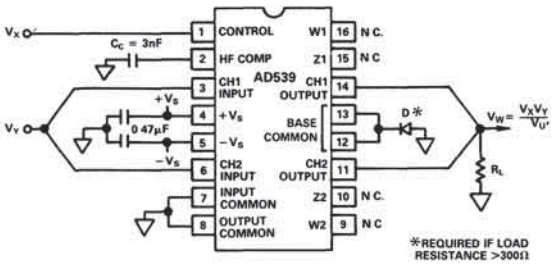


Figure 5a. Minimal Single-Channel Multiplier

Figure 5b shows the HF response for Figure 5a with the AD539 in a carefully-shielded 50Ω test-environment; the test system response was first characterized and this background removed by digital signal processing to show the inherent circuit response.

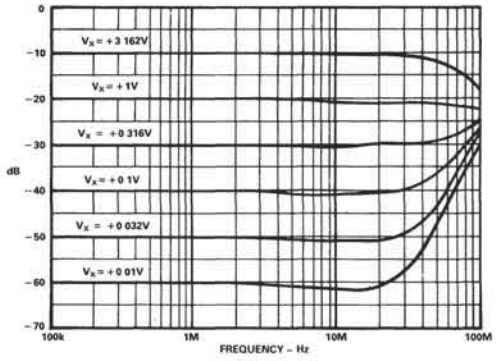


Figure 5b. HF Response in Minimal Configuration

In many applications *phase linearity* over frequency is important. Figure 5c shows the deviation from an ideal linear-phase response for a typical AD539 over the frequency range dc to 10MHz, for

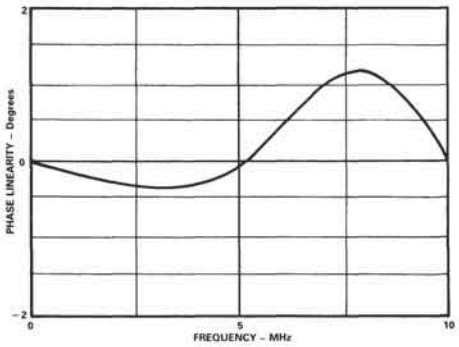


Figure 5c. Phase Linearity Error in Minimal Configuration

V_X = +3V; the peak deviation is slightly more than 1°. *Differential phase linearity* (the stability of phase over the signal window at a fixed frequency) is shown in Figure 5d for f = 3.579MHz and various values of V_X. The most rapid variation occurs for V_Y above +1V; in applications where this characteristic is critical, it is recommended that a ground-referenced, negative-going signal be used.

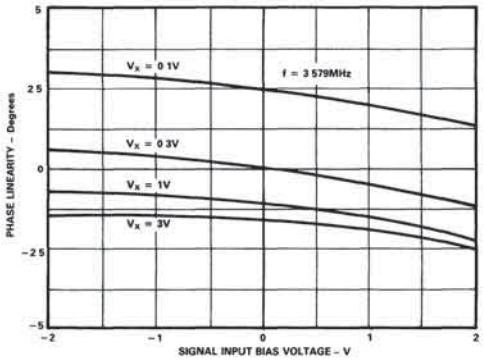


Figure 5d. Differential Phase Linearity in Minimal Configuration for a Typical Device

Differential Configurations

When only one signal channel must be handled it is often advantageous to use the channels differentially. By subtracting the CH1 and CH2 outputs any residual transient control feedthrough is virtually eliminated. Figure 6a shows a minimal configuration where it is assumed that the host system uses differential signals and a 50Ω environment throughout. This figure also shows a recommended control-feedforward network to improve large-signal

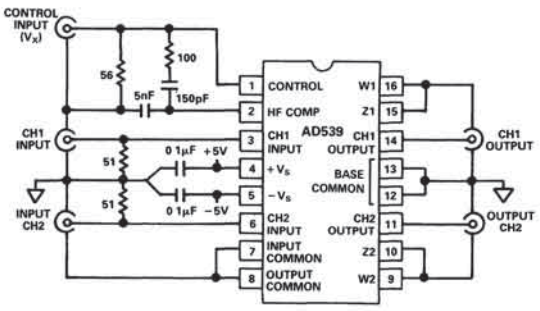


Figure 6a. High-Speed Differential Configuration

response time. The control feedthrough glitch is shown in Figure 6b, where the input was applied to CH1 and only the output of CH1 was displayed on the oscilloscope. The improvement obtained when CH1 and CH2 outputs are viewed differentially is clear in Figure 6c. The envelope rise-time is of the order of 40ns.

Lower distortion results when CH1 and CH2 are driven by *complementary* inputs and the outputs are utilized differentially, using a circuit such as Figure 7a. Resistors R1 and R2 should have a value in the range 100 to 1000Ω.

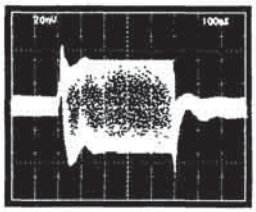


Figure 6b. Control Feedthrough One Channel of Figure 6a

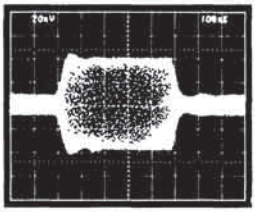


Figure 6c. Control Feedthrough Differential Mode, Figure 6a

They minimize a secondary distortion mechanism caused by a collector-modulation effect in the controlled cascodes (see CIRCUIT DESCRIPTION) by keeping the voltage-swing at the outputs to an acceptable level. Figure 7b shows the improvement in distortion over the standard configuration (compare Figure 3b). Note that the Z nodes (pins 10 and 15) are returned to the control input; this prevents the early onset of output-transistor saturation.

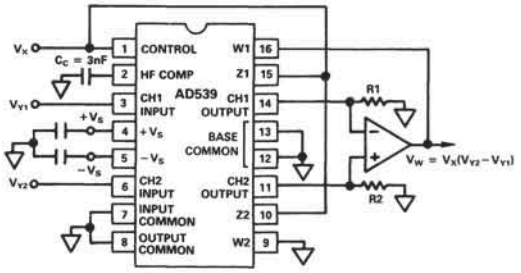


Figure 7a. Low-Distortion Differential Configuration

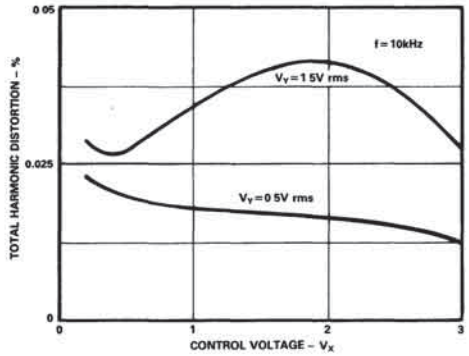


Figure 7b. Distortion in Differential Mode Using ADLH0032 Op-Amp

Even lower distortion (0.01%, or −80dB) has been measured using two output op amps in a configuration similar to Figure 2 connected as virtual-ground current-summers (to prevent the modulation effect). Note that to generate the difference output it is merely necessary to connect the output of the CH1 op amp to the Z node of CH2. In this way, the net input to the CH2 op amp is the difference signal, and the low-distortion resultant appears as its output.

A 50MHz VOLTAGE-CONTROLLED AMPLIFIER

Figure 8 is a circuit for a 50MHz voltage-controlled amplifier (VCA) suitable for use in high-quality-video-speed applications. The outputs from the two-signal channels of the AD539 are applied to the op-amp in a subtracting configuration. This connection has two main advantages: first, it results in better rejection of the control voltage, particularly when over-driven (V_X<0 or V_X>3.3V). Secondly, it provides a choice of either non-inverting or inverting responses, using either inputs V_{Y1} or V_{Y2} respectively. In this circuit, the output of the op-amp will equal:

$$V_{OUT} = \frac{V_X (V_{Y1} - V_{Y2})}{2V} \text{ for } V_X > 0$$

Hence, the gain is unity at $V_X = +2V$. Since V_X can over-range to +3.3V, the maximum gain in this configuration is about 4.3dB. (Note: If pin 9 of the AD539 is grounded, rather than connected to the output of the 5539N, the maximum gain becomes 10dB.)

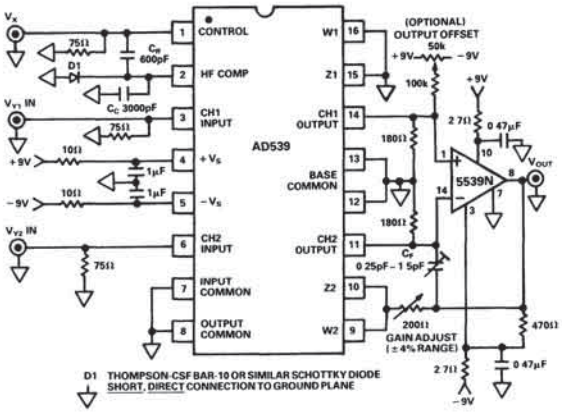


Figure 8. A Wide Bandwidth Voltage-Controlled Amplifier

The −3dB bandwidth of this circuit is over 50MHz at full gain, and is not substantially affected at lower gains. Of course, when V_X is zero (or slightly negative, to override the residual input offset) there is still a small amount of capacitive feedthrough at high frequencies; therefore, *extreme* care is needed in laying out the PC board to minimize this effect. Also, for small values of V_X, the combination of this feedthrough with the multiplier output can cause a dip in the response where they are out of phase. Figure 9a shows the ac response from the noninverting

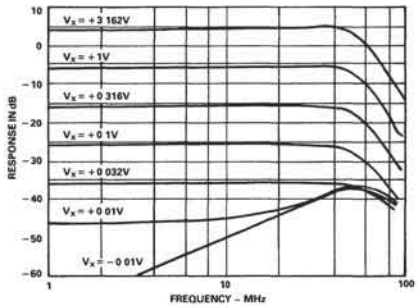


Figure 9a. AC Response of the VCA at Different Gains V_Y=0.5V RMS

input, with the response from the inverting input, V_{Y2}, essentially identical. Test conditions: $V_{Y1} = 0.5V$ rms for values of V_X from $+10mV$ to $+3.16V$; this is with a 75Ω load on the output. The feedthrough at $V_X = -10mV$ is also shown.

The transient response of the signal channel at $V_X = +2V$, $V_Y = V_{OUT} = \pm 1V$ is shown in Figure 9b; with the VCA driving a 75Ω load. The rise and fall-times are approximately 7ns.

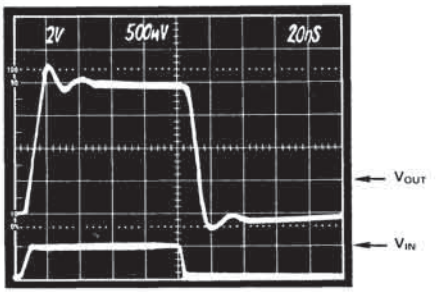


Figure 9b. Transient Response of the Voltage-Controlled Amplifier $V_X = +2$ Volts $V_Y = \pm 1$ Volt

A more detailed description of this circuit, including differential gain and phase characteristics, is given in the application note "Low Cost, Two Chip Voltage-Controlled Amplifier and Video Switch" available from Analog Devices.

BASIC DIVIDER CONNECTIONS

Standard Scaling

The AD539 provides excellent operation as a two-quadrant analog divider in wide-band wide gain-range applications, with the advantage of dual-channel operation. Figure 10a shows the simplest connections for division with a transfer function of

$$V_Y = -V_U V_W / V_X$$

Recalling that the nominal value of V_U is 1V, this can be simplified to

$$V_Y = -V_W / V_X$$

where all signals are expressed in volts. The circuit thus exhibits unity gain for $V_X = +1V$ and a gain of 40dB when $V_X = +0.01V$.

The output swing is limited to $\pm 2V$ nominal full-scale and $\pm 4.2V$ peak (using a $-V_S$ supply of at least 7.5V for the AD539). Since the maximum *loss* is 10dB (at $V_X = 3.162V$), it follows that the maximum input to V_W should be $\pm 6.3V$ (4.4V rms) for low distortion applications, and no more than $\pm 13.4V$ (9.5V rms) to avoid clipping. Note that offset adjustment will be needed

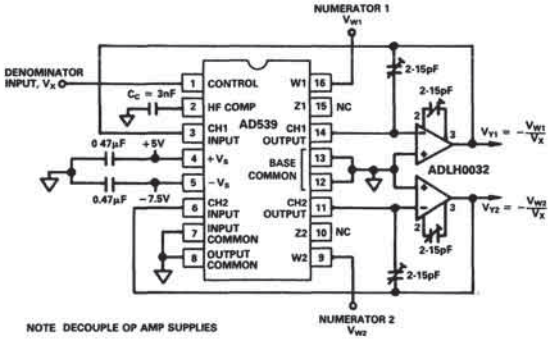


Figure 10a. Two-Channel Divider with 1V Scaling

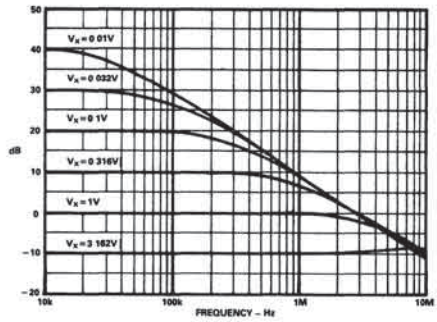


Figure 10b. HF Response of Figure 10a Divider

for the op amps to maintain accurate dc levels at the output in high gain applications: the "noise gain" is $6V/V_X$, or 600 at $V_X = +0.01V$.

The gain-magnitude response for this configuration using the ADLH0032 op amps with nominally 12pF compensation (pins 2 to 3) and $C_F = 7pF$ is shown in Figure 10b; of course, other amplifiers may also be used. Since there is some manufacturing variation in the HF response of the op amps, and load conditions will also affect the response, these capacitors should be adjustable: 5-15pF is recommended for both positions. The bandwidth in this configuration is nominally 17MHz at $V_X = +3.162V$, 4.5MHz at $V_X = +1V$, 350kHz at $V_X = +0.1V$ and 35kHz at $V_X = +0.01V$. The general recommendations regarding the use of a good ground plane and power-supply decoupling should be carefully observed.

Internally Trimmed Precision I.C. Multiplier

AD632

FEATURES

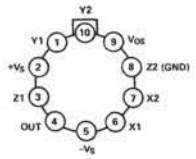
Pretrimmed to ±0.5% Max 4-Quadrant Error
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1-X_2)(Y_1-Y_2)/10]+Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X10 Gain
Low Noise Design: 90μV rms, 10Hz-10kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

APPLICATIONS

High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Accurate Voltage Controlled Oscillators and Filters

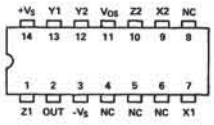
AD632 PIN CONFIGURATIONS

H-Package TO-100



TOP VIEW

D-Package TO-116



TOP VIEW

6

PRODUCT DESCRIPTION

The AD632 is an internally-trimmed monolithic four-quadrant multiplier/divider. The AD632B has a maximum multiplying error of ±0.5% without external trims.

Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried zener reference preserve accuracy even under adverse conditions. The simplicity and flexibility of use provide an attractive alternative approach to the solution of complex control functions.

The AD632 is pin for pin compatible with the industry standard AD532 with improved specifications and a fully differential high impedance Z-input. The AD632 is capable of providing gains of up to X10, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD632 can be effectively employed as a variable gain differential input amplifier with high common mode rejection. The effectiveness of the variable gain capability is enhanced by the inherent low noise of the AD632: 90μV rms.

PRODUCT HIGHLIGHTS

Guaranteed Performance Over Temperature: The AD632A and AD632B are specified for maximum multiplying errors of ±1.0% and ±0.5% of full scale, respectively at +25°C and are rated for operation from −25°C to +85°C. Maximum multiplying errors of ±2.0% (AD632S) and ±1.0% (AD632T) are guaranteed over the extended temperature range of −55°C to +125°C.

High Reliability: The AD632S and AD632T series are also available with MIL-STD-883 Level B screening and all devices are available in either the hermetically-sealed TO-100 metal can or TO-116 ceramic DIP package.

SPECIFICATIONS (@ +25°C, $V_S = \pm 15V$, $R \geq 2k\Omega$ unless otherwise noted)

Model	AD632A Min	AD632A Typ	AD632A Max	AD632B Min	AD632B Typ	AD632B Max	AD632S Min	AD632S Typ	AD632S Max	AD632T Min	AD632T Typ	AD632T Max	Units
MULTIPLIER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10V}+Z_2$		
Total Error[1] ($-10V \leq X, Y \leq +10V$)			**±1.0**			**±0.5**			**±1.0**			**±0.5**	%
T_A = min to max		**±1.5**			**±1.0**			**±2.0**			**±1.0**		%
Total Error vs Temperature		±0.022			±0.015			**±0.02**			**±0.01**		%/°C
Scale Factor Error (SF = 10.000V Nominal)[2]		±0.25			±0.1			±0.25			±0.1		%
Temperature-Coefficient of Scaling-Voltage		**±0.02**			**±0.01**			**±0.2**				**±0.005**	%/°C
Supply Rejection (±15V ±1V)		±0.01			±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20V pk-pk, Y = 10V)		±0.4			±0.2	±0.3		±0.4			±0.2	±0.3	%
Nonlinearity, Y (Y = 20V pk-pk, X = 10V)		±0.2			±0.1	±0.1		±0.2			±0.1	±0.1	%
Feedthrough[3], X (Y Nulled, X = 20V pk-pk 50Hz)		±0.3			±0.15	±0.3		±0.3			±0.15	±0.3	%
Feedthrough[3], Y (X Nulled, Y = 20V pk-pk 50Hz)		±0.01			±0.01	±0.1		±0.01			±0.01	±0.1	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±5	**±30**		±2	**±15**	mV
Output Offset Voltage Drift		200			100				**500**			**300**	µV/°C
DYNAMICS													
Small Signal BW, (V_{OUT} = 0.1rms)		1			1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000pF)		50			50			50			50		kHz
Slew Rate (V_{OUT} 20 pk-pk)		20			20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20V)		2			2			2			2		µs
NOISE													
Noise Spectral-Density SF = 10V		0.8			0.8			0.8			0.8		µV/√Hz
SF = 3V[4]		0.4			0.4			0.4			0.4		µV/√Hz
Wideband Noise A = 10Hz to 5MHz		1.0			1.0			1.0			1.0		µV/rms
P = 10Hz to 10kHz		90			90			90			90		µV/rms
OUTPUT													
Output Voltage Swing	**±11**			**±11**			**±11**			**±11**			V
Output Impedance (f ≤ 1kHz)		0.1			0.1			0.1			0 1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30			30		mA
Amplifier Open Loop Gain (f = 50Hz)		70			70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]													
Signal Voltage Range (Diff. or CM		±10			±10			±10			±10		V
Operating Diff.)		±12			±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±5	**±20**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			100			150		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±5	**±30**		±2	**±15**	mV
Offset Voltage Drift Z		200			100				500			300	µV/°C
CMRR	**60**	80		**70**	90		**60**	80		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**		0 8	**2.0**	µA
Offset Current		0.1			0.1			0.1			0 1		µA
Differential Resistance		10			10			10			10		MΩ
DIVIDER PERFORMANCE													
Transfer Function ($X_1 > X_2$)		$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1]													
($X = 10V, -10V \leq Z \leq +10V$)		±0.75			±0.35			±0.75			±0.35		%
($X = 1V, -1V \leq Z \leq +1V$)		±2 0			±1.0			±2.0			±1.0		%
($0.1V \leq X \leq 10V, -10V \leq Z \leq 10V$		±2.5			±1.0			±2.5			±1.0		%
SQUARER PERFORMANCE													
Transfer Function		$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$			$\frac{(X_1-X_2)^2}{10V}+Z_2$		
Total Error ($-10V \leq X \leq 10V$)		±0.6			±0.3			±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE													
Transfer Function, ($Z_1 \leq Z_2$)		$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$			$\sqrt{10V(Z_2-Z_1)}+X_2$		
Total Error[1] ($1V \leq Z \leq 10V$)		±1.0			±0.5			±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS													
Supply Voltage													
Rated Performance		±15			±15			±15			±15		V
Operating	±8		**±18**	±8		**±18**	±8		**±22**	±8		±22	V
Supply Current													
Quiescent		4	6		4	6		4	6		4	6	mA
PACKAGE OPTIONS[6]													
TO-100 (H-10A)		AD632AH			AD632BH			AD632SH			AD632TH		
TO-116 (D-14)		AD632AD			AD632BD			AD632SH			AD632TD		

NOTES

[1]Figures given are percent of full-scale, ±10V (i.e , 0.01% = 1mV)

[2]May be reduced down to 3V using external resistor between $-V_S$ and SF

[3]Irreducible component due to nonlinearity: excludes effect of offsets.

[4]Using external resistor adjusted to give SF = 3V.

[5]See functional block diagram for definition of sections

[6]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Typical Performance Curves (typical at +25°C with $\pm V_S$ = 15V)

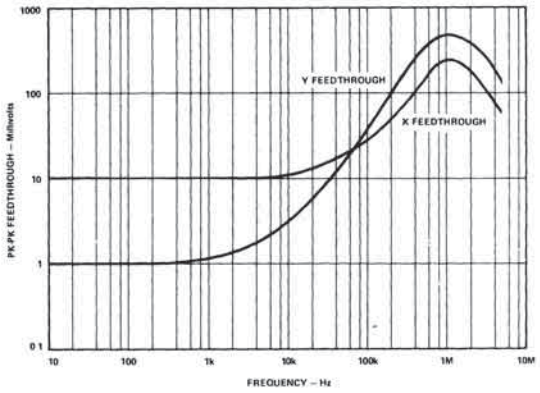


Figure 1. AC Feedthrough vs. Frequency

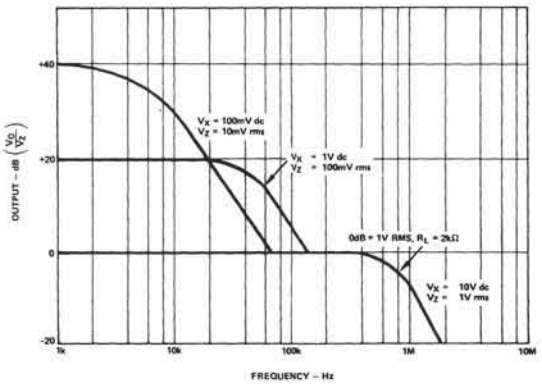


Figure 3. Frequency Response vs. Divider Denominator Input Voltage

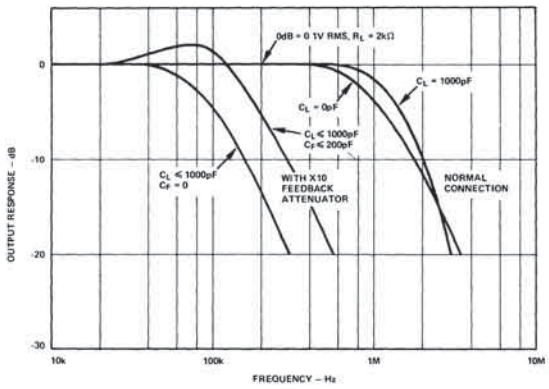
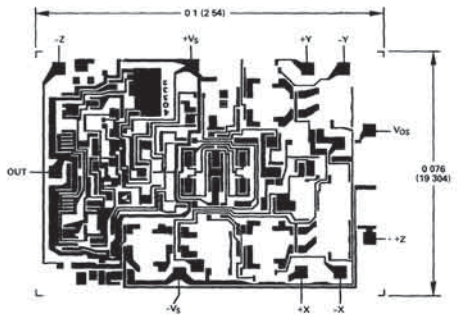


Figure 2. Frequency Response as a Multiplier

CHIP DIMENSIONS & PAD LAYOUT



For further information, consult factory

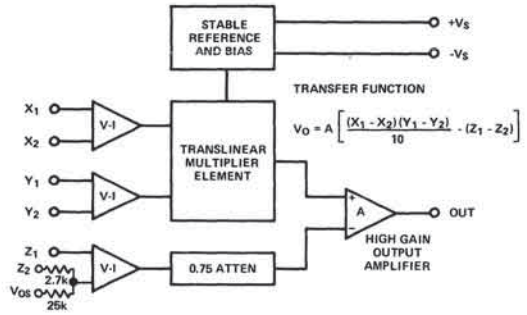


Figure 4. AD632 Functional Block Diagram

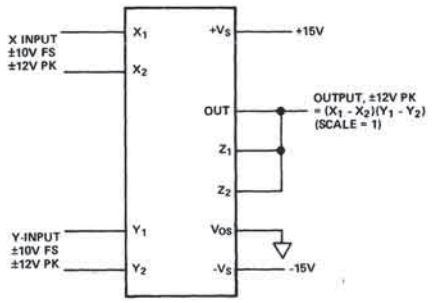


Figure 6. Connections for Scale-Factor of Unity

OPERATION AS A MULTIPLIER

Figure 5 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

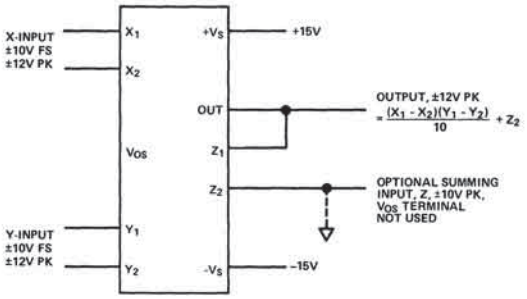


Figure 5. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30mV range required) to the X or Y input. Curve 1 shows the typical ac feedthrough with this adjustment mode. Note that the feedthrough of the Y input is a factor of 10 lower than that of the X input and should be used in applications where null suppression is critical.

The Z_2 terminal of the AD632 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1MHz small signal bandwidth and a 20V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise the differential inputs should be referenced to their respective signal common potentials to realize the full accuracy of the AD632.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 6. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80kHz without the peaking capacitor C_F. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications.

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the Z_1 terminal where they are amplified by –10 or to the common ground connection where they are amplified by –1. Input signals may also be applied to the lower end of the 2.7kΩ resistor, giving a gain of +9.

OPERATION AS A DIVIDER

Figure 7 shows the connection required for division. Unlike earlier products, the AD632 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in Figure 3.

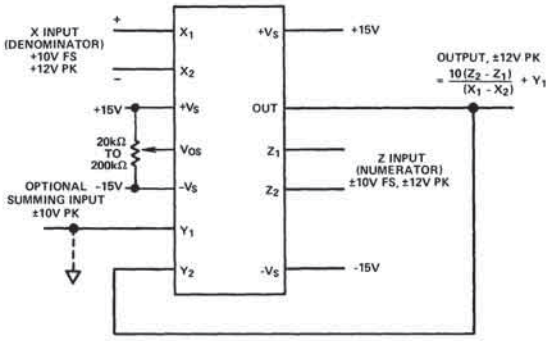


Figure 7. Basic Divider Connection

Without additional trimming, the accuracy of the AD632B is sufficient to maintain a 1% error over a 10V to 1V denominator range (The AD535 is functionally equivalent to the AD632 and has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications).

This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5mV max) applied to the unused X input. To trim, apply a ramp of +100mV to +V at 100Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

*See the AD535 Data Sheet for more details.

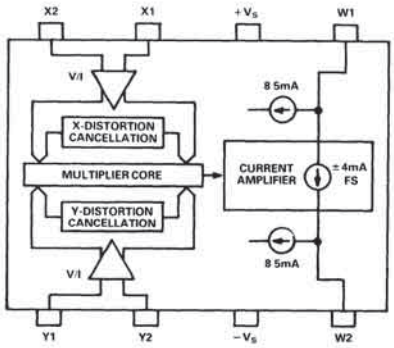
Very High Frequency Four-Quadrant Multiplier

AD834

FEATURES
500MHz Large-Signal Bandwidth
Differential ±1V Full-Scale Inputs
Differential ±4mA Full Scale Output Current
Low Distortion (≤0.05% for 10dBm Input)
Supply Voltages from ±4V to ±9V
Low Power (290mW at V_S = ±5V)

APPLICATIONS
High-Speed Real-Time Computation
Wideband Modulation and Gain Control
Signal Correlation and Power Measurement
Voltage-Controlled Filters and Oscillators
Linear Keyers for High Resolution Television
Wideband True RMS

AD834 FUNCTIONAL BLOCK DIAGRAM



6

PRODUCT DESCRIPTION

The AD834 is a monolithic laser-trimmed four-quadrant analog multiplier intended for use in high frequency applications, having differential voltage inputs and a differential current output. The transconductance bandwidth (R_L = 50Ω) is typically 500MHz from either input. Performance is relatively insensitive to temperature and supply variations, due to the use of stable biasing based on a bandgap reference generator and other design features.

To preserve the full bandwidth potential of the high-speed bipolar process used to fabricate the AD834, the outputs appear as current as a differential pair of currents at open collectors. The transfer function is accurately trimmed such that when X = Y ±1V, the differential output is ±4mA.

In multiplier modes, the maximum total full-scale error is 2%, dependent on the application mode and the external circuitry. A square-law transfer function can be achieved by connecting the inputs in parallel; in this mode, the AD834 can be used as a power detector up to 500MHz. The AD834J is specified for use over the commercial temperature range of 0°C to +70°C, and is available in either an 8-pin SO package or 8-pin cerdip. The AD834S is specified for use over the military temperature range of −55°C to +125°C, and is available in an 8-pin cerdip.

PRODUCT HIGHLIGHTS

1. The AD834 performs four-quadrant multiplication with a large-signal bandwidth in excess of 500MHz.
2. Multiplier static accuracy of 2% of full-scale can be achieved.
3. Unique design techniques result in low output distortion (≤0.05% for +10dBm inputs).
4. Low power consumption (290mW at ±5V supplies).
5. Differential current outputs ensure maximum usable bandwidth is available.
6. Laser-trimmed offsets and scale.

SPECIFICATIONS (T_A = +25°C and $\pm V_S$ = ±5V, unless otherwise noted)

Model	Conditions	AD834J Min	AD834J Typ	AD834J Max	AD834S Min	AD834S Typ	AD834S Max	Units
INPUT (X1, X2, Y1, Y2)								
Full-Scale Range	Differential		±1			±1		V
Clipping Level	Differential	**±1.2**	±1.4		**±1.2**	±1.4		V
Input Resistance	Differential	15	25		15	25		kΩ
Offset Voltage	X1, X2, Y1, Y2 = 0		0.5	5		0.5	5	mV
vs. Temperature	T_{min} to T_{max}		10			10	20	µV/°C
vs. Supplies[1]	$+V_S$ to $-V_S$		25			25		µV/V
Bias Current			45			45		µA
Common-Mode Rejection	f≤100kHz		70			70		dB
Distortion[2]	f = 10kHz							
	X = +10dBm, Y = 1V		−66			−66		dB
	X = 1V, Y = +10dBm		−55			−55		dB
OUTPUTS (W1, W2)								
Zero-Signal Current	Each Output		8.5			8.5		mA
Differential Offset	X = 0, Y = 0		±10	**±50**		±10	**±50**	µA
vs. Temperature	T_{min} to T_{max}		1			1		µA/°C
Full-Scale Output	Differential		±4			±4		mA
	X1 = Y1 = +1V							
	X2 = Y2 = 0V							
Full-Scale Accuracy			±0.1	**±1**		±0.1	**±1**	% FS
Peak Output	Differential		±16			±16		mA
	X = Y = ±2V							
Output Compliance		4.75		9	4.75		9	V
MULTIPLIER PERFORMANCE								
Transfer Function	(Figure 3)		V_{OUT} = XY/1V			V_{OUT} = XY/1V		
Total Error[3]	−1V≤X, Y≤+1V			2			2	% FS
vs. Temperature	T_{min} to T_{max}		TBD			TBD		% FS/°C
vs. Supplies[1]	$+V_S$ to $-V_S$		TBD			TBD		% FS/V
AC Feedthrough[4]	Sine Input							
X = ±1V, Y = 0	f = 10kHz		−54			−54		dB
	f = 10MHz		−50			−50		dB
X = 0, Y = ±1V	f = 10kHz		−66			−66		dB
	f = 10MHz		−50			−50		dB
Noise Spectral Density	f = 10kHz to 1MHz		TBD			TBD		nV/√Hz
Wideband Noise	f = 10Hz to 100MHz		TBD			TBD		V rms
POWER SUPPLIES								
Rated Performance			±5			±5		V
Operating Range		4		9	4		9	V
Quiescent Current[5]	T_{min} to T_{max}							
$+V_S$			10			10		mA
$-V_S$			29			29		mA
TEMPERATURE RANGE								
Commercial (0°C to +70°C)			AD834JR, AD834JQ					
Military (−55°C to +125°C)						AD834SQ		
PACKAGE OPTIONS[6]								
Small Outline (R-8)			AD834JR					
Cerdip (Q-8)			AD834JQ			AD834SQ		

NOTES
[1]Either supply taken separately; sinusoidal input at f≤10kHz.
[2]Specified in a 50Ω system.
[3]Error is defined as the maximum deviation from the ideal output, and expressed as a percentage of the full-scale output.
[4]Relative to full-scale output (X = 1V or Y = 1V); zero-input port nulled. At 10kHz, feedthrough is predominantly nonlinear residues. At frequencies above 10MHz, it is largely determined by inevitable stray capacitances.
[5]Negative supply current is approximately equal to the sum of the positive supply current and the signal currents into each output, W1 and W2.
[6]See Section 16 for package outline information.

Specifications shown in boldface are tested on all production units at final electrical test. Results from these tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Specifications subject to change without notice.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS

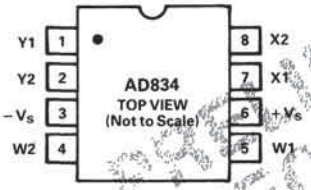
Supply Voltage ($+V_S$ to $-V_S$) . . . . . +16V
Internal Power Dissipation 500mW
Input Voltages (X1, X2, Y1, Y2) . . . . . $\pm V_S$
Operating Temperature Range
AD834J . . . . . 0°C to +70°C
AD834S . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature, Soldering 60sec . . . . . +300°C

NOTE
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CONNECTION DIAGRAM

8-Pin Cerdip (Q) Package

Small Outline (R) Package



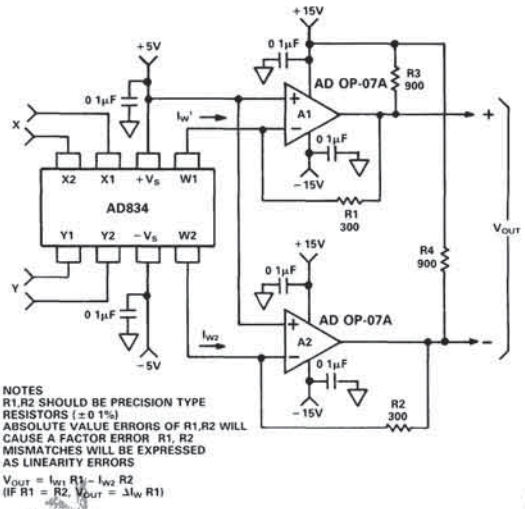


Figure 1. Low Frequency Multiplier Test Circuit

6

BASIC OPERATION

Figure 2 is a functional equivalent of the AD834. There are three differential signal interfaces: the voltage inputs X = X1 − X2 and Y = Y1 − Y2, and the current output, W = W1 − W2, which flows in the direction shown when X and Y are positive. The outputs W1 and W2 each have a standing current of typically 8.5mA ±15%.

The input voltages are first converted to differential currents which drive the translinear core. The equivalent resistance of the voltage-to-current (V-I) converters is about 285Ω. This low value results in low input-related noise and drift. However, the low full-scale input voltage results in relatively high nonlinearity in the V-I converters. This is significantly reduced by the use of distortion cancellation circuits which operate by Kelvin–sensing the voltages generated in the core–a unique feature of the AD834.

The current-mode output of the core is amplified by a special cascode stage which provides a current gain of nominally 1.6, trimmed during manufacture to set up the full-scale output current of ±4mA. This output appears at a pair of open collectors which must be supplied with a voltage slightly above the positive supply on Pin 6. As shown in Figure 3, this can be arranged by inserting a resistor in series with the supply to this pin and taking the load resistors to the full supply. With R3 = 60Ω, the voltage drop across it is about 600mV. Using two 50Ω load resistors, the full-scale differential output voltage is ±400mV (about +2dBm for a sinusoidal waveform).

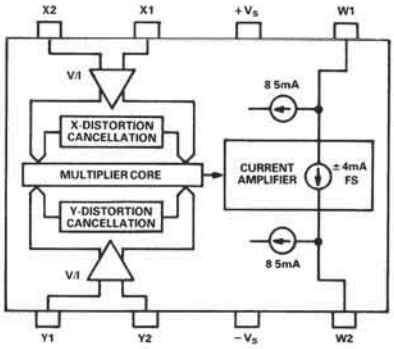


Figure 2. AD834 Functional Block Diagram

The full bandwidth potential of the AD834 can only be realized when very careful attention is paid to grounding and decoupling. The device must be mounted close to a high-quality ground plane and all lead lengths must be extremely short, in keeping with UHF circuit layout practice. In fact, the AD834 shows useful response to well beyond 1GHz, and the actual upper frequency in a typical application will usually be determined by the care with which the layout is effected. Note that R4 (in series with the $-V_S$ supply) carries about 30mA, and thus introduces a voltage drop of about 150mV. It is made large enough to reduce the Q of the resonant circuit formed by the supply lead and the decoupling capacitor. Slightly larger values can be used, particularly when using higher supply voltages. Alternatively, lossy RF chokes or ferrite beads on the supply leads may prove effective.

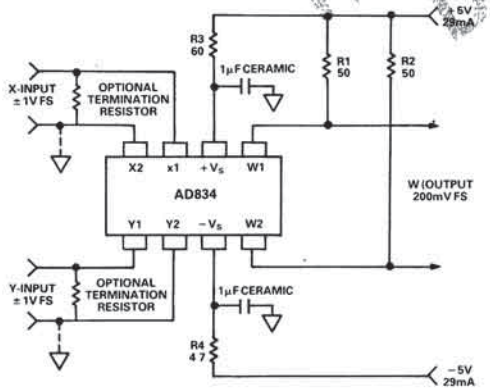


Figure 3. Basic Connections for Wideband Operation

Figure 3 shows the use of optional termination resistors at the inputs. Note that although the resistive component of the input impedance is quite high (about 25kΩ), the input bias current of typically 45µA can generate quite significant offset voltages if not compensated. For example, with a source and termination resistance of 50Ω (net source of 25Ω) the offset would be $25\Omega \times 45\mu A = 1.125mV$. This can be almost fully cancelled by including (in this example) another 25Ω resistor in series with the "unused" input (in Figure 3, either X2 or Y2). In order to minimize crosstalk the input pins closest to the output (X1 and Y2) optionally may be grounded; the effect is merely to reverse the phase of the X input and thus alter the polarity of the output.

TRANSFER FUNCTION – The output current W is the linear product of input voltages X and Y divided by $(1V)^2$ and multiplied by the "scaling current" of 4mA:

$$W = \frac{XY}{(1V)^2} 4mA$$

Provided that it is understood that the inputs are specified in volts, a simplified expression can be used:

$$W = (XY)\ 4mA$$

Alternatively, the full transfer function can be written:

$$W = \frac{XY}{1V} \cdot \frac{1}{250\Omega}$$

When both inputs are driven to their clipping level of about 1.4V, the peak output current is roughly doubled, to ±8mA, but distortion levels will then be very high.

TRANSFORMER COUPLING

In many high-frequency applications where baseband operation is not required at either inputs or output, transformer coupling can be used. Figure 4 shows the use of a center-tapped output transformer, which provides the necessary dc load condition at the outputs W1 and W2, and is designed to match into the desired load impedance by appropriate choice of turns ratio. The specific choice of the transformer design will depend entirely on the application. Transformers may also be used at the inputs. Center-tapped transformers can reduce high-frequency distortion and lower HF feedthrough by driving the inputs with balanced signals.

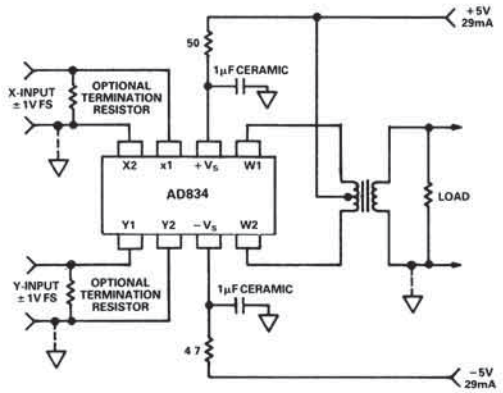


Figure 4. Transformer – Coupled Output

A particularly effective type of transformer is the balun, which is a short length of transmission line wound on to a toroidial ferrite core. Figure 5 shows this arrangement used to convert the 'bal'anced output to an 'un'-balanced one (hence the use of the term). Although the symbol used is identical to that for a transformer, the mode of operation is quite different. In the

first place, the load should now be equal to the characteristic impedance of the line, although this will usually not be critical for short line lengths. The collector load resistors R_C may also be chosen to reverse-terminate the line, but again this will only be necessary when an electrically long line is used. In most cases, R_C will be made as large as the dc conditions allow, to minimize power loss to the load. The line may be a miniature coaxial cable or a twisted pair.

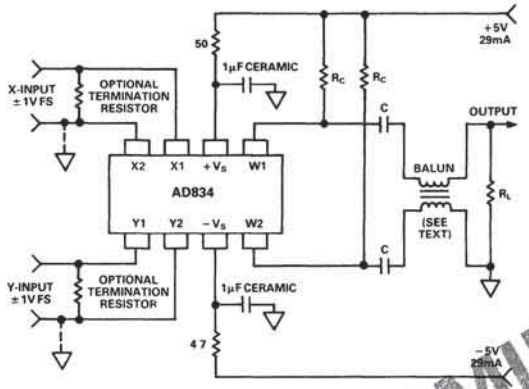


Figure 5. Using a Balun at the Output

It is important to note that the upper bandwidth limit of the balun is determined only by the quality of the transmission line; hence, it will usually exceed that of the multiplier. This is unlike a conventional transformer, where the signal is conveyed as a flux in a magnetic core, and is limited by core losses and leakage inductance. The lower limit on bandwidth is determined by the series inductance of the line, taken as a whole, and the load resistance (if the blocking capacitors C are sufficiently large). In practice, a balun can provide excellent differential-to-single-sided conversion over much wider bandwidths than a transformer.

WIDEBAND MULTIPLIER CONNECTIONS

Where operation down to dc and a ground-based output are necessary, the configuration shown in Figure 6 can be used.

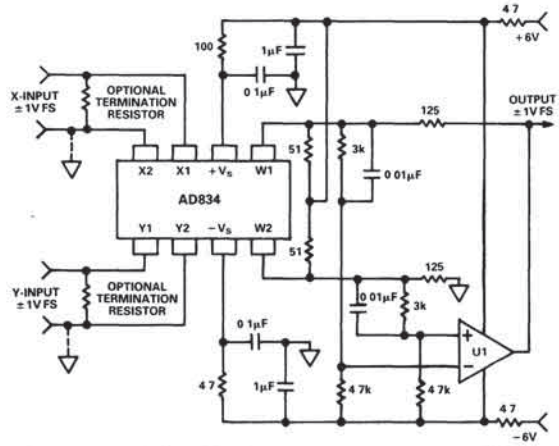


Figure 6. Wideband dc-Coupled Multiplier with ±1V Output

The element values were chosen in this example to result in a full-scale output of ±1V, so the overall multiplier transfer function is

$$W = (X1 - X2)(Y1 - Y2)$$

where it is understood that the inputs and output are in volts. The polarity of the output can be reversed simply by reversing either the X or Y input.

The op amp should be chosen to support the desired output bandwidth. The AD842 and AD5539 may be used in wideband applications – the former providing about 50MHz of usuable bandwidth. Many other choices are possible where lower post-multiplication bandwidths are acceptable. The level-shifting network places the input nodes of the op amp to within a few hundred millivolts of ground using the recommended balanced supplies. The output offset may be nulled, either by use of a 100Ω trimpot included between each of the lower pair of resistors (4.7kΩ) and the negative supply, or by the use of an adjustment to the op amp trim pins.

The scaling can be altered so that the output is ±10V full scale by raising the 125Ω feedback resistors to 1.25kΩk, raising the supply voltages to the op amp to ±15V, and optionally raising the AD834 load resistors to 100Ω. As always, attention to power supply decoupling is essential for stable wideband operation.

WIDEBAND SQUARING OPERATION

The AD834 can be used as a signal squarer by connecting the X and Y inputs in parallel, as shown in Figure 7, which shows the input arranged to provide a 50Ω termination to the source, using a pair of 100Ω resistors in a symmetrical layout to reduce the effect of resistor lead inductance. Minimum lead lengths and direct routes to the ground plane are important. The 50Ω resistors included in series with the X1 and Y2 pins reduce offset voltages generated by the input bias currents.

The same output system as used for the wideband multiplier is used here, and similar measures may be taken to alter the scaling factor and deal with output offset. Alternatively, one of the several transformer-coupled arrangements may be used.

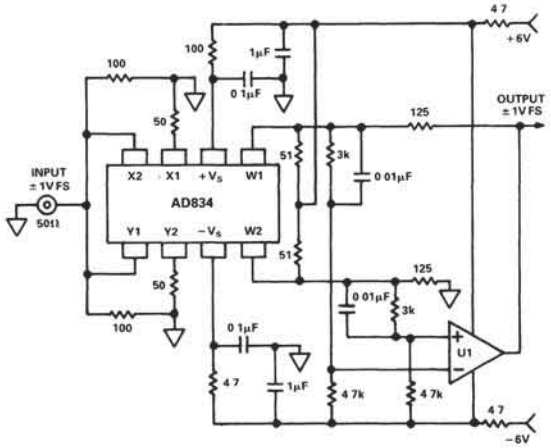


Figure 7. Wideband Squarer Connection

PRELIMINARY TECHNICAL DATA

POWER MEASUREMENT (MEAN-SQUARE)

The wide bandwidth of the AD834 makes it well suited to measurement of power, either as a multiplier for the determination of the average V × I product, or as a squarer for use with a single input. In these applications, the AD834 is followed by some sort of low-pass filtering to extract the long-term average value. If the first pole of this filter is formed by the addition of capacitors placed directly at the output Pins W1 and W2, the effective multiplication or squaring bandwidth can be limited solely by the AD834, since the following active circuitry is required to process only low-frequency signals.

Figure 8 shows a general configuration which can be adapted to suit a variety of scaling needs. The load resistors R1 are chosen to result in minimal low-frequency voltage variation at the output nodes W1 and W2, consistent with also achieving low drift in the following subtraction stage formed by the op amp U1 and resistor pairs R2 and R3. The first pole is formed by R1 and C1, the second by R3 and C2. Extreme care must be taken in the layout of the circuit near the input and in the placement of the capacitors C1; these will dominate the high-frequency behavior of the circuit, which, under favorable conditions, will extend to beyond 1GHz. Representative values are R1 = 51Ω, R2 = 430kΩ, R3 = 1MΩ, C1 = 1μF ceramic in parallel with (physically-smaller) 0.01μF capacitors, C2 = 0.01μF. The op amp may be an AD711; for maximum accuracy at the low end of the dynamic range, use the offset-nulling pins of the op amps.

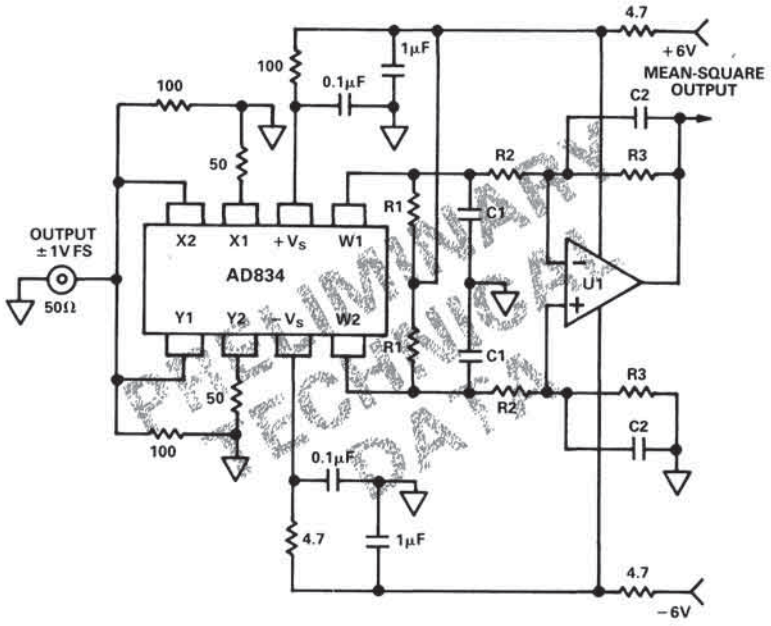


Figure 8. Connections for Extracting the Mean-Square Output

Log/Antilog Amplifiers
Contents

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7

Selection Guide
Log/Antilog Amplifiers

Model	Log Conformity Input Range	3dB Error %RTI	Bandwidth kHz	Page	Notes
755	10nA – 1mA	0.5	10	7 – 11	
757	10nA – 1mA	0.5	25	7 – 15	
759	20nA – 1mA	1.0	200	7 – 11	
AD9521	0.4V p-p	± 1dB	10MHz – 250MHz	7 – 7	Wideband amplifier w/logarithmic detected output

7

Orientation
Log/Antilog Amplifiers

The devices catalogued in this section include complete, self-contained modules that provide output voltage proportional to the logarithm or the antilogarithm (exponential) of an input quantity. These modules operate on the instantaneous values of inputs from dc to an upper cutoff frequency well below 1MHz.

Also included is the AD9521 monolithic wideband ac logarithmic amplifier with about 12dB of gain, pin compatible with the Plessey SL521 and SL1521. Wideband log amplifiers are cascaded to form "strips" with gains of 90dB and more – depending on input amplitude – over a wide dynamic range, for frequencies typically in the range of 7MHz to 250MHz.

LOGS AND LOG RATIOS

In the *logarithmic* mode, the ideal output equation is

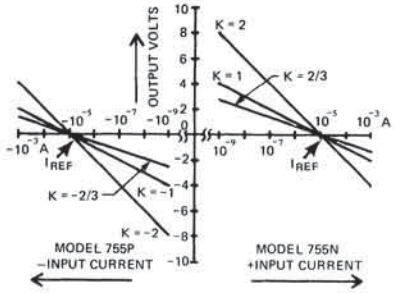
$$E_o = -K \log_{10} \left\{ \frac{I_{in}}{I_{ref}} \right\}$$

E_o can be positive or negative; it is zero when the ratio is unity, i.e., $I_{in} = I_{ref}$. K is the output scale constant; it is equal to the number of output volts corresponding to a decade* change of the ratio. In the 755 and 759 log amplifiers, K is pin programmable to be either 1V, 2V or 2/3V, or externally adjustable to any value ≥2/3V; in the model 757 log-ratio amplifier, K may be either a preset value of 1V or an arbitrary value adjustable by an external resistance ratio.

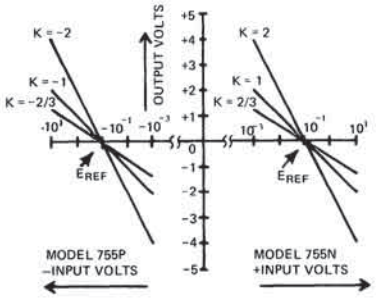
I_{in} is a unipolar input current within a 6-decade range (1nA to 1mA); it may be applied directly, as a current, or derived from an input voltage via an input resistor (in which case, the ratio becomes $E_{in}/(R_{in}I_{ref}) = E_{in}/E_{ref}$. In models 755 and 759, the magnitude of I_{ref} is internally fixed at 10μA ($E_{ref} = 0.1V$) or externally adjusted; but model 757 is *log-ratio* amplifier, in which both I_{in} and I_{ref} (or E_{in} and E_{ref}, using external scaling resistors) are input variables.

Each of the log amplifiers is available as a "P" or "N" option, depending on the polarity of the input voltage. Logarithms may be computed only for positive arguments, therefore the reference current must be of appropriate polarity to make the ratio positive. "N" indicates that the input current (or voltage) for the log mode is *positive*; "P" indicates that only *negative* voltage or current may be applied in the log mode. The polarity of K also differs: K is positive for "N" versions and negative for "P" versions. Thus, +10V applied to model 759N, with K = +1V, would produce an output voltage, $E_o = -1V \log (100) = -2V$; on the other hand, −10V applied to model 759P with K = 1V, would produce an output voltage, $E_o = -(-1V) \log (100) = +2V$. The figure shows, in condensed form, the outputs of P and N log amps, with differing K values, for both voltage and current inputs, plotted on a semi-log scale.

Log amplifiers in the log mode are useful for applications requiring *compression* of wide-range analog input data, *linearization* of transducers having exponential outputs and *analog computing*, ranging from simple translation of natural relationships in log form (e.g., computing absorbence as the log ratio of input currents), to the use of logarithms in facilitating analog computation of terms involving arbitrary exponents and multiterm products and ratios.



Log of Current



Log of Voltage

Output vs. Input of Model 755N & 755P in Log Connection (Log Input Scales), Showing Voltages, and Polarity Relationships

ANTILOGS

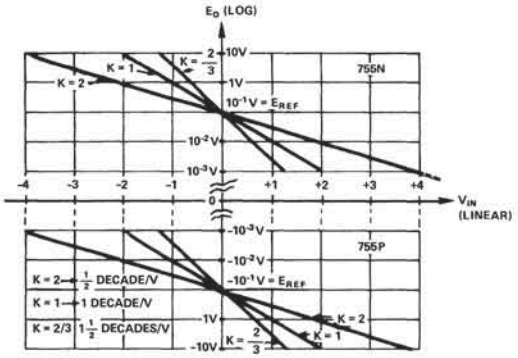
In the *antilogarithmic* (exponential) mode, the ideal output equation is

$$E_o = E_{ref} (10)^{-E_{in}/K}$$

E_{in} can be positive or negative; when it is zero, $E_o = E_{ref}$. However, E_o is always of single polarity, positive for "N" versions, negative for "P" versions. Thus, for 759P, connected for K = −2V, if $E_{in} = +4V$, and $E_{ref} = -0.1V$, then $E_o = -0.1V \cdot 10^{-4/-2}$, or −10V. If $E_{in} = -4V$, then $E_o = -0.1V \cdot 10^{-(-4)/-2} = -1mV$. The figure on the next page shows in condensed form, the outputs of P and N log amps, connected for antilogarithmic operation, with different K values.

Antilog amplifiers are useful for applications requiring *expansion* of compressed data, *linearization* of transducers having logarithmic outputs, *analog function fitting* or function generation, to obtain relationships or generate curves having voltage-programmable rates of growth or decay, and in *analog computing*, for such functions as compound multiplication and division of terms having differing exponents.

***A *decade* is a 10:1 ratio, two decades is 100:1, etc. For example, if K = 2, and the ratio is 10, the magnitude of the output would be 2V, and its polarity would depend on whether the ratio were greater or less than unity. If the input signal then changed by a factor of 1,000 (3 decades), the output would change by 6V.**



Antilog Operator Response Curves, Semilog Scale
$E_O = E_{REF}\ 10^{V_{IN}/-K}$

LOG-ANTILOG AMPLIFIER PERFORMANCE

Considerable information regarding log- and antilog-amplifier circuit design, performance, selection and applications is to be found in the *Nonlinear Circuits Handbook*[1]. Several salient points will be covered here, and specifications will be defined.

A log/antilog amplifier consists of an operational amplifier and an element with antilogarithmic transconductance (i.e., the voltage into the element produces a current that is an exponential function of the voltage). As the figure shows, for logarithmic operations, the input current is applied at the op-amp summing point, and the feedback circuit causes the amplifier output to produce whatever voltage is required to provide a feedback current that will exactly balance the input current.

In antilog operation, the input voltage is applied directly to the input of the antilog element, producing an exponential input current to the op-amp circuit. The feedback resistance transduces it to an output voltage.

The wide range of log/exponential behavior is made possible by the exponential current-voltage relationship of transistor base-emitter junctions,

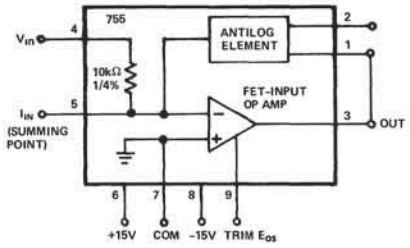
$$I = I_o(\epsilon^{qV/kT} - 1) \cong I_o\epsilon^{qV/kT}$$

and $V = (kT/q) \ln (I/I_o)$

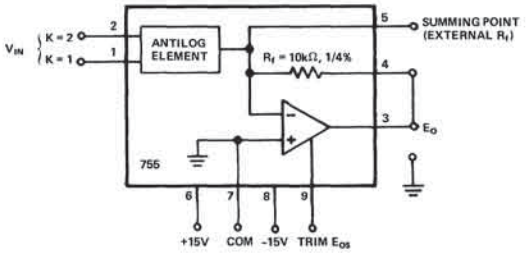
where I is the collector current, I_o is the extrapolated current for V = 0, V is the base-emitter voltage, q/k (11,605 K/V) is the ratio of charge of an electron to Boltzmann's constant and T is junction temperature in kelvins. In log/antilog devices, two matched transistors are connected so as to subtract the junction voltages associated with the input and reference currents, making the ratio independent of I_o's variation with temperature.

$$\begin{aligned}\Delta V &= (kT/q) \ln (I_{in}/I_o) - (kT/q) \ln (I_{ref}/I_o)\\ &= (kT/q)(\ln I_{in} - \ln I_{ref}) + (kT/q)(\ln I_o - \ln I_o)\\ &= (kT/q) \ln (I_{in}/I_{ref})\end{aligned}$$

[1]***Nonlinear Circuits Handbook*, Analog Devices, Inc., 1974, 1976, 536pp, edited by D. H. Sheingold, $5.95; send check or complete MasterCard data to P.O. Box 796, Norwood, MA 02062**



a) Log/Antilog Amplifier Connected in the Log Mode (K = 1)



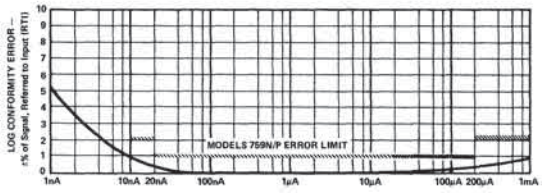
b) Log/Antilog Amplifier Connected in the Exponential Mode

The temperature dependence of gain is compensated for by a resistive attenuator that uses a temperature-sensitive resistor for compensation. The attenuator also produces amplification of K to the specified nominal values, e.g., from the basic 59mV/decade, (kT/q) ln10 at room temperature, to 1V/decade.

Errors are introduced by the offset current of the amplifier (and the offset voltage) for voltage inputs; by inaccuracy of the reference current (or the effective reference voltage, for voltage inputs) in fixed-reference devices; and by inaccuracy of setting K. Additional errors are introduced by drift of these parameters with temperature. At any temperature, if these parameters are nulled out, there remains a final irreducible difference between the actual output and the theoretical output, called *log-conformity error*, which is manifested as a "nonlinearity" of the input-output plot on semilog coordinates. Best log conformity is realized away from the extremities of the rated signal range. For example, log-conformity error of model 755 is ±1% maximum, referred to the input, over the entire 6-decade range from 1nA to 1mA; but it is only ±0.5% maximum over the 4-decade range from 10nA to 100μA. A plot of log conformity error for model 759 is shown on the following page.

Errors occurring at the input, and log-conformity errors, can only be observed at the output, but it is useful to refer them to the input (RTI). Equal percentage errors at the input, at whatever input level, produce equal incremental errors at the output, for a given value of K. For example, if K = 1, and the RTI log-conformity error is +1%, the magnitude of the output error will be

$$\begin{aligned}\text{Error} &= \text{Actual output} - \text{ideal output}\\ &= 1V \cdot \log (1.01\ I/I_{ref}) - 1V \cdot \log (I/I_{ref})\\ &= 1V \cdot \log 1.01 = 0.0043V = 4.3mV\end{aligned}$$



Log Conformity Error for Models 759N and 759P

If, in this example, the input range happens to be 5 decades, the corresponding output range will be 5 volts, and the 4.3mV log-conformity error, as a percentage of total *output* range, will be less than 0.1%. Because this ambiguity can prove confusing to the user, it is important that a manufacturer specify whether the error is referred to the input or the output. The table below indicates the conversion between RTI percentage and output error-magnitudes, for various percent errors, and various values of K.

LOG OUTPUT ERROR (mV)

% ERROR RTI	K = 1V	K = 2V	K = (2/3)V
0.1	0.43	0.86	0.28
0.5	2.2	4.3	1.4
1.0	4.3	8.6	2.9
2.0	8.6	17	5.7
3.0	13	26	8.6
4.0	17	34	11
5.0	21	42	14
10.0	41	83	28

For antilog operations, input and output errors are interchanged.

To arrive at the total error, an error budget should be made up, taking into account each of the error sources, and its contribution to the total error, over the temperature range of interest.

Dynamic response of log amps is a function of the input level. Small-signal bandwidths of ac input signals biased at currents above 1μA tend to be roughly comparable. However, below 1μA, bandwidth tends to be in rough proportion to current level. Similarly, rise time depends on step magnitude and direction – step changes in the direction of increasing current are responded to more quickly than step decreases of current.

DEFINITIONS OF SPECIFICATIONS

Log-Conformity Error: When the parameters have been adjusted to compensate for offset, scale-factor and reference errors, the *log-conformity error* is the deviation of the resulting function from a straight line on a semilog plot over the range of interest.

Offset Current (I_{os}) is the bias current of the amplifier, plus any stray leakage currents. This parameter can be a significant source of error when processing signals in the nanoampere region. Its contribution in antilog operation is negligible.

Offset Voltage (E_{os}) depends on the operational amplifier used for the log operation. Its effect is that of a small voltage in series with the input resistor. For current-logging operations, with high-impedance sources, its error contribution is negligible. However, for voltage logging, it modifies the value of V_{in}. Though it can be adjusted to zero at room temperature, its drift over the temperature range should be considered. In antilog operation, E_{os} appears at the output as an essentially constant voltage; its percentage effect on error is greatest for small outputs.

Reference Current (I_{ref}) is the effective internally-generated current-source output to which all values of input current are compared. I_{ref} tolerance appears as a dc offset at the output; it can be adjusted towards zero by adjusting the reference current, adding a voltage to the output by injecting a current into the scale-factor attenuator or simply by adding a constant bias at the output's destination.

Reference Voltage (E_{ref}) is the effective internally generated voltage to which all input voltages are compared. It is related to I_{ref} by the equation: $E_{ref} = I_{ref}R_{in}$, where R_{in} is the value of input resistance. Typically, I_{ref} is less stable than R_{in}; therefore, practically all the tolerance is due to I_{ref}.

Scale Factor (K) is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope (on a semilog plot), and is specified in percent of the nominal value.

WIDEBAND (AC) LOGARITHMIC AMPLIFIERS

Amplifiers in the class of the AD9521 are essentially *limiting amplifiers*, providing high gain for small signals and low gain for large signals. They accept high-frequency ac signals (7MHz to 250MHz) and provide two amplified outputs: a radio-frequency output (voltage) and a nonlinearly detected output (current). The amplification characteristic (current output vs. rf input) on a semilog scale is S-shaped, starting with zero slope, increasing to a linear slope, then soft-saturating (with a slight overshoot).

They are used in *strips*, or cascades, of *n* (for example, 6 to 9) stages, with the rf output of one unit becoming the input of the next, thus multiplying their gains. The nonlinearly detected (or *video*) outputs are connected together for current summation.

The resulting output-vs.-input characteristic (semilog scale) is S-shaped, with a lengthy log-linear region whose extent depends on the number of stages (about 12dB per device). Once an amplifier saturates, its contribution to the summation is fixed; thus, the maximum output for large signals is *n* times the output of one device. The maximum dynamic range has been realized when the number of stages, *n*, is such that the input-stage noise alone produces full output from the last stage.

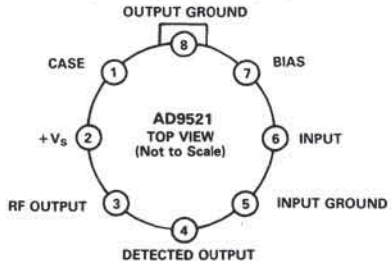
250MHz Wideband Logarithmic Amplifier

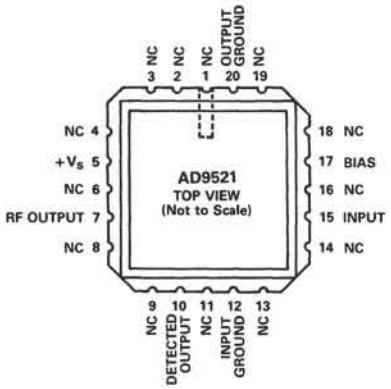
AD9521

FEATURES
250MHz Bandwidth
Monolithic Construction
Low Noise Figure 4.7dB
Excellent Detected Output Matching
Direct Replacement for SL521/SL1521

APPLICATIONS
Missile Guidance
Electronic Warfare (ECM, ECCM, ESM)
Miniaturized LOG Strips
Nuclear Instrumentation

PIN DESIGNATIONS





GENERAL DESCRIPTION

The AD9521 is a wideband amplifier stage with a logarithmic detected output. The high-performance bipolar process used to construct the AD9521 allows operation from 10MHz to 250MHz with minimal gain variation. The AD9521 is pin compatible with the SL521 and the SL1521.

The AD9521 is constructed in a well controlled monolithic process which provides very good gain tolerance (±1.5dB)over the full performance range. An added benefit of the high gain tolerance is a high degree of detected output current matching from device to device. The matching combined with the low 4dB noise figure allows the construction of 80dB to 90dB dynamic range LOG strips with better than ±1dB linearity.

The AD9521 is offered in two gain tolerance grades as both a commercial temperature range device, 0 to +70°C, and as an extended temperature range device, −55°C to +125°C. All grades are available packaged in 8-pin TO-99 metal cans with the military grades also available packaged in ceramic LCC.

7

ORDERING INFORMATION

Device	Detected Output Matching	Temperature Range	Description	Package Options*
AD9521JH	0.2mA	0 to +70°C	8-Pin Can, Industrial	H-08A
AD9521KH	0.1mA	0 to +70°C	8-Pin Can, Industrial	H-08A
AD9521SE	0.2mA	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD9521SH	0.2mA	−55°C to +125°C	8-Pin Can, Extended Temperature	H-08A
AD9521TE	0.1mA	−55°C to +125°C	20-Pin LCC, Extended Temperature	E-20A
AD9521TH	0.1mA	−55°C to +125°C	8-Pin Can, Extended Temperature	H-08A

*See Section 16 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage ($+V_S$)	+9V
Differential Voltage Between Grounds	0.5V
Maximum Input Before Overload	1.9V rms
Instantanious Voltage at the Detected Video Output	12V
RF Output Current	10mA
Power Dissipation	500mW
Operating Temperature Range[2]	
AD9521JH/KH	0 to +70°C
AD9521SE/SH/TE/TH	−55°C to +125°C
Storage Temperature Range	−55°C to +150°C
Junction Temperature	+175°C
Lead Soldering Temperature (10sec)	+300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages = +6V; INPUT connected to BIAS pin; R_S = 50Ω; $C_L \leq$ 8pF, unless otherwise stated)

			Industrial Temp. Range 0 to +70°C						Military Temp. Range −55°C to +125°C						
	Mil[3] Sub		AD9521JH			AD9521KH			AD9521SE/SH			AD9521TE/TH			
Parameter	Group	Temp	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
AC PERFORMANCE															
Voltage Gain (f_{IN} = 30MHz)	7	+25°C	11.5	12.2	12.5	11.5	12.2	12.5	11.5	12.2	12.5	11.5	12.2	12.5	dB
	8	Full	11.0		13.0	11.0		13.0	11.0		13.0	11.0		13.0	dB
Voltage Gain (f_{IN} = 60MHz)	7	+25°C	12.0	12.8	13.0	12.0	12.8	13.0	12.0	12.8	13.0	12.0	12.8	13.0	dB
	8	Full	11.7		13.7	11.7		13.7	11.7		13.7	11.7		13.7	dB
Voltage Gain (f_{IN} = 120MHz)	7	+25°C	12.2	13.0	13.8	12.2	13.0	13.8	12.2	13.0	13.8	12.2	13.0	13.8	dB
	8	Full	11.5		14.5	11.5		14.5	11.5		14.5	11.5		14.5	dB
Voltage Gain (f_{IN} = 160MHz)	7	+25°C	12.7	13.4	14.2	12.7	13.4	14.2	12.7	13.4	14.2	12.7	13.4	14.2	dB
	8	Full	11.5		14.5	11.5		14.5	11.5		14.5	11.5		14.5	dB
Input Capacitance		+25°C		6			6			6			6		pF
Noise Figure[4]	12	+25°C		4.7	4.9		4.7	4.9		4.7	4.9		4.7	4.9	dB
Gain Variation vs. Temperature[5]		Full		0.67			0.67			0.67			0.67		dB
Gain Variation vs. Supply[6]	7,8			0.74	1.15		0.74	1.15		0.74	1.15		0.74	1.15	dB/V
Frequency Response															
Upper Cutoff Frequency	7	+25°C	230	245		230	245		230	245		230	245		MHz
	8	Full	200			200			200			200			MHz
Lower Cutoff Frequency	7,8	Full		7	10		7	10		7	10		7	10	MHz
DETECTED VIDEO OUTPUT															
Output Current @ 60MHz (Max)[7]	7	+25°	0.90	1.02	1.10	0.95	1.02	1.05	0.90	1.02	1.10	0.95	1.02	1.05	mA
	8	Full	0.80		1.20	0.85		1.15	0.80		1.20	0.85		1.15	mA
(80% Input Level)[8]	7	+25°C	0.70	0.82	0.90	0.75	0.82	0.85	0.70	0.82	0.90	0.75	0.82	0.85	mA
(No Input)[9]	7	+25°C		0.02	0.04		0.02	0.04		0.02	0.04		0.02	0.04	mA
Output Current @ 120MHz (Max)[7]	7	+25°C	0.68	0.79	0.90	0.73	0.79	0.85	0.68	0.79	0.90	0.73	0.79	0.85	mA
	8	Full	0.57		0.91	0.68		0.90	0.57		0.91	0.68		0.90	mA
(80% Input Level)[8]	7	+25°C	0.66	0.76	0.86	0.71	0.76	0.81	0.66	0.76	0.86	0.71	0.76	0.81	mA
(No Input)[9]	7	+25°C		0.02	0.04		0.02	0.04		0.02	0.04		0.02	0.04	mA
Detected Output Variation vs. Supply[6]	7	+25°C		28	30		28	30		28	30		28	30	%/V
Detected Output vs. Temperature[5]		Full		9			9			9			9		%
RF OUTPUT[5,7]															
Maximum RF Output Voltage		+25°C		1.6			1.6			1.6			1.6		V p-p
RF Output Propagation Delay		+25°C		1.4			1.4			1.4			1.4		ns
POWER SUPPLY[10]															
Supply Current (+6.0V)	1	+25°C		14.0	16.0		14.0	16.0		14.0	16.0		14.0	16.0	mA
	2,3	Full			16.5			16.5			16.5			16.5	mA
Nominal Power Dissipation		+25°C		84			84			84			84		mW

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedance . . .
AD9521 Metal Can. θ_{JA} = 185°C/W; θ_{JC} = 50°C/W
AD9521 LCC θ_{JA} = 80°C/W; θ_{JC} = 50°C/W.

[3]Military subgroups apply to military qualified devices only.

[4]R_S = 450Ω; 60MHz.

[5]A_{IN} = 60MHz.

[6]Measured at ±5% of $+V_S$; A_{IN} = 60MHz.

[7]Input = 0.5V rms.

[8]Input = 0.09V rms.

[9]Input = 0.0V rms.

[10]Supply voltage should remain stable within ±5% for normal operation.

Specifications subject to change without notice.

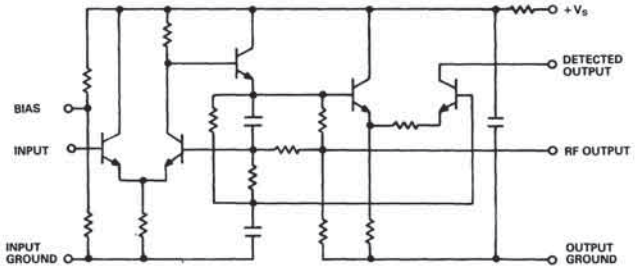
EXPLANATION OF GROUP A MILITARY SUBGROUPS

Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at max rated operating temp
Subgroup 3 – Static tests at min rated operating temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated operating temp
Subgroup 6 – Dynamic tests at min rated operating temp
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated operating temp
Subgroup 9 – Switching tests at +25°C
Subgroup 10 – Switching tests at max rated operating temp.
Subgroup 11 – Switching tests at min rated operating temp.
Subgroup 12 – Periodically sample tested.

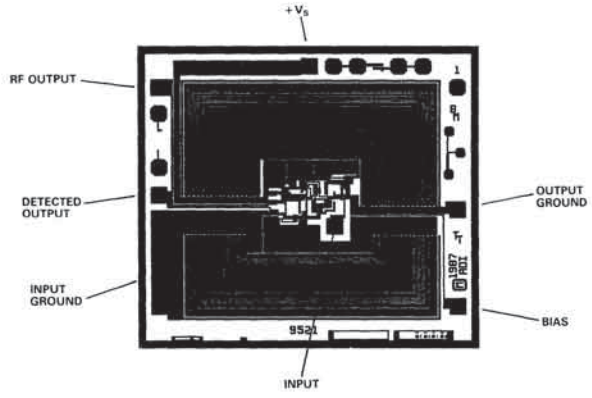
FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
CASE	– Case connection for the TO-99 metal can package only.
$+V_S$	– Positive supply terminal, nominally +6.0V.
RF OUTPUT	– The RF OUTPUT is used to drive subsequent LOG detection stages. The RF OUTPUT level is roughly +12dB above the IF signal strength at the input.
DETECTED OUTPUT	– The DETECTED OUTPUT provides a dc current logarithmicly proportional to the IF signal level at the input.
INPUT GROUND	– Isolated input ground connection. The input and output grounds should be connected together near the AD9521.
INPUT	– IF signal input.
BIAS	– The BIAS connection is tied to the INPUT pin to provide an adequate biasing level between ac coupled stages. The bias connection should be omitted between direct dc coupled stages.
OUTPUT GROUND	– Isolated output ground connection. The input and output grounds should be connected together near the AD9521.

SCHEMATIC

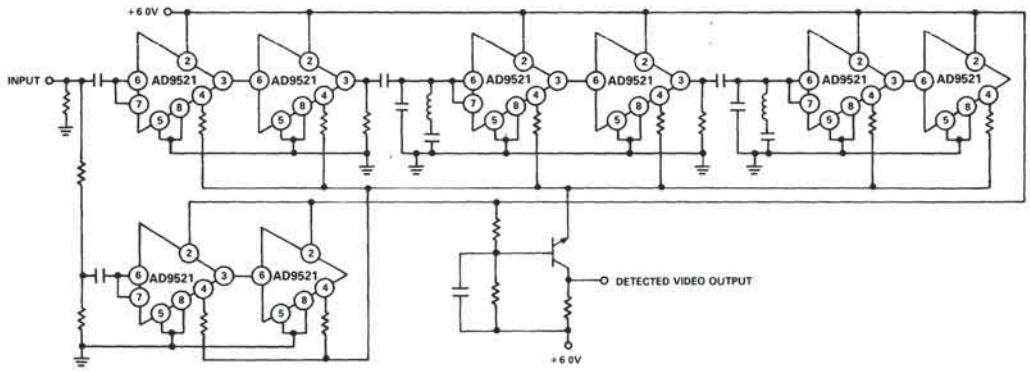


DIE LAYOUT AND MECHANICAL INFORMATION



Die Dimensions	86×97×15 (±2) mils
Pad Dimensions	4×4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil Aluminum; Ultrasonic Bonding or 1mil Gold; Gold Ball Bonding

TYPICAL LOG STRIP CONFIGURATION



APPLICATIONS INFORMATION

The AD9521 is primarily designed for use in successive detection LOG strips. The application circuit above, illustrates the typical configuration for one such design with roughly 90dB of dynamic range. In operation the IF input signal level is successively amplified by each stage in the upper chain. The IF signal at each stage generates a detected output current. The detected output current from each stage is summed in the common base follower stage at the end of the strip.

The key to the circuit is the limiting quality of the AD9521 logarithmic detected output. As the IF signal at each stage drives the detected output into saturation, the output current ceases to increase. In operation, the combined gain of all of the previous stages drives the last stage into saturation first. Any further increase in signal level will not increase the detected output level of the last stage, but all of the previous stages will enter saturation one-by-one as the signal level increases.

The limiting factor to the number of stages that can be combined is the input noise level. When the gain of the entire strip is sufficient to drive the last stage into saturation on the input noise of the first stage alone, further extensions of the strip will not increase the dynamic input range.

There are, however, two methods of increasing the dynamic range of the LOG strip which include bandwidth reduction and parallel strip configurations. The dynamic range can be extended by 20dB or more by incorporating a parallel log strip with an attenuated input. The main strip functions as before, but the second strip, because of the attenuation, only contributes to the output for signals in excess of the main strip saturation level. The ultimate limitation is the maximum input signal level which the main strip will tolerate. Any further signal level increases could damage the input stage of the AD9521. This should not be a major problem since with this technique the dynamic range of the total strip can be as high as 100dB.

The dynamic range can also be increased by reducing the bandwidth of the strip itself. The noise voltage is directly proportional to the square root of the circuit bandwidth. This means that large operating bandwidths produce large amounts of noise which translates into limited dynamic range. The AD9521 is a particularly low-noise device, but even it can benefit from bandwidth reduction which has been incorporated into the circuit above. The two interstage filters limit the noise to a smaller region of frequencies and thereby allow the strip to be extended further.

Because of the high-frequency nature of the AD9521, several guidelines should be followed to insure optimum performance. The first is the use of an adequate low impedance ground plane. Just as important is the use of power supply decoupling capacitors to prevent signal feedthrough on the supply lines. Chip capacitors are highly recommended because of their reduced lead inductance. Sockets are not likely to produce the best results because of the interlead capacitance, but if they must be used, pin sockets are preferred.

ANALOG DEVICES

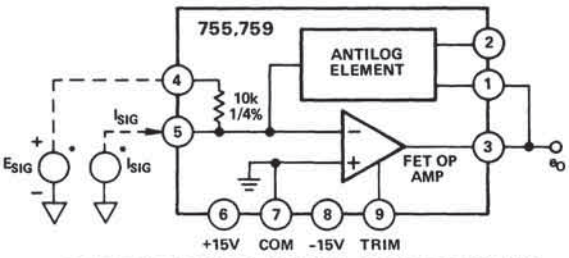
6-Decade, High Accuracy, Wideband Log, Antilog Amplifiers

Models 755N/755P/759N/759P

FEATURES

- **High Accuracy: Models 755N, 755P**
- **Wideband: Models 759N, 759P**
- **Complete Log/Antilog Amplifiers: External Components Not Required**
- **Temperature-Compensated Internal Reference**
- **6 Decades Current Operation: 1nA to 1mA**
- **1% max Error: 1nA to 1mA (755)**
  20nA to 200μA (759)
- **4 Decades Voltage Operation: 1mV to 10V**
- **1% max Error: 1mV to 10V (755)**
  1mV to 2V (759)
- **Small Size: 1.1″ × 1.1″ × 0.4″**

MODELS 755/759 FUNCTIONAL BLOCK DIAGRAM



*POSITIVE INPUT SIGNALS, AS SHOWN; USE MODEL 759N, 755N. NEGATIVE INPUT SIGNALS, USE MODEL 759N, 755P.

GENERAL DESCRIPTION

The models 755N, 755P and 759N, 759P are low cost dc logarithmic amplifiers offering conformance to ideal log operation over 6 decades of current (1nA to 1mA) and 4 decades of voltage (1mV to 10V). For high accuracy requirements, models 755N, 755P offer maximum nonconformity of 0.5%, from 10nA to 1mA, and 1mV to 1V. For wideband applications, the models 759N, 759P provide fast response (300kHz @ I_{SIG} = 10μA to 1mA) and feature maximum nonconformity of 1% from 20nA to 200μA, and 1mV to 2V. The models 755N and 759N compute the log of positive (+) input signals, while the models 755P, 759P compute the log of negative (–) signals.

Designed for ease of use, the models 755N/P and 759N/P are complete, temperature compensated log/antilog amplifiers packaged in a compact epoxy-encapsulated module. External components are not required for logging currents over the complete 6 decade range of 1μA to 1mA. Both the scale factor (K=2, 1, or 2/3 volt/decade) and log/antilog operation are selected by simple pin connection. In addition, both the internal 10μA reference current as well as the offset voltage may be externally adjusted to improve overall accuracy.

The models 755 and 759 are ideally suited as an alternative to in-house designs of OEM applications. Advanced design techniques and superior performance place the 755 and 759 ahead of competitive designs in terms of price, performance and package design.

APPLICATIONS

When connected in the current or voltage logging configuration, as shown in Figure 1, the models 755 and 759 may be used in several key applications. A plot of input current versus output voltage is also presented to illustrate the log amplifier's transfer characteristics.

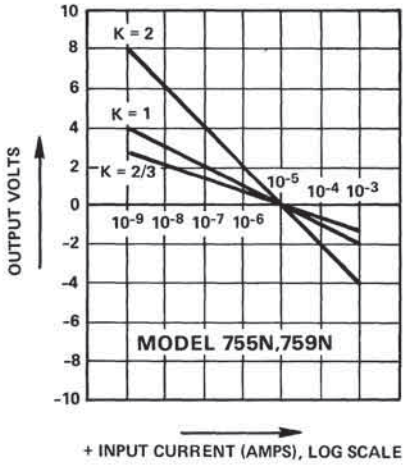


Figure 1. Transfer Function

7

SPECIFICATIONS (typical @ +25°C and ±15V dc unless otherwise noted)

MODEL	755N/P	759N/P
TRANSFER FUNCTIONS		
Current Mode	$e_O = -K\log_{10}\frac{I_{SIG}}{I_{REF}}$	*
Voltage Mode	$e_O = -K\log_{10}\frac{E_{SIG}}{E_{REF}}$	*
Antilog Mode	$e_O = E_{REF}\,10^{-\left(\frac{E_{SIG}}{K}\right)}$	*
TRANSFER FUNCTION PARAMETERS		
Scale Factor (K) Selections[1, 2]	2, 1, 2/3 Volt/Decade	*
Error @ +25°C	±1% max	*
vs Temperature (0 to +70°C)	±0.04%/°C max	*
Reference Voltage (E_{REF})[2]	0 1V	*
Error @ +25°C	±3% max	±4% max
vs Temperature (0 to +70°C)	±0 1%/°C max	±0.05%/°C
Reference Current (I_{REF})[2]	10µA	*
Error @ +25°C	±3% max	*
vs Temperature (0 to +70°C)	±0 1%/°C max	±0.05%/°C

MAXIMUM LOG CONFORMITY ERROR

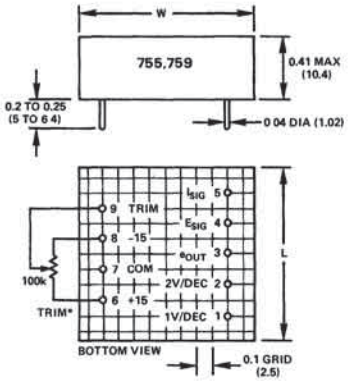
I_{SIG} RANGE	E_{SIG} RANGE	RTI	RTO (K=1)	RTI	RTO (K=1)
1nA to 10nA	–	±1%	±4 3mV	±5%	±21mV
10nA to 20nA	–	±0.5%	±2.17mV	±2%	±8.64mV
20nA to 100µA	1mV to 1V	±0.5%	±2 17mV	±1%	±4.3mV
100µA to 200µA	1V to 2V	±1%	±4 3mV	±1%	±4 3mV
200µA to 1mA	2V to 10V	±1%	±4 3mV	±2%	±8.64mV

INPUT SPECIFICATIONS		
Current Signal Range		
Model 755N, 759N	+1nA to +1mA min	*
Model 755P, 759P	−1nA to −1mA min	*
Max Safe Input Current	±10mA max	*
Bias Current @ +25°C	(0, +) 10pA max	(0, +) 200pA max
vs Temperature (0 to +70°C)	x2/+10°C	*
Voltage Signal Range (Log Mode)		
Model 755N, 759N	+1mV to +10V min	*
Model 755P, 759P	−1mV to −10V min	*
Voltage Signal Range, Antilog Mode Model 755N, 755P	$-2 \leqslant \frac{E_{SIG}}{K} \leqslant 2$	*
Offset Voltage @ +25°C (Adjustable to 0)	±400µV max	±2mV max
vs Temperature (0 to +70°C)	±15µV/°C max	±10µV/°C
vs Supply Voltage	±15µV/%	*
FREQUENCY RESPONSE, Sinewave		
Small Signal Bandwidth, −3dB		
I_{SIG} = 1nA	80Hz	250Hz
I_{SIG} = 1µA	10kHz	100kHz
I_{SIG} = 10µA	40kHz	200kHz
I_{SIG} = 1mA	100kHz	200kHz
RISE TIME		
Increasing Input Current		
10nA to 100nA	100µs	20µs
100nA to 1µA	7µs	3µs
1µA to 1mA	4µs	2 5µs
Decreasing Input Current		
1mA to 1µA	7µs	3µs
1µA to 100nA	30µs	10µs
100nA to 10nA	400µs	80µs
INPUT NOISE		
Voltage, 10Hz to 10kHz	2µV rms	10µV rms
Current, 10Hz to 10kHz	2pA rms	10pA rms
OUTPUT SPECIFICATIONS[3]		
Rated Output		
Voltage	±10V min	*
Current		
Log Mode	±5mA	*
Antilog Mode	±4mA	*
Resistance	0 5Ω	*
POWER SUPPLY[4]		
Rated Performance	±15Vdc	*
Operating	±(12 to 18)Vdc	*
Current, Quiescent	±7mA	±4mA
TEMPERATURE RANGE		
Rated Performance	0 to +70°C	*
Operating	−25°C to +85°C	*
Storage	−55°C to +125°C	*
CASE SIZE[5] (W x L x H)	1.5" x 1.5" x 0.4" (38 x 38 x 10.4)	1.125" x 1.125" x 0 4" (29 x 29 x 10 4)

NOTES
[1] Use terminal 1 for K = 1V/decade, terminal 2 for K = 2V/decade, terminals 1 or 2 (shorted together) for K = 2/3V/decade
[2] Specification is + for models 755N, 759N, − for 755P, 759P.
[3] No damage due to any pin being shorted to ground
[4] Recommended power supply, model 904, ±15V @ ±50mA output.
[5] Case size in inches (mm)
Specifications subject to change without notice.

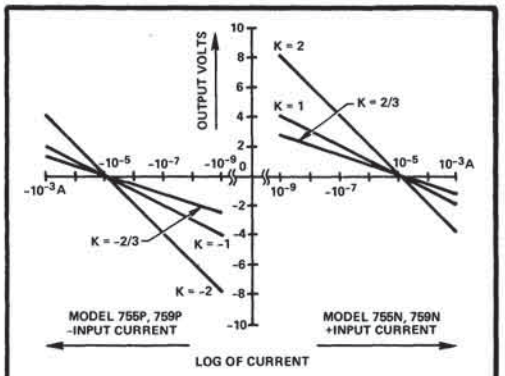
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

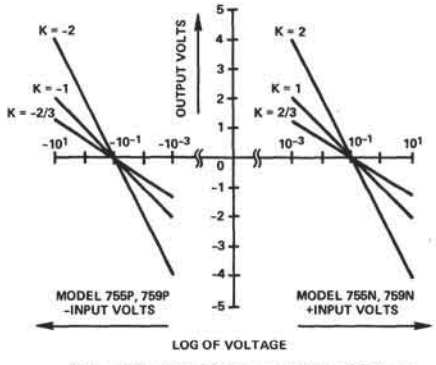


*Optional 100kΩ external trim pot. Input offset voltage may be adjusted to zero with trim pot connected as shown. With trim terminal 9 left open, input offset voltage will be ±0.4mV (755) or ±2mV (759) maximum.

MATING SOCKET AC1016



Plot of Output Voltage vs Input Current for Model 755 Connected in the Log Mode



Plot of Output Voltage vs Input Voltage for Models 755, 759 Connected in the Log Mode

Figure 2. Transfer Curves

Understanding the Log Amplifier Performance

PRINCIPLE OF OPERATION

Log operation is obtained by placing the antilog element in the feedback loop of the op amp as shown in Figure 1. At the summing junction, terminal 5, the input signal current to be processed is summed with the output current of the antilog element. To attain a balance of these two currents, the op amp provides the required output voltage to the antilog feedback element. Under these conditions the ideal transfer equation (K = 1) is:

$$e_{OUT} = 1V \log_{10} I_{SIG}/I_{REF}$$

The log is a mathematical operator which is defined only for numbers, which are dimensionless quantities. Since an input current would have the dimensions of amperes it must be referenced to another current, I_{REF}, the ratio being dimensionless. For this purpose a temperature compensated reference of 10μA is generated internally.

The scale factor, K, is a multiplying constant. For a change in input current of one decade (decade = ratio of 10:1), the output changes by K volts. K may be selected as 1V or 2V by connecting the output to pin 1 or 2, respectively. If the output is connected to both pins 1 and 2, K will be 2/3V.

REFERRING ERRORS TO INPUT

A unique property of log amplifiers is that a dc error of any given amount at the output corresponds to a constant percent of the input, regardless of input level. To illustrate this, consider the output effects due to changing the input by 1%.

The output would be:

$$e_{OUT} = 1V \log_{10} (I_{SIG}/I_{REF})(1.01) \text{ which is equivalent to:}$$

$$e_{OUT} = \underbrace{1V \log_{10} (I_{SIG}/I_{REF})}_{\text{Initial Value}} \quad \underbrace{\pm 1V \log_{10} (1.01)}_{\text{Change}}$$

The change in output, due to a 1% input change is a constant value of ±4.3mV. Conversely, a dc error at the output of ±4.3mV is equivalent to a change at the input of 1%. An abbreviated table is presented below for converting between errors referred to output (R.T.O.), and errors referred to input (R.T.I.).

	ERROR R.T.O.		
ERROR R.T.I.	K = 1	K = 2	K = 2/3
0.1%	0.43mV	0.86mV	0.28mV
0.5	2.17	4.34	1.45
1.0	4.32	8.64	2.88
3.0	12.84	25.68	8.56
4.0	17.03	34.06	11.35
5.0	21.19	42.38	14.13
10.0	41.39	82.78	27.59

Table I. Converting Output Error in mV to Input Error in %

SOURCES OF ERROR

Log Conformity Error – Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the value of the transfer equation and the actual value which occurs at the output of the log module, after scale factor, reference and offset errors are eliminated to taken into account. The best linearity performance for the models 755, 759 are obtained in the 5 decades from 10nA to 1mA. To obtain optimum performance, the input data should be scaled to this range.

Offset Voltage – The offset voltage, E_{os}, of models 755, 759 is the offset voltage of the internal FET amplifier. This voltage appears as a small dc offset voltage in series with the input terminals. For current logging applications, its error contribution is negligible. However, for log voltage applications, best performance is obtained by an offset trim adjustment.

Bias Current – The bias current of models 755, 759 is the bias current of the internal FET amplifier. This parameter can be a significant source of error when processing signals in the nanoamp region. For this reason, the bias current for model 755 is 10pA, maximum, and 200pA maximum for model 759.

Reference Current – I_{REF} is the internally generated current source to which all input currents are compared. I_{REF} tolerance errors appear as a dc offset at the output. The specified value of I_{REF} is ±3% referred to the input, and, from Table I, corresponds to a dc offset of ±12.84mV for K = 1. This offset is independent of input signal and may be removed by injecting a current into terminal 1 or 2.

Reference Voltage – E_{REF} is the effective internally generated voltage to which all input voltages are compared. It is related to I_{REF} through the equation:
$E_{REF} = I_{REF} \times R_{IN}$, where R_{IN} is an internal 10kΩ, precision resistor. Virtually all tolerance in E_{REF} is due to I_{REF}. Consequently, variations in I_{REF} cause a shift in E_{REF}.

Scale Factor – Scale factor is the voltage change at the output for a decade (i.e., 10:1) change at the input, when connected in the log mode. Error in scale factor is equivalent to a change in gain, or slope, and is specified in per cent of the nominal value. An external adjustment may be performed if fine trimming is desired for improved accuracy.

7

OPTIONAL EXTERNAL ADJUSTMENTS FOR LOG OPERATION

Trimming E_{OS} – The amplifier's offset voltage, E_{OS}, may be trimmed for improved accuracy with the models 755, 759 connected in its log circuit. To accomplish this, a 100kΩ, 10 turn pot is connected as shown in Figure 3. The input terminal, Pin 4, is connected to ground. Under these conditions the output voltage is:

$$e_{OUT} = -K \log_{10} E_{OS}/E_{REF}$$

To obtain an offset voltage of 100μV or less, for K = 1, the trim pot should be adjusted until the output voltage is between +3 and +4 volts for models 755N, 759N, and -3V to -4V for models 755P, 759P.

For other values of K, the trim pot should be adjusted for an output of e_{OUT} = 3 x K to 4 x K where K is the scale factor.

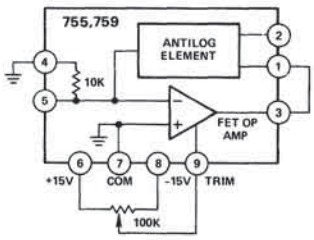


Figure 3. Trimming E_{OS} in Log Mode

Reference Current or Reference Voltage – The reference current or voltage of models 755, 759 may be shifted by injecting a constant current into the unused scale factor terminal (Pin 1 or Pin 2). The current injected will shift the reference one decade, in accordance with the expression: $I_I = 66\mu A \log 10\mu A/I_{REF}$ (755), $I_I = 330\mu A \log 10\mu A/I_{REF}$ (759), where I_I = current to be injected and I_{REF} = the desired reference current.

By changing I_{REF}, there is a corresponding change in E_{REF} since, $E_{REF} = I_{REF} \times R_{IN}$. An alternate method for rescaling E_{REF} is to connect an external R_{IN}, at the I_{IN} terminal (Pin 5) to supplant the 10kΩ supplied internally (leaving it unconnected). The expression for E_{REF} is then, $E_{REF} = R_{IN} I_{REF}$. Care must be taken to choose R_{IN} such that $(e_{SIG}$ max$)/R_{IN} \leq 1$mA.

Scale Factor (K) Adjustment – Scale factor may be increased from its nominal value by inserting a series resistor R_S between the output terminal, Pin 3, and either terminal 1 or 2. The table below should be consulted when making these scale factor changes.

RANGE OF K	CONNECT SERIES R TO PIN	VALUE OF R_S	NOTE
2/3V to 1.01V	1	R x (K - 2/3)	use pins 1, 2
1.01V to 2.02V	1	R x (K - 1)	use pin 1
>2.02V	2	R x (K - 2)	use pin 2

R = 15kΩ (755); 3kΩ (759)

Table 2. Resistor Selection Chart for Shifting Scale Factor

ANTILOG OPERATION

The models 755 and 759 may be used to develop the antilog of the input voltage when connected as shown in Figure 4. The antilog transfer function (an exponential), is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} \qquad [-2 \leq e_{IN}/K \leq 2]$$

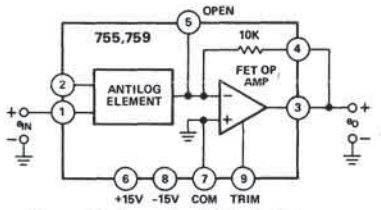


Figure 4. Functional Block Diagram

Principle of Operation – The antilog element converts the voltage input, appearing at terminal 1, to a current which is proportional to the antilog of the applied voltage. The current-to-voltage conversion is then completed by the feedback resistor in a closed-loop op amp circuit.

A more complete expression for the antilog function is:

$$e_{OUT} = E_{REF}\ 10^{-e_{IN}/K} + E_{OS}$$

The terms K, E_{OS}, and E_{REF} are those described previously in the LOG section.

Offset Voltage (E_{OS}) Adjustment – Although offset voltage of the antilog circuit may be balanced by connecting it in the log mode, and using the technique described previously, it may be more advantageous to use the circuit of Figure 5. In this configuration, offset voltage is equal to $e_{OUT}/100$. Adjust for the desired null, using the 100k trim pot. After adjusting, turn power off, remove the external 100Ω resistor, and the jumper from Pin 1 to +15V. For 755P, 759P use the same procedure but connect Pin 1 to -15V.

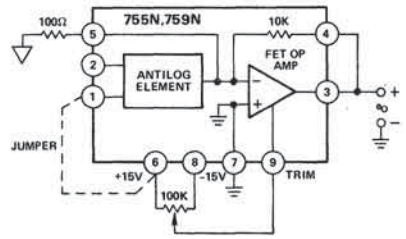


Figure 5. Trimming E_{OS} in Antilog Mode

Reference Voltage (E_{REF}) Adjustment – In antilog operation, the voltage reference appears as a multiplying constant. E_{REF} adjustment may be accomplished by connecting a resistor, R, from Pin 5 to Pin 3, in place of the internal 10kΩ. The value of R is determined by:

$$R = E_{REF} \text{ desired}/10^{-5} \text{ A}$$

Scale Factor (K) Adjustment – The scale factor may be adjusted for all values of K greater than 2/3V by the techniques described in the log section. If a value of K less than 2/3V is desired for a given application, an external op amp would be required as shown in Figure 6. The ratio of the two resistors is approximately:

$$R1/R_G = (1/K - 1) \text{ where K = desired scale factor}$$

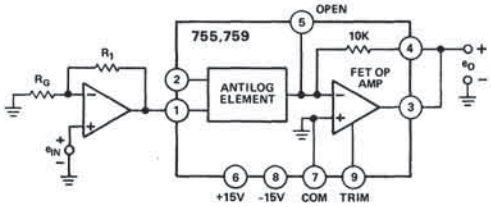


Figure 6. Method for Adjusting K<2/3V

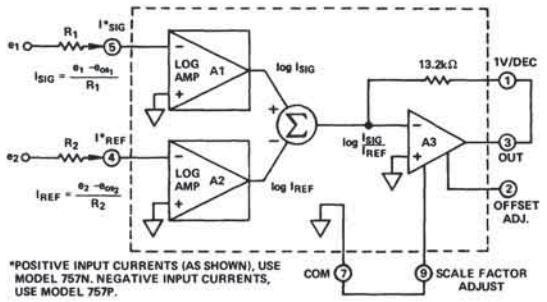
6-Decade, High Accuracy Log Ratio Amplifiers

Models 757N/757P

FEATURES
- 6 Decade Operation — 1nA to 1mA
- 1/2% Log Conformity — 10nA to 100μA
- Symmetrical FET Inputs
- Voltage or Current Operation
- Temperature Compensated

APPLICATIONS
- Absorbence Measurements
- Log Ratios of Voltages or Currents
- Data Compression
- Transducer Linearization

MODEL 757 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

Model 757 is a complete, temperature compensated, dc-coupled log ratio amplifier. It is comprised of two input channels for processing signals spanning up to 6 decades in dynamic range (1nA to 1mA). By virtue of its symmetrical FET input stages, the 757 can accommodate this 6 decade signal range at either channel. Log conformity is maintained to within 1/2% over 4 decades of input (10nA to 100μA) and to within 1% over the full input range. Unlike other log ratio designs, model 757 does not restrict the relative magnitude of the two signal inputs to achieve rated performance. Either input can be operated within the specified range regardless of the signal level at the other channel.

The model 757 log-ratio amplifier design makes available both input amplifier summing junctions. As a result, it can directly interface with photo diodes operating in the short-circuit current mode without the need of additional input circuitry.

The excellent performance of model 757 can be further improved by means of external scale factor and output offset adjustments. A significant feature of model 757 not found on competing devices is that, when the offset adjustment is used to establish a fixed bias at the output, the output offset level does not vary as a function of input signal magnitude. On other designs, the sensitivity of output offset to input levels results in output effects resembling log conformity errors.

Model 757 can operate with either current or voltage inputs. Its excellent performance makes it ideally suited for log ratio applications such as blood analysis, chromatography, chemical analysis of liquids and absorbence measurements.

CURRENT LOG RATIO

Current log ratio is accomplished by model 757 when two currents, I_{SIG} and I_{REF}, are applied directly to the input terminals (see Figure 1). The two log amps process these signals providing voltages which are proportional to the log of their respective inputs. These voltages are then subtracted and applied to an output amplifier. The scale factor, when connected as shown, is 1V/dec. However, higher scale factors may be achieved by connecting external scale factor adjusting resistors.

VOLTAGE LOG RATIO

The principle of operation for voltage log ratio is identical to that of current log ratio after the voltage signal has been converted to a current. To accomplish this conversion, an external resistor is attached from the voltage signal to the appropriate input current terminal of the 757. Input currents are then determined by:

$$I_{SIG} = \frac{e_1 - e_{os_1}}{R_1}, \quad I_{REF} = \frac{e_2 - e_{os_2}}{R_2}$$

e_{os_1} = Input Offset Voltage (I_{SIG} Channel)

e_{os_2} = Input Offset Voltage (I_{REF} Channel)

SPECIFICATIONS (typical @ +25°C and V_S = ±15V dc unless otherwise noted)

MODEL	757N/P
TRANSFER FUNCTION [1]	
Current Mode	$e_o = -K \log_{10} \frac{I_{SIG}}{I_{REF}}$
Voltage Mode	$e_o = -K \log_{10} \left[\frac{(e_1 - e_{os_1})}{(e_2 - e_{os_2})} \times \frac{R_2}{R_1} \right]$
ACCURACY	
Log Conformity[2]	
I_{SIG}, I_{REF} = 10nA to 100μA	±0.5%, max
I_{SIG}, I_{REF} = 1nA to 1mA	±1%, max
Scale Factor (1V/Dec)	(+0, -2%) max
vs Temperature (0 to +70°C)	±0.04%/°C max
INPUT SPECIFICATIONS – Both Input Channels	
Current	
Signal Range, Rated Performance	
Model 757N	+1nA to +1mA min
Model 757P	−1nA to −1mA min
Max Safe	±10mA max
Bias Current, @ +25°C	(0, +) 10pA max
vs Temperature (0 to +70°C)	x2/+10°C
Offset Voltage, @ +25°C	±1mV max
vs Temperature (0 to +70°C)	
I_{SIG} Channel	±25μV/°C max
I_{REF} Channel	±25μV/°C max
vs Supply Voltage	±5μV/%
FREQUENCY RESPONSE, Sinewave	
Small Signal Response (-3dB)	
Signal Channel	
I_{SIG} = 1nA	160Hz
I_{SIG} = 1μA	60kHz
I_{SIG} = 100μA	75kHz
Reference Channel	
I_{REF} = 1nA	60Hz
I_{REF} = 1μA	30kHz
I_{REF} = 100μA	80kHz

RISE TIME	Signal Channel (I_{REF} = 10μA)	Reference Channel (I_{SIG} = 10μA)
Increasing Input Current		
1nA to 10nA	2.5ms	1.0ms
10nA to 100nA	250μs	40μs
100nA to 1μA	25μs	30μs
1μA to 100μA	10μs	25μs
Decreasing Input Current		
100μA to 1μA	5μs	10μs
1μA to 100nA	10μs	50μs
100nA to 10nA	50μs	500μs
10nA to 1nA	500μs	10ms

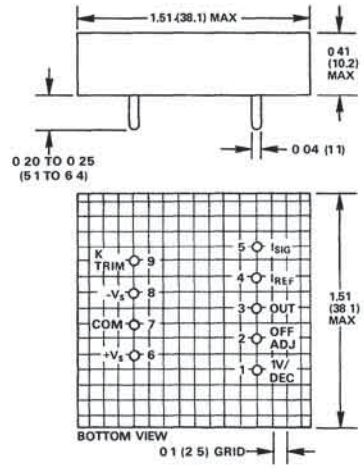
INPUT NOISE	
Voltage (10Hz to 10kHz)	3μV rms
Current (10Hz to 10kHz)	0.1pA rms
OUTPUT SPECIFICATIONS	
Rated Output	
Voltage	±10V min
Current	±5mA min
Resistance	0.1Ω
Offset Voltage[3] (K = 1V/Decade)	±15mV max
vs Temperature (0 to +70°C)	±0.3mV/°C
vs Supply	±5μV/V
POWER SUPPLY[4]	
Rated Performance	±15V dc
Operating	±(12 to 18)V dc
Current, Quiescent	±8mA
TEMPERATURE RANGE	
Rated Performance	0 to +70°C
Operating	-25°C to +85°C
Storage	-55°C to +125°C
MECHANICAL	
Case Size	1.5" x 1.5" x 0.4"
Weight	21 grams

NOTES
[1] For model 757N, K = +1V/Decade and input currents must be positive. For model 757P, K = −1V/Decade and input currents must be negative. (Input currents are defined as positive when flowing into the input terminals, 4 and 5. Refer to TRANSFER CURVES.)
[2] The log conformity error is referred to input (RTI). 1% error RTI is equivalent to 4.3mV of error at the output for K = 1V/Dec.
[3] Externally adjustable to zero.
[4] Recommended power supply: Analog Devices model 904, ±15V @ 50mA.

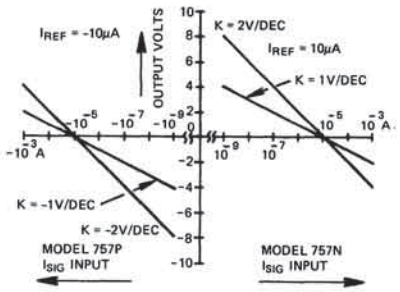
Specifications subject to change without notice.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



TRANSFER CURVES



Log mode output voltage vs. input current for I_{REF} = 10μA.

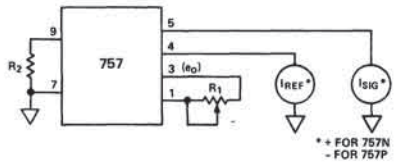


Figure 2. Scale Factor Adjustment

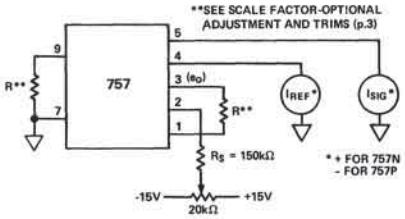


Figure 3. Output Voltage Offset Adjustments

OPTIONAL ADJUSTMENTS AND TRIMS

Scale Factor – A one volt per decade scale factor is available when pin 1 is tied to 3 and pin 7 is connected to 9. Higher scale factors are possible by using a potentiometer, R_1, between pins 1 and 3 and a resistor, R_2, between pins 7 to 9 as shown in Figure 2. The value of the required resistor is (13.2kΩ) (K-1) where K is the desired scale factor. The approximate potentiometer value is also (13.2kΩ) (K-1). The scale factor adjustment procedure is as follows:

1. Connect the appropriate value of resistor between pins 7 and 9.
2. Set I_{REF} = 1μA, I_{SIG} = 10μA. Measure e_O.
3. Set I_{REF} = 1μA, I_{SIG} = 100μA. Adjust R_1 until the difference in e_O corresponding to steps 2 and 3 is K volts.
4. Repeat steps 2 and 3 until the change in e_O = K volts.

Output Voltage Offset – Output voltage offset must be adjusted after the desired scale factor is established as indicated above. To adjust the offset, inject equal dc input currents into the reference and signal channels. The value of the input currents should approximate the average input current levels expected to be encountered in normal operation. Adjust the potentiometer shown in Figure 3 until the output voltage is zero.

LOG CONFORMITY

Log conformity in logarithmic devices is a specification similar to linearity in linear devices. Log conformity error is the difference between the theoretical value of the log of a ratio and the actual value that appears at the output of the log-ratio module after scale factor errors have been eliminated. Measurement of this error is made after initially zeroing the module at unity-ratio and adjusting the desired scale factor.

Figure 4 shows the log conformity performance of model 757 over a 6 decade input range. Log conformity for each channel does not vary noticeably as the current is varied in the other channel.

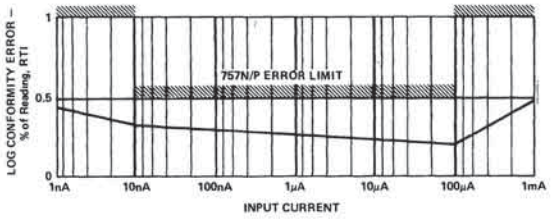
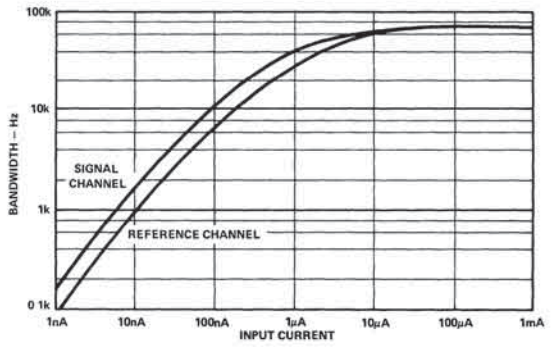


Figure 4. Log Conformity Error for Model 757. Curve is for Either Input Channel with Current Held Constant at 10μA On Other Channel.

FREQUENCY CHARACTERISTICS

Figure 5 shows a plot of small signal response (-3dB) as a function of input signal current. The graph demonstrates the frequency response performance for each input channel over the range of 1nA to 1mA, independent of current on the other channel.



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APPLICATIONS

Data Compression – Processing signals with wide dynamic range is a common problem in instrumentation and data transmission. For example, digitizing an analog signal with a range of 10nA to 100μA with 1% accuracy requires a 20 bit A/D converter. (Required resolution = 1/100 x 1/10,000 = $1/10^6 \cong 1/2^{20}$).

By using the 757 with I_{REF} adjusted to 10nA and K set for 5/4 V/decade, the input data can be compressed into a 5 volt output range. For a 1% resolution of any signal, the allowable output error is 4.32mV x K. Log conformity contributes 2.17mV x K (0.5%) over this range. The remaining error with K = 5/4 is 2.69mV and should correspond to less than the LSB of the converter. With a 5 volt output range 2.69mV corresponds just over the LSB of an 11-bit converter. Thus the 757 module can compress the data for use with a 12 bit A/D (such as Analog Devices AD574JD) to obtain the desired 1% resolution.

Absorbence Measurements – Critical properties of materials which are of particular interest in the fields of chemistry, medicine, spectrometry and pollution control are characterized by absorbence. The relationship between absorbence, A, and light intensity, I, is: $A = \log I_O/I_T$ where I_O = intensity of incident light, and I_T = intensity of transmitted light.

Figure 6 shows the 757 log-ratio module used in such a photometer application. Two inputs represent the intensities of light transmitted through space and through a medium that absorbs light. The absorbence of the medium is given by the formula

$$A = \log \frac{I_{SIGNAL}}{I_{REFERENCE}}$$

where I_{SIGNAL} and $I_{REFERENCE}$ are the currents representing the light intensities.

The transducers used in this application are photodiodes, which provide a short-circuit current proportional to the intensity of applied light. The lowest value of absorbence is determined by the value of I_{REF}, since when $I_{SIG} = I_{REF}$, A = 0. The output of the log-ratio module is externally trimmed to 1V/decade and applied to the input of a 3½-digit DPM through the scaling network R1 and R2.

Model 757 was chosen for this design because it makes available both amplifier summing junctions. When the photodiodes are connected to the summing junctions, they are operated in the short-circuit mode, that is, with zero volts across the diodes. Short-circuit loading is necessary, because accuracy of the photodiodes can be degraded several percent when operated with as little as 100mV across the diode junction.

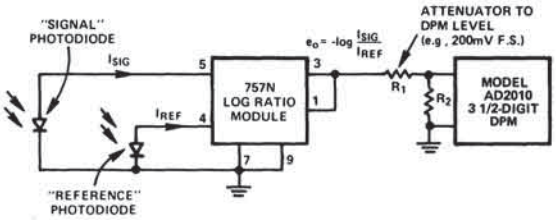


Figure 6. Model 757N Applied to Absorbence Measurements

INTERCONNECTION GUIDELINES

Model 757 is a complete log ratio amplifier that requires no additional frequency compensation for proper operation.

Input Capacitance – Model 757 is able to operate with 1000pF at both input terminals. Therefore, the 757 can be used in applications requiring long cable lengths between the module and the signal transducers.

Input-to-Output Capacitance – When using a log ratio module the user should take care in system configurations to avoid excessive stray capacitance between input and output terminals. Such precautions include avoiding running input and output signal lines close together. If long cable runs are required where inputs and output are closely bundled together, it is advisable to enclose the inputs and/or output in separate, grounded electrostatic shields. By observing simple rules of good circuit layout, problems with oscillations that may result from excessive input-to-output capacitance can easily be avoided. Model 757 can accommodate up to 33pF of input-to-output capacitance without oscillation.

Leakage Resistance – Since model 757 can operate at extremely low input current levels, precautions must be taken to prevent current leakage into the input terminals. Such leakage can cause errors when small input or reference currents are used. This problem may arise on printed circuit layouts if the inputs are run too close to the power supply busses. Providing an etched guard around the input lines, connected to analog signal ground will also reduce unwanted current leakage.

RMS-to-DC Converters
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8

Selection Guide
RMS-to-DC Converters

Model	Full-Scale Range V rms	Accuracy mV ± % of Reading	Frequency Response MHz	dB Output	Page	Notes
AD536A	7	2.0 ± 0.2	2	X	8 – 5	General purpose
AD636	0.2	0.2 ± 0.5	1.3	X	8 – 11	
AD637	7	0.5 ± 0.2	8	X	8 – 17	Highest accuracy
AD736	0.2	0.3 ± 0.3	0.19		8 – 25	Buffered output, low power
AD737	0.2	0.2 ± 0.3	0.19		8 – 29	Unbuffered output, low power

Orientation
RMS-to-DC Converters

RMS-to-DC converters continuously compute the instantaneous square of the input signal, average it, and take the square root of the result, to provide a dc voltage proportional to the rms of the input (and, in the case of the AD536, AD636 and AD736, an auxiliary dc voltage that is proportional to the *log* of the rms, for dB measurements).

Excellent pretrimmed performance, improvable by simple optional trims, makes these devices ideal for all types of laboratory and OEM rms instrumentation where amplitude measurements must be made with high accuracy, independently of waveshape.

An alternative to rms that has been widely used in the past, principally for measurements on sine waves, is mean absolute-deviation, or "ac average." It is performed by taking the absolute value of a signal (i.e., rectifying it) filtering it and scaling it by the ratio of rms to m.a.d. for sine waves, 1.111, so that it reads correctly (for undistorted sine waves). Unfortunately, this ratio varies widely as a function of the waveform; it will give grossly incorrect results in many cases. The table shows a few representative examples comparing rms with m.a.d.

An important application is noise measurement – for example, thermal noise, transistor noise, and switch-contact noise. True rms measurement is a technique that provides consistent theoretically valid measurements of noise amplitude (standard deviation) from different sources having different properties.

True rms devices are also useful for measuring electrical signals derived from mechanical phenomena, such as strain, stress, vibration, shock, expansion, bearing noise and acoustical noise.

The electrical signals produced by these mechanical actions are often noisy, nonperiodic, nonsinusoidal, and superimposed on dc levels, and require true rms for consistent, valid, accurate measurements. RMS converters are also useful for accurate measurements on low-repetition-rate pulse-trains having high *crest factors* (ratio of peak to rms), and for measurements of the energy content of SCR waveforms at differing firing angles.

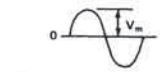
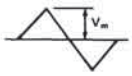
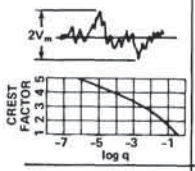
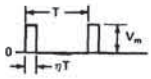
The basic approach used in these converters for computing the rms is to take the absolute value, square it and divide by the fed-back output (using the logarithmic characteristics of transistor junctions), and filter the result. The resulting approximation

$$E_o = \text{Avg.}\left[\frac{V_{in}^2}{E_o}\right] \cong \sqrt{\text{Avg.}\,(V_{in}^2)}$$

is valid if the averaging time constant is sufficiently long compared with the periods of the lowest frequency ac components of the signal.

The simplest form of averaging involves a single-pole filter using an external filtering capacitor (C_{AV}). Increased values of capacitance for filtering will improve the accuracy for low frequency rms measurements and provide reduced ripple at the output, but at the cost of increased settling time. For fastest settling and minimum ripple, an additional stage of 2-pole filtering is useful. The additional filtering permits improvement of settling time or reduction of ripple (or both) because of substantial reduction of C_{AV} .

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WAVEFORM		RMS	MAD	$\frac{\text{RMS}}{\text{MAD}}$	CREST FACTOR
	SINE WAVE	$\frac{V_m}{\sqrt{2}}$ 0 707 V_m	$\frac{2}{\pi} V_m$ 0 637 V_m	$\frac{\pi}{2\sqrt{2}} = 1\,111$	$\sqrt{2} = 1\,414$
	SYMMETRICAL SQUARE WAVE OR DC	V_m	V_m	1	1
	TRIANGULAR WAVE OR SAWTOOTH	$\frac{V_m}{\sqrt{3}}$	$\frac{V_m}{2}$	$\frac{2}{\sqrt{3}} = 1\,155$	$\sqrt{3} = 1\,732$
	GAUSSIAN NOISE CREST FACTOR IS THEORETICALLY UNLIMITED. q IS THE FRACTION OF TIME DURING WHICH GREATER PEAKS CAN BE EXPECTED TO OCCUR	RMS	$\sqrt{\frac{2}{\pi}}$ RMS = 0 798 RMS	$\sqrt{\frac{\pi}{2}}$ 1 253	C.F / q 1 / 32% 2 / 4.6% 3 / 0.37% 3 3 / 0.1% 3 9 / 0 01% 4 / 63ppm 4.4 / 10ppm 4.9 / 1ppm 6 / 2x10⁹
	PULSE TRAIN η / MARK/SPACE 1 / ∞ 0.25 / 0 3333 0.0625 / 0.0667 0.0156 / 0 0159 0.01 / 0.0101	$V_m\sqrt{\eta}$ V_m 0.5V_m 0.25V_m 0.125V_m 0.1V_m	$V_m\eta$ V_m 0.25V_m 0.0625V_m 0 0156V_m 0.01V_m	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10	$\frac{1}{\sqrt{\eta}}$ 1 2 4 8 10

η. "DUTY CYCLE"

PERFORMANCE SPECIFICATIONS

Considerable information regarding rms-to-dc converter circuit design, performance, selection and applications is to be found in the *RMS-to-DC Conversion Application Guide*.[1] In addition, useful applications information can be found in the *Nonlinear Circuits Handbook*.[2]

The most-salient feature of a true rms-to-dc converter is that *it ideally has no error due to an indirect approximation to the rms.* Static errors are due only to scale-factor, linearity and offset errors; dynamic errors are due to insufficient averaging time at the low end and finite bandwidth and slewing rate at the upper end. Linearity errors affect crest factor in midband. Dynamic errors are also a function of signal amplitude, due in part to the variation of bandwidth of the "log" transistors with signal level.

Total Error, Internal Trim, a specification for quick reference, is the maximum deviation of the dc component of the output voltage from the theoretical output value over a specified range of signal amplitude and frequency. It is shown as the sum of a fixed error and a component proportional to the theoretical output (% of reading). It is specified for a sinusoidal input in a given frequency and amplitude range. The fixed error component includes all offset errors and irreducible nonlinearities; the %-of-reading component includes the linear scale-factor error.

Total Error, External Adjustment is the amount by which the output may differ from the theoretical value when the output offset and scale factor have been trimmed. Note that the fixed error-component cannot be reduced to zero, even though the output offset can be nulled at zero input. This is because of residual input offsets and inherent nonlinearities in the converter.

Total Error vs. Temperature (T_{min} to T_{max}) is the average change of %-of-full-scale error component plus the average change of percent-of-reading error component per degree Celsius, over the rated temperature range.

Frequency for 1%-of-Reading Error is the minimum value of frequency (at the high end) at which the error increases from the midband value by 1% of reading. It is a function of peak-to-peak input amplitude.

Frequency for −3dB Reading Error is the minimum value of frequency (at the high end) at which the error may equal −30% of reading. It is a function of amplitude.

Crest Factor (to a property of the signal) is the ratio of peak signal voltage to the ideal value of rms; the specified value of crest factor is that for which the error is maintained within specified limits at a given rms level for a worst-case – rectangular pulse – input signal.

Averaging Time Constant and External Capacitor: The time constant of the internal averaging filter, and the increase of time constant per μF of added external capacitance (C_{AV}).

Input: The voltage range over which specified operation is obtained, the maximum voltage for which the unit operates, the maximum safe input voltage, and the effective input resistance.

Output: The maximum output range for rated performance, the minimum current guaranteed available at full-scale output voltage, and the source resistance of the output circuit.

Power Supply: Power-supply range for specified performance, power-supply range for operation and quiescent current drain.

Temperature Range: The range of temperature variation for operation within specifications. Temperature coefficients are determined by three-point measurements (T_H − 25°C), (25°C − T_L), when measured.

[1] ***RMS-to-DC Conversion Application Guide 2nd Edition*, by C. Kitchin and L. Counts (1986-61 pages). Available free from Analog Devices.**
[2] ***Nonlinear Circuits Handbook*, Analog Devices, Inc., 1974, 1976, 536pp, edited by D.H. Sheingold. ($5.95).**

ANALOG DEVICES

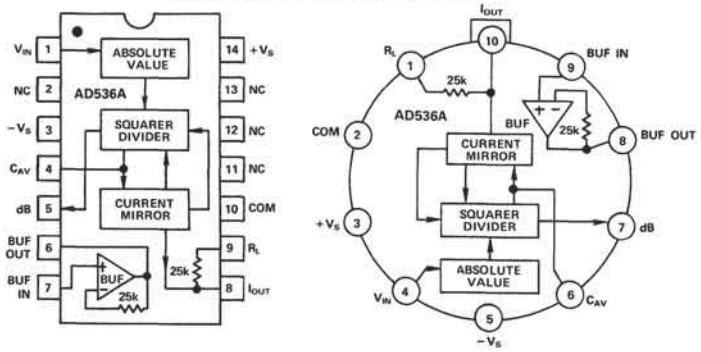
Integrated Circuit True rms-to-dc Converter

AD536A

FEATURES

- True rms-to-dc Conversion
- Laser-Trimmed to High Accuracy
  - 0.2% max Error (AD536AK)
  - 0.5% max Error (AD536AJ)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 450kHz Bandwidth: $V_{rms} > 100mV$
  - 2MHz Bandwidth: $V_{rms} > 1V$
  - Signal Crest Factor of 7 for 1% Error
- dB Output with 60dB Range
- Low Power: 1.2mA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- -55°C to +125°C Operation (AD536AS)
- Low Cost

AD536A PIN CONNECTION AND FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD536A is a complete monolithic integrated circuit which performs true rms-to-dc conversion. It offers performance which is comparable or superior to that of hybrid or modular units costing much more. The AD536A directly computes the true rms value of any complex input waveform containing ac and dc components. It has a crest factor compensation scheme which allows measurements with 1% error at crest factors up to 7. The wide bandwidth of the device extends the measurement capability to 300kHz with 3dB error for signal levels above 100mV.

An important feature of the AD536A not previously available in rms converters is an auxiliary dB output. The logarithm of the rms output signal is brought out to a separate pin to allow the dB conversion, with a useful dynamic range of 60dB. Using an externally supplied reference current, the 0dB level can be conveniently set by the user to correspond to any input level from 0.1 to 2 volts rms.

The AD536A is laser trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full scale accuracy at 7V rms. As a result, no external trims are required to achieve the rated accuracy of the unit.

There is full protection for both inputs and outputs. The input circuitry can take overload voltages well beyond the supply levels. Loss of supply voltage with inputs connected will not cause unit failure. The output is short-circuit protected.

The AD536A is available in two accuracy grades (J, K) for commercial temperature range (0 to +70°C) applications, and one grade (S) rated for the -55°C to +125°C extended range. The AD536AK offers a maximum total error of ±2mV ±0.2% of reading and the AD536AJ and AD536AS have maximum errors of ±5mV ±0.5% of reading. All three versions are available in either a hermetically sealed 14-pin DIP or 10-pin TO-100 metal can.

PRODUCT HIGHLIGHTS

1. The AD536A computes the true root-mean-square level of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it relates directly to the power of the signal. The rms value of a statistical signal also relates to its standard deviation.
2. The crest factor of a waveform is the ratio of the peak signal swing to the rms value. The crest factor compensation scheme of the AD536A allows measurement of highly complex signals with wide dynamic range.
3. The only external component required to perform measurements to the fully specified accuracy is the capacitor which sets the averaging period. The value of this capacitor determines the low frequency ac accuracy, ripple level and settling time.
4. The AD536A will operate equally well from split supplies or a single supply with total supply levels from 5 to 36 volts. The one milliampere quiescent supply current makes the device well-suited for a wide variety of remote controllers and battery powered instruments.
5. The AD536A directly replaces the AD536, and provides improved bandwidth and temperature drift specifications.

8

SPECIFICATIONS (@ +25°C, and ±15V dc unless otherwise noted)

Model	AD536AJ Min	AD536AJ Typ	AD536AJ Max	AD536AK Min	AD536AK Typ	AD536AK Max	AD536AS Min	AD536AS Typ	AD536AS Max	Units
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Figure 1)			±5 ±0.5			±2 ±0.2			±5 ±0.5	mV ± % of Reading
vs Temperature, T_{min} to +70°C			±0 1 ±0 01			±0.05 ±0.005			±0.1 ±0.005	mV ± % of Reading/°C
+70°C to +125°C									±0.3 ±0.005	mV ± % of Reading/°C
vs Supply Voltage		±0 1 ±0.01			±0.1 ±0 01			±0.1 ±0 01		mV ± % of Reading/V
dc Reversal Error		±0.2			±0 1			±0.2		± % of Reading
Total Error, External Trim[1] (Figure 2)		±3 ±0 3			±2 ±0.1			±3 ±0.3		mV ± % of Reading
ERROR VS CREST FACTOR[2]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		−0.1			−0.1			−0.1		% of Reading
Crest Factor = 7		−1 0			−1.0			−1 0		% of Reading
FREQUENCY RESPONSE[3]										
Bandwidth for 1% additional error (0.09dB)										
V_{IN} = 10mV		5			5			5		kHz
V_{IN} = 100mV		45			45			45		kHz
V_{IN} = 1V		120			120			120		kHz
±3dB Bandwidth										
V_{IN} = 10mV		90			90			90		kHz
V_{IN} = 100mV		450			450			450		kHz
V_{IN} = 1V		2 3			2.3			2.3		MHz
AVERAGING TIME CONSTANT (Figure 5)		25			25			25		ms/μF CAV
INPUT CHARACTERISTICS										
Signal Range, ± 15V Supplies										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±20			±20			±20	V peak
Continuous rms Level, ± 5V Supplies		0 to 2			0 to 2			0 to 2		V rms
Peak Transient Input, ± 5V Supplies			±7			±7			±7	V peak
Maximum Continuous Nondestructive Input Level (All Supply Voltages)			±25			±25			±25	V peak
Input Resistance	13 33	16 67	20	13 33	16.67	20	13.33	16 67	20	kΩ
Input Offset Voltage		0 8	±2		0 5	±1		0 8	±2	mV
OUTPUT CHARACTERISTICS										
Offset Voltage, V_{IN} = COM (Figure 1)		±1	±2		±0 5	±1			±2	mV
vs. Temperature		±0 1			±0 1				±0.2	mV/°C
vs Supply Voltage		±0 1			±0 1			±0.2		mV/V
Voltage Swing, ± 15V Supplies	0 to +11	+12 5		0 to +11	+12.5		0 to +11	+12.5		V
± 5V Supply	0 to +2			0 to +2			0 to +2			V
dB OUTPUT (Figure 12)										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±0.4	±0.6		±0 2	±0.3		±0 5	±0.6	dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor TC (Uncompensated, see Figure 12 for Temperature Compensation)		−0 033			−0.033			−0.033		dB/°C
		+0 33			+0.33			+0.33		% of Reading/°C
I_{RTF} for 0dB = 1V rms	5	20	80	5	20	80	5	20	80	μA
I_{RTF} Range	1		100	1		100	1		100	μA
I_{OUT} TERMINAL										
I_{OUT} Scale Factor		40			40			40		μA/V rms
I_{OUT} Scale Factor Tolerance		±10	±20		±10	±20		±10	±20	%
Output Resistance	20	25	30	20	25	30	20	25	30	kΩ
Voltage Compliance		$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2 5)			$-V_S$ to ($+V_S$ −2 5V)		V
BUFFER AMPLIFIER										
Input and Output Voltage Range		$-V_S$ to ($+V_S$ −2 5V)			$-V_S$ to ($+V_S$ −2.5V)			$-V_S$ to ($+V_S$ −2 5V)		V
Input Offset Voltage, R_S = 25k		±0.5	±4		±0.5	±4		±0.5	±4	mV
Input Bias Current		20	60		20	60		20	60	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5mA, −130μA)			(+5mA, −130μA)			(+5mA, −130μA)			
Short Circuit Current		20			20			20		mA
Output Resistance			0 5			0 5			0 5	Ω
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[4]		5			5			5		V/μs
POWER SUPPLY										
Voltage Rated Performance		±15			±15			±15		V
Dual Supply	±3 0		±18	±3 0		±18	±3 0		±18	V
Single Supply	+5		+36	+5		+36	+5		+36	V
Quiescent Current										
Total V_S, 5V to 36V, T_{min} to T_{max}		1 2	2		1 2	2		1 2	2	mA
TEMPERATURE RANGE										
Rated Performance	0		+70	0		+70	−55		+125	°C
Storage	−55		+150	−55		+150	−55		+150	°C
PACKAGE OPTIONS[5]										
Ceramic DIP (D-14)		AD536AJD			AD536AKD			AD536ASD		
Metal Can TO-100 (H-10A)		AD536AJH			AD536AKH			AD536ASH		

NOTES

[1]Accuracy is specified for 0 to 7V rms, dc or 1kHz sinewave input with the AD536A connected as in the figure referenced

[2]Error vs crest factor is specified as an additional error for 1V rms rectangular pulse input, pulse width = 200μs

[3]Input voltages are expressed in volts rms, and error is percent of reading

[4]With 2k external pulldown resistor

[5]See Section 16 for package outline information

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test Results from those tests are used to calculate outgoing quality levels All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units

STANDARD CONNECTION

The AD536A is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD536A will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD536A is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible.

The input and output signal ranges are a function of the supply voltages; these ranges are shown in Figure 16. The AD536A can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 25k resistor. The buffer amplifier can then be used for other purposes. Further the AD536A can be used in a current output mode by disconnecting the 25k resistor from ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 40μA per volt rms input, positive out.

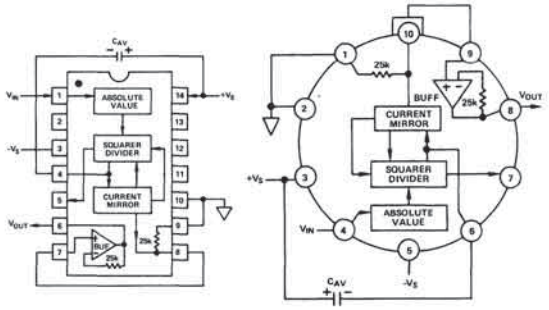


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD536A, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. Note that the offset trim circuit adds 365Ω in series with the internal 25kΩ resistor. This will cause a 1.5% increase in scale factor, which is trimmed out by using R_1 as shown. Range of scale factor adjustment is ±1.5%.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 1.000V dc input should give 1.000V dc output. Of course, a ±1.000V peak-to-peak sinewave should give a 0.707V dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

The major advantage of external trimming is to optimize device performance for a reduced signal range; the AD536A is internally trimmed for a 7V rms full scale range.

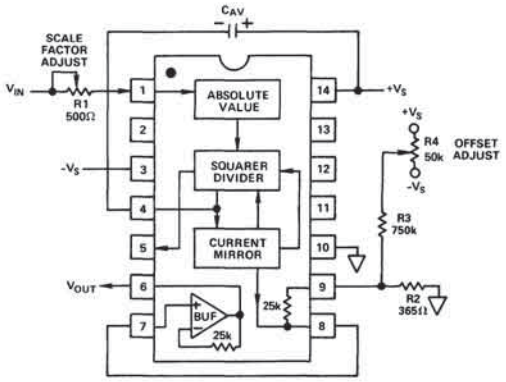


Figure 2. Optional External Gain and Output Offset Trims

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 require the use of approximately symmetrical dual supplies. The AD536A can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. The major limitation of this connection is that only ac signals can be measured since the differential input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 5 microamps of current flows into pin 10 (pin 2 on the "H" package). AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 16.7kΩ; for a cut-off at 10Hz, C_2 should be 1μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The input and output signal ranges are shown in Figure 16. The load resistor, R_L, is necessary to provide output sink current.

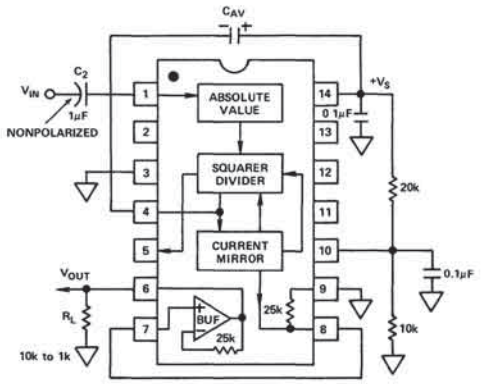


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD536A will compute the rms of both ac and dc signals. If the input is a slowly-varying dc, the output of the AD536A will track the input exactly. At higher frequencies, the average output of the AD536A will approach the rms value of the input signal. The actual output of the AD536A will differ from the ideal output by a dc (or average) error and some amount of ripple, as demonstrated in Figure 4.

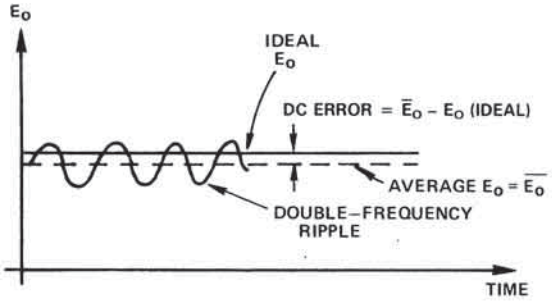


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield a given percent dc error above a given frequency using the standard rms connection.

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4μF capacitor (time constant = 25ms per μF).

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows that the relationship between C_{AV} and 1% settling time is 115 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

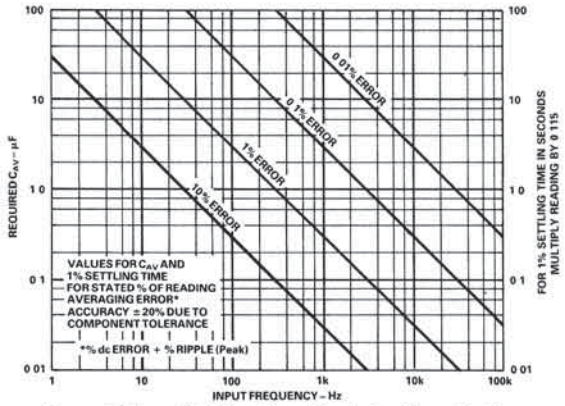


Figure 5. Error/Settling Time Graph for Use with the Standard rms Connection in Figure 1

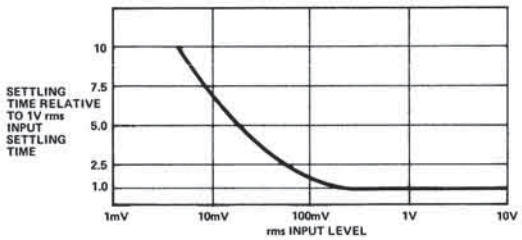


Figure 6. Settling Time vs Input Level

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately twice the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with C_{AV} = 1μF and C_2 = 2.2μF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

For a more detailed explanation of these topics refer to the *RMS to DC Conversion Application Guide 2nd Edition*, available from Analog Devices.

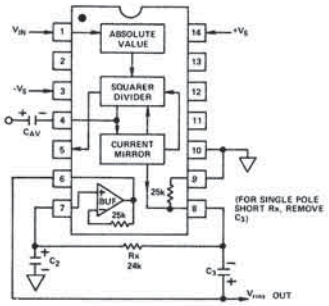


Figure 7. 2 Pole "Post" Filter

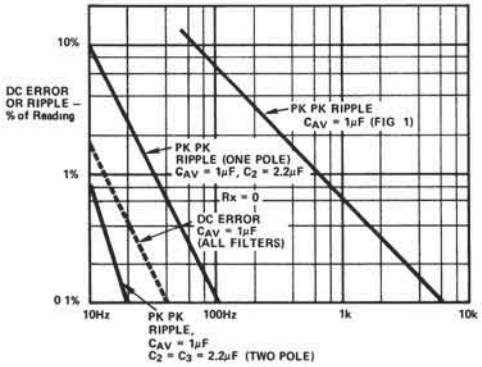


Figure 8. Performance Features of Various Filter Types

AD536A PRINCIPLE OF OPERATION

The AD536A embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD536A follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD536A; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.} [I_1^2/I_4] = I_1 \text{ rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD536A thus results:

$$V_{OUT} = 2R_2 I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to -log V_{IN}. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

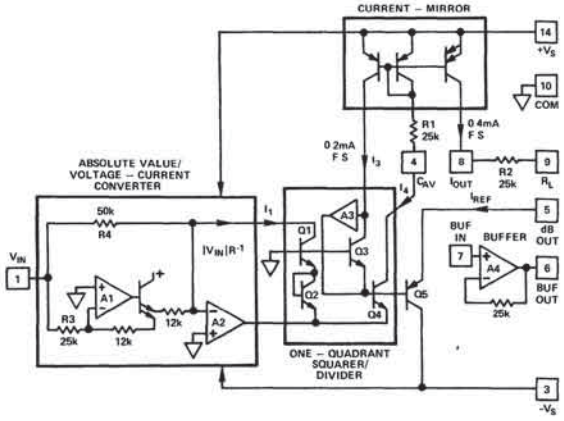


Figure 9. Simplified Schematic

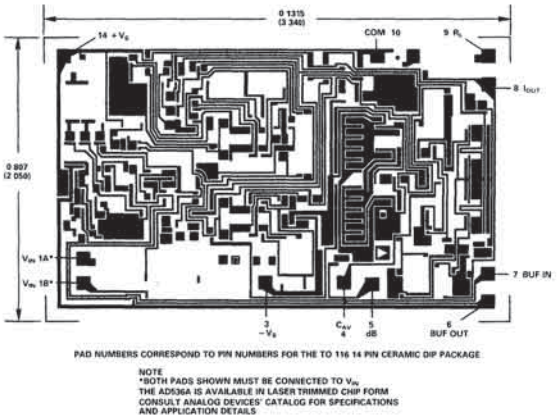


Figure 10. Chip Dimensions and Pad Layout. Dimensions shown in inches and (mm).

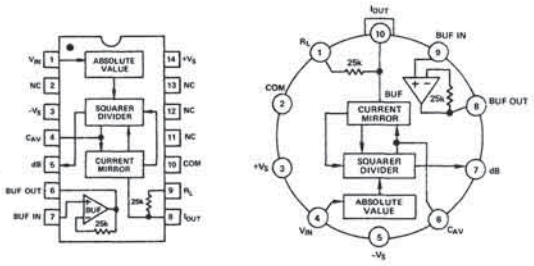


Figure 11. AD536A Pin Connections and Functional Diagram

8

CONNECTIONS FOR dB OPERATION

A powerful feature added to the AD536A is the logarithmic or decibel output. The internal circuit computing dB works accurately over a 60dB range. The connections for dB measurements are shown in Figure 12. The user selects the 0dB level by adjusting R_1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer-divider at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the +0.33%/°C scale factor drift of the dB output pin. The special T.C. resistor, R_2, is available from Tel Labs in Londenderry, N.H. (model Q-81) or from Precision Resistor Inc., Hillside, N.J. (model PT146). The averaged temperature coefficients of resistors R_2 and R_3 develop the +3300ppm needed to reverse compensate the dB output. The linear rms output is available at pin 8 on DIP or pin 10 on header device with an output impedance of 25kΩ; thus some applications may require an additional buffer amplifier if this output is desired.

dB Calibration:

1. Set V_{IN} = 1.00V dc or 1.00V rms
2. Adjust R_1 for dB out = 0.00V
3. Set V_{IN} = +0.1V dc or 0.10V rms
4. Adjust R_5 for dB out = -2.00V

Any other desired 0dB reference level can be used by setting V_{IN} and adjusting R_1 accordingly. Note that adjusting R_5 for the proper gain automatically gives the correct temperature compensation.

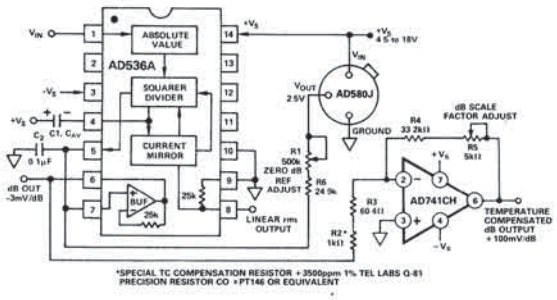


Figure 12. Temperature Compensated dB Output Circuit

FREQUENCY RESPONSE

The AD536A utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD536A at input levels from 10 millivolts to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and 3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 120kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to only 5kHz.

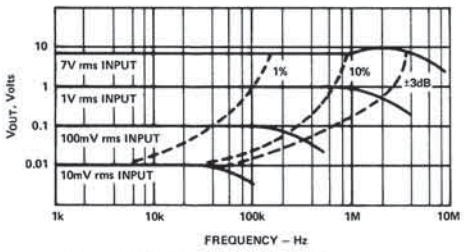


Figure 13. High Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 14 is a curve of reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 11 while maintaining a constant 1 volt rms input amplitude.

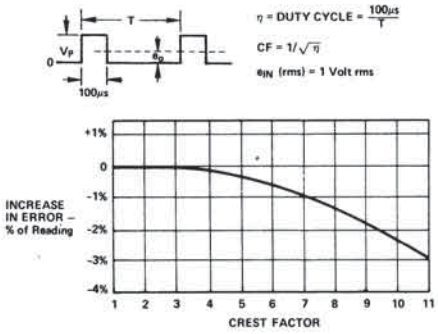


Figure 14. Error vs. Crest Factor

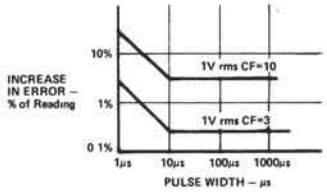


Figure 15. AD536A Error vs. Pulse Width Rectangular Pulse

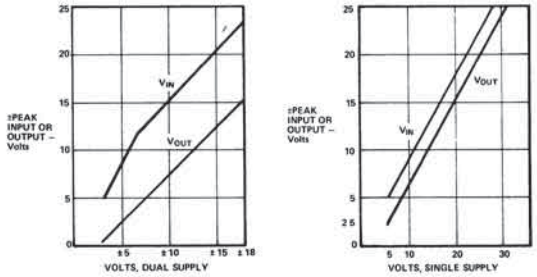


Figure 16. AD536A Input and Output Voltage Ranges vs. Supply

ANALOG DEVICES

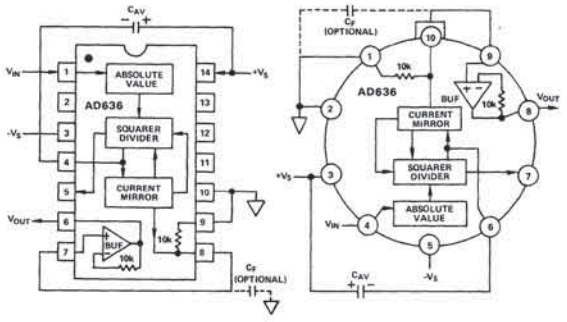
Low Level True rms-to-dc Converter

AD636

FEATURES

- True rms-to-dc Conversion
- 200mV Full Scale
- Laser-Trimmed to High Accuracy
  - 0.3% max Error (AD636K)
  - 0.6% max Error (AD636J)
- Wide Response Capability:
  - Computes rms of ac and dc Signals
  - 1MHz -3dB Bandwidth: V_{rms}>100mV
  - Signal Crest Factor of 6 for 0.5% Error
- dB Output with 50dB Range
- Low Power: 800μA Quiescent Current
- Single or Dual Supply Operation
- Monolithic Integrated Circuit
- Low Cost
- Available in Chip Form

AD636 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD636 is a low power monolithic IC which performs true rms-to-dc conversion on low level signals. It offers performance which is comparable or superior to that of hybrid and modular converters costing much more. The AD636 is specified for a signal range of 0 to 200 millivolts rms. Crest factors up to 6 can be accommodated with less than 0.5% additional error, allowing accurate measurement of complex input waveforms.

The low power supply current requirement of the AD636, typically 800μA, allows it to be used in battery-powered portable instruments. A wide range of power supplies can be used, from ±2.5V to ±16.5V or a single +5V to +24V supply. The input and output terminals are fully protected; the input signal can exceed the power supply with no damage to the device (allowing the presence of input signals in the absence of supply voltage) and the output buffer amplifier is short-circuit protected.

The AD636 includes an auxiliary dB output. This signal is derived from an internal circuit point which represents the logarithm of the rms output. The 0dB reference level is set by an externally supplied current and can be selected by the user to correspond to any input level from 0dBm (774.6mV) to -20dBm (77.46mV). Frequency response ranges from 1.2MHz at a 0dBm level to over 10kHz at -50dBm.

The AD636 is designed for ease of use. The device is factory-trimmed at the wafer level for input and output offset, positive and negative waveform symmetry (dc reversal error), and full scale accuracy at 200mV rms. Thus no external trims are required to achieve full rated accuracy.

The AD636 is available in two accuracy grades; the AD636J has a total error of ±0.5mV ±0.6% of reading, and the AD636K is accurate within ±0.2mV to ±0.3% of reading. Both versions are specified for the 0 to +70°C temperature range, and are offered in either a hermetically sealed 14-pin DIP or a 10-pin TO-100 metal can.

PRODUCT HIGHLIGHTS

1. The AD636 computes the true root-mean-square of a complex ac (or ac plus dc) input signal and gives an equivalent dc output level. The true rms value of a waveform is a more useful quantity than the average rectified value since it is a measure of the power in the signal. The rms value of an ac-coupled signal is also its standard deviation.
2. The 200 millivolt full scale range of the AD636 is compatible with many popular display-oriented analog-to-digital converters. The low power supply current requirement permits use in battery-powered hand-held instruments.
3. The only external component required to perform measurements to the fully specified accuracy is the averaging capacitor. The value of this capacitor can be selected for the desired trade-off of low frequency accuracy, ripple, and settling time.
4. The on-chip buffer amplifier can be used to buffer either the input or the output. Used as an input buffer, it provides accurate performance from standard 10MΩ input attenuators. As an output buffer, it can supply up to 5 milliamps of output current.
5. The AD636 will operate over a wide range of power supply voltages, including single +5V to +24V or split ±2.5V to ±16.5V sources. A standard 9V battery will provide several hundred hours of continuous operation.

8

SPECIFICATIONS (@ +25°C, and $+V_S = +3V$, $-V_S = -5V$ unless otherwise noted)

Model	AD636J Min	AD636J Typ	AD636J Max	AD636K Min	AD636K Typ	AD636K Max	Units
TRANSFER FUNCTION	$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			$V_{OUT} = \sqrt{avg.(V_{IN})^2}$			
CONVERSION ACCURACY							
Total Error, Internal Trim[1,2]			**±0.5 ±0.6**			**±0.2 ± 0.3**	mV ± % of Reading
vs. Temperature, 0 to +70°C			±0.1 ±0 01			±0.1 ±0.005	mV ± % of Reading/°C
vs. Supply Voltage		±0.1 ±0.01			±0.1 ±0.01		mV ± % of Reading/V
dc Reversal Error at 200mV		±0.2			±0.1		% of Reading
Total Error, External Trim[1]		±0.3 ±0.1			±0.1 ±0.1		mV ± % of Reading
ERROR VS. CREST FACTOR[3]							
Crest Factor 1 to 2	Specified Accuracy			Specified Accuracy			
Crest Factor = 3		−0.2			−0.2		% of Reading
Crest Factor = 6		−0.5			−0.5		% of Reading
AVERAGING TIME CONSTANT		25			25		ms/μF CAV
INPUT CHARACTERISTICS							
Signal Range, All Supplies							
Continuous rms Level		0 to 200			0 to 200		mV rms
Peak Transient Inputs							
+3V, −5V Supply			±2.8			±2.8	V pk
±2.5V Supply			±2.0			±2.0	V pk
±5V Supply			±5.0			±5.0	V pk
Maximum Continuous Non-Destructive							
Input Level (All Supply Voltages)			±12			±12	V pk
Input Resistance	5.33	6.67	8	5.33	6.67	8	kΩ
Input Offset Voltage			±0.5			±0.2	mV
FREQUENCY RESPONSE[2,4]							
Bandwidth for 1% additional error (0.09dB)							
V_{IN} = 10mV		14			14		kHz
V_{IN} = 100mV		90			90		kHz
V_{IN} = 200mV		130			130		kHz
±3dB Bandwidth							
V_{IN} = 10mV		100			100		kHz
V_{IN} = 100mV		900			900		MHz
V_{IN} = 200mV		1.5			1.5		MHz
OUTPUT CHARACTERISTICS[2]							
Offset Voltage, V_{IN} = COM			**±0.5**			**±0.2**	mV
vs Temperature		±10			±10		μV/°C
vs. Supply		±0.1			±0.1		mV/V
Voltage Swing							
+3V, −5V Supply	0 to +1.0			0 to +1.0			V
±5V to ±16.5V Supply	**0 to +1.0**	+1.4		**0 to +1.0**	+1.4		V
Output Impedance	8	10	12	8	10	12	kΩ
dB OUTPUT							
Error, V_{IN} = 7mV to 300mV rms		±0.3	**±0.5**		±0.1	**±0.2**	dB
Scale Factor		−3.0			−3.0		mV/dB
Scale Factor Temperature Coefficient		+0.33			+0.33		% of Reading/°C
		−0.033			−0.033		dB/°C
I_{REF} for 0dB = 1V rms	2	4	8	2	4	8	μA
I_{REF} Range	1		50	1		50	μA
I_{OUT} TERMINAL							
I_{OUT} Scale Factor		100			100		μA/V rms
I_{OUT} Scale Factor Tolerance	−20	±10	+20	−20	±10	+20	%
Output Resistance	8	10	12	8	10	12	kΩ
Voltage Compliance		$-V_S$ to ($+V_S$ −2V)			$-V_S$ to ($+V_S$ −2V)		V
BUFFER AMPLIFIER							
Input and Output Voltage Range	$-V_S$ to ($+V_S$ −2V)			$-V_S$ to ($+V_S$ −2V)			V
Input Offset Voltage, R_S = 10k		±0.8	**±2**		±0.5	**±1**	mV
Input Bias Current		20	**60**		20	**60**	nA
Input Resistance		10^8			10^8		Ω
Output Current	(+5mA, −130μA)			(+5mA, −130μA)			
Short Circuit Current		20			20		mA
Small Signal Bandwidth		1			1		MHz
Slew Rate[5]		5			5		V/μs
POWER SUPPLY							
Voltage, Rated Performance		+3, −5			+3, −5		V
Dual Suply	+2, −2.5		±16.5	+2, −2.5		±16.5	V
Single Suply	+5		+24	+5		+24	V
Quiescent Current[6]		0.80	**1.00**		0.80	**1.00**	mA
TEMPERATURE RANGE							
Rated Performance	0		+70	0		+70	°C
Storage	−55		+150	−55		+150	°C
PACKAGE OPTIONS[7]							
TO-116 (D-14)		AD636JD			AD636KD		
TL-100 (H-10A)		AD636JH			AD636KH		

NOTES

[1]Accuracy specified for 0 to 200mV rms, dc or 1kHz sinewave input. Accuracy is degraded at higher rms signal levels

[2]Measured at pin 8 of DIP (I_{OUT}), with pin 9 tied to common.

[3]Error vs. crest factor is specified as additional error for a 200mV rms rectangular pulse train, pulse width = 200μs.

[4]Input voltages are expressed in volts rms.

[5]With 10kΩ pull down resistor from pin 6 (BUF OUT) to $-V_S$.

[6]With BUF input tied to Common.

[7]See Section 16 for package outline information.

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

STANDARD CONNECTION

The AD636 is simple to connect for the majority of high accuracy rms measurements, requiring only an external capacitor to set the averaging time constant. The standard connection is shown in Figure 1. In this configuration, the AD636 will measure the rms of the ac and dc level present at the input, but will show an error for low frequency inputs as a function of the filter capacitor, C_{AV}, as shown in Figure 5. Thus, if a 4μF capacitor is used, the additional average error at 10Hz will be 0.1%, at 3Hz it will be 1%. The accuracy at higher frequencies will be according to specification. If it is desired to reject the dc input, a capacitor is added in series with with the input, as shown in Figure 3; the capacitor must be non-polar. If the AD636 is driven with power supplies with a considerable amount of high frequency ripple, it is advisable to bypass both supplies to ground with 0.1μF ceramic discs as near the device as possible. C_F is an optional output ripple filter, as discussed elsewhere in this data sheet.

The input and output signal ranges are a function of the supply voltages as detailed in the specifications. The AD636 can also be used in an unbuffered voltage output mode by disconnecting the input to the buffer. The output then appears unbuffered across the 10k resistor. The buffer amplifier can then be used for other purposes. Further, the AD636 can be used in a current output mode by disconnecting the 10k resistor from the ground. The output current is available at pin 8 (pin 10 on the "H" package) with a nominal scale of 100μA per volt rms input, positive out.

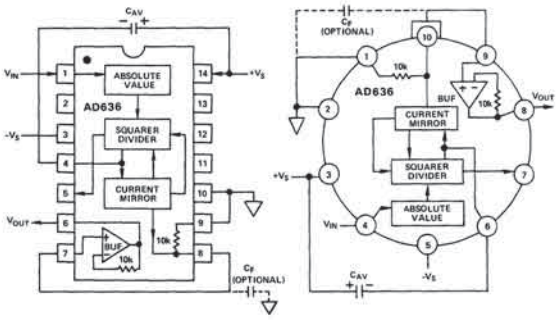


Figure 1. Standard rms Connection

OPTIONAL EXTERNAL TRIMS FOR HIGH ACCURACY

If it is desired to improve the accuracy of the AD636, the external trims shown in Figure 2 can be added. R_4 is used to trim the offset. The scale factor is trimmed by using R_1 as shown. The insertion of R_2 allows R_1 to either increase or decrease the scale factor by ±1.5%.

The trimming procedure is as follows:

1. Ground the input signal, V_{IN}, and adjust R_4 to give zero volts output from pin 6. Alternatively, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input level to V_{IN}, either dc or a calibrated ac signal (1kHz is the optimum frequency); then trim R_1 to give the correct output from pin 6, i.e., 200mV dc input should give 200mV dc output. Of course, a ±200mV peak-to-peak sinewave should give a 141.4mV dc output. The remaining errors, as given in the specifications, are due to the nonlinearity.

SINGLE SUPPLY CONNECTION

The applications in Figures 1 and 2 assume the use of dual power supplies. The AD636 can also be used with only a single positive supply down to +5 volts, as shown in Figure 3. Figure 3 is optimized for use with a 9 volt battery. The major limitation of this connection is that only ac signals can be measured since the input stage must be biased off ground for proper operation. This biasing is done at pin 10; thus it is critical that no extraneous signals be coupled into this point. Biasing can be accomplished by using a resistive divider between $+V_S$ and ground. The values of the resistors can be increased in the interest of lowered power consumption, since only 1 microamp of current flows into pin 10 (pin 2 on the "H" package). Alternately, the COM pin of some CMOS ADCs provides a suitable artificial ground for the AD636. AC input coupling requires only capacitor C_2 as shown; a dc return is not necessary as it is provided internally. C_2 is selected for the proper low frequency break point with the input resistance of 6.7kΩ; for a cut-off at 10Hz, C_2 should be 3.3μF. The signal ranges in this connection are slightly more restricted than in the dual supply connection. The load resistor, R_L, is necessary to provide current sinking capability.

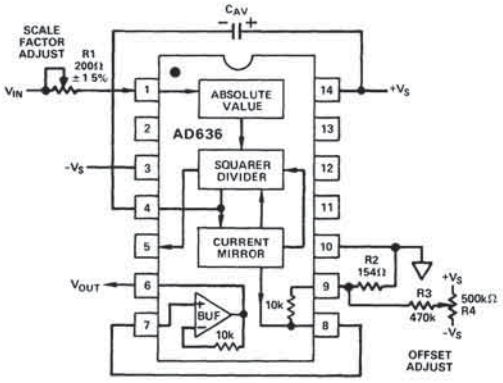


Figure 2. Optional External Gain and Output Offset Trims

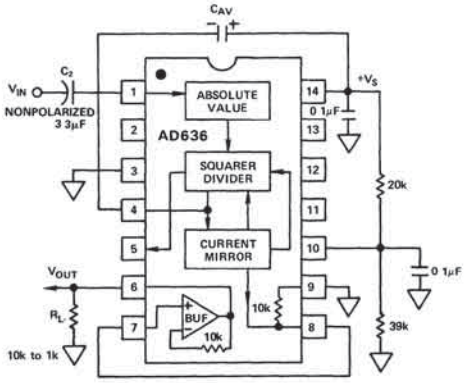


Figure 3. Single Supply Connection

CHOOSING THE AVERAGING TIME CONSTANT

The AD636 will compute the rms of both ac and dc signals. If the input is a slowly-varying dc voltage, the output of the AD636 will track the input exactly. At higher frequencies, the average output of the AD636 will approach the rms value of the input signal. The actual output of the AD636 will differ from the ideal output by a dc (or average) error and some amount of ripple, as demonstrated in Figure 4.

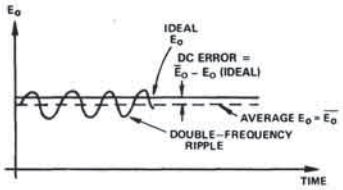


Figure 4. Typical Output Waveform for Sinusoidal Input

The dc error is dependent on the input signal frequency and the value of C_{AV}. Figure 5 can be used to determine the minimum value of C_{AV} which will yield a given % dc error above a given frequency using the standard rms connection.

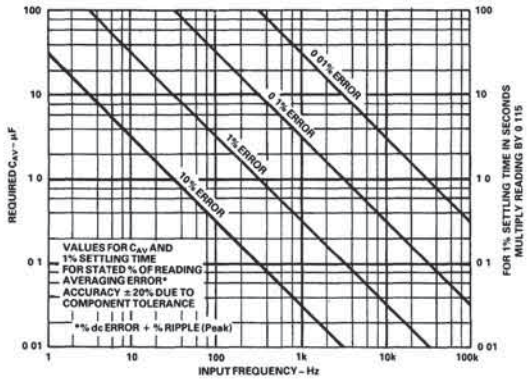


Figure 5. Error/Settling Time Graph for Use with the Standard rms Connection

The ac component of the output signal is the ripple. There are two ways to reduce the ripple. The first method involves using a large value of C_{AV}. Since the ripple is inversely proportional to C_{AV}, a tenfold increase in this capacitance will effect a tenfold reduction in ripple. When measuring waveforms with high crest factors, (such as low duty cycle pulse trains), the averaging time constant should be at least ten times the signal period. For example, a 100Hz pulse rate requires a 100ms time constant, which corresponds to a 4µF capacitor (time constant = 25ms per µF).

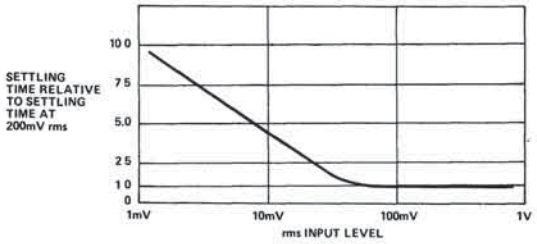


Figure 6. Settling Time vs. Input Level

The primary disadvantage in using a large C_{AV} to remove ripple is that the settling time for a step change in input level is increased proportionately. Figure 5 shows the the relationship between C_{AV} and 1% settling time is 115 milliseconds for each microfarad of C_{AV}. The settling time is twice as great for decreasing signals as for increasing signals (the values in Figure 5 are for decreasing signals). Settling time also increases for low signal levels, as shown in Figure 6.

A better method for reducing output ripple is the use of a "post-filter". Figure 7 shows a suggested circuit. If a single-pole filter is used (C_3 removed, R_X shorted), and C_2 is approximately 5 times the value of C_{AV}, the ripple is reduced as shown in Figure 8, and settling time is increased. For example, with C_{AV} = 1µF and C_2 = 4.7µF, the ripple for a 60Hz input is reduced from 10% of reading to approximately 0.3% of reading. The settling time, however, is increased by approximately a factor of 3. The values of C_{AV} and C_2 can therefore be reduced to permit faster settling times while still providing substantial ripple reduction.

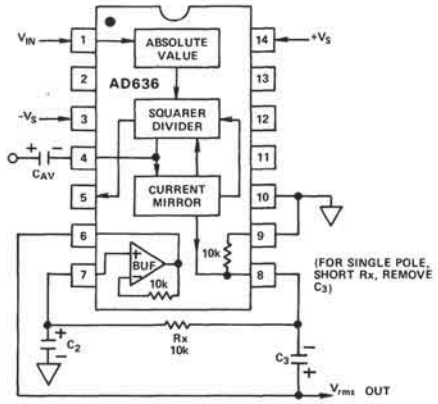


Figure 7. 2 Pole "Post" Filter

The two-pole post-filter uses an active filter stage to provide even greater ripple reduction without substantially increasing the settling times over a circuit with a one-pole filter. The values of C_{AV}, C_2, and C_3 can then be reduced to allow extremely fast settling times for a constant amount of ripple. Caution should be exercised in choosing the value of C_{AV}, since the dc error is dependent upon this value and is independent of the post filter.

For a more detailed explaination of these topics refer to the *RMS-to-DC Conversion Application Guide, 2nd Edition,* available from Analog Devices.

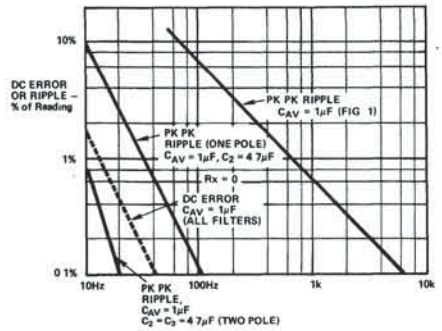


Figure 8. Performance Features of Various Filter Types

AD636 PRINCIPLE OF OPERATION

The AD636 embodies an implicit solution of the rms equation that overcomes the dynamic range as well as other limitations inherent in a straight-forward computation of rms. The actual computation performed by the AD636 follows the equation:

$$V_{rms} = \text{Avg.} \left[\frac{V_{IN}^2}{V_{rms}} \right]$$

Figure 9 is a simplified schematic of the AD636; it is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage, V_{IN}, which can be ac or dc, is converted to a unipolar current I_1, by the active rectifier A_1, A_2. I_1 drives one input of the squarer/divider, which has the transfer function:

$$I_4 = I_1^2 / I_3$$

The output current, I_4, of the squarer/divider drives the current mirror through a low pass filter formed by R_1 and the externally connected capacitor, C_{AV}. If the R_1, C_{AV} time constant is much greater than the longest period of the input signal, then I_4 is effectively averaged. The current mirror returns a current I_3, which equals Avg. $[I_4]$, back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = \text{Avg.} [I_1^2/I_4] = I_1 \text{ rms}$$

The current mirror also produces the output current, I_{OUT}, which equals $2I_4$. I_{OUT} can be used directly or converted to a voltage with R_2 and buffered by A_4 to provide a low impedance voltage output. The transfer function of the AD636 thus results:

$$V_{OUT} = 2R_2 I_{rms} = V_{IN\ rms}$$

The dB output is derived from the emitter of Q_3, since the voltage at this point is proportional to -log V_{IN}. Emitter follower, Q_5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current (I_{REF}) to Q_5 approximates I_3.

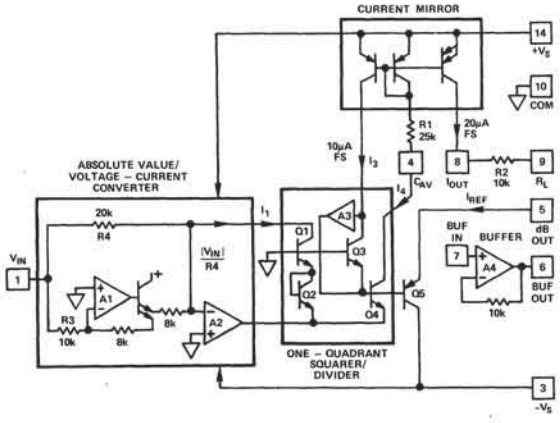


Figure 9. Simplified Schematic

THE AD636 BUFFER AMPLIFIER

The buffer amplifier included in the AD636 offers the user additional application flexibility. It is important to understand some of the characteristics of this amplifier to obtain optimum performance. Figure 10 shows a simplified schematic of the buffer.

Since the output of an rms-to-dc converter is always positive, it is not necessary to use a traditional complementary Class AB output stage. In the AD636 buffer, a Class A emitter follower is used instead. In addition to excellent positive output voltage swing, this configuration allows the output to swing fully down to ground in single-supply applications without the problems associated with most IC operational amplifiers.

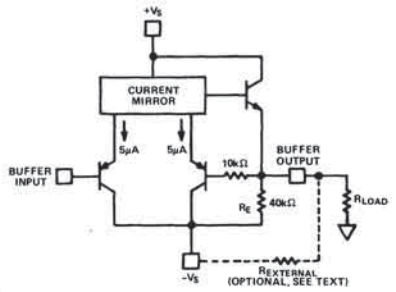


Figure 10. AD636 Buffer Amplifier Simplified Schematic

When this amplifier is used in dual-supply applications as an input buffer amplifier driving a load resistance referred to ground, steps must be taken to insure an adequate negative voltage swing. For negative outputs, current will flow from the load resistor through the 40kΩ emitter resistor, setting up a voltage divider between $-V_S$ and ground. This reduced effective $-V_S$ will limit the available negative output swing of the buffer. Addition of an external resistor in parallel with R_E alters this voltage divider such that increased negative swing is possible.

Figure 11 shows the value of $R_{EXTERNAL}$ for a particular ratio of V_{PEAK} to $-V_S$ for several values of R_{LOAD}. Addition of $R_{EXTERNAL}$ increases the quiescent current of the buffer amplifier by an amount equal to $R_{EXT}/-V_S$. Nominal buffer quiescent current with no $R_{EXTERNAL}$ is 30μA at $-V_S = -5V$.

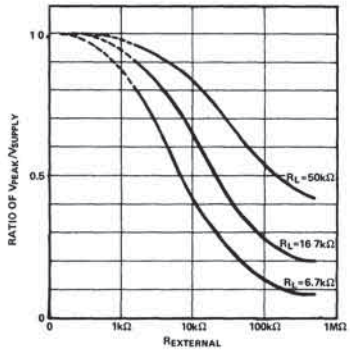


Figure 11. Ratio of Peak Negative Swing to $-V_S$ vs. $R_{EXTERNAL}$ for Several Load Resistances

FREQUENCY RESPONSE

The AD636 utilizes a logarithmic circuit in performing the implicit rms computation. As with any log circuit, bandwidth is proportional to signal level. The solid lines in the graph below represent the frequency response of the AD636 at input levels from 1 millivolt to 1 volt rms. The dashed lines indicate the upper frequency limits for 1%, 10%, and ±3dB of reading additional error. For example, note that a 1 volt rms signal will produce less than 1% of reading additional error up to 220kHz. A 10 millivolt signal can be measured with 1% of reading additional error (100μV) up to 14kHz.

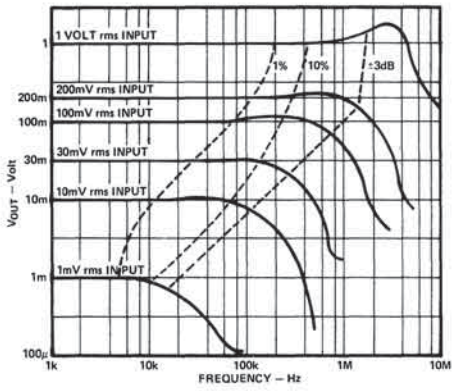


Figure 12. AD636 Frequency Response

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (<2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

Figure 13 is a curve of reading error for the AD636 for a 200mV rms input signal with crest factors from 1 to 7. A rectangular pulse train (pulse width 200μs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 7 while maintaining a constant 200mV rms input amplitude.

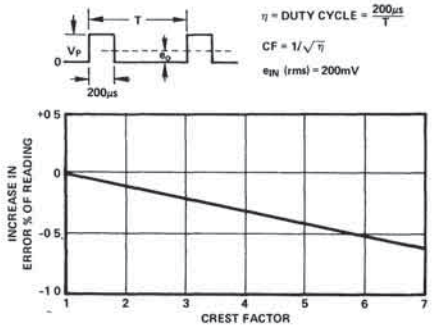


Figure 13. Error vs. Crest Factor

A COMPLETE AC DIGITAL VOLTMETER

Figure 14 shows a design for a complete low power ac digital voltmeter circuit based on the AD636. The 10MΩ input attenuator allows full scale ranges of 200mV, 2V, 20V and 200V rms. Signals are capacitively coupled to the AD636 buffer amplifier, which is connected in an ac bootstrapped configuration to minimize loading. The buffer then drives the 6.7kΩ input impedance of the AD636. The COM terminal of the ADC chip provides the false ground required by the AD636 for single supply operation. An AD589 1.2 volt reference diode is used to provide a stable 100 millivolt reference for the ADC in the linear rms mode; in the dB mode, a 1N4148 diode is inserted in series to provide correction for the temperature coefficient of the dB scale factor. Calibration of the meter is done by first adjusting offset pot R17 for a proper zero reading, then adjusting the R13 for an accurate readout at full scale.

Calibration of the dB range is accomplished by adjusting R9 for the desired 0dB reference point, then adjusting R14 for the desired dB scale factor (a scale of 10 counts per dB is convenient).

Total power supply current for this circuit is typically 2.8mA using a 7106-type ADC.

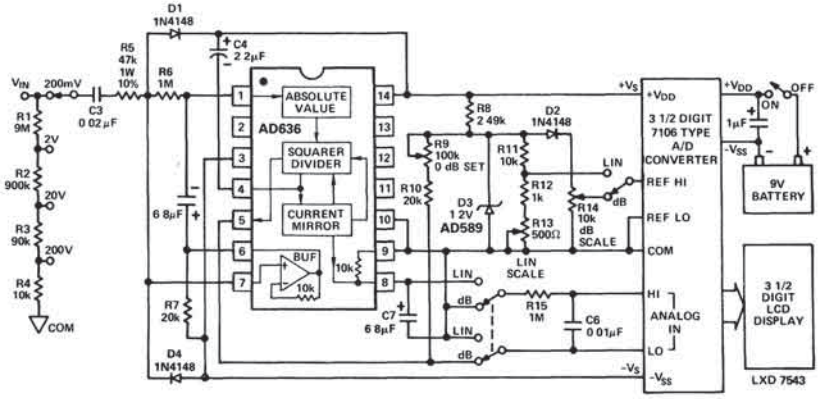


Figure 14. A Portable, High Z Input, rms DPM and dB Meter Circuit

ANALOG DEVICES

High Precision Wideband rms-to-dc Converter

AD637

FEATURES

High Accuracy
- **0.02% Max Nonlinearity, 0 to 2V rms Input**
- **0.10% Additional Error to Crest Factor of 3**

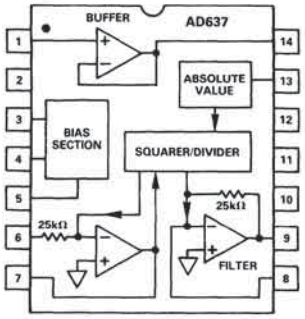
Wide Bandwidth
- **8MHz at 2V rms Input**
- **600kHz at 100mV rms**

Computes:
- **True rms**
- **Square**
- **Mean Square**
- **Absolute Value**

dB Output (60dB Range)

Chip Select-Power Down Feature Allows:
- **Analog "3-State" Operation**
- **Quiescent Current Reduction from 2.2mA to 350μA**
- **Side-Brazed DIP or Low-Cost Cerdip**

AD637 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD637 is a complete high accuracy monolithic rms to dc converter that computes the true rms value of any complex waveform. It offers performance that is unprecedented in integrated circuit rms to dc converters and comparable to discrete and modular techniques in accuracy, bandwidth and dynamic range. A crest factor compensation scheme in the AD637 permits measurements of signals with crest factors of up to 10 with less than 1% additional error. The circuit's wide bandwidth permits the measurement of signals up to 600kHz with inputs of 200mV rms and up to 8MHz when the input levels are above 2V rms.

As with previous monolithic rms converters from Analog Devices, the AD637 has an auxiliary dB output available to the user. The logarithm of the rms output signal is brought out to a separate pin allowing direct dB measurement with a useful range of 60dB. An externally programmed reference current allows the user to select the 0dB reference voltage to correspond to any level between 0.1V and 2.0V rms.

A chip select connection on the AD637 permits the user to decrease the supply current from 2.2mA to 350μA during periods when the rms function is not in use. This feature facilitates the addition of precision rms measurement to remote or hand-held applications where minimum power consumption is critical. In addition when the AD637 is powered down the output goes to a high impedance state. This allows several AD637s to be tied together to form a wide-band true rms multiplexer.

The input circuitry of the AD637 is protected from overload voltages that are in excess of the supply levels. The inputs will not be damaged by input signals if the supply voltages are lost.

The AD637 is available in two accuracy grades (J, K) for commercial (0 to +70°C) temperature range applications and one (S) rated over the −55°C to +125°C temperature range. All versions are available in hermetically-sealed, 14-pin side-brazed ceramic DIPs as well as low-cost cerdip packages.

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PRODUCT HIGHLIGHTS

1. The AD637 computes the true root-mean-square, mean square, or absolute value of any complex ac (or ac plus dc) input waveform and gives an equivalent dc output voltage. The true rms value of a waveform is more useful than an average rectified signal since it relates directly to the power of the signal. The rms value of a statistical signal is also related to the standard deviation of the signal.
2. The AD637 is laser wafer trimmed to achieve rated performance without external trimming. The only external component required is a capacitor which sets the averaging time period. The value of this capacitor also determines low frequency accuracy, ripple level and settling time.
3. The chip select feature of the AD637 permits the user to power down the device down during periods of nonuse, thereby, decreasing battery drain in remote or hand-held applications.
4. The on-chip buffer amplifier can be used as either an input buffer or in an active filter configuration. The filter can be used to reduce the amount of ac ripple, thereby, increasing the accuracy of the measurement.

SPECIFICATIONS (@ +25°C, and ±15V dc unless otherwise noted)

Model	AD637AJ Min	AD637AJ Typ	AD637AJ Max	AD637AK Min	AD637AK Typ	AD637AK Max	AD637AS Min	AD637AS Typ	AD637AS Max	Units
TRANSFER FUNCTION		$V_{OUT} = \sqrt{avg\ (V_{IN})^2}$			$V_{OUT} = \sqrt{avg\ (V_{IN})^2}$			$V_{OUT} = \sqrt{avg\ (V_{IN})^2}$		
CONVERSION ACCURACY										
Total Error, Internal Trim[1] (Fig 2)			±1 ±0.5			±0.5 ±0.2			±1 ±0.5	mV ± % of Reading
T_{min} to T_{max}			±3.0 ±0.6			±2.0 ±0.3			±6 ±0.7	mV ± % of Reading
vs Supply +		30	150		30	150		30	150	µV/V
vs Supply −		100	300		100	300		100	300	µV/V
dc Reversal Error at 2V			0.25			0.1			0.25	% of Reading
Nonlinearity 2V Full Scale[2]			0.04			0.02			0.04	% of FSR
Nonlinearity 7V Full Scale			0.05			0.05			0.05	% of FSR
Total Error, External Trim		±0 5 ±0 1			±0 25 ±0 05			±0 5 ±0 1		mV ± % of Reading
ERROR VS. CREST FACTOR[3]										
Crest Factor 1 to 2		Specified Accuracy			Specified Accuracy			Specified Accuracy		
Crest Factor = 3		±0 1			±0 1			±0 1		% of Reading
Crest Factor = 10		±1 0			±1 0			±1 0		% of Reading
AVERAGING TIME CONSTANT		25			25			25		ms/µF CAV
INPUT CHARACTERISTICS										
Signal Range, ± 15V Supply										
Continuous rms Level		0 to 7			0 to 7			0 to 7		V rms
Peak Transient Input			±15			±15			±15	V p-p
Signal Range, ± 5V Supply										
Continuous rms Level		0 to 4			0 to 4			0 to 4		V rms
Peak Transient Input			±6			±6			±6	V p-p
Maximum Continuous Non-Destructive Input Level (All Supply Voltages)			±15			±15			±15	V p-p
Input Resistance	6 4	8	9 6	6 4	8	9 6	6 4	8	9 6	kΩ
Input Offset Voltage			±0 5			±0 2			±0 5	mV
FREQUENCY RESPONSE[4]										
Bandwidth for 1% additional error (0 09dB)										
V_{IN} = 20mV		11			11			11		kHz
V_{IN} = 200mV		66			66			66		kHz
V_{IN} = 2V		200			200			200		kHz
± 3dB Bandwidth										
V_{IN} = 20mV		150			150			150		kHz
V_{IN} = 200mV		1			1			1		MHz
V_{IN} = 2V		8			8			8		MHz
OUTPUT CHARACTERISTICS										
Offset Voltage			±1			±0.5			±1	mV
vs Temperature		±0.05	±0.089		±0 04	±0.056		±0 04	±0.07	mV/°C
Voltage Swing, ± 15V Supply, 2kΩ Load	0 to +12.0	+13 5		0 to +12.0	+13 5		0 to +12.0	+13 5		V
Voltage Swing, ± 3V Supply, 2kΩ Load	0 to +2	+2.2		0 to +2	+2.2		0 to +2	+2 2		V
Output Current	6			6			6			mA
Short Circuit Current		20			20			20		mA
Resistance, Chip Select "High"		0 5			0.5			0 5		MΩ
Resistance, Chip Select "Low"		100			100			100		kΩ
dB OUTPUT										
Error, V_{IN} 7mV to 7V rms, 0dB = 1V rms		±1			±1			±1		dB
Scale Factor		−3			−3			−3		mV/dB
Scale Factor Temperature Coefficient		+0 33			+0 33			+0.33		% of Reading/°C
		−0 033			−0.033			−0.033		dB/°C
I_{RFT} for 0dB = 1V rms	5	20	80	5	20	80	5	20	80	µA
I_{RFT} Range	1		100	1		100	1		100	µA
BUFFER AMPLIFIER										
Input and Output Voltage Range	−V_S to (+V_S −2 5V)			−V_S to (+V_S −2 5V)			−V_S to (+V_S −2 5V)			V
Input Offset Voltage		±0 8	±2		±0 5	±1		±0 8	±2	mV
Input Current		±2	±10		±2	±5		±2	±10	nA
Input Resistance		10^8			10^8			10^8		Ω
Output Current	(+5mA, −130µA)			(+5mA, −130µA)			(+5mA, −130µA)			
Short Circuit Current		20			20			20		mA
Small Signal Bandwidth		1			1			1		MHz
Slew Rate[5]		5			5			5		V/µs
DENOMINATOR INPUT										
Input Range		0 to +10			0 to +10			0 to +10		V
Input Resistance	20	25	30	20	25	30	20	25	30	kΩ
Offset Voltage		±0 2	±0 5		±0 2	±0 5		±0 2	±0 5	mV
CHIP SELECT PROVISION (CS)										
rms "ON" Level		Open or +2 4V<V_C<+V_S			Open or +2 4V<V_C<+V_S			Open or +2 4V<V_C<+V_S		
rms "OFF" Level		V_C < +0 2V			V_C < +0 2V			V_C < +0 2V		
I_{OUT} of Chip Select										
CS "LOW"		10			10			10		µA
CS "HIGH"		Zero			Zero			Zero		
On Time Constant		10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})		
Off Time Constant		10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})			10µs + ((25kΩ) × C_{AV})		

Model	AD637AJ			AD637AK			AD637AS			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
POWER SUPPLY										
Operating Voltage Range	±3.0		±18	±3.0		±18	±3.0		±18	V
Quiescent Current		2.2	3		2.2	3		2.2	3	mA
Standby Current		350	450		350	450		350	450	μA
PACKAGE OPTIONS[6]										
TO-116-(D-14)		AD637AJD			AD637AKD			AD637ASD		
Cerdip (Q-14)		AD637AJQ			AD637AKQ			N/A		

NOTES
[1]Accuracy specified 0-7V rms dc with AD637 connected as shown in Figure 2.
[2]Nonlinearity is defined as the maximum deviation from the straight line connecting the readings at 10mV and 2V.
[3]Error vs. crest factor is specified as additional error for 1V rms
[4]Input voltages are expressed in volts rms. % are in % of reading.
[5]With external 2kΩ pull down resistor tied to $-V_S$
[6]See Section 16 for package outline information
Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units

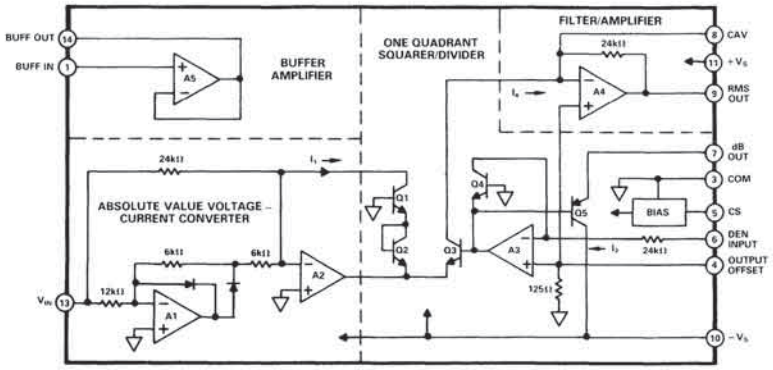


Figure 1. Simplified Schematic

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FUNCTIONAL DESCRIPTION

The AD637 embodies an implicit solution of the rms equation that overcomes the inherent limitations of straightforward rms computation. The actual computation performed by the AD637 follows the equation

$$V\ \text{rms} = \text{Avg}\left[\frac{V_{IN}^2}{V\ \text{rms}}\right]$$

Figure 1 is a simplified schematic of the AD637, it is subdivided into four major sections; absolute value circuit (active rectifier), square/divider, filter circuit and buffer amplifier. The input voltage V_{IN} which can be ac or dc is converted to a unipolar current I1 by the active rectifier A1, A2. I1 drives one input of the squarer divider which has the transfer function

$$I_4 = \frac{I_1^2}{I_3}$$

The output current of the squarer/divider, I4 drives A4 which forms a low pass filter with the external averaging capacitor. If the RC time constant of the filter is much greater than the longest period of the input signal than A4s output will be proportional to the average of I4. The output of this filter amplifier is used by A3 to provide the denominator current I3 which equals Avg. I4 and is returned to the squarer/divider to complete the implicit rms computation.

$$I_4 = \text{Avg}\left[\frac{I_1^2}{I_4}\right] = I_1\ \text{rms}$$

and

$$V_{OUT} = V_{IN}\ \text{rms}$$

If the averaging capacitor is omitted the AD637 will compute the absolute value of the input signal. A nominal 5pF capacitor should be used to insure stability. The circuit operates identically to that of the rms configuration except that I3 is now equal to I4 giving

$$I_4 = \frac{I_1^2}{I_4}$$

$$I_4 = |I_1|$$

The denominator current can also be supplied externally by providing a reference voltage, V_{REF}, to pin 6. The circuit operates identically to the rms case except that I3 is now proportional to V_{REF}. Thus:

$$I_4 = \text{Avg}\,\frac{I_1^2}{I_3}$$

and

$$V_O = \frac{V_{IN}^2}{V_{DEN}}$$

This is the mean square of the input signal.

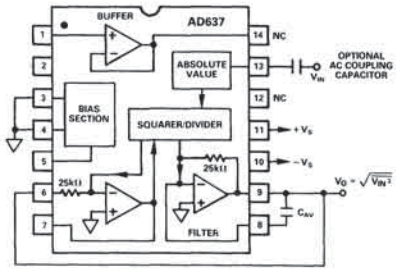


Figure 2. Standard rms Connection

STANDARD CONNECTION

The AD637 is simple to connect for a majority of rms measurements. In the standard rms connection shown in Figure 2, only a single external capacitor is required to set the averaging time constant. In this configuration, the AD637 will compute the true rms of any input signal. An averaging error, the magnitude of which will be dependent on the value of the averaging capacitor, will be present at low frequencies. For example, if the filter capacitor C_{AV}, is 4μF this error will be 0.1% at 10Hz and increases to 1% at 3Hz. If it is desired to measure only ac signals the AD637 can be ac coupled through the addition of a nonpolar capacitor in series with the input as shown in Figure 2.

The performance of the AD637 is tolerant of minor variations in the power supply voltages, however, if the supplies being used exhibit a considerable amount of high frequency ripple it is advisable to bypass both supplies to ground through a 0.1μF ceramic disc capacitor placed as close to the device as possible.

The output signal range of the AD637 is a function of the supply voltages, as shown in Figure 3. The output signal can be used buffered or nonbuffered depending on the characteristics of the load. The output of the AD637 is capable of driving 5mA into a 2kΩ load without degrading the accuracy of the device.

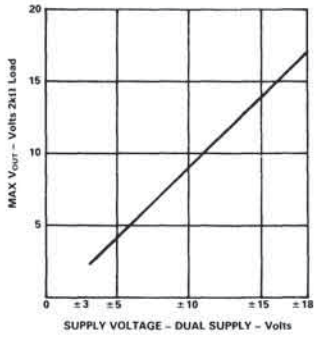


Figure 3. AD637 max V_{OUT} vs. Supply Voltage

CHIP SELECT

The AD637 includes a chip select feature which allows the user to decrease the quiescent current of the device from 2.2mA to 350μA. This is done by driving the CS, pin 5, to below 0.2V dc. Under these conditions, the output will go into a high impedance state. In addition to lowering power consumption, this feature permits bussing the outputs of a number of AD637s to form a wide bandwidth rms multiplexer. If the chip select is not being used, pin 5 should be tied high or left floating.

OPTIONAL TRIMS FOR HIGH ACCURACY

The AD637 includes provisions to allow the user to trim out both output offset and scale factor errors. These trims will result in significant reduction in the maximum total error as shown in Figure 4. This remaining error is due to a nontrimmable input offset in the absolute value circuit and the irreducible nonlinearity of the device.

The trimming procedure on the AD637 is as follows:

1. Ground the input signal, V_{IN} and adjust R1 to give 0V output from pin 9. Alternatively R1 can be adjusted to give the correct output with the lowest expected value of V_{IN}.
2. Connect the desired full scale input to V_{IN}, using either a dc or a calibrated ac signal, trim R3 to give the correct output at pin 9, i.e., 1V dc should give 1.000V dc output. Of course, a 2V peak-to-peak sine wave should give 0.707V dc output. Remaining errors are due to the nonlinearity.

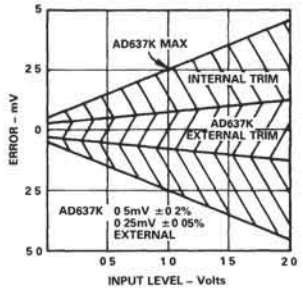


Figure 4. Max Total Error vs. Input Level AD637K Internal and External Trims

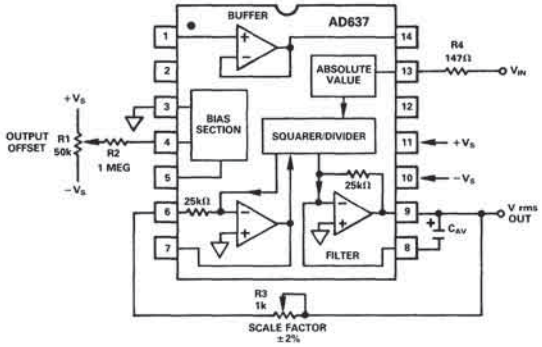


Figure 5. Optional External Gain and Offset Trims

CHOOSING THE AVERAGING TIME CONSTANT

The AD637 will compute the true rms value of both dc and ac input signals. At dc the output will track the absolute value of the input exactly; with ac signals the AD637's output will approach the true rms value of the input. The deviation from the ideal rms value is due to an averaging error. The averaging error is comprised of an ac and dc component. Both components are functions of input signal frequency f, and the averaging time constant τ (τ: 25ms/μF of averaging capacitance). As shown in Figure 6, the averaging error is defined as the peak value of the ac component, ripple, plus the value of the dc error.

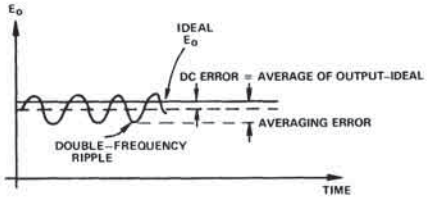


Figure 6. Typical Output Waveform for a Sinusoidal Input

The peak value of the ac ripple component of the averaging error is defined approximately by the relationship:

$$\frac{50}{6.3\tau f} \text{ in \% of reading where } (\tau > 1/f)$$

This ripple can add a significant amount of uncertainty to the accuracy of the measurement being made. The uncertainty can be significantly reduced through the use of a post filtering network or by increasing the value of the averaging capacitor.

The dc error appears as a frequency dependent offset at the output of the AD637 and follows the equation:

$$\frac{1}{0.16 + 6.4\tau^2 f^2} \text{ in \% of reading}$$

Since the averaging time constant, set by C_{AV}, directly sets the time that the rms converter "holds" the input signal during computation, the magnitude of the dc error is determined only by C_{AV} and will not be affected by post filtering.

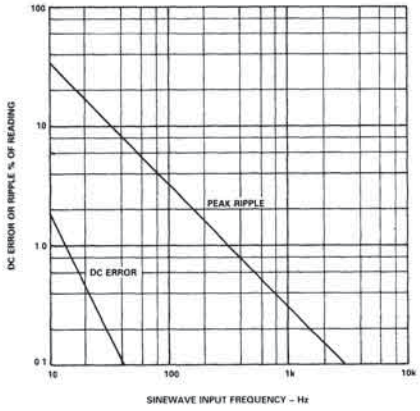


Figure 7. Comparison of Percent dc Error to the Percent Peak Ripple over Frequency Using the AD637 in the Standard rms Connection with a 1μF C_{AV}

The ac ripple component of averaging error can be greatly reduced by increasing the value of the averaging capacitor. There are two major disadvantages to this: first, the value of the averaging capacitor will become extremely large and second, the settling time of the AD637 increases in direct proportion to the value of the averaging capacitor (Ts = 115ms/μF of averaging capacitance). A preferrable method of reducing the ripple is through the use of the post filter network, shown in Figure 8. This network can be used in either a one or two pole configuration. For most applications the single pole filter will give the best overall compromise between ripple and settling time.

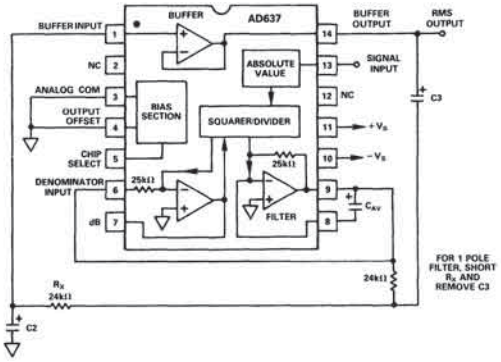


Figure 8. Two Pole Sallen-Key Filter

Figure 9a shows values of C_{AV} and the corresponding averaging error as a function of sine-wave frequency for the standard rms connection. The 1% settling time is shown on the right side of the graph.

Figure 9b shows the relationship between averaging error, signal frequency settling time and averaging capacitor value. This graph is drawn for filter capacitor values of 3.3 times the averaging capacitor value. This ratio sets the magnitude of the ac and dc errors equal at 50Hz. As an example, by using a 1μF averaging capacitor and a 3.3μF filter capacitor the ripple for a 60Hz input signal will be reduced from 5.3% of reading using the averaging capacitor alone to 0.15% using the single pole filter. This gives a factor of thirty reduction in ripple and yet the settling time would only increase by a factor of three. The values of C_{AV} and C_2, the filter capacitor, can be calculated for the desired value of averaging error and settling time by using Figure 9b.

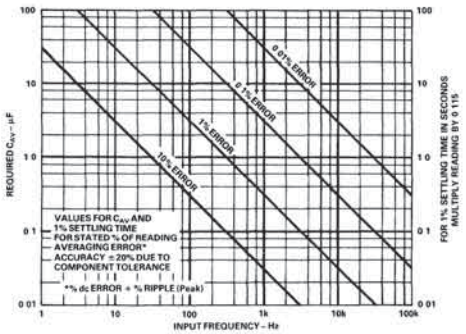


Figure 9a.

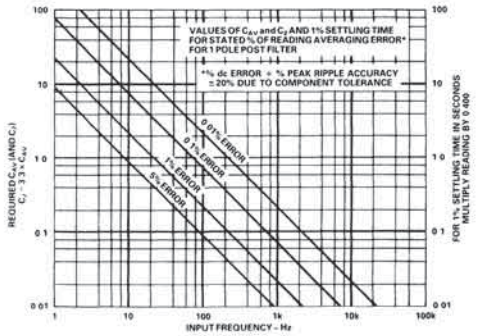


Figure 9b.

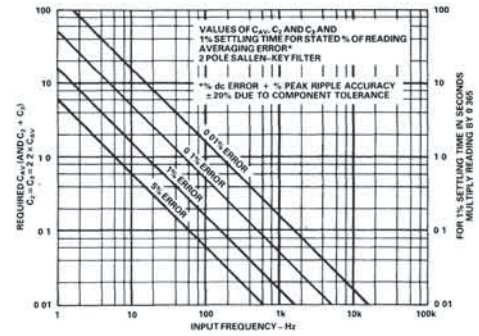


Figure 9c.

The symmetry of the input signal also has an effect on the magnitude of the averaging error. Table I gives practical component values for various types of 60Hz input signals. These capacitor values can be directly scaled for frequencies other than 60Hz, i.e., for 30Hz double these values, for 120Hz they are halved.

	Input Waveform and Period	Absolute Value Circuit Waveform and Period	Minimum $R \times C_{AV}$ Time Constant	Recommended C_{AV} and C2 Values for 1% Averaging Error@ 60Hz with T = 16.6ms		1% Settling Time
				Recommended Standard Value C_{AV}	Recommended Standard Value C2	
A	Symmetrical Sine Wave	1/2T	1/2T	0.47μF	1.5μF	181ms
B	Sine Wave with dc Offset		T	0.82μF	2.7μF	325ms
C	Pulse Train Waveform		$10(T-T_2)$	6.8μF	22μF	2.67sec
D			$10(T-2T_2)$	5.6μF	18μF	2.17sec

Table I. Practical Values of C_{AV} and C2 for Various Input Waveforms

For applications that are extremely sensitive to ripple, the two pole configuration is suggested. This configuration will minimize capacitor values and settling time while maximizing performance.

Figure 9c can be used to determine the required value of C_{AV}, C_2 and C_3 for the desired level of ripple and settling time.

FREQUENCY RESPONSE

The frequency response of the AD637 at various signal levels is shown in Figure 10. The dashed lines show the upper frequency limits for 1%, 10% and ±3dB of additional error. For example, note that for 1% additional error with a 2V rms input the highest frequency allowable is 200kHz. A 200mV signal can be measured with 1% error at signal frequencies up to 100kHz.

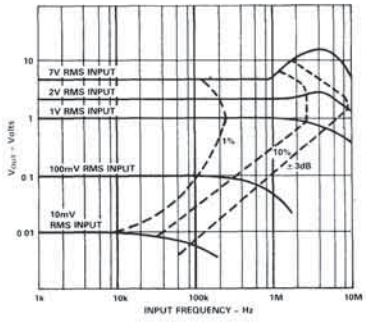


Figure 10. Frequency Response

To take full advantage of the wide bandwidth of the AD637 care must be taken in the selection of the input buffer amplifier. To insure that the input signal is accurately presented to the converter, the input buffer must have a −3dB bandwidth that is wider than that of the AD637. A point that should not be overlooked is the importance of slew rate in this application. For example, the minimum slew rate required for a 1V rms 5MHz sine-wave input signal is 44V/μs. The user is cautioned that this is the minimum rising or falling slew rate and that care must be exercised in the selection of the buffer amplifier as

some amplifiers exhibit a two-to-one difference between rising and falling slew rates. The AD381 is recommended as a precision input buffer.

AC MEASUREMENT ACCURACY AND CREST FACTOR

Crest factor is often overlooked in determining the accuracy of an ac measurement. Crest factor is defined as the ratio of the peak signal amplitude to the rms value of the signal (C.F. = V_p/V_{rms}). Most common waveforms, such as sine and triangle waves, have relatively low crest factors (≤2). Waveforms which resemble low duty cycle pulse trains, such as those occurring in switching power supplies and SCR circuits, have high crest factors. For example, a rectangular pulse train with a 1% duty cycle has a crest factor of 10 (C.F. = $1/\sqrt{\eta}$).

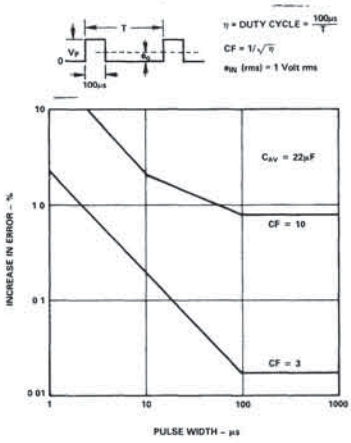


Figure 11. AD637 Error vs. Pulse Width Rectangular Pulse

Figure 12 is a curve of additional reading error for the AD637 for a 1 volt rms input signal with crest factors from 1 to 11. A rectangular pulse train (pulse width 100µs) was used for this test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce crest factors from 1 to 10 while maintaining a constant 1 volt rms input amplitude.

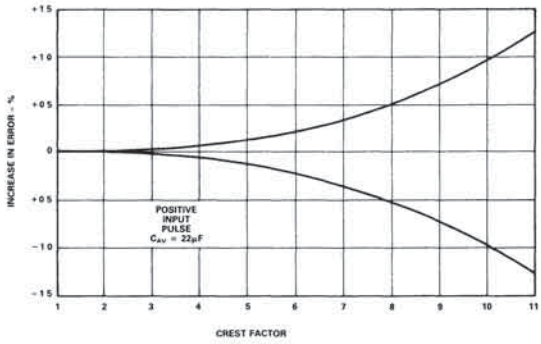


Figure 12. Additonal Error vs. Crest Factor

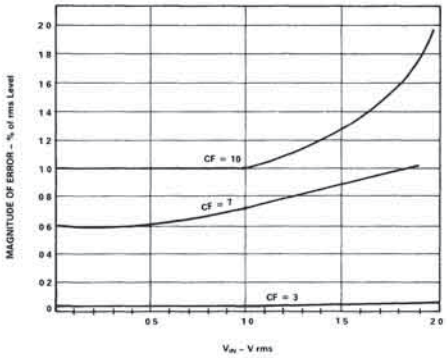


Figure 13. Error vs. rms Input Level for Three Common Crest Factors

CONNECTION FOR dB OUTPUT

Another feature of the AD637 is the logarithmic or decibel output. The internal circuit which computes dB works well over a 60dB range. The connection for dB measurement is shown in Figure 14. The user selects the 0dB level by setting R1 for the proper 0dB reference current (which is set to exactly cancel the log output current from the squarer/divider circuit at the desired 0dB point). The external op amp is used to provide a more convenient scale and to allow compensation of the +0.33%/°C temperature drift of the dB circuit. The special T.C. resistor R3 is available from Tel Labs in Londenderry, New Hampshire (model Q-81) and from Precision Resistor Inc., Hillside, N.J. (model PT146).

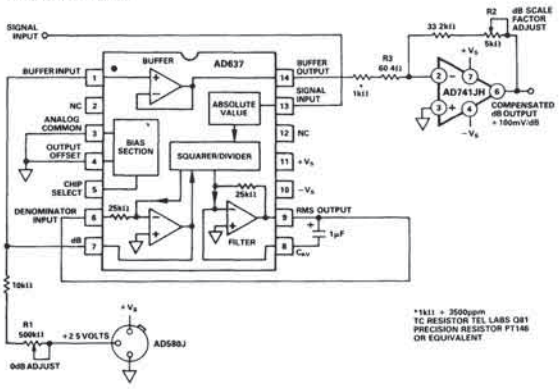


Figure 14. dB Connection

dB CALIBRATION

1. Set V_{IN} = 1.00V dc or 1.00V rms
2. Adjust R1 for 0dB out = 0.00V
3. Set V_{IN} = 0.1V dc or 0.10V rms
4. Adjust R2 for dB out = −2.00V

Any other dB reference can be used by setting V_{IN} and R1 accordingly.

8

LOW FREQUENCY MEASUREMENTS

If the frequencies of the signals to be measured are below 10Hz, the value of the averaging capacitor required to deliver even 1% averaging error in the standard rms connection becomes extremely large. The circuit shown in Figure 15 shows an alternative method of obtaining low frequency rms measurements. The averaging time constant is determined by the product of R and C_{AV1}, in this circuit 0.5s/μF of C_{AV}. This circuit permits a 20:1 reduction in the value of the averaging capacitor, permitting the use of high quality tantalum capacitors. It is suggested that the two pole Sallen-Key filter shown in the diagram be used to obtain a low ripple level and minimize the value of the averaging capacitor.

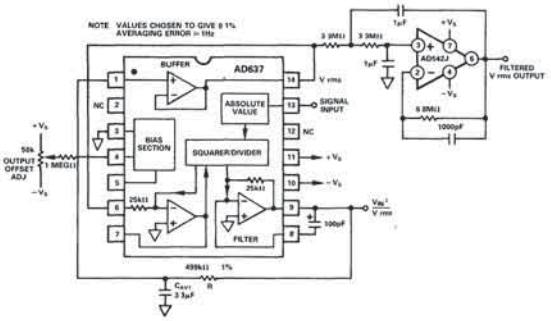


Figure 15. AD637 as a Low Frequency rms Converter

If the frequency of interest is below 1Hz, or if the value of the averaging capacitor is still too large, the 20:1 ratio can be increased. This is accomplished by increasing the value of R. If this is done it is suggested that a low input current, low offset voltage amplifier like the AD542 be used instead of the internal buffer amplifier. This is necessary to minimize the offset error introduced by the combination of amplifier input currents and the larger resistance.

VECTOR SUMMATION

Vector summation can be accomplished through the use of two AD637s as shown in Figure 16. Here the averaging capacitors are omitted (nominal 100pF capacitors are used to insure stability of the filter amplifier), and the outputs are summed as shown. The output of the circuit is

$$V_O = \sqrt{V_X^2 + V_Y^2}$$

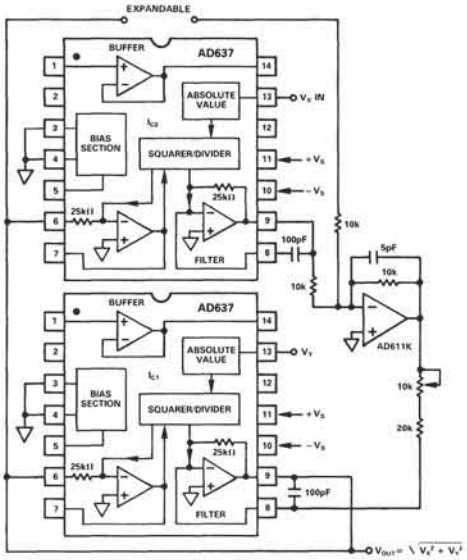


Figure 16. AD637 Vector Sum Configuration

This concept can be expanded to include additional terms by feeding the signal from pin 9 of each additional AD637 through a 10kΩ resistor to the summing junction of the AD611, and tying all of the denominator inputs (pin 6) together.

If C_{AV} is added to IC1 in this configuration the output is $\sqrt{V_X^2 + V_Y^2}$ If the averaging capacitor is included on both IC1 and IC2 the output will be $\sqrt{\overline{V_X^2} + \overline{V_Y^2}}$

This circuit has a dynamic range of 10V to 10mV and is limited only by the 0.5mV offset voltage of the AD637. The useful bandwidth is 100kHz.

Low-Cost, Low-Power True rms-to-dc Converter

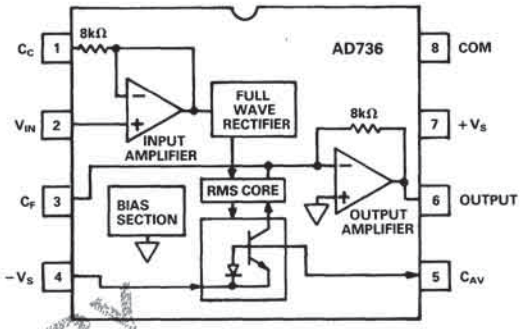
AD736

FEATURES

COMPUTES
- True rms Value
- Average Rectified Value
- Absolute Value

PROVIDES
- 200mV Full-Scale Input Range
- High Input Impedance of $10^{12}\Omega$
- Low Input Bias Current: 25pA max
- High Accuracy: ±0.5mV ±0.5% of Reading
- RMS Conversion with Signal Crest Factors Up to 5
- Wide Power Supply Range: +2.8V, −3.2V to ±16.5V
- Low Power: 200μA max Supply Current
- Buffered Voltage Output
- No External Trims Needed for Specified Accuracy
- AD737 – An Unbuffered Voltage Output Version with Chip Power Down is also Available

AD736 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD736 is a low-power, precision, monolithic true rms-to-dc converter. It is laser trimmed to provide a maximum error of less than ±0.5mV ±0.5% of reading with sine-wave inputs. Furthermore, it maintains high accuracy while measuring a wide range of input waveforms, including variable duty cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms "precision rectifiers" in many applications. Compared to these circuits, the AD736 offers higher accuracy at equal or lower cost.

The AD736 can compute the rms value of both ac and dc input voltages. It can also be operated ac coupled by adding one external capacitor. In this mode, the AD736 can resolve input signal levels of 100μV rms or less, despite variations in temperature or supply voltage. High acccuracy is also maintained for input waveforms with crest factors of 1 to 3. In addition, crest factors as high as 5 can be measured (while introducing only 2.5% additional error) at the 200mV full-scale input level.

The AD736 has its own output buffer amplifier, thereby providing a great deal of design flexibility. Requiring only 200μA of power supply current, the AD736 is optimized for use in portable multimeters and other battery powered applications.

The AD736 allows the choice of two signal input terminals: a high impedance ($10^{12}\Omega$) FET input which will directly interface with high Z input attenuators and a low impedance (8kΩ) input which allows the measurement of 300mV input levels, while operating from the minimum power supply voltage of +2.8V, −3.2V. The two inputs may be used either singly or differentially.

The AD736 achieves a 1% of reading error bandwidth exceeding 10kHz for input amplitudes from 20mV rms to 200mV rms while consuming only 1mW.

The AD736 is available in four performance grades. The AD736J and AD736K grades are rated over the commercial temperature range of 0 to +70°C. The AD736A and AD736B grades are rated over the industrial temperature range of −40°C to +85°C.

The AD736 is available in three low-cost 8-pin packages: plastic mini-DIP, plastic SO and hermetic cerdip.

PRODUCT HIGHLIGHTS

1. The AD736 is capable of computing the average rectified value, absolute value or true rms value of various input signals.
2. Only one external component, an averaging capacitor, is required for the AD736 to perform true rms measurement.
3. The low power consumption of 1mW makes the AD736 suitable for many battery powered applications.
4. A high input impedance of $10^{12}\Omega$ eliminates the need for an external buffer when interfacing with input attenuators.
5. A low impedance input is available for those applications requiring up to 300mV rms input signal operating from low power supply voltages.

SPECIFICATIONS (@ +25°C ±5V supplies, ac coupled with 1kHz sine-wave input applied unless otherwide noted.)

Model		AD736J/A			AD736K/B			
	Conditions	Min	Typ	Max	Min	Typ	Max	Units
TRANSFER FUNCTION			$V_{OUT} = \sqrt{Avg.(V_{IN}^2)}$			$V_{OUT} = \sqrt{Avg.(V_{IN}^2)}$		
CONVERSION ACCURACY	1kHz Sine Wave							
Total Error, Internal Trim[1]	ac Coupled							
All Grades	0-200mV rms		0.2/0.2	**0.5/0.5**		0.2/0.2	**0.3/0.3**	±mV/±% of Reading
	200mV-1V rms		1.2	**2.0**		**1.2**	**2.0**	±% of Reading
T_{min}-T_{max}								
A&B Grades	@ 200mV rms			**0.7/0.7**			**0.5/0.5**	±mV/±% of Reading
J&K Grades	@ 200mV rms		0.007			0.007		±% of Reading/°C
vs. Supply Voltage								
@ 200mV rms Input	V_S = ±5V to ±16.5V	**0**	+0.06	**+0.1**	**0**	+0.06	**+0.1**	%/V
@ 200mV rms Input	V_S = ±5V to ±3V	**0**	−0.18	**−0.3**	**0**	−0.18	**−0.3**	%/V
dc Reversal Error, dc Coupled	@ 600mV dc		1.3	**2.5**		1.3	**2.5**	% of Reading
Nonlinearity[2], 0-200mV	@ 100mV rms	**0**	+0.25	**+0.35**	**0**	+0.25	**+0.35**	% of Reading
Total Error, External Trim	0-200mV rms		0.1/0.5			0.1/0.3		±mV ±% of Reading
ERROR vs. CREST FACTOR[3]								
Crest Factor 1 to 3	C_{AV}, C_F = 100µF		0.7			0.7		% Additional Error
Crest Factor = 5	C_{AV}, C_F = 100µF		2.5			2.5		% Additional Error
INPUT CHARACTERISTICS								
High Impedance Input (Pin 2)								
Signal Range								
Continuous rms Level	V_S = +2.8V, −3.2V			**200**			**200**	mV rms
Continuous rms Level	V_S = ±5V to ±16.5V			**1**			**1**	V rms
Peak Transient Input	V_S = +2.8V, −3.2V	**±0.9**			**±0.9**			V
Peak Transient Input	V_S = ±5V		±2.7			±2.7		V
Peak Transient Input	V_S = ±16.5V	**±4.0**			**±4.0**			V
Input Resistance			10^{12}			10^{12}		Ω
Input Bias Current	V_S = ±3V to ±16.5V		1	**25**		1	**25**	pA
Low Impedance Input (Pin 1)								
Signal Range								
Continuous rms Level	V_S = +2.8V, −3.2V			300			300	mV rms
Continuous rms Level	V_S = ±5V to ±16.5V			1			1	V rms
Peak Transient Input	V_S = +2.8 V, −3.2V		±1.7			±1.7		V
Peak Transient Input	V_S = ±5V		±3.8			±3.8		V
Peak Transient Input	V_S = ±16.5V		±11			±11		V
Input Resistance		6.4	8	9.6	6.4	8	9.6	kΩ
Maximum Continuous Non-Destructive Input	All Supply Voltages			±12			±12	V p-p
Input Offset Voltage[4]	ac Coupled							
J&K Grades				**±3**			**±3**	mV
A&B Grades				**±3**			**±3**	mV
vs. Temperature			8	30		8	30	µV/°C
vs. Supply	V_S = ±5V to ±16.5V		50	**150**		50	**150**	µV/V
vs. Supply	V_S = ±5V to ±3V		80			80		µV/V
OUTPUT CHARACTERISTICS								
Output Offset Voltage								
J&K Grades			±0.1	**±0.5**		±0.1	**±0.3**	mV
A&B Grades				**±0.5**			**±0.3**	mV
vs. Temperature			1	20		1	20	µV/°C
vs. Supply	V_S = ±5V to ±16.5V		50	**130**		50	**130**	µV/V
	V_S = ±5V to ±3V		50			50		µV/V
Output Voltage Swing								
2kΩ Load	V_S = +2.8V, −3.2V	0 to +1.6	+1.7		0 to +1.6	+1.7		V
2kΩ Load	V_S = ±5V	0 to +3.6	+3.8		0 to +3.6	+3.8		V
2kΩ Load	V_S = ±16.5V	**0 to +4**	+5		**0 to +4**	+5		V
No Load	V_S = ±16.5V	**0 to +4**	+12		**0 to +4**	+12		V
Output Current		2			2			mA
Short-Circuit Current			3			3		mA
Output Resistance	@ dc		0.2			0.2		Ω

PRELIMINARY TECHNICAL DATA

Model	Conditions	AD736J/A Min	AD736J/A Typ	AD736J/A Max	AD736K/B Min	AD736K/B Typ	AD736K/B Max	Units
FREQUENCY RESPONSE								
High Impedance Input (Pin 2)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1mV rms			1			1		kHz
V_{IN} = 10mV rms			6			6		kHz
V_{IN} = 100mV rms			37			37		kHz
V_{IN} = 200mV rms			33			33		kHz
± 3dB Bandwidth	Sine-Wave Input							
V_{IN} = 1mV rms			5			5		kHz
V_{IN} = 10mV rms			55			55		kHz
V_{IN} = 100mV rms			170			170		kHz
V_{IN} = 200mV rms			190			190		kHz
FREQUENCY RESPONSE								
Low Impedance Input (Pin 1)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1mV rms			1			1		kHz
V_{IN} = 10mV rms			6			6		kHz
V_{IN} = 100mV rms			90			90		kHz
V_{IN} = 200mV rms			90			90		kHz
± 3dB Bandwidth	Sine-Wave Input							
V_{IN} = 1mV rms			5			5		kHz
V_{IN} = 10mV rms			55			55		kHz
V_{IN} = 100mV rms			350			350		kHz
V_{IN} = 200mV rms			460			460		kHz
POWER SUPPLY								
Operating Voltage Range		+2.8, −3.2	±5	±16.5	+2.8, −3.2	±5	±16.5	Volts
Quiescent Current	Zero Signal		160	200		160	200	μA
200mV rms, No Load	Sine-Wave Input		230	270		230	270	μA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0 to + 70°C)			AD736J			AD736K		
Industrial (−40°C to +85°C)			AD736A			AD736B		
PACKAGE OPTIONS[5]								
8-Pin Plastic Mini-DIP (N-8)			AD736JN			AD736KN		
8-Pin Plastic SO (R-8)			AD736JR			AD736KR		
8-Pin Cerdip (Q-8)			AD736AQ			AD736BQ		

NOTES
[1]Accuracy is specified with the AD736 connected as shown in Figure 1.
[2]Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 and 200mV rms. Output offset voltage is adjusted to zero.
[3]Error vs. Crest Factor is specified as additional error for a 200mV rms signal. C.F. = V_{PEAK}/V rms.
[4]DC offset does not limit ac resolution.
[5]See Section 16 for package outline information.

Specifications are subject to change without notice.
Specifications shown in **boldface** are tested on all production units at final electrical test.
Results from those tests are used to calculate outgoing quality levels.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±16.5V
Internal Power Dissipation	200mW
Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q	−65°C to +150°C
Storage Temperature Range N, R	−65°C to +125°C
Operating Temperature Range	
AD736J/K	0 to +70°C
AD736A/B	−40°C to +85°C
Lead Temperature Range (Soldering 60sec)	+300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

8

Applications Circuits

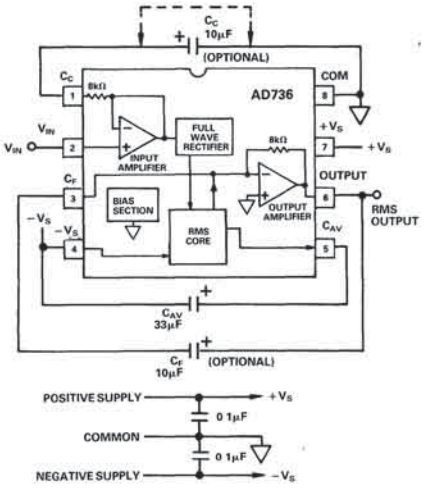


Figure 1. True rms Connection

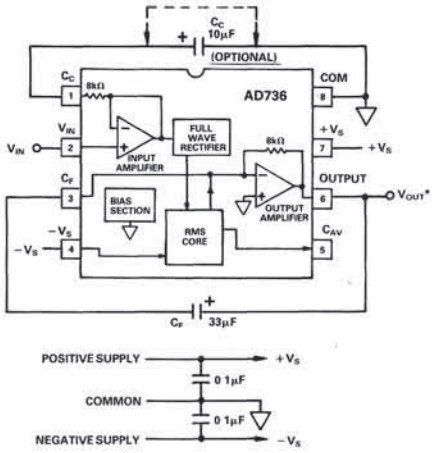


Figure 2. Average Responding Connection

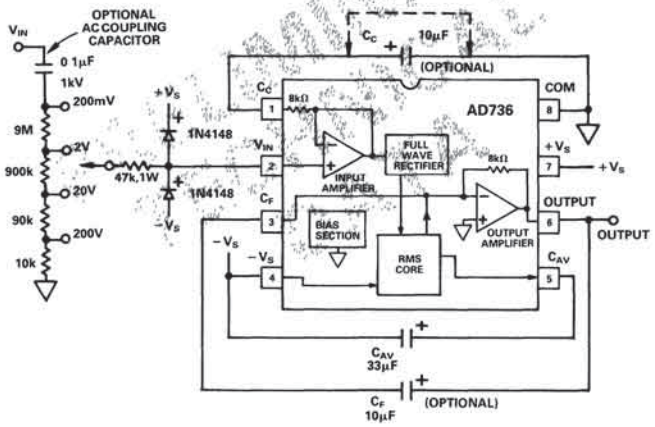


Figure 3. Connection to HI Z Input Attenuator

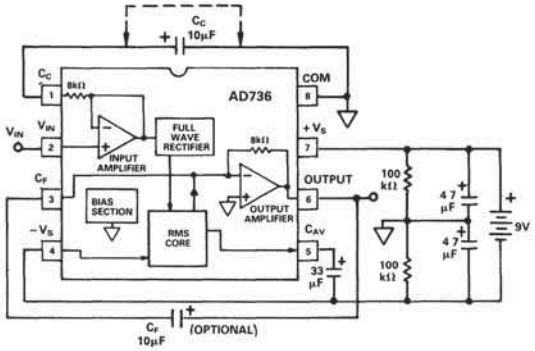


Figure 4. Connection for Battery Powered Operation.

Low-Cost, Low-Power True rms-to-dc Converter

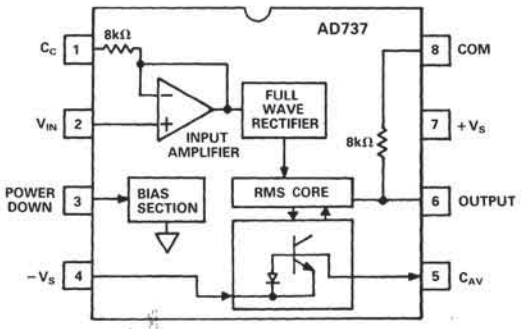
AD737

FEATURES

COMPUTES
- True rms Value
- Average Rectified Value
- Absolute Value

PROVIDES
- 200mV Full-Scale Input Range
- Direct Interfacing with 3 1/2 Digit CMOS A/D Converters
- Power Down Feature which Reduces Supply Current
- High Input Impedance: 10^{12} ohms
- Low Input Bias Current: 25pA max
- High Accuracy: ±0.2mV ±0.3% of Reading
- RMS Conversion with Signal Crest Factors Up to 5
- Wide Power Supply Range: +2.8V, −3.2V to ±16.5V
- Low Power: 160μA max Supply Current
- No External Trims Needed for Specified Accuracy
- AD736 – A General Purpose, Buffered Voltage Output Version is also Available

AD737 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD737 is a low-power, precision, monolithic true rms-to-dc converter. It is laser trimmed to provide a maximum error of less than ±0.2mV ±0.3% of reading with sine-wave inputs. Furthermore, it maintains high accuracy while measuring a wide range of input waveforms, including variable duty cycle pulses and triac (phase) controlled sine waves. The low cost and small physical size of this converter make it suitable for upgrading the performance of non-rms "precision rectifiers" in many applications. Compared to these circuits, the AD737 offers higher accuracy at equal or lower cost.

The AD737 can compute the rms value of both ac and dc input voltages. It can also be operated ac coupled by adding one external capacitor. In this mode, the AD737 can resolve input signal levels of 100μV rms or less, despite variations in temperature or supply voltage. High acccuracy is also maintained for input waveforms with crest factors of 1 to 3. In addition, crest factors as high as 5 can be measured (while introducing only 2.5% additional error) at the 200mV full-scale input level.

The AD737 has no output buffer amplifier, thereby significantly reducing dc offset errors occurring at the output. This allows the device to be highly compatible with high input impedance A/D converters.

Requiring only 160μA of power supply current, the AD737 is optimized for use in portable multimeters and other battery powered applications. This converter also provides a "power down" feature which reduces the power supply standby current to less than 30μA.

The AD737 allows the choice of two signal input terminals: a high impedance ($10^{12}\Omega$) FET input which will directly interface with high Z input attenuators and a low impedance (8kΩ) input which allows the measurement of 300mV input levels while operating from the minimum power supply voltage of +2.8V, −3.2V. The two inputs may be used either singly or differentially.

The AD737 achieves a 1% of reading error bandwidth exceeding 10kHz for input amplitudes from 20mV rms to 200mV rms while consuming only 0.72mW.

The AD737 is available in four performance grades. The AD737J and AD737K grades are rated over the commercial temperature range of 0 to +70°C. The AD737A and AD737B grades are rated over the industrial temperature range of −40°C to +85°C.

The AD737 is available in three low-cost, 8-pin packages: plastic mini-DIP, plastic SO and hermetic cerdip.

PRODUCT HIGHLIGHTS

1. The AD737 is capable of computing the average rectified value, absolute value or true rms value of various input signals.
2. Only one external component, an averaging capacitor, is required for the AD737 to perform true rms measurement.
3. The low power consumption of 0.72mW makes the AD737 suitable for many battery powered applications.

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SPECIFICATIONS (@ +25°C, ±5V supplies, ac coupled with 1kHz sine-wave input applied unless otherwise noted.)

Model	Conditions	AD737J/A Min	AD737J/A Typ	AD737J/A Max	AD737K/B Min	AD737K/B Typ	AD737K/B Max	Units
TRANSFER FUNCTION		$V_{OUT} = -\sqrt{Avg.(V_{IN}^2)}$			$V_{OUT} = -\sqrt{Avg.(V_{IN}^2)}$			
CONVERSION ACCURACY	1kHz Sine Wave							
Total Error, Internal Trim[1]	AC Coupled							
All Grades	0-200mV rms		0.2/0.3	**0.4/0.5**		0.2/0.2	**0.2/0.3**	± mV/± % of Reading
	200mV-1V rms		−1.2	**2.0**		−1.2	**2.0**	± % of Reading
T_{min}-T_{max}								
A&B Grades	@ 200mV rms			**0.5/0.7**			**0.3/0.5**	± mV/± % of Reading
J&K Grades	@ 200mV rms		0.007			0.007		± % of Reading/°C
vs. Supply Voltage								
@ 200mV rms Input	V_S = ±5V to ±16.5V	**0**	+0.06	**+0.1**	**0**	+0.06	**+0.1**	%/V
@ 200mV rms Input	V_S = ±5V to ±3V	**0**	−0.18	**−0.3**	**0**	−0.18	**−0.3**	%/V
dc Reversal Error, dc Coupled	@ 600mV dc		1.3	**2.5**		1.3	**2.5**	% of Reading
Nonlinearity[2], 0-200mV	@ 100mV rms	**0**	+0.25	**+0.35**	**0**	+0.25	**+0.35**	% of Reading
Total Error, External Trim	0-200mV rms		0.1/0.2			0.1/0.2		± mV/± % of Reading
ERROR vs. CREST FACTOR[3]								
Crest Factor 1 to 3	C_{AV}, C_F = 100µF		0.7			0.7		% Additional Error
Crest Factor = 5	C_{AV}, C_F = 100µF		2.5			2.5		% Additional Error
INPUT CHARACTERISTICS								
High Impedance Input (Pin 2)								
Signal Range								
Continuous rms Level	V_S = +2.8V, −3.2V			**200**			**200**	mV rms
Continuous rms Level	V_S = ±5V to ±16.5V			**1**			**1**	V rms
Peak Transient Input	V_S = +2.8V, −3.2V	**±0.9**			**±0.9**			V
Peak Transient Input	V_S = ±5V		±2.7			±2.7		V
Peak Transient Input	V_S = ±16.5V	**±4.0**			**±4.0**			V
Input Resistance			10^{12}			10^{12}		Ω
Input Bias Current	V_S = ±3V to ±16.5V		1	**25**		1	**25**	pA
Low Impedance Input (Pin 1)								
Signal Range								
Continuous rms Level	V_S = +2.8V, −3.2V			300			300	mV rms
Continuous rms Level	V_S = ±5V to ±16.5V			1			1	V rms
Peak Transient Input	V_S = +2.8V, −3.2V		±1.7			±1.7		V
Peak Transient Input	V_S = ±5V		±3.8			±3.8		V
Peak Transient Input	V_S = ±16.5V		±11			±11		V
Input Resistance		6.4	8	9.6	6.4	8	9.6	kΩ
Maximum Continuous Non-Destructive Input	All Supply Voltages			±12			±12	V p-p
Input Offset Voltage[4]	ac Coupled							
J&K Grades				**±3**			**±3**	mV
A&B Grades				**±3**			**±3**	mV
vs. Temperature			8	30		8	30	µV/°C
vs. Supply	V_S = ±5V to ±16.5V		50	**150**		50	**150**	µV/V
vs. Supply	V_S = ±5V to ±3V		80			80		µV/V
OUTPUT CHARACTERISTICS								
Output Voltage Swing								
No Load	V_S = +2.8V, −3.2V	0 to −1.6	−1.7		0 to −1.6	−1.7		V
No Load	V_S = ±5V	0 to −3.3	−3.4		0 to −3.3	−3.4		V
No Load	V_S = ±16.5V	**0 to −4**	−5		**0 to −4**	−5		V
Output Resistance	@ dc	6.4	8	9.6	6.4	8	9.6	kΩ
FREQUENCY RESPONSE								
High Impedance Input (Pin 2)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1mV rms			1			1		kHz
V_{IN} = 10mV rms			6			6		kHz
V_{IN} = 100mV rms			37			37		kHz
V_{IN} = 200mV rms			33			33		kHz
±3dB Bandwidth	Sine-Wave Input							
V_{IN} = 1mV rms			5			5		kHz
V_{IN} = 10mV rms			55			55		kHz
V_{IN} = 100mV rms			170			170		kHz
V_{IN} = 200mV rms			190			190		kHz

Model	Conditions	AD737J/A Min	AD737J/A Typ	AD737J/A Max	AD737K/B Min	AD737K/B Typ	AD737K/B Max	Units
FREQUENCY RESPONSE								
Low Impedance Input (Pin 1)								
For 1% Additional Error	Sine-Wave Input							
V_{IN} = 1mV rms			1			1		kHz
V_{IN} = 10mV rms			6			6		kHz
V_{IN} = 100mV rms			90			90		kHz
V_{IN} = 200mV rms			90			90		kHz
±3dB Bandwidth	Sine-Wave Input							
V_{IN} = 1mV rms			5			5		kHz
V_{IN} = 10mV rms			55			55		kHz
V_{IN} = 100mV rms			350			350		kHz
V_{IN} = 200mV rms			460			460		kHz
POWER SUPPLY								
Operating Voltage Range		+2.8, −3.2	±5	±16.5	+2.8, −3.2	±5	±16.5	V
Quiescent Current	Zero Signal		120	**160**		120	**160**	µA
V_{IN} = 200mV rms, No Load	Sine-Wave Input		170	210		170	210	µA
Power Down Mode Current	Pin 3 tied to $+V_S$		25	40		25	40	µA
TEMPERATURE RANGE								
Operating, Rated Performance								
Commercial (0 to +70°C)			AD737J			AD737K		
Industrial (−40°C to +85°C)			AD737A			AD737B		
PACKAGE OPTIONS[5]								
8-Pin Plastic Mini-DIP (N-8)			AD737JN			AD737KN		
8-Pin Plastic SO (R-8)			AD737JR			AD737KR		
8-Pin Cerdip (Q-8)			AD737AQ			AD737BQ		

NOTES
[1]Accuracy is specified with the AD737 connected as shown in Figure 1.
[2]Nonlinearity is defined as the maximum deviation (in percent error) from a straight line connecting the readings at 0 and 200mV rms
[3]Error vs. Crest Factor is specified as additional error for a 200mV rms signal. C.F. = V_{PEAK}/V rms.
[4]DC offset does not limit ac resolution.
[5]See Section 16 for package outline information.

Specifications are subject to change without notice.
Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

PRELIMINARY DATA

8

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±16.5V
Internal Power Dissipation	200mW
Input Voltage	$\pm V_S$
Output Short-Circuit Duration	Indefinite
Differential Input Voltage	$+V_S$ and $-V_S$
Storage Temperature Range Q	−65°C to +150°C
Storage Temperature Range N, R	−65°C to +125°C
Operating Temperature Range	
AD737J/K	0 to +70°C
AD737A/B	−40°C to +85°C
Lead Temperature Range (Soldering 60sec)	+300°C

NOTE
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Applications Circuits

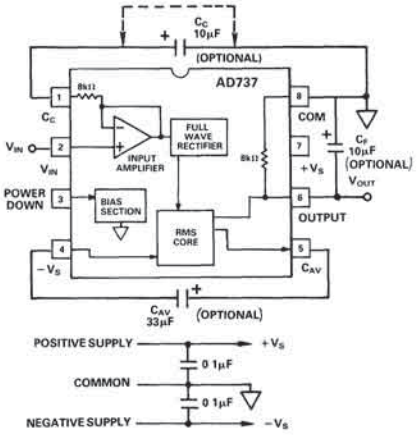


Figure 1. AD737 True rms Circuit

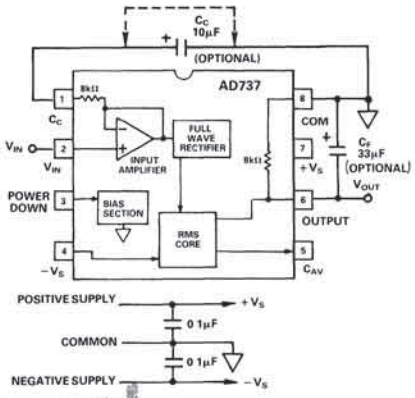


Figure 2. AD737 Average Responding Circuit

PRELIMINARY DATA

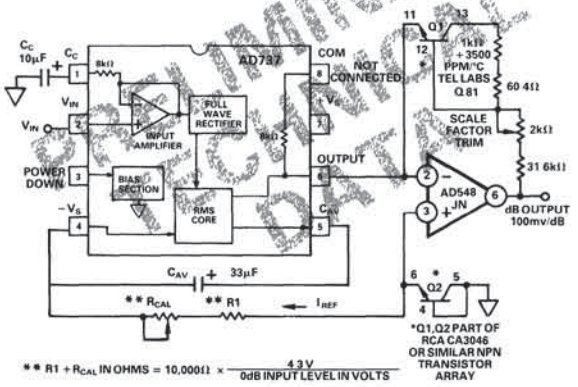


Figure 3. dB Output Connection

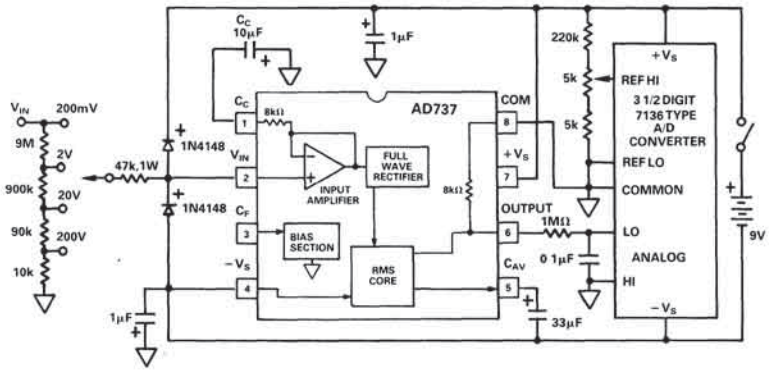


Figure 4. 3 1/2 Digit DVM Circuit

Special Function Components
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9

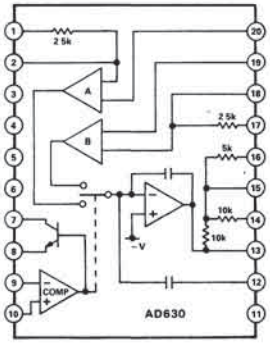
This section contains technical data on integrated-circuit chips that could not be classified in any of the major sections of this databook without losing their identities. For example, the AD639 trigonometric function generator is a close relative of analog multiplier/dividers, in both function and circuitry; but if it were listed in that section, its unique trigonometric capabilities would be "buried".

We describe briefly here the function and salient uses of these devices. For further information, consult the individual data sheets.

ANALOG FUNCTIONS

AD630 Balanced Modulator/Demodulator

The AD630 is a fast, flexible, switched dual-input op amp with an on-chip comparator. Intended for wideband, low-level, and wide-dynamic-range instrumentation applications and coherent systems, it is capable of such analog signal-processing functions as balanced modulator, balanced demodulator, absolute-value amplifier, phase detector, square-wave multiplier and two-channel precision multiplexer. It can be used as a lock-in amplifier, synchronous detector, rectifier, dual-mode circuit, and much more. Essentially a complete device with on-chip scaling resistors, it can be used for these functions with little or no additional circuitry.

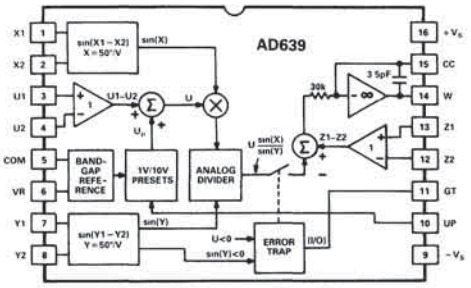


As a *lock-in amplifier*, it can recover a 0.1-Hz sine wave, transmitted as a modulation on a 400-Hz carrier, from a band-limited, clipped white-noise signal approximately 100,000 times larger – a dynamic range greater than 100dB.

It consists of a frequency-compensated op-amp-output stage, with two identical switched differential front ends (A and B), a differential comparator that controls the switching and a set of jumper-programmable matched precision resistors – trimmed to produce closed-loop gain accuracies to ±0.015% and gain match (between channels) to ±0.03%. When the net input to the comparator is positive, front-end A will be selected; when the comparator input is negative, front-end B is selected. A *status* output indicates the state of the comparator.

AD639 Universal Trigonometric Function Generator

The AD639 is an analog "trigonometric microsystem" on a single silicon chip, packaged in a 16-pin DIP. From a differential input voltage, representing an angle (20mV/°), it can be pin programmed to generate a voltage output, accurately determined by any of the standard functions – sine, cosine, tangent, secant, cosecant and cotangent – as well as some lesser known variants, such as the versine and exsecant, plus a corresponding set of inverse functions. All inputs are differential, and either polarity of input or output can be generated.



Trigonometric functions play an important role in electronics. Inherent to many communications, measurement and display systems, they also find increasing application in control and robotics. Most familiar are the *sine* and the *cosine*, which find wide use as fundamental signal sources – both separately and in orthogonal pairs. In display systems, these functions are basic to graphical manipulations (axis rotation and polar-to-Cartesian conversion), and they also appear in many antenna-related signal transformations. The *tangent* is important in scanning systems, and the *arctangent* is used in Cartesian-to-polar conversion and in determining phase angle from the real and imaginary components of a complex signal.

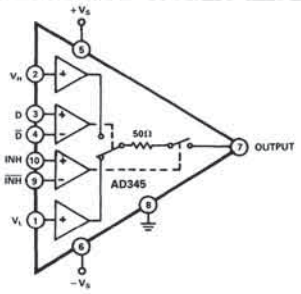
With its large repertoire of functions, the AD639 makes it possible to include trigonometric transformations in the analog portion of a system with little added cost or board space, and with high accuracy, without the overhead in software, memory or time, which would accompany such computations in an associated digital system. It also makes it easy to generate low-distortion sine-wave signals, with voltage control of amplitude and frequency, up to 10V and 1MHz, respectively.

DIGITAL FUNCTIONS

AD345 Pin Driver for Automatic Test Equipment

The AD345 is a complete high-speed pin driver designed for use in digital functional test equipment and general purpose instrumentation. It accepts digital, analog and timing information from system sources and translates them directly to digital output levels to be applied to the input of a device to be tested (DUT). By teaming up the economy of surface-mount technology and the accuracy of thick-film laser trimming, the AD345 attains superb electrical performance while preserving optimum packaging densities in a convenient 10-pin SIP package.

Its output is switched by digital control inputs, and its amplitude is derived from analog sources; its output *high* level can be set by an analog voltage at any value from −2V to +8V, and its *low* level can be set from −3V to +6V; this flexibility makes it compatible with ECL, TTL and CMOS logic levels and timing. It can drive level changes at up to 100MHz, with slewing rates better than 1V/ns; its dynamic output impedance is laser trimmed for waveform integrity and guaranteed performance with 50-ohm transmission lines. Output impedance is 50 ohms, matching it



to coaxial cable used for interconnecting the pin driver and the device's input terminal, in order to minimize error-causing reflections.

Who should use the AD345? Anyone who manufactures or designs equipment for automatic test of semiconductor devices or boards, or for instrumentation and characterization. It can also function as a high-performance, low-cost general purpose digital driver.

AD890 and AD891 Hard-Disk Bit-Recovery ICs

The AD890 Precision Wideband Channel-Processing Element and the AD891 Rigid-Disk Data-Channel Qualifier are a pair of monolithic integrated circuits that together are the key to a complete signal-processing subsystem capable of error-free high performance in demanding disk-drive applications. They take data directly from the disk-head preamplifier, condition and qualify it and produce recovered precisely timed data bits at rates in excess of 50 megabits per second (guaranteed). Such rates are essential for making efficient use of high-capacity, high-performance disk drives. This chip pair replaces slower, lower-performing discrete-circuit "kludges," and no external trims are needed.

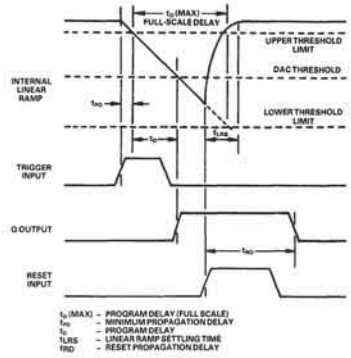
As the diagram below shows, the AD890 amplifies the signal to a normalized level, using stable variable-gain amplification with automatic gain control (AGC); and the AD891 establishes whether a pulse exists, using differentiation to find peaks, then produces data-output pulses of precise width. Since the actual timing requirements – of both the filter time constants and the differentiator characteristics – are a function of the user's system, the filter functions (using only passive elements) remain off-chip under full control of the user. In addition to the functions shown, the AGC can be turned off digitally when necessary; and input clamping can be switched in during *write* so as to avoid input overloads.

Although these circuits were developed for use in disk-drive applications, it should be apparent that their applicability may be considered wherever high-speed pulses have been degraded by attenuation and noise – and must be amplified, qualified and reconstituted. Separately, the AD890 is an excellent AGC amplifier for radio-frequency signals.

AD9500 Digitally Programmable Delay Generator

The AD9500 delays events by an interval selected by an 8-bit digital code, with settable time resolution as small as 10 picoseconds. The delay is initiated at the time a *Trigger* input goes *high*: an integrator generates a downgoing ramp, and when it crosses a preset level (established by an 8-bit DAC), a comparator output changes state to produce the delayed output, Q.

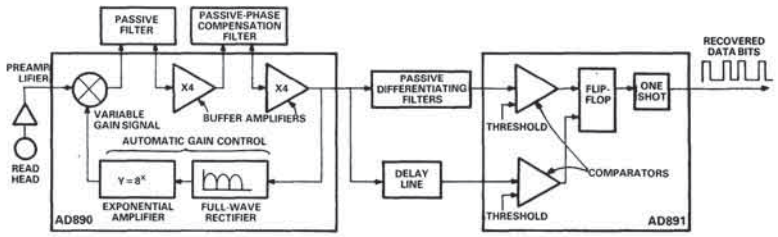
The delay is equal to the programmed delay – which depends on the integrator's selectable RC time constant and the precision threshold set by the DAC – plus a propagation delay of 5.4ns minimum. A pulse of appropriate width applied at the *Reset* input resets the integrator and the Q output to prepare the device for the next *Trigger*. The range of full-scale programmed delays is from 2.5ns to more than 1 ms, depending on the choice of R and C. When RC = 2.5ns, the LSB (or one increment of delay) is 2,500 ps/256 ≈ 10 ps, which is also the typical jitter level.



AD9500 Internal Timing Diagram

The differential *Trigger* and *Reset* inputs are designed primarily for single-ended or differential ECL, but they function with analog and TTL input levels. The Q, $\overline{Q}$ output is a complementary ECL stage, with a parallel $\overline{Q}_R$ output circuit to facilitate reset timing implementations.

An important application is in equalizing skew in multichannel systems; with one line used as the standard, the programmed delays of the other AD9500s are adjusted to eliminate the timing skews. Other applications include multiple-phase clock generators, measuring unknown delays and time response of high-speed ac waveforms, and digitally programmable oscillators.



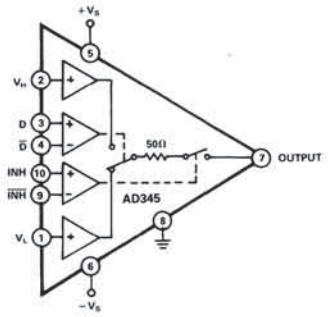
High-Speed Pin Driver with Inhibit Mode

AD345

FEATURES
- **100MHz Driver Operation**
- **Driver Inhibit (Tristate) Function**
- **Guaranteed Industry Specifications**
  - **50Ω Output Impedance**
  - **1V/ns Slew Rate**
  - **Variable Output Voltages for ECL, TTL and CMOS**
- **High-Speed Differential Inputs for Maximum Flexibility**
- **Small SIP Package**
- **Low Cost**

APPLICATIONS
- **Automatic Test Equipment**
  - **Semiconductor Test Systems**
  - **Board Test Systems**
- **Instrumentation & Characterization Equipment**
- **General Purpose Driver**

AD345 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD345 is a complete high-speed pin driver designed for use in digital test systems. By combining surface mount technology and thick-film laser trimmed technology, this product attains superb electrical performance while preserving optimum packaging densities in a convenient 10-pin SIP package.

Featuring unity gain programmable output levels of −3 to +8 volts with output amplitude capability of 700mV to 11V, the AD345 is designed to stimulate ECL, TTL and CMOS logic families. The 100MHz (5ns pulse width) data rate capacity, 1V/ns controlled slew rate, and 50Ω output impedance allows for real-time stimulation of these digital logic families. To test I/O devices the pin driver can be switched into a high impedance state (inhibit or tristate) by using the inhibit mode. The pin driver leakage in tristate is typically 50nA and output charge transfer going into tristate is guaranteed at 200pC maximum.

The AD345 transition from hi/low or to tristate is effected through the data and inhibit inputs. The input circuitry is implemented utilizing high-speed differential inputs with a common-mode range of 8 volts. This allows for direct interface to the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single ended TTL or CMOS logic source. The analog inputs V high or V low are equally easy to interface. Requiring typically 500μA of bias current, the AD345 can be directly coupled to the output of a DAC either singularly or in parallel with several other pin drivers.

The AD345 utilizes surface mount technology creating a small single in-line package which can be mounted upright or laying down (leads bent 90°) depending on the specific application. The SIP packaging enables the user to create a tight radial test head design or a custom high-speed dedicated probe card with the drivers placed in close proximity to the device under test guaranteeing optimum signal integrity. A metal tab is mounted on the back side allowing for heatsinking or mechanical support. The AD345 is available for operation over the 0 to +70°C range.

PRODUCT HIGHLIGHTS

1. The AD345 is a complete 100MHz pin driver designed to meet the requirements of ATE manufacturers.
2. Output high voltage level is adjustable from −2V to +8V and output low levels from −3 to +6V allowing compatibility with ECL, TTL, CMOS logic levels.
3. Certified large signal slew rates of better than 1V/ns with dynamic output impedance laser trimmed for waveform integrity and guaranteed performance with 50Ω transmission lines.
4. TRISTATE (inhibit) capability for testing I/O devices.
5. INHIBIT leakage current of 50nA typical virtually eliminates the requirement for a disconnect relay in a semiconductor test system.
6. Repeatability from driver-to-driver is guaranteed to meet published specifications through pretesting and active laser trimming.
7. The 10-pin SIP hybrid package with mounting tab provides high functional mechanical densities with maximum versatility.

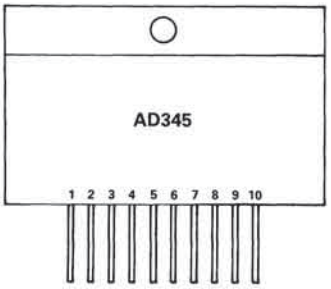
SPECIFICATIONS (All specs @ 25°C in free air, output unloaded, +V = +12V, −V = −8V, unless otherwise specified)

Parameter	AD345KY Min	Typ	Max	Units	Comments
DIFFERENTIAL INPUT CHARACTERISTICS					
D to $\overline{D}$, INH to $\overline{INH}$					
Voltage Range	$-V_S+6V$		$+V_S-6V$	Volts	
Pulse Amplitude	0.37	ECL	3.5	Volts p-p	See Note 1
Bias Current		500	750	μA	
REFERENCE INPUTS					See Note 2
V_{HIGH}	−2		+8.3	Volts	
V_{LOW}	−3		+6.2	Volts	
Bias Current		500	750	μA	
OUTPUT CHARACTERISTICS					See Notes 2 & 3
Logic High Range	−2		+8	Volts	
Logic Low Range	−3		+6	Volts	
Amplitude	0.7		11	Volts	
Initial Offset	−30		+30	mV	See Note 3
Gain Error	−1.2		+1.2	% of Set Level	Normalized to Figures 1 & 2
Output Voltage Temp. Coeff.		0.5	1.0	mV/°C	
Current Drive					
Static			60	mA	
Dynamic			100	mA	
Output Capacitance		9		pF	
Output Charge Going Into Inhibit Mode			200	pC	
Leakage Current in Inhibit Mode		50	200	nA	
Protection					
Output @ GND	INDEFINITELY				
Output @ +V	1 Minute w/o Damage				
Output @ −V	1 Minute w/o Damage				
DYNAMIC PERFORMANCE					See Notes 4 & 5
Driver Delay Time	1.5	2.0	2.5	ns	
Driver Delay Matching					
Edge to Edge	−0.5		+0.5	ns	
Driver to Driver	−1.0		+1.0	ns	
Slew Rate					
1V Swing 20%–80%		1.5	2.5	ns	
4V Swing 10%–90%		3.5	4.0	ns	
Large Signal	1.0	1.25		V/ns	
Toggle Rate			100	MHz	ECL Output Level
Overshoot and Preshoot					
In Driver Mode					
1V Swing			200	mV	
>2V Swing			120	mV	
In Inhibit Mode		350		mV	
Settling Characteristic			5	% of Steady State 50ns after Starting Time of Voltage Slew. Steady State is Greater Than 1ms after Starting Time of Voltage Slew.	
Inhibit Delay Time					
Inhibit to Active	14	15	16	ns	See Notes 6 & 7
Active to Inhibit	5.5	8	10 5	ns	See Notes 6 & 7
Output Impedance	47.5	50	52.5	Ω	See Note 8
POWER SUPPLIES					
$-V_S$ to $+V_S$ Range	20		25	Volts	
Positive Supply Range	+11	+12	+15	Volts	
Negative Supply Range	−5	−8	−10	Volts	
Current		100		mA	
+PSRR V_{OH} = 8V	−70		+70	mV	+V = ±2.5%
−PSRR V_{OL} = −3V	−60		+60	mV	−V = ±2.5%
PACKAGE OPTIONS[9]					
SIP (Y-10)		AD345KY			

NOTES
[1]The maximum allowable voltage from D to $\overline{D}$ and from INH to $\overline{INH}$ is 3 5V
[2]The output voltage range is specified for −3V to +8V for typical power supply values of −8V and +12V but can be offset for different values of V_{OUT} such as 0V to +11V as long as the required headroom of 4V between V_H and $+V_S$ are maintained and the negative headroom of 5V between V_L and $-V_S$ is preserved
[3]Dynamically trimmed at 5MHz, 50% duty cycle
[4]Delay times are measured from the crossing of differential ECL outputs at inputs of the device to a 250mV transition at output with V_H and V_L set to ±1V respectively
[5]Delay times, slew rates, overshoot and undershoot performance specified with a 10k, 2pF probe Oscilloscope bandwidth to exceed 300MHz
[6]Inhibit mode delay times are measured from the crossing of differential ECL outputs at INH inputs to threshold crossing at the pindriver output V_{OUT} is connected to a 100Ωload terminated at +2V dc The V_H and V_L are set to a normalized +3 5V and +0 5V respectively High delay times are measured to a +1 5V threshold Frequency is set to 10MHz with a 50% duty cycle
[7]The inhibit delay time specification allows for device-to-device variations. The stability and jitter of a given device is better than 1ns and 200ps respectively
[8]Dynamically trimmed at the factory for 50Ω Other impedance values can be obtained on special request
[9]See Section 16 for package outline information
Specifications subject to change without notice

PIN CONFIGURATION

Component Side View



PIN	SYMBOL	FUNCTION
1	V_L	VOLTAGE LOGIC LOW
2	V_H	VOLTAGE LOGIC HIGH
3	D	DRIVER INPUT
4	$\overline{D}$	$\overline{\text{DRIVER}}$ INPUT
5	$+V_S$	POSITIVE SUPPLY
6	$-V_S$	NEGATIVE SUPPLY
7	V_{OUT}	DRIVER OUTPUT
8	GND	CIRCUIT GROUND
9	$\overline{INH}$	$\overline{\text{INHIBIT}}$ INPUT
10	INH	INHIBIT INPUT

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range . . . . . 0 to +70°C
Storage Temperature Range . . . . . −65°C to +125°C
Power Supply Voltage
  $+V_S$ to GND . . . . . +15V
  $-V_S$ to GND . . . . . −10V
  Difference from $+V_S$ to $-V_S$ . . . . . +25V
Input . . . . . $-V_S$ to $+V_s$
V_{OUT} . . . . . $+V_S$ +0.6V or $-V_S$ −0.6V
V_{OUT} to Short Circuit
  to GND . . . . . Indefinitely
  to +V or $-V_S$ . . . . . 1 Minute

DETERMINING LOGIC SET LEVELS

Within a system it is possible to minimize gain error and increase the output level accuracy of the AD345 by using the information provided by Figures 1 and 2. Figure 1 is a table of desired output high levels followed by the recommended input reference levels. Figure 2 accomplishes the same for the output low levels. Values of output levels not supplied by the tables can simply be interpolated from the data supplied.

Another potential source of output level error is offset error. The value, once determined for a specific device, should be algebraically subtracted for the appropriate V_{HIGH} or V_{LOW} set value.

V OUTPUT HIGH	V_H INPUT LEVEL
−2.00V	−2.016
−1.00V	−1.009
+1.00V	+1.007
+2.00V	+2.018
+3.00V	+3.028
+4.00V	+4.041
+5.00V	+5.054
+6.00V	+6.070
+7.00V	+7.098
+8.00V	+8.150

Figure 1. Table of Normalized V_{HIGH} Levels

V OUTPUT LOW	V_L INPUT LEVEL
−3.00V	−3.012
−2.00V	−2.007
−1.00V	−1.008
+1.00V	+1.015
+2.00V	+2.023
+3.00V	+3.031
+4.00V	+4.040
+5.00V	+5.050
+6.00V	+6.060

Figure 2. Table of Normalized V_{LOW} Levels

FUNCTIONAL DESCRIPTION

The AD345 is a complete high-speed pin driver designed for use in general purpose instrumentation and digital functional test equipment. The purpose of a pin driver is to accept digital, analog and timing information from a system source and interface those elements to the input of a digital device to be tested.

The circuit configuration for the AD345 has been summarized in Figure 3. Simply stated a pin driver performs the function of a precise, controlled, high-speed level translator with an output which can be disabled. The AD345 accepts digital information utilizing high-speed comparators on the D, $\overline{D}$ and INH, $\overline{INH}$ from ECL differential outputs for precise timing at logic cross-over and high-noise immunity. The wide input voltage range allows for ECL operation between 0 to −5.2V, or +2V to −3.2V and +5V to 0V. Where timing is less critical TTL or CMOS logic levels may be used to toggle the AD345. By biasing the $\overline{D}$ and $\overline{INH}$ inputs to approximately +1.3V for TTL and $1/2V_{CC}$ for CMOS, the D and INH inputs can be directly stimulated from these single-ended output sources. The output of the pin driver will follow the logic state of the D input providing the inhibit input is low. When the inhibit level is asserted the output will be disconnected and any activity on the input will not be transferred to the output.

Analog information is input to the pin driver through the V_H and V_L terminals as a reference voltage. These analog voltages are then buffered using unity gain followers. The resulting gain error has been characterized in Figures 1 and 2. System timing requirements are achieved through a specified 2.0ns, ±500ps driver propagation delay, 1.25V/ns slew rate, defined preshoot and overshoot, and a dynamically trimmed 50Ω output impedance.

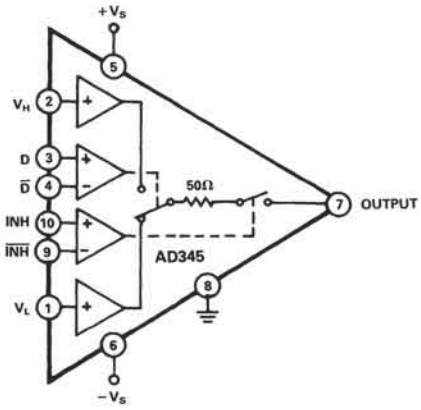


Figure 3. AD345 Block Diagram

LAYOUT CONSIDERATIONS

While it is generally considered good engineering practice to capacitively decouple an active device from the power supplies, it is absolutely essential for a high-power, high-speed device such as the AD345. The engineer merely has to consider the current pulse demanded from the power supply when a dynamic current change of -90mA to $+90$mA is required in only a few nanoseconds. Therefore, a 0.01μF high frequency decoupling capacitor must be located within 0.25 inches of the $+V_S$ and $-V_S$ terminals to a low impedance ground. A 10μF capacitor should also be situated between the power supplies and ground, however, the proximity to the device is less critical assuming low impedance power supply distribution techniques are employed. Circuit performance will be similarly enhanced and noise minimized by locating a 0.01μF capacitor as close as possible to V_H, V_L and connected to ground. Bypass considerations have been summarized in Figure 4.

An equally important consideration is the use of microwave stripline techniques on the output of the AD345. Failure to preserve the 50Ω output impedance of the pin driver will result in unwanted reflections, ringing and general corruption of the output waveshape. Care should therefore be exercised when selecting etch widths and routing, wire and cable to the device to be tested, and in choosing relays if they are required.

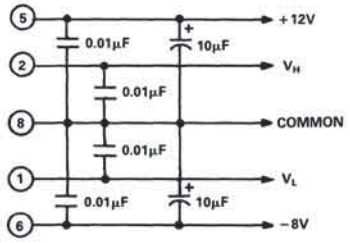


Figure 4. Basic Circuit Decoupling

The quality of the ECL differential driving source to the data inputs of the AD345 is another important consideration. The ECL driving outputs should be located close to the D and $\overline{D}$ inputs of the pin driver. Due to the low propagation delay of the AD345 excessive overshoot at the D input can be coupled to the pin driver output at low pulse amplitudes. In this case, an isolation resistor of approximately 62Ω can be inserted between the ECL output and the D input to the pin driver without any degradation in performance.

APPLICATIONS

The AD345 has been optimized to function as a pin driver in an ATE test system. Shown in Figure 5 is a block diagram illustrating the electronics behind a single pin of a high-speed digital functional test system with the ability to test I/O pins on logic devices. The AD345 pin driver, AD96687 high-speed dual comparator, and the AD394 quad 12-bit voltage DAC would comprise the pin electronics portion of the test system. Such a system could operate at 100MHz in the data mode or 50MHz in the I/O mode, yet fit into a neat trim package.

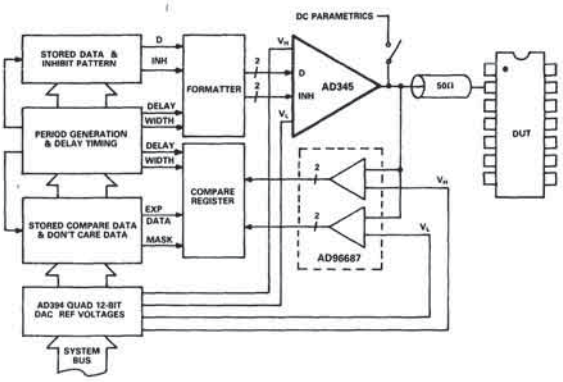


Figure 5. High-Speed Digital Test System Block Diagram

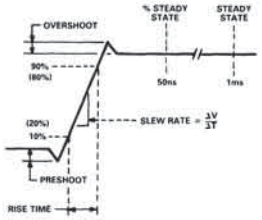


Figure 6. Definition of Terms

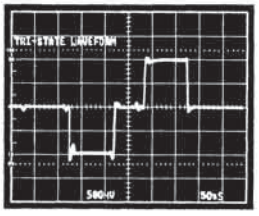


Figure 7. ±1 Volt Waveform with Inhibit (Output Terminated into 50Ω)

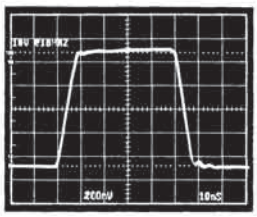


Figure 8. Large Signal 50ns Pulse

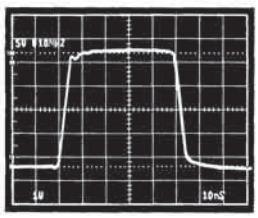
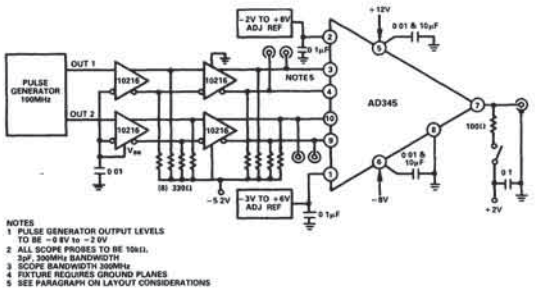


Figure 9. 5 Volt 50ns Pulse



NOTES
1 PULSE GENERATOR OUTPUT LEVELS TO BE +0.8V to −2.0V
2 ALL SCOPE PROBES TO BE 10kΩ, 3pF, 300MHz BANDWIDTH
3 SCOPE BANDWIDTH 300MHz
4 FIXTURE REQUIRES GROUND PLANES
5 SEE PARAGRAPH ON LAYOUT CONSIDERATIONS

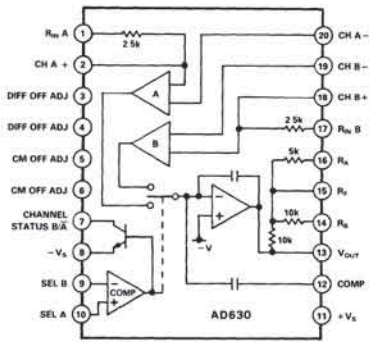
Figure 10. AD345 Test Setup

Balanced Modulator/Demodulator

AD630

FEATURES
Recovers Signal from +100dB Noise
2MHz Channel Bandwidth
45V/μs Slew Rate
−120dB Crosstalk @ 1kHz
Pin Programmable Closed Loop Gains of ±1 and ±2
0.05% Closed Loop Gain Accuracy and Match
100μV Channel Offset Voltage (AD630BD)
350kHz Full Power Bandwidth
Chips Available

AD630 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD630 is a high precision balanced modulator which combines a flexible commutating architecture with the accuracy and temperature stability afforded by laser wafer trimmed thin film resistors. Its signal processing applications include balanced modulation and demodulation, synchronous detection, phase detection, quadrature detection, phase sensitive detection, lock-in amplification and square wave multiplication. A network of on-board applications resistors provides precision closed loop gains of ±1 and ±2 with 0.05% accuracy (AD630B). These resistors may also be used to accurately configure multiplexer gains of +1, +2, +3 or +4. Alternatively, external feedback may be employed allowing the designer to implement his own high gain or complex switched feedback topologies.

The AD630 may be thought of as a precision op amp with two independent differential input stages and a precision comparator which is used to select the active front end. The rapid response time of this comparator coupled with the high slew rate and fast settling of the linear amplifiers minimize switching distortion. In addition, the AD630 has extremely low crosstalk between channels of −100dB @ 10kHz.

The AD630 is intended for use in precision signal processing and instrumentation applications requiring wide dynamic range. When used as a synchronous demodulator in a lock-in amplifier configuration, it can recover a small signal from 100dB of interfering noise (see lock-in amplifier application). Although optimized for operation up to 1kHz, the circuit is useful at frequencies up to several hundred kilohertz.

Other features of the AD630 include pin programmable frequency compensation, optional input bias current compensation resistors, common mode and differential offset voltage adjustment, and a channel status output which indicates which of the two differential inputs is active.

PRODUCT HIGHLIGHTS

1. The configuration of the AD630 makes it ideal for signal processing applications such as: balanced modulation and demodulation, lock-in amplification, phase detection, and square wave multiplication.
2. The application flexibility of the AD630 makes it the best choice for many applications requiring precisely fixed gain, switched gain, multiplexing, integrating-switching functions, and high-speed precision amplification.
3. The 100dB dynamic range of the AD630 exceeds that of any hybrid or IC balanced modulator/demodulator and is comparable to that of costly signal processing instruments.
4. The op-amp format of the AD630 ensures easy implementation of high gain or complex switched feedback functions. The application resistors facilitate the implementation of most common applications with no additional parts.
5. The AD630 can be used as a two channel multiplexer with gains of +1, +2, +3 or +4. The channel separation of 100dB @ 10kHz approaches the limit which is achievable with an empty IC package.
6. The AD630 has pin-strappable frequency compensation (no external capacitor required) for stable operation at unity gain without sacrificing dynamic performance at higher gains.
7. Laser trimming of comparator and amplifying channel offsets eliminates the need for external nulling in most cases.

SPECIFICATIONS (@ +25°C and $\pm V_S$ = ±15V unless otherwise specified)

Model	AD630J/A			AD630K/B			AD630S			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
GAIN										
Open Loop Gain	90	110		100	120		90	110		dB
±1, ±2 Closed Loop Gain Error		0.1				0.05		0.1		%
Closed Loop Gain Match		0.1				0.05		0.1		%
Closed Loop Gain Drift		2			2			2		ppm°C
CHANNEL INPUTS										
V_{IN} Operational Limit[1]	$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			$(-V_S+4V)$ to $(+V_S-1V)$			Volts
Input Offset Voltage			500			100			500	µV
Input Offset Voltage										
T_{min} to T_{max}			800			160			1000	µV
Input Bias Current		100	300		100	300		100	300	nA
Input Offset Current		10	50		10	50		10	50	nA
Channel Separation @ 10kHz		100			100			100		dB
COMPARATOR										
V_{IN} Operational Limit[1]	$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.5V)$			$(-V_S+3V)$ to $(+V_S-1.3V)$			Volts
Switching Window			±1.5			±1.5			±1.5	mV
Switching Window										
T_{min} to T_{max}[2]			±2.0			±2.0			±2.5	mV
Input Bias Current		100	300		100	300		100	300	nA
Response Time (−5mV to +5mV step)		200			200			200		ns
Channel Status										
I_{SINK} @ $V_{OL} = -V_S + 0.4V$[3]	1.6			1.6			1.6			mA
Pull-Up Voltage			$(-V_S+33V)$			$(-V_S+33V)$			$(-V_S+33V)$	Volts
DYNAMIC PERFORMANCE										
Unity Gain Bandwidth		2			2			2		MHz
Slew Rate[4]		45			45			45		V/µs
Settling Time to 0.1% (20V step)		3			3			3		µs
OPERATING CHARACTERISTICS										
Common-Mode Rejection	85	105		90	110		90	110		dB
Power Supply Rejection	90	110		90	110		90	110		dB
Supply Voltage Range	±5		±16.5	±5		±16.5	±5		±16.5	Volts
Supply Current		4	5		4	5		4	5	mA
OUTPUT VOLTAGE, @ R_L = 2kΩ										
T_{min} to T_{max}	±10			±10			±10			Volts
Output Short Circuit Current		25			25			25		mA
TEMPERATURE RANGES										
Rated Performance – N Package	0		+70	0		+70		N/A		°C
D Package	−25		+85	−25		+85	−55		+125	°C

NOTES
[1] If one terminal of each differential channel or comparator input is kept within these limits the other terminal may be taken to the positive supply.
[2] This parameter guaranteed but not tested.
[3] I_{SINK} @ $V_{OL} = (-V_S + 1)$ volt is typically 4mA.
[4] Pin 12 Open. Slew rate with Pins 12 & 13 shorted is typically 35V/µs.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	600mW
Output Short Circuit to Ground	Indefinite
Storage Temperature, Ceramic Package	−65°C to +150°C
Storage Temperature, Plastic Package	−55°C to +125°C
Lead Temperature, 10 sec. Soldering	+300°C
Max Junction Temperature	+150°C

ORDERING GUIDE

Model	Package Options*
AD630JN	Plastic (N-20)
AD630KN	Plastic (N-20)
AD630AD	Ceramic (D-20)
AD630BD	Ceramic (D-20)
AD630SD	Ceramic (D-20)

*See Section 16 for package outline information.

Typical Performance Characteristics

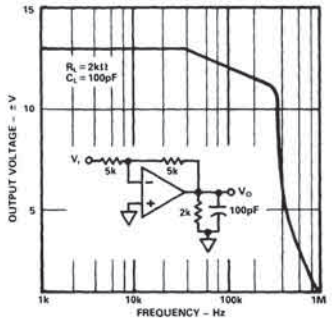


Figure 1. Output Voltage vs. Frequency

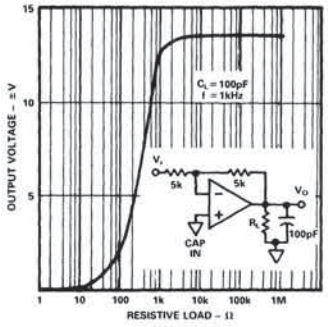


Figure 2. Output Voltage vs. Resistive Load

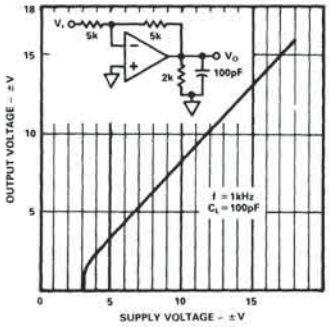


Figure 3. Output Voltage Swing vs. Supply Voltage

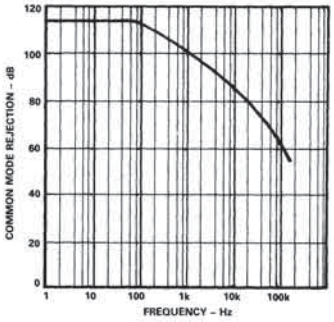


Figure 4. Common Mode Rejection vs. Frequency

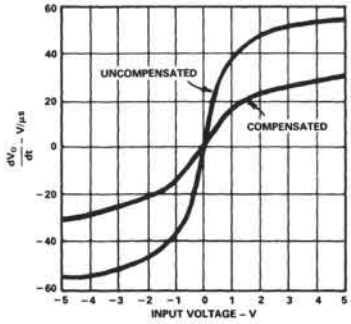


Figure 5. $\frac{dV_O}{dt}$ vs. Input Voltage

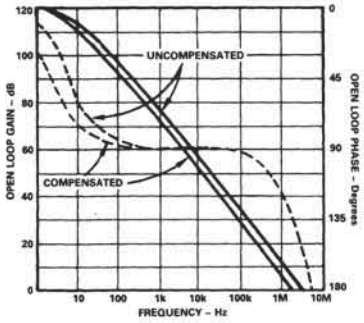
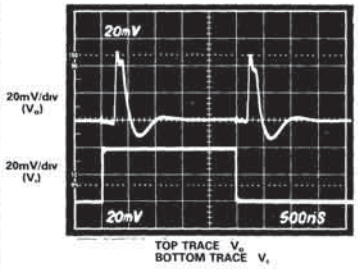


Figure 6. Gain and Phase vs. Frequency

9



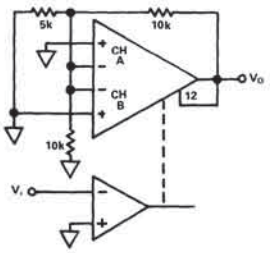
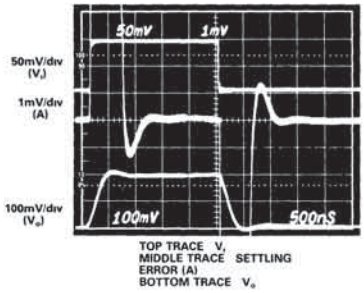


Figure 7. Channel-to-Channel Switch-Settling Characteristic



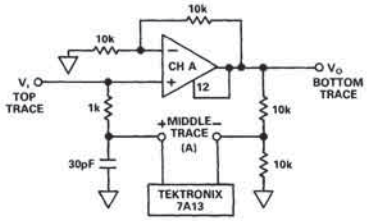
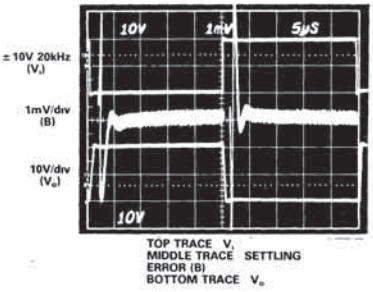


Figure 8. Small Signal Noninverting Step Response



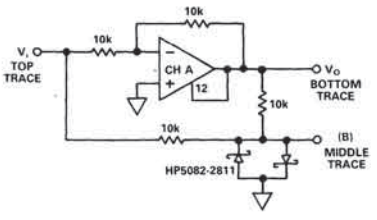
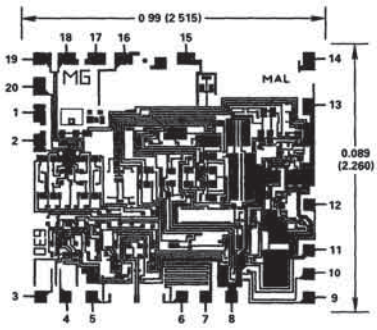


Figure 9. Large Signal Inverting Step Response

CHIP METALLIZATION AND PIN OUT

Dimensions shown in inches and (mm).



CHIP AVAILABILITY

The AD630 is available in laser trimmed, passivated chip form. The figure shows the AD630 metalization pattern, bonding pads and dimensions. AD630 chips are available; consult factory for details.

TWO WAYS TO LOOK AT THE AD630

Figure 10 is a functional block diagram of the AD630 which also shows the pin connections of the internal functions. An alternative architectural diagram is shown in Figure 11. In this diagram, the individual A and B channel pre-amps, the switch, and the integrator-output amplifier are combined in a single op amp. This amplifier has two differential input channels, only one of which is active at a time.

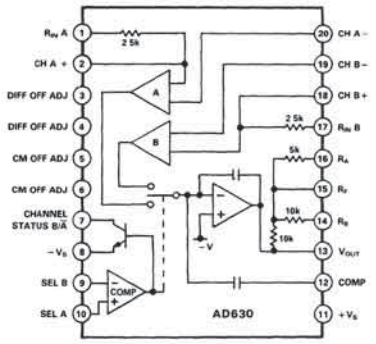


Figure 10. Functional Block Diagram

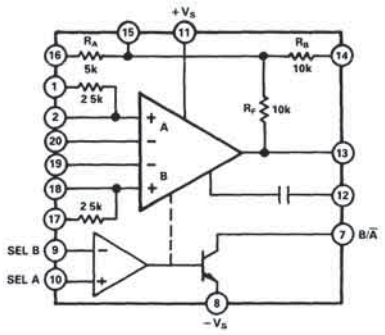


Figure 11. Architectural Block Diagram

HOW THE AD630 WORKS

The basic mode of operation of the AD630 may be more easy to recognize as two fixed gain stages which may be inserted into the signal path under the control of a sensitive voltage comparator. When the circuit is switched between inverting and noninverting gain, it provides the basic modulation/demodulation function. The AD630 is unique in that it includes laser wafer trimmed thin film feedback resistors on the monolithic chip. The configuration shown below yields a gain of ±2 and can be easily changed to ±1 by shifting R_B from its ground connection to the output.

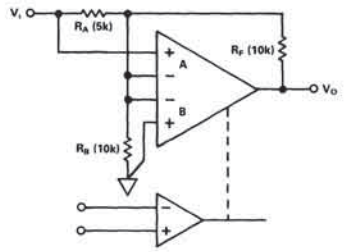


Figure 12. AD630 Symmetric Gain (±2)

The comparator selects one of the two input stages to complete an operational feedback connection around the AD630. The de-selected input is off and has negligible effect on the operation.

When channel B is selected, the resistors R_A and R_F are connected for inverting feedback as shown in the inverting gain configuration diagram in Figure 13. The amplifier has sufficient loop gain to minimize the loading effect of R_B at the virtual ground produced by the feedback connection. When the sign of the comparator input is reversed, input B will be de-selected and A will be

selected. The new equivalent circuit will be the noninverting gain configuration shown below. In this case R_A will appear across the op-amp input terminals, but since the amplifier drives this difference voltage to zero the closed loop gain is unaffected.

The two closed loop gain magnitudes will be equal when $R_F/R_A = 1 + R_F/R_B$, which will result from making R_A equal to $R_F R_B/(R_F + R_B)$ the parallel equivalent resistance of R_F and R_B.

The 5k and the two 10k resistors on the AD630 chip can be used to make a gain of two as shown here. By paralleling the 10k resistors to make R_F equal 5k and omitting R_B the circuit can be programmed for a gain of ± 1 (as shown in Figure 19a). These and other configurations using the on chip resistors present the inverting inputs with a 2.5k source impedance. The more complete AD630 diagrams show 2.5k resistors available at the noninverting inputs which can be conveniently used to minimize errors resulting from input bias currents.

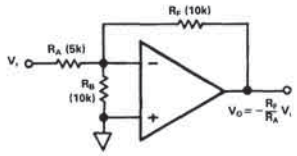


Figure 13. Inverting Gain Configuration

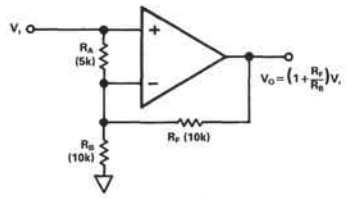


Figure 14. Noninverting Gain Configuration

CIRCUIT DESCRIPTION

The simplified schematic of the AD630 is shown in Figure 15. It has been subdivided into three major sections, the comparator, the two input stages and the output integrator. The comparator consists of a front end made up of Q52 and Q53, a flip-flop load formed by Q3 and Q4, and two current steering switching cells Q28, Q29 and Q30, Q31. This structure is designed so that a differential input voltage greater than 1.5mV in magnitude applied to the comparator inputs will completely select one of the switching cells. The sign of this input voltage determines which of the two switching cells is selected.

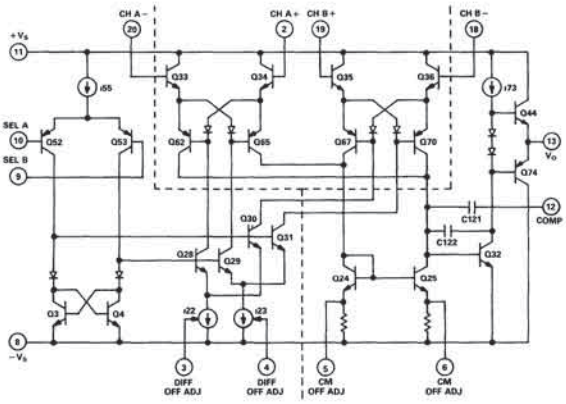


Figure 15. AD630 Simplified Schematic

The collectors of each switching cell connect to an input transconductance stage. The selected cell conveys bias currents i_{22} and i_{23} to the input stage it controls causing it to become active. The deselected cell blocks the bias to its input stage which, as a consequence, remains off.

The structure of the transconductance stages is such that they present a high impedance at their input terminals and draw no bias current when deselected. The deselected input does not interfere with the operation of the selected input insuring maximum channel separation.

Another feature of the input structure is that it enhances the slew rate of the circuit. The current output of the active stage follows a quasi-hyperbolic-sine relationship to the differential input voltage. This means that the greater the input voltage, the harder this stage will drive the output integrator, and hence, the faster the output signal will move. This feature helps insure rapid, symmetric settling when switching between inverting and noninverting closed loop configurations.

The output section of the AD630 includes a current mirror-load (Q24 and Q25), an integrator-voltage gain stage (Q32), and a complementary output buffer (Q44 and Q74). The outputs of both transconductance stages are connected in parallel to the current mirror. Since the deselected input stage produces no output current and presents a high impedance at its outputs, there is no conflict. The current mirror translates the differential output current from the active input transconductance amplifier into single ended form for the output integrator. The complementary output driver then buffers the integrator output to produce a low impedance output.

OTHER GAIN CONFIGURATIONS

Many applications require switched gains other than the ± 1 and ± 2 which the self-contained applications resistors provide. The AD630 can be readily programmed with 3 external resistors over a wide range of positive and negative gain by selecting R_B and R_F to give the noninverting gain $1 + R_F/R_B$ and subsequently R_A to give the desired inverting gain. Note that when the inverting magnitude equals the noninverting magnitude, the value of R_A is found to be $R_B R_F/(R_B + R_F)$. That is, R_A should equal the parallel combination of R_B and R_F to match positive and negative gain.

The feedback synthesis of the AD630 may also include reactive impedance. The gain magnitudes will match at all frequencies if the A impedance is made to equal the parallel combination of the B and F impedances. Essentially the same considerations apply to the AD630 as to conventional op-amp feedback circuits. Virtually any function which can be realized with simple non-inverting "L network" feedback can be used with the AD630. A common arrangement is shown in Figure 16. The low frequency gain of this circuit is 10. The response will have a pole (−3dB) at a frequency $f \simeq 1/(2\pi 100k\Omega C)$ and a zero (3dB from the high frequency asymptote) at about 10 times this frequency. The 2k resistor in series with each capacitor mitigates the loading effect on circuitry driving this circuit, eliminates stability problems, and has a minor effect on the pole-zero locations.

As a result of the reactive feedback, the high frequency components of the switched input signal will be transmitted at unity gain

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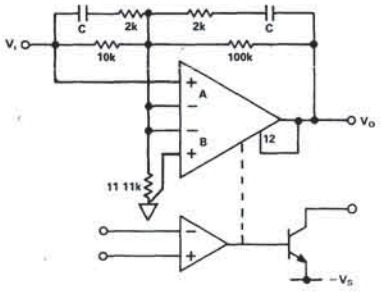


Figure 16. AD630 with External Feedback

while the low frequency components will be amplified. This arrangement is useful in demodulators and lock-in amplifiers. It increases the circuit dynamic range when the modulation or interference is substantially larger than the desired signal amplitude. The output signal will contain the desired signal multiplied by the low frequency gain (which may be several hundred for large feedback ratios) with the switching signal and interference superimposed at unity gain.

SWITCHED INPUT IMPEDANCE

The noninverting mode of operation is a high input impedance configuration while the inverting mode is a low input impedance configuration. This means that the input impedance of the circuit undergoes an abrupt change as the gain is switched under control of the comparator. If gain is switched when the input signal is not zero, as it is in many practical cases, a transient will be delivered to the circuitry driving the AD630. In most applications, this will require the AD630 circuit to be driven by a low impedance source which remains "stiff " at high frequencies. Generally this will be a wideband buffer amplifier.

FREQUENCY COMPENSATION

The AD630 combines the convenience of internal frequency compensation with the flexibility of external compensation by means of an optional self-contained compensation capacitor.

In gain of ±2 applications the noise gain which must be addressed for stability purposes is actually 4. In this circumstance, the phase margin of the loop will be on the order of 60° without the optional compensation. This condition provides the maximum bandwidth and slew-rate for closed-loop gains of |2| and above.

When the AD630 is used as a multiplexer, or in other configurations where one or both inputs are connected for unity gain feedback, the phase margin will be reduced to less than 20°. This may be acceptable in applications where fast slewing is a first priority, but the transient response will not be optimum. For these applications, the self-contained compensation capacitor may be added by connecting pin 12 to pin 13. This connection reduces the closed loop bandwidth somewhat, and improves the phase margin.

For intermediate conditions, such as gain of ±1 where loop attenuation is 2, use of the compensation should be determined by whether bandwidth or settling response must be optimized. The optional compensation should also be used when the AD630 is driving capacitive loads or whenever conservative frequency compensation is desired.

OFFSET VOLTAGE NULLING

The offset voltages of both input stages and the comparator have been pre-trimmed so that external trimming will only be required in the most demanding applications. The offset adjustment of the two input channels is accomplished by means of a differential and common mode scheme. This facilitates fine adjustment of system errors in switched gain applications. With system input tied to 0V, and a switching or carrier waveform applied to the comparator, a low level square wave will appear at the output. The differential offset adjustment pot can be used to null the amplitude of this square wave (pins 3 and 4). The common mode offset adjustment can be used to zero the residual dc output voltage (pins 5 and 6). These functions should be implemented using 10k trim pots with wipers connected directly to pin 8 as shown in Figures 19a and 19b.

CHANNEL STATUS OUTPUT

The channel status output, pin 7, is an open collector output referenced to $-V_S$ which can be used to indicate which of the two input channels is active. The output will be active (pulled low) when channel A is selected. This output can also be used to supply positive feedback around the comparator. This produces hysteresis which serves to increase noise immunity. Figure 17 shows an example of how hysteresis may be implemented. Note that the feedback signal is applied to the inverting (−) terminal of the comparator to achieve positive feedback. This is because the open collector channel status output inverts the output sense of the internal comparator.

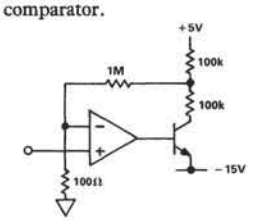


Figure 17. Comparator Hysteresis

The channel status output may be interfaced with TTL inputs as shown in Figure 18. This circuit provides appropriate level shifting from the open-collector AD630 channel status output to TTL inputs.

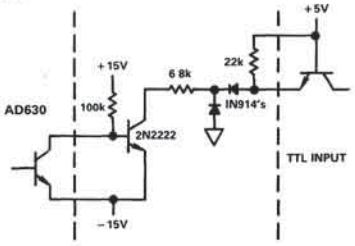


Figure 18. Channel Status – TTL Interface

APPLICATIONS:
BALANCED MODULATOR

Perhaps the most commonly used configuration of the AD630 is the balanced modulator. The application resistors provide precise symmetric gains of ±1 and ±2. The ±1 arrangement is shown in Figure 19a and the ±2 arrangement is shown in Figure 19b. These cases differ only in the connection of the 10k feedback resistor (pin 14) and the compensation capacitor (pin 12). Note the use of the 2.5kΩ bias current compensation resistors in these examples. These resistors perform the identical function in the ±1 gain case. Figure 20 demonstrates the performance of the AD630 when used to modulate a 100kHz square wave carrier with a 10kHz sinusoid. The result is the double sideband suppressed carrier waveform.

These balanced modulator topologies accept two inputs, a signal (or modulation) input applied to the amplifying channels, and a reference (or carrier) input applied to the comparator.

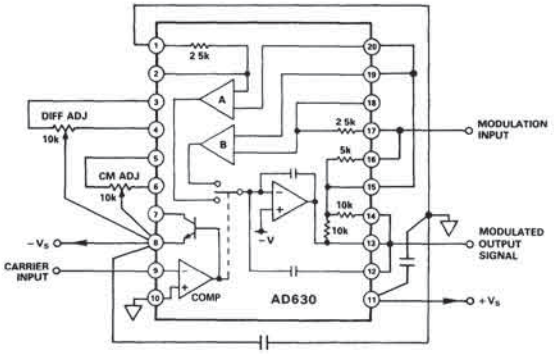


Figure 19a. AD630 Configured as a Gain-of-One Balanced Modulator

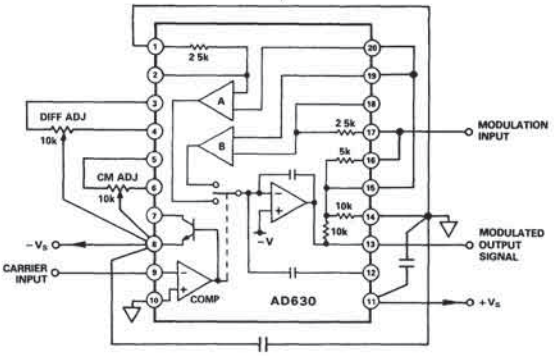


Figure 19b. AD630 Configured as a Gain-of-Two Balanced Modulator

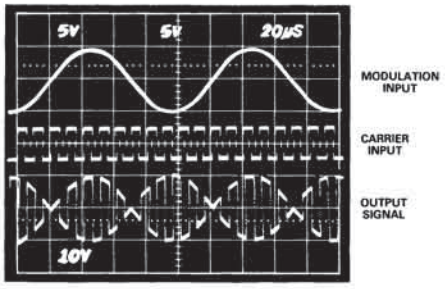


Figure 20. Gain-of-Two Balanced Modulator Sample Waveforms

BALANCED DEMODULATOR

The balanced modulator topology described above will also act as a balanced demodulator if a double sideband suppressed carrier waveform is applied to the signal input and the carrier signal is applied to the reference input. The output under these circumstances will be the baseband modulation signal. Higher order carrier components will also be present which can be removed with a low-pass filter. Other names for this function are synchronous demodulation and phase-sensitive detection.

PRECISION PHASE COMPARATOR

The balanced modulator topologies of Figures 19a and 19b can also be used as precision phase comparators. In this case, an ac waveform of a particular frequency is applied to the signal input and a waveform of the same frequency is applied to the reference input. The dc level of the output (obtained by low pass filtering) will be proportional to the signal amplitude and phase difference between the input signals. If the signal amplitude is held constant, then the output can be used as a direct indication of the phase. When these input signals are 90° out of phase, they are said to be in quadrature and the AD630 dc output will be zero.

PRECISION RECTIFIER-ABSOLUTE VALUE

If the input signal is used as its own reference in the balanced modulator topologies, the AD630 will act as a precision rectifier. The high frequency performance will be superior to that which can be achieved with diode feedback and op amps. There are no diode drops which the op amp must "leap over" with the commutating amplifier.

LVDT SIGNAL CONDITIONER

Many transducers function by modulating an ac carrier. A Linear Variable Differential Transformer (LVDT) is a transducer of this type. The amplitude of the output signal corresponds to core displacement. Figure 21 shows an accurate synchronous demodulation system which can be used to produce a dc voltage which corresponds to the LVDT core position. The inherent precision and temperature stability of the AD630 reduce demodulator drift to a second order effect.

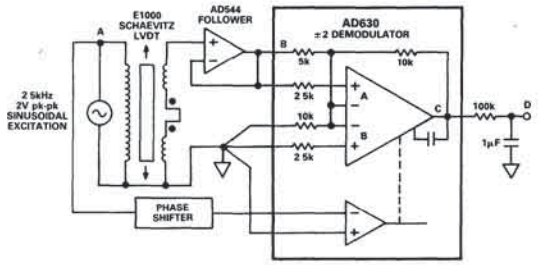


Figure 21. LVDT Signal Conditioner

AC BRIDGE

Bridge circuits which use dc excitation are often plagued by errors caused by thermocouple effects, 1/f noise, dc drifts in the electronics, and line noise pick-up. One way to get around these problems is to excite the bridge with an ac waveform, amplify the bridge output with an ac amplifier, and synchronously demodulate the resulting signal. The ac phase and amplitude information from the bridge is recovered as a dc signal at the output of the synchronous demodulator. The low frequency system noise, dc drifts, and demodulator noise all get mixed to the carrier frequency and can be removed by means of a low pass filter. Dynamic response of the bridge must be traded off against the amount of attenuation required to adequately suppress these residual carrier components in the selection of the filter.

Figure 22 is an example of an ac bridge system with the AD630 used as a synchronous demodulator. The oscilloscope photograph shows the results of a 0.05% bridge imbalance caused by the 1Meg resistor in parallel with one leg of the bridge. The top trace represents the bridge excitation, the upper-middle trace is the amplified bridge output, the lower-middle trace is the output of the synchronous demodulator and the bottom trace is the filtered dc system output.

This system can easily resolve a 0.5ppm change in bridge impedance. Such a change will produce a 3.2mV change in the low pass filtered dc output, well above the RTO drifts and noise.

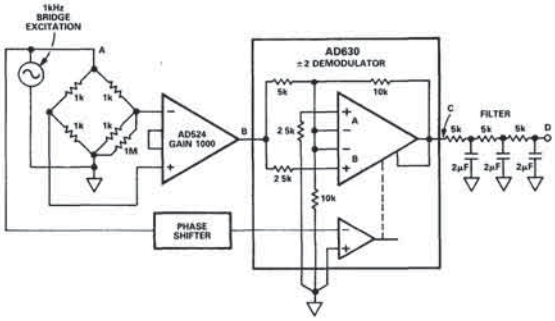


Figure 22. AC Bridge System

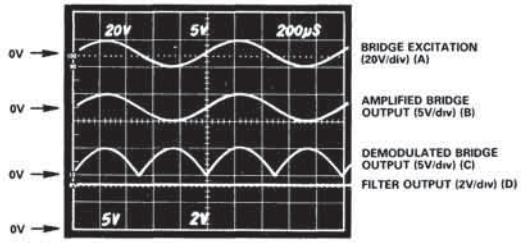


Figure 23. AC Bridge Waveforms

LOCK-IN AMPLIFIER APPLICATIONS

Lock-in amplification is a technique which is used to separate a small, narrow band signal from interfering noise. The lock-in amplifier acts as a detector and narrow band filter combined. Very small signals can be detected in the presence of large amounts of uncorrelated noise when the frequency and phase of the desired signal are known.

The lock-in amplifier is basically a synchronous demodulator followed by a low pass filter. An important measure of performance in a lock-in amplifier is the dynamic range of its demodulator. The schematic diagram of a demonstration circuit which exhibits the dynamic range of an AD630 as it might be used in a lock-in amplifier is shown in Figure 24. Figure 25 is an oscilloscope photo showing the recovery of a signal modulated at 400Hz from a noise signal approximately 100,000 times larger; a dynamic range of 100dB.

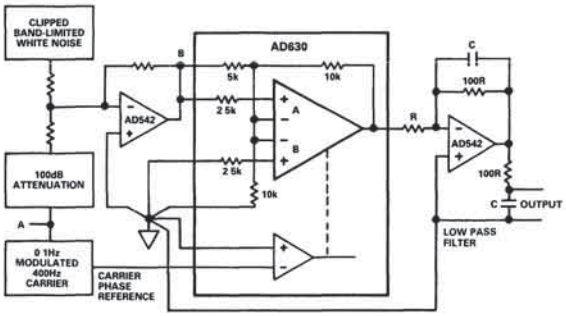


Figure 24. Lock-In Amplifier

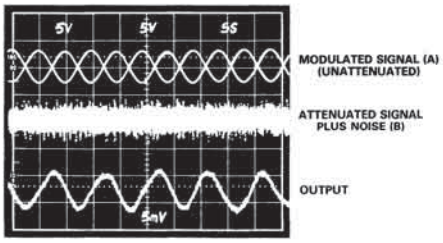


Figure 25. Lock-In Amplifier Wave Forms

The test signal is produced by modulating a 400Hz carrier with a 0.1Hz sine wave. The signals produced, for example, by chopped radiation (IR, optical, etc.) detectors may have similar low frequency components. A sinusoidal modulation is used for clarity of illustration. This signal is produced by a circuit similar to Figure 19b and is shown in the upper trace of Figure 25. It is attenuated 100,000 times normalized to the output, B, of the summing amplifier. A noise signal which might represent, for example, background and detector noise in the chopped radiation case, is added to the modulated signal by the summing amplifier. This signal is simply band limited clipped white noise. Figure 25 shows the sum of attenuated signal plus noise in the center trace. This combined signal is demodulated synchronously using phase information derived from the modulator, and the result is low pass filtered using a 2-pole simple filter which also provides a gain of 100 to the output. This recovered signal is the lower trace of Figure 25.

The combined modulated signal and interfering noise used for this illustration is similar to the signals often requiring a lock-in amplifier for detection. The precision input performance of the AD630 provides more than 100dB of signal range and its dynamic response permits it to be used with carrier frequencies more than two orders of magnitude higher than in this example. A more sophisticated low pass output filter will aid in rejecting wider bandwidth interference.

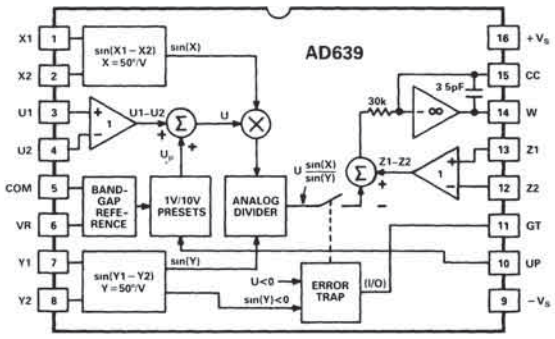
Universal Trigonometric Function Converter

AD639*

FEATURES
- Complete, Fully-Calibrated Synthesis System
- All Standard Functions: Sin, Cos, Tan, Cosec, Sec, Cot, Arcsin, Arccos, Arctan, etc.
- Accurate Law Conformance (Sine to 0.02%)
- Angular Range of ±500° (Sine Mode)
- Function Programmable by Pin Strapping
- 1.5MHz Bandwidth (Sine Mode)
- Multiplication via External Amplitude Input

APPLICATIONS
- Continuous Wave Sine Generators
- Synchro Sine/Cosine Multiplication
- Coordinate Conversion and Vector Resolution
- Imaging and Scanning Linearization Circuits
- Quadrature and Variable Phase Oscillators

AD639 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD639 is a high accuracy monolithic function converter which provides all the standard trigonometric functions and their inverses via pin-strapping. Law conformance and total harmonic distortion surpass that previously attained using analog shaping techniques. Speed also exceeds that possible using ROM look-up tables and a DAC; in the sine mode, bandwidth is typically 1.5MHz. Unlike other function synthesis circuits, the AD639 provides a smooth and continuous sine conformance over a range of −500° to +500°. A unique sine generation technique results in 0.02% law conformance errors and distortion levels of −74dB in triwave to sinewave conversion.

The AD639 is available in three performance grades. The A and B are specified from −25°C to +85°C and the S is guaranteed over the extended temperature range of −55°C to +125°C. All versions are packaged in a hermetic TO-116, 16-pin ceramic DIP.

PRODUCT HIGHLIGHTS

The AD639 generates a basic function which is the ratio of a pair of independent sines:

$$W = U \frac{\sin (x_1 - x_2)}{\sin (y_1 - y_2)}$$

The differential angle arguments are proportional to the input voltages X and Y scaled by 50°/V. Using the 1.8V on-board reference any of the angular inputs can be preset to 90°. This provides the means to set up a fixed numerator or denominator (sin 90° = 1) or to convert either sine function to a cosine (cosθ = sin (90° − θ)). Using the ratio of sines, all trigonometric functions can be generated (see Table I).

The amplitude of the function is proportional to a voltage U, which is the sum of an external differential voltage ($U_1 - U_2$) and an optional internal preset voltage (U_p). The control pin UP selects a 0V, 1V or 10V laser-trimmed preset amplitude which may be used alone ($U_1 - U_2 = 0$) or internally added to the $U_1 - U_2$ analog input. At the output, a further differential voltage Z can be added to the ratio of sines to obtain the offset trigonometric functions versine (1 − cos θ), coversine (1 − sin θ) and exsecant (1 − sec θ). A gating input is available which may be used to enable or disable the analog output. This pin also acts as an error flag output in situations where a combination of inputs will cause the output to saturate or to be undefined.

In the inverse modes, the argument can be the ratio of two input signals. This allows the user to compute the phase angle between the real and imaginary components of a signal using the arctangent mode.

*Protected by U.S. Patent Numbers 3,887,863; 4,475,169; 4,476,538.

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SPECIFICATIONS (typical @T_A = 25°C, V_S = ±15V, U or U_p = 10V unless otherwise specified)

Parameter	Conditions	AD639A Min	AD639A Typ	AD639A Max	AD639B Min	AD639B Typ	AD639B Max	AD639S Min	AD639S Typ	AD639S Max	Units
SYSTEM PERFORMANCE											
SINE AND COSINE MODE ACCURACY											
Law Conformance[1]	−90° to +90°, U = 10V		0.02			0.02			0.02		%
Total Harmonic Distortion[2]	@ 10kHz, U = 10V		−74			−74			−74		dB
Mismatch of Six Peaks	−540° to +540°		0.05			0.05			0.05		%
Output Noise	@ 10kHz, U = 10V		2.8			2.8			2.8		$\mu V/\sqrt{Hz}$
	@ 10kHz, U = 1V		0.5			0.5			0.5		$\mu V/\sqrt{Hz}$
PEAK ABSOLUTE ERROR											
Sine Mode	−90° to +90°, U_p = 10V		0.4	0.8		0.2	0.4		0.2	0.8	%FS
	T_{min} to T_{max}		1.0			0.8	1.8		1.2	2.5	%FS
Cosine Mode	−90° to +90°, U_p = 10V		0.6	1.2		0.4	0.7		0.5	1.2	%FS
	T_{min} to T_{max}		1.5			1.2	2.0		1.7	2.7	%FS
Sine or Cosine	−180° to +180°, U_p = 10V		0.8	1.5		0.5	0.8		0.6	1.5	%FS
	T_{min} to T_{max}		1.7			1.3	2.5		2.1	3.0	%FS
	−360° to +360°, U_p = 10V		1.2			1.0			0.9		%FS
	−90° to +90°, U_p = 1V		1.3	2.5		1.0	1.7		0.9	2.5	%FS
	T_{min} to T_{max}		1.5			1.0	2.3		2.0	3.5	%FS
	−180° to +180°, U_p = 1V		1.5	3.0		1.2	2.0		1.1	3.0	%FS
	T_{min} to T_{max}		1.7			1 3	2.5		2.3	4.0	%FS
	−360° to +360°, U_p = 1V		2.0			1.8			1.5		%FS
vs Supply	−360° to +360°, U_p = 10V V_s = ±15V ± 1V		0.02			0.02			0.02		%FS/V
	−360° to +360°, U_p = 1V V_s = ±15V ± 1V		0.07			0.07			0.07		%FS/V
TANGENT MODE ACCURACY											
Peak Error[3]	−45° to +45°, U_p = 10V		0.5	3.5		0.5	2.0		0.5	3.5	%FS
	T_{min} to T_{max}		2.5			1.5	2.8		3.0		%FS
	−45° to +45°, U_p = 1V		0.9	5.0		0.9	3.0		0.9	2.5	%FS
	T_{min} to T_{max}		4.0			2.0	5.0		1.5	3.0	%FS
ARCTANGENT MODE ACCURACY											
Peak Angular Error											
Fixed Scale	U_p = 1V		0.5			0.5			0 5		Degrees
Variable Scale	U = 0.1V, −11V≤Z≤+11V		1.5			1.5			1.5		Degrees
	U = 10V, −11V≤Z≤+11V		0.2			0.2			0.2		Degrees
SECTIONAL SPECIFICATIONS											
ANGLE INPUTS (X1 & X2, Y1 & Y2)[4]											
Input Resistance to COM			3.6			3.6			3.6		kΩ
Nominal Scaling Factor			50			50			50		°/V
X1 & X2 Inputs											
Angular Range For Specified Error(X1 − X2)		−360		+360	−360		+360	−360		+360	Degrees
Scaling Error X1 or X2			0.2	0.65		0.2	0.65		0 2	0.65	%
Angular Offset X1 = X2 = 0			0.1	0.3		0.1	0.3		0.1	0.3	Degrees
Y1 & Y2 Inputs											
Angular Range For Specified Error (Y1 − Y2)		0		+180	0		+180	0		+180	Degrees
Scaling Error Y1 or Y2			0.2	2.0		0.2	2.0		0.2	1.0	%
Angular Offset Y1 = Y2 = 0			0.1	1.0		0.1	1.0		0.1	0.5	Degrees
AMPLITUDE INPUTS (U1 & U2)											
Input Resistance to COM			50			50			50		kΩ
Nominal Gain	X = Y = VR, W to Z1		1			1			1		V/V
Gain Error	U = 0.1 to 10V		0.01	0.5		0.01	0.5		0.01	0.5	%
	T_{min} to T_{max}		0.08			0.08			0.25		%
Voltage Offset	$U_1 = U_2 = 0V$		.3.0	10		3.0	10		3.0	10	mV
	T_{min} to T_{max}		3.0			3.0			4.0		mV
Linearity Error	$0 \le U_1 - U_2 \le 10V$		0.1			0.1			0.1		%
AMPLITUDE PRESET (UP)											
1V Preset Enabled	UP tied to $-V_S$										
Amplitude Accuracy			0.4	2.0		0.4	2.0		0.4	2.0	%
	T_{min} to T_{max}		1.5			1.5			2.0		%
10V Preset Enabled	UP tied to $+V_S$										
Amplitude Accuracy			0.1	0.55		0.1	0.55		0.1	0.55	%
	T_{min} to T_{max}		1.0			1.0			1.5		%
INVERSE INPUTS (Z1 & Z2)											
Input Resistance to COM			50			50			50		kΩ

Parameter	Conditions	AD639A Min	AD639A Typ	AD639A Max	AD639B Min	AD639B Typ	AD639B Max	AD639S Min	AD639S Typ	AD639S Max	Units
SIGNAL OUTPUT (W)[5]	$R_L \geq 2k\Omega$, $C_L \leq 100pF$										
Small Signal Bandwidth W to Z1											
	$C_C = 0$		1.5			1.5			1.5		MHz
	$C_C = 200pF$		30			30			30		kHz
Slew Rate	$C_C = 0$		30			30			30		V/μS
Output Voltage Swing		**±11**	±13		**±11**	±13		**±11**	±13		V
Short Circuit Current		**20**	30	**45**	**20**	30	**45**	**20**	30	**45**	mA
Output Offset	$Z_1 = Z_2 = 0$, $U_p = 10$		5	**30**		5	**30**		5	**30**	mV
	T_{min} to T_{max}		10			10					mV
	$Z_1 = Z_2 = 0$, $U_p = 1V$			**20**			**20**			**20**	mV
	T_{min} to T_{max}		7			7					mV
VOLTAGE REFERENCE (VR)											
$R_L \geq = 1.8k\Omega$											
Nominal Output			+1.8			+1.8			+1.8		V
Output Voltage Tolerance			0.05	**0.45**		0.05	**0.45**		0.05	**0.45**	%
	T_{min} to T_{max}		0.08			0.08	**0.5**		0.2	**0.6**	%
Supply Regulation	$+V_S = 5V$ to 18V		150			150			150		μV/V
Maximum Output Current			4			4			4		mA
GATE I/O (GT)											
Switching Threshold as an Input	Output Valid		+1.5			+1.5			+1.5		V
	Output Invalid		0.1			0.1			0.1		V
Voltage Output	Error, $R_L = 5k\Omega$		+2.25			+2.25			+2.25		V
	No Error, $R_L = 5k\Omega$		−0.25			−0.25			−0.25		V
POWER SUPPLIES											
Operating Range		±5.5		**±18**	±5.5		**±18**	±5.5		**±18**	V
$+V_S$ Quiescent Current	U = X = 0V, Y = Vr		8.0	**11**		8.0	**11**		8.0	**11**	mA
$-V_S$, Quiescent Current	U = X = 0V, Y = Vr		5.5	**7.5**		5 5	**7.5**		5.5	**7.5**	mA
TEMPERATURE RANGE											
Operating, Rated Performance		−25		+85	−25		+85	−55		+125	°C
Storage		−65		+150	−65		+150	−65		+150	°C
PACKAGE OPTION[6]											
D-16											

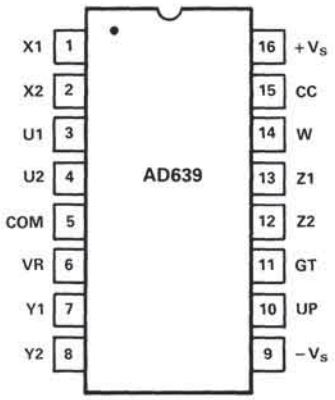
NOTES
[1]Intrinsic accuracy measured at an amplitude of 10V using external adjustments to absorb residual errors in angular scaling, angular offset, amplitude scaling and output offset
[2]Using a time and amplitude symmetric triangular wave of +3 6V peak-to-peak and external adjustments to absorb residual errors in angular scaling and offset
[3]Full-scale is defined as the ideal output when the angle input is at either end of the limit specified
[4]Specifications for the X inputs apply for range U = 1V to 10V, while the Y input errors are specifically given for U = 1V
[5]When driving loads of less than 4kΩ, a 25pF capacitor from pin 15 to pin 9 avoids possible instability, although this is unnecessary when C_L is greater than 150pF
[6]See Section 16 for package outline information.

Specifications subject to change without notice

Specifications shown in boldface are tested on all production units at final electrical test Results from those tests are used to calculate outgoing quality levels
All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.
Shaded area denotes preliminary technical data Contact the factory for details.

9

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

	AD639A,B	AD639S
Supply Voltage	±18V	*
Internal Power Dissipation	300mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages X_1, X_2, Y_1, Y_2[1]	±12V	*
Input Voltages U_p, U_1, U_2, Z_1, Z_2[1]	±25V	*
Operating Temperature Range	−25°C to +85°C	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C	*
Lead Temperature, Soldering	60sec, +300°C	*

NOTES
*Same as AD639A,B Specifications
[1]These inputs are purely resistive and the maximum inputs are determined by resistor dissipation limits, not the supply voltages.

$\sin(\theta)$	$= \frac{\sin(\theta)}{1} =$	$\frac{\sin(\theta-0)}{\sin(90°-0)}$	$\text{cosec}(\theta)$	$= \frac{1}{\sin(\theta)} =$	$\frac{\sin(90°-0)}{\sin(\theta-0)}$
$\cos(\theta)$	$= \frac{\cos(\theta)}{1} =$	$\frac{\sin(90°-\theta)}{\sin(90°-0)}$	$\sec(\theta)$	$= \frac{1}{\cos(\theta)} =$	$\frac{\sin(90°-0)}{\sin(90°-\theta)}$
$\tan(\theta)$	$= \frac{\sin(\theta)}{\cos(\theta)} =$	$\frac{\sin(\theta-0)}{\sin(90°-\theta)}$	$\text{cotan}(\theta)$	$= \frac{\cos(\theta)}{\sin(\theta)} =$	$\frac{\sin(90°-\theta)}{\sin(\theta-0)}$

Table I.

Principles Of Operation

Figure 1 is a functional equivalent of the AD639, intended to assist in understanding and utilizing the device: it is not a literal representation of the internal circuitry[1]. Two similar sine-shaping networks accept input voltages X_1, X_2, Y_1 and Y_2, proportional to the corresponding angles x_1, x_2, y_1 and y_2, with a scaling factor of 50°/V (20mV/°).

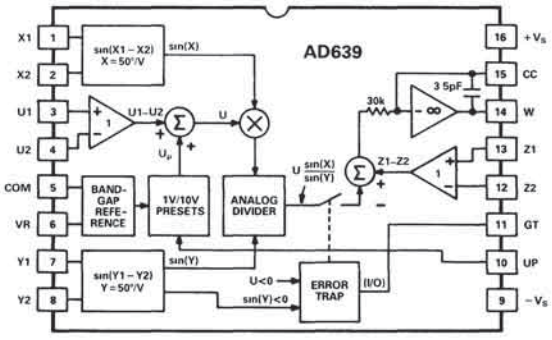


Figure 1. Equivalent Block Schematic of the AD639

The first of these networks generates an output proportional to the sine of $x=(x_1-x_2)$ over a useful operating range in excess of −500° to +500° (see Figure 3). The accuracy of the function over the central ±180° is excellent, a consequence of the optimized network design, further enhanced by precision laser wafer trimming during manufacture. The output of the X-network is multiplied by the amplitude-control voltage, U. This may be provided by applying inputs to U1 or U2, or pre-selected to be 1V or 10V by a control input to UP, or in combination; that is, the function amplitude is $U=(U_1-U_2)+U_p$.

The second network generates an output proportional to the sine of $y=(y_1-y_2)$. Although the X and Y networks are similar, other design considerations result in a smaller angular range for the Y-input. The principal range is from 0° to +180°; in the adjacent ranges (+180° to +360° and 0° to −180°) the error trap is activated.

The ratio of the two sines is generated by *implicit* division, rather than by use of a separate analog divider as indicated in Figure 1, and is summed with the voltage $Z=(Z_1-Z_2)$. The difference is applied to the high-gain output op-amp. In the *normal* modes (see below) Z1 is connected to the output W, and Z2 is grounded. Under these conditions, the function is

$$W = U\frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)}$$

Either sine function can be converted to the cosine by applying the input to X2 or Y2 and introducing a +90° offset, since

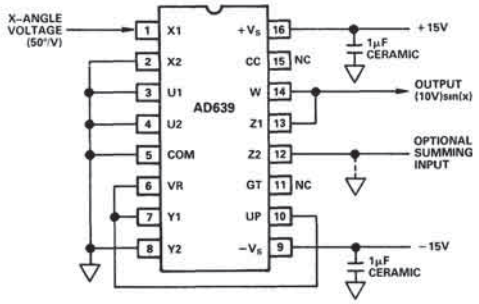


Figure 2. Connections for the Sine Mode with Amplitude Preset to 10V

[1]For details of the sine-network theory and design, see "A Monolithic Microsystem for Analog Synthesis of Trigonometric Functions and their Inverses," Barrie Gilbert, *IEEE Journal of Solid-State Circuits*, Vol. SC-17, No. 6, Dec. 1982, pp 1179-1191. Reprints available.

cos (θ) = sin(90° − θ). For example, by connecting the +1.8V reference output at pin 6 (VR) to X1 and the angle voltage, V_θ, to X2 the numerator becomes the cosine of angle θ. Alternatively, by connecting VR to either X1 or Y1 and grounding X2 or Y2, the numerator or denominator, respectively, becomes unity, since sin(90° − 0) = 1. By these means, the full set of *normal* functions shown in Table I can be generated. All functions can be sign-inverted by interchanging the X-inputs. The Z2 input can be used to sum another function to the output, W, with unity gain.

In addition to the *normal* modes providing sine, cosine, tangent, cosecant, secant and cotangent functions, the AD639 can generate the *offset* functions such as the versine, 1 − cos (θ), discussed below. The *inverse* functions such as arc-sine, arc-cosine and arc-tangent, are also supported by the AD639, by closing the feedback loop through the corresponding *normal* function. The output angle is limited to the principal range (for example, −90° to +90° for the arc-sine and arc-tangent, 0° to +180° or −180° to 0° for the arc-cosine).

TERMINOLOGY

When discussing a device having as many inputs and operating modes as the AD639, it is important to clarify the nomenclature and scaling conventions. In all cases *angles* are denoted by lower-case letters (x, y, θ) and have the dimension of angular degrees. Upper-case letters (A, V, U, W, X, Y and Z) refer to *voltages*; subscripts are used to refer to one or the other of a differential pair such as $X_1 - X_2$, or the preset value U_p. Numbered upper-case letters refer to the variable name or the package pin.

THE ANGLE INPUTS: X1, X2, Y1, Y2

The angles $x = (x_1 - x_2)$ and $y = (y_1 - y_2)$ are directly proportional to the differential voltages $X = (X_1 - X_2)$ and $Y = (Y_1 - Y_2)$ respectively, with a scaling factor of 50°/V. The X-inputs can be driven to ±12V pk, that is ±600°. The Y-input should be limited to 0 to +3.6V (0° to +180°) to satisfy certain internal requirements. The resistance at these inputs is nominally 3.6kΩ to COM.

The sine function exhibits odd-order symmetry: sin(−θ) = −sin(θ). By simply interchanging the X-inputs, the overall sign of any function can be inverted. The Y-inputs can also be interchanged to allow operation with a negative input voltage (0 to −3.6V) while maintaining the correct angular range.

It may occasionally be desirable to reduce the angular scaling factor. For example, to convert a triwave of ±10V amplitude into a continuous sinewave requires a scaling factor of 9°/V (since ±10V corresponds to ±90°). This can be achieved by using a resistor (in this case, about 16.4kΩ) in series with the X1 input; a resistor of equal value must be inserted in series with the X2 input to minimize angular offset error. Note that the on-chip thin-film resistors are not trimmed to absolute value, so a scaling adjustment is needed; however, once set, scaling will be stable.

THE AMPLITUDE-CONTROL INPUTS: U1, U2, UP

The amplitude of the function can be determined either by the application of an external voltage to the U1 and U2 inputs, or by enabling the internal preset voltage U_p by taking the control pin UP low or high, or via a combination of these modes. The net amplitude is $U = (U_1 - U_2) + U_p$. This sum must be greater than zero and less than $|-V_s|$; voltages beyond these limits activate the error trap.

In the external mode, the differential voltage $(U_1 - U_2)$ will generally be in the range 10mV to 10V. Positive inputs are applied to U1 while U2 is grounded; for negative inputs, interchange U1 and U2. The input resistance at U1 and U2 is nominally 50kΩ to analog common. A nominal bias current of −50μA is needed at the U-inputs; zero-valued inputs must therefore be connected to common to prevent offset error. The gain from the U-interface to the output is trimmed to be unity for sin(x)/sin(y) = 1. The effective gain can be lowered using a series resistor; to avoid offset an equal resistor must be used in the zero-valued input.

The UP control pin may be left unconnected (or grounded) to disable the internal amplitude preset, connected to $+V_s$ to set $U_p = 10V$, or to $-V_s$ to set $U_p = 1V$. An external resistor of 75kΩ ($\pm V_s = 5V$) to 360kΩ ($\pm V_s = 15V$) can be inserted in series with UP (which also has an input resistance of typically 50kΩ) to minimize power dissipation. Alternatively, V_r can be used to enable $U_p = 10V$ for ambient temperatures below +60°C. The UP input can be used to switch the output on or off under logic control, but requires a relatively long response time. The GT interface is more suitable for this purpose and it allows gating to any amplitude, U not just to the preset values of 1V or 10V.

THE REFERENCE OUTPUT: VR

The voltage V_r is laser-trimmed to +1.8V with respect to analog common. It can be used to fix the angle x or y to 90° and thus set sin(x) or sin(y) to unity. It can also provide a 90° offset to convert the numerator or denominator to a cosine function. Stable offsets less than 90° may be introduced using a voltage-dividing series-resistor (nominally 3.6kΩ for 45°). V_r can also be used as the amplitude input voltage $U_1 - U_2$, or as a convenient control input to set $U_p = 10V$ for ambient temperatures below +60°C. This output is short-circuit protected and can provide up to 4mA total load current.

THE ERROR-TRAP AND GATE: GT

In some applications it may be useful to know that the output is severely in error due to a dynamic combination of inputs. For example, the tangent, cotangent, secant and cosecant all exhibit regions where the function increases sharply for small angular changes, and the output may easily saturate. Consider the case where (10V) tan (θ) is being generated. W is 10V for θ = 45°, and the theoretical output of 17.3V at θ = 60° cannot be achieved using ±15V supplies. Likewise, the output is invalid whenever the angle y is outside of a valid range (principally 0 to +180°), or when $U < 0$ or $U > |-V_s|$. Under such conditions the AD639 generates a HIGH output at pin 11 and simultaneously clamps the analog output to zero (in fact, to the voltage Z_2). Grounding GT disables the error trap.

The GT pin may also be used as an *input* to gate the function output. This is achieved by raising pin 11 to a voltage above +1.5V. Response time is typically 500ns for a logic drive of 0 to +2V, and the ON/OFF ratio is greater than 83dB when used as a continuous-wave sine converter with a single-sided ±1.8V triwave drive at frequencies up to 10kHz, or 63dB at 100kHz; the feedthrough is entirely capacitive, and is equivalent to 5pF between X1 or X2 and the op-amp summing node. Feedthrough can be minimized by using a balanced drive to X1 and X2.

Operation In Normal Modes

In *normal* modes, the Z-input establishes a feedback path around the output op-amp, by connecting Z1 to the output, W, and Z2 to the ground associated with the load circuit. For the highest accuracy Z1 can be used to sense the output at the load terminals. Similarly, zero-valued angle inputs and the angle common (pin 5) should be connected to the ground associated with the source circuitry.

SINE MODE

The AD639 can generate either (1) a low-distortion continuous sinewave from a repetitive triwave input or (2) a high-accuracy sine function for use in computational applications. In most cases, the choice of preset or externally-controlled amplitude will make little difference to distortion or accuracy, and both methods are used in this section. In all of the *normal* modes, the Z2 input can be used either to sum a further signal to the output (or introduce an optional output offset trim). The denominator is set to unity by making $y = 90°$, using the $+1.8V$ output. Figure 2 shows typical connections. The 10V preset is selected, using V_r as a control input to UP, and the ideal output is (10V)sin(x). In practice, five basic types of error arise:

1. *X-angle scaling error*: The amount by which the angle generated for each volt of X-input differs from 50°. In triwave-to-sinewave (CW) applications this introduces odd-order harmonic distortion, and is indistinguishable from an incorrect triwave amplitude.
2. *X-angle offset error*: The actual angle generated when $X = (X_1 - X_2) = 0$. In CW applications this introduces even-order harmonic distortion, as a non-zero mean in the triwave would.
3. *Amplitude scaling error*: The amount by which the peak-to-peak amplitude of the sinewave differs from the ideal value, U/sin(y). This error is usually critical only in computational applications. Errors associated with the Y-network also affect the amplitude in the sine mode.
4. *Output offset error*: The amount by which the *mean value* of the sinewave differs from zero (strictly, the voltage on Z2). This error is only important in computational applications. Note that the output may also be non-zero due to angular offset on the X-input. For example, the typical specified X-angle offset of 0.1° introduces an output error of 17.45mV when U/sin(y) = 10V, more than three times the specified mean offset component of 5mV.
5. *Law-conformance error*: The residual deviation between the output function and the ideal function when all of the above errors have been removed by trimming during manufacture or further external trimming, limiting the ultimate accuracy of the function.

Figure 3 shows the function when driven well beyond the specified angular range, using a differential X-input of ±18V peak. This also shows the AD639's ability to drive ±15V into a 600Ω load, with supplies of ±18V. Using an accurate data-acquisition system the output can be compared to a computer-generated sine function. When the first four types of errors are trimmed out, the peak error over the full input range is typically less than 0.5%. Over the central −90° to +90°, the peak law-conformance error is typically only 0.02%. Figure 4 shows the law conformance for four typical samples of AD639. The differential signal interfaces simplify the inclusion of optional offset correction to any of the variables.

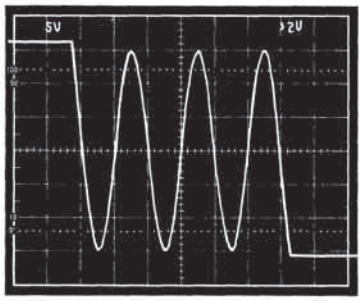


Figure 3. Output Function for Peak X-Input of ± 18V, with U = 15V, $R_L = 600\Omega$ ($\pm V_S = 18V$)

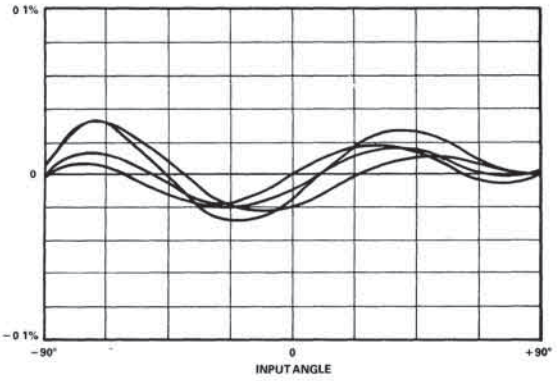


Figure 4. Residual Error Over Central 180° Using External Trimming

HARMONIC DISTORTION

The AD639 can generate continuous sinewaves of very low distortion using a linear, highly-symmetric triangle-wave of ±1.8V amplitude. Imperfections in the triwave will cause the following errors:

1. *Incorrect amplitude*: This causes odd-order distortion. Each 1% error (either too large or too small) generates 0.25% of HD3, 0.0833% of HD5 and a total harmonic distortion (THD) of 0.27% (−51.42dBs).
2. *Baseline offset*: This causes even-order distortion. Each millivolt of offset in a 1.8V triwave generates 0.037% of HD2, 0.0074% of HD4 and a THD of 0.038%, as well as a DC offset of 0.055% of the output amplitude.
3. *Time-asymmetry*: The run-up time, t_1, and run-down time, t_2, of the triwave may be unequal. This causes both odd- and even-order harmonics. Let the asymmetry in percent be $p = 100(t_1 - t_2)/(t_1 + t_2)$. The even-order terms are proportional to p; the odd-order terms increase as p^2. A 1% time-asymmetry generates 0.57% of HD2, 0.00625% of HD3, 0.043% of HD4 and 0.00167% of HD5, and a THD of −44dBs. There is no DC term.
4. *Amplitude-nonlinearity*: This can take on many forms, such as an exponential nonlinearity in the triwave, amplitude compression, and so on. Distortion can be calculated for various special cases. Fortunately, it is fairly easy to avoid these types of imperfections in the triwave generator using appropriate design methods.

When triwave errors are minimized, harmonic distortion can be as low as 0.01%. Figure 5 shows the output spectrum at 10kHz, with an output amplitude of 20V pk-pk and a load resistance of 10kΩ. An HP3325A synthesizer/function generator was used to produce the triwave. Distortion rises only slightly when using the minimum specified load of 2kΩ; in fact, the AD639 can drive loads down to 600Ω. At $\pm V_s = \pm 18V$, sine amplitudes of ±15V (10.6V rms, or 225mW of load power) can be generated, with typically 0.03% HD2 and HD3.

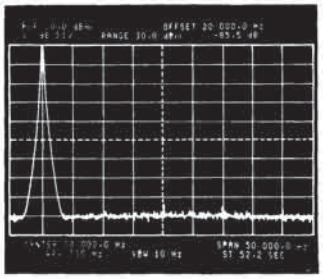


Figure 5. Spectrum of 10V Sine Output at 10kHz; HD2 = −88dBs, HD3 = −85.5dBs

COSINE MODE

The cosine function is generated by offsetting the sine by 90° using V_r. The X-input is connected to X2 and VR to X1; then

$$W = U \frac{\sin(90° - x)}{\sin(90° - 0)} = U \cos(x)$$

Connections for the cosine are shown in Figure 6; the amplitude in this case is determined externally, by way of illustration. The angular range now extends from −400° to +600°, with highest accuracy between 0° and +180°.

TANGENT AND COTANGENT MODES

The tangent function is provided by the connections shown in Figure 7. The angle voltage, corresponding to θ, is applied both to the numerator, set to the sine mode, and the denominator, set to the cosine of the same angle:

$$W = U \frac{\sin(\theta - 0)}{\sin(90° - \theta)} = U \frac{\sin(\theta)}{\cos(\theta)} = U \tan(\theta)$$

Most applications require accurate operation for angles up to nearly ±90° and accordingly U is preset to 1V (rather than 10V). Under these conditions, W = 1V when θ = 45° and 11.43V when θ = 85°. Using 15V supplies, the output op-amp will be unable to generate the tangent much beyond this point: at only 86° it would theoretically need to reach 14.3V. For an input exceeding 90° in either direction the denominator becomes negative, and the error trap is enabled. Figure 8 shows the function for inputs up to ±2.5V (±125°).

The errors associated with the sine mode, (see above) apply to the tangent mode also, but the total error in the tangent, cosecant, secant and cotangent modes (when the Y-input is also varied) are higher, since the Y network is not trimmed and the angular

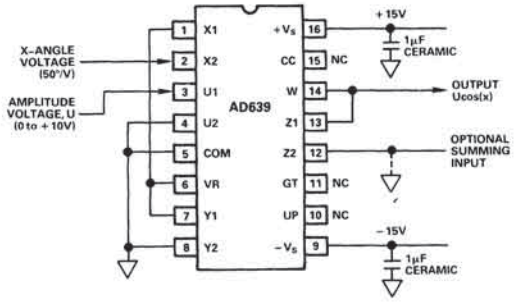


Figure 6. Connections for the Cosine Mode with External Amplitude Control

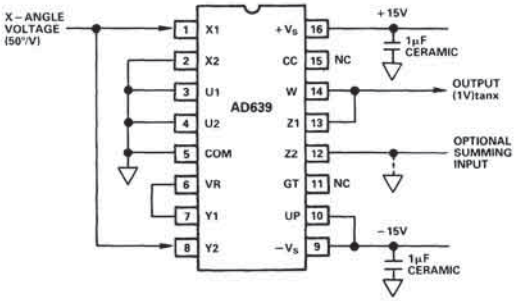


Figure 7. Connections for Tangent Mode with Amplitude Preset to 1V

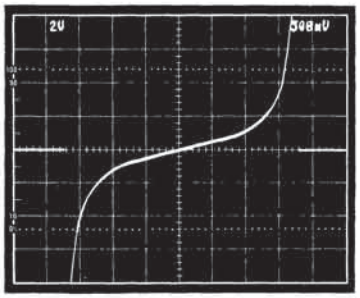


Figure 8. The Tangent Output for Angle Inputs Up to ±125° (Error Trap Activated Above 85°)

scaling and offset errors of this network are absorbed during trimming of the output in the sine mode.

The cotangent is generated by interchanging numerator and denominator. The principal range is now from 0 to +180°, and the output (1V)cot (θ) ranges from +11.43V at θ = 5°, through zero at θ = 90°, to −11.43V at θ = 175°.

SECANT AND COSECANT MODES

In secant and cosecant modes, the numerator is fixed to unity by connecting X1 to VR and X2 to analog common. For the secant, angle voltage A is connected to Y2 and Y1 is tied to VR; then

$$W = U\,\frac{\sin(90° - 0)}{\sin(90° - \theta)} = U\,\frac{1}{\cos(\theta)} = U \sec(\theta)$$

The principal range is $-90°$ to $+90°$. The most practical amplitude scaling is provided using the U-preset of 1V, when the output ranges from $+11.47$V at $\theta = -85°$ and $+85°$, to $+1$V at $\theta = 0$. The cosecant differs only slightly: the angle input is connected to Y1 and Y2 is connected to analog common, making the denominator sin (θ). The principal range is now 0 to $+180°$. When $U = 1$V the output is $+11.47$V at $\theta = +5°$ and $+175°$, and $+1$V at $\theta = 90°$.

OFFSET MODES

The versine, vers (θ) $= 1 - \cos(\theta)$, coversine, covers (θ) $= 1 - \sin(\theta)$, and exsecant, exsec (θ) $= 1 - \sec(\theta)$ involve the addition of a constant term to one of the normal trigonometric functions. These can be generated with the AD639 using the Z2 input to add a voltage to the output proportional to the amplitude of the basic function. In the versine and coversine modes this is simply the same voltage as applied to U1 (U2 grounded) to set up the amplitude of the sign-inverted cosine or sine function, respectively:

$$W = U - Uf(\theta) = U(1 - f(\theta))$$

In these two modes the output starts at zero and has a peak value of twice the amplitude voltage, U.

For the exsecant a *negative* voltage is added at Z2 and this same voltage is applied to U2 with U1 grounded; this satisfies the requirement that the sign of $U_1 - U_2$ be positive. (See comments on the Amplitude Control Inputs). The angle inputs are set up for the secant; the principal range is still $-90°$ to $+90°$, but the output is now zero when the input angle is zero.

OPERATION AT LOW SUPPLY VOLTAGES

The signal ranges at the angle interfaces are essentially independent of the supply voltages. In almost all cases, the primary limitation to the function's range will arise at the output, W, which can swing to within approximately 2V of either supply. For example, the X-input may have a peak value of ± 12V ($\pm 600°$) even when using ± 5V supplies.

Inverse Function Modes

The AD639 generates the inverse trigonometric functions by closing the feedback loop around the output op-amp through the *angle* inputs, rather than through the Z-interface, resulting in a nonlinear feedback system. To understand this, note first that the *general* transfer function (with UP disabled) is

$$W = A_{OL}\left[(U_1 - U_2)\,\frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)} - (Z_1 - Z_2)\right]$$

where A_{OL} is the open-loop gain of the output op-amp (typically 85dB). Provided that the overall feedback remains negative, the loop can be closed in many ways, so as to force the quantity inside the brackets to a null, when

$$\frac{\sin(x_1 - x_2)}{\sin(y_1 - y_2)} = \frac{(Z_1 - Z_2)}{(U_1 - U_2)}$$

whatever combinations of variables are used to set up the feedback path. In particular, when the *angle* inputs are used the system will have one of the *normal* functions in the feedback path. The input to this system is now the *ratio* (Z/U), and the output is a voltage corresponding to the angle generated by the *inverse* of the function in the feedback path.

Since all of the normal functions are periodic, and the maximum value of the op-amp output can be equivalent to angles as large as $\pm 650°$, the closed-loop system could arrive at false "solutions" to the above equation, that is, at angles outside of the principal range. Also, the feedback can become positive in the wrong angular range, causing latch-up. Hence, it is essential to limit the magnitude of the feedback voltage. Ideally, this is done using precise active clamps, but the saturated value of the output at given supply voltages, in combination with a simple resistive divider to the angle inputs, is usually sufficient to limit operation to the principal range. The voltage at the angle inputs will be accurate, but the op-amp output will in general have inaccurate scaling and may show large offsets, due to the bias currents at the angle inputs. The error-trap should be disabled in the inverse modes by grounding GT.

ARCTANGENT MODE

The arctangent is the most useful of the inverse modes. With the connections shown in Figure 9 the loop solves the equation

$$\frac{\sin(0 - \theta)}{\sin(90° - \theta)} = -\tan(\theta) = \frac{(Z_1 - Z_2)}{(U_1 - U_2)}$$

where θ is the angle corresponding to voltage A, scaled by 50°/V. It follows that

$$\theta = \tan^{-1}\frac{(Z_2 - Z_1)}{(U_1 - U_2)}$$

The reversal of Z_1 and Z_2 in the numerator is due to the negative sign in the tangent function. The numerator may be either positive or negative, and the connections can be interchanged to alter the overall sign of the function. The denominator must be positive, but U1 and U2 may be interchanged to accept a negative input voltage. The ability of the AD639 to form the ratio of two

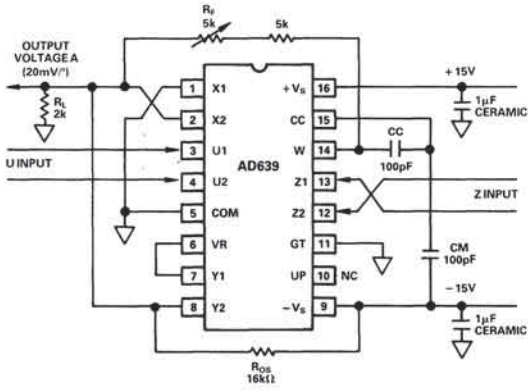


Figure 9. Connections for the General Arctangent Mode

variables prior to the arctangent operation is very useful in many applications, for example, in real-time Cartesian-to-polar conversion (see Applications section). The denominator can also be preset to 1V or 10V using the UP input; when U = 1V, the angle a is simply the arctangent of the voltage value of $Z_2 - Z_1$. Figure 10 shows an X-Y plot of the output for Z = −10V to +10V (horizontal axis of photograph) with four values of U (0.3V, 1V, 3V, 10V).

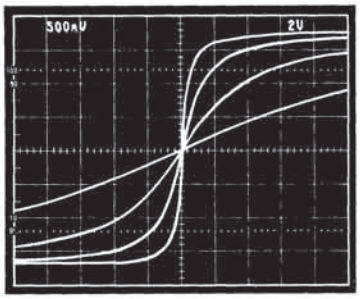


Figure 10. The Arctangent Output for Z = ±10V and U = 0.3V, 1V, 3V and 10V

Range-Limiting and Loading

Resistor R_f in Figure 9 forms a divider with the parallel sum of the input resistance at X2 and Y2 and the load resistance, shown here as 2kΩ, which prevents the output angle voltage A from exceeding ±1.7V (θ = ±85°), using ±15V supplies. This voltage is not *directly* affected by the load resistance (that is, the output behaves as a low-impedance node) but the angular range limits are. Consequently, the nominal value of R_f should be calculated for specific values of load resistance, angular range and supply voltages, and a trim range of about ±10% included to set up the angle limits correctly. R_{os} is needed to compensate the input bias currents and thus equalize the clipping limits; it does not cause an offset in θ. The direct output at pin 14 is also the arctangent but with imprecise scaling. Although this can be trimmed by R_f there will also be a supply-dependent offset due to R_{os}. For these reasons, the direct output should not be used in this mode.

HF Compensation

The output op-amp is internally compensated to be stable in all the normal modes when feedback is via the unity-gain difference amplifier associated with the Z-interface. The dominant pole is determined by the 30kΩ resistor and on-chip 3.5pF capacitor (see Figure 1) for a closed-loop bandwidth of 1.5MHz. In the arc-tangent mode, however, the gain of the feedback path is much greater than unity for practical angle values and is theoretically unbounded. For example, if the forward path is set up to generate (1V)tan(θ), the incremental gain near θ = 0 is slightly less than unity (since a 20mV change in voltage A causes a change of (1V)tan(1°) or 17.5mV in output W) but at θ = 85° the gain is 115. While the resistive divider used to limit the angle voltage A will lower the loop gain, it can still exceed unity. The capacitors C_c and C_m in Figure 9 provide the HF compensation required for operation up to ±85°, with all values of U.

ARCSINE AND ARCCOSINE MODES

The basic principles for the arcsine and arccosine are similar to those described for the arctangent. As before, the argument of the function is the ratio (−Z/U), where U may be preset to 1V or 10V, the loop gain must be negative over the principal angular range of the output, and the feedback voltage must be limited to ensure that this range is not exceeded. The loop stability is easier to ensure, since the peak gain is bounded. With U = 10V the maximum incremental gain of the forward path (at 0° for the sine and +90° for the cosine) is 8.75 and the peak loop gain is much less than this because of the attenuation used to limit the angular range. Thus relatively little additional HF compensation is required.

Connections for the arcsine are similar to the arctangent (Figure 9) except that Y2 is grounded, and C_c and C_m can be reduced or even omitted. R_f is adjusted for a peak angular range of ±90° at the (attenuated) output; if too high, the function will still be correct, but the maximum angle will be less than 90°; if too low, the function will exhibit hysteresis near the peak output. Adjustments will be needed for other values of load resistance and supply voltages. Note that the general limitation on the amplitude input ($U <= |-V_s|$) must be observed. Figure 11 shows an X-Y plot of the arcsine output for Z = −10V to +10V (horizontal axis of photograph) with three values of U (2V, 5V and 10V). The arcsine can be inverted by reversing the Z-interface.

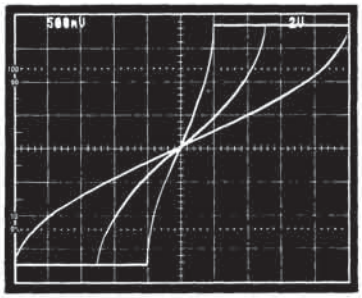


Figure 11. The Arcsine Output for Z = ±10V and U = 2V, 5V and 10V

For the arccosine, use the arcsine connections with X1 tied to V_r and insert a small-signal diode in series with R_f, having its cathode on the angle-interface side. This allows the output to move only in a positive direction. Z1 now becomes the positive numerator input, and the principal range is from 0° (when Z/U = −1) to +180°. The function is similar in appearance to the arcsine, except for the +90° output pedestal and the reversal of phase along the horizontal axis. Note that

$$\cos^{-1}(Z/U) = 90° - \sin^{-1}(Z/U) = 90° + \sin^{-1}(-Z/U).$$

To generate the negative arccosine, reverse the X- and Z-interfaces and the polarity of the diode. The output now runs from −180° for an input of $Z = (Z_1 - Z_2) = -10V$ (with U = 10V) to 0° at Z = +10V.

It is strongly recommended that X-Y oscilloscope methods are used to investigate functional behavior during the development of any of these modes of operation: time-domain displays can easily become confusing.

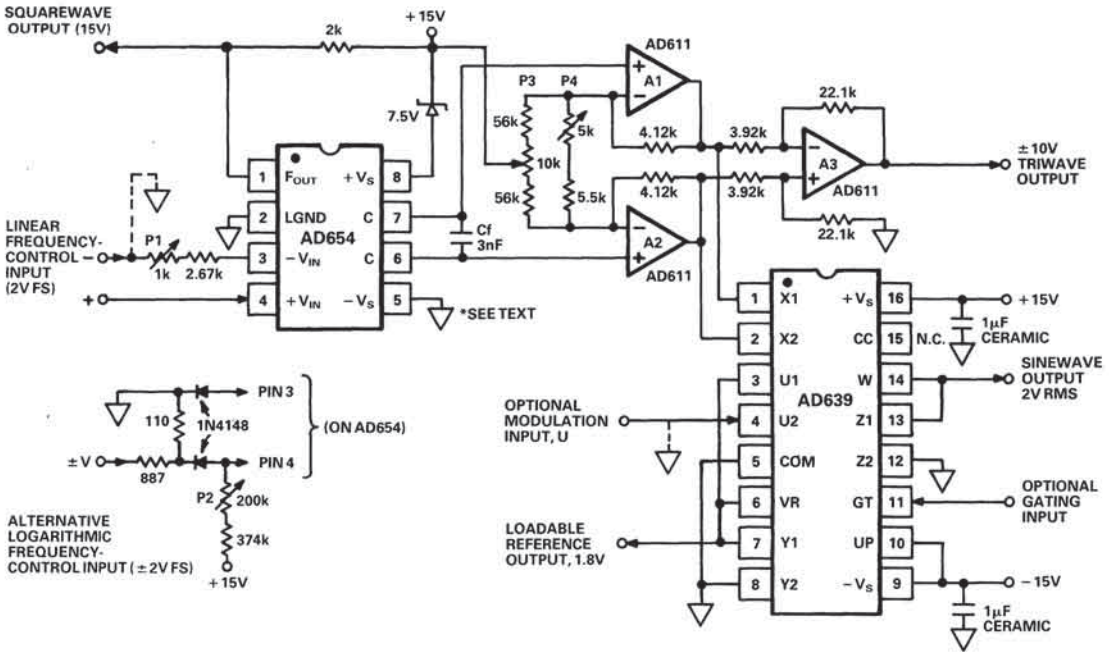


Figure 12. General-Purpose Function Generator

Applications

WIDE-RANGE WAVEFORM GENERATOR

Figure 12 shows an inexpensive signal generator, providing voltage control of frequency from 20Hz to 20kHz and a pre-set sine amplitude of 2.8V (within 0.1dB of 2V rms). This output may be further modulated by an input of up to ±2.8V to U2, or gated off by an input of +1.5V or more to GT; Figure 13 shows the gated response. If required, a further input can be summed into Z2. The sine output can be set to 10V amplitude by connecting UP to VR and grounding U1.

An AD654 is used to generate the triwave which appears across the timing capacitor C_f, and is buffered, amplified and level-shifted by A1 and A2. Using a spectrum analyzer, P3 and P4 are adjusted to minimize even- and odd-harmonic distortion, respectively. The triwave linearity is not good enough to realize the inherent capabilities of the AD639, but total harmonic distortion is in the −50dB to −60dB range. A3 provides further gain for a ±10V triwave output. The square-wave output is taken directly from the AD654 and is unbuffered. It swings between ground and +15V; if pins 2 and 5 of the AD654 are connected to −15V, this output is 30V pk-pk.

The frequency scaling with the linear input (shown) is 10kHz/V, calibrated using P1. The frequency can be controlled manually, using a potentiometer and the V_r output of the AD639. P1 has sufficient trim range to provide a full-scale frequency of 20kHz with the 1.8V peak input. The alternative input scheme provides a "log-sweep" response with an approximate scaling of 10^V kHZ (when V is in volts). The range is now from about 10Hz to 100kHz; the frequency should be set to 1kHz with V=0, using P2. The frequency is now sensitive to variations in both temperature and the +15V supply, but stability will be adequate for many applications.

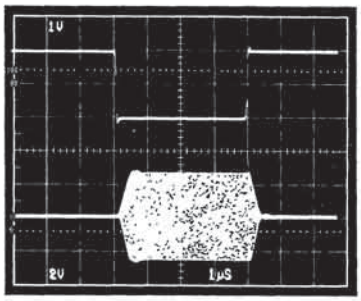


Figure 13. Gated Output. Top Trace: 0 to +2V Gate Input. Bottom Trace: 2V rms Gated Sine Output

Frequency Multiplication

Because of the exceptionally wide angular range of the numerator function of the AD639, it is possible to generate sinewave outputs with 2, 3, 4 or 5 times the triwave frequency using the cosine mode for even multiples or the sine mode for odd multiples.[2] For example, to multiply the output frequency by 3, use the sine function with the X-input driven to ±5.4V (±270°). Distortion remains low; all harmonics are typically under −50dBs, even for the frequency-quintupling mode.

[2]For full details see "A Remarkable Monolithic Microsystem Generates Trigonometric Functions," Barrie Gilbert, *Industrial Electronics Equipment Design*, September 1984, pp. 19-24. Reprints available.

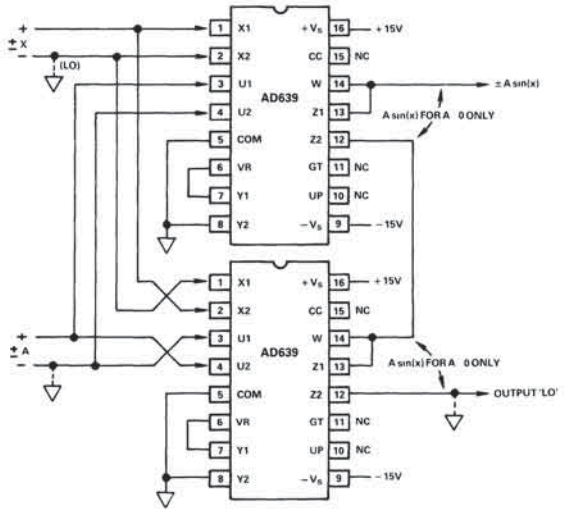


Figure 14. Four-Quadrant Sine Multiplier; for Cosine, Interchange X1 and X2 and Connect Angle 'Lo' Input to VR

FOUR-QUADRANT SINE/COSINE MULTIPLICATION

In synchro applications it is often necessary to multiply an AC sinusoidal 'carrier' by a further sine 'modulation' function. This can be achieved in two ways; the first is suitable only when there is a large ratio between the carrier frequency and the modulation frequency. Using a single AD639, the carrier input Asin(ωt) is applied to U2, and a DC bias voltage established on U1 (which can be provided by a series resistor connected to $+V_s$). The modulation input, x, is applied to angle inputs connected for $-\sin(x)$. The output is then $W = -\sin(x)(U_1 - A\sin(\omega t))$. Using AC-coupling to the load, the voltage Asin(x)sin(ωt) results. Since the peak value of W is $(U_1 + A)$, a maximum of about 6V amplitude can be achieved before output saturation. A further limitation of this approach is that the AC-coupling may allow excessive transmission of the sine modulation function. However, with typical values of 400Hz for the carrier and 10Hz for the upper modulation frequency, this simple approach is practical. Cosine modulation is similarly achieved.

An alternative method is DC-coupled and thus imposes no frequency-ratio limitations; it also allows an input/output amplitude of up to 12V. Two AD639s are used (Figure 14), the second having both the X- and U-interfaces phase-inverted relative to the first, and the two outputs are summed. The figure shows a general bipolar input, A, applied to the U-inputs. The first device generates Asin(x) when A is positive and zero when A is negative. The second device generates $-A\sin(x)$ (actually $A\sin(-x)$) when A is negative and zero when A is positive. The instantaneous sum of the two half-sines is Asin(x). The switching speed of the U-interface is adequate to handle a sinusoidal input $A = (10V)\sin(\omega t)$ at frequencies up to at least 1kHz, without significant crossover distortion. In synchro applications errors as small as 5 arc-minutes can be achieved.

Polar-to-Cartesian Conversion

Using a pair of AD639s connected as shown in Figure 14, and a second pair connected similarly for the cosine function, a vector of magnitude A and angle x can be resolved into its orthogonal components Asin(x) and Acos(x), with unrestricted operation in all quadrants and very high accuracy.

Cartesian-to-Polar Conversion

A point Z,U in a plane can be converted to a magnitude component, A, and an angle component, θ. A suitable vector summation circuit can be found in the AD637 data sheet. The AD639 in the arctangent mode can provide the angle output $\theta = \tan^{-1}(Z/U)$. If U is bipolar, an absolute-value circuit using an AD630 should be added.

9

Sine/Cosine (Quadrature) Oscillators

Quadrature oscillators generate a pair of sinusoudal outputs displaced by 90°, and invariably are based on a "state-variable" loop consisting of two integrators and a sign-inverter. Practical difficulties in this approach are (1) considerable additional circuitry is required to control the amplitude of the oscillation; (2) a trade-off arises between the settling-time of this control circuitry and the distortion level, particularly troublesome at low frequencies; (3) the amplitude balance of the two outputs is dependent on the matching of two time-constants; (4) two tracking analog multipliers or multiplying DACs are needed if the frequency is to be programmable.

These problems are avoided using a function-shaping technique based on a triwave oscillator, which requires only one time-constant, and whose frequency can thus be more easily controlled. The need for an amplitude control system is eliminated using the scheme shown in Figure 15. The two outputs have accurate amplitudes of 10V (without the need for an external reference source) or can be individually controlled by external voltages, without any effect on frequency. Variable-amplitude sine and cosine outputs can be added (using the Z-input discussed earlier) to provide continuously-variable phase-control of the output.

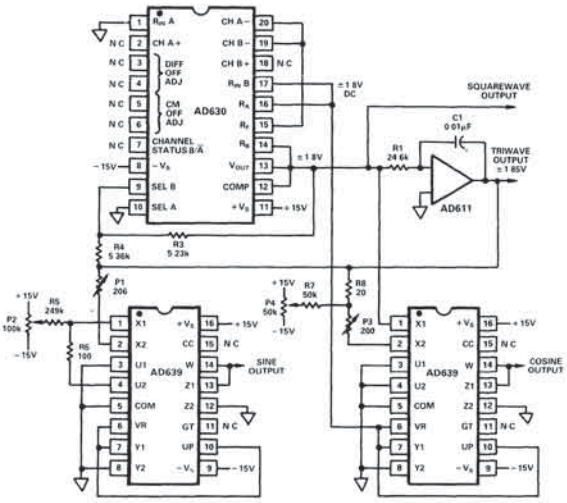


Figure 15. Quadrature Oscillator

The triwave oscillator comprises an AD630, which alternates the sign of the 1.8V reference from one of the AD639s to generate a square-wave output of ±1.8V amplitude, and an integrator formed by R1, C1 and the op-amp, which generates the triwave. The amplitude of the triwave is determined by the ratio of R3 and R4, and is nominally ±1.845V, 2.5% higher than needed at the inputs of the AD639s, providing the adjustment range needed to minimize distortion. In many applications, all adjustments can be eliminated; to do this, make R3 = R4 = 5kΩ, omit P2, P4, R5 and R7 and replace P1, P3, R6, and R8 with short circuits. The frequency is nominally $1/4C_1R_1$, and is 1kHz with the component values shown. A variety of methods may be used to provide external control of frequency, including the use of another AD630 in series with R1, or the use of a multiplying DAC.

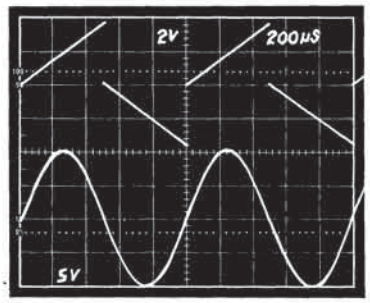


Figure 16. Top Waveform: Difference Voltage Between Triwave and Squarewave. Bottom Waveform: Resulting Output

The sine output is generated using the triwave directly. P1 and P2 should be adjusted using a spectrum analyzer for minimum odd-order and even-order harmonics, respectively. The cosine output is generated by using the *difference* between the triwave and the square-wave, shown in the upper waveform in Figure 16. This composite voltage first generates a sine-function over the range 0 to +180°, then over the range 0 to −180°, to produce the function shown in the lower waveform, which can be seen to be 90° out of phase with the triwave. The complete set of waveforms available from this generator are shown in Figure 17.

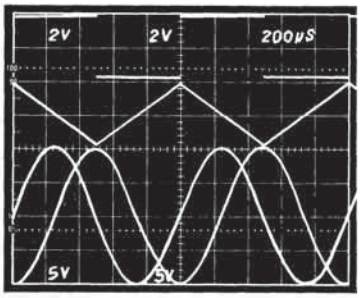


Figure 17. Timing Relationships Between All Outputs of the Quadrature Oscillator

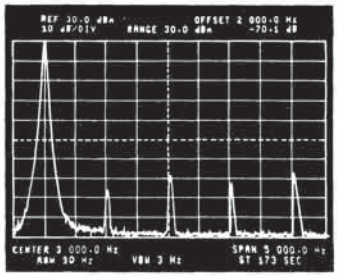


Figure 18. Spectrum of Cosine Output at 1kHz

P3 and P4 are adjusted for minimum odd-order and even-order cosine harmonics, respectively; Figure 18 shows the cosine spectrum for a well-adjusted circuit.

Due to the finite transition time back to the baseline in the drive voltage to the cosine generator, a brief spike occurs at the zero-crossing of this output. The frequency components will be beyond the bandwidth of the output amplifier in the AD639, and the energy contained in these spikes will not generally be troublesome. They may be further reduced, if necessary, by adding a capacitor between pins 14 and 15, to roll off the AD639 output response.

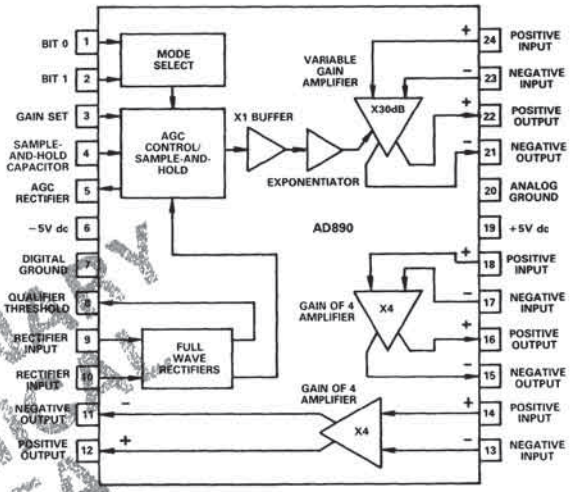
Precision, Wideband Channel Processing Element

AD890

FEATURES

- An 80MHz Bandwidth Permitting a 50Mb/s Data Transfer Rate
- A Variable Gain Amplifier with 30dB max Gain and 40dB Control Range
- Two Gain of 4 RF Buffers
- 200Ω Differential Load Drive Capability
- A Pair of Precision Rectifiers
- AGC Level and Threshold Outputs
- An Averaging, High Gain Sample-and-Hold for Accurate AGC Operation
- Typical Gain Drift in Hold Mode: 0.2dB/ms
- Gains Trimmed and Temperature Compensated
- AGC Operation Independent of AGC Level
- Symmetrical AGC Attack/Decay Times
- 1μs AGC Attack/Decay Times Using a 1000pF External Capacitor
- Suitable for Use as an Accurate Video Programmable Gain Amplifier
- Dynamic Clamp Ensures Fast Recovery After Write to Read Transients
- AGC RF Output Level is Internally Preset

AD890 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD890 is primarily intended for high-performance disk subsystem use and as such it is configured around the classic read channel processing block diagram. It is intended to be connected between the head preamplifier and the qualification circuitry required for digital data recovery. When used with the AD891 rigid disk data qualifier, data transfer rates in excess of 50Mb/s can be processed.

A temperature-compensated AGC loop, with an exponential transfer characteristic, permits optimal settling and allows for predictable performance in the classic single integrator control loop configuration. Fast acquisition and low droop while in the hold mode allow for AGC operation to be performed within the sector header without compromising channel behavior when reading data.

The AD890 processing element has the flexibility to perform both continuous and sampled AGC functions; it is also ideal for embedded, dedicated, or mixed servo applications. Two user-defined filter/equalizer stages may be employed, thus allowing maximum design flexibility. This greatly simplifies the design of the overall channel characteristics. Using the AD890, the designer no longer needs to resort to passive techniques to isolate network functions; this avoids problems of signal loss and interaction.

Two low-offset, 100MHz full-wave rectifiers provide the capability to track a 1V peak signal. The rectifier generating the "Qualifier Threshold" output may be used for creating a data qualification level. A second rectifier is used to drive the sample-and-hold circuitry.

The 80MHz bandwidth of the AD890 ensures good phase linearity up to 50MHz. Thus, data transfer rates in excess of 50Mb/s can be supported with good error rates and predictable channel behavior.

The AD890 is available in both a 24-pin, slim-line cerdip package and in a 28-pin PLCC package and is specified to operate over the 0 to 70°C commercial temperature range.

PRODUCT HIGHLIGHTS

1. A highly predictable gain control function allows the user to perform a very accurate preset operation and facilitates D/A converter control capability.
2. Two low-offset, 100MHz full-wave rectifiers are provided.
3. An internal clamping circuit ensures short recovery times after read/write switching of the external head chip.
4. An 80MHz bandwidth ensures good phase linearity.
5. A 0.2dB per ms droop in gain during AGC hold mode.
6. All RF gain stages offer calibrated temperature-stable gains.

9

SPECIFICATIONS (@ +25°C and ±5V dc, unless otherwise noted)

Model	Conditions	AD890J Min	AD890J Typ	AD890J Max	Units
VARIABLE GAIN AMPLIFIER					
Maximum Gain[1]		**29.5**	30.0	**30.5**	dB
±3dB Bandwidth	Up to 26dB Gain Reduction	100			MHz
Input Voltage Noise	0dB Gain Reduction, f = 1kHz		5		nV/√Hz
Input Signal Range	Recommended p-p Differential	10		200	mV
Input Resistance			12		kΩ
Output Impedance			5		Ω
Harmonic Distortion	0dB Gain Reduction		0.15		%
	26dB Gain Reduction		1.5		%
Output dc Level			3.5		V
INPUT CLAMP[2]					
Turn-On Time			30		ns
Turn-Off Time			200		ns
Input Signal Attenuation			45		dB
On-State Input Impedance	Differential		14		Ω
GAIN OF 4 BUFFER					
Nominal Gain		**12.50**	12.75	**13.00**	dB
Gain Variation	T_{min} to T_{max}		±0.25		dB
±3dB Bandwidth		160			MHz
Input Voltage Noise[3]	f = 1kHz		7		nV/√Hz
Input Resistance		100			kΩ
Input Common-Mode Range		−1.5		+1.5	V
Output Resistance			10		Ω
Harmonic Distortion	300mV Peak Output, 200Ω Load		0.20		%
Output Signal Level	Recommended p-p Differential		1.3		V
Output dc Level			2.5		V
FULL WAVE RECTIFIER					
Input Signal Level	p-p Differential	0.3		3	V
−3dB Bandwidth	100mV @ 1V Peak Input	100			MHz
dc Offset[4]			10	**±20**	mV
AGC CONTROL SECTION					
Attack Time	26dB Gain Step – 1000pF C_{SAMPLE}		1.0		µs
	26dB Gain Step – < 50pF C_{SAMPLE}		120		ns
Hold Time	1dB Gain Change – 1000pF C_{SAMPLE}		10		ms
AGC Control Range		**36**	40		dB
AGC Control Sensitivity	Per 20mV Input		1		dB
AGC Control Linearity	26dB AGC Range			**±0.25**	dB
Set Level Input Range	For Specified Accuracy	**0**		**800**	mV
	Nondestructive Input Range	−0.3		V_{CC}	V
MODE CONTROL SECTION					
TTL Compatible					
V_{IH}		2.0			V
V_{IL}				0.8	V
I_{IH}				100	nA
I_{IL}				2.0	µA
Mode Switching Times				50	ns
POWER SUPPLY REQUIREMENTS					
Rated Performance			±5.0		V
Operating Range		**±4.6**		**±6.5**	V
Quiescent Current	T_{min} to T_{max}				
V_{CC}		44	60	76	mA
V_{EE}		18	28	40	mA

NOTES

[1]Gain calibrated in gain set mode with 0 volts applied to the Gain Set Pin

[2]Clamp operation is specified with a source impedance of 200Ω in series with 0.1µF

[3]Over the full 100MHz bandwidth of the AD890, the worst-case rms signal-to-noise ratio is 40dB or better with a 40dB AGC range.

[4]Measured using a 4kΩ resistor connected between the Qualifier Threshold Pin and V_{11}.

Specifications subject to change without notice.

All min and max specifications are guaranteed. Specifications in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels.

Logic Assignments	Bit 0	Bit 1
AGC Acquire	0	0
AGC Hold	0	1
Gain Set	1	0
Input Clamp	1	1

ORDERING GUIDE

Model	Package	Package Options*
AD890JQ	24-Pin Cerdip	Q-24
AD890JP	28-Pin PLCC	P-28A

*See Section 16 for package outline information.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . ±7.5V
RF Gain Stage Differential Input Voltage . . . . . ±5.6V
Storage Temperature Range
AD890JP, AD890JQ . . . . . −65°C to +150°C
Operating Temperature Range[1]
AD890JP, AD890JQ . . . . . 0 to +70°C
Lead Temperature Range (Soldering 60sec) . . . . . +300°C

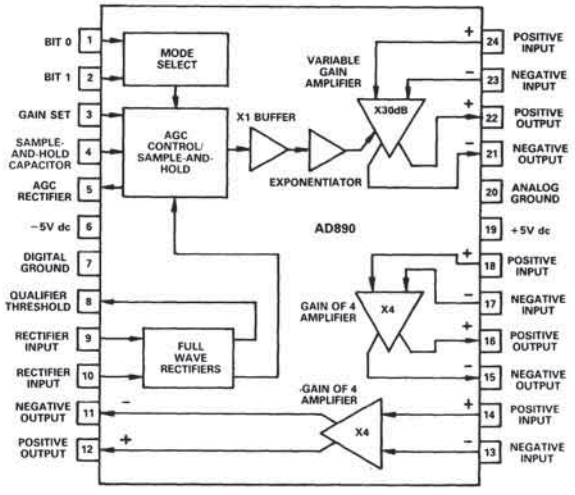
NOTE
[1]28-pin PLCC package: $\theta J_A = 100°C/W$;
24-pin cerdip package: $\theta J_A = 80°C/W$.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

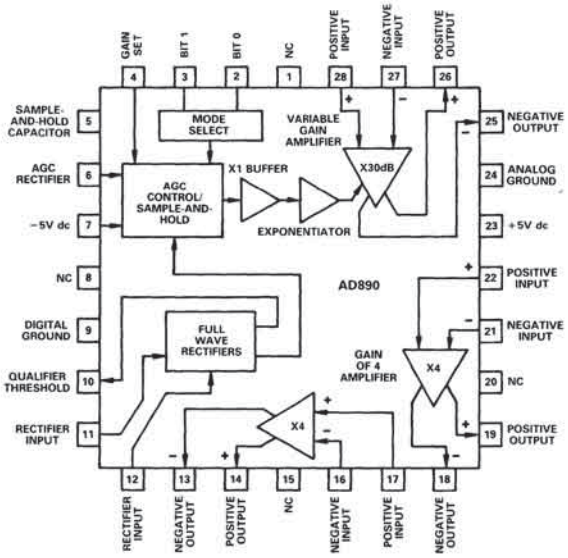
CONNECTION DIAGRAMS

9

24-Pin Cerdip Package



28-Pin PLCC Package



NC = NO CONNECT

Applying the AD890

GENERAL LAYOUT REQUIREMENTS

Almost 60dB of total gain is available at 100MHz. Care must be taken to ensure good RF practice in the PC layout to avoid oscillations in the 150MHz-350MHz region. A parallel combination of 0.1μF and 0.01μF ceramic bypass capacitors should be used as close to the supply pins as possible.

Additionally, a single pole RC filter applied at the input of each stage, with a cut off in the region of 100MHz-150MHz, will help avoid oscillation problems. As a general rule, keep the connections to interstage components as short as possible; it is also recommended that any low pass filtering function which may be required by the system be performed between the VGA stage and the first X4 buffer amplifier. A ground plane should be used to surround any interstage components wherever possible. If these simple rules are followed, stable operation should be assured.

BIASING THE RF GAIN STAGES

The VGA Stage

The 30dB variable gain stage is biased at a potential of one diode drop above analog ground. No additional dc bias is required, but ac coupling is necessary. The bias voltage is maintained during normal operation and during operation of the clamp. In order for the clamp to operate correctly with an emitter follower driven input, 50Ω-100Ω resistors should be placed in series with the input coupling capacitors. These resistors can be used in conjunction with a 5.1pF shunt capacitor to limit the input bandwidth to 150MHz. In the case of an open collector driven input with resistive termination, no additional series resistors are required.

The differential outputs have a nominal dc value of 1.5V less than the positive supply. Internal 1300Ω resistors provide bias current to the output emitter followers which operate with 2.7mA nominal current. Output drive can be increased by an additional 2.5mA by paralleling external resistors to either the analog ground or the negative power supply. However, caution should be exercised in order to avoid causing excess dissipation for the package. The recommended output level for the VGA is 300mV p-p differential into 200Ω loads.

The X4 Buffers

The inputs of these stages have no committed dc biasing, and an input bias current path must be provided. This path can normally be supplied via shunt resistors to analog ground which are generally part of the interstage filter termination networks. The inputs can be biased successfully within ±1.5V of analog ground.

Output drive can be increased in a similar manner to that described for the VGA stage. The nominal dc output level is 2.5V with the internal 500Ω load resistors connected to analog ground which provides a nominal standing current of 5mA to the output emitter followers. This current can be increased by up to an additional 5mA by paralleling external resistors to either analog ground or the negative power supply. As before, precautions to limit excessive overall power dissipation apply when steps are taken to increase the output drive capability.

OPERATING THE FULL WAVE RECTIFIERS

The full wave rectifiers consist of two nearly identical stages. Full wave rectification is performed in each stage using two transistors whose emitters are connected together. The inputs to the two full wave rectifiers are biased at one diode drop above analog ground; therefore, ac coupling is recommended. The full wave rectifier outputs – "AGC Rectifier" and "Qualifier Threshold" – are connected directly to these commoned emitters. Thus, the normal output voltage with zero input signal applied is close to analog ground. The "AGC Rectifier" pin allows access to the output of the rectifier which drives the AGC sample-and-hold section of the AD890. The "Qualifier Threshold" pin allows access to the output of the threshold rectifier.

The AGC rectifier has an internal 2kΩ resistive pull-down connected between analog ground and the negative power supply pin. The threshold line has no built in pull-down, in order to allow for a peak hold capability during thresholding. If a well controlled rectifier offset is required, an external 4kΩ pull-down resistor at the "Qualifier Threshold" pin is recommended and will produce a nominal 10mV offset.

THE AGC SAMPLE-AND-HOLD

The AGC sample-and-hold section performs averaging of the input waveform to set the RF average output level to 200mV single ended, or 330mV peak for a sinusoidal signal. Thus, without a peak hold capacitor at the "AGC Rectifier" pin, accurate AGC operation only occurs with sinusoidal input signals. An approximate 2mA pull-down current is permanently present at the "AGC Rectifier" pin, and a capacitor may be added here to provide a degree of peak hold for AGC operation within non-sinusoidal fields. A capacitance value of less than 0.03μF or less per μs of transition spacing is recommended. The addition of the capacitor alters the symmetry of the attack and decay rates of the rectifier, which is otherwise symmetric in operation. In order to ensure that the overall AGC response is the same for both high-to-low and low-to-high input level steps, it is necessary to make the rectifier attack and decay times at least a factor of two less than the AGC response time.

The AGC acquire time is approximately 1μs per 1000pF of hold capacitor. A low leakage variety of hold capacitor, such as a silver mica, is necessary to ensure low droop rates. The "Gain Set" pin should be tied to analog ground if not used, in order to prevent excessive leakage which would otherwise affect the hold performance.

The AGC control potential is present at the "Sample-and-Hold Capacitor" pin. If control over open-loop gain is desired, based on AGC control potentials obtained during trial AGC operations, a FET input op amp should be used to buffer this node in order to avoid disturbing the hold operation.

USING THE AD890 AS A PROGRAMMABLE GAIN AMPLIFIER

The AD890 is ideally suited for use as an accurate video programmable gain amplifier. If the X4 buffers are utilized with the variable gain amplifier, nearly 60dB of total gain is available at frequencies up to 100MHz. The VGA gain and exponentiator scale factors are trimmed with respect to dc control potentials applied to the "Gain Set" pin. In this mode of operation (see Logic Assignments for bit pattern to be applied to the "Bit 0" and "Bit 1" pins), a 0V dc potential applied to the "Gain Set" pin will produce a nominal VGA gain of 30dB. With an additional 12.75dB from each X4 buffer, total nominal gain is 55dB. Each 20mV increment of voltage applied will produce a 1dB reduction in gain. A simple equation can be used to calculate the nominal gain of VGA in this mode:

$$\text{VGA Gain (dB)} = (30 - V_{\text{GAIN SET}} \times 50)$$

where $V_{\text{GAIN SET}}$ is in volts.

OPERATION WITH +5V, +12V SUPPLIES

Operation with +5V (±0.25V) and +12V (±1.2V) supplies is readily achieved. Figure 1 shows the AD890 configured for +5V, +12V operation. The analog and digital grounds must be connected to the +5V line or to an available center tap of the +12V supply. Thus connected, a current of approximately 30mA will flow in this line under normal operation. The input clamping action occurs with respect to this line, increasing its current by an additional 12mA or so.

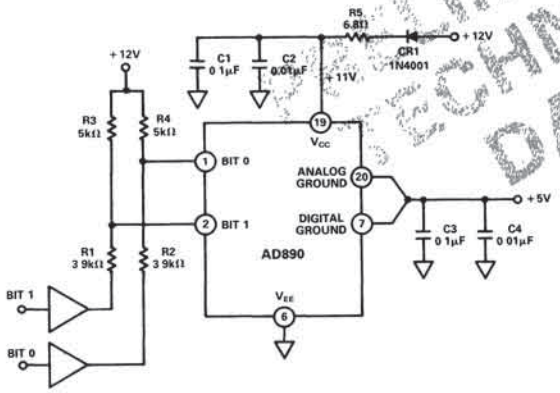


Figure 1. AD890 Connection for +5V, +12V Operation

Both the +5V and +12V supplies should be RF bypassed to ground with at least two capacitors: values of 0.1µF and 0.01µF are recommended. In addition, some higher level of decoupling capacitance such as 3.3µF value may be desirable. Next, insert a series-connected 6.8Ω 1/4W resistor and 100mA diode in series with the +12V supply. This helps to reduce overdissipation in the chip.

Power supply decoupling should occur on the circuit side of the resistor-diode network. A second diode can be substituted for the 6.8Ω resistor if the voltage difference between the two supplies is greater than 5.6 volts.

Finally, mode control is achieved by using open collector drivers and resistors as shown; 5.1V Zener diodes can be substituted for resistors R1 and R2. Internal diode clamping in the AD890 permits this mode of operation.

The mode switching times will be affected by resistor values chosen; this is due to the RC time constants formed by the resistors in conjunction with the input capacitance of the chip package.

INTEGRATING WITH THE AD891 RIGID DISK DRIVE DATA QUALIFIER

Figure 2 shows a typical application using the AD890 and AD891 connected together to create a 30MHz channel (cerdip connections shown). This circuit includes a 5-pole 30MHz Gaussian-to-6dB transitional filter plus a second-order RLC time domain equalizer. A typical second-order, fully differential, passive delay-line differentiator interface for the AD891 is also included. (For a more detailed description of the delay-line differentiator, see the AD891 data sheet.) The analog and digital grounds should be connected at the power supply common.

PRELIMINARY TECHNICAL DATA

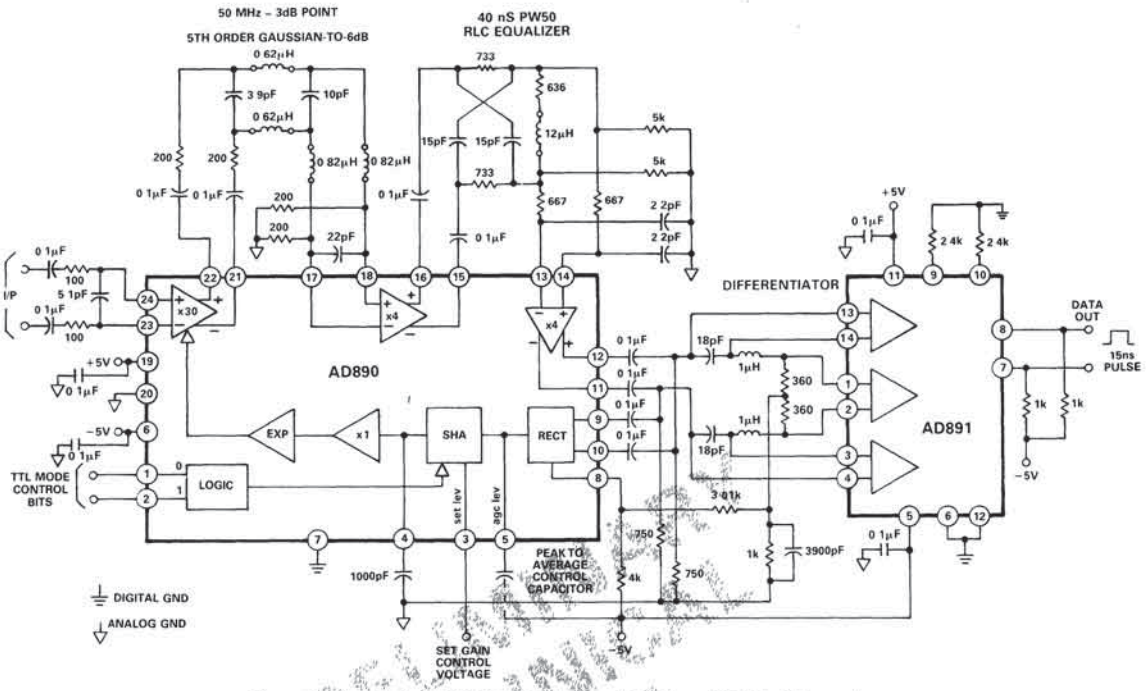


Figure 2. Typical AD890/AD891 Connection for a 30MHz Channel

USING EQUALIZERS WITH THE AD890

The AD890 is ideal for applications where equalization is employed. The X4 buffer output drivers are designed to operate into 200Ω loads, making tapped delay-line designs easy. Sum and differencing of different tap weights can be achieved by simple resistive dividers.

As an alternative, a simple RLC network can be implemented to provide a low-cost, fully differential alternative to the three-tap, tapped delay-line equalizer which often is used for pulse slimming. Essentially, the equalizer shown in Figure 3 consists of an RC lattice, which provides the magnitude characteristic, together with an LR shunt section which acts to define the overall passband group delay and the ratio of minimum to maximum gains within the passband.

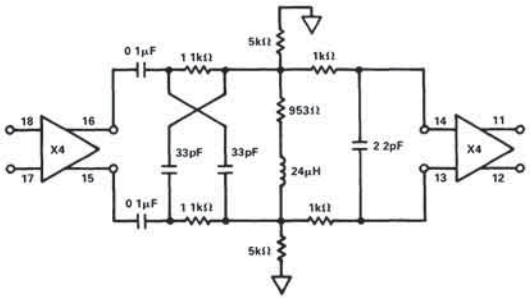


Figure 3. RLC Equalizer

The network shown approximates a function of the form:

$$F(\omega\tau) = 1 - k \cos \omega\tau, \text{ where } k = 0.6, \text{ and } \tau = 36\text{ns}.$$

The circuit is optimized for a 120ns transition PW5O. Altering the 953Ω resistor and the 24μH inductor can change both k and τ, permitting cylinder dependent equalization to be performed, thus minimizing problems of overequalization. To alter k, the ratio of the 1.1kΩ and 953Ω resistors should be changed. To alter τ, the reactive element should be scaled proportionally. The equalizer in Figure 2 is optimized for k = 0.6 and τ = 12ns.

It is important to note the benefits of fully differential (as opposed to single-ended) operation: 1) reduced harmonic distortion due to symmetric operation; 2) improved power supply noise rejection; 3) less insertion loss, allowing for reduced gain and, hence, improved distortion in stages prior to the equalizer.

CHOICE OF LOW PASS FILTER WITH THE RECOMMENDED EQUALIZER

A fifth order, Gaussian-to-6dB transitional filter is recommended for use with the equalizer. Such a low pass filter is shown in Figure 4. Low group delay ripple and high out-of-band rejection make this design work well with the recommended equalizer and the differentiator specified in the AD891 data sheet. The recommended location for the low pass filter is between the VGA and first X4 buffer. The equalizer should be placed between the first and second X4 buffers. This minimizes the potential for oscillations induced by interstage parasitic feedback.

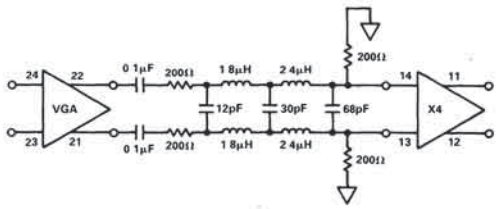


Figure 4. 5th Order Gaussian-to-6dB Transitional Filter

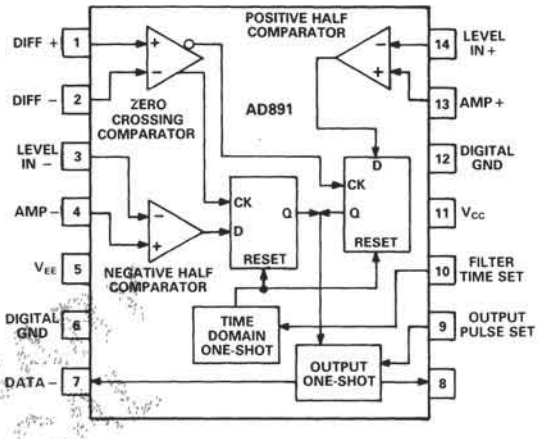
Rigid Disk Data Channel Qualifier

AD891

FEATURES

Three Matched, Offset-Trimmed Comparators
3.1ns (typ) Comparator Propagation Delay
ECL Logic Permits 50Mb/s Transfer Rates
6.8ns Delay (typ) from Inputs to Data Output
500ps (typ) Additional Pulse Pairing
Temperature-Compensated Operation
Compatible with 10kH ECL Logic
Two Temperature-Compensated One-Shots
One-Shot Periods Set Using External Resistors

AD891 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD891 disk channel qualifier is intended as a companion chip to the AD890 wideband channel processor. Together, they comprise a sophisticated package, capable of recovering binary information from differentiating channels with transfer rates in excess of 50 megabits per second.

The AD891 provides both level and time-domain qualification. Level qualification is performed on alternating half cycles of the data waveform using a user-defined threshold level which is applied to each of two 3.1ns propagation delay comparators. This technique prevents single bit errors from being propagated into two bit errors. A third comparator is used to provide zero-crossing detection. Factory trimmed offsets and a careful internal layout ensure symmetric operation and low pulse pairing with a differential input waveform.

An external RLC passive delay-line differentiator should be used with the AD891; the design for a typical network is specified in detail in the applications section of this data sheet. The use of an external network permits equal delay times through both the differentiated and undifferentiated signal paths, thus ensuring correct centering of the qualification windows. Using the recommended external network also helps ensure optimal signal passband flatness and dispersion.

The outputs from the amplitude-qualification comparators are applied to the "D" inputs of two master-slave D-type flip-flops which are then clocked by the outputs from the zero-crossing comparator. Each valid zero-crossing event causes a one-shot with a user-definable period to be triggered. This disables the operation of the flip-flops, thus preventing the detection of additional zero-crossing events during the one-shot period.

Simultaneously, an output one-shot is activated, the leading edge of which is synchronous with the change in the flip-flop outputs. The period of this one-shot is also user-definable and is intended to ensure adequate output pulse duration for transmission within the external environment. Each one-shot requires a single metal-film resistor to set its period. All one-shots have trimmed pulse periods; temperature stability is maintained by the use of an internal bandgap reference.

The AD891's internal logic consists of temperature-compensated reduced-swing ECL which exhibits typical propagation delays of 600ps per gate. The output data conforms to standard 10kH ECL logic levels. The AD891 can drive a properly terminated 75Ω transmission line.

The AD891 is specified to operate over the commercial (0 to +70°C) temperature range. It is available either in a 14-pin cerdip package or in a 20-pin PLCC package.

PRODUCT HIGHLIGHTS

1. When paired with the AD890 wideband channel processor, data can be recovered in excess of a 50 Mb/s rate.
2. Comparators have 3.1ns typical propagation delay.
3. 10kH ECL logic compatible.
4. 500ps typical additional pulse pairing through chip.
5. Two internal, temperature-compensated one shots.
6. Features both amplitude and time-delay qualification.

SPECIFICATIONS (@ +25°C and ±5V dc, unless otherwise noted)

Model	Conditions	AD891J Min	AD891J Typ	AD891J Max	Units
COMPARATOR SPECIFICATIONS					
Propagation Delay	20mV Overdrive		3.3		ns
	200mV Overdrive		3.1		ns
Comparator Mismatch				300	ps
Input Offset Voltage			0.25	**1.0**	mV
Noise Induced Offset Voltage	10^8 Error Rate		± 300		µV
Input Offset Current			100		nA
Input Bias Current			1.3		µA
Open-Loop Gain	f = 10MHz		66		dB
Input Resistance	Differential		500		kΩ
Input Common-Mode Range	Referred to Digital GND	−1.5		+2.2	V
INTERNAL LOGIC SPECIFICATIONS					
Logic "1" Level			−0.75		V
Logic "0" Level			−1.4		V
Rise Time			1.2		ns
Fall Time			1.0		ns
D-Type Flip-Flops					
Clock – Q Delay			1.3		ns
Clock – $\overline{Q}$ Delay			1.2		ns
Reset – Q Delay			0.6		ns
Reset – $\overline{Q}$ Delay			0.55		ns
ONE-SHOT SPECIFICATIONS					
Resistor Scaling[1]	One-Shot Pulse ≈ 7 + 3.1R_{SET}				
Pulse Duration	R_{SET} = R_{min} to R_{max}	9		180	ns
	R_{SET} = 30kΩ	**97**	100	**103**	ns
	R_{SET} = 10kΩ	**39**	42	**45**	ns
Resistor Range	R_{SET} = R_{min} to R_{max}	0.75		56	kΩ
EXTERNAL LOGIC SPECIFICATIONS[2]	T_J = +25°C				
Output Logic "1"			−0.85		V
Output Logic "0"			−1.85		V
Rise Time			1.4		ns
Fall Time			1.2		ns
DATA THROUGHPUT SPECIFICATIONS					
Propagation Delay[3]	Differentiator Input to Data Output		6.8		ns
Additional Pulse Pairing[4]	200mV Overdrive 5ns Input Rise Time		500	**1000**	ps
Max Transfer Rate		50			Mb/s
Min Transfer Rate[5]				1	Mb/s
POWER SUPPLY REQUIREMENTS					
Rated Performance			±5.0		V
Operating Range		±4.65		±6.8	V
Quiescent Current	T_{min} to T_{max}				
V_{CC}		**15**	23	**35**	mA
V_{EE}		**55**	68	**85**	mA

NOTES
[1]One-shot pulse in ns; R_{SET} specified in kΩ.
[2]Logic specifications obtained for the "Data +" and "Data −" outputs using 1kΩ pull-down resistors tied to V_{EE} and 100Ω resistors connected to −2V.
[3]Propagation delay is measured from the zero-crossing comparator input to the "Data +" output with 200mV overdrive.
[4]Measurements were performed using a ± 100mV square wave having a rise time under 5ns; this was applied to the input of the zero-crossing comparator. The resultant pulse pairing is the difference in delay times for two consecutive output pulses.
[5]The minimum transfer rate is limited only by the maximum recommended one-shot period of 180ns.

Specifications subject to change without notice.

Specifications in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

PRELIMINARY TECHNICAL DATA

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage	±7.5V
Comparator Differential Input Voltage	±5.6 V
Storage Temperature Range P,Q	−65°C to +150°C
Operating Temperature Range[2]	
AD891P, AD891Q	0 to +70°C
Lead Temperature Range (Soldering 60sec)	+300°C

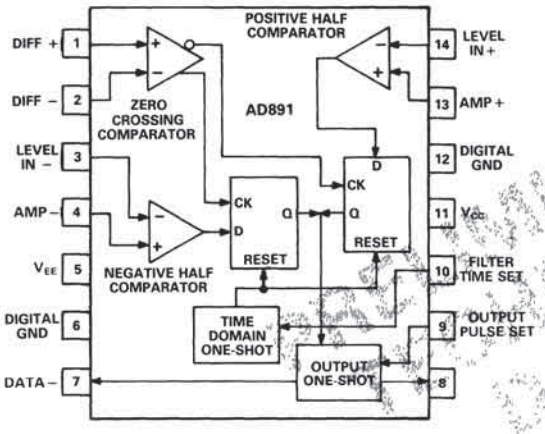
NOTES

[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

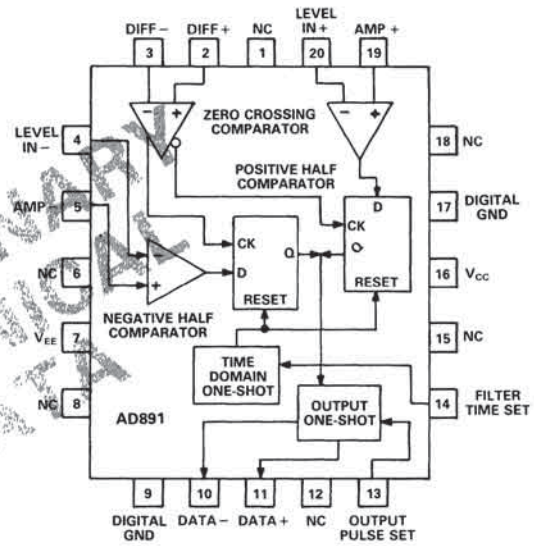
[2]20-pin PLCC package: $\theta_{JA} = +70°C/Watt$;
14-pin cerdip package: $\theta_{JA} = +105°C/Watt$.

PIN CONFIGURATIONS

14-Pin Cerdip (Q) Package



20-Pin PLCC (P) Package



ORDERING GUIDE

Model No.	Package Option*
AD891JQ	Cerdip (Q-14)
AD891JP	PLCC (P-20A)

*See Section 16 for package outline information.

9

Applying the AD891

THEORY OF OPERATION

The AD891 consists of three comparators, two D-type flip-flops, an internal bandgap reference and a pair of externally adjustable one-shots. Two comparators are used to provide data amplitude qualification, and the third acts as a zero-crossing detector when used with an external passive differentiator circuit. (Refer to the AD891 block diagram and Figure 2.)

Figure 2 illustrates the operation of the AD891, using the recommended passive delay-line differentiator described in the following section. Sequence "A" represents the pattern written on the disk, where a logic "1" is a change in magnetic state. Each change in magnetic state results in an output pulse. The analog input to the AD891 consists of a sequence of alternating pulses "B." The data pattern shown is worst case for a 1-7 code input. "C" represents the output waveform from the external differentiator, such that the points at which zero-crossings occur correspond to the peaks of the analog input "B." Sequence "D" shows the output from the zero-crossing comparator. Changes in state of this output are used to clock the two internal D-type flip-flops. The flip-flops are enabled using the output "E" from the positive and negative threshold comparators, such that the flip-flop outputs change state only when the analog input exceeds the programmed threshold levels (positive or negative). When the threshold levels are exceeded and a zero-crossing event occurs, the flip-flops change state, producing an output pulse "F." The duration of this pulse, seen at the Data+/Data− outputs, is set using an external resistor, as is the internal time-out which is used to prevent noise induced retriggering. The final output data sequence is shown in "G." As can be seen, despite inflections in the analog input, the data is correctly detected and the output is a time-shifted version of the write data.

Since the 1-7 code input is the most demanding of the popular encoding schemes to qualify, the AD891 is clearly suitable for other codes, such as MFM and 2-7. The recommended time domain filter one-shot period for MFM and 1-7 code is equal to 75% of the bit cell clock period. For 2-7 code the one-shot period can be increased to 150% of the bit cell clock period.

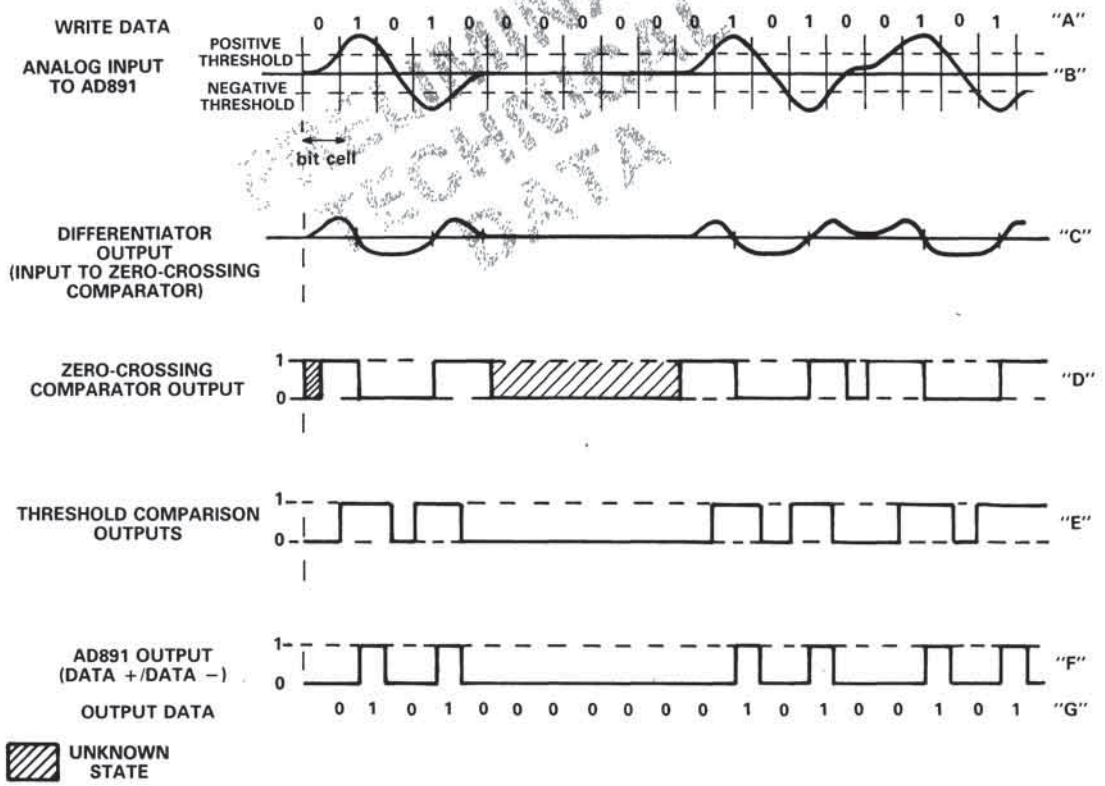


Figure 1. AD891 Operation for Worst Case 1-7 Code Pattern

DESIGN CONSIDERATIONS

In designing a suitable passive delay-line differentiator, either the fully differential (Figure 2a) or single-ended (Figure 2b) configuration can be used. The equations governing component selection for both connections are as shown.

If the single-ended configuration is employed, then the inputs to the negative half-cycle comparator need to be biased such that the comparator is turned off. This can be accomplished by placing the "Amp−" input at a potential at least 100mV more negative than the "Level In−" input. The "Amp−" pin may be connected to the "V_{EE}" pin and the "Level In−" pin may be connected to the "Digital GND" pin, provided that the potential difference does not exceed 5.6 volts, which is the absolute maximum differential input rating of the device.

Good RF layout practice should be obeyed, with decoupling networks of 0.1μF in parallel with 0.01μF at both the "V_{CC}" and "V_{EE}" pins. A ground plane should be used extensively. Two digital grounds are supplied: Pin 12 is for the internal logic while Pin 5 is provided for the "Data" outputs only. (These pins are for the cerdip package; the corresponding PLCC package pins are 17 and 9, respectively.) The filter time and output pulse setting resistors should be tied, as directly as possible, to the "Digital GND" pin.

The "Data−" and "Data+" pins require pull-down resistors to "V_{EE}" as per normal practice in ECL. The use of 30kΩ resistors connected between the "Filter Time Set" and "Output Pulse Set" pins and digital ground will produce a nominal 100ns one-shot period; 10kΩ resistors will nominally produce 42ns one-shot periods. The timing of the two one-shots may be set independently.

For best performance, the three input comparators should be operated at a common-mode potential close to digital ground. The digital ground should be connected to the analog ground as near to the power supply as possible to minimize noise injection.

INTEGRATING WITH THE AD890 WIDEBAND CHANNEL PROCESSING ELEMENT

Figure 3 shows a typical application using the AD891 and AD890 connected together to create a 30MHz channel (cerdip connections shown). This circuit includes a 5-pole 30MHz gaussian-to-6dB transitional filter plus a second-order RLC time domain equalizer. The fully differential passive delay-line differentiator previously discussed is also included. The analog and digital grounds should be connected only to the power supply common.

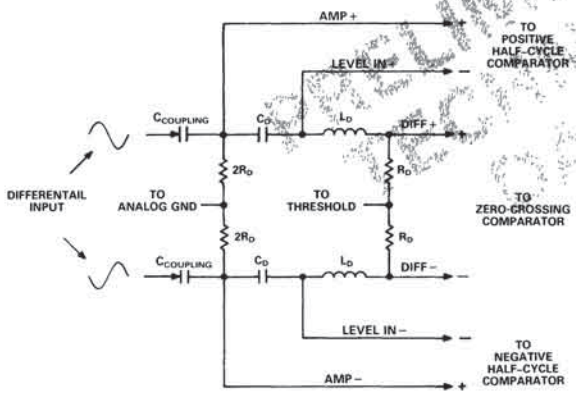


Figure 2a. Fully Differential Configuration of Passive Delay-Line Differentiator

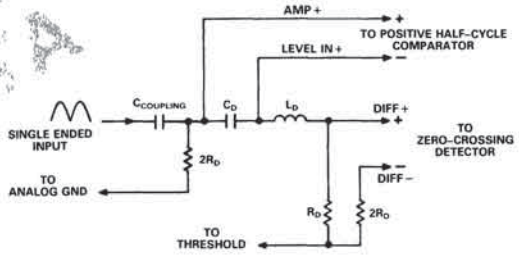


Figure 2b. Single-Ended Configuration of Passive Delay-Line Differentiator

RECOMMENDED COMPONENTS

$$f_D = \frac{1}{2\pi\sqrt{L_D C_D}}$$

f = 1.5 Times the Maximum Desired Differentiated Frequency

$$R_D = K\left[\sqrt{\frac{L_D}{C_D}}\right]$$

R_D Minimum Value: 120Ω
150Ω or Greater is Recommended

1.3 (Best Magnitude Response) ≤K ≤1.7 (Best Group Delay Response)

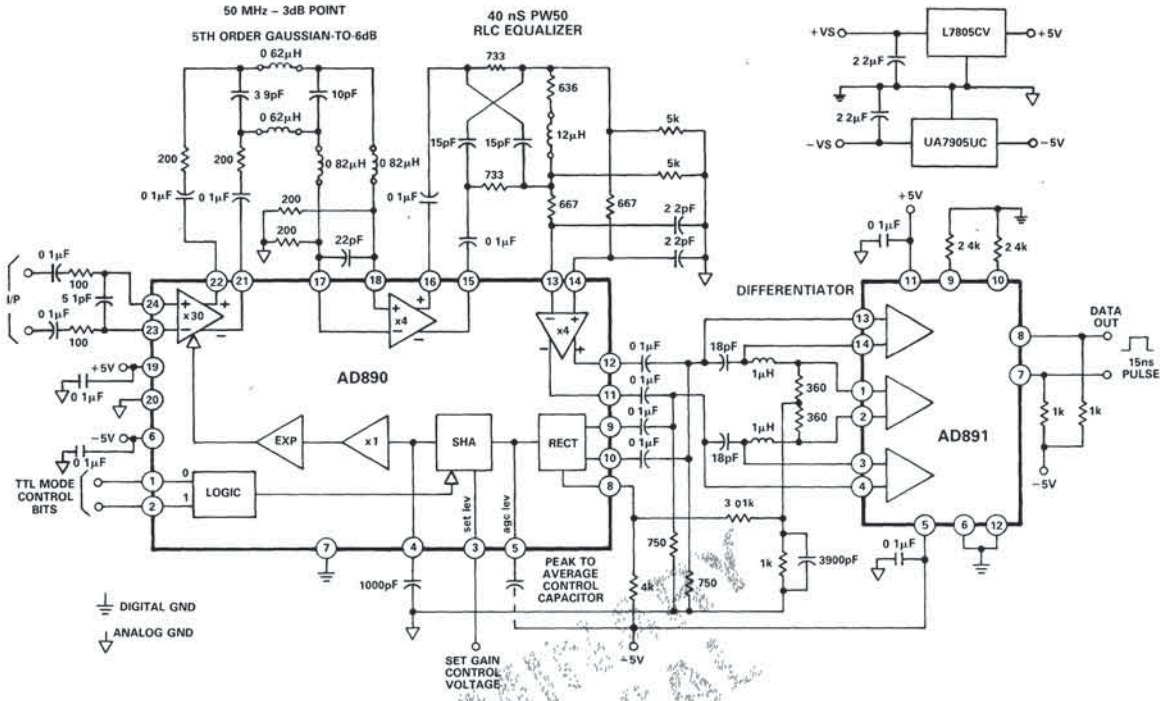


Figure 3. Typical AD890/AD891 Connection for a 30MHz Channel

OPERATION WITH +5V, +12V SUPPLIES

Operation with +5V (±0.25V) and +12V (±1.2V) supplies is readily achieved. The digital ground pins must be connected to the +5V line or to an available center tap of the +12V supply. The specified output ECL logic levels are therefore referred to the +5V supply. Pull-down resistors for the "Data+" and "Data−" pins should be connected to V_{EE}. Thus connected, a current of approximately 23mA will flow in the +5V supply under normal operation.

In order to ensure correct comparator operation, a pair of 100mA diodes should be added in series with the +12V supply which is connected to the V_{CC} terminal. This connection is shown in Figure 4 (shown for cerdip package).

Both the +5V and +12V supplies should be RF bypassed to ground; the values of 0.1µF and 0.01µF in parallel are recommended. In addition, some higher value of decoupling capacitance – such as 3.3µF – may be desirable. This decoupling should be applied directly at the AD891 "V_{CC}" and "Digital GND" pins. Finally, the common-mode range for the comparators is now referred to the +5V supply line, and care must be taken to operate within the common-mode limits.

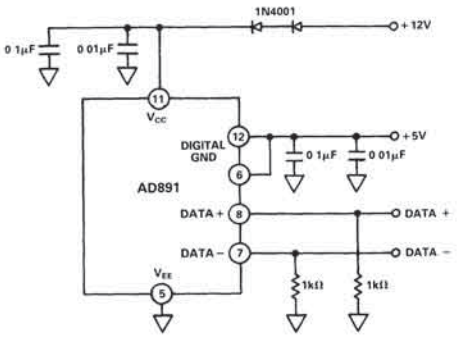


Figure 4. AD892 Connection for +5V, +12V Operation

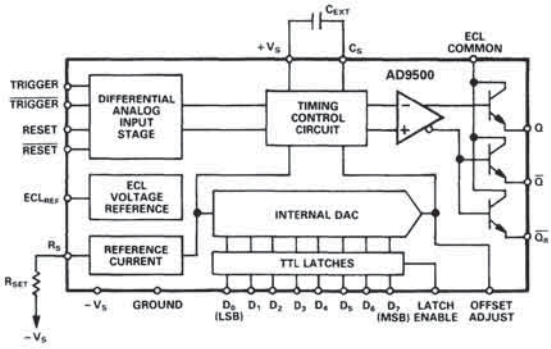
Digitally Programmable Delay Generator

AD9500

FEATURES
10ps Delay Resolution
2.5ns to 100μs+ Full-Scale Range
Fully Differential Inputs
Separate Trigger and Reset Inputs
Low Power Dissipation – 310mW

APPLICATIONS
ATE
Pulse Deskewing
Arbitrary Waveform Generators
High-Stability Timing Source
Multiple Phase Clock Generators

AD9500 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

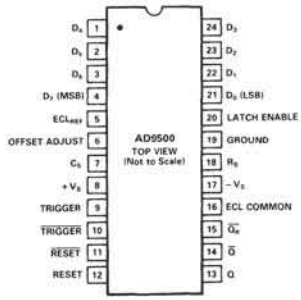
The AD9500 is a digitally programmable delay generator, which provides programmed delays, selected through an 8-bit digital code, in resolutions as small as 10ps. The AD9500 is constructed in a high-performance bipolar process, designed to provide high-speed operation for both digital and analog circuits.

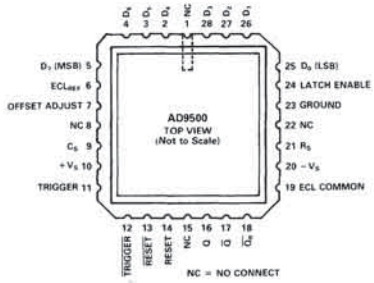
The AD9500 employs differential TRIGGER and RESET inputs which are designed primarily for ECL signal levels but function with analog and TTL input levels. An on-board ECL reference midpoint allows both of the inputs to be driven by either single ended or differential ECL circuits. The AD9500 output is a complementary ECL stage, which also provides a parallel $\overline{Q_R}$ output circuit to facilitate reset timing implementations.

The digital control data is passed to the AD9500 through a transparent latch controlled by the LATCH ENABLE signal. In the transparent mode, the internal DAC of the AD9500 will attempt to follow changes at the inputs. The LATCH ENABLE is otherwise used to strobe the digital data into the AD9500 latches.

The AD9500 is available as an industrial temperature range device, −25°C to +85°C, and as an extended temperature range device, −55°C to +125°C. Both grades are packaged in a 24-pin ceramic "Skinny" DIP (0.3" package width), as well as 28-pin surface mount packages. Contact the factory for MIL-STD-883, revision C, qualified devices.

PIN CONFIGURATIONS





ORDERING INFORMATION

Device	Temperature Range	Description	Package Options*
AD9500BP	−25°C to +85°C	28-Pin PLCC (Plastic), Industrial Temperature	P-28A
AD9500BQ	−25°C to +85°C	24-Pin "Skinny" DIP, Industrial Temperature	Q-24
AD9500TE	−55°C to +125°C	28-Pin LCC, Extended Temperature	E-28A
AD9500TQ	−55°C to +125°C	24-Pin "Skinny" DIP, Extended Temperature	Q-24

*See Section 16 for package outline information.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) . . . . . +7V
Negative Supply Voltage ($-V_S$) . . . . . −7V
ECL COMMON to Ground Differential . . −2.0V to +5.0V
Digital Input Voltage Range . . . . . −3.5V to +5.0V
Trigger/Reset Input Voltage Range . . . . . ±5.0V
Trigger/Reset Differential Voltage 5.0V
Minimum R_{SET} 220Ω
Digital Output Current (Q and $\overline{Q}$) 30mA
Digital Output Current ($\overline{Q_R}$) 2mA
Offset Adjust Current (Sinking) 4mA
Power Dissipation (+25°C Free Air)[2] 2.62W
Operating Temperature Range
AD9500BP/BQ . . . . . −25°C to +85°C
AD9500TE/TQ . . . . . −55°C to +125°C
Storage Temperature Range . . . . . −65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Soldering Temperature (10sec) . . . . . +300°C

ELECTRICAL CHARACTERISTICS (Supply Voltages + V_S = +5.0V, $-V_S$ = −5.2V; C_{EXT} = 0pF; R_{SET} = 500Ω, unless otherwise stated)

Parameter	Mil[3] Sub Group	Temp	Industrial −25°C to +85°C AD9500BP/BQ Min	Typ	Max	Military −55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
RESOLUTION			8			8			Bits
ACCURACY[4]									
Differential Linearity	7	+25°C			0.5			0.5	LSB
Integral Linearity	7	+25°C			1.0			1.0	LSB
Monotonicity	7	+25°C		Guaranteed			Guaranteed		
DIGITAL INPUT									
Logic "1" Voltage	7,8	Full	2.0			2.0			V
Logic "0" Voltage	7,8	Full			0.8			0.8	V
Logic "1" Current	1,2,3	Full			5			5	µA
Logic "0" Current	1,2,3	Full			5			5	µA
Digital Input Capacitance	12	+25°C			5.5			5.5	pF
Data Setup Time[5]	12	+25°C		0.4	0.75		0.4	0.75	ns
Data Hold Time[6]	12	+25°C		0.4	0.75		0.4	0.75	ns
Latch Pulse Width (t_{LPW})	12	+25°C	3.0			3.0			ns
RESET/TRIGGER INPUTS[7]									
TRIGGER Input Voltage Range		Full		−2.5;4.5			−2.5;4.5		V
RESET Input Voltage Range		Full		−2.5;2.0			−2.5;2.0		V
Differential Switching Voltage	7,8	Full		40	300		40	300	mV
Input Bias Current	1	+25°C		40	50		40	50	µA
	2,3	Full			75			75	µA
Input Resistance		+25°C		4			4		kΩ
Input Capacitance	12	+25°C		6.5	7.25		6.5	7.25	pF
Minimum Input Pulse Width (t_{TPW}, t_{RPW})		+25°C		2.0			2.0		ns
DYNAMIC PERFORMANCE[8]									
Maximum Trigger Rate	12	+25°C	100			100			MHz
Minimum Propagation Delay (t_{PD})[9]	4	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Minimum Propagation Delay TC[10]		Full		7.5			7.5		ps/°C
Full-Scale Range TC		Full		0.5			0.5		ps/°C
Delay Uncertainty (Jitter)		+25°C		10			10		ps
Reset Propagation Delay (t_{RD})[11]	4	+25°C	5.4	6.4	7.4	5.4	6.4	7.4	ns
Reset-to-Trigger Holdoff (t_{THO})[12]	4	+25°C	0.2	0		0.2	0		ns
Trigger-to-Reset Holdoff (t_{RHO})[13]	4	+25°C	2.0	1.5		2.0	1.5		ns
Minimum Output Pulse Width		+25°C		3.3			3.3		ns
Output Rise Time	12	+25°C			2.0			2.0	ns
Output Fall Time	12	+25°C			2.0			2.0	ns
Delay Coefficient Settling Time (t_{DAC})[14]		+25°C		29			29		ns
Linear Ramp Settling Time (t_{LRS})		+25°C		22			22		ns

Parameter	Mil[3] Sub Group	Temp	Industrial −25°C to +85°C AD9500BP/BQ Min	Typ	Max	Military −55°C to +125°C AD9500TE/TQ Min	Typ	Max	Units
SUPPORT FUNCTIONS									
ECL_{REF}	1	+25°C	−1.4	−1.3	−1.2	−1.4	−1.3	−1.2	V
ECL_{REF} Voltage Drift[15]		Full		1.1			1.1		mV/°C
Offset Adjust Range		Full		−2			−2		mA
DIGITAL OUTPUTS[8]									
Logic "1" Voltage	1, 2, 3	Full	−1.1			−1.1			V
Logic "0" Voltage	1, 2, 3	Full			−1.5			−1.5	V
POWER SUPPLY[16]									
Positive Supply Current (+5.0V)	1	+25°C		24	28		24	28	mA
	2, 3	Full			30			30	mA
Negative Supply Current (−5.2V)	1	+25°C		37	42		37	42	mA
	2, 3	Full			44			44	mA
Nominal Power Dissipation		+25°C		312			312		mW
Power Supply Rejection Ratio[17]									
Full-Scale Range Sensitivity	7	+25°C		70	300		70	300	ps/V
Minimum Propagation Delay Sensitivity	7	+25°		150	500		150	500	ps/V

NOTES

[1]Absolute maximum ratings are limiting values, to be applied individually, and beyond which serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Typical thermal impedance

24-Pin Ceramic $\theta_{JA} = 56°C/W; \theta_{JC} = 16°C/W$
28-Pin PLCC (Plastic) $\theta_{JA} = 60°C/W; \theta_{JC} = 22°C/W$
28-Pin Ceramic LCC $\theta_{JA} = 69°C/W; \theta_{JC} = 25°C/W$

[3]Military subgroups apply to military qualified devices only.

[4]$R_{SET} = 10k\Omega$. (Full-scale delay = 100ns).

[5]The digital data inputs must remain stable for the specified time prior to the LATCH ENABLE signal.

[6]The digital data inputs must remain stable for the specified time after the LATCH ENABLE signal.

[7]The TRIGGER and RESET inputs are differential and must be driven relative to one another. Both of these inputs are ECL compatible, but can also be used with TTL logic families in a limited fashion.

[8]Outputs terminated through 50Ω resistors to −2.0V.

[9]Program Delay = 0.0ps (Digital Data = 00_H). In Operation, any programmed delays are in addition to the Minimum Propagation Delay.

[10]Measured from the 50% transition point of the reset signal input, to the 50% transition point of the resetting output.

[11]Minimum time from falling edge of RESET to triggering input, to insure a valid output event.

[12]Change in total delay through AD9500, exclusive of changes in minimum-propagation delay t_{PD}.

[13]Minimum time from triggering event to rising edge of RESET, to insure a valid output event.

[14]Measured from the LATCH ENABLE input to the point when the AD9500 becomes 8-bit accurate again, after a full-scale change in the programmed delay.

[15]Standard 10K and 10KH ECL families operate with a 1.1mV/°C drift by design.

[16]Supply voltages should remain stable within ±5% for normal operation.

[17]Measured at ±5% of $-V_S$ and $+V_S$.

Specifications subject to change without notice.

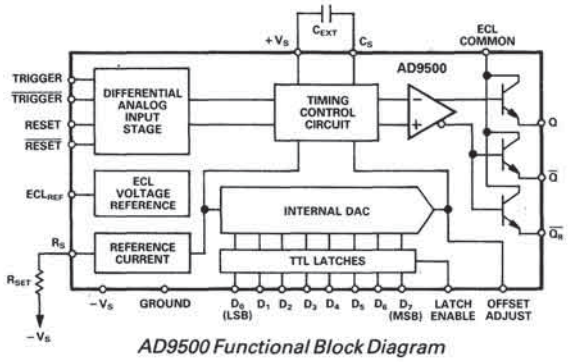
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EXPLANATION OF GROUP A MILITARY SUBGROUPS

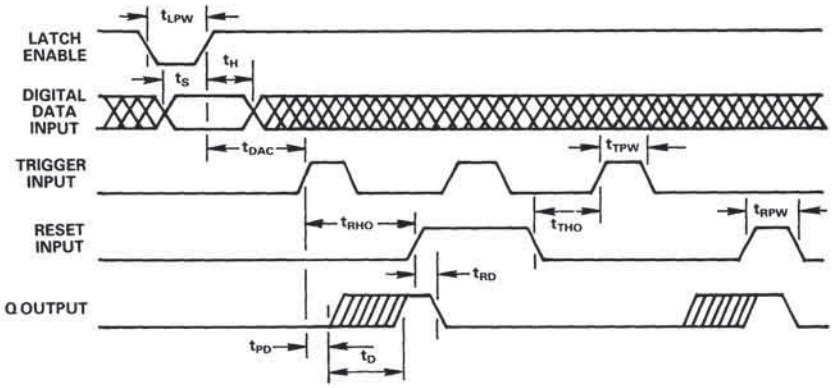
Subgroup 1 – Static tests at +25°C.
Subgroup 2 – Static tests at max rated operating temp.
Subgroup 3 – Static tests at min rated operating temp.
Subgroup 4 – Dynamic tests at +25°C.
Subgroup 5 – Dynamic tests at max rated operating temp.
Subgroup 6 – Dynamic tests at min rated operating temp.
Subgroup 7 – Functional tests at +25°C.
Subgroup 8 – Functional tests at max and min rated operating temp.
Subgroup 9 – Switching tests at +25°C.
Subgroup 10 – Switching tests at max rated operating temp.
Subgroup 11 – Switching tests at min rated operating temp.
Subgroup 12 – Periodically sample tested.

FUNCTIONAL DESCRIPTION

PIN NAME	DESCRIPTION
D_4–D_6	– One of eight digital inputs used to set the programmed delay.
D_7 (MSB)	– One of eight digital inputs used to set the programmed delay. D_7 (MSB) is the most significant bit of the digital input word.
ECL_{REF}	– ECL midpoint reference, nominally −1.3V. Use of the ECL_{REF}, allows either of the TRIGGER or the RESET inputs to be configured for single-ended ECL inputs.
OFFSET ADJUST	– The OFFSET ADJUST is used to adjust the minimum propagation delay (t_{PD}), by pulling or pushing a small current out of or into the pin.
C_S	– C_S allows the full-scale range to be extended by using an external timing capacitor. The value of C_{EXT}, connected between C_S and $+V_S$, may range from 0pF to 0.1μF+. See R_S ($C_{INTERNAL}$ = 10pF).
$+V_S$	– Positive supply terminal, nominally +5.0V.
TRIGGER	– Noninverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The TRIGGER input must be driven in conjunction with the $\overline{\text{TRIGGER}}$ input.
$\overline{\text{TRIGGER}}$	– Inverted input of the edge-sensitive differential trigger input stage. The output at Q will be delayed by the programmed delay, after the triggering event. The programmed delay is set by the digital input word. The $\overline{\text{TRIGGER}}$ input must be driven in conjunction with the TRIGGER input.
$\overline{\text{RESET}}$	– Inverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The RESET input must be driven in conjunction with the $\overline{\text{RESET}}$ input.
RESET	– Noninverted input of the level-sensitive differential reset input stage. The output at Q will be reset after a signal is received at the reset inputs. In the "minimum configuration," the minimum output pulse width will be equal to the "reset propagation delay," t_{RD}. The $\overline{\text{RESET}}$ input must be driven in conjunction with the RESET input.
Q	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic HIGH on the Q output. A "resetting" event at the inputs will produce a logic LOW on the Q output
$\overline{Q}$	– One of two complementary ECL outputs. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q}$ output.
$\overline{Q_R}$	– $\overline{Q_R}$ output is parallel to the $\overline{Q}$ output. The $\overline{Q_R}$ output is typically used to drive delaying circuits for extending output pulse widths. A "triggering" event at the inputs will produce a logic LOW on the $\overline{Q_R}$ output. A "resetting" event at the inputs will produce a logic HIGH on the $\overline{Q_R}$ output.
ECL COMMON	– The collector common for the ECL output stage. The collector common may be tied to +5.0V, but normally it is tied to the circuit ground for standard ECL outputs.
$-V_S$	– Negative supply terminal, nominally −5.2V.
R_S	– R_S is the reference current setting terminal. An external setting resistor, R_{SET}, connected between R_S and $-V_S$ determines the internal reference current. See C_S ($250\Omega \le R_{SET} \le 50k\Omega$).
GROUND	– The ground return for the TTL and analog inputs.
LATCH ENABLE	– Transparent TTL latch control line. A logic HIGH on the LATCH ENABLE freezes the digital code at the logic inputs. A logic LOW on the LATCH ENABLE allows the internal current levels to be continuously updated through the logic inputs D_0 thru D_7.
D_0 (LSB)	– One of eight digital inputs used to set the programmed delay. D_0 (LSB) is the least significant bit of the digital input word.
D_3–D_1	– One of eight digital inputs used to set the programmed delay.



AD9500 Functional Block Diagram

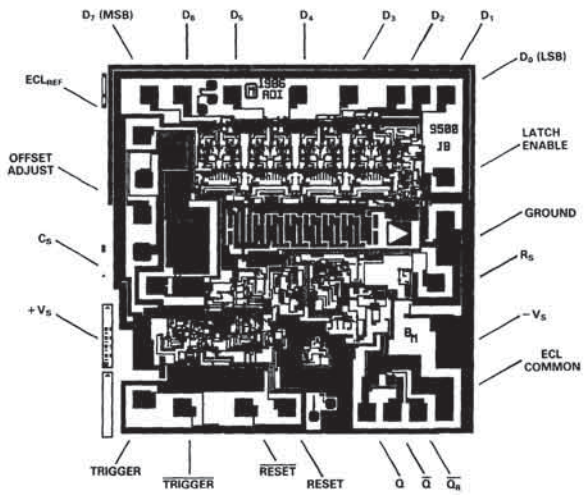


t_S – DIGITAL DATA SETUP TIME
t_H – DIGITAL DATA HOLD TIME
t_{LPW} – LATCH ENABLE PULSE WIDTH
t_{DAC} – INTERNAL DAC SETTLING TIME
t_{PD} – MINIMUM PROPAGATION DELAY
t_{RD} – RESET PROPAGATION DELAY
t_D – PROGRAMMED DELAY
t_{TPW} – TRIGGER PULSE WIDTH
t_{RPW} – RESET PULSE WIDTH
t_{THO} – RESET-TO-TRIGGER HOLDOFF
t_{RHO} – TRIGGER-TO-RESET HOLDOFF

NOTE
A TRIGGERING EVENT MAY OCCUR AT ANY TIME WHILE THE INTERNAL DAC (PROGRAMMED DELAY) IS BEING CHANGED. TRIGGERING EVENTS DURING THE INTERNAL DAC SETTLING TIME MAY NOT GENERATE AN ACCURATE PULSE DELAY.

System Timing Diagram

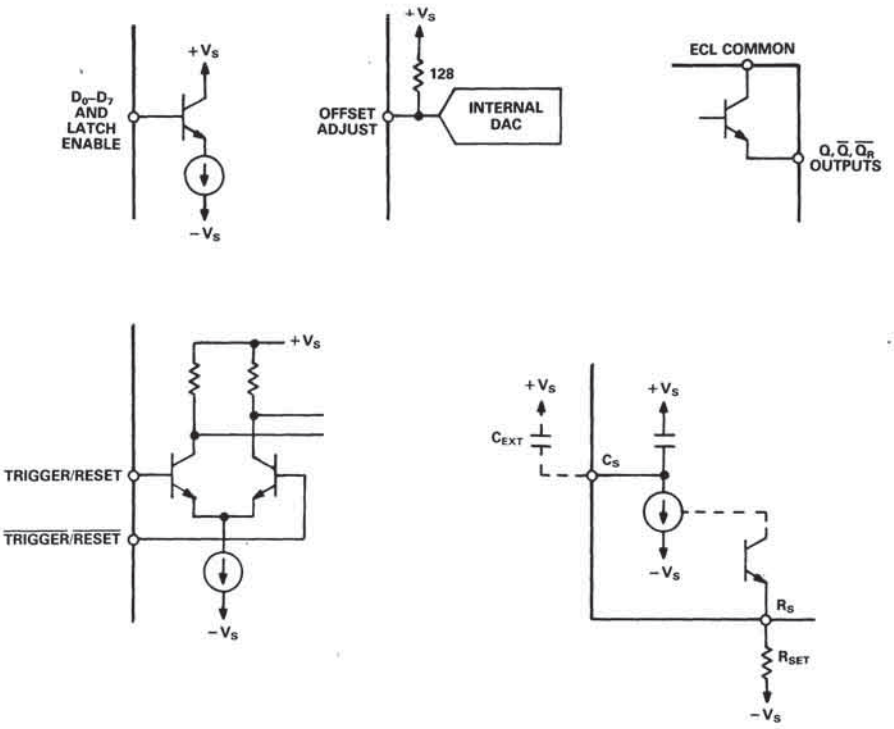
DIE LAYOUT



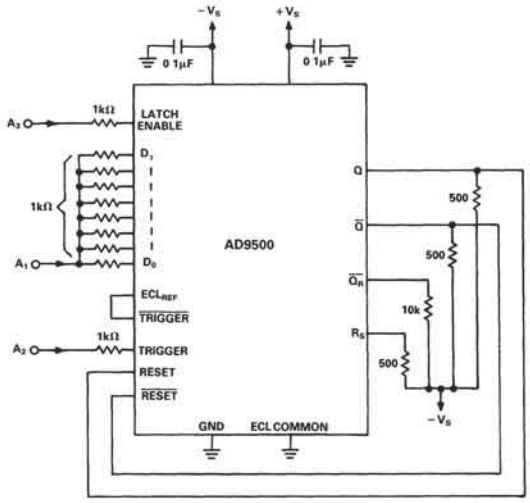
MECHANICAL INFORMATION

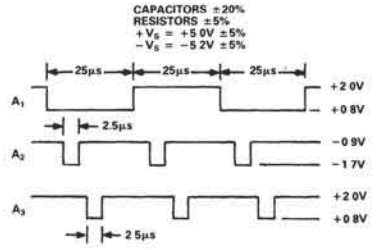
Die Dimensions	104 × 103 × 18 (max) mils
Pad Dimensions	4 × 4 (min)mils
Metalization	Aluminum
Backing	None
Substrate Potential	$-V_S$
Passivation	Oxynitride
Die Attach	Gold Eutectic
Bond Wire	1.25 mil, Aluminum; Ultrasonic Bonding or 1mil, Gold; Gold Ball Bonding

Input/Output Circuits



Burn-In Circuit





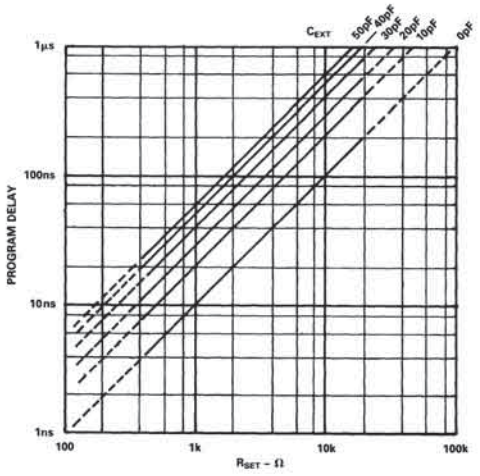
INSIDE THE AD9500

The heart of the AD9500 is the linear ramp generator. A triggering event at the input of the AD9500 initiates the ramp cycle. As the ramp voltage falls, it will eventualy go below the threshold set up by the internal DAC (digital-to-analog converter). A comparator monitors both the linear ramp voltage and the DAC threshold level. The output of the comparator serves as the output for the AD9500, and the interval from the trigger until the output switches is the total delay time of the AD9500.

The total delay through the AD9500 is made up of two components. The first is the full-scale programmed delay, $t_{D\ (max)}$, determined by R_{SET} and C_{EXT}. The second component of the total delay is the minimum propagation delay through the AD9500 (t_{PD}). The full-scale delay is variable from 2.5ns to greater than 1ms. The internal DAC is capable of generating 256 separate programmed delays within the full-scale range (this gives 10ps increments for a 2.5ns full-scale setting).

The actual programmed delay is directly related to both the digital control data (digital data to the internal DAC) and the RC time constant established by R_{SET} and C_{EXT}. The specific relationship is as follows:

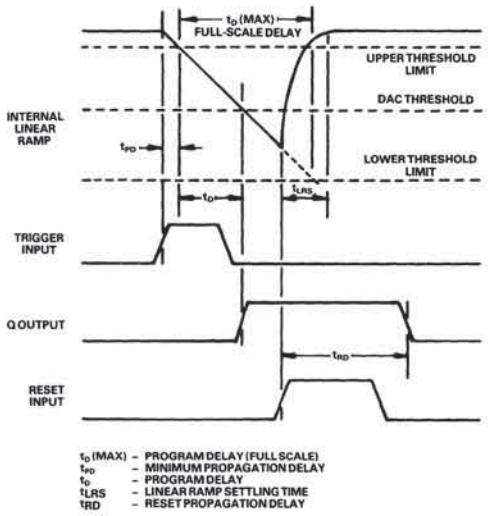
$$\text{Total Delay} = \text{Minimum Propagation Delay} + \text{Programmed Delay}$$
$$= t_{PD} + (\text{digital value}/256)\, R_{SET}\, (C_{EXT} + 10\text{pF})$$



Typical Programmed Delay Ranges

The internal DAC determines the programmed delay by way of the threshold level at its output. The LATCH ENABLE control for the on-board latch is active (latches) logic "HIGH". In the logic "LOW" state, the latch is transparent, and the internal DAC will attempt to follow changes at the digital data inputs.

Both the LATCH ENABLE control and the data inputs are TTL compatible. The internal DAC may be updated at any time, but full timing accuracy may not be attained unless triggering events are held off until after the DAC settling time (t_{DAC}).



Internal Timing Diagram

On resetting, the ramp voltage held in the timing capacitor (C_{EXT} + 10pF) is discharged. The AD9500 discharges the bulk of the ramp voltage very quickly, but to maintain *absolute* accuracy, subsequent triggering events should be held off until after the linear ramp settling time (t_{LRS}). Applications which employ high frequency triggering at a constant rate will not be affected by the slight settling errors since they will be constant for fixed reset-to-trigger cycles.

The RESET and TRIGGER inputs of the AD9500 are differential and must be driven relative to one another. Accordingly, the TRIGGER and RESET inputs are ideally suited for analog or complementary input signals. Single-ended ECL input signals can be accommodated by using the ECL midpoint reference (ECL_{REF}) to drive one side of the differential inputs.

The output of the AD9500 consists of both Q and $\overline{Q}$ driver stages, as well as the $\overline{Q_R}$ output which is used primarily for extending the output pulse width. In the most direct reset configuration, either the Q or the $\overline{Q}$ output is tied to the respective RESET input. This generates a delayed output pulse with a duration equal to the reset delay time (t_{RD}) of approximately 6ns. Note that the reset delay time (t_{RD}) becomes extended for very small programmed delay settings. The duration of the output pulse can be extended by driving the reset inputs with the $\overline{Q_R}$ output through an RC network (see "Extended Output Pulse Width" application). Using the $\overline{Q_R}$ output to drive the reset circuit avoids loading the Q or $\overline{Q}$ outputs.

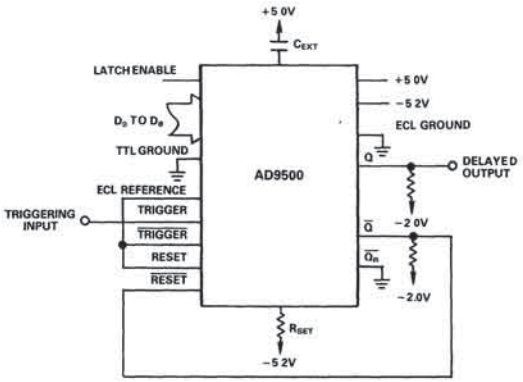
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APPLICATIONS

The AD9500 is a very versatile device, but at the same time, it is not difficult to use. Essentially there are only a few basic configurations which can be extended into a number of applications. The TRIGGER and RESET inputs of the AD9500 can be treated as single ended, or as differential, which allows the AD9500 to operate with a wide range of signal sources. The output pulse from the AD9500 can be reset in one of two ways, either immediately by driving the RESET inputs with the output itself, or in a delayed mode.

MINIMUM CONFIGURATION

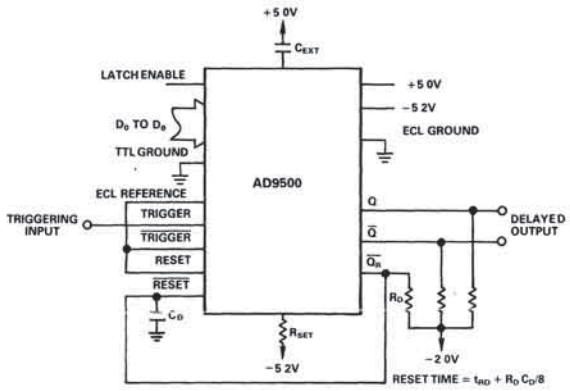
The minimum configuration uses only one of the TRIGGER inputs. The other is connected to the ECL reference midpoint, ECL_{REF}. This allows the AD9500 to be triggered with standard 10K or 10KH ECL signals. Once a triggering event occurs, the Q output will go into the logic HIGH state, and the $\overline{Q}$ output will go into the logic LOW state after the programmed delay. The Q output is then used to drive the RESET input, causing the AD9500 to reset itself. The result is a delayed output pulse which is only as wide as the reset propagation delay (t_{RD}).



Single Input – Minimum Timing Configuration

EXTENDED OUTPUT PULSE WIDTHS

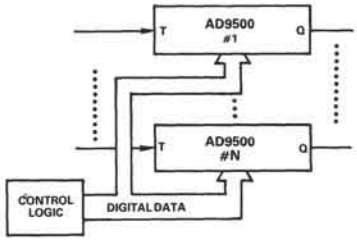
The extended pulse configuration is similar to the minimum configuration. The difference here is that the output pulse width has been extended. Operation is identical in terms of triggering the AD9500; the functional difference is in the resetting circuit. In this case the $\overline{Q_R}$ output is used to drive the $\overline{RESET}$ input through a resistor/capacitor charging network. The charging network will cause the signal at the $\overline{RESET}$ input to fall more slowly, which will extend the output pulse width. An added benefit of the extended pulse width configurations is that both the Q and the $\overline{Q}$ outputs are completely free for other uses.



Extended Output Pulse Width Configuration

MULTICHANNEL DESKEWING

Perhaps the most appropriate use of the AD9500 is in multiple delay matching applications. Slight differences in impedance and cable length can create large timing skews within a high-speed system. Much of this skew can be eliminated by running each signal through an AD9500. With one line used as a standard, the programmed delays of the other AD9500s are adjusted to eliminate the timing skews. With the very fine timing adjustments possible from the AD9500 (as small as 10ps), nearly any high-speed system should be able to automatically adjust itself to extremely tight tolerances.

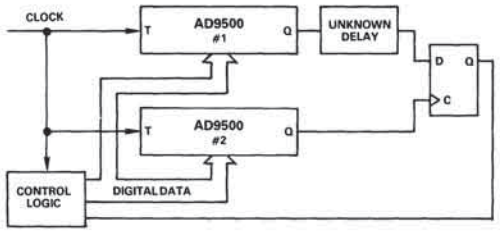


Multiple Delay Matching

MEASURING UNKNOWN DELAYS

Two AD9500s can be combined to measure delays with a high degree of precision. One AD9500 is set with little or no programmed delay, and its output is used to drive the unknown delay circuit, which in turn drives the input of a "D" type flipflop. The second AD9500 is triggered along with the first, and its output provides a clocking signal for the flipflop. The programmed delay of the second AD9500 is then varied to detect the output edge from the unknown delay circuit.

Detecting the output edge is relatively straightforward. If the programmed delay through the second AD9500 is too long, the flipflop output will be at logic HIGH. If, on the other hand, the programmed delay through the second AD9500 is too short, the flipflop output will be at logic LOW. When the programmed delay is properly adjusted, the flipflop will likely bounce between logic HIGH and logic LOW. The digital code value used to create the second programmed delay is a direct indication of the delay through the unknown circuit. The most accurate results can only be attained by calibrating the system without the unknown delay circuit in place.

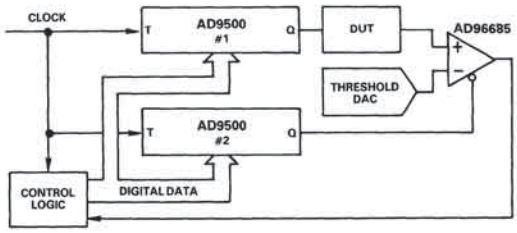


Measuring Unknown Delays

MEASURING HIGH-SPEED AC WAVEFORMS

The same circuitry used to measure unknown delays can be extended to measure the time response of high-speed ac waveforms. With the addition of a digital-to-analog converter and an analog comparator, the circuit functions very much like the previous application. The DAC sets a threshold level which drives one of the differential comparator inputs. The other comparator input is driven by the device under test (DUT). The output of the first AD9500 causes the DUT to produce an output. The second AD9500, which is also triggered along with the first AD9500, strobes the comparator latch enable.

If the DUT output is greater than the DAC threshold when the comparator is latched, the comparator output will be at logic HIGH. If the output is below the DAC threshold, the comparator will be at logic LOW. The programmed delay setting of the second AD9500 is adjusted to the point where the DUT output equals the DAC threshold. By varying the DAC threshold level and adjusting the second AD9500 programmed delay, a point by point reconstruction of the ac waveform can be created.

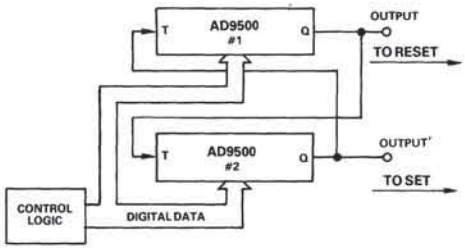


Measuring ac Waveforms

PROGRAMMABLE OSCILLATOR

Another interesting use of the AD9500 is in a digitally programmable oscillator. The highly accurate delays generated by the AD9500 can be exploited to create a ring oscillator with variable duty cycle. The delayed output of the first AD9500 is used to drive the TRIGGER input of the second AD9500. The output of the second AD9500, in turn, is used to drive the TRIGGER input of the first AD9500. Together the two devices will alternately trigger each other creating two pulse chains on the outputs.

The total delay through both AD9500s combined, determines the period of the oscillation frequency. The duty cycle can be controlled by using the outputs to drive the SET and RESET inputs of a flipflop. The total delay through the first AD9500 will control the flipflop logic LOW output pulse width, and the second AD9500 will control the flipflop logic HIGH output pulse width.



Ring Oscillator

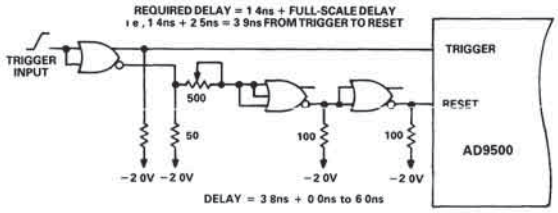
LAYOUT CONSIDERATIONS

The AD9500 is a precision timing device, and as such high-frequency design techniques must be employed to achieve the best performance. The use of a low impedance ground plane is particularly important. Ideally the ground plane should be on the component side of the layout and extend under the AD9500, to shield it from system timing signals. Sockets pose a special problem for a circuit like the AD9500 because of the additional inter-lead capacitance they create. If sockets must be used, pin sockets are generally preferred. Power supply decoupling is also critical to a high-speed design; a 0.1μF ceramic capacitor and a 0.01μF mica capacitor for both power supplies should be very effective. DAC threshold stability can be improved by decoupling the OFFSET ADJUST pin to +5.0V (note that this will lengthen the DAC settling time, t_{DAC}).

9

100MHz TRIGGERING

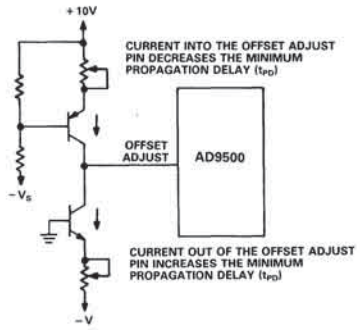
The AD9500 can be triggered at rates above 100MHz. This is accomplished by resetting the AD9500 shortly after it is triggered, which also tends to generate an extremely narrow output pulse. The delay circuit between the trigger input and the reset input provides the variable delay required for various configurations from 2.5ns full-scale to over 10ns full-scale (greater than 10ns total delay precludes 100MHz triggering).



Reset Holdoff for High-Speed Triggering

DELAY OFFSET ADJUSTMENTS

As the full-scale delay is increased, a component of the minimum propagation delay also increases. This is caused by the additional time required by the ramp (now with a much "flatter" slope) to fall below the DAC threshold corresponding to the minimum propagation delay (t_{PD}). One means of decreasing the minimum propagation delay (when the full-scale delay, set by R_{SET} and C_{EXT} is large) is to offset the internal DAC threshold toward the initial ramp levels, thus reducing the time for the internal ramp to cross the threshold once the AD9500 is triggered.



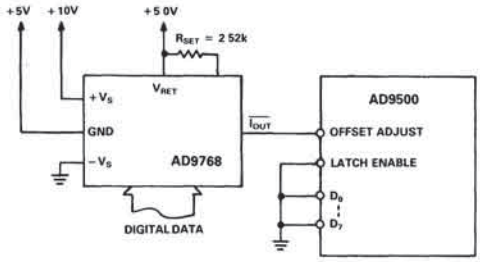
The Offset Adjust Pin Can Be Used to Match Several AD9500s

The DAC levels are offset toward the initial ramp level by injecting a small current into the offset adjust pin. Note, however, that the ramp start-up region is less linear than the later portions of the ramp, which is the primary reason for the built-in offset. If the minimum propagation delay is kept above 5ns (the linear portion of the ramp), no significant degradation in linearity should result. This concept can be extended to match the actual propagation delays of several AD9500s, by injecting or sinking a small current (<2mA) into or out of each of the OFFSET ADJUST pins.

GENERAL PERFORMANCE ENCHANCEMENTS

High-speed operation is generally more consistent if C_{EXT} is kept small (i.e., no external capacitor) to maintain small discharge time constants. Integral linearity, however, benefits from larger values of C_{EXT} by buffering small system spikes and surges. Another means of improving integral linearity is to draw a small current (≈200μA) out of the OFFSET ADJUST pin with a 47kΩ pull-down resistor. This has the effect of moving the internal DAC reference levels into a relatively more linear region of the ramp. This technique is generally only useful for small full-scale delay configurations. Its use with larger full-scale delays will extend the minimum propagation delay (t_{PD}). A pull-up resistor to +5.0V creates the opposite effect by reducing the minimum propagation delay (t_{PD}) at the expense of increased reset propagation delay (t_{RD}) and degraded linearity (see OFFSET matching circuit).

An external DAC can be used with the AD9500 for increased resolution and higher update rates. For the most part, a standard ECL DAC, operating between +5.0V and ground, should work with the AD9500. The output of the external DAC must be connected to the OFFSET ADJUST pin of the AD9500 with the internal DAC turned off (D_0 thru D_7 at logic LOW). For normal operation, the external DAC output should range from 0mA to −2mA (sinking).



Operation with External DAC

Temperature Transducers
Contents

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Selection Guide	10 – 3
Orientation	10 – 4
AC2626 – General Purpose Temperature Probe	10 – 5
AD590 – Two-Terminal IC Temperature Transducer	10 – 7
AD592 – Low Cost, Precision IC Temperature Transducer	10 – 17

10

Selection Guide
Temperature Transducers

Model	Output Current µA/K	Calibration Error °C	Nonlinearity °C	Package	Page
AC2626	1	0.5	0.3	Stainless steel probe	10 – 5
AD590	1	1.7	0.3	Hermetic can or probe-compatible ceramic	10 – 7
AD592	1	0.8	0.15	Plastic package	10 – 17

Orientation
Temperature Transducers

The devices in this section are two-terminal monolithic integrated circuits designed to measure temperatures within the range −55°C to +150°C. When +4V to +30V of excitation voltage is applied, they act as current sources that provide an output proportional to absolute temperature, 1μA/K. Expressed in degrees Celsius (T_C),

$$I = 1\mu A/^{\circ}C \cdot T_C + 273.2\mu A$$

Current sources have a number of advantages: they are based on a linear relationship and are highly repeatable; the current is independent of voltage drops, voltage noise and common-mode voltage – and practically independent of excitation voltage; the current can be translated to a voltage at a remote destination via an appropriate value of resistance (V = I R) – and simple offsetting circuitry (if necessary).

They are easy to use; they don't require linearization circuitry, high-precision voltage amplifiers, resistance-measuring circuitry or cold-junction compensation. Indeed, they are themselves widely used for cold-junction compensation of thermocouple circuitry.

There are many other applications, including appliance temperature sensing, automotive temperature measurement and control, HVAC (heating, ventilating and air conditioning) system monitoring, industrial temperature control, board-level electronics temperature diagnostics, temperature readout options in instrumentation and temperature-correction circuitry for precision electronics.

AD592 Low-Cost Precision IC Temperature Transducer
The AD592 is a low-cost, plastic packaged device with an operating temperature range of −25°C to +105°C and precalibrated accuracy (using laser wafer-trimming) to within 0.5°C (AD592CN) at +25°C. Its specified nonlinearity (maximum deviation from a best straight line) is 0.35°C maximum over temperature and less than 0.15°C from 0 to +70°C.

AD590 IC Temperature Transducer
The AD590 is similar in principle to the AD592 but is encased in a choice of a hermetically sealed metal can and a probe-compatible ceramic sensor package. Its maximum temperature range for rated performance is −55°C to +150°C, with maximum nonlinearity of 0.3°C over the temperature range (AD590M).

AC2626 General-Purpose Temperature Probe
The AC2626 is a stainless steel tubular probe containing an AD590 chip, with specifications generally similar to those of the AD590. The probe has an outside diameter of 3/16" (4.76mm); it is available in 6" (152.4mm) and 4" (101.6mm) lengths and has 3-foot Teflon-coated lead wires.

The probe is designed for immersion in both liquids and gases and can also be used for temperature measurements in refrigeration and general temperature monitoring. Its applications include flow-rate measurement, level detection of fluids and anemometry.

For measurements in pipes or other closed vessels, a compression fitting (AC2629) is available. It may be applied anywhere along the probe and is available in a choice of brass and stainless steel.

RELATED PRODUCTS
A variety of digital panel instruments are available for use in temperature monitoring. They can be found in the section on Digital Panel Instruments. The AD2040* low-cost, 3-digit temperature indicator and the AD2038* 6-channel digital scanning thermometer may be of especial interest.

For interfacing temperature measurements to systems, signal-conditioning products in wide variety of architectures and physical forms can be found in the section on signal conditioning; for the circuit designer, suitable operational, instrumentation and isolation amplifiers can be found in the respective sections.

For background information, a valuable aid to understanding, design, and applications is the *Transducer Interfacing Handbook*, published by Analog Devices (1980). It is available for $14.50 (hard cover) from P. O. Box 796, Norwood, MA 02062.

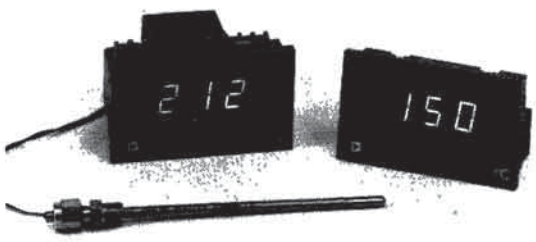
***Data sheets available upon request.**

ANALOG DEVICES

General Purpose Temperature Probe

AC2626

FEATURES
- Linear Current Output: 1μA/K
- Wide Range: -55°C to +150°C
- Laser Trimmed Sensor (AD590) to ±1.0°C Calibration Accuracy (AC2626L)
- Excellent Linearity: ±0.4°C Over Full Range (AC2626L)
- 6 Inch or 4 Inch Standard, Stainless Steel Sheath
- 3/16 Inch in Outside Diameter
- 3 Feet Teflon Coated Lead Wire
- Wide Power Supply Range +4V to +30V
- Low Cost
- Fast Response: 2 Seconds (In Stirred Water)
- Sensor Isolated From Sheath



PRODUCT DESCRIPTION

The AC2626 is a stainless steel tubular probe measuring 3/16 inch (4.76mm) in outside diameter and is available in 6 inch (152.4mm) or 4-inch (101.6mm) lengths. The probe is available in linearity grades of 0.3°C, 0.4°C, 0.8°C or 1.5°C.

The probe is designed for both liquid and gaseous immersion applications as well as temperature measurements in refrigeration or any general temperature monitoring application.

For taking measurements in pipes or other closed vessels, the AC2629 compression fitting is available. The AC2629 may be applied anywhere along the probe and is supplied in two materials. The low cost AC2629B is constructed of brass and the higher priced AC2629SS is made of stainless steel.

PRODUCT HIGHLIGHTS

The AC2626 is based on the AD590 temperature transducer, a two terminal integrated circuit which produces an output current linearly proportional to absolute temperature.

Costly linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AC2626.

Due to the high impedance current output of the AD590, the AC2626 is particularly useful in remote sensing applications, because of its insensitivity to voltage drops over lines. The output characteristics also make the AC2626 easy to multiplex.

In addition to temperature measurement, applications include temperature compensation, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry.

DIRECT INTERFACE PRODUCTS

For display and/or control applications, two companion products are available. The AD2038, 6 channel digital thermometer, and the AD2040, low cost temperature indicator, were designed to be used in conjunction with the AC2626.

1. The AD2038 is a low cost, ac line powered 6 channel digital scanning thermometer designed to interface to printers, computers, serial data transmitters, etc., for display, control, logging or transmission of multi-point temperature data. Channel selection is made via three methods: manual, using the switch provided on the front; auto/scan, where the AD2038 cycling on an internal clock can continually scan the six input channels or external selection, where control inputs provided on the rear connector enable channel selection via external BCD coding.
2. The AD2040 is a low cost, 3 digit temperature indicator. An internal precision voltage reference, resistor network and span and zero adjusts allow the AD2040 to read out directly in °C, °F, K or R. User selectable readout as well as all other connections, i.e., +5V dc power and AC2626 interface are all made via the terminal block on the rear.

APPLICATION HINTS

1. Under all operating conditions, a minimum 4V dc must be present across the AC2626.
2. Use of twisted pair wiring is recommended, particularly for remote applications or in high noise environments. Shielded wire is desirable in severe noise environments.
3. For the lowest cost, the J and K grades are recommended. Where probe interchangeability is desired, grade L is recommended.

SPECIFICATIONS (typical @ +25°C and +5V unless otherwise specified)

MODEL	AC2626J	AC2626K	AC2626L	AC2626M
ABSOLUTE MAXIMUM RATINGS[1]				
Forward Voltage (V_S)	+44V	*	*	*
Reverse Voltage (V_S)	-20V	*	*	*
Breakdown Voltage (Case to Leads)	±200V	*	*	*
Rated Performance Temp. Range	-55°C to +150°C	*	*	*
Storage Temperature Range	-60°C to +160°C	*	*	*
POWER SUPPLY				
Operating Voltage Range	+4V to +30V	*	*	*
OUTPUT				
Nominal Current Output @ +25°C (298.2°K)	298.2µA	*	*	*
Nominal Temperature Coefficient	1µA/°C	*	*	*
Calibration Error @ +25°C	±5.0°C max	±2.5°C max	±1.0°C max	±0.5°C max
Absolute Error (over rated performance temperature range)				
Without External Calibration Adjustment	±10.0°C max	±5.5°C max	±3.0°C max	±1.7°C max
With +25°C Calibration Error Set to Zero	±3.0°C max	±2.0°C max	±1.6°C max	±1.0°C max
Nonlinearity	±1.5°C max	±0.8°C max	±0.4°C max	±0.3°C max
Repeatability[2]	0.1°C	*	*	*
Long Term Drift[3]	0.1°C max/month	*	*	*
Time Constant[4] (in stirred water)	2 sec.	*	*	*
Current Noise	40pA$\sqrt{Hz}$	*	*	*
Power Supply Rejection				
+4V≤V_S≤+5V	0.5µA/V	*	*	*
+5V≤V_S≤+15V	0.2µA/V	*	*	*
+15V≤V_S≤+30V	0.1µA/V	*	*	*
Electrical Turn-On Time	20µs	*	*	*
+ Lead Color	yellow	orange	blue	green

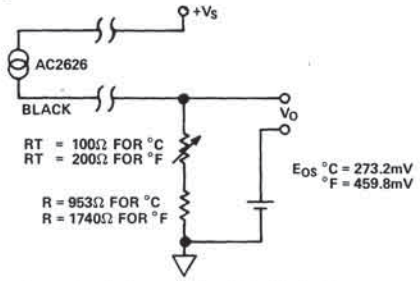
ORDERING GUIDE

AC2626
- GRADE: J, K, L — ENTER
- LENGTH: 4, 6 — ENTER

AC2629
- BRASS: B
- TYPE 316 STAINLESS: SS — ENTER

NOTES
[1] Maximum safe recommended pressure 7500psi (5.17×10^4 Kpa).
[2] Maximum deviation between +25°C readings after temperature cycling between -55°C and +150°C, guaranteed, not tested.
[3] Conditions: constant +5V, constant +125°C, guaranteed, not tested.
[4] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.
*Specifications same as AC2626J.
Specifications subject to change without notice.

CALIBRATION



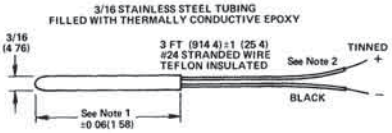
For most applications, a single point calibration is sufficient. With the probe at a known temperature, adjust R_T so that V_O corresponds to the known temperature.

If more detailed information is desired, see the AD590 data sheet and application note.

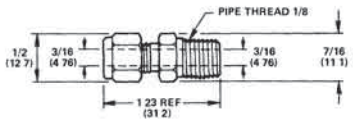
MECHANICAL OUTLINE

Dimensions shown in inches and (mm).

AC2626



AC2629



NOTE 1 Probes are available in 4 inch or 6-inch lengths
NOTE 2 + lead wire is color coded J, yellow, K, orange, L, blue.
NOTE 3 When assembling compression fitting (AC2629) to probe, tighten the 1/2" nut 3/4's of a turn from finger tight

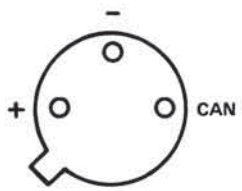
ANALOG DEVICES

Two-Terminal IC Temperature Transducer

AD590*

FEATURES
Linear Current Output: 1μA/K
Wide Range: -55°C to +150°C
Probe Compatible Ceramic Sensor Package
Two-Terminal Device: Voltage In/Current Out
Laser Trimmed to ±0.5°C Calibration Accuracy (AD590M)
Excellent Linearity: ±0.3°C Over Full Range (AD590M)
Wide Power Supply Range: +4V to +30V
Sensor Isolation from Case
Low Cost

AD590 PIN DESIGNATIONS



BOTTOM VIEW

PRODUCT DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. For supply voltages between +4V and +30V the device acts as a high impedance, constant current regulator passing 1μA/K. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2K (+25°C).

The AD590 should be used in any temperature sensing application below +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, biasing proportional to absolute temperature, flow rate measurement, level detection of fluids and anemometry. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

***Covered by Patent No. 4,123,698**

PRODUCT HIGHLIGHTS

1. The AD590 is a calibrated two terminal temperature sensor requiring only a dc voltage supply (+4V to +30V). Costly transmitters, filters, lead wire compensation and linearization circuits are all unnecessary in applying the device.
2. State-of-the-art laser trimming at the wafer level in conjunction with extensive final testing insures that AD590 units are easily interchangeable.
3. Superior interference rejection results from the output being a current rather than a voltage. In addition, power requirements are low (1.5mW's @ 5V @ +25°C). These features make the AD590 easy to apply as a remote sensor.
4. The high output impedance (>10MΩ) provides excellent rejection of supply voltage drift and ripple. For instance, changing the power supply from 5V to 10V results in only a 1μA maximum current change, or 1°C equivalent error.
5. The AD590 is electrically durable: it will withstand a forward voltage up to 44V and a reverse voltage of 20V. Hence, supply irregularities or pin reversal will not damage the device.

SPECIFICATIONS (@ +25°C and V_S = 5V unless otherwise noted)

Model	AD590J			AD590K			Units
	Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ to E−)			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			**±5.0**			**±2.5**	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			**±10**			**±5.5**	°C
With +25°C Calibration Error Set to Zero			**±3.0**			**±2.0**	°C
Nonlinearity			**±1.5**			**±0.8**	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA/$\sqrt{Hz}$
Power Supply Rejection							
+4V≤V_S≤+5V		0.5			0.5		μA/V
+5V≤V_S≤+15V		0.2			0.2		μA/V
+15V≤V_S≤+30V		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4] (Reverse Voltage = 10V)		10			10		pA
PACKAGE OPTION[5]							
TO-52 (H-03A)		AD590JH			AD590KH		
Flat Pack (F-2A)		AD590JF			AD590KF		

NOTES

[1]The AD590 has been used at −100°C and +200°C for short periods of measurement with no physical damage to the device. However, the absolute errors specified apply to only the rated performance temperature range.

[2]Maximum deviation between +25°C readings after temperature cycling between −55°C and +150°C; guaranteed not tested.

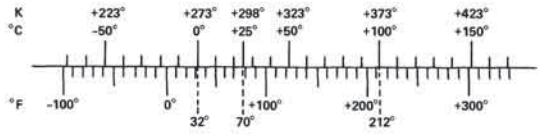
[3]Conditions: constant +5V, constant +125°C; guaranteed, not tested.

[4]Leakage current doubles every 10°C.

[5]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



TEMPERATURE SCALE CONVERSION EQUATIONS

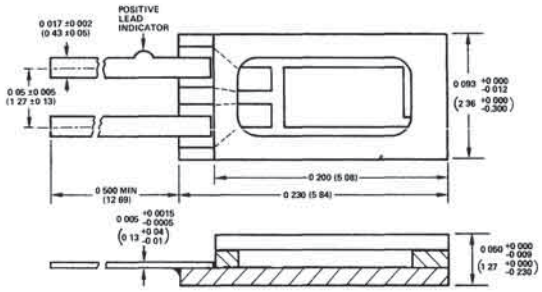
$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

Model	AD590L			AD590M			
	Min	Typ	Max	Min	Typ	Max	Units
ABSOLUTE MAXIMUM RATINGS							
Forward Voltage (E+ to E−)			+44			+44	Volts
Reverse Voltage (E+ to E−)			−20			−20	Volts
Breakdown Voltage (Case to E+ or E−)			±200			±200	Volts
Rated Performance Temperature Range[1]	−55		+150	−55		+150	°C
Storage Temperature Range[1]	−65		+155	−65		+155	°C
Lead Temperature (Soldering, 10 sec)			+300			+300	°C
POWER SUPPLY							
Operating Voltage Range	+4		+30	+4		+30	Volts
OUTPUT							
Nominal Current Output @ +25°C (298.2K)		298.2			298.2		μA
Nominal Temperature Coefficient		1			1		μA/K
Calibration Error @ +25°C			**±1.0**			**±0.5**	°C
Absolute Error (over rated performance temperature range)							
Without External Calibration Adjustment			**±3.0**			**±1.7**	°C
With +25°C Calibration Error Set to Zero			**±1.6**			**±1.0**	°C
Nonlinearity			**±0.4**			**±0.3**	°C
Repeatability[2]			±0.1			±0.1	°C
Long Term Drift[3]			±0.1			±0.1	°C
Current Noise		40			40		pA$\sqrt{\text{Hz}}$
Power Supply Rejection							
$+4V \leq V_S \leq +5V$		0.5			0.5		μA/V
$+5V \leq V_S \leq +15V$		0.2			0.2		μA/V
$+15V \leq V_S \leq +30V$		0.1			0.1		μA/V
Case Isolation to Either Lead		10^{10}			10^{10}		Ω
Effective Shunt Capacitance		100			100		pF
Electrical Turn-On Time		20			20		μs
Reverse Bias Leakage Current[4] (Reverse Voltage = 10V)		10			10		pA
PACKAGE OPTION[5]							
TO-52 (H-03A)		AD590LH			AD590MH		
Flat Pack (F-2A)		AD590LF			AD590MF		

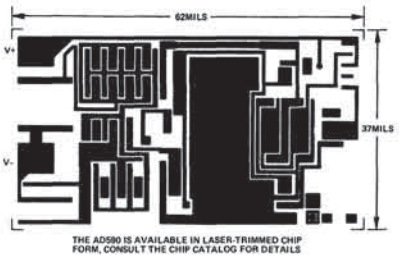
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The 590H has 60μ inches of gold plating on its Kovar leads and Kovar header. A resistance welder is used to seal the nickel cap to the header. The AD590 chip is eutectically mounted to the header and ultrasonically bonded to with 1 MIL aluminum wire. Kovar composition: 53% iron nominal; 29% ±1% nickel; 17% ±1% cobalt; 0.65% manganese max; 0.20% silicon max; 0.10% aluminum max; 0.10% magnesium max; 0.10% zirconium max; 0.10% titanium max; 0.06% carbon max.



FLAT-PACK PACKAGE: DESIGNATION "F"

The 590F is a ceramic package with gold plating on its Kovar leads, Kovar lid, and chip cavity. Solder of 80/20 Au/Sn composition is used for the 1.5 mil thick solder ring under the lid. The chip cavity has a nickel underlay between the metalization and the gold plating. The AD590 chip is eutectically mounted in the chip cavity at 410°C and ultrasonically bonded to with 1 mil aluminum wire. Note that the chip is in direct contact with the ceramic base, not the metal lid.



Metalization Diagram

CIRCUIT DESCRIPTION[1]

The AD590 uses a fundamental property of the silicon transistors from which it is made to realize its temperature proportional characteristic: if two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in their base-emitter voltages will be (kT/q)(In r). Since both k, Boltzman's constant and q, the charge of an electron, are constant, the resulting voltage is directly proportional to absolute temperature (PTAT).

In the AD590, this PTAT voltage is converted to a PTAT current by low temperature coefficient thin film resistors. The total current of the device is then forced to be a multiple of this PTAT current. Referring to Figure 1, the schematic diagram of the AD590, Q8 and Q11 are the transistors that produce the PTAT voltage. R5 and R6 convert the voltage to current. Q10, whose collector current tracks the collector currents in Q9 and Q11, supplies all the bias and substrate leakage current for the rest of the circuit, forcing the total current to be PTAT. R5 and R6 are laser trimmed on the wafer to calibrate the device at +25°C.

Figure 2 shows the typical V–I characteristic of the circuit at +25°C and the temperature extremes.

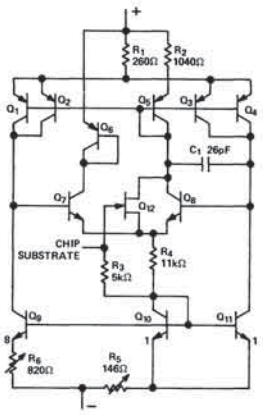


Figure 1. Schematic Diagram

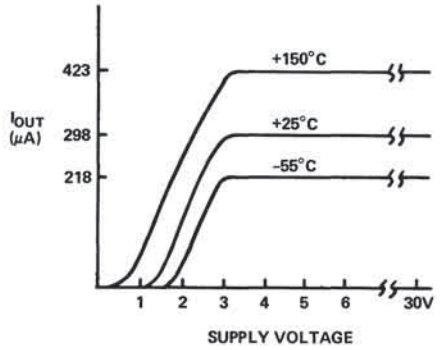


Figure 2. V–I Plot

[1] For a more detailed circuit description see M.P. Timko, "A Two-Terminal IC Temperature Transducer," IEEE J. Solid State Circuits, Vol. SC-11, p. 784-788, Dec. 1976.

Understanding the AD590 Specifications

EXPLANATION OF TEMPERATURE SENSOR SPECIFICATIONS

The way in which the AD590 is specified makes it easy to apply in a wide variety of different applications. It is important to understand the meaning of the various specifications and the effects of supply voltage and thermal environment on accuracy.

The AD590 is basically a PTAT (proportional to absolute temperature)[1] current regulator. That is, the output current is equal to a scale factor times the temperature of the sensor in degrees Kelvin. This scale factor is trimmed to 1μA/K at the factory, by adjusting the indicated temperature (i.e. the output current) to agree with the actual temperature. This is done with 5V across the device at a temperature within a few degrees of 25°C (298.2K). The device is then packaged and tested for accuracy over temperature.

CALIBRATION ERROR

At final factory test the difference between the indicated temperature and the actual temperature is called the calibration error. Since this is a scale factor error, its contribution to the total error of the device is PTAT. For example, the effect of the 1°C specified maximum error of the AD590L varies from 0.73°C at -55°C to 1.42°C at 150°C. Figure 3 shows how an exaggerated calibration error would vary from the ideal over temperature.

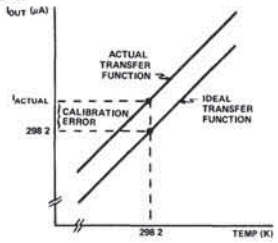


Figure 3. Calibration Error vs. Temperature

The calibration error is a primary contributor to maximum total error in all AD590 grades. However, since it is a scale factor error, it is particularly easy to trim. Figure 4 shows the most elementary way of accomplishing this. To trim this circuit the temperature of the AD590 is measured by a reference temperature sensor and R is trimmed so that V_T = 1mV/K at that temperature. Note that when this error is trimmed out at one temperature, its effect is zero over the entire temperature range. In most applications there is a current to voltage conversion resistor (or, as with a current input ADC, a reference) that can be trimmed for scale factor adjustment.

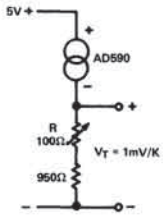


Figure 4. One Temperature Trim

[1] T(°C) = T(K) -273.2; Zero on the Kelvin scale is "absolute zero"; there is no lower temperature.

ERROR VERSUS TEMPERATURE: WITH CALIBRATION ERROR TRIMMED OUT

Each AD590 is also tested for error over the temperature range with the calibration error trimmed out. This specification could also be called the "variance from PTAT" since it is the maximum difference between the actual current over temperature and a PTAT multiplication of the actual current at 25°C. This error consists of a slope error and some curvature, mostly at the temperature extremes. Figure 5 shows a typical AD590K temperature curve before and after calibration error trimming.

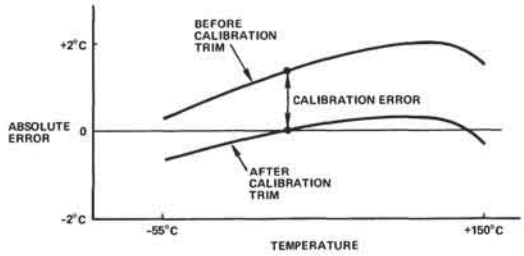


Figure 5. Effect of Scale Factor Trim on Accuracy

ERROR VERSUS TEMPERATURE: NO USER TRIMS

Using the AD590 by simply measuring the current, the total error is the "variance from PTAT" described above plus the effect of the calibration error over temperature. For example the AD590L maximum total error varies from 2.33°C at -55°C to 3.02°C at 150°C. For simplicity, only the larger figure is shown on the specification page.

NONLINEARITY

Nonlinearity as it applies to the AD590 is the maximum deviation of current over temperature from a best-fit straight line. The nonlinearity of the AD590 over the -55°C to +150°C range is superior to all conventional electrical temperature sensors such as thermocouples, RTD's and thermistors. Figure 6 shows the nonlinearity of the typical AD590K from Figure 5.

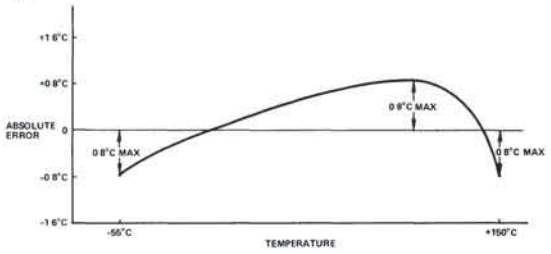


Figure 6. Nonlinearity

Figure 7A shows a circuit in which the nonlinearity is the major contributor to error over temperature. The circuit is trimmed by adjusting R_1 for a 0V output with the AD590 at 0°C. R_2 is then adjusted for 10V out with the sensor at 100°C. Other pairs of temperatures may be used with this procedure as long as they are measured accurately by a reference sensor. Note that for +15V output (150°C) the V+ of the op amp must be greater than 17V. Also note that V- should be at least -4V: if V- is ground there is no voltage applied across the device.

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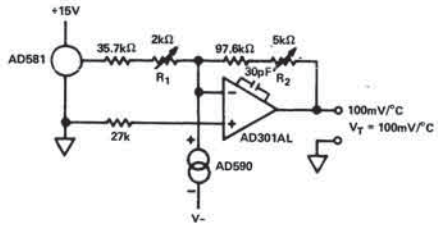


Figure 7A. Two Temperature Trim

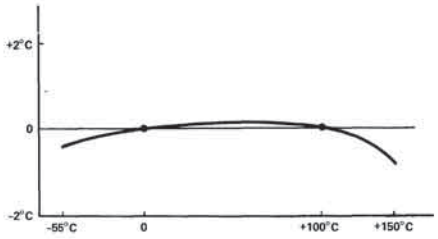


Figure 7B. Typical Two-Trim Accuracy

VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection specifications show the maximum expected change in output current versus input voltage changes. The insensitivity of the output to input voltage allows the use of unregulated supplies. It also means that hundreds of ohms of resistance (such as a CMOS multiplexer) can be tolerated in series with the device.

It is important to note that using a supply voltage other than 5V does not change the PTAT nature of the AD590. In other words, this change is equivalent to a calibration error and can be removed by the scale factor trim (see previous page).

The AD590 specifications are guaranteed for use in a low thermal resistance environment with 5V across the sensor. Large changes in the thermal resistance of the sensor's environment will change the amount of self-heating and result in changes in the output which are predictable but not necessarily desirable.

The thermal environment in which the AD590 is used determines two important characteristics: the effect of self heating and the response of the sensor with time.

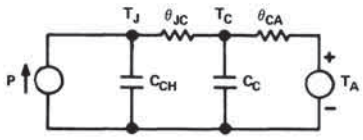


Figure 8. Thermal Circuit Model

Figure 8 is a model of the AD590 which demonstrates these characteristics. As an example, for the TO-52 package, θ_{JC} is the thermal resistance between the chip and the case, about 26°C/watt. θ_{CA} is the thermal resistance between the case and its surroundings and is determined by the characteristics of the thermal connection. Power source P represents the power dissipated on the chip. The rise of the junction temperature, T_J, above the ambient temperature T_A is:

$$T_J - T_A = P\,(\theta_{JC} + \theta_{CA}). \qquad \text{Eq. 1}$$

Table I gives the sum of θ_{JC} and θ_{CA} for several common thermal media for both the "H" and "F" packages. The heat-sink used was a common clip-on. Using Equation 1, the temperature rise of an AD590 "H" package in a stirred bath at +25°C, when driven with a 5V supply, will be 0.06°C. However, for the same conditions in still air the temperature rise is 0.72°C. For a given supply voltage, the temperature rise varies with the current and is PTAT. Therefore, if an application circuit is trimmed with the sensor in the same thermal environment in which it will be used, the scale factor trim compensates for this effect over the entire temperature range.

MEDIUM	$\theta_{JC} + \theta_{CA}$ (°C/watt)		τ (sec) (Note 3)	
	H	F	H	F
Aluminum Block	30	10	0.6	0.1
Stirred Oil[1]	42	60	1.4	0.6
Moving Air[2]				
With Heat Sink	45	—	5.0	—
Without Heat Sink	115	190	13.5	10.0
Still Air				
With Heat Sink	191	—	108	—
Without Heat Sink	480	650	60	30

[1] Note: τ is dependent upon velocity of oil; average of several velocities listed above.

[2] Air velocity ≅ 9ft/sec.

[3] The time constant is defined as the time required to reach 63.2% of an instantaneous temperature change.

Table I. Thermal Resistances

The time response of the AD590 to a step change in temperature is determined by the thermal resistances and the thermal capacities of the chip, C_{CH}, and the case, C_C. C_{CH} is about 0.04 watt-sec/°C for the AD590. C_C varies with the measured medium since it includes anything that is in direct thermal contact with the case. In most cases, the single time constant exponential curve of Figure 9 is sufficient to describe the time response, T(t). Table I shows the effective time constant, τ, for several media.

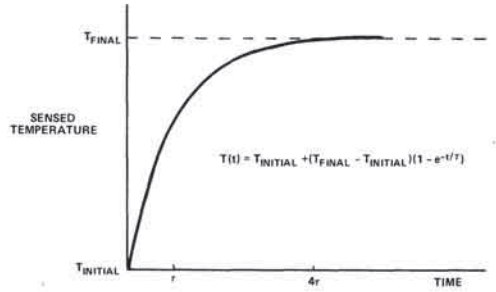


Figure 9. Time Response Curve

GENERAL APPLICATIONS

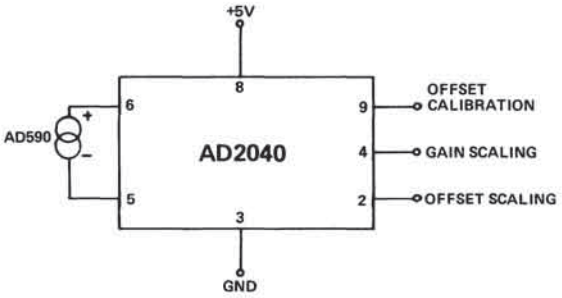


Figure 10. Variable Scale Display

Figure 10 demonstrates the use of a low-cost Digital Panel Meter for the display of temperature on either the Kelvin, Celsius or Fahrenheit scales. For Kelvin temperature Pins 9, 4 and 2 are grounded; and for Fahrenheit temperature Pins 4 and 2 are left open.

The above configuration yields a 3 digit display with 1°C or 1°F resolution, in addition to an absolute accuracy of ±2.0°C over the -55°C to +125°C temperature range if a one-temperature calibration is performed on an AD590K, L, or M.

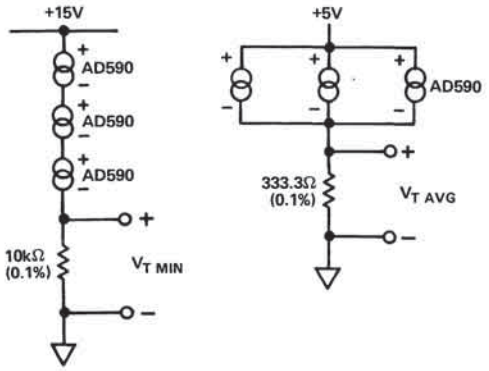


Figure 11. Series & Parallel Connection

Connecting several AD590 units in series as shown in Figure 11 allows the minimum of all the sensed temperatures to be indicated. In contrast, using the sensors in parallel yields the average of the sensed temperatures.

The circuit of Figure 12 demonstrates one method by which differential temperature measurements can be made. R_1 and R_2 can be used to trim the output of the op amp to indicate a desired temperature difference. For example, the inherent offset between the two devices can be trimmed in. If V+ and V- are radically different, then the difference in internal dissipation will cause a differential internal temperature rise. This effect can be used to measure the ambient thermal resistance seen by the sensors in applications such as fluid level detectors or anemometry.

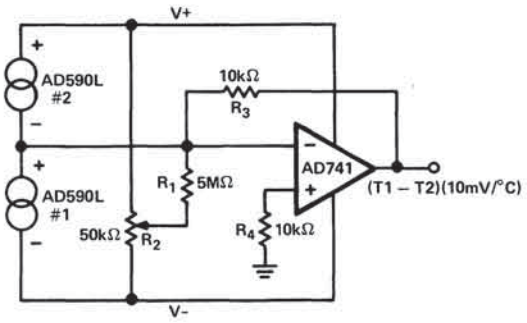


Figure 12. Differential Measurements

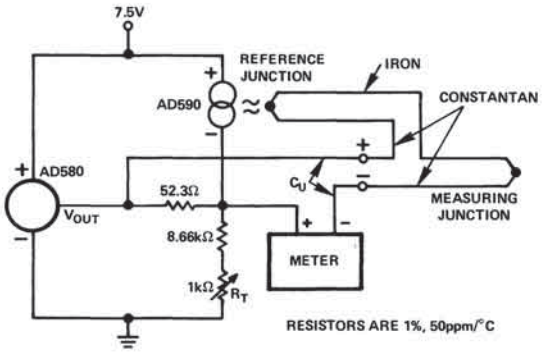


Figure 13. Cold Junction Compensation Circuit for Type J Thermocouple

Figure 13 is an example of a cold junction compensation circuit for a Type J Thermocouple using the AD590 to monitor the reference junction temperature. This circuit replaces an ice-bath as the thermocouple reference for ambient temperatures between +15°C and +35°C. The circuit is calibrated by adjusting R_T for a proper meter reading with the measuring junction at a known reference temperature and the circuit near +25°C. Using components with the T.C.'s as specified in Figure 13, compensation accuracy will be within ±0.5°C for circuit temperatures between +15°C and +35°C. Other thermocouple types can be accommodated with different resistor values. Note that the T.C.'s of the voltage reference and the resistors are the primary contributors to error.

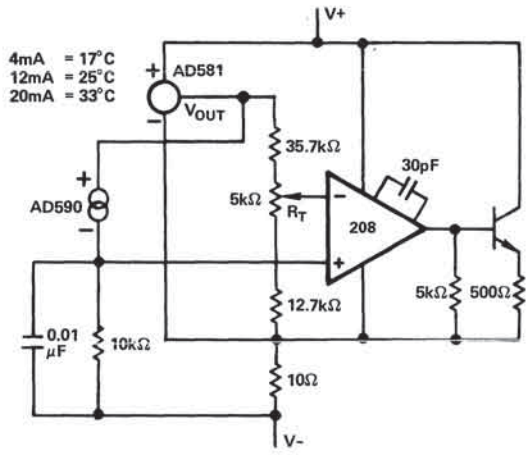


Figure 14. 4 to 20mA Current Transmitter

Figure 14 is an example of a current transmitter designed to be used with 40V, 1kΩ systems; it uses its full current range of 4mA to 20mA for a narrow span of measured temperatures. In this example the 1μA/K output of the AD590 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. R_T is trimmed for proper reading at an intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD590 may be chosen.

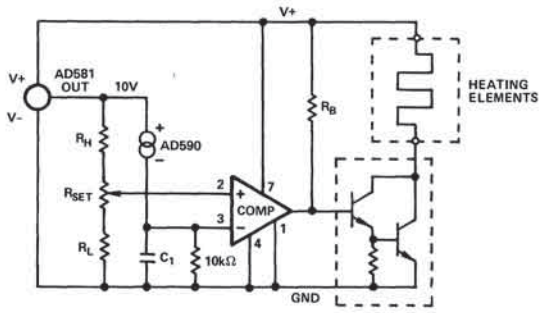


Figure 15. Simple Temperature Control Circuit

Figure 15 is an example of a variable temperature control circuit (thermostat) using the AD590. R_H and R_L are selected to set the high and low limits for R_{SET}. R_{SET} could be a simple pot, a calibrated multi-turn pot or a switched resistive divider. Powering the AD590 from the 10V reference isolates the AD590 from supply variations while maintaining a reasonable voltage (~7V) across it. Capacitor C_1 is often needed to filter extraneous noise from remote sensors. R_B is determined by the β of the power transistor and the current requirements of the load.

Figure 16 shows how the AD590 can be configured with an 8-bit DAC to produce a digitally controlled set point. This

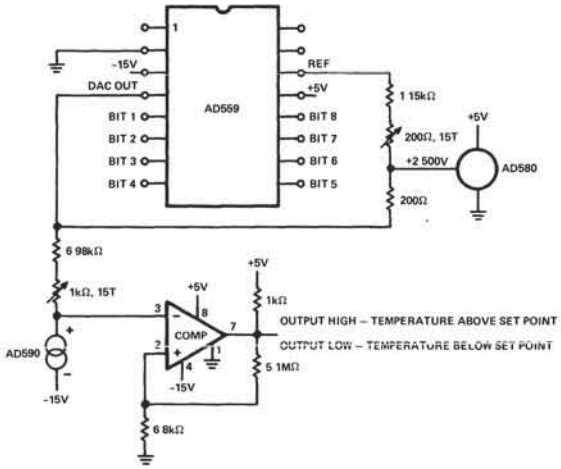


Figure 16. DAC Set Point

particular circuit operates from 0 (all inputs high) to +51°C (all inputs low) in 0.2°C steps. The comparator is shown with 1°C hysteresis which is usually necessary to guard-band for extraneous noise; omitting the 5.1MΩ resistor results in no hysteresis.

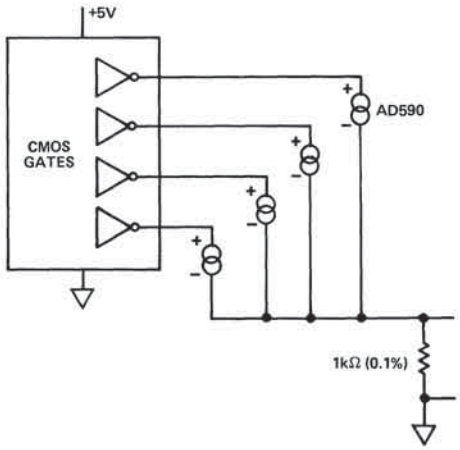


Figure 17. AD590 Driven from CMOS Logic

The voltage compliance and the reverse blocking characteristic of the AD590 allows it to be powered directly from +5V CMOS logic. This permits easy multiplexing, switching or pulsing for minimum internal heat dissipation. In Figure 17 any AD590 connected to a logic high will pass a signal current through the current measuring circuitry while those connected to a logic zero will pass insignificant current. The outputs used to drive the AD590's may be employed for other purposes, but the additional capacitance due to the AD590 should be taken into account.

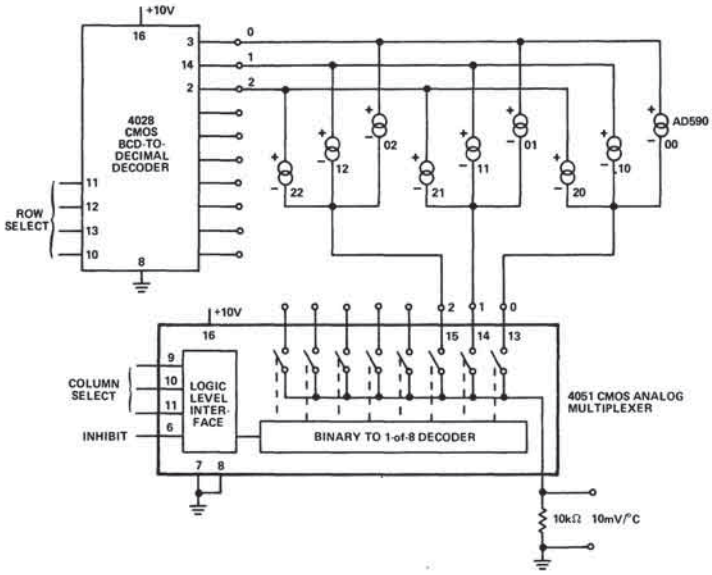


Figure 18. Matrix Multiplexer

CMOS Analog Multiplexers can also be used to switch AD590 current. Due to the AD590's current mode, the resistance of such switches is unimportant as long as 4V is maintained across the transducer. Figure 18 shows a circuit which combines the principal demonstrated in Figure 17 with an 8 channel CMOS Multiplexer. The resulting circuit can select one of eighty sensors over only 18 wires with a 7 bit binary word. The inhibit input on the multiplexer turns all sensors off for minimum dissipation while idling.

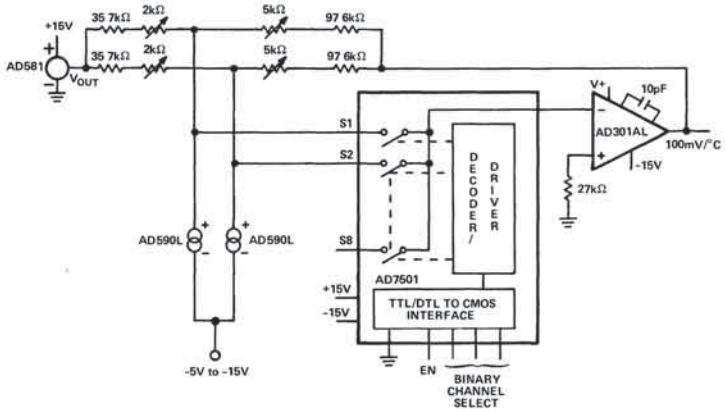


Figure 19. 8-Channel Multiplexer

Figure 19 demonstrates a method of multiplexing the AD590 in the two-trim mode (Figure 7). Additional AD590's and their associated resistors can be added to multiplex up to 8 channels of ±0.5°C absolute accuracy over the temperature range of −55°C to +125°C. The high temperature restriction of +125°C is due to the output range of the op amps; output to +150°C can be achieved by using a +20V supply for the op amp.

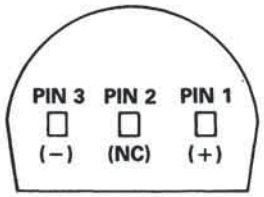
ANALOG DEVICES

Low Cost, Precision IC Temperature Transducer

AD592*

FEATURES
High Precalibrated Accuracy: 0.5°C max @ 25°C
Excellent Linearity: 0.15°C max (0 to +70°C)
Wide Operating Temperature Range: −25°C to +105°C
Single Supply Operation: +4V to +30V
Excellent Repeatability and Stability
High Level Output: 1μA/K
Two Terminal Monolithic IC: Temperature In/ Current Out
Minimal Self-Heating Errors

AD592 CONNECTING DIAGRAM



*PIN 2 CAN BE EITHER ATTACHED OR UNCONNECTED

BOTTOM VIEW

PRODUCT DESCRIPTION

The AD592 is a two terminal monolithic integrated circuit temperature transducer that provides an output current proportional to absolute temperature. For a wide range of supply voltages the transducer acts as a high impedance temperature dependent current source of 1μA/K. Improved design and laser wafer trimming of the IC's thin film resistors allows the AD592 to achieve absolute accuracy levels and nonlinearity errors previously unattainable at a comparable price.

The AD592 can be employed in applications between −25°C and +105°C where conventional temperature sensors (i.e., thermistor, RTD, thermocouple, diode) are currently being used. The inherent low cost of a monolithic integrated circuit in a plastic package, combined with a low total parts count in any given application, make the AD592 the most cost effective temperature transducer currently available. Expensive linearization circuitry, precision voltage references, bridge components, resistance measuring circuitry and cold junction compensation are not required with the AD592.

Typical application areas include; appliance temperature sensing, automotive temperature measurement and control, HVAC (heating/ventilating/air conditioning) system monitoring, industrial temperature control, thermocouple cold junction compensation, board-level electronics temperature diagnostics, temperature readout options in instrumentation, and temperature correction circuitry for precision electronics. Particularly useful in remote sensing applications, the AD592 is immune to voltage drops and voltage noise over long lines due to its high impedance current output. AD592s can easily be multiplexed; the signal current can be switched by a CMOS multiplexer or the supply voltage can be enabled with a tri-state logic gate.

*Covered by Patent No. 4,123,698.

The AD592 is available in three performance grades; the AD592AN, AD592BNand AD592CN. All devices are packaged in a plastic TO-92 case rated from −45°C to +125°C. Performance is specified from −25°C to +105°C. AD592 chips are also available, contact the factory for details.

PRODUCT HIGHLIGHTS

1. With a single supply (4V to 30V) the AD592 offers 0.5°C temperature measurement accuracy.
2. A wide operating temperature range (−25°C to +105°C) and highly linear output make the AD592 an ideal substitute for older, more limited sensor technologies (i.e., thermistors, RTDs, diodes, thermocouples).
3. The AD592 is electrically rugged; supply irregularities and variations or reverse voltages up to 20V will not damage the device.
4. Because the AD592 is a temperature dependent current source, it is immune to voltage noise pickup and IR drops in the signal leads when used remotely.
5. The high output impedance of the AD592 provides greater than 0.5°C/V rejection of supply voltage drift and ripple.
6. Laser wafer trimming and temperature testing insures that AD592 units are easily interchangeable.
7. Initial system accuracy will not degrade significantly over time. The AD592 has proven long term performance and repeatability advantages inherent in integrated circuit design and construction.

SPECIFICATIONS (typical @ 25°C, V_S = 5V, unless otherwise noted)

Model	AD592AN Min	AD592AN Typ	AD592AN Max	AD592BN Min	AD592BN Typ	AD592BN Max	AD592CN Min	AD592CN Typ	AD592CN Max	Units
ACCURACY										
Calibration Error @25°C[1]		1.5	**2.5**		0.7	**1.0**		0.3	**0.5**	°C
T_A = 0 to +70°C										
Error over Temperature		1.8	3.0		0.8	1.5		0.4	0.8	°C
Nonlinearity[2]		0.15	0.35		0.1	0.25		0.05	0.15	°C
T_A = −25 to +105°C										
Error over Temperature[3]		2.0	**3.5**		0.9	**2.0**		0.5	**1.0**	°C
Nonlinearity[2]		0.25	0.5		0.2	0.4		0.1	0.35	°C
OUTPUT CHARACTERISTICS										
Nominal Current Output @25°C (298.2K)		298.2			298.2			298.2		µA
Temperature Coefficient		1			1			1		µA/°C
Repeatability[4]			0.1			0.1			0.1	°C
Long Term Stability[5]			0.1			0.1			0.1	°C/month
ABSOLUTE MAXIMUM RATINGS										
Operating Temperature	−25		+105	−25		+105	−25		+105	°C
Package Temperature[6]	−45		+125	−45		+125	−45		+125	°C
Forward Voltage (+ to −)			**44**			**44**			**44**	V
Reverse Voltage (− to +)			**20**			**20**			**20**	V
Lead Temperature (Soldering 10 sec)			300			300			300	°C
POWER SUPPLY										
Operating Voltage Range	4		30	4		30	4		30	V
Power Supply Rejection										
+4V<V_S<+5V			**0.5**			**0.5**			**0.5**	°C/V
+5V<V_S<+15V			**0.2**			**0.2**			**0.2**	°C/V
+15V<V_S<+30V			**0.1**			**0.1**			**0.1**	°C/V

NOTES

[1]An external calibration trim can be used to zero the error @25°C.

[2]Defined as the maximum deviation from a mathematically best fit line.

[3]Parameter tested on all production units at +105°C only. C grade at −25°C also.

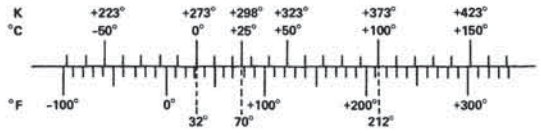
[4]Maximum deviation between +25°C readings after a temperature cycle between −45°C and +125°C. Errors of this type are noncummulative.

[5]Operation @125°C, error over time is noncummulative.

[6]Although performance is not specified beyond the operating temperature range, temperature excursions within the package temperature range will not damage the device.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.



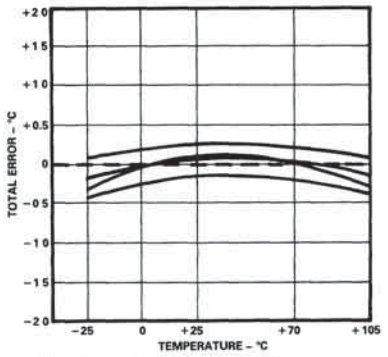
TEMPERATURE SCALE CONVERSION EQUATIONS

$$°C = \frac{5}{9}(°F - 32) \qquad K = °C + 273.15$$

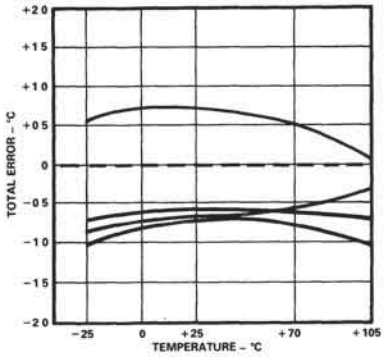
$$°F = \frac{9}{5}°C + 32 \qquad °R = °F + 459.7$$

Typical Performance Curves

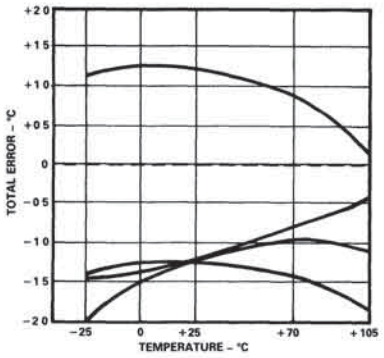
Typical @ V_S = +5V



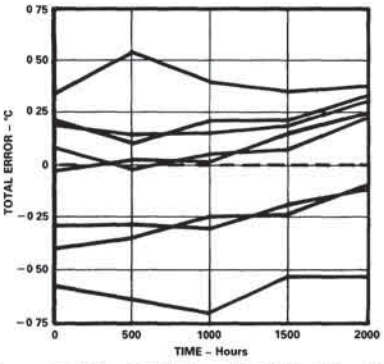
AD592CN Accuracy Over Temperature



AD592BN Accuracy Over Temperature

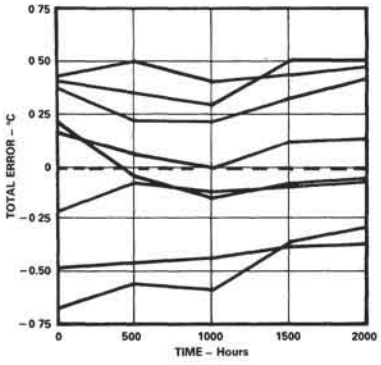


AD592AN Accuracy Over Temperature



Long-Term Stability @ 85°C and 85% Relative Humidity

10



Long-Term Stability @ 125°C

AD592 ORDERING GUIDE

Model	Package Option [1]	Max Cal Error @ 25°C	Max Error −25°C to +105°C	Max Nonlinearity −25°C to +105°C
AD592CN	TO-92	0.5°C	1.0°C	0.35°C
AD592BN	TO-92	1.0°C	2.0°C	0.4°C
AD592AN	TO-92	2.5°C	3.5°C	0.5°C

NOTE
[1]See Section 16 for package outline information.

THEORY OF OPERATION

The AD592 uses a fundamental property of silicon transistors to realize its temperature proportional output. If two identical transistors are operated at a constant ratio of collector current densities, r, then the difference in base-emitter voltages will be (kT/q)(ln r). Since both k, Boltzman's constant and q, the charge of an electron are constant, the resulting voltage is directly Proportional To Absolute Temperature (PTAT). In the AD592 this difference voltage is converted to a PTAT current by low temperature coefficient thin film resistors. This PTAT current is then used to force the total output current to be proportional to degrees Kelvin. The result is a current source with an output equal to a scale factor times the temperature (K) of the sensor. A typical V-I plot of the circuit at +25°C and the temperature extremes is shown in Figure 1.

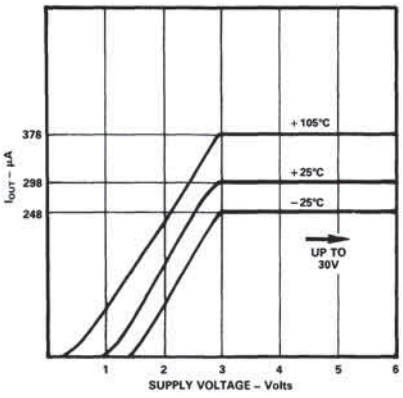


Figure 1. V–I Characteristics

Factory trimming of the scale factor to 1µA/K is accomplished at the wafer level by adjusting the AD592's temperature reading so it corresponds to the actual temperature. During laser trimming the IC is at a temperature within a few degrees of 25°C and is powered by a 5V supply. The device is then packaged and automatically temperature tested to specification.

FACTORS AFFECTING AD592 SYSTEM PRECISION

The accuracy limits given on the Specifications page for the AD592 makes it easy to apply in a variety of diverse applications. To calculate a total error budget in a given system it is important to correctly interpret the accuracy specifications, nonlinearity errors, the response of the circuit to supply voltage variations and the effect of the surrounding thermal environment. As with other electronic designs external component selection will have a major effect on accuracy.

CALIBRATION ERROR, ABSOLUTE ACCURACY AND NONLINEARITY SPECIFICATIONS

Three primary limits of error are given for the AD592 such that the correct grade for any given application can easily be chosen for the overall level of accuracy required. They are the calibration accuracy at 25°C, and the error over temperature from 0 to 70°C and −25°C to +105°C. These specifications correspond to the actual error the user would see if the current output of a AD592 were converted to a voltage with a precision resistor. Note that the maximum error at room temperature, over the commercial IC temperature range, or an extended range including the boiling point of water, can be directly read from the Specifications Table. All three error limits are a combination of initial error, scale factor variation and nonlinearity deviation from the ideal 1µA/K output. Figure 2 graphically depicts the guaranteed limits of accuracy for an AD592CN.

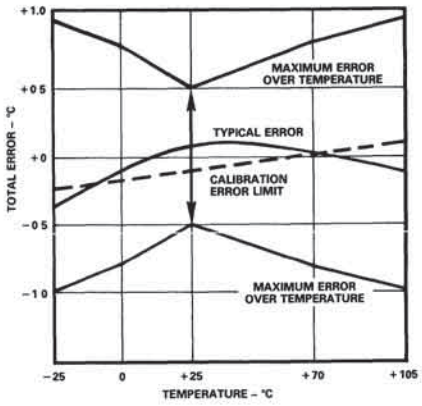


Figure 2. Error Specifications (AD592CN)

The AD592 has a highly linear output in comparison to older technology sensors (i.e., thermistors, RTDs and thermocouples), thus a nonlinearity error specification is separated from the absolute accuracy given over temperature. As a maximum deviation from a best-fit straight line this specification represents the only error which cannot be trimmed out. Figure 3 is a plot of typical AD592CN nonlinearity over the full rated temperature range.

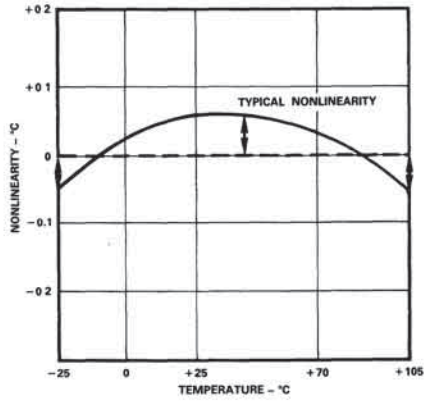


Figure 3. Nonlinearity Error (AD592CN)

TRIMMING FOR HIGHER ACCURACY

Calibration error at 25°C can be removed with a single temperature trim. Figure 4 shows how to adjust the AD592's scale factor in the basic voltage output circuit.

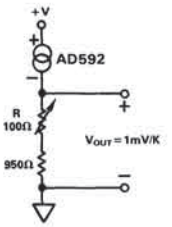


Figure 4. Basic Voltage Output (Single Temperature Trim)

To trim the circuit the temperature must be measured by a reference sensor and the value of R should be adjusted so the output (V_{OUT}) corresponds to 1mV/K. Note that the trim procedure should be implemented as close as possible to the temperature highest accuracy is desired for. In most applications if a single temperature trim is desired it can be implemented where the AD592 current-to-output voltage conversion takes place (e.g., output resistor, offset to an op amp). Figure 5 illustrates the effect on total error when using this technique.

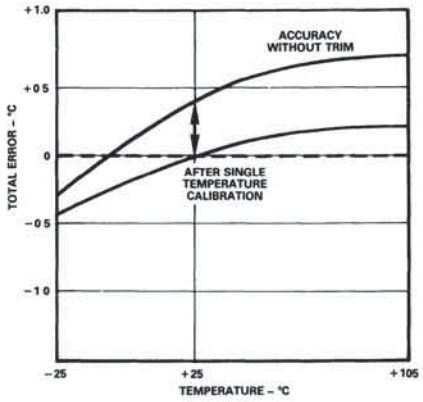


Figure 5. Effect of Scale Factor Trim on Accuracy

If greater accuracy is desired, initial calibration and scale factor errors can be removed by using the AD592 in the circuit of Figure 6.

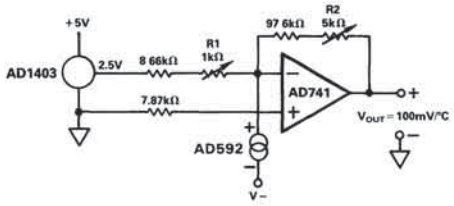


Figure 6. Two Temperature Trim Circuit

With the transducer at 0°C adjustment of R1 for a 0V output nulls the initial calibration error and shifts the output from K to °C. Tweaking the gain of the circuit at an elevated temperature by adjusting R2 trims out scale factor error. The only error remaining over the temperature range being trimmed for is nonlinearity. A typical plot of two trim accuracy is given in Figure 7.

SUPPLY VOLTAGE AND THERMAL ENVIRONMENT EFFECTS

The power supply rejection characteristics of the AD592 minimizes errors due to voltage irregularity, ripple and noise. If a supply is used other than 5V (used in factory trimming), the power supply error can be removed with a single temperature trim. The PTAT nature of the AD592 will remain unchanged. The general insensitivity of the output allows the use of lower cost unregulated supplies and means that a series resistance of several hundred ohms (e.g., CMOS multiplexer, meter coil resistance) will not degrade the overall performance.

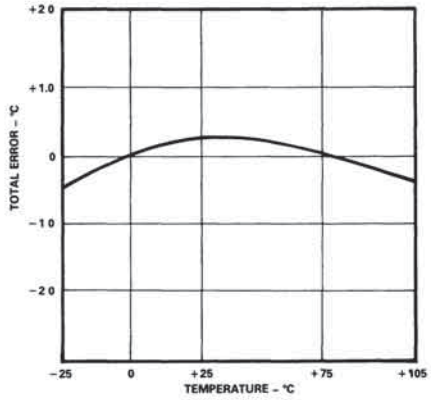


Figure 7. Typical Two Trim Accuracy

The thermal environment in which the AD592 is used determines two performance traits: the effect of self-heating on accuracy and the response time of the sensor to rapid changes in temperature. In the first case, a rise in the IC junction temperature above the ambient temperature is a function of two variables; the power consumption level of the circuit and the thermal resistance between the chip and the ambient environment (θ_{JA}). Self-heating error in °C can be derived by multiplying the power dissipation by θ_{JA}. Because errors of this type can vary widely for surroundings with different heat sinking capacities it is necessary to specify θ_{JA} under several conditions. Table I shows how the magnitude of self-heating error varies relative to the environment. In typical free air applications at 25°C with a 5V supply the magnitude of the error is 0.2°C or less. A common clip-on heat sink will reduce the error by 25% or more in critical high temperature, large supply voltage situations.

Medium	θ_{JA} (°C/watt)	τ (sec)*
Still Air		
Without Heat Sink	175	60
With Heat Sink	130	55
Moving Air		
Without Heat Sink	60	12
With Heat Sink	40	10
Fluorinert Liquid	35	5
Aluminum Block**	30	2.4

*τ is an average of five time constants (99.3% of final value). In cases where the thermal response is not a simple exponential function, the actual thermal response may be better than indicated.
**With thermal grease.

Table I. Thermal Characteristics

Response of the AD592 output to abrupt changes in ambient temperature can be modeled by a single time constant τ exponential function. Figure 8 shows typical response time plots for several media of interest.

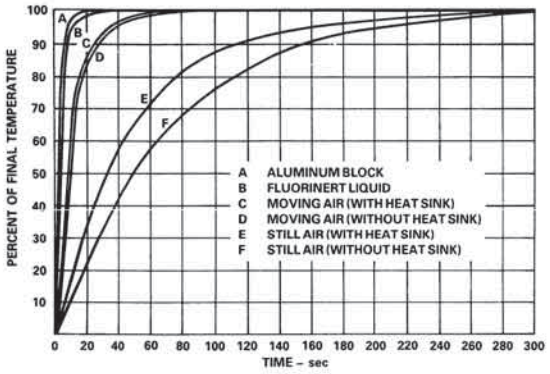


Figure 8. Thermal Response Curves

The time constant, τ, is dependent on θ_{JA} and the thermal capacities of the chip and the package. Table I lists the effective τ (time to reach 63.2% of the final value) for several different media. Copper printed circuit board connections where neglected in the analysis, however, they will sink or conduct heat directly through the AD592's solder dipped Kovar leads. When faster response is required a thermally conductive grease or glue between the AD592 and the surface temperature being measured should be used. In free air applications a clip-on heat sink will decrease output stabilization time by 10–20%.

MOUNTING CONSIDERATIONS

If the AD592 is thermally attached and properly protected, it can be used in any temperature measuring situation where the maximum range of temperatures encountered is between −25°C and +105°C. Because plastic IC packaging technology is employed, excessive mechanical stress must be safeguarded against when fastening the device with a clamp or screw-on heat tab. Thermally conductive epoxy or glue is recommended under typical mounting conditions. In wet or corrosive environments any electrically isolated metal or ceramic well can be used to shield the AD592. Condensation at cold temperatures can cause leakage current related errors and should be avoided by sealing the device in nonconductive epoxy paint or dips.

APPLICATIONS

Connecting several AD592 devices in parallel adds the currents through them and produces a reading proportional to the average temperature. Series AD592s will indicate the lowest temperature because the coldest device limits the series current flowing through the sensors. Both of these circuits are depicted in Figure 9.

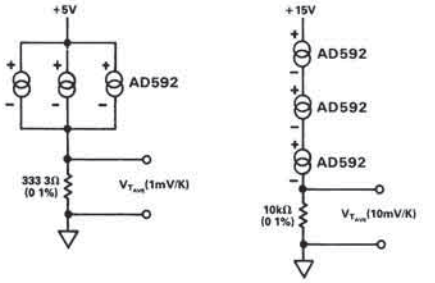


Figure 9. Average and Minimum Temperature Connections

The circuit of Figure 10 demonstrates a method in which a voltage output can be derived in a differential temperature measurement.

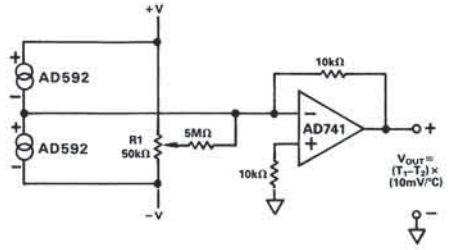


Figure 10. Differential Measurements

R1 can be used to trim out the inherent offset between the two devices. By increasing the gain resistor (10kΩ) temperature measurements can be made with higher resolution. If the magnitude of V+ and V− is not the same, the difference in power consumption between the two devices can cause a differential self-heating error.

Cold junction compensation (CJC) used in thermocouple signal conditioning can be implemented using an AD592 in the circuit configuration of Figure 11. Expensive simulated ice baths or hard to trim, inaccurate bridge circuits are no longer required.

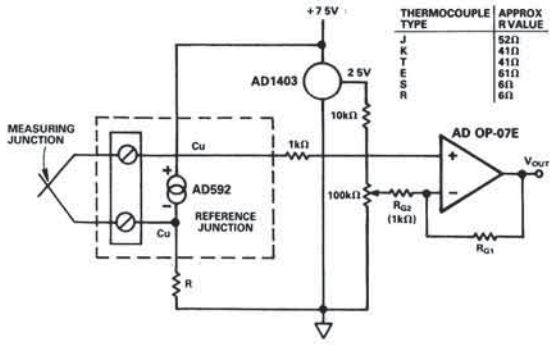


Figure 11. Thermocouple Cold Junction Compensation

The circuit shown can be optimized for any ambient temperature range or thermocouple type by simply selecting the correct value for the scaling resistor – R. The AD592 output (1μA/K) times R should approximate the line best fit to the thermocouple curve (slope in V/°C) over the most likely ambient temperature range. Additionally, the output sensitivity can be chosen by selecting the resistors R_{G1} and R_{G2} for the desired noninverting gain. The offset adjustment shown simply references the AD592 to °C. Note that the TC's of the reference and the resistors are the primary contributors to error. Temperature rejection of 40 to 1 can be easily achieved using the above technique.

Although the AD592 offers a noise immune current output, it is not compatible with process control/industrial automation current loop standards. Figure 12 is an example of a temperature to 4-20mA transmitter for use with 40V, 1kΩ systems.

In this circuit the 1μA/K output of the AD592 is amplified to 1mA/°C and offset so that 4mA is equivalent to 17°C and 20mA is equivalent to 33°C. Rt is trimmed for proper reading at an

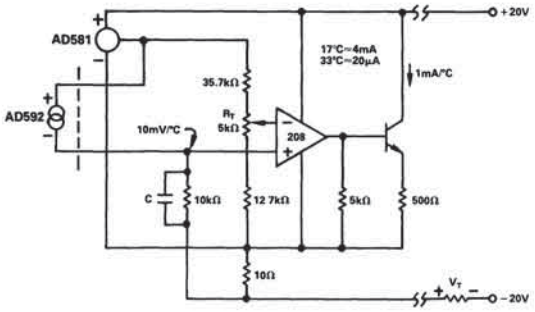


Figure 12. Temperature to 4–20mA Current Transmitter

intermediate reference temperature. With a suitable choice of resistors, any temperature range within the operating limits of the AD592 may be chosen.

Reading temperature with an AD592 in a microprocessor based system can be implemented with the circuit shown in Figure 13.

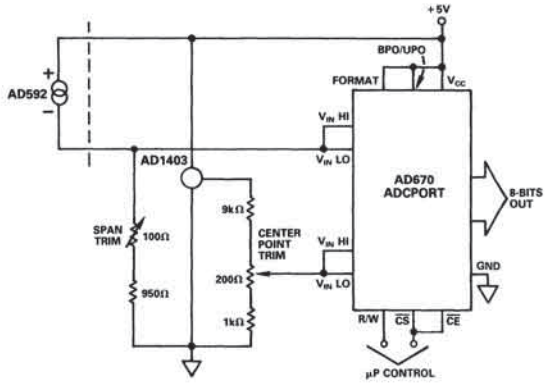


Figure 13. Temperature to Digital Output

By using a differential input A/D converter and choosing the current to voltage conversion resistor correctly any range of temperatures (up to the 130°C span the AD592 is rated for) centered at any point can be measured using a minimal number of components. In this configuration the system will resolve up to 1°C.

A variable temperature controlling thermostat can easily be built using the AD592 in the circuit of Figure 14.

R_{HIGH} and R_{LOW} determine the limits of temperature controlled by the potentiometer R_{SET}. The circuit shown operates over the full temperature range (−25°C to +105°C) the AD592 is rated for. The reference maintains a constant set point voltage and insures that approximately 7V appears across the sensor. If it is necessary to guardband for extraneous noise hysteresis can be added by tying a resistor from the output to the ungrounded end of R_{LOW}.

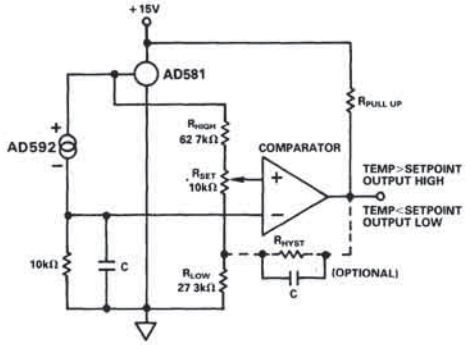


Figure 14. Variable Temperature Thermostat

Multiple remote temperatures can be measured using several AD592s with a CMOS multiplexer or a series of 5V logic gates because of the device's current-mode output and supply-voltage compliance range. The on-resistance of a FET switch or output impedance of a gate will not effect the accuracy, as long as 4V is maintained across the transducer. MUXs and logic driving circuits should be chosen to minimize leakage current related errors. Figure 15 illustrates a locally controlled MUX switching the signal current from several remote AD592s. CMOS or TTL gates can also be used to switch the AD592 supply voltages, with the multiplexed signal being transmitted over a single twisted pair to the load.

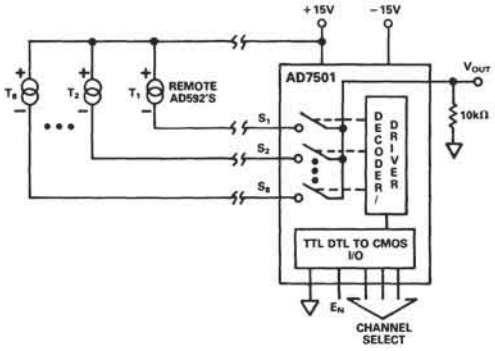


Figure 15. Remote Temperature Multiplexing

To minimize the number of MUXs required when a large number of AD592s are being used, the circuit can be configured in a matrix. That is, a decoder can be used to switch the supply voltage to a column of AD592s while a MUX is used to control which row of sensors are being measured. The maximum number of AD592s which can be used is the product of the number of channels of the decoder and MUX.

10

An example circuit controlling 80 AD592s is shown in Figure 16. A 7-bit digital word is all that is required to select one of the sensors. The enable input of the multiplexer turns all the sensors off for minimum dissipation while idling.

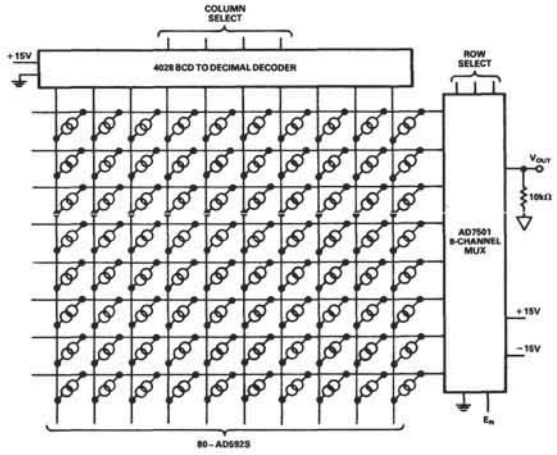


Figure 16. Matrix Multiplexer

To convert the AD592 output to °C or °F a single inexpensive reference and op amp can be used as shown in Figure 17. Although this circuit is similar to the two temperature trim circuit shown in Figure 6, two important differences exist. First, the gain resistor is fixed alleviating the need for an elevated temperature trim. Acceptable accuracy can be achieved by choosing an inexpensive resistor with the correct tolerance. Second, the AD592 calibration error can be trimmed out at a known convenient temperature (i.e., room temperature) with a single pot adjustment. This step is independent of the gain selection.

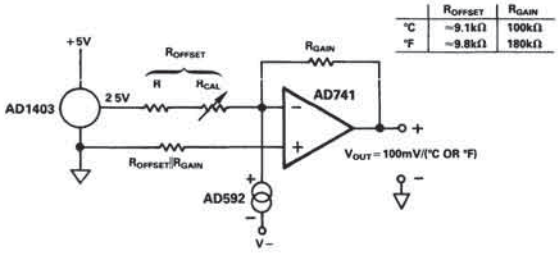


Figure 17. Celsius or Fahrenheit Thermometer

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Selection Guide
Signal Conditioning Components & Subsystems

Model	V/I Transmitters Loop Power	V/I Transmitters Local Power	Isolated	Sensor Excitation	Sensor Type(s)	IC	Hybrid Package	Module	Page
AD594/AD595					TC	X			11 – 5
AD596/AD597					TC	X			11 –13
AD693	X			X	mV: All	X			11 – 19
1B21	X		X					X	11 – 31
1B22		X	X					X	11 – 35
1B31				X	Strain Gage		X		11 – 37
1B32				X	Strain Gage, RTD		X		11 – 45
1B41			X	X	RTD			X	11 – 53
1B51			X		TC, mV			X	11 – 55
2B20		X						X	11 – 59
2B22		X	X					X	11 – 63
2B23		X	X					X	11 – 67
2B24	X		X					X	11 – 87
2B30					Strain Gage, RTD			X	11 – 71
2B31				X	Strain Gage, RTD			X	11 – 71
2B50			X		TC, mV			X	11 – 77
2B52	X		X		TC, mV			X	11 – 87
2B53	X				TC, mV			X	11 – 87
2B54/2B55			X		mV, 4-channel			X	11 – 81
2B57	X			X	Solid State (AD590)			X	11 – 87
2B58				X	3-wire RTD			X	11 – 87
2B59	X			X	2-wire RTD			X	11 – 87
3B Series	— See Orientation —								11 – 89
4B Series	— See Orientation —								11 – 93
5B Series	— See Orientation —								11 – 95

11

Orientation
Signal Conditioning Components & Subsystems

Signal conditioners provide an analog interface between sensors and the systems they serve. They amplify signals, provide zero suppression where necessary, introduce electrical isolation, furnish excitation for passive transducers and provide analog outputs in the form required by the system – either voltage or current – at appropriate levels.

The most popular sensors are thermocouples, RTDs (resistance temperature detectors) and strain gages; they are low-level devices requiring precision amplification with low drift and noise. A useful discussion of their properties and signal-conditioning requirements can be found in the Analog Devices *Transducer Interfacing Handbook* (1980, $14.50 postpaid), available from P.O.Box 796, Norwood MA 02062.

Signal-conditioning circuits can be assembled using many of the precision products to be found in this databook, such as operational amplifiers, instrumentation amplifiers, and isolation amplifiers, along with other electronic circuit elements and appropriate hardware. However, many system designers have found that with less expenditure of valuable engineering talent, excellent, reliable results can be achieved at lower cost by purchasing complete dedicated signal conditioners with fully specified performance in standard packages.

The general requirements for signal conditioners include the usual precision electrical characteristics, such as high gain, low drift and noise, accurate scale factors and fast – or filtered – response. Quite often, electrical isolation must be provided between the point of measurement and the system; besides maximizing common-mode rejection, this can provide protection of people and equipment. Where ruggedness and safety are involved, it may be useful to choose products, when available, that meet appropriate standards developed by such entities as IEEE and Factory Mutual Insurance Company.

Many sensors require auxiliary circuitry; for example, thermocouples require a constant-temperature reference junction or an equivalent "ice-point" reference circuit, and strain gages and RTDs are passive devices that need excitation. Although the results of a measurement may be produced – and are ultimately needed – in the form of voltage, they may have to be transmitted as a varying current with a standard span, such as 4 to 20mA; often the power for such current loops is furnished to the sensor and its conditioner from the remote destination.

Another requirement arises from the fact that systems often involve many diverse channels of measurement. Such systems need a *family* of signal conditioners to meet the multiplicity of functional needs, yet it is desirable that they be compactly and ruggedly housed, modular, provided with a power supply and capable of being interchanged as system needs change. It is for such applications that the 3B, 4B and 5B families and their housings were designed.

The *selection guide* lists the available devices that are recommended for new system designs, along with their salient features; detailed information will be found in the data sheets. Examples of such devices include conditioners for thermocouples, RTDs, strain gages, and low (mV)-level signal sources and current transmitters that convert the signal information to 4-20mA or 0-20mA currents for loops requiring analog information in that form. If a modular subsystem is desired, selection information for choosing specific modules within the 3B, 4B and 5B families will be found in the family data sheets.

The individually listed devices are manufactured in various forms, ranging from monolithic integrated circuits (AD594/595/596/597 and AD693) to devices in dual in-line packages – using hybrid and surface-mount technologies – to modules with either pins for chassis wiring or screw terminals for field wiring.

The *3B Series* is an integrated modular signal-conditioning subsystem consisting of a series of color-coded functionally complete plug-in mix-and-match input and output modules on a universal backplane available for mounting in either rugged industrial chassis or a standard rack. The backplane connects directly to field wiring via screw terminals and to the system destination via connectors. A standard 19″ relay rack mount will hold 16 modules; 8- and 4-module units are also available. Among the characteristics of the modules are input protection, low-pass filtering, ±1μV/°C zero drift, and galvanic isolation to ±1,500 volts peak. The output modules translate high-level voltage inputs to standard process-current levels (0-20mA or 4-20mA) with accuracy to within 0.1%.

The 4B Series Alarm Limit Subsystem is compatible in physical appearance with the 3B Series. Alarm units accept signals from 3B Series voltage or process outputs – or high-level outputs from other sensor circuitry; they make decisions and produce output indications for alarm or on-off control when monitored conditions fall outside specified limits. Typical applications include process control, factory automation, energy management, and data acquisition and control. The 4B Series subsystem comprises a backplane and a family of plug-in mix-and-match alarm limit modules (up to 12 per rack or four per 4-channel backplane).

The *5B Series* of modules comprises a family of plug-in single-channel signal conditioners for sensors that perform complete signal-conditioning functions optimized for the nature of each device's specified input. Characterized by high performance, small size and low price, they are ideal for monitoring such analog quantities as temperature, pressure and flow in industrial data-acquisition applications.

They are isolated (1,500 volts rms), operate from single 5-volt supplies and have ±0.05% calibration accuracy; they are identical in size (2.25″ × 2.25″ × 0.60″) and pinout. Physically compatible backplanes will hold as many as 16 units in a 19″ rack-mount space 3 1/2″ high. Signal-conditioning functions include input protection, filtering, chopper-stabilized low-drift amplification, isolation, linearization for RTD and thermocouple inputs and excitation for passive sensors.

5B Series modules have 240-volt protection for all field terminations. All feature excellent common-mode rejection, meet IEEE 472-1974 surge-withstand specs and operate over the −40°C to +85°C ambient temperature range. They are physically rugged, with sturdy 0.04′ pin connections and no adjustment potentiometers to compromise accuracy and system integrity; they are secured with a single self-contained mounting screw.

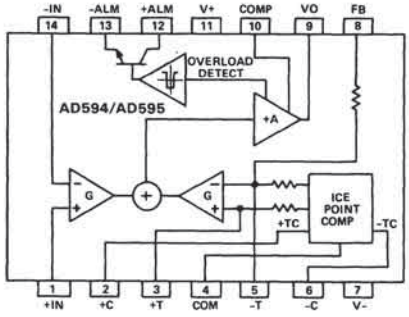
Monolithic Thermocouple Amplifiers with Cold Junction Compensation

AD594*/AD595*

FEATURES

- Pretrimmed for Type J (AD594) or Type K (AD595) Thermocouples
- Can Be Used with Type T Thermocouple Inputs
- Low Impedance Voltage Output: 10mV/°C
- Built-In Ice Point Compensation
- Wide Power Supply Range: +5V to ±15V
- Low Power: <1mW typical
- Thermocouple Failure Alarm
- Laser Wafer Trimmed to 1°C Calibration Accuracy
- Set-Point Mode Operation
- Self-Contained Celsius Thermometer Operation
- High Impedance Differential Input
- Side-Brazed DIP or Low Cost Cerdip

AD594/AD595 FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to produce a high level (10mV/°C) output directly from a thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby converting it to a stand-alone Celsius transducer with a low-impedance voltage output.

The AD594/AD595 includes a thermocouple failure alarm that indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability.

The AD594/AD595 can be powered from a single ended supply (including +5V) and by including a negative supply, temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD594/AD595 will typically operate with a total supply current of 160μA, but is also capable of delivering in excess of ±5mA to a load.

The AD594 is precalibrated by laser wafer trimming to match the characteristic of type J (iron-constantan) thermocouples and the AD595 is laser trimmed for type K (chromel-alumel) inputs. The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit can be recalibrated for other thermocouple types by the addition of two or three resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications.

*Protected by U.S. Patent No. 4,029,974.

The AD594/AD595 is available in two performance grades. The C and the A versions have calibration accuracies of ±1°C and ±3°C, respectively. Both are designed to be used from 0 to +50°C, and are available in 14-pin, hermetically sealed, side-brazed ceramic DIPs as well as low cost cerdip packages.

PRODUCT HIGHLIGHTS

1. The AD594/AD595 provides cold junction compensation, amplification, and an output buffer in a single IC package.
2. Compensation, zero, and scale factor are all precalibrated by laser wafer trimming (LWT) of each IC chip.
3. Flexible pin-out provides for operation as a set-point controller or a stand-alone temperature transducer calibrated in degrees Celsius.
4. Operation at remote application sites is facilitated by low quiescent current and a wide supply voltage range of +5V to dual supplies spanning 30V.
5. Differential input rejects common-mode noise voltage on the thermocouple leads.

SPECIFICATIONS (@ +25°C and V_S = 5V, Type J (AD594), Type K (AD595) Thermocouple, unless otherwise noted)

Model	AD594A			AD594C			AD595A			AD595C			Units
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
ABSOLUTE MAXIMUM RATINGS													
$+V_S$ to $-V_S$			36			36			36			36	Volts
Common-Mode Input Voltage	$-V_S-0.15$		$+V_S$	$-V_S-0.15$		$+V_S$	$-V_S-0.15$		$+V_S$	$-V_S-0.15$		$+V_S$	Volts
Differential Input Voltage	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Alarm Voltages													
+ALM	$-V_S$		$-V_S+36$	$-V_S$		$-V_S+36$	$-V_S$		$-V_S+36$	$-V_S$		$-V_S+36$	Volts
−ALM	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	$-V_S$		$+V_S$	Volts
Operating Temperature Range	−55		+125	−55		+125	−55		+125	−55		+125	°C
Output Short Circuit to Common	Indefinite			Indefinite			Indefinite			Indefinite			
TEMPERATURE MEASUREMENT													
(Specified Temperature Range 0 to +50°C)													
Calibration Error at +25°C[1]			±3			±1			±3			±1	°C
Stability vs Temperature[2]			**±0.05**			**±0.025**			**±0.05**			**±0.025**	°C/°C
Gain Error			**±1.5**			**±0.75**			**±1.5**			**±0.75**	%
Nominal Transfer Function			10			10			10			10	mV/°C
AMPLIFIER CHARACTERISTICS													
Closed Loop Gain[3]		**193.4**			**193.4**			**247.3**			**247.3**		
Input Offset Voltage	(Temperature in °C) × 51.70μV/°C			(Temperature in °C) × 51.70μV/°C			(Temperature in °C) × 40.44μV/°C			(Temperature in °C) × 40.44μV/°C			μV
Input Bias Current		0.1			0.1			0.1			0.1		μA
Differential Input Range	−10		+50				−10		+50	−10		+50	mV
Common-Mode Range	$-V_S-0.15$		$+V_S-4$	$-V_S-0.15$		$+V_S-4$	$-V_S-0.15$		$+V_S-4$	$-V_S-0.15$		$+V_S-4$	Volts
Common-Mode Sensitivity–RTO			**10**			**10**			**10**			**10**	mV/V
Power Supply Sensitivity–RTO			**10**			**10**			**10**			**10**	mV/V
Output Voltage Range													
Dual Supplies	$-V_S+2.5$		$+V_S-2$	$-V_S+2.5$		$+V_S-2$	$-V_S+2.5$		$+V_S-2$	$-V_S+2.5$		$+V_S-2$	Volts
Single Supply	0		$+V_S-2$	0		$+V_S-2$	0		$+V_S+2$	0		$+V_S-2$	Volts
Usable Output Current[4]		±5			±5			±5			±5		mA
3dB Bandwidth		15			15			15			15		kHz
ALARM CHARACTERISTICS													
$V_{CE(SAT)}$ at 2mA		0.3			0.3			0 3			0.3		Volts
Leakage Current			**±1**			**±1**			**±1**			**±1**	μA max
Operating Voltage at −ALM			$+V_S-4$			$+V_S-4$			$+V_S-4$			$+V_S-4$	Volts
Short Circuit Current		20			20			20			20		mA
POWER REQUIREMENTS													
Specified Performance	$+V_S=5, -V_S=0$			$+V_S=5, -V_S=0$			$+V_S=5, -V_S=0$			$+V_S=5, -V_S=0$			Volts
Operating[5]	$+V_S$ to $-V_S \leq 30$			$+V_S$ to $-V_S \leq 30$			$+V_S$ to $-V_S \leq 30$			$+V_S$ to $-V_S \leq 30$			Volts
Quiescent Current (No Load)													
$+V_S$		160	300		160	300		160	300		160	300	μA
$-V_S$		100			100			100			100		μA
PACKAGE OPTIONS[6]													
TO-116 (D-14)		AD594AD			AD594CD			AD595AD			AD595CD		
Cerdip (Q-14)		AD594AQ			AD594CQ			AD595AQ			AD595CQ		

NOTES

[1]Calibrated for minimum error at +25°C using a thermocouple sensitivity of 51.7μV/°C. Since a J type thermocouple deviates from this straight line approximation, the AD594 will normally read 3.1mV when the measuring junction is at 0°C. The AD595 will similarly read 2.7mV at 0°C.

[2]Defined as the slope of the line connecting the AD594/AD595 errors measured at 0°C and 50°C ambient temperature.

[3]Pin 8 shorted to pin 9.

[4]Current Sink Capability in single supply configuration is limited to current drawn to ground through a 50kΩ resistor at output voltages below 2.5V.

[5]$-V_S$ must not exceed −16.5V.

[6]See Section 16 for package outline information.

Specifications subject to change without notice.

Specifications shown in boldface are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Thermocouple Temperature °C	Type J Voltage mV	AD594 Output mV	Type K Voltage mV	AD595 Output mV	Thermocouple Temperature °C	Type J Voltage mV	AD594 Output mV	Type K Voltage mV	AD595 Output mV
− 200	− 7.890	−1523	− 5.891	−1454	500	27.388	5300	20.640	5107
− 180	− 7.402	−1428	− 5.550	−1370	520	28 511	5517	21.493	5318
− 160	− 6.821	−1316	− 5.141	−1269	540	29.642	5736	22.346	5529
− 140	− 6.159	−1188	− 4 669	−1152	560	30.782	5956	23.198	5740
− 120	− 5 426	−1046	− 4.138	−1021	580	31.933	6179	24.050	5950
− 100	− 4 632	− 893	− 3.553	− 876	600	33.096	6404	24.902	6161
− 80	− 3.785	− 729	− 2.920	− 719	620	34.273	6632	25.751	6371
− 60	− 2 892	− 556	− 2.243	− 552	640	35.464	6862	26.599	6581
− 40	− 1 960	− 376	− 1.527	− 375	660	36.671	7095	27.445	6790
− 20	− .995	− 189	− 777	− 189	680	37 893	7332	28.288	6998
− 10	− 501	− 94	− .392	− 94	700	39.130	7571	28.128	7206
0	0	3.1	0	2.7	720	40 382	7813	29.965	7413
10	.507	101	.397	101	740	41 647	8058	30.799	7619
20	1 019	200	798	200	750	42.283	8181	31 214	7722
25	1 277	250	1.000	250	760	–	–	31.629	7825
30	1 536	300	1 203	300	780	–	–	32.455	8029
40	2 058	401	1 611	401	800	–	–	33.277	8232
50	2 585	503	2 022	503	820	–	–	34.095	8434
60	3 115	606	2.436	605	840	–	–	34.909	8636
80	4 186	813	3 266	810	860	–	–	35.718	8836
100	5 268	1022	4 095	1015	880	–	–	36.524	9035
120	6.359	1233	4.919	1219	900	–	–	37.325	9233
140	7 457	1445	5.733	1420	920	–	–	38.122	9430
160	8.560	1659	6.539	1620	940	–	–	38.915	9626
180	9.667	1873	7.338	1817	960	–	–	39.703	9821
200	10.777	2087	8.137	2015	980	–	–	40.488	10015
220	11.887	2302	8.938	2213	1000	–	–	41.269	10209
240	12 998	2517	9.745	2413	1020	–	–	42 045	10400
260	14 108	2732	10.560	2614	1040	–	–	42.817	10591
280	15 217	2946	11.381	2817	1060	–	–	43.585	10781
300	16.325	3160	12.207	3022	1080	–	–	44.349	10970
320	17.432	3374	13.039	3327	1100	–	–	45.108	11158
340	18.537	3588	13.874	3434	1120	–	–	45.863	11345
360	19.640	3801	14.712	3641	1140	–	–	46.612	11530
380	20.743	4015	15.552	3849	1160	–	–	47.356	11714
400	21.846	4228	16.395	4057	1180	–	–	48.095	11897
420	22.949	4441	17.241	4266	1200	–	–	48.828	12078
440	24.054	4655	18.088	4476	1220	–	–	49.555	12258
460	25.161	4869	18.938	4686	1240	–	–	50.276	12436
480	26.272	5084	19.788	4896	1250	–	–	50.633	12524

Table I. Output Voltage vs. Thermocouple Temperature (Ambient +25°C, V_S = −5V, +15V)

11

INTERPRETING AD594/AD595 OUTPUT VOLTAGES

To achieve a temperature proportional output of 10mV/°C and accurately compensate for the reference junction over the rated operating range of the circuit, the AD594/AD595 is gain trimmed to match the transfer characteristic of J and K type thermocouples at 25°C. For a type J output in this temperature range the TC is 51.70μV/°C, while for a type K it is 40.44μV/°C. The resulting gain for the AD594 is 193.4 (10mV/°C divided by 51.7μV/°C) and for the AD595 is 247.3 (10mV/°C divided by 40.44μV/°C). In addition, an absolute accuracy trim induces an input offset to the output amplifier characteristic of 16μV for the AD594 and 11μV for the AD595. This offset arises because the AD594/AD595 is trimmed for a 250mV output while applying a 25°C thermocouple input.

Because a thermocouple output voltage is nonlinear with respect to temperature, and the AD594/AD595 linearly amplifies the compensated signal, the following transfer functions should be used to determine the actual output voltages:

AD594 output = (Type J Voltage + 16μV) × 193.4

AD595 output = (Type K Voltage + 11μV) × 247.3
or conversely:

Type J voltage = (AD594 output / 193.4) − 16μV

Type K voltage = (AD595 output / 247.3) − 11μV

Table I above lists the ideal AD594/AD595 output voltages as a function of Celsius temperature for type J and K ANSI standard thermocouples, with the package and reference junction at 25°C. As is normally the case, these outputs are subject to calibration, gain and temperature sensitivity errors. Output values for intermediate temperatures can be interpolated, or calculated using the output equations and ANSI thermocouple voltage tables referred to zero degrees Celsius. Due to a slight variation in alloy content between ANSI type J and DIN Fe–CuNi thermocouples Table I should not be used in conjunction with European standard thermocouples. Instead the transfer function given previously and a DIN thermocouple table should be used. ANSI type K and DIN NiCr–Ni thermocouples are composed of identical alloys and exhibit similar behavior. The upper temperature limits in Table I are those recommended for type J and type K thermocouples by the majority of vendors.

SINGLE AND DUAL SUPPLY CONNECTIONS

The AD594/AD595 is a completely self-contained thermocouple conditioner. Using a single +5V supply the interconnections shown in Figure 1 will provide a direct output from a type J thermocouple (AD594) or type K thermocouple (AD595) measuring from 0 to +300°C.

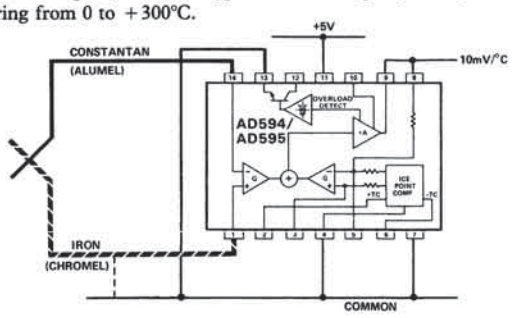


Figure 1. Basic Connection, Single Supply Operation

Any convenient supply voltage from +5V to +30V may be used, with self-heating errors being minimized at lower supply levels. In the single supply configuration the +5V supply connects to pin 11 with the V− connection at pin 7 strapped to power and signal common at pin 4. The thermocouple wire inputs connect to pins 1 and 14 either directly from the measuring point or through intervening connections of similar thermocouple wire type. When the alarm output at pin 13 is not used it should be connected to common or −V. The precalibrated feedback network at pin 8 is tied to the output at pin 9 to provide a 10mV/°C nominal temperature transfer characteristic.

By using a wider ranging dual supply, as shown in Figure 2, the AD594/AD595 can be interfaced to thermocouples measuring both negative and extended positive temperatures.

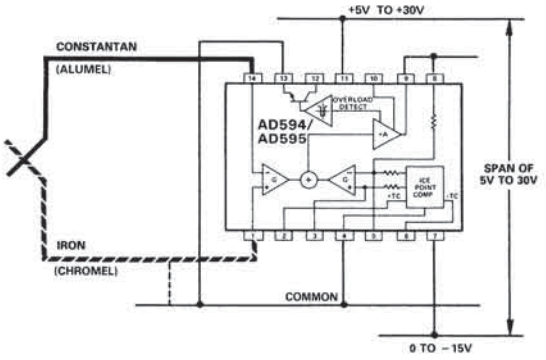


Figure 2. Dual Supply Operation

With a negative supply the output can indicate negative temperatures and drive grounded loads or loads returned to positive voltages. Increasing the positive supply from 5V to 15V extends the output voltage range well beyond the 750°C temperature limit recommended for type J thermocouples (AD594) and the 1250°C for type K thermocouples (AD595).

Common-mode voltages on the thermocouple inputs must remain within the common-mode range of the AD594/AD595, with a return path provided for the bias currents. If the thermocouple is not remotely grounded, then the dotted line connections in Figures 1 and 2 are recommended. A resistor may be needed in this connection to assure that common mode voltages induced in the thermocouple loop are not converted to normal mode.

THERMOCOUPLE CONNECTIONS

The isothermal terminating connections of a pair of themocouple wires forms an effective reference junction. This junction must be kept at the same temperature as the AD594/AD595 for the internal cold junction compensation to be effective.

A method that provides for thermal equilibrium is the printed circuit board connection layout illustrated in Figure 3.

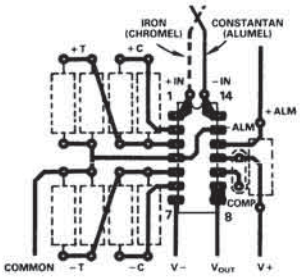


Figure 3. PCB Connections

Here the AD594/AD595 package temperature and circuit board are thermally contacted in the copper printed circuit board tracks under pins 1 and 14. The reference junction is now composed of a copper-constantan (or copper-alumel) connection and copper-iron (or copper-chromel) connection, both of which are at the same temperature as the AD594/AD595.

The printed circuit board layout shown also provides for placement of optional alarm load resistors, recalibration resistors and a compensation capacitor to limit bandwidth.

To ensure secure bonding the thermocouple wire should be cleaned to remove oxidation prior to soldering. Noncorrosive rosin flux is effective with iron, constantan, chromel and alumel and the following solders: 95% tin-5% antimony, 95% tin-5% silver or 90% tin-10% lead.

FUNCTIONAL DESCRIPTION

The AD594 behaves like two differential amplifiers. The outputs are summed and used to control a high-gain amplifier, as shown in Figure 4.

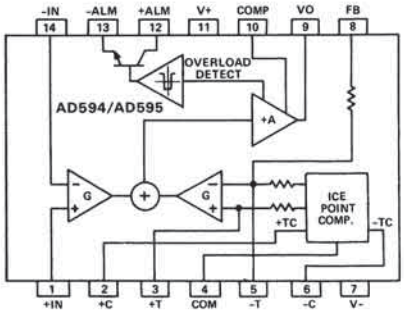


Figure 4. AD594/AD595 Block Diagram

In normal operation the main amplifier output, at pin 9, is connected to the feedback network, at pin 8. Thermocouple signals applied to the floating input stage, at pins 1 and 14, are amplified by gain G of the differential amplifier and are then further amplified by gain A in the main amplifier. The output of the main amplifier is fed back to a second differential stage in an inverting connection. The feedback signal is amplified by this stage and is also applied to the main amplifier input through a summing circuit. Because of the inversion, the amplifier causes