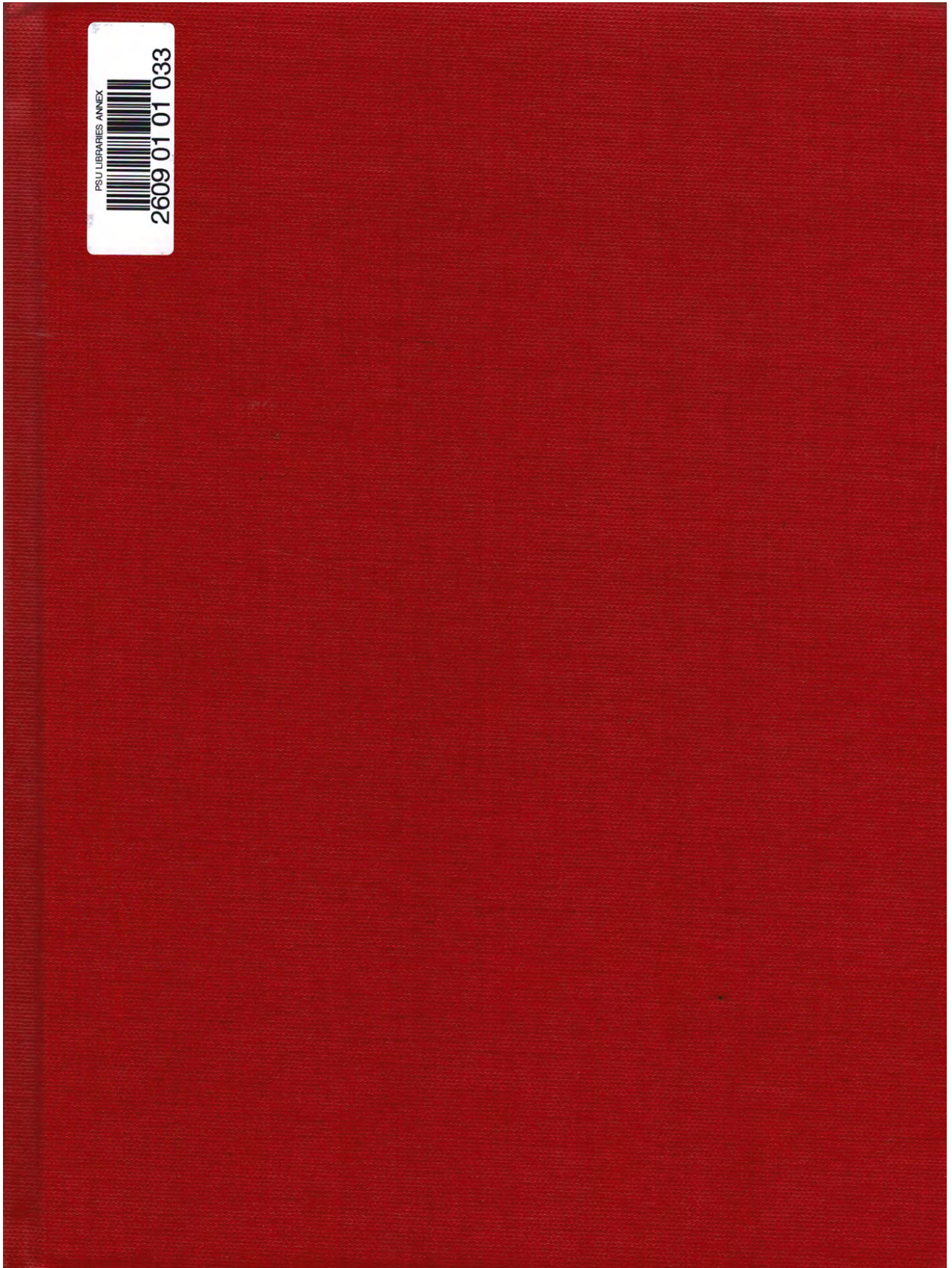




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A 1.9-GHz Wide-Band IF Double Conversion CMOS Receiver for Cordless Telephone Applications

Jacques C. Rudell, *Student Member, IEEE*, Jia-Jiunn Ou, *Student Member, IEEE*, Thomas Byunghak Cho, *Member, IEEE*, George Chien, *Student Member, IEEE*, Francesco Brianti, Jeffrey A. Weldon, *Student Member, IEEE*, and Paul R. Gray, *Fellow, IEEE*

Abstract—A monolithic 1.9-GHz, 198-mW, 0.6- μm CMOS receiver which meets the specifications of the Digital Enhanced Cordless Telecommunications (DECT) standard is described. All of the RF, IF, and baseband receiver components, with the exception of the frequency synthesizers, have been integrated into a single chip solution. A description is given of a wide-band IF with double conversion architecture which eliminates the need for the discrete-component noise and IF filters in addition to facilitating the eventual integration of the frequency synthesizer blocks with on-chip VCO's. The prototype device utilizes a 3.3-V supply and includes a low noise amplifier, an image-rejection mixer, and two quadrature baseband signal paths each of which includes a second-order Sallen and Key anti-alias filter, an eighth-order switched-capacitor filter network followed by a 10-b pipelined analog-to-digital converter (ADC). The experimental device has a measured receiver reference sensitivity of -90 dBm, an input referred IP3 of -7 dBm, a $P_{1\text{ dB}}$ of -24 dBm, and an image-rejection ratio of -55 dBc across the DECT bands.

Index Terms—Analog-to-digital converters, anti-alias filters, CMOS RF, Digital Enhanced Cordless Telecommunications, image-rejection mixers, low noise amplifiers, mixers, monolithic, radio architectures, radio receivers, switched-capacitor filters, wide-band IF double conversion, wireless communications.

I. INTRODUCTION

THE proliferation of cellular, cordless, and PCS applications has driven the demand for portable communication systems which share the common requirement of a low-cost, low-power, small form-factor transceiver [1]. To address this need, recent research has been focused toward the development of a monolithic transceiver using a low-cost CMOS technology [2]–[7]. A single-chip CMOS transceiver requires the exploration of new systems and circuit design techniques which facilitate the highest levels of receiver and transmitter integration.

Commensurate with this trend toward integration is the evolution of numerous RF standards which define the specifications of any given transceiver. A single future portable

communication system may well require the ability to utilize both the services provided by multiple RF standards and the flexibility afforded through multimodal operation. This consequently will demand the capability by a *single* transceiver to operate on standards with various carrier frequencies, channel bandwidths, sensitivity, and selectivity requirements. The increased functionality offered by a large high-integration system will be well suited to address the needs of a multimodal transceiver.

This paper describes a receiver system that achieves high levels of integration while exhibiting features potentially allowing operation on multiple RF standards. A prototype device based on this new wide-band IF double conversion (WBIFDC) architecture was realized in a 0.6- μm double-poly, triple-metal CMOS process and runs off of a 3.3-V supply. The experimental receiver, designed for specifications of the Digital Enhanced Cordless Telecommunications (DECT) standard, operates on a 1.9-GHz carrier and has the capability of detecting a signal amplitude of a microvolts at the low noise amplifier (LNA) input and generating a 10-b digital representation of the desired baseband channel. All of the required components to convert the desired signal from RF to baseband, with the exception of the frequency synthesizers, are integrated onto the prototype device which includes an LNA, an image-rejection mixer, two baseband filter stages, and two analog-to-digital converters (ADC).

Section II provides a brief review of two well-known receiver systems and introduces the wide-band IF with double conversion architecture. Section III provides an extended description of the wide-band IF system examining the merits and nonidealities of this architecture. Section IV discusses CMOS implementation issues of the wide-band IF system for the DECT standard. Finally, Section V presents test results obtained from the prototype device followed by a few concluding comments.

II. RECEIVER ARCHITECTURES

Many issues are involved when attempting to translate a discrete-component receiver into an integrated form. To understand some of the barriers to integration, a review is given of a traditional superheterodyne system. Then two approaches to integration, a homodyne receiver and the wide-band IF with double conversion architectures are evaluated. Although there have been many recently proposed integrated architectures [6], [8], for the sake of brevity, only direct

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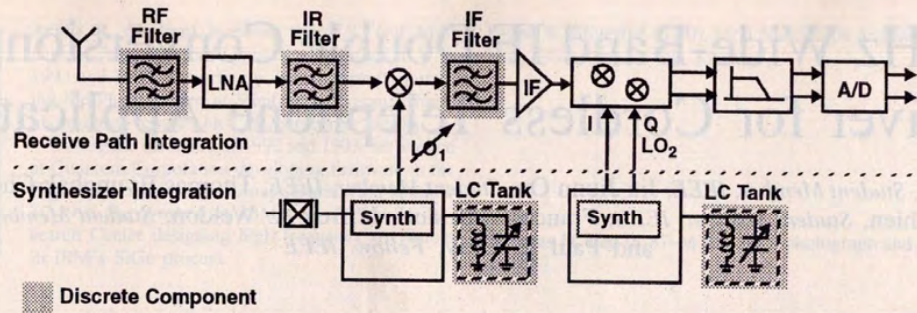


Fig. 1. Conventional superheterodyne receiver architecture.

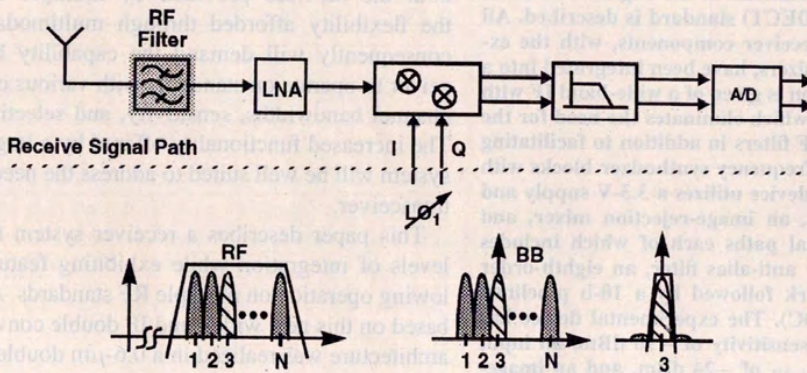


Fig. 2. Direct conversion receiver architecture.

conversion and wide-band IF with double conversion will be considered.

A. Conventional Superheterodyne Receiver

Most RF communication transceivers manufactured today utilize a conventional superheterodyne approach. In this system, shown in Fig. 1, implementation is achieved with a collection of discrete-component filters and various technologies such as gallium arsenide, silicon bipolar, and CMOS. The discrete-component RF front-end filter serves to remove out-of-band energy and perform rejection of image-band signals. The noise or image-rejection filter, which follows the LNA, further attenuates the undesired signals present at the image frequencies. An RF channel-select frequency synthesizer tunes the desired band to a fixed IF where a discrete-component filter performs a first-order attenuation of alternate channel energy. The IF filter, typically in combination with a variable gain amplifier, reduces the distortion and dynamic range requirements of the subsequent receiver blocks. High-performance, low phase-noise voltage controlled oscillators (VCO) are typically realized with discrete-component high- Q inductors and varactor diodes.

The high- Q associated with the discrete components found on a superheterodyne receiver is difficult and somewhat impractical to realize at high frequency as an integrated solution. A superior performance with respect to *selectivity*, a measure of a receiver's ability to separate the desired band about the carrier from signals received at other frequencies, and *sensitivity*, the minimal signal at the receiver input such

that there is a sufficient signal-to-noise ratio at the receiver output [9], [10], can only be achieved with the use of high- Q discrete components found on a superheterodyne receiver. However, using these components runs contrary to the goal of high integration required by modern portable communication systems.

The challenge of fully integrating a receiver is to replace the functions traditionally implemented with the high performance, high- Q discrete components with integrated on-chip solutions. Problems associated with full integration of the receiver can be separated into two categories. First, the integration of the receive signal path requires the elimination of the noise or image-rejection filter and the discrete-component IF filter (see Fig. 1). Second, a fully integrated low-phase noise channel-select synthesizer must be realized using the relatively low- Q and poor phase-noise performance associated with on-chip VCO's. Two architectures which address the issues related to integration will now be discussed.

B. Direct Conversion Receiver (Homodyne)

One receiver architecture that eliminates many off-chip components in the receive signal path is the direct conversion, or homodyne architecture. In this approach, shown in Fig. 2, all of the in-band potential channels are frequency translated from the carrier directly to baseband using a single mixer stage. Energy from undesired channels is easily removed with on-chip filtering at baseband. In a direct conversion receiver, the IF stage is eliminated as is the need for image-rejection filtering.

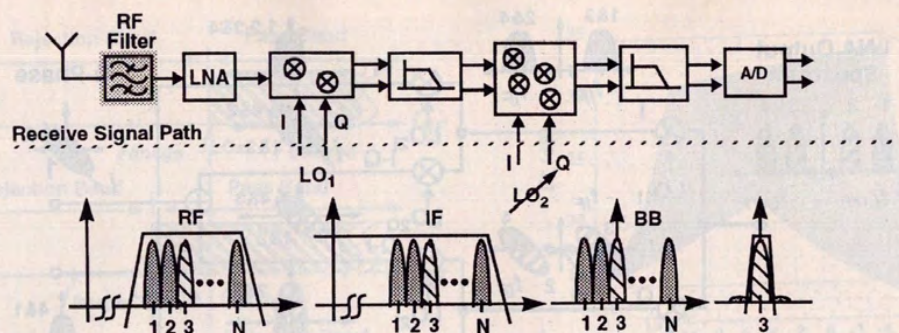


Fig. 3. Wide-band IF with double conversion receiver architecture.

TABLE I
RELATIVE COMPARISON OF RECEIVER ARCHITECTURE

Receiver Architecture	Required Discrete Filters	Channel Select Synthesizer	Potential for Multi-modal use	Channel Filtering	Image-Rejection
Superheterodyne	RF, Noise, IF	RF	Low	IF	RF & Noise Filter
Direct Conversion	RF	RF	High	Baseband	N/A
Wide-Band IF	RF	IF	High	Baseband	RF Filter & IR Mixer

Although the direct conversion receiver allows for higher levels of integration than a superheterodyne system, problems are associated with this architecture. Because the local oscillator (LO) is at the same frequency as the RF carrier, the potential exists for LO leakage to either the mixer input or to the antenna where radiation may occur. The unintentionally transmitted LO signal may reflect off of nearby objects and be "re-received," consequently self-mixing with the local oscillator resulting in a time-varying or "wandering" dc offset at the output of the mixer [11]. This time-varying dc offset together with inherent circuit offsets significantly reduces the dynamic range of the receiver. In addition, a direct conversion receiver requires a high-frequency, low phase-noise, channel-select frequency synthesizer, which is difficult to achieve with a relatively low- Q integrated VCO.

C. Wide-Band IF with Double Conversion Receiver

An alternative architecture well suited for integration of the entire receiver is wide-band IF with double conversion [7]. Shown in Fig. 3, this receiver system takes all of the potential channels and frequency translates them from RF to IF using a mixer with a single frequency local oscillator. A simple low-pass filter is used at IF to remove any upconverted frequency components, allowing all channels to pass to the second stage of mixers. All of the channels at IF are then frequency translated directly to baseband using a tunable, channel-select frequency synthesizer. Alternate channel energy is then removed with a baseband filtering network where variable gain may be provided. This approach is similar to a superheterodyne receiver architecture in that the frequency translation is accomplished in multiple steps. However, unlike a conventional superheterodyne receiver, the first local oscilla-

tor frequency translates all of the receive channels, maintaining a large bandwidth signal at IF. The channel selection is then realized with the lower frequency tunable second LO. As in the case of direct conversion, channel filtering can be performed at baseband, where digitally-programmable filter implementations can potentially enable more multistandard-capable receiver features.

In summary, Table I provides a high level comparison between the three receiver architectures discussed. Clearly, the highest performance receiver with respect to sensitivity and selectivity is the conventional superheterodyne architecture. However, the superior performance of this system is provided only with discrete-component solutions. In addition, the narrow-band discrete-component channel filters of the superheterodyne receiver tailor the particular implementation to a specific standard. Moreover, future portable transceivers will require smaller form factors which can be provided only through integrated solutions.

With respect to the two integrated architectures discussed, both direct conversion and wide-band IF perform channel filtering at baseband, allowing the possibility of a programmable integrated channel filter for multistandard receiver applications. In addition, as discussed in Section III, the wide-band IF architecture facilitates the integration of the synthesizer section of the receiver and provides a programmable image-rejection mixer.

III. WIDE-BAND IF ARCHITECTURE: EXTENDED DISCUSSION

The wide-band IF architecture offers two potential advantages with respect to integrating the frequency synthesizer over a direct conversion approach. The most important advantage is the fact that the channel tuning is performed using the second

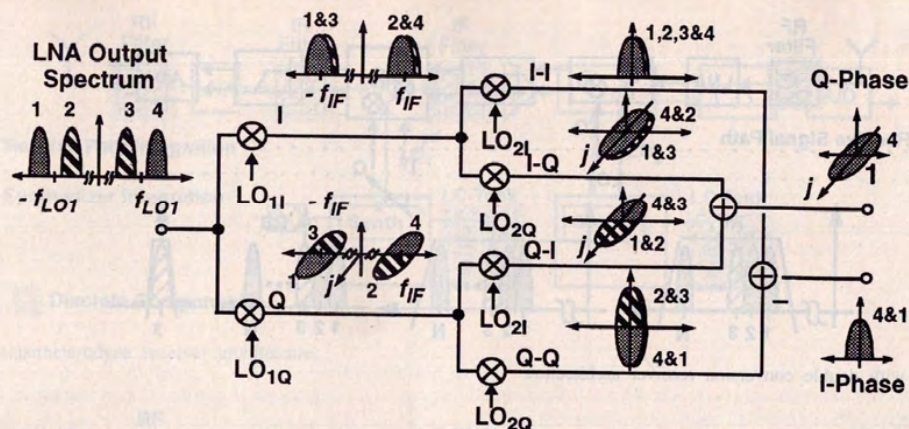


Fig. 4. Frequency domain interpretation of the wide-band IF image-rejection mixer. Low-pass filters not shown for simplicity.

lower-frequency, or IF, local oscillator but not the first, or RF, synthesizer. Consequently, the RF local oscillator can be implemented as a fixed-frequency crystal-controlled oscillator where several techniques may be utilized which allow the realization of low phase noise in the local oscillator output with low- Q on-chip components. One such approach is the use of wide phase-locked loop (PLL) bandwidth in the synthesizer to suppress the VCO contribution to phase noise near the carrier [12]–[14].

In addition, since channel tuning is performed with the IF local oscillator, operating at a lower frequency, a reduction in the required divider ratio of the phase-locked loop necessary to perform channel selection results. The noise generated by the reference oscillator, phase detector, and divider circuits of a PLL all contribute to the phase noise performance of a frequency synthesizer. With a lower divider ratio, the contribution to the frequency synthesizer output phase noise from the reference oscillator, phase detector, and divider circuits can be significantly reduced. Moreover, a lower divider ratio implies a reduction in spurious tones generated by the PLL [15], [16].

Another advantage associated with the wide-band IF architecture is that there are no local oscillators which operate at the same frequency as the incoming RF carrier. This eliminates the potential for the LO retransmission problem that plagues a direct conversion system and results in *time-varying* dc offsets. Although the second local oscillator is at the same frequency of the IF desired carrier in the wide-band IF system, the offset which results at baseband from self mixing is relatively constant and may be cancelled using one of the proposed methods described in [17] and [18].

A. Image-Rejection in the Wide-Band IF System

In the wide-band IF receiver, the signal is mixed to a finite IF; therefore, the image problem is reintroduced in this system. However, because the two frequency translations occur in cascade, the architecture used lends itself to easy implementation of the image-reject function using a six-mixer configuration. This image-rejection mixer which shares a similarity to the Weaver technique [19] is best understood

with a frequency domain interpretation for a real valued input signal (Fig. 4). The RF carrier is first multiplied by in-phase and quadrature local oscillators and converted to IF. The spectrum at IF is the result of a convolution in the frequency domain of the RF carrier with both a sine and cosine. At IF, there exists a known phase relationship between the image and desired frequency bands. This phase relationship is further exploited with a complex mixing from IF to baseband. If the upconverted terms from the mixer are removed by low-pass filtering at IF and baseband, then by properly adding the four baseband channels in pairs, the image frequencies can be made to cancel while the desired band adds constructively for both the I and Q channels. This image-rejection mixer has the property that any incoming frequency below the frequency of the first local oscillator ideally is rejected, while any frequency above the first LO is passed. If the IF is made high enough, additional image rejection may be obtained from the RF front-end filter.

This particular image-rejection mixer topology has several advantages. First, lossy passive phase-shifting filters are not required in the signal path to generate the correct phase between the image and desired bands. Second, assuming again that the upconverted terms are removed, the image-rejection is very wide-band. It can be further shown that the edge of the image-attenuation band is set by the frequency of the first local oscillator (LO1) which leads to the third advantage. If it is assumed that a multistandard capable receiver is built where the frequency of LO1 can perform a coarse adjustment to accommodate the carrier frequency of a different standard, then the image rejection will follow the first LO, or it can be thought of as a self-aligning image-rejection mixer. Two hypothetical LO1 frequencies, labeled f_{LO1a} and f_{LO1b} , necessary to properly frequency translate the carrier of two different standards are shown in Fig. 5(a) and (b). Both the passband and the rejection band as a function of the frequency referred to the mixer input are aligned to LO1. Assuming that the desired band is above LO1 in frequency, the image-rejection will be self aligned. Further flexibility using this mixer configuration may be obtained by reversing the polarity of the four baseband channels before they are summed together at the mixer output. This has the effect of retaining the lower

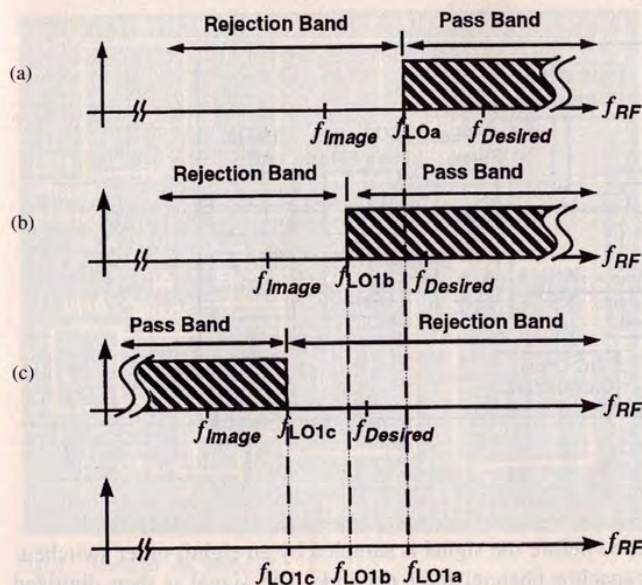


Fig. 5. Self-aligning image-rejection mixer. (a) f_{LO1a} and (b) f_{LO1b} two different LO1 frequencies and their relationship to the rejection and pass band of the image-rejection mixer. (c) f_{LO1c} case when the polarity of the baseband channels are reversed before the summation.

sideband about LO1 while rejecting the upper sideband. This concept is illustrated in Fig. 5(c).

B. Nonidealities of the Wide-Band IF Double Conversion System

Although the wide-band IF system has advantages with respect to high integration, certain nonidealities limit the overall receiver performance. These are now discussed.

Because the first local oscillator is fixed in frequency, all of the channels must pass through the IF stage and the desired channel is selected with the second LO. This has two problematic implications. First, as a result of moving the channel selection to a lower frequency, the IF synthesizers require a VCO with the capability of tuning across a broader frequency range as a percentage of the nominal operating frequency. Second, by removing the channel select filter at IF, strong adjacent channel interferers are now a concern for the second mixer stage as well as the baseband blocks. This implies a higher dynamic range requirement of these latter receiver stages. In addition, spurious tones generated by the IF local oscillator can mix with undesired IF channels creating in-band interference at the output of the second mixer stage. Additional care must be taken when developing a frequency plan to guard against digital baseband clock signals and their harmonics falling within the range of the desired IF channels.

As with conventional image-rejection mixer systems [20]–[24], the magnitude of the image attenuation in the wide-band IF architecture is a function of the phase mismatch between both the I and Q phase of the first and second local oscillators and the gain matching between the signal paths. A detailed derivation for the image-rejection performance as a function of phase and gain mismatch is given in Appendix A.

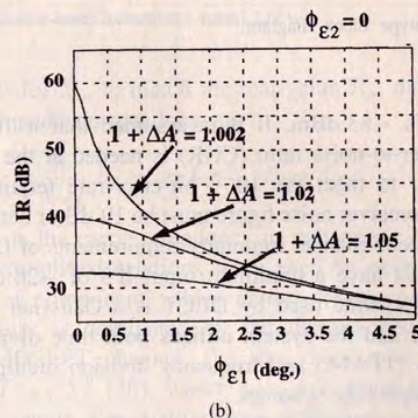
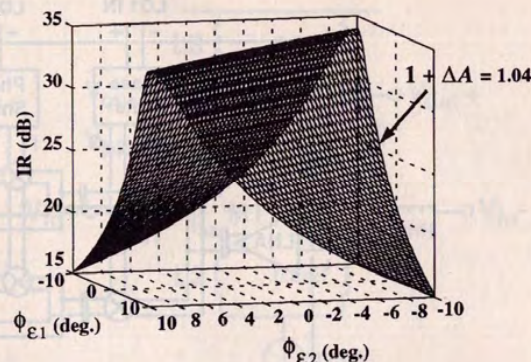


Fig. 6. Image rejection as a function of LO phase mismatch. (a) Illustrating IR dependence on ϕ_{E1} and ϕ_{E2} . (b) IR as a function of ϕ_{E1} and gain mismatch, $\phi_{E2} = 0$.

The image rejection as a function of the mismatch is given by

$$IR(\text{dB}) = 10 \cdot \log \left[\frac{1 + (1 + \Delta A)^2 + 2(1 + \Delta A) \cos(\phi_{E1} + \phi_{E2})}{1 + (1 + \Delta A)^2 - 2(1 + \Delta A) \cos(\phi_{E1} - \phi_{E2})} \right] \quad (1)$$

where ϕ_{E1} and ϕ_{E2} represent the deviation of the local oscillators from quadrature in the first and second LO's, respectively, while ΔA is the aggregate gain error along the I and Q signal paths. A plot of (1) is given in Fig. 6. With a sufficiently high intermediate frequency, the image-rejection may be performed with a combination of the RF front-end filter and this image-rejection mixer. Using this approach, most applications will require better than 35 dB of image-rejection from the six-mixer configuration. Under perfect gain matching, the phase error of the local oscillator can be no greater than 2° while with perfect phase matching the gain error between any two of the four signal paths must be less than 3.6%.

IV. DECT PROTOTYPE RECEIVER

A prototype receiver utilizing the wide-band IF architecture was designed to meet the specifications of the DECT standard [25]. In DECT, there are ten channels which are 1.728 MHz wide with carrier frequencies that range from 1.881–1.897 GHz. The required receiver reference sensitivity

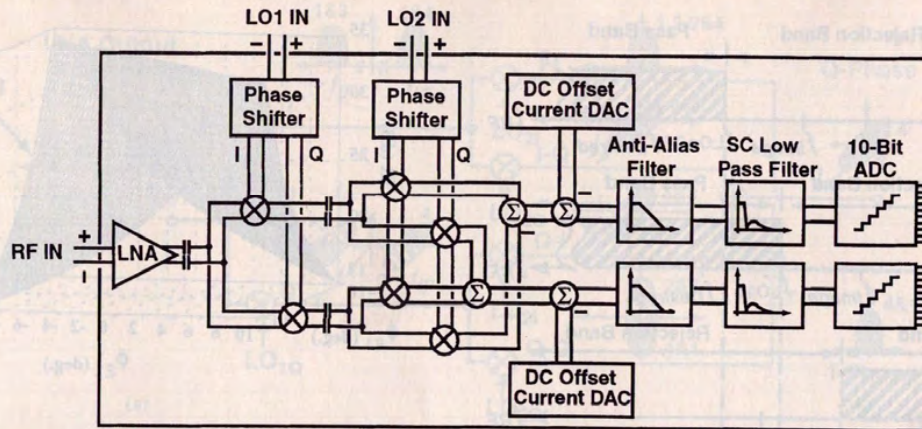


Fig. 7. Prototype block diagram.

of DECT is -83 dBm. If it is assumed that a 10.3 dB or better carrier-to-noise ratio (CNR) is needed at the output of the receiver to meet the 10^{-3} bit-error-rate requirement of DECT, the receiver noise figure must be 19 dB or better. Based on the adjacent channel immunity requirements of DECT, the receiver must have a minimum input IP3 of -26 dBm. The modulation scheme used by DECT is a Gaussian minimum shift keying and the system utilizes both time division multiple access (TDMA) and frequency division multiple access (FDMA) duplexing schemes.

As mentioned later in the mixer section, the intermediate frequency for the desired carriers reside from 181 – 197 MHz. Given that the carrier frequency is at 1.89 GHz, the image signals fall in the 1.503 – 1.519 GHz band. In DECT, the receiver is required to properly detect a -80 dBm carrier in the presence of an out-of-band blocker -23 dBm below 1.78 GHz [25]. Therefore, to obtain the required CNR in the presence of the 1.5 GHz out-of-band blocker, the image-rejection can be expressed as

$$IR(\text{dB}) = \text{CNR}(\text{dB}) + (\text{Blocker}_{1.5\text{ GHz}}(\text{dBm}) - \text{DesiredCarrier}(\text{dBm})). \quad (2)$$

Therefore, for this particular receiver implementation of DECT, approximately 70 dB or more of image-rejection is required.

A. Prototype Description

A diagram of all the blocks included on the prototype chip is shown in Fig. 7. At the RF and LO signal ports of the receiver, a single-ended-to-differential conversion takes place with an external balun allowing the higher frequency signals to be brought on-chip differentially. To reduce the impact of coupling between blocks in the receiver, the entire signal path across the chip was made fully differential. The LNA is ac-coupled to the input of the RF mixers, while the first mixer stage is ac-coupled to the second set of mixers. At baseband, two offset current digital-to-analog converters (DAC's) are used to mitigate any effect due to LO self-mixing in the second mixer stage. A Sallen and Key anti-aliasing filter is

used before the signal is sampled by an eighth-order switched-capacitor channel filter network. The signal is then digitized using a 10 -b, 10 MS/s ADC. The digital output is driven off-chip using source-coupled logic to reduce the effects of digital substrate noise coupling. Quadrature LO's are realized with a second-order polyphase filter before being applied to the mixer input [24]. The wide-band IF architecture is intended to be eventually integrated with the frequency synthesizer. Therefore, the polyphase filters found on this prototype are for testing purposes only.

All circuits on this chip use a 3.3 -V supply. All pads are electrostatic discharge (ESD) protected with reversed-biased PN diodes including the LNA input. To further reduce the possibility of coupling effects due to parasitic bondwire inductances, a self-biased on-chip current source is replicated throughout the RF and IF sections of the receiver. This bias circuit which includes an adjustable current DAC is further described in [26] and [27]. All bias circuits, gain control for the RF, and baseband sections, as well as the ADC clocking frequency and various other options are controlled by two sets of 50 -b serial-input shift registers.

A die photo is shown in Fig. 8. The chip was fabricated in a 0.6 - μm double-poly, triple-metal CMOS process. The die size is 7.5 mm by 6.5 mm while the active chip area is 15 mm². A description of each circuit block in the receiver chain will now be given starting with the LNA.

B. Low Noise Amplifier (LNA)

Essential requirements of the LNA are low noise, high linearity, moderate gain, and low power consumption. Since the linearity performance is dominated by the stages which follow the LNA, the primary goal in this LNA design is to minimize the power consumption for the required noise figure. In a standard 0.6 - μm CMOS process, the device f_T is typically below 10 GHz when biased at 0.5 V ($V_{gs} - V_t$). This makes the conventional wide-band approach somewhat impractical and a narrow-band design an attractive alternative. In addition, the bandpass frequency response of a narrow-band LNA helps to perform some image-attenuation and increases the immunity of the front-end to low-frequency digital baseband signals. To

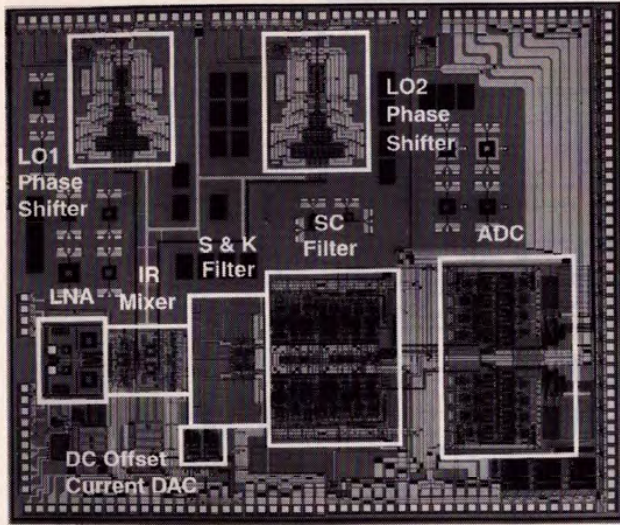


Fig. 8. Receiver die photo

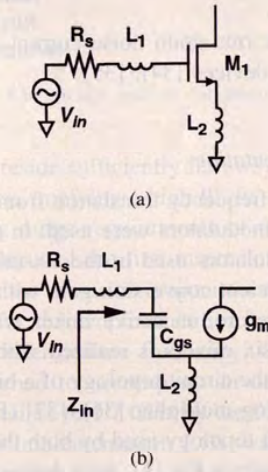


Fig. 9. Inductor-degenerated common-source LNA: (a) topology and (b) small signal model.

realize this approach, an inductively degenerated common-source amplifier topology [28], [29] was selected, as shown Fig. 9(a). This configuration has the advantage that it provides both current gain and voltage gain, thus reducing the noise contribution of the following stages. Moreover, by utilizing inductive degeneration, a real-part impedance matching is achieved without the use of a physical resistor, which would degrade the LNA's noise figure.

The actual noise performance of the LNA is heavily influenced by nonidealities in devices and passive components, which are difficult to fully model. However, some insight can be obtained from an ideal circuit model, shown in Fig. 9(b), where C_{gd} is neglected and R_s is the source impedance. The input impedance may now be expressed as

$$Z_{in} = j\omega(L_1 + L_2) + \frac{1}{j\omega C_{gs}} + \frac{g_m}{C_{gs}} L_2. \quad (3)$$

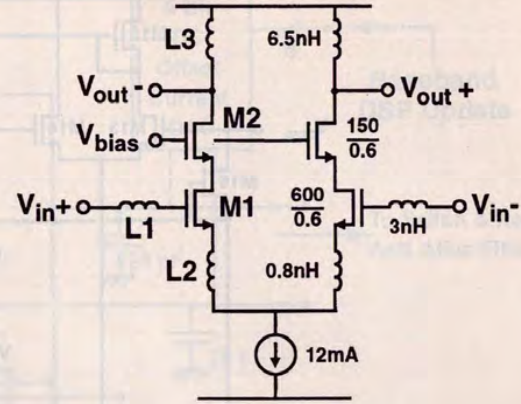


Fig. 10. Narrow-band inductively tuned LNA.

In order for Z_{in} to match the real-value R_s , the conditions for this impedance matching are

$$R_s = \frac{g_m}{C_{gs}} L_2 = \omega_T L_2; \quad (L_1 + L_2)C_{gs} = \frac{1}{\omega_c^2} \quad (4)$$

where ω_c is the carrier frequency in radians/s.

These simplified relations were used to obtain an initial estimate of component values in the design. Assuming the device noise is dominated by the thermal noise produced by the MOSFET channel, the rms drain noise current is $i_d^2 = 4kT\gamma g_m \Delta f$ [30], where $\gamma = 2/3$ when based in the saturation region. The quality factor of the entire input network is

$$Q_{in} = \frac{1}{R_s} \frac{1}{\omega_c C_{gs}} = \frac{1}{R_s} \omega_c (L_1 + L_2). \quad (5)$$

Now the input-referred noise figure (NF) under a matched condition can be expressed as

$$NF = 1 + \gamma \frac{1}{R_s} \frac{1}{g_m} \frac{1}{Q_{in}^2}. \quad (6)$$

Equation (6) shows that the NF can be reduced by increasing Q_{in} , breaking the classical tradeoff between noise figure and power consumption of the LNA. This now allows the LNA linearity to be traded-off with the noise figure for a given power consumption.

The complete implementation of the LNA is shown in Fig. 10. A differential configuration was selected to improve the common-mode rejection of spurious digital noise and substrate noise coupling. Cascode device M_2 provides better reverse isolation and alleviates the effect of C_{gd} of M_1 . The relatively high- Q parasitic inductance associated with the LNA input bondwires were used to realize L_1 . However, due to the differential configuration along with the desire to integrate all elements of the LNA, L_2 was implemented as an on-chip low- Q spiral inductor.

A key advantage associated with this highly integrated receiver architecture is that the 50- Ω matching is not required at the LNA output. Therefore, a spiral inductor L_3 was used at the LNA output to tune out the capacitance associated with the mixer input. This results in an enhancement of the output impedance and LNA voltage gain.

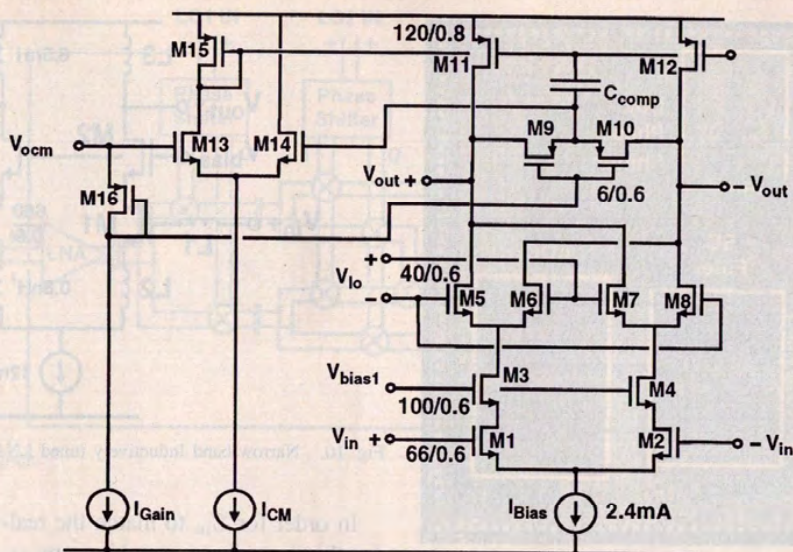


Fig. 11. One of two mixers used to translate the RF signal to IF, CMOS variant of the Gilbert cell multiplier.

On-chip spiral inductors [32] were created with the top two layers of metal, while the bottom layer of metal was used as the bridge connecting the center of the spiral to an outside terminal. Greenhouse formulas [33] were used for the initial design while EM, a commercial software package by Sonnet, performed a $2\frac{1}{2}$ -dimension electromagnetic simulation to confirm the final design. The result was transformed to a simple π model which was then used for the final circuit simulation in SPICE.

Actual LNA performance is different from the idealized model because of the nonidealities in active and passive components. As the operating frequency approaches the device f_T , the assumption of the MOSFET quasi-static behavior no longer holds. A first-order nonquasi-static (NQS) model can be applied to the circuit simulation by adding a resistor in series with the gate terminal, $R_{nqs} = 1/(5g_m)$ [31]. To improve the LNA noise figure, Q_{in} can be increased by decreasing the input device size which reduces C_{gs} . However, if the device size is too small, R_{nqs} becomes significant, increasing the overall noise figure. Ideally, an optimal Q_{in} can be achieved by balancing between the noise from the MOSFET channel and the noise which results from the NQS behavior. However, increasing Q_{in} implies large values of inductors. For this design, both on-chip spiral and bondwire inductors limited Q_{in} to approximately two to three.

In addition to the noise contribution of device M_1 , the overall noise figure is further degraded by the cascode device M_2 and a finite Q of the inductors. The noise from M_2 is nonnegligible because at high frequency the impedance looking into the drain of M_1 is low. Simulation results show the noise contribution from M_2 is approximately 2/3 of the noise contribution from M_1 .

Compared to a simulated NF of 3.5 dB, the observed noise figure of the individual LNA testing chip is 5 dB. This discrepancy mainly results from the inadequate thermal noise model of the short channel MOSFET devices. The assumption

of $\gamma = 2/3$ in the rms drain noise current may not be valid for short-channel devices [34], [35].

C. Mixer Implementation

To perform the frequency translation from RF to baseband, down-conversion modulators were used. In addition to image rejection, the modulators used in the six-mixer configuration must provide sufficient conversion gain with a minimal noise contribution. Therefore, an active mixer was selected. Each of the individual six mixers is realized with a CMOS active mixer resembling the circuit topology of a bipolar Gilbert cell four-quadrant analog multiplier [36], [37] (Fig. 11).

The basic circuit topology used by both the first and second mixer stages is shown in Fig. 11, with the exception that triode region devices M_9 and M_{10} are replaced with p^+ diffusion resistors in the second mixer stage. The input transconductance stage consists of a simple differential pair M_1 and M_2 . The cascode devices M_3 and M_4 provide better LO-to-RF isolation. M_5 – M_8 act as switches in the mixer. Triode region devices M_9 and M_{10} are used to set both the load and the gain which may be modulated on-chip by varying the current through diode-connected device M_{16} . Common-mode feedback is achieved with devices M_{13} , M_{14} , M_{15} , and the current source consisting of M_{11} and M_{12} . Compensation for the common-mode feedback loop is provided with C_{comp} . To remove any dc offsets from the first mixer and accommodate a level shift between the output of the first mixer stage and the input to the LO2 mixers, a 2.6-pF coupling capacitor was used (see Fig. 12).

Selection of the local oscillator and IF frequencies involves several tradeoffs. Gain and phase mismatch within the signal paths of the mixer limit the practical image attenuation to 35 dB. Therefore, to meet the image-rejection requirement of 70 dB, some filtering must be performed by the front-end RF filter. However, to make full use of this filter, the

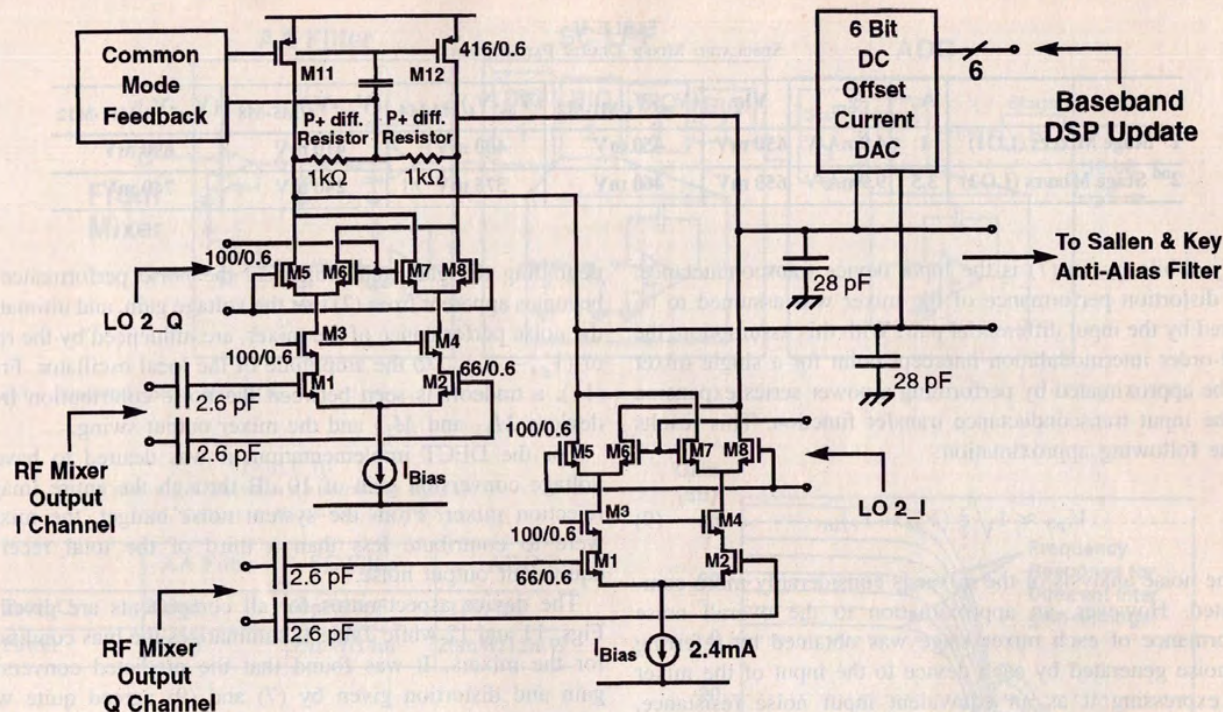


Fig. 12. Two of the four mixers used in the second mixer stage using LO2.

image-band must reside sufficiently far away from the desired carrier in frequency, implying a high IF. In addition, a high IF reduces the tuning range requirements of the IF synthesizer. In contrast, the output of the first mixer is a high impedance node. Therefore, the parasitic capacitance and the silicon technology used for this implementation set an upper bound on the allowable intermediate frequency. Originally, the RF mixers were designed to accompany an on-chip synthesizer where LO1 was limited to 1.7 GHz by the 0.6- μm technology. Therefore, in this implementation LO1 was set to 1.7 GHz requiring LO2 to range from 181–197 MHz.

To remove the upconverted terms, a low-pass filter is required at the IF node. The output resistance of the RF mixers in combination with the parasitic capacitance at the IF node together create the required RC time constant. Unfortunately, a problem associated with this particular implementation of the wide-band IF system is that at the first mixer output, the 3 dB frequency is 160 MHz which is much lower than desired. At IF, the desired channels range from 181–197 MHz which implies a significant gain penalty for the RF mixers. Using a 0.6- μm CMOS technology, the drain junction capacitance of the switches and the current source at the output of the first mixer, the gate capacitance of the input devices of the second mixer stage, and the parasitic capacitance of the ac-coupling capacitor severely limit the bandwidth and the gain of the mixer.

The output current from two of the four IF-to-baseband mixers are added together to correctly sum the signals for image cancellation, as shown in Fig. 12. A pair of 6-b dc offset current DAC's are then used to mitigate the effects of any LO2 self-mixing and to compensate for dc offset

in the subsequent baseband switched-capacitor filter stages. The offset current DAC on this chip can be updated with a baseband DSP using an algorithm as described in [17] and [18]. At the current summing node, the first pole of the anti-alias filter is created with the mixer output resistance loaded by a 28-pF capacitor. The low-pass filter created at the output of the first mixer stage in combination with the Sallen and Key filter serve a dual purpose, to remove the upconverted IF mixer components and perform anti-alias filtering for the subsequent switched-capacitor blocks.

Similar to the LNA, physical insight may be gained when designing each of the individual mixer cells by creating an idealized model. Simplified expressions for the voltage conversion gain, input referred voltage IP3, and equivalent input noise contribution from each device in the mixer are given with (8)–(11). These relationships were used to make initial estimates before simulation in SPICE.

Assuming a square-law MOSFET device, the conversion gain of an individual mixer can be approximated by averaging the gain over one period of the local oscillator, as shown in Appendix B. This results in the following analytical expression:

$$A_v \approx g_m R_L \left(\frac{2}{\pi} \right) \left(1 - \frac{\sqrt{2}(V_{gs} - V_t)_{sw}}{\pi V_{LO}} \right) \quad (7)$$

or

$$A_v \approx \frac{I_{Bias}}{(V_{gs} - V_t)_{in}} R_L \left(\frac{2}{\pi} \right) \left(1 - \frac{\sqrt{2}(V_{gs} - V_t)_{sw}}{\pi V_{LO}} \right) \quad (8)$$

where $(V_{gs} - V_t)_{in}$ and $(V_{gs} - V_t)_{sw}$ are the $(V_{gs} - V_t)$ of the input devices M_1 and M_2 and the switches M_5 – M_8 , respec-

TABLE II
SIMULATED MIXER DESIGN PARAMETERS

	A_v	g_m	V_{lo}	$(V_{gs}-V_t)_{M1-M2}$	$(V_{gs}-V_t)_{M3-M4}$	$(V_{gs}-V_t)_{M5-M8}$	$(V_{gs}-V_t)_{M11-M12}$
1 st Stage Mixers (LO1)	1	4.9mA/V	650 mV	450 mV	400 mV	410 mV	690 mV
2 nd Stage Mixers (LO2)	3.5	9.9mA/V	650 mV	460 mV	375 mV	240 mV	740 mV

tively, while g_m in (7) is the input device transconductance. The distortion performance of the mixer was assumed to be limited by the input differential pair. With this assumption, the third-order intermodulation intercept point for a single mixer can be approximated by performing a power series expansion on the input transconductance transfer function. This results in the following approximation:

$$V_{ip3} \approx 4\sqrt{\frac{2}{3}} (V_{gs} - V_t)_{in}. \quad (9)$$

The noise analysis of the mixer is considerably more complicated. However, an approximation to the overall noise performance of each mixer stage was obtained by referring the noise generated by each device to the input of the mixer and expressing it as an equivalent input noise resistance, where the equivalent input rms noise voltage is given by $v_{eqin}^2 = 4kTR_{eqin}\Delta f$.

Noise generated by the LNA in the image-band will to first-order be cancelled when going through the image-rejection mixer. Devices M_1 – M_8 in the first mixer stage add noise which is uncorrelated as the noise passes through the image-rejection mixer. Therefore, devices M_1 – M_8 in the first mixer stage are single sideband (SSB) noise sources, while all other devices in the receive path are double sideband (DSB) noise sources.

The equivalent input noise resistance generated by devices M_1 and M_2 is described as

$$R_{eqin} \approx 2 \left(\gamma \cdot \frac{(V_{gs} - V_t)}{I_{Bias}} \right) \cdot k \quad (10)$$

where $k = 2$ (SSB) for the first mixer stage (LO1) and $k = 1$ (DSB) for the second mixer stage (LO2). I_{Bias} is the mixer tail current. The equivalent input noise resistance due to the active current source and the load resistance can be referred to the input as

$$R_{eqLOAD} \approx \frac{R_L^2}{A_v^2} \left(\frac{1}{R_L} + \frac{I_{Bias}/2}{(V_{gs} - V_t)_{Load}} \right) \cdot 2 \quad (11)$$

where A_v is the voltage conversion gain given by (8). R_L is the load resistance from either the triode devices M_9 and M_{10} or the p^+ diffusion resistor in the second mixer stage, while $(V_{gs} - V_t)_{Load}$ is the $(V_{gs} - V_t)$ of M_{11} and M_{12} in Fig. 11. The noise analysis from the switches is considerably more complicated and can be analyzed using the approach given in [38].

Equations (7)–(11) reveal the classic tradeoff between gain, noise, and distortion. Essentially, a higher $(V_{gs} - V_t)$ for the input devices improves the distortion performance while

degrading the gain and ultimately the noise performance. It becomes apparent from (7) that the voltage gain, and ultimately the noise performance of the mixer, are influenced by the ratio of $(V_{gs} - V_t)_{sw}$ to the amplitude of the local oscillator. From (11), a tradeoff is seen between the noise contribution from devices M_{11} and M_{12} and the mixer output swing.

For the DECT implementation, it was desired to have a voltage conversion gain of 10 dB through the entire image-rejection mixer. From the system noise budget, the mixers were to contribute less than a third of the total receiver equivalent output noise.

The device aspect ratios for all components are given in Figs. 11 and 12 while Table II summarizes the bias conditions for the mixers. It was found that the predicted conversion gain and distortion given by (7) and (9) agreed quite well with both simulation and measured results for the individual mixers and the entire image-rejection configuration. However, the measured noise performance was significantly more than predicted. The difference is believed to be related to the inadequate device noise model. A $\gamma = \frac{2}{3}$ was assumed for the thermal noise calculations, which may not have been accurate. In addition, the unity conversion gain limitation of the first mixer stage results in a significant noise penalty.

To minimize the mismatch between the different mixer and LO signal paths, exceptional care was taken during layout. Common centroid techniques were used throughout the image-rejection mixer. The quadrature local oscillator signals used by the mixer were generated using a polyphase filter described by [24].

D. Baseband Filters and ADC

Similar to a direct conversion receiver, the wide-band IF front-end downconverts all channels to baseband before any filtering is performed. The primary objective of the baseband filter section is to remove all of the alternate channel energy while adjusting the amplitude of the desired signal which results in a reduced dynamic range requirement for the ADC. The baseband filter and ADC utilized by this receiver have been previously described [39]–[42]. A description of the baseband filter and ADC as they relate to the DECT receiver will now be outlined. A block diagram of the baseband section is given in Fig. 13.

E. Sallen and Key Anti-Alias Filter

Before the signal is sampled by the switched-capacitor filter, an anti-alias filter must be used. The objective is to filter any energy that could potentially alias into the band of the desired signal as a result of sampling. This is of particular concern in highly integrated receivers where it is possible to have a

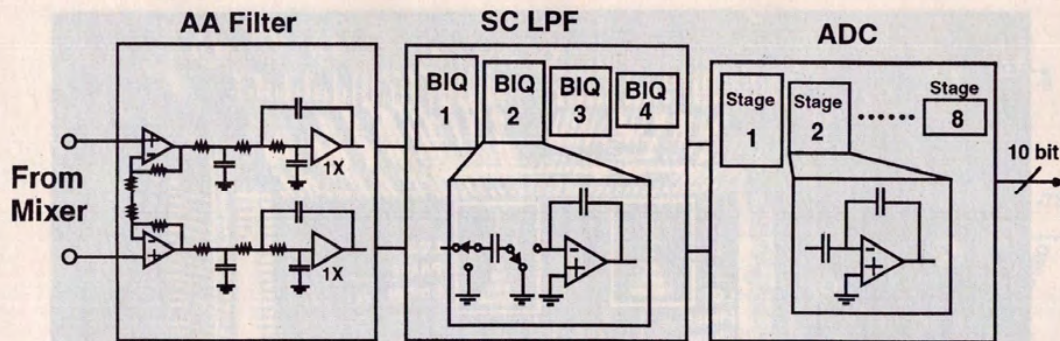


Fig. 13. Baseband filters and ADC.

TABLE III
COMPARISON BETWEEN CAPACITIVELY SCALED
AND NONSCALED BASEBAND SECTIONS

	AA Filter	SC Filter	ADC
Total C	200pF	60pF/24pF	11pF/4pF
Power	10mW	35mW/14m	20mW/12mW

weak desired signal in the presence of large adjacent channel interferers which see little if any attenuation before the anti-aliasing filter. For the DECT receiver, a sampling frequency of 31.1 MS/s was selected for the switched-capacitor sampled data circuits which follow the Sallen and Key filter. The 3-dB bandwidth of the desired signal is 700 kHz. Therefore, the blocking requirements at 30.4 MHz (31.1–700 kHz) define the required anti-alias filtering at this frequency. For DECT, a -80 -dBm desired carrier must be received with an adequate CNR in the presence of a blocker potentially -23 dBm 30.4 MHz away from the carrier. Thus, on the order of 70 dB of attenuation is required by a combination of the RF front-end filter and the anti-alias filter before sampling may occur at baseband.

Anti-alias filtering for the baseband sampled-data filters is performed by a series of cascaded poles. The output impedance of the IF-to-baseband mixers is in parallel with a 28-pF capacitance to form the first pole (see Fig. 12). A noninverting amplifier is then used with resistive feedback to create a $2\times$ gain stage which reduces the noise contribution from the subsequent filter blocks. A second pole is then introduced at the output of the $2\times$ gain stage. This is then followed by a second-order Sallen and Key filter. The 3-dB frequency of the composite continuous time filter is 1.5 MHz, which provides more than 70 dB of rejection 30.4 MHz away from the carrier. Additional attenuation in this band will also be provided by the RF front-end filter. P^+ diffusion resistors were used with poly-poly capacitors to create the filter poles. The filter was designed to have an adequate frequency response for DECT performance over all process corners.

F. Switched-Capacitor Channel-Select Filter

After the anti-alias filter, the signal is sampled and put through an eighth-order switched-capacitor filter, which

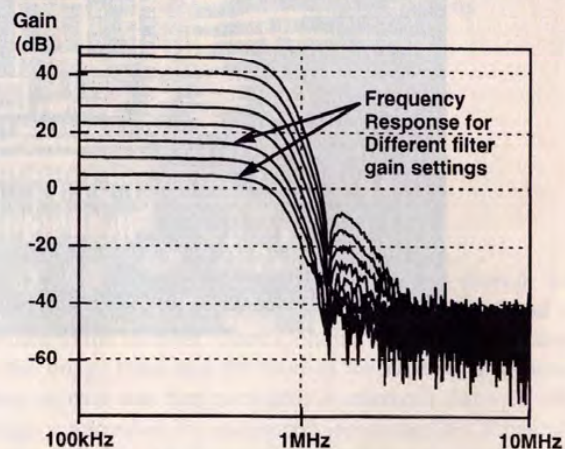
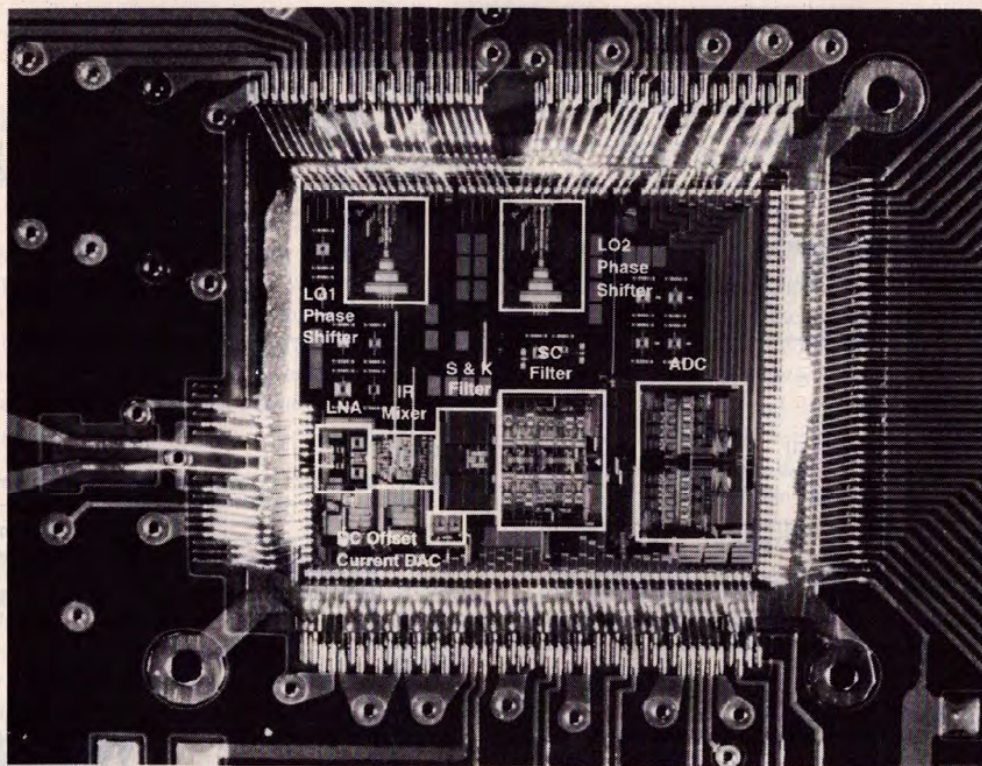


Fig. 14. Measured filter response, stand-alone baseband filters.

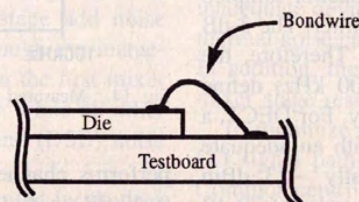
performs channel filtering and provides variable gain from 0–42 dB in 6-dB increments. The switched-capacitor filter has an equiripple frequency response. After filtering and gain control, the dynamic range requirements of the ADC are now reduced to 10 b.

The switched-capacitor filter is comprised of four biquad stages. The first three biquad stages perform channel filtering, while the last stage equalizes the phase response of the desired signal for a constant group delay to compensate for delay added by the Sallen and Key and switched-capacitor filters. In the first few switched-capacitor stages, the desired signal's amplitude may be relatively small, however, as the signal passes down the filter, gain is provided and the noise floor (predominantly from kT/C) can rise for a constant carrier-to-noise ratio. Therefore, capacitor scaling techniques were employed to optimize the overall filter configuration for the lowest power consumption. A comparison of total capacitance used by the filters and ADC is given in Table III. It was estimated that by scaling the capacitance, a reduction of 40% in the switched-capacitor filter's power consumption may be obtained. This technique is further described in [39].

A stand-alone filter section which included both the Sallen and Key and switched-capacitor filters was fabricated as a separate die on the same reticle as the receiver prototype. Fig. 14 shows the measured frequency response for all the baseband gain filter settings on the stand-alone chip.



(a)



(b)

Fig. 15. Chip-on-board (COB) assembly. (a) Chip assembled with the board. (b) Sideview of a single bondwire.

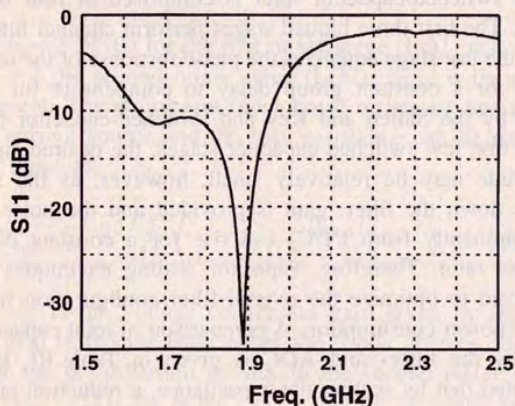


Fig. 16. Measured S11 at the receiver input.

G. Analog-to-Digital Conversion

After filtering, the signal then passes through a 10-b, 10 MS/s pipelined ADC. Similar to the switched-capacitor

filter stages, the sampling and feedback capacitors utilized by the ADC were scaled to minimize the overall power consumption. This work has been previously described in [40]–[42].

V. RECEIVER TEST RESULTS

The prototype receiver was assembled with the testboard using a chip-on-board packaging technology. Fig. 15 shows that the backside of the die is glued directly to a gold-plated landing zone found on the testboard which provides an excellent ground plane to the chip substrate. The bondwires run from the chip pads to landing zones found directly on the testboard. This is done to reduce the effects of parasitic lead inductance that otherwise would have been associated with a packaged part. With the testboard assembled, the S11 looking into the receiver input port was measured before testing began; this is shown in Fig. 16.

To test the receiver's immunity to strong adjacent channel signals, a modified version of the two-tone test was used. First, a single tone was applied to the receiver input such that

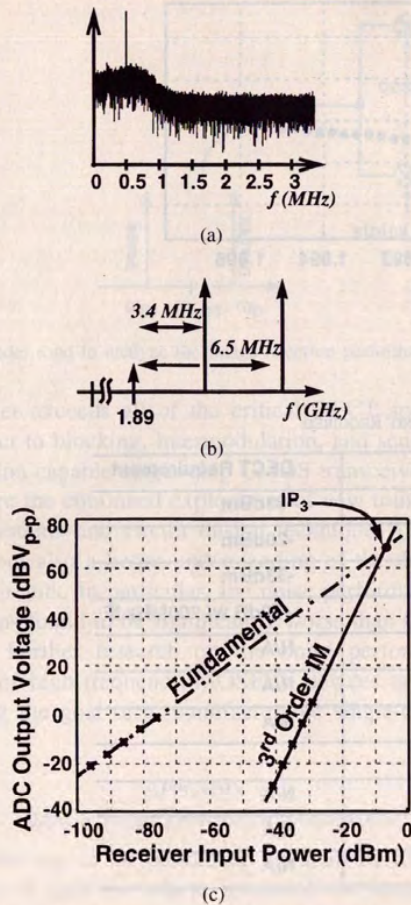


Fig. 17. Two-tone third-order intermodulation test. (a) FFT of the receiver output with a single tone input. (b) Tones applied two and four DECT channels away from the carrier. (c) Third-order IM plot showing intercept point.

when it was frequency translated to baseband, it fell within the bandwidth of the channel filter, as shown in Fig. 17(a). The power of the input signal was then varied and the linear response of the receiver was obtained. Then as outlined in the DECT specification [25], two tones were applied to the receiver two and four DECT channels away from the carrier such that when downconverted to baseband, their third-order intermodulation product fell within the pass-band of the baseband filters. The magnitude of the two input tones was varied and a third-order intermodulation intercept point of -7 dBm referred to the input of the LNA was extrapolated from Fig. 17(c).

To test the receiver's blocking performance, a -73 dBm desired signal was applied to the input in accordance with the test conditions outlined in the DECT standard. Simultaneously, a blocker was applied in the adjacent DECT channel and increased in magnitude until the CNR at the output of the receiver dropped to 10.3 dB [43], [44]. The test was repeated with a blocker in each of the DECT channels. Fig. 18 shows the magnitude of the measured blockers which resulted in a 10.3 dB CNR of the desired carrier. The shaded area in Fig. 18 represents the blocking requirements of DECT which are well below that measured on the prototype device.

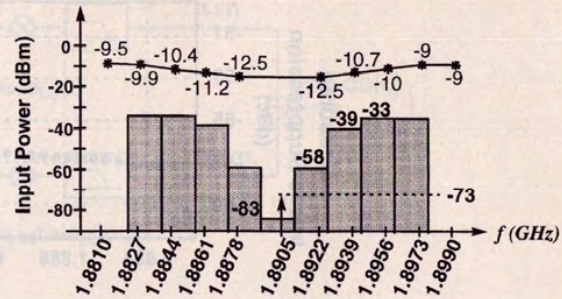


Fig. 18. Blocking performance of the DECT receiver.

TABLE IV
BREAKDOWN OF THE RECEIVER COMPONENTS
CONTRIBUTING TO IMAGE REJECTION

Balun	2dB
LNA	8dB
IR Mixer	45dB
Total IR	55dB

To test the receiver's immunity to signals present within the image-band, a series of tones in the DECT band were applied to the receiver. Corresponding tones were then applied in the image band and the ratio of the receiver's response to these signals was then recorded. A relatively flat -55 dBc of image suppression was measured across the DECT band. This is shown in Fig. 19. It should be noted that the phase between the quadrature local oscillators was tuned to give maximum image suppression. However, no tuning was provided to adjust the gain between the signal paths. A breakdown of the receiver components which contribute to image rejection is shown in Table IV. The RF filter which was not a part of the test set-up can easily provide an additional 30 dB of image attenuation. Therefore, this receiver under a tuned condition could attain 85 dB of image rejection, which is well above the requirement for the DECT standard with a ~ 190 MHz intermediate frequency.

The receiver's reference sensitivity was measured at -90 dBm which corresponds to a noise figure of 14 dB. The overall receiver's power consumption is 198 mW. A breakdown of the rms noise voltage referenced to the output of the receiver can be found in Fig. 20(a), while the contribution of each block to the overall power consumption is shown in Fig. 20(b). From Fig. 20 it can be inferred that although the first mixer contributes almost 40% of the output noise power, it dissipates less than 9% of the overall receiver's power consumption.

Although the prototype meets the sensitivity requirement of DECT, it is insufficient for other standards with more aggressive noise figure requirements. From Fig. 20 it can be seen that the noise contribution of the first mixer stage could have been traded-off with the mixer power consumption to improve the noise performance of the overall receiver. In addition, as mentioned previously, the voltage conversion gain of the first mixer was limited to unity by the parasitic capacitance at the first mixer output with the constraint of

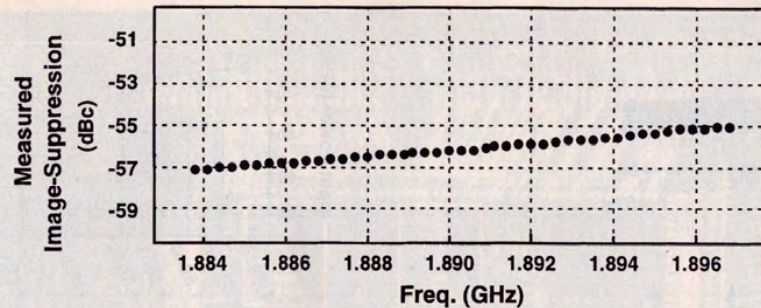


Fig. 19. Measured image suppression for the receiver.

TABLE V
RECEIVER PERFORMANCE, BOTH MEASURED AND REQUIRED

	Receiver Measurement	DECT Requirement
Sensitivity	-90dBm	-83dBm
Input IP3 (Max. gain setting)	-7dBm	-26dBm
P _{-1dB} (Min gain setting)	-24dBm	-33dBm
Receiver Image Rejection	~85dB w/ RF Filter	~70dB w/ 200MHz IF
P _{ob3dB} (Max. gain setting)	-33dBm @ 2MHz	N/A
Max. Receiver Gain	78dB	N/A
Min. Receiver Gain	26dB	N/A
Die Size	7.5mm x 6.5mm	
Active Chip Area	15mm ²	N/A
Power Supply	3.3v	N/A
Silicon Technology	0.6μm DPTM CMOS	N/A

the first mixer gain equal to one, the noise contribution from the second mixer stage becomes increasingly important. The IF bandwidth limitation problem can be more adequately addressed with an improved silicon technology with a finer feature size as is currently available with 0.35 and 0.25-μm CMOS processes. The receiver's linearity performance is set by the input stage of the first mixer. Because the input referred IP3 of the receiver was significantly above the requirement for DECT, the first mixer's linearity could have been traded-off to improve the RF mixer and receiver's noise performance.

A summary of other key receiver measurements can be found in Table V.

VI. CONCLUSION

A proposed receiver architecture, wide-band IF with double conversion, was presented in this paper. The relative merits of this system were discussed as they relate to the goal of a highly integrated receiver. The wide-band IF architecture holds promise with respect to integrating one of the more challenging components in a transceiver system, the frequency synthesizers. Moreover, the wide-band IF receiver removes the need for the discrete-component IF filter while the image-rejection mixer presented eliminates the need for the discrete-component noise filter after the LNA. In addition, the proposed architecture has features which potentially enable a single receiver to be used by multiple RF standards. A prototype

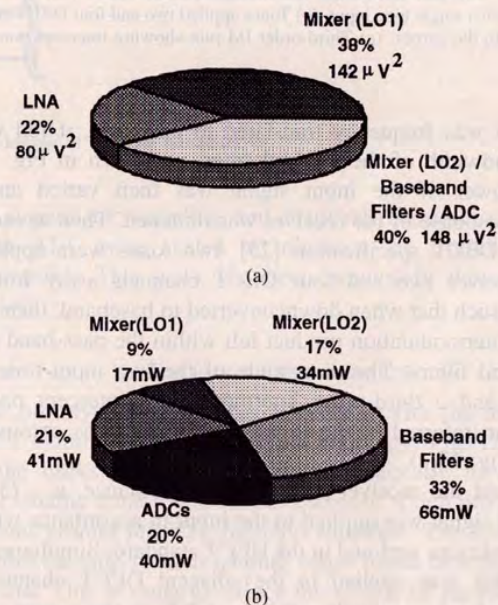


Fig. 20. (a) Breakdown of the output rms noise voltage and (b) breakdown of the receiver's power consumption.

receiver based on the wide-band IF concept was implemented in a 0.6-μm CMOS process and designed to meet the specifications of the DECT standard. Measured results indicate that

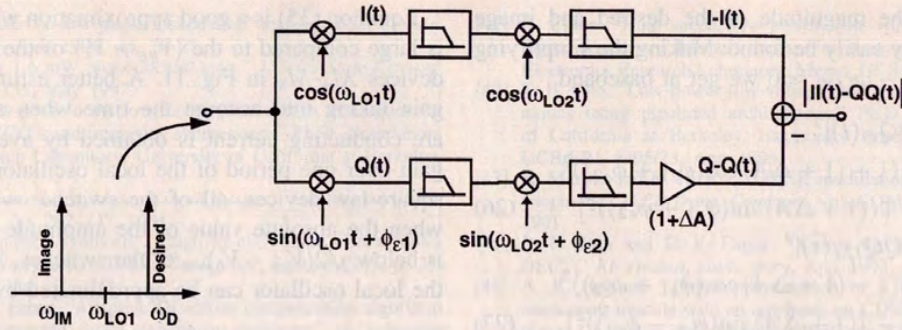


Fig. 21. Model used to analyze the image-rejection performance as a function of LO phase and gain path matching.

this receiver exceeds all of the critical DECT specifications with respect to blocking, intermodulation, and sensitivity.

Production capable single-chip CMOS transceivers will not only require the continued exploration of new transmitter and receiver systems and circuit design techniques [3], [4], [6], [8], [46], but also a better understanding of the devices used by these circuits. In particular, the noise performance of this receiver was found to be significantly worse than that initially predicted. Further research on the noise performance and modeling of high-frequency MOSFET devices is paramount to reaching the goal of a manufacturable single-chip CMOS receiver.

APPENDIX A IMAGE REJECTION WITH MISMATCH

The following is an outline of an analysis to determine the effects of gain and phase mismatch on image-rejection performance. The matching error is modeled as shown in Fig. 21. The phase mismatch between both the I and Q first and second local oscillators are defined as $\phi_{\epsilon 1}$ and $\phi_{\epsilon 2}$, respectively, which defines the deviation from ideal quadrature. For example, 91° phase difference between the I and Q LO1 would be represented by $\phi_{\epsilon 1} = 1^\circ$. ΔA represents the composite gain mismatch between two of the four image-rejection channels.

The analysis is carried out by applying an image and desired signal denoted $D(t)$ and $IM(t)$ both equally spaced in the frequency domain from the first local oscillator as shown in Fig. 21. Both the image and desired signal will be tracked as they move through the mixer to the baseband II and QQ channels where they are summed. A solution for the image-rejection ratio is found with the magnitude of the desired and image signals after summation of the II and QQ channels

$$D(t) = \cos(\omega_D t) + j \sin(\omega_D t) \quad (12)$$

$$IM(t) = \cos(\omega_{IM} t) + j \sin(\omega_{IM} t). \quad (13)$$

Assuming an idealized sinusoidal LO, the two input signals $D(t)$ and $IM(t)$ are multiplied by the I and Q local oscillators, the resulting signals at IF can be expressed as

$$I_D(t) = \frac{1}{2} [\cos((\omega_D - \omega_{LO1})t) + \cos((\omega_D + \omega_{LO1})t)] \\ + \frac{j}{2} [\sin((\omega_D + \omega_{LO1})t) + \sin((\omega_D - \omega_{LO1})t)] \quad (14)$$

$$I_{IM}(t) = \frac{1}{2} [\cos((\omega_{IM} - \omega_{LO1})t) + \cos((\omega_{IM} + \omega_{LO1})t)] \\ + \frac{j}{2} [\sin((\omega_{IM} + \omega_{LO1})t) + \sin((\omega_{IM} - \omega_{LO1})t)] \quad (15)$$

$$Q_D(t) = \frac{1}{2} [\sin((\omega_D + \omega_{LO1})t + \phi_{\epsilon 1}) \\ - \sin((\omega_D - \omega_{LO1})t - \phi_{\epsilon 1})] \\ + \frac{j}{2} [\cos((\omega_D + \omega_{LO1})t - \phi_{\epsilon 1}) \\ - \cos((\omega_D + \omega_{LO1})t + \phi_{\epsilon 1})] \quad (16)$$

$$Q_{IM}(t) = \frac{1}{2} [\sin((\omega_{IM} + \omega_{LO1})t + \phi_{\epsilon 1}) \\ - \sin((\omega_{IM} - \omega_{LO1})t - \phi_{\epsilon 1})] \\ + \frac{j}{2} [\cos((\omega_{IM} + \omega_{LO1})t - \phi_{\epsilon 1}) \\ - \cos((\omega_{IM} + \omega_{LO1})t + \phi_{\epsilon 1})]. \quad (17)$$

Assuming the upconverted terms are removed through low-pass filtering and substituting in $\omega_{IF} = \omega_D - \omega_{LO1} = \omega_{LO1} - \omega_{IM}$ results in

$$I_D(t) = \frac{1}{2} \cos(\omega_{IF} t) + \frac{j}{2} \sin(\omega_{IF} t) \quad (18)$$

$$I_{IM}(t) = \frac{1}{2} \cos(\omega_{IF} t) - \frac{j}{2} \sin(\omega_{IF} t) \quad (19)$$

$$Q_D(t) = -\frac{1}{2} \sin(\omega_{IF} t - \phi_{\epsilon 1}) + \frac{j}{2} \cos(\omega_{IF} t - \phi_{\epsilon 1}) \quad (20)$$

$$Q_{IM}(t) = \frac{1}{2} \sin(\omega_{IF} t + \phi_{\epsilon 1}) + \frac{j}{2} \cos(\omega_{IF} t + \phi_{\epsilon 1}). \quad (21)$$

Multiplying (18)–(21) by the second set of quadrature LO's and again removing the upconverted terms, the following expression may be obtained for image and desired signal present in the II and QQ baseband channels:

$$II_D(t) = \frac{1}{4} [\cos((\omega_{IF} - \omega_{LO2})t) + j \sin((\omega_{IF} - \omega_{LO2})t)] \quad (22)$$

$$II_{IM}(t) = \frac{1}{4} [\cos((\omega_{IF} - \omega_{LO2})t) - j \sin((\omega_{IF} - \omega_{LO2})t)] \quad (23)$$

$$QQ_D(t) = \frac{1}{4} (1 + \Delta A) [-\cos((\omega_{IF} - \omega_{LO2})t - (\phi_{\epsilon 1} + \phi_{\epsilon 2})) \\ - j \sin((\omega_{IF} - \omega_{LO2})t - (\phi_{\epsilon 1} + \phi_{\epsilon 2}))] \quad (24)$$

$$QQ_{IM}(t) = \frac{1}{4} (1 + \Delta A) [\cos((\omega_{IF} - \omega_{LO2})t + (\phi_{\epsilon 1} + \phi_{\epsilon 2})) \\ - j \sin((\omega_{IF} - \omega_{LO2})t + (\phi_{\epsilon 1} - \phi_{\epsilon 2}))]. \quad (25)$$

From (22)–(25) the magnitude of the desired and image baseband signals may easily be found. Making the simplifying assumption that $\omega_{IF} - \omega_{LO2} \approx 0$ we get at baseband

$$|II_D(t) - QQ_D(t)|^2 = \frac{1}{16} [(1 + (1 + \Delta A) \cos(\phi_{\varepsilon 1} + \phi_{\varepsilon 2}))^2 + ((1 + \Delta A) \sin(\phi_{\varepsilon 1} + \phi_{\varepsilon 2}))^2] \quad (26)$$

$$|II_{IM}(t) - QQ_{IM}(t)|^2 = \frac{1}{16} [(1 - (1 + \Delta A) \cos(\phi_{\varepsilon 1} + \phi_{\varepsilon 2}))^2 + ((1 + \Delta A) \sin(\phi_{\varepsilon 1} - \phi_{\varepsilon 2}))^2]. \quad (27)$$

By taking the ratio (26) and (27), the image-rejection ratio in (dB) is given by

$$IRR(\text{dB}) = 10 \cdot \log \left[\frac{1 + (1 + \Delta A)^2 + 2(1 + \Delta A) \cos(\phi_{\varepsilon 1} + \phi_{\varepsilon 2})}{1 + (1 + \Delta A)^2 - 2(1 + \Delta A) \cos(\phi_{\varepsilon 1} - \phi_{\varepsilon 2})} \right]. \quad (28)$$

Equation (28) is identical to the result given in [20] and [45] for more conventional image-rejection mixer configurations.

APPENDIX B

MIXER VOLTAGE CONVERSION GAIN

First take the idealized model where the desired signal is represented as a cosine, $V_{rf}(t)$, multiplied by an ideal squarewave local oscillator, $V_{LO}(t)$, which is represented with height ± 1

$$V_{rf}(t) = g_m R_L V_{rf} \cos(\omega_{rf} t) \quad (29)$$

$$V_{LO}(t) = \left(\frac{4}{\pi} \right) \sum_{k=1}^{\infty} \left[\frac{\sin(k\pi/2)}{k} \cdot \cos(k\omega_{LO} t) \right]. \quad (30)$$

In this model, take (29) and multiply by (30). This gives

$$V_o(t) = V_{rf}(t) \cdot V_{LO}(t) \quad (31)$$

$$V_o(t) = g_m R_L \left(\frac{4}{\pi} \right) [\cos(\omega_{LO} t) - \cos(3\omega_{LO} t) \cdots] \cdot V_{rf} \cos(\omega_{rf} t). \quad (32)$$

Ignoring the harmonics of the LO and multiplying the fundamental by the RF sinewave results in

$$V_o(t) = g_m \cdot R_L \left(\frac{4}{\pi} \right) \left(\frac{1}{2} \cos((\omega_{rf} - \omega_{LO})t) + \frac{1}{2} \cos((\omega_{rf} + \omega_{LO})t) \right). \quad (33)$$

Eliminating the upconverted term, the resulting desired signal at the mixer output is then

$$V_o(t) \approx g_m R_L \left(\frac{2}{\pi} \right) \cos((\omega_{rf} - \omega_{LO})t). \quad (34)$$

Therefore, assuming a perfect squarewave LO, the voltage conversion gain through the mixer is given by the well-known expression [47], [38], [5]

$$A_v = g_m R_L \left(\frac{2}{\pi} \right). \quad (35)$$

Equation (35) is a good approximation when the LO voltage is large compared to the $(V_{gs} - V_t)$ of the switching devices, devices M_4 – M_8 in Fig. 11. A better estimate of the voltage gain taking into account the time when all of the switches are conducting current is obtained by averaging the voltage gain over one period of the local oscillator. Again, assuming square-law devices, all of the switches will conduct current when the absolute value of the amplitude of the LO voltage is below $\sqrt{2}(V_{gs} - V_t)_{sw}$ of the switches. Assuming now that the local oscillator can be approximated by a sinewave as

$$V_{LO}(t) = V_{LO} \sin(\omega_{LO} t). \quad (36)$$

Defining the time that the switches move from the balanced state (all switches conducting), denoted t_{BAL} , to the unbalanced state (only two of the four devices are conducting) may be determined by the following relationship:

$$V_{LO}(t) = \sqrt{2}(V_{gs} - V_t)_{sw} = V_{LO} \sin(\omega_{LO} t_{BAL}). \quad (37)$$

Assuming $\sin(x) \approx x$ for small x , this gives

$$t_{BAL} = \frac{\sqrt{2}(V_{gs} - V_t)_{sw}}{V_{LO} \omega_{LO}}. \quad (38)$$

The gain is then averaged over one period of the LO assuming that the instantaneous gain increases linearly from zero conversion gain to the gain given (35) at time t_{BAL} . Averaging over one period of the LO results in

$$A_v \approx g_m R_L \left(\frac{2}{\pi} \right) \left(1 - \frac{\sqrt{2}(V_{gs} - V_t)_{sw}}{\pi V_{LO}} \right). \quad (39)$$

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